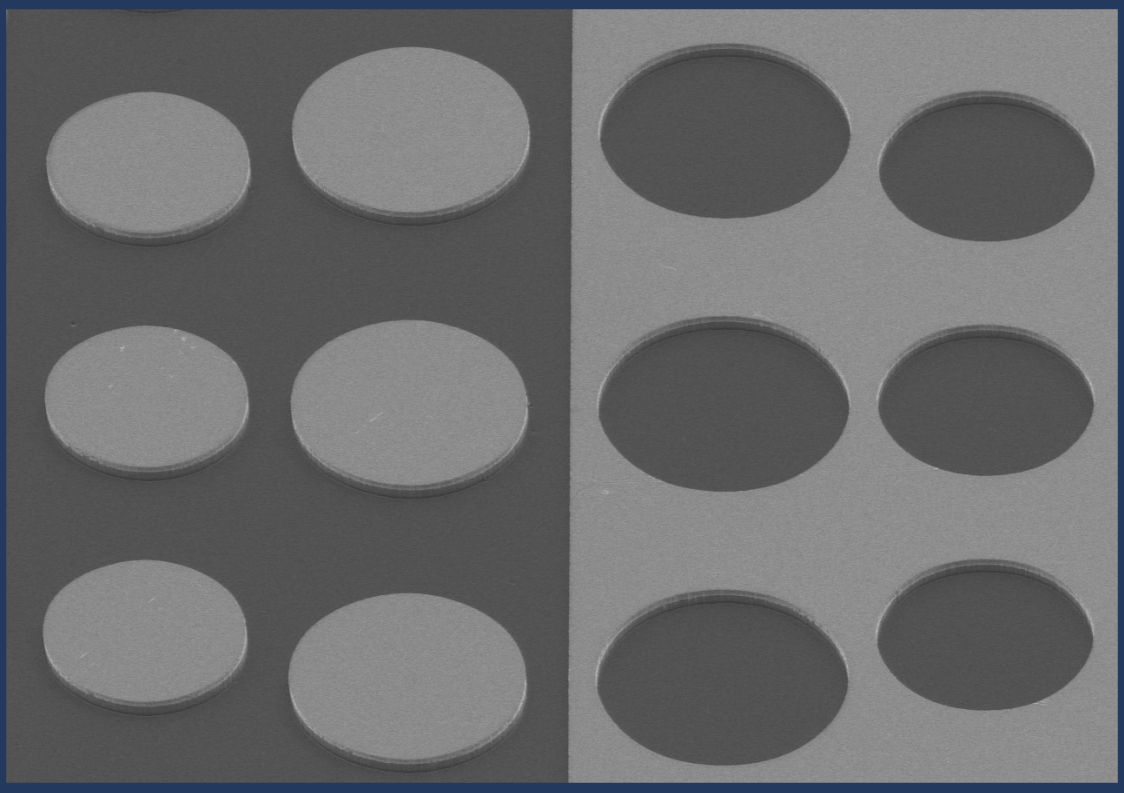
Inductively coupled plasma reactive ion etching of high aspect ratio structures on 4H-SiC for MEMS applications

Zhenhua Zhang



TU Delft

Inductively coupled plasma reactive ion etching of high aspect ratio structures on 4H-SiC for MEMS applications

Master of Science Thesis

by

Zhenhua Zhang

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Abstract

As silicon carbide(SiC) gets more and more attention from the semiconductor industry due to its robust mechanical and chemical properties, reliable and standardized processing technologies such as reactive ion etching(RIE) for SiC are in great demand. This is because of the difficulty and challenge of fabricating micro devices on the SiC substrate. Although the high hardness and chemical inertness make SiC a good candidate for applications such as sensors in harsh environments, they also impede the development of SiC-based devices when considering processing.

This thesis aims to develop a standardized inductively coupled plasma(ICP) reactive ion etching(RIE) process for 4H-SiC substrate etching. The developed process is expected to be applied in the fabrication of micro-electro-mechanical systems(MEMS). The specifications are a high etch rate, micro-masking-free surface, and high selectivity. First, a literature review was conducted to comprehensively study the characteristics of the SiC material and the mechanisms of the ICP RIE process. Second, a baseline recipe was developed guided by the theory studied in the literature works. Third, initial tests were conducted, and the preliminary optimizations with a focus on etch rate and micro masking suppression were performed. Fourth, the design of experiments(DOE) based on the preliminarily optimized recipe was conducted to study the effect of process parameters on etch rate, etch profile, and selectivity. Last, the optimized recipes with a focus on etch rate, etch profile, and selectivity were summed and listed. The achieved maximum etch rate was 1.26 μm/min. The maximum selectivity of the hard mask material to SiC was 153 when the nickel hard mask was used. A micro-masking-free surface of SiC was achieved.

Keywords: Inductively coupled plasma reactive ion etching, 4H-SiC, Design of Experiments

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Contents

Nomenclature

List of Abbreviations

Cr Chromium

Cu Copper

DOE Design of Experiments

FET Field effect transistor

ICP Inductively coupled plasma

MEMS Micro-electro-mechanical systems

Ni Nickel

PECVD Plasma enhanced chemical vapour deposition

PVD Physical vapor deposition

RIE Reactive ion etching

SEM Scanning electron microscope

SiC Silicon carbide

TEC Thermal expansion coefficient

TSiCV Through Silicon Carbide vias

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1 Introduction

SiC is one of the wide-bandgap semiconductor materials that has been getting more and more attention from the modern semiconductor industry[1]. It has unique chemical and physical properties compared to traditional semiconductor materials such as silicon. As a compound material, strong chemical bonds between silicon and carbon atoms mean it has high hardness and chemical inertness properties. Thus, it is very suitable for Micro-Electro-Mechanical Systems(MEMS) applications like sensors in harsh environments. Y. Jiang et al.[2] proposed a fiber-optic pressure sensor, making good use of the stable mechanical and electrical properties at elevated temperatures. It was reported by M. Andersson et al. that SiC can be used to make field effect transistors(FET), indicating its potential in other applications[3]. Besides, Fig. 1.1 and Table 1.1 show that SiC has high thermal conductivity and breakdown voltage, making it a good candidate for high temperature and high power applications[4]. It has also been found that there are multiple polymorphs of SiC in which the crystal structures vary based on different stacking sequences. Ramsdell[5] developed a naming method for various SiC crystal structures in 1947, which is still the method applied for naming new forms of SiC at present. 4H-SiC, named using this method, has been popular among others such as 3C-SiC and 6H-SiC for many semiconductor device applications because it has superior properties not only high electron mobilities and high breakdown electric field owing to its widest bandgap but also the availability of 4H-SiC wafers of larger diameters and better qualities[6].

However, the high hardness and chemical inertness properties of SiC turn into disadvantages and challenges in the development of processing technology. Etching technologies for SiC are still developing in industries and academia, exploring the possibilities of growing fast, accurate, defect-free, standardized solutions. Up to the present, many efforts have been put into the process technology for SiC, such as the wet etching[7], femtosecond laser drilling [8] [9]and electrochemical etching[10] technics for SiC substrate material removal.

1.1. Introduction to SiC etching technology

This section will briefly introduce available technologies for SiC processing in terms of etching.

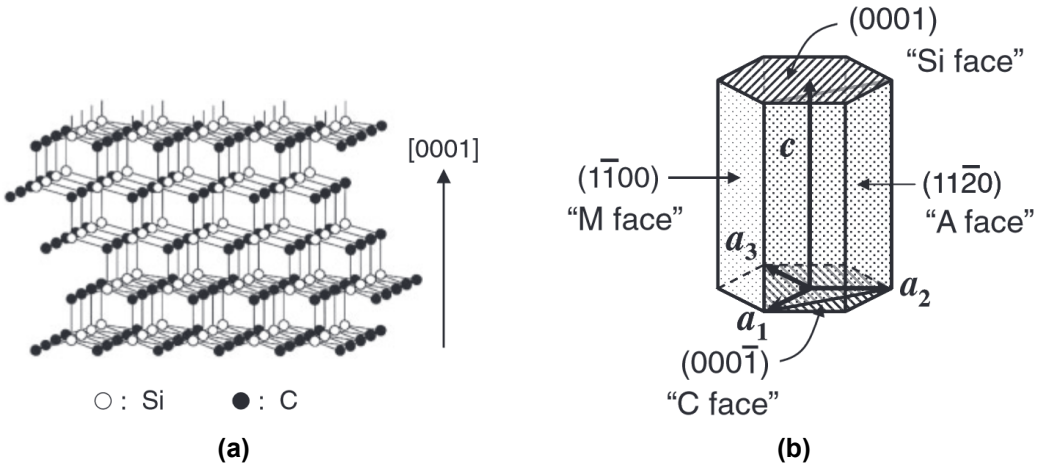


Figure 1.1: (a)Schematic crystal structure of 4H-SiC.(b)Hexagonal cell of SiC.[4]

Table 1.1: Physical properties of SiC (4H-SiC) and Si at room temperature. Adapted from [4]

	SiC	Si
Bandgap(eV)	3.26	1.12
Breakdown electric field for material with a doping density of $10^6\ cm^{-3}$ (MV/cm)		
E_B parallel to c-axis	2.8	0.3
E_B perpendicular to c-axis	2.2	0.3
Thermal conductivity (W $cm^{-1}\ K^{-1}$)	3.3-4.9	1.3-1.5

1.1.1. Wet etch

It was reported that in aqueous solutions, monocrystalline SiC such as 4H-SiC is stable because of its chemical inertness[7]. Efforts were made to explore the possibilities for SiC wet etching, but the results were not satisfying. For example, an alkaline solution of $K_3Fe(CN)_6$ at the temperature of more than 100 °C can only etch the silicon face of monocrystalline SiC while the carbon face was not attacked. Though phosphoric acid at 215 °C can etch SiC, the formation of Silicon dioxide on the surface prevented the further etching on the substrate[7]. Pearton's team[11] presented a summary of molten salt solutions used for the etching of SiC with different crystal structures, which is shown in Table 1.2. All the etching processes based on these etchants must be performed at high temperatures ranging from 180 °C to 900 °C. Such high temperatures and the corrosive characteristic prevent further applications in patterned substrate etching because few hard mask materials could survive in these solutions.

The isotropic etching characteristic is another factor that limits the use of wet etching methods for high aspect ratio structure fabrications on SiC substrate. Undercutting severely undermines the geometry control of many MEMS fab-

rication processes, where selective removal of substrate material is critical to implementing precise 3D structures. Though many efforts have been put into the wet etching methods for SiC etching, they are still faced with significant challenges and limitations.

Table 1.2: Molten salt etchants for SiC. Adapted from [11]

Solution	Material	Temperature
NaF/K_2CO_3	SiC(0001)	650°C
H_3PO_4	a-SiC(H)	180°C
NaOH	SiC(111)	900°C
Na_2O_2	SiC(0001)	>400°C
$NaOH/Na_2O_2$	SiC(0001)	700°C
$Borax/Na_2CO_3$	epi-SiC	855°C
NaOH/KOH	bulk 6H	480°C
$Na_2O_2/NaNO_2$	bulk 6H	>400°C
KOH/KNO_3	bulk 6H	350°C

1.1.2. Reactive Ion etching

Dry etching methods, also known as plasma etching methods, have been getting more and more attention for monocrystalline SiC substrate etching. However, due to the strong chemical bond between the silicon atom and the carbon atom, general isotropic plasma etching can hardly remove the substrate material because the ions cannot react with the substrate when chemical bonds are not broken. Besides, general isotropic plasma etching has the same issue as wet etching. The geometry control is a great challenge for small structure fabrications, which is very common in the MEMS devices process.

Reactive Ion etching(RIE), in which RF bias power is applied to generate an electrical field perpendicular to the substrate surface, enables anisotropic etching of SiC substrate. This makes it suitable for pattern transferring of microscopic features. The mechanism of RIE is shown in Fig. 1.2. The steps of the process include:

1) Etching gases are ionized into reactive species by the RF power source;

2) The charged reactive species are directed to the substrate surface by the vertical electrical field, which is generated by the same RF power source;

3) The physical bombardment of the plasma breaks the chemical bonds between silicon atoms and carbon atoms from the substrate surface, followed by the reaction between the substrate atoms and the reactive species;

4) The volatile reaction products desorb from the surface and are carried away from the etching chamber.

RIE for SiC is done by using the attributes from both physical and chemical mechanisms. The plasma bombardment provides significant kinetic energy

to initiate the etching, and then the reactive species can react with the atoms breaking free from the substrate surface. This method not only suppresses the undercutting effects but also increases the etch rate compared to isotropic plasma etching and pure physical etching.

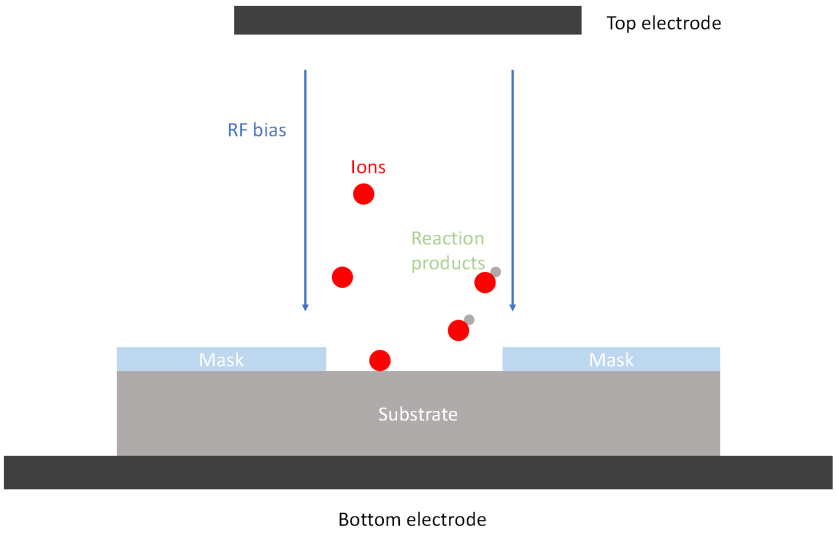


Figure 1.2: Illustration of RIE process mechanism

1.1.3. Inductively coupled plasma reactive ion etching

Inductively coupled plasma reactive ion etching(ICP RIE) is the more advanced plasma etching method, which is more suitable for deep and high aspect ratio etching. The difference between ICP RIE and RIE is that another RF source power is needed for ICP RIE, while the RIE process only needs one RF source power.

As indicated in Fig. 1.3, besides the RF source power applied to the substrate for biasing, another power source performs as ICP source power to generate plasmas of large density in the ICP chamber. The plasmas will be directed to the target surface by the substrate bias power, bombarding the sample surface and breaking chemical bonds between silicon and carbon atoms. These 'free' atoms will then react with ions from the etching gases.

The most prominent advantage of ICP RIE compared to RIE is that the extra RF source power helps generate high-density plasmas. This provides more ions to bombard and react with the substrate surface, providing possibilities for conquering the challenges of developing high etch rate plasma etching recipes for SiC processing.

1.2. Motivation and objectives

Though SiC has a promising future in MEMS applications, challenges of SiC processing stand in the way of exploiting the potential of this material. Dedicated

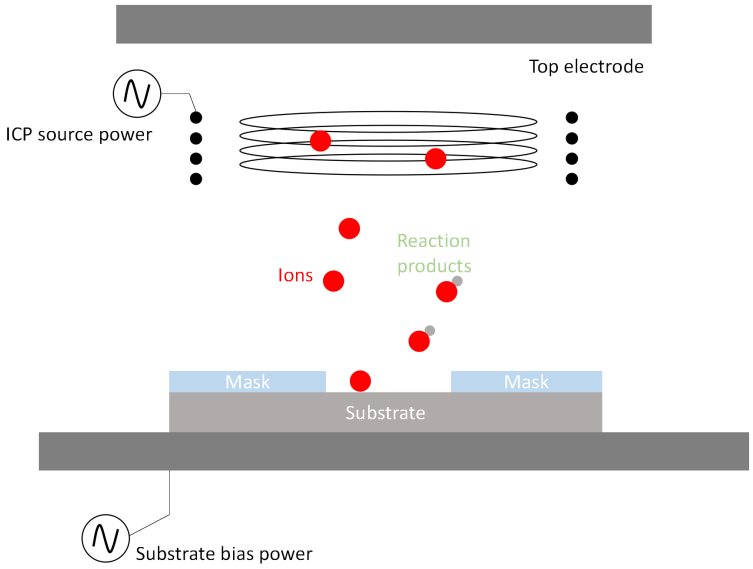


Figure 1.3: Illustration of ICP RIE process mechanism

plasma etching technology is in wide demand for MEMS devices fabricated on SiC substrate. However, no mature and commercialized SiC RIE processes are available.

In recent years, a lot of research has focused on developing the plasma etching process for SiC[12–19]. The main challenges of SiC plasma etching process development are etching morphology control and etch rate improvement. For example, J.H.Choi et al.[12] reported nanopillars formation on the etched 4H-SiC surface, the density of which varies with hard mask materials used for patterning. The nanopillars, also known as micro maskings, were formed with much lower density when copper(Cu) and nickel(Ni) were used as hard mask material. In contrast, the density of micro maskings reached the maximum value when aluminum(Al) was used for the metal hard mask layer. This happens because Al is easily sputtered by ion bombardment, which creates more Al particles. As a result, these particles have a higher chance of settling back onto the SiC surface, causing a micro-masking effect. The surface will become rough, filled with grass-like structures.

However, Osipov's team[17] and Ozgur's team[14] have reported a significant micro masking effect even when using nickel(Ni) and copper(Cu) as hard mask materials applying different experiment settings. It seems that the cause of the micro-masking effect is quite complex, involving multiple principles that could play a role in etching morphology control. There is still uncharted territory to be explored to uncover the secret of the micro-making effect.

Besides, etch rate improvement is another task for a high-efficiency SiC plasma etching process. The high energy bonds between silicon and carbon atoms in the SiC structures impede the initialization of plasma etching. So, it is intuitive that applying high bias power to the plasma will grant them more kinetic

energy to enhance the ion bombardment on the SiC surface, breaking the bonds so that the etching gas can react with these ”free” atoms. Nevertheless, the stronger the ion bombardment, the harder the mask layer is sputtered, generating more metal particles, which will cause more micro-masking effects when redeposited on the SiC surface where plasma etching is proceeding. It is evident that trade-offs must be made with parameter settings to achieve a balance between morphology control of the etched surface and optimal etch rate.

The primary motivation of this thesis is to explore the possibilities of developing a standardized inductively coupled plasma(ICP) deep reactive ion etching(DRIE) process on a 4H-SiC surface for MEMS device fabrications. This ICP DRIE process can provide a stable and reproducible solution for MEMS devices made of SiC materials, such as SiC pressure sensors. The process can also realize interconnect structures on SiC, such as Through-SiC-Vias(TSiCV), critical in SiC device packaging technology. This means the ICP RIE process could also be implemented for deep 3D structures etching into the SiC substrate, in which high selectivity specification should be achieved.

The thesis aims to develop and optimize an inductively coupled plasma(ICP) reactive ion etching(RIE) process on a 4H-SiC substrate. The objectives can be defined as follows:

1) Performing a comprehensive study on the properties of SiC materials and the mechanisms for SiC etching.

2) Investigate and assess the parameters’ possible effect on the SiC surface’s etching result.

3) Develop a baseline etching process for SiC etching based on the evaluations from step 2.

4) Perform the baseline process on 4H-SiC samples collect data, and characterize the etching profile. Optimize process settings and repeat experiments.

5) Sum and list the finalized process focusing on different specification optimizations.

1.3. Outline

The thesis aims to develop and optimize the ICP RIE process on 4H-SiC for MEMS applications. The content is divided into five parts, defined as follows:

Chapter 1 has provided background information on fabrication technologies for SiC substrates and sets forth the importance and challenges of developing a standardized plasma etching process for SiC substrates.

Chapter 2 will introduce the principles of inductively coupled plasma(ICP) reactive ion etching(RIE). The mechanism of the effect of parameters on the etch rate and etch profile will be explained.

Chapter 3 will present a solution for the design of experiments(DOE) on ICP DRIE process development. The implementation of the hard mask deposition, process parameters changing, initial test results of the baseline process, the effect of carrier wafer material on the etching results, and the characterization and analysis protocol applied to determine etch rate, etch profile, and selectivity in Chapter 4 will be introduced and explained.

Chapter 4 will illustrate the results of the design of experiments(DOE). A comprehensive study will be performed on how parameters such as ICP source power, bias power, pressure, substrate temperature, and carrier wafer materials affect the etch rate, etch profile, and selectivity. Tests using non-metal hard mask materials will be performed to explore the possibilities of implementing a ”clean” ICP RIE, which could be integrated with other processes, such as the CMOS process on SiC substrates.

Finally, Chapter 5 will summarize the results, draw a conclusion, and assess the possible future work.

2

Principles of ICP DRIE for SiC

This chapter will introduce the fundamental theories and principles of inductively coupled plasma(ICP) reactive ion etching(RIE) for SiC substrates. Firstly, a comparative study between the ICP RIE method and other etching methods for SiC substrates will be performed based on literature reviews to explain the superiority of the ICP RIE method for SiC substrates etching. The etch gases and substrate atoms' chemical reaction mechanism will be introduced. The role of process parameters in the etch rate and morphology control will be illustrated.

2.1. ICP DRIE for SiC

Initially, researchers did not turn to ICP RIE for better solutions for SiC etching. As mentioned in Chapter 1, efforts have been put into wet etching. Besides, innovative methods for SiC etching, such as femtosecond laser drilling[8, 9], and electrochemical etching[10], and electrolytic plasma hybrid etching method[20, 21] have been reported. These methods provide exciting views of exploring 4H-SiC substrates, but the limitations are inevitable. For example, C. Wu et al.[8] presented a 4H-Sic substrate etching method using a femtosecond laser, followed by ICP etching to smoothen the surface. This method combines the efficiency of femtosecond laser drilling and the good etching surface quality characteristic of ICP etching. Though this is an exciting way of realizing a 4H-SiC substrate etching method with a high etch rate and reasonable surface quality control, the results were limited to structures of large openings, which is 800 μm. S. Zhang's team[20][21] presented an innovative method for 4H-SiC substrate etching, applying plasma-enhanced electrochemical etching using NaOH electrolyte to remove the substrate material. They managed to drill a 148 μm deep hole with 312 μm opening and achieved good surface quality. However, this is a non-standardized process in the industry, which is being optimized with dedicated experiment settings.

Plasma etching, including reactive ion etching(RIE) and inductively coupled plasma(ICP) reactive ion etching(RIE), has been getting more and more attention for better etching results with lower costs than wet etching and laser drilling. Deep reactive ion etching(DRIE) has been widely used for vias fabrication on silicon substrate. Take the Bosch process as an example, Fig. 2.1 illustrated the mechanism of the Bosch process using SF_6 and C_4F_8 as etch gas and passivation

gas, respectively. Since plasma generated from SF_6 not only etch vertically but also laterally, a passivation cycle is needed after each etching cycle to prevent the side wall from being further consumed by the etching gas.

However, this is not true for 4H-SiC. The etching will not take place if there is no ion bombardment to initiate it. This is good when considering side wall protection because no passivation is needed to stop the non-existent lateral etching, as indicated inFig. 2.2 from one of the 4H-SiC plasma etching research[13]. Still, this observation shows that more stringent conditions must be met to make the etching happen on a 4H-SiC substrate and achieve a comparable etch rate to the silicon substrate. So, the effectiveness of general reactive ion etching(RIE) is limited on the 4H-SiC substrate.

The good news is that inductively coupled plasma(ICP) reactive ion etching(RIE) can increase the etch rate of 4H-SiC plasma etching significantly. As illustrated in Fig. 1.3, an extra RF power source is the key to generating high-density plasma to increase the etch rate, which is crucial to 4H-SiC etching. Since there is an independent RF power source to generate high-density plasma, the substrate RF power source can be more fully applied to enhance ion bombardment on the substrate. The increased plasma density and ion bombardment help increase the etch rate of the 4H-SiC substrate.

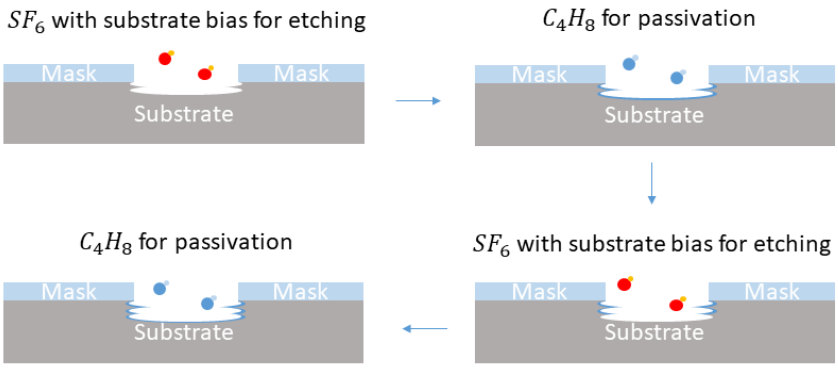


Figure 2.1: Illustration of the Bosch process mechanism for silicon etching

2.2. Etching mechanism

As mentioned in Chapter 1 and the last section, the etching of 4H-SiC substrate involves both physical and chemical mechanisms, both of which, in essence, are ion-enhanced processes. The high-density energetic ions generated by the inductively coupled RF power source are directed toward the substrate surface, breaking the chemical bond between silicon and carbon atoms so that they can react with the etching gases. The following sections will detail the critical factors of the inductively coupled plasma(ICP) reactively ion etching(RIE) process.

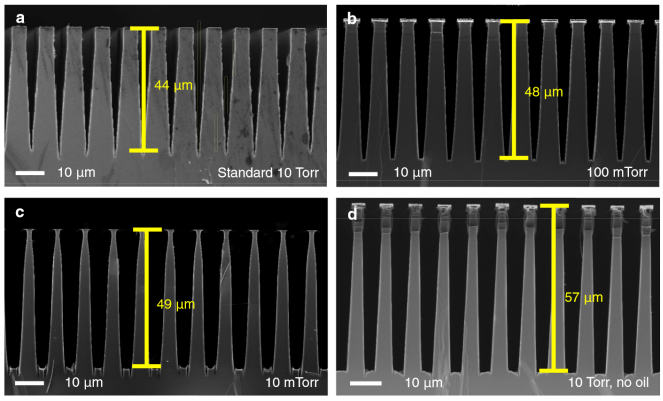


Figure 2.2: Etch profile of 4H-SiC after 2-hour etch in SF_6/O_2 etch gas[13]

2.2.1. Etch gas

The plasma etching process on the SiC surface includes the bond breaking of silicon and carbon atoms, the chemical reaction between etch gases and these atoms, and the pumping out of the volatile reaction products. It was reported that fluorine-based, chlorine-based, and bromine-based gases were chosen to etch the SiC surface because they can form volatile products after the reaction, which are easily removed from the etching chamber.

Fluorine-based gases are the more widely used gases for SiC etching, in which SF_6 is the most common choice for researchers. The primary chemical reactions regarding the removal of silicon and carbon atoms are given as follows:

$$Si + xF \longrightarrow SiF_x \; x \leqslant 1\text{-}4 \text{ (Mostly x=4)}$$

$$C + xF \longrightarrow CF_x \; x \leqslant 1\text{-}3$$

B. Lee et al. [22]reported that the etch rate of SiC when applying fluorine-based gas is almost ten times larger than that involving chlorine-based and bromine-based gases. The reason is the difference in chemical bond energies. Si-C bond energy is smaller compared to Si-F and C-F bonds but larger than Si-Cl, C-Cl, Si-Br, and C-Br bonds, which are the central primary chemical bonds formed in the reaction products from fluorine-based gases, chlorine-based and bromine-based gases, respectively. Nevertheless, chlorine-based gases are sometimes used for SiC etching because the damage induced by plasma etching can be removed by annealing at low temperatures. In contrast, for fluorine-based gases, this is not possible[23].

Besides those reacting with silicon and carbon atoms released from the substrate surface by ion bombardment, additional gases can be added to enhance the plasma etch process. For example, argon has been a prevalent additive gas because it enhances the ion bombardment on the surface to initiate etching, helps in sputtering away possible involatile products formed during etching, and increases the etch rate moderately[23]. Argon can also clean the substrate surface before etching to remove organic residuals that could attract sputtered hard mask material to be redeposited on the surface, acting as the micro mask. The other reported alternatives are oxygen and hydrogen. Oxygen is effective in

cleaning the SiC surface before etching to remove residuals, and it can also be applied together with SF_6 during etching to react with carbon atoms, forming CO and CO_2. Hydrogen effectively removes aluminum redeposited on the surface because of the aluminiferous hard mask or the wall of the etching chamber. Table 2.1 summarizes the gases used in the research about SiC plasma etching process in the last twenty years.

Table 2.1: Various gases used in ICP DRIE process for SiC etching

Author	Gases	Year	Substrate material	Reference
D. Gao et al.	HBr	2003	3C-SiC	[24]
L. Jiang et al.	Cl_2/Ar	2004	4H-SiC	[25]
S. Takenami et al.	Cl_2/O_2	2007	4H-SiC	[26]
K. M. Dowling et al.	SF_6/O_2	2015	4H-SiC	[27]
M. Ozgur et al.	SF_6/O_2	2017	4H-SiC	[14]
J. Li et al.	SF_6/O_2	2017	4H-SiC	[28]
S. Zhuang et al.	SF_6/O_2,HBr/Ar	2019	4H-SiC	[29]
A. A. Osipov et al.	SF_6/O_2	2020	6H-SiC	[18]
P. Mackowiak et al.	SF_6/O_2	2022	4H-SiC	[19]
M. Hayashi et al.	ClF_3	2022	4H-SiC	[30]

The inductively coupled plasma(ICP) reactive ion etching(RIE) process for 4H-SiC is based on removing the silicon layer and the carbon layer by the plasma generated from the etch gases. Take the high-etch rate process, where fluorine plasma, the most widely used etching plasma, is applied, as an example. The reaction products such as SiF_2 formed with fluorine plasma and silicon atoms are usually in the gas phase, so they can easily be pumped out of the etching chamber. However, the fluorine compound generated from fluorine plasma and carbon atoms such as CF and CF_2 are the primary source of the carbon-rich layer formed on the surface during etching, which leads to the decrease in etch rate. Therefore, as indicated in Table 2.1, many works applied oxygen plasma as additive gases to help generate more volatile reaction products such as CO and CO_2 so that these products do not impede the etching process on the substrate surface.

2.2.2. Hard mask material

For patterned substrate etching of 4H-SiC substrate, the material of the hard mask is another crucial factor for obtaining a high-quality etched surface.

Many works of literature have been published on how hard mask materials affect the etching process[16, 28, 31–33]. The primary concern regarding the hard mask is the selectivity of the hard mask material and the level of micro masking induced by the mask material. Photoresist[29], aluminum nitride(AlN)[32], aluminum dioxide(Al_2O_3)[16, 27, 28], silicon dioxide(SiO_2)[27, 29], nickel(Ni)[27, 33],

copper(Cu)[14, 33], chromium(Cr)[18], and aluminum(Al)[34] have been reported to be used as hard mask for SiC etching. In principle, non-metal mask materials such as photoresist and silicon dioxide are considered ”clean” so that they can be used in the CMOS-compatible etching process, but with a cost of low selectivity. Metal hard masks are more resistant against ion sputtering, thus having higher selectivity, but the contamination is significant. Besides, P. H. Yih and A. J. Steckl[34] found that an aluminum hard mask will induce many micro maskings on the etched surface, as indicated in Fig. 2.3. The micro-masking effect can be suppressed by adding hydrogen(H_2) to react with Al, forming volatile products. In contrast, Ni and Cu hard masks induce fewer micro maskings because they are more robust against ion bombardment, thus having fewer particles generated and redeposited on the etching surface.

Figure 2.3: Micro maskings induced by aluminum hard mask[34]

2.3. Etch rate control

Inductively coupled plasma(ICP) reactive ion etching(RIE) on SiC is based on physical and chemical mechanisms. The etch rate of the process is affected by multiple factors, such as ICP source power, chuck bias power, gas flow, pressure, and substrate temperature. Under various circumstances, these factors often have competing effects on the etch rate, complicating the optimization for a faster etching on the SiC substrate.

2.3.1. ICP source power

As mentioned in Chapter 1, the ICP RIE etcher has an extra RF power source to generate high-density plasma. It seems intuitive that the higher the plasma density, the more ions can react with substrate atoms and the larger the etch rate. This is true in some of the works. D. Ruixue et al.[35] reported that the etch

rate of SiC increases almost linearly with ICP coil power. As indicated in Fig. 2.4, the etch rate of SiC has a linear dependence on the ICP coil power in the range from 300W to 800W. F. A. Khan and I. Adesida also reported that in the range from 400W to 1000W, the etch rate increases linearly with ICP coil power, shown in Fig. 2.5. However, it has also been reported by J. Ruan's team[36] that for high ICP coil power in the range from 1500 W to 2500 W, the dependence of SiC etch rate is weak. Fig. 2.6 is a contour plot presented by the team, illustrating the dependence of SiC etch rate on ICP source power and bias power. This indicates a threshold value for ICP source power above which the etch rate stays approximately constant as the ICP source power varies. At high ICP source power, the number of radicals that react with substrate atoms is not the dominant limitation for the SiC etch rate.

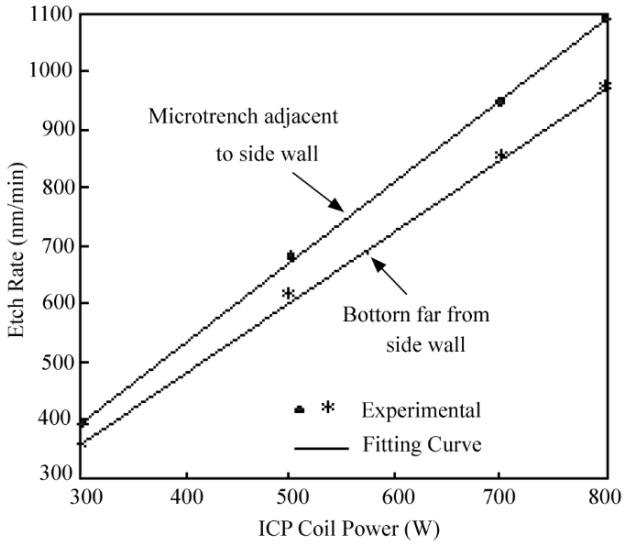


Figure 2.4: Etch rate as a function of ICP coil power in [35]

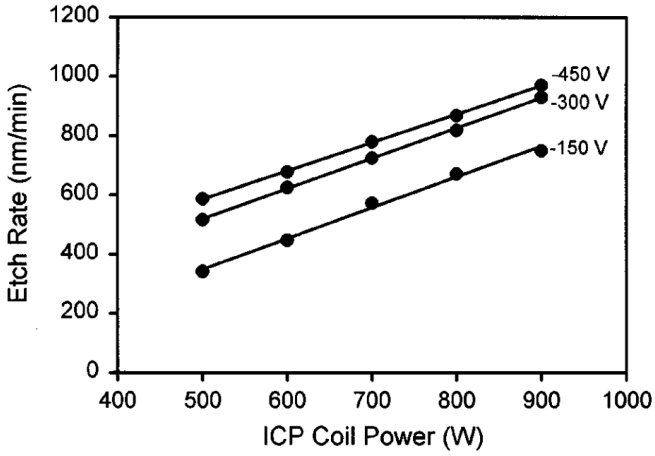


Figure 2.5: Etch rate as a function of ICP coil power in [37]

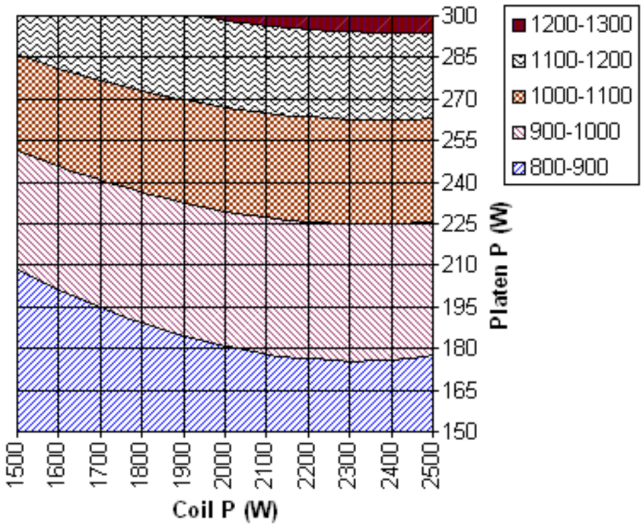


Figure 2.6: Contour plot of SiC etch rate as a function of ICP coil power and chuck bias power in [36], the nominal etch rate is 1 μm/min

2.3.2. Chuck bias power

The effect of chuck bias power, or platen power, is more regarded as a physical mechanism that initiates the etch process[23]. As explained in Chapter 1, the plasma etching on the SiC substrate must be initiated by ion bombardment because of the high bond energy of the Si-C bond. Without the ion bombardment, silicon and carbon atoms can not ”break free” to react with radicals to form volatile products. So, in principle, the bond-breaking speed is one of the crucial limitations of SiC ICP RIE. The higher the bias power or voltage of the chuck electrode, the stronger the ion bombardment so that the bond-breaking speed is higher, thus the etch rate.

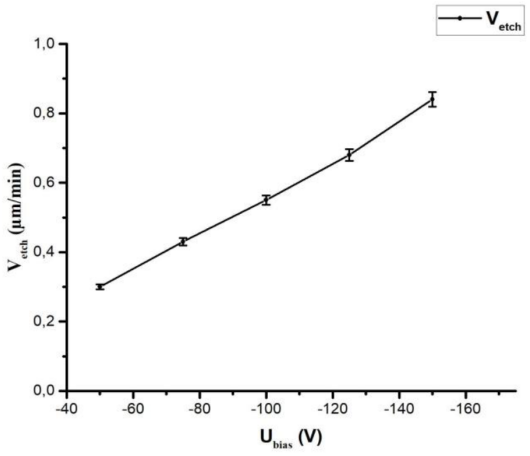


Figure 2.7: SiC etch rate as a function of chuck bias power in [38]

A. A. Osipov et al. [38]found that the etch rate of SiC increases with chuck bias voltage. Fig. 2.7 is a plot of SiC etch rate as a function of the bias voltage applied to the chuck. It shows that the etch rate increases linearly with chuck bias

voltage. The linearity dependence of SiC etch rate on chuck bias voltage/power was also reported by J. H. Choi et al.[12]. Fig. 2.8 presents the relation between SiC pillars height and chuck bias voltage after 180 seconds etch at the pressure of 6 mTorr. Similar to that of ICP source power, the effectiveness of chuck bias power on etch rate reaches a saturation when a threshold value is met, indicating that high Si-C bond breaking speed is no longer the dominant factor of SiC etch rate after getting such value. Instead, the surface-based reaction, most probably the C-F reaction, is the limiting factor for high-enough fluorine production[23].

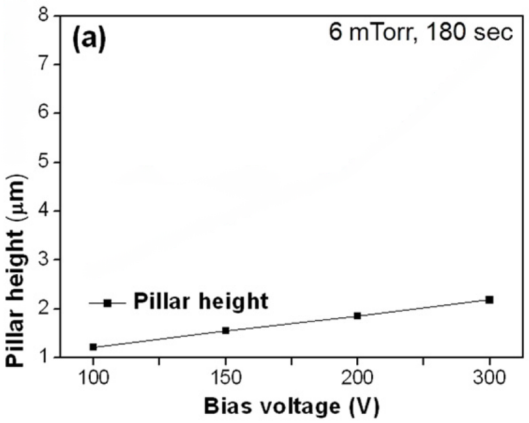


Figure 2.8: SiC etch rate as a function of chuck bias power, adapted from[12]

2.3.3. Gas flow

Not many works are exploring the possible effect of gas flow on the etch rate. It seems that gas flow is the parameter of most minor importance in etch rate control, provided that there is a sufficient gas supply, providing enough radicals to react with the SiC substrate. However, gas flow could affect the etch rate significantly if the etch gases are consumed so fast that there are not enough radicals to react with the SiC surface. This could happen when the area of the SiC surface is too large or a large amount of radicals are consumed by materials from the carrier other than silicon and carbon atoms from the SiC surface. This phenomenon is usually referred to as the loading effect, which will be further explained in the last section of this chapter.

2.3.4. Pressure

The impact of chamber pressure on SiC etch rate involves multiple physical principles that compete with each other. There are many contradictory results of the SiC etch rate as chamber pressure varies.

K. M. Dowling et al.[15] characterized the etch rate as a function of pressure. As shown in Fig. 2.9, the etch rate at the pressure of 10 mTorr is the largest compared to that at 5 mTorr and 15 mTorr. This is because of two competing mechanisms that affect the etch rate differently. One is that more radicals can be ionized at high pressure, providing higher-density plasmas to react with the SiC substrate. The other one is that the mean free path of radicals at high pressure

decreases, which means more random collisions between these radicals and chamber walls or the radicals themselves. So, the ion bombardment necessary to initiate the etching is undermined, thus decreasing the etch rate. The etch rate at low pressure is the other way around, generating fewer radicals but having less collisions. Besides, K. Yu. Osipov and L. E. Velikovskiy[39] presented very similar results in Fig. 2.10. The etch rate decreases with pressure when the value exceeds 10 mTorr. Nevertheless, N. Okamoto[40] found that the etch rate increases with pressure from 0 Pa to 5 Pa, then stays constant for pressures larger than 5 Pa, shown in Fig. 2.11.

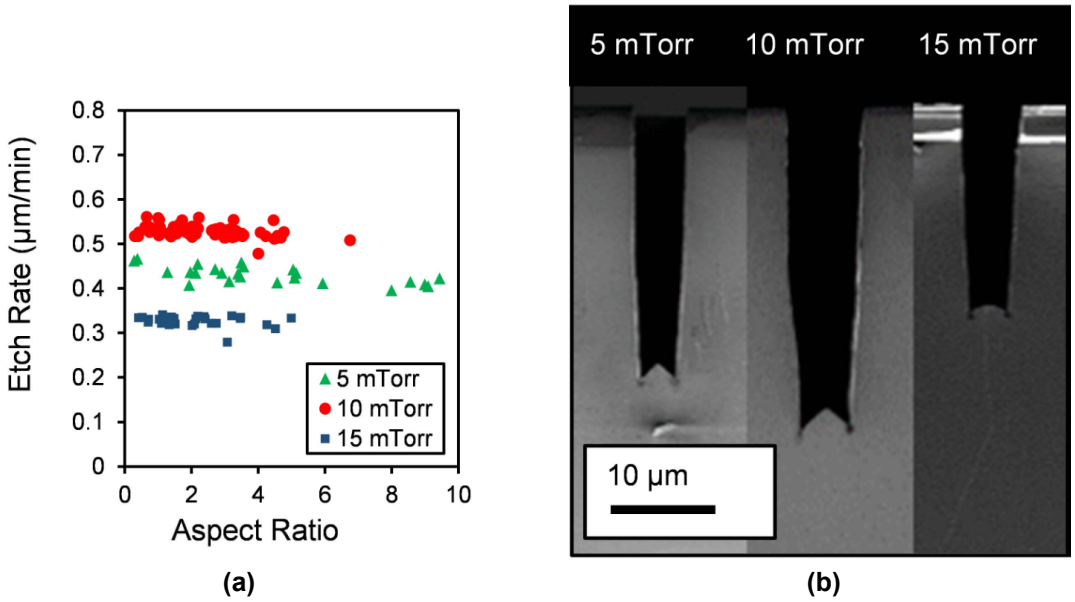


Figure 2.9: SiC Etch rate at different pressure[15]

2.3.5. Substrate temperature

The effect of substrate temperature on the etch rate depends on the chemicals applied in the plasma etch process. The impact can be completely different with various etch gases. Take fluorine-based gases as an example, A. A. Osipov et al.[18] reported that the etch rate of SiC using SF_6/O_2 increases with substrate temperatures before it reaches 150 °C. The etch rate remains constant when the temperature exceeds 150 °C. However, the effect is entirely different for chlorine-based gases. In the work[25], L. Jiang et al. used chlorine(Cl_2) and argon(Ar) to etch the SiC substrate. Fig. 2.12 shows that the etch rate decreases with temperature. This is due to the existence of a Cl_2 surface coverage at lower temperatures. This concentrated Cl layer could react more efficiently with silicon and carbon atoms, forming more $SiCl_x$ and CCl_x products. In summary, the substrate temperature can have a completely different impact on the etch rate in terms of the etch gases used in the process.

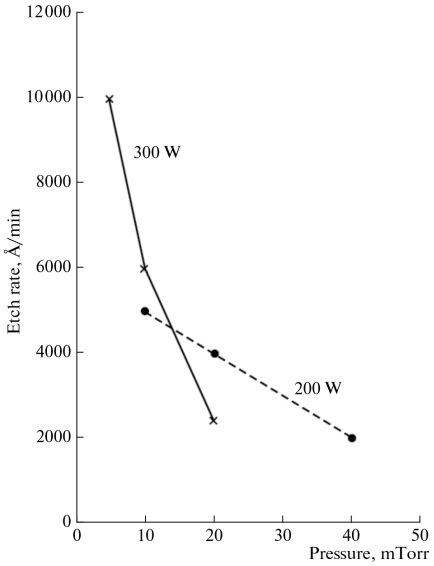


Figure 2.10: SiC Etch rate as a function of pressure at 200 W and 300 W chuck bias power, adapted from[39]

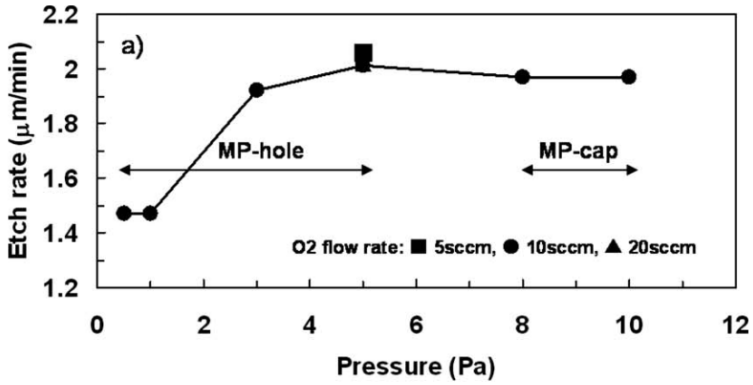


Figure 2.11: SiC Etch rate as a function of pressure in[40]

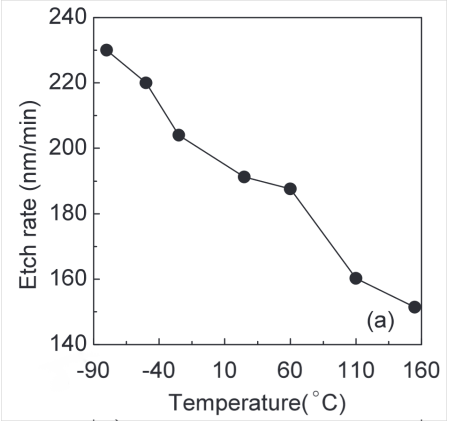


Figure 2.12: SiC Etch rate with Cl_2 and Ar as a function of temperature[25]

2.3.6. Loading effects

Loading effect, in essence, is the effect of gas supply on the etch rate of the surface being etched by the plasma. As mentioned in Subsection 2.3.3, the higher the gas flow, the more the radicals can be ionized, generating plasmas. On the other hand, the larger the exposed SiC surface, the more ions it consumes. When the gas flow is large enough to provide a sufficient dose of ions to react with the exposed SiC surface, the etch rate is more dependent on other factors. However, if the area of the exposed SiC is very large, there could be no sufficient ions to react with silicon and carbon atoms from the exposed surface. A significant decrease in the etch rate will then occur. This was called the macro loading effect in [23]. There is also a ”micro” loading effect. Getting the ions into the deep vias to react with the via bottom is more challenging for via structures with small openings because it is more difficult to pump the reaction products out of the deep via when the via gets deeper, so the etch rate decreases during long-time etching for high aspect ratio structures. Both the ”macro” loading effect and the ”micro” loading effect were reported by P. Leerungnawarat et al. in the work where SF_6 was used to etch SiC[41].

2.4. Morphology control

The morphology of the etched substrate is another crucial factor that must be considered with great care when designing the ICP RIE process. The challenges of gaining a high-quality profile of SiC substrate include conquering the micro masking effect induced by hard mask or carrier material, the micro trench effect, and achieving anisotropic etching.

2.4.1. Micro masking effect

As mentioned in Subsection 2.2.2, the ion bombardment of the hard mask can generate particles that can act as a micro mask when they redeposit on the SiC surface, leading to pillar formation. This is called the micro masking effect. Fig. 2.13 illustrate how the micro maskings are generated. In Fig. 2.13a is a SiC sample with a patterned mask layer. When the bias voltage is applied, ions are accelerated toward the sample, gaining high kinetic energy. The ions will collide with the hard mask surface or the SiC surface, depending on the location to which they are attracted. As indicated in Fig. 2.13b, ion bombardment co-occurs at the hard mask and SiC surfaces. Then, in Fig. 2.13c, particles are generated from the hard mask surface by the sputtering of the plasma. These particles can redeposit on the SiC surface where the etching occurs, as shown in Fig. 2.13d. The redeposited hard mask material will again perform as a micro mask, preventing the covered SiC area from being etched. This will lead to pillar formation on the SiC surface, as shown in Fig. 2.13e. The more the hard mask material redeposit on the SiC surface, the more pillars appear. Pillars of large densities on the surface are the ”grass formation” phenomenon reported by several researches[12, 36, 42, 43]. So, to suppress or avoid the micro masking effect, materials used as a hard mask must be as robust as possible against ion bombardment to reduce the particles generated during sputtering. The parameter

setting for ICP RIE should also be carefully decided, such as applying lower bias power for less ion bombardment.

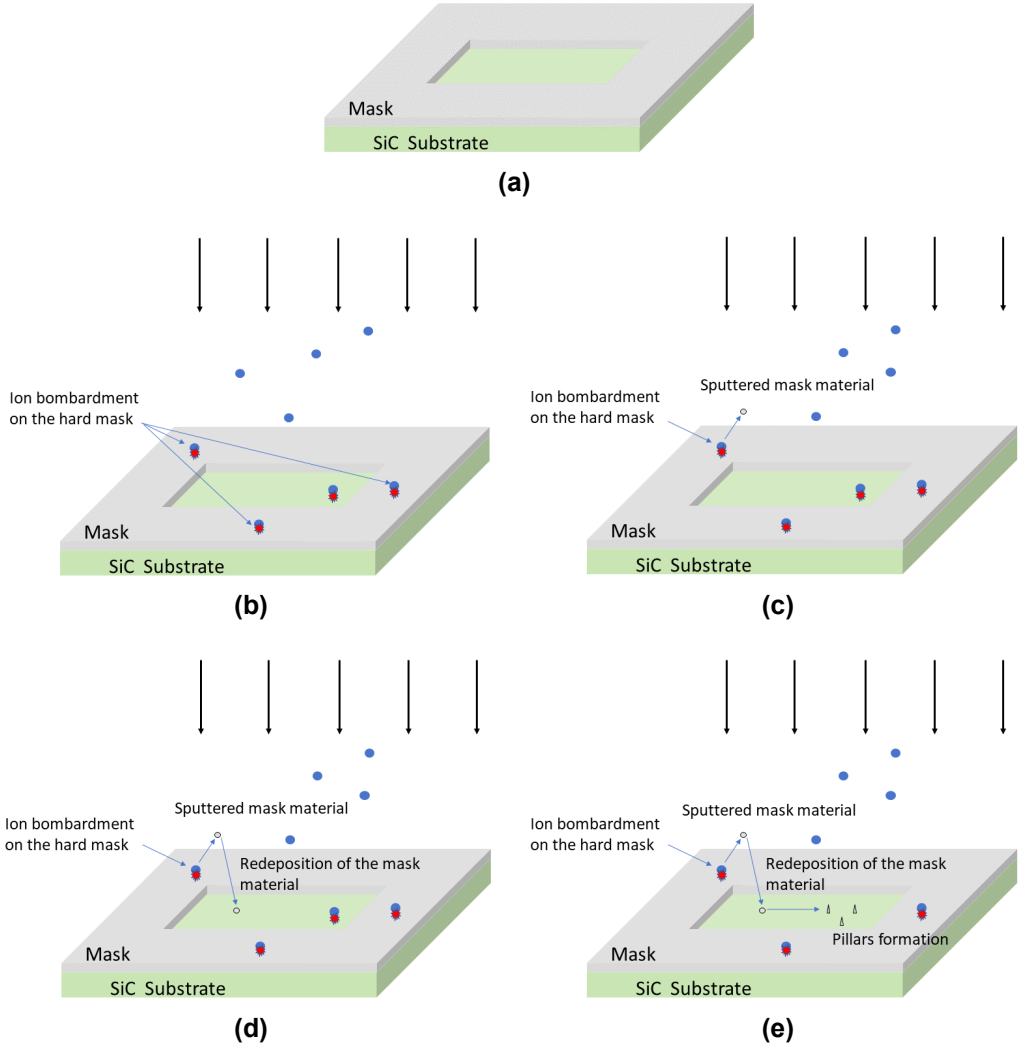


Figure 2.13: Micro masking effect mechanism

2.4.2. Micro trench effect

It has been reported that the additive oxygen gas applied when using SF_6 to etch SiC will induce an unwanted etch profile on the SiC substrate. Trenches were found at the bottom of etched SiC structures[35, 44, 45]. The reason of the formation of these trenches is that a layer composited of SiF_aO_b was formed at the bottom of the side wall during the etching[46]. This layer can easily be charged, thus attracting more ions, which are expected to reach the plane surface of SiC rather than the side wall. With more ions ”gathering” at the bottom corner

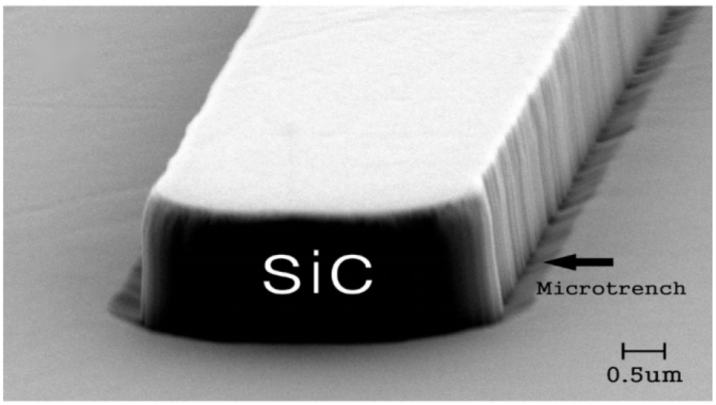


Figure 2.14: Micro trenches found at the bottom of the etched SiC structure with O_2 plasma applied during the etching[44]

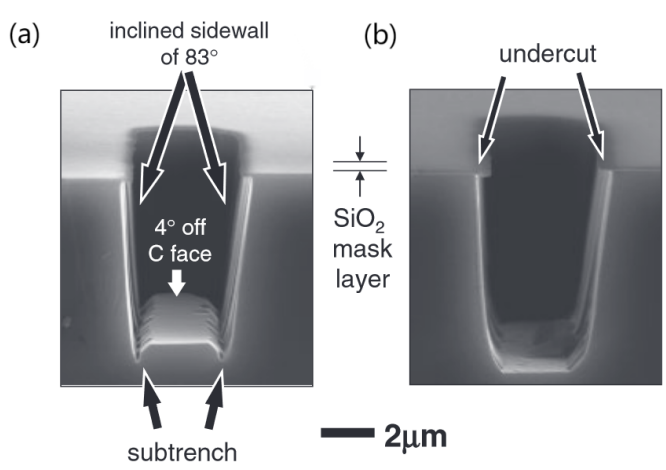


Figure 2.15: Etched 4H-SiC,(a) Before thermal Cl_2 etching.(b) After 30 min thermal Cl_2 etching[47].

of the etched SiC vias, the local ion bombardment is enhanced, leading to a higher bond-breaking speed and, thus, a higher etch rate than that at the plane surface of SiC. ”V” shape micro trenches result from such effect, as shown in Fig. 2.14.

This effect can be suppressed by applying thermal chlorine etching, reported by H. Koketsu’s team[47]. Fig. 2.15 shows the etched 4H-SiC structures before and after thermal chlorine etching. Another way is not applying oxygen plasma during etching since it will help generate SiF_aO_b, presented by H. Ru’s team[48] in Fig. 2.16.

2.4.3. Anisotropic etching

Since the bond energy is high between silicon and carbon atoms, there is almost no lateral etching on the SiC. Unlike the Bosch process for silicon plasma etching, the SiC plasma etching process does not need a passivation cycle to protect the side wall from being etched by the etching gases. As long as the bias voltage

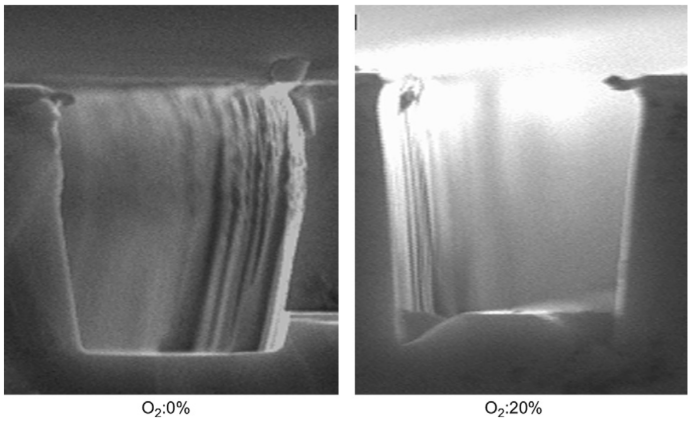


Figure 2.16: Etched 4H-SiC, with 0% O_2 and with 20% O_2[48].

is applied vertically to the SiC surface, the ion bombardment on the side wall, which initiates the SiC etching process, can be ignored. So, it is easier to achieve anisotropic etching in SiC than in silicon.

2.5. Conclusion

This chapter introduces the principles and mechanisms of ICP RIE for SiC. The effect of several crucial factors on the SiC ICP DRIE results has been explained with the support of the literature of previous works. Interestingly, the etch rate and etch profile control of SiC does not only rely on the ICP RIE process settings but also depends on the specifications of the desired structures to be fabricated on the SiC substrate. This means trade-offs must be made to develop an optimal process based on a specific application. Chapter 3 will elaborate more on these strategies in ICP RIE process development.

3

Design of Experiments

In Chapter 2, the principles of ICP RIE were introduced. This chapter will further discuss the role of these principles in ICP RIE process development and the Design of experiments(DOE), starting with the selection of the hard mask materials(Section 3.1). Then, the first version of parameter settings for the process design will be introduced(Section 3.2). The initial results will be presented, including details of sample preparation of the ICP RIE process for SiC substrate(Section 3.3). The observed experiment phenomenon and issues will be explained, followed by the preliminary optimization solutions(Section 3.4). The effect of carrier wafer materials in optimizing DOE will be discussed(Section 3.5). Finally, the characterization and analysis methods will be described to determine the etch rate, micromasking level, and selectivity. The experiments were supported by Else Kooi Laboratory(EKL) and Kavli Nanolab at Delft University of Technology.

3.1. Hardmask Materials

As presented in Subsection 2.2.2, various options of hard mask materials for patterned SiC substrate plasma etching are reported in the literature. However, not all the options are applicable due to limitations such as contamination control, project specifications, and cost-effectiveness. For example, M. Ozgur et al.[33] researched the selectivity of copper(Cu) and nickel(Ni) under SF_6 and O_2 plasmas. The result indicates that the selectivity of copper is 163.7, while that of nickel is 25.4. D.W. Kim et al.[49] presented the etch rate of copper, nickel, and aluminum in Fig. 3.1. Both works concluded that copper has the highest selectivity, making it very suitable as a hard mask material to pattern MEMS devices. The high selectivity of copper is because non-volatile products such as Cu_2F and Cu_2O are formed during etching, protecting the copper layer from the ion bombardment[12]. It seems that copper is the best candidate as a hard mask material. However, copper is considered a contaminant metal in semiconductor processing, which will significantly contaminate the fabricated devices and tools used for processing the devices. So, the use of copper is strictly limited or even forbidden in many tools in the cleanroom laboratories. Though it has the optimal characteristics, copper is not the superior choice as a hard mask material regarding contamination control.

This work chooses nickel as one option for the hard mask material. This is

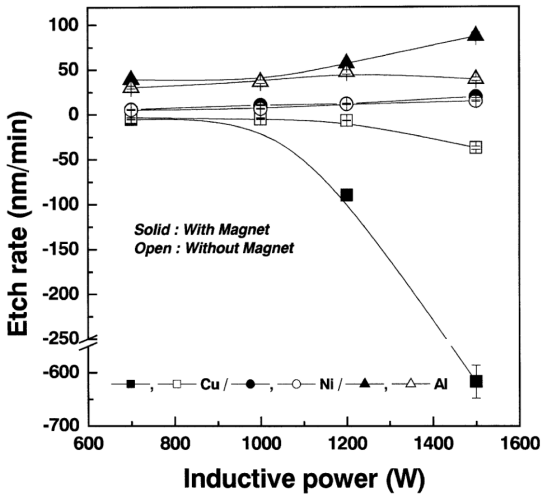


Figure 3.1: Etch rates of copper, nickel, and aluminum as a function of inductive power with and without magnetic field, at powers higher than 1200 W, deposition instead of etching of copper occured[49].

because of the contamination control requirement in the cleanroom laboratory. In this case, nickel's contamination level is lower than copper's, which is acceptable under the current management regulations. So, the responsible staff authorized the use of nickel as the hard mask in the cleanroom laboratory. On the other hand, the selectivity of nickel is much higher than aluminum's, as reported in the literature, so nickel was the optimal choice as the hard mask material.

Besides, SiO_2 is another option. Though the selectivity of SiO_2 is in the range from 0.8 to 3[23], much lower than that of nickel, which is 25.4 reported in [33], it is a ”clean” hard mask material comparing to nickel. This means that the ICP RIE process using SiO_2 as the hard mask material has the potential to be integrated into other ”clean” processes, such as the CMOS process.

To sum up, the process development follows two technical routes regarding hard mask materials. The main technical route uses the nickel hard mask, focusing on etch rate optimization and etch profile defect suppression. The exploration of the ICP RIE process using SiO_2 lays more emphasis on low-temperature plasma etching on SiC substrate, investigating the characteristics of the etched profile at extremely low temperatures.

3.2. Process design

As introduced in Chapter 2, multiple factors play a role in the ICP RIE process, such as ICP source power, chuck bias power, gas flow, pressure, and substrate temperature. This work uses SF_6 and O_2 as etch gases to etch the 4H-SiC substrate. The roles of these factors in process design are presented below:

1) ICP source power: ICP source is used to generate high-density plasma so that sufficient numbers of radicals react with the SiC substrate. In principle, the higher the ICP source power, the larger the plasma density, thus more radicals

to react with the SiC substrate, increasing the etch rate. However, J. Ruan et al.[36] reported that at high ICP source power, the etch rate no longer has a strong dependence on ICP source power, indicating that there is a saturation value, above which the etch rate stays approximately constant.

2) Chuck bias power: The chuck bias provides the ionized radicals' kinetic energies, directing them toward the substrate surface. Then, the bombarded substrate surface will generate "free" silicon and carbon atoms to react with plasma. The higher the bias power, the stronger the ion bombardment; the more "free" atoms, the higher the etch rate. However, the high etch rate is achieved by applying high chuck bias power at the cost of more severe damage to the hard mask. This leads to lower selectivity and could cause more micro maskings from the sputtered and re-deposited hard mask material.

3) Gas flow: Generally, the flow does not affect the etch rate significantly. Higher gas flow provides more etch gas molecules to be ionized. If the substrate surface's consumption of etch gas molecules is not high, the gas flow will not affect the etch rate. However, if the contrary is true, often referred to as the loading effect, the etch rate will decrease since the gas supply is insufficient for consumption due to low gas flow.

4) Pressure: There are two competing mechanisms of how pressure affects the etch results. High pressure helps generate more plasma, providing more radicals to react with the substrate surface, thus increasing the etch rate. Nevertheless, the high pressure also reduces the mean free path of plasmas, which means more random collisions between the radicals and etching chamber walls, undermining the ion bombardment effectiveness on the substrate surface, so the etch rate will decrease. Besides, random collisions between the sputtered hard mask materials might increase the chance of these particles to re-deposit on the surface, leading to the micro masking effect, as introduced in Subsection 2.4.1.

5) Substrate temperature: As introduced in Section 2.3, the SiC etching process is based on both physical removal and chemical reaction. Though higher substrate temperature enhances the chemical reaction between plasmas and the substrate, thus increasing the etch rate, the surface roughness will increase with substrate temperatures below 150 °C[18].

It can be seen that the role of these factors in ICP RIE development is complicated. Trade-offs must be made to achieve an optimal recipe for ICP RIE on 4H-SiC. The available tools are presented in Table 3.1. Last, Else Kooi Laboratory(EKL) in Delft University of Technology provides the mask used to pattern the substrate, shown in Fig. 3.2.

3.3. Initial results

This section will present the initial results of the ICP RIE process development from the main technical route, where Ni was chosen as the hard mask material. The other technical route will use SiO_2 as the hard mask material, details of which will be presented in Chapter 4. The sample preparation will be briefly described. The initial test results of SiC samples, including etch rate and etch

Table 3.1: Available tools for SiC ICP RIE

	AMS110 I-speeder(Adixen)	Plasma Pro 100 Estrelas(Oxford)
Gases	SF_6,O_2,C_4F_8,Ar,He	SF_6,O_2,C_4F_8 Ar,CH_4,He
Cooling systems	Lauda chiller -10 °C-60 °C	Liquid nitrogen or chiller -150 °C-70 °C
Sources	ICP RF 2.8kW Bias 300W	ICP RF 8kW Bias 600W
Owner	Else Kooi Laboratory	Kavli Nanolab

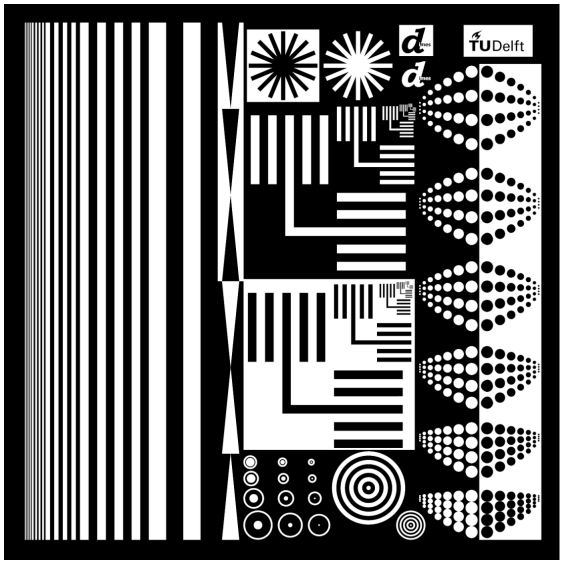


Figure 3.2: The mask used for patterning the substrate, provided by EKL

profile geometry, will be shown next. Then, the EDS analysis details on the etched surface will be presented. Finally, preliminary optimization action was performed and explained.

3.3.1. Samples preparation

A 4H-SiC wafer with 365 μm thickness was used for the experiments. The wafer was subject to nickel layer deposition, photolithography, wet etching, and dicing to make 6 mm x 6 mm SiC dies. The sample preparation process is shown below:

1) Nickel(Ni) layer deposition: The nickel layer of 1 um thickness was deposited on the front side of the 4H-SiC wafer in the Trikon Sigma 204 Dealer tool at 350 °C by physical vapor deposition(PVD). The measurement result of the nickel layer thickness is around 850 nm.

2) Photolithography: Firstly, a 10 min hexamethyldisilazane(HMDS) was done to the nickel-coated 4H-SiC wafer. Then, it was manually coated with 1.4 μm SPR3012 photoresist using the spin coat method, followed by 1 min soft bake at

95 °C on a contact hotplate. After that, the exposure was done in the ASML PAS 5500/80 wafer stepper tool. Since the mismatch of thermal expansion coefficients between the deposited nickel layer and SiC substrate induced the bowing of the SiC wafer, bringing alignment issues, the wafer was exposed using a dedicated recipe, where only central areas of the wafer were exposed. Finally, the wafer was manually developed using MF322, rinsed and dried.

3) Wet etching: To form the patterned nickel layer, the exposed nickel was removed using the wet etching method in a solution buffered hydrofluoric acid(BHF): 65% nitric acid(HNO_3): DI water in the ratio 1:1:50 for 45 minutes.

4) Dicing: 65 6 mm x 6 mm die-level samples were available for the ICP RIE test after dicing.

3.3.2. Preliminary test results

The 6 mm x 6 mm 4H-SiC samples using a nickel hard mask were cleaned with an ultrasonic tool using chemicals in sequence: Acetone, Ethanol, and IPA. Samples were cleaned in each chemical for 10 minutes, at 44 kHz, 40 °C. Then, one sample was glued on a sapphire carrier wafer with Fomblin oil. After that, this sample was etched in the Adixen AMS110 tool. The parameter settings for the initial test are shown in Table 3.2. The gas flow ratio of SF_6 and O_2 is kept at 4:1 because it has been reported that this is the best ratio to achieve maximum etch rate[12, 35, 37]. This is because the presence of O_2 increases the etch rate of the carbon layer in SiC, forming volatile products such as CO and CO_2. However, when the percentage of O_2 is too high, oxidation will occur on the SiC surface, preventing the substrate from being further etched, thus decreasing the etch rate.

Table 3.2: Patameter settings for the initial test

ICP source power	2500 W
Chuck bias power	150 W
Pressure	1.4 E-2 mbar
SF_6	240 sccm
O_2	60 sccm
Substrate temperature	20 °C
Etch time	10 minutes
Carrier wafer material	Sapphire

Fig. 3.3 are the SEM images of the etched SiC structures after a 10-minute etch. It can be seen that there are massive grass-like pillars formation on the etched SiC surface, indicating that a very significant micro masking effect was found on the etched surface. The etching profile was measured on the Dektak tool. It shows that the etched depth, including the remaining thickness of the nickel layer, was 2215 nm. The etch rate of SiC is between 100 to 140 nm/min. This result is comparable to the work presented by Middelburg, L. M.[50], in

which 135.17 nm/min was achieved with similar settings. However, the etch rate is too low, and the micro-masking level is unacceptable.

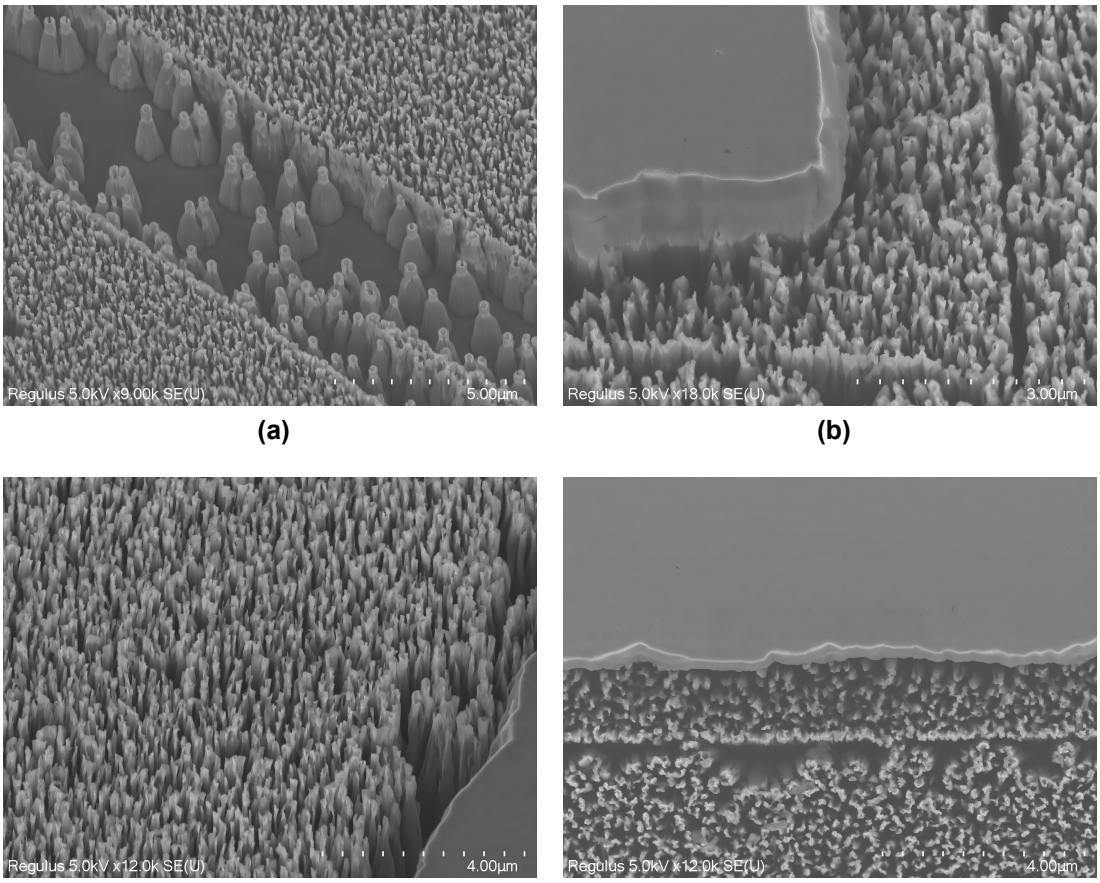
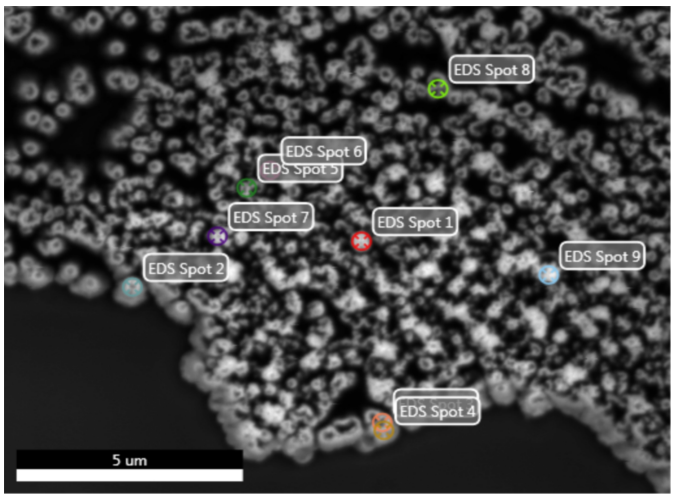
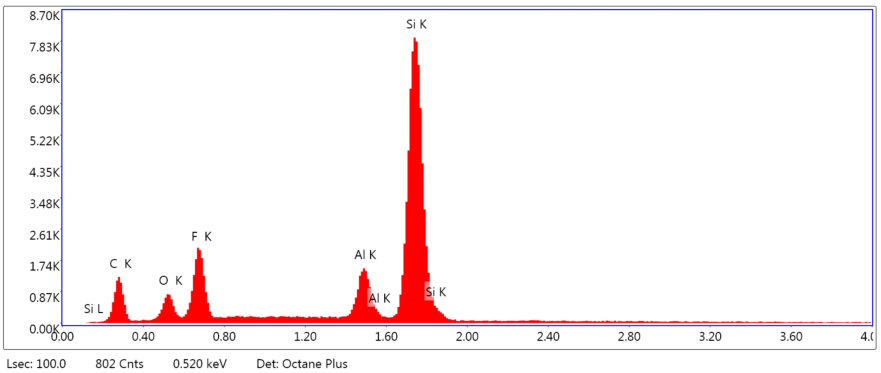


Figure 3.3: SEM images of the SiC structure after the initial test, a sapphire carrier was used. Parameters in Table 3.2 were applied

An energy-dispersive X-ray spectroscopy(EDS) analysis was performed using the SEM XL30 SFEG tool to explore the possible cause of the pillar formation on the SiC surface. Fig. 3.4 are the SEM images of the sampling area and the related spectrum. Nine points at the top of the pillars were chosen to be sampled. Since these nine figures have similar spectrums, two of them were displayed. It can be seen from the EDS spectrum that a peak of aluminum appears together with a fluorine peak of approximately the same height. This indicates that the chemical compound AlF_x was formed during the etching, where the aluminum element originates mostly from the sapphire carrier wafer because it is the closest aluminum source to the sample. This compound acts as a micro mask during the etching, causing local etch rate difference and, thus, pillar formation. On the other hand, nickel did not cause the micro-masking effect in this case. The nickel layer is more resilient against ion bombardment, and the EDS spectrum showed that almost no nickel was on the etched surface.



(a)



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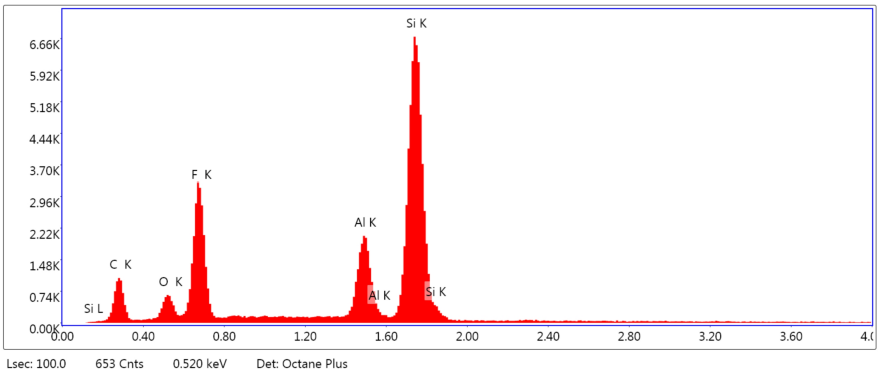


(c)

Figure 3.4: EDS results of the preliminary test:(a) is the sampling area, where 9 points were sampled. (b) and (c) are two of these nine sampling points, showing the same trend in the spectrum distribution with other points

3.4. Preliminary optimization 1: role of pre-cleaning and parameter settings

The last section presented the preliminary result of the ICP RIE process, which shows a significant micro-masking effect on the surface and a very low etch rate.

The optimization steps were performed to suppress the micro-masking effect and increase the etch rate. The optimization strategy includes three parts: 1) Sample pre-cleaning before etching process. 2) Optimizing ICP RIE parameters and 3) Testing with different carrier wafer materials. This section will introduce the first two actions to suppress the micro-masking and improve the etch rate. The role of carrier wafer materials will be explained in detail in the next section.

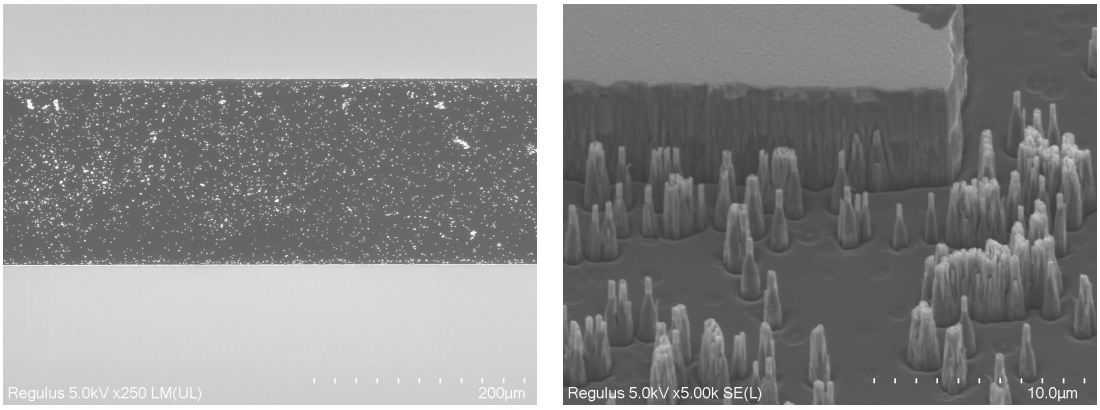
The preliminary micro-masking level optimization is done by a pre-cleaning step with argon plasma on the sample before etching. The goal is to sputter away the organic residues from previous processes, such as photoresist used during photolithography. This is to prevent the sputtered materials from being ”trapped” by those organic residues on the SiC surface, increasing the risk of re-deposition of the sputtered hard mask material or carrier wafer material on the substrate. The argon plasma cleaning parameter setting is shown inTable 3.3. Fig. 3.5 show the optimized etching results with a pre-cleaning step by the argon plasma using the same setting in Table 3.2. It can be seen from Fig. 3.6 that the micro-masking densities were reduced compared to that in Fig. 3.3, which was without the argon pre-cleaning. However, as indicated in the SEM images, the effectiveness of argon plasma pre-cleaning is limited, and the micro-masking level is still unacceptable with pillar clusters on the SiC surface. It is not possible to apply this process in MEMS device fabrications.

Another option is to perform the pre-cleaning step with oxygen plasma. Argon plasma cleaning is, in essence, a physical cleaning by sputtering the residues away from the SiC surface. In contrast, oxygen plasma cleaning is enhanced by a chemical mechanism, forming volatile products with organic residues that can be pumped out of the etching chamber easily. Fig. 3.7 shows the etched SiC surface with a pre-cleaning step by oxygen plasma. The micro-masking density is further suppressed with oxygen plasma, and some areas are almost micro-masking-free. This result proves the effectiveness of oxygen plasma pre-cleaning in suppressing the micro masking. Since argon and oxygen plasma are proven effective in micro-masking suppression, respectively, it is straightforward that a pre-cleaning step applying oxygen and argon plasma could help reduce the pillar formations on the etched surface.

The optimized pre-cleaning, applying a 15-minute oxygen plasma cleaning, followed by another 15-minute argon plasma cleaning, was added before the ICP RIE as a standardized step of the process design.

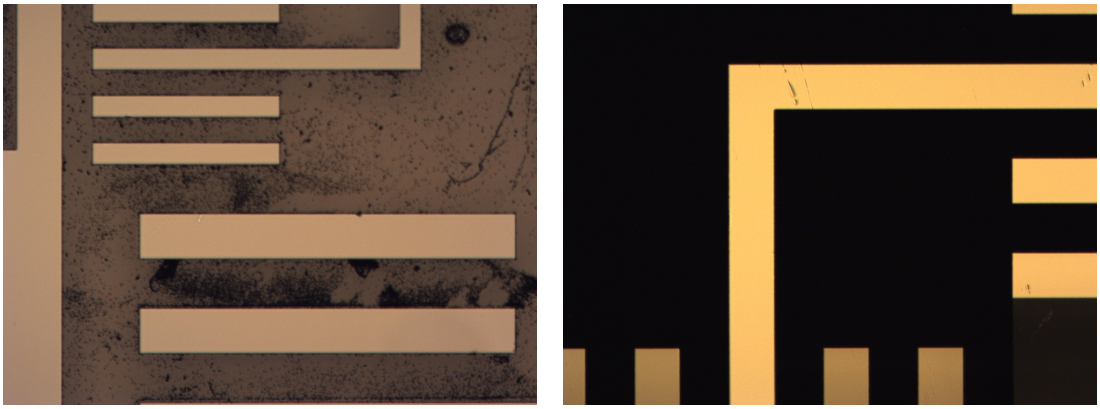
Table 3.3: Argon plasma cleaning settings

ICP source power	2000 W
Chuck bias power	20 W
Pressure	1.4 E-2 mbar
Ar	50 sccm
Substrate temperature	20 °C
Clean time	15 minutes



(a) **(b)**

Figure 3.5: SEM images of the etched 4H-SiC sample with a pre-cleaning step by argon plasma, a sapphire carrier was used.



(a) **(b)**

Figure 3.6: Microscope images of the etched 4H-SiC sample:(a)with a pre-cleaning step by argon plasma.(b)without a pre-cleaning step by argon plasma. A Sapphire carrier was used.

The preliminary etch rate optimization is conducted by changing the ICP RIE parameter settings. As discussed in Chapter 2, ICP RIE parameters can have competing effects on the etch rate of SiC. For the preliminary optimization, chuck bias power and gas flow were chosen to vary to investigate the possibilities of achieving a higher etch rate because these parameters do not have a competing effect on the etch rate. In principle, the etch rate increases with chuck bias power at the cost of lower hard mask selectivity and a higher risk of getting a micro masking effect. As for the gas flow, it affects the etch rate only when the loading effect is significant. In addition, K. Yu. Osipov and L. E. Velikovskiy[39] reported that applying argon as an additive gas with the same gas flow of SF_6 will also maximize the etch rate. Considering these factors, in the setting shown in Table 3.4, argon was added as the additive gas, and the ratio of SF_6,O_2, and Ar is 4:1:4. Finally, the chuck bias power was increased to 300 W, which is the

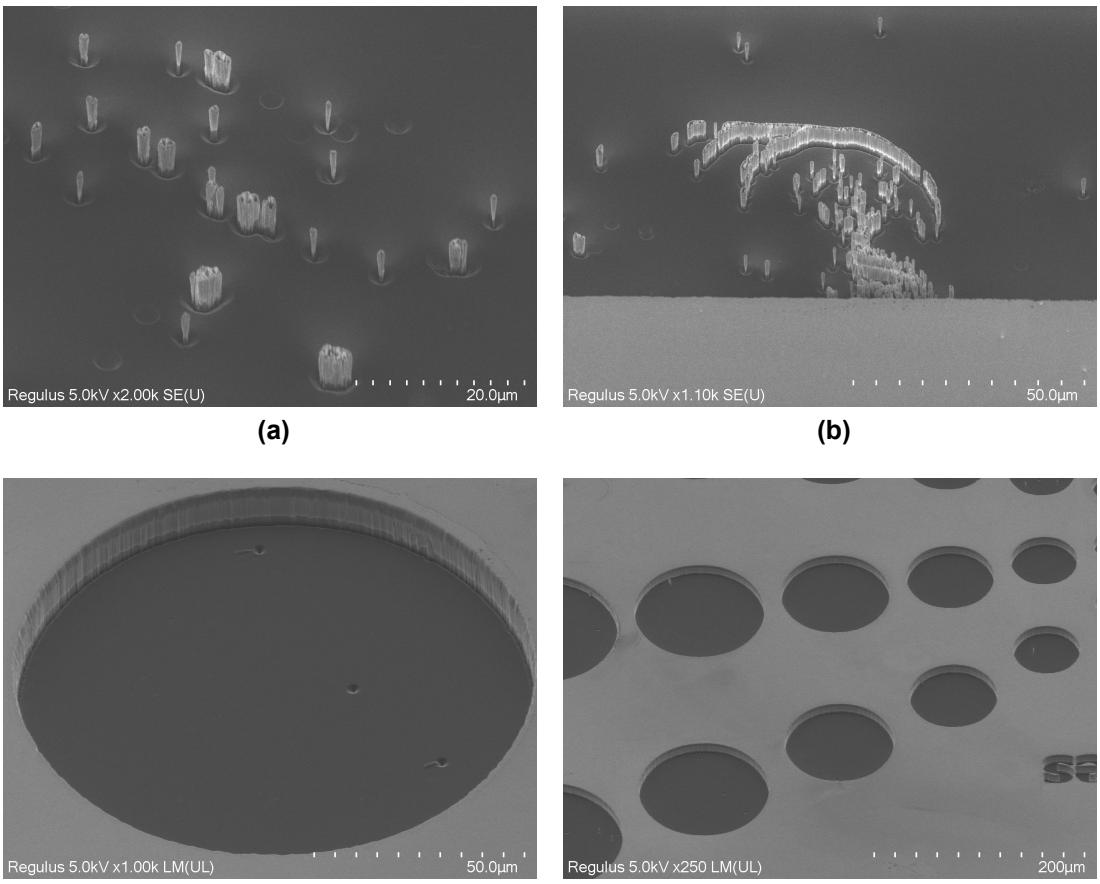


Figure 3.7: SEM images of the etched 4H-SiC sample with a pre-cleaning step by oxygen plasma. A sapphire carrier was used.

maximum value of the Adixen AMS110 tool. Fig. 3.8 shows the cross-section of the etched profile. It can be seen that the etch depth is 10.1 μm after a 10-minute etch, indicating an etch rate of 1 μm/min.

Table 3.4: ICP RIE preliminary optimization settings

ICP source power	2500 W
Chuck bias power	300 W
Pressure	1.4 E-2 mbar
SF_6	60 sccm
O_2	15 sccm
Ar	60 sccm
Substrate temperature	20 °C
Etch time	10 minutes
Carrier wafer material	Sapphire

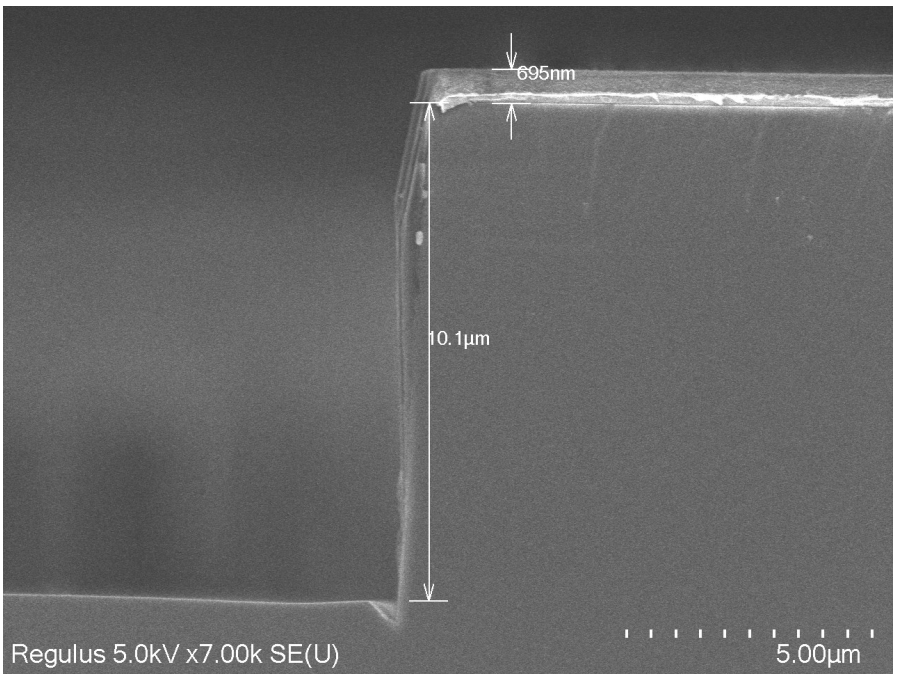


Figure 3.8: SEM image of the cross-section of the etched 4H-SiC after preliminary optimization

3.5. Preliminary optimization 2: role of carrier wafer materials

In the last section, optimization focusing on micro-masking suppression and etch rate have been introduced, respectively. However, it can be seen from Fig. 3.5 and Fig. 3.7 that the micro-masking level is still unacceptable. According to the spectrum results from EDS analysis in Fig. 3.4b and Fig. 3.4c, the pillars on the SiC surface are due to the compound formed with aluminum element, where its source is the sapphire wafer consisting of Al_2O_3. This suggests that the carrier wafer material profoundly affects the etching result. This section will introduce the preliminary optimization strategies based on the test with different carrier wafer materials.

3.5.1. Sapphire carrier wafer

It has been reported that the selectivity of Al_2O_3 to SiC is more than 8[16, 27], this makes sapphire a suitable option to be used as the carrier wafer material. It is more robust against ion bombardment than the SiC substrate, so it can be used multiple times, thus satisfying the cost-effectiveness requirement. This also means the etch rate of sapphire is low, so the consumption of etch gases by the sapphire wafer is low during the etching, which helps minimize the loading effect induced by the carrier wafer. However, it has been proven by the EDS analysis that the sapphire carrier wafer will induce micro-masking when ion bombardment occurs on the SiC substrate and the carrier wafer simultaneously during the ICP RIE process.

3.5.2. Silicon carrier wafer

The ICP RIE test using silicon carrier wafers was conducted to avoid aluminum elements, which could induce micro-masking on the surface. Table 3.5 shows the parameter settings for tests using silicon carrier wafers.

Table 3.5: ICP RIE settings for silicon carrier wafers test

ICP source power	2500 W
Chuck bias power	300 W
Pressure	1.4 E-2 mbar
SF_6	100 sccm
O_2	25 sccm
Ar	100 sccm
Substrate temperature	20 °C
Etch time	10 minutes

First, p-type silicon carrier wafers were used. With the same parameter settings in Table 3.4, the etch profile is presented in Fig. 3.9 and Fig. 3.10. The SiC etch depth is 8.6 μm after a 10-minute etch, which is lower than that using a sapphire carrier wafer. This is due to the loading effect introduced in Chapter 2. The ICP RIE process of SiC is based on silicon layer and carbon layer removal, which suggests that the etch gases will also etch the silicon carrier wafer, thus increasing the etch gas consumption on the carrier wafer. When the gas flow is too low compared to the consumption on the carrier wafer, insufficient radicals will be provided to etch the SiC surface, leading to a decrease in the etch rate. The gas flow setting was pushed to the limits of the Adixen AMS110 tool to minimize the loading effect. Besides, it can be found in Fig. 3.10 that micro-masking is suppressed by avoiding sapphire carrier wafer.

After the test on the p-type silicon wafer, n-type silicon wafers were chosen to do the ICP RIE test. The profile was measured using the Dektak tool. The measured depth is lower than that using a sapphire carrier wafer, which again suggests a loading effect because of the consumption of etch gases by the carrier wafer. Fig. 3.11 are the microscope images of the etched SiC sample. The micro-maskings on the surface were significantly suppressed. Except for several black spots on the sample, a micro-masking-free SiC etching profile was achieved.

3.5.3. SiO_2 coated silicon carrier wafer

Though an n-type silicon wafer was proven to be a superior choice as a carrier to guarantee a micro-masking-free SiC surface, the etch rate is lower compared to that using the sapphire carrier wafer because of the loading effect. To achieve a micro-masking-free SiC surface and a high etch rate simultaneously, a SiO_2 coated n-type silicon wafer was chosen for the ICP RIE test.

5 μm SiO_2 was deposited in the Novellus tool using the plasma-enhanced chemical vapor deposition(PECVD) method to make the carrier wafer. The

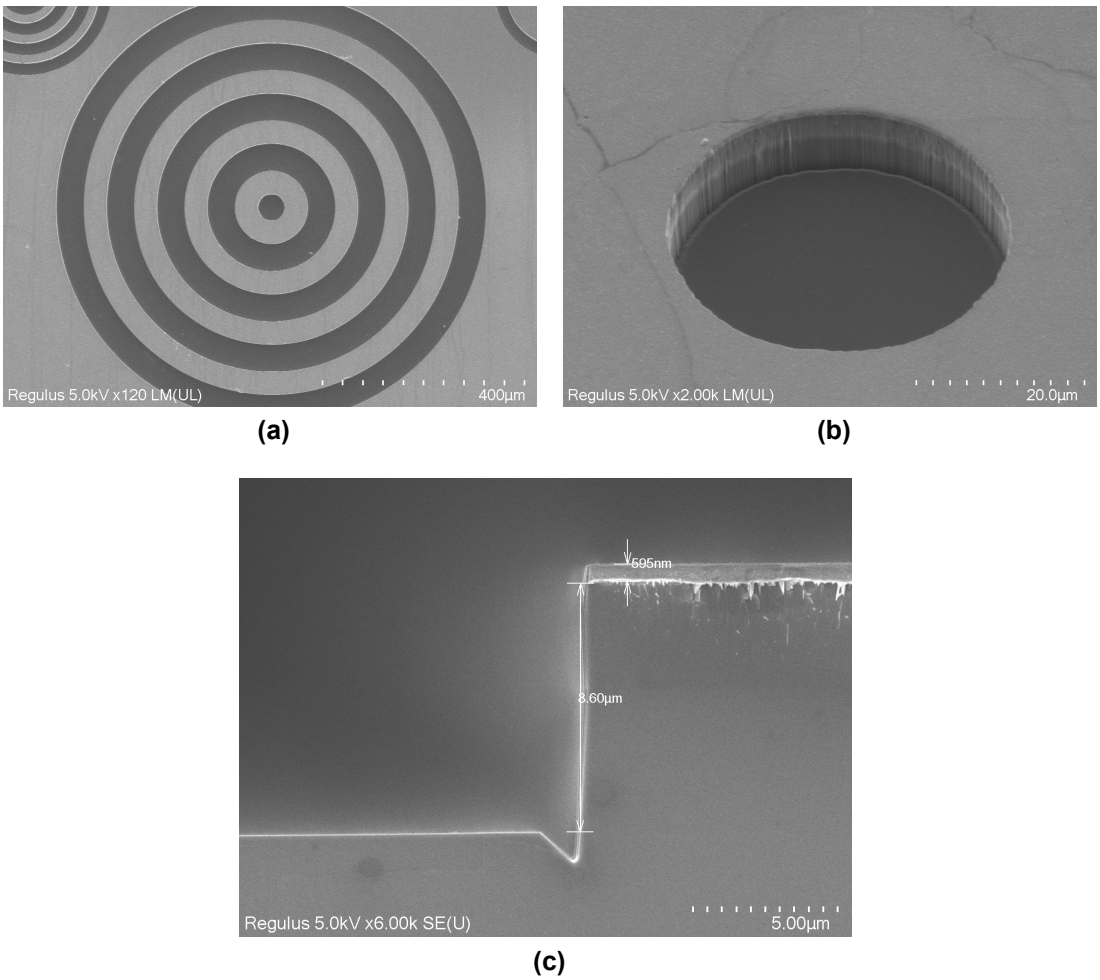


Figure 3.9: SEM images of the etched 4H-SiC sample on a P-type silicon carrier wafer:(a)Top view.(b)45 degree tilt.(c)Cross section

profile results were measured on the Dektak tool. The etch depth of the SiC sample using a SiO_2 coated n-type silicon carrier wafer is almost the same as that using a sapphire carrier wafer. A micro-masking-free surface was achieved. However, the SiO_2 layer on the carrier wafer was completely etched away after only one ICP RIE test, indicating that a SiO_2 coated silicon carrier wafer can not be used multiple times. Hence, the solution involving such a carrier wafer is not cost-effective.

3.5.4. Nickel coated silicon carrier wafer

To achieve an optimized ICP RIE process, a carrier wafer that does not induce micro-masking and does not consume too many radicals is needed. It should also be possible to be used multiple times to meet cost-effectiveness requirements. Nickel-coated n-type silicon wafer, in this case, seems to be a good candidate as the carrier.

The deposition of the nickel layer on the silicon wafers was done by sputtering in the Trikon Sigma 204 Dealer tool at 50 °C. The goal is to make silicon carrier

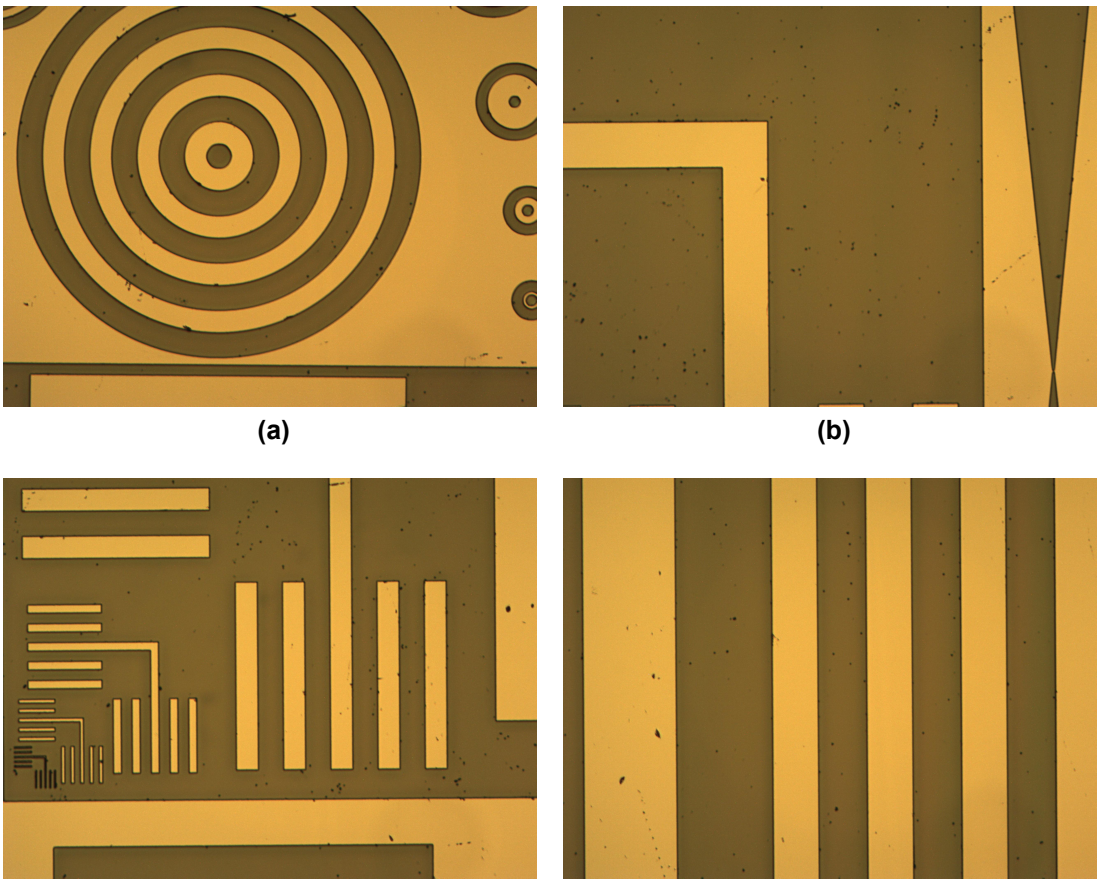


Figure 3.10: Microscope images of the etched 4H-SiC sample on a P-type silicon carrier wafer. Parameter settings in Table 3.5 apply.

wafers coated with a thick nickel layer so each carrier wafer can be used multiple times. However, a nickel layer of large thickness will induce bowing on the wafer due to a difference in thermal expansion coefficient between nickel and SiC, which will cause clamping and back-side cooling issues in the Adixen AMS110 tool. So, characterization of the deposited nickel layer is necessary.

First, a 3 μm thick nickel layer was deposited on the front side of 4 n-type silicon wafers. The measurement results of the bowing before and after deposition on the wafer are in Table 3.6. The bowing of these four wafers is more than 100 μm, which will induce thermal contact issues between the carrier and the substrate electrode. So these wafers are not suitable to be used.

The other batch of 4 wafers was deposited with 5 μm nickel layers on both sides to cancel the bowing. The measurement results of the bowing are in Table 3.7. Most of the bowing was canceled since both sides were deposited with nickel. A tape test was performed to check the adhesion status of the nickel layer. Finally, two wafers(201911-2-1379 and 201911-2-1248) were chosen as carrier wafers for the Design of experiments(DOE) in Chapter 4.

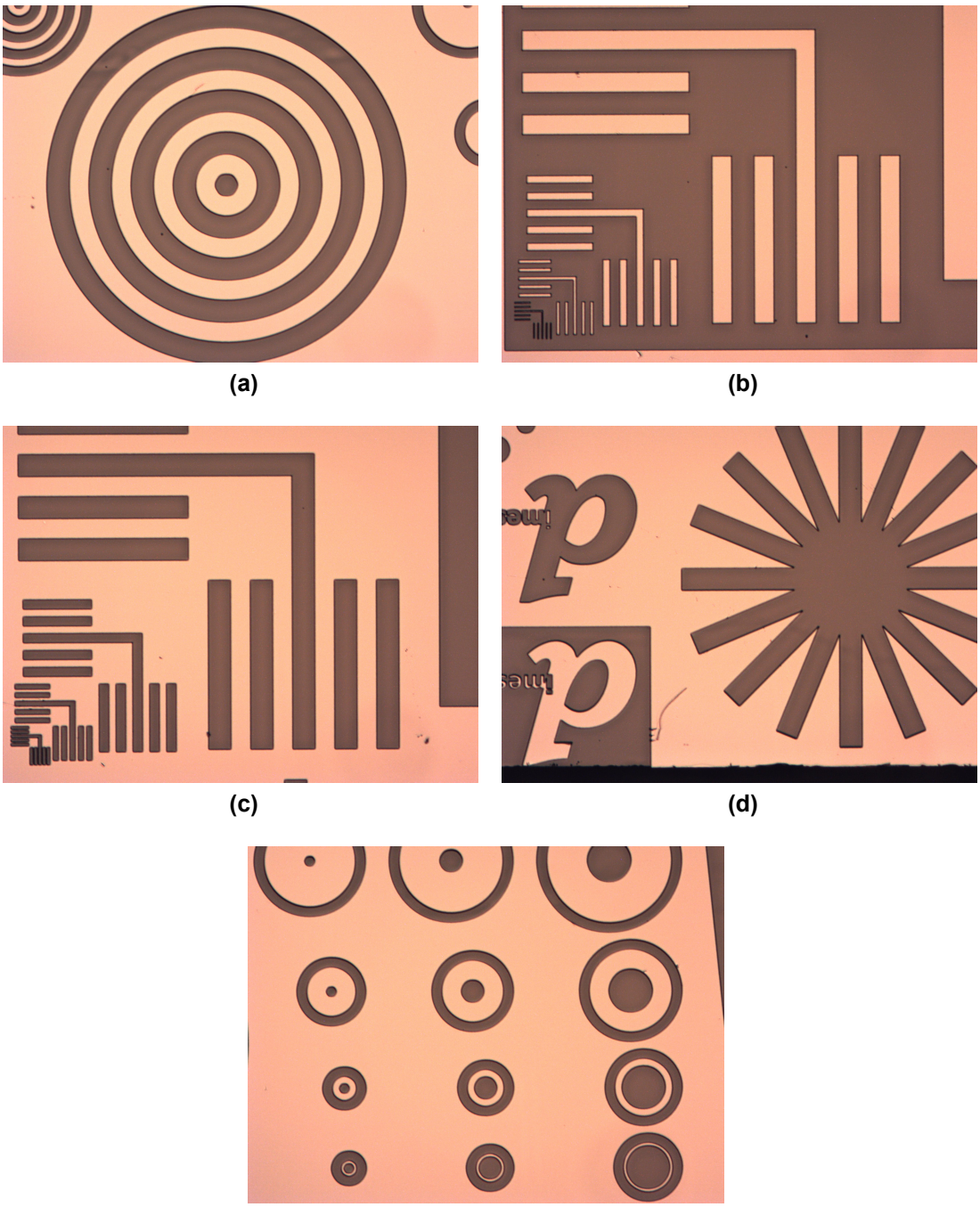


Figure 3.11: Microscope images of the etched 4H-SiC sample on an N-type silicon carrier wafer. Parameter settings in Table 3.5 apply.

3.6. Characterization and Analysis Methods

This work's primary characterization and analysis were done by taking the optical and scanning electron microscope(SEM) images. The optical microscope images presented the achieved etching surface, showing the micro masking level. The primary use of the cross-sections of the etched SiC samples presented in SEM

Table 3.6: Bowing and inner stress of carrier wafers coated with 3 μm nickel

Wafer number	Before deposition)	After deposition)	Stress
201911-2-1266	1.14 μm	137.76 μm	482.48 Mpa
201911-2-1274	0.94 μm	135.21 μm	473.31 Mpa
201911-2-0596	0.39 μm	129.59 μm	452.48 Mpa
201911-2-0614	0.45 μm	127.7 μm	443.76 Mpa

Table 3.7: Bowing of carrier wafers coated with 5 μm nickel

Wafer number	Before deposition	First deposition	Second deposition
201911-2-1388	0.7 μm	198.33 μm	-14.08 μm
201911-2-1379	1.46 μm	251.29 μm	36.45 μm
201911-2-1248	0.26 μm	212.41 μm	15.71 μm
201911-2-1103	0.88 μm	192.91 μm	20.13 Mpa

images was to derive the etch depth and the remaining thickness of the hard mask layer to calculate the etch rate and selectivity.

One cross-section was cleaved for each processed SiC sample, and two data points for etch depth and remaining hard mask thickness were taken for the cross-section, respectively. The measurement of the etch depth and remaining hard mask thickness was done on a Java-based image processing tool, ImageJ, where the calibration was done manually. Hence, a 2-3% deviation of measurement results from the actual values was expected. In addition, the etch uniformity of the SiC sample was characterized by the Keyence analysis tool, where the difference in etch depth was shown in different shades of colors.

The characterization and analysis methods described above were applied in Chapter 4 for the data acquired from the ICP RIE tests.

3.7. Conclusion

This chapter introduced the strategies of the Design of experiments(DOE), presented the initial results of the baseline ICP RIE process, and illustrated preliminary optimization performed on the process.

A baseline recipe was achieved with an etch rate of 1 μm/min, presented in Table 3.8. The results of conducted preliminary optimization with pre-cleaning and different carrier wafers are summed in Table 3.9. It can be seen that applying high bias power will significantly increase the etch rate, and silicon carrier wafers induce the least micro masking.

In addition, pre-cleaning with oxygen and argon plasma has been proven effective in suppressing the micro-masking effect. This indicates that pre-cleaning is always needed for each SiC ICP RIE test.

At last, Chapter 4 will conduct a comprehensive study based on the Design of Experiments, further investigating the role of ICP parameters and carrier wafer

Table 3.8: ICP RIE baseline settings for 4H-SiC

ICP source power	2500 W
Chuck bias power	300 W
Pressure	1.5 E-2 mbar
SF_6	100 sccm
O_2	25 sccm
Ar	100 sccm
Substrate temperature	20 °C
Etch time	10 minutes

Table 3.9: Summary of initial tests and preliminary optimizations for SiC ICP RIE

Carrier wafer material	Process settings	Micro masking level
Sapphire	no pre-cleaning	High
Sapphire	pre-cleaning with Argon plasma	Medium High
Sapphire	pre-cleaning with Oxygen plasma	Medium
P-type silicon	pre-cleaning with Oxygen and Argon plasma	Medium Low
N-type silicon	pre-cleaning with Oxygen and Argon plasma	Low
SiO_2 coated N-type silicon	pre-cleaning with Oxygen and Argon plasma	Low

materials on the etch rate and etch profile. The recipe presented in Table 3.8 was chosen as a baseline recipe. Parameters such as ICP source power, chuck bias power, pressure, and substrate temperature will vary independently to study the impact of each parameter on the etch rate and morphology.

This chapter has briefly explained the motivation for choosing a nickel-coated silicon carrier. The effect of carrier wafers coated with nickel layer on the etch rate and etch profile will be further investigated in the next chapter.

4

Process results for shallow SiC structures

This chapter will present the etching results of the DOE, introduced in Chapter 3. The results of 4H-SiC substrate shallow-etch using a nickel hard mask will be presented in terms of different carrier wafer materials, in which the role of various parameters on etch rate, the micro masking level, and selectivity will be reported and explained. In addition, the etching tests using a SiO_2 hard mask will be conducted as the secondary technical route, discussed in Chapter 3. These results will also be presented and explained.

4.1. SiC etching with Nickel hard mask

ICP RIE process development for the 4H-SiC substrate using a nickel hard mask is the primary technical route of this work because nickel is robust against ion bombardment, providing good selectivity, thus suitable for the deep etching process. This section will present the etch results using nickel as the mask material. According to the preliminary results from Chapter 3, the carrier wafer material profoundly affects the etch rate and micro masking level. This section discusses the role of two carrier wafer materials: silicon and nickel. All the ICP RIE tests using a nickel hard mask were conducted using the Adixen AMS110 tool, supported by Else Kooi Laboratory.

4.1.1. SiC etching using silicon carrier wafers

It has been discussed in Subsection 3.3.2 and Subsection 3.5.1 that the aluminum-containing carrier will induce severe micro maskings on the etched SiC surface. To avoid aluminum from the carrier, silicon was chosen as one option as a carrier material. The DOE tests were conducted by varying parameters such as pressure, chuck bias power, substrate temperature, and ICP source power based on the preliminarily optimized recipe in Table 3.8. The effect of these parameters on etch rate, selectivity, and micro masking level will be presented and discussed.

Role of pressure

The etch parameters are shown in Table 4.1. The pressure varies from 1.5E-2 mbar to 5.5E-2 mbar, while the other parameters are the same as those in

Table 3.8.

Table 4.1: ICP RIE settings for 4H-SiC: varying pressure. Silicon carriers were used.

ICP source power	2500 W
Chuck bias power	300 W
Pressure	1.5 E-2 - 5.5 E-2 mbar
SF_6	100 sccm
O_2	25 sccm
Ar	100 sccm
Substrate temperature	20 °C
Etch time	10 minutes

The etch rate and selectivity results as a function of pressure are shown in Fig. 4.1a and Fig. 4.1b, respectively.

It can be seen that the etch rate decreases as the pressure increases, while selectivity is approximately the other way around. As discussed in Subsection 2.3.4, two competing mechanisms regarding the role of pressure affect the etch rate. One is that high pressure helps generate more radicals to react with the SiC substrate, thus increasing the etch rate. The other one is that the reduced mean free path and a higher chance of random collision between radicals due to higher pressure will undermine the effectiveness of ion bombardment, slowing down the bond-breaking process of the SiC surface and leading to a lower etch rate. According to the results in Fig. 4.1a, the latter dominates in the ICP RIE process, so a decrease in etch rate with higher pressure was observed. As for the selectivity, it follows an increasing trend with pressure. This is because of the less ion bombardment on the mask material.

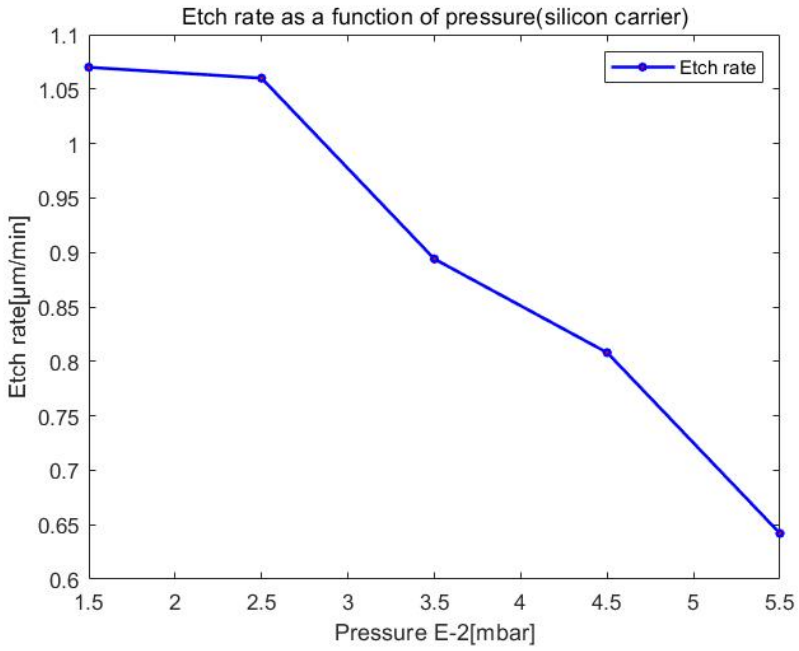
In addition, a micro-masking-free surface was achieved at both the minimum value and maximum value of the pressure, shown in Fig. 4.2a and Fig. 4.2b.

Role of chuck bias power

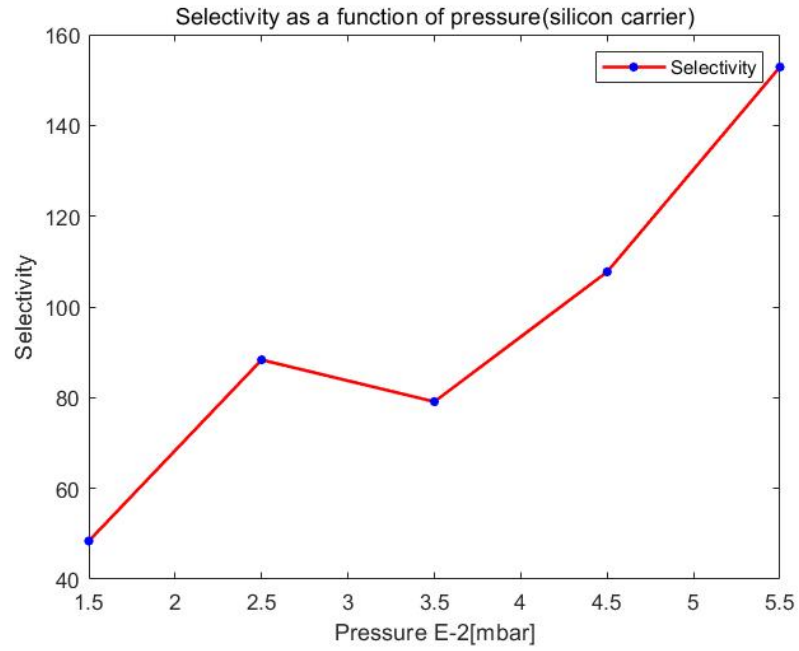
The parameter setting is shown in Table 4.2. Five values of chuck bias power were chosen for tests:100W, 150W, 200W, 250W, and 300W. The other parameters are the same as those in Table 3.8.

The etch rate and selectivity results as a function of chuck bias power are shown in Fig. 4.3a and Fig. 4.3b, respectively.

As seen from Fig. 4.3, the etch rate increases almost linearly with chuck bias power. The higher the chuck bias power, the stronger the ion bombardment on the SiC sample, leading to faster bond-breaking between silicon and carbon atoms. More ”free” atoms are available to react with radicals, so the etch rate increases. However, the intense ion bombardment occurs not only on the SiC surface to be etched but also on the hard mask layer that was removed aggressively by sputtering the radicals. In consequence, the selectivity decreases with chuck



(a)

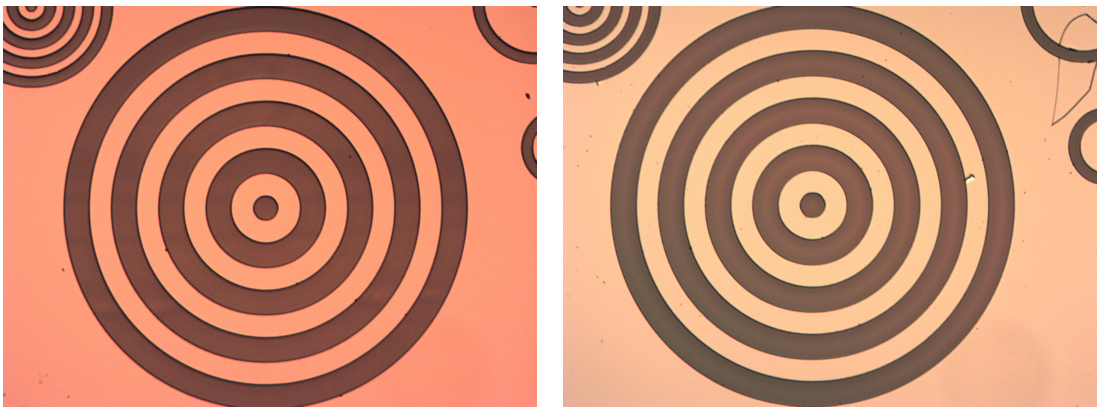


(b)

Figure 4.1: Role of pressure:(a)Etch rate as a function of pressure. (b)Selectivity as a function of pressure. Silicon carriers were used.

bias power. According to Fig. 4.3b, the selectivity of the nickel mask was more than 140 at 100W bias power, while at 300W bias power was slightly higher than 40.

The micro masking level of the etched surface is shown in Fig. 4.4. Both



(a) (b)

Figure 4.2: Microscope figures at pressure:(a)1.5 E-2 mbar(minimum setting).(b)5.5 E-2 mbar(maximum setting).

Table 4.2: ICP RIE settings for 4H-SiC: varying chuck bias power. Silicon carriers were used.

ICP source power	2500 W
Chuck bias power	100,150,200,250,300 W
Pressure	1.5 E-2 mbar
SF_6	100 sccm
O_2	25 sccm
Ar	100 sccm
Substrate temperature	20 °C
Etch time	10 minutes

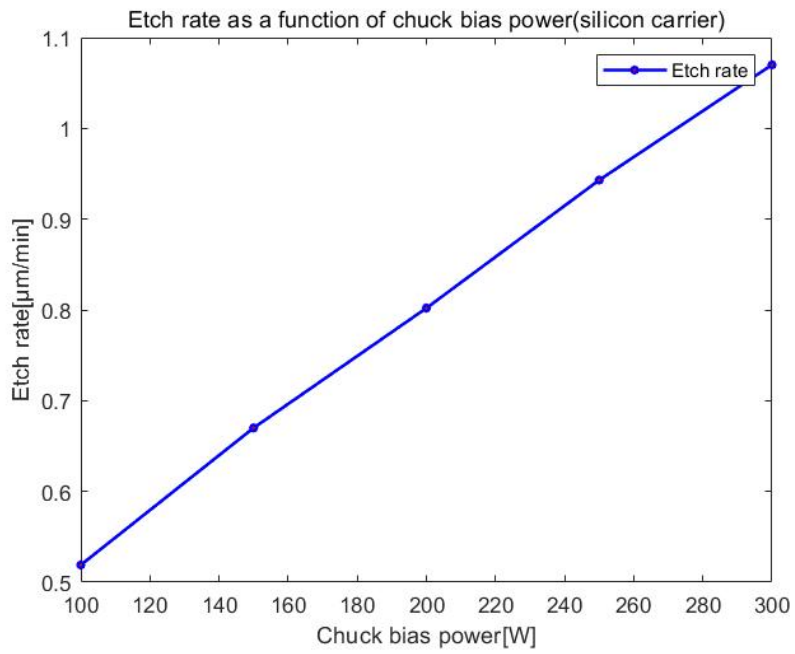
Fig. 4.4a and Fig. 4.4b show a micro-masking-free surface. This indicates that nickel is robust against ion bombardment even at high chuck bias power.

Role of substrate temperature

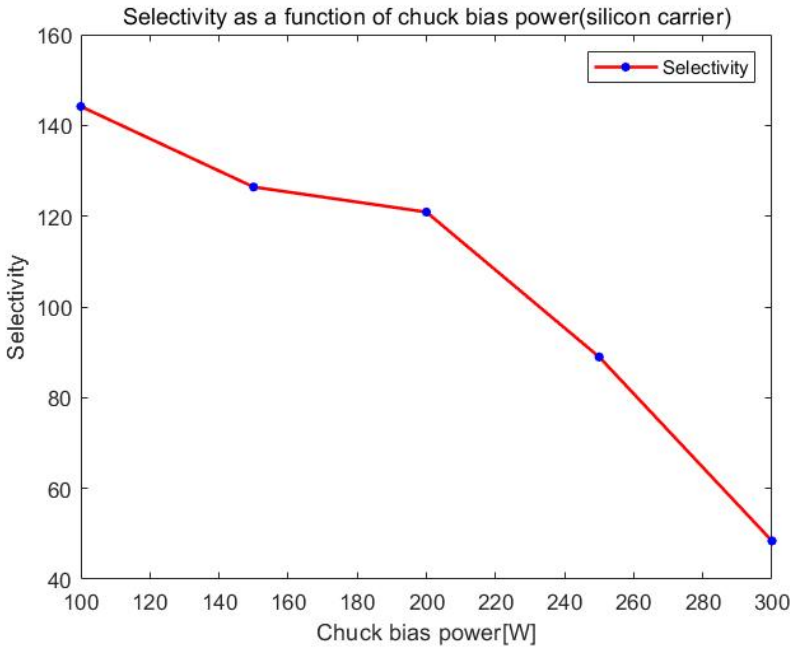
The parameter setting is shown in Table 4.3. The substrate temperatures were set to 10°C, 20°C, and 40°C. The other parameters are the same as those in Table 3.8.

The etch rate and selectivity results as a function of substrate temperature are shown in Fig. 4.5a and Fig. 4.5b, respectively.

The results in Fig. 4.5 indicate that the etch rate increases with substrate temperature from 10 °C to 20 °C, then decreases with substrate temperature from 20 °C to 40 °C. In contrast, the selectivity decreases from 10 °C to 20 °C, then increases from 20 °C to 40 °C. However, the etch rate and selectivity values do not show a considerable dependence on substrate temperature. The values of the etch rate vary in a range from 1.01 μm/min to 1.07 μm/min, while that of selectivity is larger than 48 but less than 54. Both ranges are small compared to the previous results of the other parameters. It is possible that the trends shown in



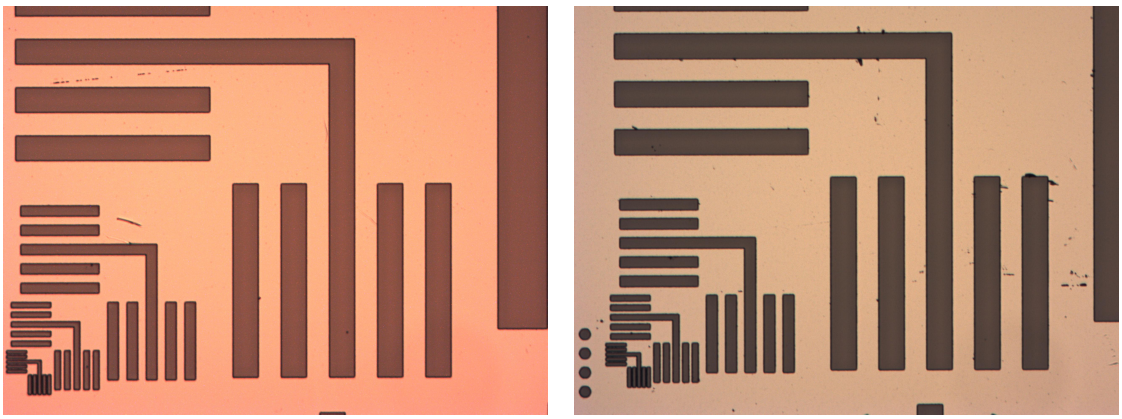
(a)



(b)

Figure 4.3: Role of chuck bias power:(a)Etch rate as a function of chuck bias power. (b)Selectivity as a function of chuck bias power. Silicon carriers were used.

Fig. 4.5a and Fig. 4.5b were caused by the measurement variations because the measurement calibration was done manually, as mentioned in Section 3.6. Due to the limitation of authorization in modifying substrate temperature in the Adixen AMS110 tool and the limitation of the tool's capability, tests were conducted at



(a) (b)

Figure 4.4: Microscope figures at chuck bias power:(a)100 W(minimum setting).(b)300 W(maximum setting).

Table 4.3: ICP RIE settings for 4H-SiC: varying substrate temperature. Silicon carriers were used.

ICP source power	2500 W
Chuck bias power	300 W
Pressure	1.5 E-2 mbar
SF_6	100 sccm
O_2	25 sccm
Ar	100 sccm
Substrate temperature	10,20,40 °C
Etch time	10 minutes

a small range of substrate temperatures. In principle, the higher the substrate temperature, the higher the etch rate. Nevertheless, this was observed at a wider range of temperatures[18].

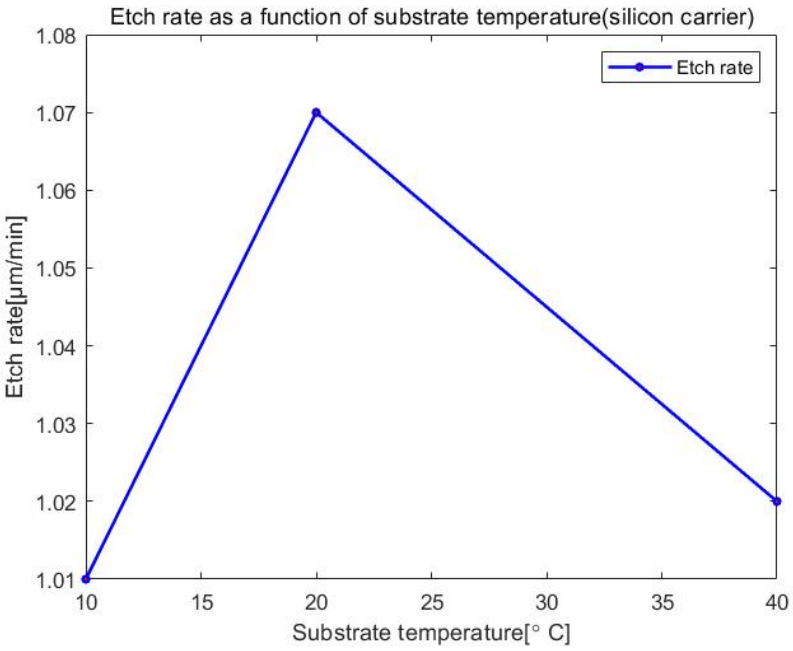
The SiC surfaces etched at 10°C, 20°C and 40°C are all micro-masking free, shown in Fig. 4.6.

Role of ICP source power

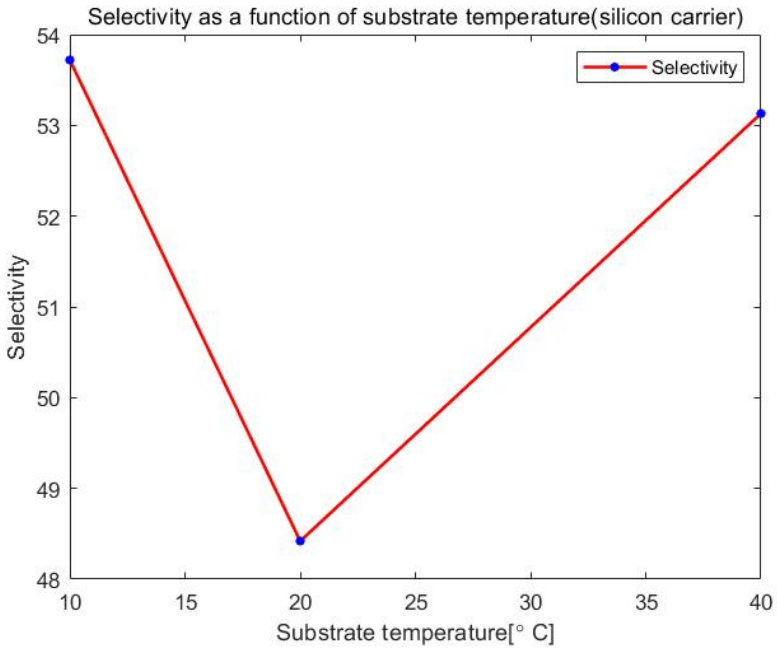
The parameter setting is shown in Table 4.4. The ICP source power was set to 2000W and 2500W. The other parameters are the same as those in Table 3.8.

The etch rate and selectivity results as a function of substrate temperature are shown in Fig. 4.7a and Fig. 4.7b, respectively.

It is indicated in Fig. 4.7a that the etch rate increases with ICP source power. This is relatively straightforward because higher ICP source power will generate more radicals to react with the SiC substrate, thus increasing the etch rate. Since the tests were conducted at high chuck bias power, the value of which is 300W, more radicals also mean more ion bombardment on the hard mask material.



(a)



(b)

Figure 4.5: Role of substrate temperature:(a)Etch rate as a function of substrate temperature. (b)Selectivity as a function of substrate temperature. Silicon carriers were used.

Hence, the selectivity decreases with ICP source power.

As for the micro masking level, Fig. 4.8a and Fig. 4.8b show micro-masking-free SiC surfaces achieved at 2000W and 2500W ICP source power, respectively.

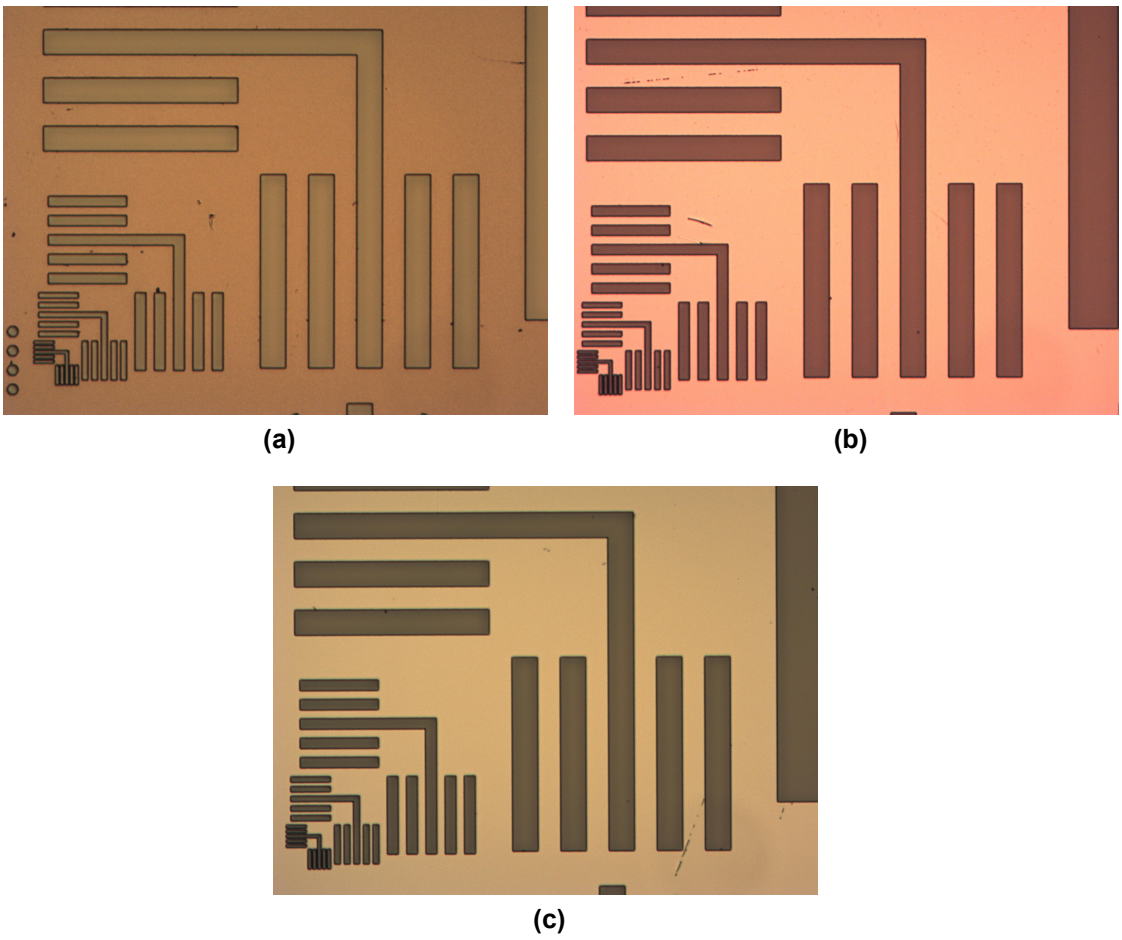


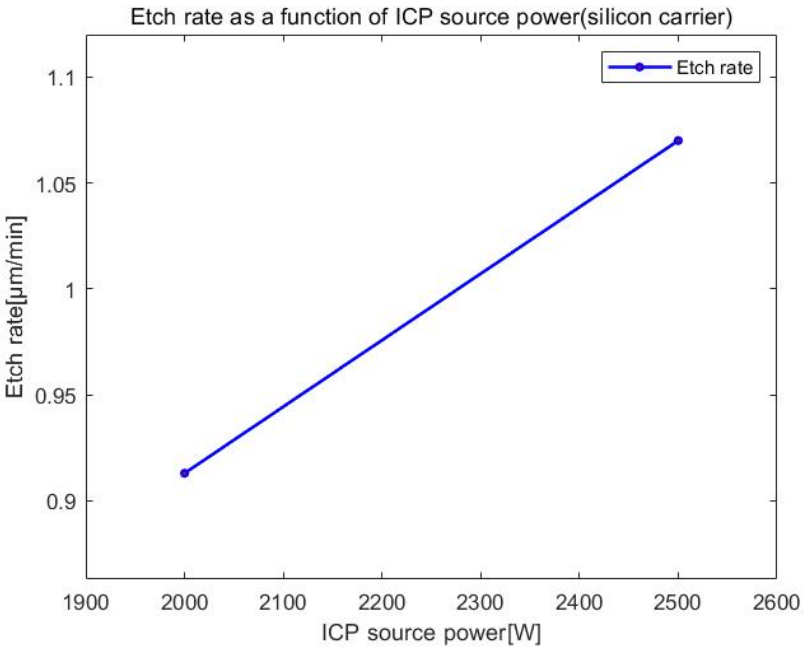
Figure 4.6: Microscope figures at substrate temperature:(a)10 °C(minimum setting).(b)20 °C.(c)40 °C(maximum setting)

Table 4.4: ICP RIE settings for 4H-SiC: varying ICP source power. Silicon carriers were used.

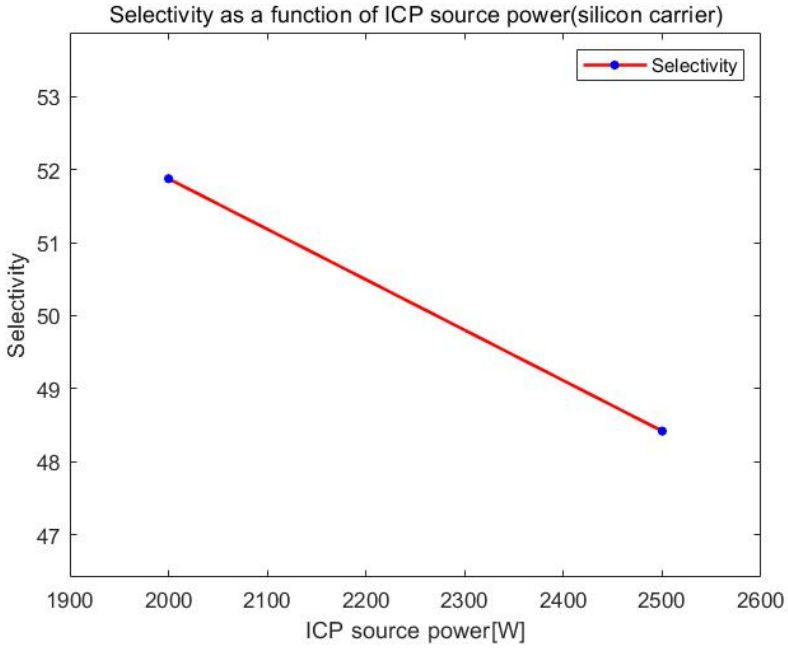
ICP source power	2000,2500 W
Chuck bias power	300 W
Pressure	1.5 E-2 mbar
SF_6	100 sccm
O_2	25 sccm
Ar	100 sccm
Substrate temperature	20 °C
Etch time	10 minutes

4.1.2. SiC etching using nickel-coated silicon carrier wafers

It was discussed in Subsection 3.5.4 that the nickel-coated silicon wafer might be a good candidate as a carrier because the EDS analysis results in Subsection 3.3.2 showed that nickel was not the cause of micro masking. It is robust against ion



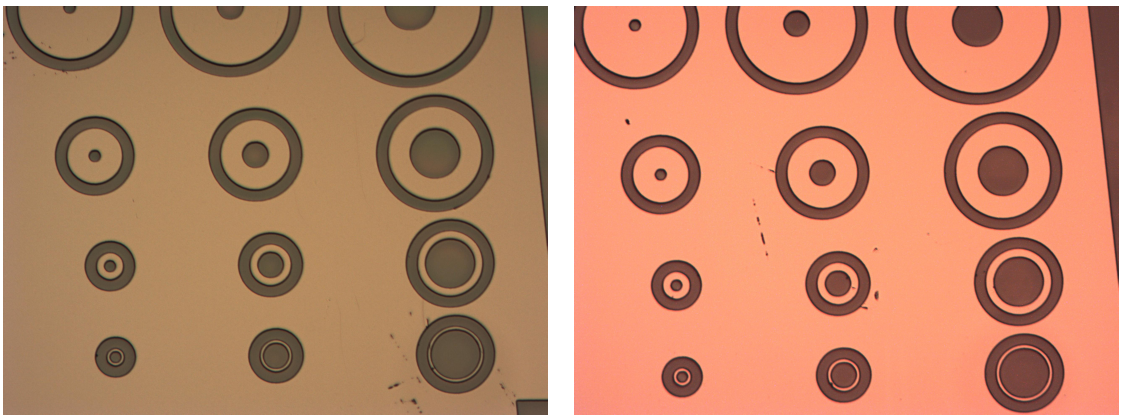
(a)



(b)

Figure 4.7: Role of ICP source power:(a)Etch rate as a function of ICP source power. (b)Selectivity as a function of ICP source power. Silicon carriers were used.

bombardment and thus can be used multiple times to meet the cost-effective requirement. Hence, ICP RIE tests with nickel-coated silicon carrier wafers were conducted. Pressure, chuck bias power, substrate temperature, and ICP source power were varied to study the impact of these parameters on the etch rate,



(a) (b)

Figure 4.8: Microscope figures at ICP source power:(a)2000W(minimum setting).(b)2500W(maximum setting)

selectivity, and micro masking level.

Role of pressure

The parameter setting is shown in Table 4.5. The pressure was set to 1.5E-2, 2.5E-2, 3.5E-2, 4.5E-2 and 5.5E-2 mbar. The other parameters are the same as those in Table 3.8.

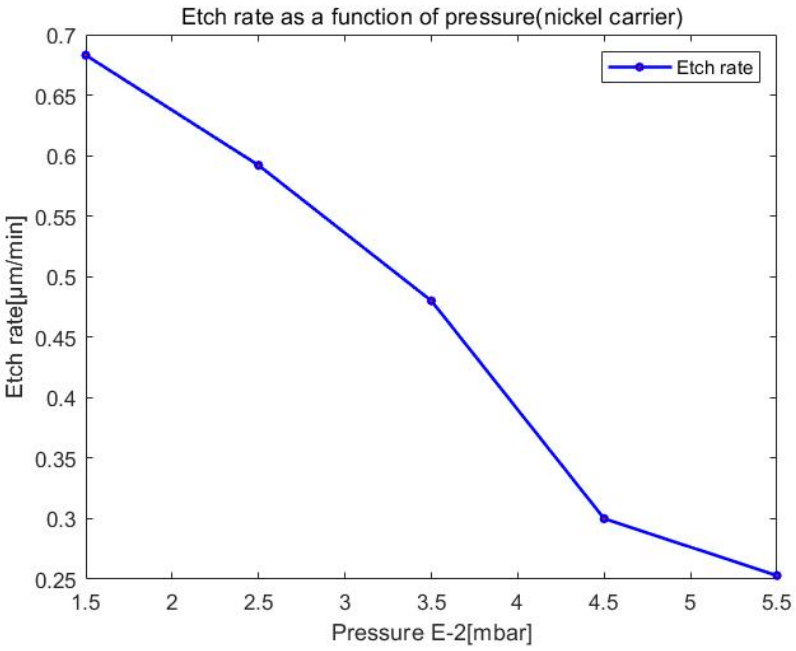
Table 4.5: ICP RIE settings for 4H-SiC: varying pressure. Nickel-coated silicon carriers were used.

ICP source power	2500 W
Chuck bias power	300 W
Pressure	1.5 E-2 - 5.5 E-2 mbar
SF_6	100 sccm
O_2	25 sccm
Ar	100 sccm
Substrate temperature	20 °C
Etch time	10 minutes

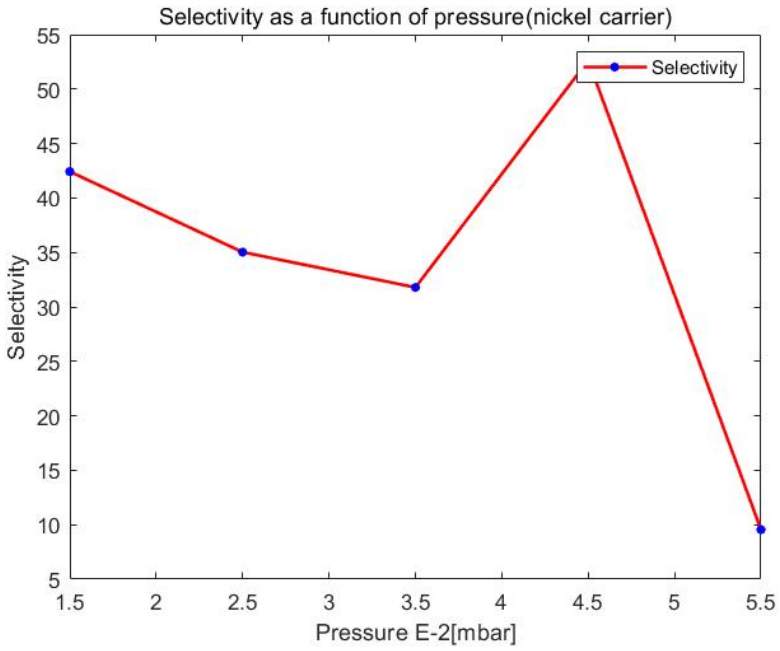
The etch rate and selectivity results as a function of substrate temperature are shown in Fig. 4.9a and Fig. 4.9b, respectively.

It can be seen that the etch rate decreases with pressure, which is similar to the results using silicon carriers, except that the etch rate values are lower than when silicon carriers were used. As for the selectivity, it did not increase with pressure except from 3.5E-2 mbar to 4.5E-2 mbar.

Interestingly, severe micro maskings were found on the SiC surface processed at pressure 4.5E-2 mbar and 5.5E-2 mbar, shown in Fig. 4.10a and Fig. 4.10b, while the etched surface in Fig. 4.10c is micro-masking-free. Fig. 4.11a and



(a)



(b)

Figure 4.9: Role of pressure:(a)Etch rate as a function of pressure. (b)Selectivity as a function of pressure. Nickel-coated silicon carriers were used.

Fig. 4.11b are SEM images of the cross sections processed at 4.5E-2 mbar and 5.5E-2 mbar, indicating a very shallow trench etched after 10 minutes. It should be pointed out that the etch depth under severe micro maskings was determined by measuring the vertical distance from the bottom of the trench to the original surface. The measured depth suggests that the micro masking

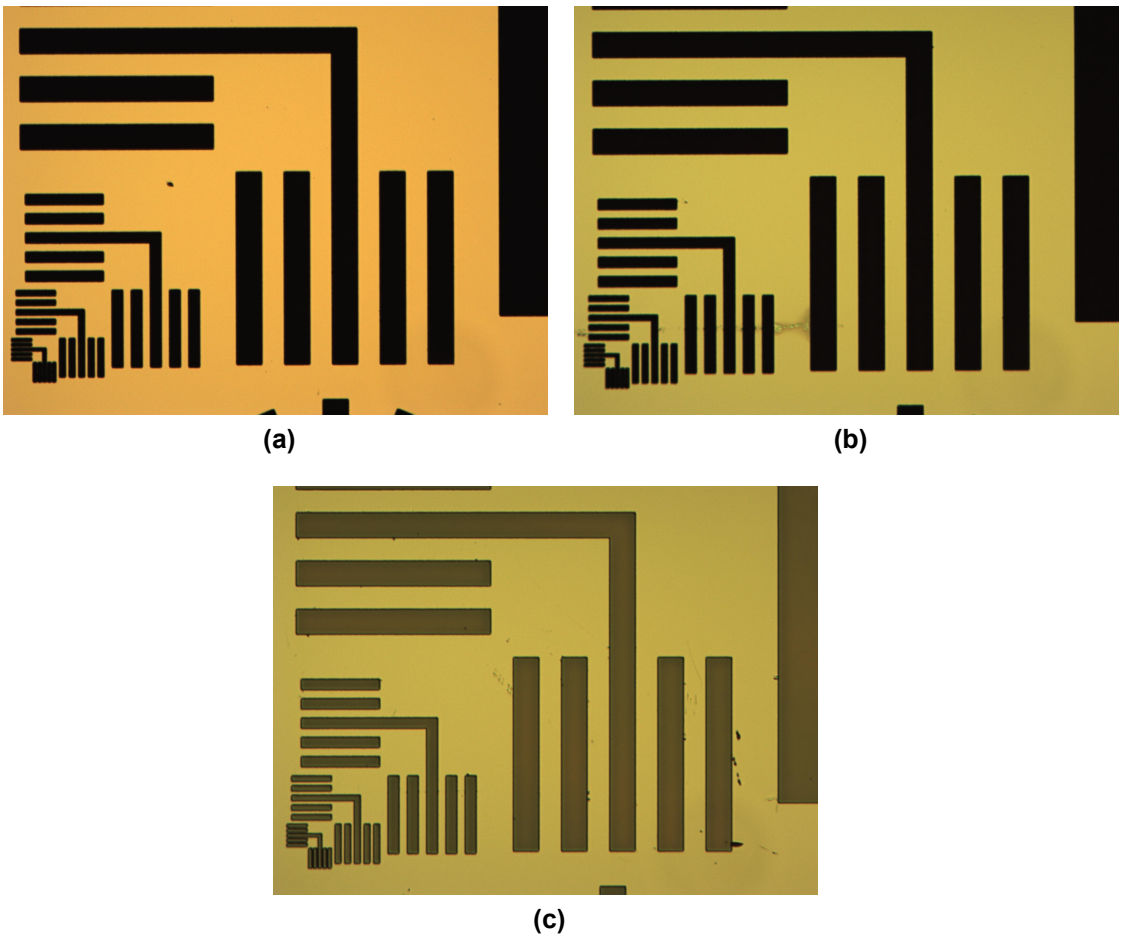
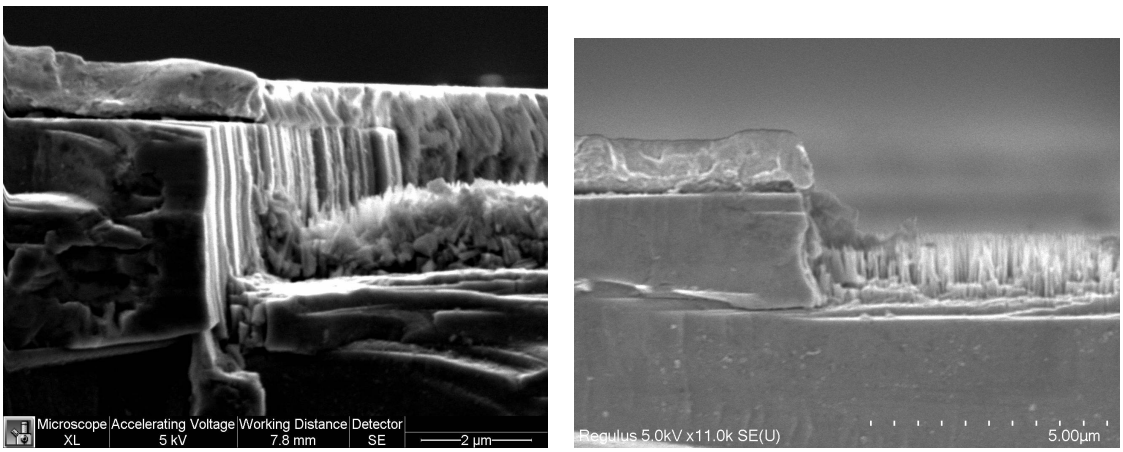


Figure 4.10: Microscope figures at pressure:(a)4.5E-2 mbar.(b)5.5E-2 mbar.(c)1.5E-2 mbar. Nickel-coated silicon carriers were used.

effect leads to a bad surface and a much lower etch rate, which reduces the selectivity, disregarding the less ion bombardment on the hard mask due to high pressure. As for the increase of selectivity from 3.5E-2 mbar to 4.5E-2 mbar, the value 4.5E-2 mbar might be the threshold point where the effect of high pressure in weakening ion bombardment, thus increasing selectivity, still dominates, but beyond which the impact of micro masking in reducing etch rate and thus selectivity, begin to play a more dominant role.

It is possible that the micro maskings were formed due to the random collisions between sputtered hard mask particles at high pressure. Fig. 4.12 is the EDS analysis result of the micro maskings on the etched surface, indicating that aluminum and nickel were both involved in the formation of micro masking. Interestingly, the SiC sample processed with the same setting but with a silicon carrier wafer(Subsection 4.1.1) did not form micro maskings on the etched surface, suggesting that large areas of exposed nickel will induce micro maskings on the SiC surface at high pressure.



(a) (b)

Figure 4.11: SEM figures of cross sections at pressure:(a)4.5E-2 mbar.(b)5.5E-2 mbar. Nickel-coated silicon carriers were used.

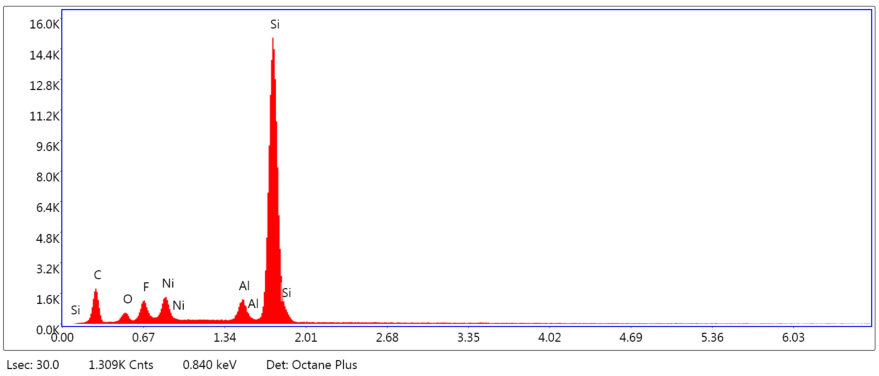


Figure 4.12: EDS analysis of SiC sample processed at pressure 5.5E-2 mbar. Nickel-coated silicon carriers were used.

Role of chuck bias power

The parameter setting is shown in Table 4.6. Five values of chuck bias power were chosen for tests:100W, 150W, 200W, 250W, and 300W. The other parameters are the same as those in Table 3.8.

Fig. 4.13a and Fig. 4.13b show the etch rate and selectivity results as a function of chuck bias power, respectively. It can be seen that the etch rate increases with chuck bias power, but the values are lower than that when silicon carriers are used. The selectivity does not decrease with chuck bias power except for the value from 200W to 250W.

More interestingly, micro maskings were found at 100W chuck bias power, while the SiC surface processed at high chuck bias power, such as 300W, is micro-masking-free, as shown in Fig. 4.14a and Fig. 4.14b, respectively. Fig. 4.15 presents the SEM image of cross-sections of the SiC sample processed at 100W chuck bias power and the EDS analysis results on the micro maskings. Again, it can be seen that both aluminum and nickel were involved when forming the micro maskings.

Table 4.6: ICP RIE settings for 4H-SiC: varying chuck bias power. Nickel-coated silicon carriers were used.

ICP source power	2500 W
Chuck bias power	100,150,200,250,300 W
Pressure	1.5 E-2 mbar
SF_6	100 sccm
O_2	25 sccm
Ar	100 sccm
Substrate temperature	20 °C
Etch time	10 minutes

Role of substrate temperature

The parameter setting is shown in Table 4.7. The substrate temperatures were set to 10°C, 20°C, and 40°C. The other parameters are the same as those in Table 3.8.

Table 4.7: ICP RIE settings for 4H-SiC: varying substrate temperature. Nickel-coated silicon carriers were used.

ICP source power	2500 W
Chuck bias power	300 W
Pressure	1.5 E-2 mbar
SF_6	100 sccm
O_2	25 sccm
Ar	100 sccm
Substrate temperature	10,20,40 °C
Etch time	10 minutes

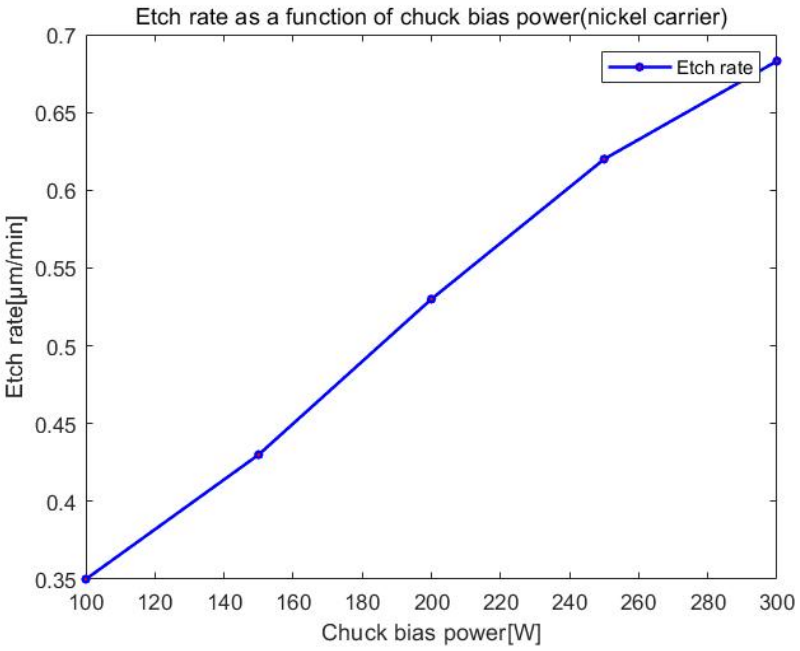
The etch rate and selectivity results as a function of substrate temperature are shown in Fig. 4.16a and Fig. 4.16b, respectively.

Both the etch rate and selectivity increase with substrate temperature from 10°C to 20°C and then decrease from 20°C to 40°C. Fig. 4.17 are the SEM images of the cross sections of samples processed at 10°C, 20°C and 40°C. Micro-masking-free surfaces were achieved according to these images.

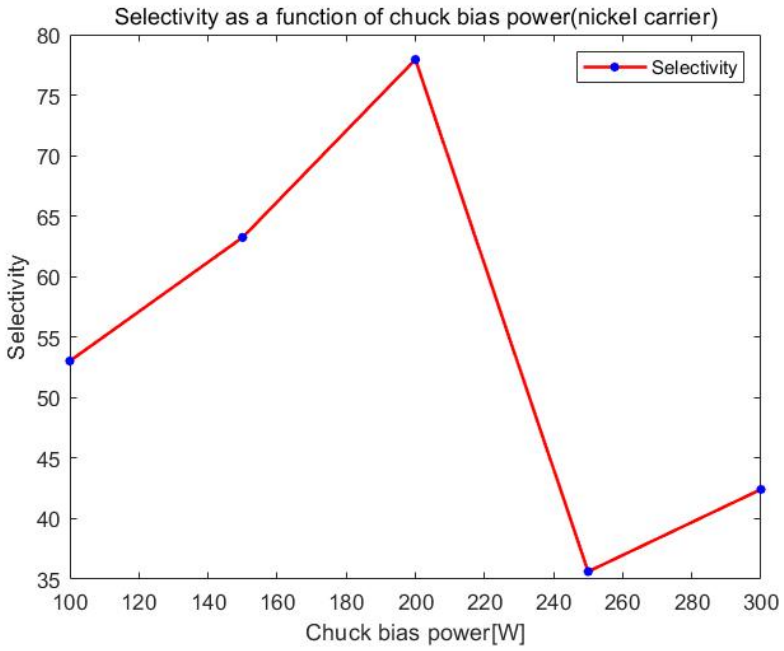
Role of ICP source power

The parameter setting is shown in Table 4.8. The ICP source power was set to 2000W, 2500W and 2800W. The other parameters are the same as those in Table 3.8.

The etch rate and selectivity results as a function of substrate temperature are shown in Fig. 4.18a and Fig. 4.18b, respectively.



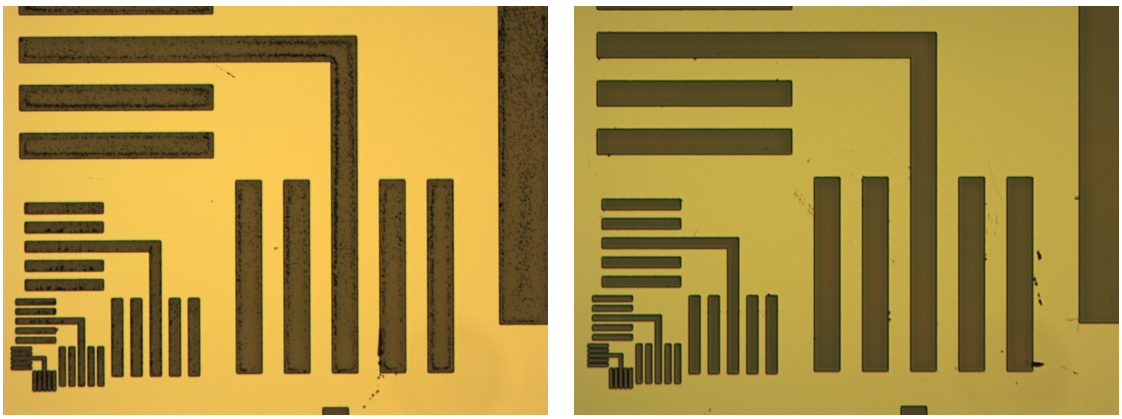
(a)



(b)

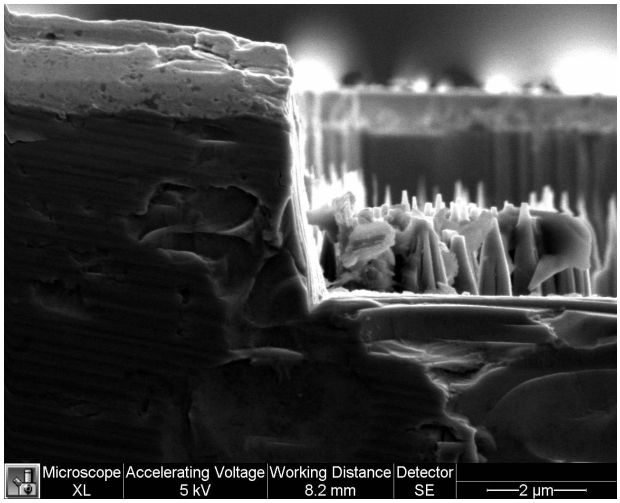
Figure 4.13: Role of chuck bias power:(a)Etch rate as a function of chuck bias power. (b)Selectivity as a function of chuck bias power. Nickel-coated silicon carriers were used.

It can be seen from Fig. 4.18a that the etch rate increases faster with ICP source power between 2000W and 2500W. When the ICP source power exceeds 2500W, the dependence of the etch rate on the ICP source power is reduced, suggesting the existence of a threshold value, above which the etch rate approxi-

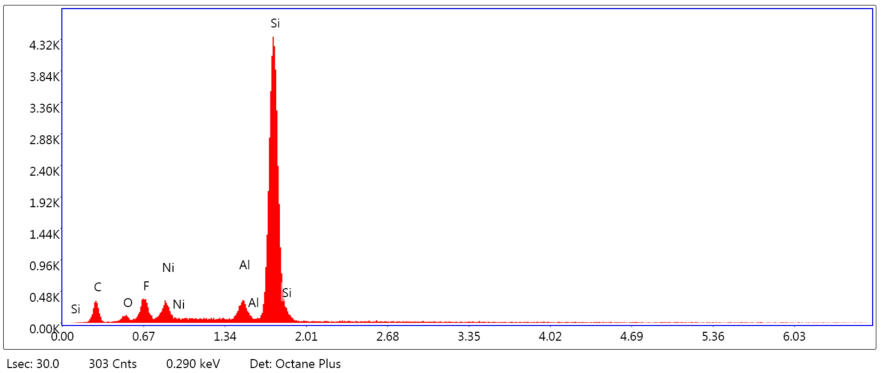


(a) (b)

Figure 4.14: Microscope figures at chuck bias power:(a)100W.(b)300W. Nickel-coated silicon carriers were used.

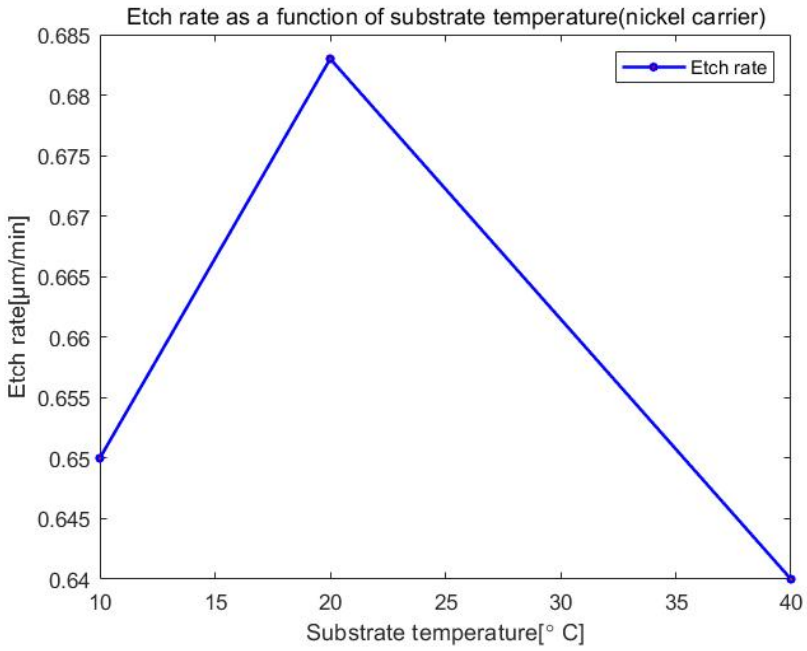


(a)

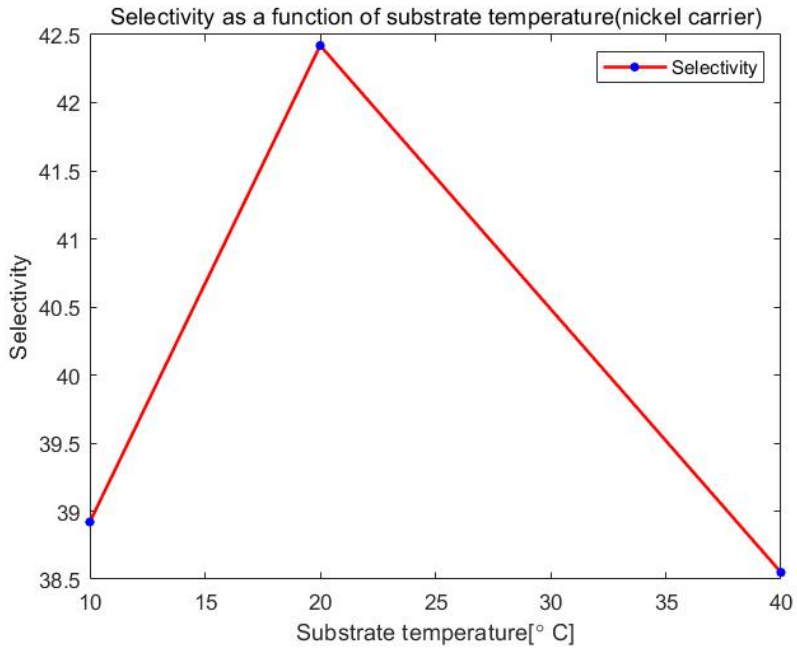


(b)

Figure 4.15: SEM figure of the cross-section and EDS analysis for SiC samples processed at 100W chuck bias power:(a)SEM image.(b)EDS analysis. Nickel-coated silicon carriers were used.



(a)



(b)

Figure 4.16: Role of substrate temperature:(a)Etch rate as a function of substrate temperature. (b)Selectivity as a function of substrate temperature. Nickel-coated carriers were used.

mately remains constant with the increase of ICP source power. The selectivity increases with ICP source power from 2000W to 2500W, then slightly decreases with ICP source power when it exceeds 2500W. The possible explanation is that from 2000W to 2500W, the etch rate increases significantly with ICP source

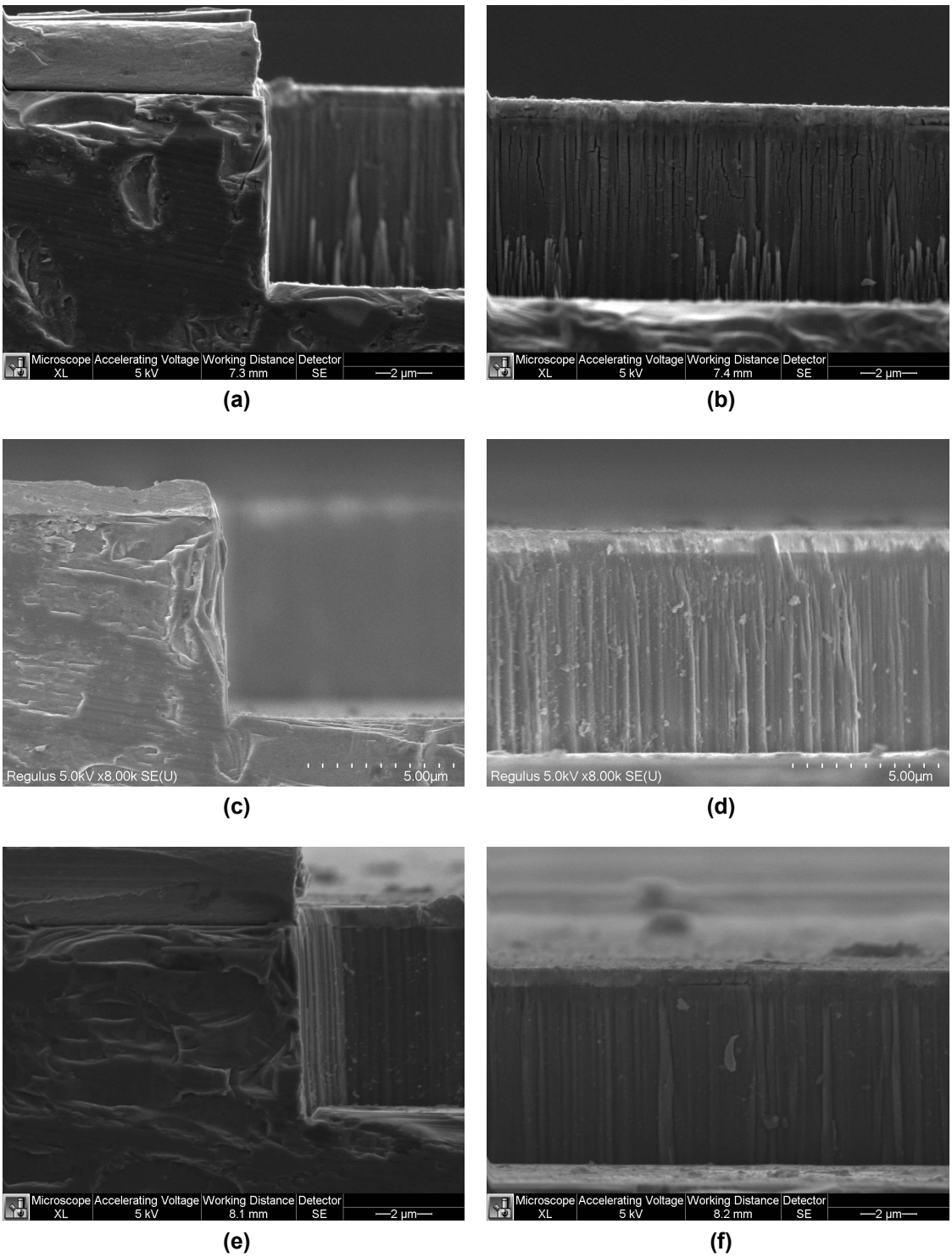


Figure 4.17: SEM figures of the cross-section.(a) and (b):10 °C. (c) and (d):20 °C. (e) and (f):40 °C. Nickel-coated carriers were used.

power, which outweighs the effect of increasing ion bombardment on the hard mask layer, increasing selectivity. However, when the ICP source power exceeds 2500W, the etch rate begins to saturate, so the effectiveness of ion bombardment

Table 4.8: ICP RIE settings for 4H-SiC: varying ICP source power. Nickel-coated silicon carriers were used.

ICP source power	2000,2500,2800 W
Chuck bias power	300 W
Pressure	1.5 E-2 mbar
SF_6	100 sccm
O_2	25 sccm
Ar	100 sccm
Substrate temperature	20 °C
Etch time	10 minutes

on the hard mask layer starts to dominate. This results in a decrease in selectivity. Hence, a threshold value exists for the best selectivity.

Both the samples processed with 2000W and 2800W ICP source power achieved a micro-masking-free surface, shown in Fig. 4.19a and Fig. 4.19b, respectively.

4.1.3. Discussion 1: Comparison between silicon carriers and nickel-coated silicon carriers

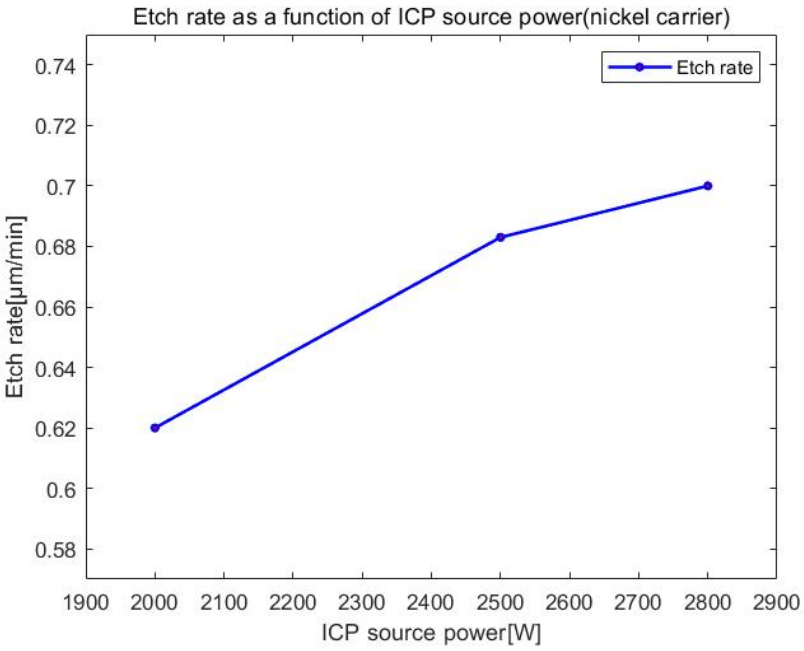
The previous sections presented the DOE results of SiC samples with a nickel hard mask but with two different kinds of carriers. It can be seen that the only advantage of using nickel-coated silicon carriers is cost-effectiveness since the nickel-coated silicon carriers are more robust against ion bombardment during etching and thus can be used multiple times. However, the SiC samples processed using silicon carriers show much better etch rate and micro masking suppression than those using nickel-coated silicon carriers. The comparisons were concluded in Table 4.9.

Table 4.9: Comparisons between silicon carriers and nickel-coated silicon carriers

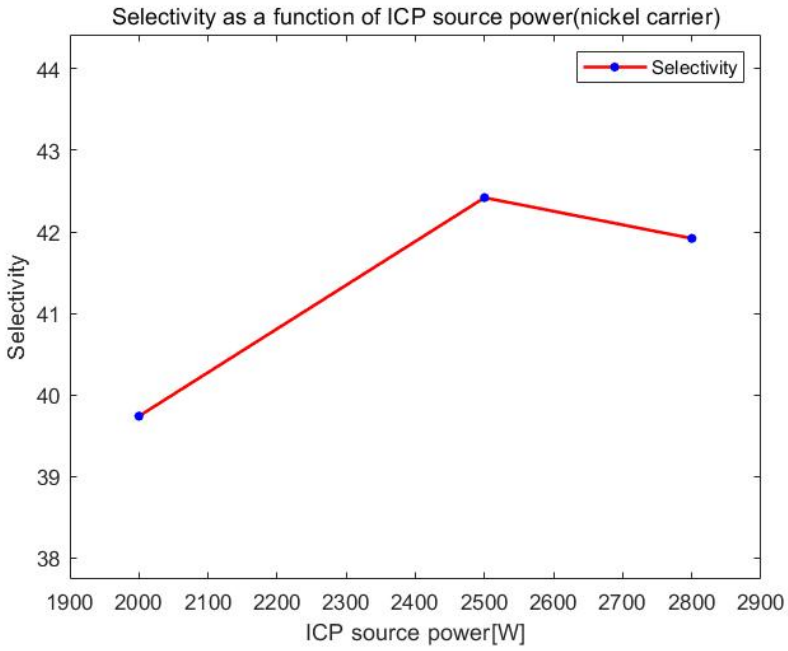
Carriers	Advantages	Disadvantages
Silicon carriers	Improved etch rate Micro-masking free surface	Limited usage times
Nickel-coated silicon carriers	Improved usage times	Limited etch rate Severe micro masking at high pressure

4.1.4. Discussion 2: Edge effects and Micro masking formation

The DOE results based on the use of silicon carriers and nickel-coated silicon carriers have been presented in the previous sections(Subsection 4.1.1 and



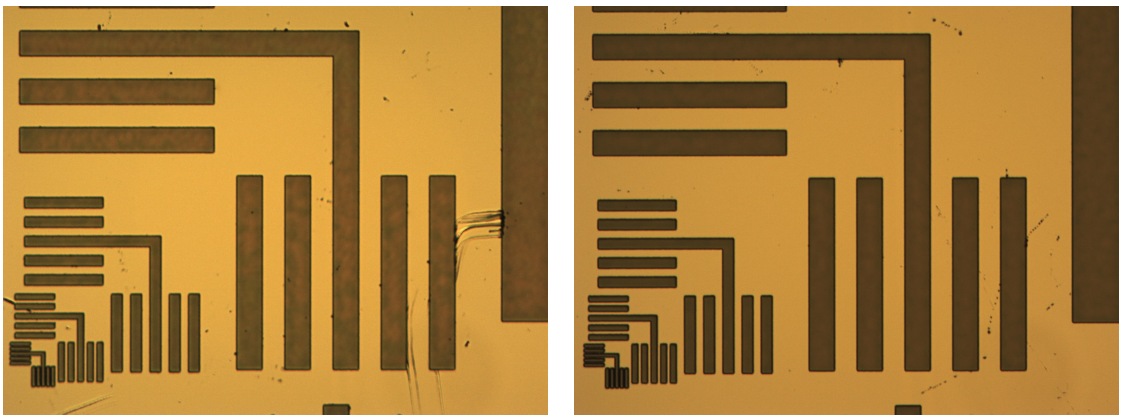
(a)



(b)

Figure 4.18: Role of ICP source power:(a)Etch rate as a function of ICP source power. (b)Selectivity as a function of ICP source power. Nickel-coated silicon carriers were used.

Subsection 4.1.2). Despite those mentioned in these sections, two interesting phenomena occurred during the tests. One is the edge effect. The other is the possible explanation of the micro maskings that appeared in Subsection 4.1.2.



(a) (b)

Figure 4.19: Microscope figures at ICP source power:(a)2000W.(b)2800W. Nickel-coated silicon carriers were used.

Edge effect

An etching non-uniformity was observed on the 6 mm x 6 mm 4H-SiC sample, where the closer it is to the center of the die where a large area of SiC is exposed to the plasma, the lower the etch rate. This is indicated in Fig. 4.20. It can be seen that the color at the edge area is much darker than that at the center, showing a faster etch rate at edge areas. This is because of the loading effect, in which the plasma was consumed more at the center; thus, the radical supply is not as sufficient as that at the edge, where the exposed SiC areas are much smaller. This finally leads to an etch rate non-uniformity on the sample.

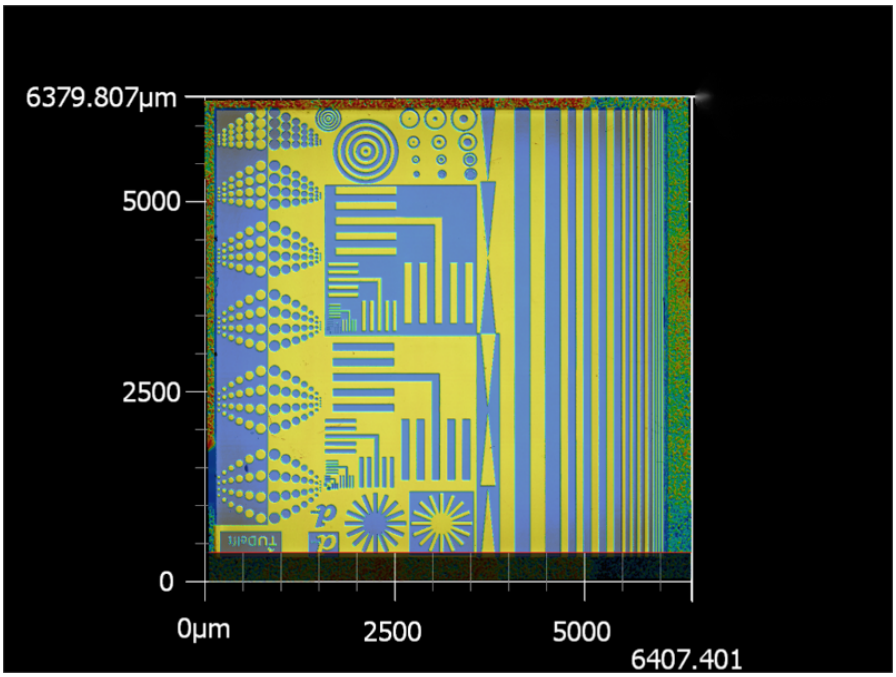


Figure 4.20: Keyence image of the SiC sample processed with the setting in Table 3.8

Micro masking formation
As presented in Subsection 4.1.2, both aluminum and nickel were involved in the formation of micro maskings. According to the EDS analysis from Fig. 4.12 and Fig. 4.15b, the appearance of nickel peak in the spectrum is always accompanied by an aluminum peak. Hence, it might be possible that an aluminum-nickel alloy might have formed during the etching process and redeposited on the SiC surface. Murdo S. MacLean[51] invented a method to produce aluminum-nickel alloy by sintering aluminum powders on an oxidized nickel surface at 610 °C. Though this is not a plasma-based process, it confirms the possibility of forming aluminum-nickel alloy at high temperatures and with the help of oxidization on the nickel surface. Another work is from L. Shevtsova's team[52], in which Ni_3Al–Ni composite materials were obtained by spark plasma sintering of Ni_3Al and metallic nickel powder mixtures at 1100 °C. However, it can not be confirmed from either of these two methods that the aluminum and nickel peak shown in the EDS results indicates the existence of an aluminum-nickel alloy. It can only be considered as a good motivation point for future work in investigating the cause of micro maskings.

4.2. SiC etching with SiO2 hard mask

ICP RIE process development for the 4H-SiC substrate using a SiO_2 hard mask is the secondary technical route of this work. Though SiO_2 does not show a good selectivity in 4H-SiC etching, it is a "clean" hard mask material, which means the ICP RIE process developed using SiO_2 can be integrated with other processes. This section will present the DOE results using SiO_2 as a hard mask material, the thickness of which is 8 μm. Silicon was chosen as the material of the carrier wafer. All the ICP RIE tests using a SiO_2 hard mask were conducted using the Oxford Plasma Pro 100 Estrelas tool, supported by Kavli Nanolab.

4.2.1. Role of substrate temperatures

The parameter setting is shown in Table 4.10. The substrate temperature range is from -120 °C to 20 °C. Since the selectivity of SiO_2 is low, the etch time was set to 5 minutes to ensure the survival of the SiO_2 layer after etching. The other parameters are the same as those in Table 3.8.

In addition, though the pressure was set to 1.5E-2 mbar, the actual values ranged from 5E-2 mbar to 5.33E-2 mbar due to the limitation of Estrelas tools.

As for the substrate temperature control, Table 3.1 mentioned that this is done by applying liquid nitrogen for cryogenic etching and Lauda chiller for standard etching. Liquid nitrogen mode is needed for temperatures below -10 °C. This means the DOE tests at temperatures from -120 °C to -20 °C were conducted using the liquid nitrogen mode.

The results of etch rate and selectivity as a function of substrate temperature are presented in Fig. 4.21a and Fig. 4.21b, respectively.

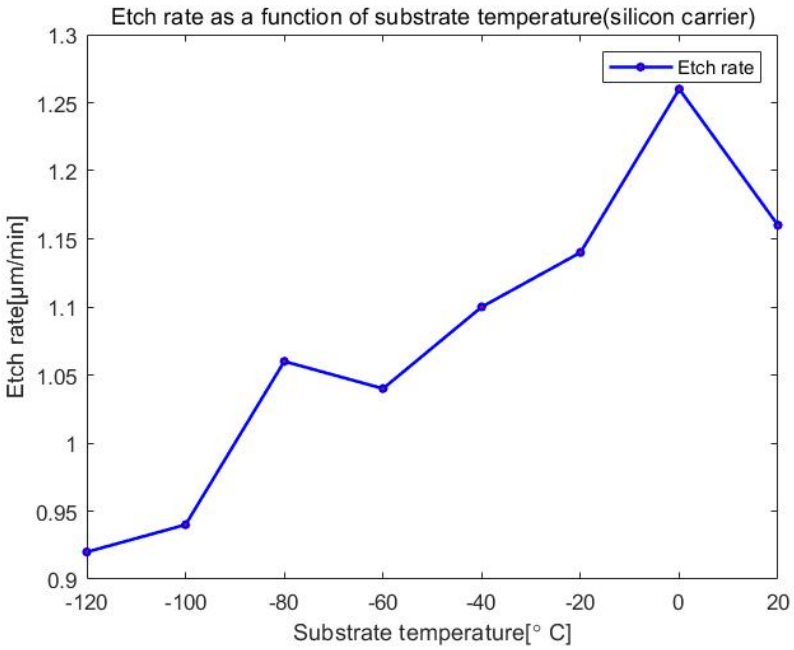
It can be seen that both etch rate and selectivity approximately increase with substrate temperature. As discussed in Section 2.2, the plasma etching process

Table 4.10: ICP RIE settings for 4H-SiC: varying substrate temperature. Silicon carriers were used.

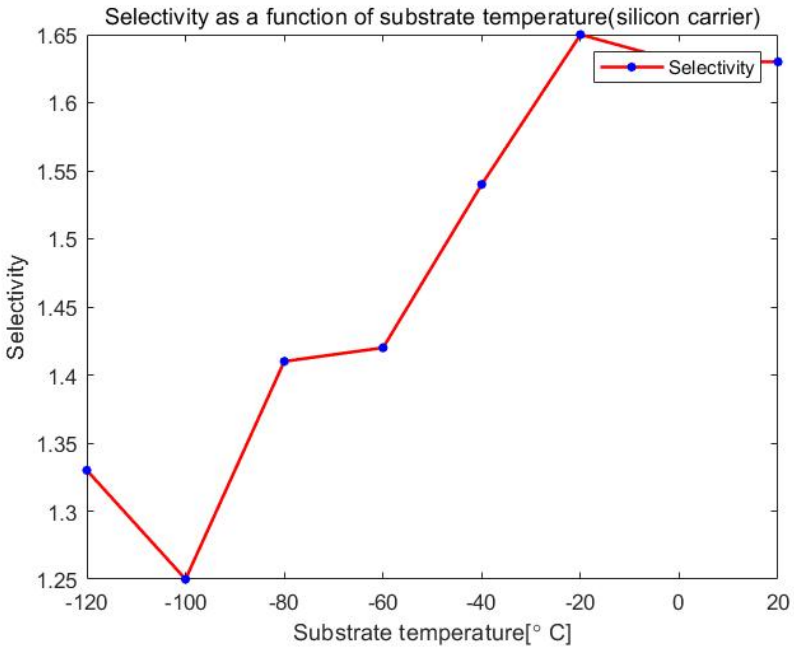
ICP source power	2500 W
Chuck bias power	300 W
Pressure	1.5 E-2 mbar
SF_6	100 sccm
O_2	25 sccm
Ar	100 sccm
Substrate temperature	-120 ,-100,-80,-60,-40 -20,0,20 °C
Etch time	5 minutes

of SiC includes both physical mechanisms and chemical mechanisms. The chemical etch is suppressed at low temperatures, leading to a lower etch rate. Thus, selectivity provided that the ion bombardment intensity does not change, which is controlled by the chuck bias power, will be small at low temperatures. The maximum achieved selectivity is 1.65.

In addition, the etch rate is larger than those presented in Subsection 4.1.1 and Subsection 4.1.2. The maximum value is 1.26 μm/min. Since the SiO_2 can react with fluorine plasma to form volatile products, there is a very limited chance of micro masking formation on the SiC surface. As shown in Fig. 4.22, micro-masking-free surfaces were achieved at both minimum and maximum values of substrate temperature.



(a)

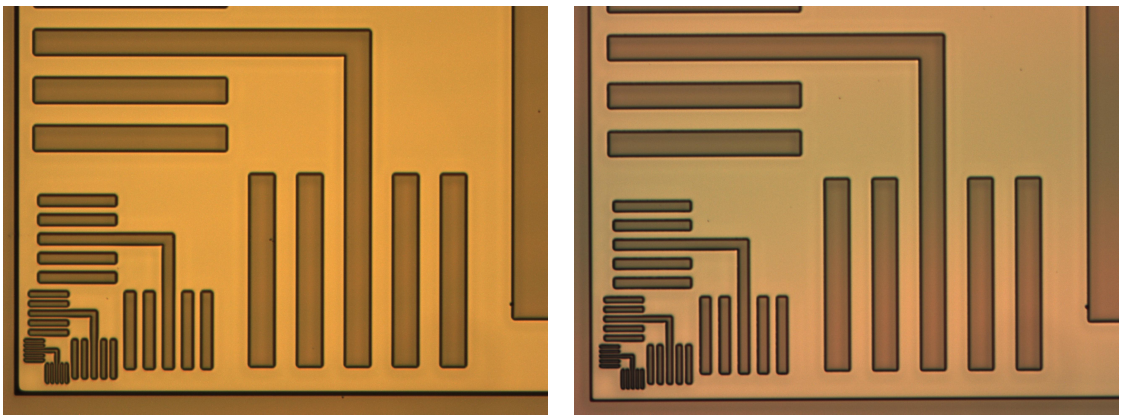


(b)

Figure 4.21: Role of substrate temperature:(a)Etch rate as a function of substrate temperature. (b)Selectivity as a function of substrate temperature. Silicon carriers were used.

4.3. Conclusion

This chapter presented the DOE results using nickel and SiO_2 as hard mask materials. For the tests using nickel mask materials, the role of silicon carriers



(a) (b)

Figure 4.22: Microscope figures at substrate temperature:(a)-120 °C.(b)20 °C. Silicon carriers were used.

and nickel-coated silicon carriers was studied. Both the technical routes using nickel and SiO_2 hard masks achieved micro-masking free surface applying the settings in Table 3.8 except for the etch time and pressure. The maximum etch rate with a nickel hard mask is 1.07 μm/min, while that using SiO_2 as a hard mask is 1.26 μm/min. The maximum selectivity with a nickel hard mask is 153. For those using SiO_2 as a hard mask, the maximum selectivity is 1.65.

5

Conclusion

This chapter will review the previous chapter, draw a conclusion, and give recommendations for future work.

5.1. Conclusion

This project aims to develop a standardized recipe for Inductively coupled plasma(ICP) reactive ion etching(RIE) process on a 4H-SiC substrate based on MEMS applications. To achieve this, several specifications must be met: high etch rate, micro-masking-free surface, and high selectivity.

When the research was finished, optimized baseline recipes for ICP RIE on 4H-SiC substrate in terms of etch rate and selectivity were developed, shown in Table 5.1 and Table 5.2, respectively. The achieved specifications are listed in Table 5.3. The optimization of the recipes was conducted by:1) Conducting a literature review. 2) Performing a pre-cleaning step. 3) Conducting EDS analysis. 4) Changing carrier wafer materials. 5) Performing Design of Experiments(DOE).

Last, the material of the carriers used during the ICP RIE process on SiC was found to play an essential role in determining the etch rate and micro masking level. Though silicon carriers were consumed much faster than nickel-coated carriers, a higher etch rate was achieved on SiC samples processed using silicon carriers.

Table 5.1: ICP RIE optimized baseline settings for 4H-SiC: high etch rate

ICP source power	2500 W
Chuck bias power	300 W
Pressure	1.5 E-2 mbar
SF_6	100 sccm
O_2	25 sccm
Ar	100 sccm
Substrate temperature	20 °C

Table 5.2: ICP RIE optimized baseline settings for 4H-SiC: high selectivity

ICP source power	2500 W
Chuck bias power	300 W
Pressure	5.5 E-2 mbar
SF_6	100 sccm
O_2	25 sccm
Ar	100 sccm
Substrate temperature	20 °C

5.2. Future work

Though a high etch rate, high selectivity, and micro-masking-free surfaces were achieved, there are still issues related to the etching profile, such as the loading and edge effects.

For ICP RIE processes using fluorine and oxygen plasma, the micro trench formation is inevitable. A way to remove the micro trench is to perform thermal chlorine etching. However, due to the limit of the tool's capability, this solution could not be tested and verified.

As for the loading effect and edge effect, more ICP RIE tests at the wafer level can be done in the future to study the effect of sample areas on the etch rate.

It is also challenging to do a long-time ICP RIE process on 4H-SiC wafers, especially for ICP DRIE. This requires a hard mask material with a high selectivity to SiC while maintaining high bias power for a large etch rate. In addition to nickel, copper is another good candidate, except for its high contamination level.

In addition, as mentioned in Subsection 4.1.4, the cause of micro masking on the SiC surface using nickel-coated silicon carriers is still unknown. More research is needed on ICP RIE process development using nickel-coated carriers.

Last but not least, the possible applications of this work include MEMS device fabrications on SiC substrates, packaging technologies such as Through SiC Vias (TSiCV), and other processes where SiC substrate etching is needed.

Table 5.3: Achieved ICP RIE specifications

Etch rate	Micro masking level	selectivity	Recipe setting
1.07 μm/min	micro-masking free	48.42	ICP power 2500W Chuck bias power 300W Pressure 1.5E-2 mbar SF_6:O_2:Ar= 100sccm:25sccm:100sccm Substrate temperature 20 °C Etch time 10 min Silicon carrier Nickel hard mask
1.26 μm/min	micro-masking free	1.63	ICP power 2500W Chuck bias power 300W Pressure 5.0E-2 mbar SF_6:O_2:Ar= 100sccm:25sccm:100sccm Substrate temperature 0 °C Etch time 5 min Silicon carrier SiO_2 hard mask
0.642 μm/min	micro-masking free	153	ICP power 2500W Chuck bias power 300W Pressure 5.5E-2 mbar SF_6:O_2:Ar= 100sccm:25sccm:100sccm Substrate temperature 20 °C Etch time 10 min Silicon carrier Nickel hard mask
1.14 μm/min	micro-masking free	1.65	ICP power 2500W Chuck bias power 300W Pressure 5.2E-2 mbar SF_6:O_2:Ar= 100sccm:25sccm:100sccm Substrate temperature -20 °C Etch time 5 min Silicon carrier SiO_2 hard mask

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A

Flowchart

Hard mask fabrication

1. Nickel METALLIZATION @ CR100

Use the TRIKON SIGMA sputter coater for the deposition of Nickel metal layer on the process wafers. Follow the operating instructions from the manual when using this machine.
Sputter a 1 um thick layer of Nickel.
Visual inspection: the metal layer must look shiny (light brown).
Turn off the wafer sensor before processing.

2. MANUAL COATING AND BAKING @ CR100

Perform a manual 10 min HMDS treatment using the HMDS station and the Pt carrier

Use the BREWER SCIENCE MANUAL SPINNER to coat the wafers with 1.4 µm resist.
Follow the instructions specified for this equipment, and always check the temperature of the hotplate first.
Use program **SPR3012_1400nm** for BREWER SCIENCE MANUAL SPINNER

After coating perform a 60 seconds softbake at 95 °C. Use the CONTAMINATED HOTPLATE to bake the wafers.

Note: use contaminated chuck for spin coat, and contaminated hotplate for soft bake

3. EXPOSURE @ CR 100

Option 1:
Processing will be performed on the ASM PAS 5500/80 automatic wafer stepper.
Follow the operating instructions from the manual when using this machine.

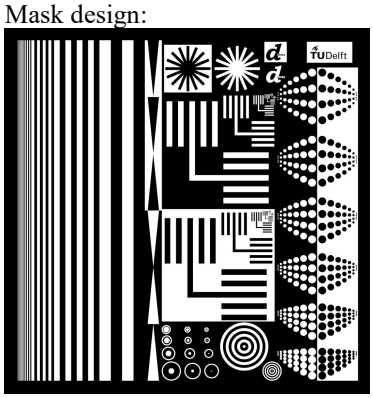
The contaminated wafer carrier has to be used during exposure

Use Photo Mask in BOX 413 SUEX.
Use the correct litho job:
Job: 6mm_diesize/ Die6x6mm_9IMG
Layer ID: Image 6
Mask name in Stepper: 3x3
Exposure energy: 140 mJ/cm^2.

Option 2:
Processing will be performed on the SUSS MicroTec MA/BA8 mask aligner.
Follow the operating instructions from the manual when using this machine. Use the contaminated chuck

Use recipe : **2-FSA_Soft_Contact**
The exposure time is 8.64 s

Mask design:



4. MANUAL DEVELOPMENT @ CR100

After exposure a post-exposure bake at 115°C for 90 seconds is performed on the CONTAMINATED HOTPLATE, followed by a 1 minute development step using Shipley MF322 developer (single puddle process), and a post (hard) bake at 100°C for 90 seconds.
Follow the instructions specified for this equipment, and always check the temperature of the hotplates first.

5. INSPECTION

Visually inspect the wafers through a microscope. Check whether there are resist residuals. Put a piece of paper underneath the wafer or use the contaminated wafer carrier.

6. MEASUREMENT @ Pavilion

Use the DEKTAK 150 MEMS to measure the height of photoresist layer.
Follow the operating instructions from the manual when using this machine.

7. WET ETCH Nickel @CR10000

Use the CR10000 wet bench 1-3 to do the wet etch
Follow the operating instructions from the manual when using this machine.
Remove the uncovered Nickel using the etchant consisting of buffered hydrofluoric acid, nitric acid(65%) and DI water in the ratio BHF: HNO3(65%): H2O = 1:1:50.

If necessary reduce the dilution to increase etch rate.

8. MEASUREMENT @ Pavilion

Use the DEKTAK 150 MEMS to measure the total height of photoresist layer and Nickel layer, so we are able to know Ni thickness by subtracting the PR thickness.
Follow the operating instructions from the manual when using this machine.

9. MANUAL COATING AND BAKING @ CR100

Perform a manual 10 min HMDS treatment using the HMDS station and the Pt carrier

Use the BREWER SCIENCE MANUAL SPINNER to coat the wafers with 3.1 µm resist.
Use the CONTAMINATED HOTPLATE to bake the wafers (soft bake).

Follow the instructions specified for this equipment, and always check the temperature of the hotplate first.
Use program **ECI3027_3100nm** for BREWER SCIENCE MANUAL SPINNER

Perform a 2 min 100 °C hard bake to fully cure the resist. Use the contaminated hotplate

Note: this step is to keep debris away during dicing.

10. DICING @ MEMS

The diamond blade has to be used. Suggested dicing size: 4 chips of 6x6 mm combined (~1.2x1.2 cm pieces)

11. RESIST STRIPPING @ CR10000

Remove the resist with acetone, IPA, DI water, all 5 min.
Note: Acetone is to remove PR and organic stuffs, and IPA is to remove the acetone residual.

12. INSPECTION

Visually inspect the wafers through a microscope. Check the structures of the geometric features of the Nickel structure.
Put tissues under the wafer because it is contaminated by Nickel.

13. MEASUREMENT @ Pavilion

Use the DEKTAK 150 MEMS to measure the height of Nickel layer.
Follow the operating instructions from the manual when using this machine.

ICP DRIE

14. ICP DRIE

Option 1:
Use the ICP Estrelas at Kavli Nanolab to etch the SiC substrate.
The SiC sample should be glued on a carrier wafer.

Option 2:
Use the ADIXEN AMS110 in Else Kooi Laboratory to etch the SiC substrate.
The SiC sample should be glued on a carrier wafer.

15. INSPECTION

Visually inspect the wafers through a microscope. Check the completeness of the etching.
Put tissues under the wafer because it is contaminated by Nickel

Etch result inspection

OPTION 1: Strip off Nickel after etching. Use the DEKTAK 150 MEMS to do the measurement

16. MEASUREMENT @ Pavilion

Use the DEKTAK 150 MEMS to measure the total height of remaining Nickel layer and the etched SiC vias.
Follow the operating instructions from the manual when using this machine.

17. STRIP OFF Ni LAYER @ CR10000

Use the CR10000 wet bench 1-3.
Follow the operating instructions from the manual when using this machine.
Remove the uncovered Nickel using the etchant consisting of buffered hydrofluoric acid, nitric acid(65%) and DI water in the ratio BHF: HNO3(65%): H2O = 1:1:50.

18. INSPECTION

Visually inspect the wafers through a microscope. Check whether there are residuals of Nickel.
Put tissues under the wafer because it is contaminated by Nickel.

19. MEASUREMENT @ Pavilion

Use the DEKTAK 150 MEMS to measure the depth of the etched SiC vias.
Follow the operating instructions from the manual when using this machine.

OPTION 2: DO NOT Strip off Nickel after etching. Use the SEM to do the measurement

16. MEASUREMENT @ Pavilion

Use the SEM to capture the profile of the SiC structures after etching.
Follow the operating instructions from the manual when using this machine.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