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T. Stavenga,[1] S. A. Khan,[2,3] Y. Liu,[2] P. Krogstrup,[4] and L. DiCarlo[1,a)]

AFFILIATIONS

[1]QuTech and Kavli Institute of Nanoscience, Delft University of Technology, P.O. Box 5046, 2600 GA Delft, The Netherlands
[2]Center for Quantum Devices, Niels Bohr Institute, University of Copenhagen, Universitetsparken 5, 2100 Copenhagen, Denmark
[3]Danish Fundamental Metrology, Kogle Alle 5, 2970 Hørsholm, Denmark
[4]NNF Quantum Computing Programme, Niels Bohr Institute, University of Copenhagen, Blegdamsvej 17, 2100 Copenhagen, Denmark

[a)]Author to whom correspondence should be addressed: l.dicarlo@tudelft.nl

ABSTRACT

Quantum hardware based on circuit quantum electrodynamics makes extensive use of airbridges to suppress unwanted modes of wave propagation in coplanar-waveguide transmission lines. Airbridges also provide an interconnect enabling transmission lines to cross. Traditional airbridge fabrication produces a curved profile by reflowing resist at elevated temperature prior to metallization. The elevated temperature can affect the coupling energy and even yield of pre-fabricated Josephson elements of superconducting qubits, tunable couplers, and resonators. We employ grayscale lithography to enable reflow and thereby reduce the peak temperature of our airbridge fabrication process from 200 to 150 °C and link this change to a substantial increase in the physical yield of transmon qubits with Josephson elements realized using Al-contacted InAs nanowires.

Free-standing metallic strips bridging separate planar conductors, called airbridges (ABs),[1] are widely used in classical[2] and quantum[3–6] microwave-frequency integrated circuits. They are most commonly employed to suppress slotline-mode wave propagation in coplanar-waveguide transmission lines (CPWs)[7,8] by connecting the ground planes flanking the central conductor, thereby avoiding spurious resonance modes and reducing crosstalk. A second use of ABs is as interconnect allowing transmission lines to cross with low impedance mismatch and crosstalk.

ABs are intensely used in superconducting quantum hardware based on circuit QED,[9,10] where CPWs are commonly used to make resonators for qubit readout and qubit-qubit coupling, as well as qubit control lines. For example, in our planar quantum hardware architecture[11] designed for surface-code error correction, 7- and 17-qubit processors contain ∼600 and ∼1200 ABs, respectively, of which 3 and 20 are used for crossovers.[12] In the 49-qubit version, the number of AB crossovers jumps to 130 owing to the routing of qubit control lines from the chip periphery to more qubits at the center. Signal routing at higher qubit counts requires advanced methods based on three-dimensional integration, including through-silicon vias,[13–15] bump bonding,[16,17] and the chip packaging itself.[18] In this context, ABs remain essential for slotline-mode suppression and crossovers.

ABs are typically added in the final fabrication step as otherwise resist non-uniformity induced by the few-micrometer height of ABs can reduce yield and increase variability of post-fabricated circuit elements (for exceptions, see Refs. 19 and 20) The most traditional AB fabrication method uses resist reflow at elevated temperature to produce ABs with smooth, rounded profile. However, many types of Josephson junctions (JJs) are not compatible with this elevated temperature. Examples include the semiconductor–normal–superconductor (SNS) JJs based on InAs[21] and InSb nanowires[22] used in SNS transmons[23,24] (also called gatemons and nanowire transmons). The temperature excursions can reduce JJ yield at worst and unpredictably affect the JJ coupling energy at best, affecting qubit frequency targeting.

In this Letter, we apply grayscale lithography (GSL), a method most commonly used to fabricate microlenses,[25–27] to reduce the peak

temperature in our AB fabrication procedure from 200 °C (required for standard reflow) to 150 °C (limited by resist adhesion). Our main result is the demonstration that lowering the peak AB processing temperature by incorporating GSL (and without changing resist stack) benefits the physical yield of SNS transmons. These SNS transmons have junctions realized using epitaxially grown, Al-contacted InAs nanowires and do not have voltage sidegates allowing *in situ* control of carrier density.[23,24] We perform our demonstration in two steps. First, we use test chips to show that a peak temperature of 150 °C does not increase the room-temperature (RT) resistance of nanowire junctions, whereas 200 °C does. Second, we establish a negative correlation between RT junction resistance and physical yield of SNS transmons (Fig. 5) in complete circuit QED devices. We note that recent work[6] has shown the use of GSL to reduce the number of electron-beam (e-beam) lithography steps required to fabricate ABs (from two to one), showing compatibility with transmons based on standard superconductor–insulator–superconductor (SIS) JJs only. Our focus here is SNS JJ compatibility rather than fabrication complexity, with emphasis on the positive impact that replacing reflow with GSL in our AB fabrication procedure has on SNS-transmon physical yield. We believe that GSL can serve as the enabling factor for AB integration when using other resist stacks for which the resist-reflow temperature increases junction resistance but the temperatures of resist baking and stripping do not.

AB fabrication by GSL (Fig. 1) starts after defining the chip base layer containing all CPW structures and transmons, including their SNS junctions. A layer of PMGI (blue) SF15 (6.4 or 3 μm thick, see below) is spun and baked for 5 min on a hotplate at 150 °C. This is found to be the lowest viable temperature avoiding resist adhesion problems. Using e-beam lithography and GSL, the AB profile and clearances are then written. An AZ400K/water mixture in a 1:4 volume ratio is used for development. The chip is dunked into the developer for 35 s followed by a thorough water rinse for 30 s and blow-drying. At this point, we typically check for correctness by measuring the height profile along the curve of an AB using a profilometer [Fig. 3(c)]. Next, a 400 nm thick layer of PMMA 495k (orange) is spun and baked in a vacuum oven at 100 °C for 10 min, immediately followed by a 1.5 μm thick layer of PMMA 950k (orange) spun and baked in the same way. E-beam lithography and resist development define the lateral dimensions of the ABs. The top-layer resists must be compatible with the bottom-layer resist. This means that the top layer solvent cannot dissolve the bottom resist after it has been developed and that the developer for the top layer resists cannot develop the bottom layer. A 30 s buffered oxide etch with 1:1 dilution factor is performed prior to metal deposition. We next sputter 200 nm of NbTiN (yellow) without any argon milling as the plasma can induce currents in the SNS junctions, causing their failure. A photoresist, 700 nm of S1805 baked at 85 °C for 3 min, is used for protection during dicing. After dicing, this resist is liftoff using 88 °C N-methyl pyrrolidone (NMP) for 15 min and followed by two rinses in isopropanol (IPA) at 80 °C for 10 min. Due to the conformal nature of sputtering, there is a vertical edge of NbTiN in the AB periphery. The height of this vertical edge is ∼400 nm, while the deposited NbTiN thickness is 200 nm. We do not expect the vertical edge to affect qubit performance as all ABs are far away from the transmons and the edge constitutes only a small part of the ABs.

Figure 2 shows a complete circuit QED test device with 185 identical ABs (with dimensions as in Fig. 1), fabricated by GSL. An AB yield of 100% was observed over four runs of device fabrication. Each device consists of 12 flux-tunable SNS transmons each with a dedicated readout resonator coupling to a common feedline. Six of the transmons have dedicated flux bias lines, but all can be globally tuned using an external coil. The flux-tunable Josephson element in each transmon consists of two Al/InAs/Al junctions in parallel with loop area ∼20 μm^2. The two junctions are fabricated from a common hexagonal InAs nanowire with 100 nm diameter and two facets covered with epitaxially grown Al (10 nm thick). Each SNS junction is defined by etching a ∼200 nm section of Al [Fig. 2(e)].

Contrary to the traditional method of producing a curved AB profile by reflowing the PMGI at elevated temperature (200 °C), GSL achieves the rounding by spatial control of the e-beam dose. For a

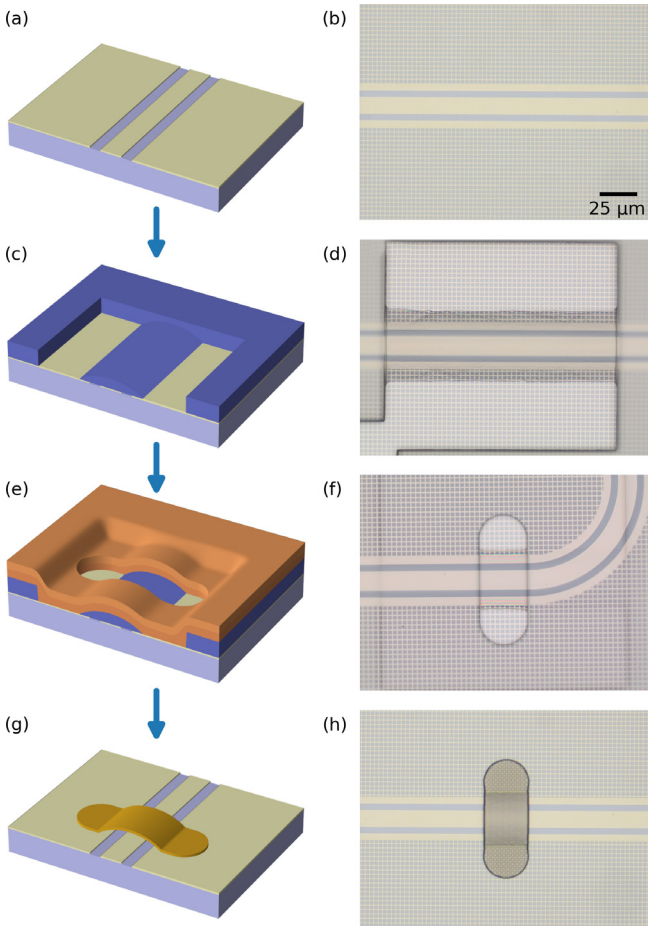

FIG. 1. Overview of airbridge fabrication by the GSL method, using (left) schematics and (right) optical images. (a) and (b) Pre-fabrication of the base layer. All CPW transmission lines have 12 μm center conductor width and 4 μm gaps between the central conductor and the flanking ground planes. (c) and (d) Patterning of the PMGI (blue) bottom resist layer using GSL. (e) and (f) Patterning of the PMMA top resist bilayer (orange) defining the lateral dimensions of airbridges. (g) and (h) Sputtering of NbTiN (yellow) and liftoff. All ABs in our study have the same nominal dimensions shown here.

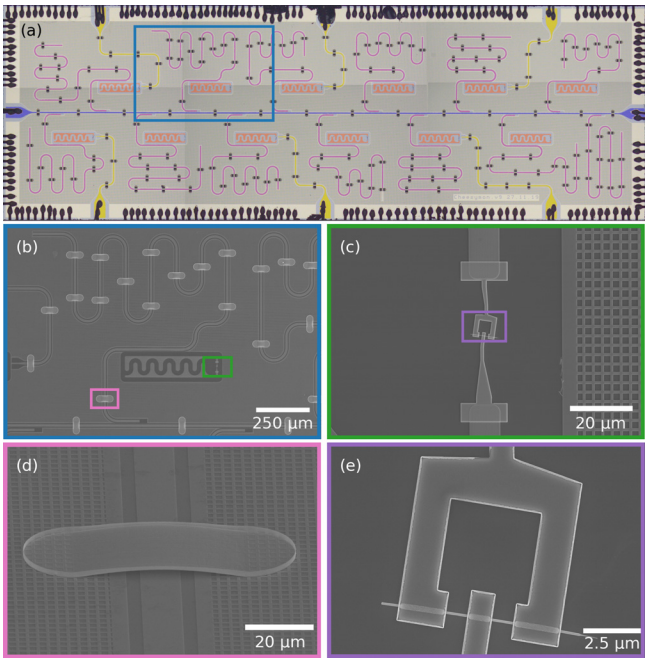

FIG. 2. Images at various length scales of a circuit QED test device with 100% yield of 185 airbridges fabricated by the GSL method. (a) Optical image of the full device ($7 \times 2.3\,\mathrm{mm}^2$), with added false color. The device has 12 flux-tunable SNS transmons (red) with dedicated readout resonators (purple) coupled to a common readout feedline (blue). Six of the SNS transmons have dedicated flux-control lines (yellow). (b) and (e) Scanning electron micrographs (SEM) showing (b) one SNS transmon and its dedicated readout resonator; (c) the SNS junction pair and its connection to the transmon capacitor pads; (e) zoom-in on the SNS junction pair and SQUID loop; and (d) an example airbridge.

positive resist like PMGI, a lower (higher) dose causes slower (faster) removal of the resist, resulting in a higher (lower) remnant resist thickness. Our desired resist-height profile is semi-circular, mimicking the profile achieved in the reflow process by surface tension. To achieve this, it is necessary to correct for proximity error as long-range scattering deposits up to 30% of the e-beam energy at a range exceeding 20 μm [Fig. 3(a)]. If this effect is not compensated, areas with dense (sparse) features are overexposed (underexposed). It is also important to calibrate the non-linear dose-height correspondence (contrast curve). Non-linearity is desirable in typical microfabrication, as almost all processes require a binary resist profile (so-called perfect contrast) in which the resist is either not exposed or fully exposed. On the other hand, a linear resist is ideal for GSL. The non-linearity of PMGI (6.4 μm thick) is evident in the measured contrast curve shown Fig. 3(b). We precompensate proximity and resist nonlinearity using the three-dimensional proximity effect correction (3D-PEC) module in the GenISys BEAMER software.[28] The inputs are the point spread function of the energy deposited by the e-beam lithography machine on the resist stack, the interpolated contrast curve[29] and the desired height map [Fig. 3(c)]. The output is a prescribed position-dependent dose. Following these calibrations, we actually reduced the thickness of the PMGI layer to 3 μm in order to reduce stress in the film, which at the original thickness caused cracks in the resist and many nanowires to detach. By reducing the development time from 50 to 30 s, the

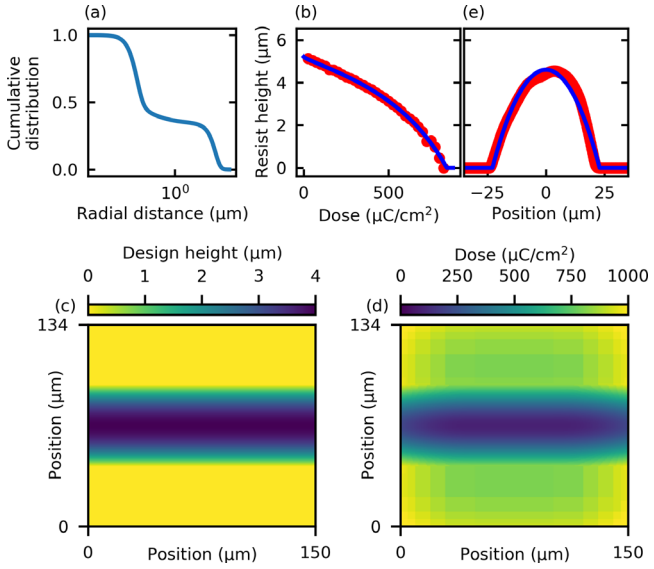

FIG. 3. Calibration of grayscale e-beam lithography. (a) CDF of the energy of the e-beam in PMGI on top of NbTiN. Note that more than 30% of the energy is deposited beyond a 20 μm radius. (b) Calibration of PMGI height as a function of local e-beam dose (red) and fit (blue) used for interpolation by the software. (c) Two-dimensional image of the targeted resist height for the airbridge. (d) Image of the dose map required to achieve the height map in (d) with precompensation for proximity effect and resist nonlinearity. (e) Vertical line cut (red) of actual PMGI resist height as measured with a profilometer and best fit to a circle function (blue).

calibrations were found to remain valid. This GSL process has very high yield and is stable with time. The first and last fabrication runs performed using the process, 16 months apart, yielded very similar airbridges without recipe adjustments.

GSL avoids the PMGI reflow step needed in the traditional method, reducing the peak PMGI temperature from 200 °C to 150 °C. We devise a simplified test to investigate the effect of PMGI peak temperature on SNS JJ resistance at RT. This test entails spinning 3 μm of PMGI on two chips with arrays of single junctions. Next, one chip is heated on a hotplate for 5 min to 150 °C while the other is heated to 200 °C. The chips are not directly placed on the hotplate; rather, as is standard practice, a Si wafer (6″ diameter) is placed in between. Finally, the resist is stripped off using a bath of NMP at 88 °C followed by two baths of IPA at 80 °C.

The purpose of this test is to show a general trend toward an increase in junction resistance for the higher processing temperature. For a valid comparison, it is important that initial junction resistances for both chips be similar. Two-point resistance measurements using a manual probe station confirm the overlap of cumulative distribution functions (CDFs) of initial resistance for both chips, as shown in Fig. 4(a). We perform a fit using kernel density estimation[30] to each of these CDFs and compute the derivative of the best fits to estimate the probability distribution functions (PDFs) of resistance. The results, shown in Fig. 5(c), reveal a pretest concentration around 20 kΩ for both chips. The different temperature excursions make the resistance distributions become qualitatively different, as shown by the CDFs in Fig. 4(b) and the PDFs in Fig. 4(d) (similarly obtained). For junctions exposed to 150 °C(200 °C), the distribution of resistances shifts

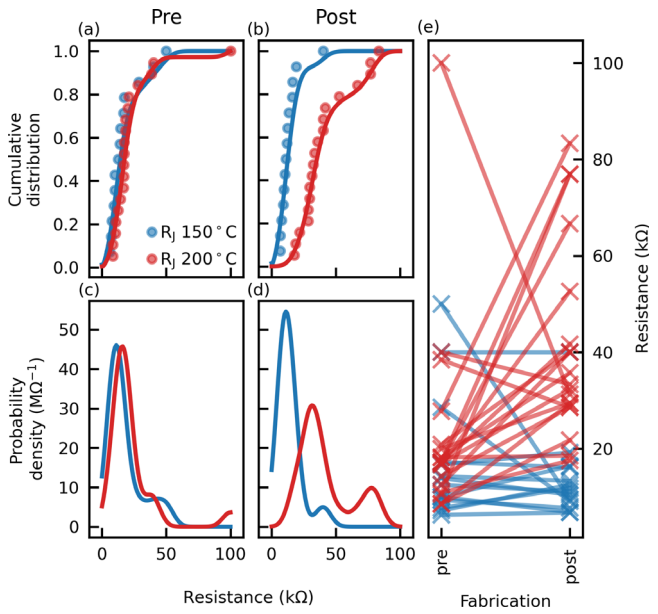

FIG. 4. Temperature tests of two arrays of single SNS junctions that are exposed to either 150 °C (blue) and 200 °C (red) for 5 min in PMGI. The tests simulate the temperature excursions of the GSL method and the traditional reflow method, respectively. (a) and (b) CDFs of junction resistance (a) prior to and (b) following the temperature test. (c) and (d) PDFs derived from the CDFs (c) prior to and (d) following the temperature test. A clear shift toward higher resistances is observed for the 200 °C test. (e) Comparison of each junction resistance before and after the test. Note the relatively similar initial distributions of resistance and the different final distributions.

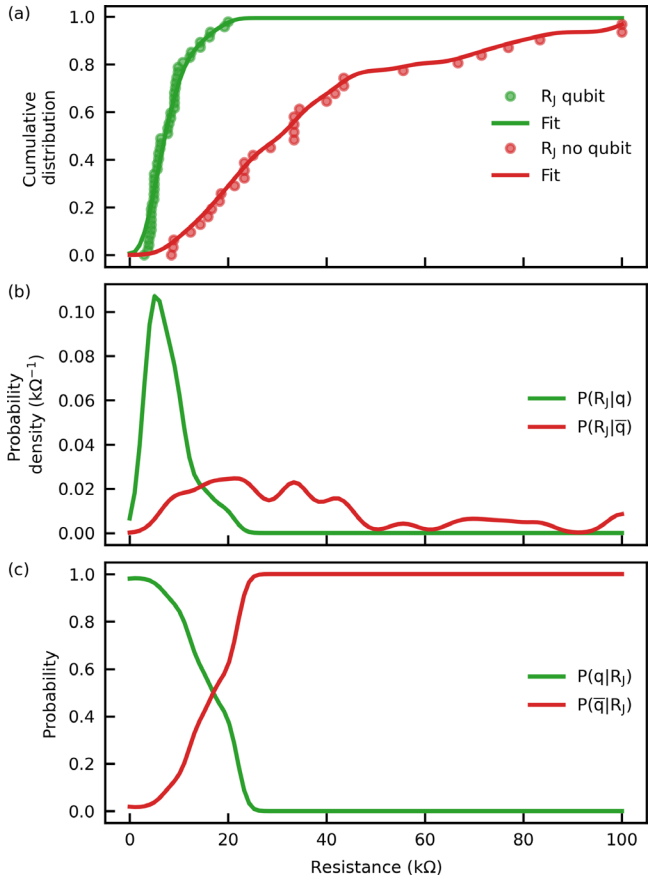

FIG. 5. Study of the physical yield of junction pairs based on their RT resistance. (a) Cumulative distribution function of the resistance for yielding (green) and non-yielding (red) transmons. Here, physical yield is conditioned on the observation of a power-dependent frequency shift in the dedicated readout resonator (see supplementary material Fig. S2 for an example). (b) PDF derived from (a). (c) Posterior probability [calculated from (b)] of the physical yield of a transmon as a function of its JJ resistance at RT.

downward (upward). The trajectory of individual junctions can be followed in Fig. 4(e). For 150 °C, the majority of resistances stay close to their initial values. For 200 °C, however, the majority increase. Some junction resistances do decrease in both cases, particularly ones starting at the high end. While we do not understand the reason for this decrease, we speculate that it may arise from the different cleaning procedures used after the initial JJ contacting (see the supplementary material) and after the simulated AB step.

Finally, we connect the physical yield of a SNS transmon at cryogenic temperature to the RT resistance of its nanowire-junction pair. We define physical yield as the fraction of the transmons where we can simply observe of a power-dependent shift of the frequency of its readout resonator (see supplementary material Fig. S2 for an example). Such a shift attests to the presence of a non-linear element, i.e., a junction, and this junction having high enough Josephson coupling energy. We distinguish physical yield from performance yield, which would further condition on criteria, such as qubit relaxation and dephasing times, gate fidelities, etc. In total, 78 qubits were measured from 8 devices. These devices fall into three categories: three devices without ABs, for which the physical yield was 18 of 25 transmons; one device with ABs fabricated by reflow, for which the physical yield was 1 of 9 transmons; and four devices with ABs fabricated by GSL, for which the physical yield was 28 of 44 transmons. Using optical inspection, all trivial cases where the transmon would not have worked for extraneous reasons were excluded from the total count. Figure 5(a) shows numerical CDFs of the junction pair resistance for transmons that exhibit resonator power shifts (green) and for transmons that do not (red). These data clearly show that the physical yield corresponding to a lower junction resistance is generally higher than the physical yield corresponding to a higher resistance. Fits to these numerical CDFs are done using kernel density estimation.[30] The derivative of each best fit gives a probability density function (PDF) [Fig. 5(b)]. Using a Bayesian update, we extract the posterior probability corresponding to the physical yield of a transmon given its RT resistance. The probability [Fig. 5(c)] starts off close to unity and decreases to 0.5 by ∼18 kΩ. The probability reduces to near zero by ∼25 kΩ. We conclude that for a good SNS Josephson junction it is vital that the RT resistance be as low as possible, cementing the benefits of replacing resist reflow by GSL in our AB fabrication process.

In summary, we have employed grayscale lithography to reduce the peak temperature of our airbridge fabrication procedure by eliminating the need for resist reflow and without changing resist stack. We have shown that lowering peak processing temperature from 200 °C (needed for PMGI reflow) to 150 °C (limited by PMGI adhesion)

increases the yield of SNS transmons based on InAs-nanowire Josephson junctions. We have done this in two steps. First, we showed that GSL-based fabrication produces lower JJ resistances. Second, we showed that lower JJ resistance increases the probability of having a higher yield of SNS transmons at cryogenic temperature. For future work, it remains important to attempt to correlate the AB fabrication process with SNS transmon qubit performance yield. It is also very worthwhile to investigate the dependence of RT junction resistance over a wider range of temperature and with finer resolution, for PMGI and especially for other resists. This study would allow assessing whether variants of the fabrication procedure and other resist stacks are suitable for AB integration on SNS transmon devices and whether GSL may serve as the enabling integration factor (i.e., the reflow temperature increases resistance but baking and stripping temperatures do not). It is specially interesting to explore other e-beam resists that bake at lower temperatures without suffering adhesion problems as well as optical GSL using a direct laser writer, which could possibly lower baking even to room temperature.

See the supplementary material for details regarding the SNS junction fabrication, comparison of the processes for AB fabrication using GSL and traditional reflow; and a typical example of a power-dependent resonator frequency shift.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

S.A.K. and Y.L. grew the nanowires and performed their post-growth characterization, under supervision of P.K. T.S. developed the airbridge fabrication recipe, fabricated the circuit QED test devices, and performed all measurements and data analysis. T.S. co-wrote the manuscript with L.D.C., who supervised the project.

Thijs Stavenga: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Writing – original draft (equal). **Sabbir Ahmed Khan:** Resources (equal). **Yu Liu:** Resources (equal). **Peter Krogstrup:** Resources (equal); Supervision (equal). **Leonardo DiCarlo:** Funding acquisition (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data shown in all figures of the main text and Supplementary Information are available at http://github.com/DiCarloLab-Delft/Grayscale_Lithography.

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