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Ultra-Thin Deformable Silicon Substrates with Lateral Segmentation and Flexible Metal Interconnect

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Our progress in developing technology modules for deformable single-crystalline-silicon electronics is presented in this contribution. Additional deformability/reliability is accomplished by modifications of the previously reported ultra-thin and flexible CIRCONFLEX technology (1). The flexibility is added in the last steps of the process flow using a combination of lateral segmentation and flexible metal interconnects. The post-processing nature of the added mechanical flexibility is thought to allow sensors and electronics to be built with proven technologies before they are rendered flexible. The additional deformability/reliability is achieved by lateral segmentation of silicon/dielectric layers and connecting these using flexible electrical interconnect. In the current study, segment thickness (silicon/SiO_2) of ~1 µm, segment size between 150 and 450 µm, spacing of 20-200 µm and serpentine-shaped aluminum interconnect transferred onto 8-10 µm thick polyimide film are characterized by tensile stretching to find out the reliability limits. Compared to our previous reports (2, 3), next to the processing issues also new electrical integrity results obtained from passive electrical test structures implemented on fully segmented polymer-embedded silicon islands are presented.

1. Introduction

Mechanically flexible systems containing electronic or sensory functionality (i.e. sensory-skins (4)) are expected to facilitate the seamless deployment of a variety of sensors in the human environment or in spaces where the available volume is limited (e.g. inside diagnostic medical instrumentation such as catheters, Fig.1). A number of different

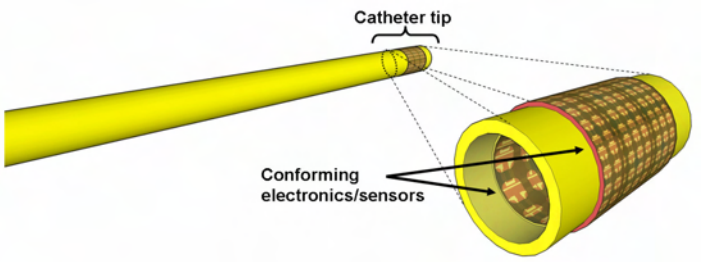

Figure 1. Illustration of a flexible system containing electronic and sensory functionality conforming on the inside and/or outside surface of e.g. an intracardiac catheter.

approaches to render an electronic system mechanically deformable have been reported in literature and a selection of them is discussed in the following before presenting the chosen approach.

A distinction is attempted between approaches that focus on rendering flexible the interconnects that lead to otherwise stiff components or assemblies and approaches that consider flexibility a global property of the system/assembly. Examples of the first approach are i.e. the flexible interconnect for two-dimensional ultrasound arrays (5) which allow the placement of a stiff transducer matrix on the sides or tip of transthoracic or intracardiac catheters or the "Microflex" technology (6) which allows the assembly of individual components, such as SMD's or chips using ball studs as rivets to connect them both electrically and mechanically to the flexible ribbon. A different approach is to design the system with global flexibility in mind. Examples of this approach are flexible skins inspired by the interwoven structure of fabrics (7, 8) where the repeatability of certain geometries gives the overall flexibility and even more, stretchability of the structure. Stretchability is a desired property when the assembly should conform on fixed two dimensional curved surfaces like a sphere or follow the movement of a non-rigid surface like skin or textiles. The difficulty of the second approach mainly lies in the fact that the materials used for building the highly flexible surfaces (parylene (7), polyimide (9)) are not commonly used to serve as substrates for high performance electronics. Property desirable since the ability to locally process information, which becomes necessary when the derived sensory output of the envisioned sensory matrices is overwhelming, is based on the possibility to build the electronics close to the generated data (4).

A straightforward solution is the use of silicon-based electronics embedded within relatively stiff silicon segments surrounded by a flexible medium. Flexible/stretchable interconnect between the stiff segments is one requirement in order to allow the transmission of control and data signals and at the same time allow the matrix to remain functional even under varying deformations (stretching, bending). Barth at al. (10) was one of the first, if not the first, demonstrating the feasibility of the island approach with a one-dimensional sensor array of p-n junction based thermometers built on 1500 μm spaced, 400 μm thick silicon islands connected with 20 μm wide, 1 μm thick evaporated gold wires. Jiang at al. (11) uses the same island concept and demonstrates a shear-stress sensor skin. The resulting sensor matrix is around 70 μm thick (silicon islands thickness) and results in a 2D densely spaced sensor matrix (50 μm spacing between sensing elements) and therefore with high sensing resolution. The sensor matrix is flexible enough to conform on the cylindrical surface of a delta wing. The requirement for one dimensional conformability of the sensor is fully covered by the design without any special concern on the design of the interconnects that lay between the islands. The processing of the sensors and interconnects is almost identical to that of a similar sensor matrix on a rigid substrate (apart from electrically passive metallization that serves as etch stop during backside island segmentation).

In our approach the metal interconnects are structured in a way to be able to demonstrate local (Fig. 3) and global stretchability. The interconnects due to their meander shape can mechanically deform under loading and prevent early failure. The distance between the silicon partitions varies from 20 to 200 μm, while their size varies from 150 to 450 μm (side of square partition). The proposed approach renders the silicon

substrate flexible and preserves a dense silicon matrix (gaps 20-200 μm) allowing for high resolution of a sensor array since the sensing elements can be placed in such proximity from one another. An extension of the substrate transfer technology (12) for SOI wafers (Circonflex) (1) has been previously used for demonstrating wireless ID tags (RF-ID tags). In this technology the active circuitry is transferred on a flexible ultra-thin (<10 μm) polyimide substrate. It was demonstrated that it is possible to bend the polyimide substrate and the circuitry to a radius of 0.7 mm while still remaining functional. In previous work (2) the transfer on a polyimide layer was combined with vertical thinning of the silicon substrate and its lateral partitioning. It was observed that with increasing loading, cracks that initially appear at the dielectric layers at the regions between the segmented polysilicon islands propagate to the islands themselves. To increase the reliability of the structure a new set of masks has been designed and used to remove the silicon oxide from the in-between segments regions.

Additionally, electrical interconnects of different geometrical shapes are fabricated between the islands. Electrical test structures have been integrated on the silicon islands to verify the electrical integrity of the flexible interconnects. By measuring the electrical resistivity before and after the substrate transfer step as well as during mechanical deformations (stretching), new reliability results were obtained. Compared to partially segmented structures (segmented silicon and continuous PECVD oxide layers (2)), significant improvement of mechanical reliability has been achieved.

2. Design choices and processing

2.1 Design choices

A four mask set was designed and used to prepare fully segmented polycrystalline silicon segments and the flexible aluminum interconnect structure. The aluminum interconnects are supported by polysilicon bridges of the same shape as the metal interconnects. On each wafer (4 inch) there are 20 samples with dimensions 5.6 by 30 mm with varying island size (from 150 to 450 μm) and varying inter-island spacing (from 20 to 200 μm). The maximum segment size has been limited to 450 μm, since previous work (2) demonstrated that larger side lengths (i.e. 600 μm) result in samples with island structures (square) that are already vulnerable (crack formation and fracture) at bending diameter of 8 mm.

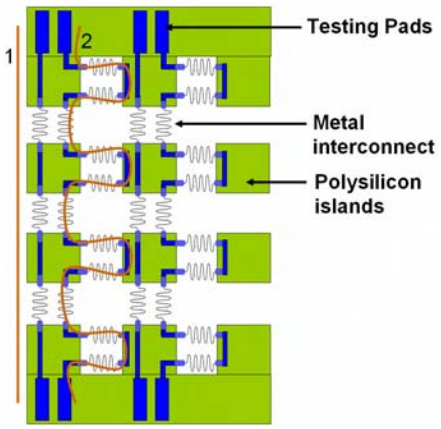

Figure 2. Testing paths for verifying integrity of interconnects: (1) Straight path, (2) Path including interconnects at orthogonal directions.

Different interconnect shapes were designed in order to get an idea of the relationship of the shape with the degree of elongation achievable before failure. The serpentine interconnect shapes were derived by interpolating several points with a b-spline function. Figure 3 shows some of the different interconnect shapes implemented. In order to verify the integrity of the conductive paths before and after mechanical loading, one metal layer test structures are integrated on the polysilicon segments. Bonding pads for accessing the test structures were positioned at the opposite edges of the samples. Two testing paths were designed (Fig. 2). The first one spans the sample from one side to the opposite in a straight path while the second includes interconnects in orthogonal directions. The second test structure gives the possibility to evaluate the integrity of interconnects for loadings applied perpendicularly to the interconnect axis. The width of the aluminum path is 2 μm in the regions between the silicon segments. The width of the conductive path is much larger on top of the silicon segments to limit the overall path resistivity.

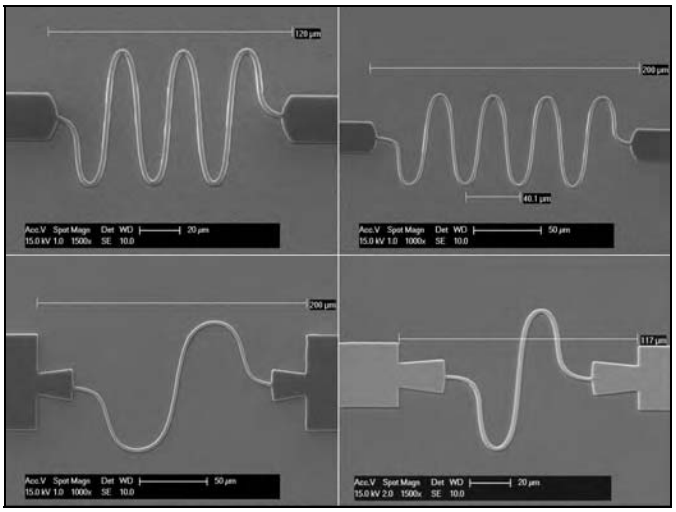

Figure 3. SEM pictures of different interconnect shapes.

2.2 Processing

The following flowchart is a variation of the one presented in (3) and is included here with all modifications for sake of clarity. The complete flow chart requires four masks. Initially, a 500 nm thermal oxide is grown on a 500-525 μm thick p-type <100> wafer followed by a 500 nm low-stress LPCVD polycrystalline silicon layer (undoped). These two layers are meant as a replacement for the more expensive SOI wafers, for the initial stages of the process development. In the final stages of development SOI wafers can be used to integrate sensors and/or electronics if required.

The polycrystalline layer is first deposited on the silicon oxide layer, followed by the deposition of the aluminum layer. A 600 nm layer of aluminum (99%Al, 1%Si) is sputtered at 50°C and is patterned using the first mask (Fig. 4.1a). This mask contains both the interconnects and the test structures within the islands. A plasma chemistry is used to etch the exposed aluminum layer (Cl_2, Br_2). Before depositing the aluminum layer, polysilicon is etched from two windows at the edges of the final samples to provide access to the test structures after full processing and delamination of the flexible foils. After patterning the aluminum layer, photoresist is spun on the wafer and exposed through the second mask (Fig. 4.1b). After development, the polysilicon layer is etched using both the aluminum interconnects and the patterned resist as a mask. The areas

under the photoresist define the polysilicon islands and the areas under the metal serpentine structures define the polysilicon bridges under the interconnects. Polysilicon is etched using a plasma chemistry (SF_6, O_2) that does not attack aluminum.

After resist stripping, a 500 nm thick PECVD oxide is deposited and patterned using the same mask as used for the segmentation of the polysilicon layer. In this way, the PECVD oxide is removed from the regions between the islands (Figs. 4.2d and 4.2e). This is important to avoid cracks appearing within the dielectric layer in the inter-island region (2). In the following steps, a polyamic acid (Durimide^{TM}) is spin coated at 1000 rpm and soft baked at 120°C for 6 minutes (Fig. 4.2f). Before curing, the polyimide at the edge of the wafer is removed (not shown in Fig. 4) to withstand the KOH wet etching during the following steps. The photoresist is patterned using an additional mask and an outer ring (~5 mm) is exposed. First the photoresist and then the polyimide are removed by developing for 7 minutes using a TMAOH based developer. The photoresist is removed with acetone and the patterned polyimide is cured for ~1 hour at 385°C in a N_2 environment. The cured polyimide has a thickness of 8-10 μm. On the cured polyimide layer, a 500 nm PECVD oxide layer is deposited at 300°C. At this point the wafers are prepared for adhesive bonding to a temporary glass carrier. An acrylic glue with a UV-sensitive component is used to achieve the bonding. The entire side of the glass wafer and only the outer ring of the silicon wafers are primered. The glue is purred on the silicon wafer and after the glass wafer is placed on top, the silicon wafer-glue-glass sandwich is rotated at a high speed. The spinning of the wafer sandwich results is a more uniform glue layer and wafer stack. After spinning, the glue is exposed under UV light for 5 minutes to cure the glue. The silicon substrate is etched for around 6 hours at 33% KOH at 85°C. The complete removal of the silicon substrate is finished at TMAOH at 85°C because of its increased selectivity towards the silicon oxide stop layer.

The glass carrier wafer is diced in the dimensions of the test samples and after delamination of the polyimide foil (which contain the segments and flexible interconnect) from the glass carrier, the silicon oxide layers from both sides are removed in a BHF 7:1 solution and the aluminum bondpads are exposed. At this point the integrity of the conductive paths is tested by resistivity measurements.

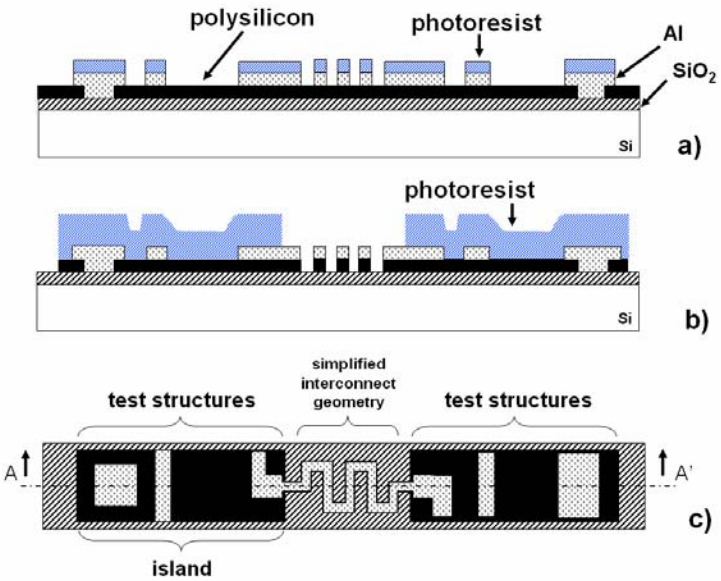

Figure 4.1 Flowchart of polysilicon-supported aluminum interconnect.

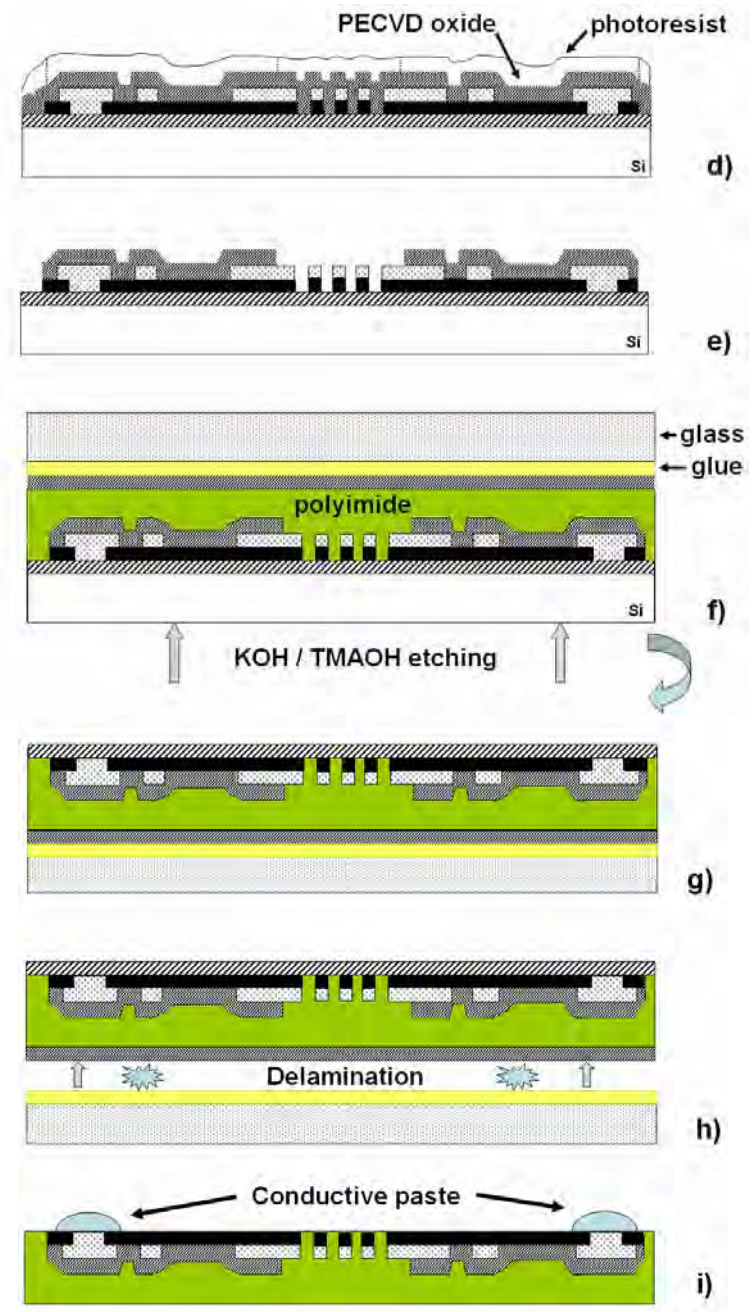

Figure 4.2. Flowchart of polysilicon-supported aluminum interconnect.

3. Results and Discussion

3.1 Segment integrity

Like in previous cases no cracks are observed in the silicon segments after sample delamination. The integrity of the silicon segments is not an issue before applying any load using the custom-built measurement setup. For the partly segmented samples of the first generation described in (2), under increasing loading, the cracks appeared at the oxide layer and propagated to the silicon segments (Fig. 5a).

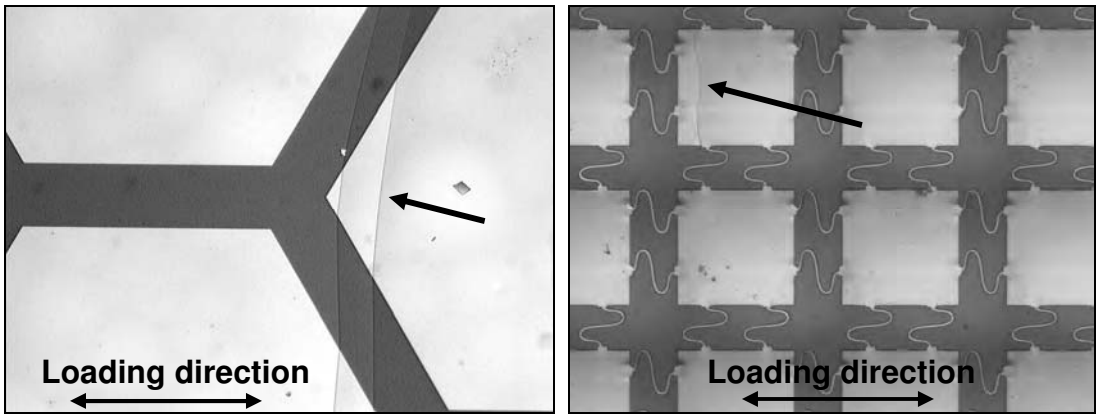

Figure 5. a) Crack propagation for partly segmented segments (segmented silicon/unsegmented silicon oxide), b) Crack confined in one silicon segment

Figure 6 illustrates the increase in achievable strain values of the fully segmented segments (complete isolation of the segment by removal of the inter-segment oxide) of the new samples, to the values obtained (2) from the partially segmented segments (old samples). Only the new samples that are comparable with respect to segment and gap sizes with the old samples are included. The failure strain of each completely segmented segment is met at higher value compared to the failure strain value of the partially segmented segments. The mechanical reliability of the segments has significantly improved, depending on the sample, from 67.9% (450 by 450 μm, 120 μm gap) to 257% (150 by 150 μm, 20 μm gap). Note should be taken here that the strain value of sample 150_20 is the final loading value reached since there were no cracks observed. Also the strain values refer to the onset of *segment* cracking and the improvement of the reliability of segments. The following section deals with the reliability of the interconnects.

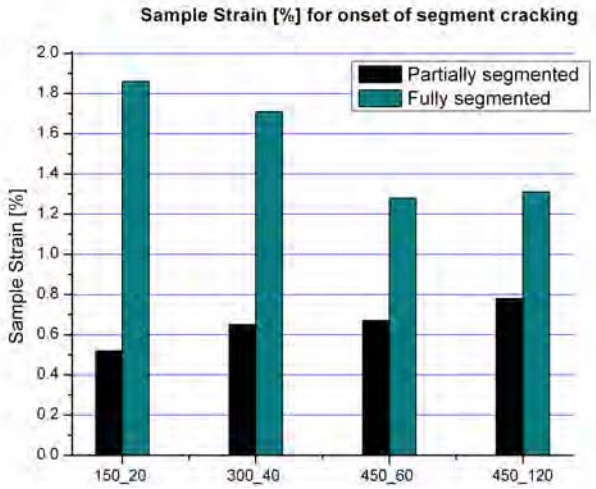

Figure 6. Strain values for onset of segment cracking for fully and partially segmented segments (segmented silicon / unsegmented silicon oxide). The first number of each sample refers to the size of the segment side length and the second to the gap between the segments.

3.2 Interconnect integrity

The integrity of the interconnects is verified, during processing, after their patterning and before the deposition of the PECVD oxide (Fig. 4.1c). A series of resistance

measurements were performed on both test paths (single and bi-directional) for the 20 different samples and interconnect geometries. The values range from 100 to 2000 Ohm depending on the actual interconnect length as defined by the number of periods of the serpentine geometry, the gap size between segments and their size. All of the tested paths were conductive. After delaminating the samples from the glass carrier, their resistancies are measured again and are found to correspond to the pre-released measurements which verifies the integrity of the interconnects after release from the temporary carrier.

A number of samples were tested under increasing tensile loading. At each increase of the tensile loading, the sample elongation, applied force, and resistance was recorded. Snapshots of the sample were taken (Fig. 7) at each loading step to link the crack onset to a specific loading condition. To facilitate the electrical testing of the interconnects under different loading conditions, all the resistive paths are connected in parallel at the two ends of the sample using a conductive adhesive paste. The total resistance of the individual samples is measured and found higher than expected. This indicates that the interface between the aluminum bondpads and the conductive paste adds to the overall sample resistance.

By recording the sample resistance during sample loading we are able to identify failures in the conductive paths by means of resistance changes. The complete failure of the conductive paths is also indicated by a recording of an infinite resistance. A typical behavior of a sample under increasing tensile loading consists of the recording of one or more increases in the sample resistivity value, followed by an observation of segment cracking, followed by further steps in increasing resistivity, followed by the total loss of the conductive path, followed by cracking of the sample itself.

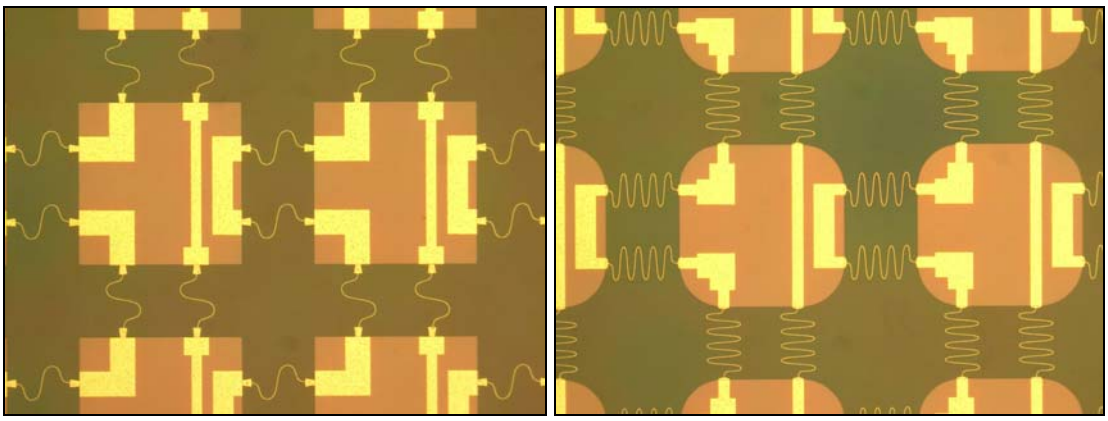

Figure 7. Snapshot of samples 450 by 450 μm (200 μm gap) taken after sample delamination.

The increase of the total resistance in steps is due to the failure in the conductive paths as the tensile loading increases. As it can be observed in Fig. 6 each conductive path consists of serpentine shaped parts and wider parts patterned on the silicon segments. When a resistance increase takes place it means that either an interconnect or a wide aluminum path on the segment has failed. The later could occur after a segment is cracked and pulled apart under increasing tensile loading. Only in the case of the 150 by 150 μm square segment samples (20 μm gap) no cracks were observed at the segments up until the complete loss of conductivity (at 1.86% strain). This indicates that the failure of

the conductive paths were due only to the failure of the interconnects. For the rest of the samples, segment cracks were observed as well, before complete loss of all conductive paths, which indicates a mixed failure mechanism of the samples.

Fig. 8 presents the maximum strain reached by individual samples before loss of conductivity and compares it with the strain values for the first increase in resistivity (conductive path failure). In most of the samples the strain increase for the total loss of conductivity from the onset of failure is less than the strain increase required to cause the first failure. An exception is sample 300 by 300 μm (gap 20 μm) where the first failure occurs at much lower strain values. The early failure could be due to processing defects in some of the conducting paths.

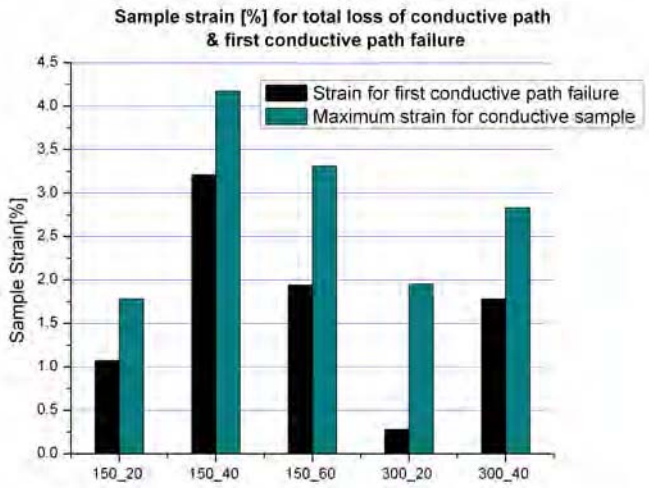

Figure 8. Strain for first conductive path failure and total loss of conductive path.

4. Conclusion

In previous work (2) it was determined that the cracks appear first in the silicon oxide layers between the islands and with increasing bending diameters then propagate in the islands themselves. The onset of cracks was around 0.5% while the best performing samples reached a 0.8% strain before crack formation.

Our first concern is to increase the reliability of the silicon segments. Simulations have shown that the encapsulation of the segments within a flexible medium (polyimide) causes the induced stresses from tensile and bending loading to concentrate in the flexible medium, reducing the stress concentration at the segments (13). Samples have been processed to verify the simulations. In order to increase the reliability of the structure, the dielectric layers are removed from those regions. The crack onset strain values are found higher for all sample configurations (segment and gap size) compared to the respective old samples. It is concluded that the complete removal of the oxide layer increases the reliability of the segments. The increase in mechanical reliability, measured by the increase from the previous crack onset strain value, was from 67.9% up to 257% depending on the sample configuration.

Since these experiments are conducted to develop technology modules for flexible substrates that are meant to integrate electronic and/or sensory functionality, a flexible electrical interconnect scheme is additionally tested. Conductive paths are laid out from

one side of the sample to the other between and on top of silicon segments. The meander shape of the interconnect between the segments allows the survival of conductive paths under increasing tensile loading. The maximum tensile loading depends on the segment gap size configuration. An indication of the failure strain loads of the interconnects is given by the recorded resistance increases of the samples.

As further steps, the thickness of the segments will be increased to improve their stiffness, to avoid segment cracking and to allow the integration of sensory functionality. Also by avoiding segment cracking, the failure mechanism of the conductive path will be limited to the interconnect failure which is expected to simplify the evaluation of different interconnect geometries. Additionally, materials with lower tensile strengths than polyimide such as parylene and elastomers as encapsulants are considered and first samples are processed. A comparison of the different materials as encapsulants will follow.

Acknowledgments

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