Addressing large-scale qubit arrays for quantum computer

By

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in partial fulfilment of the requirements for the degree of

Master of Science

in Electrical Engineering

at the Delft University of Technology,

to be defended publicly on Thursday December 17th, 2015 at 10:00 AM.

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Abstract

The recent implementation of single electron quantum dots (QDs) in semiconductor hetero-structures as quantum bits (Qbits) [1] disclosed a promising route for the forthcoming creation of the first quantum computers based on a large set of Qbits. The scaling up of Qbits would indeed exhibit the full potential of quantum computation. Confinement of electrons in QDs takes place at cryogenic temperatures by applying specific constant voltages to the gates of the QD [1]. The goal of this thesis has been the design and the analysis of a circuit providing constant voltages, with accuracy of 5 μV, to a set of 768 QDs kept at 20 mK. The proposed circuit would supply up to 2304 different voltages (3 biases/QD) employing only one DC bias, thus minimizing the thermal power dissipated into the cryogenic environment. Each Qbit is biased to its specific voltage (between -1 V and 1 V with accuracy of 5 μV) by dedicated capacitors. The charge stored in a capacitor is dynamically maintained around a constant value by the charging-discharging cycle driven by a MOSFET switch. The input controlling each switch, in turn, is managed by a digital devices assembly, which coordinates the 2304 different cycles. This part of the circuit is in contact with the Qbits matrix only through demultiplexers; therefore it does neither interfere with the cryogenic environment nor with the delicate coherent states of the Qbits.

The experimental section of this thesis focused on the fabrication and the characterization at room temperature and 4.2 K of MOS and parallel plate capacitors with thin (30 nm) SiO_2 film. The measured capacities for the smallest area capacitors have a value of 6.6 pF. While, the mean leakage current density through the oxide layer between -1 V and 1 V is at most 6 nA/cm^2. The average leakage current density at 4.2 K, between -10 V and 10 V, is 4 nA/cm^2 for the smallest MOS capacitors. This observation proved that the structural integrity of the capacitors is preserved at extremely low temperatures.

The quantitative analysis of the analog circuit dedicated to the charging-discharging cycles showed that a MOSFET switching frequency of 38 MHz is sufficient for the operation with 6.6 pF capacitor connected in series with 1 GΩ resistor. Moreover, the circuit stability analysis revealed that the system has a good resilience against random fluctuations of several variables. The results obtained in this work help us to sketch the future outlook to create a complete and efficient driving circuitry for large scale single electron Qbits computers.

Contents

Acknowledgements

At the beginning of this acknowledgement, I would like to thank my parents and my little sister for their support throughout my studies at the TU Delft. They have supported me during the difficult moments throughout these years and were always successful in reinforcing my persistence to reach the final pinnacle of a MSc student.

I would like to thank my responsible professor Dr. Ryoichi Ishihara from the Thin Film Transistors group at ECTM. He was the one who introduced me to this exciting and challenging project, which resulted into an immensely valuable experience concerning the interaction of two different engineering disciplines. I also received numerous valuable and original suggestions throughout the duration of the thesis work and was always welcome to discuss any arising issues or doubts along the way.

I would like to thank Prof. Lieven Vandersypen for the crucial discussions on the topic of quantum dots. It would have been impossible to make any progress without his insights and explanations. I also received numerous replies to my questions, especially at the early stages of the thesis work.

I would like to express my gratitude towards my daily supervisors, PhD candidate Juan Alfaro Barrantes, PhD candidate Yuanxing Xu, PhD candidate Pengfei Sun and Postdoctoral researcher Paolo Sberna. Juans knowledge and experience of the Clean Room processing was of great assistance during the fabrication and measurement stages of this thesis work. Yuanxing and me had many discussions on the architecture of the qubit arrays, which solved a lot of doubts and prevented unnecessary complications. She has also been extremely helpful with the performances of the measurements at the cryogenic temperature. Pengfei provided me with interesting and constructive information concerning the available MOSFET technology and its performance. Paolo and me had numerous discussions on all the elements of this thesis work. These conversations resulted into a significant increase of my insight in many different areas and resulted into a more detailed and tenacious approach towards science in general. Although not one of my daily supervisors, I would like to thank Takafumi Fujita as well. Takafumi was really helpful in explaining me the ideas behind the biasing configuration of a quantum dot.

I would like to thank Silvana Milosavljevic and Gregory Pandraud for their valuable knowledge on the Clean Room processing and their desire to solve issues at any given time.

I would like to pay my respects to the technical support team of the EKL lab. Alex van den Bogaard, Johan van der Cingel, Koos van Hartingsveldt, Mario Laros, Loek Steenweg, Cassan Visser, Wim Wien, Johannes van Wingerden and Henk van Zeijl have all been extremely helpful and kind to introduce me to the world of Clean Room. I would especially like to thank Wim Wien, Johannes van Wingerden, Johan van der Cingel and Henk Zeijl for their numerous assistances during my fabrication process. I am also very thankful to Loek Steenweg for aiding me during the dicing and wirebonding processes.

I would also like to express my gratitude to the many fellow MSc, most of whom I met two years ago for the first time. I would like to thank Sotiris Thomas, Rishi Raghav, Kiki Wirianto, Accel Nicolás Abarca Prouza, Hengqian Yi, Revanth Bellamkonda, Weihan Hu, Yiwen Chen, Debarshi Saha, Yingjie Shen, Lei Zou, Yiming Hu. I really enjoyed lunch conversations with Yingjie Shen and Lei Zou, as well as their tasty dishes and will remember the philosophical conversations with Debarshi Saha, Hengqian Yi, Yiming Hu for a long time.

At the end I would like to express my greatest gratitude to everyone involved with this thesis work and wish everyone good luck in the future.

1 Introduction

1.1. Quantum computation

A large class of problems is efficiently solved by employing classical computation algorithms. However, there is a set of tasks which cannot be practically faced by classical computation. Specifically, this set includes the factorization of large numbers, searching an unsorted database and simulation of many-body quantum systems. Nevertheless, these problems could be still efficiently solved thanks to the peculiar nature of quantum computation, which accounts for superposition, interference and entanglement of states.

Quantum computation, as elementary blocks of information, employs quantum bits (Qbits) which can assume a superposition of the classical states (0) and (1): $\alpha \cdot [0\rangle + \beta \cdot [1\rangle$.

The coefficients α and β are complex numbers and their square modulus respectively represents the probability that one can measure the Qbit being in state $[0\rangle$ or $[1\rangle$.

As complex numbers, the coefficients have a phase and this property allows to the Qbit state to undergo interference phenomena with other Qbits. When the computer can deal with a large number of Qbits, it can benefit from great computational advantages provided by the interference phenomena. This is basically what Peter Shor [2], [3], [4], [5] showed in 1994 when he presented the quantum algorithm for a large number N factorization. For a classical algorithm, factorization would take an exponential time, while, for the Shor's algorithm, a time of the order of N^3 is enough. Later Grover has proposed a multi-Qbit algorithm for searching an element in an unsorted database [6]. If the database contains N items, the Groove's algorithm will find the item in a time of order $N^{1/2}$, while any classical algorithm would take a time of order N. As with regards to the future simulation of multi-body quantum systems [4], the availability of a computer equipped with at least thousands of Qbits will be the most powerful tool.

There are quite a few different practical possibilities to create a Qbit [7-11], The major ones make use of either ion traps, nitrogen vacancies in diamond [12], [13], [14] or single-electron spin state in semiconductor quantum dots [1], [15], [16]. The details concerning these approaches are given in the following paragraphs, emphasizing the advantages and the drawbacks for future large scale implementation and integration.

1.2. Ion traps

In this methodology atomic or molecular ions are confined to a small volume for a long period of time by a particular arrangement of electro-magnetic fields generated by macroscopic components [19], [20], [22], [23]. Due to the confinement, it is possible to use the particle spin state as the variable for the quantum bit. Two kinds of traps can be employed and the difference lies in the typology of the applied fields.

1. Paul traps [21]: the charged particle is confined by RF fields applied to hyperbolic electrodes. With these oscillating fields and the specific design of the electrodes the electric potential felt by the particle has a time-average minimum.
2. Penning traps [17], [18]: this type of traps for charged particles consists in the superposition of a strong homogeneous magnetic field and a weak electrostatic quadrupole field. The electrodes can be hyperbolic or cylindrical. The generated confining force is proportional to the distance of the particle from the potential minimum, thus the particle undergoes harmonic oscillations.

The greatest advantage to employ ion traps for quantum bits is the virtual long stability of the particle inside, which would guarantee a long coherence time of the quantum state. Unfortunately, this comes at the cost of fabricating big electrodes which need to be cooled down to cryogenic temperatures. Despite ion traps being interesting for sub-nuclear physics research, these constraints and the overall functioning do not allow arranging an ensemble of numerous quantum bits.

1.3. Nitrogen vacancy defects in Diamond

Nitrogen impurities in crystalline diamond are able to create a charged vacancy defect (NV), which has a spin triplet ground state [24]. The spin state can be coherently manipulated by specific electro-magnetic fields at room temperatures [24]. Moreover, the fluorescence emission from the defect centers depends on their spin state; therefore the read-out of the spin variable is possible [24].

The quantum states associated with NV defects are relatively long-lived [13] and compared to ion traps, they restrict the existence of the quantum bit at the microscopic scale. This fact, in principle, would make NV centers one of the best candidates for many Qbits computers. However, the fluorescence collection efficiency is very low for diamond and the read-out operation results not reliable [25]. Some scientists suggested overcoming this problem using photonic amplifying structures [25] next to the NV arrays. Thou being interesting, this task is

very difficult to accomplish with the standard technologies, since it would require performance of complex fabrication processes at the microscopic scale. The fabrication of thousands of Qbits computer would thus be difficult, unless integrated on Si substrate.

1.4. Semiconductor quantum dots

In 1998 Loss and Di Vincenzo came up with the idea to define Qbits by the state of a single-electron spin in a semiconductor quantum dot (QD) at cryogenic temperatures [26]. In the QD, the electron is basically confined in a potential well properly created by the electronic bands mismatch and the local application of electric fields [15]. The bands mismatch can be created synthesizing hetero-structures with materials with different band gaps and electron affinities, such as Ge/Si core/shell nano-wires and Si/SiGe multilayers [15] on Si sibstrate [1]. Fig. 1.1 depicts a fabricated spin qubit with pattern of split gates on SiGe heterostructure.

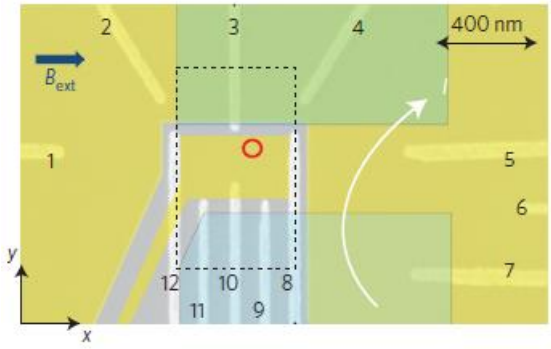

Fig. 1.1 A fabricated spin qubit with pattern of split gates on SiGe heterostructure. Adapted from " Electrical control of a long-lived spin qubit in a Si/SiGe quantum dot ", E.Kawakami, P.Scarlino, D.R.Ward, F.R.Braakman, D.E.Savage, M.G.Lagally, M.Friesen, S.N.Coppersmith, M.A.Eriksson, L.M.K.Vandersypen, 2014, Nature Nanotechnology, Vol. 9, pp. 666-670

A single quantum dot is created in this situation, the location of which is indicated by the red circle in Fig. 1.1. To confine the electron, voltages are applied to the gates 3, 8, 9 and 11 to deplete the semiconductor and hence form the quantum well. Four-stage pulses are applied to gate 3 to perform the following:

1. Initialization of the electron within the quantum dot to spin-down
2. Manipulation of the spin of the electron by applying a microwave signal at gate 8
3. Read out of the spin of the electron by RF reflectometry
4. Emptying of the quantum dot

The decoherence time of a spin qubit in a Si/SiGe quantum dot has recently been improved to 750-910 ns [27].

Semiconductor QDs are very promising for multi-Qbits computers because the fabrication processes are compatible with the current large scale integration technologies with Si [15], [28].

However, this approach faces a number of challenges: limited cooling power at 20 mK (~ 100 μW) [29], thermal flux due to the employment of cables (~$\frac{1\mu W}{cable}$), a deviation in the confinement voltages in the order of a few μV and the difficulty of scaling up a combination of a chemical battery and the control circuitry currently used.

1.5. The aim and content of the thesis

Thus single-electron QDs are promising building blocks for the future multi-Qbits computers due to their scalability.

The next fundamental challenge would be to implement the circuitry to support the stability of these Qbits and to allow confinement and the manipulation of the electron spin states. For this task, the circuitry must be accurate, reliable but at the same time simple and of extremely low-power at 20 mK.

The goal of this thesis is the investigation of the implementation of a circuit to provide constant voltages with an accuracy of 5 μV to the gates of a large amount (768) of quantum dots. As a quantum dot requires ~ 3-5 gates for the confinement process, every QDs in Si/SiGe hetero-structures needs 3 specific confining bias ~ 1 V with an accuracy of few μV. Hence, the greatest challenge is to address, to each QD, 3 different accurate voltages.

In this work a proposal is made to use an LCD-like array of voltage address lines. A general overview of the proposed system is displayed in Fig. 1.2.

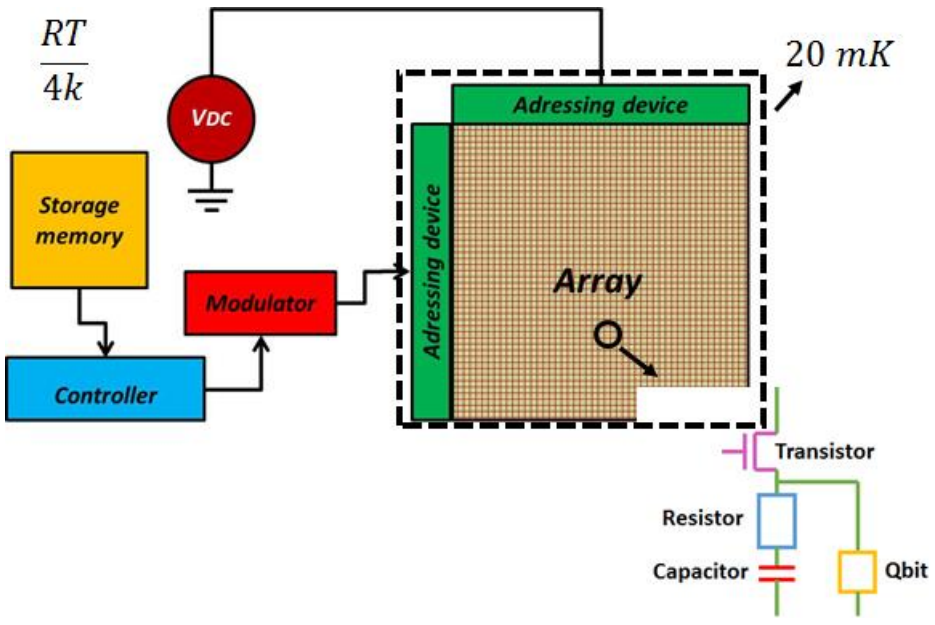

Fig. 1.2 General overview of the proposed system

Each node of the square array contains:

1. The Qbit/QD with a single gate, which, as described above, is located in the hetero-structure with all the electrodes;
2. A resistor, connected in parallel with the capacitor, to ensure a practically realizable charging time of the capacitor;
3. A small capacitor, connected in parallel with the QD, to provide the confinement voltage. It can be either a MOS capacitor or a parallel plate capacitor;
4. A MOSFET connected in series with the storage capacitor. It simply operates as a current switch and accurately controls the charging cycles of the capacitor. The bias applied to the QD depends at any time on the amount of charge stored in the capacitor, which in turn depends on the charging current modulated by the MOSFET switch. The current flow occurs due to a common external DC voltage supply;

The X and Y array lines are connected to two dedicated devices that address the specific signals to each MOSFET. The analogical signal addressed to each MOSFET switch drives it to modulate the charging current, keeping the bias of the capacitor fixed within a certain narrow (few μV) range. The input of these addressing devices comes from a section of the circuit containing a digital memory for the storage of the 2304 different bias values and components for the manipulation of the signals to be addressed to the array.

Chapter 2 deals with the fabrication process of the capacitor: both a MOS capacitor as well as a parallel plate device have been fabricated. The step by step procedure performed in the cleanroom to realize the two capacitors can be found in the appendices. A C-V as well as an I-V characterization at both room and cryogenic temperatures (4.2 K) of one of these devices[1] are presented and explored in chapter 3. The cryogenic measurements were performed at a 3He cryostat by means of an IVVI rack and the preparations involved included the wire bonding of several devices. Chapter 4 discusses the proposed system to provide constant voltages to the gates of a large amount of qubits in more detail. It also discusses whether the charging phase of each node of the array is error prone and to which degree. Another topics discussed in this chapter are the areal scalability of the proposed analog circuit and the power consumption of the entire QDs array.

[1] MOS capacitor

2 MOS capacitor fabrication

In the previous chapter quantum computation was discussed and it was concluded that the semiconductor quantum dots are the most promising methodology to realize it. Also the goal of the thesis was described and a short overview of the proposed approach was given. This chapter focusses on the fabrication process of a MOS and a parallel plate capacitors employed at each of the nodes of the square array mentioned in chapter 1. Chapter 3 will deal with the electrical characterization of the two fabricated devices.

In this work two capacitor structures have been considered for fabrication: a Metal-Oxide-Semiconductor (MOS) capacitor and a parallel plate (PP) capacitor. For the MOS and PP capacitors, SiO_2 has been used as the dielectric film, because of its good electrical properties and stability. For the electrodes of both kinds of devices Al has been firstly employed. Only for the MOS capacitors Nb has also been used due to its relatively high (9.26 K) superconductive temperature threshold [30]. The overview of the fabricated devices is given in Tab. 2.1.

Tab. 2.1 List of the fabricated capacitors

	Electrodes	Dielectric
MOS 1	Al / p-type c-Si	Thermal SiO_2
MOS 2	Nb / p-type c-Si	Thermal SiO_2
PP	Al / Al	PE-CVD SiO_2

Each type of capacitor has specific advantages and drawbacks. For instance, these MOS capacitors have thermal grown oxide, which has the best achievable qualities for SiO_2. However the disadvantages are that the MOS structure takes a large amount of space and its capacity is a function of the stored voltage. On the other hand, PP capacitors can be stacked, saving a big portion of area on the chip, and the capacity is constant with the voltage at the electrodes. However, the oxide of a PP capacitor cannot be a thermal grown SiO_2, thus the electrical quality of the dielectric is lower.

2.1. MOS capacitor fabrication

The structure of the fabricated MOS 1 capacitors (see Fig. 2.1-a) consists of a very thin (30 nm) SiO_2 film grown on top and bottom surface of a p-type crystalline Si wafer[2] and two Al films

[2] The wafer diameter is 4", the thickness is 525 µm, the surface orientation is <100> and the doping concentration is between 10^{15} and 10^{16} cm^{-3}.

(2 μm thick) deposited on the back side of the Si wafer (back-contact) and on the surface of the oxide (front-contact). This low thickness for the oxide layer has been chosen in order to have an as high as possible capacitance. The structure of the MOS 2 capacitors (see Fig. 2.1-b) is the same, except for the substitution of Al with Nb. The most important fabrication steps are illustrated in Fig. 2.2. The complete flow chart is provided in Appendix A.

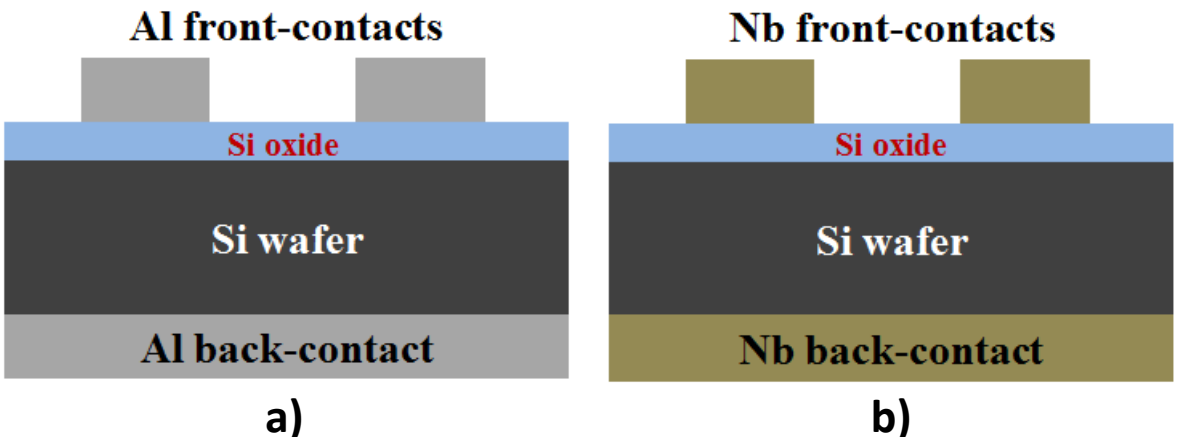

Fig. 2.1 Structure cross-section of the a) Al and b) Nb MOS capacitors

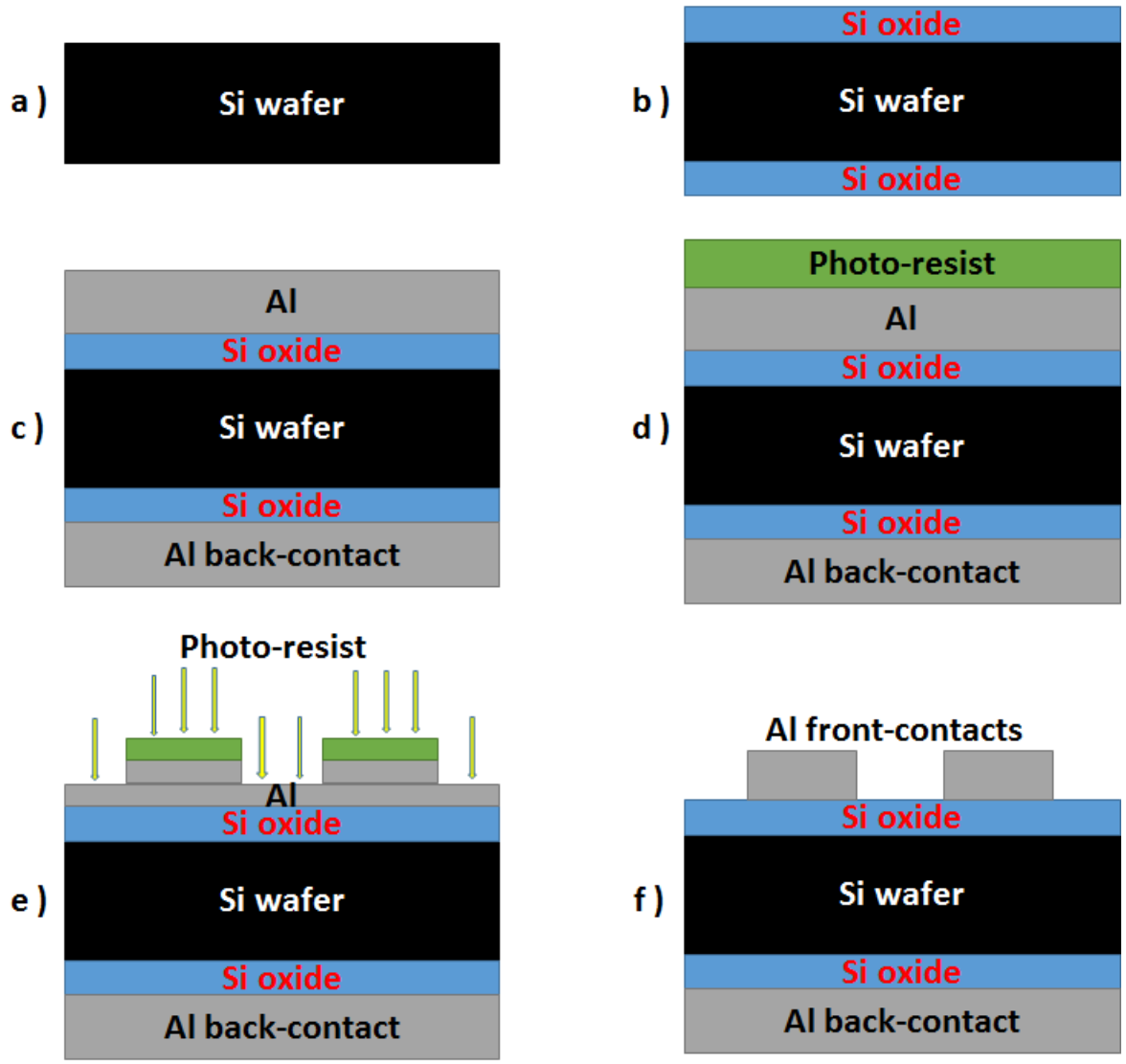

Fig. 2.2 MOS fabrication steps: a) Si wafer preparation, b) Si wafer thermal oxidation, c) Al films deposition, d) photo-resist top surface coating and exposure, e) Al dry etching and f) photo-resist removal

The first step of the fabrication (Fig. 2.2-a) is the cleaning of the Si wafer to remove all the possible organic and metallic contaminations from its surface and the backside. After cleaning, the wafer has been put in a tube furnace to perform the dry thermal oxidation (constant pure O_2 flux of 3 SLM) of Si top and bottom surfaces at T = 1100 °C.

The chemical reaction for the growth of the high density Si dioxide is:

$$Si_{(s)} + O_{2_{(g)}} = SiO_{2_{(s)}} \qquad (2.1)$$

After the first few nanometers of SiO_2 have been formed, the oxygen atoms diffuse towards the interface to react with Si. Based on this mechanism, the evolution of oxide thickness with time is well described by the Dear-Grove model [31]. However, for the growth evolution of the first layers of oxide there is not yet a clear model, thus in our case, the oxidation time has been calculated according to the empirical calibration curve available in our laboratory. To obtain 30 nm of SiO_2 film, a furnace-processing time of 1.5 hours has been set. The actual thickness of the film has been measured by the automatic Leitz MPV SP system and is equal to 34 nm.

The third fabrication step is the deposition of Al front and back contacts by means of sputtering (Fig. 2.2-c). This technique consists of the bombardment by Ar atoms of a pure Al target. Due to impacts with Ar atoms, high energy Al ions are removed from the target. These atoms then arrive with a certain amount of kinetic energy on the substrate surface, forming the Al film layer by layer. The sputtering deposition conditions are reported in Tab. 2.2.

Tab. 2.2 Parameters set for the sputtering deposition of the Al films

Ar flux	100 sccm
RF power	5 kW
Substrate temperature	50 °C

The oxide film grown at the back surface of the wafer actually creates a wide capacitor, connected in series with the MOS capacitors to be fabricated on the wafer front surface. The back surface electrode and the oxide film will not be patterned; therefore the capacitor extends along the whole wafer back area. Due to this, the associated capacity will be very high compared to the capacity of the MOS capacitors. Since the back capacitor and the MOS capacitors are connected in series, it follows:

$$\frac{1}{C_{tot}} = \frac{1}{C_{MOS}} + \frac{1}{C_{back}} \approx \frac{1}{C_{MOS}} \tag{2.2}$$

Hence, the C-V measurements will be not affected by the presence of the oxide between the wafer and the Al back contact.

The Al front film has been subsequently covered with an uniform layer of photoresist (PR) by an automatic spin coater (Fig. 2.2-d). The coated wafer has then been put in a stepper to impress film the image to be patterned on the Al film (islands of areas 80x80 (6.6 pF), 250x250 (60 pF)

and 700x700 (540 pF) μm^2) on the PR. The operation of the stepper is firstly to align the wafer to an above-lying quartz mask which already has the image patterned on a chromium layer. Then, the stepper proceeds shining a strong UV light on the wafer through the mask to impress the PR. The areas of the PR film which are invested by the UV photons undergo a photo-chemical modification of the inter-molecular structure. After these stepper operations, the wafer has been put again in the automatic coater to develop the PR image and leave PR islands with the requested shape and dimensions. The development is performed using a solvent which removes only the photo-chemically modified parts of the PR film.

Once the PR film has been patterned into islands, the wafer has been put in the dry etcher (Trikon Omega 201 system) to transfer the PR pattern to the Al front layer (Fig. 2.2-e). Indeed, during the dry etching, the energetic ions of the plasma, generated upon the wafer surface, attack and remove only the Al atoms from the areas not covered by the PR. The film areas capped with the PR, despite being bombarded are protected by the thick PR and maintain the original thickness of 2 μm. The dry etching conditions are being depicted in Tab. 2.3.

Tab. 2.3 Trikon Omega 201 system parameters set for the etching of Al front film

Platen temperature	25 ± 4 °C
He pressure	9.5 ± 5% Torr
Working pressure	5 ± 10% mTorr
Cl_2 flux	30 ± 10% sccm
HBr flux	40 ± 10% sccm
RF Power	50 ± 10% W
ICP Power	500 ± 10% W

The last step has been the removal of the residual PR (Fig. 2.2-f) by oxygen plasma cleaning.

At this point the Al MOS capacitors were ready to be characterized since all the inspections under the optical microscope revealed the successful achievement of the fabrication process.

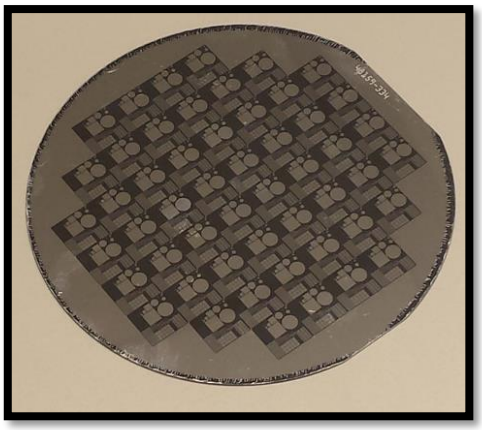

Fig. 2.3 Wafer containing Al MOS capacitors of different areas

In regards to the Nb MOS capacitors (MOS 2), unfortunately, the etching of the Nb front layer to pattern it into island has been not efficacious and the film remained continuous on the entire wafer surface (see the continuous shiny metal layer on the whole surface of the wafer in Fig. 2.4).

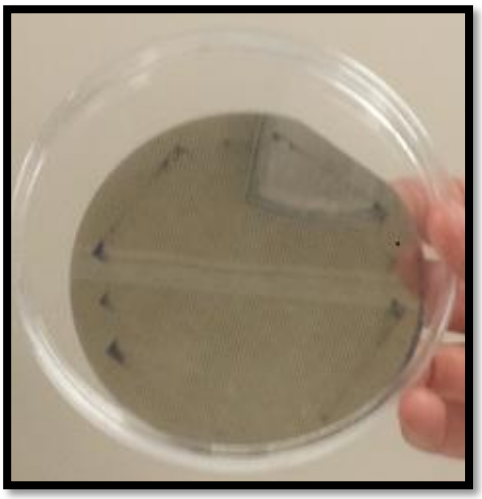

Fig. 2.4 Wafer containing Nb MOS capacitors. The central part of the Nb film surface appears not patterned, indicating a non-effective Nb etching. On the contrary, the etching is efficaciously close tot he edge of the wafer

Hence, the devices are not electrically isolated one from the other and their proper operation is undermined. The Nb dry etching has to be improved reviewing the parameters involved in the process, such as the etching duration. The parameters of the process are shown in Tab. 2.4.

Tab. 2.4 Parameters of the dry etching of niobium

Platen temperature	20 ± 3 ^{0}C
Helium BP	9.5 ± 5% Torr
Pressure	5 ± 20% mTorr
SF_6 flux	30 ± 15% sccm
RF Power	125 ± 10% Watt
ICP Power	500 ± 10% Watt

2.2. Parallel plate capacitors fabrication

The structure of the parallel plate capacitors (Fig. 2.5) consists of a very thin (30 nm) SiO_2 layer between two Al films (2 μm thick). The bottom Al film is deposited on a p-type Si wafer (back-contact), while the top Al layer is patterned into islands (front-contacts) to isolate the various capacitors from one another. The flow chart of the entire process is to be found in Appendix B.

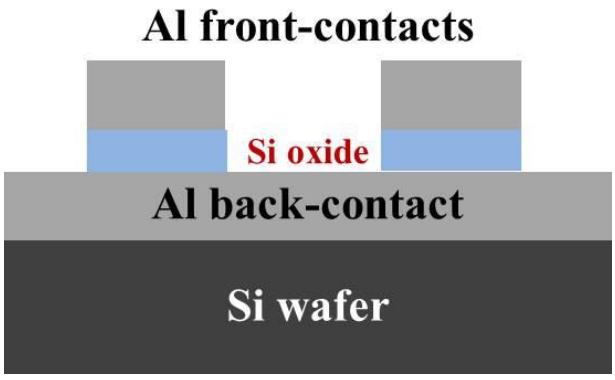

Fig. 2.5 Structure cross-section of a parallel plate capacitor

The fabrication process of the parallel plate capacitors starts with the standard cleaning of the Si wafer. Then the sputtering deposition (conditions reported in Tab. 2.2) of Al film has been made on the wafer clean surface. The synthesis of the oxide onto the metal layer has been made by plasma enhanced chemical vapor deposition (PE-CVD). In PE-CVD synthesis the precursor gases are mixed with plasma in the deposition chamber. Owing to the high energy stored in the plasma, the precursor molecules are fragmented and become highly reactive radicals, which, in contact with the substrate surface, start the formation and growth of the SiO_2 film. The most important details of the deposition are reported in Tab. 2.5.

Tab. 2.5 Details of the PE-CVD SiO_2 deposition

Precursor gases	SiH_4 and N_2O
Substrate temperature	400 °C

The actual oxide film thickness has been measured by the Leitz MPV SP system and is equal to 30 nm.

The following step has been the sputtering deposition of the second Al film on the oxide.

Since the Si oxide films synthesized by PE-CVD are not as dense as the films grown by thermal oxidation, after the second metallization, the sample has been annealed at T = 400 °C for 20 minutes in nitrogen atmosphere to induce the oxide densification.

The patterning of the front Al film into islands of 80x80, 250x250 and 700x700 μm^2 area has been achieved by the photolithographic and dry etching processes described earlier.

The final fabrication step has been the dry etching (performed by Alcatel GIR 300 F Etcher) of the oxide layer areas not covered by the Al islands. In this manner, the Al pattern has been transferred to the oxide layer and the PP capacitors have been separated one from the other for their proper functioning.

2.3. Packaging for cryogenic measurements

To perform the electrical characterizations at 4.2 K, the fabricated devices have to be specifically prepared; in fact they have to be put in thermal contact with a He refrigerator, while all the electrical connections with the measuring equipment are properly made as well. It was chosen to perform the measurements at this temperature instead of the aimed 20 mK as the current measured at this stage was already in the fA range, which is on the verge of the detection limit of the multi-meter employed. Thus measurements at lower temperatures would probably be undetectable by the equipment used.

The first step of the device packaging has been the dicing of the wafer containing the MOS capacitors. The 1x1 cm^2 die is then mounted in a case (the black square in Fig. 2.6-a) and connected to the printed circuit board (PCB) contacts by the gold wires of the case (Fig. 2.6-b). The whole case is subsequently attached to a metal bar (the left gold square with four holes in Fig. 2.6-a), which serves as thermal contact in the refrigerator.

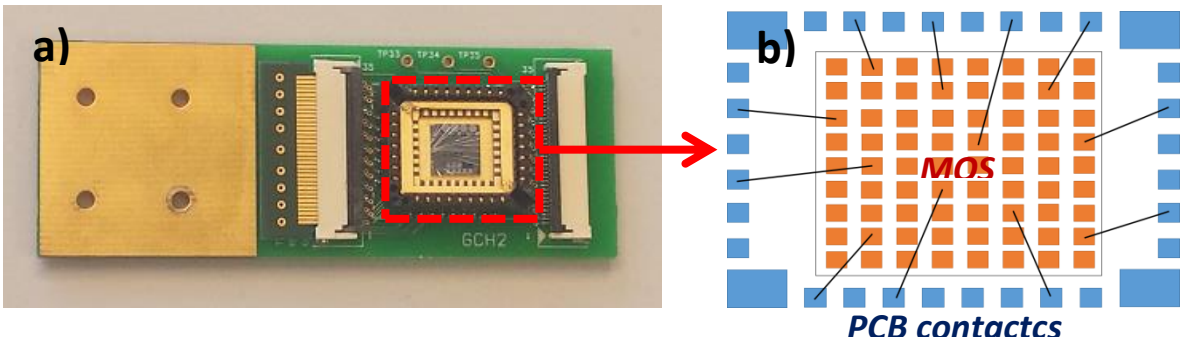

Fig. 2.6 a) wire bonded die of the wafer containing several MOS capacitors of 80umx80um and b) details of the electrical connections of the devices on the die

The die is then connected to the IVVI rack (Fig. 2.7) for the IV-measurements. The IVVI rack is not connected to the electrical net in order to keep the noise propagating through the equipment as small as possible. The working mechanism of the rack is as follows: a desired digital signal is sent from a computer to the rack by means of an optical fiber[3]. This signal is then converted to the equivalent analogic voltage signal by means of a digital-to-analogical converter (DAC) and is directed towards the sample. The voltage signal causes the pile up of charges and flux of current through the capacitor. The recorded amplified output signal has been the current through the capacitor.

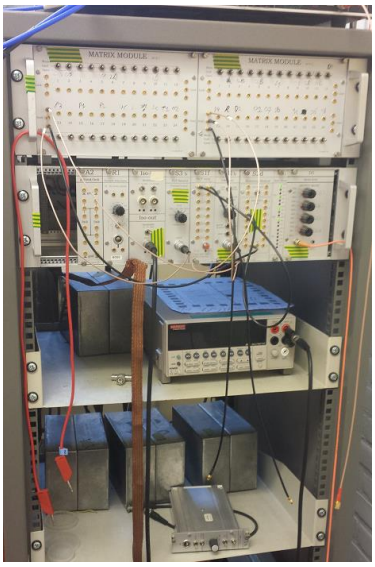

Fig. 2.7 IVVI rack used for the I-V characterization of the MOS capacitors at 4.2 K

[3] This ensures the protection of the measurement equipment from the noise from the PC.

2.4. Conclusions

Both MOS and parallel plate capacitors with a SiO_2 thickness of 30nm were fabricated with the goal of studying their leakage characteristics at cryogenic temperatures. The characterization of the parallel plate capacitors leaves a lot to be desired as it did not provide any useful results due to the probable presence of the pin holes in the oxide. In order to perform the measurements at low temperatures (T = 4.2 K), a die of $1cm^2$ containing several MOS capacitors of 80x80 μm^2 was wire bonded. IVVI rack was used to characterize the MOS capacitors at 4.2 K.

3 Electrical characterization

The previous chapter dealt with the fabrication of MOS and parallel plate capacitors which are used at each of the nodes of the square array. In this chapter electrical characterization of MOS capacitor at room temperature and a temperature of 4.2 K is discussed as well as the electrical characterization of the parallel plate capacitor at room temperature. Chapter 4 will describe the proposed system to provide constant voltages to the gates of a large amount of quantum bits in great detail with the extracted parameters.

The electrical characteristics of the fabricated MOS and parallel plate capacitors have been investigated by the measurements of capacity C and current I as functions of the applied voltage V. The C-V curve study allowed the derivation of the capacitance of the devices, which is a crucial parameter for the successful realization of the biasing system for the Qbits. On the other hand, the I-V characterizations, led to the measurement of the capacitors leakage current at the operational voltages. I-V electrical characterizations were also performed at extremely low temperatures (4.2 K), in order to investigate the leakages of the capacitors in cryogenic environment, which is required for the existence and the proper operation of electronic spin-based Qbits [26], [28], [32], [33].

3.1. Theoretical model of the capacitance for MOS capacitors

For the discussion of the theoretical model describing the C-V characteristics of a MOS structure, the case of an ideal device with a p-type semiconductor will be presented firstly.

A MOS capacitor is considered ideal if [34]:

1. The electron work functions of the metal, ϕ_m and of the semiconductor, ϕ_s are equal under the zero bias condition (Fig. 3.1-a);
2. The charges of the structure are located only in the semiconductor and on the metal surface;
3. No conduction occurs through the oxide (no leakage and break-down).

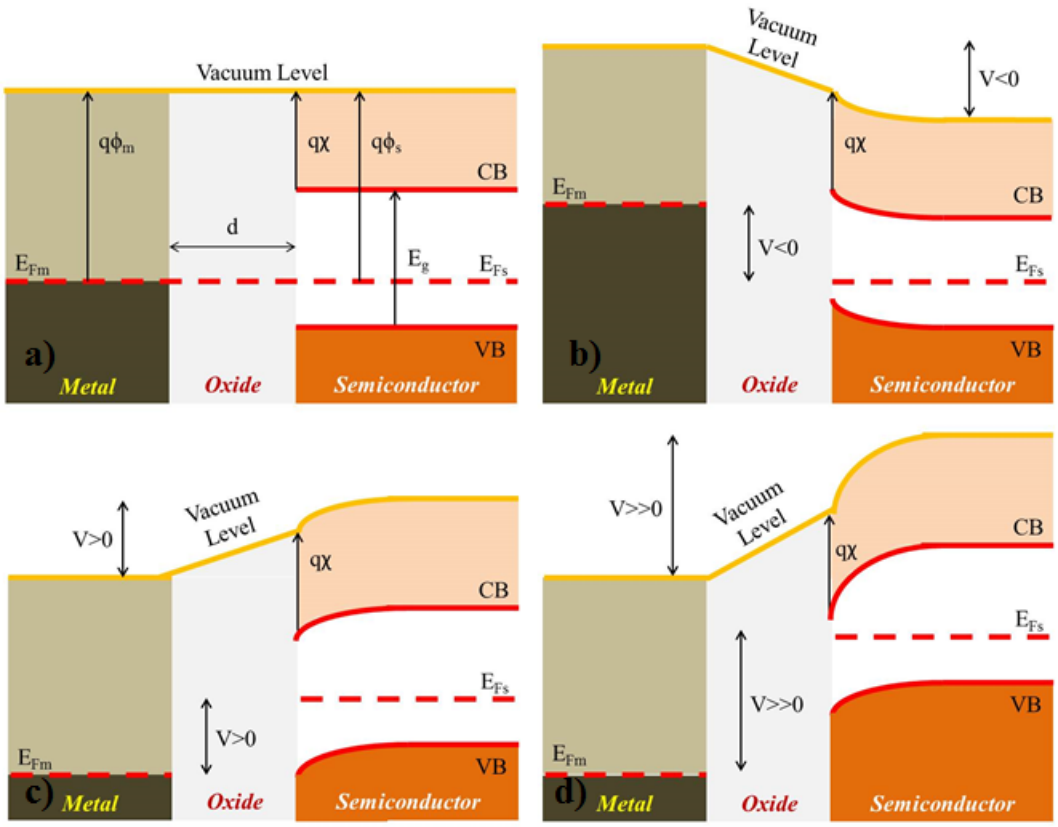

Fig. 3.1 MOS bands diagrams for a) no bias, b) accumulation regime, c) depletion regime and d) inversion regime

If the metal is biased with positive or negative voltages (compared to the p-type semiconductor) three different situations can take place [34]:

1) **Negative tension (V<0).** The Fermi level of the metal E_{Fm} and its vacuum level are raised to a height V from the Fermi level of the semiconductor E_{Fs} and its vacuum level respectively; moreover, since the electron affinity χ and the band gap E_g of the semiconductor are constants, the bands edges are bent upwards. The position of E_{Fs} is, on the contrary, constant from the surface to the interior of the semiconductor because no charge carriers flux occurs through the MOS structure. The bias-induced bands curvature leads the valence band (VB) edge closer to E_{Fs}, thus a higher concentration of holes builds up at the oxide-semiconductor interface, which is counter-balanced by an equal negative charge distribution at the metal-oxide interface. This is the "*accumulation regime"* (Fig. 3.1-b), where the tension V is basically applied only at the oxide edges, therefore the MOS capacity (per unit area) and the applied voltage are related by:

$$C = C_{ox} = \frac{Q_s}{V_0} = \frac{\varepsilon_{ox}}{d} \tag{3.1}$$

,where C_{ox} is the capacity per unit area of the oxide layer, Q_s is the charge per unit area on the semiconductor surface, V_0 is the bias, ε_{ox} is the oxide dielectric constant and d is the oxide film thickness.

2) **Small positive tension (V>0).** In this case the energy bands of the semiconductor are bent downwards, and, close to the oxide-semiconductor interface the valence band edge is farther from E_{Fs}, hence the hole density decreases, leaving a depleted volume with a negative space charge (due to the dopant ions), whose value per unit area is:

$$Q = -qN_A W \tag{3.2}$$

,where q is the elementary charge, N_A is the dopant atoms volume density and W is the depletion region thickness. At the metal-oxide interface an equal positive charge per unit area Q_s is accumulated. This is the "*depletion regime"* (Fig. 3.1-c) and the tension is now applied partly at the oxide edges and partly at the depletion region boundaries according to:

$$V = V_0 + V_s \tag{3.3}$$

,where V is the total bias, V_0 is the tension on the oxide given by eq. (3.1) and V_s is the tension on the depletion region, equal to:

$$V_s = \frac{qN_A W^2}{2\varepsilon_s} \tag{3.4}$$

,where ε_s is the dielectric constant of the semiconductor. The total capacity per unit area of the MOS capacitor in this regime is the series combination of the oxide capacity C_{ox} and the capacity C_d, associated to the depletion region:

$$C = \frac{C_{ox}C_d}{C_{ox} + C_d} \tag{3.5}$$

Combining equations (3.1), (3.3), (3.4) and (3.5) results in the following:

$$\frac{C}{C_{ox}} = \left(\sqrt{1 + \frac{2\varepsilon_{ox}^2 V}{qN_A \varepsilon_s d^2}}\right)^{-1} \tag{3.6}$$

1) **Large positive tension (V>>0).** For larger positive bias, the bands bending is enough to bring, close to the oxide-semiconductor interface, E_{Fs} above the intrinsic Fermi level E_i in the mid-gap. This fact means that $E_{Fs} - E_i > 0$ and the electrons (minority carriers) density surpasses the holes (majority carriers) concentration, leading to a local inversion of population. A superficial charge per unit area Q_n builds up in the semiconductor,

along with the depletion region space charge. In this case the MOS capacitor is in the *"inversion regime"* (Fig. 3.1-d). If the applied voltage is further increased, the concentration of the electrons at the semiconductor surface becomes as large as the dopant atoms density N_A. This is the threshold of the "*strong inversion regime"*, beyond which any bias augmentation leads to the increase of only Q_n (confined within the first 10 nm), keeping the space charge of the depletion region unvaried. In this situation the depletion region reaches its maximum thickness W_m and the associated capacity is fixed to the value $\frac{\varepsilon_s}{W_m}$ for any value of V bigger than the threshold V_T. The capacity per unit area of the MOS capacitor, in the strong inversion regime, assumes its minimum value, equal to:

$$C_m = \frac{\varepsilon_{ox}}{d + \frac{\varepsilon_{ox}}{\varepsilon_s} W_m} \tag{3.7}$$

The C-V characteristics for a MOS capacitor with an n-type substrate have specular behavior.

The capacity C_{ox} of the oxide film in the MOS capacitor, the maximum thickness of the depletion region in the semiconductor W_m and all the parameters that appear in the expressions defined in this ideal MOS model can be measured setting the capacitor at all the three discussed regimes, that is measuring the values of C as a function of a sweeping tension V.

The C-V curve is acquired with a special current meter which applies a sweeping DC bias and a small sinusoidal AC voltage while measuring the capacitive current i_c. The capacitance is indeed calculated from: $C = \frac{i_c}{v\omega}$, where v is the AC tension amplitude and ω its frequency.

In the inversion regime, the electrons density Q_n can increase and decrease according to the AC bias if ω is low (typically below 10^2 Hz) because electrons can be supplied by the slow generation-recombination mechanism or diffusion. Thus, for low frequency measurements, the inversion charged layer behaves as one of the MOS electrodes and the total capacity is C_{ox}. The C-V diagram for an ideal MOS at low frequency (quasi-static) is depicted in Fig. 3.2.

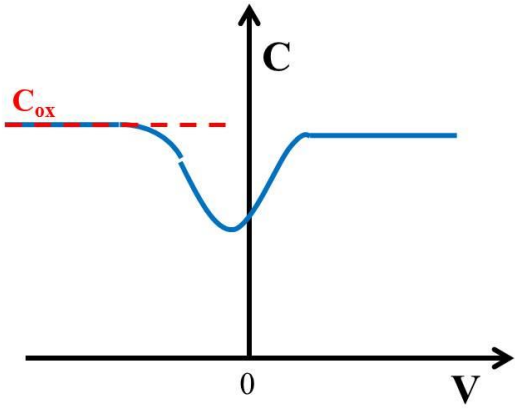

Fig. 3.2 C-V diagram for an ideal MOS capacitor acquired during measurements at a low frequency

When ω is high (typically 10^6 Hz), Q_n cannot respond to the AC signal and remains constant at its DC value, while only the depletion region thickness W expands and contracts slightly around the maximum value W_m. As a consequence, the measured MOS capacity is equal to eq. 3.7) for strong inversion regime. At high measurement frequencies the C-V appear as reported in Fig. 3.3.

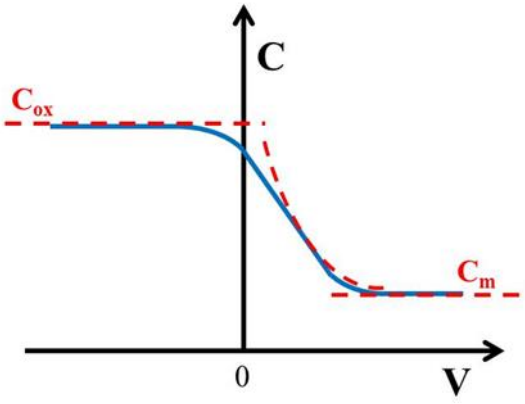

Fig. 3.3 C-V diagram for an ideal MOS capacitor, where the fitting curves given by eq. 1), 6) and 7) are portrayed by the red dotted lines

For a real MOS the electron work functions ϕ_m and ϕ_s are not equal under the zero bias condition, In particular it always happens that the difference $\phi_m - \phi_s$ is negative. For zero bias condition, the Fermi level through all the structure has to be constant (thermodynamic equilibrium), thus the bands of the semiconductor bend downwards, leading the capacitor in the depletion regime [34]. As a consequence the C-V curve will be rigidly translated to negative voltages of the quantity $V_{wf} = \phi_m - \phi_s$.

Moreover, the oxide could contain some charged defects, whose quantity does not depend on the applied voltage. Specifically, they are fixed charges, mobile trapped charges and mobile free charges [34]. Fixed charges are positive and their distribution and amount depend on the oxide growth conditions, while mobile trapped charges are associated to the defects of the oxide generated by ions or electrons bombardment. Mobile free charges are Na^+ and the other alkali ions, whose origin is related to former contamination of the semiconductor surface.

Taking into account the discussed difference in the work functions and the charges in the oxide, the C-V is translated towards negative voltages by:

$$V_t = V_{wf} - V_D \tag{3.8}$$

The semiconductor-oxide interface can contain trapped charges, which are also positive but their density depends on the applied bias. Therefore the C-V curve not only is translated to negative voltages, but has also a distorted slope in the depletion regime (smearing out) [34].

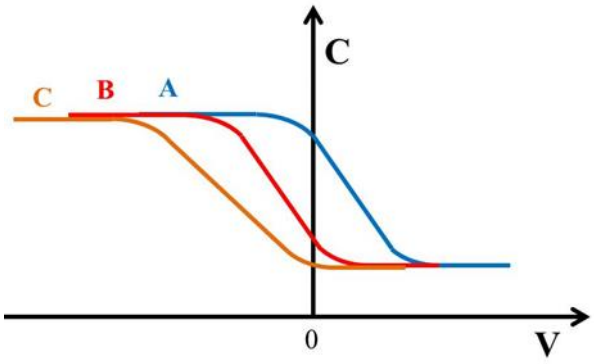

Fig. 3.4 C-V diagrams for (A) an ideal MOS capacitor, (B) a real MOS capacitor without charges at the semiconductor-oxide interface and (C) a real MOS capacitor with charges both in the oxide and interface

3.2. Room temperature C-V measurements of the MOS capacitors

The C-V characteristics of the fabricated MOS capacitors have been acquired employing a *Cascade Microtech* probe station connected with a *Hewlett Packard 4284A 20 Hz-100 MHz Precision* L-C-R Meter (Fig. 3.5). The voltage applied to the MOS capacitors has been a superposition of a continuous (DC) and alternate (AC) components. The DC part has been swept from -10 V to 10 V, while the AC part has been set with amplitude equal to 500 mV (small signal analysis regime) and frequencies of 100 Hz and 1 MHz for low and high frequency measurements respectively.

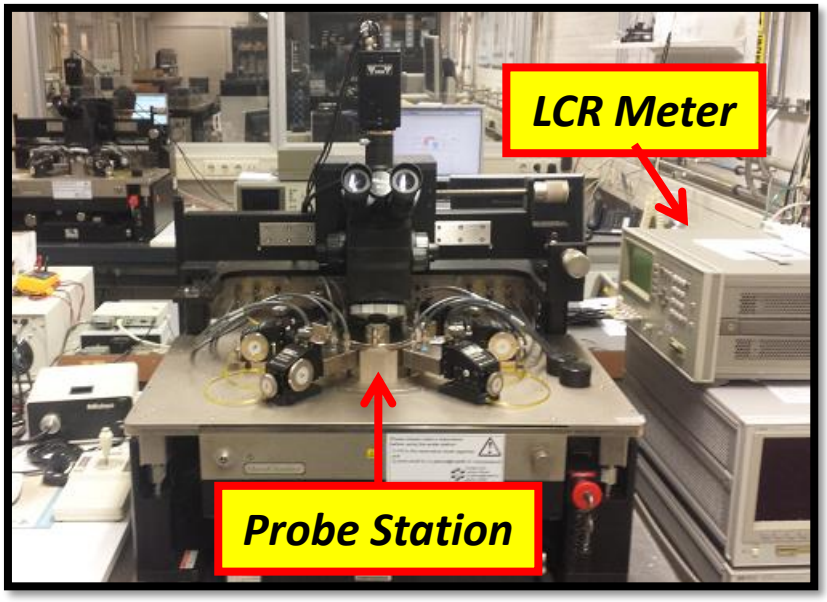

Fig. 3.5 Experimental set-up employed for the electrical characterization of the capacitors

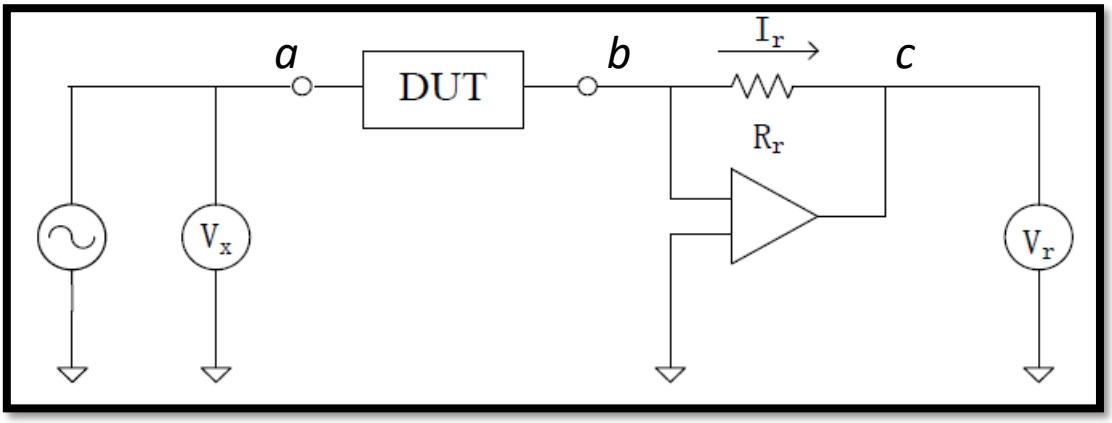

Fig. 3.6 Simplified circuit scheme for the L-C-R meter

The L-C-R meter circuitry is sketched in Fig. 3.6. *DUT* is the device under test and the operational amplifier of the L-C-R meter is set at negative feedback configuration, thus the node *b* in the figure is at "virtual ground". This allows for the voltmeter V_x to measure the voltage across the device directly. The current I_r is calculated by dividing the measured bias V_r and the known resistance R_r (assumed ideal). The complex impedance Z of the device is simply the ratio between V_x and I_r and the capacity is equal to the imaginary part of Z.

The C-V curve acquired at high frequency (HF) for the Al MOS capacitors with an area of 80x80 μm^2 is showed in Fig. 3.7.

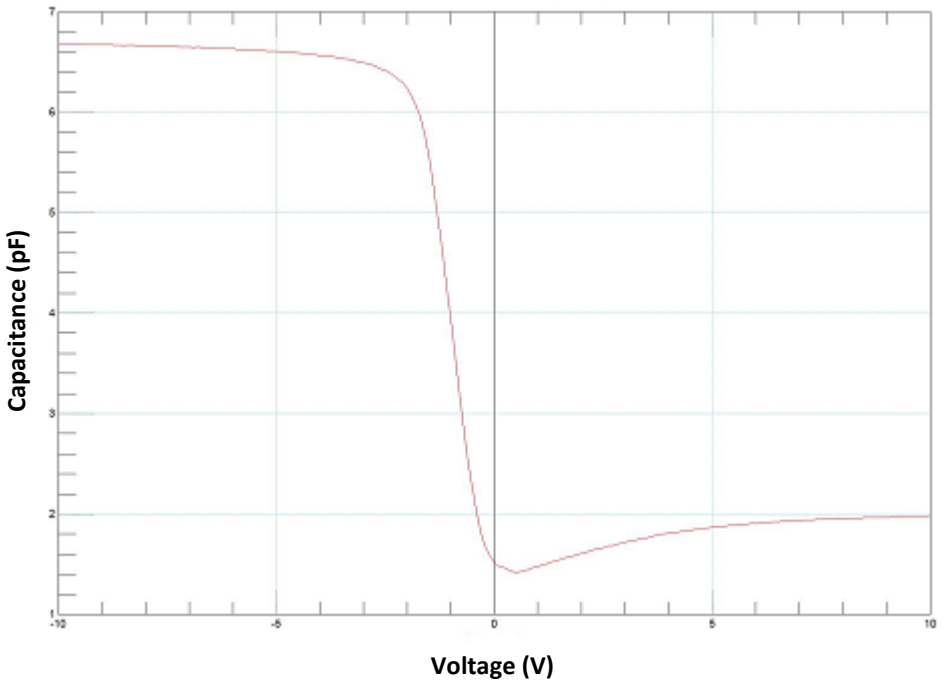

Fig. 3.7 C-V curve taken at HF for the 80x80 µm² Al MOS capacitors

When operating in the accumulation regime (-10 V < bias < -2 V), the capacitance of the MOS is 6.6 pF and according to eq. (3.1) is expected to be equal to $\frac{\varepsilon_{ox}}{d}$. Since the oxide thickness has been previously measured (around 30 nm), the dielectric constant of the grown oxide is 4.0, which is very close to the typical values for thermal grown SiO_2 (3.9) [35], [36].

The depletion regime starts at negative bias (around -2 V) because of the difference in the work functions of the Al contact and the p-type Si and due to the presence of charges in the oxide and interface. The Boron concentration in the used p-type Si wafer is 10^{15} - 10^{16} cm^{-3} and the work function of Al is 4.1 eV [34], therefore of this -2 V shift, -0.9 V accounts for the Al and Si work functions difference [34]. The remaining -1.1 V is related to the presence of charged defects and contaminants distributed in the oxide (created mostly during Al film sputtering deposition) and interface. In the strong inversion regime the minimum capacitance is 1.8 pF. According to eq. (3.7) the maximal depletion region thickness W_m is 0.4 µm. This value is expected for a dopant concentration of 10^{15} - 10^{16} cm^{-3} [34].

The C-V curve taken at low frequency (LF) for the same capacitors is shown in Fig. 3.8.

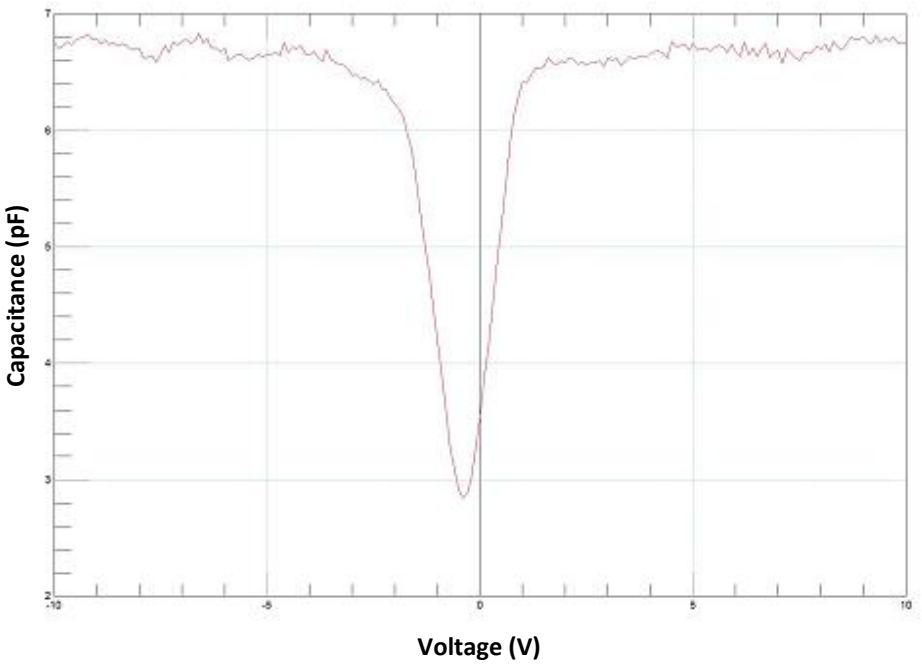

Fig. 3.8 C-V curve taken at LF for the 80x80 µm² Al MOS devices

As mentioned in chapter 1, each quantum bit will be confined by a voltage of around 1 V. It is clear from the CV-curves in Fig. 3.8 that this might become a problem: at this bias voltage the capacitance is strongly dependent on the voltage applied. According to eq. 3.8 this problem can be solved in one of the two following ways: decrease the work function by changing the material employed for the electrode (n^+ poly instead of aluminum) or increase the dopant concentration of the semiconductor part of the MOS capacitor. The first solution will ensure the decrease of V_{wf} and therefore result in a shift of the C-V curve, as displayed in Fig. 3.8, to the left. The second solution will cause an increase of V_D and also result in a shift of the C-V curve to the left. [34].

As predicted by the theoretical model, the capacitance in the accumulation and strong inversion regimes in Fig. 3.8 is equal to the oxide capacitance, 6.6 pF. In the depletion regime, the charged defects at the oxide-silicon interface contribute in a different manner to the HF and LF C-V curves. Specifically, this fact is evidenced by a difference in the HF and LF C-V curves slope. It is possible to derive the density of the interface states using the following formula [37]:

$$D_{it} = \frac{\frac{C_{LF}C_{ox}}{C_{ox}-C_{LF}} - \frac{C_{HF}C_{ox}}{C_{ox}-C_{HF}}}{qA} \tag{3.9}$$

,where C_{LF} and C_{HF} are, respectively, the capacities at low and high frequency, C_{ox} is the oxide capacity, q the elementary charge and A the MOS capacitor area. In this case the density of the defects appeared to be equal to $1.26 \cdot 10^{11}$ cm^{-2}.

Low and high frequency C-V curves have also been acquired for the Al MOS capacitors with areas of 250x250 μm^2 and 700x700 μm^2.

The properties obtained by the room temperature C-V diagrams for all the Al MOS capacitors are reported in Tab. 3.1.

Tab. 3.1 Parameters extracted from the HF and LF C-V curves of the 80x80, 250x250 and 700x700 μm^2 Al MOS capacitors

Al MOS capacitor Area (μm^2)	**80x80**	**250x250**	**700x700**
C oxide (pF)	*6.6*	*60*	*540*
Oxide dielectric constant	*4.0*	*3.7*	*4.3*
C-V curve shift (V)	*-2*	*-2*	*-2*
Interface defects density (cm^{-2})	*$1.26 \cdot 10^{11}$*	*$2.72 \cdot 10^{11}$*	*$2.51 \cdot 10^{11}$*

3.3. Room temperature I-V measurements of the MOS capacitors

The I-V characteristics of the fabricated MOS capacitors have been acquired at room temperature. In this case, the voltage applied to the MOS capacitors has been only continuous (DC). The I-V curves for the 80x80, 250x250 and 700x700 μm^2 Al MOS capacitors at room temperature have been acquired sweeping the voltages from -1 V to 1 V (Fig. 3.9)

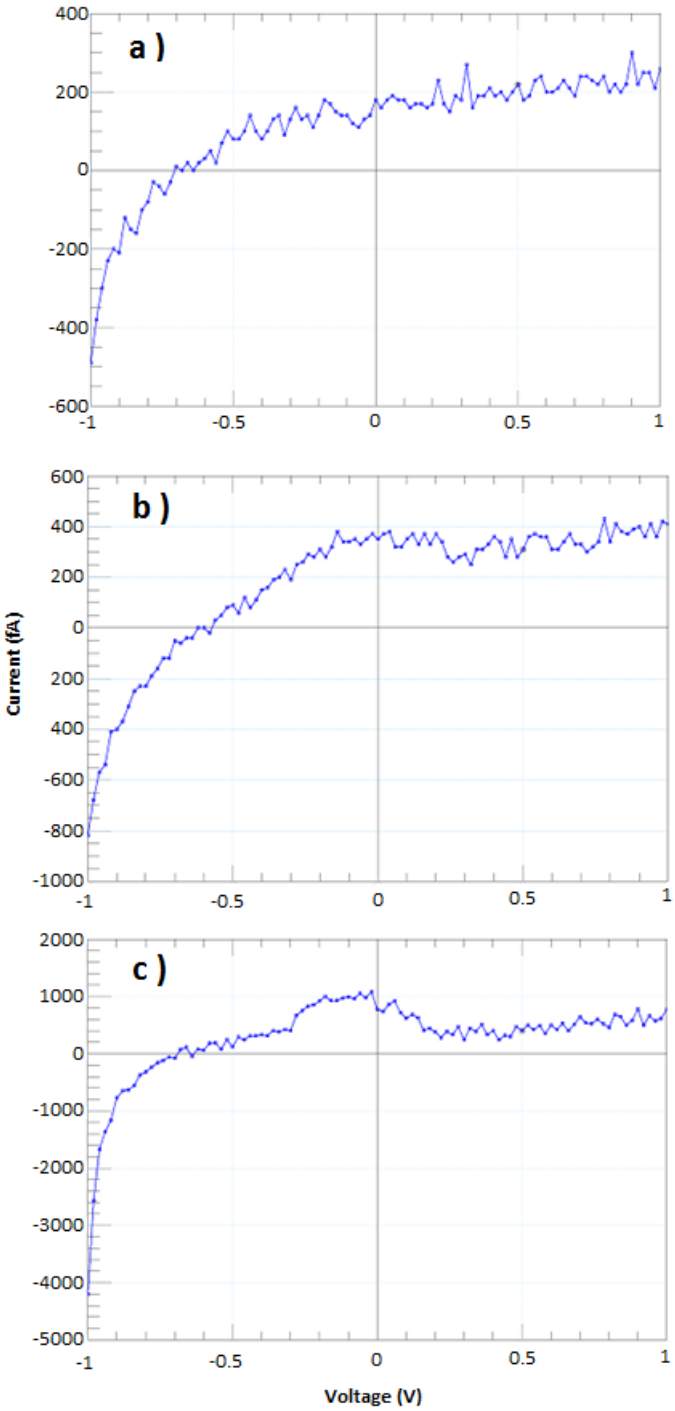

Fig. 3.9 I-V curves taken from -1 V to 1 V for the a) 80x80 µm^2, b) 250x250 µm^2 and c) 700x700 µm^2 Al MOS capacitors

It is clear from Fig. 3.9 that the leakage currents of the capacitors increase with an increasing applied negative bias voltage. This is due to the fact that the MOS capacitors are in the inversion region at that point. When the MOS capacitor is operating in this particular region the charge per unit area of the inversion layer and therefore the leakage current increase.

Since no current should flow for zero applied voltage, it is evident that for all the acquired curves there is an offset. This shift may be caused by the charging of the capacitors and the intrinsic offset of the measurement equipment.

The leakage current ranges at room temperature between -1 V and 1 V for the Al MOS capacitors are reported in Tab. 3.2.

Tab. 3.2 Leakage current between -1V and 1V measured for all the Al MOS capacitors

SAMPLE	CURRENT AT (-1V-1V) [pA]	CURRENT DENSITY AT (-1V – 1V) [nA/cm^2]
80x80 µm^2	*-0.5 - 0.25*	*-7.8 - 3.9*
250x250 µm^2	*-0.81 - 0.4*	*-1.3 - 0.6*
700x700 µm^2	*-4.2 - 0.8*	*-0.8 - 0.2*

The leakage current range widens as the area of the MOS becomes larger. However, the range of the current density decreases, thus the current increase is merely a geometric effect and not a sign of structural degradation of the larger devices.

The values of the resistance associated to the MOS capacitors are finally shown in Tab. 3.3.

Tab. 3.3 Values of the resistance associated with the MOS capacitors

SAMPLE	RESISTIVITY AT (-1V – 1V) [PΩcm]
80x80 µm^2	*5.7*
250x250 µm^2	*34.4*
700x700 µm^2	*65.3*

One can see from Tab. 3.3 that the resistivity of the three different MOS capacitors does not vary by a large order of magnitude which was to be expected as all the three structures are made of the same materials. These values of the resistivity are comparable to ones perceived at some

companies [38]. These resistivity values affect the discharge time of the MOS capacitors when a certain voltage between -1 V and 1 V will be stored, which will be discussed in chapter 4.

3.4. Low temperature I-V measurements of the MOS capacitors

The cryogenic I-V measurements were performed for the 80x80 μm^2 MOS capacitors at a temperature of 4.2 K, reached by means of a He^4 refrigerator (Fig. 3.10).

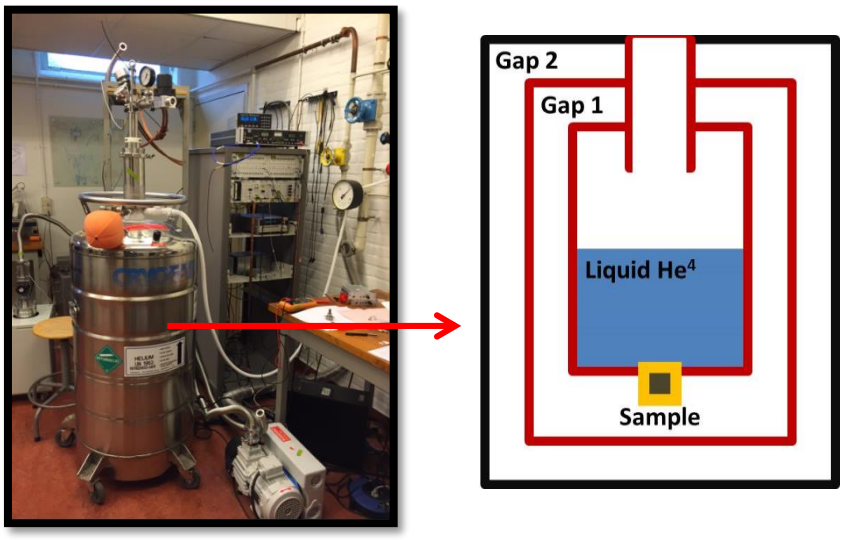

Fig. 3.10 Set-up used for the I-V measurements at 4.2 K and its main internal structure

The refrigerator brings a specific sample to 4.2 K by putting it in thermal contact to a reservoir of liquid He^4 (boiling temperature 4.2 K). To keep the liquid He^4 below its boiling temperature, the container where it is poured is thermally insulated from the environment by three walls and 2 gaps. The outermost gap is pumped out to low pressure ($\approx 10^{-7}$ Torr) to prevent heat exchange through convection and conduction. Moreover, the innermost walls have Mylar multilayers, which hinder the radiative heat flux.

The leakage current has been measured between -10 V and 10 V (Fig. 3.11). Its value ranges from only -0.5 pA to 0.05 pA, but the curve is not symmetric around the origin and there is an offset of -0.2 pA. As noticed for the room temperature measurements, the offset is caused by the measuring equipment. This offset makes it difficult to observe the actual leakage current caused by free charge carriers tunneling through the oxide (Fowler-Nordheim) [34]. At 4.2 K, the leakage current is expected to be lower, because the free charge carriers available for tunneling are mostly frozen.

Since the MOS capacitor consists of three different materials (aluminum, silicon dioxide, and silicon), all of which have different coefficients of thermal expansion [39], [40], formation of

cracks at cryogenic temperatures was a distinct possibility. Such cracks would have led to an increase of the leakage current at 4.2 K. However, there is no such increase to be witnessed from Fig. 3.11 which implies that the MOS capacitor did not undergo any mechanical damage at the cryogenic temperature.

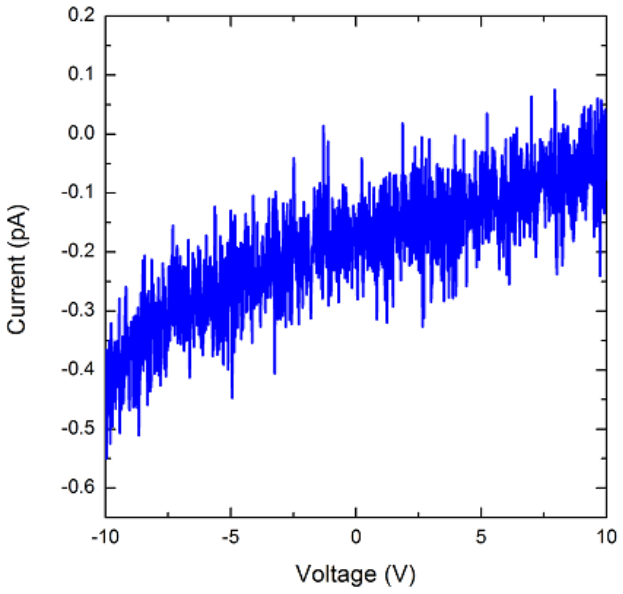

Fig. 3.11 I-V curve from -10 V to 10 V for the 80x80 µm² Al MOS capacitors at 4.2 K

3.5. Room temperature C-V measurements of the parallel plate capacitors

During the C-V characterization of these capacitors no correct curves could be acquired. The main reason can be the short-circuits caused by the presence of pin-holes in the thin oxide layer. Such defects are faults of the fabrication process which can easily occur for very thin oxide films.

3.6. Conclusions

C-V and I-V characterizations of the MOS capacitors were performed. Leakage currents at room temperature and at a temperature of 4.2 K of the MOS capacitors were derived. The resistivity of the MOS structures was calculated and appears to be in conjunction with the findings at a company. The structures did not undergo any mechanical damage when exposed to the cryogenic environment.

4 Qbits bias circuitry design and analysis

In the previous chapter electrical characterization of a MOS and a parallel plate capacitor was discussed. In this chapter, every component of the circuitry designed to provide confinement voltage to the gate of each Qbits/QDs will be described. A detailed overview of the circuitry is depicted in Fig. 4.1. It basically consists of analogic and digital sections. The analogic part includes the matrix with the capacitors, the transistors and the QDs, while the digital part contains the storage memories (RAM), the controller, the clock (CLK), the pulse width modulator (PWM) and the two demultiplexers (Demux). Firstly, the QDs matrix circuit will be described after which a stability, areal scalability and power consumption analysis of it will be performed. Then the procedure concerning the voltages of the transistor gates will be elaborated on. After that detailed descriptions of demultiplexers, pulse width modulator, controller and memory elements respectively will be given. The chapter will end with a conclusion.

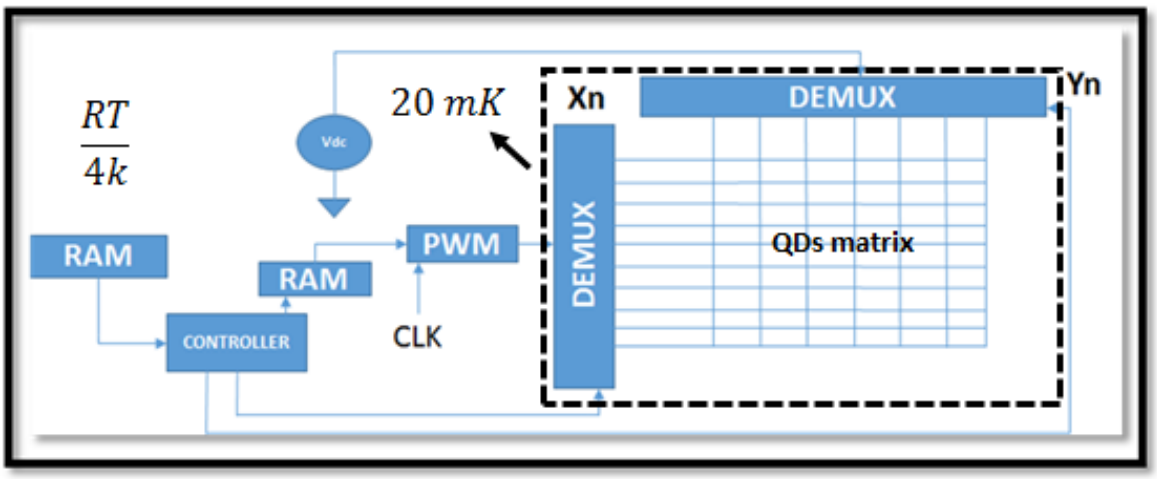

Fig. 4.1 Detailed overview of the circuitry to provide confinement voltages to the gate of each qubit

Since the confinement of the electron in the QD strictly requires a bias variance of maximum ± 5 μV, along with the design of the circuit, an analysis of the stability of the transistor-RC circuit directly biasing each QD has been performed. In particular, the stability against the random variations of the DC voltage applied to the whole array, of the transistor switching modulation time and of the residual voltage stored in the capacitor have been studied.

4.1. QDs matrix circuit

Each point of the matrix consists of the small analog circuit shown in Fig. 4.2.

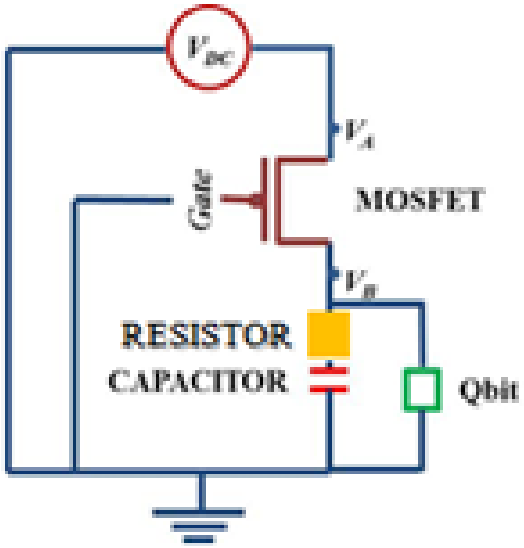

Fig. 4.2 Small analog circuit at each point of the QDs matrix

The confinement voltage for the Qbit is applied by the capacitor connected in parallel. This small capacitor can be either a metal-oxide-semiconductor (MOS) capacitor or a parallel plate capacitor. Both devices can indeed be easily fabricated and integrated on a large scale.

The instantaneous voltage difference V(t') between the electrodes of the capacitor is related to the stored charge Q(t'). The stored charge is provided by the external DC bias, V_{DC}, to which every capacitor of the matrix is connected through the transistor switch. When V(t') is lower than V_{DC} and the transistor allows the current to flow, the capacitor accumulates charge and increases its voltage according to:

$$V\,(t) = [V(t') - V_{DC}]e^{-(t-t')/RC} + V_{DC};\ for\ t > t' \tag{4.1}$$

, where R is the resistance connected in series with the capacitor and includes the resistance of the transistor channel and of the resistor next to it.

The increase of the capacitor voltage halts when the transistor switch interrupts the current flux. For this design, the interruption is forced as V(t) reaches the confinement voltage V_{QD} at time t_c.

After the interruption of the charging, the capacitor voltage spontaneously decreases due to the current leakage through the dielectric layer of the capacitor. The discharging voltage is described by the following formula:

$$V\,(t) = V_{QD} \cdot e^{-(t-t_c)/R_{ox}C};\ for\ t > t_c \tag{4.2}$$

, where R_{ox} is the resistance of the oxide film between the capacitor electrodes.

In order to have uninterrupted electron confinement in the QD, V(t) must be equal to $V_{QD} \pm 5$ μV at any time. This specifically means that during the capacitor charging: $V(t) \leq V_{QD} + 5$ μV, while during the leakage discharge: $V(t) \geq V_{QD} - 5$ μV. When the capacitor voltage becomes approximately equal to $V_{QD} - 5$ μV, after the discharging time t_d, the transistor switch commutes again to the conductive state, triggering the capacitor charging (described by eq. 4.1).

The whole time evolution of V(t), driven by the transistor switch commutation between the open and closed states, is shown in Fig. 4.3.

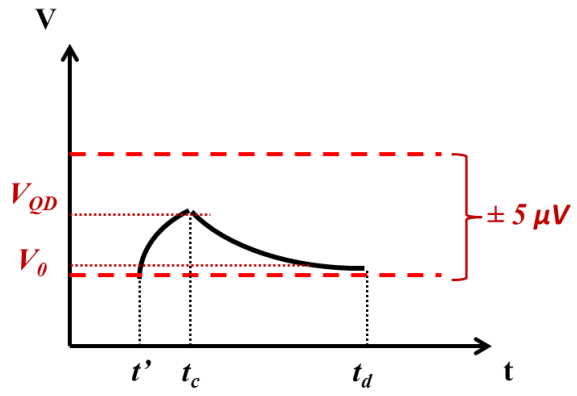

Fig. 4.3 Time evolution of V(t) driven by the transistor switch commutation

The transistor switch is in the conductive mode between t' and t_c, for a duration of $T = t_c - t'$. On the other hand, it stays in the non-conductive mode for a period $T' = t_d - t_c$. The commutation of a transistor switch is driven by the voltage $V_G(t)$ applied to its gate electrode. Considering an n-type channel transistor and the circuit in Fig. 4.2, the whole channel is in conduction mode if:

$$\begin{cases} V_G - V_A > V_T \\ V_G - V_B > V_T \end{cases} \tag{4.3}$$

V_T is the characteristic transistor threshold voltage, and is generally equal to 0.7 V. The transistor is surely in an on-state for $V_G = 3$ V. On the other hand, the MOSFET does not allow current flow in the channel if:

$$\begin{cases} V_G - V_A < V_T \\ V_G - V_B < V_T \end{cases} \tag{4.4}$$

This conditions occur if, for instance, V_G is 0 V.

For the required commutation, $V_G(t)$ has to be a cyclic square-wave (Fig. 4.4).

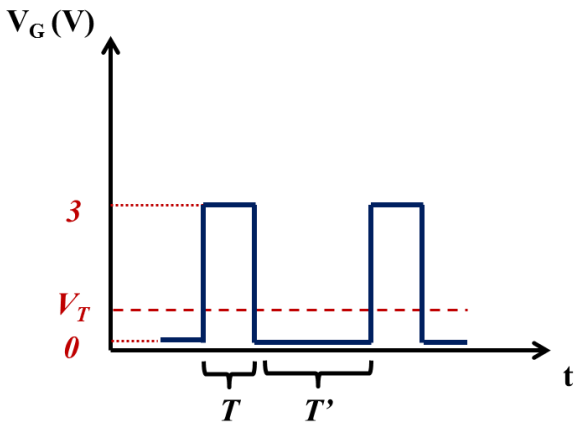

Fig. 4.4 A graphical representation of $V_G(t)$

MOSFET with n-type channel would be preferred over p-type channel transistor since the mobility of the electrons in c-Si is greater than the mobility of the holes. As a consequence, the commutation of channel state is faster for a n-channel MOSFET.

Since V_{QD} depends on the QD characteristics and V_{DC} is the same for the whole matrix, each transistor has to operate with different charging and discharging periods T and T', thus with a specific time modulation of $V_G(t)$. The time modulated $V_G(t)$ for the transistor located in the node Xn-Ym is addressed through the gate lines of the matrix by the demultiplexers. These voltage signals are elaborated by the digital components described in the next paragraphs.

4.2. Switching speed analysis

For a quantitative analysis of the designed matrix-node functioning, the following parameters have been considered:

Tab. 4.1 Parameters employed during the quantitative analysis of the QDs matrix

R	C	V_{DC}	V_{QD}	ΔV_{QD}
$10^9\ \Omega$	6.6 pF	2 V	1 V	± 5 μV

The high value for the resistance was chosen in order to make sure that the time that it takes for the capacitor to charge to V_{QD} (T) is not too short. This charging time is related to the amount of charge stored on the capacitor and the current flowing through it by means of the following relationship:

$$Q = I\Delta t \tag{4.5}$$

Q , on the other hand, is related to voltage across the capacitor and its capacitance by means of the following relationship:

$$Q = CV_{QD} \tag{4.6}$$

, where C represents the voltage across the capacitor and C its capacitance.

I is related to the source voltage (V_{DC}), the resistor of the circuit (see Fig. 4.2) and the capacitance of the capacitor in the following way:

$$I = \frac{V_{DC}}{R} e^{-\frac{t}{RC}} \tag{4.7}$$

Using the values of C and V_{QD} from Tab. 4.1 in conjunction with eq. 4.6, results into Q being equal to $6.6*10^{-12}$ C. In order to achieve a charging time of the capacitor in the ns range, a resistor in the GΩ range needs to be employed. It is also possible to estimate the amount of electrons that should be "put" on the capacitor to charge it to the desired value of V_{QD} by means of the following relation:

$$N = \frac{C(V_{QD} - V_0)}{e} \tag{4.8}$$

, where N represents the amount of electrons and e represents the elementary charge (~ $1.60*10^{-19}$ C) and V_0 represents the voltage across the capacitor after the first discharging process.

Substituting all the necessary values into eq. 4.8 reveals that around 165 electrons are needed to increase the voltage across the capacitor by a value of 4 µV.

Assuming that the initial bias in the capacitor V_0 is V_{QD} – 4 µV, the following relation can be employed to calculate the charging period T:

$$t = -RC \ln\left(\frac{V_{QD}(t) - V_{DC}}{V_0(t) - V_{DC}}\right) \tag{4.9}$$

Using eq. 4.9 and substituting all the necessary parameters results in a charging period T of 26 ns to charge the capacitor to 1 V. In other words, the transistor has to stay in the conductive mode for 26 ns. This time corresponds to a switching frequency of 38 MHz, which can be realized by a MOS transistor with a channel length of 10 µm. If the value for capacitor oxide resistance of 2.67 TΩ of a 80 um x 80 um MOS capacitor is used and assuming that the current

is zero when the transistor is off, it is possible to derive the time in which the capacitor bias drops from V_{QD} to V_{QD} – 4 μV by means of the following:

$$t = -RC \ln\left(\frac{V_0(t)}{V_{QD}(t)}\right) \tag{4.10}$$

Using eq. 4.10 and substituting all the necessary parameters results in a discharging time of 70.5 us, when the transistor is in non-conductive mode. This is the discharging period T' (and thus the time after which the refreshing action should take place), as mentioned above.

4.3. Areal scalability analysis

Suppose that one would like to implement the entire QDs matrix and two demultiplexers on a die of 1 cm^2. Lets begin by considering the area taken by a single element of the QDs matrix first. The estimated area of a quantum dot is equal to ~ $2.40*10^{-8}$ cm^2 [1]. Let us consider a high performance MOSFET with a physical gate length of 13 nm [41]. Assuming that the source and the drain of the MOSFET combined are about 52 nm and the $\frac{W}{L}$ ratio is 1.5 [42], the MOSFET will occupy an area of ~ $2*10^{-11}$ cm^2. The area of the 80x80 μm^2 MOS capacitor is $6.4*10^{-5}$ cm^2. If one considers a die doped with $N_a = 1*10^{14}$, one will be dealing with a resistivity of ~ 100 Ωcm [43]. Considering the value of 1 GΩ being employed for resistance during the stability analysis and assuming the thickness of the resistor to be 100 nm, it appears that the ratio $\frac{L}{W}$ should be equal to 100. An assumption was made for the width of the resistor to be 10 μm and its length to be 1000 μm. This results into the resistor occupying an area of ~ $1*10^{-4}$ cm^2. Assuming a wire with a length of 500 μm and a width of 1 μm (due to the skin-effect-induced increase in resistance as a function of frequency) [42], the area of the die occupied by the wiring in between the component of each of the elements of the QDs matrix is ~ $5*10^{-6}$ cm^2. Thus the total area occupied by all the components of a single element of the QDs matrix ~ $1.69*10^{-4}$ cm^2. Naturally, 768 of these will occupy a space of ~ 0.39 cm^2 which is around 40 % of the available die area. However, in this case it is assumed that all the elements are packed closely together, which cannot be allowed to enable proper functioning of the circuit. Suppose that all the elements of the QDs matrix as well as sufficient space between them take up a space of around 50 % of the die. This leaves around 50 % for the implementation of the two demultiplexers. As the amount of transistors required to employ both demultiplexers is 1368, 0.5 cm^2 should be more than sufficient for this purpose. Fig. 4.5 represents an overview of the placement of components of a single element of the QDs matrix on a chip.

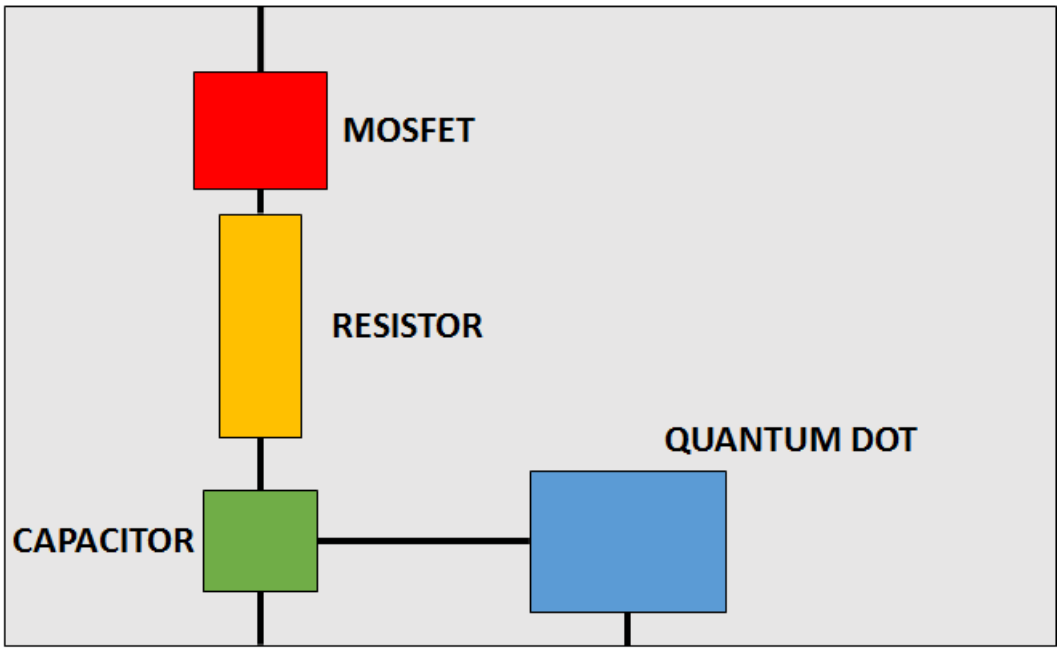

Figure 4.5: Overview of the placement of components of a single element of the QDs matrix on a chip

4.4. Power consumption scalability analysis

If once again the assumption is made (as in section 4.2) that the current is zero when the transistor is off, only the charging part of the cycle needs to be considered during the analysis of power consumption.

The power consumption in an electrical circuit can be derived by employing the following relationship:

$$P(t) = I(t)^2 R \tag{4.11}$$

, where P(t) represents the power consumption, I(t) represents the current flowing through the circuit and R represents the total resistance of the circuit.

When one substitutes eq. 4.7 in eq. 4.11, the following relation is the result:

$$P(t) = \frac{{V_{DC}}^2}{R} e^{-\frac{2t}{RC}} \tag{4.12}$$

In order to derive the average power consumption of a single element of the QDs matrix one needs to integrate eq. 4.12 over the time that the MOSFET is on and divide that result by the charging time, or in equation form:

$$\bar{P} = \frac{\int_{t\prime}^{tc} \frac{{V_{DC}}^2}{R} e^{-\frac{2t}{RC}} dt}{T} \tag{4.13}$$

, where t_c represents the time that it takes for the voltage across the capacitor to reach the value of V_0 and t' represents the time at which voltage across the capacitor has reached a value of 1 V (V_{QD}).

Solving eq. 4.13 result into an average power consumption of ~ 1 nW per period of $V_G(t)$. This implies that the average power consumption of the entire QDs array is ~ 2.3 µW. This value is comparable to the value caused by the thermal flux in case of using a single cable. As at least two cables will surely be employed in the entire design (to connect the V_{dc} to the one of the demultiplexers (DM_c) and pulse width modulator to the other (DM_r)), the power consumption of the QDs array seems to be of a reasonable value.

4.5. Stability analysis of the Qbits matrix-node circuit

The stability of the described circuit (Fig. 4.2) is the property that enables this system to continue providing the proper V_{QD} in the event of the deviation of some of its parameters. The random parameter variations that could occur are δV_{DC} (power supply noise), δT (transistor commutation faults) and δV_0 (deviation of the initial capacitor bias). In order to have a stable system during the capacitor charging, the capacitor bias must lay within $V_{QD} \pm 5$ µV, despite the casual occurrence of δV_{DC}, δT and δV_0. These deviations in general are not correlated to each other and can randomly be, at any time, null, negative or positive.

The partial derivatives $\partial V/\partial t$, $\partial V/\partial V_{DC}$ and $\partial V/\partial V_0$ of the capacitor bias V given by eq. 4.1 are positive around $V = V_{QD}$, hence the highest deviations $|V - V_{QD}|$ take place when δV_{DC}, δT and δV_0 are all positive or all negative. The quantity $|V - V_{QD}|$ is less than 5 µV (the QD is still properly biased) if the highest $|\delta V_{DC}|$, $|\delta T|$ and $|\delta V_0|$ are:

Tab. 4.2 Absolute values of the random variations of V_{DC}, T and V_0

$\|\delta V_{DC}\|$	$\|\delta T\|$	$\|\delta V_0\|$
0.5 V	*5 ns*	*1 µV*

4.6. Demultiplexers and controller circuits

As stated in paragraph 4.1, each transistor gate voltage has to be a square-wave with period $T_n + T'_n$ and duty cycle T_n. The time constants T_n and T'_n depend on the bias voltages V_{QDn} required by the n^{th} Qbit/QD in the matrix. The different V_{QDn} have to be stored and accessed fast by the system in order to calculate the corresponding T_n and T'_n and generate the proper

V_{Gn} (t) signals. The generated V_{Gn}(t) signals then have to be addressed to the respective MOSFETs. This coordinated set of operations is performed by the digital part of the designed circuitry and can be resumed as follows:

1. Encoding of confinement voltages V_{QDn} into binary values and storing them in one RAM memory;
2. Reading of the V_{QDn} and translation of it into the corresponding charging and discharging times T_n and T'_n by a controller unit;
3. Generation of the square-wave V_{Gn} signals by the combined operations of a clock and a pulse width modulator (PWM) according to the inputs sent by the controller;
4. Addressing of the V_{Gn} signals to the relative QDs matrix nodes performed by two demultiplexers.

Every digital component involved for this task is described in detail in the following paragraphs.

Demultiplexers

A demultiplexer is basically a device which receives a single input and connects it to one of the M given outputs. This operation needs also the use of an external control signal, indeed only a certain output is connected at a time depending on the value of the control signal.

For the proposed circuit, which should operate at 20 mK, two demultiplexers are employed because one addresses the rows of the QDs matrix (DM_r) and the other one the columns (DM_c). The conceived QDs matrix is a square of 48x48 nodes, thus DM_r and DM_c must connect 48 outputs. For each capacitor refreshing cycle, firstly DM_c receives a control signal from the controller unit and uses this information to connect the V_{DC} to a specific column. Subsequently DM_r receives the V_{Gn}(t) signal from the PWM unit and addresses it to the specific MOSFET in the column selected by DM_c. This signal, for T_n seconds, turns on the transistor which allows the flux of current from the V_{DC} node to the n^{th} capacitor (Fig. 4.6).

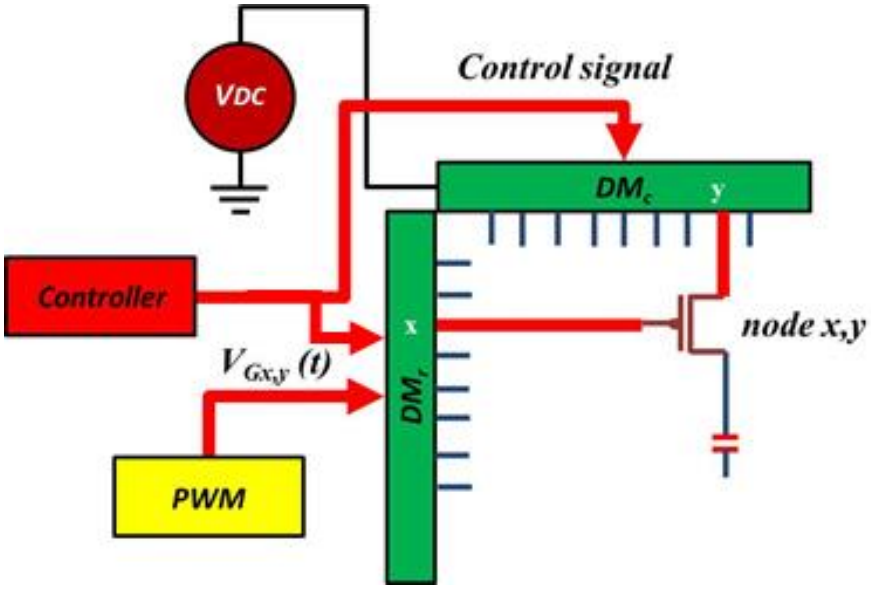

Fig. 4.6 A graphical overview of the functioning of the two demultiplexers

Pulse width modulator

The PWM unit generates the $V_{Gn}(t)$ signals. In particular, it acts on the duty cycle T_n and the period $T_n + T'_n$ of the signal. Since the Qbits in the matrix are 768, in principle the PWM unit should produce and deliver 2304 $V_{Gn}(t)$ signals with different T_n and T'_n (Fig. 4.7). This operation is fulfilled as follows:

1. The PWM unit reads the T_n and T'_n values from a dedicated dual-port RAM;
2. The PWM receives a base low-high clock signal;
3. The PWM modulates the received clock signal into the $V_{Gn}(t)$ signal with duty cycle T_n and period $T_n + T'_n$. According to the analysis of the first subsection of this chapter the duty cycle T_n is equal to 26 ns while the period $T_n + T'_n$ is equal to 70.5 us.

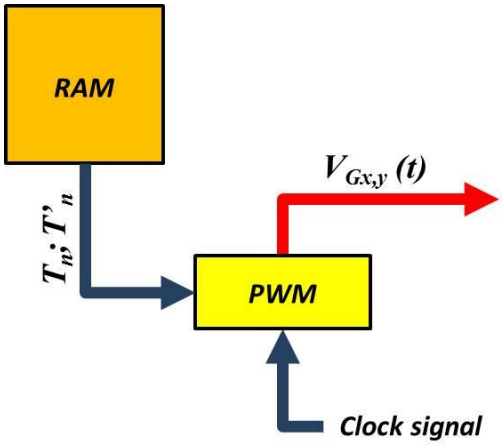

Fig. 4.7 A graphical overview of the functioning of the pulse width modulator

Controller

The controller unit coordinates all the system actions and performs the calculation of the time constants T_n and T'_n. The time constants are extrapolated by the V_{QDn} read from a dedicated memory (RAM_1). Then T_n and T'_n are written into the second memory (RAM_2) to be available for the PWM. Moreover, the controller unit sends control signals to DM_r and DM_c to coordinate their addressing operations.

Memory elements

The 2304 V_{QDn} are stored in RAM_1. According to the QD fabrication characteristics, each confinement voltage can assume a value within the 0 V-1 V range with a maximum variance ΔV_{QD} equal to ±5uV. This variance consists in the resolution of the numerical value of V_{QDn}. The number N of bits needed to encode a V_{QDn} is given by the following equation:

$$R = \frac{V_r}{2^N} \tag{4.14}$$

, where R is the resolution and V_r represents the voltage range. For R = 5 μV and V_r = 1 V, N = 18 bits are necessary. Hence, RAM_1 capacity should be around 6 kB.

On the other hand, RAM_2 is used to store the time constants T_n and T'_n. As the PWM needs to receive the two variables simultaneously to perform its task, a dual-port RAM has to be employed.

For RAM_1 and RAM_2, two types of memories can be used, the static (SRAM) and dynamic (DRAM) RAM. Since DM_c connects a matrix column to the V_{DC} already before the $V_{Gn}(t)$ is sent, a quick memory will reduce unnecessary usage of the V_{DC}. Moreover a SRAM requires less power than a DRAM to work. Therefore, SRAM seems to be the appropriate choice to minimize the system power consumption.

4.7. Conclusions

The proposed circuitry, which resembles the system employed for LCD monitors, allows biasing each of the 768 Qbits/QDs with their specific voltage using a common fixed DC voltage source. This would minimize the complexity and the power consumption of the system. The design and functioning of the QD matrix ensures to keep the bias voltages within the ± 5 μV variance intervals, which are needed to have the perpetual electron confinement in the QD. This task can be fulfilled employing the typical micro-electronic devices such as MOS capacitors (capacity of tens of pF) and MOSFET. Moreover, it has been shown that the system is stable

for DC source noise of 0.5 V and for MOSFET switch commutation faults up to 5 ns (20% of the necessary commutation time).

5 Conclusions and recommendations

5.1. Conclusions

The recent implementation of single electron QDs in semiconductor hetero-structures as Qbits traced a feasible road-map for the future fabrication of quantum computers based on a coherent large set of Qbits. The envisioned scaling up of Qbits involved in computation would disclose the full potential of these machines.

Since dealing with single electron QDs requires a high precision control on our electrical interactions with semiconductor nano-metric structures, the development and assesment of driving circuitry for the future Qbits is an aim of paramount importance. For instance, the voltage needed to confine one electron in a QD strongly depends on the local properties of the semiconductor hetero-structure. The variation of these properties from QD to QD would not be fully controllable during their very large scale integration, thus challenging the design of the quantum computer biasing circuit.

The goal of this thesis is the investigation of the implementation of a circuit to provide constant voltages with an accuracy of 5 µV to the gates of a large amount (768) of quantum dots. The suggested circuit employs one fixed DC bias source, common to all the Qbits, yet it is able to address 2304 different voltages with a precision of ± 5 µV. This task is fulfilled driving 2304 different charging-discharging cycles for the storage capacitors, each coupled with one Qbit. The circuitry consists of a digital and an analog part and is fully based on the very large scale integration technology. In this work it has been assessed that the performances demanded for its devices are compatible with the standards of microelectronic industry. In fact, the employed components in the digital part are the two RAM memories, a controller, a PWM and the two demultiplexers while each element of QDs matrix consists of a MOSFET, a resistor, a micro-fabricated capacitor (as MOS and parallel plate capacitors) and a QD. Despite the apparent difficulty in supplying 2304 different confinement voltages, we proved that the coordinated functioning of these devices simply resembles the working principle of the LCD monitor circuits.

Measurements of both MOS and parallel plate capacitors of three different sizes (80x80 um^2, 250x250 um^2 and 700x700 um^2) were performed to derive their capacitances. The corresponding values of the capacitances, from the smallest device to the largest one, are the following: 6.6 pF, 60 pF and 540 pF. The most interesting part of the C-V characteristic of the MOS devices is their behavior around a biasing voltage of 1 V, as this is the required voltage

for the confinement of the electron(s) in the QD. The capacitance of the 80x80 um^2 capacitor is strongly dependent on the voltage applied at a bias voltage of 1 V. According to eq. 3.8 this problem can be solved in one of the two following ways: decrease the work function by changing the material employed for the electrode (n^+ poly instead of aluminum) or increase the dopant concentration of the semiconductor part of the MOS capacitor. The first solution will ensure the decrease of V_{wf} and therefore result in a shift of the C-V curve, as displayed in Fig. 3.8, to the left. The second solution will cause an increase of V_D and also result in a shift of the C-V curve to the left. The mean leakage current density of each of the three different MOS capacitors was measured as well, with the following results: 5.85 nA/cm^2 (80x80 um^2), 0.95 nA/cm^2 (250x250 um^2) and 0.5 nA/cm^2 (700x700 um^2). The MOS capacitor of the smallest area was placed in a cryogenic environment (T = 4.2 K) and did not show any signs of mechanical damage after the event. This despite the fact that its three layers have different thermal expansion coefficients. No satisfactory results were derived from the C-V measurements of the parallel plate capacitor, the most likely cause being the presence of the pin holes in the oxide layer of the device. Dealing with cryogenic temperatures other than being a challenge could also be an opportunity. Indeed some materials, like niobium, in these conditions, behave like superconductors. For this reason, part of this work has been dedicated to the fabrication of MOS capacitors with Nb electrodes.

In this work the magnitude of the supply voltage (V_{dc}) to provide all the gates of the quantum dots with constant voltages was chosen to be 2 V. A resistor of 1 GΩ was assumed in the small analog circuit which makes up the element of QDs array, while the deviation of the constant voltage at the gate of a quantum dot was allowed to deviate from the desired value by ±5 uV only. With these specifications it appears that the MOSFET should be in the on state for 26 ns in order to charge the capacitor to the proper value while the refresh time of the system is equal to 70.5 us. This charging of the capacitor is stable in case of a fluctuation of the supply voltage of 0.5 V, a fluctuation in the charging time of 5 ns and a fluctuation in the initial charge stored on the capacitor of 1 uV.

A quantitative analysis of the areal scalability and the power consumption of the QDs array has been performed. From this it was gathered that the power consumption of the entire QDs array is equal to 2.3 µW and that the entire array would occupy an area of 0.39 cm^2. The major accomplishments are the simplicity of the proposed design as well as the employment of available technologies only. The simplicity comes from the fact that the entire design consists of seven relatively common digital components and an array made up of a RC-like analog

circuit. With respect to the second accomplishment: no novel devices are required to realize the proposed scheme. Both of these facts ensure the upscaling of qubit systems to at least 768 qubits in the near future.

5.2. Recommendations

The results obtained in this work help us to sketch the future outlook to create a complete and efficient driving circuitry on large scale single electron Qbits plane.

- In this thesis only QDs confinement voltages were envisioned, but it would also be possible to apply the same approach to the initialization, the spin state manipulation and read-out operations.
- As this work focused on the investigation of the implementation of a circuit to provide constant voltages with an accuracy of 5 µV to the gates of a large amount (768) of quantum dots, the next logical step would be the actual implementation of the proposed concept.
- A follow-up to this could be the implementation of a measurement and a feedback mechanism concerning the confinement voltages to ensure a minimal fluctuation of their values.
- It would also be a worthy try to not to etch the SiO_2 of the parallel plate device to see whether that would solve the pin hole problem.
- As with regards to the recommendations for the superconducting device fabrication, Nb thin films etching and processing need to be optimized according to the outcomes observed in this work.

Appendix A

Flowchart MOS capacitor with SiO_2 as dielectric

GENERAL REMARKS

1. Always follow the "Security and Behavior" rules when working in the Dimes cleanrooms.

2. Always handle wafers with care during processing. Use cleanroom gloves and work as clean as possible.

3. Always check equipment and process conditions before starting a process.

Directly notify the responsible person(s) **and** other users when there are problems with equipment operation or contamination. Do not try to repair or clean unknown equipment yourself, and never try to refresh a contaminated etch or cleaning bath !

4. Always clean wafers after several hours of storage **before** performing a coating, furnace, epitaxy or deposition step. Wafers do not have to be cleaned **after** a furnace or epitaxy step if the next process step is carried out immediately.

Use the correct cleaning procedure:

- Acetone or Tepla stripper	for photoresist removal
- HNO_3 100%	for wafers which do not need a HNO_3 65% step
- HNO_3 100% metaal	for wafers which are or have been in contact with a metal
- HNO_3 100% and HNO3 65%	for all other wafers

5. Wafers that are covered with a resist or a metal layer may **never** be processed in a furnace. Only alloying is allowed for wafers with an aluminium layer.

6. It is allowed to use the Leitz MPV-SP or WOOLLAM measurement system for layer thickness measurements on the wafers of a process batch. These measurements are non-destructive and without contact to the wafer surface. If these methods can not be used on your wafer, or when sheet resistance and/or junction depth measurements must be performed, an extra wafer has to be processed for measuring.

7. All substrates, layers and chemicals which are not standard being used in the Dimes 01/02/03/04 or Dimos 01 production processes are considered to be "non-standard" materials, and can be possibly contaminating.

The use of those materials for processing in the class 100 cleanroom and SAL must **always** be evaluated and approved by the PAC committee. It is strictly forbidden to use "non-standard"materials without permission.

Check the PAC "Rules & Instructions" - available on the internet - for more details.

8. Wafers that are contaminated may never be processed in any of the equipment without permission of the PAC committee. Special precautions may have to be taken, like the use of a special substrate holder or container.

9. **Always perform all the measurements and inspection steps, and write down the results in your journal and in the result tables in the cleanroom !!** The results can be used to check the condition of processes and/or equipment.

STARTING MATERIAL: Lres PT

Use SINGLE SIDE polished LOW RESISTIVITY wafers, with the following specifications:

Type	p – type, boron
Grade	test
Orientation	1-0-0, 0 deg off
Resistivity	10-20 Ωcm
Thickness	525 ± 15 µm
Diameter	100 mm

1. CLEAN FURNACE

Furnace: A1
Recipe: AutoTCA
Total time= 8 hours

2. CLEANING PROCEDURE: HNO3 99% and 69.5% (W1, W2)

Cleaning 10 minutes in fuming nitric acid (Merck: HNO_3 99% selectipur) at ambient temperature.

Use wet bench "HNO_3 (99%)" and the carrier with the red dot.

QDR Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Cleaning 10 minutes in concentrated nitric acid (Merck: HNO_3 69.5% selectipur) at 110 °C.

Use wet bench "HNO_3 (69.5%)" and the carrier with the red dot.

QDR Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ

Drying Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a red dot.

NOTE The next step must be performed immediately after drying.

3. DRY OXIDATION: 30 nm SiO_2 (W1, W2 + T1)

Furnace: A1
Recipe: N13
Process: DIBARVAR
Oxidation time= 1hour and 30 minutes

4. MEASUREMENT: OXIDE THICKNESS (T1)

Use the Leitz MPV-SP measurement system to measure the oxide thickness:

Program: Th. SiO2 on Si, <50nm auto5pts
Oxide thickness: 30 nm on your process wafers

5. FRONT SIDE METALLIZATION: 2000 nm Al (W1, W2 +T1)

Use the TRIKON SIGMA sputter coater for the deposition of an Al layer on the wafers.
The target must exist of Al and deposition must be done at 50 °C. Follow the operating instructions from the manual when using this machine.

Use recipe Al_2000nm_50C to sputter a 2000 nm thick layer.
Visual inspection: the metal layer must look shiny.

6. BACK SIDE METALLIZATION: 2000 nm Al on back side (W1, W2 + T1)

Use a clean transport wafer under your process wafer to avoid contamination

Use the TRIKON SIGMA sputter coater for the deposition of an Al layer on the wafers.
The target must exist of Al and deposition must be done at 50 °C. Follow the operating instructions from the manual when using this machine.

Use recipe Al_2000nm_50C to sputter a 2000 nm thick layer.
Visual inspection: the metal layer must look shiny.

7. FRONT SIDE COATING: Co - 3012 – 2.1 um (W1, W2 + T1)

Use the EVG120 system to coat the wafers with photoresist, and follow the instructions specified for this equipment.
The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with **SPR 3012positive** resist, and a soft bake at 95 °C for 90 seconds. The resist will be dispensed with a pump. Always check the relative humidity (48 ± 2 %) in the room before coating.

Use program "**SPR 3012 – 2.1 um**"" on the coating station

8. Expose ASM PAS 5500 - Mask P2688 MINOX (box364) -- n10a-1 (W1, W2 +T1)

Processing will be performed on the ASM PAS 5500/80 automatic wafer stepper.
Follow the operating instructions from the manual when using this machine.

Expose mask P2688 MINOX (box364), with the litho job n10a-1 and layer ID 1.
Use exposure 260 mJ/cm^2.

9. Dev - Single puddle (W1, W2 +T1)

Use the EVG120 system to develop the wafers, and follow the instructions specified for this equipment.
The process consists of a post-exposure bake at 115 °C for 90 seconds, developing with Shipley MF322 with a single puddle process, and a hard bake at 100 °C for 90 seconds.

Use program "Single puddle" on the developer station.

10. INSPECTION:LINEWIDTH AND OVERLAY (T1)

Visually inspect the wafers through a microscope, and check line width and overlay. No resist residues are allowed.

11. DRY ETCH ALUMINIUM (W1, W2)

2.1um Al was etched by AL2MU_50 (OMEGA).

12. CLEANING PROCEDURE :Plasmaoxygen (W1, W2)

TePla: Receipe 1.

13. CLEANING PROCEDURE: HNO3 99% (metal) (W1, W2)

Cleaning 10 minutes in fuming nitric acid(Merck: HNO_3 99% selectipur) at ambient temperature.
Use wet bench "HNO_3 (99%) **metal**" and the carrier with the yellow and red dots.

QDR Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Drying Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a black dot.

NOTE: No 69.5% HNO_3 cleaning step!

Appendix B

Flowchart Parallel plate capacitor with SiO_2 as dielectric

GENERAL REMARKS

1. Always follow the "Security and Behavior" rules when working in the Dimes cleanrooms.

2. Always handle wafers with care during processing. Use cleanroom gloves and work as clean as possible.

3. Always check equipment and process conditions before starting a process.

Directly notify the responsible person(s) **and** other users when there are problems with equipment operation or contamination. Do not try to repair or clean unknown equipment yourself, and never try to refresh a contaminated etch or cleaning bath !

4. Always clean wafers after several hours of storage **before** performing a coating, furnace, epitaxy or deposition step. Wafers do not have to be cleaned **after** a furnace or epitaxy step if the next process step is carried out immediately.

Use the correct cleaning procedure:

- Acetone or Tepla stripper	for photoresist removal
- HNO_3 100%	for wafers which do not need a HNO_3 65% step
- HNO_3 100% metaal	for wafers which are or have been in contact with a metal
- HNO_3 100% and HNO3 65%	for all other wafers

5. Wafers that are covered with a resist or a metal layer may **never** be processed in a furnace. Only alloying is allowed for wafers with an aluminium layer.

6. It is allowed to use the Leitz MPV-SP or WOOLLAM measurement system for layer thickness measurements on the wafers of a process batch. These measurements are non-destructive and without contact to the wafer surface. If these methods can not be used on your wafer, or when sheet resistance and/or junction depth measurements must be performed, an extra wafer has to be processed for measuring.

7. All substrates, layers and chemicals which are not standard being used in the Dimes 01/02/03/04 or Dimos 01 production processes are considered to be "non-standard" materials, and can be possibly contaminating.

The use of those materials for processing in the class 100 cleanroom and SAL must **always** be evaluated and approved by the PAC committee. It is strictly forbidden to use "non-standard"materials without permission.

Check the PAC "Rules & Instructions" - available on the internet - for more details.

8. Wafers that are contaminated may never be processed in any of the equipment without permission of the PAC committee. Special precautions may have to be taken, like the use of a special substrate holder or container.

9. **Always perform all the measurements and inspection steps, and write down the results in your journal and in the result tables in the cleanroom !!** The results can be used to check the condition of processes and/or equipment.

STARTING MATERIAL: Lres PT

Use SINGLE SIDE polished LOW RESISTIVITY wafers, with the following specifications:

Type	p – type, boron
Grade	test
Orientation	1-0-0, 0 deg off
Resistivity	10-20 Ωcm
Thickness	525 ± 15 µm
Diameter	100 mm

1. CLEANING PROCEDURE: HNO3 99% and 69.5% (W1, W2)

Cleaning 10 minutes in fuming nitric acid (Merck: HNO_3 99% selectipur) at ambient temperature.
Use wet bench "HNO_3 (99%)" and the carrier with the red dot.

QDR Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Cleaning 10 minutes in concentrated nitric acid (Merck: HNO_3 69.5% selectipur) at 110 °C.
Use wet bench "HNO_3 (69.5%)" and the carrier with the red dot.

QDR Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ
Drying Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a red dot.
NOTE The next step must be performed immediately after drying.

2. Metallization 1: 2000 nm Al (W1, W2 + T1)

Use the TRIKON SIGMA sputter coater for the deposition of an Al layer on the wafers.
The target must exist of Al and deposition must be done at 50 °C. Follow the operating instructions from the manual when using this machine.

Use recipe Al_2000nm_50C to sputter a 2000 nm thick layer.
Visual inspection: the metal layer must look shiny.

3. Oxide deposition: PECVD SiO_2 (W1, W2 + T1)

Receipe: xxxSiOstd.
Time:1sec.

4. Metallization 2: 2000 nm Al (W1, W2 + T1)

Use the TRIKON SIGMA sputter coater for the deposition of an Al layer on the wafers.
The target must exist of Al and deposition must be done at 50 °C. Follow the operating instructions from the manual when using this machine.

Use recipe Al_2000nm_50C to sputter a 2000 nm thick layer.
Visual inspection: the metal layer must look shiny.

5. COATING: Co - 3012 – 2.1 um (W1, W2 + T1)

Use the EVG120 system to coat the wafers with photoresist, and follow the instructions specified for this equipment.
The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with **SPR 3012positive** resist, and a soft bake at 95 °C for 90 seconds. The resist will be dispensed with a pump. Always check the relative humidity (48 ± 2 %) in the room before coating.

Use program "**SPR 3012 – 2.1 um**"" on the coating station

6. Expose ASM PAS 5500 - Mask P2688 MINOX (box364) -- n10a-1 (W1, W2 +T1)

Processing will be performed on the ASM PAS 5500/80 automatic wafer stepper.
Follow the operating instructions from the manual when using this machine.

Expose mask P2688 MINOX (box364), with the litho job n10a-1 and layer ID 1.
Use exposure 260 mJ/cm^2.

7. Dev - Single puddle (W1, W2 +T1)

Usethe EVG120 system to develop the wafers, and follow the instructions specified for this equipment.
The process consists of a post-exposure bake at 115 °C for 90 seconds, developing with Shipley MF322 with a single puddle process, and a hard bake at 100 °C for 90 seconds.

Use program "Single puddle" on the developer station.

8. INSPECTION:LINEWIDTH AND OVERLAY (T1)

Visually inspect the wafers through a microscope, and check line width and overlay. No resist residues are allowed.

9. DRY ETCH ALUMINIUM (W1, W2)

2.1um Al was etched by AL2MU_50 (OMEGA).

10. CLEANING PROCEDURE :Plasmaoxygen (W1, W2)

TePla: Receipe 1.

11. CLEANING PROCEDURE: HNO3 99% (metal) (W1, W2)

Cleaning 10 minutes in fuming nitric acid(Merck: HNO_3 99% selectipur) at ambient temperature.
Use wet bench "HNO_3 (99%) **metal**" and the carrier with the yellow and red dots.

QDR Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Drying Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a black dot.

NOTE: No 69.5% HNO_3 cleaning step!

12. Etching oxide (Alcatel) (W1,W2)

Gasses: CF_4/CHF_3/He = 50/25/40 sccm
Pressure: 0.05mBar
Power: Beplox = 60 Watt
Plasmox = 50 Watt
Etch time: 1 min.

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