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Sense amplifier offset voltage analysis for both time-zero and time-dependent variability

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ABSTRACT

This paper presents an accurate technique to extensively analyze the impact of time-zero (i.e., global and local variation) and time-dependent (i.e., voltage, temperature, workload, and aging) variation on the offset voltage specification of a memory sense amplifier design using 45 nm predictive technology model (PTM) high performance library. The results show that increasing the supply voltage both for time-zero and time-dependent reduces the offset voltage specification marginally, irrespective of the process corners. In contrast, the offset voltage specification is very sensitive to the temperature and the workload, i.e., the applied voltage patterns. The results also show that a balanced workload results in a significantly lower offset voltage specification. The above results can be used to estimate the required offset voltage accurately for a given lifetime, and operational conditions such as workload, temperature, and voltage; hence, enable the designer to take appropriate measures for a high quality, robust, optimal and reliable design.

1. Introduction

In the past decades, CMOS technology has undergone assertive down-scaling that causes significant bottleneck on the reliability of devices [1,2]. Nowadays, the unreliability sources of nano-scaled technologies are mostly induced by manufacturing or time-dependent variability [1,2]. During the manufacturing process, devices are affected by process variation, which changes the properties of the manufactured devices from the targeted ones. Consequently, the *process* or *time-zero variation* [3,4] is referred to as similar manufactured devices end up having various characteristics.

They can be further classified into global (i.e., different process corners) and local (i.e., mismatch) variations. In addition, *time-dependent variations* result in the device properties to vary and/or degrade during their operational lifetime. Such variations are mostly as a result of *environmental variations* for instance, supply voltage variations and temperature fluctuations [5-8], and *temporal* or *aging variations* for example, *Bias Temperature Instability (BTI)*; both depict an extremely growing effect with CMOS scaling [9-11]. All these variations result in the devices to behave in a different manner than proposed, which may result in the devices (or circuits) to fail if adequate measures are not taken. Designers normally utilize a conservative guard-band and use extra design margins [12] to ensure the proper operation for the worst-case variations until the aimed circuit lifetime. Nevertheless, a pessimistic guard-band guides to either yield or performance loss, while an optimistic guard-band enhances the test escapes and in-field failures. Therefore, it is crucial to consider *all kinds of* variations for both manufacturing and time-dependent to estimate their impact accurately to prevent an overly pessimistic design. Guaranteeing a resilient Sense Amplifier (SA) requires not only a correct sensing delay, but also an appropriate offset-voltage during the memory operational lifetime.

Much work has been done on the impact of reliability on *Static Random Access Memory (SRAM)* cell array but not much work has been investigated for the offset voltage characterization in SAs. Kumar et al. [13] and Andrew et al. [14] investigated the impact of Negative Bias Temperate Instability (NBTI) on the read stability and the Static Noise Margin (SNM) of SRAM cells. Khan et al. [15,16] analyzed the impact of BTI on FinFET based memory cells for different SRAM designs using SNM, Read Noise Margin (RNM) and Write Triple Point (WTP) as metrics. In [17-19], the authors investigated a tunable SA to deal with within-die variations; the authors predicted the offset voltage at design time built on process variations. In [20], the authors distinguished the SA Input Offset by a physical monitoring circuit (implemented in silicon) in order to estimate the yield. In [21], the authors investigated a

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technique to ascertain the signal margins for *Dynamic Random Access Memory (DRAM)* SAs built on offset distribution quantification. The above prior work only focused on time-zero variation. It is crucial to use the right techniques to quantify the offset voltage. Hence, in our previous work [22], we presented an accurate technique to estimate the impact of both time-zero and time-dependent variability on the offset voltage of sense amplifiers, while considering various workloads and process voltage temperature (PVT) variations. However, the impact of global process variation has not been considered. In addition, both SA's sensitivity and reliability failure analysis have not been explored yet.

In this respect, the main contributions of the paper are:

- Sensitivity analysis of the SA.
- Investigation of the SA offset voltage specification while considering five global process corners at time-zero. The offset voltage specification is the minimum input voltage of the SA to function properly within the 6σ margin.
- Thorough voltage, temperature and workload analysis of process and time-dependent variation on the offset voltage specification while considering different process corners.
- Failure rate analysis for the offset voltage specification at *Nominal* process corner, while considering different workloads, supply voltages, and temperatures.

The results show that by incorporating time-zero and time-dependent variability, the offset voltage specification worsens for the *Fast-Slow (FS)* corner with a factor up to 3 × as compared to the *Slow-Fast (SF)* corner. Hence, it is of great importance to take this into consideration when designing robust and reliable memory systems.

The rest of the paper is organized as follows. Section 2 provides a background with respect to the targeted standard latch-type sense amplifier and variability sources. Section 3 discusses the proposed methodology for offset voltage quantification. Section 4 presents the experiments performed. Section 5 analyzes the sensitivity and time-zero variability results. Section 6 analyzes both the time-zero and time-dependent variability results. Section 7 analyzes the reliability failure rate results. Section 8 discusses the crucial messages of the paper. Finally, Section 9 concludes the paper.

2. Background

The standard latch-type sense amplifier which is used in this work is first presented. Thereafter, the variability sources studied in this paper are explained.

2.1. Sense amplifier

Fig. 1 shows the structure of Standard Latch-Type Sense Amplifier (SLTSA) [23], it is in-charge for the amplification of a small voltage change between BL and BLBar during read operations. It produces amplified signals on the output (i.e., *Out* and *Outbar*). The circuit consists of pull-up transistors (i.e., Mup and MupBar), pull-down transistors (i.e., Mdown and MdownBar), two access transistors (i.e., Mpass and MpassBar), two current source transistors (i.e., Mtop and Mbottom), and two inverters at the output of the Sense Amplifier each with a load capacitance of 1 fF. The internal cross coupled inverters consist of two pull-up transistors Mup and MupBar and two pull-down transistors Mdown and MdownBar. They have BL and BLBar as inputs and produce amplified outputs (i.e., *Out* and *Outbar*).

The operation of the sense amplifier comprises of two stages. In the first stage, while SAenable is low, the access transistor Mpass connects BL with the internal node *S* while the access transistor MpassBar connects BLBar with the internal node *SBar*. In this stage, Mtop and Mbottom transistors are turned off. In the second stage, while SAenable is high, the access transistors disconnect the BL(BLBar) input from the internal nodes. The cross coupled inverters obtain their current from Mtop and Mbottom and afterward amplify the change in voltage between *S* and *Sbar*. *S(SBar)* node is actively pulled down when *SBar(S)* exceeds the threshold voltage of Mdown. The positive feedback loop ensures low amplification time and produces the read value at its output. All current paths are disabled when *S(SBar)* is at 0 V and *SBar (S)* is at V_{dd} or vice versa. This process is repeated for each read operation.

2.2. Variation sources

In this paper we analyzed several sources of variability. Fig. 2 shows their relation; They are comprised of time-zero and time-dependent variability. Each is briefly explained next.

2.2.1. Time-zero or process variations (PV)

These impact the circuit at time $t = 0$ and comprise of variations in various parameters incorporating effective channel length (L), oxide thickness (t_{ox}), dopant concentration (N_a), transistor width (W), and threshold voltage V_t. The variations can be classified into local and global variations. Each is briefly described.

2.2.1.1. Local variation. Local variation can be modeled by variation in V_{th} with a standard deviation equal to:

$$\sigma_{V_{TH0}} = \frac{A_{\Delta V_{TH}}}{\sqrt{2WL}} \tag{1}$$

where $A_{\Delta V_{TH}}$ is the Pelgrom's constant [24], and W is the transistor width while L is the transistor length.

2.2.1.2. Global variation. Global process variations are typically a consequence of wafer etching and deviations during the lithography process [25]. These variations are constant over larger areas, and lead to different process corners. In this work we consider the following corners: typical-typical (*TT*), fast-fast (*FF*), slow-slow (*SS*), slow-fast (*SF*) and fast-slow (*FS*). The *TT*, *FF*, and *SS* are uniform corners since they impact both NMOS and PMOS devices uniformly. However, *FS* and *SF* cause an unequal switching in the circuit [25].

2.2.2. Time-dependent variations

These impact the circuit at time $t > 0$ and they are environmental and temporal/aging variations.

2.2.2.1. Environmental variation. In this work, we consider two types of environmental variations and they are supply voltage and temperature variations which will be explained next.

2.2.2.2. Supply voltage variation. The change in supply voltage impacts the operating speed of MOS transistors. The fluctuation in switching activity across the die/circuitry causes an irregular power/current demand and may cause logic failures [26]. In addition, transistor subthreshold leakage fluctuations affect the irregular distribution of supply voltage across the circuitry as well [26]. Thus, reducing the supply voltage degrades the performance of the circuit/transistors and raising supply voltage compensates/improves the performance and significantly reduces circuit failure rates due to variability [26].

2.2.2.3. Temperature variation. They affect the operating condition of MOS transistors. An increase in temperature causes a threshold voltage reduction (which has a positive effect on delay), and a carrier mobility decrement (which has a negative impact on delay and consequently leakage current increment [27]).

The reliance of the threshold voltage on the temperature is stated by [27]:

$$V_{th} = C_{vt} - \frac{Q_{ss}}{C_o} + \Phi_{ms} \tag{2}$$

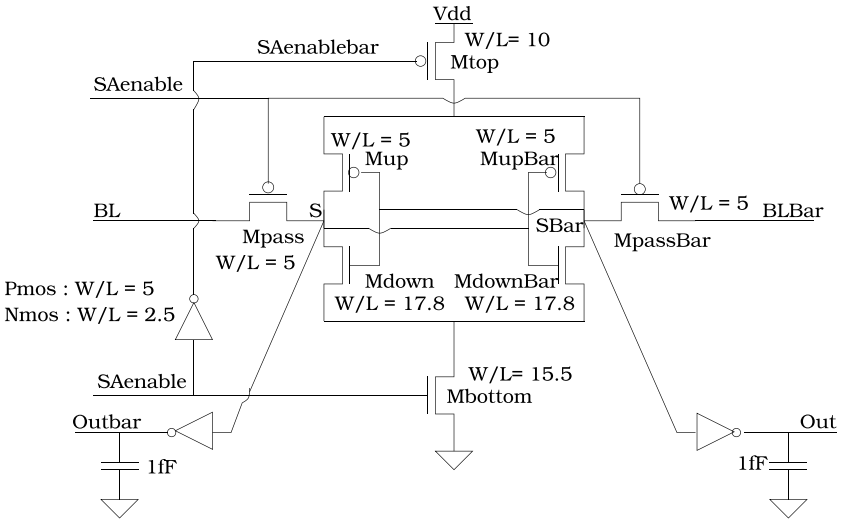

Fig. 1. Standard latch-type Sense Amplifier.

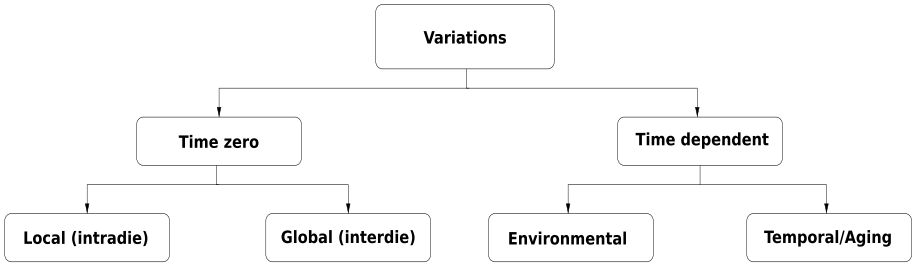

Fig. 2. Classification of the sources of variation.

where C_{vt} is a constant that denotes the fermi potential, Q_{ss} denotes the surface charge at the Si-SiO_2 interface, C_o denotes the gate oxide capacitance and Φ_{ms} denotes the change in work function depending on the temperature, T [27] as stated next:

$$\Phi_{ms} = -0.61 - \Phi_F(T) \tag{3}$$

Here Φ_F(T) represents the Fermi potential. Expression (3) depicts that the change in work function reduces with respect to a rise in temperature and therefore causes a threshold voltage decrement.

2.2.2.4. Temporal/Aging Variations. There are various aging techniques such as Bias Temperature Instability (BTI) [9,28], Hot Carrier Injection [29], and Time Dependent Dielectric Breakdown [30]; BTI is assessed to be the most significant of them [31-34]; hence it is the focal point of this paper. BTI has two major components i.e., Negative (BTI) and Positive (BTI). Atomistic model is proposed to correctly model BTI [31,35–37]; it impacts threshold voltage fluctuation for time $t > 0$ and is founded on the capture and emission of single traps during stress and relaxation stages of NBTI/PBTI, respectively. The threshold voltage variation of the device ΔV_{th} is the amassed result of all the capture and emission of carriers in gate oxide defect traps. The probabilities of the defect occupancy in case of capture P_C and emission P_E are defined by [38] as:

$$P_C(t_{STRESS}) = \frac{\tau_e}{\tau_c + \tau_e}\left\{1 - \exp\left[-\left(\frac{1}{\tau_e} + \frac{1}{\tau_c}\right)t_{STRESS}\right]\right\} \tag{4}$$

$$P_E(t_{RELAX}) = \frac{\tau_c}{\tau_c + \tau_e}\left\{1 - exp\left[-\left(\frac{1}{\tau_e} + \frac{1}{\tau_c}\right)t_{RELAX}\right]\right\} \tag{5}$$

where τ_c is the mean capture time constant and τ_e is the mean emission time constant, while t_{STRESS} is the stress period and t_{RELAX} is relaxation period. Moreover, BTI impacted V_{th} is a combined function of capture emission time map, workloads, duty factor and transistor dimensions, which gives the average number of available traps in each device [33]; the model also consists the temperature impact [31,32].

3. Proposed methodology

Fig. 3 (a) shows a comprehensive flow to ascertain the offset voltage specification of the SA explained. It comprises of five steps. The first four steps are based on 400 Monte Carlo simulations and are replicated for each experiment. Step 5 ascertains the offset specification based on the whole population. Each of the steps is explained next in more details.

1. **Simulate BTI:** First the SA netlist is generated using 45-nm PTM high performance library [39]. To simulate the BTI, we use the atomistic model described in Section 2. The simulations are regulated by a Perl script that produces different instantiations where the BTI induced V_{th} distribution depends on the transistor dimensions, stress time (3 years), duty factor (which depends on the workloads that will be described in Section 4) and frequency (1.32 GHz) [8]. Every produced instance has a certain number of traps (with their unique timing constants) in each transistor, and are integrated in a Verilog-A module of the SA netlist. The module reacts to every individual trap, and changes the transistors concerned parameters. All these parameters can be effectively modeled by a voltage source (the so called BTI-induced threshold voltage) as depicted in Fig. 3 (b). The severity of the BTI effect depends on the workload, temperature, etc. The workload sequence is supposed to be replicated once completed until the age time of three years is attained. Dependent on the workload, we obtain individual duty factors for each transistor depended on the waveforms and workload sequence. This

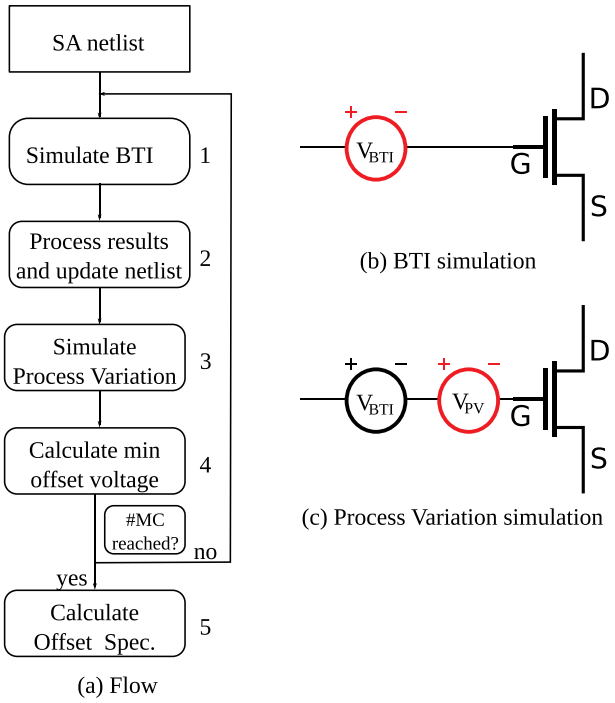

Fig. 3. Offset voltage specification flow.

improves the accuracy of our simulation results.

2. **Process results and update netlist:** In this step, the BTI induced V_{th} shift of each individual transistor is obtained from the earlier step and injected as a voltage source (see Fig. 3 (b)) to the netlist. Note that as a result of the stochastic nature of BTI, each instantiation will have varying threshold voltage shift.
3. **Simulate process variations:** The next step simulates the time zero variations as depicted in Fig. 3 (c). Here we follow the same technique as in [17] where the process V_{th} variations are modeled by a voltage source, V_{pv}. We utilize the build-in Monte Carlo simulations in Spectre [40] to allocate a V_{pv} based on a normal distribution for each transistor with a zero mean and a sigma related by Eq. (1).
4. **Calculate minimum offset voltage:** The SA input voltage is vital for accurate operation of any SA design. We define the minimum *offset voltage* of the SA as the lowest voltage where the SA still successfully completes a read 0 and 1 operations. This voltage can be found for each specific SA instance by looking for the input voltage where the cross-coupled inverters of the SA remain in their metastable point, i.e., where the output starts to change its value. In this work, the minimum offset voltage is determined by applying a binary search on the SA input voltage while considering a sufficient input voltage range (e.g., from − 200 mV to 200 mV). It is worth noting that the offset voltage specification is impacted by process, temperature, voltage, aging variations and workload.
5. **Calculate offset specification:** The offset specification of the SA is computed based on 400 Monte Carlo samples and depends on the desired failure rate or yield. In a good SA design, the offset voltage has a nearly normal distribution and this means that the relation between this distribution and failure rate can be summarized as [23]:

$$\int_{V_{in}=-V_{Offset}}^{V_{Offset}} \mathcal{N}(\mu_{MC}, \sigma_{MC}) = 1 - f_r \tag{6}$$

In this equation, V_{in} presents the input voltage of the SA, V_{Offset} means the offset voltage specification, $\mathcal{N}$ is the probability density function (PDF) of the offset voltages obtained from step 4; μ_{MC} and σ_{MC} are mean and standard deviation, while f_r the failure rate. The equation states that all SA instantiations that need an offset outside the range $[-V_{Offset}, +V_{Offset}]$ result in failures. The objective is to find the SA offset specification V_{Offset}. Note that we verified the normal distribution of the offset voltages using a normal probability plot. At time $t = 0$, this equation can be solved as follows [23]:

$$V_{Offset} = |norminv(\frac{f_r}{2}, \mu_{MC} = 0, \sigma_{MC})| = f(f_r)\cdot\sigma_{MC} \tag{7}$$

where *norminv* presents the normal inverse cumulative distribution function providing the offset voltage for a given f_r, $\mu_{MC} = 0$ and σ_{MC}. The equation can be simplified as depicted at right-hand side, here f is a function that presents a constant depending on f_r. However, depending on the workload for time $t > 0$ aging can shift this distribution (i.e., have a non-zero mean); this invalidates Eq. (7). As a consequence, we determine V_{Offset} directly from Eq. (6) by solving this equation numerically. In this work a failure rate $f_r = 10^{-9}$ leading to $f(f_r) = 6.1$ is assumed. This means that for time $t = 0$ we obtain $V_{Offset} = 6.1 \cdot \sigma_{MC}$. The right-hand side of Eq. (7) is only valid when $\mu_{MC} = 0$.

It is worth noting that the steps 1 and 3 in Fig. 3 (a) should ideally be swapped. However, due to constraints in our available scripts we reversed both steps for our convenience. Compared to the state-of-the-art, where the focus is typically either on BTI or process variation, the presented flow in Fig. 3 is flexible and can be generally extended to include other types of variation (such as systematic variation, process variation, Hot Carrier Injection (HCI), etc.) In addition, it can be applied to any digital circuit, when a clear aging metric can be identified.

4. Experiments performed

In this work, we performed four sets of experiments for the different process corners while considering the impact of both time-zero variability and time-dependent variability on the offset specification. They are:

- **Sensitivity analysis:** The sensitivity analysis for the SA's offset voltage specification is performed for five process corners (i.e., *Nominal (Nom.), Fast-Fast (FF), Fast-Slow (FS), Slow-Fast (SF), and Slow-Slow (SS)*); this analysis is done without the BTI impact. The target is to investigate the contribution of each transistor to the offset voltage specification. During this sensitivity analysis, only the results of the pass transistors, pull-down and pull-up transistors are reported. Note that the transistors *Mtop* and *Mbottom* of Fig. 1 do not impact the offset voltage specification, since the transistors *Mtop* and *Mbottom* are common to the cross-coupled inverters of the SA. We have verified this in simulation.
- **Process variation (PV):** The impact of process variation on the offset voltage specification is performed for all process corners, while considering different voltages (i.e., −10% V_{dd}, nominal $V_{dd} = 1.0$ V, and +10% V_{dd}) and temperatures (i.e., nominal temperature = 298 K, 348 K, and 398 K).
- **Process and aging variation:** We examine the combined effect of both time-zero and time-dependent variability (for 3 years) for the five process corners. The examination is performed while considering varying supply voltage, temperature conditions, and workloads. We suppose that 80% of the executed instructions (e.g., by a CPU) are read instructions (which activate the SA). Furthermore, we define three distinct sequences to introduce the 80% of the reads: {r0} (all the reads are 0), {r1} (all the reads are 1) and {r0r1} (50% {r0} and 50% {r1}). It is worth noting that the aging variability is workload dependent, while PV is not. The explanation for the workload stresses have been given in [22].
- **Reliability failure analysis:** In this experiment, failure rate analysis is performed for the nominal process corner, while considering various supply voltages, temperatures, and workloads.

Table 1
Sensitivity analysis at time-zero.

Process corners	σ offset voltage Due to Pass transistors (mV)	Due to Pull-down Transistors (mV)	Due to Pull-up Transistors (mV)	Overall (mV)	Offset spec. (mV)
Nom.	0.17	11.16	0.69	15.84	96.06
FF	0.40	11.46	0.80	16.26	96.41
FS	0.28	11.77	0.55	16.69	101.00
SF	0.06	10.68	0.91	15.17	92.30
SS	0.13	10.83	0.60	15.37	94.30

5. Time-zero variability

5.1. A sensitivity analysis

Table 1 depicts the results of the sense amplifier's sensitivity analysis due to time-zero variability. Note that the sensitivity analysis of the transistors (i.e., pass transistors, pull-down and pull-up transistors) is performed using the same approach as explained in Step 5 of Section 3, but it considers only process variations. During the sensitivity analysis, process variation is only injected in one of the transistors, while the sigma of the input offset voltage is measured.

The table reports the standard deviation of the input voltage of the SA of all the process corners considering PV in individual transistors (column 2 to column 4) and PV in all transistors (column 5). The last column provides the offset voltage specification (derived from Eq. (6)). The table shows that the pull-down transistor is the most dominant contributor to the offset voltage specification, irrespective of the process corner. For example, at nominal process corner, the standard deviation due to the pull-down transistor is 11.16 mV, while this does not exceed 0.17 mV and 0.69 mV for the pass transistor and pull-up transistor, respectively. The pull-down transistors are mostly responsible for discharging the inputs to the SA after being pre-charged; in case these pull-down transistors are implemented with the fast corner library (i.e., they have a lower V_{th}), the impact of local PV is larger, leading to a larger offset voltage impact. In addition, the table also shows that the shift in offset voltage is the worst (5%) in case of *FS* process corner as compared with nominal case, while the *SF* corner reduces the offset specification voltage with 4.1%.

5.2. Process variability

The results of the impact of PV experiments, varying supply voltages, and temperatures on the voltage offset are discussed next.

5.3. Voltage dependency

Fig. 4 depicts the probability density function (PDF) of the normal distributed offset voltages of three process corners (i.e., *FS*, *Nom.*, and *SF*) for two voltages (i.e., $-10\%V_{dd}$ and $+10\%V_{dd}$) at nominal temperature at time-zero. The y-axis represents the PDF, while the x-axis represents the *minimum offset voltage of the SA* denoted as Vin. The plots for the two other process corners (i.e., *FF* and *SS*) are omitted for clearness. Note that the results for *FF* and *SS* are within the boundaries of *FS* (max value) and *SF* (min values). Nevertheless, they are all included in Table 2 which presents all voltage dependency results; the μ, σ and the offset voltage specification are also added. The figure clearly shows that the voltage offset specification dependency on the varying supply voltage at time-zero is marginal, irrespective of the three process corners; the voltage offset increment does not exceed 2.4% in the worst case, which is for *SF* corner. Note that the supply voltage has a marginal impact, as it is not favoring one of the preferred values of the SA, i.e., it does not create an unbalance in the cross-coupled inverters. Note also

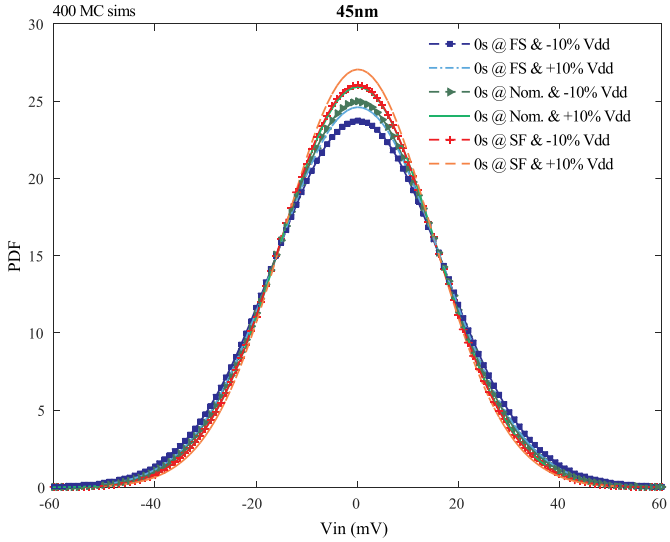

Fig. 4. Supply voltage impact at time-zero for three process corners.

Table 2
Voltage and temperature impact at time-zero.

	Values	V_{dd}			Temp.		
	(mV)	−10%	Nom.	+10%	298 K	348 K	398 K
Nom. corner	μ	0.09	0.12	0.15	0.12	0.12	0.13
	σ	16.0	15.7	15.4	15.7	16.3	16.9
	Offset	97.51	96.06	94.03	96.06	99.51	103.5
FF corner	μ	0.15	0.19	0.21	0.19	0.18	0.17
	σ	16.2	15.8	15.4	15.8	16.5	17.1
	Offset	99.17	96.41	93.95	96.4	100.6	104.6
FS corner	μ	0.12	0.14	0.16	0.14	0.15	0.18
	σ	16.8	16.5	16.2	16.5	17.4	18.4
	Offset	102.7	101.0	99.0	101.0	106.1	112.7
SF corner	μ	0.06	0.10	0.15	0.10	0.093	0.097
	σ	15.3	15.1	14.7	15.1	15.5	15.9
	Offset	93.6	92.3	90.1	92.3	94.6	96.9
SS corner	μ	0.07	0.08	0.10	0.08	0.10	0.12
	σ	15.5	15.4	15.3	15.4	16.0	16.8
	Offset	94.90	94.29	93.20	94.30	97.70	102.4

that relatively the lower the supply voltage, the higher the required voltage offset specification, irrespective of the process corner. For example, at *FF corner* the offset voltage is 99.17 mV at $-10\%V_{dd}$ while this is 93.95 mV at $+10\%V_{dd}$. This can be explained by the impact of PV; the lower the V_{dd} the higher the impact of PV.

5.4. Temperature dependency

Fig. 5 depicts the PDF of the offset voltage distribution of three process corners (*FS*, *Nom.*, and *SF*) for two temperatures (298 K and 398 K) at nominal supply voltage. The plots for the other two process corners (*FF* and *SS*) are omitted for the same reasons as for Fig. 4. Nevertheless, they are all included in Table 2. The figure and table show that the offset voltage specification increases with temperature, reaching 12% for T = 398 K *FS* (worst case) as compared with T = 298 K. The figure and table also show that the average, $\mu = 0$, irrespective of the process corners. Note that higher temperatures lead to higher σ shifts, irrespective of the process corners; this is caused by the impact of temperature on the V_{th}. V_{th} reduces with temperature; therefore, the impact of PV is bigger at higher temperatures. For example, at *nominal* corner the standard deviation is 15.7 mV at 298 K and 16.9 mV at 398 K; an increment of 7.6%. In conclusion, the impact of PV at time zero on the SA voltage offset is marginally dependent on supply voltage (only 2.4% increment), while it is reasonably dependent

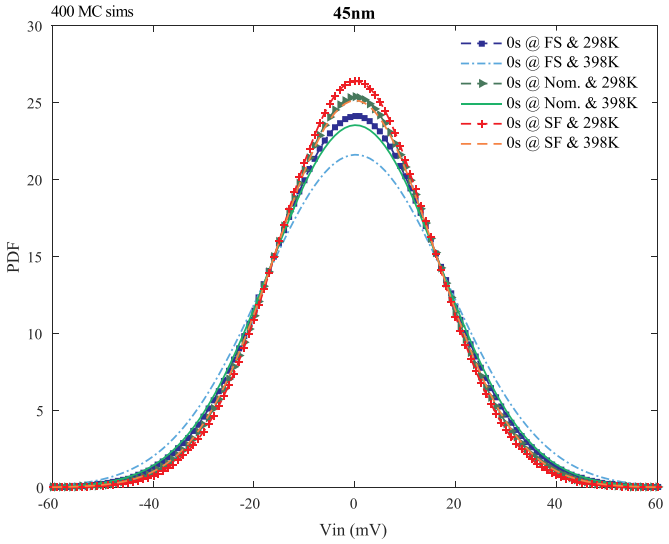

Fig. 5. Temperature impact at time-zero for three process corners.

on the temperature (up to 12% increment).

6. Time-dependent variability

The same experiments of the previous section will be performed but now considering both time-zero and time-dependent variability. As time-dependent variability is workload dependent, also different workloads will be analyzed.

6.1. Voltage dependency

Fig. 6 depicts the PDF of the offset voltage for different supply voltages and workloads using the *Nominal* process corner at 298 K. For the sake of clarity, only *Nominal* corner has been provided. The other cases can be found in Table 3. The figure shows 6 plots: $2V_{dd}$'s (-10% and $+10\%V_{dd}$) $\times$ 3 workloads (see Section 4). The plots for the nominal V_{dd}'s and for the other process corners are left out for clarity reasons; nevertheless, all the results are listed in Table 3. The figure depicts that unbalanced workloads shift the mean offset voltage distribution to the right (for {r0}) or left (for {r1}), while the mean shift of balanced workloads ({r0r1}) equals zero. Although local PV causes mean shifts, BTI might influence them. Note that in BTI only stressed

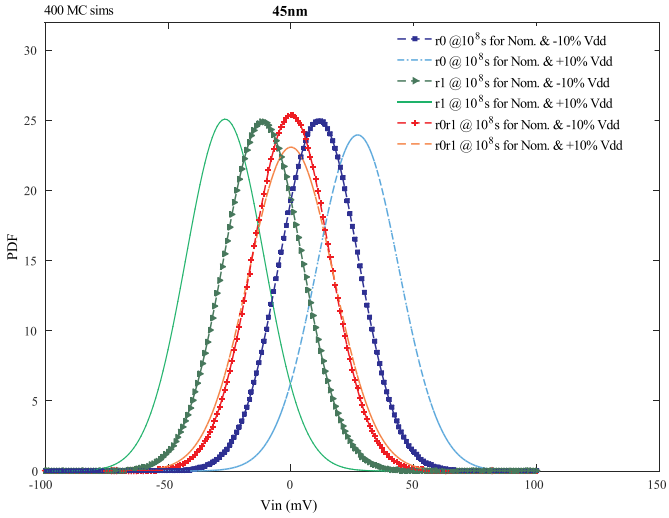

Fig. 6. Voltage impact at time-dependent for *Nominal* corner.

transistors are impacted and therefore an unbalanced workload will lead to an unbalanced cross coupled inverter pair (see transistors *Mup*, *Mupbar*, *Mdown*, and *Mdownbar* in Fig. 1). This will favor either {r0} or {r1} operations and eventually cause the means to shift.

The figure also shows that this mean offset voltage shift worsens for higher V_{dd}. A V_{dd} increment accelerates the BTI process due to a larger electrical field across the gate. This mean shift eventually impacts the BTI offset voltage specification negatively. For example, in Fig. 6 and Table 3, for {r0} at Nom.V_{dd}, the mean shift is 18.1 mV, while this is 27.2 mV at $+10\%V_{dd}$ and 10^8 s. The figure and table also show that the standard deviation of the offset voltage shift marginally increases both for unbalanced and balanced workloads. Furthermore, the combined impact of both mean and standard deviation offset voltage shift significantly increases the offset voltage specification for unbalanced workloads (up to 127.1 mV); while this marginally increases for the balanced workloads (up to 105.6 mV).

Table 3 also tabulates the results of the other process corners. The table depicts that the offset voltage specification significantly increases at 10^8 s with respect to time-zero at Nom.V_{dd}, irrespective of the process corners. For example, at time-zero and *FF* corner, the offset voltage specification is 96.4 mV at time-zero while it increases to 119.5 mV at 10^8 s, (which is up to 23.6%); similar results but with different degradations are obtained for the other corners. For *FS*, this increment is 34.3%, while for *SF* only 11.5%.

The table further reveals that the impact of V_{dd} is marginal on the voltage specification. For example, for the *Nominal* corner at $+10\%V_{dd}$ the *mean and sigma* are -26.8 mV and 15.9 mV for workload {r1} and they are equal to -17.9 mV and 16.5 mV at Nom.V_{dd}.

Fig. 7 depicts the PDF of the offset voltage for the extreme voltage condition i.e., ($+10\%$ V_{dd}) for both *FS* (worst case) and *SF* (best case) process corners, irrespective of the applied workloads. The figure shows that at 10^8 s and $+10\%$ V_{dd}, the offset voltage distribution is wider for *FS* process corner than for *SF* process corner; overall *FS* has a high offset voltage specification. This is due to an increase in both μ and σ offset shift (see Table 3). For example, the offset voltage shift at {r0} is 122.5 mV for *SF* corner while this is only 133.2 mV for *FS* corner (which is up to 8.7% higher).

6.2. Temperature dependency

Fig. 8 depicts the PDF of the offset voltage for various temperatures, and workloads for the *Nominal* process corner at nominal voltage. In addition to the time-zero plot; the figure also depicts six plots with respect to time-dependent variability, two temperatures (298 K and 398K) $\times$ 3 workloads. The plots for 348 K and the other four process corners (i.e., *FF*, *FS*, *SF*, and *SS*) are omitted due to limited space. However, their results are included in Table 4.

Fig. 8 shows that the average offset voltage shift increases significantly at a high temperature (398 K) for the unbalanced workloads, while the mean offset shift is zero for the balanced workload. For example, at 10^8 s and 298 K, the mean offset voltage shift is 18.1 mV while this increases to 87.1 mV at 398 K (this is up to 381.2%!) for the unbalanced workload (results of {r0} are taken). The figure and Table 4 also show that a temperature rise increases the standard deviation, irrespective of the workloads. For example, at 10^8 s and for 298 K the standard deviation equals 16.6 mV while this is 20.3 mV at 398 K (this increases up to 22.3%) for {r0} workload.

The figure and in particular Table 4 show that the offset voltage specification increases significantly, especially for the unbalanced workload. This can be explained by the increment in σ and μ (for unbalanced workloads) when the temperature increases.

The higher the temperature, the larger the offset voltage specification; e.g., at 398 K the {r0} causes an offset voltage specification of 208.9 mV for nominal corner, while this is 117.7 mV at 298 K (this increases up to 77.5%). Obviously, the offset voltage specification increment is much higher for the *FS* process corner, unbalanced

Table 3
Voltage impact at time-dependent.

Aging (s)	WL	Vdd. (V)	Nominal			FF			FS			SF			SS		
			μ (mV)	σ (mV)	Offset (mV)	μ (mV)	σ (mV)	Offset (mV)	μ (mV)	σ (mV)	Offset (mV)	μ (mV)	σ (mV)	Offset (mV)	μ (mV)	σ (mV)	Offset (mV)
0	–	Nom.	0.1	15.7	96.1	0.2	15.8	96.4	0.1	16.5	101.0	0.1	15.1	92.3	0.1	15.4	94.3
10^8	{r0}	− 10%	11.5	16.0	107.3	11.9	16.3	109.9	12.0	16.8	112.9	11.2	15.3	103.2	11.1	15.5	104.0
10^8	{r0}	Nom.	18.1	16.6	117.7	18.4	16.8	119.5	28.9	17.8	135.6	17.6	16.0	113.3	17.5	16.2	114.6
10^8	{r0}	+ 10%	27.2	16.7	127.1	27.4	16.8	127.9	28.3	17.5	133.2	26.5	16.0	122.5	26.6	16.3	124.5
10^8	{r1}	− 10%	−11.4	16.0	107.5	−11.7	16.3	109.5	−11.8	16.9	113.0	−11.2	15.4	103.3	−11.0	15.6	104.4
10^8	{r1}	Nom.	−17.9	16.5	117.0	−18.0	16.7	117.9	−28.5	17.0	130.6	−17.5	15.9	112.7	−17.5	16.2	114.5
10^8	{r1}	+ 10%	−26.8	15.9	122.2	−26.8	16.0	122.5	−27.9	16.7	128.2	−26.1	15.3	117.6	−26.4	15.7	120.6
10^8	{r0r1}	− 10%	0.1	15.7	96.0	0.2	15.8	96.6	0.1	16.5	100.9	0.1	15.1	92.3	0.1	15.4	94.0
10^8	{r0r1}	Nom.	−0.2	17.1	104.6	−0.1	17.3	105.5	−0.2	18.0	109.9	−0.2	16.4	100.5	−0.2	16.7	102.2
10^8	{r0r1}	+ 10%	0.0	17.3	105.6	0.1	17.5	106.7	0.1	18.1	110.9	−0.0	16.6	101.5	−0.0	16.9	103.1

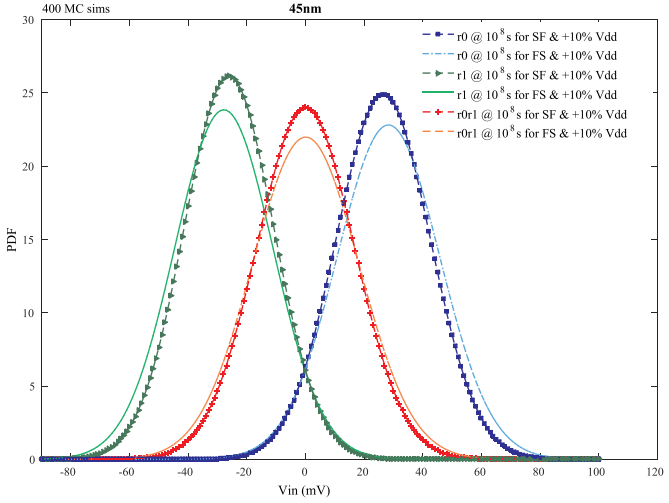

Fig. 7. Voltage impact at time-dependent for both *SF* & *FS* corner at +10% V_{dd}.

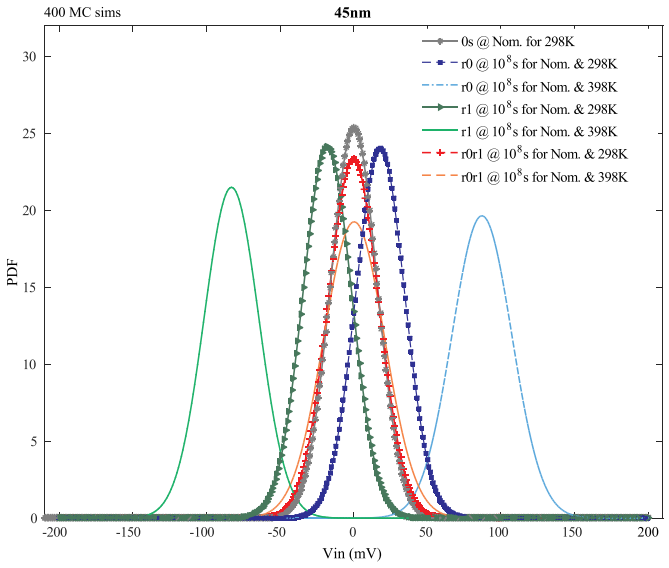

Fig. 8. Temperature impact at time-dependent for *Nominal* corner.

workload, and higher temperature. Note that applying a balanced workload can reduce the impact of offset voltage specification at time-dependent and higher temperature (up to 4 ×) in the worst case.

Fig. 9 depicts the PDF of the offset voltage for extreme temperature conditions, i.e., 398 K for both *FS* (worst case) and *SF* (best case) process corners, irrespective of the applied workloads. Fig. 9 shows a similar trend as Fig. 7; however the offset distribution is wider at higher temperature. This is attributed to the severity of temperature impact on the BTI V_{th}. Note that critical temperatures impact the offset voltage more than the supply voltage, irrespective of the process corners and workloads.

7. Reliability failure analysis

This section performs reliability failure analysis for the sense amplifier and analyzes the failure rate over time. Both the impact of voltage and temperature are considered.

7.1. Methodology

To evaluate the added value of our framework, we will be analyzing the failure rate based on an offset voltage specification which is determined by the previous work. Previously, this offset voltage specification is solely derived from time-zero variations [22]. We add a 10% margin for aging and use our methodology to examine how the failure rate increases over time when actual workloads and aging are considered. The reason for selecting a 10% margin is due to the fact that it is a classical margin for the Design for Manufacturability (DFM) in the ITRS 2005 edition [1,12]. In order to obtain the failure rate f_r over time, Eq. (6) will be solved for different time steps.

$$f_r(t) = 1 - \int_{Vin=-V_{Offset}}^{V_{Offset}} \mathcal{N}(\mu_{MC}, \sigma_{MC}, t) \tag{8}$$

In order to obtain f_r at time t, both V_{Offset} (i.e., the offset voltage specification from time-zero plus 10% margin) and the distribution of the input voltages of the SA $\mathcal{N}(\mu_{MC}, \sigma_{MC}, t)$ must be known. The offset voltage specification at time-zero for a failure rate of 10^{-9} equals 6.1σ using only local process variation [23]; subsequently, by adding a 10% margin, we obtain the interval values from $-V_{Offset}$ and V_{Offset} of the integral in Eq. (8). For example, in Table 4 the offset specification is 96.1 mV at time 0 (solely based on 6.1σ as average is 0 using a failure rate $f_r = 10^{-9}$) for the *Nominal* corner. Adding the 10% margin leads to an offset specification of 105.7 mV, which is used in the experiments of the following subsections. The distribution of the input offset voltages (i.e., $\mathcal{N}(\mu_{MC}, \sigma_{MC}, t)$) will be simulated for different time steps, similarly as done for 10^8 s in Tables 3 and 4. Next, we will analyze the impact of voltage and temperature for different workloads.

7.2. Voltage dependency

Fig. 10 depicts the failure rate for the balanced and unbalanced workloads for the various supply voltages for the *Nominal* process corner. The same 10^{-9} failure rate as for time-zero is used as a reference. Note that for the unbalanced workload only {r0} has been

Table 4
Temperature variation at time-dependent.

Aging (s)	WL	Temp. (K)	Nominal μ (mV)	Nominal σ (mV)	Nominal Offset (mV)	FF μ (mV)	FF σ (mV)	FF Offset (mV)	FS μ (mV)	FS σ (mV)	FS Offset (mV)	SF μ (mV)	SF σ (mV)	SF Offset (mV)	SS μ (mV)	SS σ (mV)	SS Offset (mV)
0	–	298	0.1	15.7	96.1	0.2	15.8	96.4	0.1	16.5	101.0	0.10	15.1	92.3	0.1	15.4	94.3
10^8	{r0}	298	18.1	16.6	117.7	18.4	16.8	119.5	18.8	17.5	123.5	17.6	16.0	113.3	17.5	16.2	114.6
10^8	{r0}	348	47.7	18.1	156.5	49.1	18.6	160.7	50.5	19.5	167.3	46.1	17.2	149.0	46.5	17.7	152.9
10^8	{r0}	398	87.1	20.3	208.9	89.1	20.6	212.6	94.8	22.7	231.1	82.5	18.7	194.5	86.3	20.4	208.6
10^8	{r1}	298	−17.9	16.5	117.0	−18.0	16.7	117.9	−18.6	17.4	122.7	−17.5	15.9	112.7	−17.5	16.2	114.5
10^8	{r1}	348	−46.6	17.5	151.3	−47.6	17.7	153.9	−49.0	18.6	160.4	−45.2	16.6	144.8	−45.4	17.1	147.9
10^8	{r1}	398	−83.0	18.6	194.4	−84.9	18.9	198.2	−89.0	20.1	209.5	−79.4	17.4	183.9	−81.6	18.3	191.5
10^8	{r0r1}	298	−0.2	17.1	104.6	−0.1	17.3	105.5	−0.2	18.0	109.9	−0.2	16.4	100.5	−0.2	16.7	102.2
10^8	{r0r1}	348	0.0	18.8	114.8	0.1	19.2	117.1	0.1	20.1	122.5	−0.0	17.8	109.0	0.0	18.4	112.3
10^8	{r0r1}	398	0.3	20.7	126.6	0.3	21.1	129.1	0.4	22.7	138.5	0.2	19.3	118.1	0.3	20.5	125.5

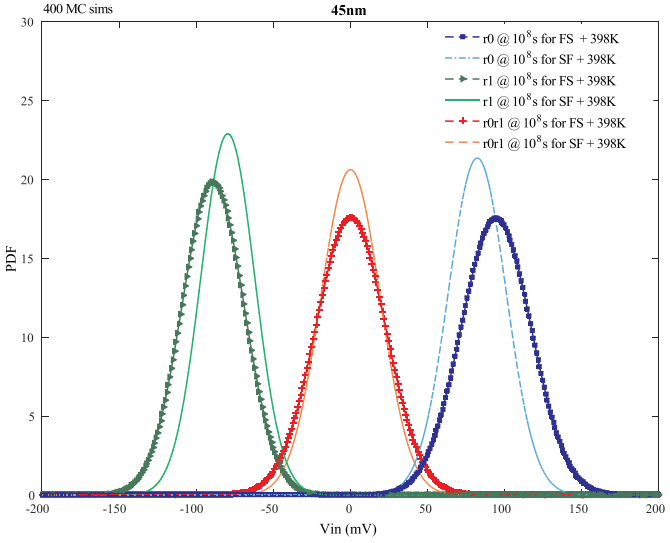

Fig. 9. Temperature impact at time-dependent for both *FS* & *SF* corner at 398 K.

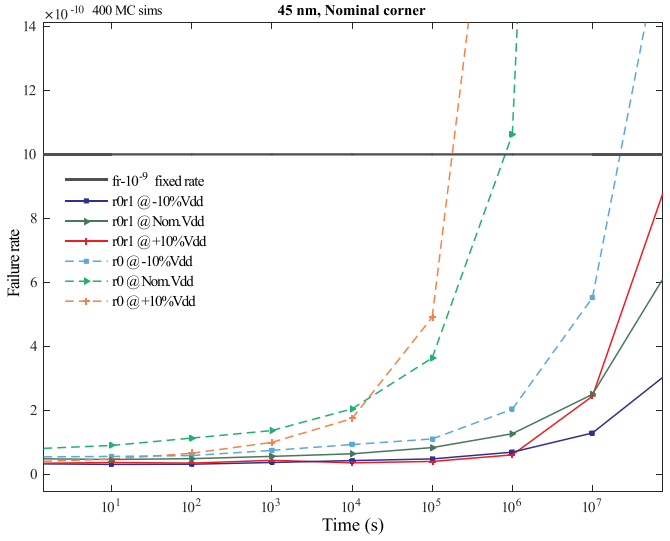

Fig. 10. Voltage impact at time-dependent failure rate analysis for *Nominal* corner.

added as {r1} gives similar results. Note that ideally they lead to the same results.

The figure shows that after a certain amount of time, the failure rate starts to increase exponentially. This effect is worse for unbalanced workloads and higher V_{dd}. The 10% added margin to the time-zero offset specification is enough to keep the failure rate below 10^{-9} for balanced workloads. For example, at 10^8 s and for $-10\%V_{dd}$ the failure rate for the balanced {r0r1} workload is 0.33×10^{-9} which is 67% less than the targeted failure rate, while this is 34% and 3.4% less for Nom.V_{dd} and $+10\%V_{dd}$, respectively. However, for the unbalanced workload at $-10\%V_{dd}$, the failure rate exceeds 10^{-9} by 84.8% after an operational life time of 10^8 s, while for the Nom.V_{dd} the failure rate already increases with 562.5% after 10^7 s. Hence, more SAs than expected will fail if previous methods based on time-zero will be used. Therefore, it is important to characterize the degradation accurately and have mitigation schemes to remedy the unreliability of the SA.

7.3. Temperature dependency

Fig. 11 shows a similar graph as Fig. 9 but for different temperatures. The figure also shows that the failure rate strongly increases with the temperature and that the time-zero approach fails significantly. The figure shows that at 398 K, also *balanced* workloads do not meet the target of 10^{-9} failure rate after 10^8 s. The above results can be even worse for different process corners. Therefore, our presented framework is required to accurately determine the offset voltage specifications.

8. Discussion

Memory sense amplifier robustness and reliability are very

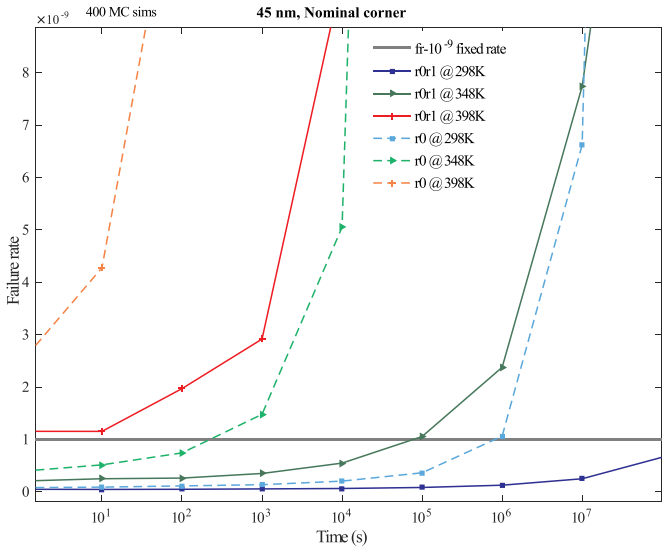

Fig. 11. Temperature impact at time-dependent failure rate analysis for *Nominal* corner.

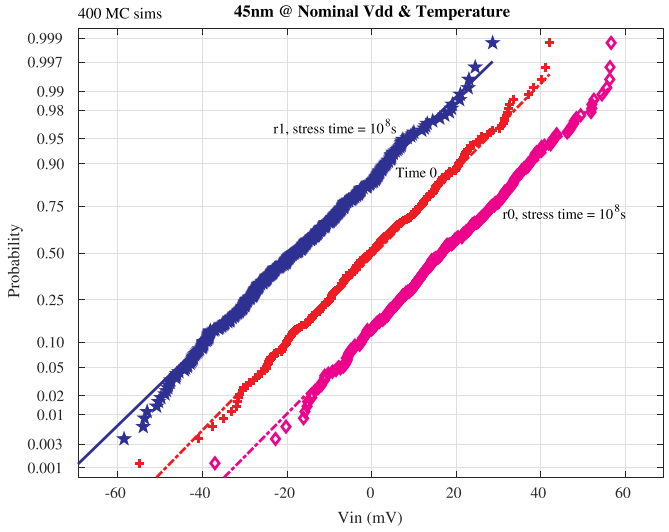

Fig. 12. Validation of Offset Voltage expression in Eq. (6) at both time 0 and 10^8 s.

important for the overall design of memory systems. The presented analysis showed that the offset voltage specification and failure rate of the SA design are dependent on the process corner, supply voltage, temperature, workload etc. After the evaluation of the simulation results, we conclude the following:

- The results of the experiments in this paper are only valid if the offset distributions follow the normal distribution as specified in Eq. (6). To illustrate that this is the case, consider for example the normal probability plot of the offset voltage distribution in Fig. 12 for the nominal process corner for both time-zero and after a stress time of 10^8 s (i.e., r1 and r0), under nominal conditions (i.e., Vdd = 1.0 V and Temperature = 273 K). The figure reveals that the offset voltage specification distribution both for time 0 and after a stress time of 10^8 s matches well with the fitted normal distribution plots. Therefore, the figure shows that Eq. (6) is valid. Moreover, the plots clearly show that after stress, unbalanced workloads create a shift in the mean; either to the left for r1 or to the right for r0.
- The offset voltage specification at time-zero variability is marginal for varying supply voltage and this is significant for varying temperature; however, the offset voltage specification is higher for the *FS* corner as compared to the other process corners.
- The offset voltage specification at time-dependent variability and at varying supply voltage for the 5 process corners maintain a unique trend with respect to the average shift, standard deviation and its offset shift; however, the *FS* process corner proves to be the worst corner while *SF* is the least impacted corner.
- The offset specification at time-dependent variability and at varying temperature for the various process corners, irrespective of the workloads follow the same trend; however, the offset specification is more severe at higher temperature and for unbalanced workloads, irrespective of the process corner being considered. *Note that efficient application of balanced workload can reduce the impact of offset specification at time-dependent variability and 398K* (up to 4 ×), irrespective of the process corner considered.
- The proposed technique for offset voltage computation is unique not only in the sense that it utilizes an accurate BTI model and involves the workload dependency for various process corners, but also because it integrates both the time-zero variability as well as time-dependent variability. The extracted results clearly show that using only environmental time-dependent variability for various process corners while considering zero-time variability analysis is not accurate enough. The change in offset voltage between time-zero and time-dependent variability for the different process corners is maximum for *FS* corner and minimum for the *SF*. Hence, the other three process corners fall in between the two extreme corners.
- In addition, the dependency of offset voltage on workload (application) has been depicted to be significant. Applying balanced workload results in reduced impact. Thus, thinking about integrating some features in the circuits to internally create a balance workload during the lifetime of the application is crucial for optimal and reliable designs. Schemes such as bit-flipping [41] can be useful.
- Our failure analysis results in Section 7 showed that the observed failure rate can be much higher than expected when factors such as workloads, voltage, temperature etc. are not properly considered. Hence, insufficient margins will increase the number of failing devices with needlessly high costs.
- The failure rate results show that adding a 10% margin to the offset voltage specification at time-zero is typically sufficient. However, the failure rate is much worse at high temperatures, irrespective of the workloads and added margins.
- Finally, It is worth noting that the described technique of Fig. 3 can be extended to any digital circuit, as long as there is an obvious metric (for example offset specification) to be quantified. For instance, the critical paths in a pipeline stage can be computed based on the path delay metric.

9. Conclusion

This paper investigated an accurate methodology to thoroughly analyze the impact of time-zero and time-dependent variation on offset voltage specification for an SRAM SA design utilizing 45 nm PTM high performance library. The technique considers also the sensitivity analysis, five global process corners (for both time-zero and time-dependent) while taking into account different supply voltages, temperatures, and workloads, and failure analysis as well as degradation as a result of aging. The results of this investigation show that at time-zero variation the SA offset voltage specification sensitivity analysis is clearly dominated by the pull down transistors which means that SA designers should be more concerned on the pull down transistors for a better SA offset voltage specification quantification. Furthermore, at time zero variability the offset voltage specification is marginally dependent on varying supply voltages and temperatures. However, this becomes more significant when time-dependent variability for unbalanced workloads are taken into account which implies that balanced workloads can reduce the offset voltage specification impact (up to 4 ×) in the worst case. In addition, at time-dependent variability the SAs failure rate are mainly not met, hence it is critical to characterize the degradation accurately and provide mitigation techniques to compensate the SA unreliability. The proposed technique gives designers a preferable way of ascertaining the offset voltage specification; hence, aiding designers in making appropriate design choices based on the workloads and environmental conditions.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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