Belgian Rectifier

Analysis and Optimization of a Novel Three-Phase Boost-Type PFC Rectifier

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PRODRIVE TECHNOLOGIES

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Abstract

This project investigates the newly proposed Belgian Rectifier, a novel three-phase boost power factor correction rectifier which is advantageous for AC-to-DC conversion in applications, such as, off-board and on-board chargers for electric vehicles. The Belgian rectifier can achieve very high levels of efficiency and power density, while its components endure much lower stress than in other rectifier topologies. The capacitive midpoint produces a three-level voltage over the switches and inductors, therefore a number of advantages can be pointed out such as low stress of the MOSFETs, low magnetic energy requirement for the inductors and low EMI filtering. Two modulation schemes have been analyzed with regard to component stresses and soft switching and one of them is proposed. The modulation scheme derivation is followed by a full analysis of the converter that consists of steady-state modelling, dynamic closed-loop modelling, component loss and volume modelling. In addition, by sweeping through different parameters in the aforementioned models, a Pareto-front in the efficiency versus power density performance space is created. Thereby, an optimal design can be picked out using multi-objective optimization. Finally, a comparison between the Belgian Rectifier and Six-Switch Rectifier is done to reveal the advantages and disadvantages of the former topology.

Dimitrios Tsiakos
Eindhoven, September 2020

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1 Introduction

1.1. Background

Globally, the electric car deployment has seen a rapid growth over the last decade, with the global number of electric passenger vehicles surpassing the number of 5 million in 2018, thus a growth of 63% from the previous year. The distribution of this growth, however, is uneven since 45% of the electric cars that circulated on the roads in 2018 were in China - a total of 2.3 million - compared to 39% in 2017. On the other hand, the United States accounted for 22% of the global fleet, and Europe 24%. [1]

The very quick increase of the electric vehicle global market share has a lot of implications for the energy transition. The evolution of the well-to-wheel (WTW) greenhouse emissions from the EV fleet is determined by the combined evolution of the energy used by EVs and the carbon intensity of the electricity generation. Therefore, as the grid becomes less carbon intensive, so do the electric vehicles. It is clear that the benefits of the transport electrification will be greater if the EV deployment takes place in parallel with the decarbonisation of power systems.

On the same time, a rapid rise of the number of charging points across the globe is evident with approximately 5.2 million at the end of 2018, in other words, up to 44% increase from 2017. It is worth noting that the private sector contributed for more than 90% of the 1.6 million installations in 2018.[1]

The growth of the EVs cannot be sustained without the technology advances that are delivering substantial cost cuts. Very crucial technologies that need to be developed are the battery chemistry, the expansion of production capacity in manufacturing plants, as well as the power electronics that facilitate proper electric power conversion to charge the batteries.

The power electronics are part of the charger that supplies energy to the battery. These chargers can be categorized into two groups: the on-board and off-board chargers. The difference between the two is that the former is a part of the EV whereas the latter is part of a charging station. There are similar challenges when designing each of them, with the most important being the efficiency, power density and cost. For the on-board chargers, the size and weight are crucial since they affect directly the performance of the EV.

As can be seen in Fig.1.1, the off-board charger's main objective is to convert the electric power from AC-to-DC, therefore it is an intermediate step between the AC grid and the DC input of the battery. The sub-systems of the charger are the EMI filter, the PFC rectifier, the DC-bus and finally, a DC-DC converter that provides the right level of power to the EV battery. Starting from left to right in Fig.1.1, the EMI filter is useful to eliminate the high frequency components of the AC current produced by the HF switching of the PFC rectifier. This is necessary because there are certain IEC standards with whom the charger has to comply. Next, the PFC rectifier converts the electric power from AC-to-DC and at the same time delivers unit power factor. The DC-Link is actually maintaining a constant DC voltage

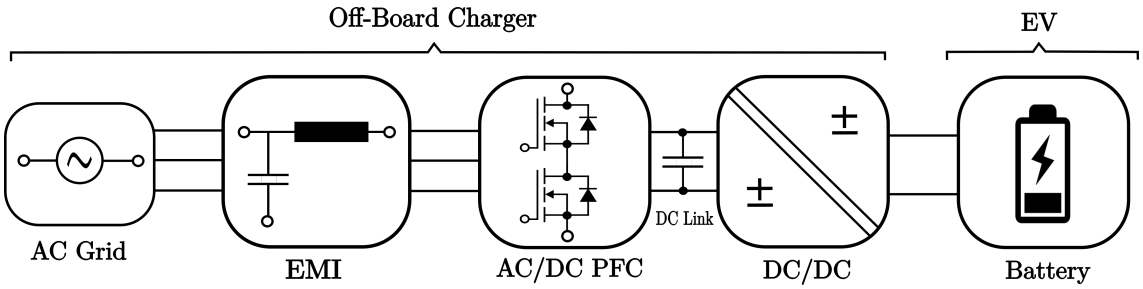


Figure 1.1: Block diagram of an off-board charger with its main parts.

which is connected to the input of a DC-DC converter. The latter introduces isolation between the grid-rectifier and the battery, as well as the option to increase or decrease the output power according to the charging state of the EV battery.

This work is focused on the investigation of a novel 3-phase PFC rectifier that consists of a semi-active rectification stage and an integrated active boost stage which is called the Belgian Rectifier. The Belgian Rectifier can be used in off-board and on board chargers due to its advantages regarding efficiency, power density, as well as its ability to operate with a 3-phase or 1-phase voltage input [25, 29]. This topology is analyzed mathematically, modelled in steady-state, as well as during dynamic transients and finally, it is compared to another boost-type PFC rectifier, namely the Six-Switch Boost.

1.2. Objective

The objective of this project is to model and design a recently proposed boost-type 3-phase PFC rectifier, named the Belgian Rectifier. In particular regarding the efficiency versus power density trade-off, a complete evaluation of the Belgian Rectifier will be conducted and conclusions will be drawn about its advantages for applications in EV chargers. The application however, can also be different such as DC motor drive systems, MRI systems in healthcare and basically all applications that require a constant DC voltage supply.

More specifically, the research objectives of this project are the following:

- *Describe the operational principle of the Belgian Rectifier mathematically and derive a proper modulation scheme that provides the smallest possible stresses on the components and as much as possible zero-voltage switching.*
- *Investigate what are the capabilities of the Belgian Rectifier regarding efficiency and power density for the use case of an off-board charger.*
- *Compare the Belgian Rectifier to a similar 3-phase boost-type PFC topology to make a final evaluation.*

In order to reach these research objectives, a certain methodology has to be followed for the most efficient results. After understanding the operation of the ”unconventional” Belgian Rectifier, a steady-state model is formulated. Secondly, the derivation of an appropriate modulation scheme that facilitates low component stresses is derived. Using the derived modulation scheme, all the relevant currents and voltages are calculated analytically through a Matlab model. Furthermore, detailed models for all components’ losses and volumes are used and an EMI filter design procedure is followed. Through the aforementioned Matlab models, the expected efficiency and power density of the Belgian Rectifier is calculated and a multi-objective optimization is conducted for a wide global design and component design space. Finally, the Belgian Rectifier is compared in terms of efficiency and power density with the Six-Switch Rectifier.

1.3. Outline

Apart of the introductory chapter, the thesis report content is presented as follows.

In the *second* chapter, a literature review of relevant subjects is organized. The conventional six-switch boost-type rectifier is described in order to introduce the reader to a topology that is in the same category as the Belgian Rectifier. Secondly, the fundamental concept of zero-voltage switching (ZVS) is explained in detail, in particular how it applies in the operation of the topology under investigation.

In the *third* chapter, the topology of the Belgian Rectifier is explained in detail. More specifically, by separating the full topology into individual blocks, each one of them is described in terms of functionality. Secondly, in-depth analysis of the operation of the topology is done and an average model is developed. Finally, using the average model, an appropriate modulation scheme is derived and its advantages are explained in terms of semiconductor stresses and switching losses.

In the *fourth* chapter, the closed-loop control is explained. Starting from the control scheme itself, an overview of the strategy that is followed is presented. Moreover, the actual model implemented in Simulink/Matlab is analyzed briefly and finally, the results of that model are shown and discussed.

In the *fifth* chapter, the analytical models that are built or used are explained in detail. More specifically, starting from the approach that is followed, the separate models of different components such as the semiconductors, inductors and EMI filter are discussed. Finally, the efficiency and volume models that give an overview of the converter are analyzed in detail.

In the *sixth* chapter, the models that are described in chapter 5 are used to create a virtual prototyping routine that gives the optimal design of the converter. The design space of the multi-objective optimization is explained and the optimal performance of the converter regarding efficiency and power density is demonstrated.

In the *seventh* chapter, the Belgian Rectifier is compared in terms of semiconductor stresses, semiconductor losses, peak stored enerfy of the boost inductors and EMI filter volume with the Six-Switch Rectifier. Therefore, a comparative evaluation is conducted which reveals the advantages of the Belgian Rectifier.

In the *eighth* chapter, the conclusions of this project together with some recommendations are summarized.

2

Literature review

2.1. Introduction

In this chapter, a literature review of relevant topics to the Belgian rectifier is provided. The three-phase boost-type PFC rectifiers that are mostly used in the industry like the six-switch boost PFC rectifier and the Vienna rectifier will be presented to introduce the reader with similar topologies and an average model will be formulated for the former. Starting from the basics, the function of the rectifier is to convert the 3-phase AC voltage of the grid into a DC voltage. This project is mostly focused on chargers for battery charging, but the aforementioned rectifiers can be also used in other cases such as wireless charging systems for electric cars or gradient amplifiers for Magnetic Resonance Imaging (MRI) scanners where there is typically a need to create a high-voltage DC bus from a three-phase AC input.

The phase and spectrum of the current that is drawn from the AC side of the converter are significant since they define the power factor which indicates the grid pollution that the converter adds to the grid. In Fig.2.1(a), the desired waveforms of AC voltage and current are presented, whereas Fig.2.1(b),(c) depicts the cases that need to be avoided. The PFC, which stands for power factor correction, makes sure that the power factor of the rectifier is unit, therefore the apparent power is equal to the active power. Moreover, the term ”boost-type” in the name of this category of rectifiers means that the output DC voltage is higher than full-wave rectified mains voltage, and there is always a boost circuit that is controlled by pulse width modulation control signals.

Significant for the evaluation of a certain converter is the efficiency and power density. Since the project investigates a topology with high-frequency PWM control, the switching losses play a crucial role for the overall evaluation of that converter. More specifically, in order to increase the power density, the switching frequency needs to be increased, so that the stored energy in the magnetic components is decreased together with their size. But, the switching losses are proportional to the operating frequency, therefore there is a trade-off between switching losses and power density. To tackle this problem, soft switching is often desired in order to minimize the switching losses and be able to increase more the frequency further. In particular, zero-voltage switching is explained in a later section.

2.2. Three-phase boost-type PFC rectifiers

The three-phase PFC rectifier systems are classified into hybrid and fully active pulsewidth modulation boost-type and buck-type. This section will focus on the boost-type rectifiers since the Belgian rectifier falls in that category. As can be seen in Fig.1.1, the stages of the power supply to high-power electrical systems such as EV batteries, is executed in two steps, i.e., the rectification and boosting of the AC voltage is conducted by the PFC rectifier and the adaptation of the DC voltage to the load is performed by a DC-DC converter like the DAB which provides galvanic isolation.[12]

In the main objectives of a PFC rectifier, except rectifying the AC voltage to DC, is to draw sinusoidal current from each phase with the same phase as the voltages and with minimal high-frequency distortion. That said, the power factor λ, the fundamental current-to-voltage displacement factor $cos(\Phi)$ and

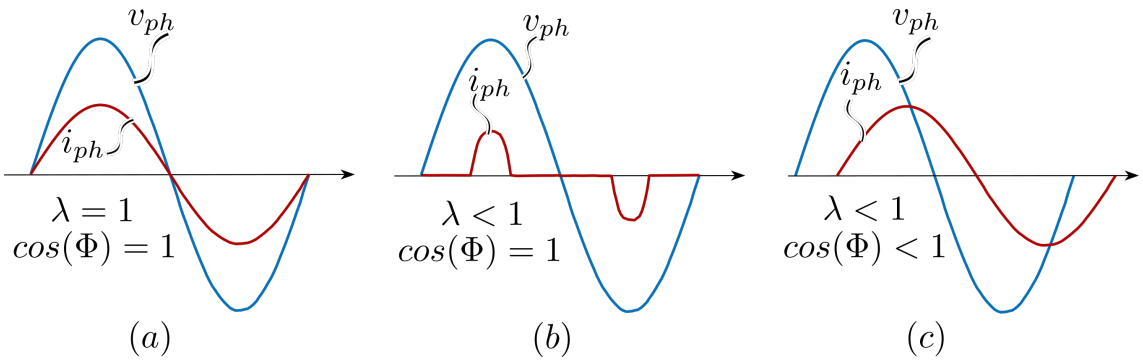


Figure 2.1: AC side phase voltage v_{ph} and phase current i_{ph} for different values of power factor λ and displacement factor Φ.

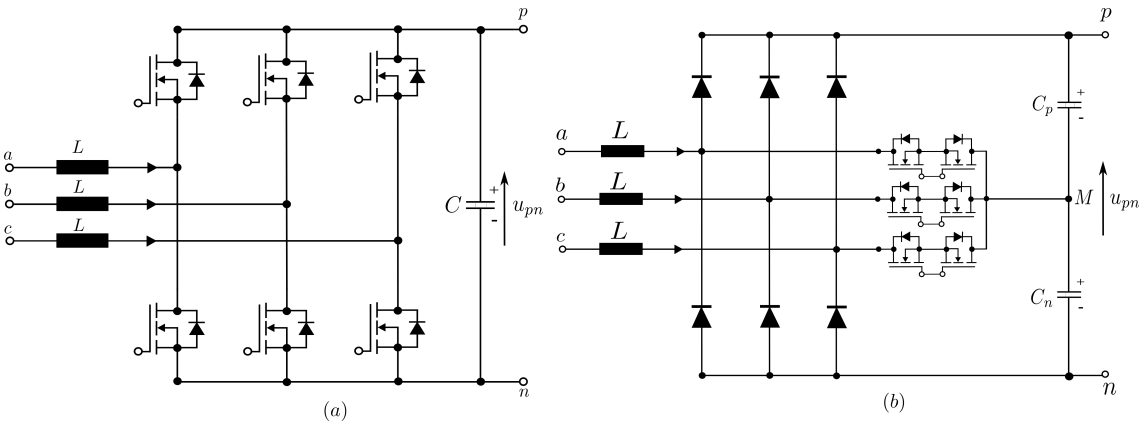


Figure 2.2: Circuit topologies of (a) Six-switch boost-type PFC rectifier (bidirectional power flow) and (b) Vienna Rectifier (unidirectional power flow).

the total harmonic distortion of the input current THD_i are the factors that describe the mains behavior. The three quantities are related to each other by the equation

$$\lambda = \frac{1}{\sqrt{1 + THD_i^2}} cos(\Phi) \tag{2.1}$$

In order to limit the voltage distortions that arise from the excitation of resonances in the distribution grid or the voltage drops across the inner inductive mains impedance, a $THD_i < 5\%$ is required in vehicle charging applications. In other applications such as aircraft power supplies, where high inner mains impedance take place anyway, the limit becomes more stringent to the level of $THD_i < 3\%$ [12]. The THD_i can be calculated with the following equation

$$THD_i = \frac{\sqrt{\sum_{h_2}^{h_{max}} I_h^2}}{I_1} [\%] \tag{2.2}$$

Two of the boost-type rectifiers that are extensively used in the industry are the six-switch boost PFC rectifier and the Vienna rectifier whose topologies can be seen in Fig.2.2. The two topologies that are presented in Fig.2.2 are preferred in the industry for several features, i.e., ohmic fundamental mains behavior, controlled dc output voltage that can be higher than the amplitude of the line-to-line input voltage, no galvanic isolation, circuit topology with phase/bridge symmetry [12], simple modulation and control scheme and the possibility for high efficiency. The first major difference between Vienna and six-switch boost is that the former is a 3-level rectifier and the latter is a 2-level rectifier. That said, the Vienna Rectifier(VR) provides the highest degree of freedom in modulation due to its three-level characteristic. The switching losses of VR are lower than those of six-switch boost since the commutation voltage of the transistors is half of the commutation voltage of the six-switch boost rectifier.

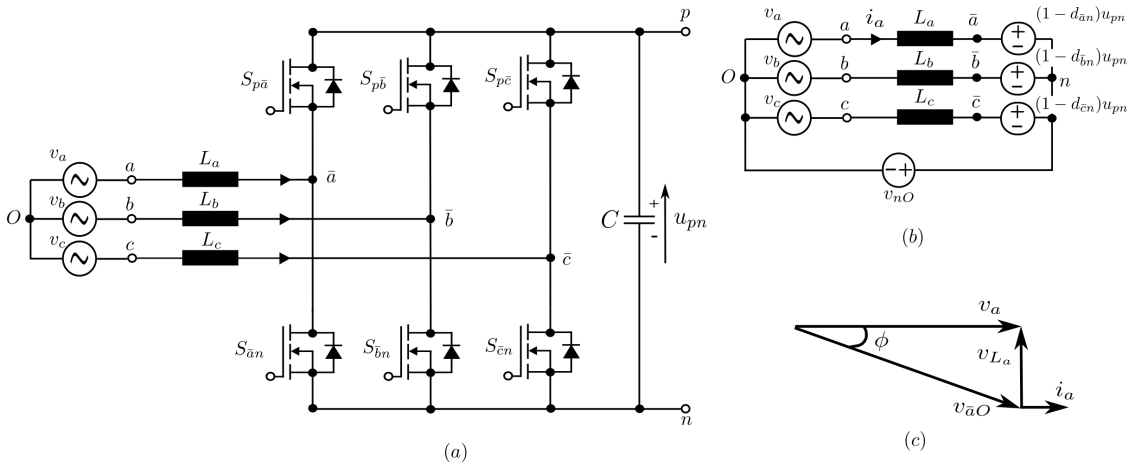


Figure 2.3: (a) Circuit topologies of six-switch boost-type PFC rectifier (bidirectional power flow), (b) Average model of the rectifier and (c) a phasor diagram for phase a.

Thereby, 650-V switches can be used for the VR instead of 1200-V switches. The main advantage of the three-level characteristic of the VR is the lower volume of the boost inductors compared to the two-level six-switch boost rectifier. On the other hand, the advantage of the six-switch boost is the simple structure of its power circuit. However, VR provides smaller volume due to its high power density [27].

2.2.1. Six-switch boost PFC rectifier

In this section, the six-switch boost rectifier will be described and the average model will be derived.[3]. This rectifier is widely used in the industry because of its advantages such as high efficiency and simplicity. The topology of the active six-switch boost-type PFC rectifier that enables bidirectional power flow is shown in Fig.2.3(a). In particular, the voltage over the switches can be formed independent of the current, since for a switched-on MOSFET, the current flows through the transistor or its antiparallel diode at all times. At the bridge leg midpoint a positive or negative voltage can be generated referred to the virtual output voltage midpoint, therefore a two-level PWM voltage is applied which can facilitate the impression of sinusoidal phase currents of any displacement compared to the phase voltages. That said, the sinusoidal currents can be formed in antiphase with the phase voltages, thus achieving the opposite power flow. In that case, the topology can be used in variable speed AC machine drives and can allow to feed back the braking energy into the mains [12].

Therefore, the simplicity combined with the high performance and features such as the bidirectionality of power flow without the need for a higher number of switches, makes the six-switch boost PFC rectifier a very appealing option for industrial applications. On the other hand, however, the fact that the full DC-bus voltage is switched is translated into high stresses on the semiconductors, as well as the need for larger passive components. The semiconductors need to have a rated voltage higher than DC-bus voltage, therefore the losses will be higher than what would be in semiconductors which are rated to half DC-bus voltage. Moreover, the switching of the full output voltage makes necessary, not only larger boost inductors, but also larger EMI filter. These facts decrease the overall performance and power density of the converter.

Average model:

The average model of the six-switch boost-type PFC rectifier is shown in Fig.2.3(b) [3]. Duty-cycle $d_{\bar{a}n}$ is corresponding to switch $S_{\bar{a}n}$, likewise for all the other switches. The average voltages at the nodes $\bar{a}$,$\bar{b}$,$\bar{c}$ to n are shown in (2.3).

$$\begin{cases} \langle v_{\bar{a}n} \rangle = (1 - d_{\bar{a}n}) \cdot u_{pn} \\ \langle v_{\bar{b}n} \rangle = (1 - d_{\bar{a}n}) \cdot u_{pn} \\ \langle v_{\bar{c}n} \rangle = (1 - d_{\bar{a}n}) \cdot u_{pn} \end{cases} \tag{2.3}$$

The average voltage over an inductor during a switching cycle is considered to be zero $v_L = 0$, therefore the average voltage at the nodes $\bar{a},\bar{b},\bar{c}$ referred to O are shown in (2.4).

$$\begin{cases} \langle v_{\bar{a}O} \rangle = \langle v_a \rangle = \sqrt{2} V_{RMS} \cdot sin(\omega t) \\ \langle v_{\bar{b}O} \rangle = \langle v_b \rangle = \sqrt{2} V_{RMS} \cdot sin(\omega t - 120^o) \\ \langle v_{\bar{c}O} \rangle = \langle v_c \rangle = \sqrt{2} V_{RMS} \cdot sin(\omega t + 120^o) \end{cases} \tag{2.4}$$

It is assumed that the three-phase system is symmetric, thus

$$v_a + v_b + v_c = 0 => \langle v_{\bar{a}O} \rangle + \langle v_{\bar{b}O} \rangle + \langle v_{\bar{c}O} \rangle = 0 \tag{2.5}$$

Now, the voltages at nodes $\bar{a},\bar{b},\bar{c}$ referred to the neutral point, are derived from the voltage law in a closed loop as follows

$$\begin{cases} \langle v_{\bar{a}O} \rangle = \langle v_{\bar{a}n} \rangle + \langle v_{nO} \rangle \\ \langle v_{\bar{b}O} \rangle = \langle v_{\bar{b}n} \rangle + \langle v_{nO} \rangle \\ \langle v_{\bar{c}O} \rangle = \langle v_{\bar{c}n} \rangle + \langle v_{nO} \rangle \end{cases} \tag{2.6}$$

(2.5) together with (2.6) gives

$$-\frac{1}{3}(\langle v_{\bar{a}n} \rangle + \langle v_{\bar{b}n} \rangle + \langle v_{\bar{c}n} \rangle) = \langle v_{nO} \rangle \tag{2.7}$$

Therefore,

$$\begin{cases} \langle v_a \rangle = \langle v_{\bar{a}n} \rangle - \frac{1}{3}(\langle v_{\bar{a}n} \rangle + \langle v_{\bar{b}n} \rangle + \langle v_{\bar{c}n} \rangle) \\ \langle v_b \rangle = \langle v_{\bar{b}n} \rangle - \frac{1}{3}(\langle v_{\bar{a}n} \rangle + \langle v_{\bar{b}n} \rangle + \langle v_{\bar{c}n} \rangle) \\ \langle v_c \rangle = \langle v_{\bar{c}n} \rangle - \frac{1}{3}(\langle v_{\bar{a}n} \rangle + \langle v_{\bar{b}n} \rangle + \langle v_{\bar{c}n} \rangle) \end{cases} \tag{2.8}$$

If (2.3) is combined with (2.8), a relationship between the duty cycles and phase voltages can be derived.

$$\begin{bmatrix} -\frac{2}{3} & \frac{1}{3} & \frac{1}{3} \\ \frac{1}{3} & -\frac{2}{3} & \frac{1}{3} \\ \frac{1}{3} & \frac{1}{3} & -\frac{2}{3} \end{bmatrix} \cdot \begin{bmatrix} d_{\bar{a}n} \\ d_{\bar{b}n} \\ d_{\bar{c}n} \end{bmatrix} = \frac{1}{v_{pn}} \begin{bmatrix} \langle v_a \rangle \\ \langle v_b \rangle \\ \langle v_c \rangle \end{bmatrix} \tag{2.9}$$

(2.9) relates the average duty cycle ratio of the switches to the line voltages. There are infinite solutions to this equation, therefore a possible solution can be:

$$\begin{cases} d_{\bar{a}n} = K_1 + K_2 \cdot \frac{\langle v_a \rangle}{v_{pn}} \\ d_{\bar{b}n} = K_1 + K_2 \cdot \frac{\langle v_b \rangle}{v_{pn}} \\ d_{\bar{c}n} = K_1 + K_2 \cdot \frac{\langle v_c \rangle}{v_{pn}}) \end{cases} \tag{2.10}$$

The parameter $K_2 = -1$ and K_1 can be chosen such that it fulfills the following condition in order to maintain the duty cycles in the range of [0,1].

$$0 \leq d_{\bar{a}n} = K_1 - \frac{\langle v_a \rangle}{v_{pn}} \leq 1 \tag{2.11}$$

From the above equation, the parameter K_1 is 0.5 for a LF common-mode voltage $\langle v_{nO} \rangle = 0$. Therefore, the duty cycle and phase voltage relation is the following:

$$\begin{cases} d_{\bar{a}n} = 0.5 - \frac{\langle v_a \rangle}{v_{pn}} \\ d_{\bar{b}n} = 0.5 - \frac{\langle v_b \rangle}{v_{pn}} \\ d_{\bar{c}n} = 0.5 - \frac{\langle v_c \rangle}{v_{pn}}) \end{cases} \tag{2.12}$$

2.3. Zero-voltage switching

SiC MOSFETS and GaN HEMTs have facilitated an increase of the performance of power electronics in general because of the enhanced figure-of-merit [10].

$$FOM = \frac{1}{\sqrt{R_{DS,on} \cdot C_{oss}}} \tag{2.13}$$

Despite the improved performance that these wide-bandgap semiconductors provide, the switching losses increase as the frequency increases, thus it constitutes a limiting factor even for these semiconductors. Therefore, soft-switching is often preferred and, for the design and optimization of a converter, it is important to identify the conditions under which soft switching (i.e. by means of zero-voltage switching) can be achieved.

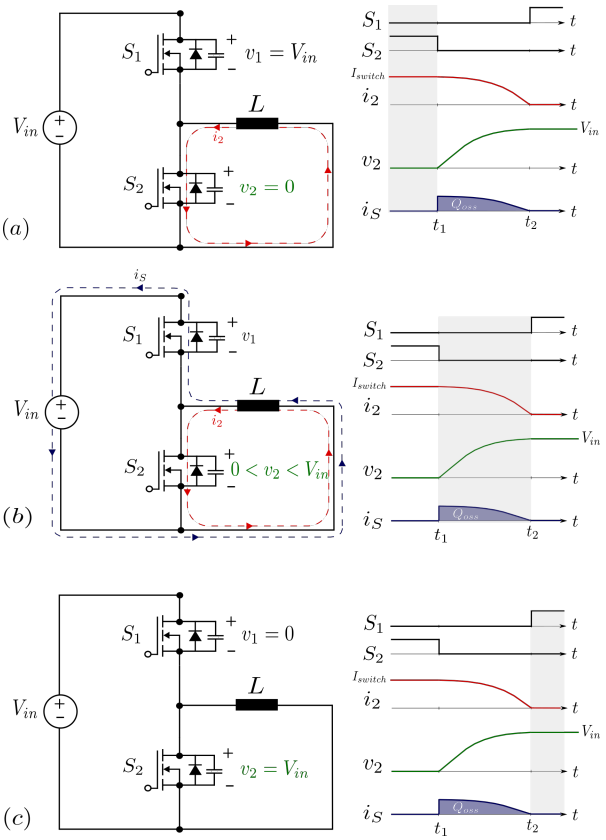


Figure 2.4: Soft-switching transition of a MOSFET bridge leg: (a) Switch S_2 on and inductor current $i_L = I_{switch}$; (b) switch S_2 turns off and resonant transition initiates with added current path through the voltage source; (c) v_2 has reached the V_{in} and switch S_1 turns on at zero voltage.

The ZVS process where the switch S_2 turns off and switch S_1 turns on can be seen in Fig.2.4. In order to achieve soft switching the following energy balance has to be valid as can be seen in (2.14) [17].

$$E_{init} + E_{del} = E_{final} + E_{diss} \tag{2.14}$$

where E_{init} is the energy within the system before t_1, E_{final} is the energy after the switching took place, E_{del} is the energy delivered by the source and E_{diss} is the energy dissipated during the ZVS - it is considered zero for full soft-switching.

$t < t_1$:

As can be seen in Fig.2.4(a), before the switching transition starts happening, the current of the inductor is free-wheeling through switch S_2 which is on. The output capacitance of the switch S_1 is charged to the source voltage V_{in}. Therefore, the system energy is defined by the energy stored in the inductor L and the paracitic capacitance as follows:

$$E_{init} = E_{oss}(V_{in}) + \frac{1}{2} L I_{switch}^2 \tag{2.15}$$

$t_1 < t < t_2$:

When the switch S_2 turns off, the inductor current starts flowing to both parasitic capacitances of the switches S_1 and S_2, thus discharging the capacitance $C_{oss,1}$ and charging $C_{oss,2}$. Since both switches of the bridge are assumed to have the same parasitic capacitances, the charging/discharging is considered to finish at the same time t_2 when the inductor current reaches $i_L = 0A$. In order to achieve full ZVS, switch S_1 has to be turned on after the corresponding parasitic capacitance has been fully discharged. This resonant transition is illustrated in Fig.2.4(b). That said, the system energy after the transition is:

$$E_{final} = E_{oss}(V_{in}) \tag{2.16}$$

and the energy that was delivered from the source V_{in} is:

$$E_{del} = -Q_{oss}(V_{in}) \times V_{in} \tag{2.17}$$

$t > t_2$:

Therefore, in order to accomplish full ZVS the following relation has to be valid:

$$\frac{1}{2} L I_{switch}^2 \geq Q_{oss}(V_{in}) \times V_{in} \tag{2.18}$$

In other words, for a constant dead-time that is defined beforehand, the current has to be sufficiently negative to discharge fully the parasitic capacitance of the switch which is turning on [17].

2.4. Summary

In this section, a literature review of the relevant topics regarding the three-phase boost type PFC rectifiers is given. Starting from the main objectives of the PFC rectifiers, two of the most widely used boost topologies, namely the six-switch boost and the Vienna Rectifier are briefly explained to introduce the reader to this category of converters. The average model of the six-switch rectifier is derived.

Furthermore, the concept of zero-voltage switching is explained by giving an example of a bridge-leg with a voltage source and an inductor whose current is assumed to go to zero.

3

The Belgian rectifier

3.1. Introduction

In this chapter, the Belgian Rectifier is described in detail. Starting from the structure of this novel topology, its separate parts are presented and explained in terms of functionality and operation. Furthermore, the conduction states of this rectifier are shown and information is provided of why this topology is classified as a three-level PFC rectifier. To continue with, two modulation schemes are examined, the average model for these modulations is formulated mathematically and the duty-cycles are derived. One of the modulation schemes is selected and its advantages are presented. Finally, the component stresses of the semiconductors, soft-switching capabilities are shown and the advantages/disadvantages of the Belgian Rectifier are analysed.

3.2. Structure

In Fig.3.2, the topology of the Belgian Rectifier is presented. Starting from the left of the topology, there are three boost inductors that are part of a boost circuit which is virtually integrated with a three phase bridge rectifier stage to allow the formation of a pulsed voltage at the rectifier output. The topology consists of ten switching elements (e.g. MOSFETs) which are actively or semi-actively controlled, six of them being part of the semi-active rectifier stage and four of them being part of the top and bottom active boost converters.[6]

Boost bridges:

The boost circuit semiconductor switches $S_{p\bar{x}}$, $S_{\bar{x}m}$, $S_{m\bar{y}}$, $S_{\bar{y}n}$ are actively controlled in order to obtain a switched voltage between 0 V and half DC bus voltage of the corresponding capacitor. This facilitates to control the current of two out of three phases, the ones that have the highest and lowest voltage levels. The top and bottom converters can be analyzed independently and their task is to provide the average voltages $\langle v_{\bar{x}m} \rangle$ and $\langle v_{\bar{y}m} \rangle$ that can be seen in Fig. 3.3.

Rectifier stage:

The rectifier stage consists of three bridge-legs $S_{\bar{x}\bar{a}}$, $S_{\bar{a}\bar{y}}$, $S_{\bar{x}\bar{b}}$, $S_{\bar{b}\bar{y}}$, $S_{\bar{x}\bar{c}}$, $S_{\bar{c}\bar{y}}$, with each phase connected to the corresponding midpoint $\bar{a}$, $\bar{b}$, $\bar{c}$. As mentioned above, the current of two out of three phases with the highest and lowest voltage are controlled by the active boost circuits. The corresponding bridge legs of the rectifier connected to the three-phase input voltage are in selection state. In Fig. 3.1, in the interval $[\frac{\pi}{2}, \frac{5}{6}\pi]$, phases A and C have the highest and lowest voltages, respectively. The remaining bridge leg is connected to the third phase which has an intermediate voltage level (phase B in the same interval in Fig.3.1) between the highest and lowest voltages and is actively controlled by PWM modulation in contrary to the other two bridge legs of the rectifier stage.

Boost Inductors:

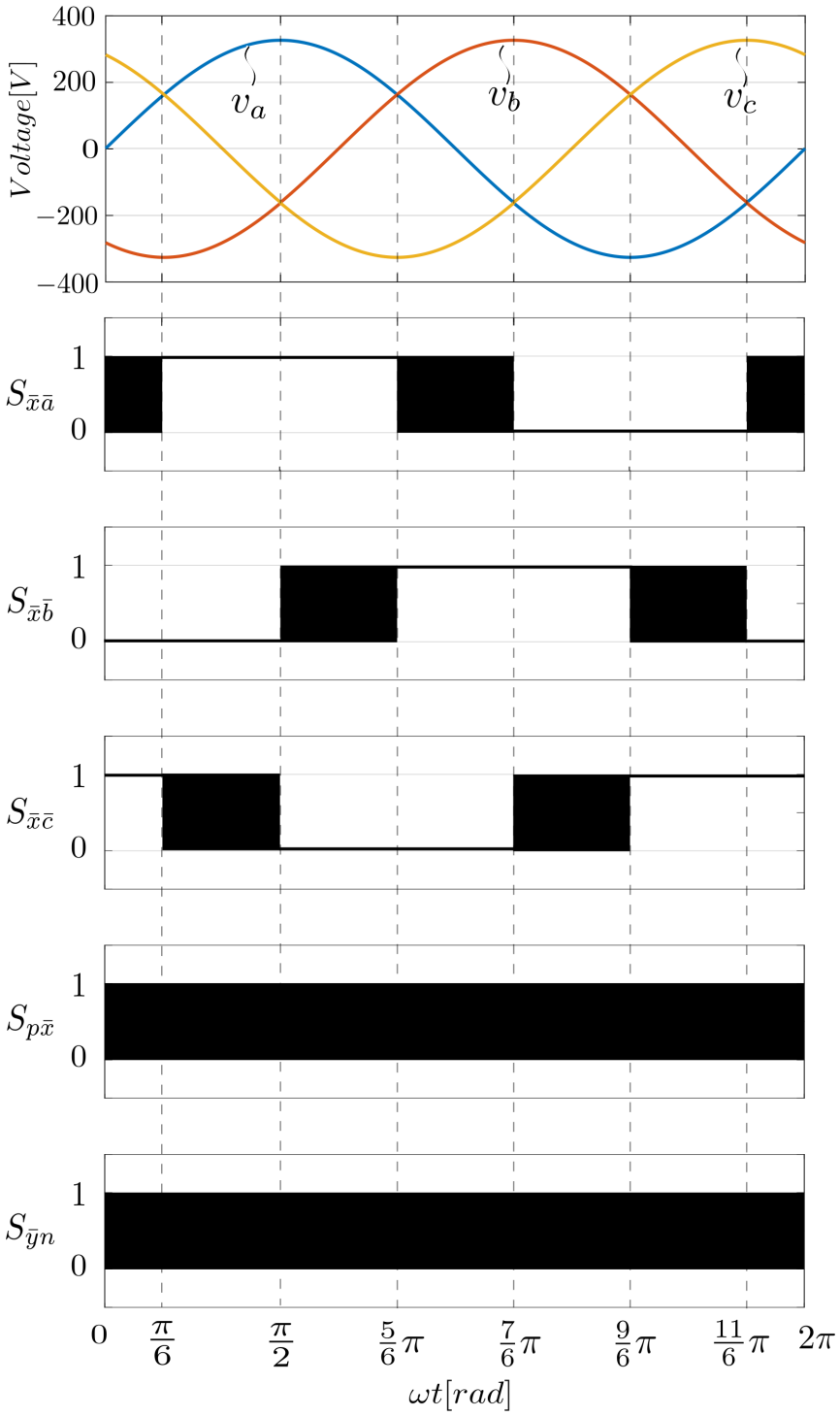


Figure 3.1: Phase voltages and switching states (PWM signals) during a 2π period of the AC mains voltage.

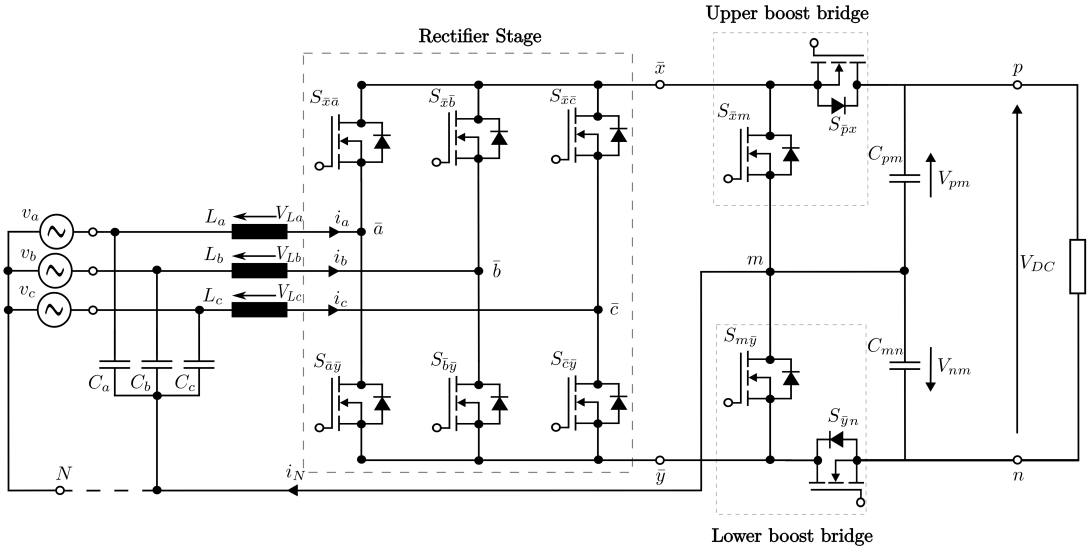


Figure 3.2: Topology of the Belgian Rectifier.

The boost inductors are located between the three-phase AC mains and the rectifier stage. The fact that they are not located after the rectification stage gives the flexibility to exploit the pulsed voltage for the current control to the maximum. It should be noted that the controlling voltage over the inductor is half the DC bus voltage for the phases in selection state and multi-level voltage for the phase with intermediate voltage. This allows for smaller inductors to be used since less magnetic energy is needed to be stored compared to the conventional six-switch boost rectifier.

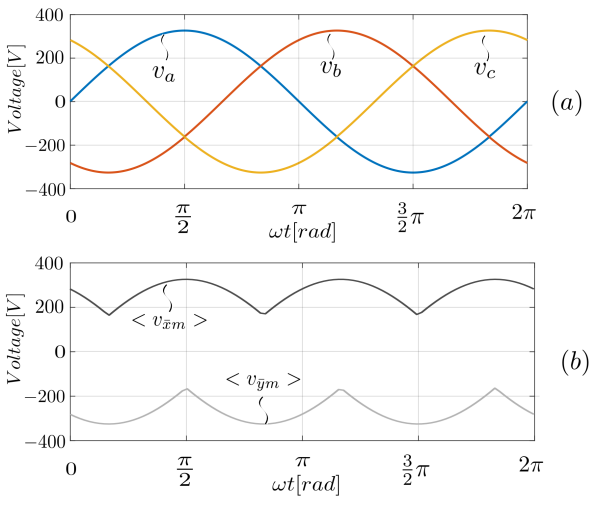


Figure 3.3: (a) Input three-phase AC voltage (b) Average voltages $\langle v_{\bar{x}m} \rangle$, $\langle v_{\bar{y}m} \rangle$.

Moreover, an advantage of the Belgian Rectifier is that the boost circuits are actively switching the voltages v_{pm} and v_{nm} which are half the DC bus in contrary to the six-switch boost-type rectifier whose bridge legs are actively switching the full DC bus.

3.2.1. Conduction states

The conduction states of only phase A are shown in Fig.3.4. It can be assumed that the same conduction states are possible for phases B, C and their respective bridge legs in the rectifier stage. As can be seen in Fig.3.4, there are four possible conduction states for phase A. When the top switch $S_{\bar{x}\bar{a}}$ is on, the voltage over the inductor L_a is determined by the switched voltage $v_{\bar{x}m}$ which can either be 0 V or v_{pm}, as well as by the phase voltage v_a and LF common-mode voltage v_{mN}.

When the bottom switch $S_{\bar{a}\bar{y}}$ is on, the voltage over the inductor is dependent on the switched voltage $v_{\bar{y}m}$ which can either be $0V$ or v_{nm}, the phase voltage v_a and LF common-mode voltage v_{mN}. It is obvious at this point that the voltage at the midpoint $v_{\bar{a}m}$ can have three possible values, namely $v_{\bar{a}m} = v_{nm} = -\frac{V_{DC}}{2}$, $v_{\bar{a}m} = 0$ and $v_{\bar{a}m} = v_{pm} = \frac{V_{DC}}{2}$. Therefore, the Belgian Rectifier is a three-level rectifier and enjoys low ripple and component stresses.

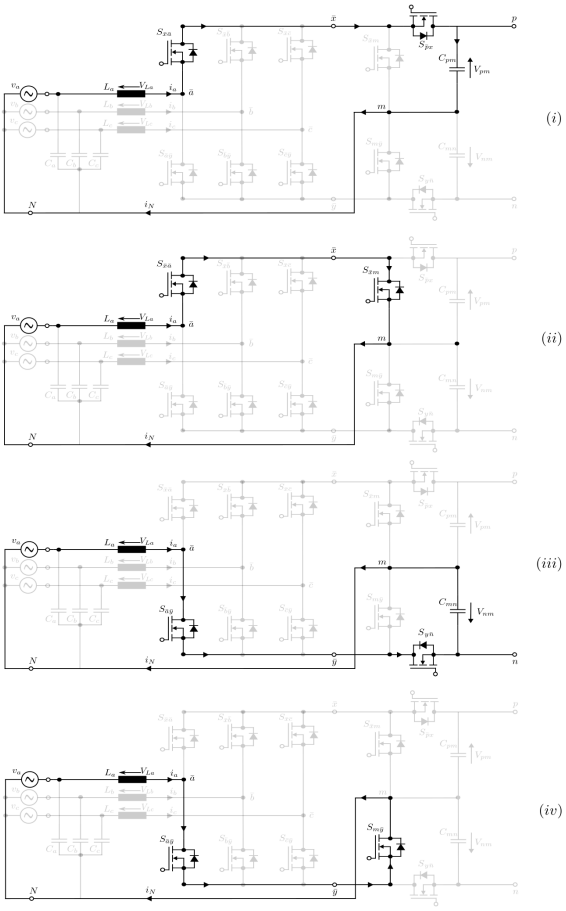


Figure 3.4: Possible conduction states considering only phase A.

It is assumed that the voltage v_{mN} is zero, so that the analysis is more clear for the reader.

$$v_{mN} = 0 \tag{3.1}$$

The voltage over the inductor L_a for different conduction states is the following:

$$\begin{cases} v_{L_a} = v_a - v_{pm} & \text{for state } (i) \\ v_{L_a} = v_a & \text{for states } (ii),(iv) \\ v_{L_a} = v_a - v_{nm} & \text{for state } (iii) \end{cases} \tag{3.2}$$

3.3. Average model

To derive an average model for the Belgian Rectifier, certain assumption have to be made. Firstly, the switching frequency f_{sw} of the semiconductors is considered high frequency (HF) whereas the grid frequency f_{grid} is considered to be low frequency (LF). Moreover, HF is considered to be much higher than LF $f_{sw} >> f_{grid}$. Therefore, it can be assumed that in a switching cycle, the average voltage over an inductor is zero $\langle v_L \rangle = 0$. The methodology that is followed in this mathematical approach starts from the boost circuits and later continues to the rectifier stage. Hence, the boost circuits are the first ones to be analysed in steady-state.

Boost Circuit:

As aforementioned, the top and bottom boost circuit can be analysed independently from each other. As can be seen in Fig.3.3, the rectified average voltages $v_{\bar{x}m}$ and $v_{\bar{y}m}$ can be defined as follows:

$$\begin{cases} \langle v_{\bar{x}m} \rangle = max(v_a, v_b, v_c) \\ \langle v_{\bar{y}m} \rangle = min(v_a, v_b, v_c) \end{cases} \tag{3.3}$$

The switching-cycle-averaged values are the following:

$$\begin{cases} v_{pm} = \langle v_{pm} \rangle \\ v_{nm} = \langle v_{nm} \rangle \\ v_{pn} = \langle v_{pn} \rangle = V_{DC} \end{cases} \tag{3.4}$$

The output DC bus voltage and the separate voltages of bulk capacitors v_{pm} and v_{mn}, can be related to the rectified voltages $v_{\bar{x}m}$ and $v_{\bar{y}m}$ through the duty cycles as follows:

$$\begin{cases} v_{pm} \cdot d_{p\bar{x}} = \langle v_{\bar{x}m} \rangle \\ v_{nm} \cdot d_{\bar{y}n} = \langle v_{\bar{y}m} \rangle \end{cases} \tag{3.5}$$

As can be seen in Fig.3.5(a), the voltage $v_{\bar{x}m}$ is a switched voltage with two levels, 0 V and v_{pm}. The average voltage $\langle v_{\bar{x}m} \rangle$ is defined from the duty cycle of the top boost circuit. Voltage $v_{\bar{y}m}$ (See Fig.3.5(b)) is a switched voltage with two levels as well, specifically 0 V and v_{nm}. Therefore, the boost circuits are

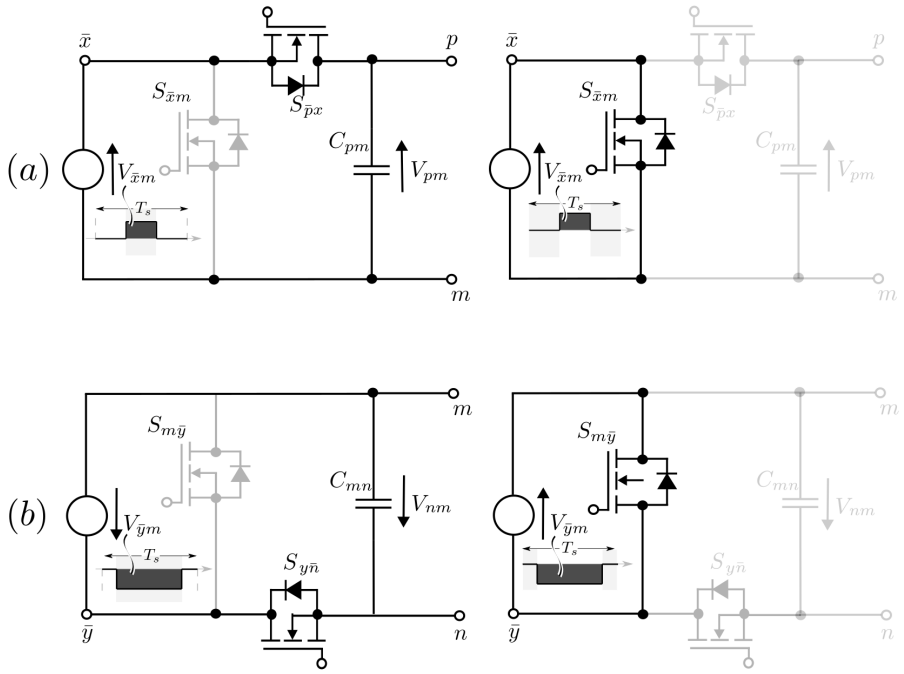


Figure 3.5: Switched voltage that is formed by the (a) top boost circuit on the nodes $\bar{x} - m$ and (b) bottom boost circuit on the nodes $\bar{y} - m$.

completely independent and are analysed as such.

Until this point of the analysis, the average model does not depend on the modulation and the phase shift of the PWM pulses, but later in the analysis, these factors contribute to the formulation of different average models and derivation of different duty cycles, particularly for the rectifier bridge leg that is in active PWM switching, which is the case when the corresponding phase voltage is the intermediate voltage. Therefore, two modulations with triangular carrier are examined, only one is chosen and its advantages over the other are pointed out.

3.3.1. Modulation 1

In this section, the modulation is explained by considering only phase A, because the same applies to the other phases with a phase shift of 120^o. As can be seen in Fig.3.6, the voltage at the output nodes $\bar{x}$ and $\bar{y}$ of the rectifier stage is the subtraction of voltages $v_{\bar{x}m}$ and $v_{\bar{y}m}$:

$$v_{\bar{x}\bar{y}} = v_{\bar{x}m} - v_{\bar{y}m} \tag{3.6}$$

If it assumed that the bridge leg of phase A is actively switching and its corresponding phase voltage is the intermediate voltage between the highest and lowest voltages as can be seen in the intervals $[0, \frac{\pi}{6}]$, $[\frac{5}{6}\pi, \frac{7}{6}\pi]$ and $[\frac{11}{6}\pi, 2\pi]$ in Fig.3.1. Then, the voltage over the switch $S_{\bar{x}\bar{a}}$ is dependent on the voltage $v_{\bar{x}\bar{y}}$ and the duty-cycle of the switch as can be seen in Fig.3.6. it is evident that there are several possible cases for the average voltage of switch $S_{\bar{x}\bar{a}}$, there is switching of a ”switched” voltage and not an average one as it happens in other PFC topologies.

The PWM control signals of interest are the ones of switches $S_{p\bar{x}}$, $S_{\bar{y}n}$ and $S_{\bar{x}\bar{a}}$. In this modulation scheme, the aforementioned PWM pulses are chosen to be aligned and centered as can be seen in Fig.3.6. Three different cases/intervals can be distinguished as can be seen in Fig.3.6(d) and those are the following:

$$\begin{cases} \langle v_{\bar{x}m} \rangle < \langle -v_{\bar{y}m} \rangle & \text{in Fig.3.6 (a)} \\ \langle v_{\bar{x}m} \rangle > \langle -v_{\bar{y}m} \rangle & \text{in Fig.3.6 (b)} \\ \langle v_{\bar{x}m} \rangle = \langle -v_{\bar{y}m} \rangle & \text{in Fig.3.6 (c)} \end{cases} \tag{3.7}$$

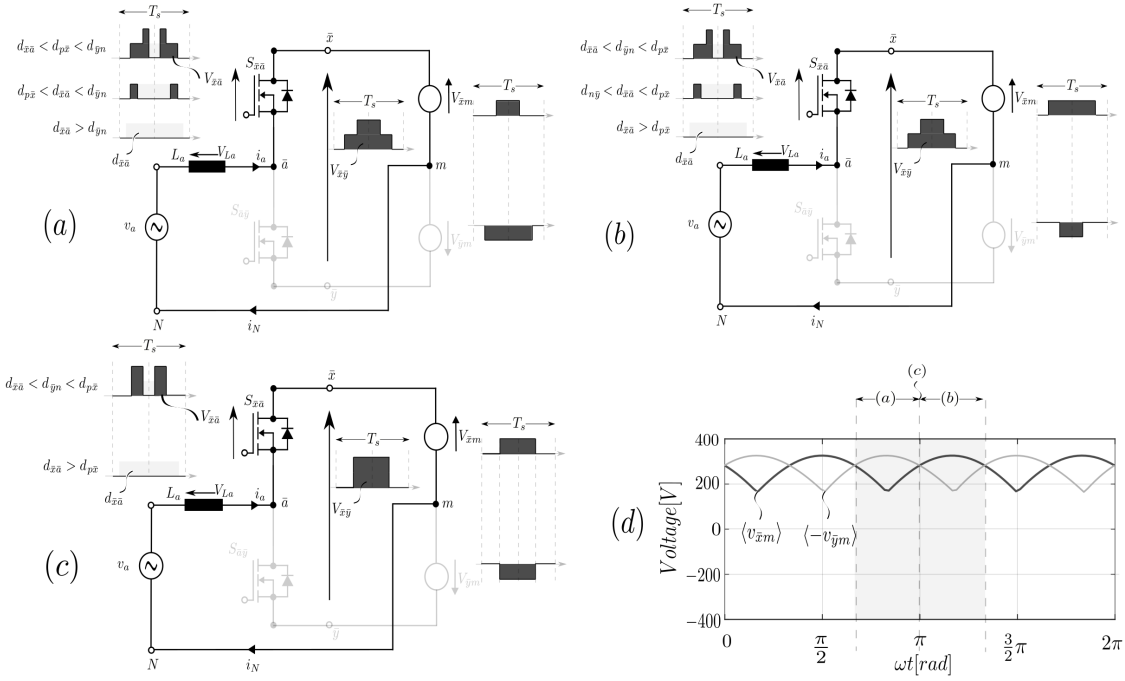


Figure 3.6: Switched voltages for cases (a) $\langle v_{\bar{x}m}\rangle < \langle -v_{\bar{y}m}\rangle$ (b) $\langle v_{\bar{x}m}\rangle > \langle -v_{\bar{y}m}\rangle$ (c) $\langle v_{\bar{x}m}\rangle = \langle -v_{\bar{y}m}\rangle$ and (d) the relevant intervals.

Starting from the case where $\langle v_{\bar{x}m}\rangle < \langle -v_{\bar{y}m}\rangle$. The average voltage over the switch $S_{\bar{x}\bar{a}}$ depends on the duty cycle of the corresponding switch and the switched voltage of the nodes $v_{\bar{x}\bar{y}}$. Three states can be distinguished as can be observed in Fig.3.6(a) on the top left. The average voltage $\langle v_{\bar{x}\bar{a}}\rangle$ in these states is:

$$\langle v_{\bar{x}\bar{a}}\rangle = \begin{cases} (d_{\bar{y}n} - d_{p\bar{x}}) \cdot v_{mn} + (d_{p\bar{x}} - d_{\bar{x}\bar{a}}) \cdot (v_{pm} + v_{mn}) & \text{for } d_{\bar{x}\bar{a}} < d_{p\bar{x}} < d_{\bar{y}n} \\ (d_{\bar{y}n} - d_{\bar{x}\bar{a}}) \cdot v_{mn} & \text{for } d_{p\bar{x}} < d_{\bar{x}\bar{a}} < d_{\bar{y}n} \\ 0 & \text{for } d_{\bar{x}\bar{a}} > d_{\bar{y}n} > d_{p\bar{x}} \end{cases} \tag{3.8}$$

For the second case which is depicted in Fig.3.6(b), the average voltage $\langle v_{\bar{x}\bar{a}}\rangle$ can be calculated as follows:

$$\langle v_{\bar{x}\bar{a}}\rangle = \begin{cases} (d_{p\bar{x}} - d_{\bar{y}n}) \cdot v_{pm} + (d_{\bar{y}n} - d_{\bar{x}\bar{a}}) \cdot (v_{pm} + v_{mn}) & \text{for } d_{\bar{x}\bar{a}} < d_{\bar{y}n} < d_{p\bar{x}} \\ (d_{p\bar{x}} - d_{\bar{x}\bar{a}}) \cdot v_{pm} & \text{for } d_{\bar{y}n} < d_{\bar{x}\bar{a}} < d_{p\bar{x}} \\ 0 & \text{for } d_{\bar{x}\bar{a}} > d_{p\bar{x}} > d_{\bar{y}n} \end{cases} \tag{3.9}$$

Finally, for the third case which is depicted in Fig.3.6(c), the average voltage $\langle v_{\bar{x}\bar{a}}\rangle$ can be calculated as follows:

$$\langle v_{\bar{x}\bar{a}}\rangle = \begin{cases} (d_{p\bar{x}} - d_{\bar{x}\bar{a}}) \cdot (v_{pm} + v_{mn}) & \text{for } d_{\bar{x}\bar{a}} < d_{\bar{y}n}, d_{p\bar{x}} \\ 0 & \text{for } d_{\bar{x}\bar{a}} > d_{\bar{y}n}, d_{p\bar{x}} \end{cases} \tag{3.10}$$

3.3.2. Duty-cycle derivation

The duty cycles of the boost circuits switches $S_{p\bar{x}}$, $S_{\bar{y}n}$ are simple to derive from (3.5):

$$\begin{cases} d_{p\bar{x}} = \frac{\langle v_{\bar{x}m}\rangle}{v_{pm}} \\ d_{\bar{y}m} = \frac{\langle v_{\bar{y}m}\rangle}{v_{nm}} \end{cases} \tag{3.11}$$

To calculate the duty cycle of switch $S_{\bar{x}\bar{a}}$, Kirchhoff's voltage law has to be applied in the closed-loop that is shown in Fig.3.6 as follows:

$$\langle v_{\bar{x}\bar{a}}\rangle + \langle v_a\rangle - \langle v_{\bar{x}m}\rangle = 0 \tag{3.12}$$

Therefore, from the equations (3.8), (3.9) and (3.10) the following cases of duty cycle $d_{\bar{x}\bar{a}}$ are derived:

$$d_{\bar{x}\bar{a}} = \begin{cases} d_{\bar{y}n} - \frac{2(\langle v_{\bar{x}m}\rangle - v_a)}{v_{pm}+v_{mn}} & \text{,condition } d_{p\bar{x}} < d_{\bar{x}\bar{a}} < d_{\bar{y}n} \\ d_{p\bar{x}} - \frac{2(\langle v_{\bar{x}m}\rangle - v_a) - (d_{\bar{y}n} - d_{p\bar{x}})\cdot(v_{pm}+v_{mn})}{2(v_{pm}+v_{mn})} & \text{,condition } d_{\bar{x}\bar{a}} < d_{p\bar{x}} < d_{\bar{y}n} \\ d_{p\bar{x}} - \frac{2(\langle v_{\bar{x}m}\rangle - v_a)}{v_{pm}+v_{mn}} & \text{,condition } d_{\bar{y}n} < d_{\bar{x}\bar{a}} < d_{p\bar{x}} \\ d_{\bar{y}n} - \frac{2(\langle v_{\bar{x}m}\rangle - v_a) - (d_{p\bar{x}} - d_{\bar{y}n})\cdot(v_{pm}+v_{mn})}{2(v_{pm}+v_{mn})} & \text{,condition } d_{\bar{x}\bar{a}} < d_{\bar{y}n} < d_{p\bar{x}} \\ d_{p\bar{x}} - \frac{\langle v_{\bar{x}m}\rangle - v_a}{v_{pm}+v_{mn}} & \text{,condition } d_{\bar{x}\bar{a}} < d_{\bar{y}n} = d_{p\bar{x}} \end{cases} \tag{3.13}$$

The duty-cycle of switch $S_{\bar{x}\bar{a}}$ can be calculated using (3.13) and only one of the conditions is true at each time instance of the grid cycle.

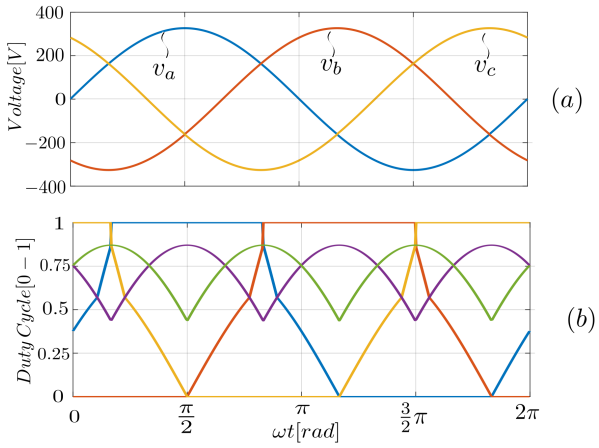


Figure 3.7: (a) Phase voltages (b) Duty cycles for switches $S_{p\bar{x}}$ - purple, $S_{\bar{y}n}$ - green, $S_{\bar{x}\bar{a}}$ - blue, $S_{\bar{x}\bar{b}}$ - red and $S_{\bar{x}\bar{c}}$ - orange.

In Fig.3.7(b), the duty cycles of all relevant switches are depicted. It can be observed that the duty cycles of the bridge legs are not symmetrical and this brings a number of disadvantages to the operation of the rectifier. The main reason is that the loss distribution in the converter and the semiconductor stresses are uneven and this increases the risk of failure of several components. Moreover, the common-mode noise with unsymmetrical PWM switching is higher, thus requiring a bigger EMI filter that decreases the overall power density and performance of the rectifier. Therefore, a second triangular carrier positioning is investigated to achieve symmetrical duty cycles in the next section.

3.3.3. Modulation 2

In this section, a second modulation scheme with different carrier positioning is presented and compared to the one described in the previous sections. The relevant PWM control pulses are again the ones of the switches $S_{p\bar{x}}$, $S_{\bar{y}n}$ and $S_{\bar{x}\bar{a}}$. In this modulation, the PWM carriers are centered, but the carriers of $S_{\bar{y}n}$ and $S_{\bar{x}\bar{a}}$ are in anti-phase compared to the carrier of $S_{p\bar{x}}$. This shift can be observed in Fig.3.8.

The voltage at the output nodes of the rectifier stage $\bar{x}$ and $\bar{y}$ is the difference of voltages $v_{\bar{x}m}$ and $v_{\bar{y}m}$ like in modulation 1, but in this case it is observed that the voltage only has two levels (with double frequency), rather than three. These levels are half and full DC-bus voltage. As can be observed in Fig.3.8 on the top left, the voltage over the switch $S_{\bar{x}\bar{a}}$ is dependent on its duty cycle and the voltage $v_{\bar{x}\bar{y}}$ that falls over that switch when it is off. Therefore, the average voltage $v_{\bar{x}\bar{a}}$ over the switch is the following:

$$\langle v_{\bar{x}\bar{a}}\rangle = \begin{cases} (d_{\bar{y}n} - d_{\bar{x}\bar{a}})\cdot v_{mn} + d_{p\bar{x}}\cdot v_{pm} & \text{for } 1-d_{\bar{y}n} < d_{p\bar{x}} < 1-d_{\bar{x}\bar{a}} \\ (1-d_{\bar{x}\bar{a}})\cdot v_{pm} + (d_{\bar{y}n} - d_{\bar{x}\bar{a}})\cdot v_{mn} & \text{for } 1-d_{\bar{y}n} < 1-d_{\bar{x}\bar{a}} < d_{p\bar{x}} \\ (1-d_{\bar{x}\bar{a}})\cdot v_{pm} & \text{for } 1-d_{\bar{x}\bar{a}} < 1-d_{\bar{y}n} < d_{p\bar{x}} \end{cases} \tag{3.14}$$

3.3.4. Duty-cycle derivation

As in the previous modulation, the duty cycles of the boost circuit switches $S_{p\bar{x}}$, $S_{\bar{y}n}$ are simple to derive from (3.5):

$$\begin{cases} d_{p\bar{x}} = \frac{\langle v_{\bar{x}m}\rangle}{v_{pm}} \\ d_{\bar{y}m} = \frac{\langle v_{\bar{y}m}\rangle}{v_{nm}} \end{cases} \tag{3.15}$$

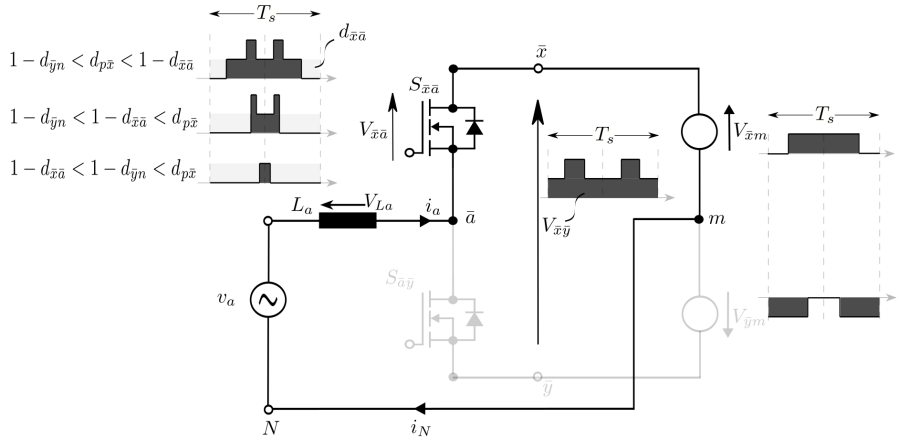


Figure 3.8: Switched voltages for the case of modulation 2.

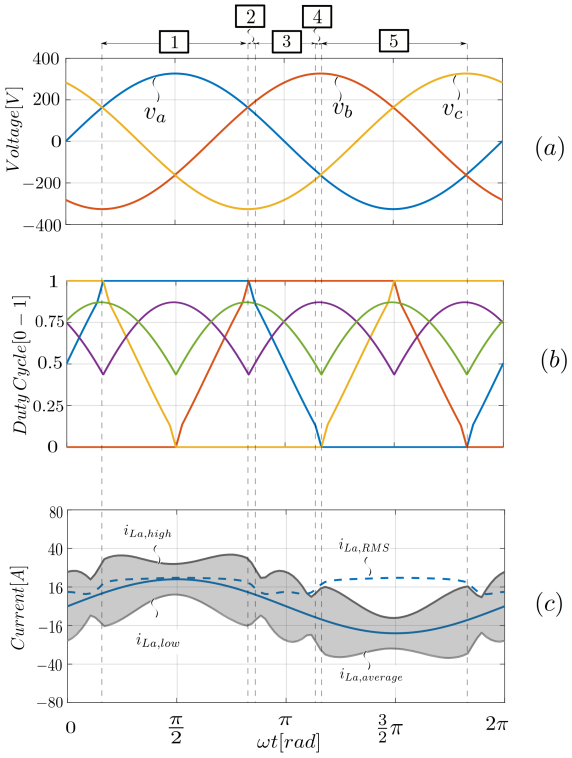


Figure 3.9: (a) Phase voltages (b) Duty cycles for switches $S_{p\bar{x}}$ - purple, $S_{\bar{y}n}$ - green, $S_{\bar{x}\bar{a}}$ - blue, $S_{\bar{x}\bar{b}}$ - red and $S_{\bar{x}\bar{c}}$ - orange (c) Inductor current for output power $P_o = 22kW$ and output voltage $V_o = 750V$.

To calculate the duty cycle of switch $S_{\bar{x}\bar{a}}$, Kirchhoff's voltage law has to be applied in the closed-loop that is shown in Fig.3.8 as follows:

$$\langle v_{\bar{x}\bar{a}} \rangle = -\langle v_a \rangle + \langle v_{\bar{x}m} \rangle = C \tag{3.16}$$

The constant C is defined to make the duty cycle equations simpler. From (3.14) the following cases of duty cycle $d_{\bar{x}\bar{a}}$ are derived:

$$d_{\bar{x}\bar{a}} = \begin{cases} d_{\bar{y}n} + \frac{d_{p\bar{x}} \cdot v_{pm} - C}{v_{mn}} & \text{,condition } 1-d_{\bar{y}n} < d_{p\bar{x}} < 1-d_{\bar{x}\bar{a}} \\ \frac{v_{pm} + d_{\bar{y}n} \cdot v_{mn} - C}{(v_{pm}+v_{mn})} & \text{,condition } 1-d_{\bar{y}n} < 1-d_{\bar{x}\bar{a}} < d_{p\bar{x}} \\ 1 - \frac{C}{v_{pm}} & \text{,condition } 1-d_{\bar{x}\bar{a}} < 1-d_{\bar{y}n} < d_{p\bar{x}} \end{cases} \tag{3.17}$$

In Fig.3.9(b), the duty cycles of all relevant switches for the three phases of the rectifier stage and the boost circuits are shown. The duty cycles of the boost circuit PWM pulses are the same as in modulation 1, because the carrier phase shift is not affecting them. On the other hand, the duty cycles of the rectifier stage switches are much different than the ones in modulation 1 as can be seen in Fig.3.7(b). On the contrary to the duty cycles of modulation 1, the ones of modulation 2 present a perfect symmetry which can be translated in a number of benefits. Firstly, the losses and stresses of the semiconductors are evenly distributed in the converter, thus making it more reliable and robust. Furthermore, the common-mode noise is significantly decreased, therefore the filtering requirement is also limited. That said, the required EMI filter can be smaller which can help improve the power density of the converter. In Fig.3.9(c), the current of the inductor can be seen. The $i_{La,high}$ and $i_{La,low}$ are the highest and lowest values of the current for each switching cycle, respectively. Therefore, the grey area between the two waveforms is the HF switched current of the boost inductor L_a and the LF average inductor current is the $i_{La,average}$. The specific current is true for an inductance of $25\mu H$ and frequency 71.7 kHz. The peak-to-peak inductor current can be increased if the inductance is smaller or if the frequency is lower. This is a way to decrease the switching losses in the converter since more zero-voltage switching is

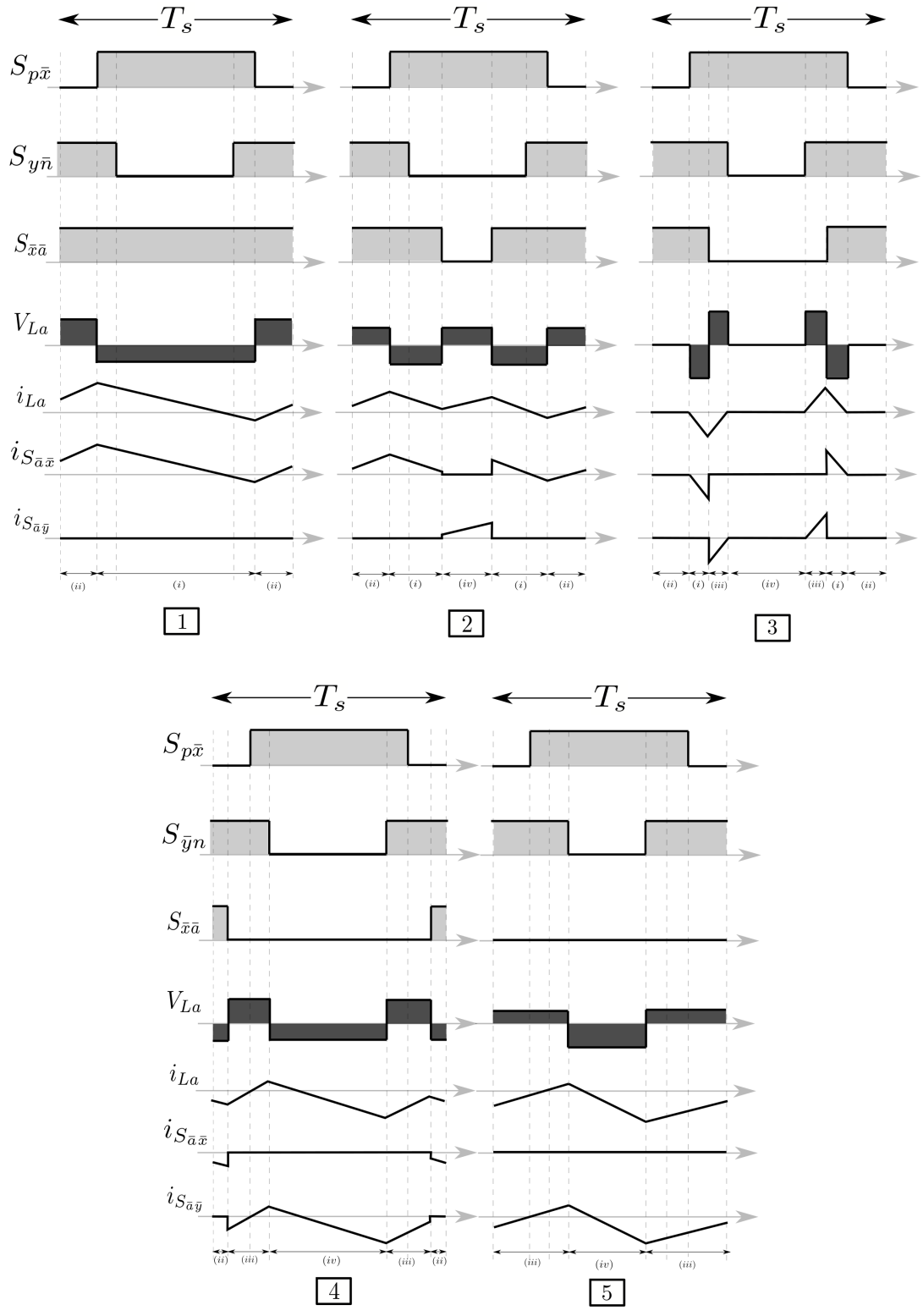


Figure 3.10: Switched voltages for the case of modulation 2.

achieved.

In Fig.3.10, the duty cycles, the voltage over the inductor and the current that flows the bridge leg relevant switches is shown. There are 5 cases that can be analysed and seen in Fig.3.9 and Fig. 3.10. The first case occurs when $S_{\bar{x}\bar{a}}$ is constantly on in selection mode, the second case happens when $1-d_{\bar{x}\bar{a}} < 1-d_{\bar{y}n} < d_{p\bar{x}}$ is true, the third case appears when $1-d_{\bar{y}n} < 1-d_{\bar{x}\bar{a}} < d_{p\bar{x}}$ is true, the forth case takes place when $1-d_{\bar{y}n} < d_{p\bar{x}} < 1-d_{\bar{x}\bar{a}}$ is true and the fifth case arises when $S_{\bar{x}\bar{a}}$ is constantly off in selection mode. Moreover, in the bottom of the waveforms of each case, the conduction state of the switches is indicated as it is specified in Fig.3.4.

Starting from the first case, it can be observed that the voltage over the inductor is only specified from the top boost circuit. The inductor voltage during the first case is independent from $S_{\bar{y}n}$, since $S_{\bar{x}\bar{a}}$ is constantly on. On the other hand, in the fifth case, the voltage over the inductor is only specified from the bottom boost circuit, because $S_{\bar{x}\bar{a}}$ is constantly off ($S_{\bar{a}\bar{y}}$ is on). In cases 2,3 and 4 the inductor voltage is dependent on the duty cycles of all three relevant switches and it can be observed that the double frequency two-level voltage of this modulation can achieve smaller ripple in the current, which means less stresses over the switch and less conduction losses.

Zero-voltage switching:

As it was explained in section 2.3, maximizing the zero-voltage switching is generally desired in HF switching converters such as the Belgian Rectifier. As can be seen in Fig.3.11, the current modulation can achieve partial ZVS, but for the most part, soft-switching is accomplished. Zero-voltage switching is accomplished by enforcing a negative current in the inductor before the turn-off of the switch. This inductor current must be high enough to discharge fully the parasitic capacitance C_{oss}, otherwise partial hard-switching occurs. In Fig.3.9(c), the lower current envelope is not always negative when the average inductor current is positive and the high current envelope is not always positive when the average inductor current is negative, hence hard-switching can be detected as can be seen in Fig.3.11(d). More specifically, the turn-on of the switch $S_{\bar{x}m}$ occurs at a positive voltage over the switch, therefore the switching losses need attention. The turn-on losses of $S_{\bar{x}m}$ can become zero if the boost inductance is decreased. That way, only some hard switching in the bridge legs would occur, which cannot be avoided by the decrease of the inductance.

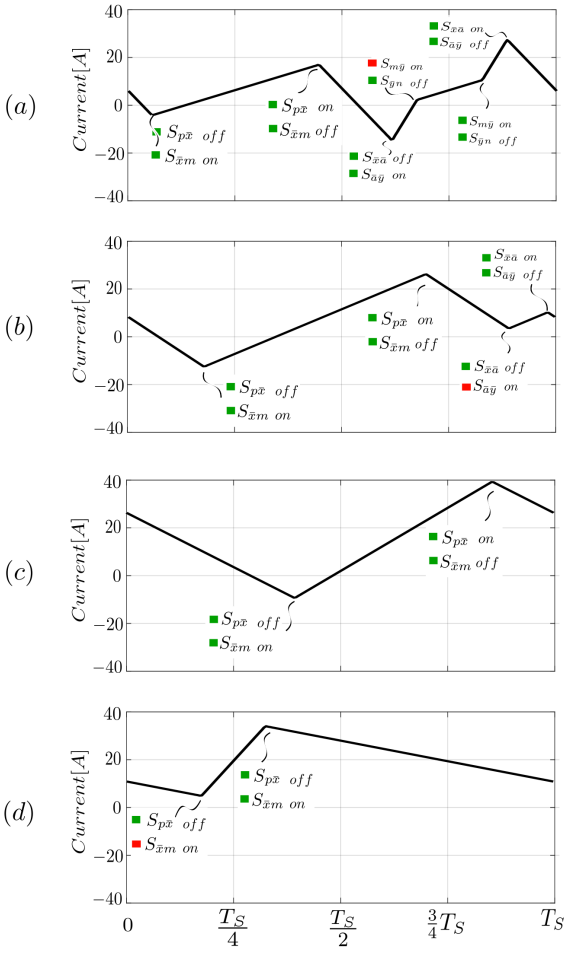


Figure 3.11: Inductor current of one switching cycle when (a) $1-d_{\bar{y}n} < 1-d_{\bar{x}\bar{a}} < d_{p\bar{x}}$ (b) $1-d_{\bar{x}\bar{a}} < 1-d_{\bar{y}n} < d_{p\bar{x}}$ (c) $d_{\bar{x}\bar{a}} = 1$ - soft switching (d) $d_{\bar{x}\bar{a}} = 1$ - hard switching.

Nevertheless, in Fig.3.12, it can be observed that when the turn-off current is negative (the complementary switch turn-on is hard-switching), the absolute value of the current is quite low, which means low switching losses. In Fig.3.12(b), the turn-off current of switch $S_{p\bar{x}}$ is shown and it can be observed that for a short time of the grid cycle, the

turn-off current is negative, thus the turn-on of the $S_{\bar{x}m}$ occurs at a finite voltage. This hard switching is the same one that is observed in Fig.3.11(d).

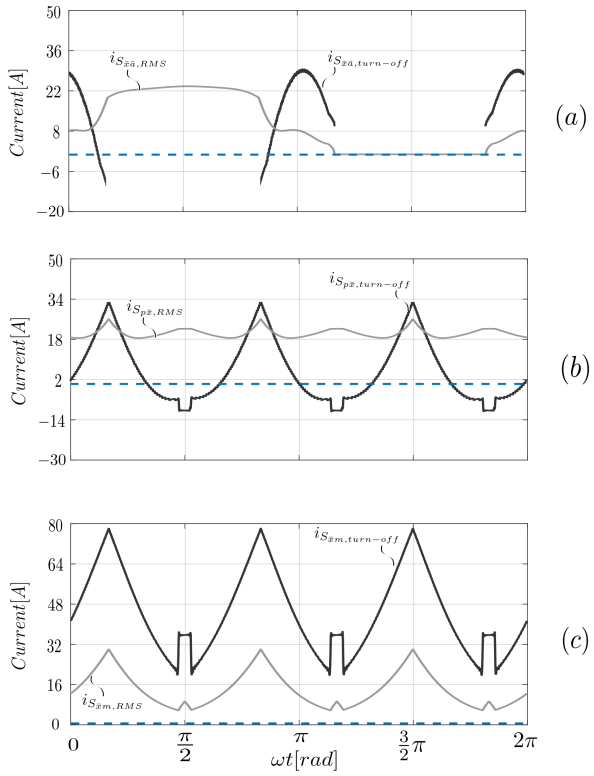


Figure 3.12: RMS and turn-off current of switches (a) $S_{\bar{x}\bar{a}}$ (b) $S_{p\bar{x}}$ and (c) $S_{\bar{x}m}$

However, the current during the hard switching is quite low, thus making the switching losses minimal. On the other hand, in Fig.3.12(c), the turn-off current of switch $S_{\bar{x}m}$ is always positive, thus the turn-on of switch $S_{p\bar{x}}$ is always soft-switching. Overall, the hard switching of the boost circuit switches in Fig.3.12 can be totally avoided if the boost inductance is decreased to a lower level, however the peak current becomes higher with all the consequences that it brings to stresses and conduction losses.

In the rectifier bridge legs, there is also some hard switching that can be observed in Fig.3.12(a). This time instance can be linked to the inductor current of one switching cycle that is depicted in Fig.3.11(b). The hard switching in this case cannot be avoided by decreasing the inductance because it is dependent on the combined states of the rectifier bridge leg switches and the boost circuit switches. However, the Belgian Rectifier can accomplish zero-voltage switching at the majority of the switching cycles and by decreasing the boost inductance, the hard switching can be limited only in the switches of the rectifier bridge. Moreover, hard-switching occurs at very low turn-on currents, therefore the total switching losses are largely limited and the topology can achieve high levels of efficiency.

3.4. Semiconductor Stresses

Starting from the boost circuits on the right of the Belgian Rectifier that can be seen in Fig.3.2, it can be observed that half the DC bus voltage is switched actively. On the other hand, the rectifier bridge switches semi-actively switch full, half the DC bus voltage or zero volts as can be seen in Fig.3.6 and Fig.3.8, therefore they have to be rated to higher than the full DC voltage. In the case of this research where the nominal output voltage is 750V, the boost circuit switches are rated 650V and the rectifier bridge switches are rated to 1200-V. However, the output voltage is considered that it can be in the range of $[660, 850]V$ since transients of the output power can occur at time instances. Therefore, this has to be taken into account when selecting the switches.

The maximum voltage of the top boost circuit switches is the following:

$$v_{S_{p\bar{x}},max} = v_{S_{\bar{x}m},max} = v_{pm,max} = 425V \tag{3.18}$$

The maximum voltage that the switches of the bottom boost converter have to endure is the following:

$$v_{S_{m\bar{y}},max} = v_{S_{\bar{y}n},max} = v_{mn,max} = 425V \tag{3.19}$$

The maximum voltage that the switches of phase A rectifier bridge leg have to endure is the following:

$$v_{S_{\bar{x}\bar{a}},max} = v_{S_{\bar{a}\bar{y}},max} = v_{xy,max} = v_{pn,max} = 850V \tag{3.20}$$

Switch	Maximum voltage [V]
$S_{p\bar{x},max}$	$425V$
$S_{\bar{x}m,max}$	$425V$
$S_{m\bar{y},max}$	$425V$
$S_{\bar{y}n,max}$	$425V$
$S_{\bar{x}\bar{a},max}$	$850V$
$S_{\bar{a}\bar{y},max}$	$850V$
$S_{\bar{x}\bar{b},max}$	$850V$
$S_{\bar{b}\bar{y},max}$	$850V$
$S_{\bar{x}\bar{c},max}$	$850V$
$S_{\bar{c}\bar{y},max}$	$850V$

Table 3.1: Maximum voltages of every switch in the Belgian Rectifier.

The maximum voltage that the switches of phase B rectifier bridge leg have to endure is the following:

$$v_{S_{\bar{x}\bar{b}},max} = v_{S_{\bar{b}\bar{y}},max} = v_{xy,max} = v_{pn,max} = 850V \tag{3.21}$$

And finally, the maximum voltage of the switches of phase C rectifier bridge leg are the following:

$$v_{S_{\bar{x}\bar{c}},max} = v_{S_{\bar{c}\bar{y}},max} = v_{xy,max} = v_{pn,max} = 850V \tag{3.22}$$

The boost switches as mentioned above are selected to be rated at 650-V, thus 51% higher voltage than the maximum voltage they are expected to withstand. The rectifier bridge switches are selected to be rated at 1200-V, thus 39.5% higher than the maximum voltage that these switches are expected to withstand. This fact makes evident the advantage of the Belgian Rectifier which is the active switching of 650-V rated MOSFETs and not 1200-V MOSFETs which have a higher on-resistance $R_{DS,on}$. All the MOSFETs must be chosen to have a very low on-resistance, especially the $S_{p\bar{x}}$ and $S_{\bar{y}n}$ which are turned-on for a relative longer time than their complementary switches in the corresponding bridge legs. In Table 3.1, all the relevant switches maximum voltages are summarized.

Regarding the current of the semiconductors, the RMS and average values are not analytically calculated because they depend on the modulation, the inductance and other factors. However, the formula for the calculation of the RMS current that is used in the average model is the following:

$$i_{RMS} = \sqrt{\frac{1}{n}\sum_{h=1}^{n} i_h^2} = \sqrt{\frac{i_1^2 + i_2^2 + ... + i_n^2}{n}} \tag{3.23}$$

Whereas, the formula for the average current that is used in the model is:

$$i_{average} = \frac{1}{n}\sum_{h=1}^{n} i_h = \frac{i_1 + i_2 + ... + i_n}{n} \tag{3.24}$$

where n are the total harmonics of the current.

The RMS current of the relevant switches can be seen in detail in Fig.3.13. This current is valid for maximum power and the parameters that are set in Table 4.1. It is evident that the maximum RMS current of the relevant switches at this operating point are $i_{S_{\bar{x}\bar{a}},max} = 23A$, $i_{S_{p\bar{x}},max} = 26A$ and $i_{S_{\bar{x}m}} = 29.5A$. Therefore, rated drain current of the selected switches must be higher than these values to cover the whole power range of the rectifier.

The switches are chosen to be SiC MOSFETs, since they show better performance in terms of conduction and switching losses compared to simple Si MOSFETs. Another option could also be 650-V GaN switches since they also have positive performance compared to that of the Si MOSFETs.

3.5. Summary

The Belgian Rectifier topology is described in detail in this chapter, its structure and topology are introduced to the reader and the functionality of separate parts is explained thoroughly.

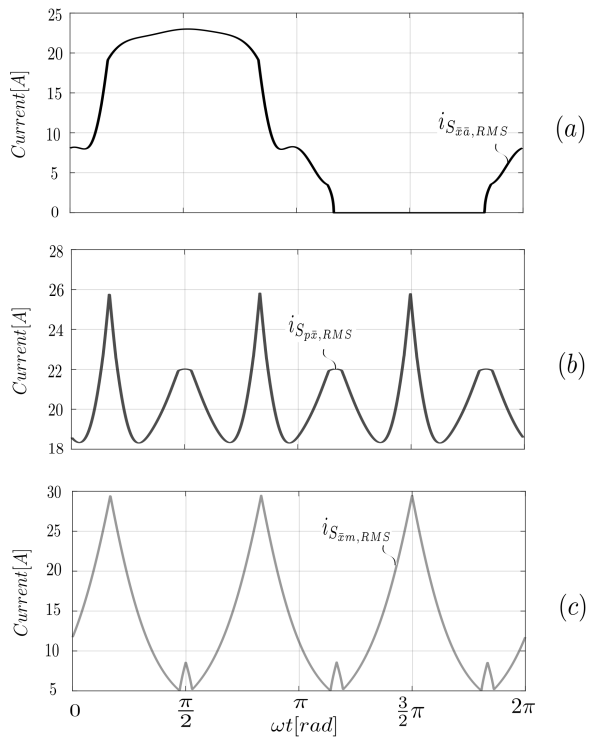


Figure 3.13: RMS current of switches (a) $S_{\bar{x}\bar{a}}$ (b) $S_{p\bar{x}}$ and (c) $S_{\bar{x}m}$

Moreover, an average model is formulated for two different modulations with triangular carriers. The duty cycles of the PWM pulses are derived mathematically and modulation 2 is selected due to its advantages in loss and stress distribution, EMI noise generation, power density and robustness. All the explanations are supported with relevant figures that show the voltages, currents and PWM pulses of the switches and inductor in order to give a good idea of the operation of the Belgian Rectifier.

The investigated topology is being examined in terms of soft switching. It is proven than the Belgian Rectifier can accomplish soft-switching in the largest part of a grid cycle. The boost circuit switches can operate in total soft switching if chosen so, but the rectifier stage switches has a small period of hard switching, which occurs with very low turn-on current, thus making the switching losses affordable.

Finally, the component stresses of the rectifier are investigated. It becomes evident that the Belgian Rectifier can advantageously use 650V rated SiC MOSFET at the boost circuits that are actively switching. Therefore, the losses are significantly lower because of the smaller on-resistance $R_{DS,on}$ of these switches compared to the 1200V rated ones.

4

Closed-loop control

4.1. Introduction

In this chapter, the control scheme that is implemented is described. Different options of controlling the output voltage or the current are presented and the ideal way of controlling the Belgian Rectifier for the research purpose of this project is discussed. Furthermore, the model that is constructed in Simulink/PLECS is described and the waveforms of current and voltage that are generated are shown and explained. The main parameters that are of relevance in this chapter are the start-up of the converter, the total harmonic distortion(THD_i) of the input current, the power factor λ and the transient behavior when reaching full power from zero. The effect of the dead-time in the distortion of the current is discussed. A comparison of the phase current is done when incorporating dead-time compensation and when not doing so. Finally, the overall performance of the control is evaluated and a summary is provided.

4.2. Control scheme

In Fig.4.1, the voltage control scheme can be observed. Starting from the measurements, it can be seen that the output voltages of the bulk capacitors v_{pm}, v_{mn}, the currents of the inductors $i_{L,abc}$ and the input AC phase voltages v_{abc} are fed to the controller. These measurements are firstly put through a low pass filter to emit the undesired noise and later follow quantization and digitization through ADCs. On the right of Fig.4.1, it can be seen that the voltages v_{pm} and v_{mn} are summed to obtain the measured output voltage v_{pn}. It is later subtracted from the set value of the output voltage v_{pn}^*. The voltage error is then fed to a PI controller which gives the set amplitude of the inductor current i_{ampl}^*.

Parameter	Value
$v_{ac,line-line}$	$400V \pm 10\%$
v_{out}	$750V$
$v_{out,range}$	$[650, 850]V$
P_{out}	$22kW$
f_{grid}	$50Hz$
$f_{switching}$	$71.4kHz$
L_{boost}	$25\mu H$
THD_i	$< 5\%$
$cos(\Phi)$	> 0.99
λ	> 0.99

Table 4.1: Relevant parameter values that the Belgian Rectifier is expected to have during operation.

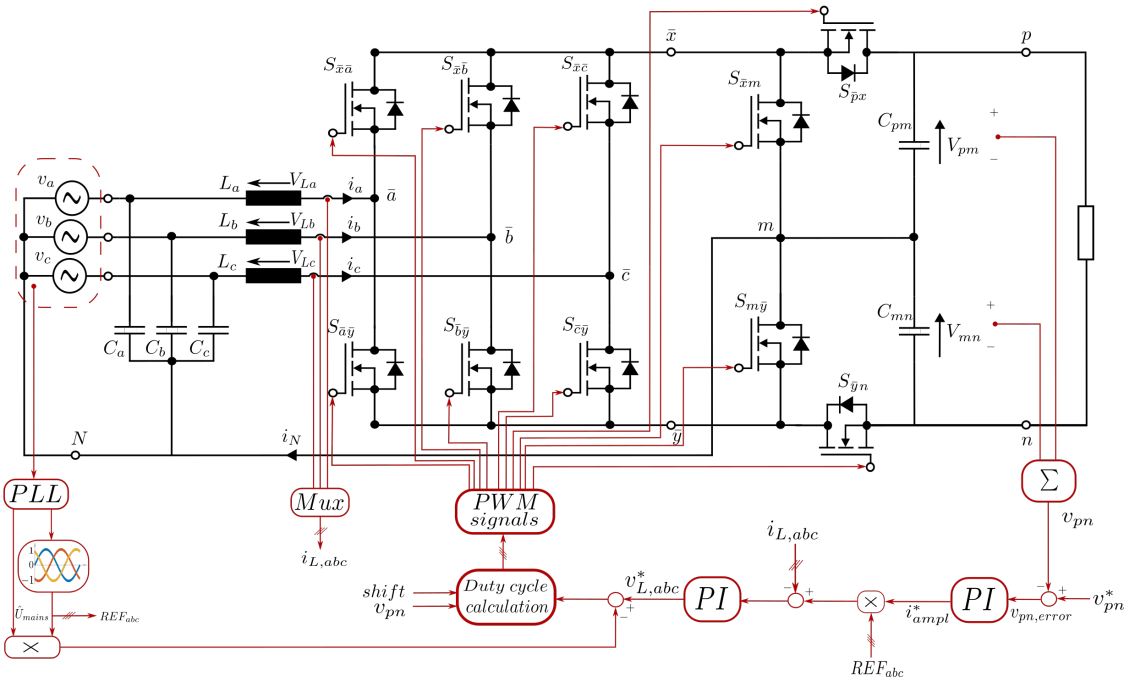


Figure 4.1: Control scheme of Belgian Rectifier for voltage control.

On the left side, it can be seen that the mains input voltage measurements are fed to a phase-locked loop (PLL) which locks onto the grid frequency, generates the reference signals for sinusoidal current and voltage and outputs the amplitude of the phase voltages $\hat{U}_{abc}$. The locked unit reference signals are multiplied with $\hat{U}_{abc}$ to obtain the phase voltages. The locked unit reference signals are multiplied with the set value of the inductor current amplitude, as well. The actual measured inductor currents $i_{L,abc}$ are subtracted from the set values and the error is fed to a PI controller. To continue with, the PI controller calculates the set voltage of the inductors $v^*_{L,abc}$ which is subtracted from the input phase voltages v_{abc} to acquire the required voltages between the midpoints $\bar{a}, \bar{b}, \bar{c}$ and midpoint m. The duty cycle calculation is later done by implementing the modulation 2 of Section 3.3.3. The constant $shift$ is 0.5 and is actually used to indicate the carriers phase shift as it was specified in the selected modulation.

The high input current quality of a THD_i below 5% is only achieved by proper control of the rectifier and it will be explained further below what are the challenges of such a control. Current control methods of active three-phase PWM rectifiers can be found in [13]. Due to disturbances and spikes that might occur in the grid, it is advantageous to use approaches of direct control of the input current. One example could be to use three independent current controllers as is proposed in [16]. Moreover, in three-phase PFC rectifiers such as the six-switch boost, with average current control, mismatched input voltage and current sensing gains as well as offset errors, the current controller with proportional compensation(P) could display lower harmonic distortion (THD) and higher power factor than that of PI compensation [14]. This method can be used in a future project to compare the two controllers. However, in this research typical PI controllers were used as can be seen in Fig.4.1 and Fig.4.2.

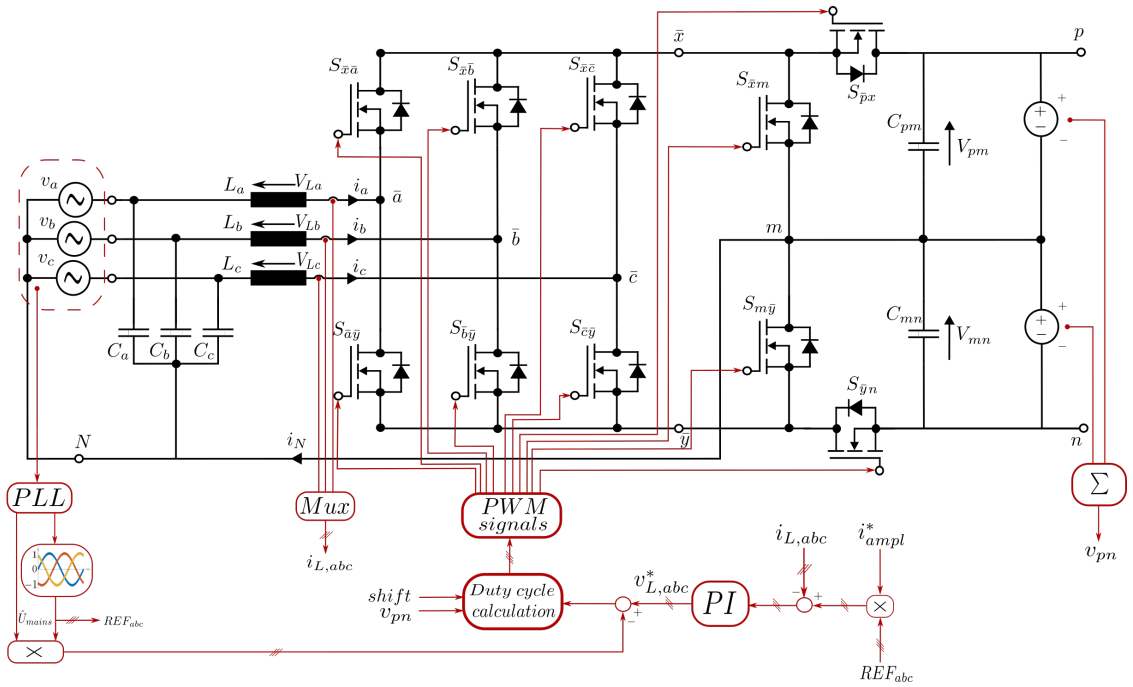


Figure 4.2: Control scheme of Belgian Rectifier for current control.

The current control scheme can be observed in Fig.4.2. In this case, the load has a constant voltage and the current that is drawn from it is defined by the controller. It can be seen that the voltage PI controller and the set value of output voltage are taken out of the control scheme. The set value of the inductor currents' amplitude is given as an input and it specifies what amount of power will be drawn from the grid. This method is considered more suitable to implement testing since in the voltage control scheme, when the start up happens with discharched output capacitor, there is a very high current that is drawn from the three-phase AC-source to the output capacitors through the body diodes. Therefore, the way to start up the converter is to have a constant voltage load at the output, increase gradually the input voltage so that no high current flows through the body diodes and then control the set value of the current in order to increase the power to the desired level.

Dead-time effect

The effect of the dead-time when controlling the Belgian Rectifier has an important effect on the total harmonic distortion (THD) of the phase currents because it introduces a mismatch of voltage over the switches. In other words, the duty cycles are calculated as such to produce a certain voltage (e.g. $v_{\bar{a}m}$), but the actual voltage is different because of dead-time. This effect is described by means of one leg (e.g. phase A) of the rectifier stage as presented in Fig.4.3(b). Since the turn-off and turn-on times associated with any type of switch is finite, a dead-time is defined which is the delay between the turn-off of a switch and the turn-on of its complementary. The dead-time is chosen conservatively to avoid a cross-conduction current through the leg. In Fig.4.3(a), the switch control signals for the two switches without and with the presence of dead-time are depicted.

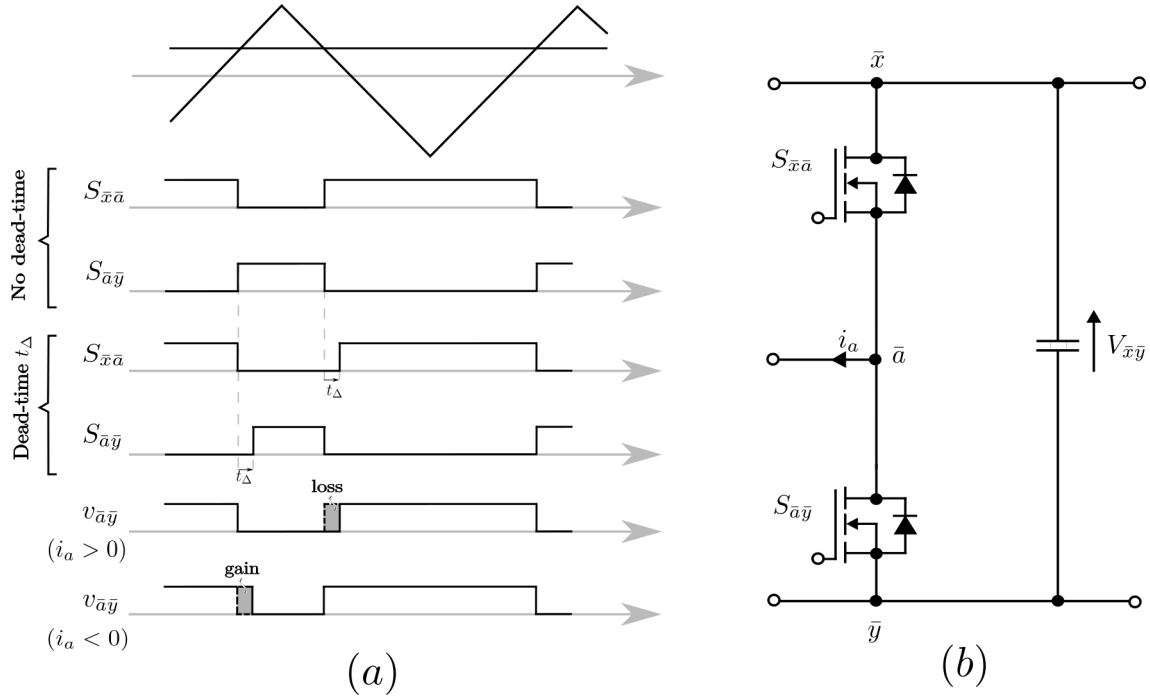


Figure 4.3: (a) PWM signals and switch voltage with and without dead-time (b) Phase A leg of the rectifier bridge leg.

Since both switches are off during the dead-time, $v_{\bar{a}\bar{y}}$ during that interval depends on the current value i_a. As can be seen in Fig.4.3(a), when $i_a > 0$ the voltage over the switch $S_{\bar{a}\bar{y}}$ is decreased and when $i_a > 0$ voltage $v_{\bar{a}\bar{y}}$ is increased. The change can be calculated by averaging the gain or loss over one period of the switching frequency T_{sw} (positive as a drop of voltage) as is shown in (4.1) [22].

$$\Delta v_{\bar{a}\bar{y}} = \begin{cases} \frac{t_\Delta}{T_{sw}} & i_a > 0 \\ -\frac{t_\Delta}{T_{sw}} & i_a < 0 \end{cases} \tag{4.1}$$

From (4.1) it can be observed that the magnitude of the current does not affect the change of the voltage $\Delta v_{\bar{a}\bar{y}}$, but the current direction (polarity) does. The magnitude of the current affects the $\Delta v_{\bar{a}\bar{y}}$ when partial hard switching takes place. At full hard switching, $\Delta v_{\bar{a}\bar{y}}$ is proportional to the dead-time t_Δ and the switching frequency f_{sw}, therefore it is important to use fast switching devices such as SiC MOSFETs that allow to decrease the dead-time and its consequences as described above.

An approach that is widely used is to compensate the dutycycles of the converter for the voltage mismatch caused by the dead-time. A feed-forward is built in the control scheme which calculates the current at the moment of switching and based on its value, it can be determined if the switching moment is hard or soft. For the hard switching that is detected, the dutycycle is increased or decreased in order to compensate for the voltage that is added or subtracted due to dead-time t_Δ.

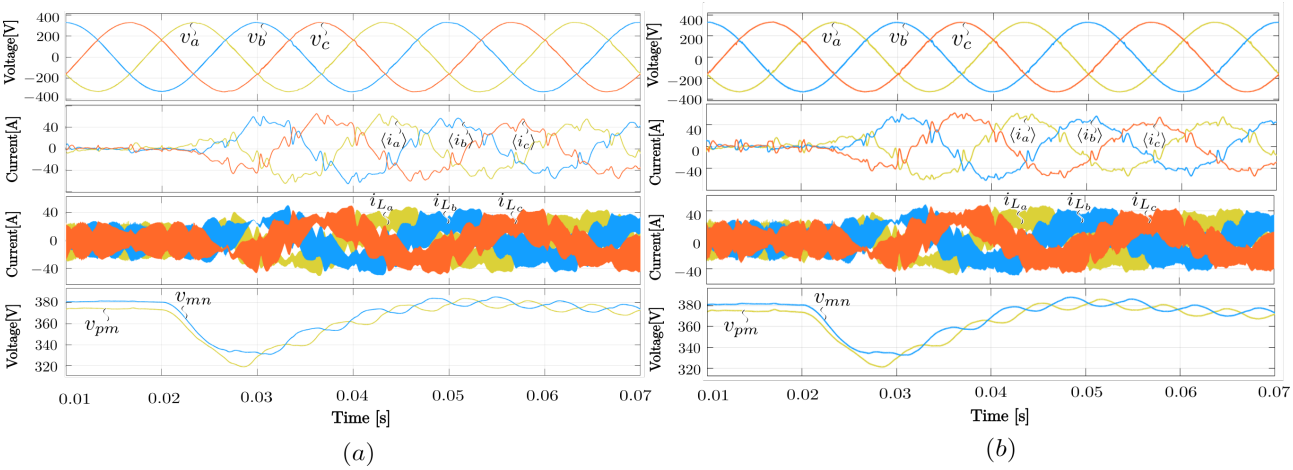


Figure 4.4: Simulation in Simulink/PLECS of the transient of load increase from 0 to 22 kW (a) without dead-time compensation and (b) with dead-time compensation.

4.3. Model & results

The control scheme is implemented in Simulink/PLECS and the relevant waveforms can be seen in Fig.4.4 during the load increase from 0 kW to 22 kW. The parameters of the model in Simulink/PLECS are the same as the ones that are used in the prototype, namely the inductance of the boost inductors L_{abc} is 25 μF, the switching frequency is $71.4kHz$. As it was discussed in Section 3.3.4, hard switching occurs at certain intervals during a grid period. Previously, the effect of dead-time during hard switching moments and how it can be tackled is explained. Dead-time compensation is implemented during the intervals where turn-off current of the boost circuit switches is negative (see Fig.3.12(b)). In Fig. 4.4(a), the relevant waveforms without dead-time compensation are depicted whereas in Fig.4.4(b), dead-time compensation is incorporated, but not for all hard-switching moments (Not the hard switching depicted in Fig.3.12(a)). Except the distortion that is produced from the introduction of dead-time, there are non-linear effects and parameter variation that produce mismatch between the real voltage and the one that is estimated to be generated from the duty cycles calculation.

Comparing Fig.4.4(a) and Fig.4.4(b), it can be observed that the quality of the phase currents in steady-state are improved for the latter case due to the duty-cycle compensation. More specifically, the THD of the phase currents (see second plot) in Fig.4.4(a) is around 20% whereas in Fig.4.4(b) is less than 12.9%. The displacement factor in both cases is $cos(\Phi) > 0.99$. Therefore, it can be calculated from (2.1) that, without dead-time compensation, the power factor is $\lambda > 0.98$ and, with dead-time compensation, the power factor is $\lambda > 0.99$.

Finally, it can be seen in Fig.4.4(a),(b) that using this controller, the converter can reach the nominal power $22kW$ in around $0.03s$ and a voltage drop of $85V$ occurs during the same time for an output capacitor $C_{out} = 1.25mF$. The inductor currents $i_{L_{abc}}$ (see third plot Fig.4.4) can be compared with the shape of the current in Fig.3.9(c) and it can be observed that they have the same shape, but with relative distortion as discussed above.

4.4. Summary

The control scheme of the Belgian Rectifier is described in this chapter. It consists of an outer voltage PI controller and an inner current controller with the former being possible to disable by putting a constant voltage DC load at the output of the converter. The effect of the dead-time is discussed and partial dead-time compensation of the duty cycles is implemented. For both cases, the relevant parameters such as the THD, displacement factor and power factor are discussed and compared.

5

Multi-Physics Component Modelling

5.1. Introduction

An essential part of every reliable virtual prototyping routine are the multi-physics component models. The main duty of these models is to provide a numerical evaluation on the component performance measures (losses, volume) as a function of the design variables. The models make possible the multi-objective optimization routine that is presented in later sections. Therefore, the significance of the accuracy of the employed models for the Pareto-optimal solutions becomes obvious.

In this chapter, the switching model is explained thoroughly and the analytical operations in frequency domain are described together with the Fourier analysis. This is required for the transformation of signals from time-domain to frequency domain-and vice versa. Precise models for the typical power components of the state-of-the-art switched-mode power electronic converters like the semiconductors, inductors, the cooling system and the EMI filter are discussed.

The objective of the analytical modelling is to obtain the overall performance of the Belgian Rectifier in terms of efficiency and power density, detect what are the capabilities of this topology and figure out the trade-offs regarding the design space parameters, in particular for this project, switching frequency and boost inductance.

5.2. Approach

In Fig. 5.1, an overview of the approach for the modelling of the Belgian Rectifier is shown. Starting from the top of the diagram, the main specifications are the input voltage V_i, the output voltage V_o, the output power P_o as well as the EMC standards (CISPR 22 A) that need to be defined. Moreover, the converter topology and the modulation scheme are specified together with other parameters such as the interleaving branches, the number of parallel transistors, the size of the passive components and the switching frequency among others.

After specifying the aforementioned parameters, the steady-state model of the converter takes place to obtain the voltages and currents of relevance which will be used in the semiconductor, inductor and EMI filter models. Some of the waveforms that are generated from the steady-state model can be seen in chapter 3. In particular, the phase voltages, the duty cycles of the switches and the inductor current that are depicted in Fig.3.9 are generated from the steady-state model. The RMS and peak current of the inductor, for instance, are later used in the loss model of the inductor. Furthermore, the turn-off current of the switches that can be observed in Fig.3.12 is again calculated from the steady-state model and is later used from the semiconductor model for the switching losses calculation.

Fourier analysis is used from the switching model to derive the switching cycle waveforms of relevance like the inductor current $i_{L_{abc}}$, the inductor voltage $v_{L_{abc}}$, the switch currents i_S and voltages v_S and other switch cycle waveforms of interest. The analysis is done in the frequency domain because this offers more possibilities like, for instance, to calculate the currents from known voltages and

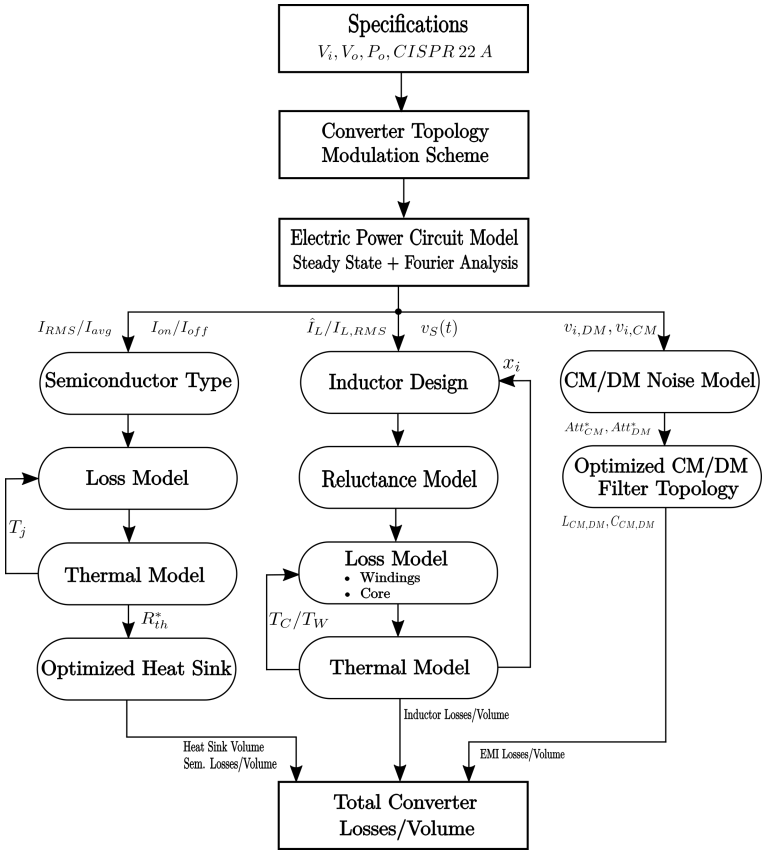


Figure 5.1: Modelling approach that is followed to obtain the total efficiency and power density of the Belgian Rectifier.

impedances instead of integrating. Another advantage of operating in the frequency domain is when modelling the EMI filtering of the converter, since the required input in this case is the spectrum of CM and DM signals. Finally, coefficients of currents and voltages in the frequency domain can be used to obtain the waveform in time-domain for purposes of plotting essentially through inverse-Fourier transformation. An example of such a switching cycle waveform in time domain is the inductor current that can be seen in Fig.3.11.

The grid cycle and switching cycle waveforms that are calculated in the steady-state model are later given as an input to the semiconductor, inductor and EMI filter models. Starting from the semiconductor model, the first thing to define is the type of the semiconductor and its datasheet information to be used in the converter. Secondly, from the average current I_{avg} and RMS current I_{RMS} of each switch that is calculated in the steady-state model, the losses of the semiconductors can be calculated by defining an initial junction temperature. Next, the thermal model takes place and calculates the junction temperature according to the semiconductor losses. Finally, the semiconductor model outputs the volume and the losses of the switches (including cooling materials).

Secondly, the inductor model conducts an inductor design and calculates the losses and the volume of the component using the inductor peak current $\hat{I}_L$ and RMS current I_{RMS}. Moreover, the inductor core and winding temperature T_C/T_W are calculated using a thermal model in order to validate if a certain design is valid. Finally, the output of the inductor model are the losses and the volume of the designed inductors.

Next, the steady-state model outputs the coefficients of the common-mode and differential mode currents that are used from the EMI model. Initially, the spectrum of the unfiltered CM and DM signals is calculated and, according to the CISPR standards, the required attenuation is calculated. Furthermore, the optimized CM/DM filter topology is chosen and the size of the passive components is calculated.

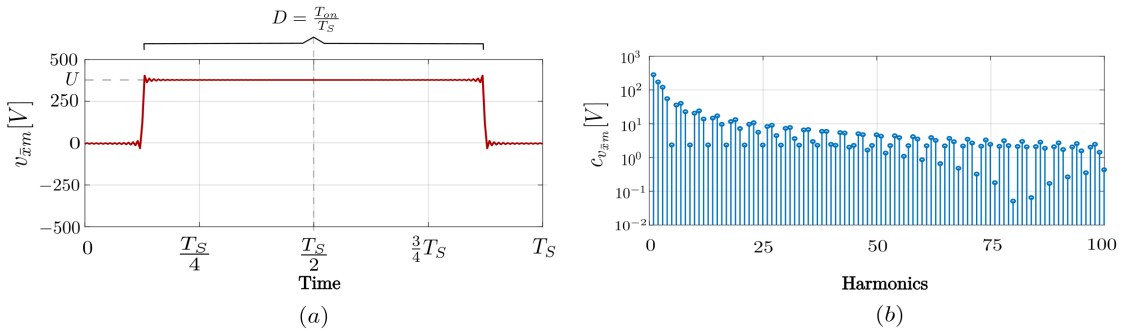


Figure 5.2: (a) Switching cycle waveform and (b) fourier coefficients of $v_{\bar{x}m}$ voltage.

The losses and the volume of the EMI filter are the final output.

Finally, the losses and the volumes from each of the three aforementioned models are summed up in order with others (control board ect) to obtain the total converter losses and volume. Therefore, the efficiency and the power density of the power converter are calculated to obtain an idea of the overall performance of the Belgian Rectifier. The same process is used in a loop for a wide design space to conduct a multi-objective optimization for the converter under investigation.

5.3. Switching model - Fourier analysis

As it is discussed in the previous section, for the most part of the calculations in the steady-state model, the frequency domain is preferred compared to the time domain. Fourier analysis is used to generate the switching cycle waveforms of the voltages, currents and other quantities by calculating the Fourier coefficients. Every periodic function can be described using the generalized Fourier series which is based on the biorthogonality of the functions $cos(nx)$ and $sin(nx)$. The usual Fourier series of a function $f(x)$ is given by [30]:

$$f(x) = a_0 + \sum_{n=1}^{\infty} a_n cos(nx) + \sum_{n=1}^{\infty} b_n sin(nx) \tag{5.1}$$

where the coefficients are

$$\begin{aligned} a_n &= \frac{2}{T_S}\int_0^{T_S} f(x)cos(nx)dx \\ b_n &= \frac{2}{T_S}\int_0^{T_S} f(x)sin(nx)dx \\ a_0 &= \frac{1}{T_S}\int_0^{T_S} f(x)dx \end{aligned} \tag{5.2}$$

and $n \neq 0$.

In Fig.5.2(a), the voltage $v_{\bar{x}m}$ is shown. This voltage is a two-level square-wave with amplitude $U = v_{pm}$, duty cycle $D = \frac{T_{on,S_{p\bar{x}}}}{T_S}$ and phase shift $\phi = 0$. In order to produce this switching waveform, the Fourier coefficients have to be calculated using the following equations

$$\begin{aligned} a_n &= \frac{2U}{n\omega T_S}(sin(n\omega T_S(D + \frac{1}{\phi})) - sin(\frac{n\omega T_S}{\phi})) \\ b_n &= \frac{2U}{n\omega T_S}(cos(\frac{n\omega T_S}{\phi})) - cos(n\omega T_S(D + \frac{1}{\phi})) \\ a_0 &= U \cdot D \end{aligned} \tag{5.3}$$

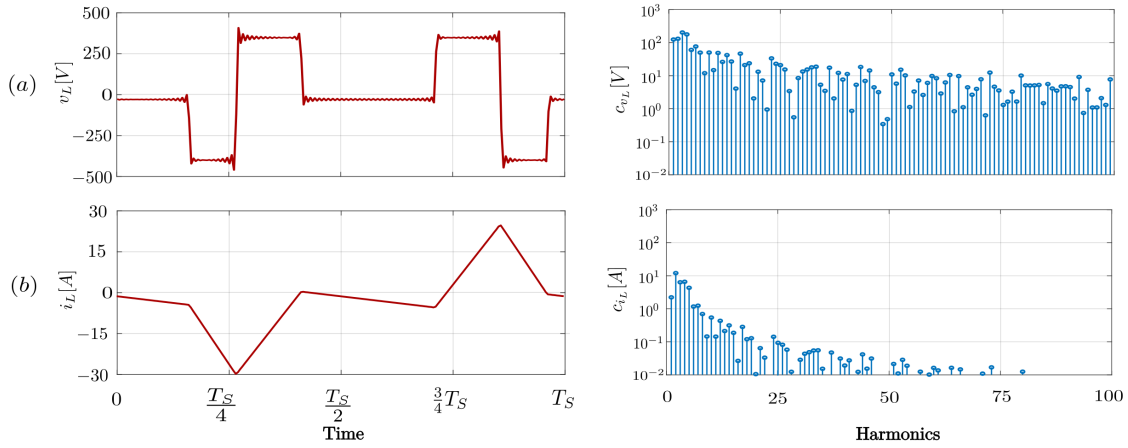


Figure 5.3: Switching cycle waveforms and fourier coefficients for an arbitrary time instant of the grid period of the (a) inductor voltage and (b) inductor current.

The complex form of Fourier series can be written as follows:

$$f(x) = \sum_{n=-\infty}^{\infty} c_n e^{(jnx)} \tag{5.4}$$

And the complex Fourier coefficients are defined by the formula

$$c_n = \frac{1}{T_S} \int_0^{T_S} f(x) e^{(-jnx} dx, n = 0, \pm 1, \pm 2, \ldots \tag{5.5}$$

The complex coefficients c_n can be related to the coeffiecients a_n and b_n through the following equations

$$\begin{aligned} c_0 &= a_0 \\ c_n &= \frac{a_n - jb_n}{2} \\ c_{-n} &= \frac{a_n + jb_n}{2} \end{aligned} \tag{5.6}$$

The complex form of Fourier series is algebraically simpler and more symmetric. Therefore, it is often used in many sciences and it is used for the modelling of switched waveforms in the switching model.

With the equations that are seen in (5.3),(5.6), voltages $v_{\bar{x}m}$ (See Fig.5.2(b)) and $v_{m\bar{y}}$ can be produced by calculating the coefficients. Using the coefficients of these voltages, several calculations can be implemented to obtain other waveforms in the Belgian Rectifier, i.e. voltage $v_{\bar{x}\bar{y}}$ which is the sum of the two aforementioned switched voltages.

Moreover, in order to produce the voltages over the switches of the rectifier bridge, a windowing function is used. A windowing function is a square-wave which has two values, one or zero, and is generated as it is explained for the case of voltage $v_{\bar{x}m}$. For example, windowing functions are multiplied in time-domain with the voltage $v_{\bar{x}\bar{y}}$ to obtain the voltages of the switches of the rectifier bridge and it is evident that the value of the windowing functions is zero when the switches are on and one when the switches are off. Multiplication of signals in time-domain is translated to convolution in frequency-domain.

Therefore, at this point that the input voltage v_{abc}, the rectifier switch voltages and voltages $v_{\bar{x}m}$ and $v_{m\bar{y}}$ are known, Kirchhoff law of voltages can be applied in the closed loop shown in Fig.3.8 and the inductor switched voltage $v_{L_{abc}}$ can be calculated. In Fig.5.3(a) on the right, the coefficients of the inductor voltage can be seen for an arbitrary time instant of the grid period. In Fig.5.3(a) on the left, the time-domain switching cycle waveform of the inductor voltage is obtained by applying the inverse-Fourier transform.

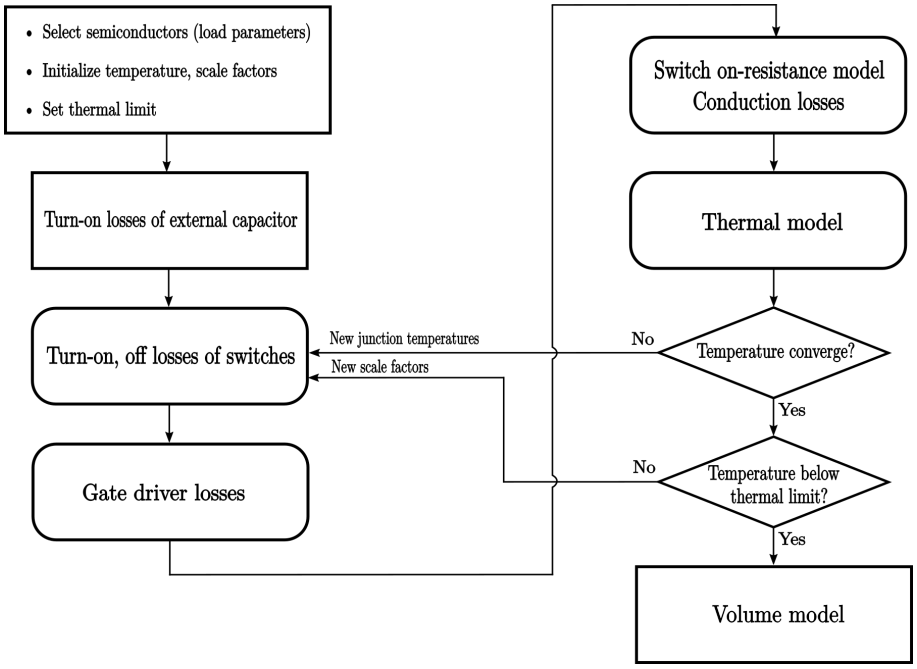


Figure 5.4: Flow diagram of the semiconductor model as it is implemented in Matlab.

Since the coefficients of the inductor voltage $v_{L_{abc}}$ are known, the current coefficients can be calculated simply by dividing the voltage coefficients c_{v_L} by the inductor impedance at each harmonic

$$c_{i_L} = \frac{c_{v_L}}{jn\omega L} \tag{5.7}$$

In Fig.5.3(b), the current Fourier complex coefficients c_{i_L} are shown on the right and the time-domain inductor current i_L, obtained by applying the inverse-Fourier transform, is depicted on the left.

5.4. Components modelling

5.4.1. Semiconductors

Models that are used to accurately estimate the losses generated, and the volume occupied by the semiconductor switching devices (i.e. SiC MOSFETs and heatsinks) are presented in this section. Firstly, the semiconductors that were selected for the rectifier bridge stage and the boost circuits are presented together with the reasoning of this selection. Secondly, as it is already presented in Chapter 3, the modulation scheme that is followed presents hard-switching at certain intervals, thus making it important to make an accurate estimation/calculation of the relevant semiconductor switching losses. Moreover, the conduction losses are the other part of the total loss of the semiconductors that needs to be calculated. However, in order to make an accurate calculation of the conduction losses, the dependency of the on-resistance $R_{DS,(on)}$ of the switching device on the junction temperature T_J, the gate-to-source voltage V_{GS} and the drain current I_D has to be considered.

It is significant that the thermal resistance between the junction of the semiconductor devices and the ambient is as low as possible to maintain a low on-resistance $R_{DS,(on)}$ and therefore, to minimize the conduction losses. This is achieved by increasing or the area around the semiconductor device that is occupied from the cooling material until the required temperature of the junction is reached. For the determination of the thermal resistance, a thermal model is used which takes into consideration all the materials that are between the junction of the semiconductor to the cold plate which is considered to have a constant temperature. Using the aforementioned models, the total losses of the semiconductors and the total volume occupied by the semiconductors and cooling system are determined.

In Fig.5.4, a flow diagram that presents all the taken steps for an accurate semiconductor loss and

Parameter	Value (STCH90...)	Value (STCH10...)	Condition	Description
$V_{DSS}[V]$	650	1200	–	Drain-source voltage
$I_D[A]$	116	75	$T_J = 25^oC$	Continuous drain current
$I_D[A]$	82	53	$T_J = 100^oC$	Continuous drain current
$R_{th,J-C}[^oC/W]$	0.31	0.31	–	Junction-case thermal resistance
$R_{DS,(on)}[m\Omega]$	30	69	$V_{GS} = 18V$ $T_J = 25^oC$	Typical drain to source on-resistance
$Q_g[nC]$	157 ($V_{DS} = 400V$)	163 ($V_{DS} = 800V$)	$V_{GS} = -5/18V$ $I_D = 50A$	Total gate charge
$E_{on}[mJ]$	0.13 ($V_{DD} = 400V$)	1.6 ($V_{DD} = 800V$)	$V_{GS} = -5/18V$ $I_D = 50A$ $R_G = 2.2\Omega$ $T_J = 25^oC$	Typical turn-on switching energy
$E_{off}[mJ]$	0.21 ($V_{DD} = 400V$)	0.46 ($V_{DD} = 800V$)	$V_{GS} = -5/18V$ $I_D = 50A$ $R_G = 2.2\Omega$ $T_J = 25^oC$	Typical turn-off switching energy
–	H^2PAK-7	H^2PAK-7	–	Package

Table 5.1: Relevant parameters of the SiC MOSFETs employed in the Belgian Rectifier (i.e. *SCTH90N65G2V-7*[19] and *SCTH100N120G2-AG*[18] from ST Microelectronics).

volume modelling is presented. It can be observed that starting from an initial temperature of the semiconductors, the loss generation is calculated. Using the calculated semiconductor losses and the calculated thermal resistance between the junction and the cold plate, the junction temperature of the semiconductor is calculated. However, the junction temperature affects several parameters such as the switching energy during turn-on,off and the on-resistance $R_{DS,(on)}$, thus the overall semiconductor losses. Therefore, new calculations of the semiconductor losses are conducted in a loop until the junction temperature converges to a certain value. Initially, a thermal limit is set for the semiconductors in order to determine how much area is needed for cooling. More specifically, scale factors are multiplied with the footprint area of the semiconductor and define how much ”more” area is provided for the cooling for a semiconductor. These scale factors are initialized to a certain value that provides enough area for the routing of the PCB. As long as the junction temperature is above the defined thermal limit, the scaling factors are increased. The loop ends when the junction temperature is below the thermal limit and the last scale factors are kept for the volume calculation.

Semiconductor selection

The selected semiconductor for the boost circuit is the Silicon carbite Power MOSFET *SCTH90N65G2V-7* [19] and for the rectifier bridge legs is the Silicon carbite Power MOSFET *SCTH100N120G2-AG* [18], both from ST Microelectronics. The most relevant parameters of the selected semiconductor devices are shown in Table 5.1. For both semiconductors, major importance play the maximum blocking voltage V_{DSS} and the maximum continuous drain current I_D:

- V_{DSS}: For the boost circuit switches $S_{p\bar{x}}$, $S_{\bar{x}m}$, $S_{m\bar{y}}$, $S_{\bar{y}n}$, the nominal required blocking voltage is half the DC bus voltage $v_{pm} = v_{mn} = 375V$, but as explained in Chapter 3, transients of the output power can increase this voltage (i.e. load transient from nominal power 22kW to 0) up to 430V. Therefore, the absolute minimum required blocking voltage of the switches is the maximum voltage of the output bulk capacitors $v_{pm,max} = v_{nm,max} = 430V$. Moreover, for the rectifier bridge leg switches $S_{\bar{x}\bar{a}}$, $S_{\bar{x}\bar{b}}$, $S_{\bar{x}\bar{c}}$, $S_{\bar{a}\bar{y}}$, $S_{\bar{b}\bar{y}}$, $S_{\bar{c}\bar{y}}$, the absolute minimum required blocking voltage is voltage $v_{\bar{x}\bar{y}}$ which is the sum of v_{pm} and v_{mn}. Therefore, the absolute minimum required blocking voltage of the rectifier bridge legs is $v_{\bar{x}\bar{y},max} = 860V$. It is important that a safety margin of the maximum blocking voltage is considered due to the voltages induced across the parasitics of the switches and the PCB inductances which add up to the aforementioned values [5].
- I_D: The minimum required continuous drain current of a switch is approximately equal to the

maximum RMS value of the current that flows across its drain-source. The switches of the Belgian Rectifier can be separated in 3 groups depending on the drain current. The first group consists of switches $S_{p\bar{x}}$ and $S_{\bar{y}n}$, the second group consists of switches $S_{\bar{x}m}$ and $S_{m\bar{y}}$ and the third group consists of the rectifier bridge leg switches. In Fig.3.13, the maximum RMS current of the three aforementioned group of switches is shown for the parameters defined in Table 4.1.

The SiC MOSFETs whose parameters are shown in Table 5.1, satisfy the requirements that are defined from the maximum voltage and maximum continuous current.

Other important parameters that can be seen in Table 5.1 are the on-resistance $R_{DS,(on)}$, the total gate charge Q_g and the turn on,off switching energy. Starting from the total gate charge Q_g, it is important to be low in order to reduce the turn-on, turn-off times and the gate driver losses. The on-resistance $R_{DS,(on)}$ plays a crucial role on the conduction losses. It can be seen in Table 5.1 that the 650V rated SiC MOSFET's typical $R_{DS,(on)}$ is less than half the one of the 1200V Sic MOSFET. This means that the conduction losses of the boost circuits are significantly lower than the ones of the rectifier stage. A low junction to case thermal resistance $R_{th,J-C}$ is of high importance as well regarding the converter's conduction losses. Finally, the switching energy during turn-on and turn-off play a crucial role in the switching losses of the converter. Again, it is evident that the 650V rated selected semiconductor device exhibits lower turn-on and turn-off typical switching energy (Note that the switching voltage is double in the case of 1200V rated switch). Therefore, the fact that the fully active boost circuits consist of 650V rated switches gives an advantage to the Belgian Rectifier regarding switching losses.

Conduction losses

The conduction losses of the semiconductors are proportional to the on-resistance $R_{DS,(on)}$ and the squared RMS value of the current that flows through the switch. It is assumed that the temperature does not change during a line(grid) cycle, therefore the on-resistance remains constant during one period. The equivalent RMS current $I_{S,eq}$ of a semiconductor is

$$I_{S,eq} = \sqrt{\frac{1}{T_L}\int_0^{T_S} I_S(t)dt} \tag{5.8}$$

where I_S is the instantaneous current that flows over the switch under investigation. The conduction losses averaged over a full line cycle T_L are described as follows:

$$P_{S,cond} = R_{DS,(on)} \cdot I_{S,eq}^2 \tag{5.9}$$

However, there is a strong dependency of the on-resistance $R_{DS,(on)}$ on the junction temperature T_J, the drain current I_D and the gate to source voltage V_{GS} as can be seen in Fig. 5.5. A 2^{nd} order approximation is used in order to describe the on-resistance $R_{DS,(on)}$ depending on the junction temperature T_J and the drain to source current I_D.

$$R_{DS,(on)} = a_0 + a_1 T_J + a_2 T_J^2 \tag{5.10}$$

$$R_{DS,(on)} = b_0 + b_1 I_D + b_2 I_D^2 \tag{5.11}$$

It should be noted that in (5.10) the coefficients $a_{0,1,2}$ are valid only for fixed drain to source current $I_{D,ref}$ and gate to source voltage $V_{GS,ref}$. Likewise, the coefficients $b_{0,1,2}$ in (5.11) are only valid for fixed junction temperature $T_{J,ref}$ and gate to source voltage $V_{GS,ref}$. In the graphs shown in Fig.5.5, the fixed values are depicted in all three dependencies and are also depicted in Table 5.1 at the "Conditions" column for the typical values. By defining the deviation from the reference junction temperature ΔT_J, the deviation from the drain to source current ΔI_D and the deviation from gate to source voltage ΔV_{GS}, a generic equation that calculates the $R_{DS,(on)}$ is given:

$$R_{DS,(on)}(T_J, I_D, V_{GS}) = (a_0 + a_1 T_J + a_2 T_J^2) \cdot (b_0 + b_1 I_D + b_2 I_D^2) + (c_0 + c_1 T_J + c_2 T_J^2 \Delta V_{GS}) \tag{5.12}$$

where $T_J = T_{J,ref} + \Delta T_J$, $I_D = I_{D,ref} + \Delta I_D$ and $V_{GS} = V_{GS,ref} + \Delta V_{GS}$.

Therefore, in order to calculate the conduction losses, the first input required is the time-domain

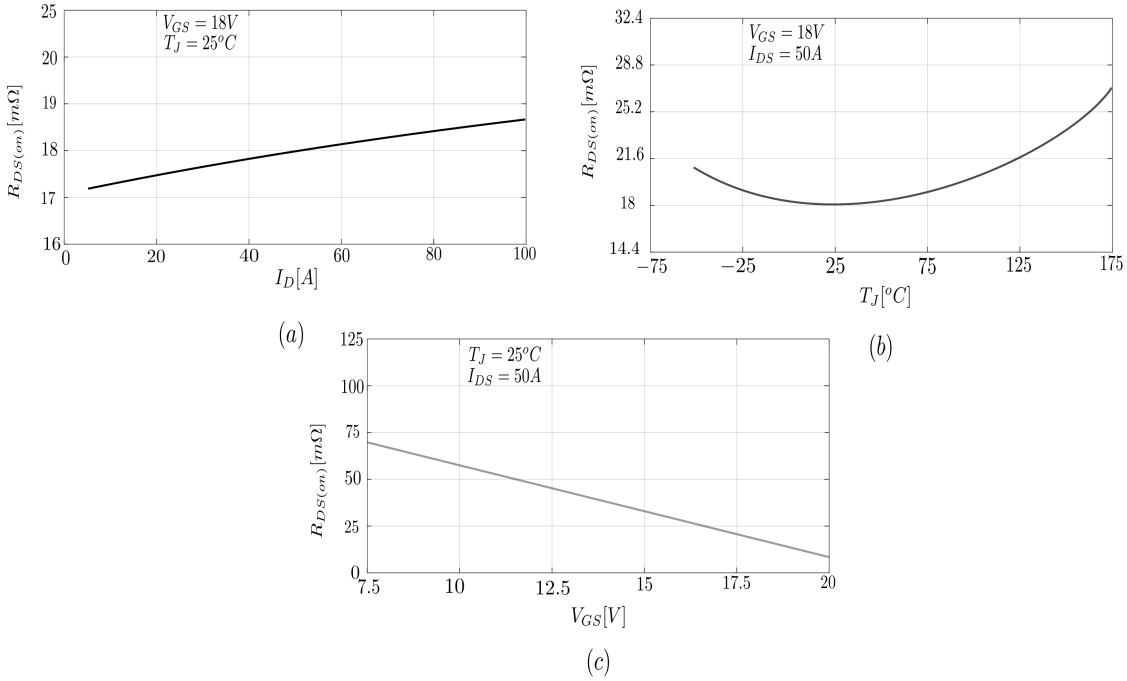


Figure 5.5: On-resistance dependency of SiC MOSFET *SCTH90N65G2V-7* on (a) drain to source current I_D (b) junction temperature T_J and (c) gate to source voltage V_{GS}.

semiconductor RMS current for each switching cycle. This can be obtained from the steady-state model that is described previously and it can be seen for three relevant switches in Fig.3.13. The time-domain current is needed because of its dependency to the on-resistance $R_{DS,(on)}$ as it is explained above. Moreover, the gate to source voltage V_{GS} and the junction temperature T_J are also required because of their dependency with the on-resistance $R_{DS,(on)}$.

Finally, the conduction loss model outputs the conduction losses for each semiconductor. These losses are used together with others in order to determine the junction temperature T_J over a line cycle, as well as the efficiency of the total converter.

Gate drive losses

The gate drive losses play a minor role, it is however desirable to calculate them for higher precision. For the boost circuits, the gate drive losses are calculated for the whole line cycle, whereas in the rectifier stage, the gate drive losses are considered negligible when the switches are in selection state, thus they are only calculated when they are actively switching. The losses of the gate drive occur when the gate to source voltage changes from the on-value to off-value and thus charges or discharges the gate capacitance that consists of a certain gate charge. Therefore, the gate drive power loss can be calculated with the following formula using the total gate charge Q_g (See Table 5.1), the gate to source differential voltage $\Delta V_{GS} = V_{DS,(on)} - V_{GS,(off)}$ and the switching frequency f_{sw} for a fully active switch over a line cycle:

$$P_{GDr,avg} = Q_g \cdot \Delta V_{GS} \cdot f_{sw} \tag{5.13}$$

Switching losses

The switching losses P_{sw} of the semiconductors are calculated with the following formula:

$$P_{sw} = \frac{1}{T_L} \cdot \left(\sum_{i=1}^{N_{sw,on}} E_{on}(I_{on,i}, V_{on,i}, T_J, V_{GS,(on)}, R_{G,on}) + \sum_{i=1}^{N_{sw,off}} E_{off}(I_{off,i}, V_{off,i}, T_J, V_{GS,(off)}, R_{G,off}) \right) \tag{5.14}$$

where the number of turn-on and turn-off switching transitions with a grid cycle T are $N_{sw,on}$ and $N_{sw,off}$.

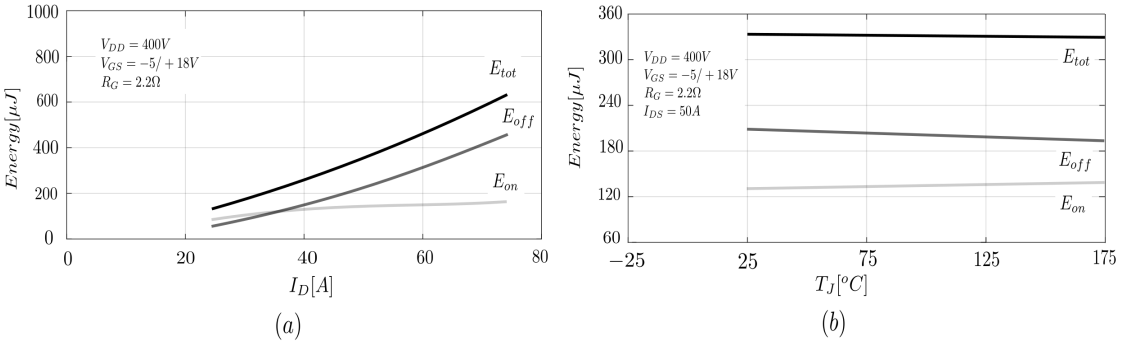


Figure 5.6: Dependency of the turn-on, turn-off and total switching loss enegies E_{on}, E_{off}, E_{tot} on (a) drain to source current I_D and (b) the junction temperature T_J [19].

The turn-on and turn-off switching loss energies E_{on}, E_{off} (See Table 5.1 for the typical values) are dependent on the average junction temperature of the semiconductor T_J, the switched currents $I_{on,i}$, $I_{off,i}$, the blocking voltage $V_{on,i}$, $V_{off,i}$, the gate to source voltage $V_{GS,on}$, $V_{gs,off}$ and finally the gate resistors for the turn-on $R_{G,on}$ and turn-off $R_{G,off}$ [2].

The input variables for the semiconductor switching losses are the the following:

- Switched current $I_{on,i}$, $I_{off,i}$ and blocking voltage $V_{on,i}$, $V_{off,i}$ of all switching instances that happen for an investigated semiconductor. These values can be extracted from the time-domain waveforms which are calculated in the steady state model for a grid cycle.
- The average junction temperature of the semiconductor which is firstly initialized and later determined using the thermal model that is explained further below in this section.
- The gate to source turn-on and turn-off voltage $V_{GS,on}$, $V_{gs,off}$ as well as the turn-on and turn-off gate resistances $R_{G,on}, R_{G,off}$. These variables are considered constant is this thesis and are defined from the gate drivers used in the prototype. Research on the dynamic of the gate drives can be provided from [15].

It is evident that the turn-on and turn-off switching loss energies E_{on}, E_{off} are the required parameters for the proposed switching loss model. The typical values of these energies for both selected semiconductors can be seen in Table 5.1. However, these values are valid for a specific operating point which is described in the column ”Condition”. It is not correct to use the those two values for every case and the dependency between the switching energies on the other parameters, mentioned above, has to be taken into account.

In Fig.5.6(a), the dependency of the turn-on, turn-off and total switching energies E_{on}, E_{off}, E_{tot} on the drain to source current I_D of 650V semiconductor *SCTH90N65G2V-7* is depicted for fixed values of blocking voltage V_{DD}, gate to source voltage V_{GS}, gate resistance R_G and junction temperature T_J. As expected, for higher drain to source current, the switching energies increase as well. On the other hand, the dependency of the switching energies on the junction temperature by keeping all the other relevant values fixed, is depicted in Fig.5.6(b). It can be observed that the temperature dependency is not that crucial as that of the drain to source current or the blocking voltage.

However, in order to obtain the switching energies of each semiconductor for given parameters, 2^{nd} order equations are formulated that simulate the dependencies that are shown in the datasheets. By defining the reference energies $E_{on,ref}$, $E_{off,ref}$ and the reference parameters $V_{DD,ref}$, $I_{D,ref}$, $R_{G,ref}$, $T_{J,ref}$ for which those energies are valid, the 2^{nd} order equation of the switching energies at a variable point with parameters $V_{DD,set}$, $I_{D,set}$, $R_{G,set}$ and $T_{J,set}$ has the following form:

$$E_{on,off,set} = E_{on,off,ref} \cdot f(\Delta T_J, \Delta I_D, \Delta R_G, V_{DD,set}) \tag{5.15}$$

where $\Delta T_J = T_{J,set} - T_{J,ref}$, $\Delta I_D = I_{D,set} - I_{D,ref}$ and $\Delta R_G = R_{G,set} - R_{G,ref}$.

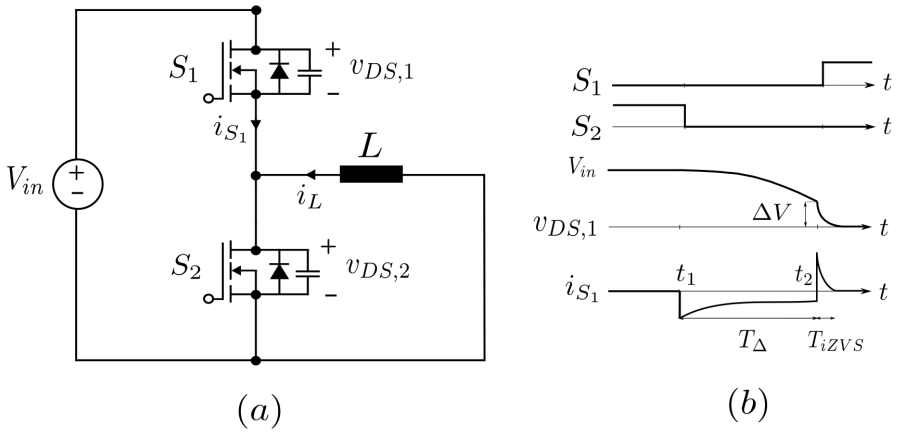


Figure 5.7: Incomplete ZVS transition of a SiC MOSFET half bridge leg. (a) Considered circuit including capacitors in parallel with the switch representing the sum of the non-linear paracitic capacitance C_{oss} and the added parallel external capacitance C_{ext} to show a switching transition where S_1 turns on at a finite drain to source voltage $V_{DS,q} = \Delta V$. (b) The relevant waveforms on the interval of the dead-time T_d and the dissipative phase T_{iZVS} which occurs when S_1 is turned on at a finite voltage [2].

Full and incomplete zero-voltage switching

In chapter 2, complete zero voltage switching is explained by analysing a half bridge leg with an inductor L, two switches S_1, S_2 and a voltage source V_{in}. In Fig.5.7(a), the same half bridge leg is depicted where in parallel with the switches, a capacitor is drawn that represents the output parasitic capacitance C_{oss} and the external capacitance C_{ext}. As explained in above, the switch capacitances have a certain stored charge Q_{oss} that during the resonant transition is relocated from the switch which is turned-on to the switch which is turned-off. A challenge in modelling such a transition is the non-linearity of the output capacitance and its dependency on the drain to source voltage V_{DS}.

In Fig.5.7(b), an incomplete ZVS transition where switch S_1 turn-on at a finite voltage ΔV is depicted. It is assumed that the inductor current becomes zero at the time instant t_2. For a given dead-time T_Δ and output capacitance of the switch $C_{oss} + C_{ext}$, the parameter that defines if complete or incomplete ZVS switching will occur is the inductor current. The inductor current is required to discharge fully the parallel capacitance of switch S_1 before t_2 in order to achieve complete ZVS. If the inductor current cannot move the charge in time T_Δ, then the turn-on voltage of switch S_1 will not be zero, but a finite value when the turn-on happens. When hard switching occurs, the lost energy of the external capacitor C_{ext} is dependent on the blocking voltage of the switch as follows:

$$E_{on,hard,C_{ext}} = \frac{1}{2} \cdot C_{ext} \cdot V_{DD}^2 \tag{5.16}$$

When there is incomplete ZVS as it is depicted in Fig. 5.7(b), the partial lost energy of the external capacitor is calculated:

$$E_{on,partial,C_{ext}} = E_{on,hard,C_{ext}} \cdot (1 - \frac{1}{I_{cut,off} - I_D}) \tag{5.17}$$

where the current $I_{cut,off}$ is the minimum current that facilitates a complete ZVS transition and I_D is the turn-on current of the switch under investigation.

The external capacitor that is placed in parallel to the switch reduces the turn-off losses because it slows down the ramp-up of the drain-to-source voltage V_{DS} during the dead-time T_Δ. Moreover, it reduces the CM noise generated by the HF switching and therefore decreases the size of the EMI required for the filtering. On the other hand, increased parallel capacitance to the switch means more charge that needs to be relocated to achieve ZVS and, thus, higher I_{cutoff} which brings more partial hard switching.

The semiconductor switching model outputs are the average switching-cycle and line-cycle switching losses of the SiC MOSFETs as can be seen in Fig.5.8. The calculated losses are summed up with

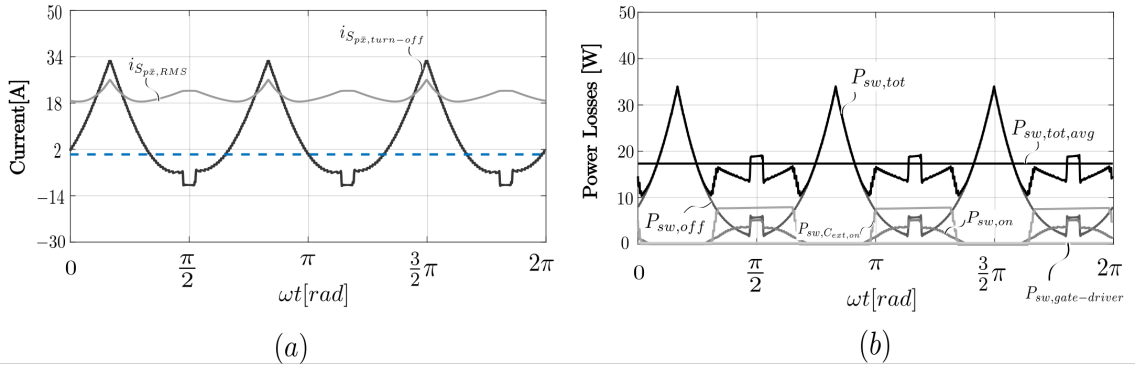


Figure 5.8: (a) RMS and turn-off current of switch $S_{p\tilde{x}}$ depicting the intervals that hard-switching occur for turn-off current below zero. (b) Switching losses for turn-on $P_{sw,on}$ and turn-off $P_{sw,off}$, external capacitor turn-on losses $P_{sw,C_{ext,on}}$, gate driver losses $P_{sw,gate-driver}$, the switching-cycle averaged $P_{sw,tot}$ and the line-cycle averaged total switching losses $P_{sw,to,avg}$ of switch $S_{p\tilde{x}}$.

the rest of the of the losses in order to calculate the switching-cycle and line-cycle averaged junction temperature of the semiconductors. The calculated junction temperature T_J is later compared with the thermal limit and the heatsink area is adjusted so that the limit is not exceeded. Finally, the line-cycle average switching losses contribute to the calculation of the overall efficiency of the converter.

Thermal model

The semiconductor thermal model is used to estimate the junction temperature T_J of the semiconductor device and is dependent on the several materials that exist between the semiconductor and the cold plate which is considered to have a constant cooling temperature. As can be seen in Fig.5.9(a), the semiconductor is mounted in a metal core PCB (MCPCB) and has a certain area around it to provide space for the routing and cooling. In Fig.5.9(b), it can be seen that the bottom of the semiconductor touches the MCPCB and thereafter, the PCB is linked to the cold plate through an aluminium block. Therefore, a path is provided for the heat to flow from the semiconductor through the MCPCB and the aluminium block to the cold plate.

Each of the materials that are between the semiconductor and the cold plate have a certain thermal resistance. For the semiconductor device junction to case thermal resistance, the datasheet is a reliable reference and for the selected SiC MOSFETs, the relevant values are depicted in Table 5.1. The thermal resistance of the other materials between the semiconductor and the cold plate can be calculated by using their dimensions and the thermal conductivity $k_{th}[w/mK]$. Therefore, using the thickness $d_{material}$, the area $A_{material}$ and the thermal conductivity, the thermal resistance of each material $R_{th,material}$ can be estimated:

$$R_{th,material} = \frac{d_{material}}{A_{material} \cdot k_{material}} \tag{5.18}$$

After calculating the thermal resistances of each material, the electrical equivalent of the thermal model can be drawn as in Fig.5.9(c), and therefore the junction temperature can be calculated with a given total power loss of the semiconductor under investigation.

It should be noted that the temperature of the cold plate is considered constant 50^oC, the thickness $d_{material}$ and the thermal conductivity $k_{material}$ of each material is fixed. Therefore, in order to control the average temperature of the semiconductors, the area around the semiconductor is increased until the point when the junction temperature is lower than the thermal limit.

Volume model

The volume of the semiconductor is dependent on all the materials that are depicted in Fig.5.9(b). In the top view, that can be seen in Fig.5.9(a), the area given to a single semiconductor device is presented. This area is initialized as three times the area of the semiconductor footprint for practical

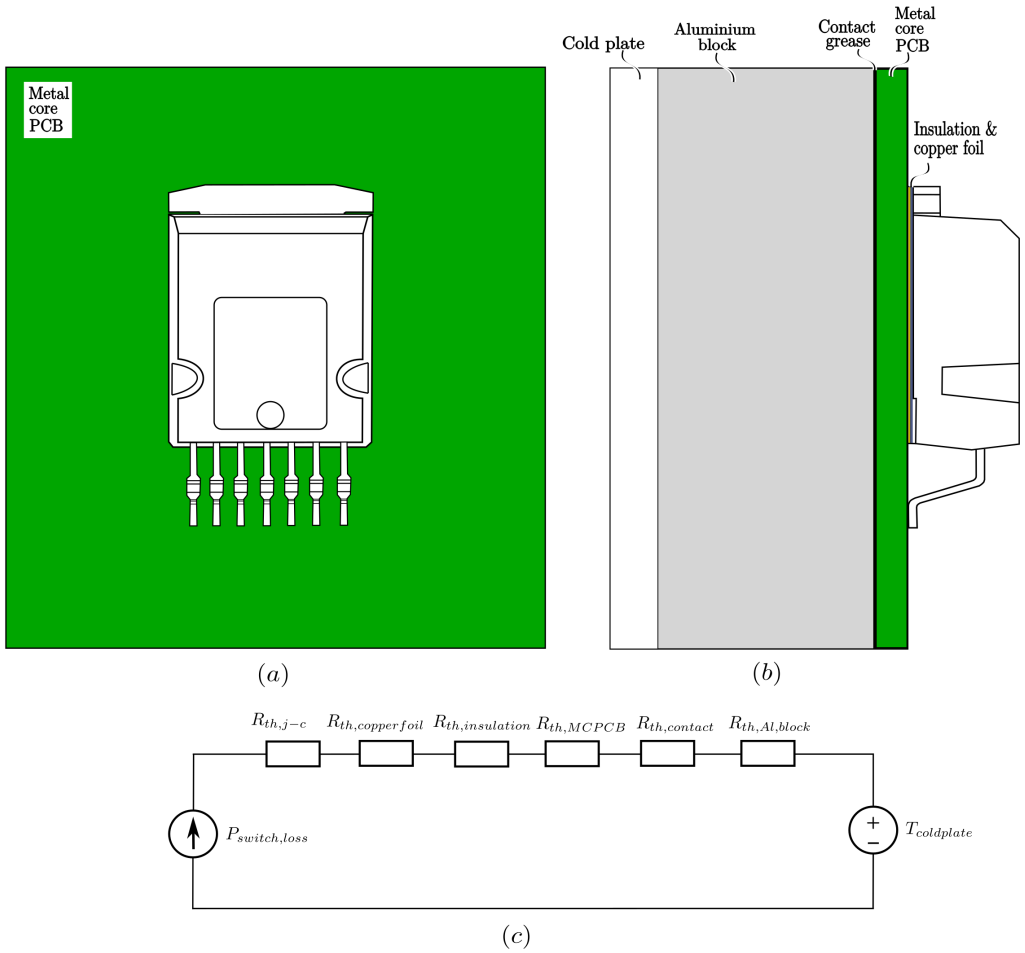


Figure 5.9: (a) Top view of the semiconductor device and the MCPCB, (b) side view of the semiconductor thermal model and (c) the electrical equivalent of the semiconductor thermal model.

reason (i.e. routing, gate drivers, snubbers etc). If the initialized area is not sufficient for the cooling of the device, then it is increased until the temperature of the SiC MOSFET is lower than the thermal limit. The other dimension required to obtain the volume is the thickness from the top of the semiconductor to the bottom of the cold plate. The total thickness is the sum of the semiconductor, the metal core PCB, the aluminium block and the cold plate thicknesses. The total thickness is multiplied with the area (See Fig.5.9(a) with green color) that is occupied from one semiconductor to obtain the total volume for each semiconductor. The total volume is the sum of the volumes required for each semiconductor.

5.4.2. Inductors

The passive components of any power electronic converter play a crucial role in its steady-state/dynamic operation and its overall performance. In the scope of this work, an optimization algorithm is used that aims for the lowest possible occupied volume and power losses. The power losses of the inductors are dependent on the currents and voltages, but also on the geometry, the arrangement and the type of the windings, as well as the geometry, the material and the type of the core [5]. In this project the total occupied volume of the inductor is dependent on the dimensions of the core whereas the windings (end turns) are not considered to take more space. For the calculation of the inductor core and winding losses the current and voltage waveforms and their spectrum is required. The steady-state model calculates the inductor voltage and current in frequency-domain, as well as the RMS current and the peak current in time-domain that are crucial for the calculation of the inductor losses. For the modelling of inductive power components, the procedure followed is structured as [11]:

- Set up a magnetic circuit model (i.e. reluctance model).
- Determine winding losses.
- Determine core losses.
- Set up a thermal model.

Inductor model input

The inductor model inputs are the time-domain and frequency domain currents and voltages of the inductor, the RMS current and the peak inductor current that are extracted from the steady-state model. Furthermore, libraries with information regarding the core type, size, material, air gap characteristics, winding geometry and arrangement, wire specifications, boost inductance ect. are needed for the design of the inductor. Finally, information from the datasheets of the core and wire manufacturers are required.

Inductor design

Starting from a design space regarding the inductor parameters such as the core material, type, dimensions, winding type, geometry and arrangement, the value of the inductance, air gap type and position, an inductor design is implemented which gives the main parameters of the inductor such as the core, number of turns, the length of the air gap, the final inductance and reluctance. The peak current is required for the design in order to define the saturation limits. For the purposes of this project the design space consists of different core dimensions and materials and the design serves for the calculation of the number of wires, diameter and air gap. Litz wire is selected due to its advantageous behaviour in HF and the limited eddy current losses [7]. The current is divided equally among the strands that constitute the Litz wire, thus decreasing the AC resistance and the total winding losses. A design is finally chosen according the lowest losses and/or volume.

Inductor reluctance

The magnetic circuit is set up to determine the inductance, predict the flux density in every part of the core and estimate the effect of the air gap fringing field on winding losses. In order to calculate the core losses and avoid saturation, the flux density is important to calculate in each section. The reluctance of the core is straightforward to calculate since it depends on its dimensions and its material. The core is split into several sections that have a certain length l, cross-section A_c and permeability $\mu_r\mu_0$ whose reluctance is calculated as:

$$R_c = \frac{l_c}{A_c \mu_r \mu_0} \tag{5.19}$$

The total reluctance of the core is the sum of the reluctances of each section.

The air gap reluctance is more complicated to calculate because of the fringing field estimation. An approach that is based on a modular concept where basic geometry is used as a building block to describe three different dimensional air gap shapes is proposed in [11], [20] and is used for the calculation of the air gap reluctance. However, under the assumption of a homogenous flux density distribution in the air gap without fringing flux, the air gap reluctance can be calculated as

$$R_g = \frac{l_g}{A_g \mu_0} \tag{5.20}$$

Winding losses

The winding losses of Litz wires are separated into three different power losses: skin effect losses P_S, external proximity effect losses $P_{P,e}$ and internal proximity effect losses $P_{P,i}$. First, self-induced eddy currents inside the wire produce the skin effect losses P_S, the air gap fringing field and the magnetic field of neighboring wires produce eddy currents than generate the external proximity effect losses $P_{P,e}$ and the magnetic field of the same wire produces eddy currents as well, which generate the internal

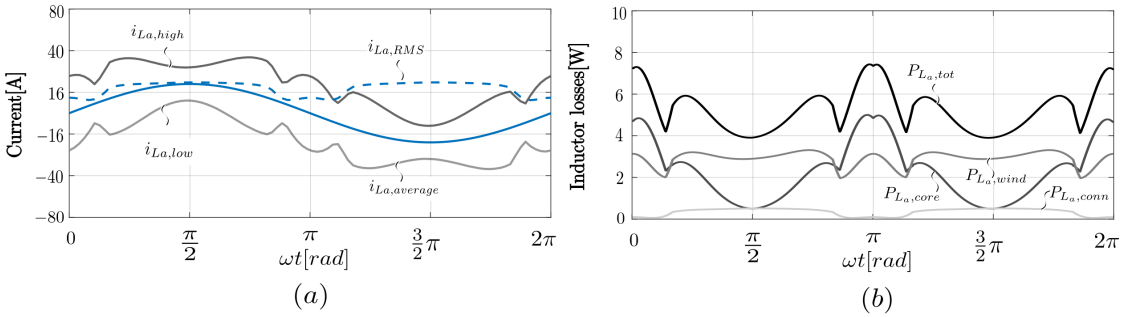


Figure 5.10: (a) Average, RMS and peak-to-peak current of inductor L_a. (b) The winding losses $P_{L_a,wind}$, core losses $P_{L_a,core}$ and the total power losses $P_{L_a,tot}$ of inductor L_a switch-cycle averaged.

proximity effect losses $P_{P,i}$. The skin effect losses have a dependency on the Fourier amplitude coefficients of the total current in the Litz-wire $\hat{I}$, on the DC resistance per unit length of a single strand $R_{DC,s,L}$, on the number of strands n_s and on the skin effect factor F_R as follows:

$$P_{S,L} = n_s \cdot R_{DC,s,L} \cdot F_R(f) \cdot (\frac{\hat{I}}{n_s})^2 \tag{5.21}$$

,where the DC resistance per unit length is dependent on the diameter of the strand d_s and the electric conductivity σ as:

$$R_{DC,s,L} = \frac{4}{\sigma \pi d_s^2} \tag{5.22}$$

The skin effect factor F_R is defined as:

$$F_R = \frac{\xi}{4\sqrt{2}}\left(\frac{ber_0(\xi)\cdot bei_1(\xi) - ber_0(\xi)\cdot ber_1(\xi)}{ber_1(\xi)^2 + bei_1(\xi)^2} - \frac{bei_0(\xi)\cdot ber_1(\xi) + bei_0(\xi)\cdot bei_1(\xi)}{ber_1(\xi)^2 + bei_1(\xi)^2}\right) \tag{5.23}$$

where

$$\xi = \frac{d_s}{\sqrt{2}\delta}, \delta = \frac{1}{\sqrt{\pi \mu_0 \sigma f}} \tag{5.24}$$

δ is the skin depth and μ_0 is the the permeability of copper. The total proximity losses per unit length (sum of internal and external proximity losses) can be calculated with the following formula:

$$P_{P,L} = n_s \cdot R_{DC,s,L} \cdot G_R(f) \cdot \left(\hat{H}_e^2 + \frac{\hat{I}^2}{2\pi^2 d_b^2}\right) \tag{5.25}$$

where $\frac{\hat{I}^2}{2\pi^2 d_b^2} = \hat{H}_i$ is the peak internal magnetic field across one strand of the Litz wire and $\hat{H}_e$ is the peak external magnetic field which is calculated using a 2D analytical approach proposed in [11]. The proximity effect factor G_R is defined as:

$$G_R = \frac{\xi \pi^2 d_s^2}{2\sqrt{2}}\left(\frac{ber_2(\xi)\cdot ber_1(\xi) + ber_2(\xi)\cdot bei_1(\xi)}{ber_0(\xi)^2 + bei_0(\xi)^2} - \frac{bei_2(\xi)\cdot bei_1(\xi) - bei_2(\xi)\cdot ber_1(\xi)}{ber_0(\xi)^2 + bei_0(\xi)^2}\right) \tag{5.26}$$

Core losses

For the calculation of the core losses, the Generalized Steinmetz Equation (iGSE) [28] is used. This method does not require extra characterization of material parameters except the Steinmetz material parameters. The losses due to domain wall motion are considered. The latter is directly related to the core flux density's dependency on time $\Delta B/dt$. Other methods such as the improved Generalized Steinmetz Equation [21] require information that is not provided in core manufacturer datasheets, therefore the standard equation is used.

The advantage of the link between core losses to the change of the flux density, makes possible the calculation of core losses for non-sinusoidal flux waveforms such as in the case of the Belgian Rectifier inductor flux density. Therefore, using the Steinmetz parameters k, α and β, the core losses per unit volume are:

$$P_{core,V} = \frac{1}{T_L}\int_0^{T_L} k_i \left|\frac{dB}{dt}\right|^{\alpha} (\Delta B)^{(\beta-\alpha)} dt, \tag{5.27}$$

where k_i is the defined as:

$$k_i = \frac{k}{(2\pi)^{(\alpha-1)} \int_0^{2\pi} |cos\theta|^{\alpha} 2^{(\beta-\alpha)} d\theta} \tag{5.28}$$

The calculation of the Steinmetz parameters k, α and β is possible due to the dependency of the core losses per unit volume $P_{core,V}$ on the frequency f, temperature T and the peak flux density $\hat{B}$ for sinusoidal excitation as:

$$P_{core,V} = k f^{\alpha} \hat{B}^{\beta} \tag{5.29}$$

The manufacturers provide graphs that show the dependency of the core losses per unit volume on the aforementioned parameters and the Steinmetz parameters can be extracted from them. In Fig. 5.10(a), the current of the inductor for the converter parameters shown in Table 4.1 is shown and in Fig.5.10(b), the modelled inductor losses are depicted. It is evident that the peak current of the inductor affects the winding losses as well as the core losses because there is a dependency with the flux density whose derivative is used in the core loss calculations. The estimated core losses averaged in a line-cycle are almost $6W$ for the shown inductor design.

Thermal model

In order to determine if a certain inductor design is valid, the thermal behavior of its core and windings have to be analyzed. In order to check if the temperature of the core and the windings of the inductor are below a certain thermal limit, a thermal model is set up. Therefore, using the thermal model that can be seen in Fig.5.11, the temperature of the windings and the core can be determined. There are two separate thermal models for the windings and the core as can be seen in Fig.5.11(b),(c). The temperature of the windings T_W can be calculated as

$$T_W = P_W \cdot R_{th,W} + T_{coldplate} \tag{5.30}$$

where P_W are the winding losses as were described above and the $R_{th,W}$ is the thermal resistance of the windings to the cold plate where the heat is assumed to be dissipated. The thermal resistance of the windings depends on the area A_W, the length A_W, the number of turns N and the thermal conductivity of copper λ_{Cu}. The temperature of the inductor core T_{core} is similarly calculated as

$$T_{core} = P_{core} \cdot R_{th,core} + T_{ambient} \tag{5.31}$$

where P_{core} are the losses of the core as described above and $R_{th,core}$ is the core thermal resistance to the ambient where it is assumed to be dissipated. The thermal resistance of the core is dependent on the material specific thermal resistance and its dimensions. These losses are summed up with the other losses that are calculated for the semiconductors and the EMI filter in order to obtain the overall efficiency of the converter. The volume, as mentioned above, is calculated using the dimensions of the core and the bobbin size. This information is provided from the inductor manufacturers.

5.4.3. EMI filter

A filter circuit which might consist of one or several stages, is required at the input of a power converter for compliance with high frequency EMC (electromagnetic compatability) standards [24]. The filter attenuates high frequency conducted emission (CE) noise that is generated from the power converter in multiple frequencies of the switching frequency. Besides the EMI filter's role in minimizing the CE noise, the modulation scheme, the control technique as well as the appropriate switching frequency selection can also contribute in the reduction of noise.

On the other hand, the design of the input filter in power electronic systems is a crucial part of the

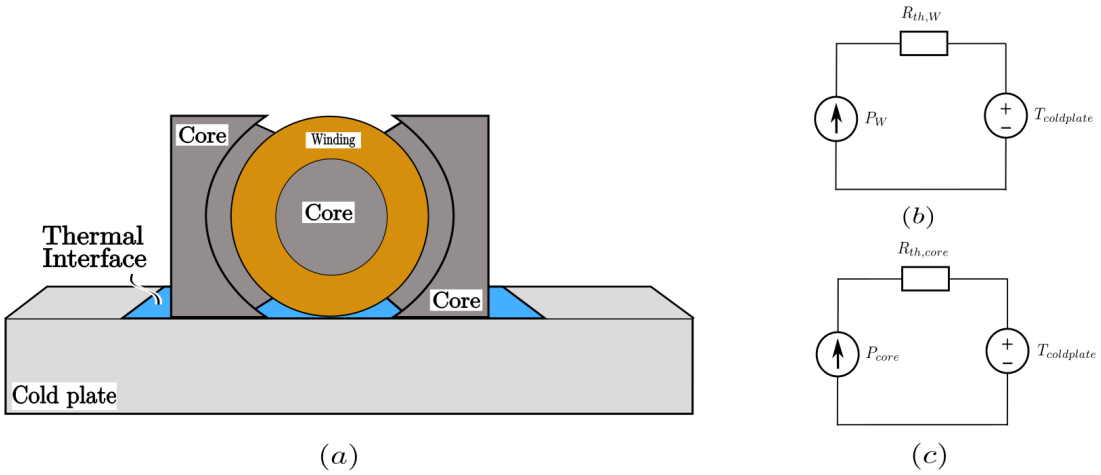


Figure 5.11: (a) Side view of inductor attached to the cold plate. (b) Electrical equivalent of the thermal model of the inductor winding and (b) the inductor core.

whole design procedure because of its significant contribution to the total volume, thus the power density of the converter. Therefore, the optimization of the volume and the power losses of the EMI filter is of high importance. Moreover, when introducing a filter in a converter, it influences the stability, size and function of the whole system. When designing an input filter, there are several design goals some of which are listed below [23]:

- Differential-mode (DM) and common-mode (CM) conducted emissions have to comply with the international EMC standard
- Passive components have limited energy storage/size capabilities.
- Sufficient passive damping with minimal losses.
- Minimum displacement factor.
- Minimum occupied volume.
- Minimization of cost.

The design of the EMI filter is based on the harmonic analysis of the input current and a model of the measurement procedure including the line impedance stabilization network (LISN). In Fig.5.12, the design procedure that is followed is depicted with the following steps.

- First, the DM/CM current in the frequency-domain is extracted from the steady-state model.
- Secondly, without the EMI filter placed between the converter and the LISN, the voltage over the LISN is calculated in order to obtain the spectrum of the unfiltered noise.
- Thirdly, the frequency of the quasi-peak (QP) is detected (the first harmonic above 150 kHz) and the amplitude of the harmonic is determined.
- The quasi-peak is compared with the EMC limit from the international standards and the required attenuation is calculated.
- Next, the filter topology is determined using PLECS/Simulink including the number of stages, the damping elements ect.
- The values of the components of the EMI filter are calculated using formulas shown below to achieve an optimized filter in terms of volume.
- The designed filter is evaluated if it fulfills the requirements regarding attenuation, losses and volume.

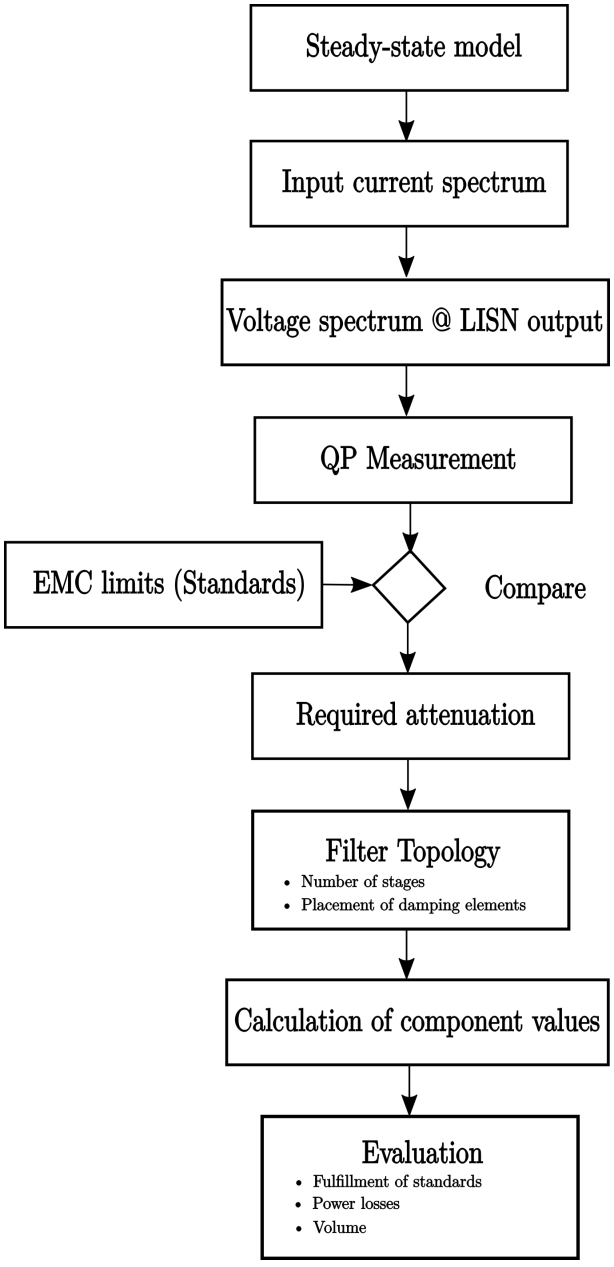


Figure 5.12: DM mode input EMI filter design procedure.

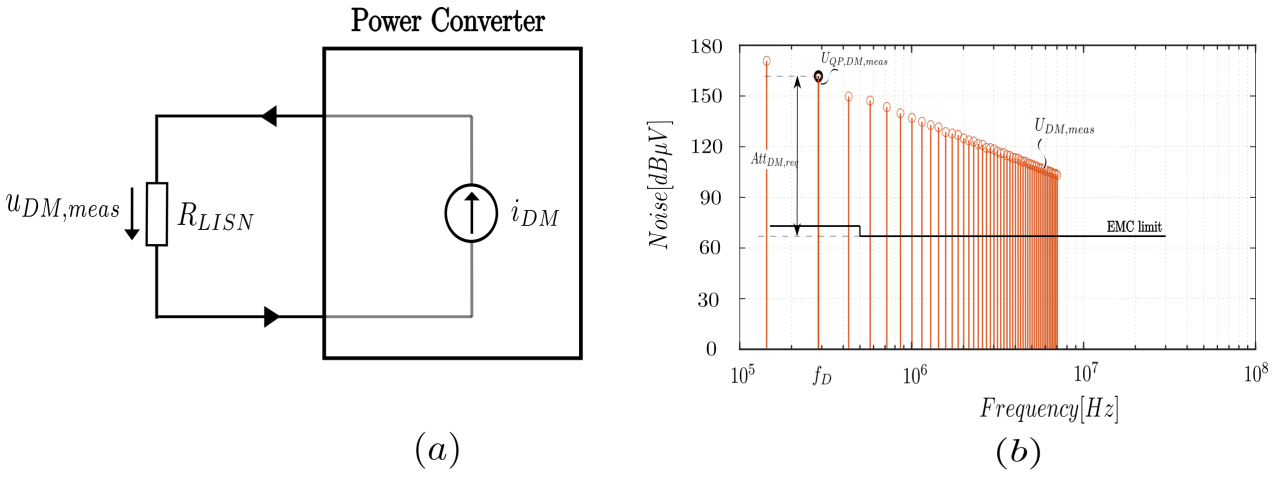


Figure 5.13: (a) Circuit representing the modelling for the calculation of the unfiltered DM noise voltage spectrum. (b) Modelled quasi-peak detection of the DM unfiltered noise voltage spectrum.

The required filter attenuation Att_{req} depends on several parameters of the converter such as the modulation scheme, the control (in Chapter 4, the importance of dead-time compensation is explained), the output power and the switching frequency. In the Belgian Rectifier, when rectifying a three-phase input, which is the main focus of this project, the switching frequency is constant, thus the most important frequency of the DM noise is the first harmonic that is higher than 150 kHz. Moreover, when there are n branches of interleaved converters, the harmonics of the DM noise are the n^{th} multiples of the switching frequency. Therefore, the first harmonic beyond 150kHz is defined as the design frequency f_D, for which a filter has to be designed to provide the required attenuation Att_{req}. In Fig.5.13(a), a simplified circuit of the line impedance stabilizing network (LISN) which is connected to the input of the power converter is depicted. This circuit is modelled in order to obtain the measured voltage spectrum $u_{DM,meas}$, using the converter spectrum $i_{DM}(j\omega)$ and the LISN impedance which in the case of this project is simply defined as a resistance $R_{LISN} = 50\Omega$. Using the voltage spectrum of the voltage over the LISN, the required attenuation of the filter for fulfilling the EMC regulation can be determined.

The spectrum of the measured voltage is the following:

$$u_{meas,DM}(j\omega) = i_{DM}(j\omega) \cdot Z_{LISN}(j\omega) \tag{5.32}$$

An EMC test receiver is used in practice to perform a quasi-peak(QP) measurement in order to determine the annoyance of a signal as can be seen in Fig.5.15(a). In this project the quasi-peak is calculated as the voltage over the R_{LISN} by assuming that the RMS of the $v_{DM,meas}$ is an estimation of the QP detection voltage.

In Fig.5.13(b), the modelled QP detection of the DM unfiltered noise can be seen. The Belgian Rectifier switching frequency is specified in Table 4.1 as $f_{sw} = 71.4kHZ$ and the number of interleaving branches is two. Therefore, the relevant harmonics of the noise are the n^{th} multiples of the switching frequency $2f_{sw}, 4f_{sw}, \ldots$. Since the international standards (CISPR 22) cover the frequencies higher than 150kHz, the first harmonic or the estimated differential-mode quasi-peak measurement is located at the frequency $4f_{sw} = 286kHz$ which is also the design frequency f_D and its amplitude can be seen in Fig.5.13(b). On the other hand, the EMC limit that is specified from the guideline CISPR 22 Class A is evidently not fulfilled without the use of an input EMI filter. The limit specified for frequencies in the range of $[150kHz, 500kHz]$ is $79dB\mu V$ and for harmonics higher than $500kHz$, the limit is $73dB\mu V$. Therefore, the required attenuation Att_{req} can be simply calculated as:

$$Att_{req}[dB\mu V] = U_{QP,DM,meas} - 79 + U_{margin} \tag{5.33}$$

Now that the required attenuation is calculated, the next step according to the procedure followed, (shown in Fig.5.12) is to define the filter topology of the DM filter. It is shown in [9, 26] that to obtain a filter with minimal volume, an LC topology with n stages, equal stage inductances $L_1 = L_2 = \ldots = L_n$

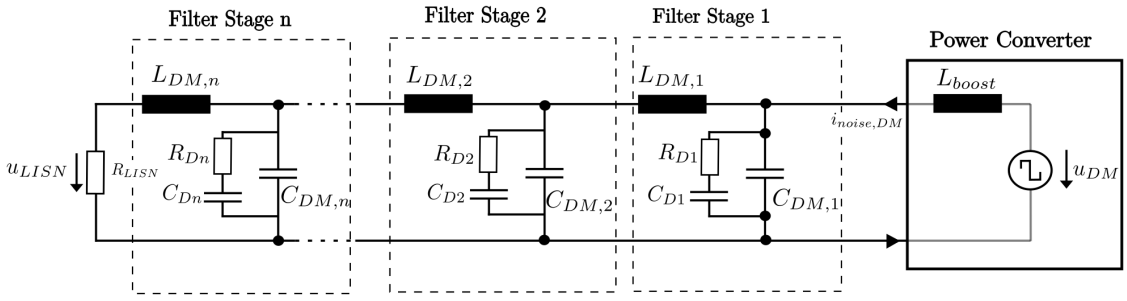


Figure 5.14: Differential-mode equivalent of the n stages LC input filter proposed in [9, 26] with RC damping branches in parallel with the capacitors.

and capacitances $C_1 = C_2 = ... = C_n$ is the optimal solution. Such an equivalent of the topology of a DM filter can be seen in Fig.5.14. The attenuation that such a topology provides assuming that the LISN is not used, is the following:

$$Att_{DM} = \frac{1}{(2\pi f_D)^{2n} \cdot L^n \cdot C^n} \tag{5.34}$$

For the filter topology, different LC structures are examined in [23]. The damping of the resonance can be implemented with three basic LC structures(among others) that are described below:

- Add in parallel with the capacitor $C_{DM,n}$, a damping capacitor C_{Dn} and a damping resistor R_{Dn} connected in series.
- Add in series with the inductor $L_{DM,n}$, a damping inductor L_{Dn} and a damping resistor L_{Dn} connected in parallel.
- Add in parallel with the inductor $L_{DM,n}$, a damping inductor L_{Dn} and a damping resistor L_{Dn} connected in series.

In the third case when a damping inductor is introduced in parallel with the inductor of the LC filter stage, the cut-off frequency is determined not only by the values of $L_{DM,n}$ and $C_{DM,n}$, but also by the damping ration $n = L_{Dn}/L_{DM,n}$ [4]. This complicates the procedure of dimensioning, therefore the first option is chosen.

If a single-stage filter is to be chosen, the cut-off frequency would have to be very low because of the -40dB/decade filter attenuation. The low cut-off frequency would require large size of filter component L, C which would result in lower power density of the overall converter. Finally, such a solution would also put a limitation in the control bandwidth and the dynamic performance of the power converter, therefore a two-stage filter is chosen [23].

The resulting topology has filter stage 1 with components $L_{DM,1} - C_{DM,1} - C_{D1} - R_{D1}$ and filter stage 2 with components $L_{DM,2} - C_{DM,2} - C_{D2} - R_{D2}$. However, the inner impedance of mains is always present, therefore $L_{DM,2}$ could be omitted. The simplified equivalent of the final selected topology of the differential-mode filter and the CE test setup can be seen in Fig.5.15.

The attenuation of this topology if the resistance of the LISN is taken into account is:

$$Att_{DM} = \frac{1}{(2\pi f_D)^{(2n-1)} \cdot R_{LISN} \cdot L^{(n-1)} \cdot C^n} \tag{5.35}$$

Since, the topology selected, the components have to be calculated. The first limitation that the EMI filter introduces is the reduction of power factor when overdimensioning the total capacitance of the system. Therefore, by setting a minimum power factor λ_{min}, the maximum allowed total DM capacitance is calculated as:

$$C_{DM,tot,max} = \frac{\sqrt{(\frac{P_{out}}{\lambda_{min}})^2 - P_{out}^2}}{\hat{V}_{ph}^2 \cdot 2\pi f_L} \tag{5.36}$$

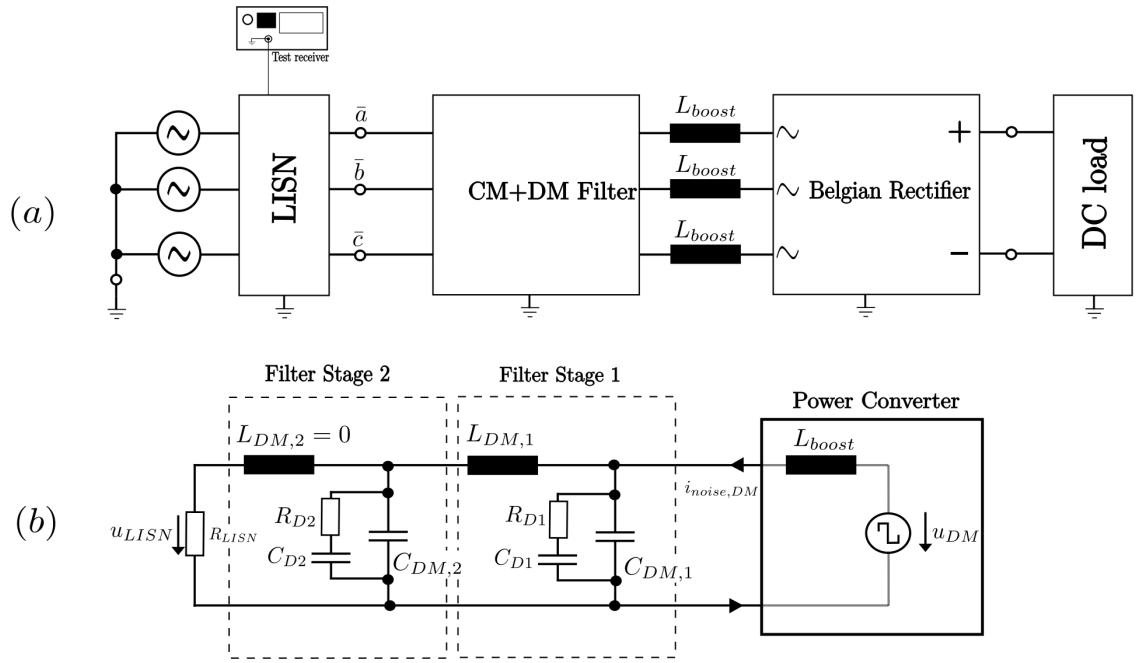


Figure 5.15: (a) CE test setup. (b) Two-stage differential-mode equivalent filter with two stages where $L_{DM,2}$ is omitted because of the inner mains impedance.

where f_L is the line frequency, P_{out} is the output active power and $\hat{V_{ph}}$ is the amplitude of the input phase voltage.

In [26], a DM filter optimization technique for minimal volume has been proposed for an n stage LCLC filter. With the same approach, but by adjusting to the CLC filter topology that can be seen in Fig.5.15, the following formula can be used to calculate the DM capacitance:

$$C_{DM,n} = \sqrt[3]{\frac{2 \cdot a_{DM} \cdot b_{DM}}{d_{DM}}}, \tag{5.37}$$

where the coefficients a_{DM}, b_{DM} and d_{DM} are defined as follows:

$$\begin{aligned} a_{DM} &= \frac{10^{(Att_{req}/20)}}{R_{LISN} \cdot (2\pi f_D)^{(2n-1)}} \\ b_{DM} &= \frac{2}{3} \cdot k_{L,powder} \cdot \hat{I}_{L_{DM}}^2 \\ d_{DM} &= 3 \cdot k_{C,foil,X2} \cdot \hat{V}_{C_{DM}}^2 \end{aligned} \tag{5.38}$$

and $k_{L,powder}$, $k_{C,foil,X2}$ are the volumetric coefficients for powder core inductors and X2 foil capacitors. $\hat{V}_{C_{DM}}$ and $\hat{I}_{L_{DM}}$ are the rated voltage and current of the capacitors and inductors, respectively. The capacitance calculated with (5.37) is compared with the maximum allowed capacitance calculated in (5.36) and if the former is lower, it is selected, otherwise the maximum allowed capacitance is selected. For the calculation of the inductance, the following relation is used [23]:

$$L_{DM,n} = \frac{a_{DM}}{C_{DM}^n} \tag{5.39}$$

where a_{DM} is defined in (5.38) and C_{DM} is calculated in (5.37) or (5.36).

Using the aforementioned methodology for the differential-mode filter design, the attenuation and the filtered differential-mode noise of the designed filter can be seen in Fig.5.16. As can be seen in Fig.

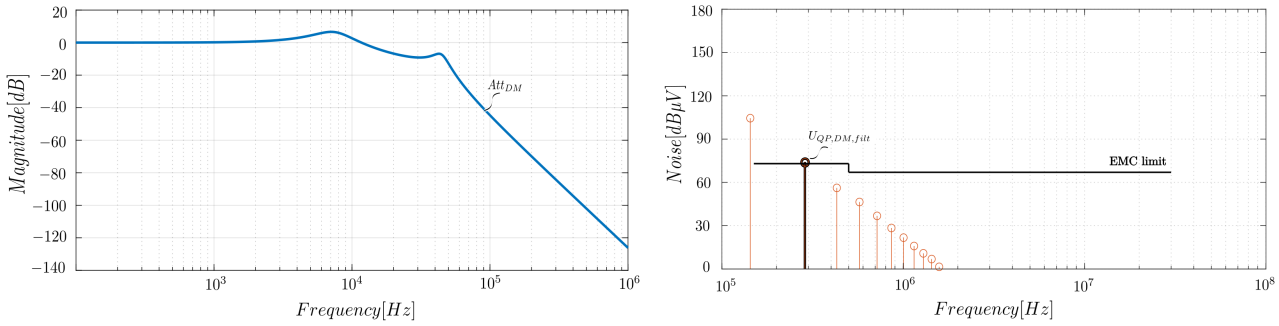


Figure 5.16: (a) Modelled filter attenuation of the designed CLC filter. (b) Modelled DM noise (voltage over the LISN) after the CLC filtering.

5.16(b), the filtered differential-mode noise is below the EMC limit defined by the CISPR standards, therefore it fulfills the relevant regulations.

Common-mode filter

For the common-mode filter, a similar approach is followed for the modelling of the quasi-peak calculation as in the differential-mode filter. In Fig.5.17(a), a simplified circuit of the line impedance stabilizing network (LISN) which is connected to the CM noise source without an EMI filter is depicted. The circuit is modelled in order to obtain the measured voltage spectrum $u_{CM,meas}$ over the LISN impedance which in the case of this project is defined as a resistance $R_{LISN} = 50\Omega$. The design procedure starts by defining the common-mode noise source u_{CM} and later by defining the equivalent circuit of filter and its components. The relevant spectrum for the CM filter design is the voltage between the DC-link center point m and the bridge leg nodes $\bar{a}$, $\bar{b}$ and $\bar{c}$ (see Fig.3.2) as can be seen below [8]:

$$u_{CM} = u_m - \frac{u_{\bar{a}} + u_{\bar{b}} + u_{\bar{c}}}{3} \tag{5.40}$$

In Fig.5.17(b), the modelled QP detection of the CM unfiltered noise can be seen as it was calculated using (5.40). As it is explained in the case of the DM filter, the harmonics of the CM are dependent on the interleaving branches and the switching frequency f_{sw}. As mentioned in the DM filter design [9, 26], to obtain a filter with minimal volume, an LC topology with n stages, equal stage inductances $L_1 = L_2 = \ldots = L_n$ and capacitances $C_1 = C_2 = \ldots C_n$ is the optimal solution. In this case the L_2 is not omitted because the equivalent resistance of the LISN is $R_{LISN}/3$. In Fig.5.18, the defined equivalent circuit of the CM filter is depicted. In the equivalent circuit, the voltage u_{CM}, the boost inductor L_{boost}, the capacitance C_{par}, as well as the LC stages of the filter can be observed.

Capacitance C_{par} emulates all the parasitic capacitances from the power circuit and the load to the protective earth (PE). If it is assumed that the heatsink is bonded to PE and the load stray capacitance is not considered, the main capacitances that contribute to C_{par} are the ones from the semiconductors to the heatsink. It is assumed that the parasitic capacitance of a single semiconductor is 120pF and the total parasitic capacitance is the sum of the capacitances of each semiconductor. Moreover, typically, a 50% margin is added to the total C_{par} to take into consideration other stray capacitances like the ones from the load to PE.

When calculating the component size of the CM filter, the main components are the inductors and the capacitors of the two stages. The main factor that plays a role in the dimensioning of the capacitor of the CM filter is the limitation introduced from the equipment safety regulations. The regulations restrain the allowable earth leakage current and therefore define requirements for the capacitors of the CM filter [8]. Typically, earth leakage is limited to $I_{PE,RMS,max} = 3.5mA$, thus the total capacitance between an input phase and the PE is limited to:

$$C_{CM,sum,max} = \frac{I_{PE,RMS,max}}{1.1 \cdot \hat{U}_{ph} \cdot 2\pi \cdot f_l} \tag{5.41}$$

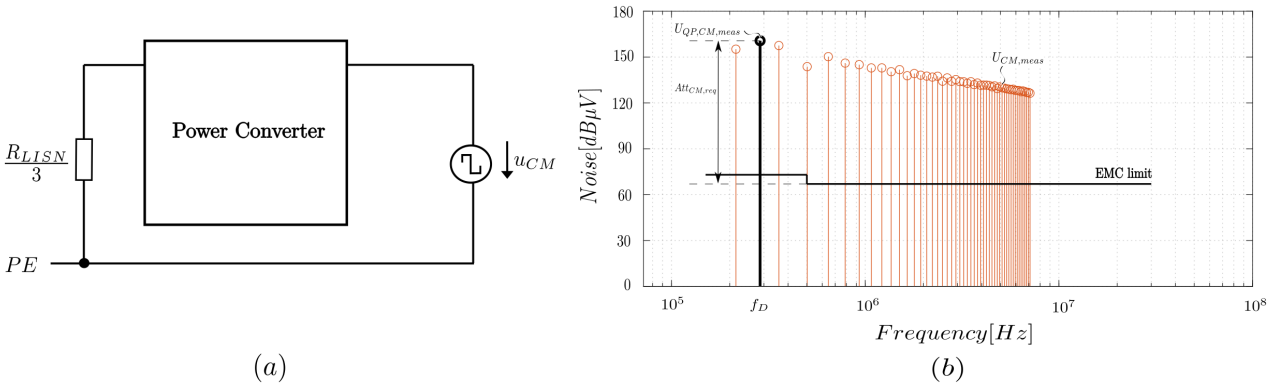


Figure 5.17: (a) Circuit representing the modelling for the calculation of the unfiltered CM noise voltage spectrum. (b) Modelled quasi-peak detection of the CM unfiltered noise voltage spectrum.

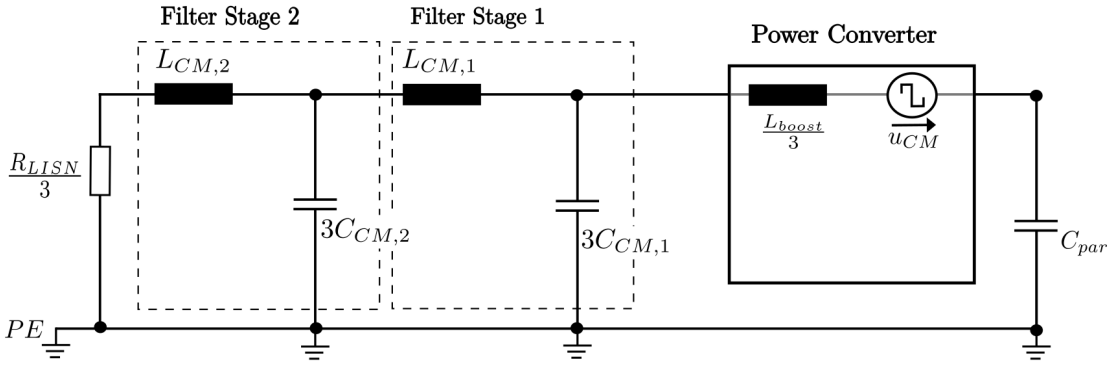


Figure 5.18: Two-stage common-mode equivalent filter with two stages LC stages.

Due to safety requirements, Y2 rated capacitors are chosen. As mentioned above, the system consists of other capacitances as well such as arrestors, stray capacitances, output CM capacitances ect. Those capacitances and a certain margin have to be subtracted from the $C_{CM,sum,max}$ as follows:

$$C_{CM,LC,max} = C_{CM,sum,max} - C_{par} - C_{CM,out} - C_{margin} \tag{5.42}$$

Therefore, the obtained maximum capacitance can be divided equally among the stages to achieve maximum attenuation. As discussed in [26], for an LCLC topology the relation between the inductance and the capacitance of a stage is:

$$L_{CM} = a_{CM} \cdot \frac{1}{C_{CM}} \tag{5.43}$$

where a_{CM} is equal to:

$$a_{CM} = \frac{\sqrt[2]{10^{Att_{req}/20}}}{(2\pi \cdot f_D)^2} \tag{5.44}$$

EMI filter losses

Starting from the DM input filter, the main contributors to the power losses are the LF losses of the inductors, the capacitors because of the equivalent series resistance and the damping. The DM inductors that are used in the EMI filter have a certain winding resistance which can be calculated or extracted from datasheets. Therefore, the losses of DM inductors is calculated as:

$$P_{L_{DM}} = 3 \cdot n \cdot (I_{ph,RMS}^2 \cdot R_{L_{DM}}) \tag{5.45}$$

For the losses of the capacitors, the ELR is extracted from the datasheet provided by the manufacturer. The resistance of the capacitor depends on the frequency f, the temperature T_c and the DC offset

voltage V_{DC}. The RMS current that flows through the capacitor is calculated using the state space equations of the EMI circuit built in PLECS. Therefore, the power loss of the DM capacitor is:

$$P_{C_{DM}} = 3 \cdot n \cdot (I^2_{C_{DM},RMS} \cdot R_{C_{DM}}) \tag{5.46}$$

The losses of the damping resistors can be calculated using the RMS current that flows through them and their resistance. This current is calculated using the state space equations (extracted from a PLECS model where the topology of the EMI filter is built) of the filter where the relevant DM current input is given. Therefore, the power loss of the DM damping resistors are:

$$P_{R_D} = 3 \cdot n \cdot (I^2_{R_D,RMS} \cdot R_D) \tag{5.47}$$

The losses of the CM part of the EMI filter are mainly specified by the LF current that flows through the windings of the CM choke. Using the skin depth δ at 50Hz, the effective area of the current flow can be calculated as:

$$A_{eff} = (d_w - 2\delta)^2 \cdot \frac{\pi}{4} \tag{5.48}$$

Moreover, assuming that the temperature of the CM choke winding is T_{CM}, the specific resistance of copper at T_{CM} is:

$$\rho_{T_{CM}} = \rho_{20} \cdot (1 + \alpha \cdot (T_{CM} - 20)) \tag{5.49}$$

, where ρ_{20} is the specific resistance of copper at $20^o C$ and α is the thermal resistance coefficient of copper. Therefore, the resistance of the common-mode choke winding is:

$$R_{CM,choke,wind} = \frac{\rho_{T_{CM}} \cdot l_w}{A_{eff}} \tag{5.50}$$

where l_w is the length of the wire of one winding. Finally, the power loss of a CM choke with N windings is calculated as:

$$P_{CM,choke} = (I^2_{ph,RMS} \cdot N \cdot R_{CM,choke,wind}) \tag{5.51}$$

EMI filter volume

Starting with the DM filter, the volume of the inductors and capacitors are dependant on the rated current and voltage, respectively, as well as on their inductance and capacitance. This relationship can be visually described in Fig.5.19 where the volumetric coefficients of the components specify the final volume they occupy. The calculation of the volume for the DM inductors is done as follows:

$$V_{LDM} = k_{L,powder} \cdot L_{DM} \cdot I^2_{RMS} \tag{5.52}$$

The calculation of the volume for the DM X2 foil capacitors is done as follows:

$$V_{CDM} = k_{C,X2,foil} \cdot C_{DM} \cdot V^2_{RMS} \tag{5.53}$$

Similarly, for the CM filter Y1 capacitors, the volume is derived from the volumetric coefficients, the amount of capacitance and the rated RMS voltage as follows:

$$V_{CCM} = k_{C,Y1,foil} \cdot C_{CM} \cdot V^2_{RMS} \tag{5.54}$$

In order to take into consideration the routing, connections and other practical parameters that take space around these components, a certain margin is added to the volume of each inductor and capacitor.

Finally, the large component that takes significant amount of space in the EMI filter is the common-mode choke. As proposed in [8], the selected material is nanocrystalline VITROPERM500F because of its low volume per unit inductance. The impedance of the choke has been empirically derived from the material's complex permeability curves as:

$$Z_{choke}(f) \cong 10^{2.243 - 2 \cdot log(I_{RMS}) + 0.181 \cdot log(|\mu(f)| \cdot f) \cdot log(A_e A_w))} \tag{5.55}$$

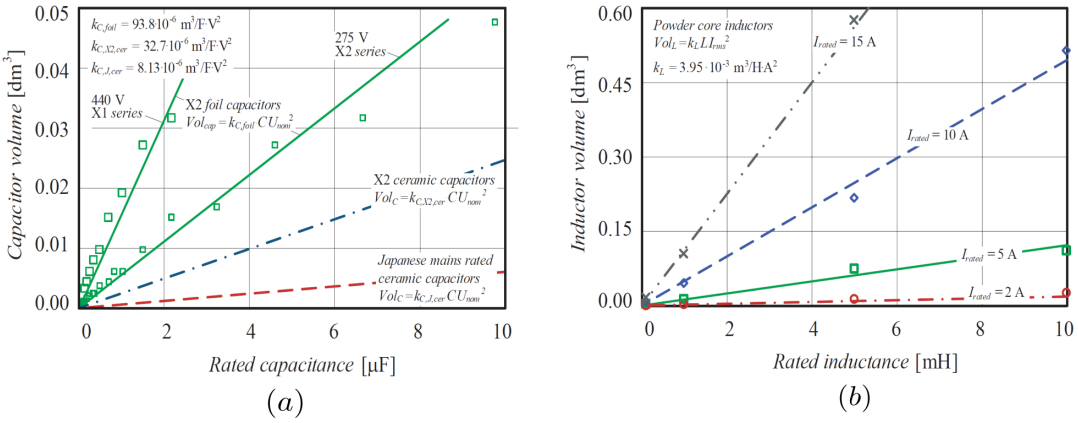


Figure 5.19: Volume and volumetric coefficients of (a) capacitors for various mains rated type and (b) of powder core inductors [8].

However, the impedance of the CM choke can be calculated from the inductance specified in (5.43) as:

$$Z_{choke}(f) = L_{CM} \cdot f \cdot 2\pi \tag{5.56}$$

If (5.55),(5.56) are solved for the design frequency f_D, the product of areas $A_e A_w$ can be calculated. This leads to the core size and volume calculation using the curves that describe the properties of the core material VAC VITROPERM 500F shown in [8]. In Matlab, the relation between the product of areas and the boxed volume is done using interpolation.

5.5. Efficiency & volume

The main parts of the Belgian Rectifier that cause power losses are HF semiconductors, the boost inductors, the EMI input and output filters, as well as losses of the control circuit, connectors and bleeding losses. For the control/auxiliary circuit that consists of the low voltage supplies, the microprocessor on chip (SoC) ets, the losses are estimated from the datasheets. The semiconductor, boost inductor and the EMI losses are calculated as explained in the previous section. Therefore, the total losses of the converter are calculated as:

$$P_{loss,tot} = P_{semi} + P_{ind} + P_{EMI} + P_{bleed} + P_{control} \tag{5.57}$$

And from the total losses, the efficiency of the converter is calculated as:

$$\eta_{converter} = \frac{P_{in} - P_{loss,tot}}{P_{in}} \tag{5.58}$$

For the volume calculation, the sub-volumes considered in the model of the Belgian Rectifier are the volumes of the inductors, the semiconductors together with the metal core PCB, the water cooling plate, the EMI filter, the output bulk capacitors, the control/auxiliary board and the aluminium block connecting thermally the semiconductors to the cooling plate. The volumes of these sub-systems are added to gain the total volume of the converter as:

$$V_{tot} = V_{semi,MCPCB} + V_{ind} + V_{EMI} + V_{bulk} + V_{control} + V_{alum,block} \tag{5.59}$$

Using the total volume V_{tot} calculated with (5.59) and the output power P_{out} of the converter, the power density can be calculated as:

$$\rho_{converter} = \frac{P_{out}}{V_{tot}} \tag{5.60}$$

In Fig. 5.20, a representation of the total volume of the converter is depicted. It should be noted that the output bulk capacitors do not take place in the compact converter design, but are considered to be on a separate board. Moreover, in Fig.5.20, the EMI volume is presented as a boxed volume next to the boost inductors and semiconductors. This boxed volume represents the sum of the volumes of the CM chokes, the DM inductors and the DM/CM capacitors of the input and output EMI filter.

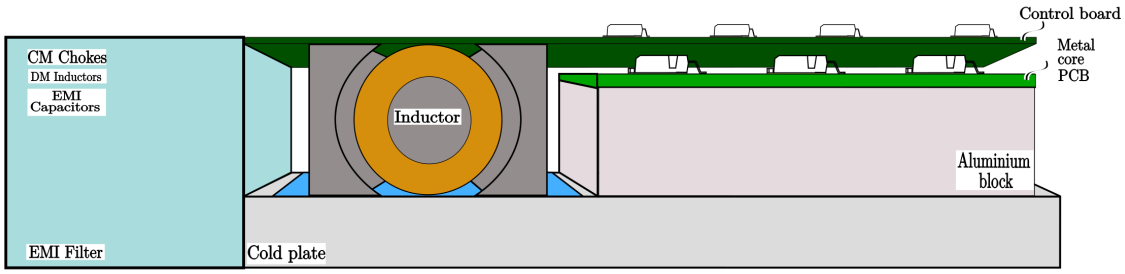


Figure 5.20: Representation of the total volume of the converter including the semiconductors, inductors, EMI components, control board and wasted volume of air and aluminium block.

5.6. Summary

In this chapter, a detailed explanation of the modelling approach of the converter is conducted. Starting from the high level specifications of the converter, the full procedure is covered until the calculation of the efficiency and power density of the converter. The use of Fourier analysis in the switching model, that provides the waveforms and spectrum of all the relevant voltages and current, is argued regarding its benefits.

Additionally, a detailed analysis of the multi-physics semiconductor, inductor and EMI filter models is executed. The thermal models of the semiconductors and inductors are discussed and their electrical equivalents are derived. An automated procedure of input DM/CM EMI filter design which aims for the lowest possible volume is presented.

Finally, the total calculation of efficiency and volume is described, accompanied by a $3D$ schematic of the designed converter in order to give an idea of how the components are connected to each other in terms of space.

6

Multi-Objective Optimization

6.1. Introduction

The models described in Chapter 5 are used to conduct a virtual prototyping routine by sweeping through a number of inductance and frequency values, as well as the number of interleaving branches of the converter and the number of parallel transistors per switch. The aim of the virtual prototyping routine is to derive the performance trade-offs dependent on the aforementioned parameters for the Belgian Rectifier. Therefore, a wide design space can be specified and several implementations can be designed and evaluated in a performance space which consists of the efficiency and power density.

From the virtual prototyping routine, one or multiple optimal designs are possible to appear. The generated designs are explained in terms of the dependencies and the trade-offs in order to demonstrate the accuracy of the proposed method and analyze what design parameters conclude in optimal designs.

For every iteration on the design space, the efficiency and power density are calculated, therefore the design space is drafted onto the performance space fully. Pareto-fronts are the outcome of the developed performance space. This front of power density versus efficiency offer the possibility to select an optimal design which depends on the optimization objective (efficiency, power density).

6.2. Virtual prototyping routine

As mentioned above, a virtual prototyping routine is used to automatically map the design space onto the performance space of a certain converter topology, in particular for this project, the Belgian Rectifier. The performance space is derived and it consists of the power density and the efficiency of the converter for the parameters defined in the design space. In Fig.6.1, the flow diagram of the proposed virtual prototyping routine can be seen. It is evident that it consists of three major blocks, namely the Global Design Space, the Component Design Space and the Performance Space.

The parameters that define the Global Design Space of a PFC Rectifier are the input, output voltages and currents, the line and switching frequencies, the number of interleaved branches, the number of parallel transistors per bridge leg etc. These parameters can either be set to a constant single-element value or to a multiple-element vector that is used to conduct a routine. As it is mentioned above, the parameters that are chosen in this project to constitute a vector, and therefore sweep through them, are the switching frequency f_{sw}, the boost inductance L_{boost}, the interleaving branches N_{br} and the parallel transistors per switch Tr_{par}. The component design space consists of the parameters for the components selection such as the boost inductors, the semiconductors and the EMI filter. Finally, the models that are described in Chapter 5 and can be seen in Fig.5.1 output the power losses and the volume of the each component group (inductors, semiconductors, EMI) which are summed up to obtain the total efficiency and power density of a single design. By iterating through the parameters of the design space, a Pareto front of the power density versus efficiency is achieved which can be seen in Fig.6.1.

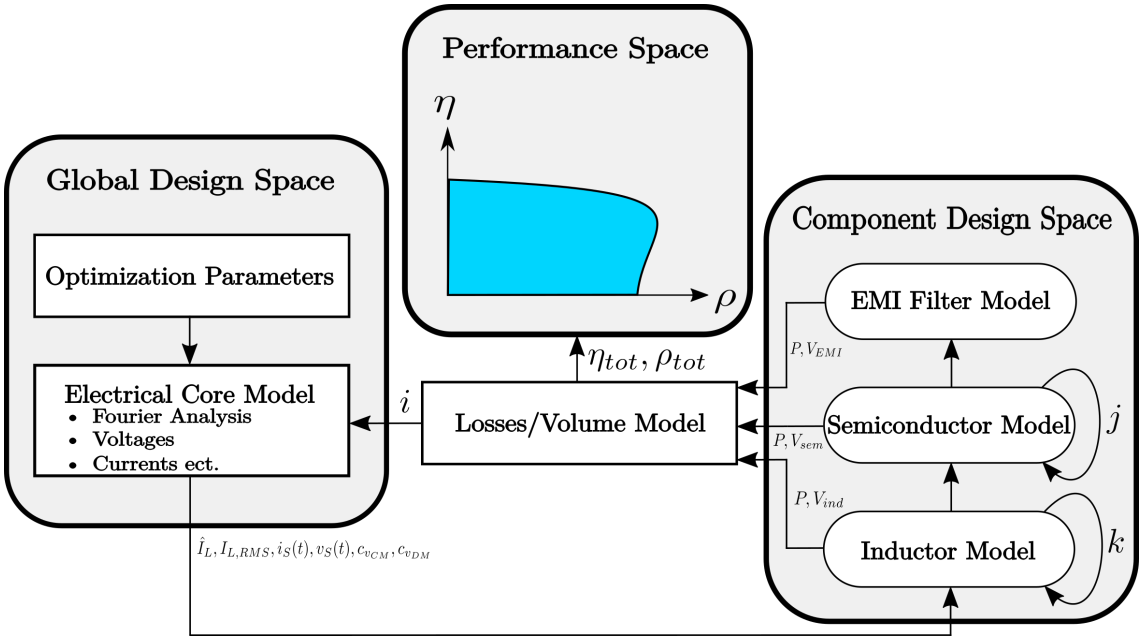


Figure 6.1: Virtual prototyping routine that employs the models described in Chapter 5.

Looking closely at Fig.6.1, it can be observed that several loops take place in the whole virtual prototyping routine. The procedure starts by specifying the global design space and is followed by a large loop (iterations i) that starts with the electrical core model. The latter generates all the quantities (voltages, currents ect) and waveforms in time-domain and frequency-domain that are required from the component models. Next, the component models take place that also execute smaller loops (iterations j, k). The iterations of the component models sweep through the component design space which consists of parameters such as inductor cores or type of core material and conclude with an optimal design of the component that respects the thermal limits and demonstrate the lowest possible power losses and/or volume. Finally, the large loop results with calculating the power density and the efficiency of a converter for a single set of global design space parameters. After i iterations of the large loop, the whole of the global design space is drafted onto the performance space in the form of a Pareto-front from which an optimal design is picked out.

6.3. Approach

For the purpose of this research project, a 22kW Belgian Rectifier is designed. In Table 6.1, the design requirements for which the Belgian Rectifier is optimized are shown. Therefore, the converter is assumed to be connected to a $400V$ line-to-line, $50Hz$ AC grid and the output nominal DC voltage is assumed to be 750V for charging an electric vehicle battery. For providing isolation and voltage adjustment, an isolated DC-DC supply (e.g. DAB) is the intermediate part between the three-phase PFC rectifier and the battery, but it is not in the scope of this project and does not participate in the total efficiency and power density calculation. Moreover, the full output power of the converter is assumed to be 22kW. Finally, the requirements on the performance space are efficiency higher than 97.5% and power density higher than $3kW/L$.

The aforementioned design requirements (except the performance space requirements) are part of the global design space and are set to the fixed values displayed in Table 6.1. The other global design space parameters that need to be defined are the EMI compliance, the power factor λ, the switching frequency f_{sw}, the boost inductance L_{boost}, the number of interleaving branches N_{br} and the number of parallel transistors per bridge-leg Tr_{par}. The last four parameters play a significant role in the mapping of the performance space, therefore a large range of values is set to achieve an optimal design. The switching frequency f_{sw} and boost inductance L_{boost} vectors are chosen such that an inductor design can be achieved and thermal limitations can be respected for both the inductors and semiconductors.

Description	Parameter	Value
AC line input voltage	$v_{ac,line-line}$	$400V$
DC output nominal voltage	$v_{out,nom}$	$750V$
DC output voltage range	$v_{out,range}$	$[650, 850]V$
Full output power	P_{out}	$22kW$
Line frequency	f_L	$50Hz$
Full load efficiency	$\eta_{Full,load}$	$> 97.5\%$
Power density	$\rho_{Full,load}$	$> 3kW/L$
Power factor	$\lambda_{Full,load}$	> 0.99
EMI	-	CISPR 22, Class A
Maximum earth leakage	$I_{PE,RMS,max}$	$3.5mA$

Table 6.1: Design requirements for the three-phase boost-type Belgian PFC Rectifier.

Description	Parameter	Vector	Unit
Switching frequency	f_{sw}	$[24, ..., 300]$	kHz
Boost inductance	L_{boost}	$[2.5, ..., 150]$	μH
Interleaving branches	N_{br}	$[1, 2, 3]$	Branches
Parallel transistors	Tr_{par}	$[1, 2]$	Transistors

Table 6.2: Global design space parameters selected as variables with a large range to deliver a performance space that demonstrates the limits of the converter.

The vectors of the design space parameters can be seen in Table 6.2. The switching frequency and the boost inductor play a crucial role in the performance of the inductor because they specify quantities such as the inductor current ripple, peak current and ZVS switching among others. Therefore, the inductance L_{boost} is specified as a 22-element vector in the range of $[2.5, ..., 150]\mu H$ and the switching frequency f_{sw} is specified as a 20-element vector in the range of $[24, ..., 300]kHz$.

The number of interleaving branches also plays a crucial role in the performance of the converter because they split the power into the number of branches and they decrease the ripple of the input/output current. An example of two interleaving branches can be seen in Fig. 6.10. The chosen carrier wave is the triangular carrier due to the symmetrical modulation that can be achieved as it is explained in Chapter 3. For each interleaving branch of the converter, there is a carrier phase shift which depends on the number of branches as

$$\phi_i = \phi_1 + (\frac{2 \cdot \pi}{N_{br}}) \cdot i, i = [1, 2, ..., N_{br}] \tag{6.1}$$

Where i is the index of the interleaving branch and N_{br} is the total number of interleaving branches. As it is mentioned in Chapter 3, the derived duty cycles are valid for a certain phase-shift between the carrier waves of the top boost circuit, the bottom boost circuit and the rectifier stage at one interleaving branch. For each of the rest of the interleaving branches, all the carrier waves have an equal phase-shift calculated in (6.1). The introduction of interleaving introduces benefits such as lower ripple of the phase current and smaller EMI filtering requirements.

The number of transistors placed in parallel is also significant especially at high power levels where the switch currents can increase the junction temperatures to unaccepted levels. If a number of parallel transistors is introduced, the current is split between them, thus making possible the flow of higher current. Moreover, parallel transistors decrease the equivalent $R_{DS,(on)}$ resistance, thus the conduction losses of the switches. The bridge leg A of the rectifier stage when the number of parallel switches is $Tr_{par} = 1$ is shown in Fig.6.2(a) and when the number of parallel switches is $Tr_{par} = 2$ is shown in Fig.6.2(b). The component design space can be seen in Table 6.3 where the most important component design parameters are shown. As can be seen in Fig. 6.1, the main parts or components of a power electronics converter like the Belgian Rectifier are the Semiconductors (only HF semiconductors

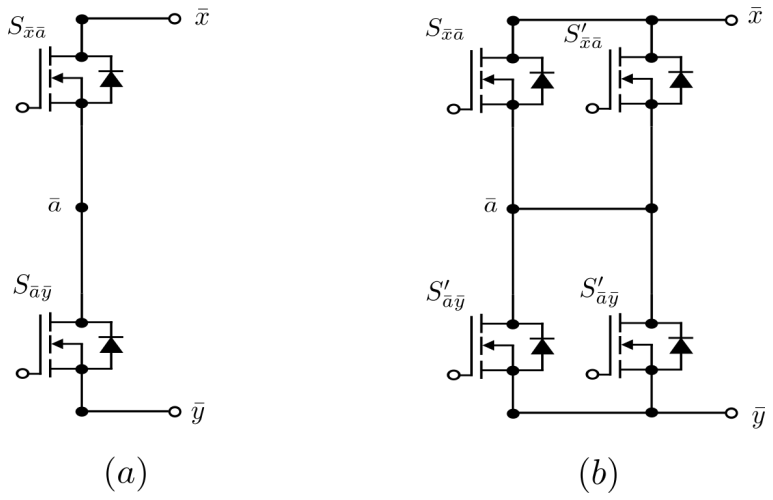


Figure 6.2: Bridge leg A of the rectifier stage and the number of parallel transistors is (a) one and (b) two.

in the Belgian Rectifier), the inductors and the EMI filter.

The semiconductors that are chosen are two SiC MOSFETS that were discussed in Chapter 5 as well (See Table 5.1). These semiconductors are selected due to their advantageous characteristics regarding power losses and thermal limits, and most importantly because of their rated voltage and current. For the cooling of the semiconductors, a coldplate and metal-core PCB are used which can be observed in Fig.5.9. Between the metal-core PCB and the coldplate, an aluminium block is placed for practical limitations of the board. The height of the aluminium block, as can be seen in Fig.5.20, is adjusted according to the height of the inductor core that sits on its left. Moreover, the cooling area around a semiconductor is chosen such that the semiconductor does not exceed the thermal limits. Therefore, the cooling block is optimized for volume and makes sure that all semiconductors operate inside the safe thermal limits.

Five inductor core sizes participate in the inductor design space. The core size plays an important role on the power density of the converter and PQ cores are selected as can be seen in Table 6.3. In order to limit the component design space and make the virtual prototyping routine faster, the inductor core material is specified as N95 because of the advantages it demonstrates regarding flux density and core losses and, the selected inductor wire is specified as Litz wire because of its low skin effect and proximity effect losses which are calculated in Chapter 5. An optimal design which is optimized for volume and power losses is provided from the inductor design model. The inductor thermal model calculates the winding and core temperature of each designed inductor and the ones that exceed the thermal limits are rejected. The cooling material for the inductor is the coldplate as can be seen in Fig.5.20. The cooling area of the inductor is not adjustable as it is the case for the semiconductors.

As it is explained in Chapter 5, the DM EMI input filter is designed as a CLC topology and its components are calculated for optimal volume. Similarly, the CM input filter is designed as a $LCLC$ topology and its components are calculated for optimal volume and for the limitation of the leakage current to a certain value (3.5mA). The DM output EMI filter is a fixed design since there are no requirements regarding the attenuation of the noise at the output. The bulk capacitor is again set to a fixed value $V_{out} = 1.25mF$ and its volume is calculated from datasheet information provided by the manufacturers.

Using the global and local design space that is described above, a certain number of iterations, that are dependent on the size of the parameter vectors, are performed. For each iteration, if an inductor and heatsink design that respect the thermal limits are achieved, the efficiency and the power density of the converter are calculated. Therefore, because of the wide range of boost inductance and switching frequency values, a satisfactory projection of the performance space is accomplished on a Pareto-front.

Regarding the modelling time consumption, the most important parameters are the grid cycle points,

Component	Alternatives	Remarks
Semiconductors	SCTH100N120G2AG SCTH90N65G2V7	1200V SiC MOSFET 600V SiC MOSFET
Cooling	Metal-core PCB Coldplate	Aluminium block separates the two. See. Fig.5.20
Inductor core	PQ50/50 PQ60/42 PQ60/52 PQ65/44 PQ65/54	
Core material	N95	
Inductor winding	Litz wire	
DM EMI input filter	CLC filter	Volume optimized
CM EMI input filter	LCLC filter	Volume optimized
EMI output filter	DM: LC filter Bulk Capacitors	Fixed arrangement and size

Table 6.3: Component design space for the Belgian Rectifier virtual prototyping routine.

Modelling Parameter	Value
Grid cycle points	96
Switching cycle points	200
Fourier Harmonics	100

Table 6.4: Modelling variables that affect significantly the calculation time of the virtual prototyping routine.

the switching cycle points and the fourier harmonics. The values of these modelling parameters can be seen in Table 6.4. The reason why these values were chosen is the shorter computational time per iteration which is around 37 seconds and the total calculation time of the virtual prototyping routine which is approximately 4.6 hours for 440 iterations. It should be noted that significant time is saved when there is no inductor design because the semiconductor, EMI, inductor calculation, efficiency and volume models are not run at all for the specific iteration.

6.4. Optimization outcome

In this section, the outcome of the virtual prototyping routine for the global design space and the component design space shown in Table 6.2 and Table 6.3 is shown and interpreted. Except the switching frequency f_{sw} and boost inductance L_{boost}, there are Pareto-fronts generated for different values of interleaving branches $N_{br} = 1, 2, 3$ and parallel transistors per switch $Tr_{par} = 1, 2$.

In Fig.6.3(a) and Fig.6.3(b), the Pareto-fronts of the Belgian Rectifier are shown for different number of interleaving branches and fixed number of paralleled transistors per switch, no-transistors in parallel per switch $Tr_{par} = 1$ and one-transistor in parallel per switch $Tr_{par} = 2$, respectively. It can be observed that the Pareto-front for no-interleaving branches in Fig.6.3(a) is missing because the topology cannot deliver the required output power $P_{out} = 22kW$ with $N_{br} = 1$ and $Tr_{par} = 1$. However, in Fig. 6.3(a) it can be observed that the Pareto-front for once-interleaving $N_{br} = 2$ shows higher power density and lower efficiency than the twice-interleaving $N_{br} = 3$ case. This happens because for each interleaving branch, there is a need for three extra boost inductors that occupy space and decrease the power density. Moreover, due to the fact that the number of HF semiconductors used for the delivery of the power for twice-inteleaving $N_{br} = 3$ is 50% larger than for once-interleaving $N_{br} = 2$, the efficiency increases. The same pattern can be seen in Fig.6.3(b) for $Tr_{par} = 2$ where the power density drops and the efficiency increases as the number of interleaving branches increase. Nevertheless, it can be seen that for once-interleving $N_{br} = 2$, the power density and efficiency are the highest possible, therefore this is the design choice for the Belgian Rectifier.

Another important parameter is the number of transistors in parallel per switch Tr_{par}. In Fig.6.4(a)

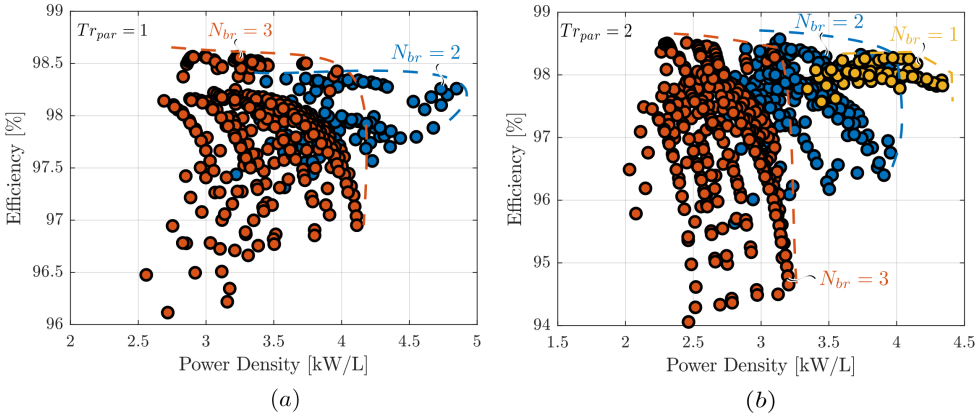


Figure 6.3: Pareto-front of efficiency versus power density demonstrating the impact of interleaving branches on the performance space of the Belgian Rectifier for the global and component design spaces defined in Table 6.2 and Table 6.3. (a) Performance space for once-interleaved $N_{br} = 2$ versus twice-interleaved $N_{br} = 3$ for no transistors in parallel per switch $Tr_{par} = 1$. (b) Performance space for non-interleaved $N_{br} = 1$ versus once-interleaved $N_{br} = 2$ versus twice-interleaved $N_{br} = 3$ for one transistor in parallel per switch $Tr_{par} = 2$. Semiconductor used in the rectifier stage is the SCTH100N120G2AG and in the boost circuits is the SCTH90N65G2V7.

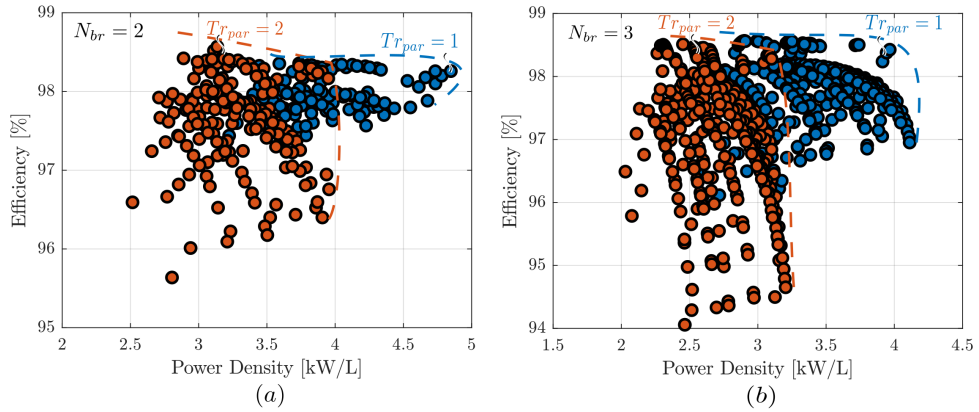


Figure 6.4: Pareto-front of efficiency versus power density demonstrating the impact of parallel transistors per switch on the performance space of the Belgian Rectifier for the global and component design spaces defined in Table 6.2 and Table 6.3. (a) Performance space for no-transistors in parallel per switch $Tr_{par} = 1$ versus one-transistor in parallel per switch $Tr_{par} = 2$ for once-interleaved $N_{br} = 2$. (b) Performance space for no-transistors in parallel per switch $Tr_{par} = 1$ versus one-transistor in parallel per switch $Tr_{par} = 2$ for twice-interleaved $N_{br} = 3$. Semiconductor used in the rectifier stage is the SCTH100N120G2AG and in the boost circuits is the SCTH90N65G2V7.

and Fig.6.4(b), the dependency of the efficiency and power density on $Tr_{par} = 1, 2$ is shown and interpreted, for once-interleaved $N_{br} = 2$ and twice-interleaved $N_{br} = 3$, respectively. By introducing the number of paralleled transistors, it is obvious that the power density will decrease due to the larger space that the semiconductors, MCPCB, aluminium block and cold plate occupy. However, the equivalent on-resistance $R_{DS,(on)}$ decreases because of the simple principle of paralleled resistances, therefore the efficiency is expected to increase overall. This can be proven in Fig.6.4(a) where it is evident that the $Tr_{par} = 2$ Pareto-front shows higher efficiency on the expense of power density. It is decided, however, that the cost of the power density (around $1kW/L$) is too high for the higher efficiency, therefore no-transistors in parallel $Tr_{par} = 1$ is the design choice for the Belgian Rectifier. A more detailed analysis of the impact of paralleled transistors can be seen further below in this section.

Moreover, there are two semiconductors in the component design space, namely SCTH100N120G2AG (1200-V) and SCTH90N65G2V7(650-V). For the rectifier stage, the only option is the SCTH100N120G2AG because the voltage that falls over the switches is higher than 650V in nominal condition. In the boost circuits, however, both semiconductors can be used and in Fig.6.5, the Pareto-fronts for boost circuit semiconductors SCTH90N65G2V7 and SCTH100N120G2AG are shown. It can be observed

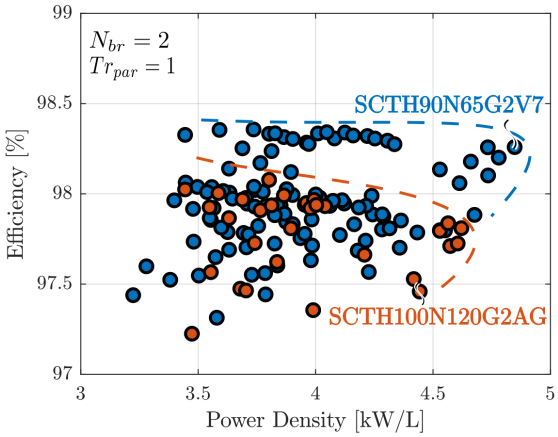


Figure 6.5: Pareto-front of efficiency versus power density demonstrating the impact of the semiconductor type on the performance space of the Belgian Rectifier for the global and component design spaces defined in Table 6.2 and Table 6.3. Semiconductor used in the rectifier stage is the SCTH100N120G2AG, whereas semiconductor used in the boost circuits is SCTH100N120G2AG (red Pareto front) and SCTH90N65G2V7 (blue Pareto front).

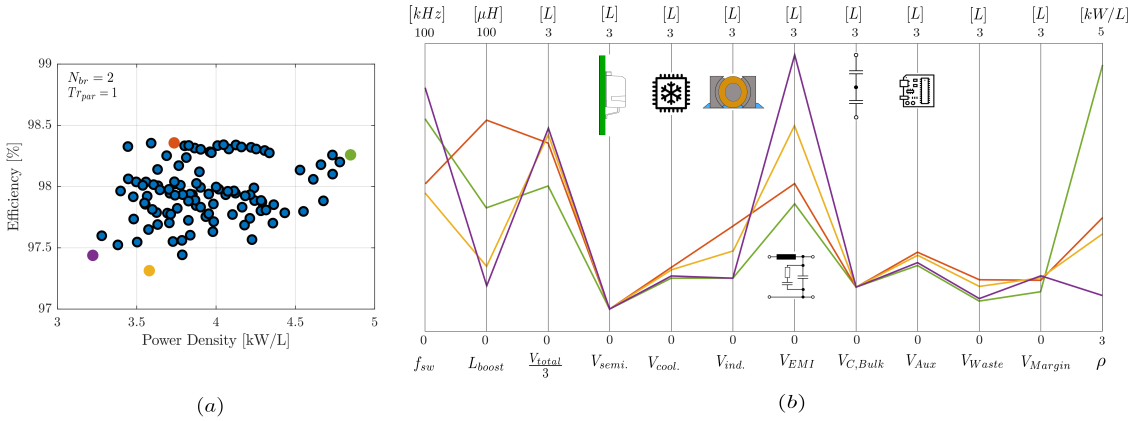
that when using SCTH90N65G2V7, the efficiency and power density are higher than when using SCTH100N120G2AG. This can be explained from the fact that the turn-on E_{on}, turn-off E_{off} energies and the on-resistance $R_{DS,(on)}$ of SCTH90N65G2V7 (see Table 5.1 for typical values) are lower than the values of SCTH100N120G2AG. This means less conduction and switching losses, thus smaller heatsink. Therefore, SCTH90N65G2V7 is the design choice for the boost circuits of the Belgian Rectifier.

Volume breakdown

To understand the main volume contributors in the Belgian Rectifier, a volume breakdown is done for four different designs that exhibit highest and lowest efficiencies and power densities. The analyzed designs can be seen in Fig.6.6(a) where the performance space for once-interleaved $N_{br} = 2$ and no-transistors in parallel per switch $Tr_{par} = 1$ is shown. The volume breakdown of the four designs can be seen in Fig.6.6(b). Starting from the semiconductors, there is no difference since the number of transistors is the same. Moreover, the cooling volume (cold plate and MCPCB) has some minor variation which depends on the junction temperature of the semiconductors and the inductor volume depends on the selected inductor core.

The inductor volume plays a significant role in the total volume of the converter and it varies importantly for different cores. However, the main contributor of volume for all the designs is the EMI filter. There is a significant dependency of the EMI filter volume on the switching frequency f_{sw} and the CISPR standards (150kHz threshold). The green design has a switching frequency of $f_{sw} = 72kHz$, thus, for once-interleaving $N_{br} = 2$, the effective frequency is $2 \cdot f_{sw} = 144kHz$ and the first harmonic above the $150kHz$ threshold defined in CISPR 22 Class A is $288kHz$. On the other hand, the purple design switching frequency is $f_{sw} = 84kHz$, thus the effective frequency of the DM/CM noise is $2 \cdot f_{sw} = 168kHz$ which is already above the $150kHz$ threshold. Therefore, the EMI in the second case has to attenuate a lower frequency which requires larger passive components (inductors, capacitors). Therefore, the large difference of EMI filter between the designs is fully justified. Moreover, the EMI filter occupies approximately one third of the total volume as it is generally expected.

The bulk capacitors also play a significant role in the total volume, but in this research, they are a fixed design. If there was a specific voltage ripple requirement considered, they could also become a variable. Finally, the control/auxiliary board volume, the wasted volume (aluminium block) and the margin volumes mainly depend on the semiconductors and the total volume, therefore they do not defer significantly between designs.



(a) (b)

Figure 6.6: (a) Performance space for no-transistors in parallel per switch $Tr_{par} = 1$ and once-interleaved $N_{br} = 2$ Belgian Rectifier. (b) Volume breakdown of four designs of the Belgian Rectifier with the following colors: Red - Highest efficiency design ($\eta = 98.36\%, \rho = 3.736kW/L$, $f_{sw} = 54kHz$, $L_{boost} = 70\mu H$), Green - Highest power density design ($\eta = 98.26\%, \rho = 4.848kW/L$, $f_{sw} = 72kHz$, $L_{boost} = 40\mu H$), Orange - Lowest efficiency design ($\eta = 97.31\%, \rho = 3.579kW/L$, $f_{sw} = 48kHz$, $L_{boost} = 20\mu H$), Purple - Lowest power density design ($\eta = 97.44\%, \rho = 3.223kW/L$, $f_{sw} = 84kHz$, $L_{boost} = 15\mu H$). Semiconductor used in rectifier stage is the SCTH100N120G2AG and in the boost circuits is the SCTH90N65G2V7.

Finally, two things worth mentioning: First, the aluminium block(wasted volume) occupies important space. This can be improved by making a new mechanical design where the metal-core PCB is connected immediately to the coldplate without the intermediate aluminium block. Secondly, the number of inductor cores in the component design space can be further extended. These two facts can result in a higher power density of the converter, as well as in more performance space variances.

Power loss breakdown

For the same designs, a power loss breakdown is done to understand the main loss contributors in the Belgian Rectifier. The analyzed designs can be seen in Fig.6.7(a) where the performance space is shown. By looking at Fig.6.7(b), it can be easily observed that the semiconductor losses play the most significant role in the Belgian Rectifier (more than half of the total losses in two designs). This is justified from the large number of switches (10 per branch) that participate in the converter topology. The designs (purple, orange) with the lowest boost inductances show higher semiconductor losses as expected, but for different reasons. For the orange design, the conduction losses are more important because of the high current ripple that occurs due to low inductance $L_{boost} = 20\mu H$ and $f_{sw} = 48kHz$ whereas the switching losses are relatively limited due to soft-switching (not in the whole line cycle). For the purple design($L_{boost} = 15\mu H$ and $f_{sw} = 84kHz$), the conduction losses are limited since the ripple is lower due to higher switching frequency, whereas the switching losses are higher due to higher switching frequency and more hard-switching (smaller ripple). The green and red designs have larger inductances, thus the conduction losses are lower, whereas the switching losses are limited due to lower switching frequency and partial soft-switching.

Boost inductors also play a role in the total losses. It can be seen that for the orange (PQ60/52) and purple (PQ 50/50) designs, the losses are around $8.5W$ per inductor. The core P_{core} and winding P_{wind} losses are almost equal. In the case of the red (PQ65/54) and green(PQ50/50) designs, the losses are around $4-5W$ per inductor. These designs have a higher number of turns(red-29, green-21), therefore the winding losses P_{wind} are slightly more significant than the core losses P_{core}.

Finally, the EMI losses follow the same trend as the EMI volume, which is expected since the bigger the passive components, the higher the power losses as it is explained in Section 5.4.3. The bleeding losses and auxiliary losses are a fixed design which is derived from datasheets of the components used in the prototype.

Parallel transistors effect

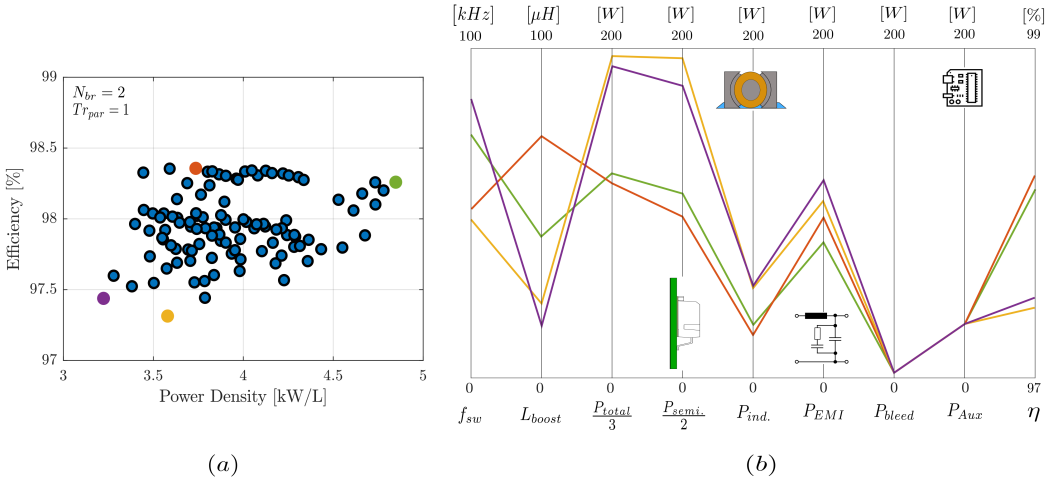


Figure 6.7: (a) Performance space for no-transistors in parallel per switch $Tr_{par} = 1$ and once-interleaved $N_{br} = 2$ Belgian Rectifier. (b) Power loss breakdown of four designs of the Belgian Rectifier with the following colors: Red - Highest efficiency design ($\eta = 98.36\%, \rho = 3.736kW/L$, $f_{sw} = 54kHz$, $L_{boost} = 70\mu H$), Green - Highest power density design ($\eta = 98.26\%, \rho = 4.848kW/L$, $f_{sw} = 72kHz$, $L_{boost} = 40\mu H$), Orange - Lowest efficiency design ($\eta = 97.31\%, \rho = 3.579kW/L$, $f_{sw} = 48kHz$, $L_{boost} = 20\mu H$), Purple - Lowest power density design ($\eta = 97.44\%, \rho = 3.223kW/L$, $f_{sw} = 84kHz$, $L_{boost} = 15\mu H$). Semiconductor used in rectifier stage is the SCTH100N120G2AG and in the boost circuits is the SCTH90N65G2V7.

Description	Parameter	Vector	Unit
Switching frequency	f_{sw}	72	kHz
Boost inductance	L_{boost}	$24, 26, 28, 30, 32, 34, 36, 38, 40$	μH
Interleaving branches	N_{br}	2	Branches
Parallel transistors	Tr_{par}	1	Transistors
Output voltage	V_o	$650, 750, 850$	V

Table 6.5: Narrow global design space parameters that take into consideration the voltage range of the Belgian Rectifier.

In Fig.6.8(a), the performance space of the Belgian Rectifier for no-transistors in parallel $Tr_{par} = 1$ and one-transistor in parallel $Tr_{par} = 2$ is shown, whereas in Fig.6.8(b), the relevant power loss and volume breakdown is depicted. Starting from the conduction losses, it is evident that by introducing one-transistor in parallel $Tr_{par} = 2$, the on-resistance $R_{DS,(on)}$ drops almost to half and so do the conduction losses. The switching losses, on the other hand, slightly increase because, even though the turn-on, turn-off voltages and currents are half, the number of transistors is double. The non-linear dependency of turn-on E_{on} and turn-off E_{off} switching energies on the switching current I_D results in the slight increase of the total switching losses. However, the disadvantage of parallel transistors $Tr_{par} = 2$ is obvious regarding the volume of the converter, especially regarding the semiconductors. For double the number of semiconductors, there is a need for larger cooling heatsink (cold plate) and aluminium block (wasted space), therefore the power density drops around $0.7kW/L$. The efficiency only increases with 0.25%, therefore no-transistors in parallel $Tr_{par} = 1$ is the design choice as mentioned above in this section.

Optimized design

The previous Pareto-front trajectories are generated considering the output voltage to be fixed at $V_o = 750V$. This approach can provide a good idea of what value of interleaving branches N_{br}, parallel transistors Tr_{par} and switching frequency f_{sw} leads to the optimal design. However, the Belgian Rectifier is designed to operate at an output voltage range $V_o = [650, 850]V$ because the battery's voltage is usually not constant and depends on the level of energy that it has stored. Therefore, a virtual prototyping routine with the design parameters shown in Table 6.5 is conducted. These design parameters are defined from the Pareto-trajectory "knee" for once-interleaving $N_{br} = 2$ and no-transistors in parallel $Tr_{par} = 1$. The switching frequency $f_{sw} = 72kHz$ is the optimal frequency due to the small filter it

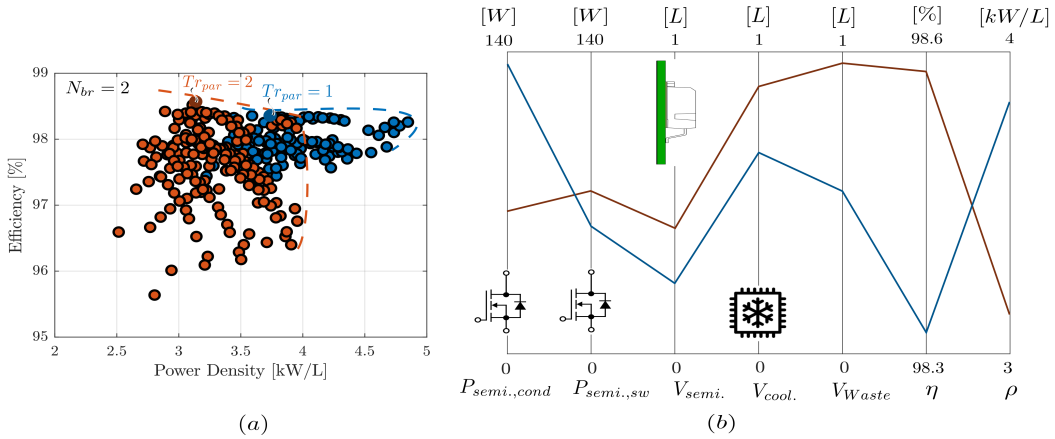


Figure 6.8: (a) Performance space for no-transistors in parallel per switch $Tr_{par} = 1$ versus one-transistor in parallel per switch $Tr_{par} = 2$ for once-interleaved $N_{br} = 2$ Belgian Rectifier. (b) Relevant power loss and volume breakdown of two designs of the Belgian Rectifier with $f_{sw} = 36kHz$, $L_{boost} = 50\mu H$ for no-transistors in parallel per switch $Tr_{par} = 1$ (Dark red color) and one-transistor in parallel per switch $Tr_{par} = 2$ (Dark blue color). Semiconductor used in rectifier stage is the SCTH100N120G2AG and in the boost circuits is the SCTH90N65G2V7.

requires as explained above. In order to define the optimal boost inductance L_{boost}, the voltage range has be included in the design procedure with the following proposed method.

The design of the boost inductor, the EMI filter and the semiconductor heatsink is conducted for the maximum $V_{o,max} = 850V$ and minimum output voltage $V_{o,min} = 650V$. In the case of the boost inductor, the largest inductor is selected since it has to be operational at the whole voltage range. Likewise, the attenuation required for the maximum and minimum voltages are compared and the EMI filter design for the highest required attenuation is selected. Finally, the largest scale factors for the semiconductor cooling area are chosen, so that the switches' junction temperature is always below the thermal limit.

As it is also explained previously (See Fig.6.5), the optimal semiconductor type choice is SCTH100N120G2AG for the rectifier stage and SCTH90N65G2V7 for the boost circuits. By applying the proposed virtual prototyping routine for the output voltage range and a narrow boost inductance design vector, the Pareto-trajectory depicted in Fig.6.9 is derived.

It can be observed that the boost inductance for which the Belgian Rectifier can achieve the highest power density is $L_{boost} = 32\mu H$. For this value of boost inductance, partial hard-switching occurs during the operation of the Belgian Rectifier. However, as explained in Chapter 3, the partial hard-switching occurs at low current, thus decreasing the total losses of the semiconductors. Moreover, the partial hard-switching introduces challenges regarding control stability due the dead-time that is described in Chapter 4. This problem can be tackled either by compensating for the voltage mismatch or by lowering the dead-time to a minimum since the SiC MoSFETs have very quick transition times. For higher inductances, a larger core is required and therefore, the power density of the converter drops significantly.

Since the converter is expected to operate at the whole voltage range, the final efficiency is the average of the efficiencies at $650V, 750V, 850V$, but the efficiency at the nominal voltage is weighted twice as follows:

$$\eta_{avg} = \frac{\eta_{650V} + 2 \cdot \eta_{750} + \eta_{850V}}{4} \tag{6.2}$$

Finally, the boost inductance $L_{boost} = 32\mu H$ and switching frequency $f_{sw} = 72kHz$ result in a small volume of EMI filter due to the lowest possible current ripple for inductor core PQ50/50. Therefore, this is chosen as the optimal design implementation and can be seen in Fig.6.9 as a yellow star.

From the optimal Pareto-front that is derived from the virtual prototyping routine, a certain design (EMI,inductor etc.) is picked as the optimal. As mentioned above, the topology of the EMI DM fil-

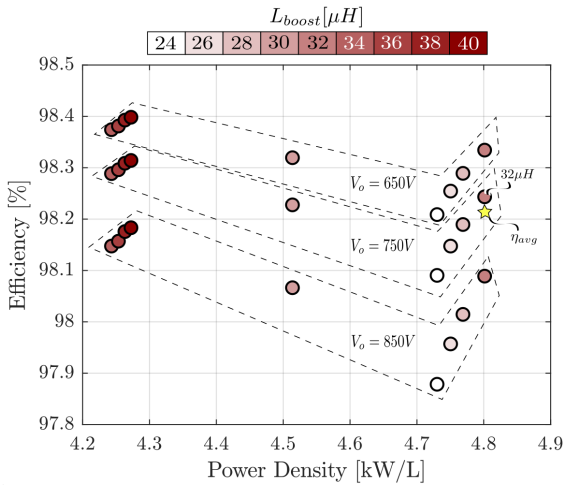


Figure 6.9: Pareto-front of efficiency versus power density when taking into consideration the voltage range $V_o = [650, 850]V$, setting switching frequency $f_{sw} = 72kHz$ and the boost inductance vector shown in Table 6.5. Semiconductor used in rectifier stage is the SCTH100N120G2AG and in the boost circuits is the SCTH90N65G2V7. The optimal design averaged efficiency is shown with the yellow star.

ter is a CLC filter and the the CM input filter has an $LCLC$ topology as can be seen in Fig.6.10.. The components of the input EMI filter are calculated automatically with the goal of optimizing the converter regarding its volume. Moreover, the selection of the semiconductors, inductor core, wire and inductance value are based on the optimal performance accomplished as it is shown in Pareto-front in Fig.6.9. The values of the components for the optimal design can be seen in Table 6.6.

6.5. Summary

In this chapter, the reader is introduced to the concept of the virtual prototyping routine that is implemented using Matlab/PLECS. Global design space, component design space, performance space and their interaction is described in detail.

Secondly, the global design space for the prototyping routine of the Belgian Rectifier is specified. The design requirements of the converter are defined and the and the global design parameters selected as variables with a large range such as the switching frequency and the boost inductance are determined. Furthermore, the effect of multiple interleaving branches N_{br} and parallel transistors Tr_{par} is discussed in terms of current ripple, power delivery capabilities, efficiency and power density. Thereafter, the component design space for the semiconductors, boost inductors and EMI filter is defined, the importance of the thermal limits consideration is pointed out and the modelling parameters that influence the calculation time of the routine are explained.

Thirdly, the resulting power density versus efficiency performance space from the previously defined global design space and component design space at the nominal voltage is demonstrated and discussed. An analysis of the loss distribution of the converter is done, as well as of the volume contribution of each part (Inductors, EMI, Semiconductors etc.) is discussed.

Finally, by including a vector of output voltages in order to evaluate the converter performance over a certain voltage range, by giving a narrow vector of boost inductance around the knee of the Pareto-trajectory and setting the optimal switching frequency $72kHz$, an optimized design is specified which results with efficiency $\eta_{avg} = 98.2\%$ and power density $\rho = 4.8kW/L$.

Parameter	Symbol	Value	Selection
Switching frequency	f_{sw}	$72kHz$	
Boost inductance	L_{boost}	$32\mu H$	
Interleaving branches	N_{br}	2	
Parallel transistors	Tr_{pr}	1	
Rectifier stage semiconductors	$S_{\bar{x}\bar{a}}, S_{\bar{x}\bar{b}}, S_{\bar{x}\bar{c}}$ $S_{\bar{a}\bar{y}}, S_{\bar{b}\bar{y}}, S_{\bar{c}\bar{y}}$		SCTH100N120G2AG
Top boost semiconductors	$S_{p\bar{x}}, S_{\bar{x}m}$		SCTH90N65G2V7
Bottom boost semiconductors	$S_{m\bar{y}}, S_{\bar{y}n}$		SCTH90N65G2V7
Boost inductors	Core Number of turns Strands Air gap		$PQ50/50$ 19 $1287 \cdot 0.071mm$ $4.5mm$
DM input filter Stage 1	$L_{DM,1}$ $C_{DM,1}, C_{D1}$ R_{D1}	$3.9\mu H$ $2.9\mu F$ 0.86Ω	
DM input filter Stage 2	$C_{DM,2}, C_{D2}$ R_{D2}	$2.9\mu F$ 0.86Ω	
CM input filter Stage 1	$L_{CM,1}$ $C_{CM,1}$	$1.7mH$ $20nF$	
CM input filter Stage 2	$L_{CM,2}$ $C_{CM,2}$	$1.7mH$ $20nF$	
DM output filter	$L_{DM,o}$ $C_{DM,o}$ $C_{D,o}$ $R_{D,o}$	$2.2\mu H$ $0.38\mu F$ $0.38\mu F$ 0.5Ω	
Output bulk capacitors	C_{pm}, C_{mn}	$2.5mH$	

Table 6.6: Belgian Rectifier optimized design parameters.

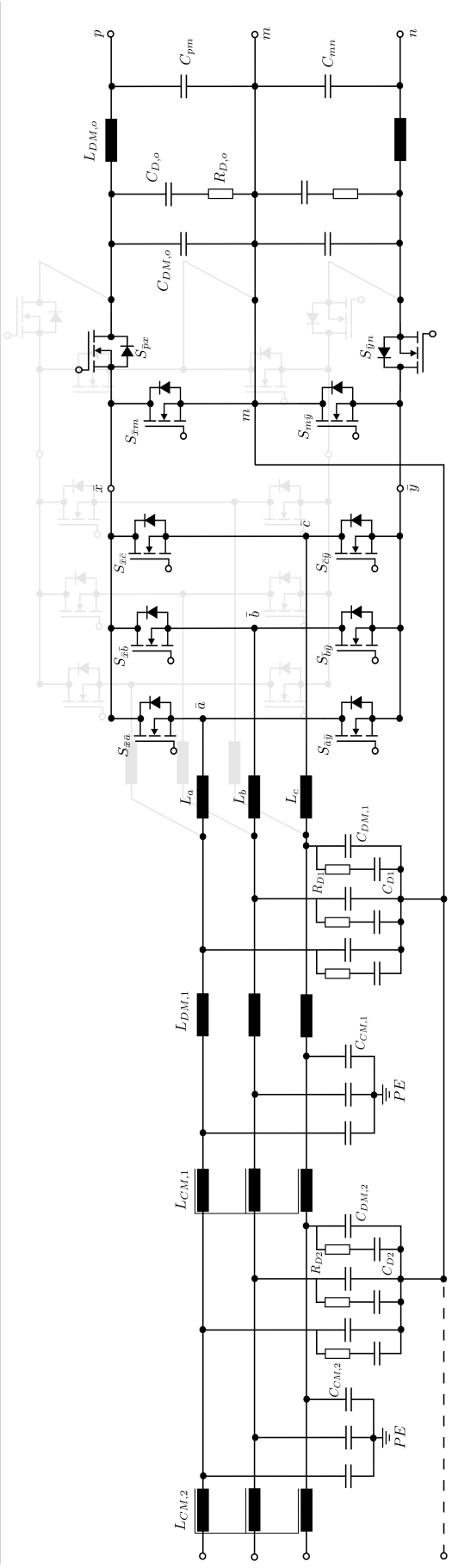


Figure 6.10: The optimal Belgian Rectifier topology including the EMI filter components.

7

Comparison

7.1. Introduction

In this chapter, a comparison of the Belgian Rectifier with the conventional Six-Switch Boost Rectifier is done. Starting from the semiconductor stresses and losses of the two topologies, an analysis and explanation of this major contributor of losses is presented. A reasoning of the semiconductor type selection for the two topologies is given. Secondly, the inductor requirements of each topology are discussed, focusing on the required stored energy that is an indicator of the inductor volume. Thirdly, the EMI required volume is shown in order to conduct a comparison between the Belgian and Six-switch. Finally, the Pareto-fronts of the two topologies are presented to understand what are their capabilities in terms of efficiency and power density.

The component design space used for the comparison is shown in Table 6.3 whereas the global design space is slightly changed (or limited) compared to the design space of Table 6.1 and Table 6.2. More specifically, the new design space can be seen in Table 7.1.

It can be observed that the output power of the converters is specified to half the nominal power. The reason for this change is that for 22kW output power, there are not enough feasible designs in the case of the six-switch rectifier, due to the thermal runway of the semiconductors (very high power losses). In order to expose the differences of the topologies, a higher number of feasible designs is required, therefore the output power is limited. The interleaving branches and the parallel-transistors per switch are fixed since their effect is explained thoroughly in Chapter 6.

7.2. Semiconductors

Semiconductor Stresses

As explained in Section 5.4.1, the major parameters that define what semiconductor type is required

Description	Parameter	Value
AC line input voltage	$v_{ac,line-line}$	$400V$
DC output nominal voltage	$v_{out,nom}$	$750V$
Full output power	P_{out}	$11kW$
Line frequency	f_L	$50Hz$
Switching frequency	f_{sw}	$[48, ..., 180]kHz$
Boost inductance	L_{boost}	$[10, ..., 110]\mu H$
Interleaving branches	N_{br}	2 Branches
Parallel transistors	Tr_{par}	1 Transistor

Table 7.1: Global design space for the comparison of the Belgian Rectifier and the conventional Six-Switch Rectifier.

Switch	Maximum voltage [V]	Selection
$S_{p\bar{a},max}$	$850V$	SCTH100N120G2AG
$S_{\bar{a}n,max}$	$850V$	SCTH100N120G2AG
$S_{p\bar{b},max}$	$850V$	SCTH100N120G2AG
$S_{\bar{b}n,max}$	$850V$	SCTH100N120G2AG
$S_{p\bar{c},max}$	$850V$	SCTH100N120G2AG
$S_{\bar{c}n,max}$	$850V$	SCTH100N120G2AG

Table 7.2: Maximum voltages of every switch in the Six-Switch Rectifier.

are the maximum voltage and maximum current of the transistor. Therefore, before selecting the semiconductor type, the voltage stresses of the six-switch rectifier switches are analyzed.

In Fig.2.2(a), the topology of the six-switch rectifier can be observed. It is obvious that the switch of the bridge leg can have two levels of voltage, namely $0V$ and u_{pn}. The nominal output voltage is $V_{out,nom} = u_{pn,nom} = 750V$, however, as it is assumed in Section 3.4, the output voltage is considered that it can be in the range $[660, 850]V$ due to transients and the output voltage range. Therefore, the rated voltage of the semiconductors of the six-switch has to be higher than their maximum voltages which can be seen in Table 7.2.

It is obvious that a 1200-V rated semiconductor has to be chosen and $SCTH100N120G2AG$ is the selected type as can be seen in Table 7.2. The semiconductor selection for the Belgian Rectifier switches is already discussed in Section 5.4.1.

At this point, it can be observed that the semiconductors of the Six-Switch Rectifier are actively switching the full DC-bus voltage. On the other hand, in the Belgian Rectifier, the switches that are actively switching for the whole line period are 650-V rated $SCTH90N65G2V7$, thus the switching losses are significantly lower. Moreover, in the rectifier stage one out of three bridge legs is actively switches which also contributes to the overall reduction of switching losses. However, there are also a few switching transitions where the full DC bus voltage is switched in the rectifier stage bridge legs. But, overall the Belgian Rectifier compared to the Six-Switch Rectifier has a significant advantage regarding semiconductor losses.

Semiconductor losses

In Fig. 7.1, the conduction, switching and total semiconductor losses of the Belgian Rectifier and the Six-Switch Rectifier can be observed. The color range indicates the level of losses starting from low (blue) to high (yellow), whereas the white color indicates that no design is achieved for the specific set of switching frequency f_{sw} and boost inductance L_{boost}. Starting from the conduction losses in Fig.7.1(a), it is observed that they are higher for lower values of switching frequency and boost inductance. This can be attributed to high current ripple that increases the RMS current of the switches. For high values of switching frequency and boost inductance, the current ripple is decreased and therefore, the conduction losses are decreased, as well. The conduction losses of the Belgian Rectifier reach higher levels than the ones of the Six-Switch Rectifier, but this is mainly attributed to the fact that designs with lower switching frequency and boost inductance are feasible for the Belgian.

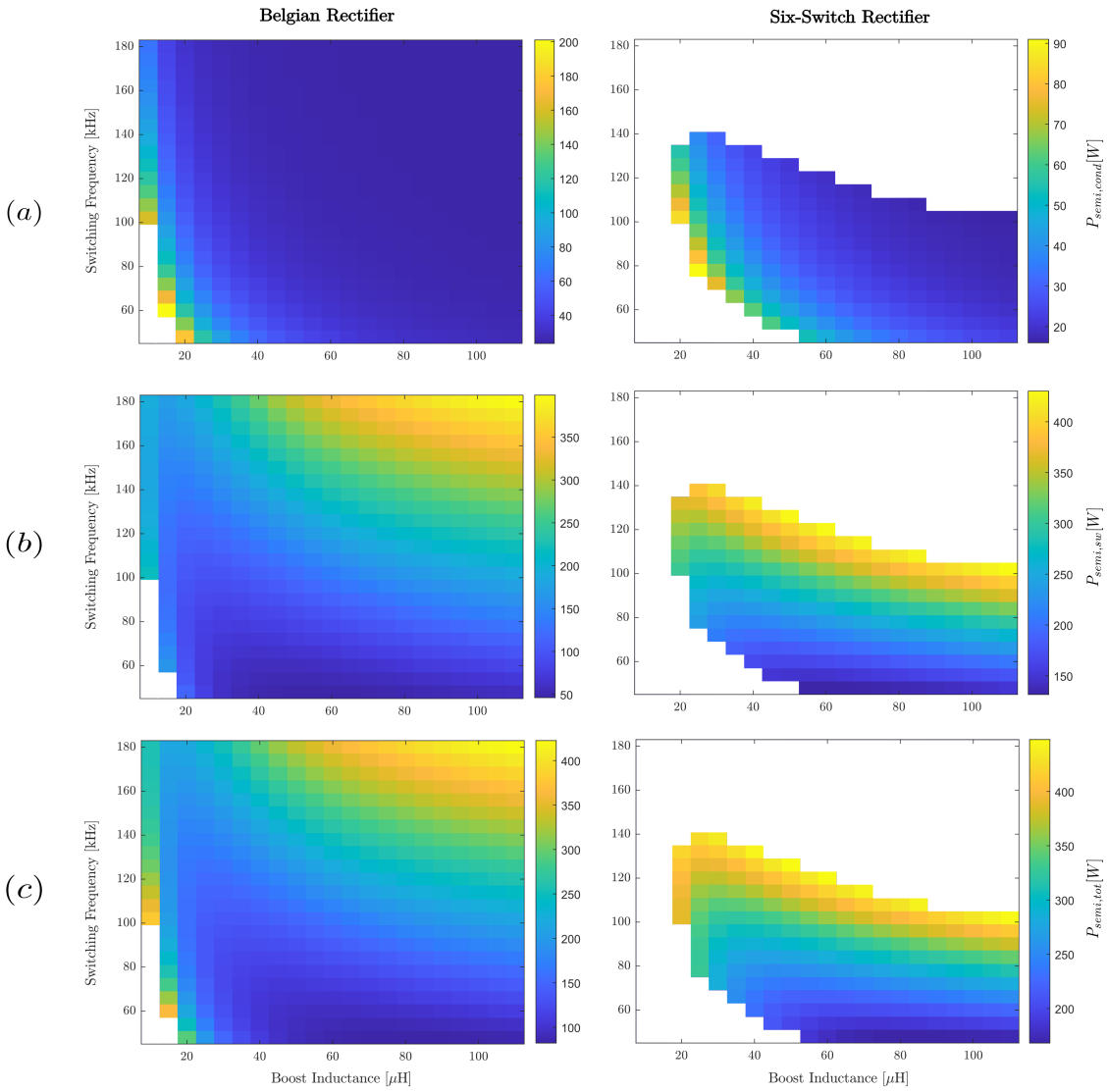


Figure 7.1: (a) Conduction losses, (b) switching losses and (c) total semiconductor losses for the Belgian Rectifier and Six-Switch Rectifier.

Regarding the switching losses, it is obvious that the increase of the switching frequency increases the switching losses. In the case of the Six-Switch Rectifier, the switching losses reach a higher level than the ones of the Belgian Rectifier for the same switching frequency and boost inductance. After some point, the thermal limit of the semiconductors is reached for the Six-Switch, therefore no more designs are feasible.

Finally, in Fig.7.1(c), the total semiconductor losses for the two topologies are shown. It can be concluded that the Belgian Rectifier has advantages in many aspects regarding the semiconductors. Firstly, for the same switching frequency and boost inductance, the Belgian Rectifier demonstrates lower semiconductor losses. Secondly, the Belgian Rectifier can be designed for a wider range of the design space because the thermal limits of the semiconductors are met for higher values of switching frequency and boost inductance. This means that the Belgian Rectifier can operate for higher power levels within the thermal limits. Last, the total semiconductor losses plots verify the region where Pareto-optimal designs are found. More specifically, it can be observed that for boost inductance $L_{boost} = 32\mu H$ and switching frequency $f_{sw} = 72kHz$, the total semiconductor losses have a low value (dark blue), as it is shown in Fig.7.1(c).

7.3. Inductors

In Fig.7.2, the peak energy of the boost inductors for both topologies is shown. It can be observed that for the same switching frequency f_{sw} and boost inductance L_{boost}, the Six-Switch Rectifier has higher peak energy per inductor as expected. This is the result of higher levels of voltage over the inductor that produce higher current ripple. Therefore, the Six-Switch Rectifier needs larger inductors that are able to store the required energy.

It is worth noting that after a certain value of stored peak energy, the design of a boost inductor is not feasible for the given component design space. The failure of designs in the bottom right corner of Fig.7.2(Six-Switch Rectifier) is attributed to the unfeasible boost inductor design which is a result of the limited set of core sizes in the component design space. The rest of the unfeasible designs(top white space) is attributed to the thermal limit of the semiconductors.

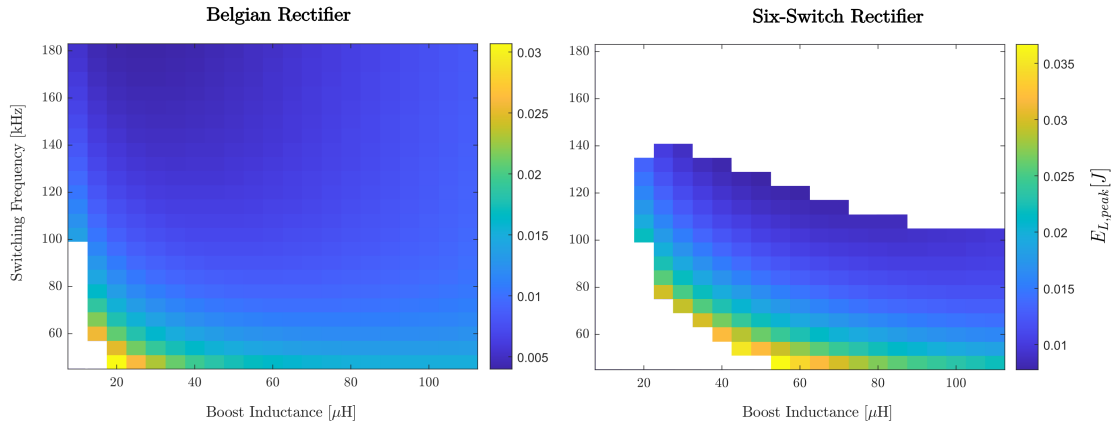


Figure 7.2: Peak stored energy of the boost inductors for the Belgian Rectifier and Six-Switch Rectifier.

7.4. EMI filter

In Fig.7.3, the volume of the EMI filter for the Belgian Rectifier and the Six-Switch Rectifier is compared. It can be observed that the Belgian Rectifier achieves slightly smaller EMI volume than the Six-Switch Rectifier for the same switching frequency and boost inductance. It is evident that the smaller EMI volume is achieved for switching frequency $72kHz$ due to reasons explained in Chapter 6. It can also be concluded that the Belgian Rectifier has lower filtering requirements which is reflected in the component size and the volume of the EMI filter.

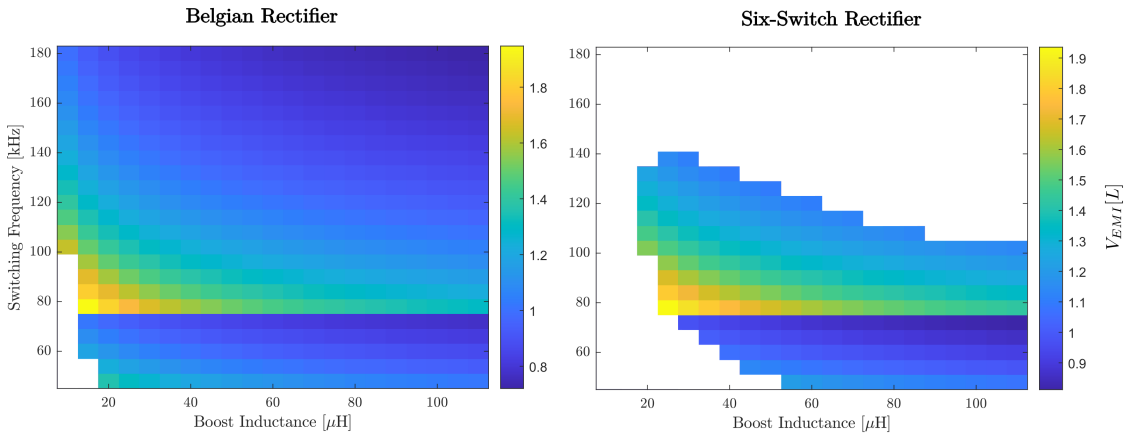


Figure 7.3: EMI volume for the Belgian Rectifier and Six-Switch Rectifier.

7.5. Pareto-front

The performance space of the two topologies for the design space of Table 7.1 and Tables 6.1, 6.2 are shown in Fig.7.4(a) and Fig.7.4(b), respectively.

Starting from Fig.7.4(a), it can be observed that the efficiency of the Belgian Rectifier is higher than that of the Six-Switch Rectifier. In the former topology, the boost circuits are actively switching only half the DC bus voltage and in the rectifier stage, only one out of three bridge legs is actively switching half or full DC bus voltage. In the latter topology, the three bridge-legs are actively switching the full DC-bus voltage, therefore the switching losses are increased as it is also observed in Fig.7.1(b). Moreover, the semiconductor conduction losses and the inductor core losses are again higher in the case of the Six-Switch Rectifier due to the higher current ripple. All these factors contribute to the better performance of the Belgian rectifier regarding efficiency.

However, it can be observed that the Six-Switch Rectifier can achieve slightly higher power density for a nominal power of 11kW. This is attributed to the fact that the semiconductors of the Belgian Rectifier take more space due to their higher number. This is related to the mechanical design of the converters, where each semiconductor is linked to a ”piece” of aluminium block for the thermal connection to the coldplate. If the aluminium block can omitted with a different mechanical design, the Belgian Rectifier could have higher power density. Another significant contribution to this result are the boost inductors that in the case of the Belgian Rectifier are overdimensioned for 11kW. If a wider range of inductor core was to be used, the power density of the Belgian Rectifier would further increase because the peak energy of the inductors is significantly lower than in the case of the Six-Switch Rectifier.

Nevertheless, when modelling for the full power 22kW as can be seen in Fig.7.4(b), it can be seen that the Belgian Rectifier can achieve higher power density. This means that in the case of 11kW, the Belgian Rectifier still has significant ”thermal space”, meaning that the power can be increased significantly without meeting the thermal limits. On the other hand, only few designs are feasible in the case of the Six-Switch Rectifier because the thermal limits are surpassed for most points of the design space.

Finally, the Belgian Rectifier can achieve higher efficiency and power density than the Six-Switch Rectifier for a nominal power $P_o = 22kW$.

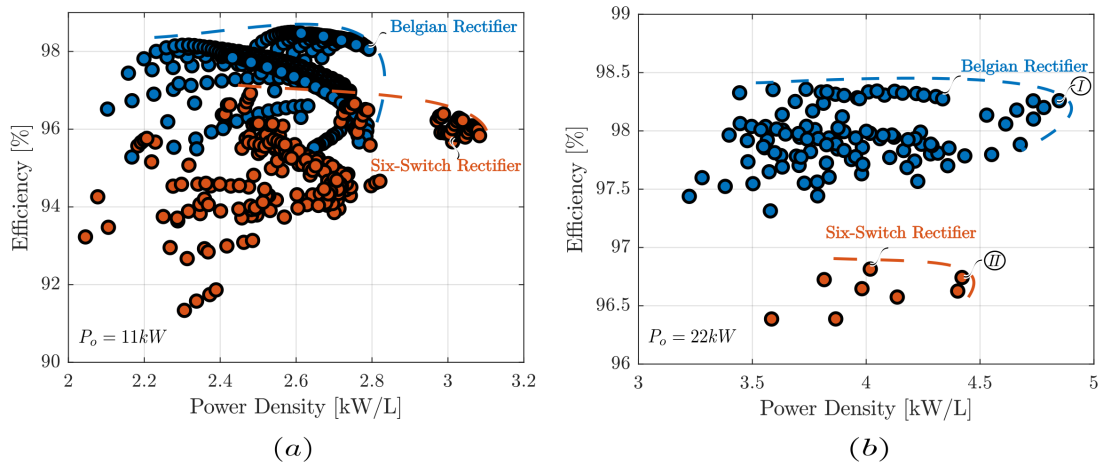


Figure 7.4: Pareto-front of efficiency versus power density (performance space) of the Belgian Rectifier(blue) and Six-Switch Rectifier(red) for output power (a) $P_o = 11kW$ and (b) $P_o = 22kW$.

In Fig.7.5, the power loss breakdown of the optimal designs of the Belgian and the Six-Switch rectifiers are depicted. It can be easily observed that the semiconductor losses and the inductor losses of the Six-Switch Rectifier are significantly higher than the respective losses of the Belgian Rectifier. The semiconductor losses difference is already explained in previous subsections, however, the inductor losses are mainly attributed to the high current ripple of the Six-Switch Rectifier. The high ripple results

in significantly higher core losses.

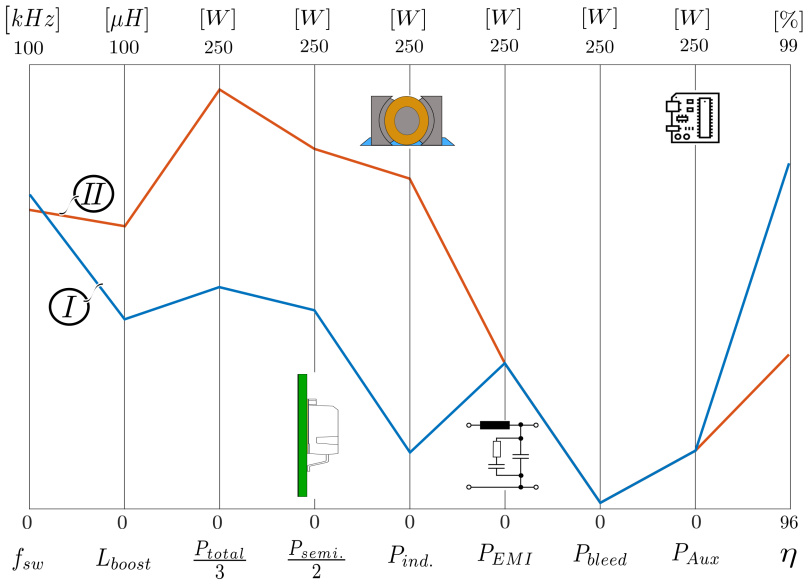


Figure 7.5: Power losses breakdown of the optimal designs of the Belgian Rectifier (I) and the Six-Switch Rectifier (II) which can be found in the performance space of Fig.7.4(b)

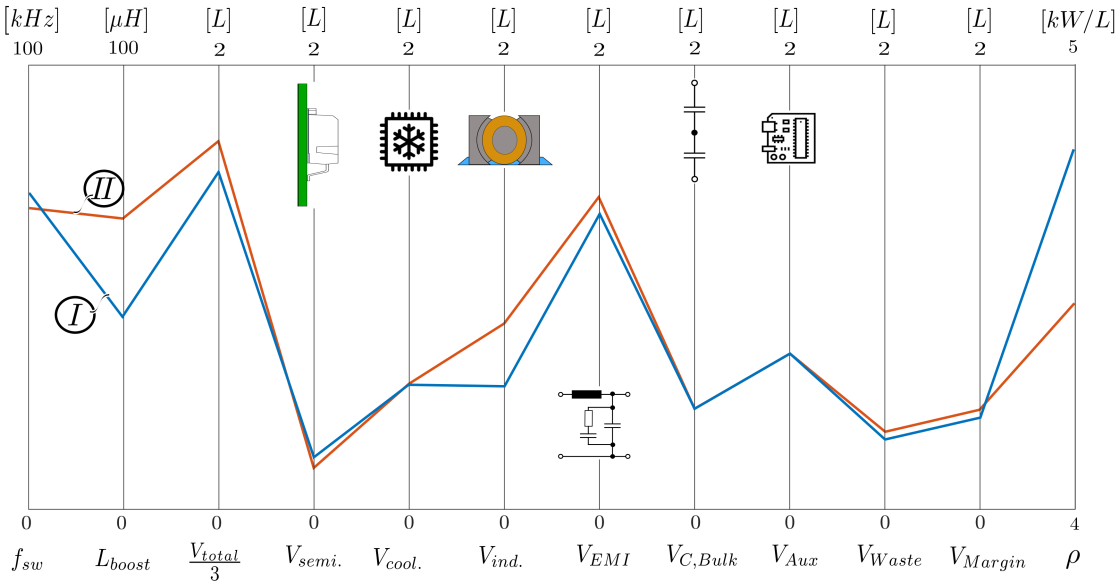


Figure 7.6: Volume breakdown of the optimal designs of the Belgian Rectifier (I) and the Six-Switch Rectifier (II) which can be found in the performance space of Fig.7.4(b)

In Fig.7.6, the volume breakdown of the two designs is presented. The most significant difference is that the Belgian Rectifier has smaller boost inductors. If the inductor core range of the component design space would be increased, then the volume of the inductors of the Belgian Rectifier could be further decreased due to the low peak stored energy. Moreover, the aluminium block(wasted volume)

of the Belgian Rectifier is smaller than the one of the Six-Switch rectifier even though it consists of a higher number of switches. This is attributed to the fact that the switches of the Belgian Rectifier need less cooling, therefore the area around them is designed to be smaller.

7.6. Summary

In this chapter, a comparative evaluation of the Belgian Rectifier is conducted. The reference topology is the Six-Switch Rectifier which is widely used in the industry due to its simplicity and low cost. The comparison is done on the performance of the semiconductors, boost inductors and EMI filter.

It is concluded that the Belgian Rectifier has lower semiconductor losses, semiconductor stresses, requires lower peak inductor energy, thus smaller inductor volume, and lower filter requirements. However, due to the higher number of switches, the effective volume of the semiconductors is slightly higher, but the thermal limits are reached for significantly higher power than in the Six-Switch Rectifier.

Due to the aforementioned factors, the Belgian Rectifier achieves higher levels of efficiency and power density for nominal power $P_o = 22kW$ and therefore, constitutes a better option compared to the Six-Switch Rectifier.

8

Conclusions

This project focuses on a recently proposed novel three-phase boost-type PFC rectifier, called the Belgian Rectifier. This rectifier facilitates the conversion of AC-to-DC voltage and in the same time provides power factor correction, meaning that the current is modulated to have the same phase with the voltage and minimal total harmonic distortion (THD). The use case for which the Belgian Rectifier is designed is EV charging systems where high efficiency and power density are required. The research objectives of this thesis start from the mathematical description of the operational principle of the topology under investigation, the derivation of a proper modulation scheme that provides the smallest possible stresses on the components and decreases the power losses. Moreover, the modelling and the design of the Belgian Rectifier with $P_o = 22kW$ and $V_o = 750V$ is required and by means of a virtual prototyping routine, the investigation of the capabilities of the converter regarding efficiency and power density is conducted for a wide design space.

Thereafter, literature review is provided regarding the conventional six-switch boost-type PFC rectifier in order to examine its advantages and disadvantages. It is noted that the 6-switch boost rectifier has several disadvantages such as the active switching of the full DC-bus voltage from the semiconductors and the large required magnetic energy of the inductors. Therefore, the power density of the 6-switch PFC rectifier decreases significantly. Moreover, the concept of zero-voltage switching is demonstrated by showing a soft-switching transition of a bridge leg.

Next, the focus drops on the Belgian Rectifier which is the main topic of this thesis. Starting from the structure of the converter, the several parts are described in terms of functionality and the operational principle is explained in detail. In this context, the conduction states are presented in order to demonstrate the three-level voltage feature of this rectifier and illustrate the advantages it enjoys in terms of low current ripple and component stresses. Furthermore, the average model of the rectifier is built for two different modulation schemes using triangular carriers. The duty cycles of the switches are derived for both modulations. The selected modulation scheme advantageously shows even distribution of component stresses and power losses, as well as low switching losses due to soft switching in a significant portion of the line cycle. Finally, zero-voltage switching and its impact on the power losses of the Belgian Rectifier are discussed, together with the semiconductor stresses in terms of maximum voltage and current.

It is concluded that high performance can be achieved also when hard switching occurs, because the SiC MOSFETs allow it in terms of switching losses and thermal limits. Moreover, by allowing some hard switching, lower current ripple is achieved that enables less conduction losses and a smaller EMI filter due to lower filtering requirements.

To continue with, the closed loop control scheme that is proposed for this converter is presented in detail. Moreover, the effect of dead-time on the stability of the system is discussed and a possible solution with a feed-forward dead-time compensation is proposed.

The modelling approach of the converter is thoroughly explained starting from the definition of the specifications to the calculation of the efficiency and power density. The benefits of the Fourier analysis for the formation of a switching model, that serves for the generation of current and voltage waveforms, are demonstrated. Furthermore, the multi-physics modelling of the semiconductors, inductors and EMI filter is discussed with an emphasis to the optimization regarding the power losses and volume. In that context, the electrical equivalents of the thermal models of the semiconductors and inductors are presented to indicate the thermal limits that play a crucial role for the design of a converter. Finally, the separate models of the semiconductors, inductors and EMI provide the total power losses and volume of the components, therefore the overall efficiency and power density of the converter is calculated.

Using the aforementioned multi-physics models, a global design space and component design space are defined in order to map the performance space of a $22kW$ Belgian Rectifier with $400V$ input AC line-to-line voltage and $750V$ output DC voltage. The global design space consists of a large range of switching frequency and boost inductance values, as well as a number of interleaving branches and parallel transistors. These parameters affect greatly the performance of the Belgian Rectifier and their effect is discussed in detail. Moreover, a components design space is chosen for the inductor design which is limited to a number of core sizes with a satisfying range. The importance of the inductor core regarding the total power density is emphasized. The realization of the virtual prototyping routine using the aforementioned global and component design spaces outputs the performance space (efficiency versus power density) of the converter in the form of a Pareto-front. The optimal design is determined to have two interleaving branches $N_{br} = 2$, no-transistors in parallel $Tr_{par} = 1$, switching frequency $f_{sw} = 72kHz$ and boost inductance $L_{boost} = 32\mu H$. The Belgian Rectifier for these parameter achieves an efficiency of $\eta = 98.2\%$ and power density $\rho = 4.8kW/L$.

The Belgian Rectifier is compared to the Six-Switch Rectifier to obtain a performance reference. The comparison is conducted in regard to the semiconductor stresses, losses, inductor peak stored energy and EMI filter volume. The Belgian Rectifier has advantages in most of the aspects except the volume required for the semiconductors. Therefore, it outperforms the Six-Switch Rectifier in terms of efficiency and power density for nominal power $P_o = 22kW$ as it is demonstrated from their performance spaces.

Finally, the operational principle of the Belgian Rectifier is described and the derivation of a proper modulation scheme is completed. The converter's capabilities regarding efficiency and power density are investigated for the use case of an off-board charger and it is compared to the Six-Switch Rectifier to make a final evaluation. Therefore, the research objectives defined in Chapter 1 are fulfilled completely.

8.1. Future work

During this project, the essential research objectives were completed. However, some of the topics and the methodology could be further improved. Therefore, several steps that can be taken in the future are listed in this section.

Firstly, the calculation of the switching and conduction losses is done using information from the datasheets. However, the semiconductor losses model can be elaborated to an analytical calculation using the parasitic capacitances and inductances of the semiconductors. In the current models, the parasitic capacitances are considered to be included in the E_{on}, E_{off} energies and the effect of the external capacitances is modelled as independent. However, these quantities are interconnected and their dependecies should be taken into account.

Secondly, as it is explained in Chapter 4, the effect of the dead-time is significant on the total harmonic distortion (THD) of the phase currents as it introduces a mismatch of voltage over the switches. Compensating for the duty cycles can reduce the THD and therefore improve the current quality and power factor of the converter. It is recommended that further elaboration is done on the development of dead-time compensation which takes into consideration hard-switching as well as partial soft-switching by linearization.

Thirdly, the volume model of the converter consists of an aluminium block that serves for the thermal connection of the semiconductors to the coldplate. It is suggested that a new mechanical design of the converter to be elaborated with the direct contact of Metal-Core PCB to the coldplate. That way, the wasted volume can be decreased and the Belgian Rectifier can achieve higher power density.

Forth, the performance space of the multi-objective optimization can be extended to including the cost of the converter as well. The cost is an important feature for the industry and can make a certain topology appealing or not.

Finally, a prototype of the Belgian Rectifier should be designed in practice in order to be tested in the lab for verification of the Pareto-fronts. For this purpose, a new design of the Belgian Rectifier has to be done including mechanical elements and electronics in order to achieve the optimal performance that is modelled theoretically.

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