

Reliability Optimization of Gold-Tin Eutectic Die Attach Layer in HEMT Package

Zhang, Hao; Fan, Jiajie; Zhang, Jing; Qian, Cheng; Fan, Xuejun; Sun, Fenglian; Zhang, G.Q.

DOI

[10.1109/SSLCHINA.2016.7804349](https://doi.org/10.1109/SSLCHINA.2016.7804349)

Publication date

2017

Document Version

Final published version

Published in

2016 13th China International Forum on Solid State Lighting (SSLChina)

Citation (APA)

Zhang, H., Fan, J., Zhang, J., Qian, C., Fan, X., Sun, F., & Zhang, G. Q. (2017). Reliability Optimization of Gold-Tin Eutectic Die Attach Layer in HEMT Package. In *2016 13th China International Forum on Solid State Lighting (SSLChina)* (pp. 52-56). Article 16579876 IEEE.
<https://doi.org/10.1109/SSLCHINA.2016.7804349>

Important note

To cite this publication, please use the final published version (if applicable).
Please check the document version above.

Copyright

Other than for strictly personal use, it is not permitted to download, forward or distribute the text or part of it, without the consent of the author(s) and/or copyright holder(s), unless the work is under an open content license such as Creative Commons.

Takedown policy

Please contact us and provide details if you believe this document breaches copyrights.
We will remove access to the work immediately and investigate your claim.

Reliability Optimization of Gold-Tin Eutectic Die Attach Layer in HEMT Package

Hao Zhang^{1,2,3}, Jiajie Fan^{1,3,4}, Jing Zhang^{3,7}, Cheng Qian^{3,5}, Xuejun Fan^{3,6}, Fenglian Sun², Guoqi Zhang^{3,5,7*}

¹Beijing Research Center, Delft University of Technology, Beijing, China

²Harbin University of Science and Technology, Harbin, China

³Changzhou Institute of Technology Research for Solid State Lighting, Changzhou, China

⁴College of Mechanical and Electrical Engineering, Hohai University, Changzhou, China

⁵Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China

⁶Department of Mechanical Engineering, Lamar University, Beaumont, USA

⁷EEMCS Faculty, Delft University of Technology, Delft, the Netherlands

*Corresponding: G.Q.Zhang@tudelft.nl

Abstract

This paper compared the fatigue damage accumulation of the gold-tin eutectic die attach layer in different high electron mobility transistor (HEMT) packages with various types of die attach layers and substrates under thermal cyclic loading. The fatigue damage per cycle used in this study was characterized by the accumulation of plastic work, which was derived by the finite element analysis (FEA). The effects of die attach layer's standoff height and thickness of substrate on fatigue damage accumulation were discussed. The results show that increasing the standoff height of the die attach layer is an effective way to prevent the early crack initiation in gold-tin die attach layer especially for a gallium nitride (GaN) die. It is also indicated that for a GaN die, a thicker die attach layer and a thinner substrate are preferable in order to retain a comparable lifetime with silicon (Si) die and Cu substrate system.

1. Introduction

Wide band gap semiconductors, typically based on silicon carbide (SiC) and gallium nitride (GaN), have attracted much attention in power devices, due to their advantages of higher thermal conductivity, higher breakdown field strength, higher operating temperature above 200°C and lower power loss compared to the commonly adopted silicon (Si) based devices [1, 2]. Among which, the GaN based semiconductors are mainly used in the high electron mobility transistor (HEMT), which combines the advantages of high speed and low-loss switching performance and makes them very attractive for switching power supplies and microwave power devices [3].

The die attach layer plays an important role in HEMT devices, including the mechanical adhesion, thermal stress compensation, as well as heat dissipation. The gold-tin (Au80Sn20) eutectic solder alloy has been widely adopted as die attach materials in many power devices, especially for microwave devices and laser diodes [4]. Advantages have been proved for gold-tin eutectic solder alloy, such as high melting temperature of 278 °C, preferable high temperature reliability, high electrical (1.64×10⁷/(Ω·m)) [5] and high thermal conductivity (57 W/(m·K)) [6], high stiffness, as well as possibility of flux-free soldering.

Considering the high operation temperature and the large mismatch of coefficients of thermal expansion (CTE) between die and substrate, large thermal stress level and deformation may be expected in power semiconductor devices. These will cause all kinds of delamination and consequently poor thermal

interface between different materials, in which the fatigue damage of die attach layer will finally result in the failure of devices. However, currently, there are few publications regarding design rules of this type of package in terms of geometry and substrate materials preference. Therefore, in order to optimize the package design, it is necessary to investigate the geometric effects of the whole package structure on the reliability of die attach layer.

By using the finite element analysis (FEA) method, this paper compared the fatigue damage accumulation in gold-tin eutectic die attach layer in different HEMT packages under temperature cycling. Effects of die materials, standoff height (SOH) of die attach layer and thickness of substrate on the accumulation of fatigue damage under thermal cyclic loading were investigated.

2. Finite element analysis method

The Anand constitutive model is a rate-dependent plasticity model for simulations such as metal forming [7, 8]. It is widely applicable for analyzing strain and temperature effects including solder joints and their high temperature creep [9]. Two main features are defined in the Anand constitutive model. Firstly, the explicit yield surface and loading/unloading criterion are not required for this model. The plastic strain is supposed to generate at all non-zero stress values, even if the plastic flow is extremely small at low stresses. Secondly, a single internal scalar "s" termed as deformation resistance is used to describe the averaged isotropic resistance to inelastic flow of the material [10, 11].

The deformation resistance, s , is an averaged isotropic resistance to macroscopic plastic flow, which is resulted from strengthening mechanisms such as dislocation density, solid solution hardening, and grain size effects. Therefore, the deformation resistance, s , can be regarded proportional to the equivalent stress σ , as shown in eq. (1) [7]:

$$\sigma = c \cdot s; c < 1 \quad (1)$$

where c is defined as eq. (2) [7]:

$$c = \frac{1}{\xi} \sin h^{-1} \left[\left(\frac{\dot{\epsilon}_p}{A} \exp \left(\frac{Q}{RT} \right) \right)^m \right] \quad (2)$$

Where $\dot{\epsilon}_p$ is the plastic strain rate, A is the pre-exponential factor, Q the activation energy, m is the strain rate sensitivity, ξ is the stress multiplier, R is the universal gas constant, and T is the absolute temperature.

The plastic strain rate $\dot{\epsilon}_p$ can be described as eq. (3) [7]:

$$\dot{\epsilon}_p = A \exp\left(-\frac{Q}{R\theta}\right) \left[\sinh\left(\xi \frac{\sigma}{s}\right)\right]^{1/m} \quad (3)$$

The evolution equation is given by eq. (4) [7] and eq. (5)[7]:

$$\dot{s} = \left\{h_0 \left|1 - \frac{s}{s^*}\right|^a \cdot \text{sign}\left(1 - \frac{s}{s^*}\right)\right\} \cdot \dot{\epsilon}_p; a > 1 \quad (4)$$

with

$$s^* = \hat{s} \left[\frac{\dot{\epsilon}_p}{A} \exp\left(\frac{Q}{RT}\right)\right]^n \quad (5)$$

where h_0 is the hardening/softening constant, a is the strain rate sensitivity of hardening/softening, s^* is the saturation value of s , \hat{s} is the coefficient for saturation value of deformation resistance, and n is the strain rate sensitivity.

The parameters in Anand model are related to material properties, such as A , Q , ξ , m , h_0 , \hat{s} , n , a , and s_0 , s_0 is the initial value of the deformation resistance. The parameters of gold-tin eutectic solder alloy in Anand model are listed in Table 2.1[12].

Table 2.1 Anand model constant for gold-tin eutectic solder alloy[12]

Anand constant	Units	Value	Description
s_0	MPa	69.99	Initial value of deformation resistance
Q/R	1/K	7578.7	Q = Activation energy R = Universal gas constant
A	S ⁻¹	93.07	Pre-exponential factor
ξ	-	11	Stress multiplier
m	-	306280	Strain rate sensitivity of stress
h_0	MPa	0.573	Hardening / softening constant
\hat{s}	MPa	466.13	Coefficient for deformation resistance saturation value
n	-	0.046	Strain rate sensitivity of saturation (deformation resistance) value
a	-	1.402	Strain rate sensitivity of hardening / softening

In order to simplify the solution of model, some assumptions have been applied to the model as follows:

- The 3D model is considered as a symmetrical model and a half model was simulated to save computational time without affecting the accuracy of the solution.

- The material parameters of substrate and die were considered as constant during modeling;

- The formation of intermetallic compounds and the microstructure evolution of Au-Sn eutectic solder alloy were neglected in the modeling, since they have limited effects on joint properties in low cooling rate cycles [13];

- The effects of the metallization layers of the die and substrate were not taken into account in order to simplify the simulation process.

3. Package structure and materials

According to an actual HEMT device, a simplified model with a symmetric structure was used for simulation, as seen in Figure 3.1 (a) and (b). The simplified 3D model consists of three layers: copper substrate, die attach layer and semiconductor die with Si or GaN material. The material properties adopted in this study are shown in Table 3.1[14-

16]. The Young's modulus of gold-tin eutectic solder alloy is considered to be linear with temperature ramp up.

According to JEDEC Standard JESD22-A104D, the temperature profile from 0 to 125 °C is used as boundary conditions during modeling. The rate for temperature ramp up and down is set as 5 °C /min, and the dwell times at maximum and minimum temperature are 10 min and 5 min, respectively. Furthermore, it is assumed that the plastic work accumulation became stabilized after the first three cycles[17]. Therefore, four thermal cycles are performed in this study for modeling, and the temperature profile is designed in Figure 3.2.

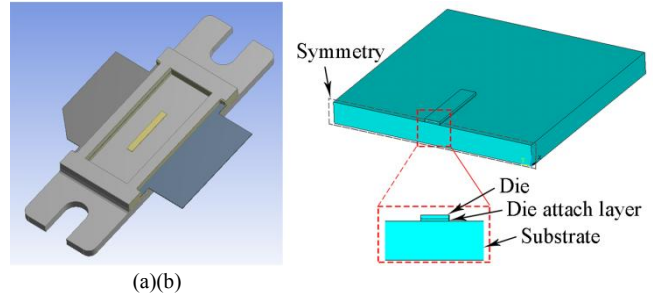


Fig. 3.1 (a) Schematic diagram of product, (b) Simplified structure

Table 3.1 Material properties[14-16]

Material	Young's modulus (GPa)	Poisson ratio	CTE (10 ⁻⁶ ·K ⁻¹)
Si	120	0.28	2.8
GaN	295	0.25	3.2
Au80Sn20	0, 79.45	0.3	18
	25 °C, 70.95		
	50 °C, 62.45		
	100 °C, 45.45		
125 °C, 36.95			
Cu	124	0.34	16.9

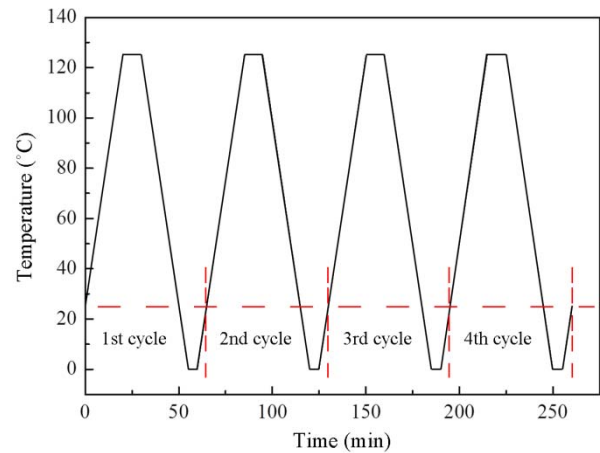


Fig. 3.2 Temperature cycle profiles used in the simulation

4. Results and discussion

4.1 Effects of die materials on plastic work density evolution

The plastic work density distribution in the die attach layers of packages with different die materials after the 4th thermal cycle were simulated with FEA, as shown in Figure 4.1 (a) and (b). It shows that the maximum plastic work density is located in the outer lower corner for both cases, which is the most critical area to be considered.

In this paper, the elements with maximum plastic work energy are considered as critical elements. The plastic work density obtained in this study was the average value of these elements. The evolution of plastic work density for Si and GaN based model was plotted in Figure 4.2. The plastic work densities in die attach layer increase linearly with the increase of thermal cycle number for both Si and GaN based models.

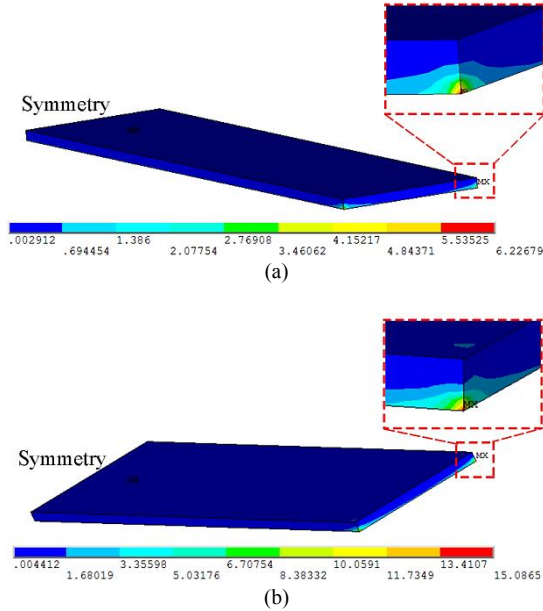


Figure 4.1 Distributions of plastic work density in die attach layer after 4th cycle, (a) Si based model, (b) GaN based model

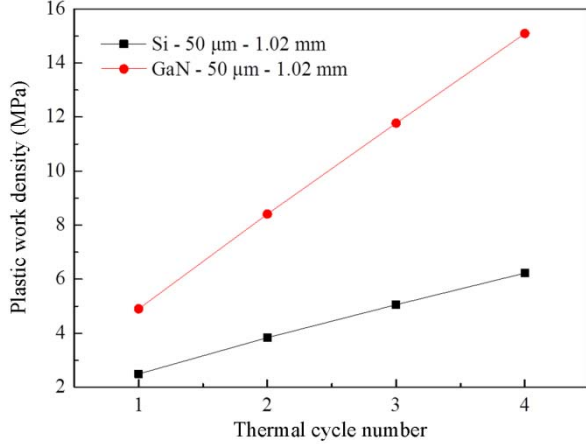


Fig 4.2 Evolution of plastic work density in die attach layer

However, a larger plastic work density was obtained in GaN based model after the fourth cycle when compared with Si based model. It is suggested that the larger deformation will be induced at the corner of die attach layer due to the much larger difference of Young's modulus between GaN die and gold-tin layer. Therefore, higher plastic work density generated in GaN based model, which will lead to a shorter fatigue life time when compared with Si based model.

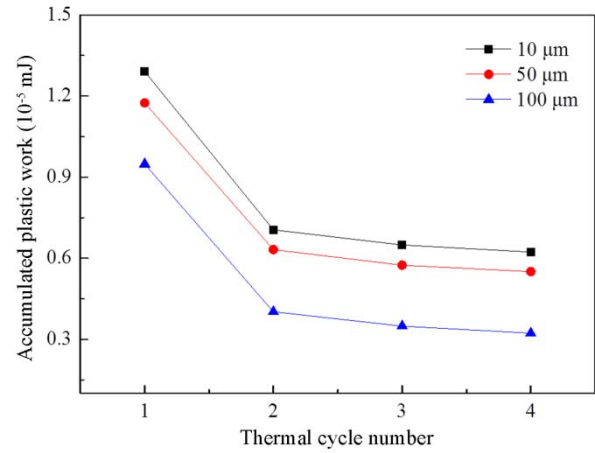
4.2 Effects of SOH on the accumulation of plastic work

It is reported that the accumulated plastic work of critical elements over load step can be termed as ametric for predicting the fatigue life time of solder alloys[10]. The accumulated plastic work ΔW can be described as eq. (6):

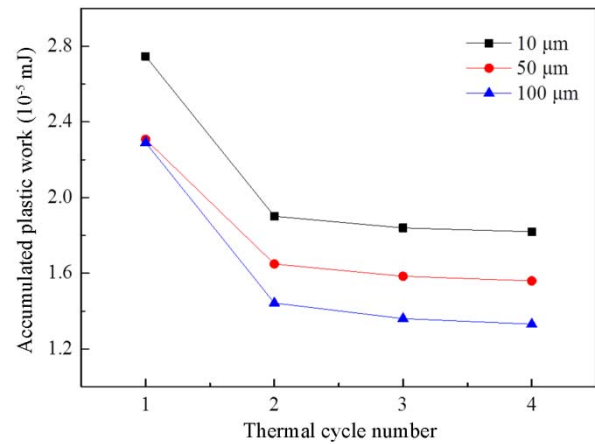
$$\Delta W = W_i - W_{i-1}, i = 1, 2, 3, 4(6)$$

where W_{i-1} is the plastic work of the last cycle. In this study, the effects of die attach layer's SOH on the accumulation of plastic work ΔW were analyzed as shown in Figure 4.3 (a) and (b). Similar trends have been observed for both Si and GaN based models. Firstly, the accumulation of plastic work tends to be stable after the second thermal cycle in all models. The accumulated plastic work after the third and fourth cycle is quite similar. Secondly, the amount of accumulated plastic work increases with decreasing SOH after each cycle in all models. Moreover, the accumulation of plastic work in GaN based models appears to be more sensitive to SOH.

It is suggested that the die attach layer with a higher SOH is more capable of accommodating plastic deformation. Consequently the higher SOH results in less plastic work accumulation inside die attach layer, which implies that a longer crack initiation time is expected. Based on the results above, it is notable that increasing the standoff height of the die attach layer is an effective way to prevent the early crack initiation in gold-tin die attach layer especially for a GaN die.



(a)



(b)

Fig 4.3 Effects of SOH on the accumulation of plastic work in die attach layer, (a) Si based model, (b) GaN based model

4.3 Effects of substrate thickness on the accumulation of plastic work

The effects of substrate thickness on the accumulation of plastic work were simulated and shown in Figure 4.4 (a) and

(b). As shown in the figure, the accumulation of plastic work in die attach layer became stable after the second thermal cycle in both Si based and GaN based models. Moreover, due to the higher Young's modulus of GaN die material, there are more plastic work accumulated in die attach layer in the same geometry model, as seen in Figure 4.4 (b).

However, the highest plastic work accumulation was gained with the thickest substrate in both Si and GaN based models in this paper. The thicker substrate has less flexibility in deformation during thermal cycling, which will transfer more stress into die attach layer and result in higher plastic work accumulation.

Therefore, in order to have a longer fatigue life time, a thinner substrate is more desirable for GaN based power devices. Furthermore, a thinner substrate has a higher efficiency in transferring heat from package to heat sink, which is essential to maintain a stable work for power devices.

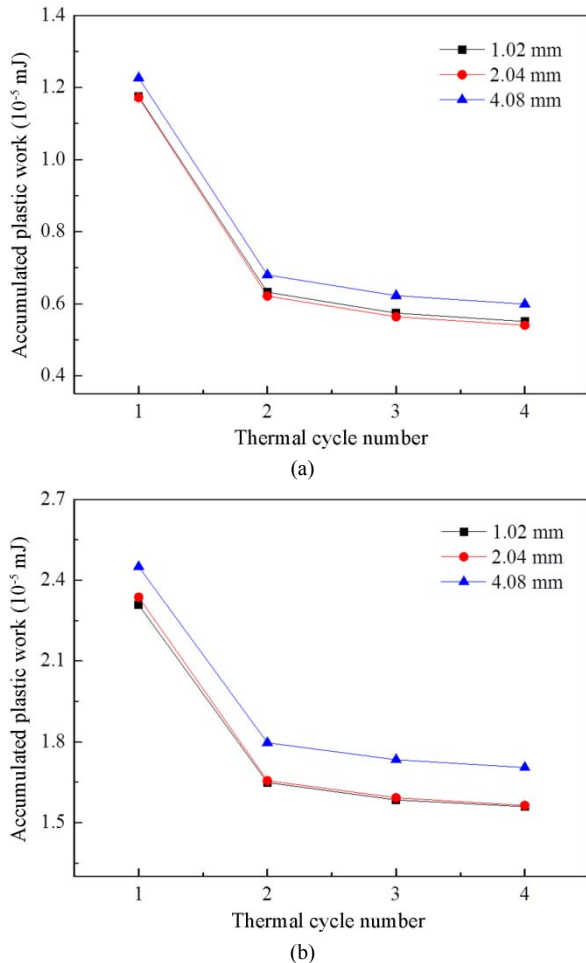


Fig 4.4 Effects of substrate thickness on the accumulation of plastic work in die attach layer, (a) Si based model, (b) GaN based model

5. Conclusions

In this paper, finite element analysis was performed to comparatively investigate the influence of die materials, die attach layer's standoff height and substrate thickness on the fatigue damage accumulation in gold-tin eutectic die attach layer under thermal cyclic loading. The results suggested that a much higher plastic work density was gained in gold-tin die attach layer in the GaN based model. Moreover, it is

suggested that a thicker die attach layer and a thinner substrate are more preferable for GaN power devices in this paper. The optimization of package design helps to maintain a longer fatigue life for power devices. In the future, more works will be focused on the optimization of package design for various working conditions, and a guideline is expected to be given.

Acknowledgments

The work described in this paper was supported by the National High Technology Research and Development Program of China (863 Program) (No. 2015AA033304) and also partially supported by the Natural Science Foundation of Jiangsu Province (No. BK20150249) and the International Science & Technology Cooperation Program of China (No. 2015DFG62430).

References

1. R. Khazaka, L. Mendizabal, D. Henry, and R. Hanna, "Survey of high-temperature reliability of power electronics packaging components," *IEEE Transactions on Power Electronics*, vol. 30, pp. 2456-2464, 2015.
2. L. A. Navarro, X. Perpiñà, P. Godignon, J. Montserrat, V. Banu, M. Vellvehi, et al., "Thermomechanical assessment of die-attach materials for wide bandgap semiconductor devices and harsh environment applications," *IEEE Transactions on Power Electronics*, vol. 29, pp. 2261-2271, 2014.
3. J. Millan, P. Godignon, X. Perpina, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE transactions on Power Electronics*, vol. 29, pp. 2155-2163, 2014.
4. A. A. Bajwa, "New assembly and packaging technologies for high-power and high-temperature GaN and SiC devices," 2015.
5. Z. Tao, T. Bobal, M. Oud, and J. Song-Hang, "An Introduction to Eutectic Au/Sn Solder Alloy and Its Preforms in Microelectronics/Optoelectronic Packaging Applications [J]," *Electronics & Packaging*, vol. 8, pp. 2-8, 2005.
6. J.-W. Yoon, H.-S. Chun, J.-M. Koo, and S.-B. Jung, "Au-Sn flip-chip solder bump for microelectronic and optoelectronic applications," *Microsystem Technologies*, vol. 13, pp. 1463-1469, 2007.
7. S. B. Brown, K. H. Kim, and L. Anand, "An internal variable constitutive model for hot working of metals," *International journal of plasticity*, vol. 5, pp. 95-130, 1989.
8. L. Anand, "Constitutive equations for hot-working of metals," *International Journal of Plasticity*, vol. 1, pp. 213-231, 1985.
9. I. SAS, "ANSYS Mechanical APDL Theory Reference," p. 110, 2012.
10. K. C. Otiaba, R. Bhatti, N. Ekere, S. Mallik, and M. Ekpu, "Finite element analysis of the effect of silver content for Sn-Ag-Cu alloy compositions on thermal cycling reliability of solder die attach," *Engineering Failure Analysis*, vol. 28, pp. 192-207, 2013.
11. G. Wang, Z. Cheng, K. Becker, and J. Wilde, "Applying Anand model to represent the viscoplastic deformation

- behavior of solder alloys," *Journal of electronic packaging*, vol. 123, pp. 247-253, 2001.
12. Y. Liu and Z. Wu, "Simulation Research on Solder Joint Residual Strain Energy of Au80/Sn20 Eutectic Soldering GaAs Chip," 2015.
 13. J. Zhang, *Fast Qualification of Solder Reliability in Solid-state Lighting System: TU Delft, Delft University of Technology*, 2015.
 14. F. Le Henaff, S. Azzopardi, E. Woïrgard, T. Youssef, S. Bontemps, and J. Joguet, "Lifetime Evaluation of Nanoscale Silver Sintered Power Modules for Automotive Application Based on Experiments and Finite-Element Modeling," *IEEE Transactions on Device and Materials Reliability*, vol. 15, pp. 326-334, 2015.
 15. J. P. Calame, R. E. Myers, F. N. Wood, and S. C. Binari, "Simulations of direct-die-attached microchannel coolers for the thermal management of GaN-on-SiC microwave amplifiers," *IEEE Transactions on Components and Packaging Technologies*, vol. 28, pp. 797-809, 2005.
 16. Y. Liu, J. Zhao, C. C.-A. Yuan, G. Q. Zhang, and F. Sun, "Chip-on-flexible packaging for high-power flip-chip light-emitting diode by AuSn and SAC soldering," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 4, pp. 1754-1759, 2014.
 17. J. Kwak, "Strain behaviors of solder bump with underfill for flip chip package under thermal loading condition," *Journal of Mechanical Science and Technology*, vol. 28, pp. 4899-4906, 2014.