Thermotransport phenomena in quantum point contacts and quantum dots

by

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Abstract

Electrostatically-defined nanostructures in bilayer graphene (BLG), known for its tunable bandgap, have promising applications in spintronics and valleytronics, however, its thermotransport phenomena have not yet been investigated. This thesis aims to fabricate a BLG field-effect transistor (FET) device and characterize the thermotransport phenomena (Seebeck coefficient) in electrostatically defined quantum point contacts (QPCs) and quantum dots (QDs). For this purpose, a bilayer graphene flake is encapsulated in hexagonal boron nitride (hBN) with Ti/Au heaters, top gates and 100-nm-separated split gates placed on top of the upper hBN flake. To define a QD, the 100 nm wide finger gates were separated from the top gates by a 30 nm Al_2O_3 dielectric. However, the electric field induced by the back gate was being screened by a layer of charges somewhere between the back gate and the bilayer graphene. The origin of this layer of charges remains unknown. As a result, the channel could not be fully depleted (unless when $B = 5$ T) and showed features indicating an unintended charging and discharging effect somewhere in the sample. As a consequence, the formation of a QD or a QPC at $B = 0$ T was not possible. Despite that, thermal voltages were measured in the two-dimensional BLG, applying currents up to 50 μA to the aforementioned heaters. The estimated Seebeck coefficient (based on resistance characterizations) was in the range of μV/K (corresponding with theoretical predictions) and enabled an estimate of an induced temperature gradient of 0.5 ± 0.2 K.

1. Introduction

One of the great challenges of contemporary electronics is the exponentially increasing dissipated power density in integrated electronics circuits [1] [2]. Due to the high power density, excess heat produced by electric currents in circuit elements cannot be entirely dissipated, which results in higher operating temperatures for devices, decreased performance, and eventually hardware failures. The power efficiency of the device and its longevity can be increased by harvesting this dissipation energy [3]. Furthermore, nanopatterned graphene devices in particular such as quantum dots and field-effect transistors are the topic of intense research due to their recently found electrical characteristics [4] [5]. Graphene is widely regarded as a promising material, partly because it has both valley and spin degrees of freedom available to encode information [6] [7]. This makes graphene a candidate for potential valleytronic and spintronic applications [8], which could help sustain the constant miniaturization improvements described by Moore's law [9].

Previous experiments have shown that nanostructures defined in graphene through dry etching suffer from randomly positioned localized states along the etches [10] [11]. As a result, electrostatic gates are unable to monotonically tune the barrier transmission [10] [11]. In bilayer graphene, however, a bandgap can be opened through the application of a vertical electric field [12] [13]. This suppresses the conduction under the top gates, and has been used by several research groups to define one-dimensional channels or zero-dimensional quantum dots (QDs) [14] [15] [16], which can be applied in quantum-dot based qubit systems. Characterizing the thermotransport phenomena in these quantum point contacts (QPCs) and QDs in bilayer graphene has not yet been explored, but would yield additional insight into the transport properties of these geometries and, when being harvested, can increase their longevity.

For this purpose, a bilayer graphene sample is encapsulated in the insulator hexagonal boron nitride (hBN) with a Ti/Au heater placed on top of the upper hBN flake. The top gate and bottom gate voltages were measured for AC currents with different amplitudes (at frequency ω) to heat up the sample. Meanwhile, thermal voltages were monitored in the two-dimensional BLG at the frequencies ω and 2ω, corresponding to the characterization of the first and second harmonic (Peltier and Joule heating, respectively). Through the application of a vertical electric field, a bandgap is opened in bilayer graphene [12] [13]. This suppresses the conduction under the top gates, and has been used by several research groups to define one-dimensional channels (QPCs) or QDs [14] [15] [16] using split-gates structures to guide the carriers. The existing resistance measurements reveal that the lowest possible conductance in such structures is constrained by leakage currents underneath the split-gates, which may be attributed to either hopping transport or a narrow energy gap. If tunnel barriers are to be effective in generating high-quality quantum devices, then the tunnelling resistance needs to significantly surpass the resistance quantum h/e^2 [17].

This thesis is part of the M.Sc. Applied Physics curriculum at the TU Delft. Chapter 2 contains an overview of the relevant background required to understand the following chapters. Chapter 3 contains the experimental method, including an outline of the fabrication processes and the measurement setup. Chapter 4 reports and discusses the results and chapter 5 concludes the thesis.

2. Theoretical Background

2.1. Two-dimensional materials

2.1.1. Graphene

Graphene is a single layer of carbon atoms packed into a benzene-ring structure and is one of the allotropes of carbon. The existence of a real two-dimensional material with a thickness of one atom was claimed to be impossible by the Mermin-Wagner theorem [18]. Nevertheless, graphene was first isolated by Novoselov and Geim [19] in 2004 through cleaving a graphite crystal using scotch tape. Since then, graphene's remarkable qualities — including the fact that it is 100 times stronger than steel [20], very flexible [21], and a superior conductor of electricity [5] — have captivated the attention of scientists.

In the reciprocal space, the structure of graphene is characterized by a uniquely defined hexagonal primitive cell [22], an example of a Brillouin zone. Only two of the six valleys, K_i, are in the first Brillouin zone and inequivalent (not linked by a reciprocal lattice vector): K and K'. Every unit cell consists of two identical carbon sublattices A and B in the real space, see Fig. 1a, which characterizes the honeycomb lattice. The honeycomb structure gives birth to the valley degree of freedom [6] [7] in reciprocal space since electrons can be in both spots. The vicinity of these two spots is also known as the two valleys of graphene's electronic spectrum, see Fig. 1. The electronic spectrum can be derived using the tight-binding Hamiltonian [22], which accounts for quantum hopping between the atoms. This is done through writing down the eigenstates $\langle\phi|$ of the Hamiltonian through Bloch's theorem [23] and then evaluating the eigenvalues through $\langle\phi|H|\phi\rangle$ [24], which gives the energy spectrum shown in Fig. 1b. Because of graphene's crystal structure, charge carriers have a low energy Dirac-like linear spectrum [22], $E(k) = \pm v_{F0}\hbar|k|$; with $v_{F0} \approx 10^6$ m/s [25] [26] the carrier (or Fermi) velocity, resembling the spectrum of massless relativistic particles (for instance, photons) [27] rather than the standard parabolic relation for massive quasi-particles. The conical energy spectra of these quasi-particles intersect close to the boundaries of the Brillouin zone. Even though there is no bandgap, there is zero density of states where the two bands intersect (the K point in the Brillouin zone). This point is the charge neutrality point (CNP) or Dirac point (see Fig. 1b), with the lower and upper cone the valence and conduction bands, respectively.

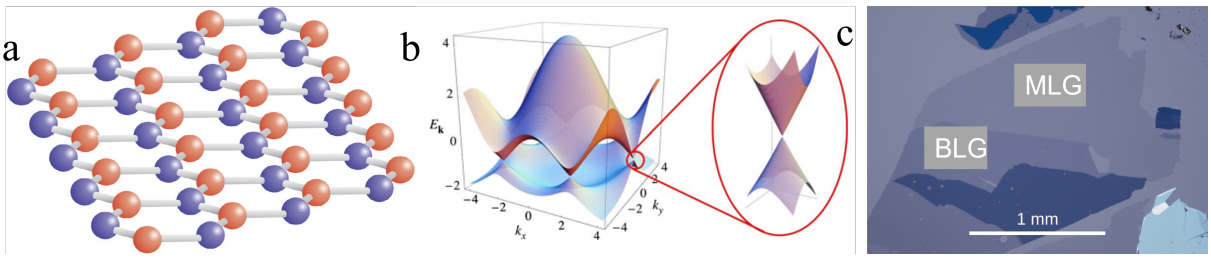

Figure 1: a) The atomic structure of graphene, with atoms from sublattices A and B marked with different colors, from [27]. b) The band structure of graphene, with a magnified Dirac cone around the K point. Taken from [21]. c) Microscope image of graphene, including monolayer graphene (marked MLG) and bilayer graphene (BLG) [28] with different optical contrasts.

Close to the K-points, the low-energy Hamiltonian can be written as $H = v_{\mathrm{F0}} \cdot \sigma \cdot p$, with σ the pseudo-spin [5] (describing the electronic amplitudes on the sublattices A and B). Chirality, which takes on positive values for electrons and negative values for holes, projects pseudospin onto the direction of motion. It is a conserved quantity as backscattering is suppressed in graphene [21].

The density of states associated with the conical dispersion of electrons in graphene is computed by use of the dispersion relation [22]:

$$\nu(E_{\mathrm{F}}) = \frac{g_{\mathrm{s}} g_{\mathrm{v}} |E_{\mathrm{F}}|}{2\pi\hbar^2 v_{\mathrm{F0}}^2}. \tag{1}$$

One of the characteristics of massless Dirac electrons is the linear dependence of the density of states on energy. Moreover, it vanishes at the Fermi energy, giving rise to the so-called pseudo-diffusion effect [29]. The density of states also influences the quantum capacitance, which depends on the carrier density [30] (see Eq. 4).

2.1.2. Bilayer graphene

Fig. 2a depicts the structure of bilayer graphene (BLG), which is constructed by stacking two graphene monolayers on top of each other. BLG may be found naturally in two different configurations: the AB, or Bernal-stacked [31], where half of the atoms are immediately over a hexagon's center in the bottom graphene sheet and the other half are over an atom; and the less frequent AA, where the layers are perfectly aligned [32]. Here, we study naturally occuring BLG, which we assume to be AB-aligned, as AB stacking results in a parabolic low energy spectrum rather than the linear energy spectrum found in graphene. The bandgap in BLG may be controlled using a vertical electric field, which breaks the two layers' inversion symmetry [12] [13], see Fig. 2b. In the figure, the band structure (the blue and yellow parabolas signifying the conduction and valence band, respectively) of BLG for when the bandgap is zero (left panel) and nonzero (right panel) are visualised. This ability to open the bandgap in BLG offers up new application domains, as bandgap has a significant impact on the transport and optical characteristics [13] of a given material. As a result, it allows semiconductor devices such as p-n junctions, transistors, photodiodes, and lasers operate with unprecedented tuneability [33]. To make use of the bandgap in an electronic transport measurement, as shown in

Fig. 2b, one needs to tune E_{F} into the bandgap. For this purpose, one needs a device with two gates, one on top and another one underneath. The difference between the top and bottom electrical displacement fields (the displacement of charge per unit area due to an electric field) also causes net carrier doping, or a change in the Fermi energy (E_{F}). By adding more carriers in the BLG, the Fermi energy is shifted into the electron regime (away from the CNP) and the resistivity decreases again (with respect to the resistance at the CNP). By depleting the system from carriers, the Fermi energy is instead shifted into the hole regime; again with the same effect on resistivity.

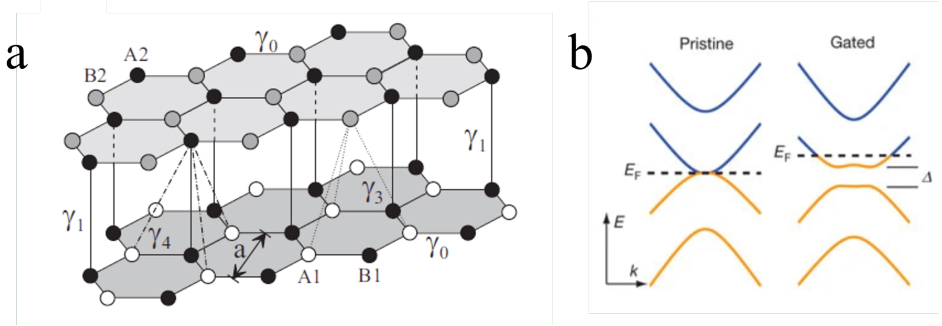

Figure 2: a) Bernal-stacked BLG. In this schematic, $a = 2.46$ Å the lattice constant (distance between adjacent unit cells), $\gamma_0 = a/\sqrt{3} = 1.42$ Å the distance between two carbon atoms and $\gamma_1 = 3.35$ Å the distance between the two sheets of graphene. Adapted from [34]. b) Low energy band structures for BLG. For $\Delta = 0$ (left panel), the electric field is zero and thus no energy bandgap. For $\Delta \neq 0$ (see right panel), the bandgap was opened by an electric field. The blue band represents the conduction band and the yellow parabolas represent the valence band. Obtained from [13].

When there is no perpendicular electric field, the energy spectrum of BLG is described by:

$$E(k) = \pm\frac{\hbar^2 v_{F0}^2 |k|^2}{\gamma_1} = \pm\frac{\hbar^2 |k^2|}{2m^*}. \tag{2}$$

In this equation, $\gamma_1 \approx 0.4$ eV is the coupling parameter between A1 and B2 atoms, as defined in Fig. 2, $m^* = \gamma_1/2v_{\mathrm{F0}}^2$ is the effective mass.

The energy-dependent density of states for BLG is:

$$\nu(E) = \frac{g_s g_v}{4\pi\hbar^2 v_{F0}^2}(2|E| + \gamma_1) \tag{3}$$

which is similar to the density of states of monolayer graphene if $|E| \gg \gamma_1$, see Equation 1. Here, $g_s = 2$ and $g_v = 2$ are the spin and valley degeneracies, respectively.

According to the Drude model [35], the square resistance R_{sq} (units: Ωm in 3D and Ω in 2D) as a function of two-dimensional carrier density is given by $R_{\mathrm{sq}} = (ne\mu)^{-1}$, with $n = C_{\mathrm{g}}(V_{\mathrm{g}} - V_{\mathrm{g}}^0)/e$ (also see Section 2.2). In this equation, C_{g} and V_{g} are the capacitance and voltage of the gate, respectively, and ${V_{\mathrm{g}}}^0$ the CNP of graphene. This means that the resistance has a sharp peak (strictly: a divergence) when V_{g}= ${V_{\mathrm{g}}}^0$, and should theoretically occur at ${V_{\mathrm{g}}}^0 = 0$ V (see Fig. 1). This divergence, however, does not occur in real devices because of

inhomogeneous doping (electron-hole puddling [36]), molecular doping and thermal broadening. Inhomogeneous doping is caused by charged impurities above and below the graphene, which lead to a local shift in the Fermi energy. This results in a non-homogeneous gating in the graphene, splitting into hole-rich and electron-rich puddles modifying the electrostatic potential. In addition, thermal broadening gives rise to thermally excited carriers, limiting the minimal carrier density at the CNP. According to the Drude model, the electron mobility is given by $\mu = |e|\tau/m^*$, where τ is the momentum scattering time and m^* the effective mass (see Equation 2). Besides inducing variations in potential, charged impurities can also act as dopants and form a source of long range scattering (as they produce a Coulomb potential). Neutral impurities, caused by defects or dislocations in the carbon lattice), could induce short range scattering (and may play a role at high carrier densities and in high mobility samples where localized charges are screened by the large amount of free charges). These scattering effects limit τ and determine the conductivity in BLG.

2.1.3. Hexagonal Boron Nitride

Hexagonal boron nitride (hBN), an isostructural to graphite, possesses characteristics that are quite different from those of graphite. hBN is an insulator with a bandgap of around 5.9 eV [37] and an atomic structure that alternates boron and nitrogen atoms. The lattice constant of hBN is 1.8% greater than graphene's lattice constant [38]. When compared to SiO_2 substrates, hBN is the cleanest dielectric gate available for graphene devices, significantly and is utilized as an alternative substrate for high-quality graphene devices [39] [40]. Encapsulating graphene with hBN leads to the highest-mobility graphene transistors [15] [41]. Stacking 2D van der Waals materials vertically, like stacking hBN and graphene as done in this thesis, offers new fundamental physics and quantum device applications [42]. The stack is held together by weak van der Waals forces. When the lattices of the materials in a van der Waals heterostructure are rotationally aligned, it gives rise to a Moiré superlattice, and thereby exhibiting a distinct Moiré pattern.

2.2. Electronics

The design of the device is similar to that of a field-effect transistor. This is a device which uses an electric field to control the flow of electrons, by creating a field between the source (where the carriers enters the transistor) and the drain (leaving the transistor). The gate is used to modulate channel conductivity, influencing the source-drain current.

The dual-gate field-effect transistor prepared in this thesis is made through encapsulating a BLG flake in hBN and placing it on a graphite back gate. The stack is placed on an insulating silicon dioxide layer with a conductive, heavily doped silicon substrate. The BLG is contacted with Ti/Au contacts. Moreover, split gates and heaters are placed on top, complemented with a layer of Al_2O_3 that serves as a gate dielectric for the finger gates. The top layer consists of the finger gates, that are used to control carrier density in the areas underneath the split gates. The combination of split gates and finger gates can then be used to define QPCs and QDs. For a schematic overview of the stack, see Fig. 3.

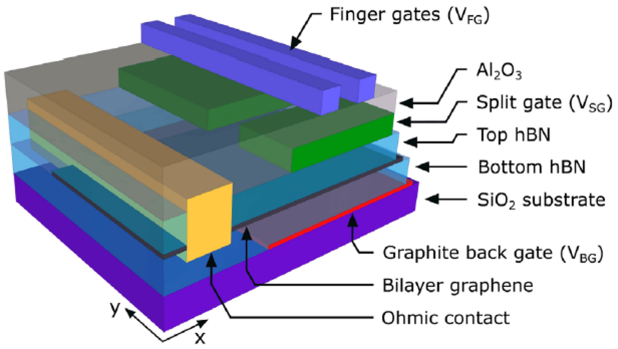

Figure 3: A schematic of the device prepared, taken from [43]. It features the finger gates (purple), split gates (green), dielectric Al_2O_3 (gray), hBN (blue), a contact (yellow), BLG (black) and a graphite backgate (red). The combination of split gates and finger gates can be used to define QPCs and QDs.

When tuning the BLG with the combined action of both top and backgate, the carrier density induced can be written as:

$$n = \frac{1}{e}(C_{\mathrm{bg}}(V_{\mathrm{bg}} - V_{\mathrm{bg}}^{(0)}) + C_{\mathrm{tg}}(V_{\mathrm{tg}} - V_{\mathrm{tg}}^{(0)})), \tag{4}$$

with $C_{\mathrm{bg}} = \epsilon_0\epsilon_{\mathrm{bg}}/d_{\mathrm{bg}}$. In this equation, C_{bg} is the capacitance of the back gate per unit area, e the elementary charge, $\epsilon_0 = 8.854 \times 10^{-12}$ F/m the vacuum permittivity, $\epsilon_{\mathrm{bg}} = 3.9$ the relative dielectric permittivity of SiO_2 and d_{bg} the thickness of the bottom hBN flake. Furthermore, $V_{\mathrm{bg}}^{(0)}$ is the Similarly, C_{tg} can be defined, using the thickness of the top hBN flake and $\epsilon_{\mathrm{tg}} = 3.75$ the relative dielectric permittivity of hBN. Typically, the carrier density can range between being depleted and $\pm 10^{16}$ m^{-2}.

The resulting electric field is:

$$E = \frac{\epsilon_{\mathrm{bg}}(V_{\mathrm{bg}} - V_{\mathrm{bg}}^{(0)})}{2d_{\mathrm{bg}}} - \frac{\epsilon_{\mathrm{tg}}(V_{\mathrm{tg}} - V_{\mathrm{tg}}^{(0)})}{2d_{\mathrm{tg}}}. \tag{5}$$

Typical values for the displacement electric field in BLG in this configuration range up to around 3 V/nm [44]. For this value of the electric field, the bandgap has been shown to open up to 250 meV [13].

The combination of top and back gate voltages creates an electric displacement field, which changes the density of the underlying electron gas (like in the case of a capacitor) and also change its Fermi energy. At specific voltage configurations (the CNP), the density of states is tuned to very small values (theoretically: zero), thus yielding a resistance various orders of magnitude larger. At zero carrier density ($n = 0$ in Eq. 4), the linear relation between V_{bg} and V_{tg} can be written as follows:

$$V_{\mathrm{tg}}(V_{\mathrm{bg}}) = -aV_{\mathrm{bg}} + b, \tag{6}$$

with $a = C_{\mathrm{bg}}/C_{\mathrm{tg}}$ and $b = V_{\mathrm{tg}}^0 - V_{\mathrm{bg}}^0 C_{\mathrm{bg}}/C_{\mathrm{tg}}$. This has also been confirmed experimentally in [12], see Fig 4a for the measurement circuit and b for the resulting 3D plot. By shifting the Fermi energy away from the CNP into the hole or electron regime, we decrease the resistivity inside the BLG. Besides changing the carrier density, applying an electric field also opens a bandgap due to the layer symmetry breaking (see Section 2.1.1). Using specific voltage combinations of the top gates, finger gates and backgate as described in Fig. 3, we can tune the structure to create QPCs (Section 2.3) and QDs (Section 2.4).

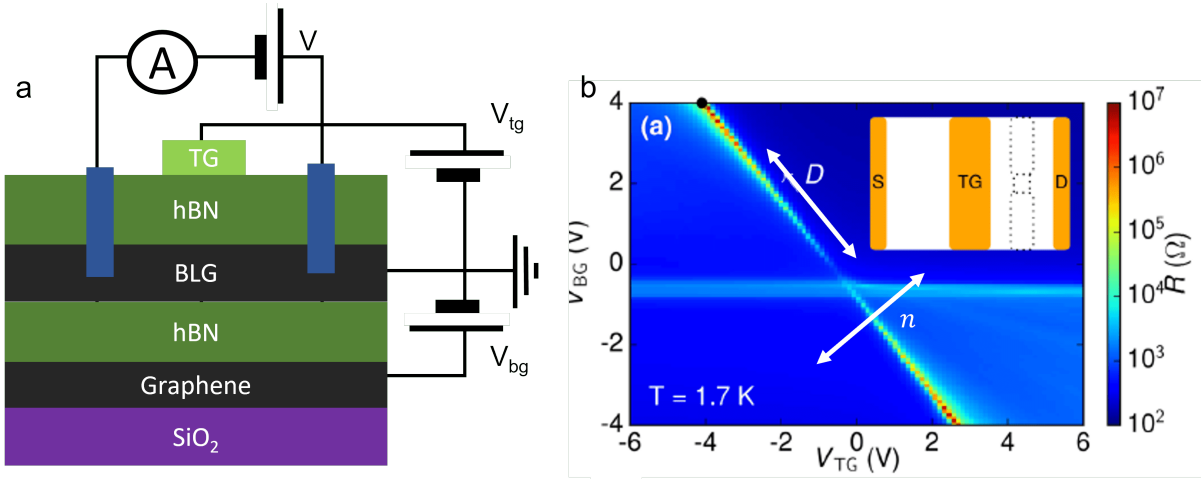

Figure 4: a) Side view of the stack, top gate (light green) and two contacts (source and drain) etched into the BLG (blue). The combined action of V_{tg} and V_{bg} create an electric field, depleting the sample from carriers at certain configurations of V_{tg} and V_{bg}. Furthermore, the BLG is grounded, a voltage is applied between source and drain and the current is monitored (from which the resistance can be determined). b) A typical 3D plot of opening the bandgap in BLG. The main features are the diagonal line across the graph, which follows from setting $n = 0$ in Eq. 4, and the horizontal line at $V_{\mathrm{tg}} = 0$ V. They correspond with the CNP underneath V_{tg} and the CNP of the BLG sample not affected by V_{tg}. The displacement field D and carrier density are varied along and perpendicular to the diagonal line, respectively. Adapted from [12].

2.3. Quantum Point Contacts

Quantum point contacts were first fabricated independently by a team from Cavendish Laboratory [45] and TU Delft & Philips [46] in 1988. Through reducing the width of the underlying two-dimensional electron gas (2DEG) by applying a voltage through a split gate configuration (with a minimal separation in the order of the Fermi wavelength, which is the De Broglie wavelength of electrons at the Fermi energy), the conductance of the structure becomes quantized in steps of $\frac{2e^2}{h}$, see Fig. 5. Also, the mean free path of the electrons should exceed the size of the structure (ensuring ballistic transport) and temperatures should be sufficiently low such that electron-electron and electron-phonon interactions are weak. Even if there are no impurities, reflections occur when a small number of propagating modes in the point contact are matched to a greater number of modes in the reservoir, resulting in a non-zero resistance. Quantum mechanically, the net current flowing through the QPC is equally distributed among the 1D subbands, or transverse modes [47] (signified by n in Eq. 7). In Fig. 5c, the

shaded area is the net current at the Fermi surface in the QPC. The permitted states are located on the horizontal lines, which correspond to continuous values for k_x and quantized values for $k_y = \pm n\pi/W$, respectively (with n = 1, 2, . . . , N and $N = \text{Int}(k_F W/\pi)$. A quantized conductance is produced as a result of the development of these 1D subbands. The equipartitioning of current, which is the fundamental process for conductance quantization, is shown for a square-well lateral confining potential with width W. As n increases, the group velocity $v_n = \hbar k_x/m$ drops since it is proportional to cosϕ. The rise in the 1D density of states (ρ_n), however, offsets the decline in v_n. The product $v_n\rho_n$ does not depend on the subband index since ρ_n is proportional to $1/\cos\phi$ and n is proportional to the length of the horizontal lines inside the dashed region in Fig. 5.

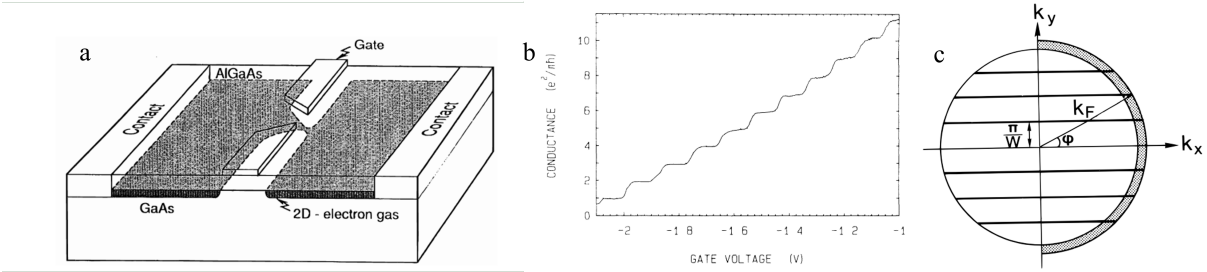

Figure 5: a) A schematic cross-sectional view of a QPC, defined in a high-mobility 2D electron gas [48]. The area between the split gates defines a QPC when a negative voltage is applied. The contacts are used to measure the conductance. b) Conductance of the QPC versus the finger gate voltage. The expected quantized behavior ($\Delta G = 2e^2/h$) can be seen [46]. c) Fermi surface, obtained from [47]. The shaded area is the net current in the QPC, with the permitted states located on the horizontal lines corresponding to a square-well lateral confining potential with width W.

The Landauer formula may be used to describe the quantized conductance of a point contact (see Fig. 5b):

$$G = \frac{2e^2}{h} \sum_n t_n \tag{7}$$

with G the conductance, and $0 \leq t_n \leq 1$ the eigenvalues of the transmission matrix t, which are all 1 in an ideal QPC. Deviations in conductance are $\sim 1\%$ due to the difficulty to determine the series resistance from the wide regions accurately, and due to backscattering as a result of abrupt widening of the geometry.

Recently, QPCs have been defined in BLG encapsulated in hBN through the combined action of multiple gates [12]. The combination of back gate and top gate allows for the independent control of the Fermi level beneath the split gates and the bandgap [49]. With the appropriate gate voltages, the carrier density underneath the split gates can become zero, making it insulating. The channel between the split gates, however, still has a finite carrier density and defines a point contact. If there is ballistic transport, the conductance of the point contact is quantized as in equation 7 and becomes a QPC.

Experimentally, the minimal conductance is limited by leakage currents below the split gates. This leakage current could be the result of hopping transport or a small energy gap. The Fermi energy can be calculated by integrating formula 3:

$$n = \int_0^{E_F} \frac{g_s g_v}{4\pi\hbar^2 v_{F0}^2}(2|E| + \gamma_1)dE \tag{8}$$

By then using the dispersion relation described in equation 2, we can substitute E_F and calculate k. Using $m^* = 0.033 \times \mathrm{m_e}$ [50], $n = 1 \times 10^{16}$ and $v_{F0} = 1 \times 10^6$, we get $E_F = 16.67$ meV. By using the relation $\lambda = 2\pi/k$, a Fermi wavelength of 50 nm is obtained, indicating that the separation between the split gates must be in the 100 nm range. Since the mean free path of the electrons should exceed the size of the structure, the maximum length of the split gates is in the micrometer range [51]. For the correct combination of voltages in split gates and back gate, the carrier density can be depleted underneath the split gates to define a QPC. Using the finger gates, the carrier density in the QPC can then be modulated.

Quantized conductance in 2D materials can also be induced through the application of an increasing magnetic field (in the Tesla range) perpendicular to the BLG plane and current; known as the quantum Hall effect. The quantum Hall effect was discovered by Klaus von Klitzing [52] and has been first shown in graphene by [26] [25].

2.4. Quantum dots

Quantum dots (QDs), which can be created through colloidal synthesis [53], self-assembly [54], or electrical gating [55], isolate a single charge carrier (electron or hole). Following the QPC procedure, one may define smaller finger gates or use multiple of them to define not only narrow, but also short islands with sizes of the order of the Fermi wavelength [43] [56]. A positive back-gate voltage causes a finite electron density inside the channel, which can further be reduced under each finger gate by applying a negative voltage to that gate. At some point, transport via the channel is suppressed because the electron gas beneath the finger gate has been depleted. Further lowering the finger gate voltage results in the induction of a limited hole density, which creates a tiny p-type island (containing a single hole) inside the n-type channel. The negative charge on the p-type channel is connected to the positive charge on the n-type channel via a pn-junction. The edge has been stripped of charge carriers, creating a natural tunnel barrier that enables the formation of a p-type QD beneath each of the finger gates.

As zero-dimensional structures, QDs have a sharper density of states than structures with greater dimensions, such as quantum point contacts [43]. They thus possess better optical and transport qualities. Lorentzian peaks in the conductivity of QDs indicate that electrons are regionally constrained. In Fig. 6a, the conductance spectrum of a QD is featured, recognizable due to the Lorentzian peaks. Fig. 6b contains the band structure in the channel.

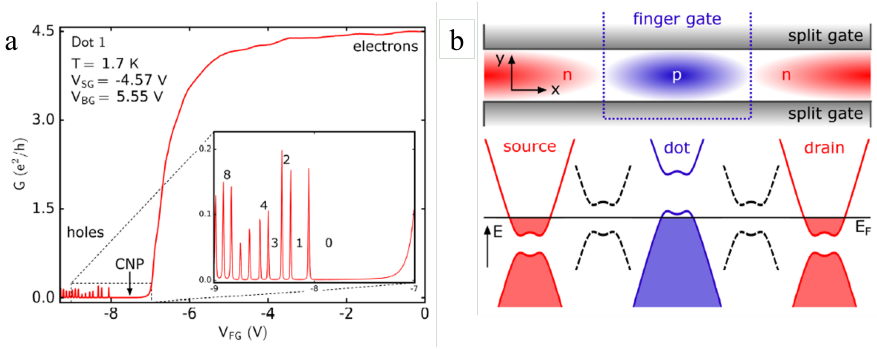

Figure 6: a) The conductance spectrum of a quantum dot [43]. It features several conductance peaks clearly distinguishable in the zoomed box. b) Diagram illustrating the band structure in the channel at various points along the current direction. The band alignment between the dot area and the leads is depicted graphically by black dashed lines.

In [56], the researchers defined split gates with 160 nm separation. On top, they defined three 40 nm narrow finger gates, separated by 120 nm. With these narrow finger gates, they were able to define a single n-type QD. This is done by setting a bias voltage (source-drain voltage) across the n-type channel and then tuning the two outmost finger gates close to their CNP, such that the regions underneath these gates are depleted. This forms tunnel barriers to the n-type QD in the middle. As the voltages of the outmost finger gates are decreasing, p-type QDs can form (to obtain double QD or triple QD). In [43], the researchers defined split gates with 100 nm separation and 100 nm wide finger gates, with which they were also able to define QDs.

2.5. Thermoelectric phenomena

A thermocouple is an electrical device made of two electrical conductors creating an electrical junction [57], and is used by the thermoelectric effect to convert a temperature difference into an electric voltage and vice versa. It creates a voltage when the temperature (T) is different on each side, by diffusing charge carriers in the material from the hot side (T_{hot}) to the cold (T_{cold}) side (Seebeck effect, see Section 2.5.1). In contrast, when a voltage is applied, heat is transferred from one side to the other, resulting in a difference in temperature (Peltier effect, see Section 2.5.2). Both the Peltier and Seebeck effect are thermodynamically reversible, meaning that their direction may be changed by infinitesimal variations in the environment's pressure or temperature without causing the system or its surroundings to change [57]. Also, Joule heating will be covered.

2.5.1. Seebeck effect

The Seebeck effect is the development of an electromotive field between a thermocouple when the ends are subjected to a temperature difference ΔT between them [58]. At the absolute zero, $T_0 = 0$ K, the probability that an electron has an energy below the Fermi level is 1, while the probability that an electron has an energy higher than the Fermi level is 0. At temperatures $T > 0$ K, electrons below E_{F} are excited to higher energies according to the Fermi-Dirac distribution function, see Fig. 7. So this means that for $\Delta T = T_{\text{hot}} - T_{\text{cold}}$, some electrons locally in the T_{hot} area have a higher energy than all the electrons in the area T_{cold}.

Therefore, these aforementioned electrons in T_{hot} will move to T_{cold} and increase electron density there. At the same time, electrons below E_{F} will diffuse from the cold towards the hot area to fill up the lower energy states available there. As a consequence, if the density of states does not change with E_{F}, no net thermal current is expected. However, as the density of states is dependent on energy (Equation 1 for graphene and Equation 3 for BLG), the number of electrons above the Fermi energy becomes larger than below or vice versa, depending on the location of the Fermi energy. This leads to a net thermocurrent.

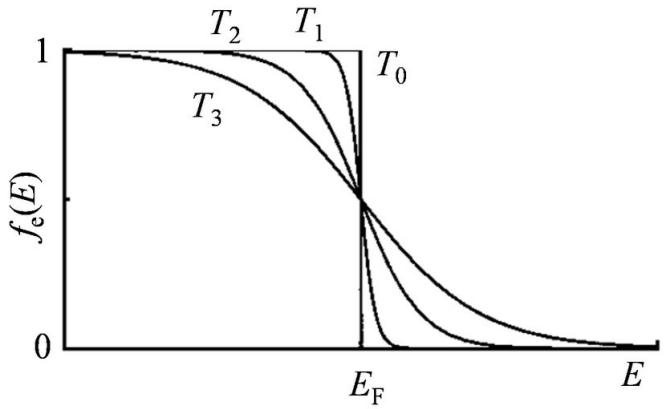

Figure 7: The Fermi-Dirac distribution functions for electrons at T_{i}, with $T_3 > T_2 > T_1$ and ($T_0 = 0$K), with the electron energy on the x-axis values and on the y-axis their corresponding probabilities. At $T_0 = 0$ K, all the states below E_{F} are occupied and above are empty, a picture that changes upon heating. Obtained from [59].

The local current density can be described using:

$$J = \sigma(-\nabla V + E_{emf}) \tag{9}$$

in which V is the developed voltage (which has units of V), E_{emf} the electromotive field (units V/m) and σ the conductance. The Seebeck coefficient S (with units of V/K) is described by the following relation:

$$S = -\lim_{\Delta T \to 0} \frac{V}{\Delta T} \tag{10}$$

V the thermoelectric voltage and ΔT the temperature gradient. Physically, the Seebeck coefficient (or thermopower) is a measure for the magnitude of an induced thermoelectric voltage in response to a temperature difference across that material. It can be thought of as heat per carrier over temperature (entropy per carrier).

For graphene, the Seebeck coefficient can be estimated using the Mott formula [60] [61].

$$S_{Mott} = \frac{\pi^2 k_{\mathrm{b}}^2 T}{3e} \frac{\mathrm{d}\ln(R)}{\mathrm{d}E_{\mathrm{F}}} \tag{11}$$

with k_{b} the Boltzmann constant (JK^{-1}) and R the resistance (Ω). The Seebeck coefficient depends on the density of states and resistance of the material, which are different for 2D,

1D and 0D structures (see Equation 3 for 2D, a step function with stepsize $2e^2/h$ for 1D and Lorentzian peaks for 0D). The Mott's formula is valid at low temperatures ($k_BT \ll \mu$) to approximate the Seebeck coefficient in quantum point contacts [62]. For quantum dots, the Mott's formula can still be used as a rule of thumb for approximating the Seebeck coefficient, but is a factor of e^2/CkT smaller than the correct result [63]. It predicts sawtooth-like oscillations in the thermopower for low lattice temperatures and small heating currents [64] [63]. Therefore, we can model the Seebeck coefficients for these cases for BLG, see Fig. 8. The code used to create these figures is shown in the Appendix, the 1D graph was obtained from processing previous measurements on a gate-defined QPC in BLG. The 2D case is very similar to [65]. The large value obtained in the quantum point contact originates from the density of states becoming too small to conduct the current, resulting in an infinite resistance value - and thus, a diverging Seebeck coefficient. The width of the peaks in the thermopower in the quantum dot depends on the coupling of the leads' coupling strengths [66].

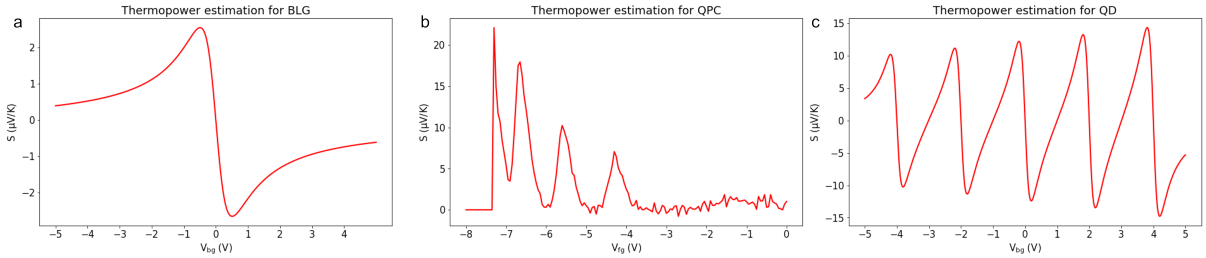

Figure 8: The expected behavior of the Seebeck coefficients for a) BLG (2D), b) a QPC (1D) and c) a QD (0D). In the 1D case, there are peaks at the conduction plateaus. The width of the peaks in the thermopower in the quantum dot depends on the coupling to the leads [66].

The Seebeck effect is reversible, meaning that when switching the T_{hot} and T_{cold} areas, it changes sign. The calculations in Fig. 8 agree with experiments in the past for the Seebeck coefficient for BLG [67], QPCs [68] and QDs in GaAs/AlGaAs [69].

2.5.2. Peltier effect

The Peltier effect is a measure for the amount of thermal energy emitted or absorbed by an electrical current [70]. The heat generated by Peltier heating is:

$$\dot{Q} = \Pi I \tag{12}$$

with $\Pi = TS$ (Kelvin Onsager relation) the Peltier coefficient and I the (AC) current.

The Peltier effect arises due to the difference in average electron energy (or chemical potential) in dissimilar conductors. Depending on the directionality of the current, electrons either transfer their excess energy (leading to heating) or absorb the energy of surrounding atoms (cooling). In QPCs, Peltier heating is quantized as the conductance is also quantized in steps of $2e^2/h$. In QDs, the Peltier coefficient exhibits a sawtooth behavior as in agreement with [63].

2.5.3. Joule heating

Joule heating, or Ohmic heating, is the heating of a conductor through the passage of an electrical current. The power released is proportional to the product of the current and the voltage drop; or, by substituting V with Ohm's law, current squared divided by the resistance.

$$P = IV = I^2/R \tag{13}$$

since Joule heating is proportional to I^2 ($Q \propto \Delta T \propto I^2$, see Equation 13), it can be distinguished from Peltier heating that is linear with I through lock-in measurements (see Section 2.5.2). In QPCs, Joule heating causes broadening in the quantized conductance. Although inside the quantum point contact the transport is ballistic, the exits are not sharply defined. Asymmetries in the banks of QPCs have been predicted to deliver different amounts of Joule heating on both sides of the contact, leading to thermoelectric effects without applying an external temperature gradient [71] but by a voltage drop. In QDs, nonlinear contributions to the power in response to voltage or temperature shifts have been predicted with increasing voltages [72].

3. Experimental method

This section discusses the fabrication process (section 3.1), the characterization method (section 3.2) and the preparation steps to measure.

3.1. Fabrication Process

The chip has the same features as shown in Fig. 3 in section 2.2. The manufacturing of the nanostructures is done in the state-of-the-art cleanroom of the Kavli Nanolaboratory and in the laboraties of the Quantum Nanoscience department at the TU Delft.

3.1.1. Creating the stack

The fabrication of the stack consists of three parts: preparing the crystals (BLG and hBN, respectively), stacking the crystals and graphite back gate through the dry-transfer technique [73] and transferring the stack on a Si/SiO_2 wafer. First, a Si/SiO_2 wafer is cleaned using an O_2 plasma. Then, highly ordered pyrolytic graphite is exfoliated using scotch tape as done originally by [19] by gluing flat graphite crystals in blue tape and then carefully pulling off. When the graphite is thin enough, it is pressed on the SiO_2 substrate. Under the optical microscope, bilayer graphene flakes are selected based on their size (~ 10 μm) and optical contrast relative to the optical contrast of the SiO_2 background. The contrast values are compared with other graphene flakes, such as monolayer graphene. The same exfoliation procedure is repeated for hBN, however, this time we use Blue tape (although less sticky than scotch tape, it suffices for exfoliating hBN and results in less glue residues on the SiO_2). The hBN flakes are then selected based on homogeneity of the flakes. This is important because some parts of the device need to be etched through the hBN to make contact with the BLG, and folds in the flakes could even cause cracks. In Fig. 9, the hBN flakes (a and b) and BLG flakes (c and d) which are used in the stack are shown. More specifically, Fig. 9a was used as the bottom hBN (with a thickness of 22 nm, determined using AFM), Fig. 9b the top hBN (18 nm thick), Fig. 9c the BLG of the stack and Fig. 9d the backgate (the flake with the lowest optical contrast). The bottom hBN flake is thicker than the top hBN flake for additional margin when etching into the BLG through the top hBN, preventing a potential higher etching rate from contacting the BLG with the backgate.

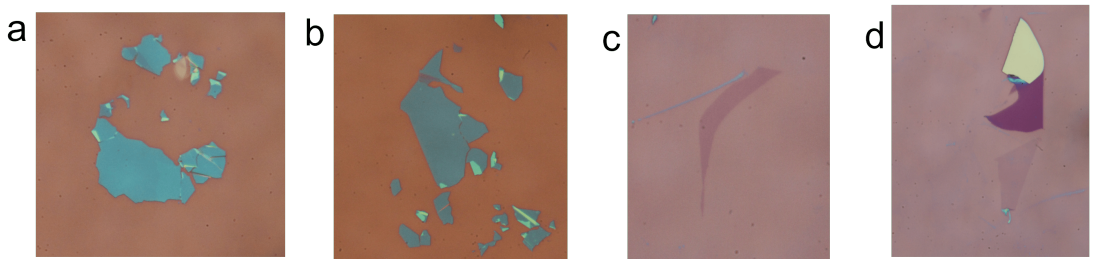

Figure 9: Optical images of the four flakes used to make the stack. a) The bottom hBN flake (thickness of 22 nm). b) The top hBN flake (18 nm). c) The BLG. d) The monolayer graphene flake, used as a backgate.

Subsequently, a glass slide is covered with a thin layer of polycarbonate (PC, 6% dissolved in

chloroform) using a pipette. After that, a thin layer is formed by placing another glass plate on top of the PC-covered slide to spread the PC. The resulting uniform PC film is allowed to dry for 15 minutes in air. Then, a small window in regular tape is cut, placed over the PC and carefully pulled off. Then, a fresh glass slide is taken and a 4-by-4-by-1-millimeter piece of polydimethylsiloxane (PDMS) is placed on it. By aligning the PC covered window with the PDMS, a stamp is created (see Fig. 10).

Then, the stack is made with the dry-transfer technique, see Fig. 10. For this purpose, the SiO_2 with the top hBN flake is fixed by a vacuum underneath a modified microscope with long working distance objectives and x, y and z micromanipulators. Then, the stamp is mounted upside down under the long lens setup and slowly lowered to establish contact with the SiO_2. The chuck is now heated to a temperature of 60 °C to 80 °C. This causes the PC to become more sticky, helps remove water from the interface and facilitates the transfer process. The contact area between the PC and SiO_2 steadily grows as the PC warms up and expands thermally. We turn off the heating after the hBN and PC make contact which results in a slow retraction of the PC film from the substrate as it cools down. The flake is picked up as the PC film remained intact on the PDMS while retracting. This process is repeated for the BLG, the bottom hBN flake and graphite, forming a multilayer heterostructure. The flakes can be precisely aligned with respect to each other by fixing the SiO_2 containing the flake to the chuck of the mask aligner.

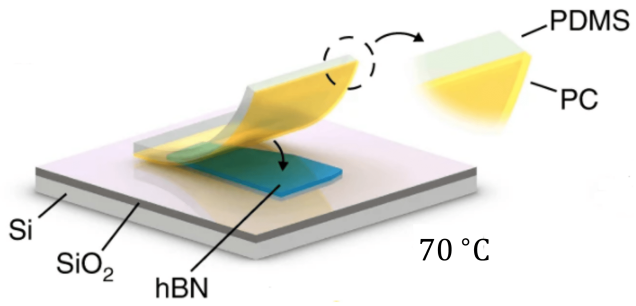

Figure 10: Dry-transfer technique to pick-up hBN (blue) on a Si/SiO_2 wafer with a stamp consisting of PMDS and PC. After this step, the stamp with hBN is lowered to reach BLG, hBN (lower flake) and graphite (back gate). From [74].

Finally, the stack is transferred to a Si/SiO_2 wafer containing different markers for alignment. This is done by melting the PC at 150 °C with the stack placed between the markers. This causes blisters to move in the direction of the PC and aggregate at the edges of the heterostructure, reducing the number of blisters in the stack [74]. As a result, the stack is now on SiO_2 and covered by a PC film that has been molten on top. By soaking for 10 minutes in chloroform, the PC is eliminated. Afterwards, the sample was annealed for 4 hours to clean the stack further. The resulting stack is shown in Fig. 11.

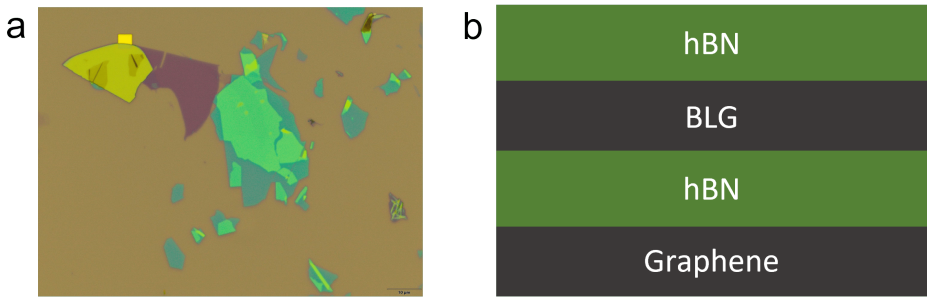

Figure 11: a) Optical image (100x) of the stack after annealing. b) Schematic drawing of the stack, starting with the top hBN, BLG, bottom hBN and the graphene backgate.

3.1.2. Design and considerations

The geometry of the device should allow for heating experiments in quantum point contacts and quantum dots in bilayer graphene. For this purpose, a dual-gate graphene field-effect transistor is made (see section 2.2). A cross-section of the device is shown in Fig. 12a. On top of the SiO_2, the gray area represents the graphene backgate. For this sample, the backgate was a bilayer graphene flake. On the backgate, a 20 nm thick hBN flake acts as a dielectric to gate the BLG, that is right on top. The BLG is protected by another hBN flake on top. The green areas represent the top gates and the blue box is contacting the BLG. Using the combined action of the top gate and back gate, an electric field can be created, which opens a bandgap in BLG. When using the split gates, at an appropriate voltage, the carrier density can locally be made zero, making it insulating. The point contact can be defined as the channel between the split gates still has a finite carrier density and if there is ballistic transport, the conductance is quantized. In this QPC, heating experiments will be done by applying a current through the heaters and measuring the Seebeck effect as described in section 2.5.1. In Fig. 12, the gray area is an Al_2O_3 layer to separate the finger gates from the top gates. This material was chosen because it is an insulator and high quality films can be grown by atomic layer deposition. On top, the finger gates are deposited. In Fig. 12b, the design of the device contacts is shown on top of an optical microscope image. In this map, the blue lines contact the BLG (except the blue figure in the top left, which is the backgate). The green lines are top gates, the continuous ones can also be used as heaters. There are also two split gates, separated by 100 nm. The separation needs to be small enough to define the QPC (meaning, the separation should be in the range of the Fermi wavelength, see section 2.3), but should still be feasible to produce with the EBPG5000. This separation is in line with for instance [12], where they were able to successfully define QPCs with a similar separation in split gates. The length of the split gates should be smaller than the mean free path of the electrons in the BLG. Although the mean free path of homogeneous ballistic BLG channels can reach up to several micrometers, inhomogeneous gating near the split gates may reduce this. Therefore, we decided to make the split gates length in the micrometer range as inhomogeneous gating near the split gates may reduce it. The yellow lines are finger gates (100 nm wide and separated with 100 nm). The separation of the finger gates is comparable with [12] [56] [75], where they successfully defined QDs and QPCs, respectively. The width is chosen as results of [12] suggest a 200 nm width to define QPCs and [56] have used 40 nm to define QDs. In [76], multiple QDs were defined between 200 nm wide finger gates. Furthermore, in [75], 100 nm wide finger gates

were used to define QDs. Thus, we decided to define our finger gates with a 100 nm width.

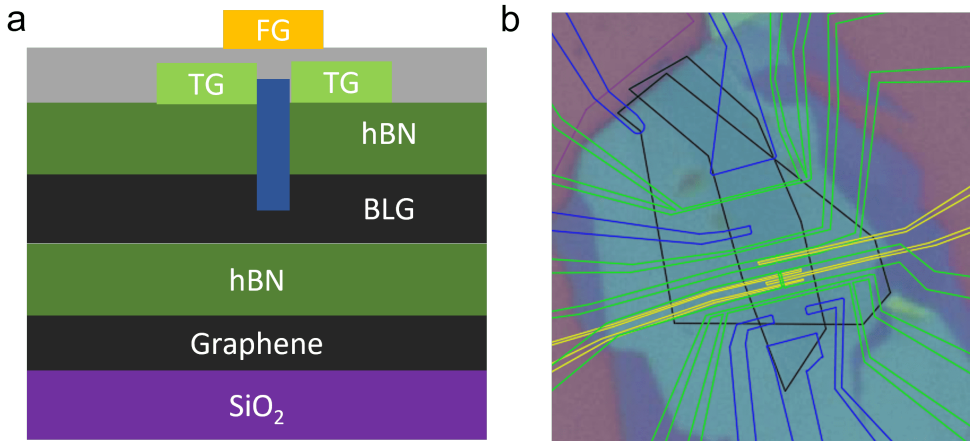

Figure 12: a) Side view of the stack. The middle black area represents the bilayer graphene (BLG) and the bottom layer the back gate. The green areas are the hexagonal boron nitride (hBN). The green areas on top are the top gates and the blue box is a contact. The gray area is the Al_2O_3, with finger gates (yellow) on top. b) Top view of the first finished device, captured by an optical microscope. The green lines in the middle are the split gates and heater elements. The blue lines are the contacts (etched into the BLG). The smaller area surrounded by a black continuous line is the graphene flake, the light green is the top layer of hBN and the dark green is the bottom layer of hBN. The larger area outlined by a black line represents the graphite backgate.

3.1.3. Contacting the device

First, the stack from Fig. 11 is spin-coated at 4500 rotations per minute (RPM) with 495A6 poly-methyl-methacrylate (PMMA) and then baked at 180 °C for 2 minutes. The process is repeated for another layer of 950A3 PMMA on top. As can be seen in Fig. 11, there is a large graphene flake around the stack, which needs to be removed to make space for the contacts. Electron-beam (e-beam) lithography is used to define a mask in concordance with the design of the etch mask (see Fig. 13a). The system used is the EBPG5k+ in the Kavli Nanolab. From here on, it will be referred to as EBL. Subsequently, the mask is developed by placing the sample in the cold developer H_20 IPA (1:3) for 90 seconds and then for 30 seconds in IPA. The etching is done with plasma reactive ion etching through a mixture of CHF_3 and O_2. The etching rate of this recipe was confirmed to be 30 nm/min in hBN by etching on a reference flake. Afterwards, the sample is placed in aceton to remove the PMMA. For the final result of this step, refer to Fig. 13b.

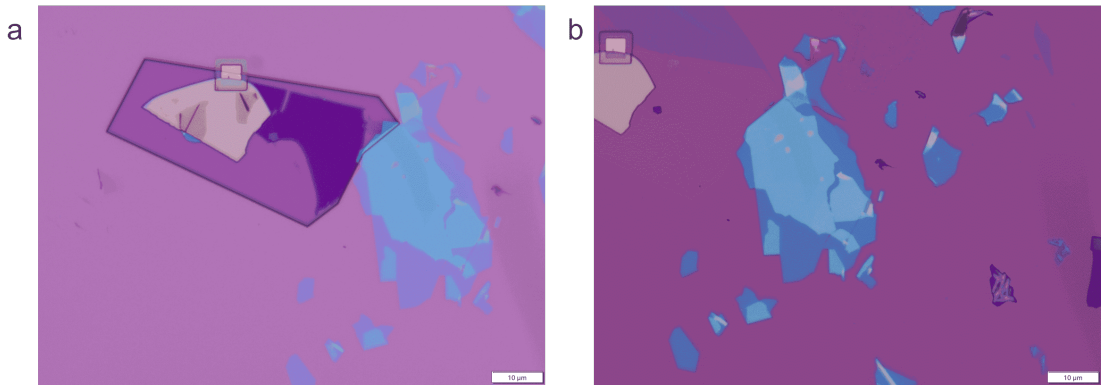

Figure 13: a) Optical image with 100x zoom of the EBL defined pattern around the large graphite flake. This serves as an etching mask to remove the flake and make space for the contacts. b) The result after CHF_3 etching and PMMA removal, showing that the flake is etched away, als an optical image with 100x zoom.

The next step is to define the large and small contacts, which contact the BLG (brown box in Fig. 3) and the backgate. Firstly, the sample is spincoated using the PMMA double layer defined above and then EBL used to define the patterns. Since the top hBN is 18 nm, around 45 seconds of etching was performed. Note that, since we do not want to connect the BLG with the back gate, we must over etch significantly less than 22 nm, the thickness of the lower hBN. To define the Ti/Au contacts, we used e-beam evaporation at high vacuum (10^{-7} Pa $< p < 10^{-6}$ Pa) to deposit 5 nm of titanium and 30 nm of gold. See Fig. 14 for the 5x (a) and 100x (b) optical images of the contacts.

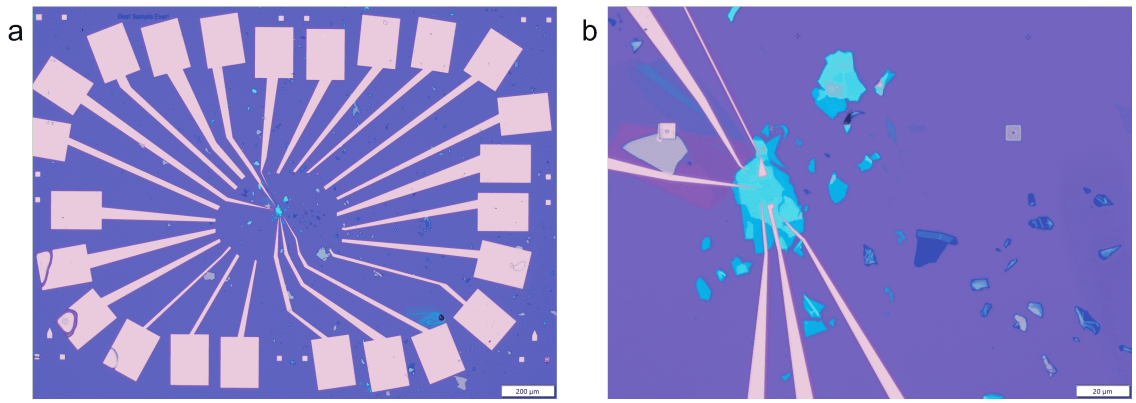

Figure 14: a) 5x optical image of the device, featuring the large Ti/Au contacs. b) 100x optical image of the contacts, showing the backgate and five contacts etched through the hBN to contact the BLG.

Then, the contact resistances were tested in a probe station. As a result, it showed that two contacts were not connected to the BLG. This indicates that the hBN was slightly thicker at specific areas. To fix this, an extra fabrication step was needed in which pads were designed around the contacts. Instead of etching for 45 s, we etched for 50 s to make sure we will contact the pads while preventing the full etching of the lower hBN flake. After this fabrication

step, electronic measurements confirmed contact with the BLG.

Due to the narrow spacings between split gates and small widths of the finger gates, dose tests of the split gates and finger gates were made to verify the feasibility of the design and determine the correct dose to accurately define the structures. The same procedure is used here as in fabricating the large contacts, however, reactive ion etching is instead executed with a mild O_2 plasma (for 10 s at 15 W) to remove the PMMA residues and improve adhesion to the hBN surface. Also, 25 nm of gold was deposited on 5 nm of titanium. From the AFM scans, the dose of 1450 uC/cm^2 was selected for both the split gates and finger gates. The next step in fabrication is producing the top gates (including split gates), as can be seen in Fig. 15. To produce the top gates, the stack was spin-coated with 496A6 and 950A3 PMMA, exposed using EBL at 1450uC/cm^2, followed by a mild O_2 DESCUM and then deposition of Ti/Au for 5 nm and 25 nm, respectively at the AJA-QT. The device with top gates is shown in Fig. 15. Tests at the probe station showed that the heaters were connected, the split gates well separated and all top gates not connected to the backgate and the BLG contacts.

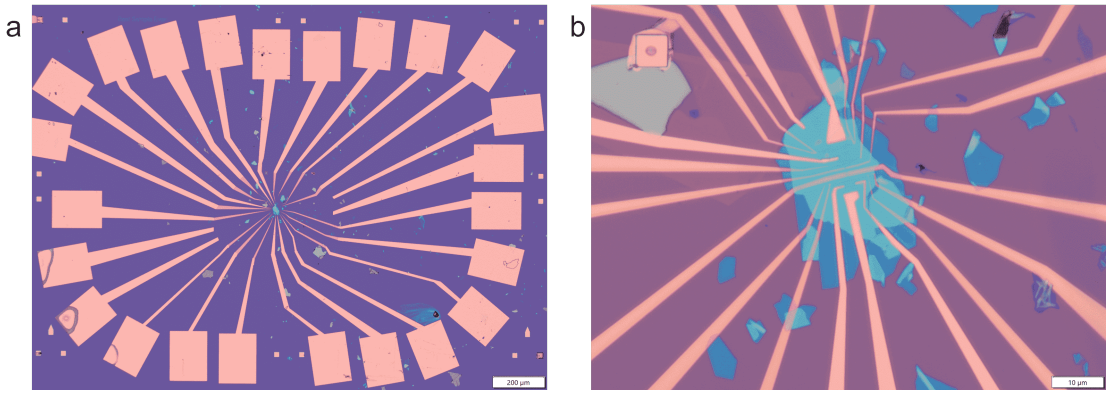

Figure 15: a) The 5x optical image of the device, featuring the large Ti/Au contacts and top gates. b) The 100x optical image of the contacts, showing the split gates and top gates, which will also be used as heaters in the experiments.

As shown in Fig. 3, the next layer consists of a 30 nm Al_2O_3 dielectric. However, as the dielectric, which is grown using atomic layer deposition, does not bond to hBN, the device is first functionalized with an O_2 plasma for 30 seconds. Before depositing on the device, first, a height calibration measurement was done on an empty Si wafer using an ellipsometer. Then, atomic layer deposition is executed at 150 °C on both the device and the test sample to deposit approximately 30 nm of Al_2O_3. After deposition, the total thickness of Al_2O_3 can be determined using the test sample. To contact the bond pads and the finger gates, the Al_2O_3 needs to be etched in the areas shown in Fig. 16. For this purpose, we do e-beam lithography to define an etch mask, followed by wet etching of the Al_2O_3 using an inorganic developer containing tetra-methyl ammonium hydroxide (MF21A). Before working on the device, the etch rate of MF21A is determined by etching the Al_2O_3 of the test sample. Since we have measured how much Al_2O_3 has been deposited, we can measure the height of this sample again after etching and thus determine how much has been etched in the given period of time. Since over-etching is not a problem (as the etch rate on hBN and Au is much smaller than the etch rate in Al_2O_3), we etched for 15 minutes on the device after defining the windows using EBL. See Fig. 16 for

a 5x optical image featuring the EBL etch mask (blue/purple color). The windows on the bond pads are not visible.

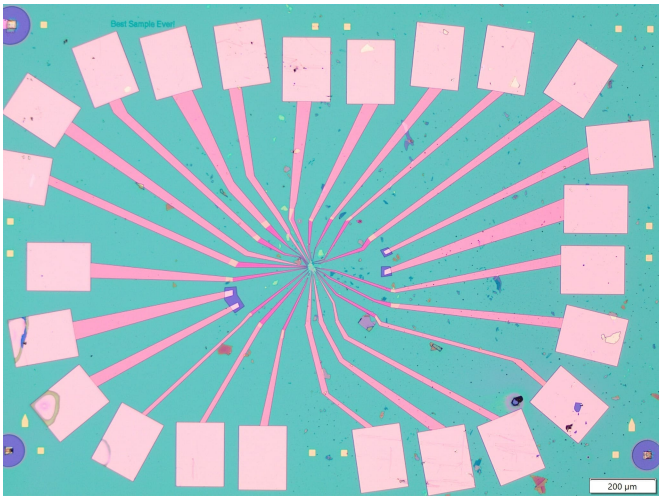

Figure 16: The 5x optical image of the device after ALD, showing the windows on the contacts where the finger gates will be contacted (blue/purple color). The windows on the bond pads are not visible. The greenish color of the device is the result of the Al_2O_3.

The finger gates are defined on top of the dielectric layer with the same recipe as for the top gates. In Fig. 17, a top overview of the final device is shown.

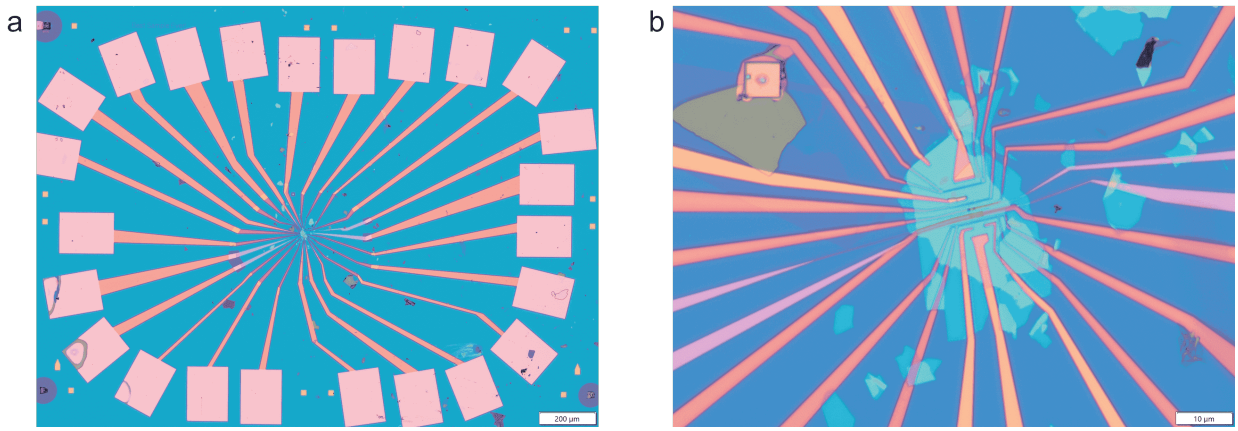

Figure 17: a) The 5x optical image of the final device. b) The 100x optical image of the final device, including the four finger gates.

In Fig. 18, an AFM scan of the final device is shown. It was taken after the measurements have been done, in order not to potentially damage the device.

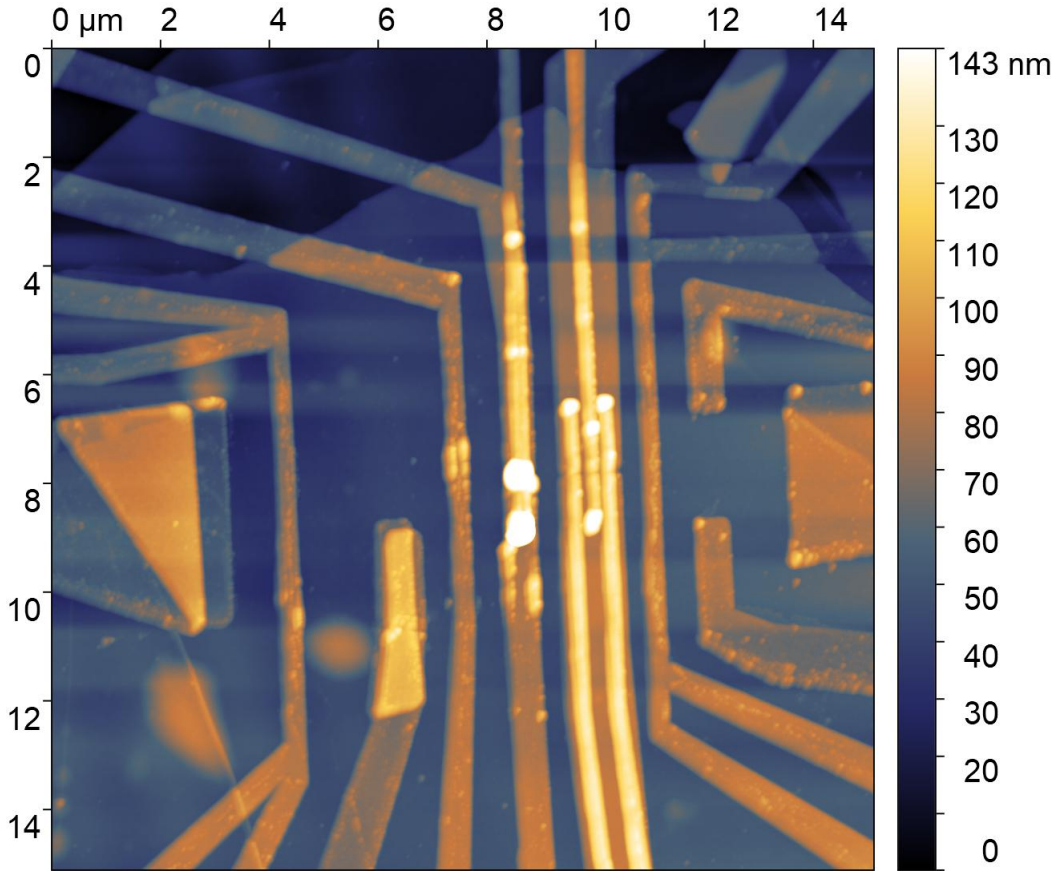

Figure 18: a) An AFM scan of the device, after measurements.

3.2. Measurements

To perform electronic measurements, the sample needs to be connected to a socket. For this purpose, we glue it on a chip carrier and use Au wires to bond the device pads with the chip carrier connections. Then, this chip carrier with the device is placed inside a vacuum chamber. The sample is connected thermally to a small chamber (called 1 K pot) which has a small aperture controlled by a needle valve. This chamber is also connected to a pump that can reduce the Helium pressure in the chamber, allowing the temperature around the device to drop to as low as 1 K (hence the name). The device is connected to a dewar with liquid He, which enters the 1 K pot through the needle valve aperture and contains a superconducting magnet capable of applying magnetic fields up to 8 Tesla. Furthermore, the large helium cryostat contains helium level probe and the temperature readout is connected to the cold finger. The sample holder has 32 connections which allows us to apply and measure voltages across gates of the device. The connections to the socket are connected to two Fisher connectors, that are connected to a matrix rack which allows us to safely connect and disconnect the sample. Furthermore, the IVVY-DAC-rack allows us to source and measure currents and voltages. It allows one to use external outputs and inputs, which we exploit by connecting a Lock-in system (SRS 830). The Lockin system can be used to tune the current's frequency, harmonic, amplitude and phase. Peltier heating can be detected by tuning the Lock-in to the first harmonic of the AC current (since $\dot{Q} \propto I$, see Eq. 12). Similarly, Joule heating can be monitored by tuning the Lock-in to the second harmonic of the AC current (see Eq. 13) to calculate the

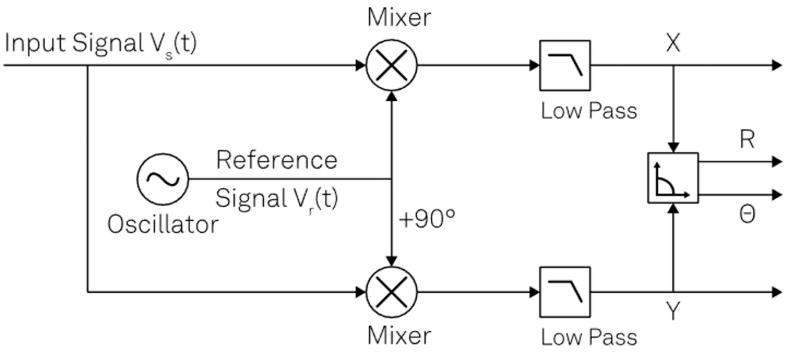

Figure 19: A simplified schematic of the working principle of a Lock-in amplifier. The input signal V_s is duplicated and both are multiplied with a reference signal V_r, generated from the internal oscillator of the Lock-in. One copy is multiplied with V_r containing the same phase as V_s whereby the in-phase component (X-component) is generated, and the other copy is multiplied with V_r having a 90 degrees phase shift to create the quadrature signal (Y-component). After multiplying with the reference signal, both functions are passed through a low pass filter to remove any other frequencies and converted into polar coordinates to obtain amplitude R and phase θ of the signals. Obtained from [77].

Seebeck effect. The system is controlled through Python scripts. Likewise, the processing and analysis of the acquired data is done in Python.

A schematic of the Lock-in amplifier is shown in Fig. 19. The Lock-in is able to extract very small signals in noisy environments. The operation relies on the orthogonality of sinusoidal functions. When multiplying two sinusoidal functions with frequencies f_1 and f_2, with $f_1 \neq f_2$, and integrated over time T ($T \gg T_1 \wedge T \gg T_2$, with $T_i = 1/f_i$ the period of function i), this results in zero. If $f_1 = f_2$ and $\psi_1 = \psi_2$ (equal phases), the average value equals half of the product of the amplitudes if integrated over a large enough T. If $f_1 = f_2$ but $\psi_1 \neq \psi_2$ the product is also attenuated (since the sine is orthogonal to the cosine). The input signal V_s can generally be described by:

$$V_s = A \sin(\omega_s t + \psi), \tag{14}$$

in which A the amplitude of the input voltage V_s, $\omega_s = 2\pi f_s$ the angular frequency (units: radians per second), t the time (seconds), and ψ the phase (radians). The input voltage is first filtered with a band pass filter and then amplified with a low noise amplifier (not shown) and split into two copies. Each copy is multiplied with a reference signal V_r (provided from the internal oscillator). One copy is multiplied with V_r containing the same phase as V_s, generating the so-called in-phase component (commonly denoted as X); and the other copy is multiplied with V_r shifted 90 degrees such that the so-called quadrature signal is generated (the Y component). In Fig. 19, the in-phase component is the upper branch and the quadrature component the lower branch. After multiplying with the reference signal, both functions are passed through a low pass filter to remove noise and finally through an output amplifier (not shown). The amplitude R and phase $\theta = \arctan(Y/X)$ of the signal are determined by transforming X and Y from Cartesian coordinates to polar coordinates. Since multiplying two

sinusoidal functions with the same ω and ψ is nonzero, we expect the X component to yield nonzero values. However, since multiplying two sinusoidal functions with the same ω but different ψ is attenuated, the amplitude of the Y component should be much smaller (near zero) than the amplitude of the X component. In this thesis, the sample is excited with a signal that is proportional to the reference signal, which is why V_{s} is having a component at the reference frequency and phase.

In some cases, the measured signal is proportional to higher powers of the current I_0. In particular, if $V_{\mathrm{s}} \sim I^2$:

$$(\frac{I}{I_0})^2 = \sin(\omega t)^2 = \frac{1}{2}(1 - \cos(2\omega)). \tag{15}$$

Therefore, when multiplying with a sinusoidal V_{r}, the integral over T will be zero (as the sine and cosine are orthogonal). However, when multiplying with the 90 degrees shifted V_{r} (which will also be a cosine), the integral over T will be nonzero. We expect the second harmonic X-component to be attenuated and the Y-component to be dominating. In the third harmonic, the AC source can be simplified into:

$$(\frac{I}{I_0})^3 = \sin(\omega t)^3 = \frac{1}{4}(3\sin(\omega t) - \sin(3\omega t)). \tag{16}$$

Since the third harmonic only contains terms with $\sin(\omega t)$, we expect the X-component to be much larger than the Y-component of the output voltages processed by the Lock-in system. In the fourth harmonic, the AC source can be written as:

$$(\frac{I}{I_0})^4 = \frac{1}{4}(1 - 2\cos(2\omega t) + \frac{1}{2}(1 + \cos(4\omega t))). \tag{17}$$

The expression of the fourth harmonic only contain terms with $\cos(\omega t)$, and therefore, we expect the Y-component to be much larger than the X-component.

In this thesis, we will also perform a combination of two-terminal, three-terminal and four-terminal measurements to characterize the device. The two-terminal measurement, sometimes called two-probe measurement, contacts the device, as the name suggests, on two leads. The sample is represented by resistors in Fig. 20a and b with the a) two and three-terminal and b) a four-terminal measurement circuit. The red lines are the two-terminal measurement, the combination of V_1 and V_3 form a three-terminal measurement. In Fig 20b, a four-terminal measurement is drawn.

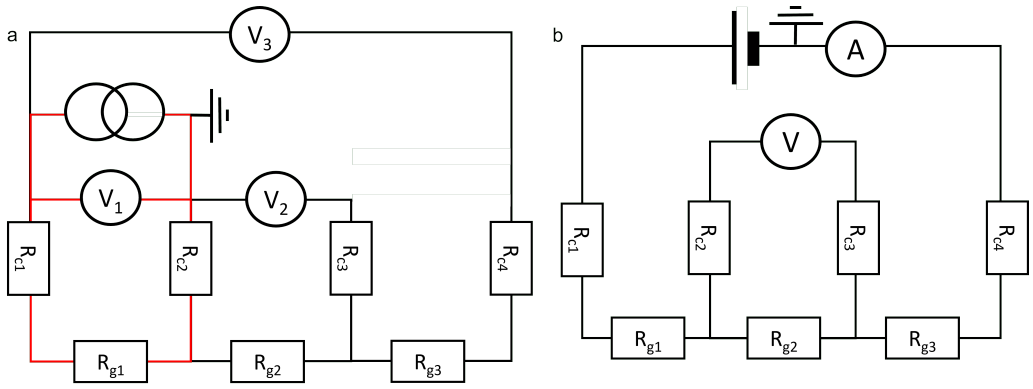

Figure 20: A schematic overview of the two-terminal, three-terminal and four-terminal measurement circuits. The R_{g} symbolizes the resistance of the BLG between the contacts. R_{ci} is the resistance of contact i. a) The red lines indicates a two-terminal measurement circuit between contacts c1 and c2 (with voltage meter V_1). A three-terminal circuit is drawn using V_1 and V_3. b) Four terminal measurement circuit.

Using Fig. 20 and Ohm's law, we can conclude why a four-terminal measurement is more accurate than a two-terminal measurement to determine the BLG channel resistance. Suppose that the current source generates a current I. Then the voltage measured in V_1, V_2 and V_3 can be written as:

$$V_1 = I(R_{\mathrm{c1}} + R_{\mathrm{g1}} + R_{\mathrm{c2}}). \tag{18}$$

$$V_2 = IR_{\mathrm{c2}}. \tag{19}$$

$$V_3 = I(R_{\mathrm{c1}} + R_{\mathrm{g1}}). \tag{20}$$

From Eq. 18, it becomes clear that in a two-terminal measurement, we also measure the resistance of the contacts - besides measuring the resistance of the BLG. Since the resistance of the contacts is an unknown but significant value, R_{g1} cannot be measured reliably. The current does not go through other parts of the BLG. Hence, with voltage meter V_2 (see Eq. 19), only R_{c2} is can be determined. For the same reason, both R_{c1} and R_{g1} can be determined with V_3 described in Eq. 20. When doing a three-terminal measurement, we have can subtract Eq. 18 from Eq. 20 to determine R_{c2}. This means the three-terminal measurement better approximates the resistance of the BLG R_g, but still contains the unknown R_{c1}, which causes systematic measurement errors when characterizing R_{g} (especially when $R_{\mathrm{g}} < R_{\mathrm{c}}$). A solution is the four-terminal measurement, shown in Fig. 20b. Four-terminal sensing separates current carrying and voltage sensing electrodes. Assuming that the voltage source generates a voltage V_{s}, and that the Ampere meter reads current I the voltage drops according to the following.

$$V_s = R_{\mathrm{c1}}I + R_{\mathrm{g1}}I + R_{\mathrm{g2}}I + R_{\mathrm{g3}}I. \tag{21}$$

As no current will flow into the voltage meter (assuming a perfect voltage meter with infinite resistance), the voltage meter V will read:

$$V = R_{\mathrm{g2}} I. \tag{22}$$

Since both V (from the voltage meter) and I (from the Ampere meter) are known, the resistance of the BLG between the two contacts can be determined (R_{g2}).

4. Results

All measurements described in this chapter are done at $T = 1.8$ K, unless specified otherwise. In Fig. 21, a schematic of the contacts of the device is shown. This helps in discussing which gates and contacts are connected. As can be seen, the split gates are purple with yellow corresponding finger gates. The other top gates are represented by the green shapes. Furthermore, the contacts etched into the BLG are dark blue. The back gate is not shown here, but can be seen in Fig. 17. When showing which contacts are connected, the connected contacts will be colored.

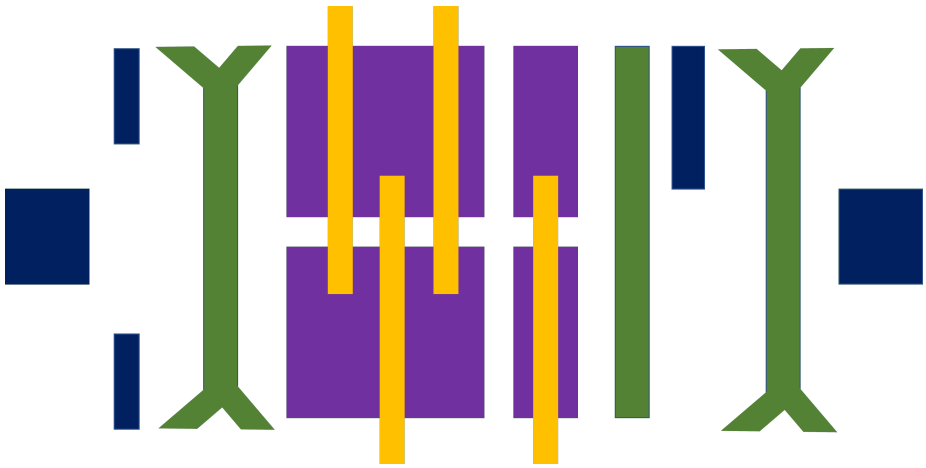

Figure 21: Schematic of the contacts of the device. The blue contacts are connected to the BLG. The purple contacts represent the large (left) and small (right) set of split gates. The green contacts are the other top gates on top of the hBN. The finger gates are represented by the yellow rectangles.

First, a 4-terminal measurement with back gate sweep is done to determine the resistance R of the BLG for -3 V $\leq V_{\mathrm{bg}} \leq 3$ V, see Fig. 22a for the circuit. A 4-terminal measurement is done such that the contact resistances are not measured, and only the resistance of BLG is returned (see section 3.2). Besides sweeping the back gate, an AC bias of 1 μA is applied between the outer dark blue contacts in Fig. 22a, which contact the BLG, to measure the resistance. Meanwhile, the voltage difference between is monitored between the two other blue contacts through the Lock-in. The 4-terminal-resistance ($R_{4\mathrm{p}}$) of the BLG can then be determined through Ohm's law, using the measured voltage V_x and the bias current. It is expected for $R_{4\mathrm{p}}$ to peak at the charge neutrality point (see section 2.1.2) as the number of carriers available for transport is minimal (see the Drude model and formula for carrier density as explained in section 2.1.2). The measurement circuit is drawn in Fig. 22a. In Fig. 22b, the data is visualized in a simple plot, with $R_{4\mathrm{p}}$ the four-terminal resistance on the y-axis, which is the BLG resistance as shown in Section 3.2. On the x-axis, the various values of the back gate are plotted. At around $V_{\mathrm{bg}} = -2$ V, a significant peak in resistivity can be seen. This corresponds with the charge neutrality point of this device.

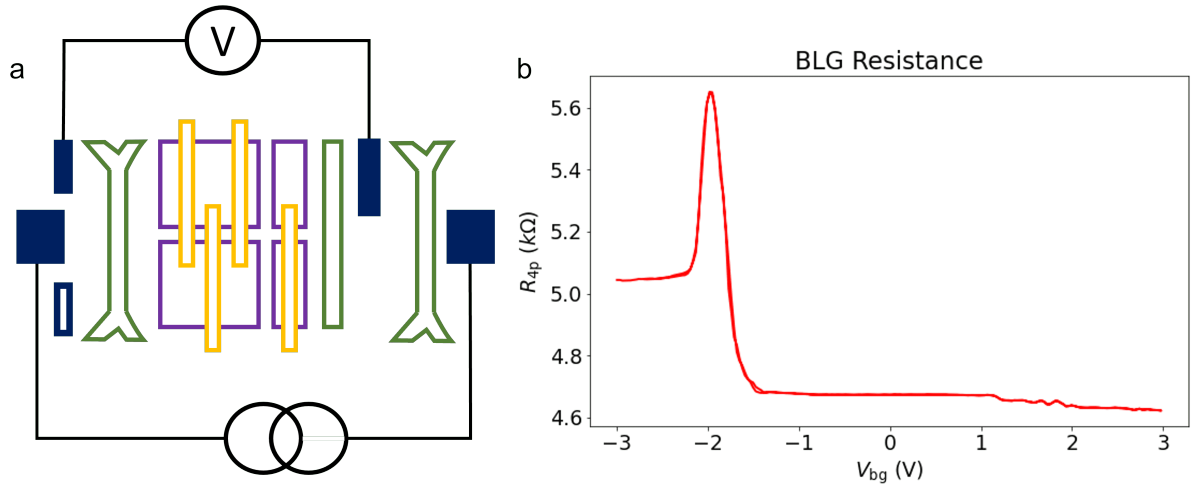

Figure 22: a) The circuit of the four-terminal measurement. The voltage meter is connected between the dark blue colored contacts in the BLG. The current sources $1\ \mu$A between two different contacts, making it a four-point measurement. b) The measurement result, featuring R_{4p} (BLG resistance) on the y-axis and values of the back gate sweep on the x-axis. The significant peak in resistivity around $V_{bg} = -2$ V corresponds with the charge neutrality point of this device.

4.1. Opening a bandgap

To experimentally show that a bandgap can be opened under an electric field, voltages on the back gate and various top gates are applied. For each value of the back gate voltage, the top gate voltages are swept. A bias current is set and the voltage difference between contacts in the BLG is monitored (creating a 3D plot). The resistance of the BLG can then be calculated using Ohm's law. In homogeneous BLG, we expect to see the resistance go as $1/n$ far from the CNP and saturate at a value of several kΩs which increases as the displacement field increases (see section 2.2). These indicate the charge neutrality point of the outer regions of the BLG not affected by the top gate voltage and the charge neutrality point underneath the top gate, respectively (see section 2.2, and Fig. 4).

For the four-terminal measurement in Fig. 23a, an AC bias current of $1\ \mu$A is applied between the outer contacts in the BLG, while monitoring the voltage difference between two other contacts in the BLG. Moreover, for each value of the back gate voltage V_{bg} ($-4\,\text{V} \leq V_{bg} \leq 4\,\text{V}$), the voltage V_{sg} on the small split gates is swept from $-5\,\text{V}$ to $5\,\text{V}$. The voltage difference is then converted into resistance through Ohm's law and is signified by the color scale. In Fig. 23b, the resulting 3D plot is shown. As expected, there is a significant increase in resistivity around $V_{bg} = -2$ V, as demonstrated in Fig. 22, corresponding with the charge neutrality point (for the parts of the BLG not affected by V_{tg}). However, instead of a diagonal line having a resistivity which increases with $|V_{bg}|$ (as predicted in section 2.2), the resistivity increases in a step-wise fashion. This indicates that the back gate voltage is not changing the carrier density constantly. Another observation is that R_{4p} takes on values between $460\ \Omega$ and $560\ \Omega$ - which are approximately 10x smaller than the ones measured in Fig. 22 (setting $V_{tg} = 0$ V in Fig. 23).

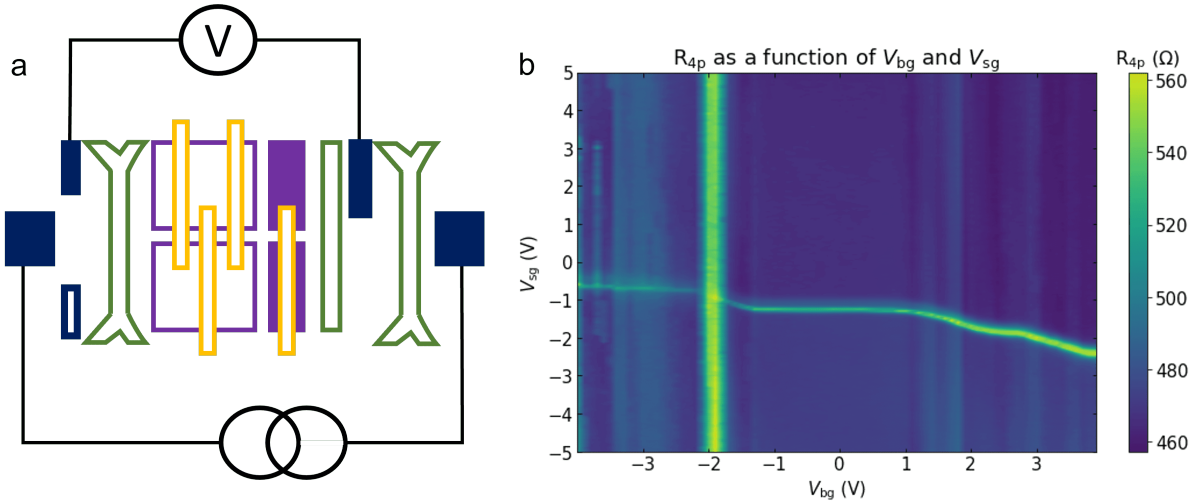

Figure 23: a) Four-terminal measurement circuit. The voltage meter is connected between two contacts in the BLG. The current sources $1\ \mu$A between two contacts in the BLG. b) The resulting 3D plot, with the back gate voltages and the split gate voltages. The color signifies the resistance measured using the Lock-in system. As expected, there is a significant increase in resistance around $V_{\text{bg}} = -2$ V. However, instead of a diagonal line having large resistivity, the resistivity seems to have a step-like behavior in this sample.

The smaller values for R at $V_{\text{tg}} = 0$ V can, at least partly, be explained when converting the values of R to R_{sq}:

$$R_{\text{sq}} = R\frac{W}{L}, \tag{23}$$

in which R_{sq} is the square resistance (units: Ω), W the width of the measured sample (in this case: $4\ \mu$m) and L the separation between the voltage probes (around $7\ \mu$m) - which results in a factor of 0.57. In Fig. 24, the R_{sq} for the back gate sweep and for measurement in Fig. 23 are shown, respectively. As can be seen, the peak in Fig. 24b is cut-off, hinting that too little points are available to fully characterize the trace. Furthermore, this difference in resistivity might hint at a secondary channel being formed in Fig. 22 (as an extra resistance in parallel decreases overall resistance). According to Ohm's law for parallel resistances, this resistance should equal:

$$R_{\text{ch}} = \frac{R_{\text{bgsweep}}R_{\text{g}}}{-R_{\text{g}} + R_{\text{bgsweep}}}. \tag{24}$$

In this equation, R_{ch} is R_{sq} of the hypothetical extra channel, R_{g} the R_{sq} of the measured graphene from Fig. 23 and R_{bgsweep} the R_{sq} of Fig. 22. From this, the channel resistance should be in the order of $1.1R_{\text{g}} \approx 315\ \Omega \pm 28\ \Omega$.

To further investigate the step-like voltage response, various top gate geometries in combination with the back gate have been used. Since at this time, the phase of the Lock-in started to deviate largely from zero, a two-terminal measurement was performed on the same small split gates. In Fig. 25a, the measurement circuit is drawn and the used contacts are colored. Both the voltage meter as the AC source are connected between the same contacts in the BLG, to apply $I_{\text{bias}} = 100$ nA. The results are shown in Fig. 25b. The values for $R_{2\text{p}}$ are significantly

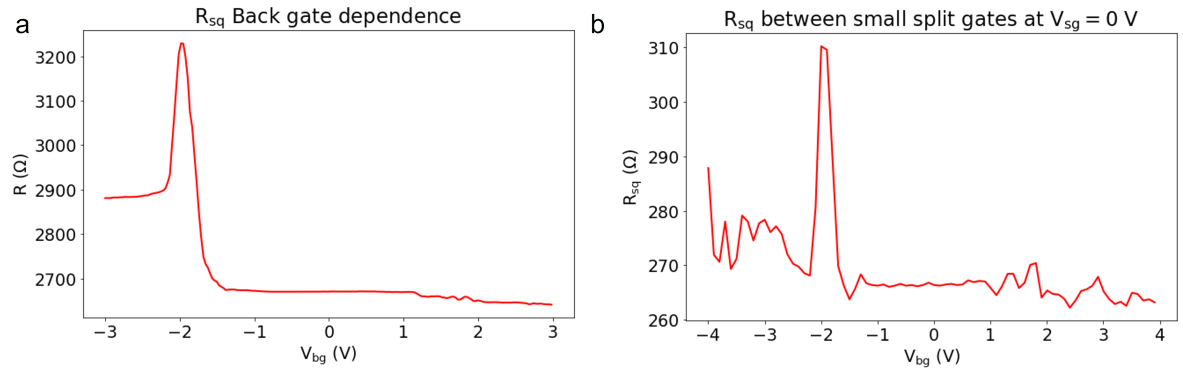

Figure 24: a) R_{sq} for back gate dependence as shown in Fig. 22. This is done by converting the values of R into R_{sq} by using Eq. 23, with $W = 4$ μm and $L = 7$ μm, corresponding with the width and length of the gated region. b) R_{sq} for measurement as shown in Fig. 23. In this case, the same values for W and L are used.

larger than for $R_{4\mathrm{p}}$, which makes sense because $R_{2\mathrm{p}}$ also measured the contact resistances (see section 3.2). Since we have also measured the resistance using a four-terminal measurement, the sum of these contact resistances can be determined and are approximately equal to the values shown in the $R_{2\mathrm{p}}$ results of Fig. 25. The contact resistances are well above 15 kΩ, significantly larger than the previous results reported in such etch-defined contacts.

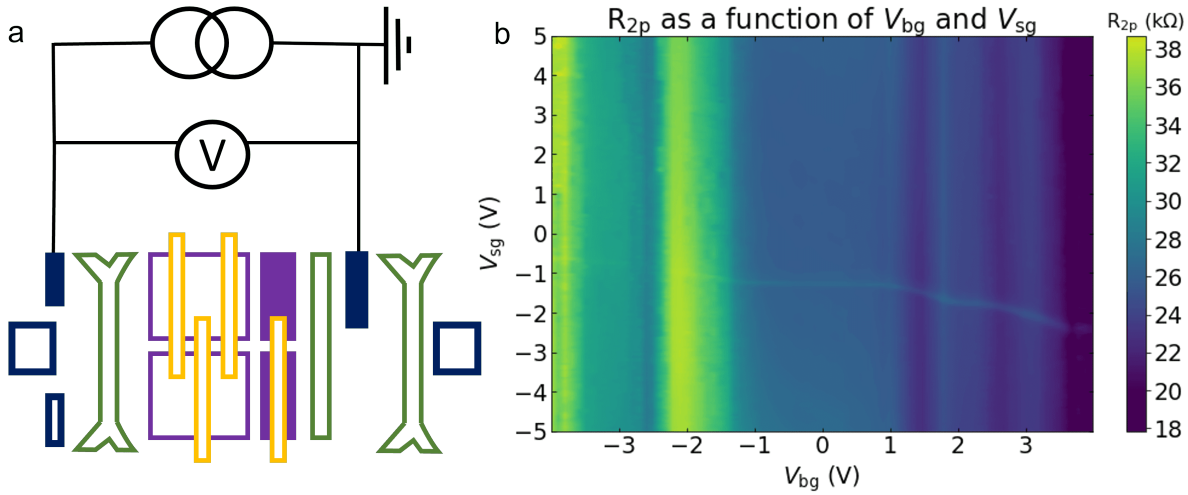

Figure 25: a) The circuit of the two-terminal measurement. The voltage meter is connected between two blue colored contacts in the BLG. The current sources 1 μA between the same contact (a two-terminal measurement). We swept the small split gates (purple, colored) voltages V_{sg} between -5 V and 5 V, for each value of V_{bg} between -4 V and 4 V. b) The resulting 3D plot, with the back gate voltages and the split gate voltages. The color signifies the resistivity measured using the Lock-in system.

In Fig. 26a, a heater is connected and used as a top gate. Also here, an AC bias of $I_{\mathrm{bias}} = 100$ nA was set in two contacts in the BLG, while the voltage difference was monitored. The top gate is swept between -5 V and 5 V for back gate voltages between -4 V and 4 V. The results are shown in Fig. 26b, consistent with Fig. 25.

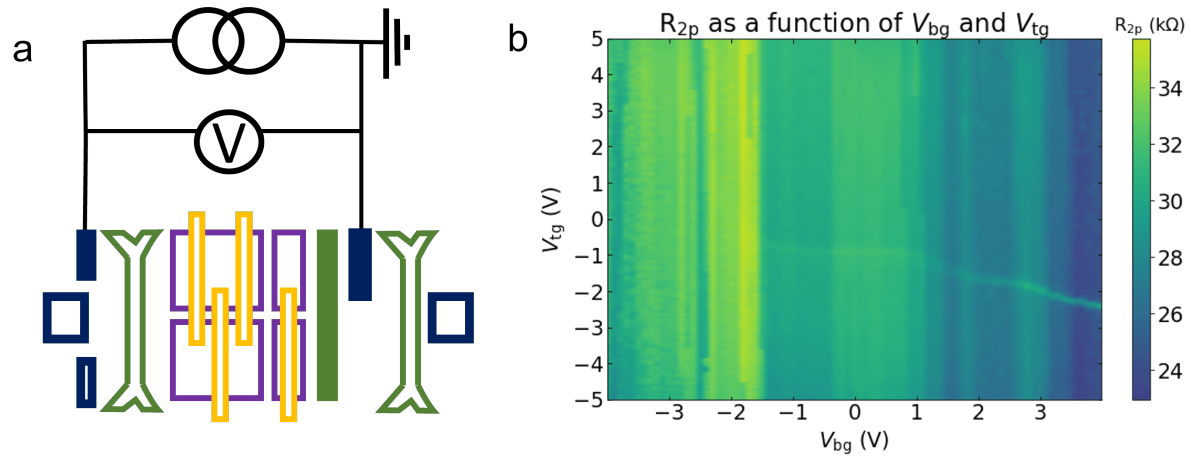

Figure 26: a) Two-terminal resistance measurement circuit. Here, we swept a top gate (green, colored) and applied $I_{\text{bias}} = 100$ nA between the dark blue filled contacts (contacting the BLG). The measured voltage response is then converted into resistance using Ohm's law. b) The result of the two-terminal resistance measurement according to a). The measurement agrees with previous measurements in their resistance peaks around $V_{\text{bg}} = -2$ V and step-like behavior in resistance.

In Fig. 27a, the larger split gates were connected in a two-terminal resistance measurement. An AC bias of 100 nA was used. The split gates were swept between -4 V and 4 V, while sweeping the back gate between -3 V and 3 V. Based on the difference between this measurement, which is a two probe measurement, and the measurement described in Fig. 28, the contact resistances can be retrieved. These are in the same order of magnitude as the contact resistances determined between Fig. 25 and Fig. 23.

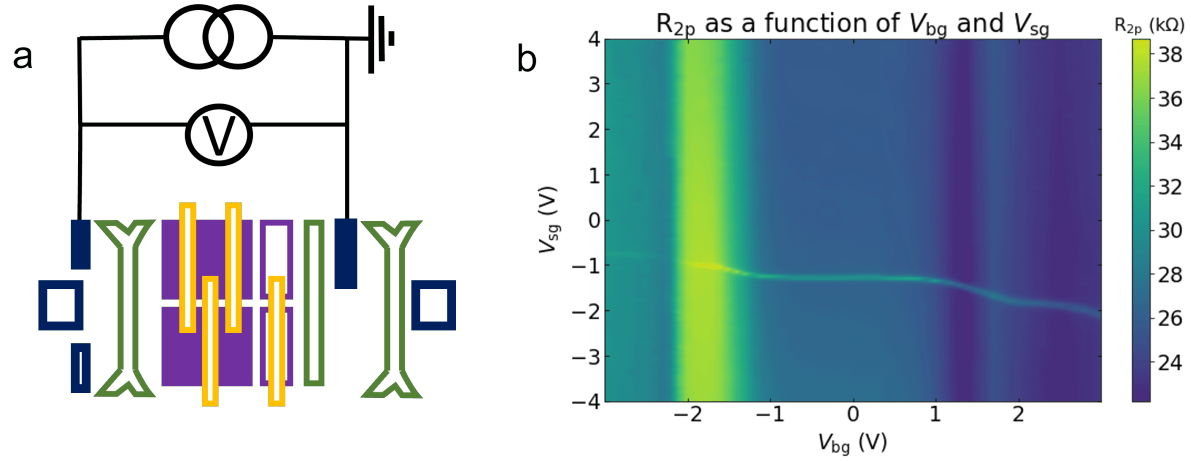

Figure 27: a) Two-terminal resistance measurement according to Fig. 25. Here, we swept the large split gates (filled with purple) and applied $I_{\text{bias}} = 100$ nA between the two blue colored contacts in the BLG. b) The resulting 3D plot, agreeing with previous resistance measurements.

Moreover, in Fig. 28, the larger split gates (colored with purple) were connected for another 4-probe measurement as described in Fig. 28a using a voltage source instead of a current

source. The voltage meter is connected between the two outer dark blue contacts, which are etched into the BLG. The voltage source and Ampère meter are both connected to the other set of blue colored contacts. In this measurement, a voltage of $100\ \mu$V was applied with this voltage source. The split gate voltage was swept ($-3\,\mathrm{V} \leq V_{\mathrm{sg}} \leq 3\,\mathrm{V}$) for values of the back gate ranging between $-3\,\mathrm{V} \leq V_{\mathrm{bg}} \leq 3\,\mathrm{V}$. The results are shown in Fig. 28b. The values for $R_{4\mathrm{p}}$ range between $3.6\ \mathrm{k}\Omega$ and $0.25\ \mathrm{k}\Omega$.

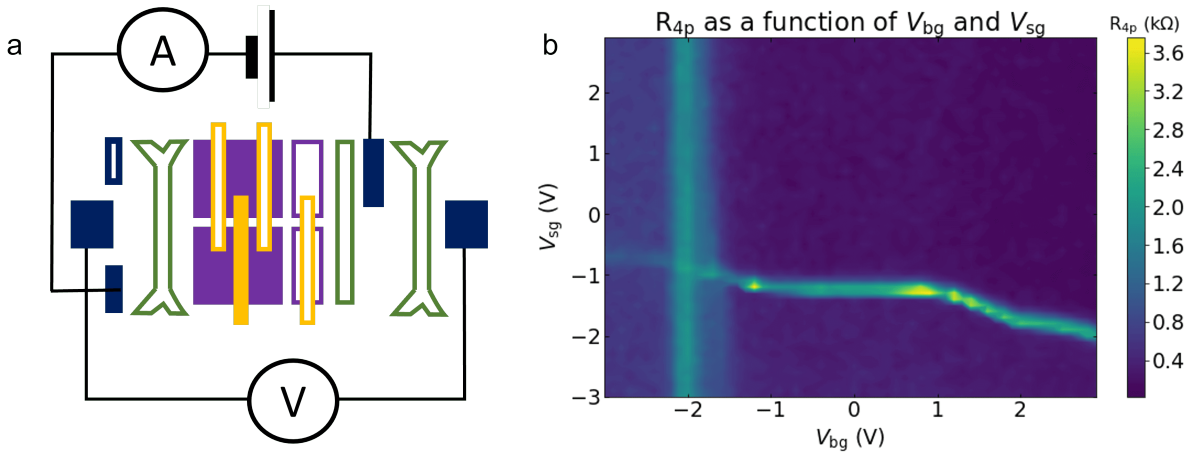

Figure 28: a) The circuit of the four-terminal measurement. The voltage meter is connected between the two outer contacts in the BLG (dark blue). Between the other set of blue colored contacts, a voltage of $100\ \mu$V is applied and a current is measured. Furthermore, the split gates (purple) were connected and swept with voltages between -3 V and 3 V for each value of the back gate voltage V_{bg} between -3 V and 3 V. b) The resulting 3D plot, with the back gate voltages and the split gate voltages. The color signifies the resistance (calculated by measuring the voltage response and current of the Lock-in system).

The resistance measured in Fig. 28 at $V_{\mathrm{tg}} = 0$ V can be converted into R_{sq} to compare it to the R_{sq} of earlier measurements (see Fig. 24a), see Fig. 29. It is expected that the shape of this graph is similar to Fig. 24b, especially at low values of R_{sq}, as there were not enough points to complete characterize the higher peak. As hypothesized, the small values are around $200\ \Omega$, and the peak reaches into the $1\ k\Omega$ regime. Based on this measurement, the resistance of the hypothetically parallel channel in the back gate sweep of Fig. 24a should be between $60\ \Omega$ and $1800\ \Omega$. In Fig. 29b, for each value of V_{bg}, the maximum R_{sq} is taken from the split gate sweep $-3\ \mathrm{V} \leq V_{\mathrm{sg}} \leq 3$ V. As V_{tg} is nonzero, we can approximate through the sum of R_{sq} in the top gated region (with length L_{tg}), and R_{sq} in the rest of the sample (dimensions: $L - L_{\mathrm{tg}}$ and W, if we assume diffusion. Using $R_{\mathrm{sq}} = RW/L$ and $R = R_t + R_{\mathrm{nt}}$, this simplifies to:

$$R_{\mathrm{sq,tot}} = R_{\mathrm{sq,nt}}\left(\frac{L - L_{\mathrm{tg}}}{L}\right) + R_{\mathrm{sq,t}}\left(\frac{L_{\mathrm{tg}}}{W}\right). \tag{25}$$

In this formula, $R_{\mathrm{sq,tot}}$ is the R_{sq} of the total device, $R_{\mathrm{sq,nt}}$ is R_{sq} corresponding to the area of the sample unaffected by top gating, $R_{\mathrm{sq,t}}$ is R_{sq} corresponding to the area of the sample affected by top gating, L_{tg} is the length of the top gated area, L is the length of the channel and W is the width of the channel. As can be seen in Fig. 29b, there is an increasing trend in R_{sq} (corresponding to $R_{\mathrm{sq,tot}}$ in Eq. 25) as V_{bg} increases. This trend indicates that there is indeed a bandgap opening in this measurement.

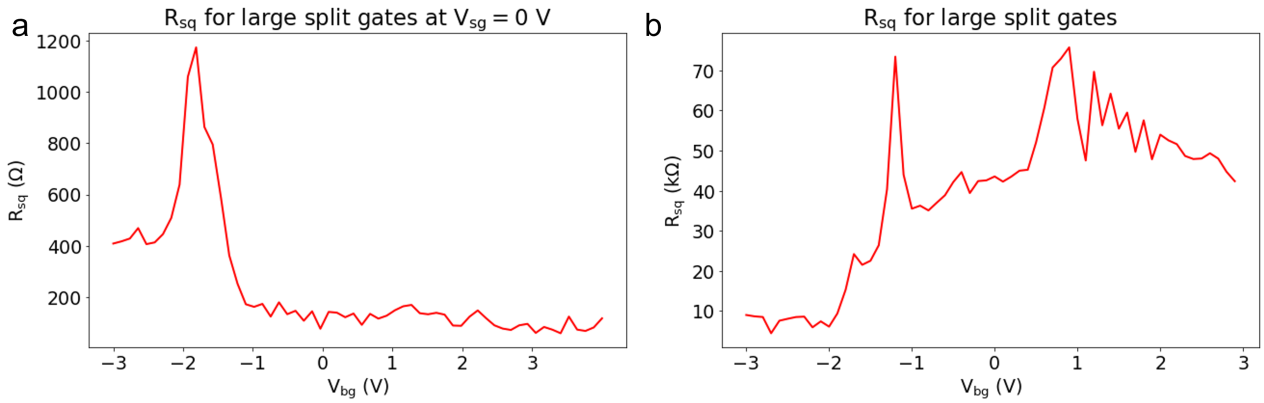

Figure 29: a) R_{sq} for the resistances taken in Fig. 28. b) Maximum values for R_{sq} for each value of V_{bg} (selected from the various V_{sg}). The upward trend indicates that a bandgap is opening in this measurement.

Using the same configuration as described in Fig. 28, the source-drain current was measured. In Fig. 30a, the back gate leakage current is displayed from the setup of Fig. 25. This is done in preparation of defining the quantum point contact and quantum dot, as there is a trade-off between a higher back gate (which results in a higher displacement field) and consequently a higher leakage current (which is ideally kept < 10 nA) to guarantee that the applied voltage is transferred to the gate.

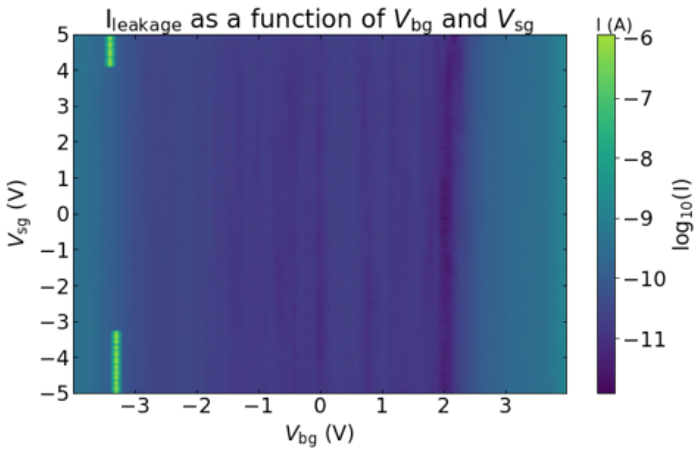

Figure 30: The measured leakage current during the two-terminal measurement described in Fig. 25. Here, we swept the large split gates (see Fig. 28a) and applied $I_{\mathrm{bias}} = 100$ nA. The current is on a log scale. As can be seen, the leakage current is mostly in the (sub) nA range, and increases fast for $V_{\mathrm{bg}} > 3$ V into the μA regime. The outliers at $V_{\mathrm{bg}} = -3$ V are likely not real as the leakage decreases again for lower V_{bg}.

Tuning V_{bg} seems to have no effect on the resistance for -1 V $\leq V_{\mathrm{bg}} \leq 1$ V, $V_{\mathrm{bg}} \leq -2$ V, 2 V $\leq V_{\mathrm{bg}} \leq 2.75$ V and $V_{\mathrm{bg}} \geq 4$ V. This feature is reproducible for different top gates and split gates (See Fig. 23, Fig. 25, Fig. 26, Fig. 27 and Fig. 28), and thus is a feature of the sample. As can be seen in equation 4, we expect a linear change of the CNP position with V_{bg}: for a lower value of back gate voltage, we expect a higher top gate voltage to tune towards the charge

neutrality point. This behavior indicates that, for the aforementioned ranges, the voltage applied to the back gate does not translate into a bigger electric field on the BLG. The electric field induced by the back gate is being screened by a layer of charges somewhere between the back gate and the bilayer graphene. The origin of this layer of charges remains unknown.

The estimation of the Seebeck coefficient in BLG is obtained in Fig. 31, based on the resistances of the back gate sweep (Fig. 22). The shape and range are in agreement with the modelling of the Seebeck coefficient described in Fig. 8.

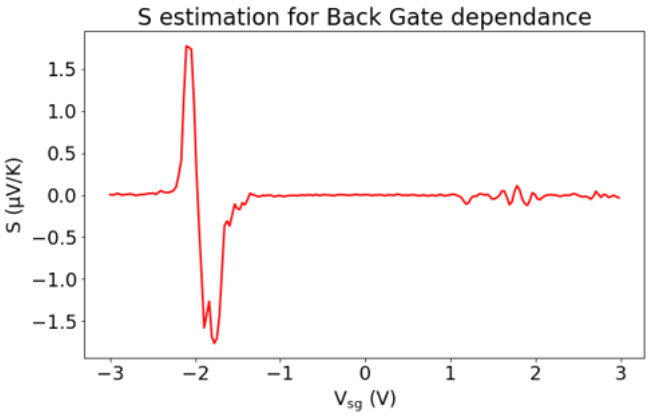

Figure 31: The Seebeck coefficient estimate based on the back gate sweep taken in Fig. 22. The shape and range are in agreement with the modelling of the Seebeck coefficient described in Fig. 8.

4.2. Tuning into quantum dot

Then, we attempted to deplete the channels under the two sets of split gates. This was done through setting the back gate voltage at a value which results in maximum electric field while maintaining a small leakage current (idealistically: < 1 nA). According to Fig. 23-28, we can see that tuning V_{bg} did not effect the resistivity of the BLG for $-1\ \mathrm{V} \leq V_{\mathrm{bg}} \leq 1\ \mathrm{V}$, $V_{\mathrm{bg}} \leq -2\ \mathrm{V}$, $2\ \mathrm{V} \leq V_{\mathrm{bg}} \leq 2.75\ \mathrm{V}$ and $V_{\mathrm{bg}} \geq 4\ \mathrm{V}$. Also, the back gate leakage current for V_{bg} greater than -3 V or 3 V too high to be considered safe. Therefore, we define a QD in this sample around $V_{\mathrm{bg}} = 3$ V. At this value for V_{bg}, a displacement field of approximately 0.1 V/nm was achieved (See Appendix), and therefore a bandgap of 8 ± 2 meV is estimated to open [49]. Fig. 30a illustrates that the back gate leakage current is in the nA range for $V_{\mathrm{bg}} = 3$ V. Although the electric field might be stronger at $V_{\mathrm{bg}} = 4$ V (see for instance Fig. 23), the leakage current will be in the μA range (See Fig. 30), which might break the sample. A sudden break of the gate can lead to the application of several volts across the sample in a very fast way, leading to large currents that can blow up the flake. In our measurements, we take the precaution of connecting a $10\ \mathrm{M}\Omega$ resistor in series with the backgate. As a consequence, the current would be limited but the voltage applied to the gate would become minimal, as the voltage drop across the series resistor would become comparable to V_{bg}. Once we have set the V_{bg}, we sweep the finger gate for a predefined set of voltages on the split gates. In this way, we monitor the effect of the finger gates and split gates on the carrier density inside the channel. For a specific combination, the carrier density underneath the finger gate should deplete and

the density under the split gates minimizes. This experiment will be repeated for a variety of geometries.

We start by setting up the same measurement circuit as shown in Fig. 28. For this experiment, the larger split gates and corresponding middle finger gate were connected. For each value of the finger gate ($-10\,\mathrm{V} \leq V_{\mathrm{fg}} \leq 0\,\mathrm{V}$), the split gates ($-2.1\,\mathrm{V} \leq V_{\mathrm{sg}} \leq 1.9\,\mathrm{V}$) were swept at $V_{\mathrm{bg}} = 3\,\mathrm{V}$. Note that $V_{\mathrm{tg}} \approx -2\,\mathrm{V}$ corresponds to the CNP of the double-gated region in Fig. 27. The result is shown in Fig. 32a, with a darker horizontal area near $V_{\mathrm{sg}} = 1.97\,\mathrm{V}$ - as this is one of the areas with minimum conductance (implying most of the charge current is carried between the split gates). As shown in Fig. 32c, decreasing V_{fg} leads to a significant decrease of the current, indicating that the channel between the split gates is depleted. Even though in Fig. 32a there seems to be a step, indicating size quantization, individual horizontal profiles indicate that the noise level is too high to make such a claim. However, averaging several profiles over a certain voltage range suppresses this noise level and step quantization can be seen around $4e^2/h$, which is slightly lowered due to the resistance of the bilayer graphene outside the channel between the outer contacts. However, no Coulomb blockade oscillations are visible as the background noise is in the order of e^2/h and Coulomb blockade oscillations usually have an amplitude of $0.15 \times e^2/h$. Furthermore, there are vertical features present in the 3D plot and are also present in other geometries of finger gates and this split gate (not shown here). To see if these features persist, the sweeping order was changed for the same geometry as in Fig. 32. Thus, for each value of the split gate voltage, the finger gate voltages were swept. In Fig. 32b, the resulting 3D plot is shown for $V_{\mathrm{bg}} = 3\,\mathrm{V}$, with a corresponding trace in Fig. 32. Again, we were not able to deplete the channel (as expected) and, surprisingly, the vertical features persist. The persistence of the vertical features when changing the sweeping order indicates that they are not intrinsic to the device characteristics but a consequence of the sweeping process. This indicates that a charging and discharging mechanism may be at play.

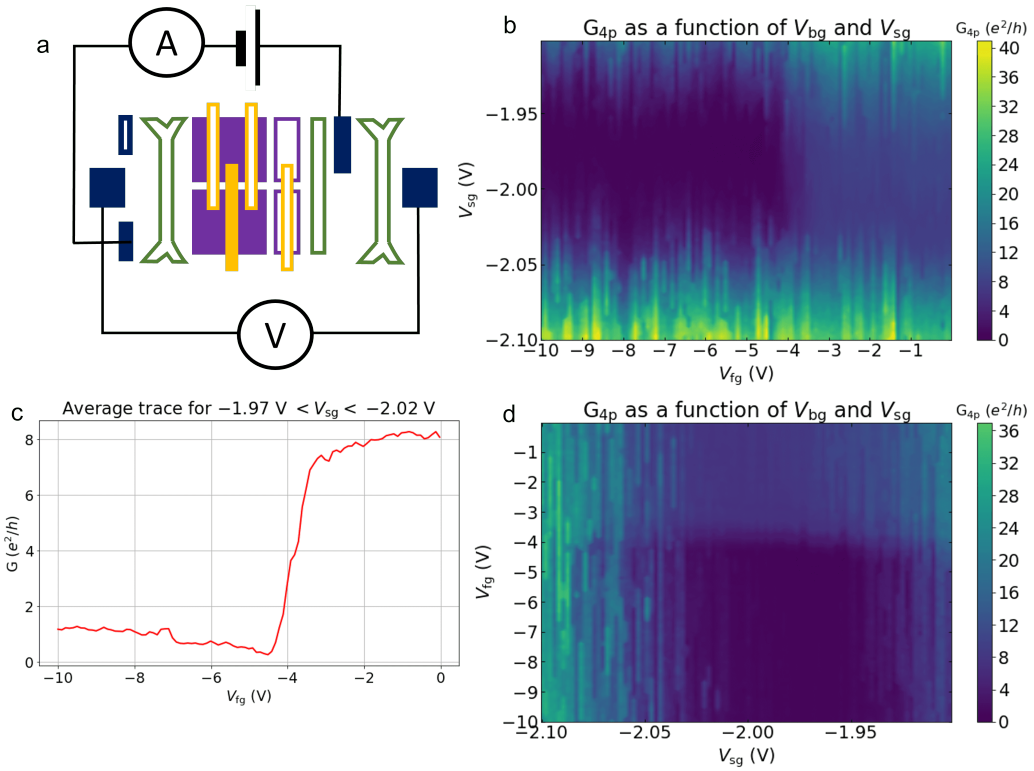

Figure 32: a) The four-terminal measurement circuit used. The voltage meter is connected between the outer contacts in the BLG (dark blue). The Ampere meter and voltage source ($100\ \mu$V) are connected to the other two contacts in the BLG (dark blue). Furthermore, the larger split gates (purple) and middle finger gate (yellow) are connected. b) The result of sweeping the split gate voltages for each value of the middle finger gate. V_{bg} was fixed at 3 V. c) An average trace for V_{tg}between -1.97 V and -2.02 V in a), corresponding with the region with minimum conductance. There seems to be a slight step quantization around $4e^2/h$. The channel was not fully depleted. No Coulomb blockade oscillations can be observed. Taking an average trace in d) in the same range for V_{sg} returns the same result (not shown). d) Changing the sweeping order of the measurement described in b). For every value of V_{tg}, V_{fg} was swept and the current was measured. As in panel a), $V_{\mathrm{bg}} = 3$ V. No depletion of the channel was noted and the vertical features persisted. These seem to hint at an unintended charging and discharging mechanism in the sample.

Moreover, depletion of the channel defined by the smaller split gates has been attempted, see Fig. 33. This has been done by sweeping the corresponding finger gate for each value of the split gates, at $V_{\mathrm{bg}} = 3$ V.

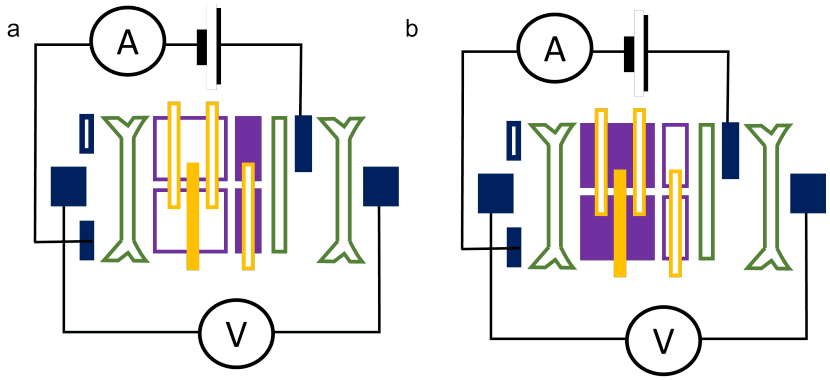

Figure 33: a) The measurement circuit used in Fig. 34a. Here, we connected the Ampere meter and voltage source between two contacts in the BLG (dark blue). Furthermore, an AC source was connected between the outer contacts in the BLG (dark blue). Meanwhile, the finger gate (yellow) was swept between -10 V and 0 V while sweeping the small split gates (purple) between -2.10 V and -1.90 V. The back gate voltage V_{bg} was 3 V. b) The measurement circuit used in Fig. 34b. The Ampere meter, voltage source and current source were connected in the same way as in a). However, now a finger gate (yellow) was swept between -10 V and 0 V while sweeping the large split gates (purple) between -2.30 V and -2.10 V. The back gate voltage V_{bg} was set at 3.5 V.

In Fig. 34, the resulting 3D plots are shown. In Fig. 34a, the result is shown from sweeping the smaller split gate as shown in Fig. 33. This channel was also not depleted and quantized conductance is not well defined. In Fig. 34b, the measurement of Fig. 32b was repeated but for $V_{\mathrm{bg}} = 3.5$ V. This is done to increase the electric field in the FET device, which should help depleting the channel. A trace of this measurement at $V_{\mathrm{sg}} = -2.21$ V (c) is shown. There is no full depletion visible and steps are still dominated by the unintended charging and discharging mechanism. No persistent Coulomb blockade oscillations are visible, which shows that no QD has formed. In Fig. 34d, an average trace for V_{sg} between -2.25 V and -2.20 V is displayed. Steps around $4e^2/h$ and $7e^2/h$ can be observed, slightly lowered due to measuring also the resistance of the BLG between the contacts outside of the channel. Since a quantization of $8e^2/h$ is expected and only $7e^2/h$ is measured, the series resistance should be around $460\ \Omega$. This corresponds with the measurement described in Fig. 23, where we have measured $R_{4\mathrm{p}}$ using the same contacts in the BLG.

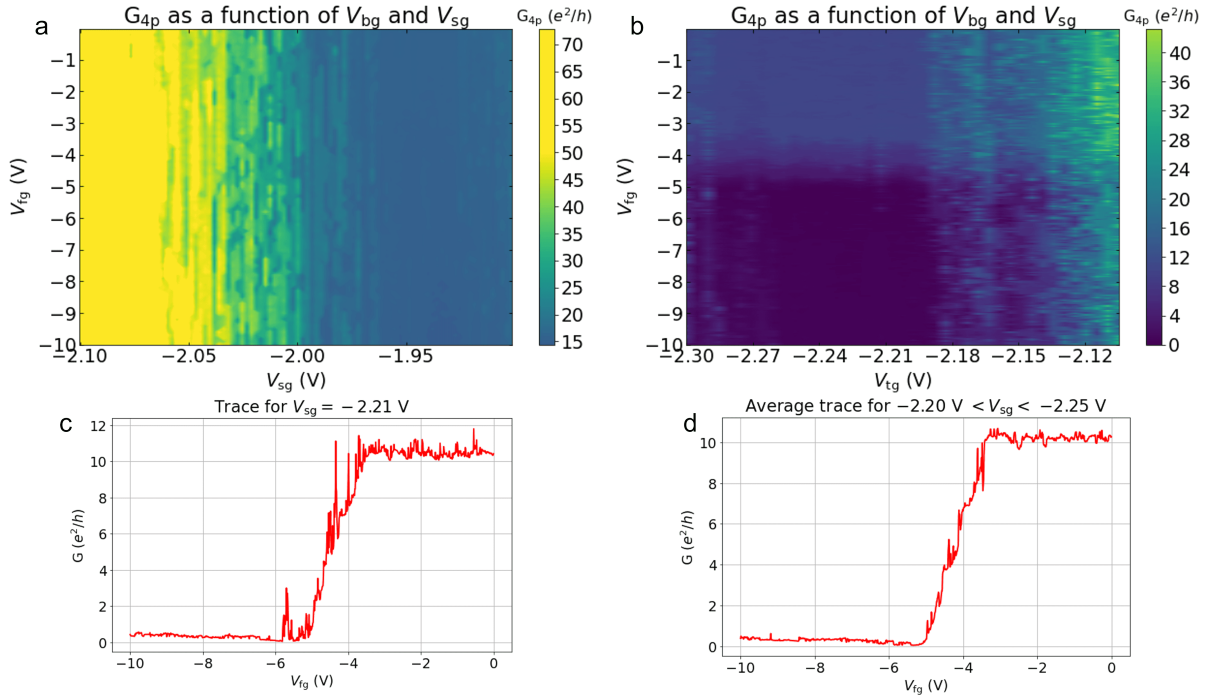

Figure 34: a) The 3D plot resulting from the measurement setup described in Fig. 33a. The channel was not depleted. b) The resulting 3D plot arising from the setup described in Fig. 33b. On the x-axis, the split gate voltages are displayed and on the y-axis the finger gate voltages. The color signifies the conductance measured using the Lock-in system, which is showed in terms of e^2/h. There is no clear depletion, however, step quantization is visible. c) A trace taken at $V_{\text{sg}} = -2.21$ V. Step quantization in the conductance can be observed, but is dominated by an unintended charging and discharging mechanism. d) An averaged trace taken for V_{sg} between -2.25 V and -2.20 V. Steps around $4e^2/h$ and $7e^2/h$ can be observed.

Furthermore, by tuning multiple finger gates simultaneously (as done in [56]), we attempted to confine charges, i.e. to form a quantum dot. In Fig. 35a, the larger split gates (purple) were connected, combined with two of the three finger gates (yellow). For each value of the split gates, both finger gates were swept simultaneously. However, this also did not deplete the channel, as can clearly be seen from the vertical trace taken at $V_{\text{sg}} = -1.97$ V (Fig. 35b), nor did it confine charges as in this case the characteristic Lorentzian peaks are expected in the density of states (and conductance).

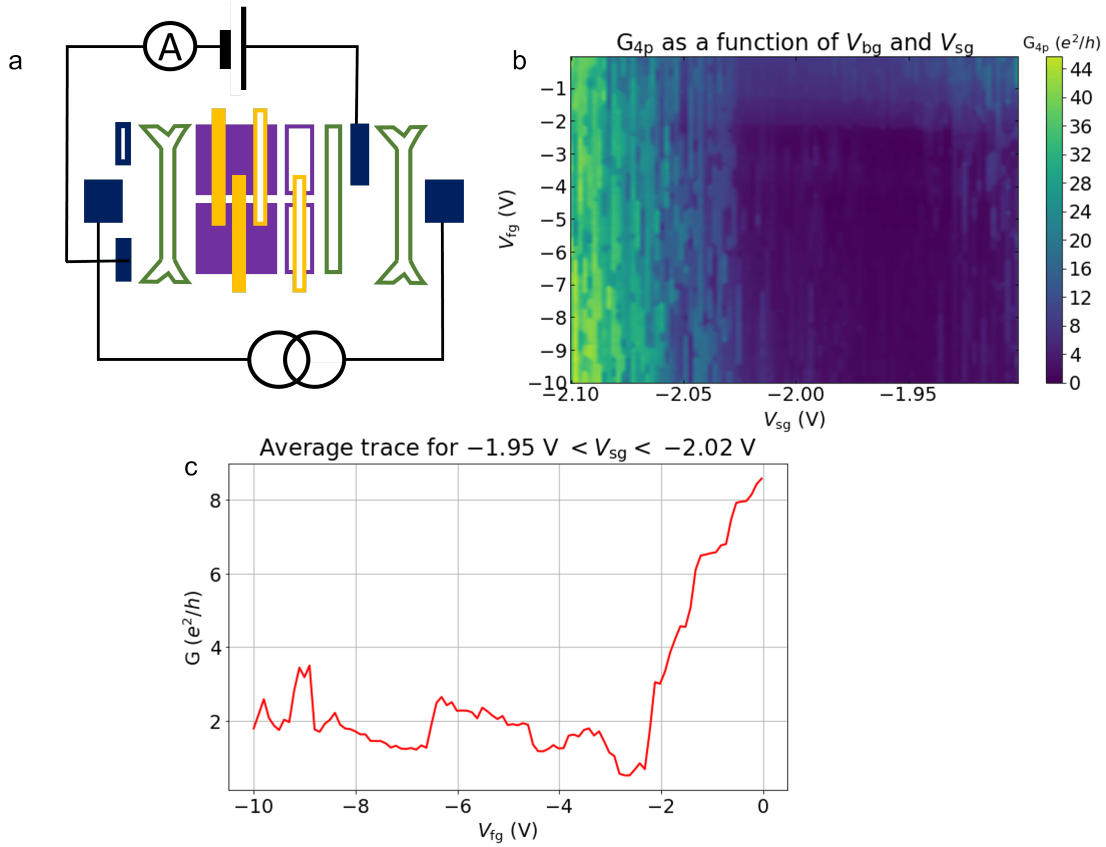

Figure 35: a) The circuit used in this measurement. Two finger gates were set between 0 V and -10 V for each V_{tg} on the split gates (purple) between -2.1 V and -1.9 V. Meanwhile, a c bias voltage of $V_{\text{bias}} = 100$ μV was applied and the current between the outer contacts in the BLG (dark blue) was monitored. By measuring the the voltage between , the conductivity can be calculated (z-scale). b) An averaged vertical trace for V_{sg} between -1.97 V and -2.02 V, with on the x-axis the finger gate voltage V_{fg} and on the y-axis the current in the channel.

As from the Hall Theory (see section 2.3), step quantization should be more defined at higher magnetic fields. Therefore, another attempt was made to deplete the channel defined by the large split gates, with corresponding middle finger gate, at $B = 5$ T (see Fig. 33b). The result looks a lot cleaner, with a clear depletion of the channel (see Fig. 36a-b). The corresponding averaged trace clearly shows depletion and signs of step quantization of the conductivity. To take a closer look, the measurement was executed again with smaller stepsize for -5 V $\leq$ $V_{\text{fg}} \leq -3$ V. A corresponding trace of this measurement is shown in Fig. 36 and shows an additional feature, related with an unintended charging and discharging mechanism in the sample.

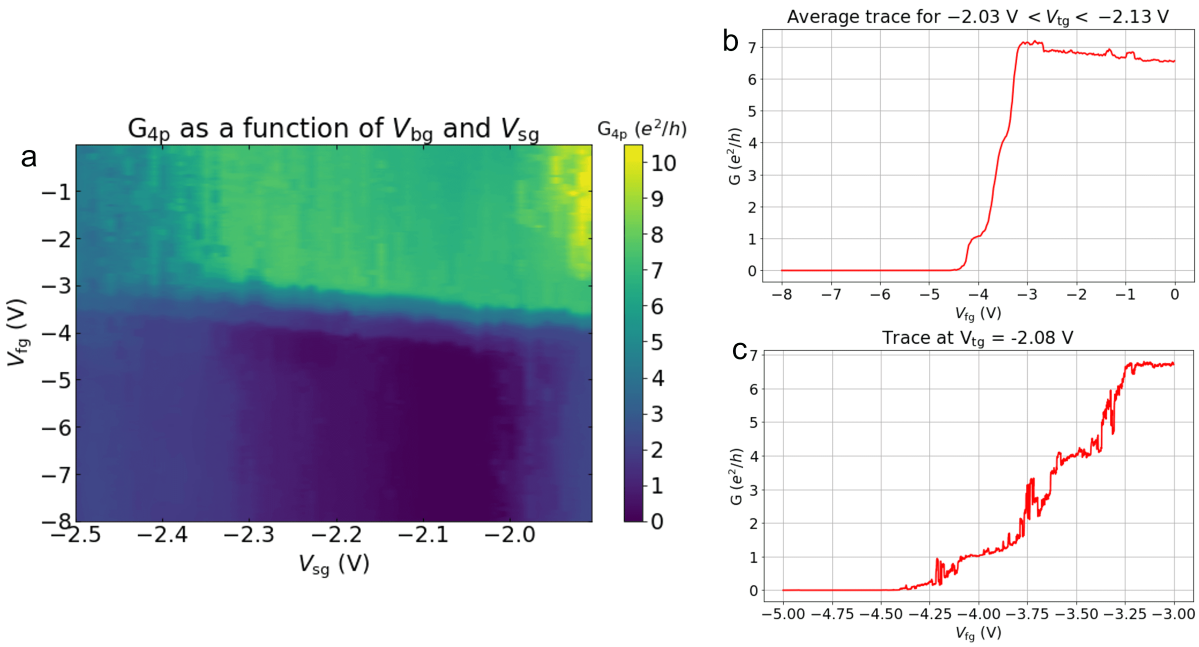

Figure 36: a) 3D plot obtained by sweeping the large split gates with the middle finger gate at $B = 5$ T, see Fig. 33b for the circuit. It shows clear depletion of the channel and quantization in the current. b) An averaged trace for V_{sg} between -2.03 V and 2.13 V, with on the x-axis V_{sg} and on the y-axis the current. The current shows quantized steps and shows that there is a depletion in the channel. c) A trace at $V_{\mathrm{sg}} = -2.08$ V, taken from a more detailed sweep.

4.3. Measuring voltages

This section describes the heating experiments conducted in the previously defined structures. To select an appropriate heating current for the thermovoltage characterizations, the voltages in the first and second harmonic for different heating current values and back gate voltages were mapped. For this purpose, an AC current was applied on the right heater (see circuit in Fig. 37), varying between 5 μA and 50 μA in steps of 5μA. For each current value, the back gate V_{bg} was varied between $-3\,\mathrm{V} \leq V_{\mathrm{bg}} \leq -1$ V. The voltage response was measured between 23 and 9 with two Lock-ins, one was tuned to measure the first harmonic voltage and the other one for the second harmonic voltage (see section 3.2 for more details on the Lock-in). The first harmonic voltage is the result of Peltier heating (see Section 2.5.2) and the second harmonic is a consequence of Joule heating (see Section 2.5.3). The measurement circuit is drawn in Fig. 37a. In Fig. 38, the results of this measurement are shown. Fig. 38a contains the x-component of voltage response in the second harmonic for $-3\,\mathrm{V} \leq V_{\mathrm{bg}} \leq -1$ V. It features a sign change around the charge neutrality point ($V_{\mathrm{bg}} = -2$ V), and values are in the 0.1 μV range. The sign change indicates the carrier type change from electrons to holes [61]. Fig. 38b shows the corresponding y-component of the second harmonic voltage response. It contains a peak around the charge neutrality point ($V_{\mathrm{bg}} = -2$ V), and values are 10x larger than in the x-component (as expected, the y-component in the second harmonic should be lower than the x-component, see section 3.2). Therefore, in the rest of this chapter, only the y-component of the second harmonic will be shown. Fig. 38c contains the x-component of the first harmonic voltage response for $-3\,\mathrm{V} \leq V_{\mathrm{bg}} \leq -1$ V. It also shows a peak around the charge neutrality

point ($V_{\mathrm{bg}} = -2$ V), with values in the μV range. Since the x-component of the first harmonic is much larger than its corresponding y-component (see Fig. 38d), only the x-component of the first harmonic will be shown in the rest of this chapter. Based on Eq. 15 and Eq. 14, we expect the first harmonic and second harmonic to have opposite sign.

Based on this measurement (specifically: Fig. 38b and c) and the estimation of the Seebeck coefficient in Fig. 31, a rough estimation can be made for the temperature induced by the heaters. By rewriting Eq. 11 to $\Delta T = -S/\Delta V$, a ΔT in the range of 0.5 ± 0.2 K is expected (for $I_{\mathrm{heat}} = 50$ μA, as this current will be used when measuring the thermal voltages in other geometries).

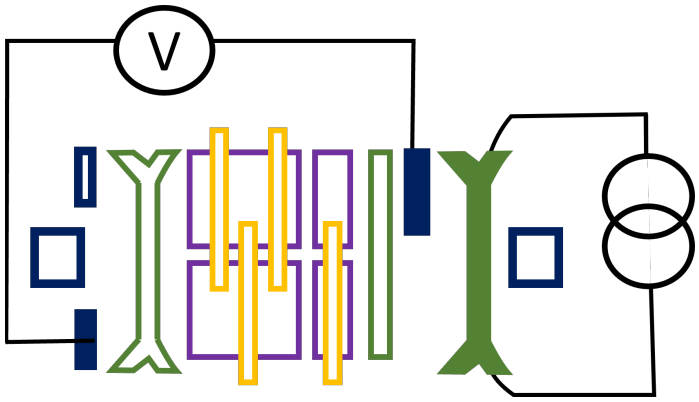

Figure 37: The circuit used in Fig. 38 and in Fig. 39. The current source (ac) of 1 μA is connected to the right heater (from now on: I_{heat}), and the voltage meter is connected between two contacts in the BLG. The output voltage is then connected to two Lock-ins, which are tuned to monitor the voltages in the first and second harmonic.

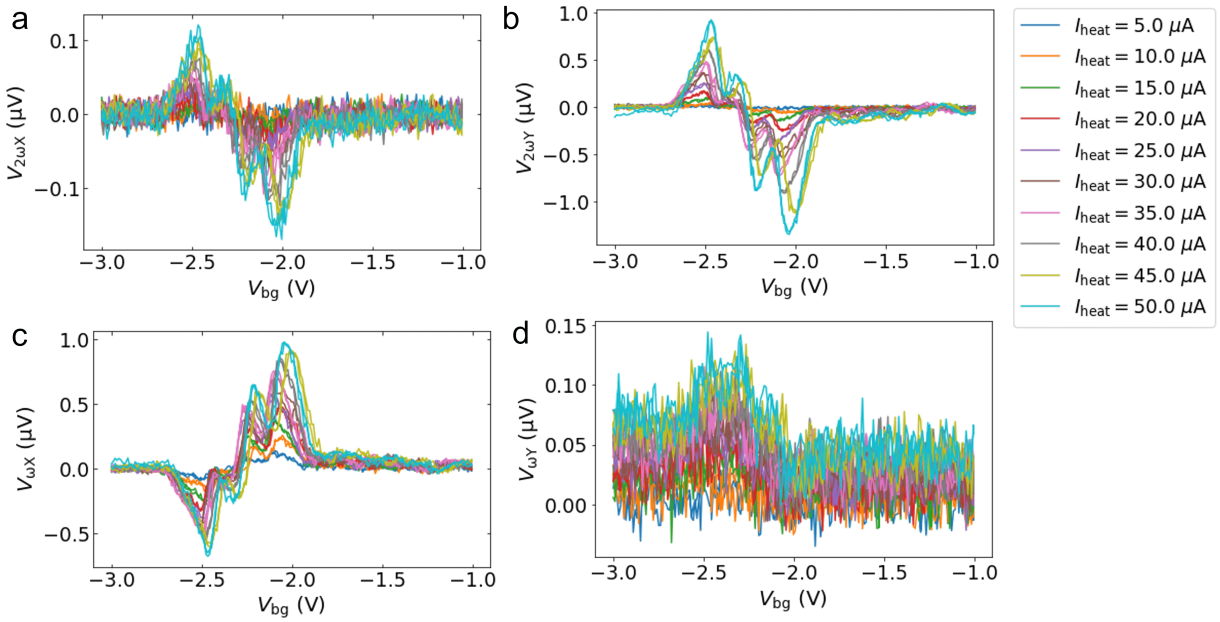

Figure 38: Voltage responses in the first and second harmonic for varying values of heating current I_{heat} through the right heater, using measurement circuit 37a. a) The x-component of the second harmonic voltage response for $-3\text{ V} \leq V_{\text{bg}} \leq -1\text{ V}$. b) The y-component of the second harmonic voltage response for for V_{bg} between -3 V and -1 V. It contains a peak around the charge neutrality point ($V_{\text{bg}} = -2$ V), and values are 10x larger than in the x-component. c) The x-component of the first harmonic voltage response for the same range of V_{bg}. It contains a peak around the charge neutrality point ($V_{\text{bg}} = -2$ V), with values in the μV range. d) The y-component of the first harmonic voltage response for $-3\text{ V} \leq V_{\text{bg}} \leq -1\text{ V}$ at different current values.

Possibly, gating from the contacts could have induced a change in resistance of the BLG proportional to frequency ω, as:

$$R = R_0 + \Delta R \sin(\omega t), \tag{26}$$

in which R_0 the resistance of the BLG without a gating effect ΔR the resistance change due to a gating effect. Having a second harmonic and a DC component signal coming from the I^2 term (see Eq. 15), the ΔR term could generate a first and a third harmonic contribution. Therefore, this measurement has been repeated to characterize the voltage responses in the third and fourth harmonic for the same range of heater currents. The results are shown in Fig. 39. Again, Fig. 39a contains the x-component of the third harmonic, Fig. 39b the corresponding y-component, Fig. 39c the x-component of the fourth harmonic and Fig. 39d its corresponding y-component.

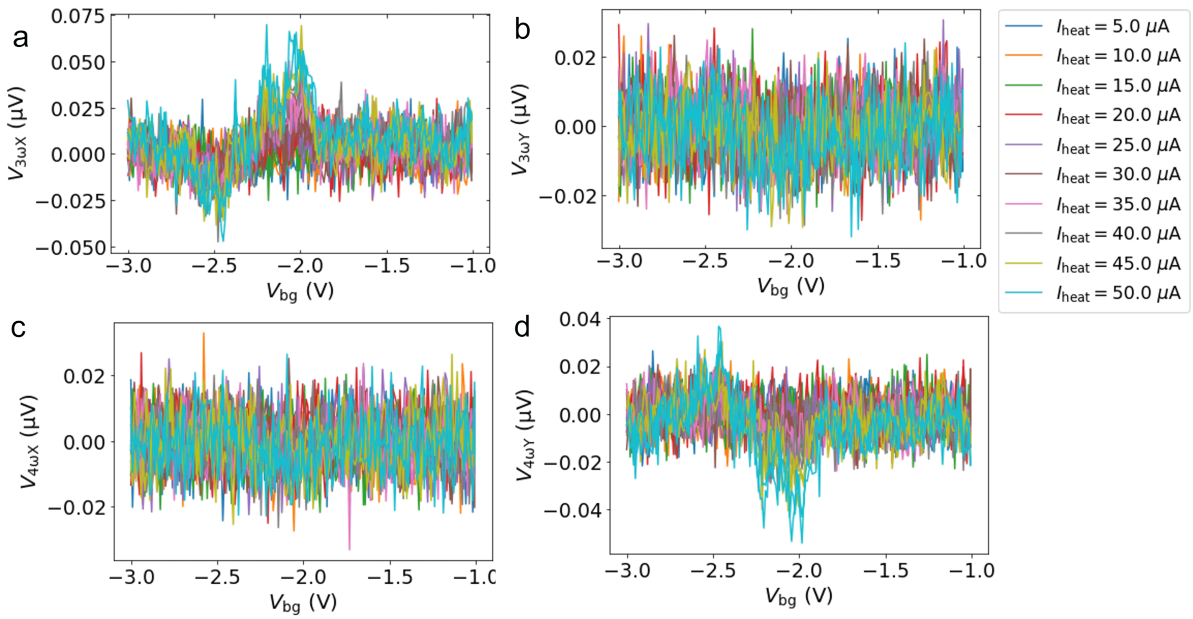

Figure 39: Voltage responses in the third and fourth harmonic for varying values of heating current through the right heater, using measurement circuit 37a. a) The x-component of the third harmonic voltage response for $-3\text{ V} \leq V_{\text{bg}} \leq -1\text{ V}$. It contains a slight peak around the charge neutrality point ($V_{\text{bg}} = -2\text{ V}$), but values are in the $0.05\ \mu$V range. b) The y-component of the third harmonic voltage response for V_{bg} between -3 V and -1 V. No clear features can be distinguished here. c) The x-component of the fourth harmonic voltage response for the same range of V_{bg}. Only noise was measured. d) The y-component of the fourth harmonic voltage response at different current values. A slight peak can be seen at $V_{\text{bg}} = -2$ V.

As can be seen in Fig. 39, $V_{3\omega\text{Y}} \ll V_{3\omega\text{X}}$ and $V_{4\omega\text{X}} \ll V_{4\omega\text{Y}}$. Furthermore, the magnitude of the third harmonic is 15 to 20 times smaller than the first harmonic. Based on Eq. 16, we expect that the contribution of the first harmonic is only 3 times larger than the third harmonic. However, the magnitude of this gating effect would be limited, as the gating effect is only a small modulation of the thermal voltage, and cannot explain this feature entirely. Therefore there must be another source from the first harmonic, which is yet unclear.

In addition, the resistance of the heater was measured for a constant current at different temperatures, characterizing $R(T)$. For the measurement shown in Fig. 40b, an AC heating current of $1\ \mu$A was applied on the right heater, and simultaneously, the voltage drop was measured between the other ends of the heater (for a schematic overview, consult Fig. 40a). This was done at varying temperatures between 1.8 K and 50 K. Before measuring the voltage difference at each temperature, a 5 s waiting period has been set to let the temperature stabilize. As temperature increases, an increasing trend is expected in the resistance of the gold heaters [78]. However, as can be seen in Fig. 40, the resistivity of the gold heaters at low temperatures is relatively constant, which indicates that the gold heaters are not appropriate to use as thermometers at low temperatures.

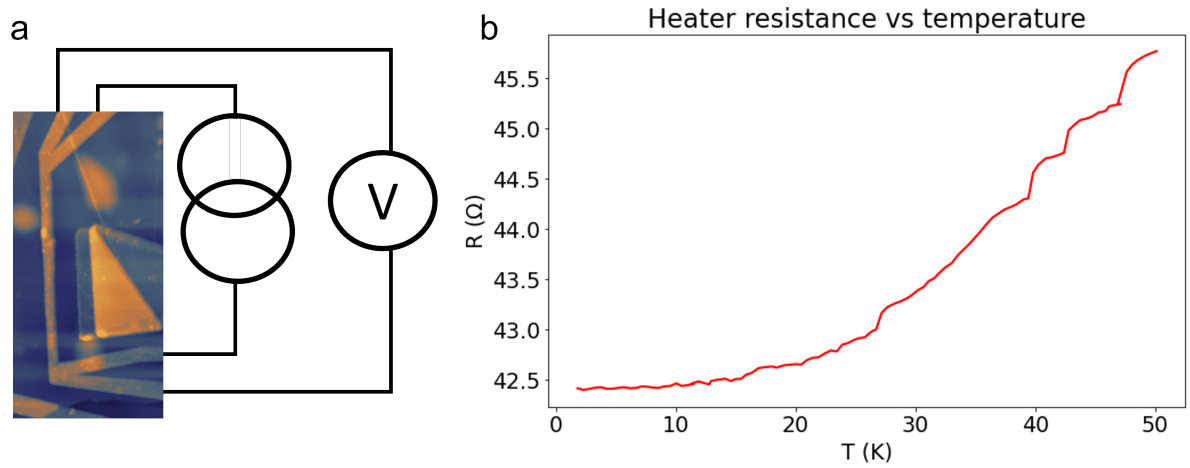

Figure 40: a) Measurement circuit used to perform a heater resistance versus temperature measurement. The right heater was connected to an AC bias of 50 μA, while a voltage meter (using the Lock-in) was connected to two contacts in the BLG. b) The heater is connected to an AC of 50 μA and voltage meter using a four-probe measurement to exclude the heater resistances. The temperature of the setup was varied between 1.8 K and 100 K, and an increasing trend in the resistance of the gold heater is demonstrated. However, in the low temperature range, the resistance shows almost no change, indicating that the gold heaters cannot be used as thermometers at low temperatures.

Instead, a theoretical model was constructed to calibrate the heaters, based on [79] and [80]. The temperature rise as a result of Joule heating can be estimated by making assumptions about the thermal resistance of the SiO_2 at low temperatures and the thermal conductance of the graphene - SiO_2 boundary, however, these estimations are not obvious thus this model was not used to calibrate the heaters. For more details, please consult the Appendix.

As the calibration was unsuccessful, the rest of the chapter will feature a selection of the measured voltages (and not the thermopowers). First, an overview of the measurement circuits will be given, see Fig. 41. The voltages were measured in the smaller split gates (panel a), the larger split gates (panel b), and a top gate (panel c). In these measurements, the top gates were swept between -3 V and 0 V (as we expect the charge neutrality point to be at -2 V). An AC heating current of $I_{\text{heat}} = 50$ μA was applied through the right heater (green). Meanwhile, the resulting voltage was monitored through a dual Lock-in setup across the bilayer graphene from the dark blue contacts, which is tuned to monitor the first and second harmonic of the voltage.

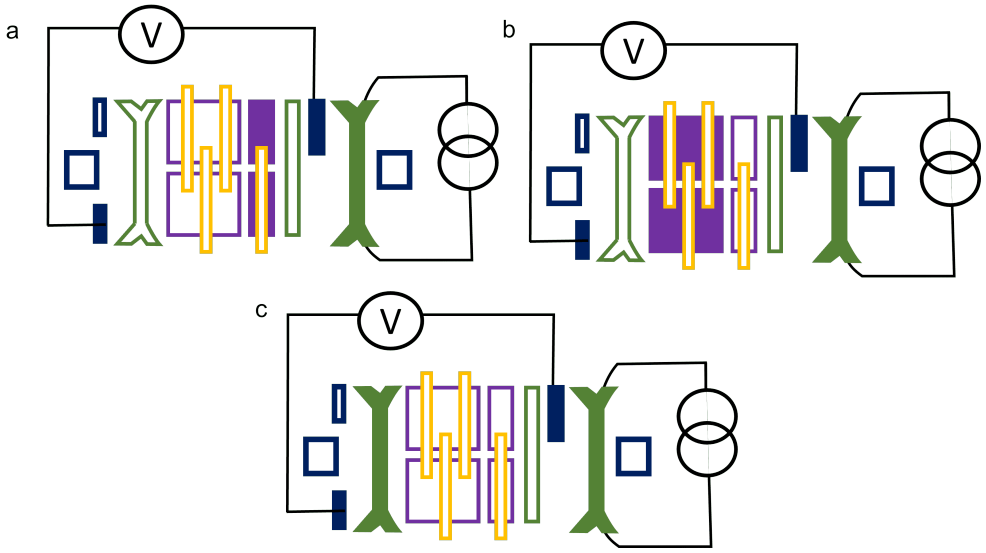

Figure 41: These panels represent the measurement circuits used in Fig. 42, Fig. 43 and Fig. 44, respectively. In all setups, the current source (ac) of $50\ \mu$A is connected to the right heater, and the voltage meter is connected between two contacts in the BLG. The output voltage is then connected to two Lock-ins, which are tuned to monitor the voltages in the first and second harmonic. The top gates were swept between -3 V and 0 V (as we expect the charge neutrality point to be at -2 V). a) The measurement circuit used in Fig. 42. The small split gates (purple) are connected. The back gate voltage was set to $V_{\mathrm{bg}} = 0$ V (see Fig. 42a and c) and $V_{\mathrm{bg}} = 3$ V (see Fig. 42b and d). b) The measurement circuit used in Fig. 43, with the large split gates (purple) connected. The back gate voltage was set to $V_{\mathrm{bg}} = 3$ V. c) The measurement circuit used in Fig. 44, with the left green top gate connected.

Furthermore, the back gate voltage was set to $V_{\mathrm{bg}} = 0$ V (see Fig. 42a and c) and $V_{\mathrm{bg}} = 3$ V (see Fig. 42b and d), to map the effect of the split gates only and at maximum bandgap opening, respectively. In Fig. 42a and b, the second harmonic voltages are shown for $V_{\mathrm{bg}} = 0$ V and $V_{\mathrm{bg}} = 3$ V, respectively. Fig. 42c and d are the corresponding voltages in the first harmonic.

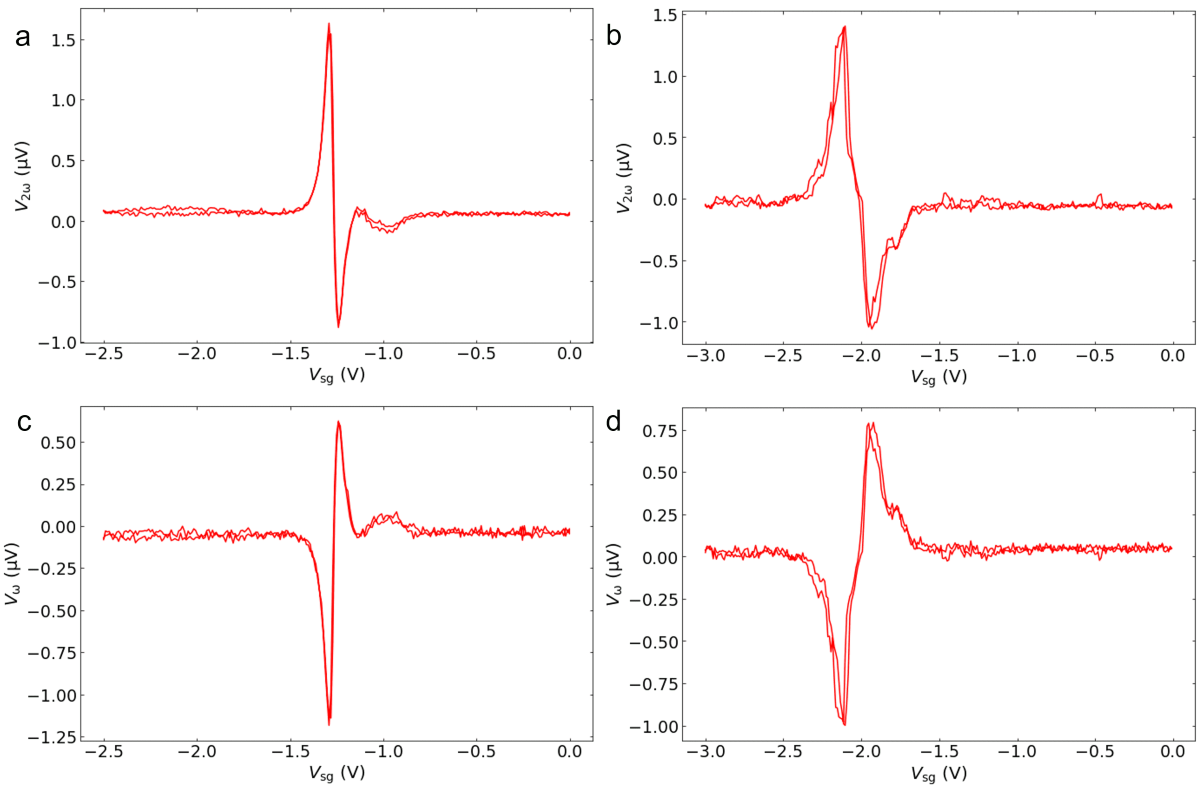

Figure 42: Voltage responses in the second and first harmonic for $I_{\text{heat}} = 50\ \mu$A through the right heater, using measurement circuit 41a. a) The y-component of the second harmonic voltage response for $-2.5\ \text{V} \leq V_{\text{sg}} \leq 0\ \text{V}$, for $V_{\text{bg}} = 0\ \text{V}$. It contains a peak around the charge neutrality point ($V_{\text{sg}} = -1.5\ \text{V}$). b) The y-component of the second harmonic voltage response for $-2.5\ \text{V} \leq V_{\text{bg}} \leq 0\ \text{V}$, for $V_{\text{bg}} = 3\ \text{V}$. It contains a peak around the charge neutrality point ($V_{\text{sg}} = -1.5\ \text{V}$). c) The x-component of the first harmonic voltage response for V_{sg} in the same range as in a. Also here, the charge neutrality point is around $V_{\text{sg}} = -2\ \text{V}$, with values in the μV range. d) The x-component of the first harmonic voltage response for V_{sg} in the same range as in b.

Additionally, the large split gates were connected in accordance with Fig. 41b and voltages between $-3\ \text{V}$ and $0\ \text{V}$ were applied. An AC heating current of $I_{\text{heat}} = 50\ \mu$A was applied on the right heater (green) and the voltage was measured between two contacts in the BLG (dark blue). The back gate voltage was set at $V_{\text{bg}} = 3\ \text{V}$. The results are shown in Fig. 43. As this measurement was done at a later stage, the doping of the device has changed, which might have caused the charge neutrality point to shift.

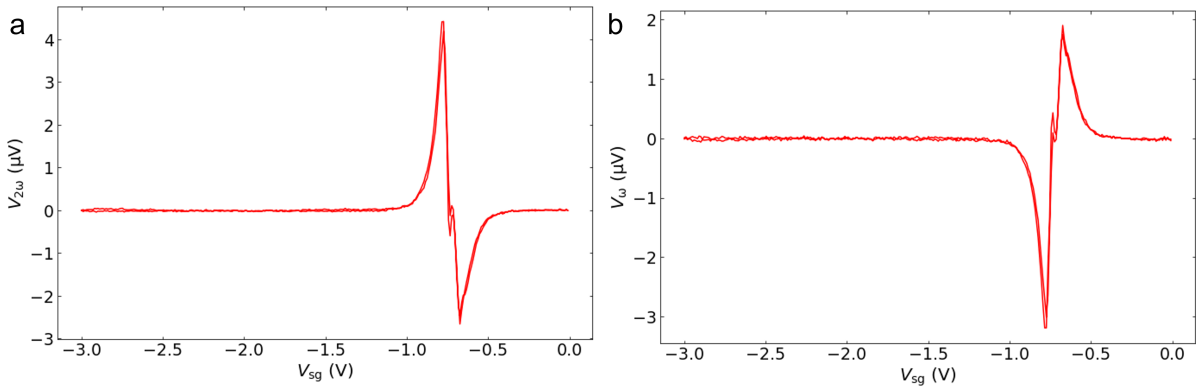

Figure 43: Voltage responses in the second and first harmonic for $I_{\text{heat}} = 50$ μA through the right heater, using measurement circuit described in Fig. 41b. a) The y-component of the second harmonic voltage response for -3 V $\leq V_{\text{bg}} \leq 0$ V, for $V_{\text{bg}} = 3$ V. The peak of the CNP (now, at $V_{\text{sg}} = -0.75$ V) has been shifted, which could be the result of a change in doping due to repeated sweeping. b) The x-component of the first harmonic voltage response for the same range in V_{sg} as in a, for $V_{\text{bg}} = 0$ V.

In Fig. 44, results from the measurement circuit described in Fig. 41c are shown. The top gate (green) is swept between -3 V and 0 V. The right heater (green) is used to apply $I_{\text{heat}} = 50$ μA. Meanwhile, the voltage across two contacts in the BLG (dark blue) was measured with two Lock-ins tuned to the first and second harmonic.

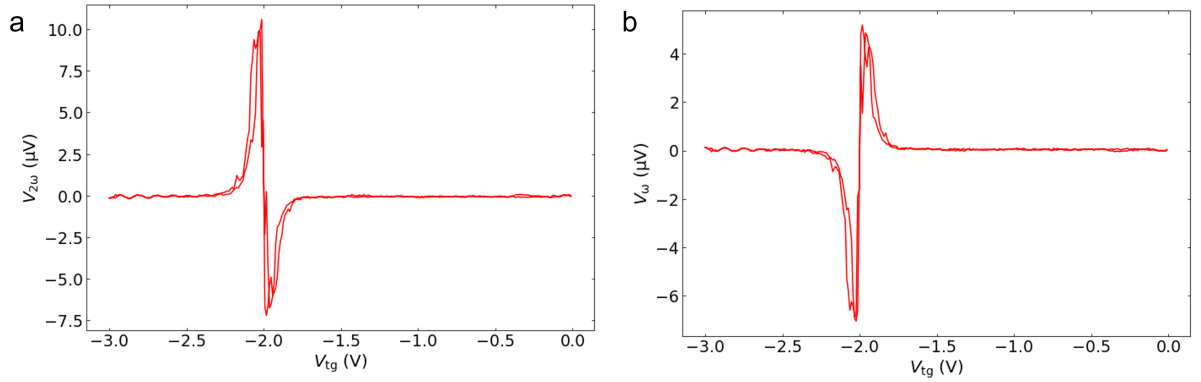

Figure 44: Voltage responses in the second and first harmonic for $I_{\text{heat}} = 50$ μA through the right, using measurement circuit 41c. a) The y-component of the second harmonic voltage response for -3 V $\leq V_{\text{tg}} \leq 0$ V, for $V_{\text{bg}} = 3$ V. It contains a peak around the charge neutrality point ($V_{\text{sg}} = -2$ V). b) The x-component of the first harmonic voltage response, measured for the same range of V_{tg} at $V_{\text{bg}} = 3$ V.

Besides this selection, heating measurements were done in the large split gate configuration at higher magnetic fields ($B = 2$ T, $B = 5$ T; see Fig. 36, giving us a QPC), while sweeping finger gate 19. Furthermore, the right heater was swapped for the left heater to repeat a top gate measurement. In these aforementioned measurements, however, no significant signal was picked up.

5. Conclusion

Nanostructures in bilayer graphene have promising potential applications in spintronics and valleytronics - and is therefore a widely researched area since its discovery in 2004 [19]. Characterizing thermotransport phenomena in bilayer graphene based quantum point contacts and quantum dots brings additional insight into their transport phenomena and could pave the way for more durable devices as harvesting thermopowers can increase longevity.

In this thesis, a BLG sample is encapsulated in hBN, with a graphene backgate. The top hBN was etched to contact the BLG with Ti/Au to inject carriers and perform voltage measurements (resistance characterizations) over the BLG. On top of the hBN, a series of top gates and heaters (Ti/Au) were fabricated, amongst two series of 100nm separated split gates. The sample was covered with a 30 nm Al_2O_3 dielectric layer to separate top gates from the four 100 nm wide finger gates, placed on top of the split gates. Through the combined action of a top gate and back gate, an electric field was created which opened the band gap of the BLG. However, gate-dependent resistance measurements indicate that the electric field induced by the back gate is being screened by a layer of charges somewhere between the back gate and the bilayer graphene. The origin of this layer of charges remains unknown. As a result, we were not able to fully deplete the channel as defined by the split gates through the combined action of back gate, split gates and (multiple) finger gate(s). By swapping the gate sweeping order, we observed persisting vertical features in the results, which hint at an unintended charging and discharging mechanism in the sample. Through applying a large magnetic field ($B = 5$ T), we were able to deplete the channel and got a quantized conductance response, however, a clean and detailed sweep could not be obtained due to the charging mechanism described above.

Thermal transport measurements were also performed in the sample using the heaters. Based on the resistance characterization of the sample, the Seebeck coefficient was estimated using Mott's formula (in the range of μV/K) and were in the similar range of the measured signals. The temperature rise as a result of applying 50 μA in heating was estimated to be 0.5 ± 0.2 K and clearly defined thermovoltages were measured as a result.

6. Recommendations

For further research, it is recommended to use a different material for the heater, since the golden heaters have almost no resistance change response in the low temperature range. Furthermore, the fabrication steps described in this thesis can be used as a guide in the complex manufacturing of this device. More devices need to be prepared to remove the effect of the charging layer which we observed in this device. As a result, experiments may be realized with larger electric fields , leading to cleaner size quantization steps and Coulomb oscillations.

Furthermore, the narrowing of the splitting between the split gates has been shown to result in cleaner step-like structures in BLG [56] and may be useful to increase the expected thermal signals from the QPCs.

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Appendix

Bandgap calculation

To estimate the bandgap opening in our sample, first, the electric field is calculated at the charge neutrality point (as a reference, where $V_{\mathrm{bg}} - V_{\mathrm{bg}}^{(0)} = 0$) and is subtracted from the electric field at $V_{\mathrm{sg}} = 3$ V. This is done as the back gate did not tune the electric field constantly and thus the back gate contribution needs to be estimated. Rewriting Eq. 4 at $n = 0$ gives:

$$C_{\mathrm{bg}}(V_{\mathrm{bg}} - V_{\mathrm{bg}}^{(0)}) = C_{\mathrm{tg}}(_{\mathrm{tg,CNP}} - V_{\mathrm{tg,3}}), \tag{27}$$

where the $C_{\mathrm{bg}}(V_{\mathrm{bg}} - V_{\mathrm{bg}}^{(0)})$ is the contribution from the back gate, $_{\mathrm{tg,CNP}}$ is the top gate voltage at the CNP (-2 V) and V_{tg3} is the top gate voltage at $V_{\mathrm{bg}} = 3$ V and for $n = 0$ (-1 V). As $V_{\mathrm{tg0}} - V_{\mathrm{tg3}}$ reduces to 1V, we can substitute this into Eq. 5:

$$E = \frac{C_{\mathrm{tg}}}{2} - \frac{C_{\mathrm{tg}}(V_{\mathrm{tg}} - V_{\mathrm{tg}}^{(0)})}{2}. \tag{28}$$

Filling in $V_{\mathrm{tg}} = -2$ V and $V_{\mathrm{tg}}^{(0)} = -1$ V, we obtain $E = 0.1$ V/nm (or: $D/0$). This can be converted into bandgap opening using [49], resulting in a bandgap of approximately 8 ± 2 meV.

Temperature calibration

Heating of the device as a result of Joule heating was estimated through the following formula:

$$\Delta T = P(R_{\mathrm{B}} + R_{\mathrm{ox}} + R_{\mathrm{Si}}), \tag{29}$$

in which $\Delta T = T - T_0$ is the temperature difference as a result of applying a voltage through a heater, $P = I^2/R_{\mathrm{h}}$ the dissipated power (with corresponding current I and resistance of heater R_{h}), $R_{\mathrm{B}} = 1/(hA)$ is the thermal resistance of the graphene - SiO_2 boundary, $R_{\mathrm{ox}} = t_{\mathrm{ox}}/\kappa_{\mathrm{ox}}$ the thermal resistance of the 300 nm SiO_2 and $R_{\mathrm{Si}} = 1/(2\kappa_{\mathrm{Si}}A^{1/2})$ the thermal resistance of the Silicon wafer. Furthermore, $A = LW$ is the area of the channel, h the thermal conductance of the graphene - SiO_2 boundary, κ_{Si} is the thermal conductance of the silicon and κ_{ox} the thermal conductance of the SiO_2. However, the parameter κ_{ox} was only available for the 70 K - 500 K regime, as well as an appropriate choice for h for the device in this thesis. A linear extrapolation of $\kappa_{\mathrm{ox}}$and keeping $h = 10^8$ W m^{-2} K^{-1} resulted in ΔT in the range of 10^{-5} K. As a temperature induced by the heaters of around 0.5 ± 0.2 K is expected (for I $= 50$ μA), this model cannot be used to calibrate the heaters.

Code

In this section, the code to model the thermpower for 2D, 1D and 0D are shown. It only displays the relevant functions - for all of the code, please consult my github link, $https://github.com/ianmrosales/quantum$. The gate V_g was chosen to range from -5V to 5V (in the bilayer graphene case) and the temperature was set at $T = 1.8$ K.

```
def dRdu(R):
    """
```

```
    Parameters:
    -----------
    R: array
        Values of resistances.

    Returns:
    --------
    derivative: array
        The numerical derivative of R, logarithmically transformed.
    """
    log = np.log(R)
    derivative = np.gradient(log)
    return derivative


def Mott(f, T, Ef):
    """
    Mott formula to calculate the Seebeck coefficient

    Parameters:
    -----------
    f: array
        The numerical derivative of log(R).
    T: array
        The measurement temperature (1.8K)
    Ef: array
        Fermi energy
    Returns:
    --------
    mott: array
        An array with Seebeck coefficients for different temperature
    ↪   values.
    """
    mott = cns.pi**2 * cns.k**2 * T * f / (3*cns.e*np.gradient(Ef))
    return mott

def Efn(Vg):

    # fermi velocity, 10^6
    vf0 = 1e6
    n = cns.epsilon_0*er*(Vg)/(cns.e*tbg)

    #spin and valley degeneracies
    gs = 2
    gv = 2

    # coupling coefficient, eV to Joule
    gamma1 = 0.4 * cns.e

    # effective mass
    m = 0.033 * cns.m_e

    # defining prefactor
    A = 2 * gs * gv / (4 * cns.pi * cns.hbar**2 * vf0**2)

```

```
    # calculation of Ef
    Ef = (-gamma1 * A + np.sqrt(gamma1**2 * A**2 + 2 * A * n))/(A)

    n0 = cns.epsilon_0*er*(0.5)/(cns.e*tbg)
    n_eff = np.sqrt(n**2 + n0**2)
    return Ef

kox = lambda T: 0.515 + (0.515 - 0.658) / 25 * (T-75)

# assuming for silicon wafer:3e2 for T=1.8 and
# only valid for T<75
def Rox(dT, tox, T0, Lh, Wh):
    kox = lambda dT: 0.515 + (0.515 - 0.658) / 25 * (T0+ dT/2-75)
    return tox/(kox(dT)*Lh*Wh) # + dT/2s

def dT_fun(dT, P, tox, T0, Lh, Wh):
    ksi = 3e2 # at K=0
    h = 1e8 # thermal conductance of the graphene-SiO2 boundary
    Rsi = 1/(2*ksi*np.sqrt(Lh*Wh))
    Rb = 1/(h*Lh*Wh)
    #T0 = 1.8
    return P*(Rb + Rox(dT, tox, T0, Lh, Wh) + Rsi) *
     ↪  np.ones(np.size(dT)) #- dT

tox, T0, Lh, Wh = 300e-9, 1.8, 7.77e-6, 0.2e-6
T0 = 1.8
P = (5e-3) ** 2 / 30
dT_opti = lambda dT: np.abs(dT_fun(dT, P, tox, T0, Lh, Wh) - dT)

f = minimize_scalar(dT_opti, bounds=[0, 1])
```