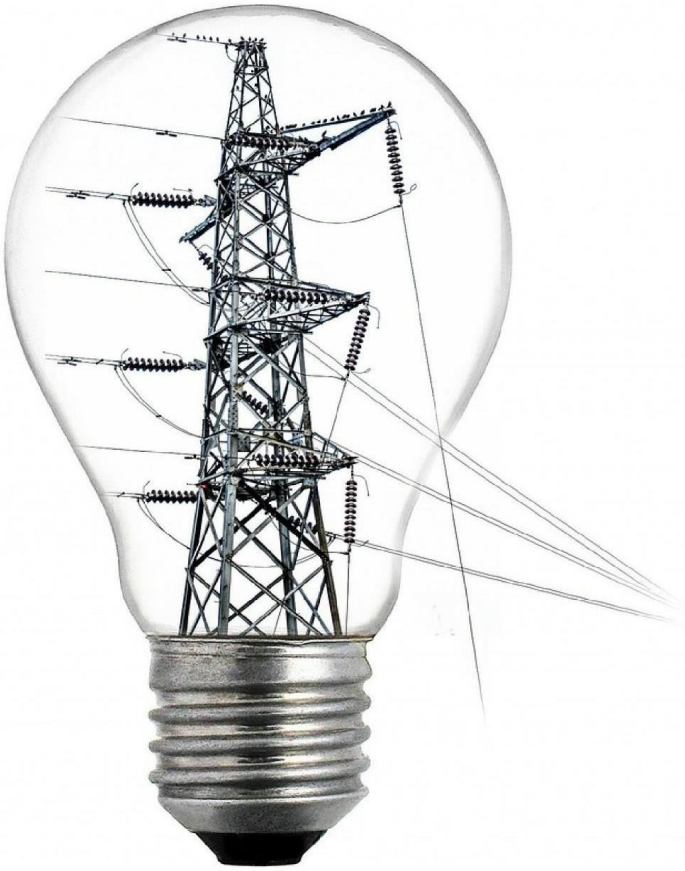
Control Strategy in Parallel AC-DC Re-configurable Links System



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Control Strategy in Parallel AC-DC Re-configurable Links System

A thesis submitted to the Delft University of Technology in partial fulfillment of the requirements for the degree of

Master of Science in Electrical Power Engineering

by

Yang Wu

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ABSTRACT

Recent studies have shown that energy distribution systems based on hybrid (or parallel) point-to-point AC and DC links are interesting solutions for capacity enhancement and on-line improvement of energy efficiency under specific operating conditions, particularly for high power, medium to high voltage levels and long-enough distances, e.g. > 5 km. Additionally, due to the power controlability provided by the power electronic circuits within the DC links the parallel distribution system can be re-configured through GIS disconnectors operating with improved switching performance. In this work this feature is explored and strategies for the system re-configurations are proposed. These aim to provide a nearly zero current switching for the GIS in order to prevent its deterioration and to extend the number of maneuvers for the typical GIS lifetime.

In fact, the proposed re-configuration strategies rely on the DC bus voltage and power controls of a Back-to-Back (B2B) power electronic system constructed with Voltage Source Converters (VSC). Herein, three-wire three-phase two-level VSCs with thrid-order AC harmonic filters (or LCL filter) are adopted in the B2B system. Moreover, Grid-side Current Controls (GCC) for the inner/fast control loops of the front- and back-end circuits are implemented in order to enhance the system performance against grid disturbances. Herein, a notch filter-based GCC scheme with a harmonic rejection control is proposed. This is able to deliver attenuation to the LCL filter resonances while suppressing the harmonics in the grid-side currents originated when the AC voltages are distorted. Interestingly, the parallel AC and DC links provides a low impedance path for the zero-sequence components which can be created by the power electronics, thus the implementation of a Zero-sequence Circulating Current (ZSCC) controller becomes necessary for the proper operation of the system. Hence, ZSCC controllers for the VSCs are used, while both front- and back-end circuits are modulated with constant switching frequency using the conventional sinusoidal PWM strategy.

All in all, results are obtained in both, computational simulations carried out in MATLAB/SIMULINK and laboratory experiments performed in a 5 kVA VSC or a B2B circuit, are used to verify the study and to prove the superior performance of the investigated and proposed technical concepts. Herein, more specifically for the re-configuration study of the parallel AC and DC links, the standalone mode control of the receiving-end VSC in the full DC link configuration is investigated and the smooth transition between grid-connected and standalone modes are realized in both simulation and experimental tests.

ACKNOWLEDGEMENTS

The thesis work has been conducted throughout the 9 months of my MSc thesis and it has been of great significance to me. It has been a fruitful time where I was able to publish my first academic paper. Additionally, I have learned to be more inquisitive and to enjoy the research on power electronics and its feedback control strategy. I particularly value the help from the experienced people that I had the opportunity to work with. The technical discussions and hands-on activities have definitely help me to grow from an academic and practice standpoints.

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Finally, I must express my very profound gratitude to my parents for supporting me mentally and financially throughout my life, especially the last two years. This accomplishment would not have been possible without them. Thank you.

Yang Wu
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LIST OF SYMBOLS

α, p_1	The parameter for the lead filter
$\bar{x}$	The averaged variable
$\Delta\omega_{res}$	The resonance band of the notch filter
δ_m	The phase increase of the lead filter
λ	The integer variable
ω	The fundamental angular frequency
ω_m	The frequency for the maximum phase increase in the lead filter
ω_n	The natural frequency of the closed loop system of the SRF-PLL
$\omega_{0,0}$	The anti-resonance frequency
ω_{ref}	The compensation frequency of the zero compensation
ω_{res}, f_{res}	The resonance frequency
τ	The time constant of the DC bus dynamics
θ	The phase of the three phase voltage
θ_0	The initial phase of the three phase voltage
$\widehat{m}_{a,b,c}$	The peak amplitude of the three phase modulation index
$\widehat{V}$	The peak amplitude of the voltage
ζ	The damping ratio of the closed loop system of the SRF-PLL
ζ_p, ζ_z	The damping factors in the notch filter
a_Δ	The attenuation of the notch filter at the border of the resonance band
$a_{\omega_{res}}$	The attenuation of the notch filter at the resonance frequency
C_f	The capacitance of the LCL filter
C_p	The DC link capacitor
C_n	The configuration of the parallel AC-DC system
d	The duty cycle
$D_{1,\ldots,6}$,	The anti-parallel diodes in three phase two-level VSC
e	The natural base

f_s The switching frequency of the PWM

$f_{\alpha,\beta}(t)$ The $\alpha\beta$ representation of the space phasor

$f_{a,b,c}(t)$ The balanced three phase quantities

$f_{d,q}(t)$ The dq representation of the space phasor

$F_{lead}(s)$ The transfer function of the lead filter

f_{res} The critical frequency

$G_d(s)$ The digital controller delay

$G_i(s)$ The closed loop transfer function of the current control

$G_p(s)$ The closed loop transfer function of the power control

$G_v(s)$ The compensator of the DC link voltage control

$G_c(s)$ The transfer function of the current controller

$G_{i_c}(s)$ The transfer function from AC terminal voltage to the converter side current

$G_{i_g}(s)$ The transfer function from AC terminal voltage to the grid side current

$G_{notch-PLL}(s)$ The transfer function of the notch filter in the SRF-PLL

$G_{PI}(s)$ The transfer function of the PI controller in the SRF-PLL

$G_{PLL}(s)$ The closed loop transfer function of the SRF-PLL

$G_{PWM}(s)$ The PWM delay

$H(s)$ The compensator in the SRF-PLL

i^*_{dq} The current references in dq frame

i_0 The zero-sequence circulating current

$i_{a,b,c}$ The three phase output currents of the VSC

I_{dc} The DC side current

$k(s)$ The compensator of the voltage controller in standalone mode control

k_p, k_i The proportional and integral gains for current controller

k_r The resonator gain

K_{ipll} The integral gain for the PI controller in the SRF-PLL

K_{ppll} The proportional gain for the PI controller in the SRF-PLL

k_{pwm} The modulation ratio

L The coupled inductance of the L_g and L_c

L_c The converter side inductance of the LCL filter

L_g The grid side inductance of the LCL filter

m The amplitude modulation index

$m_{a,b,c}(t)$ The three phase modulation index functions

N The total number of conductor links

N_{ac} The number of conductor links in AC operation

N_{dc} The number of conductor links in DC operation

P_s^* The active power reference

$P_{dc}(t)$ The DC side power

P_{ext} The DC side external power

$P_t(t)$ The AC terminal active power

Q_s^* The reactive power reference

$Q_{1,\ldots,6}$, The active switches in three phase two-level VSC

$Q_t(t)$ The AC terminal reactive power

R_c The converter side resistance of the LCL filter

R_d The damping resistor

R_g The grid side resistance of the LCL filter

$s(t)$ The switching function

$S_{1,2,\ldots,6}$, The switching signals for three phase two-level VSC

$s_{lower}(t)$ The switching function for switch in the lower bridge

$s_{upper}(t)$ The switching function for switch in the upper bridge

Sac_n The three phase AC switches

Sdc_n The ungrounded monopolar DC switches

T The digital control delay

T_d The digital controller delay time

T_s The switching period of the PWM

$V_{d,q}(t)$ The dq representation of the three phase voltage

V_{dc} The DC link voltage of the VSC

V_{gabc} The three phase grid voltage

$V_{ta,b,c}$	The three phase terminal voltages of the VSC
$x(t)$	The time dependent variable
$\overrightarrow{f}(t)$	The space phasor

1 INTRODUCTION

1.1 MOTIVATION

1.1.1 Hybrid AC-DC links system.

The difference of Alternating Current (AC) and Direct Current (DC) power transmission has been discussed over many years. AC transmission lines are widely used in modern power systems due to the easy control of voltage step-up and step-down by AC transformers [1]. However, DC transmission has many advantages over AC transmission. For instance, the DC transmission utilizes fewer number of conductors and requires smaller effective conductor cross-section compared with AC transmission because of better utilization of the conductor area (or absence of skin effect). Additionally, the effects of inductance, capacitance and phase angle displacement as well as the synchronizing problems which exist in AC transmission lines are not observed in the DC solutions. Thus, better voltage regulation in DC transmission lines are expected. In the past, the complexity and cost of DC transmissions have hindered its applications, however, recently these limitations have been gradually mitigated with the rapid development of power electronics and other enabling technologies [2, 3]. While High Voltage Direct Current (HVDC) lines have proven benefits in modern long-distance power transmission systems, in the medium-voltage distribution energy systems many people are skeptical. For example, the distribution network operators (DNOs) have difficulty in adopting DC-based infrastructures because these technologies are less mature than the existing AC grid infrastructure [4]. It has been identified in [4, 5] that greater power transfer capacity can be achieved without major modification of the original power grid by refurbishing the existing AC lines for DC operation, alongside other advantages in terms of efficiency and flexibility in power and voltage control. The enhancement of the power transfer capacity based on the refurbished DC links can offer an interesting solution to the rapidly growing power demand on the aging AC infrastructure.

Recent studies on hybrid (or parallel) point-to-point AC and DC distribution links, such as the one depicted in Fig.1.1, have shown interesting performance on capacity enhancement and superior energy distribution efficiency under specific operating conditions, particularly for high power, medium to high voltage level and moderate distribution distances, e.g. 5....20 km, [6]. Back-to-Back (B2B) Voltage Source Converters (VSCs) with long DC buried cables in-between the transmitting- and receiving-end substations are suitable solutions for the DC distribution.

In fact, the parallel operation of AC and DC lines was earliest considered in [7] for HVDC transmission because of the greater flexibility of DC transmission as well as rapid control of the combined system. Some difficulty and challenges have been explored in [8].

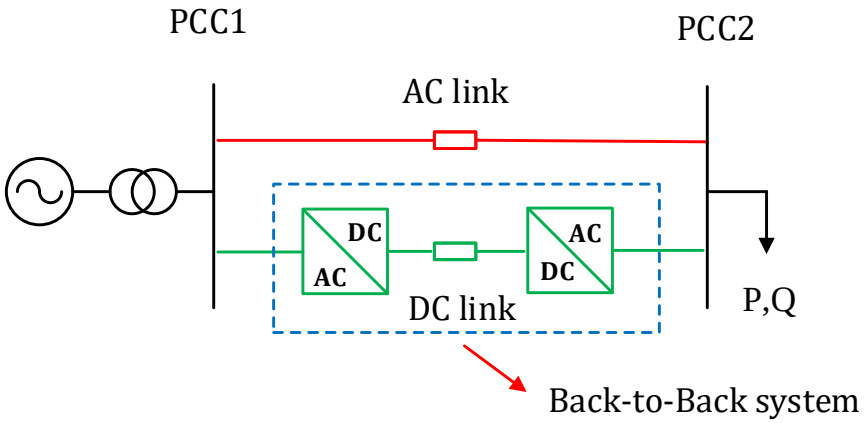


Figure 1.1: Basic concept of a Point-to-Point parallel AC-DC re-configurable links system.

1.1.2 Parallel AC and DC Re-configurable Links

As presented in [6], the optimal efficiency configuration in a parallel point-to-point AC and DC links varies according to the load demand and link/cable length, thus the distribution network can be manoeuvred on-line into an optimal configuration in terms of power transfer efficiency. The realization of the system re-configuration relies on the switching devices in both AC and DC links. Circuit breakers and disconnectors are suitable devices for this application. Compared to circuit breakers, switching power requirements for disconnectors is lower but they are of critical importance for substation and grid operation [9]. The use of disconnectors to transfer load currents between parallel conductors have been well documented and reported in [10, 11] The improved Gas-Insulated Switch-Gear (GIS) disconnectors [9] has revealed promising enhancement of the re-ignition behavior and increasing switching performance for bus-transfer switching cases. Such a performance is beneficial for the parallel AC and DC links system as this can be seen as an example of load bus transfer application. Hence, the use of parallel AC and DC re-configurable links system is feasible and it constitutes a promising MV application for future power distribution system.

The parallel AC and DC re-configurable links is the key component of the proposed system. Fig.1.2 shows such a energy distribution system implementing six conductor links. Herein, the link conductors are connected to the power electronics and grid through DC and AC feeders, where the reported GIS disconnectors can be adopted to realize improved switching performance. The conductor links are the aforementioned refurbished links which can be operated under both AC and DC conditions. DC power delivery is realized through the DC links once they are connected with the Back-to-Back power converters. The efficiency of the power transfer from complete usage of the DC links also strongly depends on the converters and their respective operational DC-link voltage. Modular Multilevel Converter (MMC) can be chosen as the power converters because

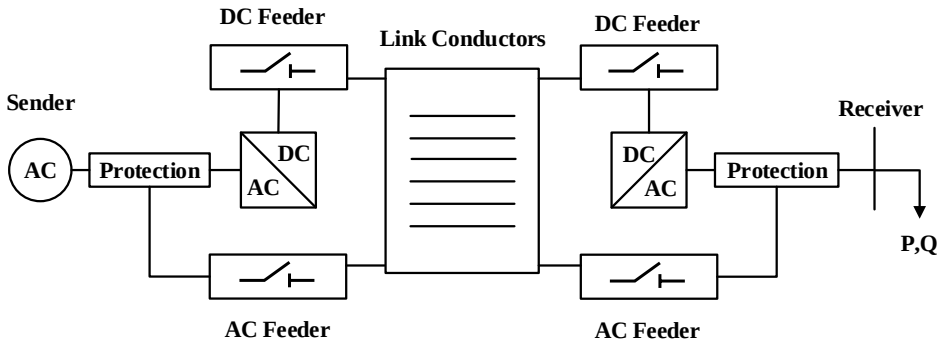


Figure 1.2: Parallel AC-DC re-configurable links system.

of its modularity, scalability, good harmonic performance and higher efficiency [12]. As shown in Fig.1.2, the DC links are connected to only one pair of power converters. For practical implementation of the parallel AC and DC re-configurable links, the choice of number of DC link converter pairs is associated with the desired DC link capacity and the power rating of converter itself, which is also related to the size and cost of the system. Thereby, the choice of DC link converters requires a combined consideration of converter rating, efficiency and cost [13]. Three phase two-level voltage-source converters (VSCs) is adopted in many AC medium and high power applications because of its simplicity and low cost [14]. In medium voltage applications, series connection of IGBTs could be used to achieve higher blocking voltage capability. Therefore, in this thesi, one pair of two-level VSCs is adopted as the back-to-back system.

1.1.3 Re-configuration Strategy

The re-configurations of the studied energy distribution system require the switch-on and -off actions of the adopted switches, for example, the GIS disconnectors or circuit breakers. The devices will experience large stress if they are triggered to be opened without creating a current-zero condition, which may deteriorate the lifetime of the switches and even create an undesired electric arc. In order to avoid this problem, this thesis proposes re-configuration strategies to provide nearly zero current switching condition in the cables to be disconnected. This is achieved by exploiting the power steering capability of the Back-to-Back VSCs when this is placed in parallel to a AC-link. To be more specific, the idea is to utilize the power controller of the receiving-end VSC to bring the power flow to zero across the links which are to be opened/closed during the desired re-configuration. Hence, the switches have relatively low current in their links while manoeuvring. The expected improved lifetime of the switches under zero current thus make the parallel AC and DC links system feasible for sustainable use and on-line re-configuration.

1.1.4 Control of LCL-filtered VSC under Grid Voltage Distortion Condition

Three-wire three-phase two-level VSC with LCL filter is adopted as building block converter for the DC links because of its high-frequency attenuation capability. The control of grid-connected LCL-filtered VSCs requires more sophisticated control when compared with VSCs employed in drives of motors/generators where equivalent single AC inductor filter exists. More specifically, in the former system instability problem can be caused by the LCL filter resonance and/or equivalent grid impedance. Moreover, in practice the grid voltage of energy distribution systems may contain low-order harmonics distortions, which can result in deteriorated waveform in both converter and grid side currents of the LCL filter. Therefore, current harmonics must be controlled under the range recommended by the newly revised IEEE Standard 519-2014. Above all, the precise power and DC link voltage controls for the three phase two-level VSC with LCL filter under grid distortion, should be investigated and realized to serve the proposed re-configuration strategy.

1.2 SPECIFIC OBJECTIVES

The objectives of this thesis are listed as follows:

- Achieve controlled sinusoidal grid side converter currents under distorted grid voltage in a parallel operating AC and DC link system.
- Improve the stability of the 2-level VSC under distorted grid voltage.
- Design a notch filter to avoid instability due to resonance associated with the LCL filter of the VSC.
- Develop harmonic resonators with proper phase compensation to improve converter performance under specific low order harmonics (or to improve the THD).
- Realize seamless transition between grid-connected and stand-alone mode control of the VSC.
- Implement online reconfigurations in hybrid AC and DC links system at near zero switching currents.

1.3 RESEARCH QUESTIONS AND CHALLENGES

The research questions and the corresponding challenges are:

1. What is the control method and associated gains necessary to achieve sinusoidal currents with low harmonic distortion under distorted grid voltages?

   Key Challenges:

   - Filter capacitor of the VSC acts as a sink for the grid harmonic voltages. Therefore, for the current feedback control loop of the power electronics the LCL

filter grid side current measurement is preferred over the inverter side current measurement. This choice can have a strong impact on the stable operation of the converter.

- While higher current control loop gain (or Gain Margin) can reject higher order harmonics in the LCL filter grid side current, its choice for stable operation is strictly limited according to the LCL resonance, semiconductor switching and digital sampling frequencies. This is particularly more severe for grid side current control under distorted grid voltage.
- The PLL (phase-lock loop) also influences the harmonics performance of the output current under a distorted grid voltage. For SRF-PLL, the design trade-off lies in the dynamic response and attenuation capability of harmonic components in the output frequency.

2. How to simultaneously improve the stability and output current performance of the VSC under distorted grid voltage?

   Key Challenges:

   - If the available control bandwidth does not adequately reject the current harmonics, the simultaneous improvement of harmonic performance and stability needs insight on the required bandwidth and unstable frequency points in the system. Both these aspects can vary according to the grid impedance, harmonic frequencies in the grid voltage and the converter component parameters.
   - Several passive and active damping methods are available. The choice for implementation should be made based on available flexibility in modifying the infrastructure, system efficiency and performance constraints.

3. What are the design parameters of the notch filter for improving the stability range of the VSC?

   Key Challenges:

   - While strong LCL filter resonance current attenuation by implementing active damping at theoretical unstable frequency points can make the system stable, the width of the studied notch filter strategy can reduce the closed loop gain in the required controller frequency bandwidth. This design trade-off should be explored in detail.
   - The converter and grid parameters that influence operational requirements and unstable regions can vary in practical scenarios. This aspect can put design constraints on achieving acceptable converter operational performance.

4. What are the harmonics resonator parameters for increasing the low order harmonics rejection capability of the VSC?

   Key Challenges:

   - While the grid impedance for the low order harmonics can be increased by adding control resonators, the phase reduction of such technique can hinder the feedback control's phase margin which may lead to system instabilities.

- While adding the phase compensation to the resonator can improve the phase reduction while maintaining the same low order harmonics rejection capability, the open loop gain at lower frequency ranges will be decreased by either lead-filter or zero compensation techniques.

5. What are the control strategy for the seamless mode transitions?

   Key Challenges:

   - The standalone mode operation requires a different control structure from grid-connected mode. The transition between the different controller can result in undesirable transients in the VSC system.
   - The interface of the LCL filter with the load leads to variation of the characteristics of the system control loop.

6. How to ensure a near zero r.m.s switching current during online re-configurations?

   Key Challenges:

   - The synchronization between the signals for the circuit switches and VSC mode control is required, otherwise it leads to the mismatch between the control and operation of the VSC.
   - The existence of zero-sequence circulating current in the parallel AC and DC system adds complexity in realizing near zero r.m.s switching current.

1.4 MAIN CONTRIBUTIONS

The first contribution in this thesis work is to implement the notch-filter based active damping in the grid-side current control together with the tuned resonant controller to remove the currents harmonics caused by grid voltage distortions and to realize a stable voltage and current control in the LCL-filtered two-level VSC.

The second contribution is the realization of the re-configuration of the parallel AC-DC system based on the control strategy to achieve nearly zero current transition in the links disconnecting switches.

1.5 THESIS STRUCTURE

Chapter 1 introduces the motivation and objectives of this thesis.

Chapter 2 reports the state-of-art of three phase two-level VSC and it also presents the control structure of the DC-link voltage and power controls, including the design of Synchronous Reference Frame - Phase-Locked Loop (SRF-PLL).

Chapter 3 presents the controller design based on the combined considerations of stability and harmonics performance. The instability problem caused by LCL filter resonance and the choice of controlled current (GCC or CCC) with regard to the delay influence are thoroughly discussed. Moreover, the current controller with notch filter is designed and

tested. Finally, the composite current controller with notch filter and harmonics control is verified in both simulation and experiments.

Chapter 4 studies the re-configuration of parallel AC and DC links system. The zero-sequence circulating current problem is solved by employing a PI-based ZSCC controller. Additionally, the standalone mode control strategy is presented and the transition between standalone and grid-connected modes is studied. These methods are validated in both simulation and experimental tests. Finally, the re-configuration strategy to provide almost zero current switching for the mechanical switches is realized in the parallel AC and DC re-configurable links system with nine link conductors in simulation.

Chapter 5 presents the conclusion of this thesis work and possible future works.

1.6 LIST OF PUBLICATIONS

- Y Wu, A. Shekhar, T. B. Soeiro and P. Bauer, "Voltage Source Converter Control under Distorted Grid Voltage for Hybrid AC-DC Distribution Links," *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society,* Lisbon. **(Accepted)**

- A. Shekhar, L. B. Larumbe, T. B. Soeiro, Y Wu and P. Bauer, "Number of Levels, Arm Inductance and Modulation Trade-offs for High Power Medium Voltage Modular Multilevel Converters," *2019 IEEE ECCE Asia Busan,* Korea. **(Accepted)**

- A. Shekhar, T. B. Soeiro, Y Wu and P. Bauer, "Optimal Power Flow Control in Parallel Operating AC and DC Distribution Links," *IEEE Trans. Ind. Electron* **(Submitted)**

2 CONTROL OF GRID CONNECTED TWO-LEVEL VSC

The Back-to-Back (B2B) system composed of two Voltage Source Converters (VSCs) are the fundamental circuit in the re-configurable hybrid AC and DC links. Herein, the conventional two-Level VSC is adopted because of its simplicity and robustness.

The objective of this chapter is to elaborate the control method of the grid-connected two-level VSC. Firstly, the averaged analytic model is introduced in order to describe the principle of operation of the circuit and to analyze the performance of the feedback control schemes commonly employed in VSCs. An improved SRF-PLL with mitigation of negative-sequence fundamental component in the grid voltage is described in this chapter. The power and DC-link voltage controls are described in terms of their equivalent control loop transfer function and respective circuit diagram in dq-frame.

2.1 TWO-LEVEL VOLTAGE SOURCE CONVERTER

2.1.1 Circuitry Structure

Figure 2.1 shows the circuit schematics of the three phase two-level voltage sourced converter. The circuit employs three identical half-bridge converters, which consists of two controllable power semiconductors with anti-parallel diodes. At the DC side of the VSC, two series connected DC pole capacitor are used to stabilize the DC voltage and to reduce its voltage ripples to an acceptable level for any connected DC load or DC power source. For analysis convenience, the mid-point of the two DC link capacitors is set as the voltage reference point o. Then the AC-side terminal voltage of the converter $V_{ta,b,c}$ represents the voltage difference between the mid-point of each half-bridge leg and the terminal o. This converter is called two-level VSC because during operation the generated terminal voltage can assume either $-V_{dc}/2$ or $V_{dc}/2$. The converter output currents $i_{a,b,c}$ flow into the AC system connected to the converter. Generally, filters are adopted between the 2-level VSC and the AC system. AC-side output current is equal to converter output current when a single L filter is used. However, LCL filter instead of a single L filter is chosen for this research because of its superior high frequency harmonics suppression performance. The implementation of LCL filter can bring control challenges in a digital controlled system, mainly because the controlled variable must be converted into a digital number with a limited sampling frequency. This is discussed in Section2.2. The 2-level VSC can operate as a STACOM (static synchronous compensator) [15]. This operation is possible when the DC bus is floating and the converter is absorbing or delivering reactive power to the interfaced AC system. This application will be introduced and implemented in Chapter 4. In inverter mode (or power flow from the DC- to the AC-side), a DC voltage source is connected to the DC-side terminals of the converter while its AC-side is either interfaced

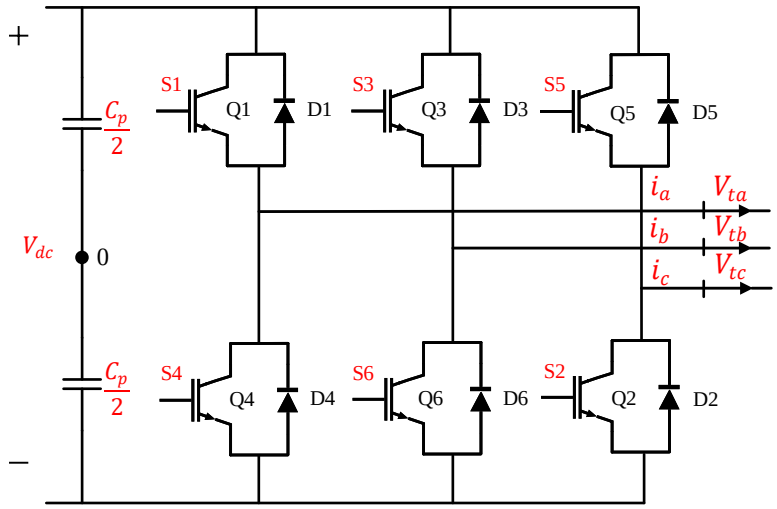


Figure 2.1: Circuity of the Two-level VSC.

with the grid or an AC load. The operation of VSCs in these two cases is called Grid-connected or Standalone mode, respectively. Both operational modes are required in the re-configurations of parallel AC and DC links. Grid-connected control is introduced in this chapter and Standalone mode control will be discussed in Chapter 4.

2.1.2 Principles of Operation

The 2-level VSC operates based on the switching states of the upper and lower active semiconductors. The switching function is defined as:

$$s(t) = \begin{cases} 1, & switch - on\ command \\ 0, & switch - off\ command \end{cases} \tag{2.1}$$

The switch-on and -off commands are typically generated through a pulse-width modulation (PWM) strategy, e.g. Sinusoidal Pulse-Width Modulation (SPWM) or Space-Vector Pulse-Width Modulation (SV-PWM). Most PWM techniques requires a carrier signal, i.e. a high frequency periodic triangular signal, and a modulating signal with a desired fundamental frequency and amplitude for generating the AC-side terminal voltage. The switching states are determined by comparing the carrier signal with the modulating signal and the intersections of them determine the switching instants. An example of switch signals for Q1 and Q4 is given in Fig.2.2. The switching signals for the active devices in a half-bridge leg are complementary, which has the relation $s_{upper}(t) + s_{lower}(t) \equiv 1$. The waveform of the AC-side terminal voltage is determined by the switching functions as shown in eqs. (2.2) and (2.3).

$$V_t(t) = \frac{V_{dc}}{2}(s_{upper}(t) - s_{lower}(t)) \tag{2.2}$$

$$s_{upper}(t) + s_{lower}(t) \equiv 1 \tag{2.3}$$

The bridge currents and power dynamics can be also derived based on the switching functions and these relations are called switched model. Switched model accurately describes the steady-state and dynamic behavior of the converter and also contains high-frequency component information [15]. If elaborated model of the switch cell is available, then the transients and instantaneous information in the VSC can be computed by an analytic model. Additionally, the high-frequency information is dispensable from the control point of view and dynamic analysis since the closed loop control of the VSC usually presents a low-pass characteristics. Herein, the averaged model is preferred when describing the converter dynamics [16].

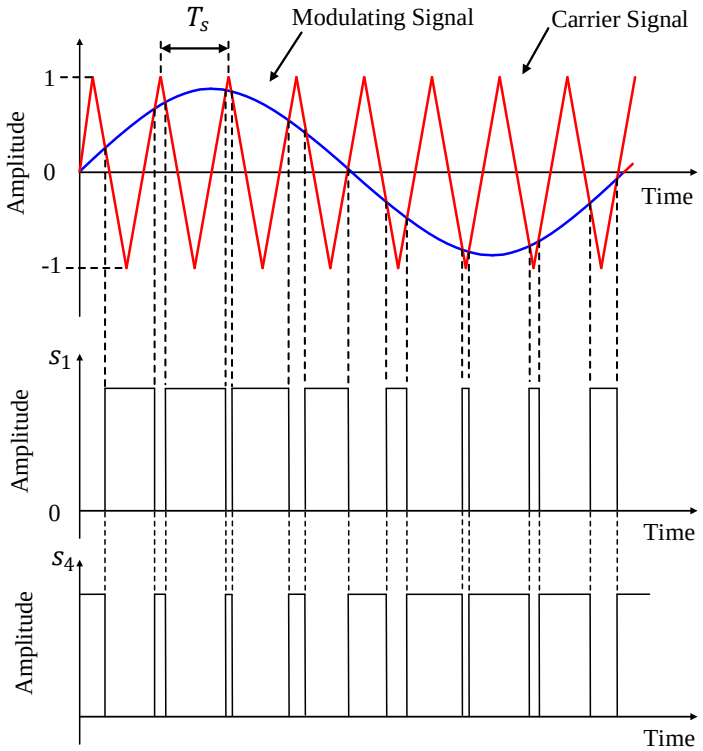


Figure 2.2: Signals based on the PWM switching strategy.

Therefore for dynamic analysis, the average of a time-dependent variable is defined as its integral average during one switching cycle, as eq. (2.4)

$$\bar{x} = \int_{t-T_s}^{t} x(\tau) d\tau \tag{2.4}$$

where $x(t)$ is the time-dependent variable and the over-bar denotes the averaged variable. The concept of averaging is introduced in many non-linear systems theory [17]and power electronics literature [18] and [16]. The periodical switched waveform generated by the PWM process will be a pulse waveform with constant duty cycle if a constant modulating

signal is applied, as shown in Fig.2.3. The symbol 'd' denotes the duty cycle and 'm' is the magnitude of the constant modulating signal. The following relation is identified:

$$m = 2d - 1 \tag{2.5}$$

If the averaging operator is applied to the switching function $s_1(t)$, then $\bar{s}_1(t) = d$ holds for the case of constant modulating signal. However, practically, in grid-connected ap-

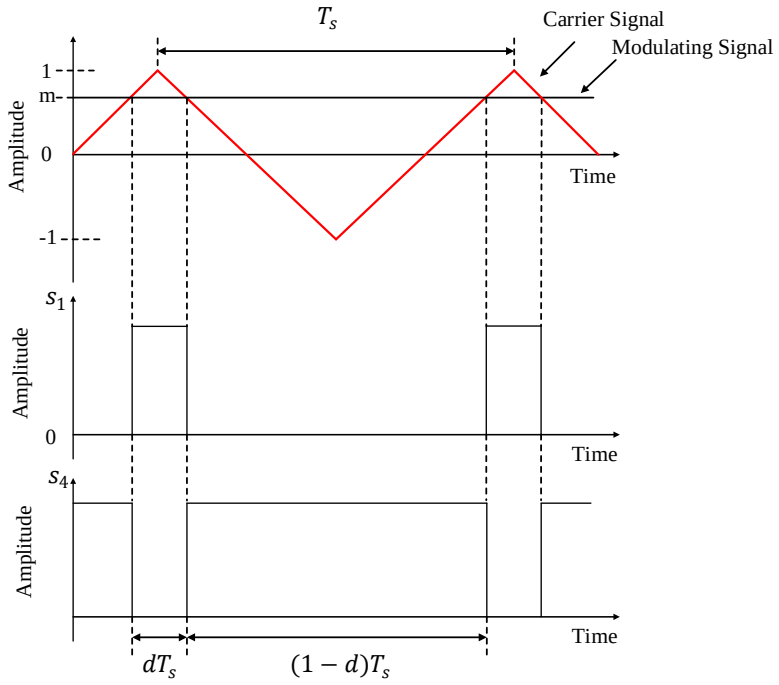


Figure 2.3: PWM with a constant modulating signal.

plications, the modulating signal is a sinusoidal waveform with fundamental frequency (50Hz or 60Hz), which implies that the generated switched waveform has different duty cycle in each switching cycle. Herein, eq. (2.5) can not be directly applied to the averaging of the switching function with sinusoidal modulating signal. A prerequisite is required here to allow one to include eq. (2.5) in this case, namely the frequency of the carrier signal must be sufficiently larger than that of the modulating signal. This is because the modulating signal during each switching cycle can be regarded as a nearly constant value if the switching frequency is far larger than the modulating signal frequency and then eq. (2.5) can give more accurate results. Generally, switching frequency will be chosen as at least 10 times larger than of that fundamental frequency. For example, during one switching period, eq. (2.4) can be applied to the switching functions $s_1(t)$ and $s_4(t)$, and the following equations are derived:

$$\bar{s}_1(t) = d \tag{2.6}$$

$$\bar{s}_4(t) = 1 - d \tag{2.7}$$

Based on the aforementioned assumption, in each switching period, eq. (2.5) holds for the duty cycle and the value of modulating signal in that period. Take the averaging process of both sides of eq. (2.3) and substitute in eq. (2.5), one gets:

$$\bar{V}_t = \frac{V_{dc}}{2}(2d - 1) = m\frac{V_{dc}}{2} \tag{2.8}$$

where duty cycle d can vary from 0 to 1 while m changes from -1 to 1. As eq. (2.8) illustrates, the magnitude of the averaged AC-side terminal voltage depends on the modulating signal magnitude when the DC link voltage is constant. These relations also apply to phase B and C legs in the two-level VSC. Considering the whole time scope of these averaged variables, the three phase AC-side terminal voltages are expressed as follows:

$$V_{t_a}(t) = m_a(t)\frac{V_{dc}}{2} = \widehat{m}_a sin(\omega t)\frac{V_{dc}}{2} \tag{2.9}$$

$$V_{t_b}(t) = m_b(t)\frac{V_{dc}}{2} = \widehat{m}_b sin(\omega t - \frac{2\pi}{3})\frac{V_{dc}}{2} \tag{2.10}$$

$$V_{t_c}(t) = m_c(t)\frac{V_{dc}}{2} = \widehat{m}_c sin(\omega t + \frac{2\pi}{3})\frac{V_{dc}}{2} \tag{2.11}$$

where ω is the fundamental angular frequency and the initial phase of the reference terminal voltage is assumed as zero. The DC-side and AC-side quantities of the three phase 2-level VSC are related to each other based on the power balancing, namely DC-side power equals AC-side power when the power losses are neglected:

$$V_{dc}(t)I_{dc}(t) = V_{t_a}(t)I_a(t) + V_{t_b}(t)I_b(t) + V_{t_c}(t)I_c(t) \tag{2.12}$$

where $I_{dc}(t)$ and $I_{a,b,c}(t)$ are the DC and AC-side currents, respectively. This relation is important as it is the bridge between the DC- and AC-side power and it will be used again for deriving the power dynamics of the DC-link voltage control. The averaged model of a non-ideal three phase 2-level VSC includes the effects of the switching and conduction losses of the IGBTs and anti-parallel diodes [15]. For simplicity, an ideal three-phase 2-level VSC is assumed here, i.e. linear switching devices and no losses.

2.2 MODEL AND CONTROL OF GRID-CONNECTED TWO-LEVEL VSC

2.2.1 Model in $dq-$Frame

The space phasor is the transformed representation of a balanced three phase system:

$$\overrightarrow{f}(t) = \frac{2}{3}[e^{j0}f_a(t) + e^{j\frac{2\pi}{3}}f_b(t) + e^{j\frac{-2\pi}{3}}f_c(t)] \tag{2.13}$$

where $\overrightarrow{f}(t)$ is the space phasor and $f_a(t), f_b(t), f_c(t)$ are the balanced three phase quantities. Based on the trigonometric identity and three phase balanced system identity:

$$cos\theta = \frac{1}{2}(e^{j\theta} + e^{-j\theta}) \tag{2.14}$$

$$e^{j0} + e^{j\frac{2\pi}{3}} + e^{\frac{-2\pi}{3}} \equiv 0 \tag{2.15}$$

One can derive:

$$\overrightarrow{f}(t) = \widehat{f}e^{j(\omega t+\theta_0)} \tag{2.16}$$

where ω and θ_0 are the fundamental angular frequency and the initial phase of the three phase balanced system, respectively.$\widehat{f}$ is the magnitude of the three phase quantities. The space phasor $\overrightarrow{f}(t)$ can be projected to the real and imaginary axis, respectively, and decomposed into two components:

$$\overrightarrow{f}(t) = f_\alpha(t) + jf_\beta(t) \tag{2.17}$$

Substituteeq. (2.16) into eq. (2.17), the two components can be written as:

$$f_\alpha(t) = \widehat{f}cos(\omega t + \theta_0) \tag{2.18}$$

$$f_\beta(t) = \widehat{f}sin(\omega t + \theta_0) \tag{2.19}$$

The space phasor is decoupled into frame with two orthogonal components and this frame is called $\alpha\beta$-frame (or stationary frame). The $\alpha\beta$-to dq-frame (rotating frame) is realized by shifting the space phase angle with $\theta(t)$ clock-wisely as eq. (2.20) shown:

$$f_d(t) + jf_q(t) = (f_\alpha(t) + jf_\beta(t))e^{-j\theta(t)} = \widehat{f}e^{j(\omega t+\theta_0-\theta(t))} \tag{2.20}$$

If $\theta(t)$ is chosen as ωt, then the space phasor is represented by two orthogonal DC quantities. Practically, $\theta(t)$ is chosen exactly as $\omega t + \theta_0$ and the q component becomes zero while the d component has a purely DC value. Vector control ($\alpha\beta$ or dq) is adopted in the three phase VSCs. While control in $\alpha\beta-$ frame can decouple the original system (three control loops) into two independent subsystems and track sinusoidal reference, the control in dq-frame can track DC references with simpler controller structure. Additionally, control in dq-frame adopts simple integrator in controller to achieve zero steady-state error instead of high order compensators in $\alpha\beta$-frame. Therefore, the control of three phase 2-level VSC will be discussed and analyzed in dq-frame. The dq-frame representations of the averaged model eqs. (2.9) to (2.11) are shown below:

$$V_{td}(t) = \frac{V_{dc}}{2}m_d(t) \tag{2.21}$$

$$V_{tq}(t) = \frac{V_{dc}}{2}m_q(t) \tag{2.22}$$

$$P_{dc}(t) = V_{dc}(t)I_{dc}(t) = P_t(t) = \frac{3}{2}[V_{td}(t)I_d(t) + V_{tq}(t)I_q(t)] \tag{2.23}$$

$$Q_t(t) = \frac{3}{2}[-V_{td}(t)I_q(t) + V_{tq}(t)I_d(t)] \tag{2.24}$$

The coefficient $\frac{3}{2}$ comes from the *Amplitude-invariant* transformation. The coefficient becomes 1 (one) when *Power-invariant* transformation is adopted [19]. The eqs. (2.21) to (2.24) constitute a control model for the two-level VSC as shown in Fig.2.4

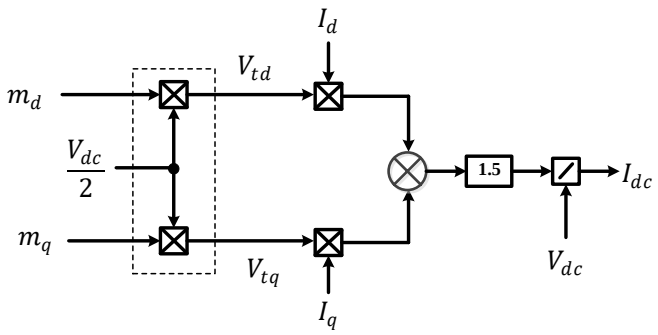


Figure 2.4: Control model for the ideal 2-level VSC.

2.2.2 Control of Grid-connected Three-Phase 2-level VSC

There are two main control methods for controlling the AC-side power: *voltage-mode control* and *current-mode control*. The first approach is widely used in high-power/voltage applications [20] and the AC-side power is controlled based on the angle and amplitude of the AC-side terminal voltage with respect to the Point of Common Coupling (PCC). *Current-model control* regulates the AC-side current with a current control loop while the power is controlled based on the generated angle and amplitude of the AC-side currents with respect to the amplitude and angle of the voltage at PCC. The *current-mode control* hence can protect the VSC against over-current and have better control precision.

The control of grid-connected 2-level VSCs includes two parts: power control and DC link voltage control, which corresponds to two different operating modes: Inverter mode (power flow from the DC- to AC-side - or DC/AC) and Rectifier mode (power flow from the AC- to AC-side - or AC/DC). The complete control diagram of a 2-level VSC in dq-frame is illustrated in Fig.2.5. Phase-Locked Loop (PLL) is required for grid-connected VSC control in both inverter and rectifier modes. The function of the PLL is to realize the synchronization of the converter generated output voltage with the grid in terms of frequency and initial phase. The PLL outputs the dq-frame currents and voltages for the controllers. The Inner current controller is the key part for controlling the AC-side current and, consequently the power flow. The output of the current controller is the generated voltage reference for the modulating signal in the PWM block, which produces the switching signals for the three-phase 2-level VSC. The outer voltage control loop regulates the error between the actual DC voltage and the reference value and its output is regarded as the d component of the reference current. In this diagram, the controlled variable is chosen as the grid-side current. Nevertheless, the converter-side current can be also chosen as the controlled variable. The choice of Grid-Side Current Control (GCC) and Converter-Side Current Control (CCC) is discussed in Chapter.3.

Phase-Locked Loop Design

Control of the currents in dq-frame is adopted because the control will be simplified into two decoupled subsystems, which means d and q components of the currents can be con-

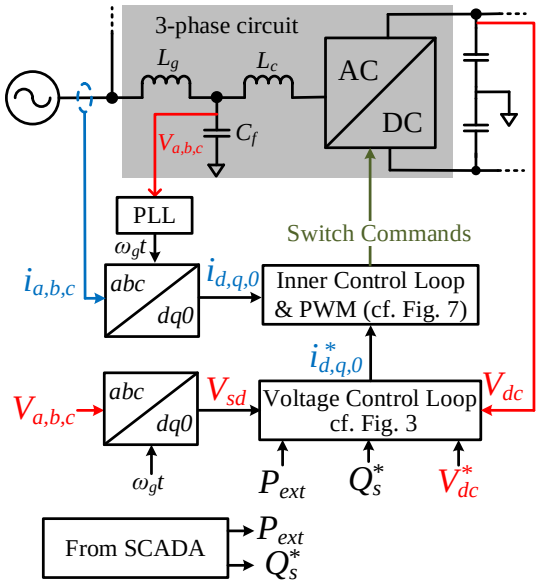


Figure 2.5: Control diagram of a grid-connected 2-level VSC.

trolled separately. Aside from this, the phase shift done by the $abc - dq$ transformation must be exactly the phase of the grid voltage, otherwise the power to current conversion is not properly decoupled and the active and reactive powers can not be independently controlled. Thereby, the grid voltage synchronization is indispensable to realize this objective. The most widely adopted PLL technique is the Synchronous Reference Frame-PLL (SRF-PLL) as shown in Fig.2.6. As shown in eq. (2.20), if $\theta(t)$ is controlled exactly as $\omega t + \theta_0$, one can obtain:

$$\begin{cases} V_d = \widehat{V} \\ V_q = 0 \end{cases} \tag{2.25}$$

The VCO is a re-settable integrator which nullifies its output whenever it reaches 2π. Commonly, the grid voltage has a distorted waveform with some low-order harmonics (e.g. 5^{th},7^{th} and 11^{th}) and V_d is not a purely DC value. Thus, a low-pass filter (LPF) is implemented to eliminate the harmonics components and to produce a DC value equal to the amplitude of grid voltage if amplitude-invariant transformation is used. The SRF-PLL regulates V_q in such a way that the V_q is controlled at zero, which means $\theta(t)$ is aligned with $\omega t + \theta_0$. If the SRF-PLL tracks the phase with a small error, V_q can be approximated as:

$$V_q = \widehat{V} sin(\omega t + \theta_0 - \theta(t)) \approx \omega t + \theta_0 - \theta(t) \tag{2.26}$$

From the control point of view, $\omega t + \theta_0$ is the reference and $\theta(t)$ is the actual variable. Hence, V_q is approximated as the error input of the control system and the closed loop transfer function of the SRF-PLL is depicted in Fig.2.7. The term ω is regarded as a disturbance. The compensator should be designed in such a way that the closed loop system can fulfill: 1) zero steady-state error tracking 2) enough phase margin (PM).

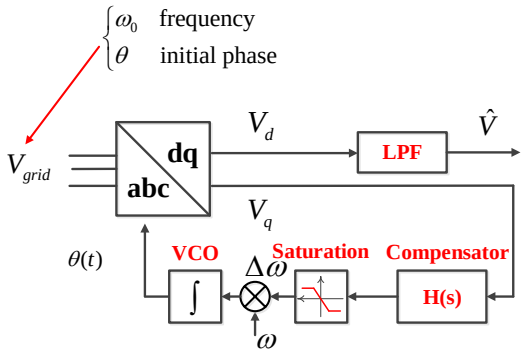


Figure 2.6: Schematic diagram of the conventional SRF-PLL.

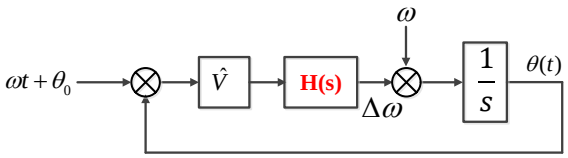


Figure 2.7: The closed loop transfer function of SRF-PLL.

The design of the compensator is straightforward since the open loop gain has already one integral element. From the control theory [21], at least two integral elements are required for the open loop gain to realize the zero steady-state error when the input is a ramp function of time. Therefore, the compensator must include one integral. PI control is recommended here since it includes one pole at origin. Thus the closed loop transfer function of the SRF-PLL can be written as:

$$G_{PLL}(s) = \frac{\frac{\hat{V}}{s}G_{PI}(s)}{1+\frac{\hat{V}}{s}G_{PI}(s)} = \frac{\hat{V}G_{PI}(s)}{s+\hat{V}G_{PI}(s)} \tag{2.27}$$

where $G_{PI}(s)$ is defined as:

$$G_{PI}(s) = K_{ppll} + \frac{K_{ipll}}{s} \tag{2.28}$$

Substitute eq. (2.28) into eq. (2.27), the closed loop transfer function becomes:

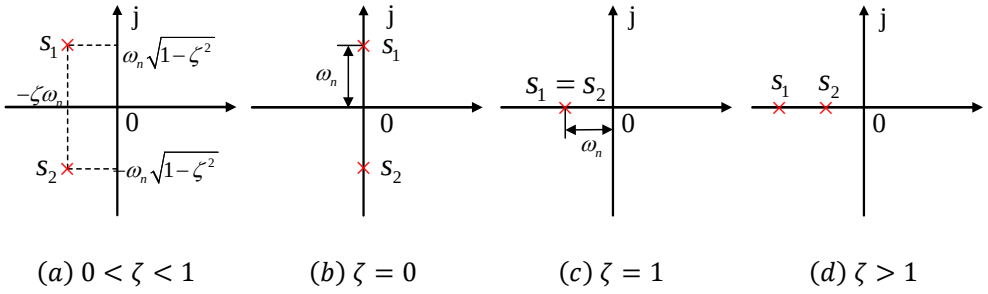
$$\begin{aligned} G_{PLL}(s) &= \frac{\hat{V}K_{ppll}s + \hat{V}K_{ipll}}{s^2 + \hat{V}K_{ppll}s + \hat{V}K_{ipll}} \\ &= \frac{2\zeta\omega_n s + {\omega_n}^2}{s^2 + 2\zeta\omega_n s + {\omega_n}^2} \end{aligned} \tag{2.29}$$

where $\omega_n = \sqrt{\hat{V}K_{ipll}}$ and $\zeta = \frac{K_{ppll}\sqrt{\hat{V}}}{2\sqrt{K_{ipll}}}$. The closed loop transfer function can be written in standard form of a second order system. The system is stable if the two poles of the

closed loop transfer function are located in the Left-Half Plane (LHP). The two poles are solved as:

$$s_{1,2} = -\zeta\omega_n \pm \omega_n\sqrt{\zeta^2 - 1} \tag{2.30}$$

The natural frequency ω_n is larger than zero and the damping ratio ζ has different possible values depending on the choice of K_{pll}. The possible distribution of poles in the s-Plane is depicted in Fig.2.8. The closed loop system is marginally stable without damping when



$(a)\ 0 < \zeta < 1$ $(b)\ \zeta = 0$ $(c)\ \zeta = 1$ $(d)\ \zeta > 1$

Figure 2.8: Poles of the closed loop transfer function of the SRF-PLL.

only an integrator is used for compenastor. Practically, the system is unstable without any other phase compensation methods under this case. In the over-damped condition ($\zeta > 1$), the response of the closed loop system is quite slow compared with the under-damped condition. Generally, the PI controller parameters should be chosen in such a way that the closed loop transfer function of the SRF-PLL has an under-damped characteristics. The dynamics performance e.g. overshoot and rise time can be adjusted by changing the PI parameters to strategically locate the two conjugate poles [21]. Since the SRF-PLL closed loop system is stable with a PI compensator, the phase margin and the bandwidth are the merits of tuning for the design of the compensator. The natural frequency ω_n is related to the closed loop bandwidth when optimal damping ratio $\zeta = 0.707$ is chosen according to [22]. The bode plot of the open loop transfer function of the SRF-PLL with different parameters and the closed loop bandwidth are shown in Fig.2.9 and 2.10. With the higher natural frequency, the phase margin remains the same while the bandwidth increases.

SRF-PLL can achieve satisfactory performance provided that the grid voltage contains negligible low order harmonics [23]. However, grid voltage inevitably has some harmonic components or negative sequence components under unbalanced condition. Therefore, another important consideration in designing the compensator is the mitigation ability of harmonics and negative sequence components in the PLL output variables V_d and V_q. Without the mitigation of the grid distortion, the outputs of the PLL: $\theta(t)$ and $\Delta\omega$ will have the fluctuations due to the harmonics and negative sequence components [24], which will be passed onto the the current control.

Since SRF-PLL generally exhibits a low-pass characteristics as shown in Fig.2.10, the high frequency components can be attenuated effectively if the closed loop bandwidth is selected properly. The component of the fundamental negative sequence is of concern because the magnitude of this component is much larger than the other harmonics and it can

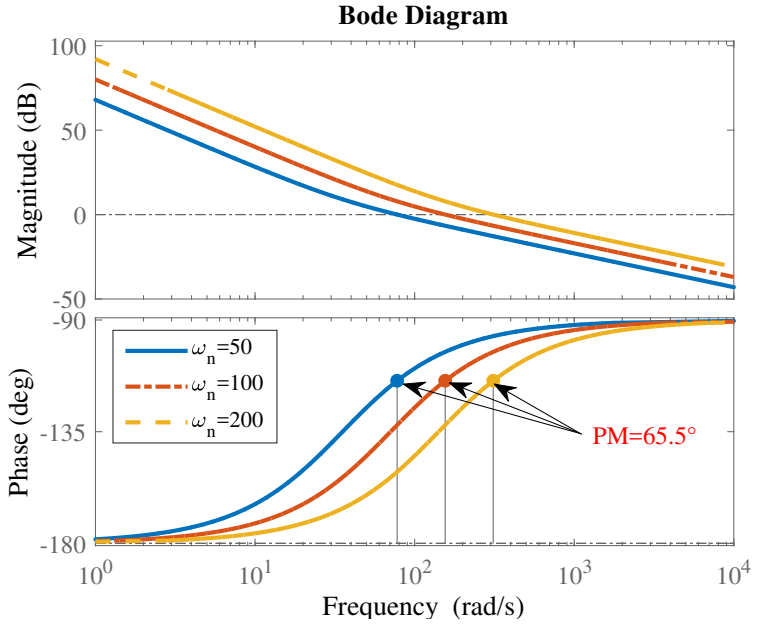


Figure 2.9: Bode plot of open-loop transfer function of SRF-PLL with different ω_n.

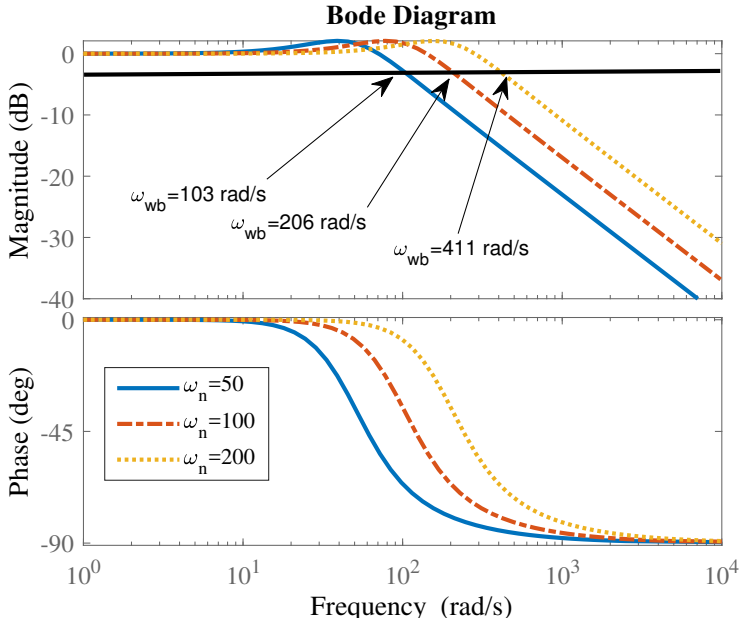


Figure 2.10: Bode plot of the closed loop transfer function of SRF-PLL with different ω_n.

be further enlarged during a fault such as phase-to-ground fault. Assume that V_{gabc} represents an unbalanced grid voltage with a negative-sequence fundamental component,as given in eq. (2.31).

$$\begin{aligned} V_{ga}(t) &= \widehat{V}cos(\omega t + \theta_0) + k_1\widehat{V}cos(\omega t + \theta_0) \\ V_{gb}(t) &= \widehat{V}cos(\omega t + \theta_0 - \frac{2\pi}{3}) + k_1\widehat{V}cos(\omega t + \theta_0 - \frac{4\pi}{3}) \\ V_{gc}(t) &= \widehat{V}cos(\omega t + \theta_0 - \frac{4\pi}{3}) + k_1\widehat{V}cos(\omega t + \theta_0 - \frac{2\pi}{3}) \end{aligned} \tag{2.31}$$

where k_1 is the amplitude of the negative-sequence fundamental component. Based on eqs. (2.13) and (2.20), one can deduce the space phasor representation of the grid voltage and the dq-frame representation assuming that the SRF-PLL works in steady-state, which means $\theta(t) = \omega t + \theta_0$. The space phasor form is

$$\overrightarrow{V_g} = \widehat{V}e^{j(\omega t+\theta_0)} + k_1\widehat{V}e^{-j(\omega t+\theta_0)} \tag{2.32}$$

The dq-frame representation is

$$\begin{aligned} V_{gd} &= \widehat{V} + k_1\widehat{V}cos(2\omega t + 2\theta_0) \\ V_{gq} &= -k_1\widehat{V}sin(2\omega t + 2\theta_0) \end{aligned} \tag{2.33}$$

This implies that the negative-sequence component becomes a fluctuation with twice fundamental frequency after the $abc - dq$ transformation. There are two possible approaches to eliminate this component in the PLL output. The first approach is to design a SRF-PLL in such a way that the closed loop system has strong low-pass characteristics to reject the frequency 2ω, which means the bandwidth has to be sacrificed. Another method is to adopted Decoupled Double Synchronous Reference Frame PLL (DDSRF-PLL), which has a decoupling network consisting of two separate SRF-PLL for positive and negative-sequence components [25]. To avoid the complicated structure, a notch-filter with the anti-resonance frequency at 2ω can be added to the basic SRF-PLL to eliminate the negative-sequence fundamental component, as shown in eq. (2.34)

$$G_{notch-PLL}(s) = \frac{s^2 + 2 * \zeta s + (2\omega)^2}{(s + 2\omega)^2} \tag{2.34}$$

This notch filter provides two conjugate zeros at 2ω and the double frequency component oscillation will be "notched". The coefficient ζ is used to adjust the anti-resonance peak of the notch filter. Note that the phase margin of the SRF-PLL will be greatly influenced by the notch filter, hence it may require a phase compensation method for suggested stability. A lead filter can be adopted here to increase the phase margin of the SRF-PLL with the notch filter [26]. A simple lead filter can provide a maximum phase increase of 90° and it is generally described as:

$$F_{lead}(s) = \frac{s + (p_1/\alpha)}{s + p_1} \tag{2.35}$$

where

$$\begin{aligned} \delta_m &= \arcsin\frac{\alpha - 1}{\alpha + 1} \\ \omega_m &= \frac{p_1}{\sqrt{\alpha}} \end{aligned} \tag{2.36}$$

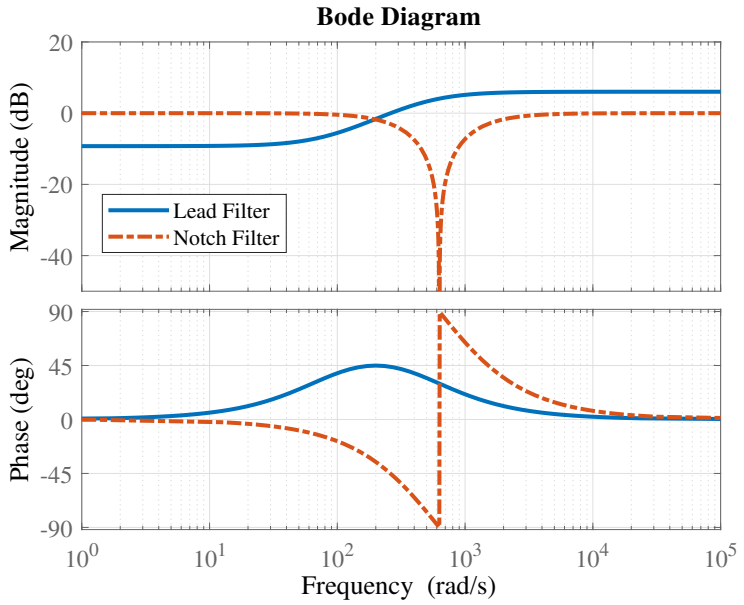


Figure 2.11: Bode plot of the notch and lead filters.

where δ_m is the maximum phase of the lead filter and it occurs at frequency ω_m. Fig.2.11 shows the frequency response of the notch and lead filters. The bode plot of the open and closed loop transfer function of the modified SRF-PLL is presented in Fig.2.12 and 2.13. The bandwidth of the modified SRF-PLL does not change significantly while maintaining enough phase margin and rejecting the negative-sequence fundamental component. In fact, the notch filter can be added at the harmonic frequency to mitigate the influence of the low order harmonics distortion from the grid voltage. The relation between the controller parameter ω_n and thedynamic response of the PLL to the frequency change is verified in the simulation result (Fig.2.14). The grid voltage experiences a 0.5 Hz step down of the frequency at 2 s. The results shows that the SRF-PLL with higher natural frequency has faster response to the frequency change. Therefore, the SRF-PLL controller with higher natural frequency (also bandwidth) is desirable as it can quickly respond to the frequency variation of the grid voltage. The simulation and experimental tests are done in MATLAB/SIMULINK to verify the harmonics mitigation capability of the proposed SRF-PLL under a distorted voltage source (see Table.3.2)

Fig.2.16 and 2.17 show the simulation results of the output frequency of the SRF-PLL with and without notch filter for different PI parameters. The distorted grid in simulation is shown in Fig.2.15 and the main harmonics are the 5^{th} and 7^{th} components.

The results show that with a larger ω_n, the SRF-PLL has worse mitigation capability of the harmonics influence from the distorted grid. The implementation of the notch filter at 6^{th} fundamental frequency can significantly reduce the harmonics ripple in the output frequency.

Fig.2.19 and 2.20 show the experimental results of the output frequency of the SRF-PLL with and without notch filter for different PI parameters. The distorted grid is shown

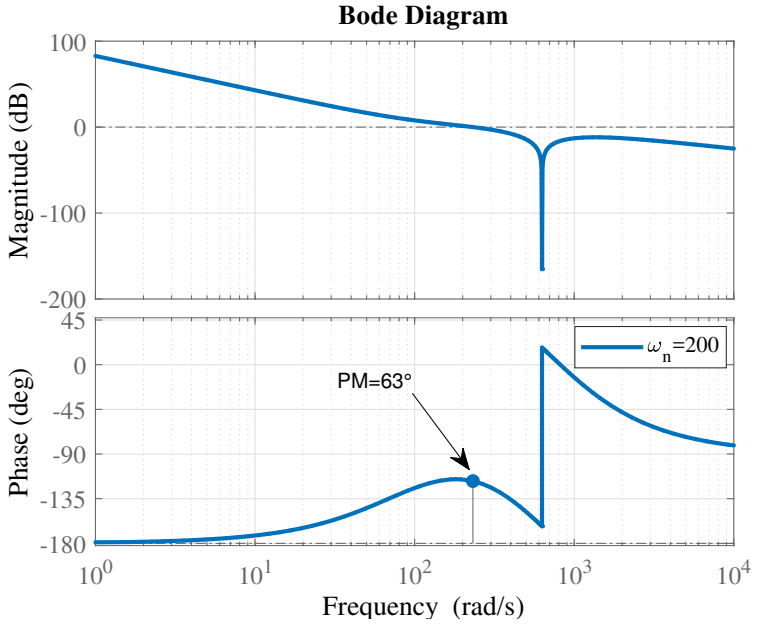


Figure 2.12: Bode plot of the open-loop transfer function of the modified SRF-PLL.

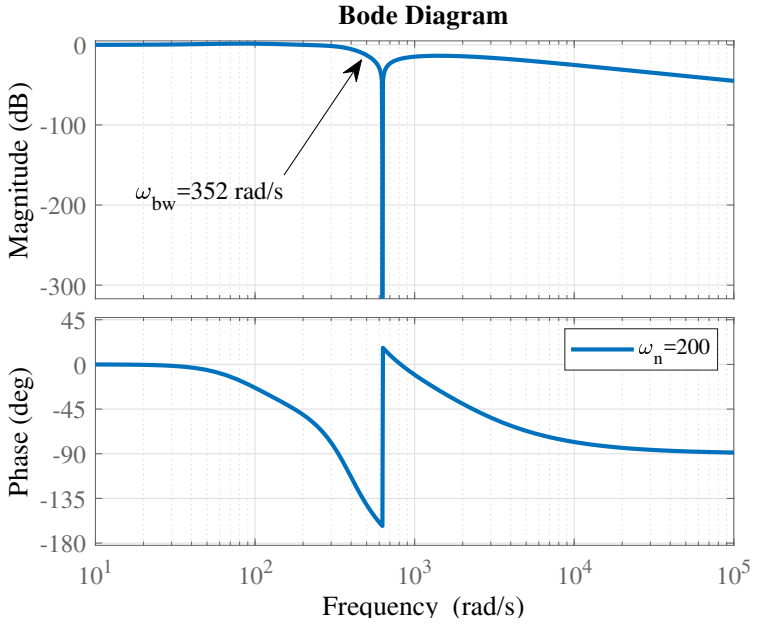


Figure 2.13: Bode plot of the closed loop transfer function of the modified SRF-PLL.

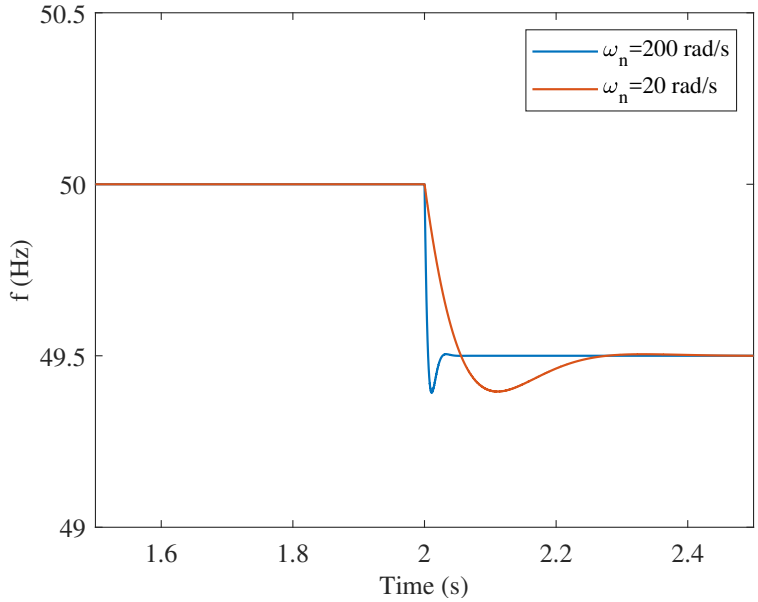


Figure 2.14: Dynamic response of SRF-PLL to the frequency drop of the grid voltage.

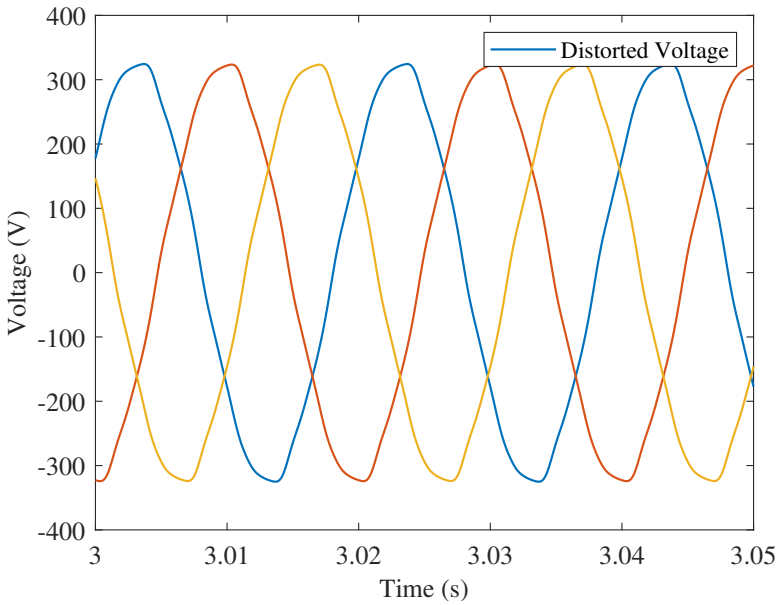


Figure 2.15: Distorted grid voltage in the simulation.

in Fig.2.18. The experimental results also validated that the basic SRF-PLL (PI control only) does not have a good harmonics rejection capability. In order to achieve smaller harmonics ripple in the output frequency with basic SRF-PLL, a smaller bandwidth should

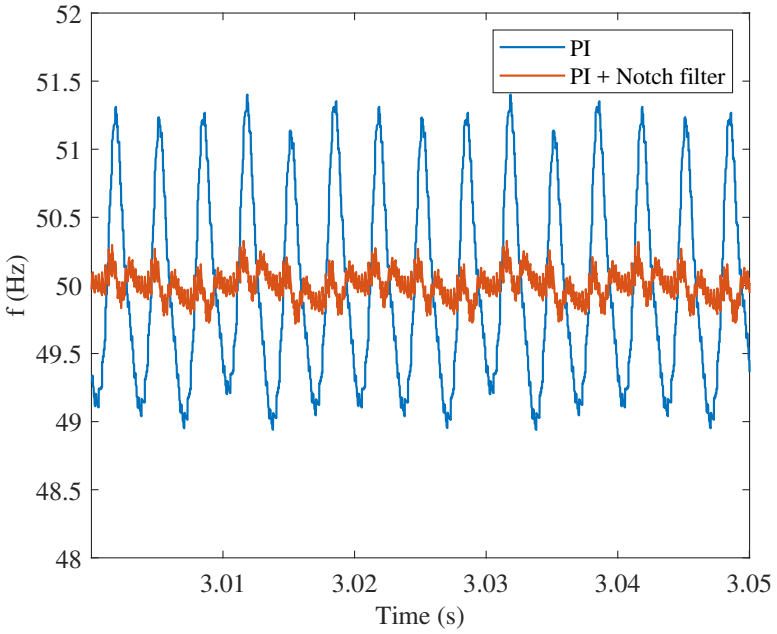


Figure 2.16: Simulation test of proposed SRF-PLL with ω_n=200 rad/s: output frequency.

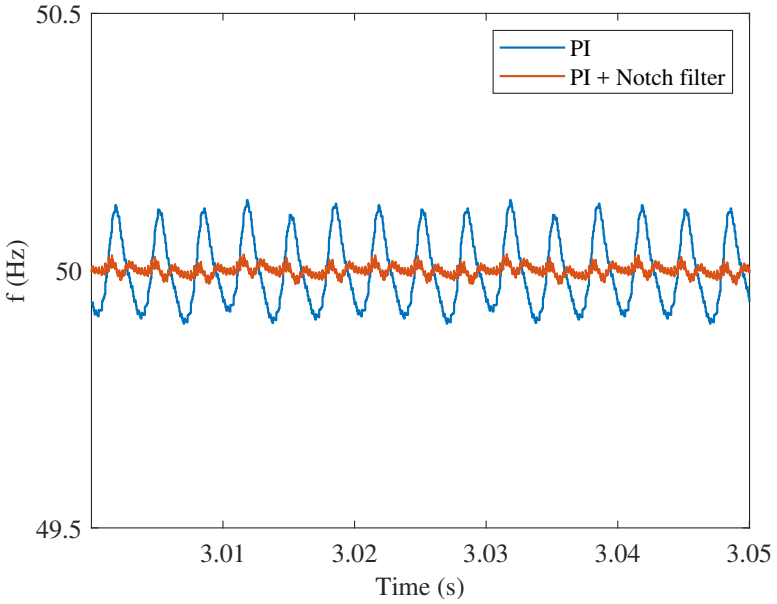


Figure 2.17: Simulation test of proposed SRF-PLL with ω_n=20 rad/s: output frequency.

be chosen. The SRF-PLL with notch filter can effectively reduce the harmonics in the output frequency.

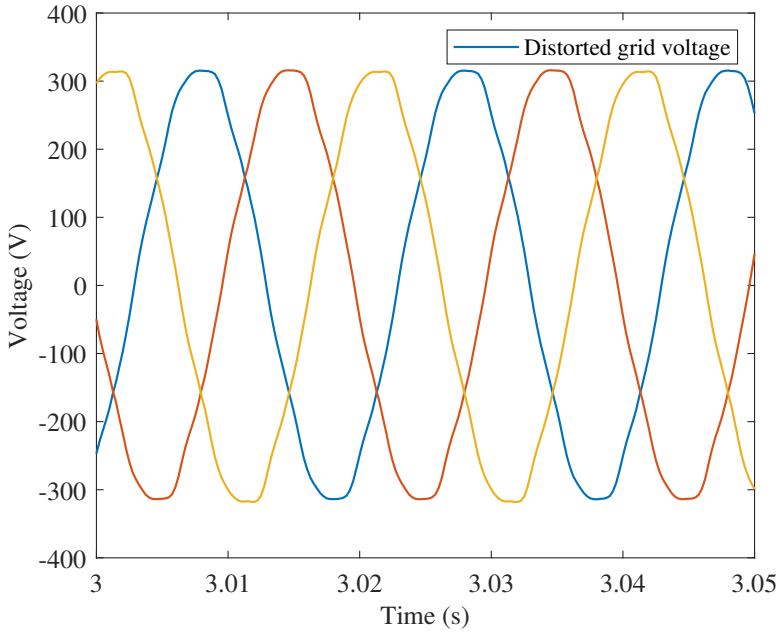


Figure 2.18: Distorted grid voltage in the experiment.

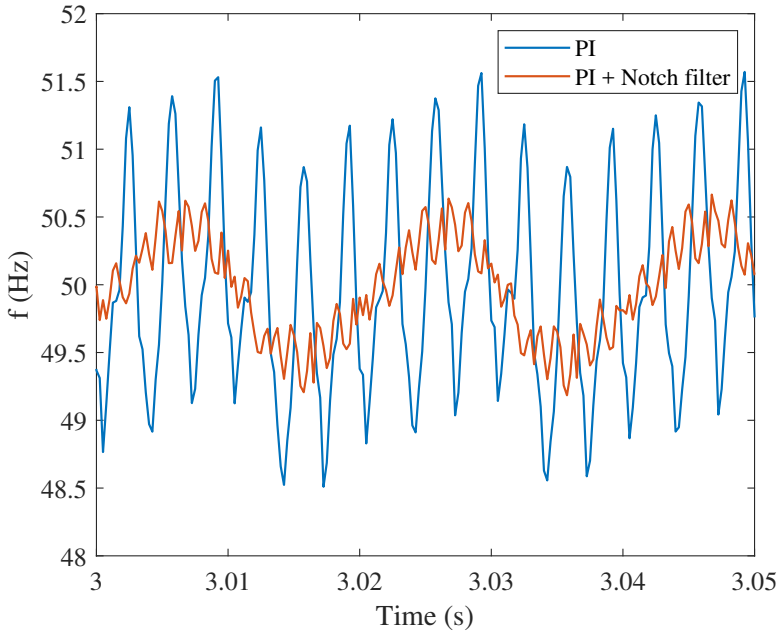


Figure 2.19: Experiment test of the proposed SRF-PLL with ω_n=200 rad/s: output frequency.

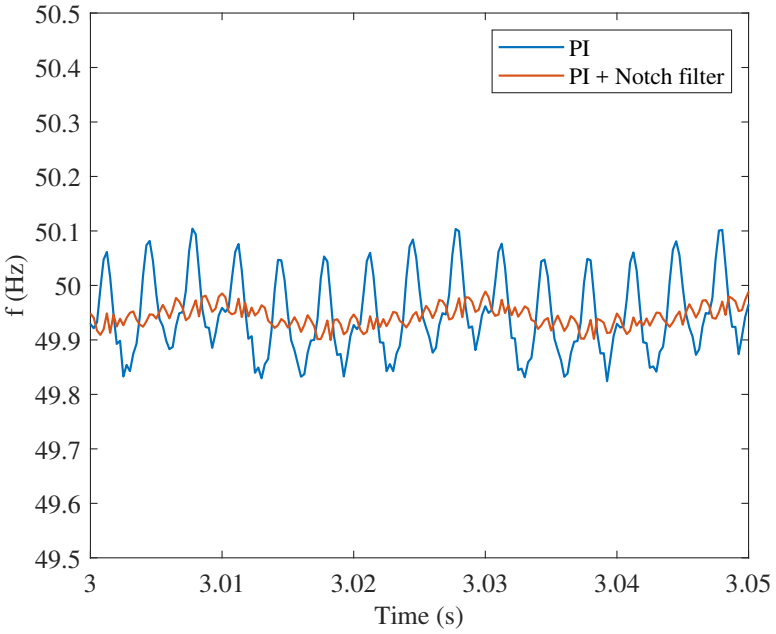


Figure 2.20: Experiment test of the proposed SRF-PLL with ω_n=20 rad/s: output frequency.

Power Control

Provided that SRF-PLL works in steady-state condition, the current control loop is equivalent to power control loop because the active power and reactive powers are decoupled into separated control of d and q components of the controlled current based on eqs. (2.23) to (2.25). The power references can be converted into current references according to eqs. (2.37) and (2.38)

$$i_d^* = \frac{2}{3V_{gd}} P_s^* \tag{2.37}$$

$$i_q^* = -\frac{2}{3V_{gd}} Q_s^* \tag{2.38}$$

The simplified current control loop without detailed power plant is shown in Fig.2.22.$G_c(s)$ is the current controller and a PI control is adopted for $G_c(s)$ in dq-frame:

$$G_c(s) = k_p + \frac{k_i}{s} \tag{2.39}$$

$G_d(s)$ represents the digital controller delay due to sampling and computation:

$$G_d(s) = e^{-sT} \tag{2.40}$$

where T is the digital controller sampling period.(i.e., $T = T_s = \frac{1}{f_s}$) is applicable for typical digital implementations [27]. $G_{inv}(s)$ is the transfer function of the PWM modulator

and is called PWM delay. The PWM delay is approximately modelled as a zero-order-holder (ZOH) and G_{inv} can be mathematically derived by eq. (2.41) if synchronous PWM sampling is considered [28]:

$$G_{inv}(s) = \frac{1}{T_s}\frac{1-e^{-sT_s}}{s}k_{pwm} \approx k_{pwm}e^{-0.5sT_s} \tag{2.41}$$

where k_{pwm} is the ratio between DC voltage and the amplitude of the triangular carrier. The single sampling and update of the digital controller in PWM process is illustrated in Fig.2.21. The control delay results in the time difference, which is labeled k in Fig.2.21. The total delay in the current control loop becomes $1.5T_s$ when single update is adopted.

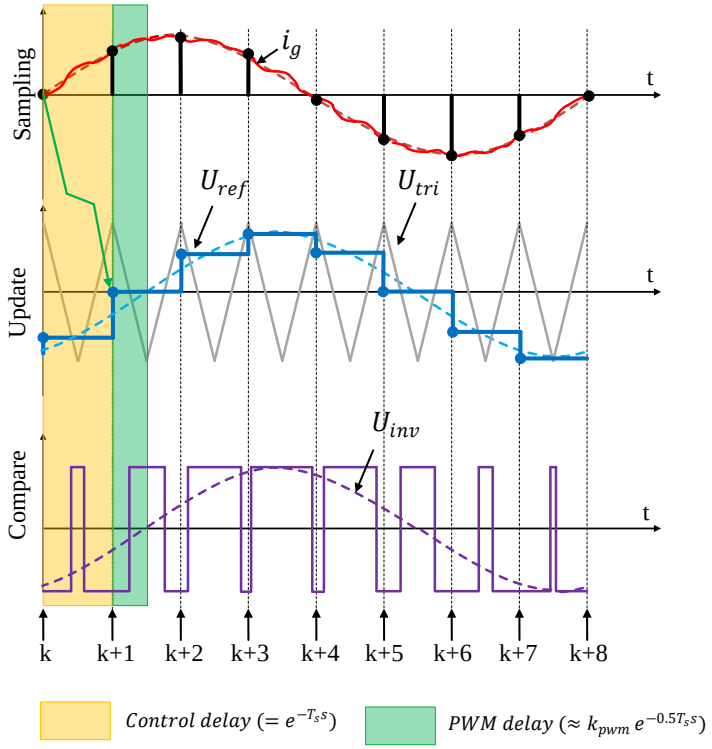


Figure 2.21: Digital controller delay and PWM zero-order hold effect (single update).

The grid voltage feed-forward is adopted in the current control to improve dynamic response of current to grid voltage disturbances [29]. The control diagram in dq-frame is illustrated in Fig.2.23. As it can be observed from the control diagram, a PI controller is used for the current loop compensator and i_d, i_q are fed to the compensator output to decouple the dq-frame. SPWM technique is adopted in this thesis for the VSC modulation. The controlled current can be either grid-side current or converter-side current in the VSC with LCL filter. The choice of controlled current and the parameters design are discussed in Chapter.3.

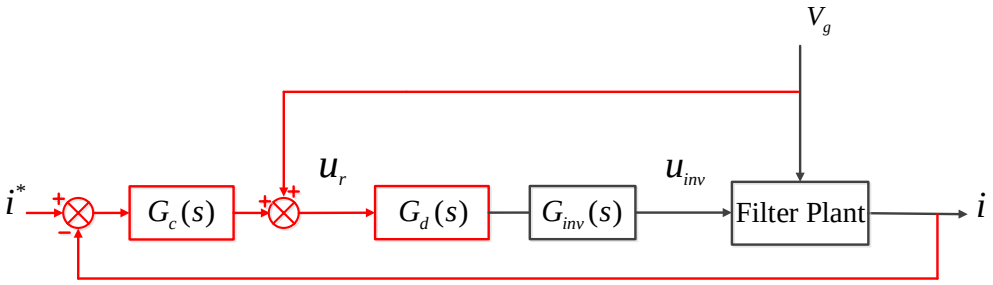


Figure 2.22: Simplified current loop transfer function.

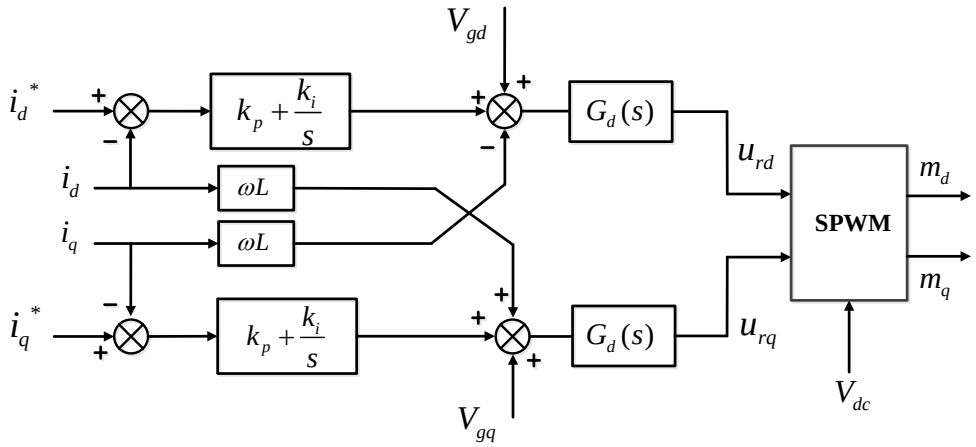


Figure 2.23: Current control diagram in dq-frame.

DC-link Voltage Control

The control loop for the DC bus voltage consists of two parts: the voltage controller and composite control plant or power control loop cascaded with the DC-bus dynamic block. The control loop transfer function is presented in Fig.2.24. The voltage controller regulates V_{dc}^2 and generates the active power reference through the compensator $G_v(s)$ which is usually represented by a PI control. The compensator has a negative sign to compensate the negative sign in the DC bus voltage dynamics. C_p is the DC pole capacitor value and τ is the time constant of the DC bus dynamics which is proportional to the product of AC side inductance of the VSC and the steady-state real power flow. For low power applications, τ is negligible and the DC-bus power plant can be approximated as an integral term. The power controller dynamics $G_p(s)$ is the closed loop transfer function of

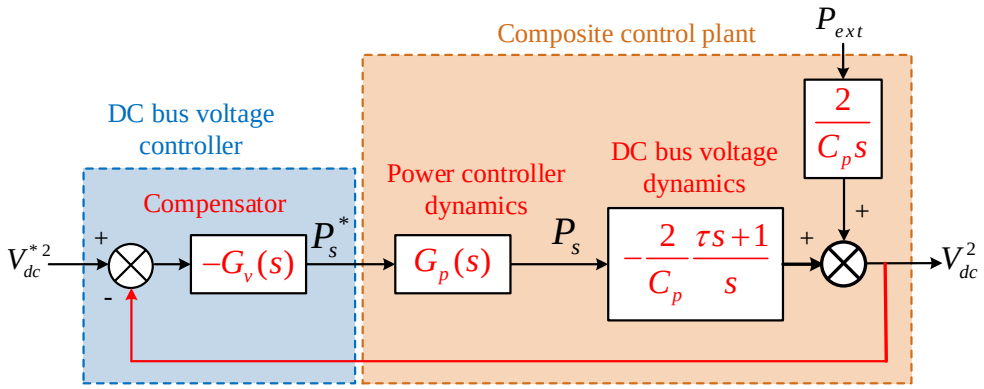


Figure 2.24: DC bus voltage control loop transfer function.

power loop, which is equivalent to the closed loop transfer function of the current control ($G_i(s)$) loop as shown in eq. (2.42).

$$\begin{aligned} P_s(s) &= G_p(s)P_s{}^*(s) \\ I_d(s) &= G_i(s)I_d{}^*(s) \end{aligned} \tag{2.42}$$

Based on eqs. (2.23), (2.24), (2.37) and (2.38), dividing both sides of the first line of eq. (2.42) with $\frac{3}{2}V_{gd}$, one obtains

$$I_d(s) = G_p(s)I_d{}^*(s) \tag{2.43}$$

Therefore, $G_i(s) = G_p(s)$. The DC voltage controller structure is illustrated in Fig.2.25. The DC side external power is fed forward to the DC voltage controller to improve the dynamic response when the external power source suddenly changes. A saturation block is indispensable for limiting the power reference in order to protect the system from the over-current.

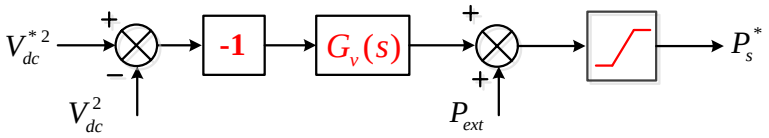


Figure 2.25: DC bus voltage controller diagram.

Generally, the voltage controller should be designed in such a way that the response speed of the current control loop is at least 10 times faster than that of the voltage control loop. Otherwise, the voltage control can not be fully decoupled from the current control loop.

3 CONTROLLER DESIGN FOR LCL-FILTERED VSC WITH DISTORTED GRID VOLTAGE

The previous chapter describes the general vector control of a 2-level VSC connected with the grid. The power and DC link voltage controller design is not straightforward due to the resonance in the LCL filter. This resonance can lead to instability of the control, especially when grid-side current control (GCC) is chosen. Practically, the grid voltage inevitably has some low order harmonics, especially 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonics. GCC can lead to better attenuation performance of these low order harmonics. This chapter goal is to propose a Notch filter-based active damping method to improve the stability of the GCC scheme. The choice of GCC and CCC (converter-side current control) is also investigated. PIR (PI+Resonators) based harmonics control is proposed in this chapter to mitigate the harmonics in the grid side current resulted by distorted grid voltage. Lead filter is also adopted to improve the phase margin when harmonics controller is used. The controller design is based on the circuit parameters of the available 2-level VSC in laboratory. The complete control method is validated in both simulation and experimental tests.

3.1 CONTROL OF LCL-FILTERED VSC

3.1.1 Influence of LCL Filter

With a LCL filter between the converter AC-side terminals and the grid, the control plant of the current loop becomes significantly different compared with a L-filtered VSC. A single-phase grid-connected VSC with LCL filter is depicted in Fig.3.2 Based on the circuit, the following relations are derived:

$$\begin{aligned} V_t(t) &= V_C(t) + L_c\frac{di_c(t)}{dt} + i_c(t)R_c \\ V_C(t) &= V_g(t) + L_c\frac{di_g(t)}{dt} + i_g(t)R_g \\ i_C(t) &= C_f\frac{dV_C(t)}{dt} \end{aligned} \tag{3.1}$$

where i_g, i_c and i_C are the grid-side, converter-side and capacitor current respectively. V_g and V_t are the grid and AC-side terminal voltage of the VSC. R_g and R_c are the internal

resistors in the filter inductors L_g and L_c. Rewriting the relations in laplacian form (s-form), one can obtain the transfer functions:

$$G_{i_{c-d}}(s) = \frac{i_c(s)}{V_t(s)} = \frac{s^2 C_f L_g + s C_f R_g + 1}{s^3 C_f L_g L_c + s^2 C_f (L_c R_g + L_g R_c) + s(C_f R_g R_c + L_g + L_C) + R_c + R_g} \tag{3.2}$$

$$G_{i_{g-d}}(s) = \frac{i_g(s)}{V_t(s)} = \frac{1}{s^3 C_f L_g L_c + s^2 C_f (L_c R_g + L_g R_c) + s(C_f R_g R_c + L_g + L_C) + R_c + R_g} \tag{3.3}$$

where the notation $'d'$ means the system is damped. The current control loop shown in Fig.2.22 can be extended to Fig.3.1.

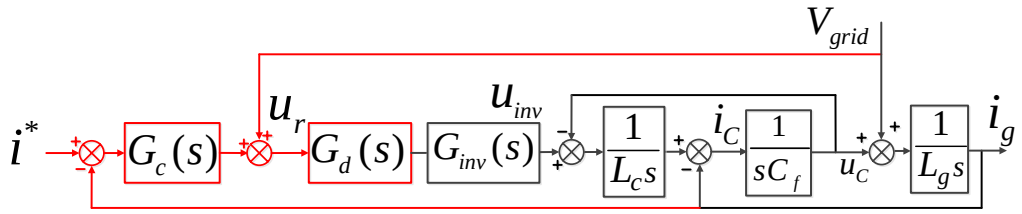


Figure 3.1: Current control loop with LCL filter.

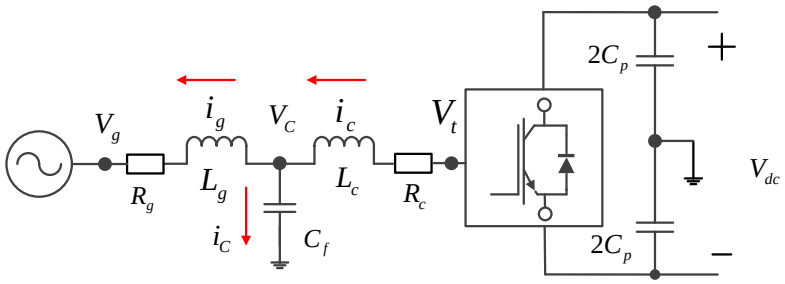


Figure 3.2: Circuit of single-phase grid-connected VSC with LCL.

If the inductors internal resistors and the wires resistances are neglected, which assumes $R_g = R_c = 0$, then eqs. (3.2) and (3.3) evolves into:

$$\begin{aligned} G_{i_c}(s) = \frac{i_c(s)}{V_t(s)} &= \frac{s^2 C_f L_g + 1}{s^3 C_f L_g L_c + s(L_g + L_C)} \\ &= \frac{1}{sL_c} \frac{s^2 + \omega_0^2}{s^2 + \omega_{res}^2} \end{aligned} \tag{3.4}$$

$$G_{i_g}(s) = \frac{i_c(s)}{V_t(s)} = \frac{I_c(s)}{V_t(s)} = \frac{1}{s^3 C_f L_g L_c + s(L_g + L_C)} = \frac{1}{sC_f L_c L_g} \frac{1}{s^2 + \omega_{res}^2} \tag{3.5}$$

where the resonance frequency ω_{res} and the anti-resonance frequency ω_0 are derived as:

$$\omega_{res} = \frac{I_g(s)}{V_t(s)} = \sqrt{\frac{L_c + L_g}{L_c L_g C_f}}$$
$$\omega_0 = \sqrt{\frac{1}{L_g C_f}} \tag{3.6}$$

The bode plot of the two LCL filter transfer functions without internal resistance is shown in Fig.3.3. In this bode plot, $L_g = L_c\, 1.6\ mH, C_f = 20\,\mu F$ are chosen as the same values of the realistic parameters in the VSC available in the laboratory. As it can be seen from the bode diagram, at the resonance frequency ω_{res}, a sharp step down of -180 ° in the phase and a high gain in the magnitude for $G_{i_g}(s)$ occurs. Conversely, for $G_{i_c}(s)$, there is a sharp step up of 180° in the phase. A low gain occurs at the anti-resonance frequency while a high gain occurs at the resonance frequency. From a control perspective, this -180 ° crossing in $G_{i_g}(s)$ frequency response is a negative crossing, and it will create a pair of closed loop poles in the right-half plane [22], leading to system instability. $G_{i_c}(s)$ is stable since it has positive gain margin and phase margin.

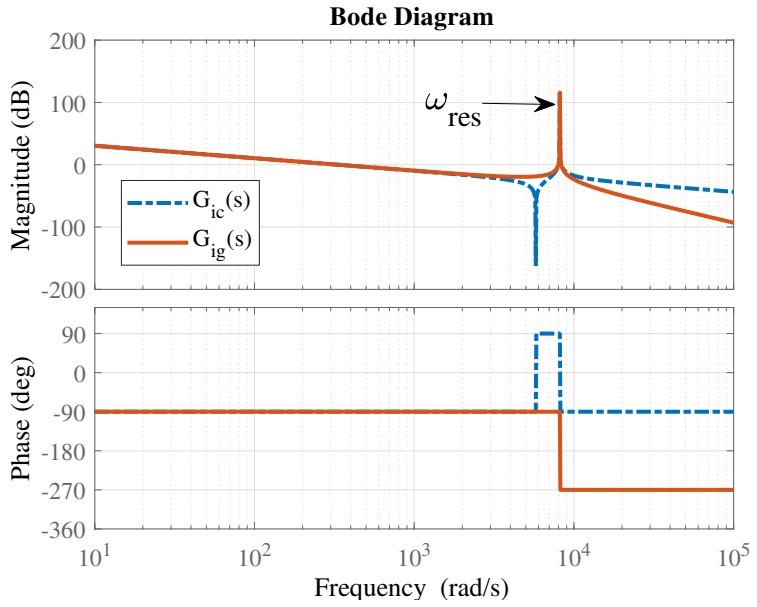


Figure 3.3: Frequency response of the LCL filter.

3.1.2 Choice between GCC and CCC

As previously discussed, the control plant $G_{i_c}(s)$ is more stable compared with $G_{i_g}(s)$ because the converter-side current feedback control provides inherent damping. In fact, in both cases, the current control loop can be designed to be stable. However, the gain margin left for GCC is comparatively smaller than that for CCC. Hence CCC is more robust than the GCC scheme.

Additionally, another important consideration while choosing the controlled current is the effects of sampling and control delays of the digital control implementation. They have a significant influence on the stability of current control loop under both GCC and CCC schemes. From the stability stand-point the choice of the controlled current side of the LCL filter, depends on the relation between the resonance frequency, f_{res}, and the critical frequency f_c. The latter is defined by the sampling frequency, f_s, of the digital control, where f_c is different based on the type of sampling [30–32]. More specifically, according to [30], there are different stable regions for the GCC and CCC schemes. Generally CCC is preferred if f_{res} is smaller than f_c. On the other hand, GCC is recommended if f_{res} lies between f_c and $\frac{1}{2}f_s$ (the Nyquist frequency) [30, 31]. Theoretically, the stable region for GCC and CCC with consideration of delay influence is defined by the critical frequency and the Nyquist frequency. The critical frequency is related to the choice of delay. The total delay consists of the digital controller delay and PWM delay, which are described in Chapter.2. Specifically, the digital controller delay is composed of time delay for the necessary Analog-to-Digital (A/D) conversion T_{d1}, data processing/computation delay T_{d2} and a duty-ratio update delay T_{d3}. Hence the total digital controller delay time T_d is expressed as:

$$T_d = T_{d1} + T_{d2} + T_{d3} = \lambda T_s \tag{3.7}$$

where T_s is the sampling frequency and the value of λ depends on the sampling type of the digital controller. Normally, λT_s is not larger than one sampling period T_s, and its typical values in real operation are $0.5T_s$ and T_s [33], corresponding to the double and single PWM update modes widely used on commercial digital signal processors with internal A/D converters. Note that multi-sampling techniques could be used to reduce the delay effect on the system stability. The critical frequency can be derived from both s-domain and z-domain representations based on Nyquist Stability Criterion [30, 31, 33]. The stable ranges for CCC and GCC under the delay influence are expressed in eqs. (3.8) and (3.9)

- Stable ranges for CCC scheme:

$$\begin{gathered}(\lambda+\frac{1}{2})T_s < \frac{\pi}{2\omega_{res}}, (\lambda \geq k, k=0) \\ \frac{(4k-1)\pi}{2\omega_{res}} < (\lambda+\frac{1}{2})T_s < (\lambda+\frac{1}{2})\frac{\pi}{\omega_{res}}, (2k-1 < \lambda \leq 2k, k=1,2,3\dots) \\ \frac{(4k-1)\pi}{2\omega_{res}} < (\lambda+\frac{1}{2})T_s < \frac{(4k+1)\pi}{2\omega_{res}}, (\lambda > 2k, k=1,2,3\dots)\end{gathered} \tag{3.8}$$

- Stable ranges for GCC scheme:

$$\begin{aligned}\frac{(4k+1)\pi}{2\omega_{res}} < (\lambda+\frac{1}{2})T_s < (\lambda+\frac{1}{2})\frac{\pi}{\omega_{res}}, (2k<\lambda\leq 2k+1, k=0,1,2\dots)\\ \frac{(4k+1)\pi}{2\omega_{res}} < (\lambda+\frac{1}{2})T_s < \frac{(4k+3)\pi}{2\omega_{res}}, (\lambda>2k+1, k=0,1,2\dots)\end{aligned} \tag{3.9}$$

However for controllability, ω_{res} should be smaller than half of the sampling frequency namely the Nyquist frequency $\frac{\omega_{res}}{2}$ [34, 35]. Therefore, the stable region can be narrowed further:

- $\lambda T_s = T_s(Single-sampling)$

$$\begin{aligned} f_{res} <= f_c = \frac{f_s}{6}, (CCC)\\ \frac{f_s}{6} = f_c < f_{res} < \frac{f_s}{2}, (GCC)\end{aligned} \tag{3.10}$$

- $\lambda T_s = 0.5T_s(Double-sampling)$

$$\begin{aligned} f_{res} < f_c = \frac{f_s}{4}, (CCC)\\ \frac{f_s}{4} = f_c < f_{res} < \frac{f_s}{2}, (GCC)\end{aligned} \tag{3.11}$$

Hence, the critical frequency is derived as $\frac{f_s}{6}$ and $\frac{f_s}{4}$ for single- and double-sampling, respectively. Normally, the pre-design of the LCL filter with regard to its control scheme is always firstly taken so that the resonance frequency falls within the stable region. However, the designer needs to investigate the sensitivity of the system because of the typical shift of resonance frequency during operation caused by the variation of LCL filter parameters, e.g. drop of core permeability with the current flowing through in the inductors, and the changing equivalent grid impedance. For correcting a possible deviation in the filter parameter, the sampling frequency could be changed dynamically to make the GCC or CCC schemes fall in the stable region. However, in order to avoid innacuracies in the A/D conversions, the switching frequency of the VSC must follow the same tendency.

Fig.3.4 and 3.5 shows the influence of sampling frequency on the stability of GCC and CCC with digital controller adopting single-sampling. As it can be seen from the bode diagrams, with smallest sampling frequency f_s=4kHz, $f_{res}>f_c$, hence CCC is unstable while GCC is stable. On the other hand, with the larger sampling frequency f_s equals 8kHz and 16kHz, $f_{res} < f_c$, hence GCC is unstable while CCC is stable.

For this research, single-sampling is adopted and the LCL resonance frequency of the VSC in the laboratory is around 1.3kHz, which is smaller than the critical frequency $\frac{f_s}{6}$=2.7kHz when a sampling frequency of 16kHz is implemented in the digital controller. Therefore, GCC lies in the unstable region while CCC is found in the stable region. Therefore, from the perspective of control, CCC is recommended to achieve stable operation of the current control.

However, for the merits of rejecting the grid distortion the grid-side current measurements for the feedback control are preferable over the converter-side currents. Fig.3.6 illustrates the flow of harmonics components of the grid-side currents. If the capacitor of the LCL filter is considerably large, it exhibits the desired low impedance to the VSC generated switching frequency harmonics. However, it may also display undesirable low impedance to the the low-order harmonics e.g. 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonics. This

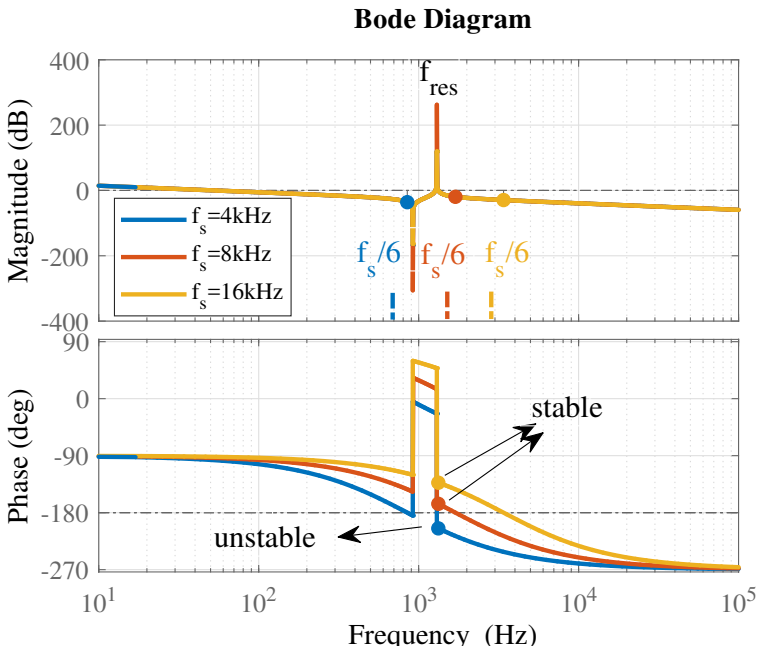


Figure 3.4: Influence of the sampling frequency on CCC.

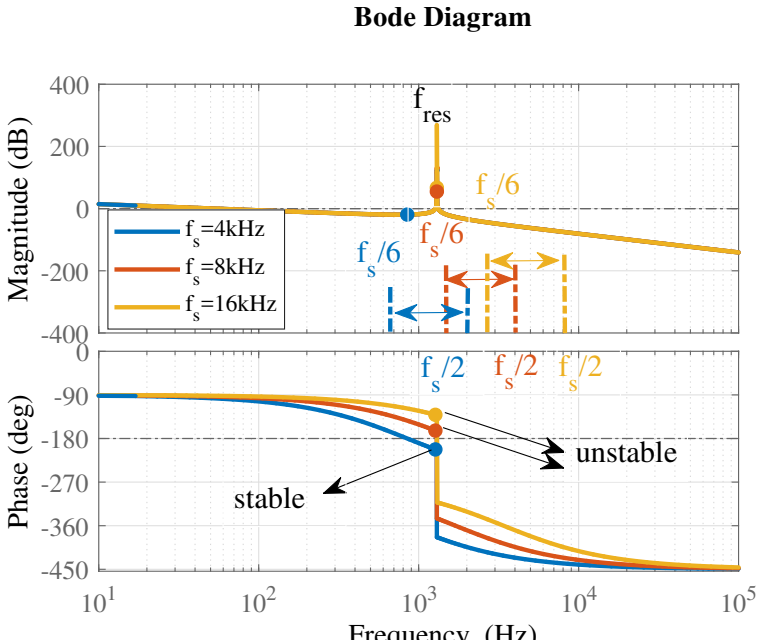


Figure 3.5: Influence of the sampling frequency on GCC.

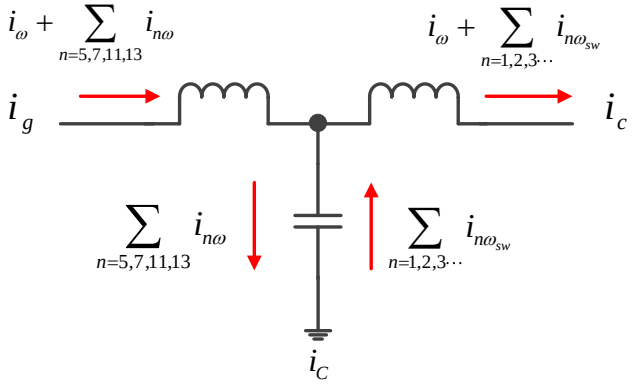


Figure 3.6: Current flow of harmonics components.

high-pass characteristics of the filter capacitor results in some magnitude of low-order harmonics drawn from the grid-side current due to grid voltage distortions. This means the detection of those harmonic components in the converter-side current measurement is hence less effective than that of the grid-side current.

3.1.3 Resonance Damping of LCL filter

As previously reported, for the laboratory available 2-level VSCs the GCC control becomes unstable because the LCL resonance frequency falls into the undesirable region. However, in order to utilize the advantage of GCC for the grid voltage harmonics mitigation while maintaining stable current control of the GCC, some damping method should be taken to compensate the resonance in the LCL filter. Generally speaking, circuit damping techniques can be classified into to categories: Passive Damping (PD) and Active Damping (AD) methods.

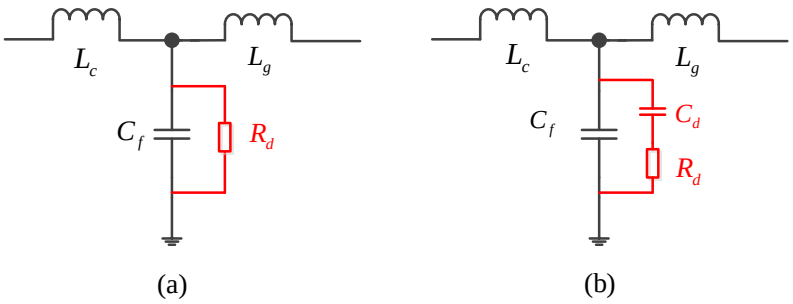


Figure 3.7: Exemplary of passive damping placed across C_f: (a) R_d (b)R_d and C_d.

Passive Damping

Passive damping methods are widely accepted due to its simplicity and effectiveness. Theses methods generally add resistors to the filter inductors or capacitor to suppress the gain at the resonance frequency in the LCL filter plant. The idea is to add zeroes or to move the plant poles to left-half-plane (or LHP) to compensate the resonance peak. It has been verified in [36], that introducing a resistor in parallel with a filter capacitor (Fig.3.7(a)) shows the best damping performance since this circuit has the highest loop gain in the high frequency range. The transfer function of the LCL plant with a parallel-connected RC damper (Fig.3.8) is expressed as follow:

$$\begin{aligned} G_{i_g-D} &= \frac{1}{s^3 L_c L_g C_f + s^2 L_c L_g / R_d + s(L_c + L_g)} \\ &= \frac{1}{sC_f L_c L_G} \frac{1}{s^2 + 2\zeta\omega_{res} s + \omega_{res}^2} \end{aligned} \tag{3.12}$$

where $\zeta = \frac{1}{2R_d}\sqrt{\frac{L_c L_g}{(L_c+L_g)C_f}}$. The bode diagram of the transfer function of the LCL plant with R_d= 10 Ω is shown in Fig.3.8. The resonance peak is effectively attenuated and the

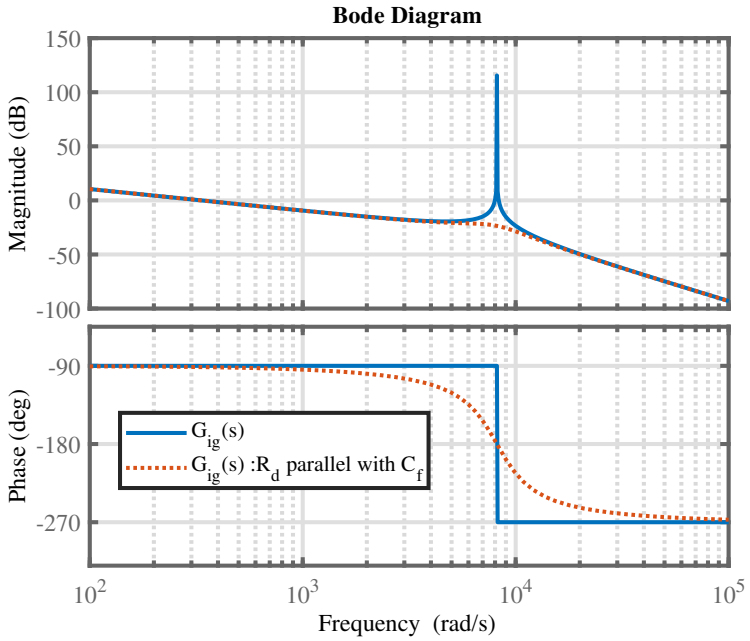


Figure 3.8: Bode diagram of the studied *LCL* filter with passive damping.

phase response is not substantially changed by the additional resistor. Series connected R-C damping circuit placed in parallel with the filter capacitor C_f, as shown in Fig.3.7(b), can maintain the advantages of the previous solution and provide additional phase margin. For this reason, the series R-C damper circuit parallel with filter capacitor is widely adopted in LCL filters.

Since the filter inductors are typically designed to have a low impedance at low frequency, the voltage drop across them in this frequency range is negligible, which means the capacitor voltage is close to the grid voltage. Hence, the damping resistor under grid voltage can result in significant power loss. Additionally, the added resistors will not only deteriorate the overall efficiency of the system but also reduce filter effectiveness [32]. For example, the low-frequency gains or the high-frequency harmonic attenuating ability of the LCL filter will be sacrificed with passive damping methods, which makes PDs an unsatisfactory choice for the application at hand.

Active Damping

Recently, active damping methods have been widely investigated because they can effectively solve the resonance influence in the system operation at the cost of reduced control bandwidth [37]. State-Variable-Feedback and notch filter-based active damping are the two most commonly used methods.

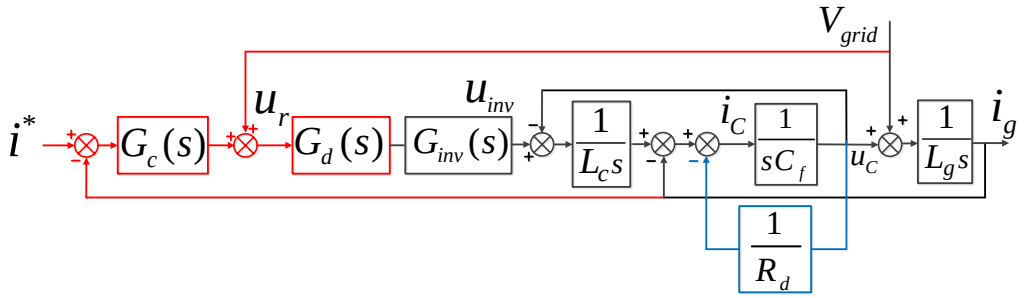
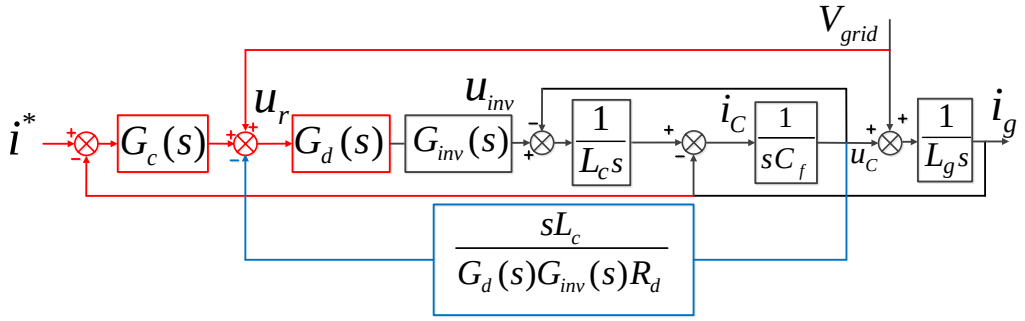


Figure 3.9: Current control loop with parallel damping resistor R_d.

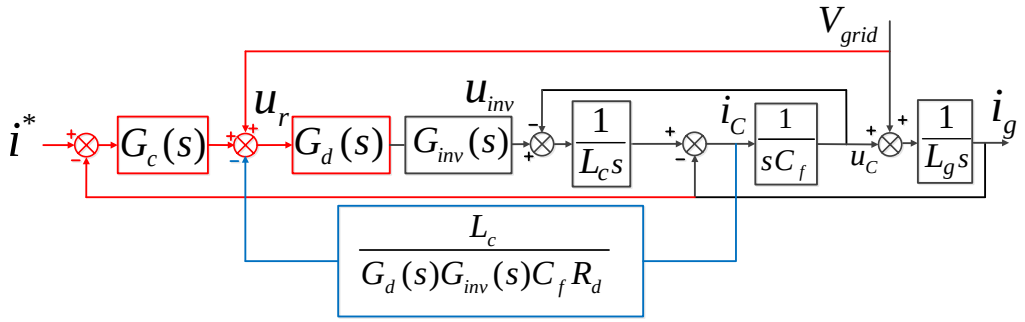
State-Variable-Feedback active damping, which is also called Virtual resistor method, brings the filter capacitor voltage (or current) back to the control loop. The feedback information of the capacitor voltages or capacitor currents are manipulated and then added to the generated voltage reference through a feed-forward control loop. The added signal can be manipulated to mimic the effect of an equivalent damping resistor seen by the filter capacitor. As discussed, the implementation of this strategy comes at the cost of adding more measurements into the circuit.

Fig.3.9 shows the current control loop of the grid-connected VSC with a physical parallel damping resistor R_d in the LCL filter (in parallel to C_f). The idea behind the virtual resistor method is to move the feedback node of the capacitor voltage to other positions instead of the input of the capacitor transfer function. The feedback of the capacitor voltage and the capacitor current to the node where the reference voltage is generated is depicted in Fig.3.10. As it can be seen from the control loop with the virtual resistor R_d, the feedback of the capacitor voltage and current mimics the equivalent damping resistor. If the delays and zero-order hold effect of the PWM are neglected, then the capacitor voltage feedback requires a derivative-based feedback gain and capacitor current only uses a proportional gain. In fact, the equivalent transformation of the control structure can be realized with the grid-side current feedback through a second-order derivative transfer function.

Practically, the derivative element can lead to the amplification of high-frequency noise especially when the grid-side current contains 11^{th} and 13^{th} components. Moreover, an ideal derivator is difficult to implement in the digital controller. The discretization error introduced by a digital derivator will degrade the performance of the active damping method [36]. Conversely, from the control point of view, capacitor current feedback-based virtual resistor is preferred and thus has been widely adopted for its simplicity of implementation and effectiveness.



(a) Virtual Resistor: Derivative feedback of the capacitor voltage



(b) Virtual Resistor: Proportional feedback of the capacitor current

Figure 3.10: Virtual resistor R_d with the capacitor voltage and current feedback.

However, the virtual resistor method requires one more measurement of either capacitor voltage or current. In order to realize single feedback loop control, Notch filter is chosen as the active damping method in this thesis since this can realize effective damping while maintaining a single current measurement for the feedback control loop [38]. Similar to the notch filter introduced in the PLL control, where the double fundamental frequency is trapped, the notch filter implemented here is tuned to trap the open loop gain at the resonance frequency to avoid a 0 dB crossing in magnitude for the frequency response. The notch filter is added in the current control loop as illustrated in Fig.3.11. The notch filter works in such a way that it can realize equivalent damping performance as the

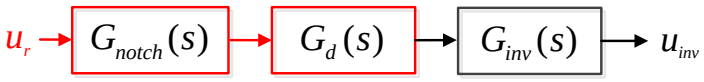


Figure 3.11: Notch filter added in the control loop.

parallel-connected R_d. Thereby, notch filter transfer function for active damping of LCL resonance peak can be derived from dividing eq. (3.12) by eq. (3.5):

$$G_{notch}(s) = \frac{G_{i_g-D}(s)}{G_{i_g}(s)} = \frac{s^2 + \omega_{res}^2}{s^2 + 2\zeta\omega_{res}s + \omega_{res}^2} \tag{3.13}$$

This expression of notch filter implies that the active damping based on this technique has the same open loop gain as the aforementioned passive damper. The bode diagram of the LCL filter with notch filter is shown in Fig.3.12. The frequency response is exactly the same compared with that of Fig.3.8. Compared with virtual resistor active damping, notch filter avoids one more measurement feedback but achieves the equal damping performance at the cost of higher control computation. Practically, the inductance in the LCL filter may

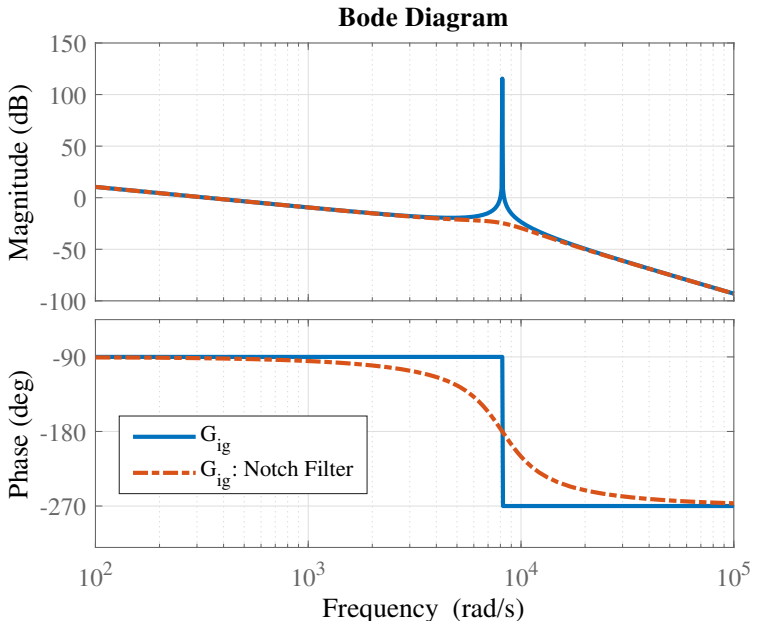


Figure 3.12: Bode diagram of LCL plant with notch filter.

vary during operation due to the magnetic saturation effect of the magnetic core. Thus the resonance frequency changes according to the variation of inductance. In order to precisely trap the resonance peak of the LCL filter, the notch filter should be designed to be robust enough against the variation of resonance frequency. Based on [38–41], an

improved notch filter design against LCL parameter variation has been researched and implemented. The width and depth of the notch filter attenuation can be set according to design requirements. The idea is to design the notch filter based on the desired wideness and depth of the gain attenuation. The generic transfer function of the notch filter to be implemented is expressed as:

$$G_{notch}(s) = \frac{s^2 + 2\zeta_z \omega_{res} s + \omega_{res}^2}{s^2 + 2\zeta_p \omega_{res} s + \omega_{res}^2} \tag{3.14}$$

where ζ_z and ζ_p are the damping ratio for the complex conjugate zeros and poles [41]. Generally, the depth and width of the notch filter in the bode plot is related to ζ_z and ζ_p.

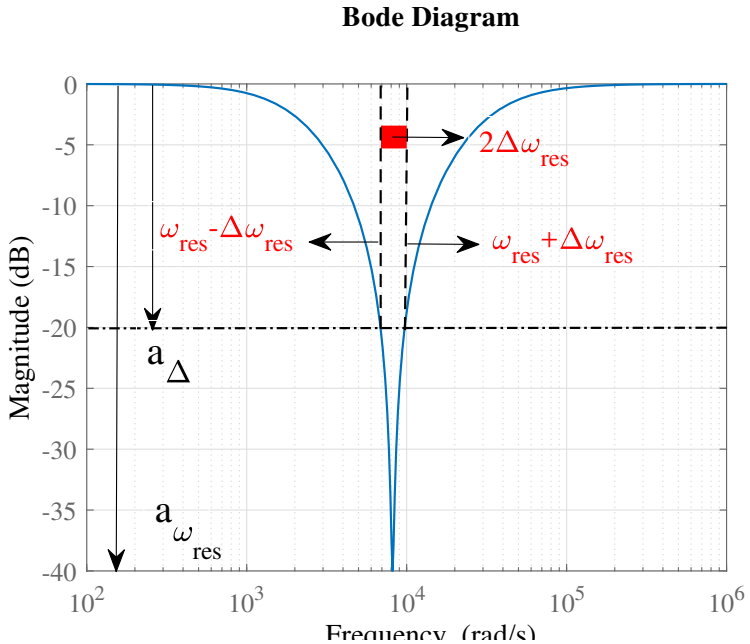


Figure 3.13: Design parameters of notch filter.

To be more specifically, the depth and width of the notch filter is determined by the attenuation $a_{\omega_{res}}$ at the resonance frequency ω_{res} and the attenuation a_Δ at the border of a specified frequency band $\omega_{res} \pm \Delta_\omega$ [41]. The relations between the damping coefficients and the attenuation are derived as:

$$\begin{aligned} \zeta_p &= \left| \frac{2\omega_{res}\Delta\omega_{res} + \Delta\omega_{res}^2}{2\omega_{res}\Delta\omega_{res} + \omega_{res}^2} \right| \sqrt{\frac{1 - a_\Delta^2}{a_\Delta^2 - a_{\omega_{res}}^2}} \\ \zeta_z &= a_{\omega_{res}}^2 \zeta_p < a_\Delta \end{aligned} \tag{3.15}$$

The attenuation ability of the notch filter is tunable at those frequency to adjust the depth and width, as shown in Fig.3.14 and 3.15.

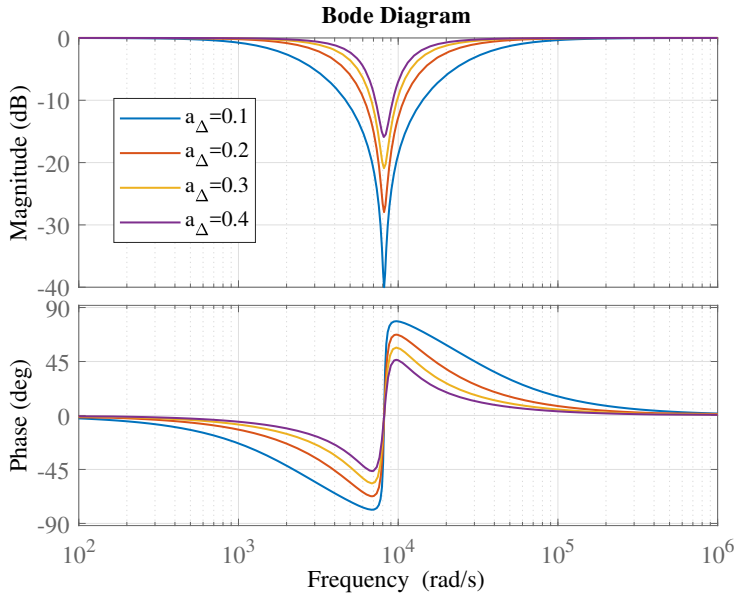


Figure 3.14: Influence of a_Δ.

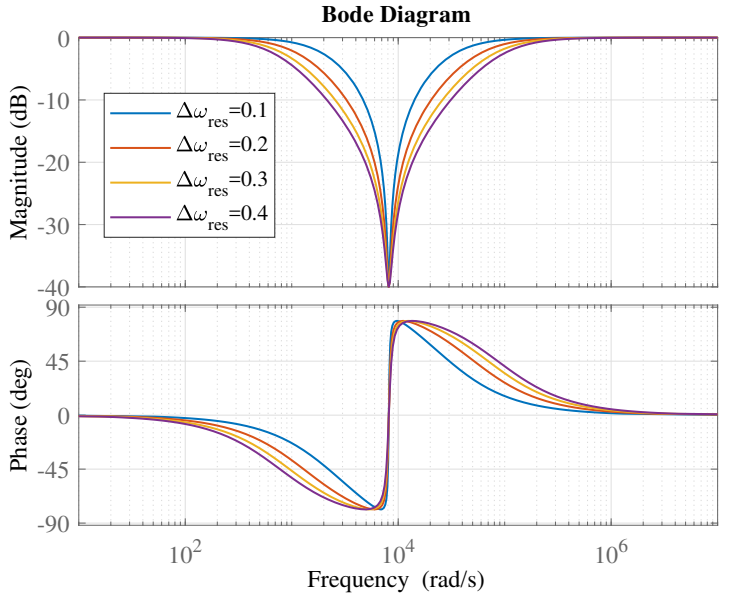


Figure 3.15: Influence of $\Delta_{\omega_{res}}$.

The attenuation at the notch frequency is chosen based on the trade-off between the damping performance in nominal and other cases. If the frequency band is chosen too small or the attenuation a_Δ is not enough, then the notch filter will not have a satisfactory

damping when the resonance frequency varies. Generally, $a_\Delta = 1a_{peak}$ and $\Delta\omega_{res} = 0.1\omega_{res}$ are chosen to satisfy the robustness requirement, where a_{peak} is the attenuation of the LCL resonance peak. A good selection for attenuation is $a_{\omega_{res}} = a_\Delta^2$, which is $a_{\omega_{res},dB} = 2a_{\Delta,dB}$ in the decibel scale. The design parameters are shown in the bode diagram in Fig.3.13. The width of the notch filter depends on the $\Delta\omega_{res}$ and depth depends on a_Δ, as shown in Fig.3.14 and 3.15. Small a_Δ and large $\Delta_{\omega_{res}}$ can result in a over-damped situation, where the phase of the control loop will be greatly influenced.

3.1.4 Controller parameters design

The controller for the power and the DC link voltage controls is designed based on the GCC scheme and the notch filter-based active damping. The circuit parameters are listed in Table.3.1.

Parameter	Value
L_c	1.6 mH
L_g	1.6 mH
C_f	20μF
C_p	600 mF
R_c	2Ω
R_g	2Ω

Table 3.1: VSC circuit parameters.

The compensator of the current controller adopts the PI control:

$$G_c(s) = k_p + \frac{k_i}{s} = k_p(1 + \frac{1}{T_i s}) \tag{3.16}$$

where T_i is the integral time constant which is also called reset time of a PI controller. Due to the existence of inductor winding resistors, the LCL filter plant transfer function has multiple poles close to the origin since $\frac{R}{L}$ is quite small, as eq. (3.5) indicates. The pole close to origin causes the rolling of the magnitude of loop gain and the phase drop of loop phase at low frequency ranges [21]. According to [42], the PI controller should be designed in such a way that the pole provided by the PI compensator cancels out the smallest pole, which means the pole in the LCL plant transfer function with the slowest time constant. This method is called Pole-zero cancellation. Meanwhile, k_p can be adjusted to ensure stability, increase bandwidth and phase margin.

The grid-side and converter-side, inductor resistance and other circuit losses such as the semiconductor losses provide an equivalent damp resistance of 2Ω. Thus the integral time constant T_i is set as 0.8ms. Root locus method is used here to identify the optimized range for k_p. The root loci plot is illustrated in Fig.3.16.

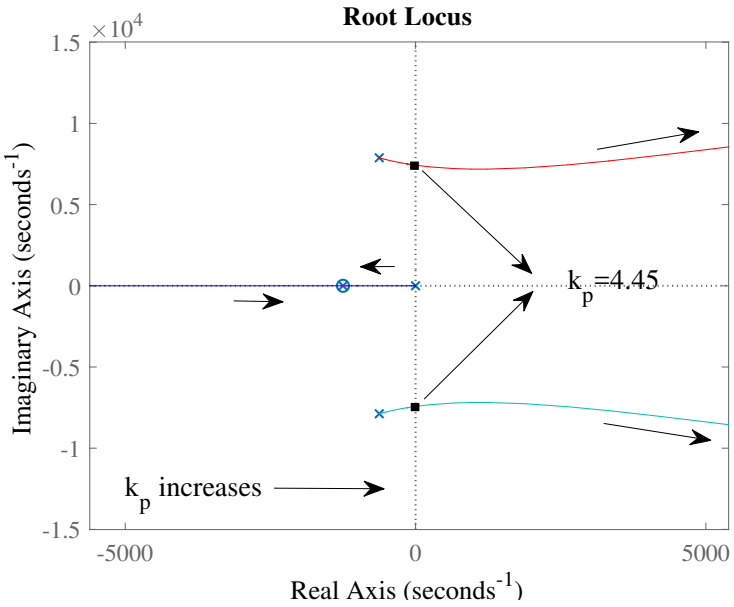


Figure 3.16: Root loci: current control loop.

As it can be seen from the root locus, the stable range for k_p is $0 < k_p < 4.45$. The step response of the closed loop system of the current control loop is shown below:

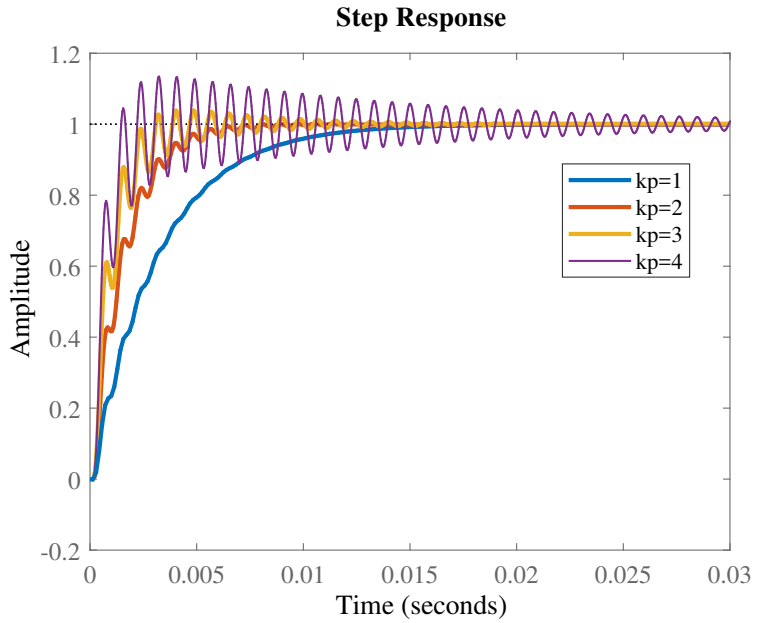


Figure 3.17: Step response: current control loop.

With larger gain, the overshoot becomes larger but response is faster. k_P can be chosen as 3 for the current control with basic PI controller. As discussed in Chapter.2, the compensator for the DC-link voltage control is also a PI controller:

$$G_v(s) = k_{p_{dc}}(1 + \frac{1}{T_{i_{dc}}s}) \tag{3.17}$$

The voltage control loop has the current control loop nested inside. Theoretically, the outer loop (voltage control) should respond slower than the inner loop (current loop). Equivalently, the bandwidth of the voltage loop should be smaller than current loop and then the two control loops are fully decoupled. Ideally, the bandwidth of voltage loop is 10 times smaller than that of the current loop.

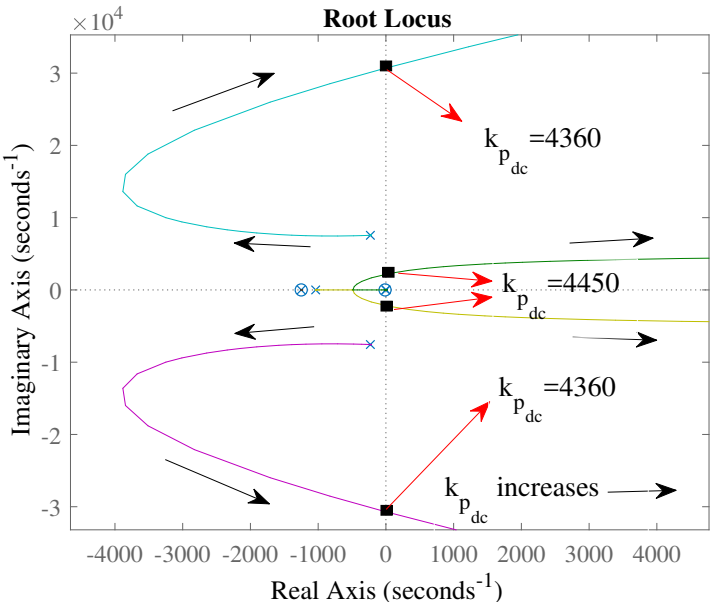


Figure 3.18: Root loci: voltage control loop.

Firstly, $k_p = 3$ is chosen for current loop PI controller and the integral time constant $T_{i_{dc}}$ is set as 100 times that of the current controller T_i. External power source in steady state P_{ext0} is set as rated power value 5 kVA and C_p is 600 μF. The root loci plot of the DC voltage control loop is illustrated in Fig.3.18. As it can be seen the maximum $k_{p_{dc}}$ for stability is 4550. Aside from the range for stability, $k_{p_{dc}}$ should be optimized based on the transient response e.g. overshoot and rise time. Fig.3.19 shows the step response of the closed loop system of the voltage loop. After $k_{p_{dc}}$ exceeds 500, the overshoot is too large for the start-up process of the VSC since the large overshoot will cause DC bus protection to trip. $K_{p_{dc}} = 300$ is selected based on consideration of both overshoot and response time. The bode plot of the current and voltage loops with selected parameters are shown in Fig.3.20 and 3.21.

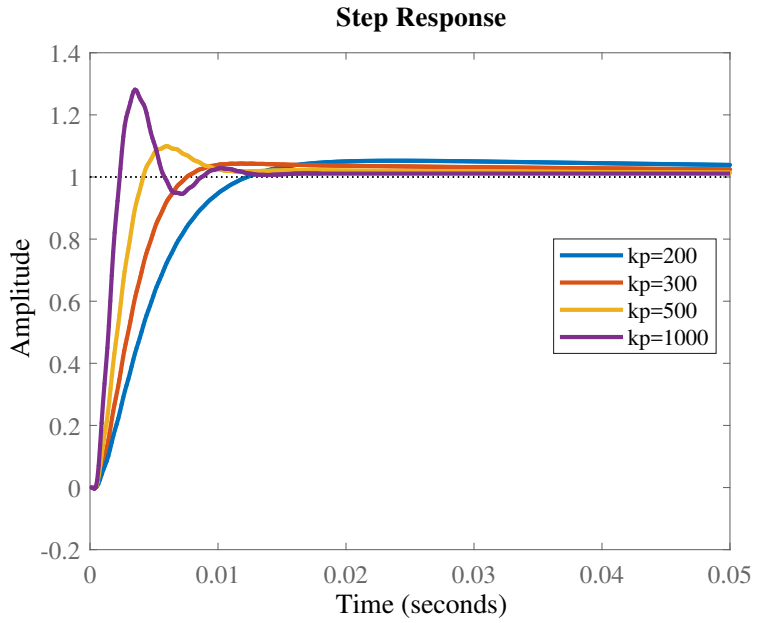


Figure 3.19: Step response: voltage control loop.

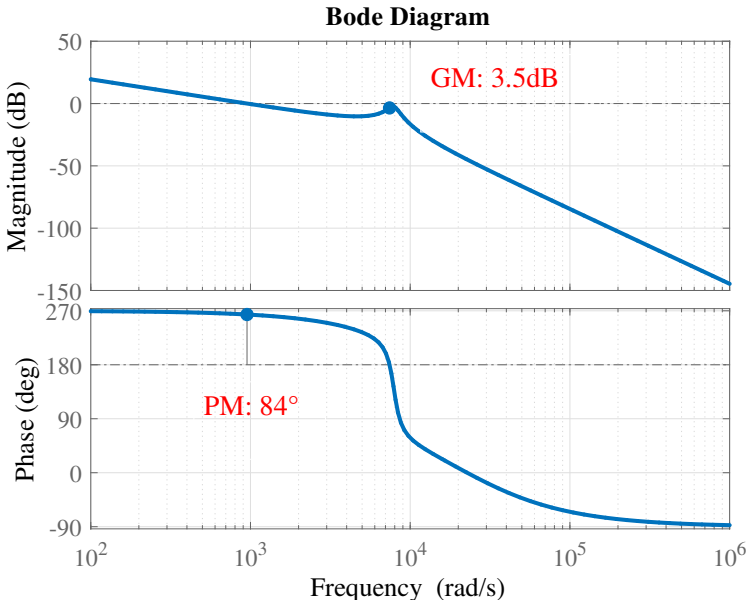


Figure 3.20: Bode plot of designed current loop.

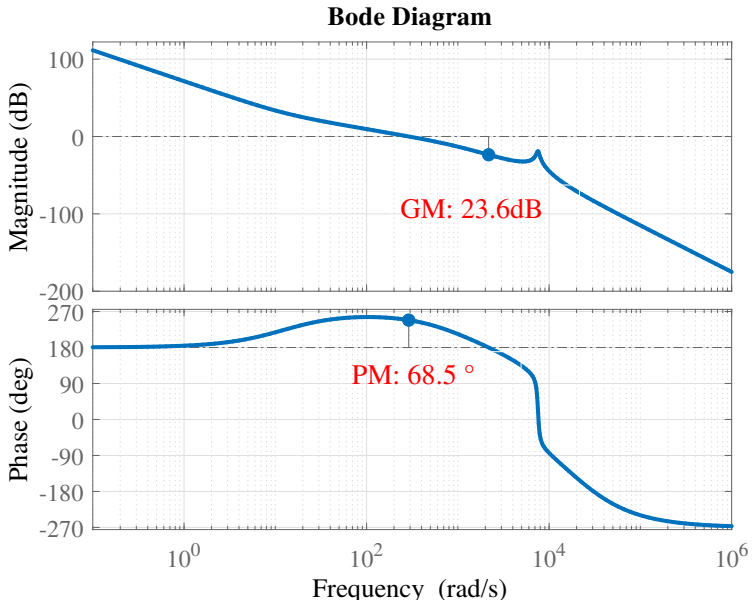


Figure 3.21: Bode plot of designed voltage loop.

Both the current and voltage loops have enough phase margin but the current loop has a small gain margin. The gain margin of the current loop is limited by the resonance of the LCL filter and it requires to be improved by the notch filter. After the notch filter is implemented, the range for k_P of the current loop is increased significantly, which is validated by the root loci plot in Fig3.22. Maximum value for k_p which guarantees stability is increased to 22. The step response is shown in Fig.3.23.

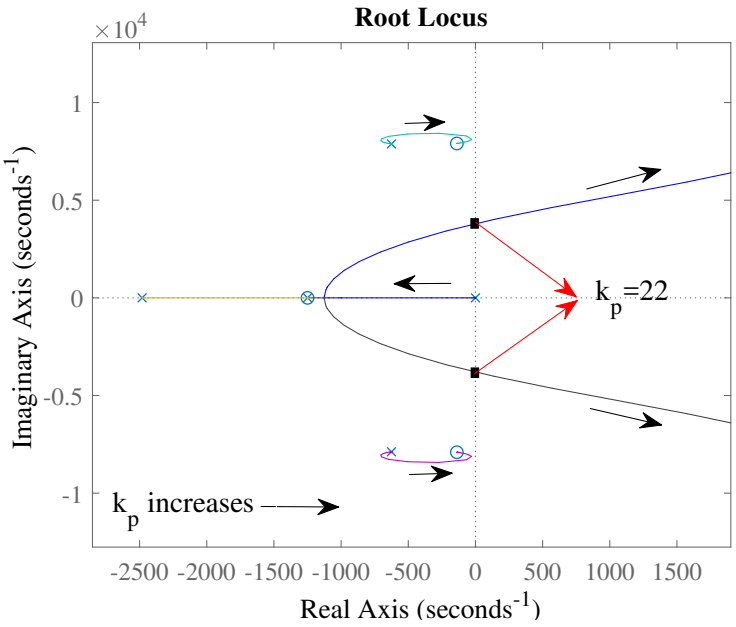


Figure 3.22: Root loci: current control loop with notch filter.

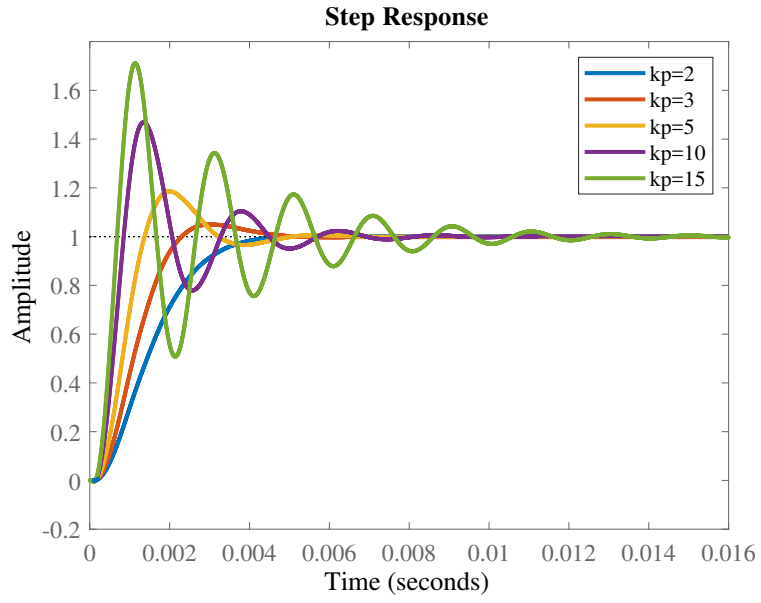


Figure 3.23: Step response: current control loop with notch filter.

$k_p = 3$ is still the optimal choice since it has a small overshoot and a relatively fast response. For the voltage control loop the root loci plot and the step responses are shown below:

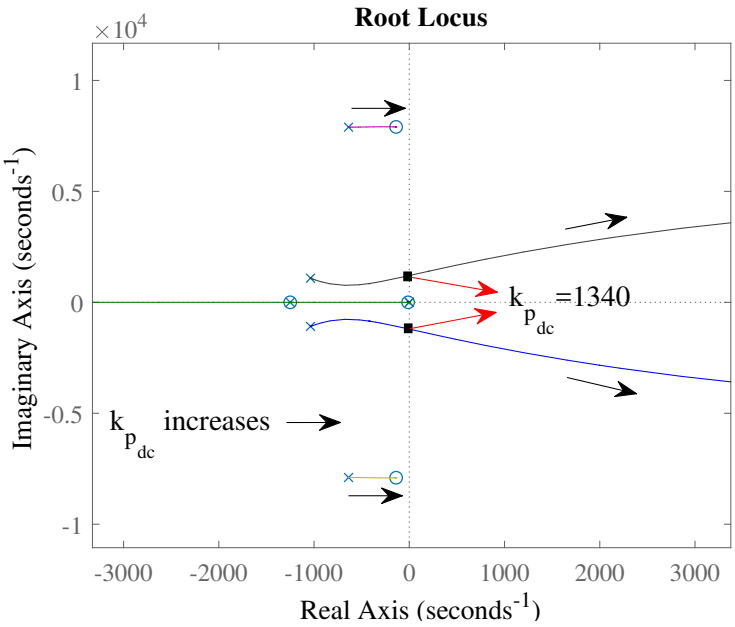


Figure 3.24: Root loci: voltage control loop with notch filter.

The range for $k_{p_{dc}}$ is reduced significantly to 1340 but the poles at low $k_{p_{dc}}$ values are more distant from origin, which means they have faster response. As it can be seen from 3.25, the step responses are not influenced by the notch filter. In fact, the notch filter greatly increases the gain margin of the current loop but reduces that of the voltage loop, as shown in Fig.3.26 and 3.27. Such a reduction of the gain margin in the voltage loop is acceptable since it is large enough.

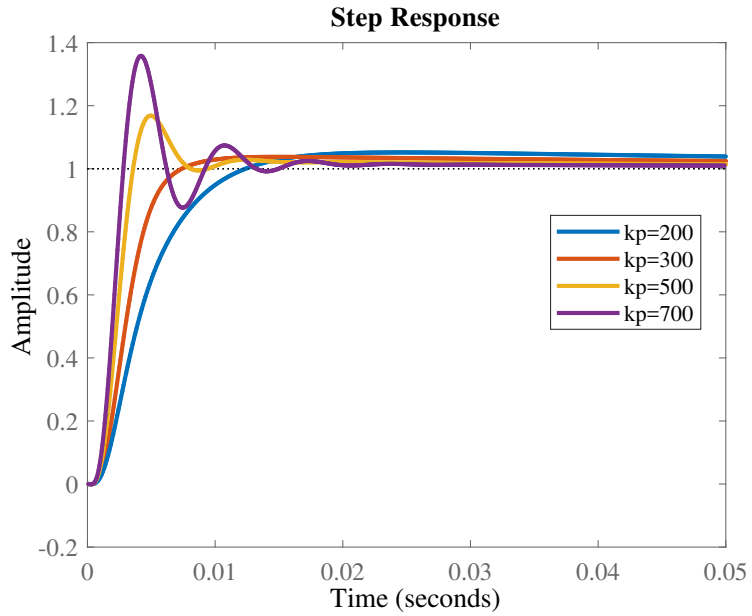


Figure 3.25: Step response: voltage control loop with notch filter.

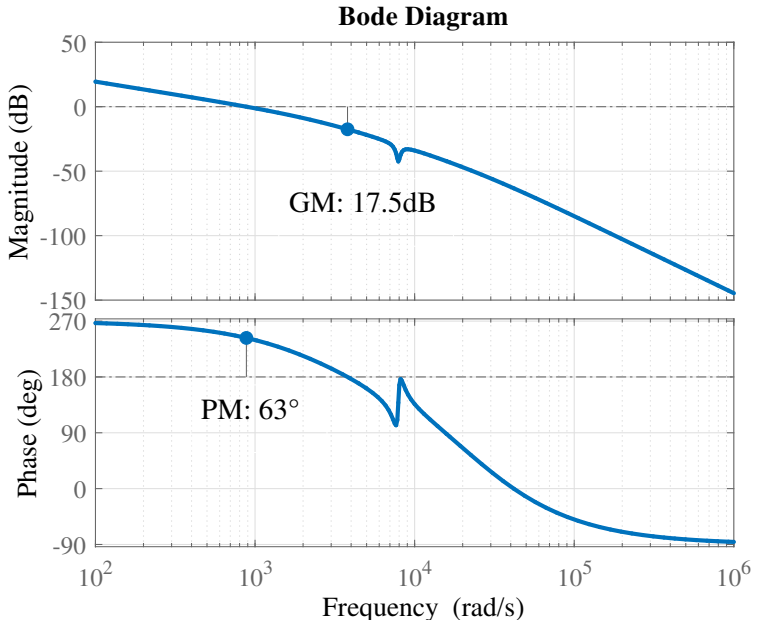


Figure 3.26: Bode plot of the designed current loop with notch filter.

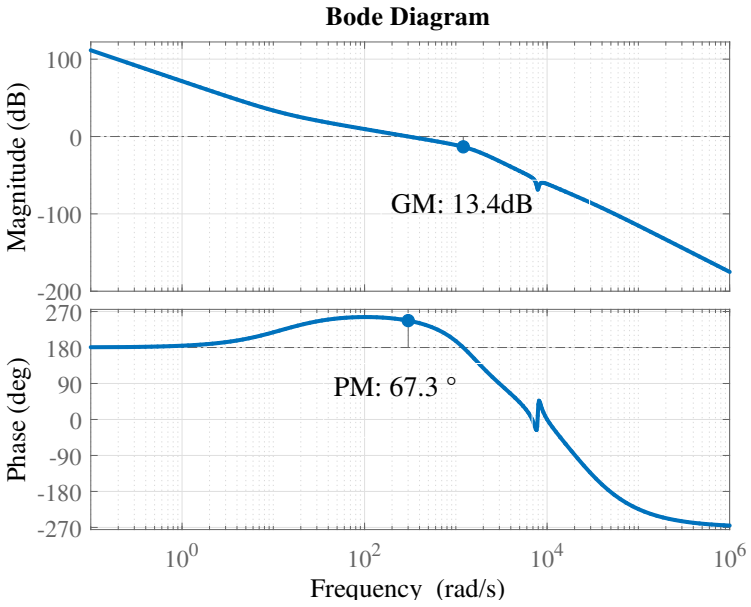


Figure 3.27: Bode plot of the designed voltage loop with notch filter.

Additionally, the bandwidth of the current and voltage loops are slightly increased after implementing the notch filter, as shown in Fig.3.28 and 3.29.

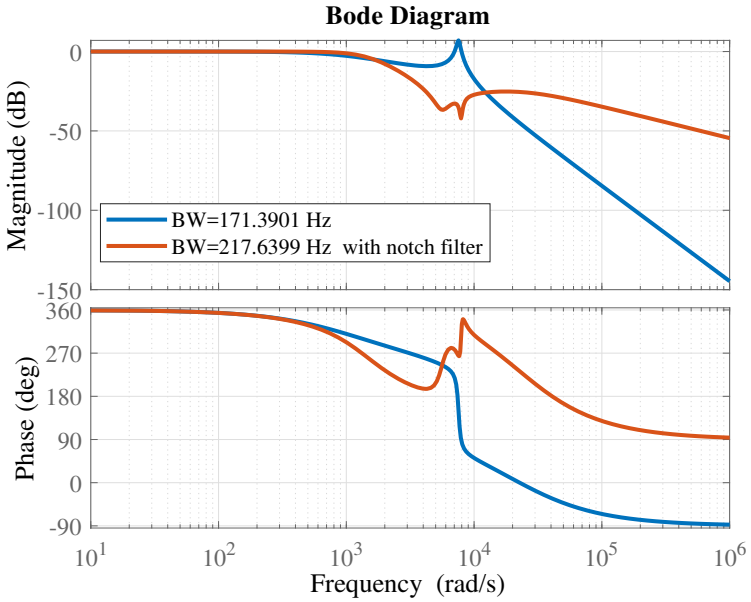


Figure 3.28: Bode plot: the closed loop system of current loop.

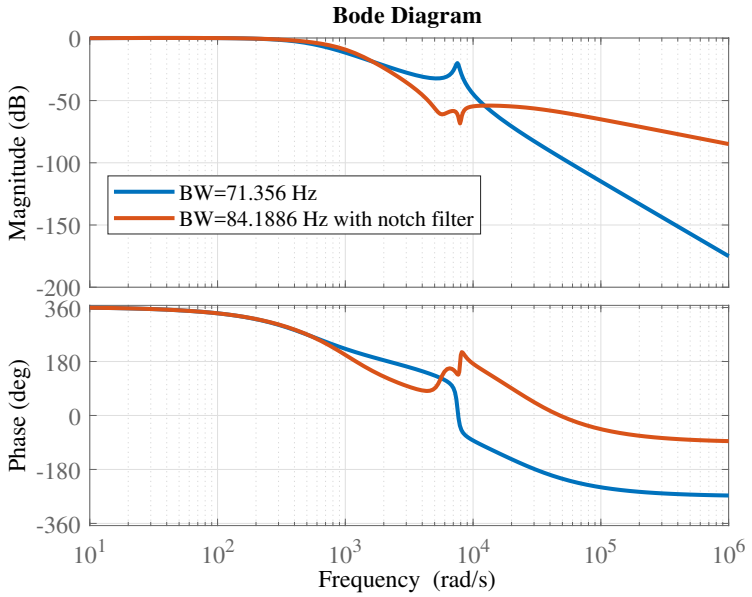


Figure 3.29: Bode plot: the closed loop system of voltage loop.

The simulations are done in MATLAB/SIMULINK to verify the stability improvement of the notch filter, as shown in Fig.3.30.

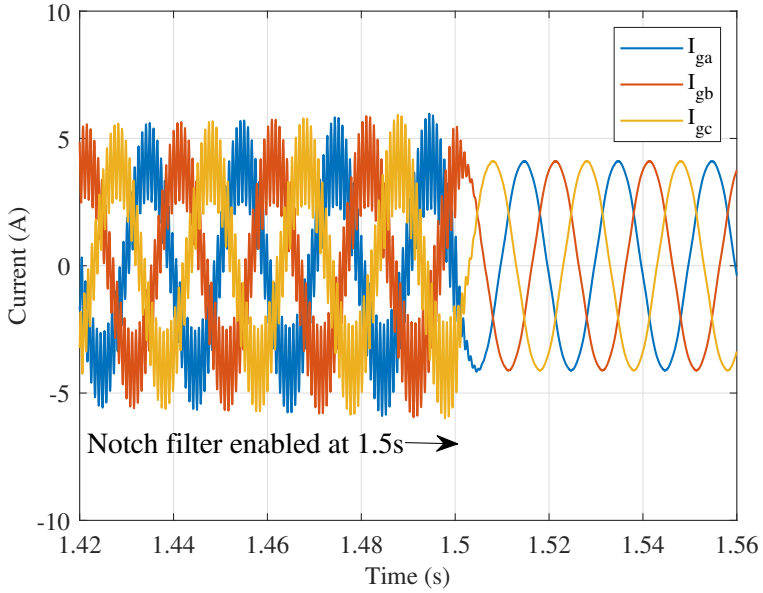


Figure 3.30: Influence of notch filter on stability.

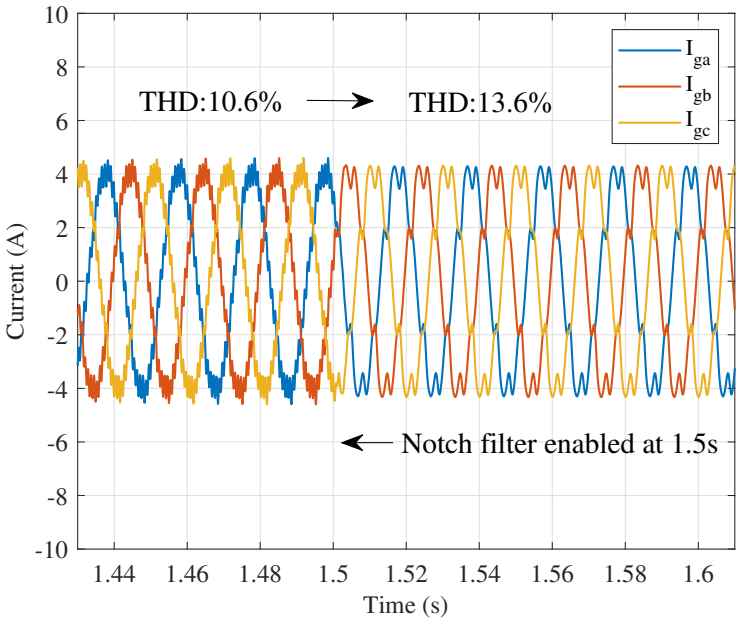


Figure 3.31: Influence of notch filter on harmonics.

The simulation is based on the voltage control of the LCL-filtered 2-level VSC without external power source (STACOM mode). The VSC is connected to a grid emulator delivering an ideal voltage source (V_{rms}= 220 V at 50 Hz) and the DC link voltage is regulated to 750 V. The converter delivers 2 kVAR reactive power to the grid. The current controller gain k_p is chosen such that the control is marginally stable. At t=1.5s, the notch filter is enabled and the control becomes stable.

The simulations indicate that the implementation of notch filter can improve the stability of grid-side current control. With the notch filter, a higher loop gain is achieved when the desired stability margin is fixed, or stability margin is improved with the same controller gain. However, the loop gain at higher harmonics frequency e.g. 13^{th} is reduced by the notch filter since the harmonics frequency is close to the LCL filter resonance frequency. This will result in worse current waveform in grid distortion condition, when the distortion components have the frequency close to the resonance frequency of the LCL filter. Fig.3.31 shows the simulation of the DC link voltage control of the two-level VSC with LCL filter under distorted AC source (5^{th}, 7^{th}, 11^{th} and 13^{th}). The THD of the grid-side current increases from 10.6% to 13.6% after the notch filter is enabled at 1.5s despite of the transition of the system from marginally stable condition to stable operation. This fact proves that the notch filter worsens the attenuation of harmonics in the grid-side current. Therefore, specific harmonics controller is required if the AC source has distorted waveforms.

3.2 HARMONICS MITIGATION IN GRID-SIDE CURRENT UNDER DISTORTED GRID VOLTAGE

Low-order harmonics components (5^{th}, 7^{th}, 11^{th} and 13^{th}) are detected in the phase-to-neutral grid voltage, as shown in Fig.3.32. The harmonic components values are listed in Table.3.2. The simulation results in Section.3.1 show that notch filter can improve

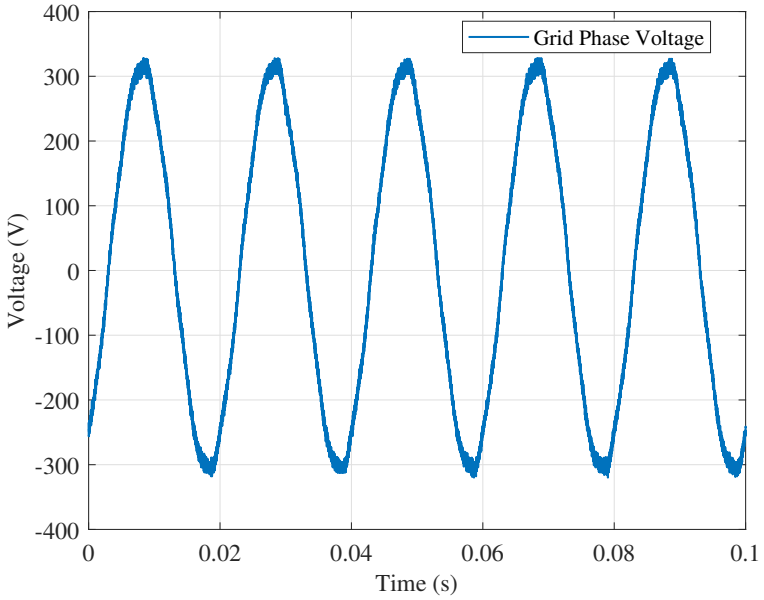


Figure 3.32: Phase-to-neutral grid voltage.

Harmonics	% of Fundamental
Total	2.94%
5_{th}	0.46%
7_{th}	1.88%
11_{th}	0.46%
13_{th}	0.33%

Table 3.2: Harmonic components in the grid voltage.

the stability of the grid-side current control but worsens the high frequency loop gain, which is undesired for the current harmonics attenuation. Since the 11^{th}, 13^{th} harmonics components exist in the grid voltage, these harmonics reflected in the grid-side current can not be rejected by the PI+Notch-Filter based current controller. In this case a well-tuned harmonics controller is recommended to effectively reject the grid-side current harmonics.

From the current control loop shown in Fig.3.1, the grid voltage is coupled in the LCL plant and contributes to the grid current. The harmonics ripple in the grid-side current deteriorates the power quality and can also influence the operational range of other equipments, e.g. circuit breakers [43]. The grid voltage is regarded as a disturbance term from

the perspective of control and its feed-forward method can be adopted in the current control to mitigate the influence of the grid distortion. The transfer function of the grid voltage feed-forward is expressed as $G_f(s)$. As illustrated in Fig.3.1, the current control loop in the GCC scheme adopts the unity feed-forward of the grid voltage. However, grid voltage feed-forward can not eliminate the harmonics components in the grid-side current with a satisfactory result. Thereby, a resonator-based PIR (PI+Resonator) compensator can be used to increase the harmonics rejection capability at specific frequencies.

3.2.1 Grid Impedance Analysis

In order to analyze the rejection capability of the current harmonics, the grid impedance for those harmonic frequencies should be investigated since these come from the grid voltage distortions [43, 44]. To analyze the equivalent impedance transfer function from the grid voltage to the grid-side current output, the current control loop can be simplified to the model shown in Fig.3.33, where the control output depends on the input i_{ref} and disturbance V_g. As given in Fig.3.33, grid-side current is controlled by the reference and

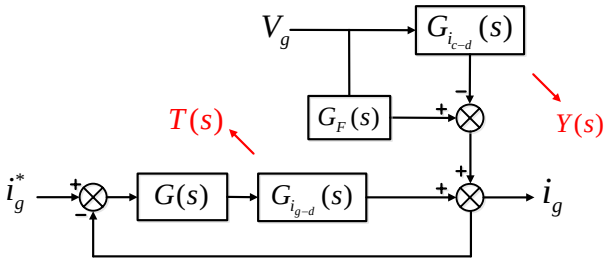


Figure 3.33: Simplified current control structure.

disturbance terms:

$$i_g = i^* \frac{G(s)T(s)}{1+G(s)T(s)} + V_g \frac{G_F(s) - Y(s)}{1+G(s)T(s)} \tag{3.18}$$

where $G_{i_{c-d}}$ and $G_{i_{g-d}}$ are the aforementioned voltage to current transfer functions with regard to the converter-side and grid-side currents, considering the resistors on both sides. They are replaced by the $T(s)$ and $Y(s)$, which are regarded as the admittance transfer function seen from the converter output voltage and grid voltage respectively [43].

$G(s)$ is $G_c(s)G_{notch}G_d(s)G_{inv}(s)$ and $G_F(s)$ represents $G_f(s)G_d(s)G_{inv}(s)$. The transfer function of the equivalent grid impedance can be written as:

$$Z_g(s) = \frac{1+G(s)T(s)}{G_F(s) - Y(s)} \tag{3.19}$$

Theoretically, a high (or infinite) grid impedance at the frequency implies a high blocking capability of the flow of harmonics components into the grid. As it can be observed from the grid impedance formula, the filter-related admittance transfer functions are fixed once the LCL parameters are selected. However, if a resonator at a specific frequency is adopted in the compensator, then $G_c(s)$ has a large magnitude at that frequency, which means the

grid impedance also becomes large at that frequency [44–46]. Hence the resonators can be added to the current controller to shape the whole grid impedance transfer function. The idea of implementing a resonator comes from the Proportional Resonant (PR) control

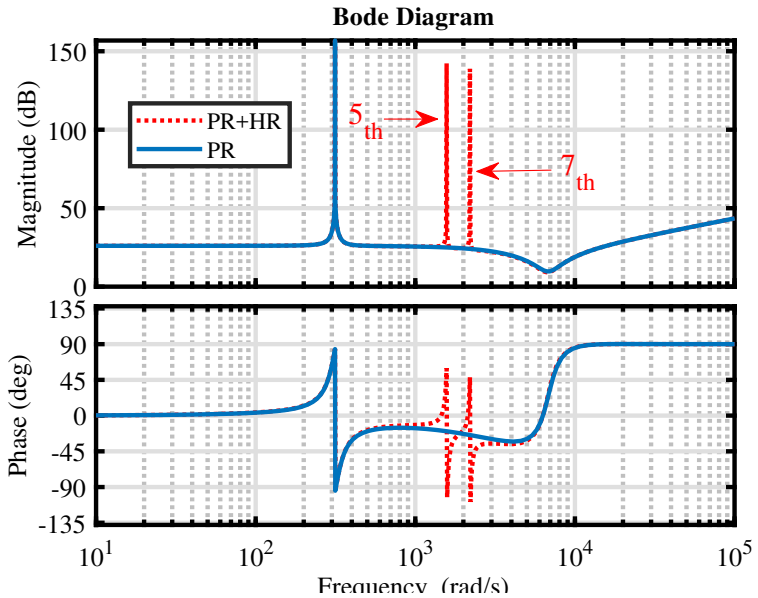


Figure 3.34: Bode plot of Z_g with PR and PR+HR controller.

in $\alpha\beta$-frame. In stationary ($\alpha\beta$) frame, PR is used for tracking the sinusoidal reference at fundamental frequency. Adding harmonic resonators (HR) in parallel with the PR compensator will not affect the reference tracking capability and can effectively increase those harmonic impedance, as shown in Fig.3.34. The transfer function of PR + HR controller can be generally expressed as:

$$G_{PR+HR}(s) = \underbrace{k_p + \frac{k_r s}{s^2+\omega^2}}_{\text{PR}} + \underbrace{\sum_{h=3,5,7\ldots}^{\infty} \frac{k_{rh} s}{s^2+\omega_h^2}}_{\text{HR}} \tag{3.20}$$

where ω_h ($\omega_h = h\omega$) is the frequency of the harmonics to be eliminated, e.g., 5_{th} and 7_{th} harmonics in Fig.3.34. K_{rh} is the resonant coefficient for the corresponding frequency.

3.2.2 Harmonics Controller in *dq* Frame

Nevertheless, the control used in this thesis is based on the rotating frame for the control of power with regard to the dq components of the grid-side current. Therefore, the relation between a space vector in different coordinates should be identified to transform the resonators into dq frame:

$$\vec{f} = f_\alpha + jf_\beta \tag{3.21}$$

$$f_d + jf_q = (f_\alpha + jf_\beta)e^{-j\omega t} \tag{3.22}$$

where $\vec{f}$ refers to the space vector representation of the controlled signal. The harmonics are generally classified into three types in space vector form: positive-sequence, negative-sequence and zero-sequence (or triple harmonics). Only positive- and negative-sequence harmonics are considered in grid distortion in this thesis because the three-wire system has a high impedance for zero-sequence components. The positive and negative-sequence harmonic frequencies are generally expressed as follows:

$$\begin{cases} \omega_+ = (3n+1)\omega t, & n = 1,2,3\cdots \quad (3.23) \\ \omega_- = -(3n-1)\omega t, & n = 1,2,3\cdots \quad (3.24) \end{cases}$$

After one fundamental frequency unit shift, the frequency in dq frame becomes:

$$\begin{cases} \omega_{dq+} = 3n\omega t, & n = 1,2,3\cdots \quad (3.25) \\ \omega_{dq-} = -3n\omega t, & n = 1,2,3\cdots \quad (3.26) \end{cases}$$

which means one resonator in dq frame is able to reject adjacent positive and negative-sequence harmonics [46]. This is the advantage of adopting harmonics controller in dq frame for this thesis because only two resonators (6^{th} and 12^{th}) are required to reject the influence of 5^{th},7^{th},11^{th} and 13^{th} harmonics in the grid voltage on the grid-side currents. The transfer function of the compensator $G_c(s)$ in dq-frame becomes:

$$G_c(s) = k_p + \frac{1}{T_i s} + \frac{k_{r6} s}{s^2 + (6\omega)^2} + \frac{k_{r12} s}{s^2 + (12\omega)^2} \quad (3.27)$$

The control structure of the PIR is illustrated in Fig.3.35, where the PI controller is in parallel with the resonators. The bode diagram of the current control loop with the PIR

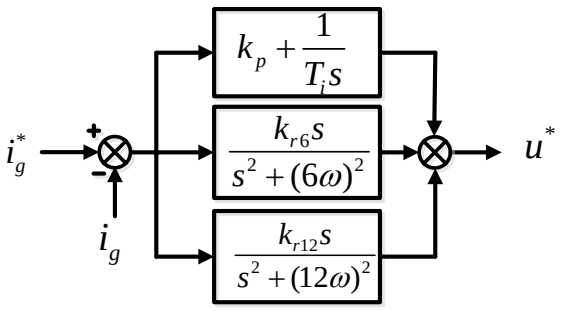


Figure 3.35: Control structure of PI+HR controller.

structure is shown in Fig.3.36. The parameters are shown in Table.3.3.

Parameter	Value
k_p	3
T_i	0.8ms
a_Δ	0.1
$\Delta_{\omega_{res}}$	$0.1\omega_{res}$
k_{r6}	200
k_{r12}	200

Table 3.3: Controller parameters.

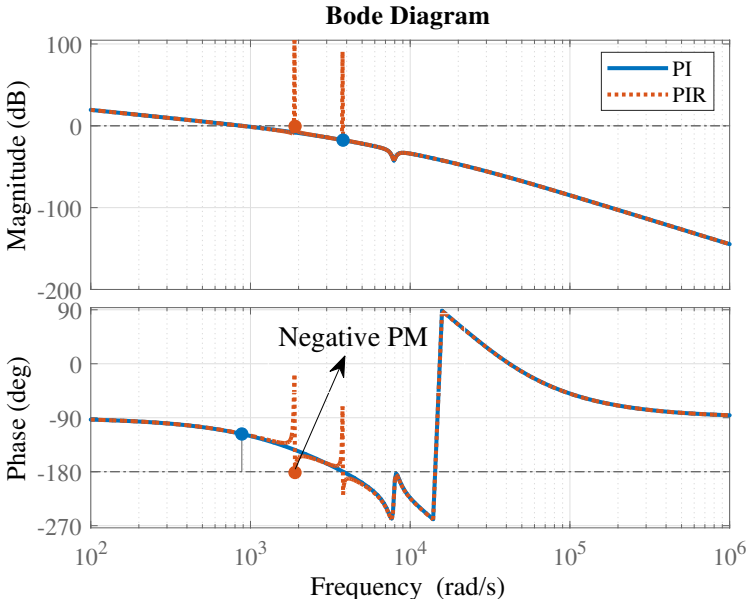


Figure 3.36: Bode plot: current loop with PI and PIR compensator.

As depicted in Fig.3.36, the current control loop has a smaller phase margin and even becomes unstable due to the sharp phase drop of the resonator. In fact, eq. (3.27) describes an ideal PI+Resonator control structure with a large gain at the specified frequencies. Besides, there is no phase shift and gain for the other frequencies [45]. Practically, the drawback of implementing this ideal resonator is the potential stability problem caused by the phase margin reduction. Another disadvantage is the very narrow bandwidth of the ideal resonator, which results in a high sensitivity of the control toward a slight variation of frequency in a typical power system [47].

To avoid the aforementioned problems, the non-ideal resonator [45, 47, 48] is adopted here and the modified current compensator is expressed as:

$$G_c(s) = k_p + \frac{1}{T_i s} + \frac{k_{r6}\omega_c s}{s^2 + 2\omega_c s + (6\omega)^2} + \frac{k_{r12}\omega_c s}{s^2 + 2\omega_c s + (12\omega)^2} \tag{3.28}$$

where ω_c is the cut-off frequency, representing the limits of the non-ideal resonator. Typically, ω_c is chosen as 1 .. 10 [47] and 2 is chosen in this thesis. The bode diagram of

the current loop with the modified PIR is shown in Fig.3.37. As it can be seen from the

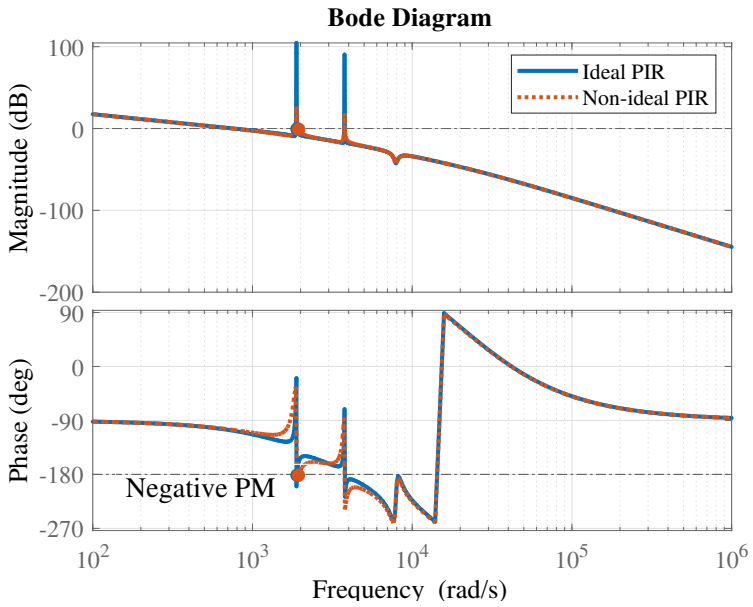


Figure 3.37: Bode plot: current loop with ideal and non-ideal PIR compensator.

bode diagram, adopting non-ideal resonator can not solve the stability problem due to the phase lag of the resonator, even though the phase margin is improved slightly.

3.2.3 Phase Compensation

In order to improve the negative phase margin of the current control loop due to the phase lag of resonators, some phase compensation methods can be used. Two generally adopted methods are introduced here: *Zero Compensation* and *Lead Filter* .

- Zero Compensation

The transfer function of the zero compensation is expressed as:

$$G_z(s) = (1 + \frac{s}{\omega_{ref}}) \tag{3.29}$$

where ω_{ref} is the zero that the transfer function provides.

- Lead Filter

The lead filter and its transfer function are introduced in Chapter.2. The transfer function is written here again to compare with that of the zero compensation.

$$F_{lead}(s) = \frac{s + (p_1/\alpha)}{s + p_1} \tag{3.30}$$

where

$$\delta_m = \arcsin \frac{\alpha - 1}{\alpha + 1}$$
$$\omega_m = \frac{p_1}{\sqrt{\alpha}} \tag{3.31}$$

The bode diagrams of the two phase compensation methods are shown in Fig.3.38. Lead

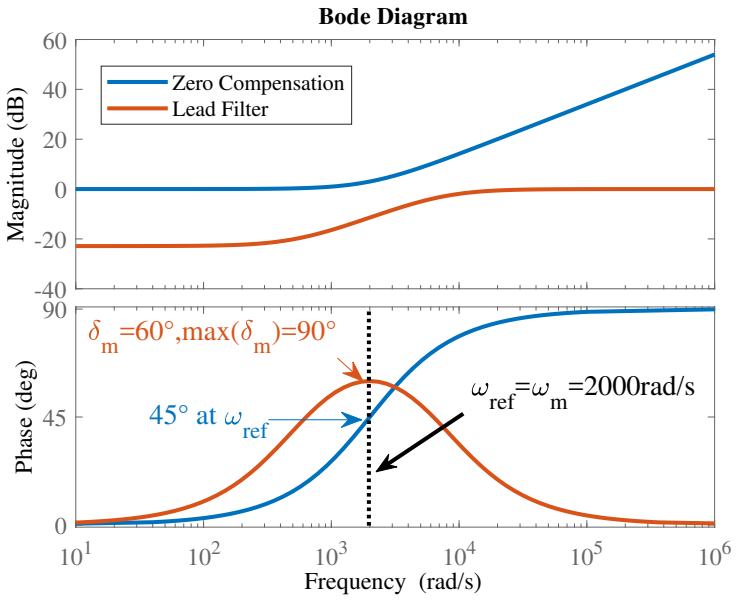


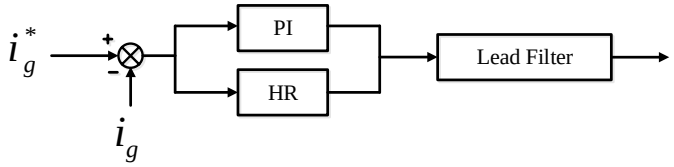
Figure 3.38: Bode plot: zero compensation and lead filter.

filter can provide a maximum phase lead δ_m of 90° at ω_m while not influencing the phase at both low and high frequency range. In contrast, zero compensation can provide 45° at ω_{ref} while exhibiting 90° at the high frequency region. Additionally, the lead filter decreases the magnitude of the open loop gain at the low frequency range while the zero compensation increases the magnitude of the open loop gain at the high frequency range. On one hand, the phase compensation should be achieved without sacrificing the open loop gain. On the other hand, gain increase near resonance frequency is not desired because this will deteriorate the effectiveness of notch filter on the resonance problem.

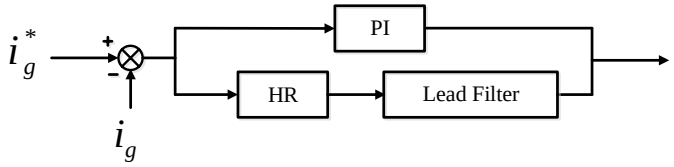
The placement of the phase compensation makes a significant difference to the open loop gain and phase of the current loop. The lead filter or the zero compensation can be put in series with the compensator or only in series with the harmonics resonators part. The four different types of structures are depicted in Fig.3.39. The bode diagram of the current loop with the aforementioned four different compensation types are shown in Fig.3.40. The ω_{ref} for zero compensation is set as 1000 in order to provide as large phase lead as possible at frequency larger than 6ω. ω_m for the lead filter is selected as 12ω to increase the phase margin of the last resonator. A maximum of 60° is provided by the lead filter in this comparison. Other control parameters remain as listed in Table.3.3.

As it can be seen from the bode diagram, Lead filter after the compensator can realize adequate gain and phase margins but it results in significant gain drop for the low

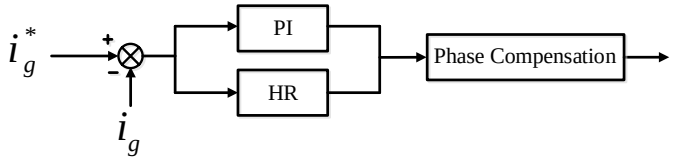
frequency range, which reduces the bandwidth of the closed loop of the current control. By contrast, lead filter after the harmonics resonators can achieve suitable gain margin and phase margin (GM:10.5dB, PM:35°) while maintaining the original loop gain at the low frequency range. Zero compensation after the controller can provide a sufficient gain and phase margins (GM:17.5dB, PM:34.5°) while increasing the loop gain at the high frequency range without influencing the stability. This occurs because the notch filter has a quite large attenuation at the notch frequency, which guarantees a safe gain margin despite the increase of the gain due to the phase compensation. In comparison, the phase compensation after the harmonic resonators has the worst condition, which displays marginal stability due to the low gain and phase margins.



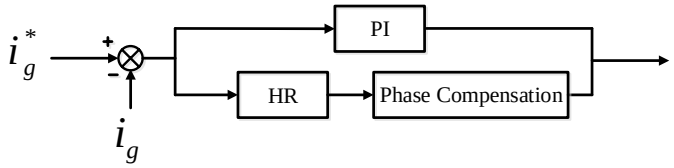
(a) Lead filter after the compensator



(b) Lead filter after harmonics resonators part



(c) Zero compensation after the compensator



(d) Zero compensation after harmonics resonators part

Figure 3.39: Structure of different phase compensation cases.

It is noteworthy that lead filter after the harmonics resonators and phase compensation after compensator can avoid the disadvantages of the lead filter and the phase compensation methods while increasing the phase margin significantly. However, the open loop gain of the current control with the lead filter at the low-order harmonic frequencies is much smaller than that of the current control with the zero compensation. This leads to the small grid impedance at those harmonic frequencies in the current control with

lead filter, which means the harmonics distortion from the grid voltage can not be sufficiently rejected . This is because the notch filter decreases the gain in the frequency band $\omega_{res} \pm \Delta\omega_{res}$. If smaller $\Delta\omega_{res}$ is chosen e.g. $0.01\omega_{res}$, the open loop gain at the specified frequency will become larger for the current control with lead filter.

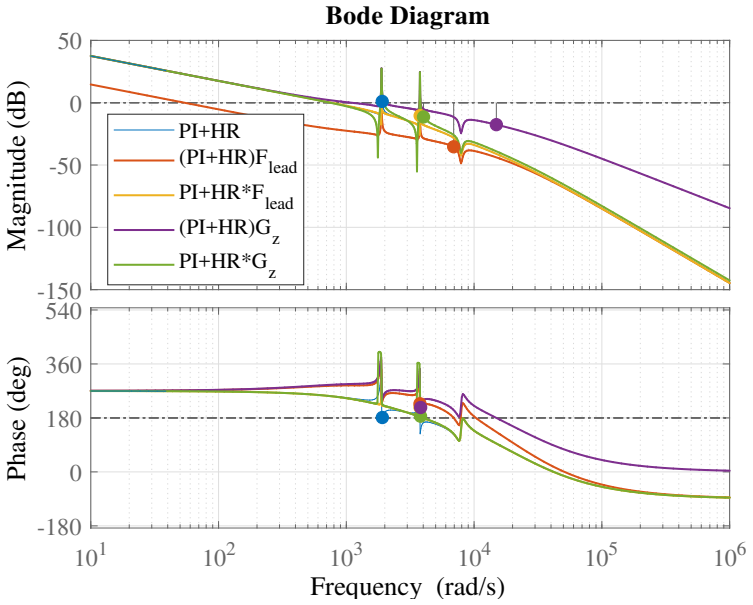


Figure 3.40: Bode plot: comparison between different phase compensation cases.

Fig.3.41 and 3.42 show that with smaller $\Delta\omega_{res}$, the phase margin of the current control loop with both lead filter and zero compensation will be improved. Additionally, the open loop gain at the low-order harmonic frequencies are increased significantly. For the current loop with the zero compensation, $\Delta\omega_{res}$ can not be made too small, otherwise the resonance of the LCL filter can not be effectively damped by the notch filter and this results in instability. Therefore, for this thesis, lead filter is adopted because of its easier implementation in continuous control in MATLAB/Simulink.

Fig.3.43 presents the complete control structure of the current loop with the notch filter, harmonics resonators and lead filter. The dq components of the grid current must be decoupled to be controlled independently, otherwise the aforementioned design can not be directly applied in this structure. However, due to the existence of filter capacitor, the dq components of the capacitor and the grid currents are coupled together. Ideally, an additional current measurement or capacitor voltage is required to be fed forward to the control loop to fully decouple the dq components of the grid-side current. The feed-forward decoupling term can be simplified as ωL ($L = L_g + L_c$). However, this approximation is reliable provided that the filter capacitor is large enough.

The harmonics control is verified in the simulation based on the STACOM mode operation of the described VSC system. The VSC is connected to the grid described in Table.3.2. The controller parameters are chosen based on Table.3.3. The VSC system delivers 2000 VAR reactive power to the PCC and regulates the DC link voltage to 750V. The grid-side

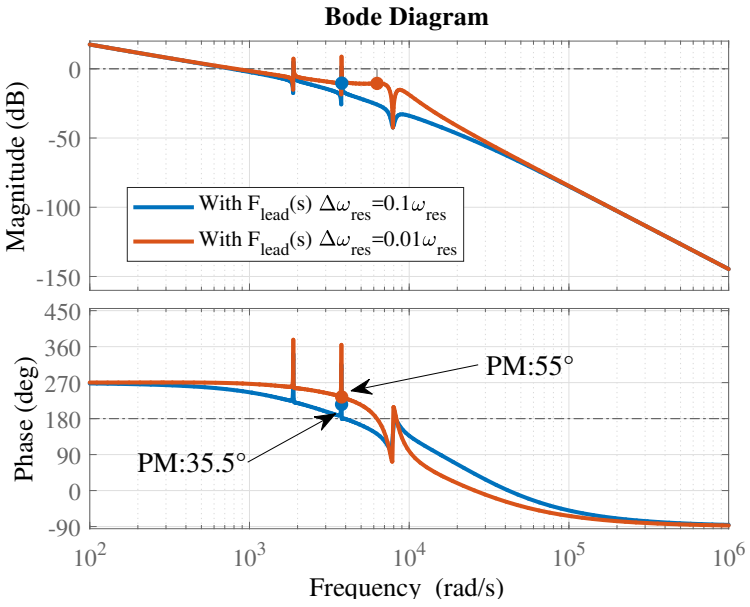


Figure 3.41: Bode plot: increased gain of the current loop with the lead filter at the harmonic frequencies with smaller $\Delta\omega_{res}$.

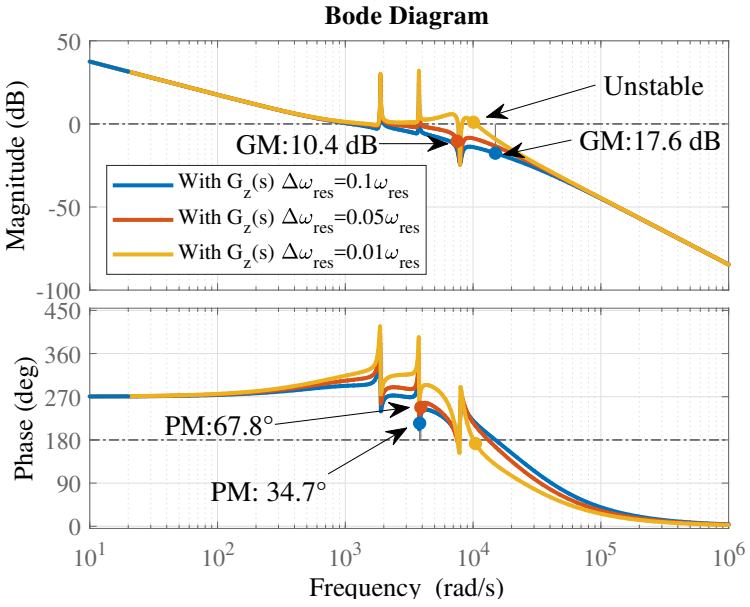


Figure 3.42: Bode plot: increased phase margin of the current loop with the lead filter at the harmonic frequencies with smaller $\Delta\omega_{res}$.

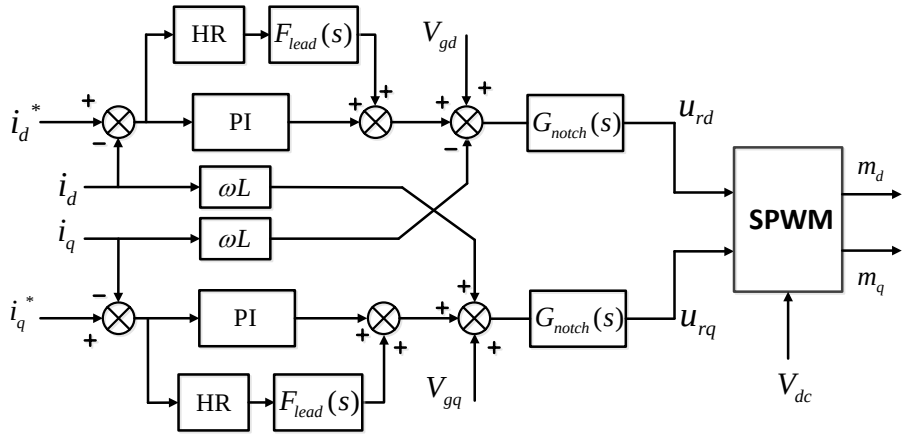


Figure 3.43: Complete control structure of the current loop.

current of the VSC system with and without the harmonics controller are shown in Fig.3.44 and 3.45, respectively.

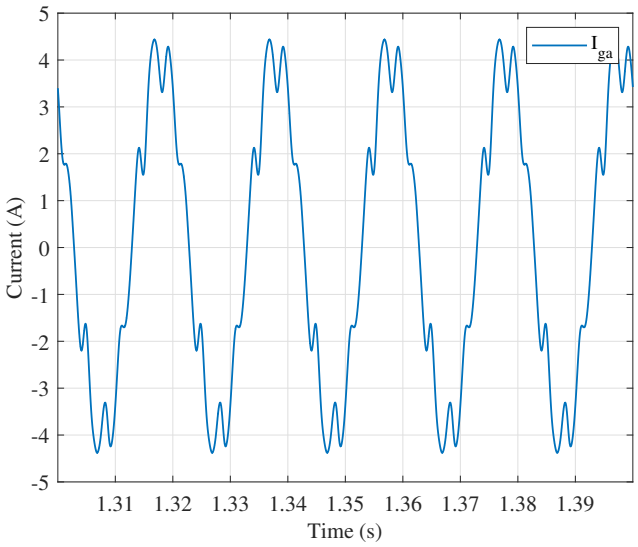


Figure 3.44: Grid-side current under the distorted grid (no harmonics control).

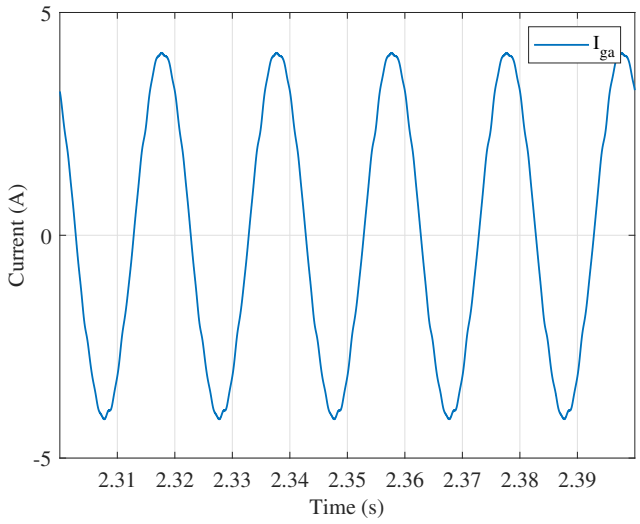


Figure 3.45: Grid-side current under the distorted grid (with harmonics control).

The current THD is reduced from 15.57% to 2.03% after the harmonics controller is used. Specifically, the $5^{th}, 7^{th}, 11^{th} and 13^{th}$ harmonics components drop from 3%, 14.7%, 3% and 2.4% to 0.54%, 1.2%, 0.3% and 0.6% respectively. According to the IEEE STD 519-2014, the 3_{rd} to 10_{th} harmonics in the current should be below 4% and $11_{th} to 17_{th}$ harmonic components should be below 2% for a system rated between 120 V to 69 kV. Meanwhile, the total THD should be smaller than 4%. Therefore, the simulated grid-side current is acceptable after the implementation of harmonic resonators.

3.3 EXPERIMENTAL RESULTS

3.3.1 Verification of Voltage and Power Controller in STACOM mode

With the designed notch-filter based current controller, the lab-scaled three phase two-level VSC operates in STACOM mode (Fig.3.46) while delivering 1000 VAR to the PCC with the connection to the ideal voltage source (V_{rms}=230V, f=50Hz). The output AC voltage and the grid-side current are shown in Fig.3.47.

The power spectrum analysis on the grid-side current shows that the THD is found to be at 1.43% and the THD for the harmonics performance is acceptable IEEE standard 519. The DC link voltage ripple is around 0.6 V at 750 V, which is relatively small.

3.3.2 Verification of Harmonics Control

The verification of the harmonics controller is done in STACOM mode. The experimental results are shown in Fig.3.48a and 3.48b.

The amplitude (in % of the fundamental) of the harmonics in the grid-side current without resonators at Q^*=2000 VAR are 5^{th}:15.7%, 7^{th}:6.7%, 11^{th}:4.7%, 17^{th}:2.8%, which

Figure 3.46: Experimental setup showing a single grid connected VSC operating as a STATCOM under distorted voltage.

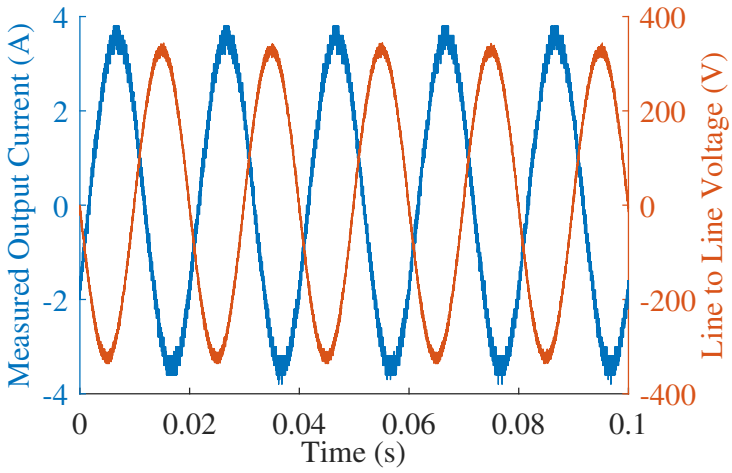
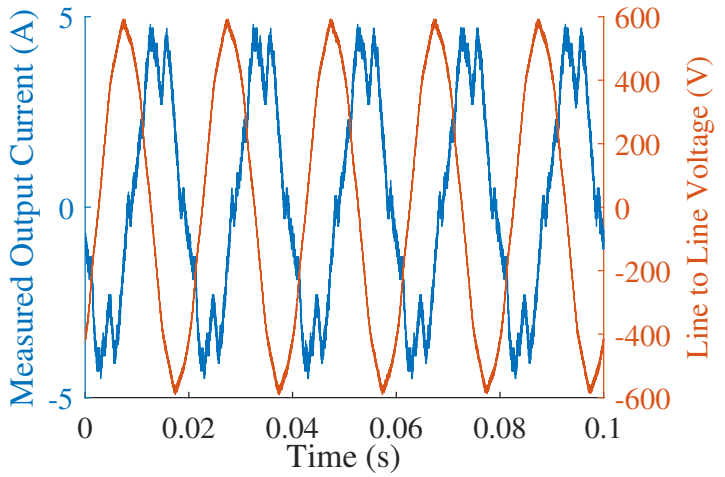
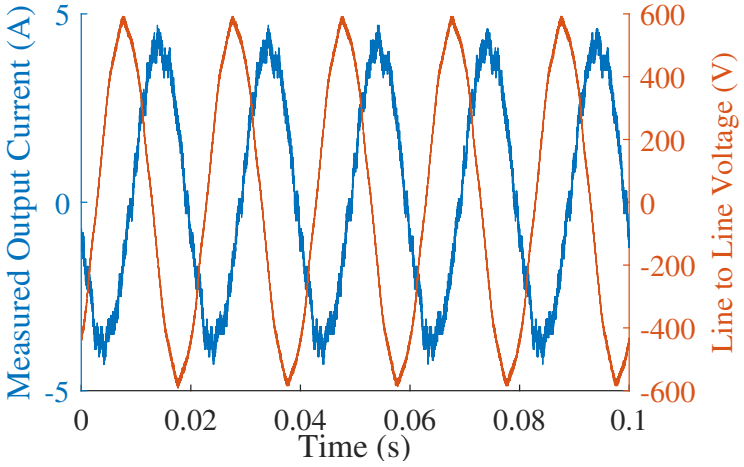


Figure 3.47: Measured waveforms with purely sinusoidal 50 Hz grid voltage.



(a) Without HR control.



(b) With HR control.

Figure 3.48: Measured converter output currents under distorted grid voltage.

leads to an THD of 18.86%. After implementing the harmonics resonators, the THD improved to 7.37% and the individual current harmonics to: 5^{th}:2%, 7^{th}:1.9%, 11^{th}:2.96%, 13^{th}:1%, 17^{th}:1.4%. The 5^{th} and 7^{th} resonators can effectively reduce the selected harmonics in the grid-side current. However, the current THD is still very high. The reason for the difference between the simulation and experimental results can be explained by the fact that the influence of the necessary half-bridge switches dead-time effect as well as the influence of sensor delay are not considered in the simulation and for the control design. The dead-time effect will contribute to the distortion of the output voltage and thus increase the harmonics in the current. Additionally, the delay effect of the current and voltage sensors can influence the open loop system as the control delay does to the system. However, these information are absent and the VSC system has some unknown damping elements which make the design of the notch filter more complicated.

4 RE-CONFIGURATIONS OF POINT-TO-POINT ENERGY DISTRIBUTION SYSTEM BASED ON PARALLEL AC AND DC LINKS

The objective of this chapter is to show the capability of online reconfiguration of parallel AC and DC links to be used in point-to-point energy distribution systems. the re-configurations are achieved at near-zero currents to minimize arcing formation in mechanical switchgears. This re-configuration strategy is verified in the simulations of the parallel AC and DC links with 9 conductors. The control for ZSCC suppression and standalone mode are also tested in laboratory experiments for further validation of this re-configuration.

4.1 PARALLEL AC AND DC RE-CONFIGURABLE LINKS SYSTEM

4.1.1 System Description

The structure of the studied parallel AC and DC re-configurable links is symmetric in relation to the middle point of the distribution cables. Thus both the receiving- and sending-end substations of the point-to-point energy distribution system have a symmetric circuit structure. A suitable schematic for the sending-end side of the re-configurable links with 6 conductors/cables is illustrated in Fig.4.1. Generally,the total number of link conductors N is a multiple of three, which in most cases would be 6 or 9 to meet the potential redundancy requirements [6]. The number of links operating in AC (N_{ac}) is always the multiple of three because of the three-phase three-wire AC implementation. Meanwhile, the number of links operating in DC (N_{dc}) is always even when the symmetrical monopolar DC link is implemented (no grounded line), as shown in the DC feeder in Fig.4.1. $Sac_n(n = 1,2,3)$ and $Sdc_n(n = 1,2,3)$ in Fig.4.1 represent the three phase AC and the un-grounded monopolar DC switches, namely the switches in each pair of AC links (3X AC1,3X AC2) and DC links (2X DC1, 2X DC2, 2X DC3) on both sending- and receiving-end sides.

The parallel AC and DC re-configurable links system has $\frac{N}{3}$ possible configurations (full AC links operation is excluded) to fully utilize the link conductors [6]. For the case of 6 link conductors, the re-configurable system has 3 configurations. C_n represents a n configuration, where n assumes an integer from 1 to $\frac{N}{3}$ and $C_{\frac{N}{3}+1}$ (C_3 in this case)

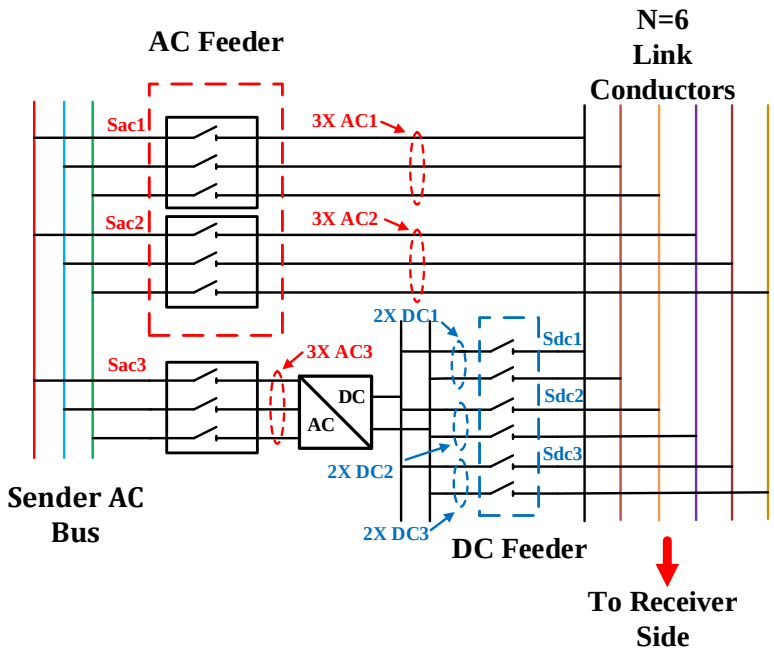


Figure 4.1: Sending-end side of the re-configurable link (6 link conductors).

especially refers to the configuration of full AC links operation. The number of links for AC operation is represented by:

$$N_{ac,C_n} = 3(n-1) \tag{4.1}$$

where n is the integer from 1 to $\frac{N}{3}$. Hence, the number of links operating in DC is given by:

$$N_{dc,C_n} = \begin{cases} N - N_{ac,C_n}, & \text{if } N - N_{ac,C_n} \text{ is even} \\ N - N_{ac,C_n} - 1, & \text{otherwise} \end{cases} \tag{4.2}$$

The number of redundant link conductor is the subtraction of total links number and the links in AC and DC operations, as shown in eq. (4.3).

$$N_r = N - (N_{ac,C_n} + N_{dc,C_n}) \tag{4.3}$$

For the case of 6 link conductors, there is one redundant link available for hybrid AC-DC operation. The redundant link can be inserted into the system to maintain or enhance the total system transfer capacity when a single fault happens in one healthy link, as explained in [13]. The re-configuration during fault is out of scope of this thesis and the redundant link is not used during normal operation of this system.

The on and off states of the switches (or disconnectors) of the re-configurable links determine the operation of the parallel AC and DC links. Theoretically, this system has three types of operations: hybrid AC-DC configuration, full (only) AC or DC links operations. Table.4.1 gives the configurations of the system with 6 link conductors.

	full DC links (C_1)	hybrid AC-DC links (C_2)	full AC links (C_3)
N_{ac}	0	3	6
N_{dc}	6	2	0
B2B control mode	Voltage+Standalone	Voltage+Power	Voltage+Voltage

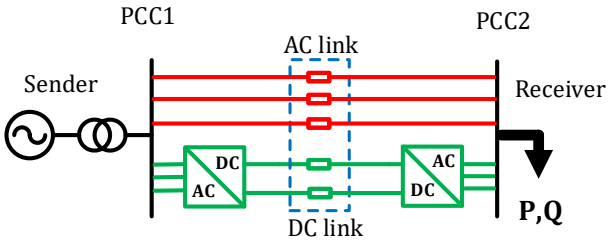
Table 4.1: Number of AC and DC links, mode of control under different configuration with 6 link conductors.

The Back-to-Back (B2B) system is the fundamental operational block for performance enhancement in parallel AC and DC re-configurable links. For different operational configuration, the B2B converters should operate in corresponding mode and thus different control techniques are required, as specified in Table.4.1. The different configurations are depicted in Fig.4.2, where the AC links (3X) and DC links (2X) are simplified as a single link in red and green respectively. In the hybrid AC-DC configuration - C2, both the sending- and receiving-end VSC operate in grid-connected mode because the sender VSC at the AC side is connected to the grid through the enabled AC links. This VSC operates as a DC voltage source to adjust/control the DC-link voltage while the receiver VSC controls the active and reactive power flows from or to the AC side. In full (only) DC links operation - C1, the control of the sending-end VSC remains while the receiving-end VSC is required to operate in standalone (island) mode to deliver full power to the load due to the absence of grid connection. When the system is configured into full (only) AC links - C3, it loses the controllability of power since the DC links are disconnected. Hence, the active and reactive powers flowing through the AC links are defined by the AC loads in the receiving-end substation. Meanwhile the two grid connected VSCs are isolated from each other due to the disconnection of DC links and they could be advantageously used for operation as Static Synchronous Compensators (STACOMs) in order to provide reactive power to the PCC. This can potentially reduce the reactive power circulation through the AC links, improving energy efficiency, and above all the voltage stability of the distribution network [15, 49].

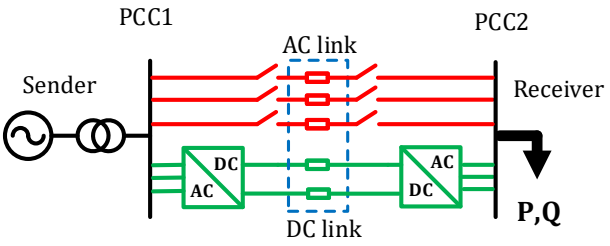
4.1.2 Prototype Design of Re-configurable Links

In this thesis, a prototype of parallel AC and DC re-configurable based on 6 link conductors is designed and realized. Due to the practical limitations, Single Pole Single Throw - Normally Open (SPST-NO) relays are chosen as the mechanical switches in the re-configurable links because the aim of this thesis is to validate the proposed manoeuvring strategies and thus a more practical designof a high power MV application becomes out of concern.

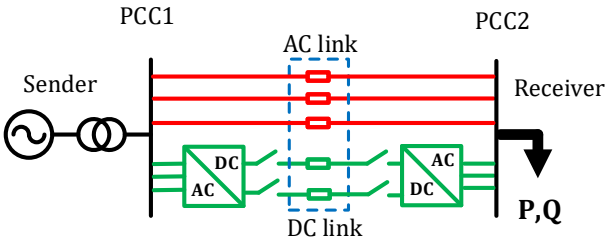
As shown in Fig.4.1, the AC and DC line are connected to the conductors corresponding to the specified phase in the three phase AC lines (3X AC1 and 3X AC2) and un-grounded monopolar DC lines (2X DC1, 2X DC2, 2X DC3). The arrangements of the link conductors are made in such a way that they are connected to the AC and DC lines in the sequence from 3X AC1 to 3X AC2 and from 2X DC1 to 2X DC3 respectively. In the design of the re-configurable links, the switches are optically commanded by an external controller. However, to prevent the connection of a specific link conductor to both AC and DC operation modes, an additional protection layer in the hardware using digital logics is implemented.



(a) C2: Hybrid AC-DC links.



(b) C1: Full DC links.



(c) C3: Full AC links.

Figure 4.2: Circuits for different configurations.

Therefore, the three phase switches *Sac* and DC switches *Sdc* occupying the same link conductors must have a NAND logic of operation and the truth table of the NAND logic is listed below:

Sac	Sdc	Y
0	0	1
0	1	1
1	0	1
1	1	0

Table 4.2: Truth table of NAND logic.

Based on this principle, the hardware protection logics for the re-configurable links with 6 link conductors is designed as shown in Fig.4.3. The output of the control variable E represents an enable signal for all the switches. A wrong control commands for the switches will disable all the switch signals to the relays. The control logic for protection can be similarly designed for the 9 links case. The prototype of the re-configurable links

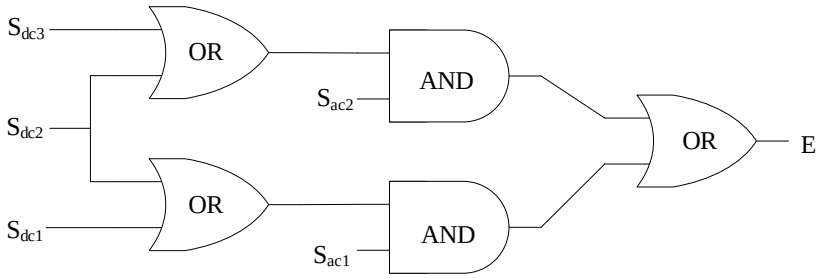


Figure 4.3: Protection control logic.

with 6 conductors is shown in Fig.4.4. The input signal for the relays in this prototype is connected to the optical fiber devices, whose inputs is provided by a OPAL-RT, i.e. a Real-time digital simulator. A 2Ω link conductor is emulated as the resistance of the long distribution lines.

4.2 ZSCC CONTROL IN GRID-CONNECTED BACK-TO-BACK SYSTEM

4.2.1 ZSCC in Parallel VSCs

With the proposed control in Chapter.3, both of the B2B VSCs can operate in grid-connected mode while realizing the DC link voltage and power control. Nevertheless, previously reported research shows that a potential zero-sequence circulating problem occurs in the applications of parallel inter-leaved VSCs [50–53]. According to [54] , flow of ZSCC (zero-sequence circulating current) is founded in the hybrid AC-DC operation with MMC VSCs due to the existence of low impedance path for the zero-sequence circulating current.The

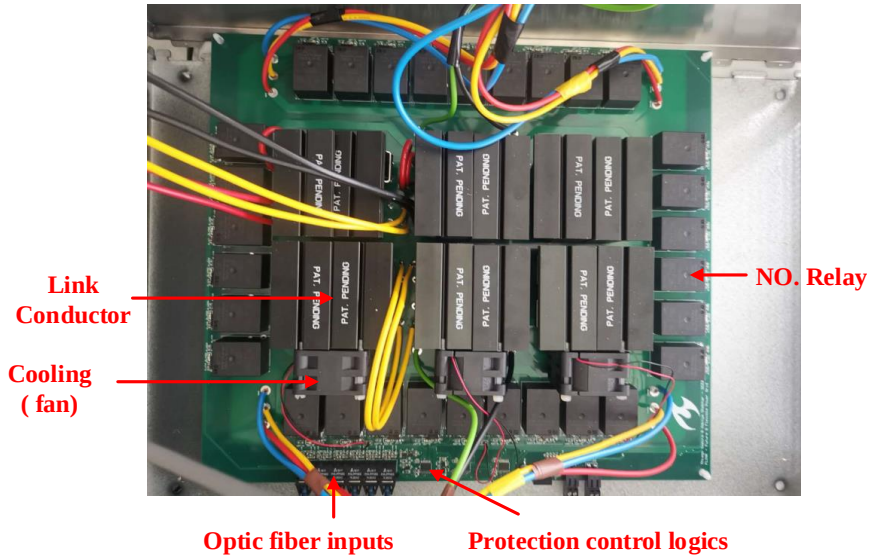


Figure 4.4: Prototype of re-configurable links.

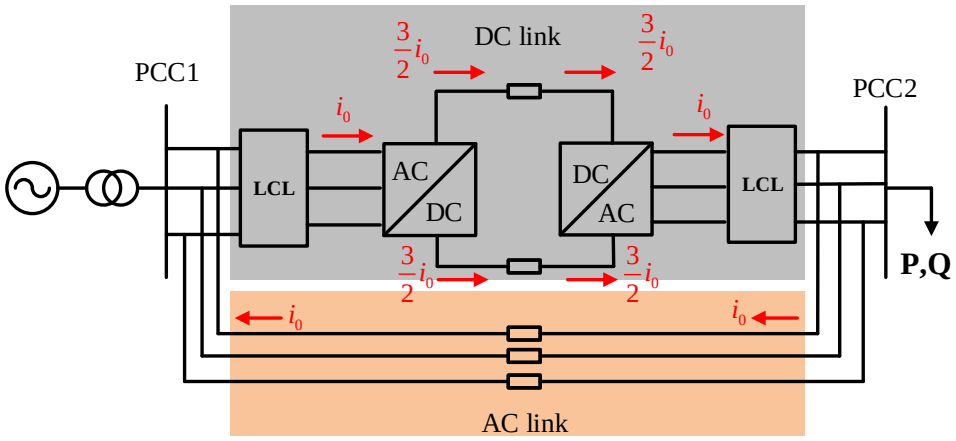


Figure 4.5: A path for zero-sequence current component is shown between the hybrid AC-DC links system.

circulating current path in the hybrid AC-DC links operation or C2 is shown in Fig.4.5. As it can be observed, when considering a symmetric circuit arrangement, in each conductor of the DC link, the ZSCC component has a magnitude of $\frac{3}{2}$ times that of the one in the AC link. The DC link ZSCC component is also divided equally into three parts flowing into the VSC and the three AC link conductors. Note that ZSCC can cause undesirable effects and problems, such as saturation of common-mode inductors, distorted output currents and lower system efficiency [55]. Therefore, ZSCC should be suppressed.

Note that the ZSCC can have both high-frequency and low-frequency order harmonic components. In parallel AC and DC links, the later contributes the most to the ZSCC because the AC filter inductances and cables are the major components defining the system impedances, hence it is the most critical component [52].

The ZSCC can be generated in this parallel AC-DC system if the asymmetries exist in both hardware and modulations (or control). To be more specific, the ZSCC is created because of the difference between the switching states of the parallel connected VSCs [56]. One the other hand, the low-frequency ZSCC is initiated on accounts off the different common-mode (CM) injection modulation strategies of the parallel VSCs [57]. Even if the same modulation strategies are adopted for the parallel VSCs, the low-frequency is still present if the fundamental components of the terminal voltage of the two VSCs are different. That is, the CM voltage difference between the two parallel VSCs is the reason for the generation of ZSCC in this application [58]. Therefore, the Zero-Sequence Voltage (ZSV) generated by the VSC is of concern. The suppression of ZSCC can be realized by eliminating the difference between the ZSV of the two parallel VSCs or removing the ZSV in each VSC [59].

The choice of modulation technique is thus crucial since the ZSV generated in the terminal voltage relies on the modulation implementation. The conventional SV-PWM, both continuous (CSV-PWM) and discontinuous (DSV-PWM) add the zero-sequence signals to the modulation in order to improve the DC-bus voltage utilization Employing the SPWM technique can avoid the problem of adding the zero-sequence component to the system. However, this results in lower dc-bus utilization but can achieve satisfactory THD. Therefore, SPWM is employed in both VSCs in this thesis.

4.2.2 Suppression of ZSCC

Traditionally, the separation of the AC and DC power supplies as well as the addition of an isolation transformer to the AC side can make an equipment open circuit for the zero-sequence component, thus suppressing the circulating current effectively. However, this method results in a bulky and costly system [52, 55]. Additionally, other solutions such as adopting CM inductors or high-impedance coupled inductors in the circulating path could be used to limit the circulating current [53, 59]. However, these method can only efficiently suppress the ZSCC components at medium and high frequency.

Active methods are the preferred options for attenuating the low-frequency order ZSCC in order to avoid unnecessary bulky passive elements [53]. An effective active method to suppress the ZSCC in the system is adding an ZSCC controller in the current control loop. The PI-based control is the widely used in the ZSCC controller [50, 60]. The control structure of the PI-based ZSCC controller with anti-windup is shown in Fig.4.6. The reference of ZSCC is set as zero and the actual ZSCC is calculated as $\frac{1}{3}$ of the sum of the three

phase currents. The function of the anti-windup part is to avoid high currents flowing into the converters due to the non-linearity caused by the saturation block. The controller parameters k_p and k_i are tuned based on the link length dependent inductance [54].

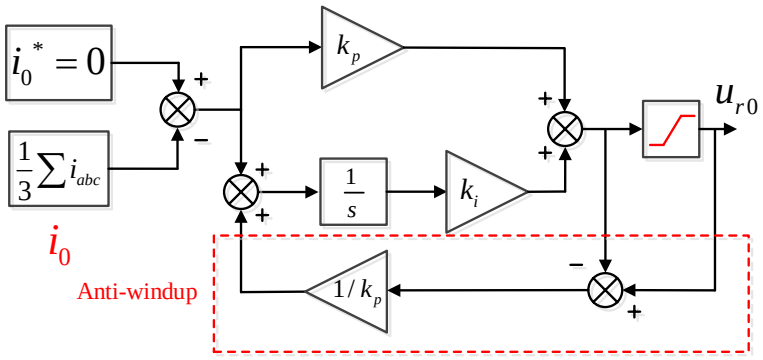


Figure 4.6: ZSCC PI control structure with anti-windup.

Aside from PI controller, PIR (PI+Resonator) controller is proposed in [61] to effectively mitigate the low-frequency ZSCC components. The third harmonic component in the ZSCC observes a large grid-side impedance after the resonator tuned at 3ω is implemented. Thus the third harmonic component in the ZSCC can be effectively suppressed. The PIR structure is the same as the one adopted in Chapter.3 for eliminating the grid-side current harmonics from the grid distortions.

Therefore, the complete current control diagram of the VSC in this system is shown in Fig.4.7. Theoretically, the function of the ZSCC controller is to inject some zero-sequence

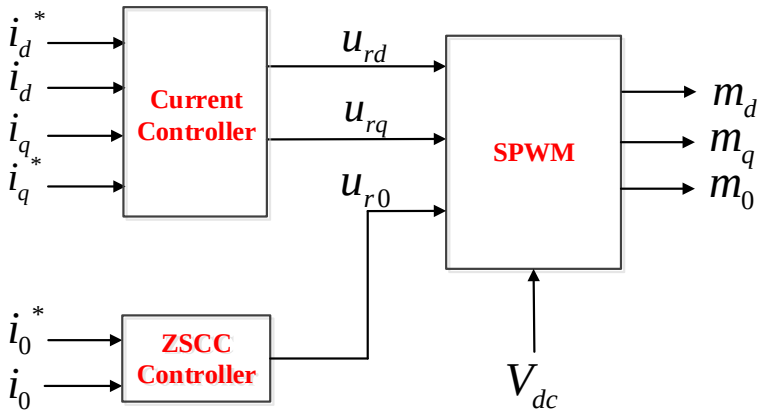


Figure 4.7: Current control diagram with the ZSCC controller.

component to the voltage reference and thus compensate the difference between the ZSV

of the terminal voltages in the parallel VSCs. Therefore, both VSCs can employ the ZSCC control.

4.3 STANDALONE MODE CONTROL IN BACK-TO-BACK SYSTEM

4.3.1 Standalone Operation

In the C1 configuration, when there are no AC links connected, the sender VSC of the back-to-back system is always connected to the grid as discusses in Section.4.1 while the receiver VSC is required to operate in standalone mode.

A VSC system can be connected to an AC system (such as the grid) or it can be used to supply power directly and exclusively to an AC load. The connection point of the VSC system to the AC system refers to the PCC (point of common coupling) in the former case. Conversely, in the latter case The VSC system is required to provide the voltage and its frequency to the AC load. Since the frequency of the voltage is not imposed by the grid, the VSC is commonly referred as the Controlled-Frequency VSC System [15]. This VSC operation is also called standalone (islanded or autonomous) mode.

4.3.2 Voltage Control

As earlier explained, the objective of the control in standalone mode is to regulate the voltage and frequency generated at the PCC. According to [62, 63], the frequency-imposed VSC generally implements the control scheme depicted in Fig.4.8, where two closed control loops are observed, namely the voltage and current loops. The voltage loop regulates the PCC voltage amplitude and frequency by controlling the dq components of the voltage with set references and the frequency reference in the PLL. The q component reference is usually set as zero and then the d component can be set as the nominal value of the expected amplitude of the generated voltage. This is similar to the PLL action in Chapter.2, where V_{gq} is forced to become zero by the controller. Therefore, the PLL block shown in Fig.4.8 is simply the integrator of a fixed frequency with saturation VCO block. The current control remains the same structure which is discussed in Chapter.2. The only difference is that the controlled current in the standalone mode is the converter-side current instead of the grid-side current. However, [15, 63] show that the grid-side current (in this case it is the load current) can be also controlled. The voltage control structure is similar to the current control structure, which is shown in Fig.4.9. The decoupling feed-forward is used to decouple the $d-q$ components in the control loops. After this is performed, the voltage V_d and V_q can be controlled independently, as indicated in the control loop diagram in Fig.4.10. The compensators $k_d(s)$ and $k_q(s)$ for the $d-q$ component are the same, namely $k(s)$. The voltage control loop is shown in Fig.4.10. $K(s)$ is the general compensator for the voltage controller, which usually employs a PI control structure. The second block represents the closed-loop transfer function of the current control loop and $\frac{1}{\tau_i}$ is the bandwidth of the closed-loop of the current control. The last block models the influence of the filter capacitor, which is represented by an integral element.

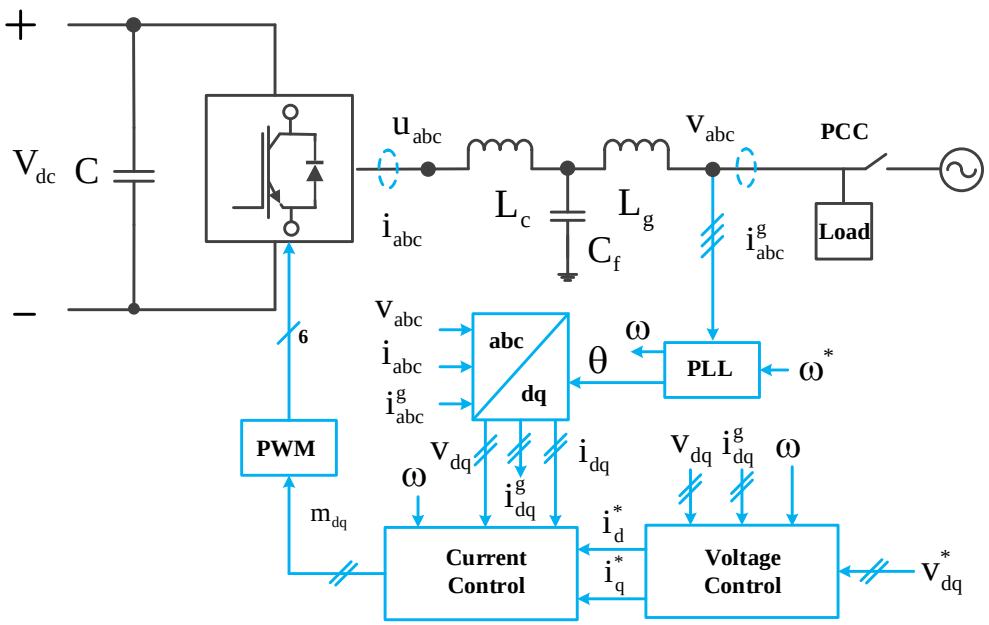


Figure 4.8: Schematic diagram of the voltage control in standalone mode.

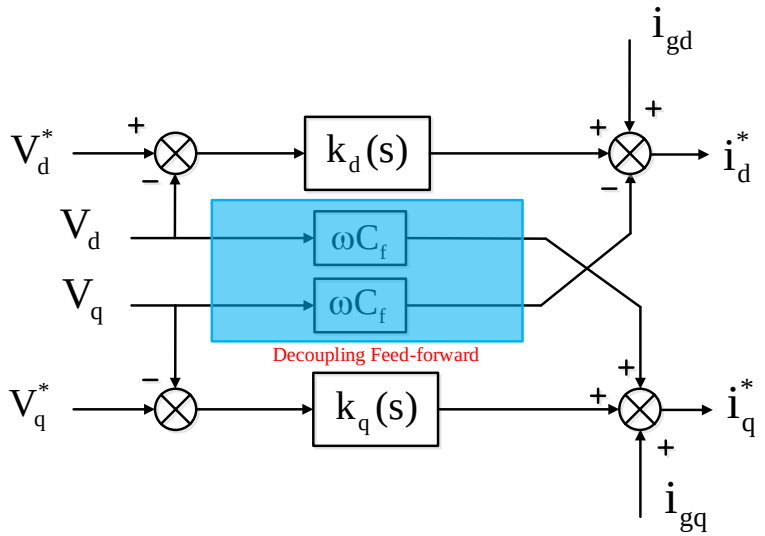


Figure 4.9: Structure of the voltage controller.

The proportional and integrator gains can be designed and chosen based on the similar method used in Chapter.3. Alternatively, since the open loop has two poles at the origin (two integral elements), the symmetrical optimum method introduced in [15, 21, 22] is a suitable way for shaping the loop with two poles at origins.

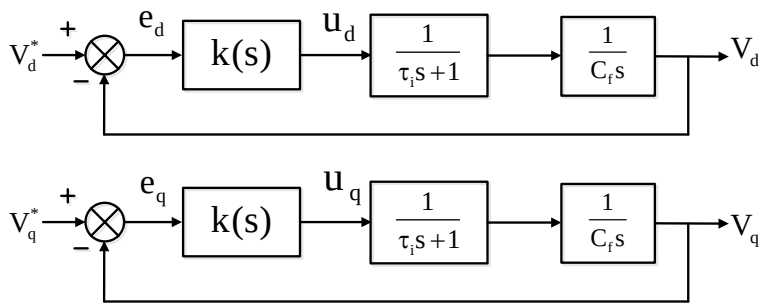


Figure 4.10: Equivalent control diagrams for the closed-loop voltage control.

4.3.3 Transition from Grid-connected to Standalone mode

Since the current control loop remains the same in both grid-connected and standalone mode controls, the transition between both modes is straightforward from the perspective of control. In grid-connected mode, the receiver VSC controls the power and the $d-q$ reference currents derived based on the power to current transformations equations (eqs. (2.37) and (2.38)) while the voltage controller outputs the reference currents in standalone mode. Therefore, a digital switch (or multiplexer) is used to connect the inputs of the current controller to the corresponding blocks, as illustrated in Fig.4.11. The synchro-

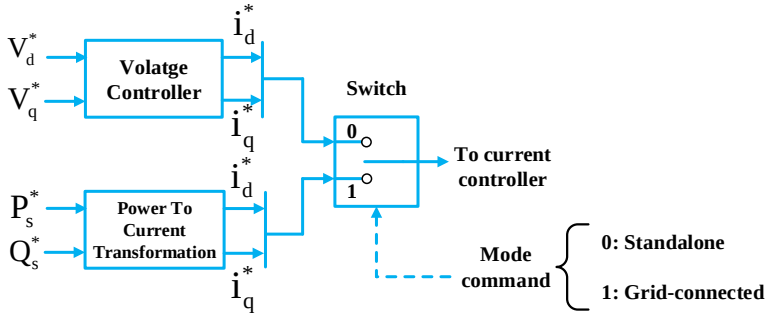


Figure 4.11: Control scheme for operation in both grid-connected and standalone modes.

nization between the mode command signal and the connection or disconnection signal is indispensable. The absence of the synchronization between the two signals will result

in the generation of a voltage with unexpected frequency during the time period between the two signals. This occurs because the VSC will operate in standalone mode with grid-connected control. The unexpected frequency is caused by the saturation block in the PLL of the grid-connected control. Practically, the mock-up of the parallel AC and DC system for this thesis can not realize the synchronization of those signals due to the fact that the triggering signals for the switches and the control signals for the VSC system are generated by two independent communication systems, which are difficult to synchronize.

4.4 RE-CONFIGURATIONS STRATEGY

Aside from the realization of control mode of the B2B VSCs in different configurations, the transition from one mode to another is of great importance. The goal of this thesis is to achieve current zero in the links to be opened during re-configurations in order to prolong the lifetime of the mechanical switch disconnectors or circuit breakers, by means of adjusting the power controllability of B2B system. The idea is to control the receiver VSC to deliver full power to the load before opening the AC links, and to deliver zero power to the load before opening the DC links.

However, it is noteworthy that once the system is configured into full AC links, the VSCs operate in STACOM mode. In this mode, the VSCs can deliver or draw reactive power to the PCC but no control of active power is performed. This implies that this configuration is unable to control active DC power flowing in the link conductors, particularly if there is no available DC conductors in case all of them are currently being used as AC links. In this case a zero current condition (for the switches to be opened) during any re-configuration is impossible and the re-configuration has to be conducted at the cost of opening the AC link switches at rated operating power (current). Similarly, such a system with only one pair of converters in full DC links operation can not re-configure to other configurations with the zero current condition for switches because in standalone mode the DC links are providing the full power to the receiver VSC.

Nevertheless, if an individual pair of converters is connected to each pair of DC links, the zero current condition for switches can be fulfilled because each pair of converter has its own controllability of power and can control the power flowing in their DC links to be zero before the switches are opened. However, the implementation of multiple converter pairs for DC links will most likely increase the system cost and complexity. Therefore, in this thesis only one pair of converter is implemented in the parallel AC and DC re-configurable links system. The re-configurations from full (only) AC or DC links operation to others are not considered. Moreover, the optimal power sharing between AC and DC links power delivery is suggested in [6], where y represents the ratio between power flowing in DC links and the total power in the links, namely P_{dc}/P_{total}. With this optimal power sharing value which is a function of the power factor, power demand, VSCs and cables power efficiency, always the highest achievable efficiency can be attained during operation. Therefore, for hybrid AC-DC links operation, the active power reference for the receiver-end VSC is always set as $y^* \cdot P_{load}$, where y^* is the optimal DC power sharing.

The flow chart for the re-configuration strategy is shown in Fig.4.12. N is the total number of the link conductors and $n1$, $n2$ refer to the current configuration number and the configuration number after re-configuration respectively.

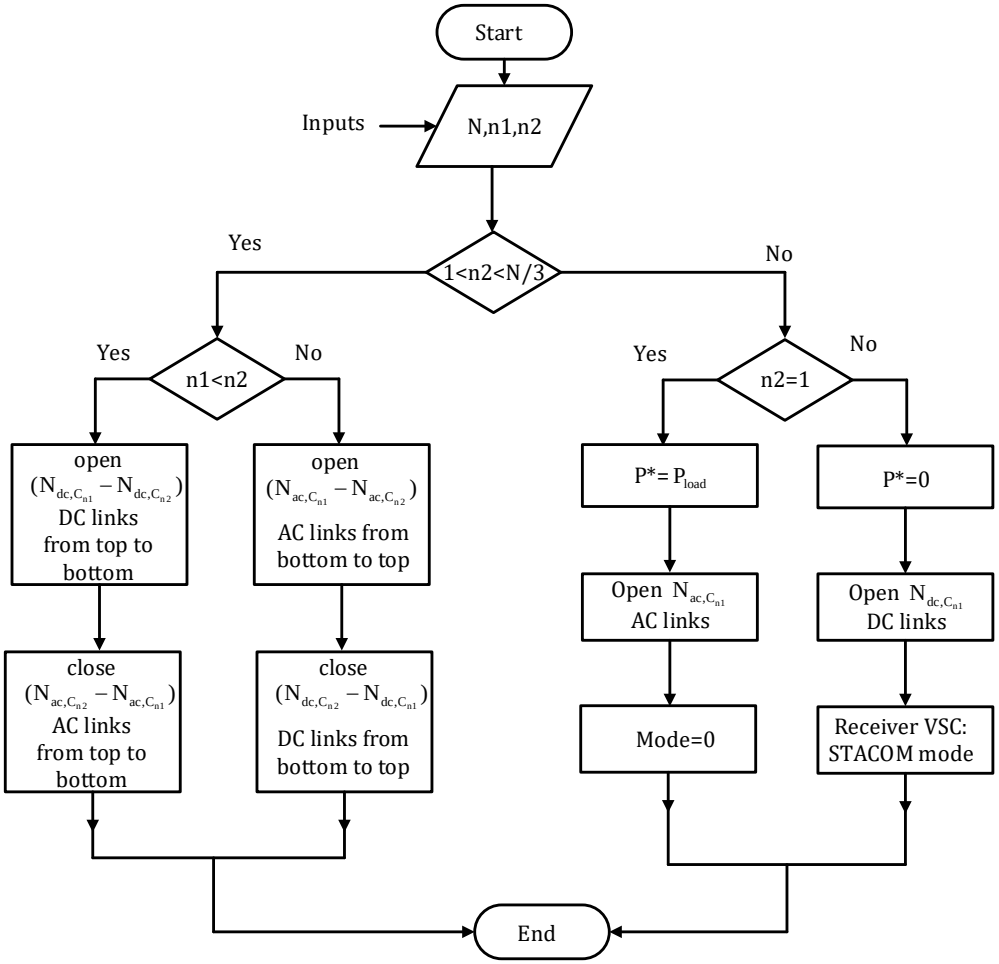


Figure 4.12: Flow chart for re-configuration strategy.

4.5 SIMULATION AND EXPERIMENTAL RESULTS

The experimental is tested in the mock-up of a 6 links parallel AC-DC system shown in Fig.4.13.

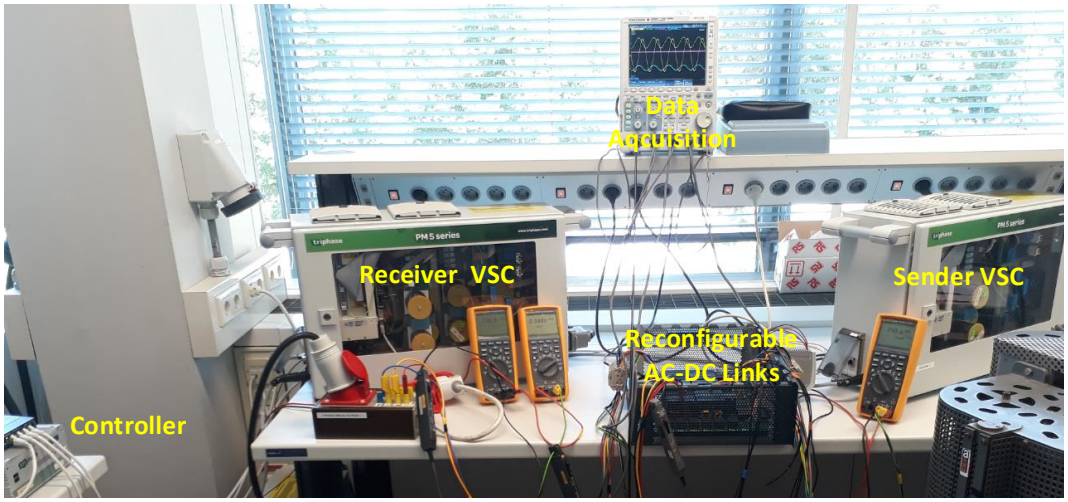


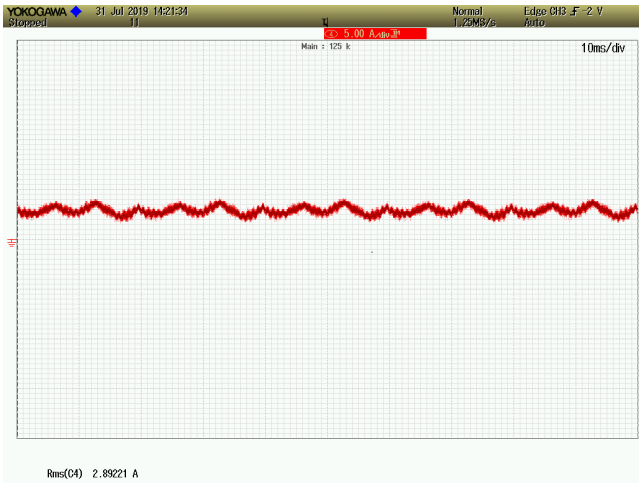
Figure 4.13: Lab-scaled parallel AC-DC links system.

4.5.1 ZSCC Control Test

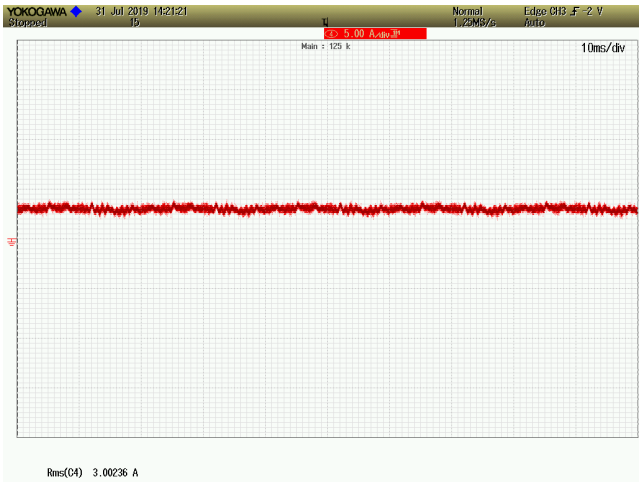
The grid-connected back-2-back system is tested in experimental setups. The two VSCs have identical circuit structure and parameters. The sender VSC regulates the DC-link voltage at 750 V and the receiver VSC delivers 2000 W to the PCC. The DC-link current is shown in Fig.4.14a and 4.14b. As it can be seen from the results, the ripple in the DC link current has significantly reduced and becomes flatter after the ZSCC controller is used. The effective value of the DC link current increased from 2.89 A to 3 A.

4.5.2 Grid-connected B2B Test

The operation condition remains the same in the ZSCC control test. The grid voltages and grid-side currents of the two VSCs are obtained experimentally before and after the implementation of both harmonics resonators and ZSCC controller, as shown in Fig.4.15. The power spectrum analysis shows that the THD of both currents deceases from 12% and 10.7% to 6% and 7.25% respectively. The distortion harmonics $5^{th} and 7^{th}$ harmonics are effectively mitigated under 1%. The waveforms are still distorted because the system is operating near to the marginal stability and the resonator gains can not be increased any further. The resonance frequency bands appear in the power spectrum of the currents and verifies the small stability margins of the system.

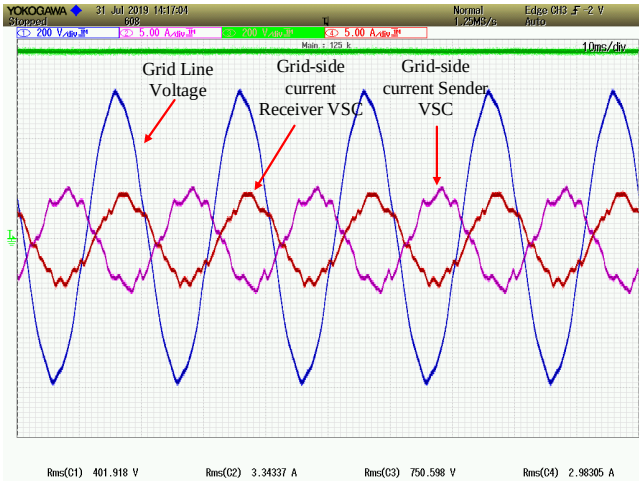


(a) DC link current at P^*=2000 W (no ZSCC controller).

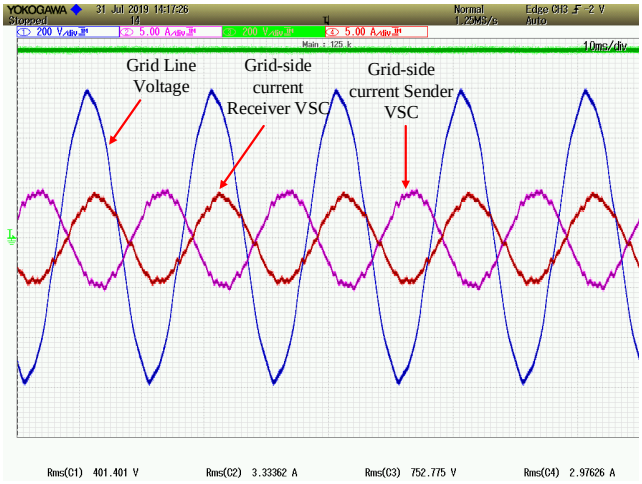


(b) DC link current at P^*=2000 W (with ZSCC controller).

Figure 4.14: Zero-sequence circulating current in grid-connected B2B system.



(a) Grid-side currents of grid-connected B2B system at P^*=2000W (no harmonics control).



(b) Grid-side currents of grid-connected B2B system at P^*=2000W (with harmonics control)

Figure 4.15: Grid-connected operation of the B2B system.

4.5.3 Standalone Mode Test in B2B System

The receiver VSC is connected to a balanced three phase resistive load (47Ω each phase). The DC-link voltage is still regulated at 750V. The generated PCC voltage is expected to be 220 V (phase effective value) with 50 Hz frequency. The sender VSC grid-side current, voltage and the receiver VSC output current and voltage obtained in the experimental test are shown in Fig.4.16 As shown in the results, the generated voltage and current have 50

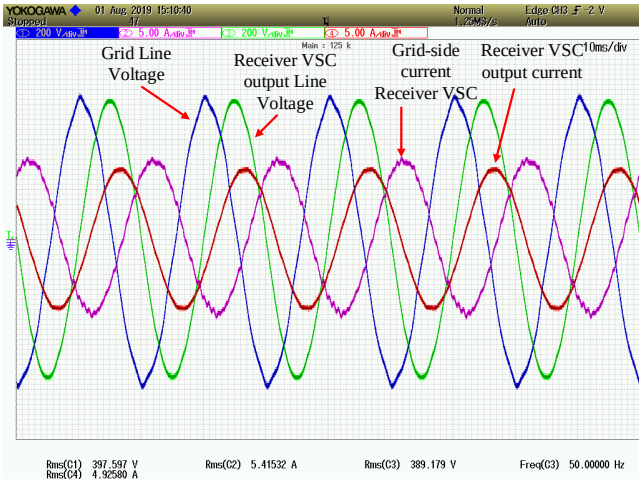


Figure 4.16: Standalone mode in B2B system.

Hz frequency with small error. The magnitude of the generated voltage is 389 V and it corresponds to an effective phase voltage of 224 V, which is slightly different from the reference value of 220V. This occurs because the generated voltage has a phase shift with the current, which means the reactive power is also flowing into the system. The reactive power generated in the capacitor still influences the voltage control, which means the decoupling part in the controller is not so effective. The power spectrum analysis shows that the generated voltage and current by the receiver VSC has very low THD (1.1% and 1.2% respectively). The grid-side current has better harmonics performance (3.5%), this is partly due to the increase of the fundamental current in this case (load power is 3000 W).

4.5.4 Verification of proposed re-configuration strategy in 9 Links System

In order to present adverse re-configurations, the parallel AC-DC re-configurable links system with 9 link conductors and one pair of VSCs is simulated in MATLAB/SIMULINK with the proposed re-configuration strategy explained in Fig.4.12. The switches are arranged according to Appendix.A, where Sac1, Sac2, Sac3 and Sdc1, Sdc2, Sdc3, Sdc4 are the three phase switches and the DC link switches respectively. The configurations are namely C1 (0 AC links, 8 DC links), C2 (3 AC links, 6 DC links), C3 (6 AC links, 2 DC links) and C4 (9 AC links, 0 DC links) and the AC links number increases with 3 accordingly.

Three different re-configuration cases are simulated: (1) C2 to C3 to C2; (2) C2 to C3 to C4; (3) C2 to C1 to C2. These three cases cover all the possible operation modes and

transitions of the converters and hence are chosen here. The operating parameters of the system is listed in Table 4.3.

Parameter	Value
V_g(phase)	230V(rms), 50Hz
Vdc^*	1000V
$P_{load}(P)$	5kW (V_{rms}=230V)
R_{link}	0.5Ω
y^*	0.8

Table 4.3: VSC circuit parameters.

Case 1: C2-C3-C2

The diagram for the re-configuration C2-C3-C2 is shown in Fig.4.17. The system initially operates in C2 with optimal power sharing and then is configured to C3 with zero power flowing in the DC links. Subsequently, the system controls the DC link power at optimal power sharing point. Contrarily, the system is configured from C3 to C2 with full load power delivery in the DC links firstly and then provides optimal DC power according to power reference command.

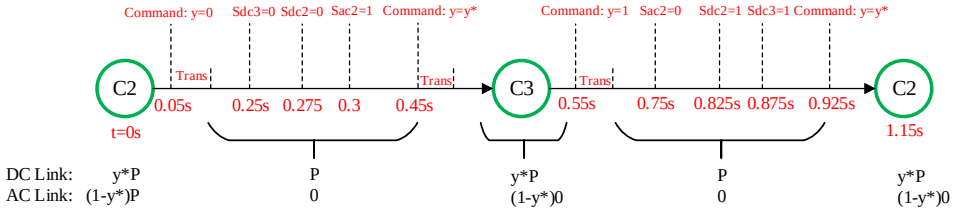


Figure 4.17: C2-C3-C2 diagram.

The DC link voltage, power flow in the AC and DC links, the power from the receiver VSC and the links current are shown in Fig.4.18, 4.19, 4.20 and 4.21 and the results are shown in p.u (per unit).

At t=0.05s, the power command is set at zero (previously at y^*) to reduce the DC link current to zero. At t=0.25s and t=0.275s, when the current in the DC links is nearly zero (Fig.4.20), Sdc3 and Sdc2 are opened. Three of the released link conductors from the DC feeder are then connected to the AC feeder when Sac is closed at t=0.3s. The system is configured to C3 and then the power controller of the receiver VSC acts at t=0.45s to deliver optimal DC power (y^*P), as indicated in Fig.4.19 and 4.18.

At t=0.55s, the command for full load power delivery by receiver VSC is initiated to provide near zero r.m.s current condition for the switches to be opened. At t=0.75s, when the AC links currents are nearly zero, as shown in Fig.4.20, Sac2 is opened and three link conductors are released. Then Sdc2 and Sdc3 are closed subsequently at t=0.825s and t=0.875s, after which the system is configured back to C2. The optimal power sharing command is then created at t=0.925s.

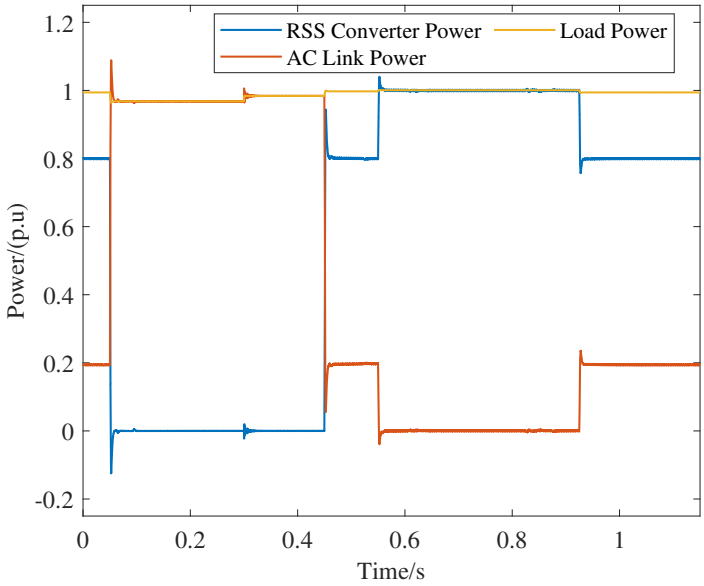


Figure 4.18: C2-C3-C2: receiver VSC and AC links powers.

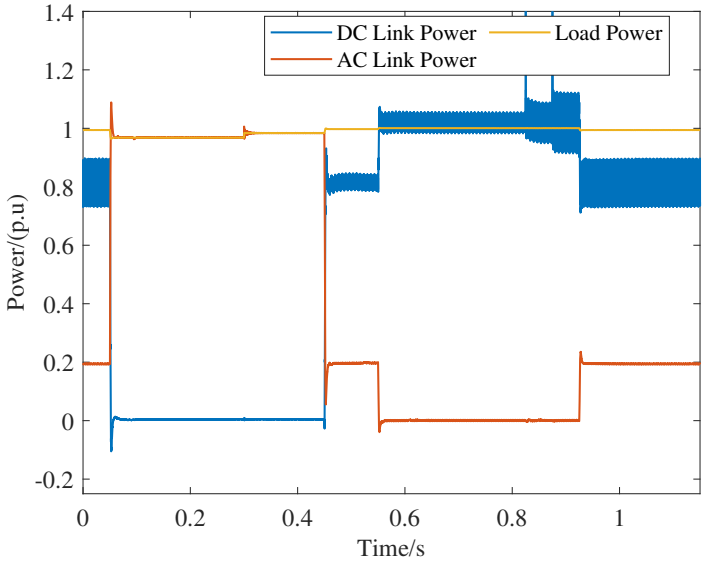


Figure 4.19: C2-C3-C2: AC and DC links powers.

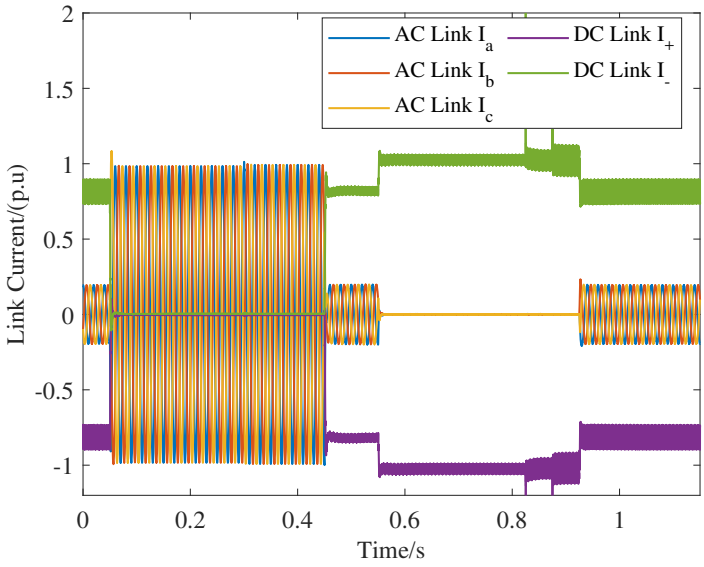


Figure 4.20: C2-C3-C2: AC and DC links currents.

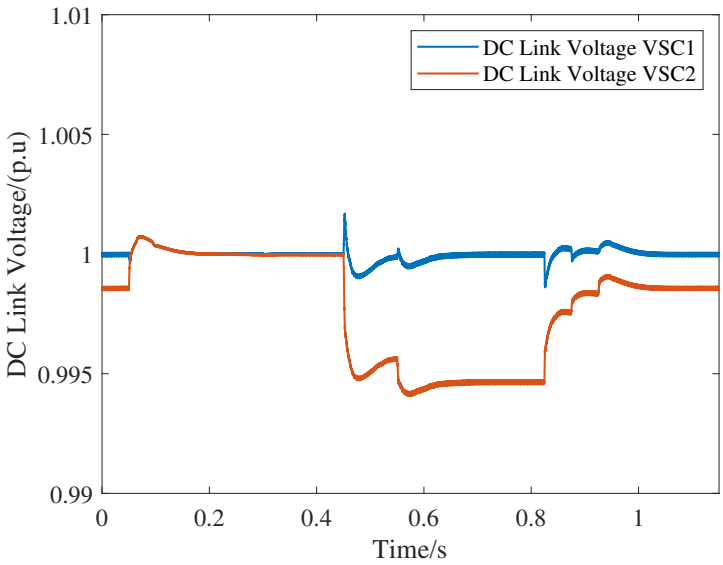


Figure 4.21: C2-C3-C2: DC link voltage of the sender and receiver VSCs (VSC1, VSC2).

In summary, the load power is always fed by either AC links or the receiver VSC before opening the switches. Hence, a near zero r.m.s current is provided for the switching transitions. The results show that the proposed control strategy is feasible to the re-configurations between different hybrid AC-DC systems.

Case 2: C2-C3-C4

The diagram for the re-configuration C2-C3-C4 is shown in Fig.4.22. The process of the system from C2 to C3 is exactly the same as that in case C2-C3-C2. After the system is configured to C3 with the optimal power sharing, the reference for active power in the receiver VSC is set to zero before opening the DC links.

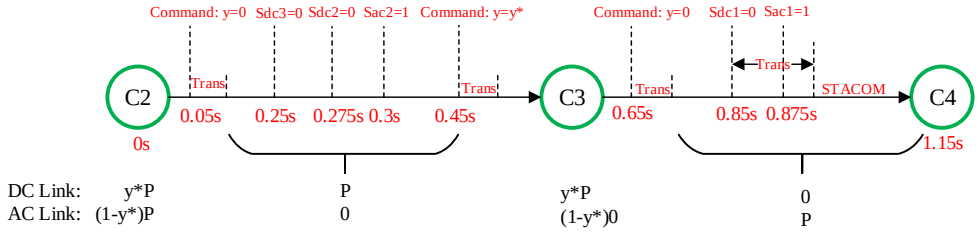


Figure 4.22: C2-C3-C4 diagram.

The simulation results are shown in Fig.4.23, 4.24, 4.25 and 4.26 in terms of the the DC link voltage, the power flow in the links and the power delivered by the receiver VSC.

Before t=0.65s, the reconfiguration from C2 to C3 has the same results which are discussed in C2-C3-C2 case. At t=0.65s, the power reference for receiver VSC is set to zero to create the nearly zero current condition for the DC links. At t=0.85s, Sdc1 is opened when the DC links have the near zero r.m.s currents, which can be observed in Fig.4.25.

The results verify that the parallel AC-DC system can also re-configure into full AC links operation while having a near zero r.m.s current in the DC links to be opened.

Case 3: C2-C1-C2

The diagram for the re-configuration C2-C1-C2 is shown in Fig.4.27. The system firstly controls the DC link to provide full load power and creates a near zero r.m.s current in the AC links. After the switches in the AC links are opened under zero current, the receiver VSC changes its mode from grid-connected inverting mode (power control) to standalone mode with 6 DC links. After the remaining two link conductors are inserted to the DC feeder, the system is finally configured to C1. The re-configuration from C1 to C2 experiences a reverse process. However, the DC link switches e.g. Sdc4 has to be opened at a current with certain value because the current in all DC links is controlled by only one pair of VSCs. After the AC links are inserted, the control mode of receiver VSC changes back to inverting mode with power control. Finally, the system is configured back to C2 with the optimal power sharing.

The simulation results are shown in Fig.4.28, 4.24, 4.25 and 4.26 in terms of the DC link voltage and the power flow in the links and receiver VSC.

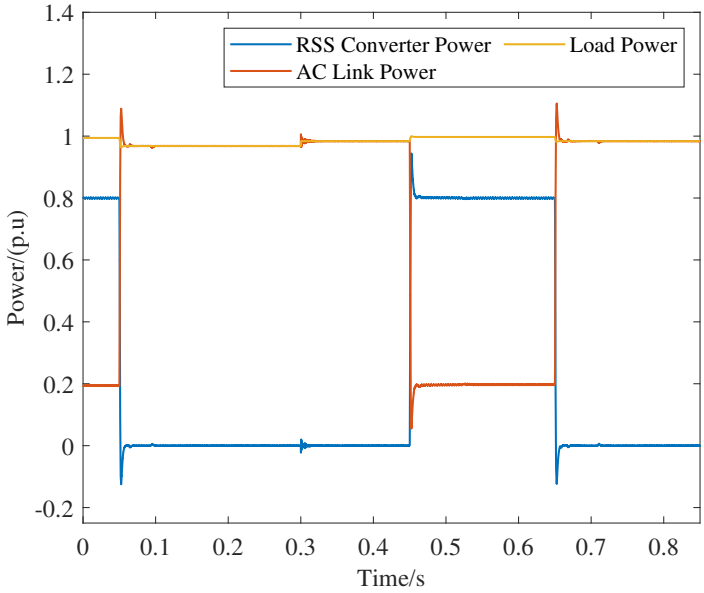


Figure 4.23: C2-C3-C4: receiver VSC power and AC links power.

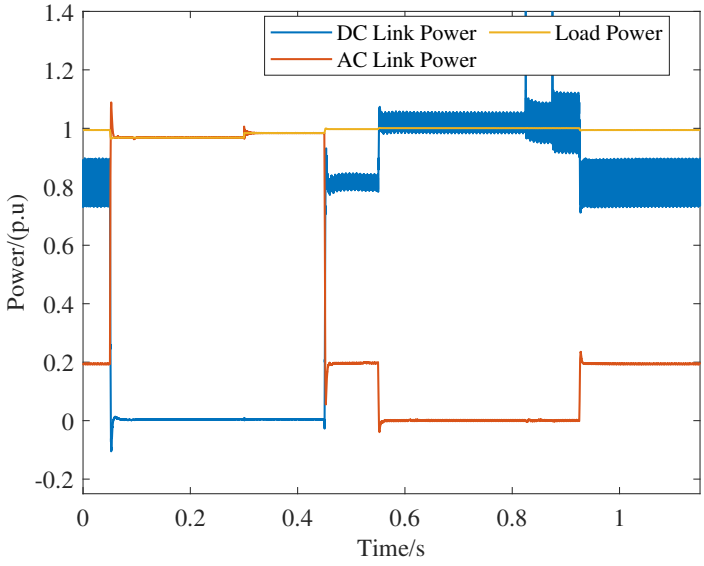


Figure 4.24: C2-C3-C4: AC and DC links power.

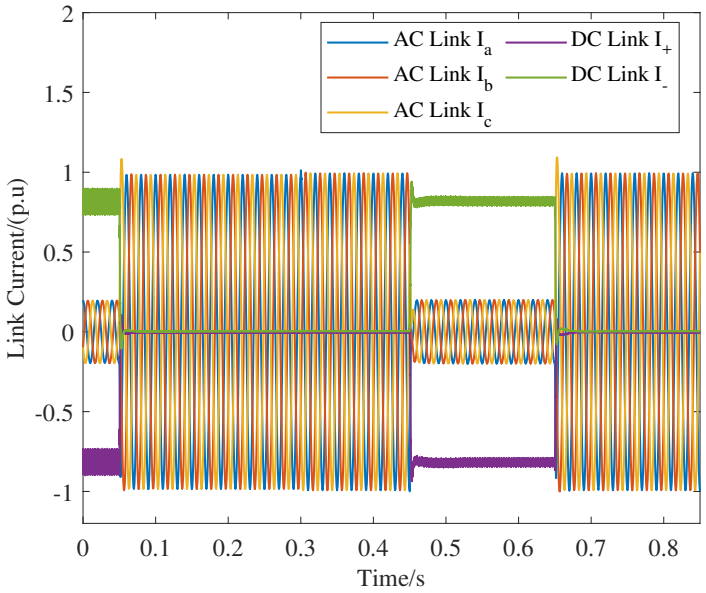


Figure 4.25: C2-C3-C4: AC and DC links current.

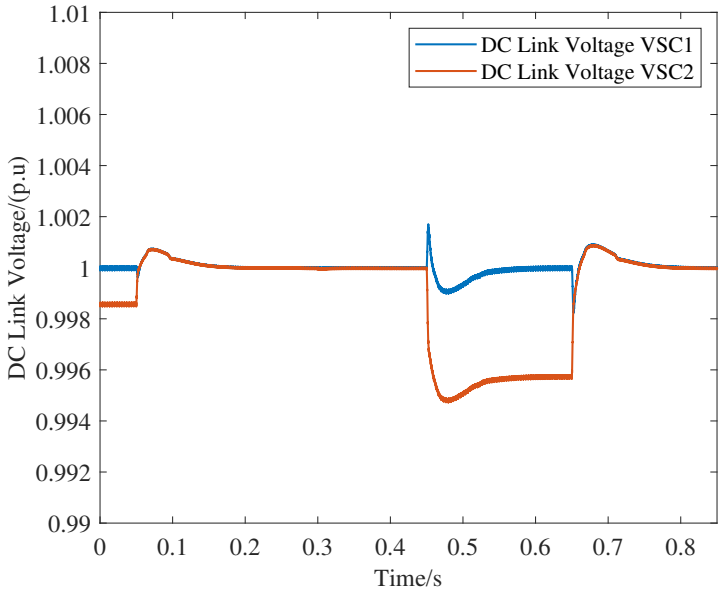


Figure 4.26: C2-C3-C4: DC link voltage of the sender and receiver VSC (VSC1, VSC2).

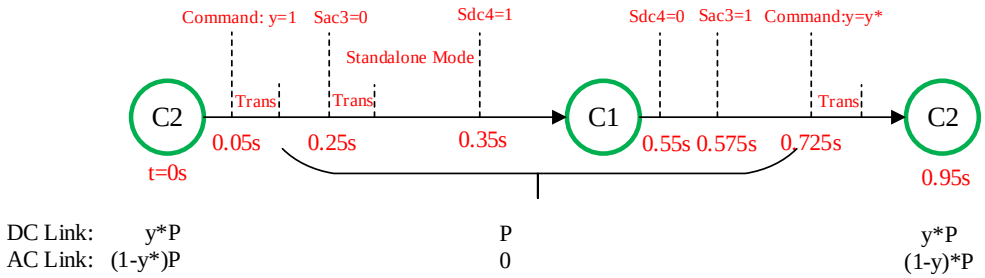


Figure 4.27: C2-C1-C2 diagram.

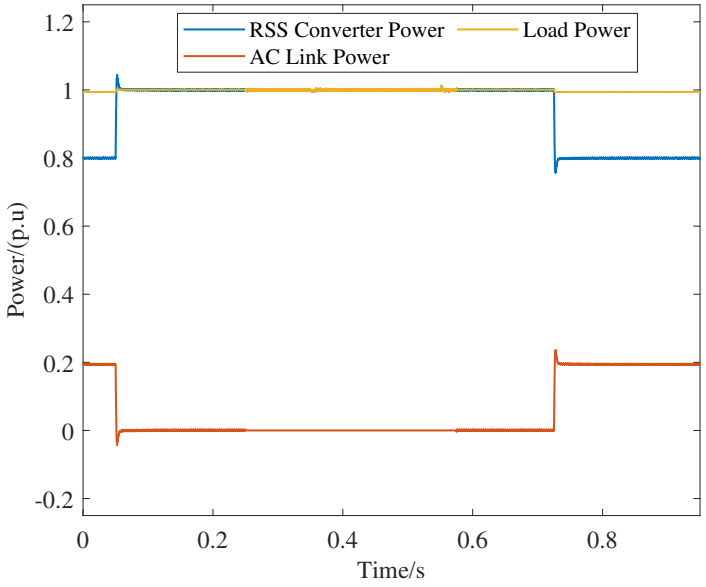


Figure 4.28: C2-C1-C2: receiver VSC power and AC links power.

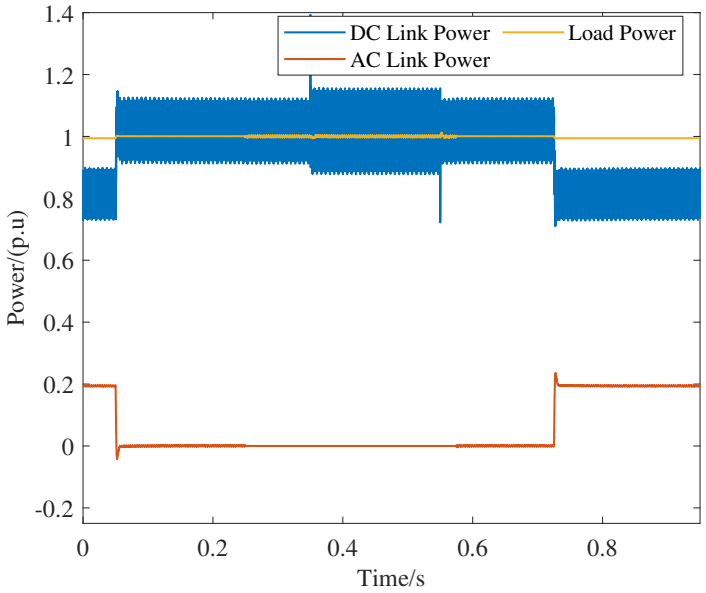


Figure 4.29: C2-C1-C2: AC and DC links power.

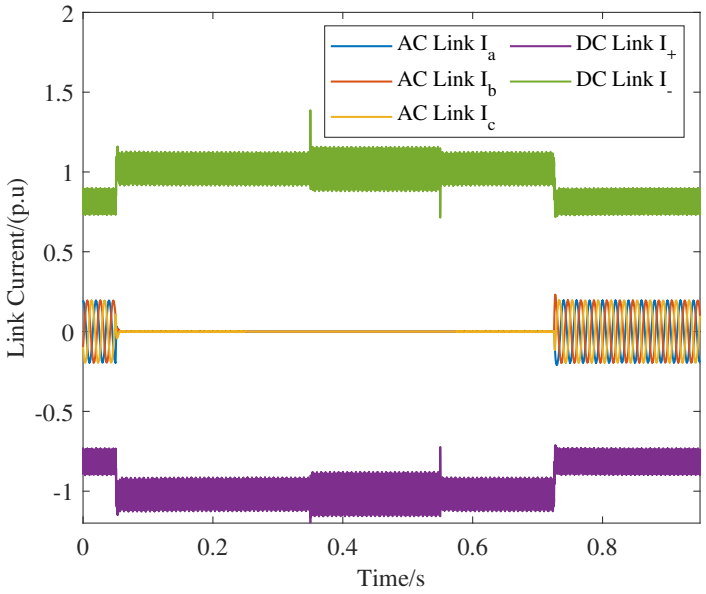


Figure 4.30: C2-C1-C2: AC and DC links current.

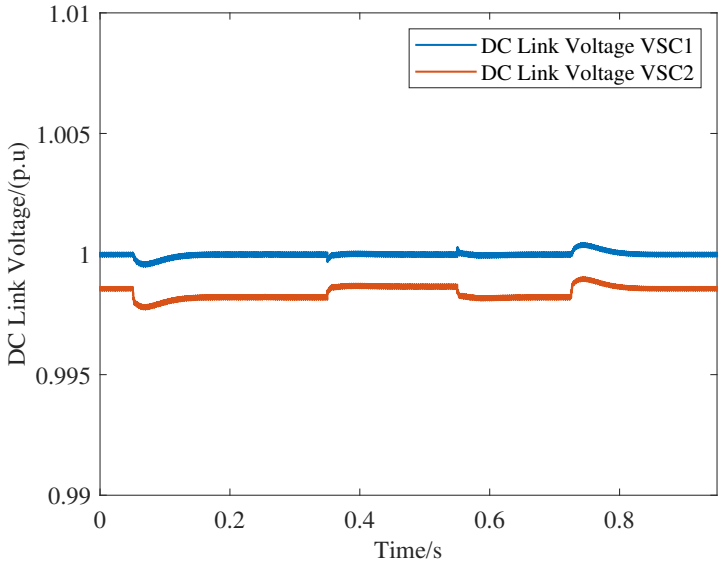


Figure 4.31: C2-C1-C2: DC link voltage of the sender and receiver VSC (VSC1, VSC2).

The system is initially in C2 with optimal power sharing, which can be seen from Fig.4.28 and 4.29. At t=0.05s, the receiver VSC power is increased to full load power and thus the currents in the AC links starts decreasing until zero. At t=0.25s, Sac3 is opened with a near zero r.m.s switching current and the receiver VSC changes to standalone mode with 6 DC links. At t=0.35s, when the system is in steady state, another two remaining link conductors are inserted to DC feeder and the system is configured into C1.

Sdc4 is opened at t=0.55 with a non-zero current. At t=0.575s, the released link conductors are connected to the AC feeder, which initiates a grid-connected mode command to the receiver VSC. Still, the DC links are providing full power to the load. At t=0.725s, the optimal power sharing command is generated and the system operates in C2 with the optimal power sharing between the AC and DC links.

To summarize, the system is re-configured to the full DC links operation with a near zero r.m.s switching current in the switches. In addition, the seamless transition between the grid-connected and standalone modes is realized. The DC link switches have to be opened under full power to re-configure back to C2 since there are no extra link conductors available for the AC connection.

5 CONCLUSION AND FUTURE WORK

5.1 CONCLUSION

In this thesis, the basic vector control of the grid-connected VSC system is investigated in Chapter.2. Harmonics rejection performance of the SRF-PLL with the notch filter is researched based on frequency-response method. Both the simulation and experimental results show that the SRF-PLL with the notch filter can effectively mitigate the influence of low order harmonics from the grid. Under distorted grid voltage with 5^{th} (1.88%) and 7^{th} (0.45%), the ripple in the output frequency of the PLL is reduced to below 0.1 Hz, which has negligible influences on the harmonics performance of the grid side current.

Chapter.3 investigates the design considerations of the notch filter and the harmonics resonators based on the trade-off between the control stability of the VSC system and its current harmonics rejection capability. The controller gain is chosen to provide enough stability margin while having sufficient control gain at the low order harmonic frequencies. The simulation results of the notch filter shows that the system changes from a marginally stable to a stable operation after the notch filter is used, which verifies the improvement of stability with this active damping technique. In simulations with a distorted grid voltage, the 5^{th} and 7^{th} harmonics in the grid-side current reduces from 3% and 14.7% to 0.54% and 1.2%, respectively, which proves the high rejection capability of the designed harmonics resonators at the low order frequencies. The experimental results show that the designed controller can realize a stable operation and while achieving a good sinusoidal grid side currents (THD = 1.43%). In the experimental test of the designed controller on the practical VSC system connected with a distorted grid voltage, a significant reduction of amplitudes of the 5^{th} and 7^{th} current harmonics frequencies is achieved, i.e. from 15.7% and 6.7% (initial) to 2% and 1.9% (final), respectively.

Chapter.4 proposes a control strategy for online re-configurations of the parallel AC-DC system with near zero r.m.s switching current. The control methods including the ZSCC control and standalone mode are researched. The PI controller with anti-windup is employed in the control loop. The experimental result shows that the ripple in the DC link current is significantly reduced and the effective value is increased from 2.89 A to 3 A, in the B2B system delivering 2000 W to the load. The standalone mode control is developed based on the current controller used in the grid-connected mode. The designed controller for standalone mode is verified by the experimental test, where the standalone VSC is delivering 3000 W to the load. The frequency of the generated voltage is well regulated at 50 Hz and its amplitude has a small error (4 V) compared with the reference value. The control strategy for online re-configurations was validated by the simulation results of a 9 links parallel AC-DC system. The results showed that the online re-configuration can be successfully realized with the proposed control strategy and the designed controllers for the VSCs.

5.2 RESEARCH QUESTIONS

1. What is the control method and associated gains necessary to achieve sinusoidal currents with low harmonic distortion under distorted grid voltages?

   The GCC control scheme is adopted in this thesis for the control of the current under distorted grid. The benefit of the GCC control for mitigating the low order harmonics is explained by Fig.3.6.

2. How to simultaneously improve the stability and output current performance of the VSC under distorted grid voltage?

   The current control structure shown in Fig.3.43 combines the notch filter and harmonics resonator with lead filter to simultaneously mitigate the harmonics in the grid side current while achieving the stability. The simulation results presented in Fig.3.44 and 3.45 show that the grid side current with low THD is obtained under the distorted grid with the low order harmonics.

3. What are the design parameters of the notch filter for improving the stability range of the VSC?

   The resonance band Δ is selected as 0.1 times the resonance frequency of the LCL filter and a_Δ is chosen as the $1a_{peak}$. For the practical VSC system used in this system, $a_\Delta = 0.1$ is selected for the notch filter. The effectiveness of the designed notch filter is verified by the simulation result shown in Fig.3.30.

4. What are the harmonics resonator parameters for increasing the low order harmonics rejection capability of the VSC?

   The resonator gain is selected as 200 while a 90°phase is provided by the lead filter. The lead filter provides the phase increases at 6^{th} fundamental frequency. The results in Fig.3.44, 3.45 and 3.48 show that the selected parameters of the harmonics resonator can significantly mitigate the 5^{th} and 7^{th} harmonics.

5. What are the control strategy for the seamless mode transitions?

   The control strategy for the seamless mode transitions is proposed in Fig.4.11. The synchronization between the switch and VSC control signals is realized in the simulation. The simulation results (Fig.4.28, 4.24, 4.25 and 4.26) of the re-configurations in the 9 links parallel AC-DC system show that the feasibility of the control strategy.

6. How to ensure a near zero r.m.s switching current during online re-configurations?

   The PI based ZSCC controller described in Fig.4.6 is implemented in the current controller to reduce the ZSCC, the existence of which is shown in Fig.4.14a. The experimental result in 4.14b shows that the ZSCC is effectively suppressed. Besides, the control algorithm illustrated in the flow chart (Fig.4.12.) is employed alongside the ZSCC controller in the simulation tests of the parallel AC-DC system. The simu-

lation results in the Subsection.4.5.4 show that the near zero r.m.s switching current is realized in the online re-configurations.

5.3 FUTURE WORK

Generally, many aspects in this thesis, from the control methods to the hardware can be improved further.

5.3.1 Improvement of the control for the VSC system

- The SRF-PLL is proved to be unable to mitigate the influence of grid voltage distortion well with an adequate bandwidth. Synchronization algorithm based on a Dual Second Order Generalized Integrator PLL (DSOGI-PLL) can be used for further improvement since it is verified to have better harmonics rejection capability than SRF-PLL.
- The notch filter designed in this thesis does not have enough damping performance against parameters variation in the VSC system. The adaptive notch filter detects the current information and estimate the resonance frequency based on specific algorithm. The notch filter parameters can vary according to the variation of the resonance frequency. The digital adaptive notch filter can be adopted to realize stability improvement in the practical VSC system.
- In this thesis, only one pair of converters is adopted. This limits the control strategy of near zero r.m.s switching current in the re-configuration from full DC links operation to others. Therefore, each pair of DC links can be assigned with an individual pair of converters.

5.3.2 Experimental validation of the control strategy for re-configurations

- The synchronization between the independent communication systems in the parallel AC-DC system can be solved by either using the detection of grid voltage or building a new communication system for the power electronics and the mechanical switches.
- MMC can be adopted in both the VSCs of the B2B system because of its superior harmonics performance.

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A APPENDIX

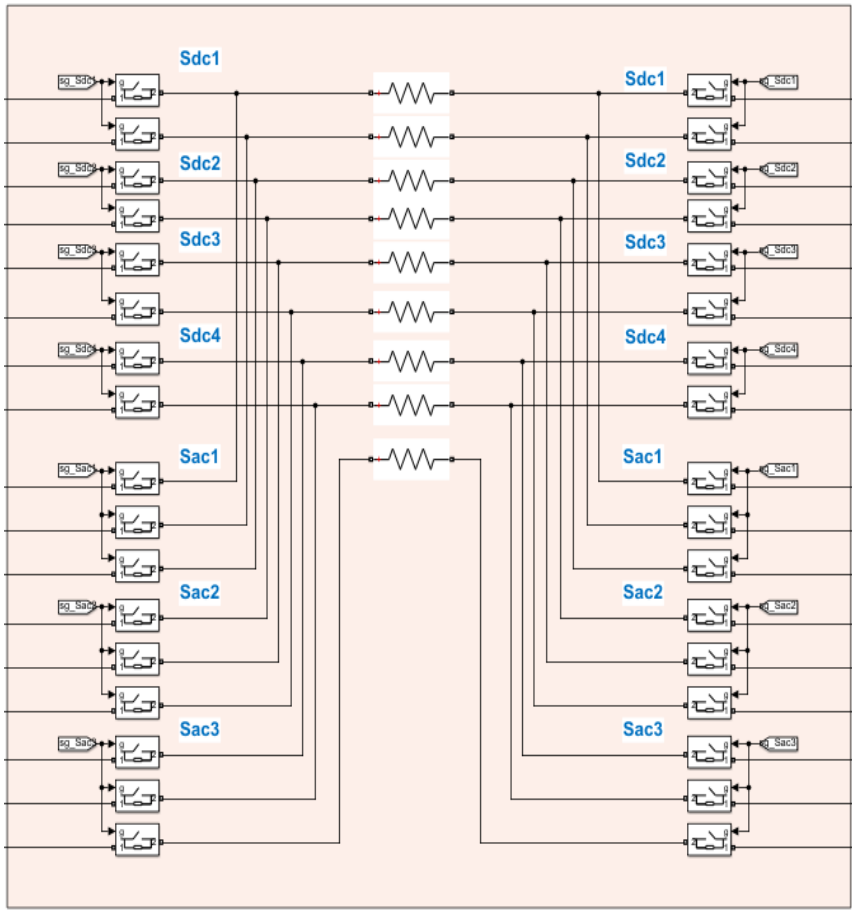

Figure A.1: Switches arrangement for 9 links simulation case