A versatile output stage for implantable neural stimulators

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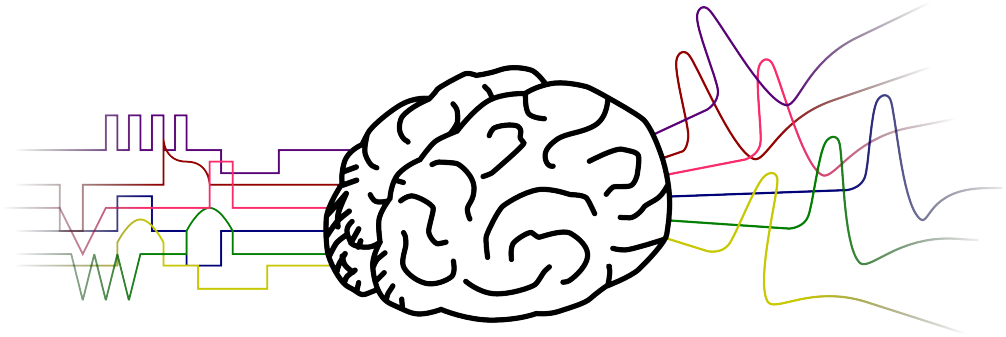

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Challenge the future

Wovon man nicht sprechen kann, darüber muß man schweigen ∼ Ludwig Wittgenstein

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by

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Abstract

Neural stimulators have the potential of becoming very important devices for the treatment of a wide variety of diseases. One of the major problems with existing stimulators is the limited waveform adjustability. This precludes the use of sophisticated stimulation programs and thereby affects the efficacy of the therapy applied. Another issue is the limitted implantability of the device, resulting in long subcutaneous wires. Because of these two reasons a new type of stimulator is required.

Electrodes implanted in neural tissue are modeled using a highly non linear model with a capacitive nature. It is however shown that the response of the electrode tissue interface can be modeled accurately enough using a linear capacitive model.

The physical process associated with the stimulation of neural tissue essentially comprises lifting up the tissue potential above (or below) a certain threshold value. This means that stimulation essentially is the injection of a particular amount of *charge* into the tissue in order to lift the potential of the tissue. Furthermore the injected charge needs to be canceled precisely in order to prevent tissue damage.

First a system level design of a complete stimulator system is presented. This design includes the possibility of feedback: based on the brain activity recorded by electrodes a certain stimulation pattern is applied. After the system definition the design of the output stage, responsible for injecting the stimulation pattern into the tissue, is treated.

Most existing stimulators use a current based architecture in which the charge is controlled by enabling the stimulator for a certain amount of time. Voltage based stimulation however is shown to have a higher power efficiency. A novel type of voltage based architecture is proposed using indirect current feedback of the tissue current. Using a current integrator with a very high dynamic range the injected charge can be controlled very precisely, while any arbitrary voltage waveform can be used for stimulation.

Circuit simulations prove the feasibility of the approach and show a charge mismatch in the order of 0.1% is possible, paving the way to full charge balancing. Furthermore, they predict correct functionality over all process corners, including mismatch. The system only uses a single-ended supply and the quiescent power consumption of the system is less than 17 μW.

Therefore it can be concluded that the novel approach for the output stage design proposed in this thesis allows the use of a very versatile stimulator; any arbritrary waveform can be injected while assuring charge balancing. Furthermore power consumption is minimized in order to relax the requirements for the battery and thus improve the implantability of the system.

Acknowledgements

This report is the result of spending many hours at my desk in the Electronics Research Department. The fact you are reading this report now proofs that I somehow managed to put something together from many Cadence simulations, Matlab scripts and scientific papers. Without any doubt it would however been impossible to come to this point without the help of many people.

First of all I want to thank my supervisor Wouter Serdijn. I greatly appreciate all his efforts to guide me through the process of the Master thesis. I greatly admire how much time he has always taken for the many fruitful discussions we have had. I also thank him for the trust he has given me to start this project in a rather unexplored area within our group.

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Finally I want to thank my family, especially my parents and sister for their love and support. I am very thankfully for the confidence they have put in me. I also look back with great gratitude to the support and interest my granddad has shown during my studies. It pains my heart severely that he is not able to witness this completion, but I am sure he would have loved it.

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Contents

Introduction

Throughout history medicine has been going through an extensive development. Prehistoric medicine consisted of a combination of very basic drugs (extracted from plants and herbs) and treatments consisting of ceremonies carried out by shamans using supernatural powers and objects (charms, spells, amulets, etc). Gradually during history more and more knowledge was gained about the use of drugs for treating diseases. From the 19th century on medicine has gone through a revolution due to advances in for example chemistry and today drugs form utterly important ingredient of medical treatments.

However it is more and more realized that drugs only cannot cure all diseases efficient enough. Most drugs suffer from unwanted side effects and the spatial selectivity of drugs is usually low: it will have effects on the whole body, while usually a disease is limited to only certain parts. Another form of treatment consists of electromagnetic stimulation of the body. Cells use electromagnetic signals to operate. These signals can be affected by artificially generated electromagnetic signals in order to establish a certain desired effect.

Probably the most well known form of stimulation is the pacemaker: a stimulator for the heart muscle. This particular technique has gone through an extensive development as well. As early as 1820 Richard Reece described in his 'Medical Guide' a method of stimulating the heart. A metal rod was inserted in the esophagus and connected to a voltaic cell, while another rod was pushed to the chest by the physician. In this way a 'manual' pacemaker was comprised. Nowadays pacemakers are very sophisticated implantable stimulators: they record heart activity and based on this activity the device can decide when and how the heart needs to be stimulated.

The brain essentially works in a similar manner as the heart muscle: neural cells communicate by 'activating' each other using electrical impulses. This means that the activity of the brain can be affected by means of electrical stimulation as well. Since many, many diseases find their origin in abnormal brain functionality it is in principle possible to eliminate this unwanted activity by using brain stimulation. Well known examples include the suppression of the effects of Parkinson's disease [39] or tinnitus [61]. Both examples use implanted electrodes connected to a stimulator, which can deliver stimulation pulses to the tissue. It is shown that these treatments can obtain better results then any type of drugs currently available.

Besides these well known examples the potential applications for neural stimulators are almost endless. In principle any symptom that originates from abnormal behavior in the brain can be treated using brain stimulation. Although in most cases additional knowledge is required about the location and nature of the abnormality, brain stimulation might open up a huge field of new treatment methods.

The development of neural stimulators however is in some way comparable to the first pacemaker from 1820. Most currently available stimulators have limited implantability and do not incorporate any feedback: they simply stimulate the neural tissue using a fixed stimulation pattern, without recording the activity in order to know if stimulation is required.

In addition current stimulators only offer a limited number of stimulation waveforms. Usually only block shaped current based pulses can be injected. From a clinical point of view the application of other types of waveform might yield more efficient ways to treat patients. Furthermore neural tissue tends to have a large adaptability. This means that due to the fixed stimulation pattern the tissue will gradually habituate to the stimulation pattern, which means the symptoms of the disease return.

Therefore there is a need for more sophisticated brain stimulators. In this project the design of such a stimulator is treated. The focus of the design is put on the following aspects:

- The design needs to be *implantable* in the head in order to minimize the burden for the body. It is evident that at this location there is very limited space available. This means that not only chip area is a limiting factor, but also the battery size is limited. This means that the circuit should have an extremely low power consumption. The available space is about comparable to a pair of stacked 2 euro coins.

- The design needs to be *safe*. When applied in the correct way, stimulation can lead to beneficial results in the brain. However, stimulation can also lead to damage to the tissue when certain requirements of the stimulation waveform are not met. Therefore safety is considered to be very important to prevent damage to the tissue.

- The design should be *versatile*. With the versatility of the system actually two aspects are meant. First of all there should be a very high flexibility in waveforms and stimulation patterns in order to prevent tissue habituation, since tissue habituation is one of the biggest problems in the application of current stimulators. Furthermore feedback might be included in the system. This means that the system should also be able to record neural activity and based on this apply a certain stimulation pattern.

In the following chapters the design of this stimulator system is treated. Chapter one gives an extensive introduction in the physical principles underlying the working of neural cells. This includes the electromagnetic behavior of neural cells, but also safety aspects related with stimulation of cells. This knowledge is required in order to design a stimulator which actually conforms to these physical principles.

In Chapter two the design of the complete stimulator system is treated. Possible system architectures are presented and compared. Subsequently we zoom in on the design of one of those blocks in the third chapter: the output stage. This block is responsible for generating the stimulation pulses which are injected into the tissue. For the design of this block the medical principles explained in the first chapter are used extensively. At the end of the third chapter a system description of the output stage is obtained.

The fourth chapter subsequently deals with the circuit implementation of the output stage block. For each part of the block several circuit solutions are discussed and compared. The optimal solution is chosen and a complete system is designed. In Chapter five the output stage is simulated to check the correct functionality and to evaluate the performance of the circuit. The report subsequently ends with the conclusions and recommendations for further research.

Chapter 1

Neural cells and their electrical behavior

The purpose of a brain stimulator is to interact with neural tissue in order to accomplish some desired activity in the brain. The interaction between the stimulator and the neural tissue is chosen to take place in the electrical (energy) domain. When designing a stimulator it is therefore of great importance to have a thorough understanding of how neural tissue works and more even important: how it responds to electrical impulses.

In this chapter the working principle of neural cells is outlined with an emphasize on the electrical behavior. First the basic working principle of neural cells is explained. This principle is used to explain the consequences of applying stimulation impulses to the tissue. Subsequently an electrical model is given for the electrode-tissue interface, which can be used when designing the output stage of the stimulator. Finally the consequences of stimulation in terms of safety constraints are investigated.

1.1 Working principle of nerve cells

In this section the basic working principle of nerve cells is explained. First an overview is given of the structure of nerve cells. Subsequently the activation mechanism of a cell is outlined, first in a qualitative way and after that in a quantitative way.

Most of the material presented here can be considered as basic cell theory and can be found in many textbooks. The material presented here and the notation of the equations is based on [48].

1.1.1 Structure of nerve cells

In Figure 1.1 the structure of a nerve cell is depicted. Nerve cells are often reffered to as neurons and they are composed of the following parts:

- The *cell body*, also called the *soma*. It is similar in structure to all other kinds of cells, including a nucleus and DNA. The cell body can be seen as the central unit of the neural cell: it processes the incoming neural signals and initiates any output behavior.
- Numerous short extensions, called *dendrites*. These tentacle shaped extensions can be seen as the inputs of the cell. The dendrites transfer the impulses from the incoming nerve fibers toward the cell body. The input impulses can result in excitatory as well as inhibitory impulses. Neural cells can have many inputs (up to hundreds of thousands connected neurons) per soma.
- A single long nerve fiber, called an *axon*. This can be seen as the output of the cell. The output signal is transferred from the cell body through the axon towards other cells or

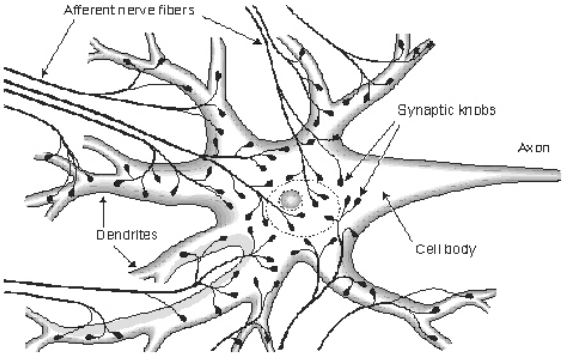


Figure 1.1: Structure of a neural cell (from [48])

muscles. The connection between the far most end of the axon with the next cell or muscle is called a *synapse* and by means of a chemical reaction this connection is a unidirectional, so only output signals travel through the axon.
An *Myelinated* axon is surrounded by myelin sheath, which forms an insulating layer. This layer is discontinuous and the points where it is absent are called *Nodes of Ranvier*.

Each cell is enclosed by a membrane, which separates the inside of the cell with the outside. The membrane consists of two layers of chemical structures called phosphoglycerides: special kind of acids with a hydrophilic head and hydrophobic tail. Their structure is depicted in Figure 1.2. The thickness of the membrane is generally smaller than 10 nm.

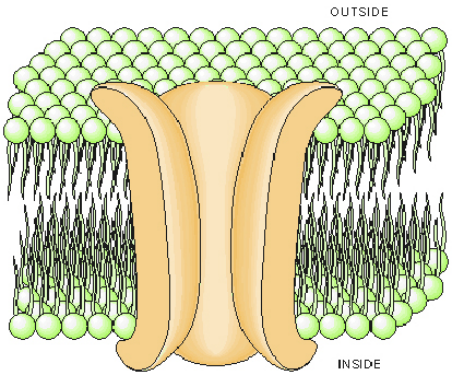


Figure 1.2: Structure of the cell membrane (from [48])

Nerve cells interact with each other by means of impulse signals. These signals are observed as changes in the membrane voltage. The transmembrane voltage V_m is defined as the potential difference between the inside and outside of the cell:

$$V_m = \Phi_i - \Phi_o \tag{1.1}$$

When the membrane voltage is raised up to a certain threshold voltage, the membrane is 'activated' and a process is triggered to generate a membrane voltage impulse. This impulse signal can travel through an axon towards other cells. The membrane voltage impuls is the fundamental proces underlying the working principle of neural cells and networks. In order to understand this process a model for the membrane is to be developed in the next sections. The next step is then to artificially modify the activation process by means of brain stimulation.

1.1.2 Basic membrane model

In this section a basic model in the electrical domain for the cell membrane is developed. A closer look at Figure 1.2 shows that within the membrane there are ionic channels through which ions can flow from the outside to the inside of the cell and vice versa. In equilibrium, at the inside of the cell, a surplus of Na^+-ions (sodium) is present, while at the outside a surplus of K^+-ions (potassium) is present.

This concentration gradient would normally lead to sodium and potassium ion fluxes. However due to the membrane potential difference and a limited ion channel conductivity, a concentration gradient is maintained. This equillibrium condition is much like the equillibrium in a semiconductor *pn*-junction: due to a large concentration gradient, electrodes and holes will diffuse, but this process is limited due to the built-in potential and a limited conductivity. A typical transmembrane voltage at equilibrium (rest) of a nerve cell is $-80\,\mathrm{mV}$.

When the membrane voltage is increased to about $-50\,\mathrm{mV}$ (by depolarization), the conductivity of the membrane for sodium ions increases very rapidly. Simultaneously the potassium ion permeability starts to increase as well, but the process is much slower. This means the sodium ions start to flow from the outside to the inside first, making the inside more positive. When the membrane voltage is increased up to about $20\,\mathrm{mV}$ the potassium conductivity is increased as well and potassium ions begin to flow from the inside to the outside, decreasing the membrane voltage. Finally, the membrane will have reached its equillibrium voltage again. The ion conductivities (both depending on the membrane voltage) have also reached their equillibrium again.

This process described qualitatively what happens during an activation pulse. The stimulation pulse (the membrane voltage) always has the same shape, which is depicted in Figure 1.3. The duration is about $1\,\mathrm{ms}$ and the change in voltage about $100\,\mathrm{mV}$.

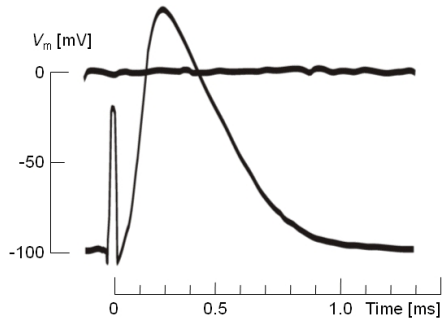


Figure 1.3: Activation pulse of a neural cell (from [48])

The process described above could not be repeated endlessly if there was no mechanism involved that maintains the concentrations gradients. Ions flowing through the membrane should be somehow transported back. For this purpose each cell has a built-in Na-K pump, which continuously restores the sodium and potassium ion concentrations at the inside and the outside. The energy required for this pump comes from the cell's metabolism (chemical reactions occuring in living organisms in order to maintain live).

A first step in modelling the cell membrane in the electrical domain is given in Figure 1.4. As can be seen this model comprises three components, which are explained shortly here:

- *Capacitor* C_m
  Since the membrane is a poor electrical conductor and a very good dielectric, the membrance behaves as a capacitor. A typical value for C_m is $1\,\mu\mathrm{F/cm^2}$.

- *Conductor* G_m
  This conductor respresents the ion channel in the membrane. When ions flow through the channel, the membrane voltage is affected. The conductivity of the ion channel depends heavily on the membrane voltage.

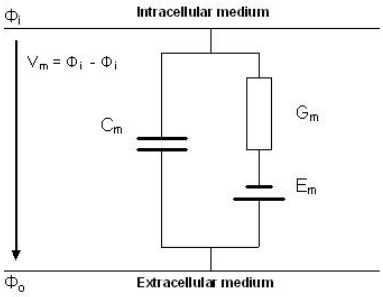


Figure 1.4: Basic electrical model for the cell membrane (from [48])

- *Voltage source E_m*
  This voltage source represents the built-in potential of the membrane for ions. The value of this source is equal to the equillibrium voltage of the membrane. If the membrane voltage is at equillibrium as well, the voltage over G_m is zero and the net ion flux is zero, corresponding to the equillibrium condition.

Using this model it is possible to explain the basic operation of the membrane. However, the voltage dependent relation for the conductance is yet to be found. Furthermore the value for the built-in potential also needs to be found. To overcome these problems a more elaborate membrane model needs to be developed.

1.1.3 Advanced membrane model

In this section, the basic membrane model is improved towards a more advanced model in order to be able to explain the membrane properties more qualitatively. The model is shown in Figure 1.5. The most important improvement is made by realizing that the total ion flux is composed of the movement of ions of different types. Three channels are to be distinguished.

The first two channels are for the sodium and potassium ion flux. Both have their own channel conductance, which depends on the membrane voltage. As will be seen in section 1.1.3 the dependencies are ion specific. Furthermore they also have their own built-in potentials. These potentials are called the Nernst potentials and are also ion type specific (see section 1.1.3).

The third channel is to represent the remaining ion types, mainly Cl^- ions. In most cells, the internal concentration of chloride is very small. Therefore a very small chloride flux will already bring the system in equillibrium. For this reason the contribution to the total flux is small and is therefore approximated with a constant channel conductance.

The model from Figure 1.5 is extensive enough to quantitatively describe the cell properties. In literature many more extensive models exists, but they are not treated here. In the remaining of this section the values for the Nernst potential and the channel conductance are found.

Nernst Potential

As explained earlier, the Nernst potential is the built-in potential of the membrane for which it is in equillibrium, meaning that there is no net current. To find this potential, it is first assumed there is only one type of ion in the channel. After that the other ion types are taken into consideration as well.

Channels permeable for one type of ion First it is is assumed the channel is only permeable to for example K^+-ions (potassium). This corresponds to taking into account only the first channel in Figure 1.5. Two processes occur simultaneously now. Due to the concentration difference between the outside and inside, diffusion starts to occur, where potassium ions will flow from

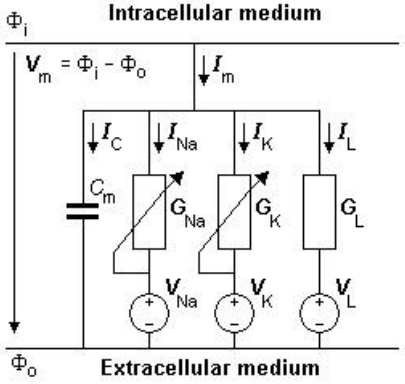


Figure 1.5: Advanced model for the membrane (from [48])

the inside to the outside. Due to the movement of charge, an electric field forms across the membrane, which will limit the diffusion current. These two processes will lead to an equilibrium. To quantitatively describe this situation, the ion fluxes as a result from an electric field as well as diffusion are obtained. By summing these two fluxes the total flux can be found as a function of the membrane voltage. Now the equillibrium potential can be found as the potential for which the total flux is zero. For the sake of clarity the complete derivation is incorporated in appendix A.1. The Nerst Potential is described by the equation:

$$V_k = \frac{RT}{z_k F} \ln \frac{c_{i,k}}{c_{o,k}} \tag{1.2}$$

Here V_k is the Nernst potential for potassium, R is the gas constant [8.314 J/mol K], T is the temperature [K], z is the valence of the ion, F is Faraday's constant [$9.6 \cdot 10^4$ C/mol] and c_i and c_o are the the intracellular and extracellular ionic concentrations [mol/cm^3] respectively. All the k-subscripts are denoted to emphasize that the Nernst potential is specific to one type of ion (in this case potassium).

Channels permeable for more types of ions In this section we incorporate all channels from Figure 1.5 again. As can be seen from the figure and from Equation 1.2, each ion has its own Nernst potential. At this point there is a 'conflict' in equilibrium between the different types of ions. Equillibrium cannot correspond anymore to a single voltage for which there is no ion flux, because the respective Nernst-voltages are not equal. Therefore the membrane voltage for which the cell is at rest corresponds to an 'intermediate' voltage, where the fluxes of the ions (which are in opposite directions) cancel each other. This means that the net flux is again zero, but ions are still flowing through the channel. The equilibrium is therefore not passive, but it corresponds to an active state.

By obtaining the Nernst potentials for all ions, the model from Figure 1.5 is already fully defined in terms of the voltage sources. To show that the resting potential (equillibrium) of the cell is indeed a compromise of all the individual Nernst potentials, an equation for the resting potential is derived. If the Nernst voltage is derived for all ion types involved (Na^+, K^+ and Cl^-), the membrane resting potential has the following form (Goldman-Hodgkin-Katz equation) [48]:

$$V_m = \frac{RT}{F} \ln \frac{P_K c_{i,K} + P_{Na} c_{i,Na} + P_{Cl} c_{o,Cl}}{P_K c_{o,K} + P_{Na} c_{o,Na} + P_{Cl} c_{i,Cl}} \tag{1.3}$$

Here P is the permeability of the ion and is defined as:

$$P_x = \frac{D_x \beta_x}{h} \tag{1.4}$$

Here D_x is the diffusion constant (of the ion of type x), β_x is the partition coefficient defined as the ratio between the concentration of the x^{th}ion and the total ion concentration. Finally h is the membrane thickness. For a derivation of the Goldman-Hodgkin-Katz equation the reader is again referred to appendix A.2. The equation shows the resting potential of the cell is indeed a 'compromise' between the (weighted) Nernst potentials of the different types of ions.

Channel conductance (Hodgkin-Huxley model)

The most widely used model to describe the channel conductance as a function of the membrane voltage ($G_{Na}(V_m)$ and $G_K(V_m)$) is given by the Hodgkin-Huxley membrane model. The model explaines many of the membrane properties with great accuracy. The model however was not derived on a theoretical basis, but only based on experimental results and curve fitting techniques. The experimental results used to obtain the equations are not incorporated in this discussion. Only the results are discussed.

Potassium conductance Based on the experiments, Hodgkin and Huxley assumed the permeability of the potassium channels is determined by a special kind of particle (called an n-particle) inside that channel. In other words: the channel conductivity is modulated by the number of n-particles within that channel. Based on the experimental results they assumed there must be 4 n-particles within a channel to make it conductive for potassium ions.

To describe the distribution of n-particles, they are assumed to be either within a channel (in the open state) or outside the channel (in the blocking state). The fraction of open state n-particles is denoted with n, which means the fraction of closed state n-particles must be $1 - n$. When the membrane voltage is changed, n and $1 - n$ will change accordingly, changing the membrane permeability as well. This process can be described using:

$$\frac{dn}{dt} = \alpha_n(1 - n) - \beta_n n \tag{1.5}$$

Where α_n is the transfer rate of n-particles from closed to open state and β_n is the transfer rate of n-particles from open to closed state. Equations for the values of α_n and β_n as a function of the membrane voltage are given in Table 1.1 and their curves are shown in Figure 1.6. As can be seen, at higher potentials the value of α_n increases, which means more channels will open and a larger potassium flux will result. When the voltage at a voltage clamp experiment is changed abruptly, the value for n can be determined using the equation above:

$$n(t) = n_\infty - (n_\infty - n_0)\exp(\frac{-t}{\tau_n}) \tag{1.6}$$

Here $n_\infty = \alpha_n/(\alpha_n + \beta_n)$ is the steady state value and $\tau_n = 1/(\alpha_n + \beta_n)$ is the time constant. In the Figure 1.6 n_∞ is plotted against the membrane voltage as well, showing again the increase in open state particles for increasing membrane voltage.

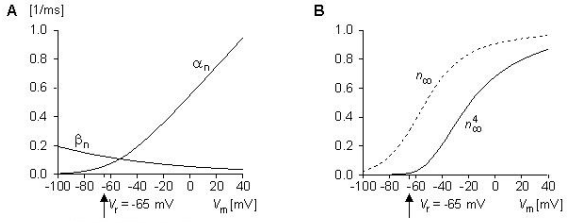


Figure 1.6: α_n and β_n (left) and the number of n-particles as a function of the membrane voltage (from [48])

Because four n-particles must be in the open state within one channel, the channel conductance is proportional to the number of n-particles to the fourth power:

$$G_K = G_{K,\max} n^4 \tag{1.7}$$

Sodium conductance The conductivity of sodium ions is for some part analogous to the potassium ions. Again the conductivity is modified by some special particles called m-particles, of which the number is determined by the voltage dependent α_m and β_m. The curves for α_m and β_m are plotted in Figure 1.7. Because of their values, the time constant is about 10 times smaller than for potassium, meaning a fast increase in sodium flux, which is in accordance with the experiments. For sodium channels, the channel is considered to be open if three m-particles are in the open state, meaning the conductance is proportional to m to the power 3.

However in sodium channels a second charged particle called h is present, which will inactivate the channel, no matter how many m-particles are in the open state. The h-particle can be described similar to the m and n particles by means of α_h and β_h parameters, which are plotted in Figure 1.7. The h-particles have a slightly higher time constant, meaning the channel conductivity will first increase and then decrease, because the h-particles become activated.

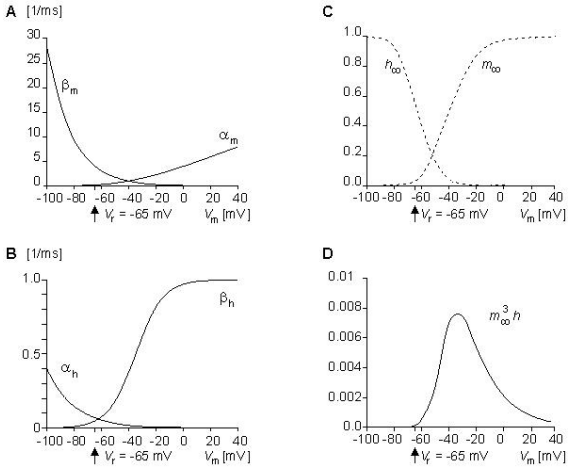


Figure 1.7: α_m and β_m (A), α_h and β_h (C), the number of m-particles (B) and h-particles (D) as a function of the membrane voltage (from [48])

Total channel conductance of the sodium channel is therefore described by the following equation:

$$G_{Na} = G_{Na,\max} m^3 h \tag{1.8}$$

Now that the two conductances are defined as a function of the voltage, the membrane model is complete. All equations associated with the Hodgkin-Huxley model are summarized in Table 1.1. In this table some of the constants used in practice are depicted as well. As can be seen in the top equation in this table the conductance derived in the previous sections is used to express the membrane current in terms of the membrane voltage. This equation will be used in the next sections to describe the membrane voltage when a stimulation impuls is applied.

1.2 Stimulation of the membrane

Now that a model has been developed for the membrane, the activation mechanism can be described. Therefore it is investigated how the membrane reacts on voltage changes due to stimulation from the outside world. Two types of stimulation are to be distiguished:

Table 1.1: Hodgkin-Huxley equations

Transmembrane current	
$I_m = C_m \frac{dV_m}{dt} + (V_m - V_{Na})G_{Na} + (V_m - V_K)G_K + (V_m - V_L)G_L$	
Ionic Conductances	
$G_K = G_{K,\max} n^4$	$\frac{dn}{dt} = \alpha_n(1-n) - \beta_n n$
$G_{Na} = G_{Na,\max} m^3 h$	$\frac{dm}{dt} = \alpha_m(1-m) - \beta_m m$
	$\frac{dh}{dt} = \alpha_h(1-h) - \beta_h h$
$G_L = \text{constant}$	
Transfer rate coefficients [ms^{-1}]	
$\alpha_m = \frac{0.1 \cdot (25 - V')}{\exp \frac{25-V'}{10} - 1}$	$\beta_m = \frac{4}{\exp \frac{V'}{18}}$
$\alpha_h = \frac{0.07}{\exp \frac{V'}{20}}$	$\beta_h = \frac{1}{\exp \frac{30-V'}{10} + 1}$
$\alpha_n = \frac{0.01(10 - V')}{\exp \frac{10-V'}{10} - 1}$	$\beta_n = \frac{0.125}{\exp \frac{V'}{80}}$
Constants	
$V_r - V_{Na} = -115\,\text{mV}$	$C_m = 1\,\mu\text{F/cm}^2$
$V_r - V_K = 12\,\text{mV}$	$G_{Na,\max} = 120\,\text{mS/cm}^2$
$V_r - V_L = -10.613\,\text{mV}$	$G_{K,\max} = 36\,\text{mS/cm}^2$
	$G_L = 0.3\,\text{mS/cm}^2$

- Excitatory stimulation (depolarization) is an increase in the membrane voltage. If the increase is large enough (above a certain threshold), a characteristic impulse can be produced by the membrane.

- Inhibitory stimulation (hyperpolarizing) is a decreasing in the membrane potential. This means the cell is 'blocked' even more than in equilibrium and an impulse will most likely not be produced.

Cells are subject to accommodation after a long period of continuous stimulation. In the case of *habituation* this results in an increase of the threshold. Similary *facilitation* is also possible, resulting in a decrease of the threshold. The *latency* of the cell is defined as the delay between the stimulation impulse and the 'reaction' of the cell by means of an impulse. The cell also demonstrates *refractory behavior*. Once an impulse is generated, the cell is insensitive to any new external stimulation pulses. At the end of the impulse, the cell is sensitive again, but the threshold is increased significantly (relative refraction).

1.2.1 Subthreshold stimulation

In this section the response of the membrane potential to a step current is derived, assuming the membrane voltage does not yet reach threshold. The current is injected into the membrane of an axon directly. It was chosen to model an axon instead of the cell body, because it is more easy to describe the structure of the axon. The axon can be modeled by the electric circuit depicted in Figure 1.8.

The axon is modelled using identical stages, each representing an infinitely small axial element of the axon. The axon is assumed to be infinitely long. In the figure x corresponds to the axial position of the axon. The r_i and r_o are impedances modeling the electric resistance of the intracellular and extracellular fluids. Since the membrane is assumed to stay in subthreshold, the

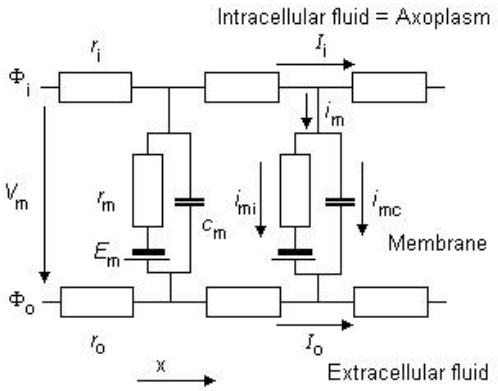


Figure 1.8: Membrane model for subthreshold membrane voltages (from [48])

channel conductance does not vary significantly and the membrane can be modeled using the basic model.

The response of the membrane voltage to a step current, can be found using standard circuit techniques. First we apply the general cable equation to the model:

$$\frac{\partial^2 V'}{\partial x^2} = (r_i + r_o) i_m \tag{1.9}$$

Here $V' = V_m - V_r$ is the membrane voltage deviation from the equillibrium point. Considering the structure of the membrane model (a capacitor and a conductance in parallel), the membrane current can be devided into a capactive and an ionic part, yielding:

$$\frac{1}{r_i + r_o} \frac{\partial^2 V'}{\partial x^2} = \frac{V'}{r_m} + c_m \frac{\partial V'}{\partial t} \tag{1.10}$$

Equation 1.10 sets the total membrane current equal to the resistive part (the ionic current) and the capacitive part. Rearranging the equation the following result is obtained:

$$-\lambda^2 \frac{\partial^2 V'}{\partial x^2} + \tau \frac{\partial V'}{\partial t} + V' = 0 \tag{1.11}$$

$\lambda = \sqrt{r_m/(r_i + r_o)}$ is the characteristic length of the axon describing how fast the introduced step decays along the axial length of the axon. Furthermore $\tau = r_m c_m$ is the time contant of the membrane, describing how fast the membrane voltage changes.

Equation 1.11 can be solved. The waveform has an exponential decaying form along the x-axis, determined by the space constant of the axon. The time response is also exponential, determined by the time constant of the membrane. A square shaped pulse will therefore invoke an exponentially growing voltage with an exponentially decaying shape along the axon. After the pulse, the voltage will again decrease exponentially back to its resting membrane voltage. This is illustrated in Figure 1.9.

Strength-duration curve

The purpose of stimulation is to bring the membrane voltage up to the threshold value in order to activate the cell. If it is assumed the membrane can be modeled using the subthreshold model described in the previous section, a relation between the stimulation pulse and the threshold conditions can be found. If it is assumed the stimulation current is constant, two variables remain: the pulse amplitude (in Amperes) and the pulse width (in seconds).

Because of the exponential nature, the stimulation current can either be short with high amplitude or long with low amplitude to reach a certain membrane voltage. This relation is visualized

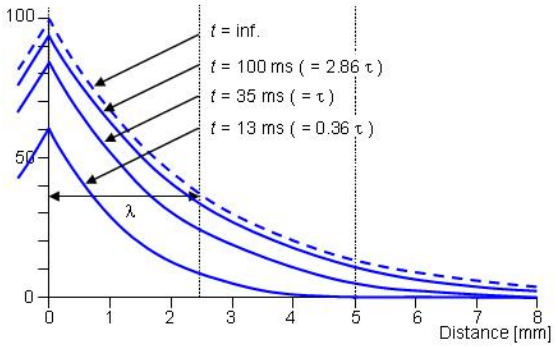


Figure 1.9: Membrane voltage respons to a voltage step function (subthreshold) (from [48])

in the strength-duration curve where the required amplitude is sketched as a function of the pulse width to reach threshold. If only the voltage of the membrane is considered at the point of stimulation (in other words: eliminate x from Equation 1.11 and return to the model from Figure 1.4) the following equation results:

$$I_s = \frac{V'}{R_m(1 - \exp\frac{-t}{\tau})} \tag{1.12}$$

If the voltage $V' = \Delta V$ is now defined as the change of the membrane voltage required to reach threshold, this equation describes the strength-duration curve. It is plotted in Figure 1.10. This widely used curve can be characterized by two parameters:

- The *Rheobase current* is the smallest amplitude for which threshold can be reached. Theoretically the pulse width should be infinitely long before threshold is reached. In Figure 1.10 the current is normalized to $I_{rh} = \Delta V / R_m$.
- The *Chronaxie* is the time needed to reach threshold with an amplitude of twice the rheobase current. This time is equivalent to 0.69τ.

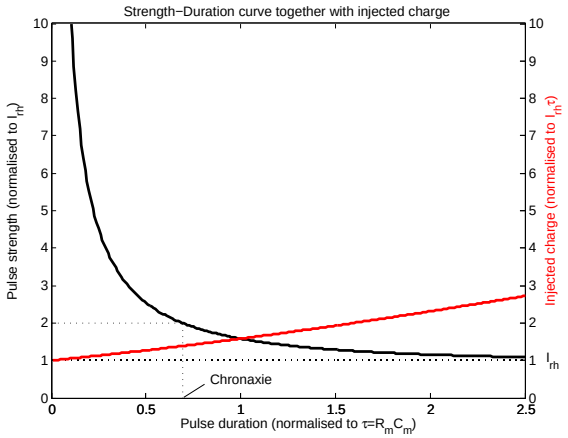


Figure 1.10: Strength-duraction curve together with the injected charge (red line)

In the figure the (normalized) charge injected to the tissue is also depicted. Since the current is constant, this curve is obtained by simply multiplying I_s with the time ($q = \int I dt$). As can be seen the lowest amount of charge is injected when using a short pulse duration. This can be explained by the fact that for longer pulse width the conductance is dissipating more energy. The

limit for $t \to 0$ is $I_{rh}\tau$. Although the current I_s would be infinitely large for $t = 0$, the total charge needed to charge the capacitor towards the required threshold value is $I_{rh}\tau$. Since no current is dissipated in the resistance during an infinitely small time interval, the total charge injected is simply $I_{rh}\tau$.

For minimal energy consumption the pulse width should therefore be chosen to be as short as possible. However, in practice the pulse duration is limited by safety constraints: the charge density cannot be too high in order to prevent electrolysis from happening. More about safe stimulation in Section 1.5.

1.2.2 Superthresold stimulation respons

In Equation 1.11 it was assumed the membrane impedance (r_m and c_m) remained constant. As long as V_m does not reach threshold, this assumption is reasonable. However, when threshold is reached the permeability of the membrane changes dramaticly, which means also the impedance will change. This will result in a non linear system, which is described in this section. To describe this situation a model similar to the model used in the subthreshold condition is used. The model for the membrane has now only be replaced by the Hodgkin-Huxley model from Figure 1.5. The result is depicted in Figure 1.11.

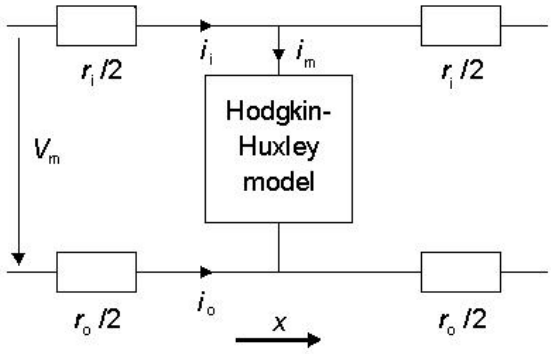


Figure 1.11: The axon model of Figure 1.8 with the Hodgkin-Huxley model incorporated for the superthreshold mode (from [48])

The total membrane current according to the Hodgkin-Huxley model was already found in Table 1.1 and is repeated here for convenience:

$$I_m = C_m \frac{dV_m}{dt} + (V_m - V_{Na})G_{Na} + (V_m - V_K)G_K + (V_m - V_L)G_L \tag{1.13}$$

This equation simply sums the currents through the three conductances (for sodium, potassium and chloride) and the capacitive current. Since the model in Figure 1.11 is almost identical to the subthreshold model, the differential equation describing the membrane voltage is similar as well. We only need to substitute Equation 1.13 for the ionic current in Equation 1.10.

$$\frac{a}{2\rho_i}\frac{\partial^2 V_m}{\partial x^2} = C_m \frac{\partial V_m}{\partial t} + (V_m - V_{Na})G_{Na} + (V_m - V_K)G_K + (V_m - V_L)G_L \tag{1.14}$$

Here it is assumed the space outside the cell is very large, which means the extracellular resistance is very small and can therefore be neglected. Here a is the axon radius and ρ_i is the axoplasm resistivity (resistivity of the material inside the axon [kΩ cm]). This differential equation is hard to solve and it can be modified slightly using the wave equation:

$$\frac{a}{2\rho_i\Theta^2}\frac{\partial^2 V_m}{\partial t^2} = C_m \frac{\partial V_m}{\partial t} + (V_m - V_{Na})G_{Na} + (V_m - V_K)G_K + (V_m - V_L)G_L \tag{1.15}$$

In this form the membrane voltage is evaluated on a fixed point x on the axon. Θ is the wave velocity within the axon. It can be either guessed or found via equations which are not discussed here. A numerical solution to this differential equation is given in Figure 1.12. The voltage of the axon has the specific form of the propagating pulse which was discussed before. This means that the Hodgkin-Huxley model is able to explain the most basic waveform in the cells.

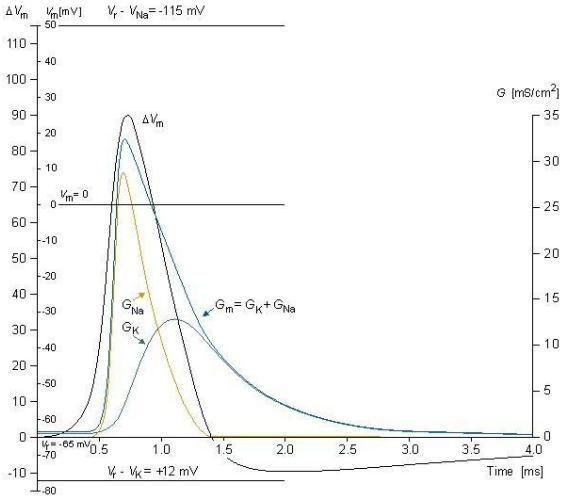


Figure 1.12: Activation pulse according to the Hodgkin-Huxley model (from [48])

Looking at the waveform in the figure above, 5 phases are to be distinguished:

1. The membrane voltage is raised, but is still under threshold. This means the conductances did not yet changed and the membrane current mainly consists of the capacitive current.

2. Threshold is reached and the activation begins. Sodium conductance increases. Sodium ions start to flow inward, causing the membrane voltage to become less negative and even positive in the end.

3. The membrane voltage reaches its maximum and starts to decrease again. This is because the sodium flow stops (due to the h-particles), which stops the increase in membrane voltage. Furthermore the potassium flow starts to grow more and more, which decreases the membrane voltage. The potassium conductance starts to increase much later, because of the larger time constant.

4. The membrane voltage keeps decreasing. Because of the higher potassium conductance the membrane voltage will even drop below the resting voltage for a while, hyperpolarizing the membrane.

5. Finally the conductances reach the resting value, as will be the case with the membrane voltage.

In this section the complete stimulation process was described qualitatively. It was shown that the stimulation process is started when the membrane voltage is lifted above a certain threshold value. At this point the ion channel conductance is changed, which triggers an activation pulse. Using the emperical Hodgkin-Huxley model this process can be described with sufficient accuracy.

1.3 Stimulating nerves with electrodes

In the previous section the respons of the membrane was derived when the membrane voltage was modified directly. In a practical situation however, electrodes are positioned at a distant

location from the axon itself. The electric field generated by the electrode has to travel through the tissue towards an axon in order to modify the potential. In this section a model is found for this situation.

1.3.1 Respons of a myelinated axon

The system which is to be modeled in this section is depicted in Figure 1.13. A point source I_a (representing an electrode) is placed at a distance h from a myelinated axon. The response of the axon in terms of membrane voltage and ionic currents is investigated.

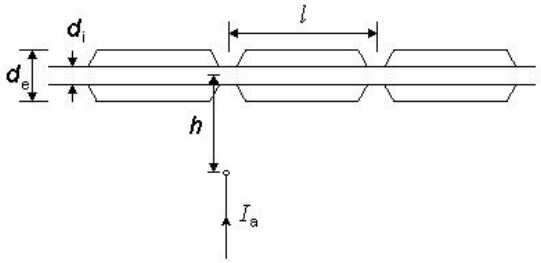


Figure 1.13: Stimulating a myelinated axon with a distant electrode (from [48])

First step is to model the axon itself. It is assumed that current can only flow through the membrane at the nodes of Ranvier (the places where no myelin sheath is present). Furthermore it is assumed that as long as the membrane voltage is below threshold, the membrane can be modeled by a parallel combination of a resistor and a capacitor (as was derived in the previous section). The membrane which is most likely to cross the sub-threshold condition is the one closest to the point source. This membrane must therefore be modeled by the Hodgkin-Huxley equation. Furthermore the axial current through the axon is determined by the conductance of the axon itself, which is given by:

$$r_i = \frac{4\rho_i l}{\pi d_i^2} \tag{1.16}$$

Here r_i is the axial intracellular resistance per internodal length, ρ_i is the intracellular resistivity [S cm], l is the internodal length and d_i is the axon diameter. Now the axon source combination can be modeled as illustrated in Figure 1.14. Each node of Ranvier is numbered, in order to be able to refer to them in an easy way.

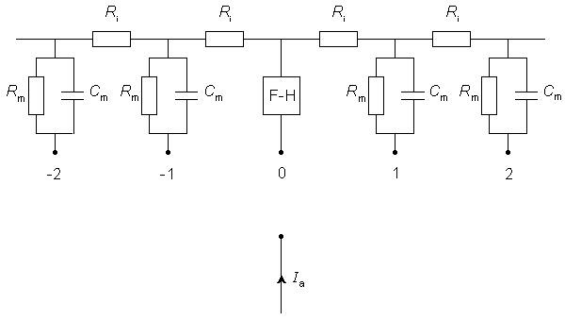


Figure 1.14: Model of the axon using the Hodgkin-Huxley equation for the central node (from [48])

Next step is to determine the (extracellular) voltage at each node of Ranvier. It is assumed this voltage is solely determined by the stimulation current (which is a good approximation if the

stimulation current is relatively strong). It holds:

$$\Phi_o = \frac{I_a}{4\pi\sigma_o r} \tag{1.17}$$

Here Φ_o is the (extracellular) stimulating potential field at a particular node, σ_o is the extracellular conductivity of the medium [kW cm] and r is the distance from the node to the point source.

Now using this equation and the model given in the figure, the membrane current at any node of Ranvier can be found. This current is simply the axial intracellular axial current entering the node $(V_{i,n-1} - V_{i,n})/r_i)$ minus the intracellular axial current leaving the node $(V_{i,n} - V_{i,n+1})/r_i)$:

$$I_{m,n} = \frac{1}{r_i}\left(V_{i,n-1} - 2V_{i,n} + V_{i,n+1}\right) = C_m \frac{dV_{m,n}}{dt} + I_{i,n} \tag{1.18}$$

The third term is composed of the capacitive current and the ionic current. Rearranging terms gives an equation for the membrane voltage:

$$\frac{dV_{m,n}}{dt} = \frac{1}{C_m}\left[\frac{1}{r_i}\left(V_{i,n-1} - 2V_{i,n} + V_{i,n+1}\right) - I_{i,n}\right] \tag{1.19}$$

In order to find an equation for the ionic current $I_{i,n}$ two situations need to be distinguished. First the membrane is assumed to be in subthreshold conditions $(I_{i,n} = V_{m,n}/R_m)$:

$$\frac{dV_{m,n}}{dt} = \frac{1}{C_m}\left[\frac{1}{r_i}\left(V_{m,n-1} - 2V_{m,n} + V_{m,n+1} + V_{o,n-1} - 2V_{o,n} + V_{o,n+1}\right) - \frac{V_{m,n}}{R_m}\right] \tag{1.20}$$

Where it is used that $V_i = V_m + V_o$. The other situation occurs when the membrane is activated:

$$\frac{dV_{m,0}}{dt} = \frac{1}{C_m}\left[\frac{1}{r_i}\left(V_{m,-1} - 2V_{m,0} + V_{m,1} + V_{o,-1} - 2V_{o,0} + V_{o,1}\right) - \pi d_i \nu (i_{Na} + i_K + i_p)\right] \tag{1.21}$$

Here ν is the nodal width. First we consider the case when the stimulus current is not high enough to reach threshold in node 0. In this case all nodes can be described using Equation 1.20. A typical response to a (positive) current step is given in Figure 1.15.

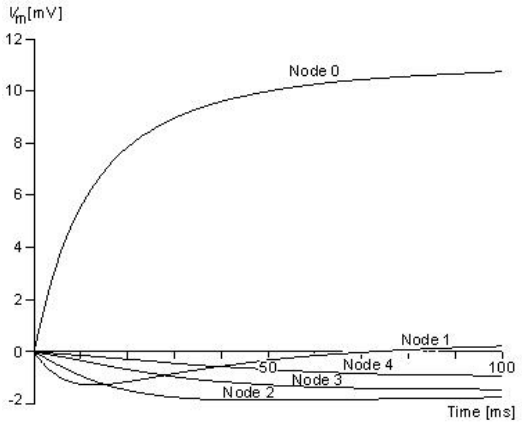


Figure 1.15: Membrane currents at different nodes as a result of a current step function in the electrode (from [48])

As can be seen the current enters in node 0 and depolarizes the node slightly, although not enough to let it reach its threshold value. The currents leave through nodes ± 2, ± 3 and ± 4 hyperpolarizing these nodes slightly. The nodes ± 1 are first hyperpolarized slightly, but after switching effects are diminished, they are both depolarized a little. If the current is reversed

(cathodic stimulation), all voltages reverse as well. This means that activation might take place at node 2 if the voltage is high enough.

In the case of a stimulating current which is strong enough to depolarize a node through the threshold value, the second equation needs to be evaluated for each activated node. Equations become much more complex, but using the equations from Hodgkin and Huxley it is possible to determine the threshold current and pulse duration. Using these data, a strength duration curve can be made again. This curve is slightly different from the idealized one from the previous section. Furthermore using these equations the effect of the axon diameter can be shown. As is shown the threshold increases for nerves with a smaller diameter.

The resulting strenght-duration curves are however omitted here for simplicity and the interested reader is refered to [48]. Key point however is that by stimulating nerves using electrodes the axon is activated at the point closest to the electrode. Furthermore the activation process is still similar to what was described in the previous sections (without electrodes): the membrane voltage needs to be lifted up to a certain threshold to start the activation process.

1.3.2 Respons of an unmyelinated axon

For the unmyelinated axon, the transmembrane current is not confined anymore to the nodes of Ranvier, but it can flow at any point along the axon. This situation can be approximated using the same model as the myelinated axon, but this time the segments are not of length l, but of length Δx, which can be made very small. Using a similar reasoning as for the myelinated axon, a differential equation for the transmembrane voltage can be found:

$$\frac{dV_{m,n}}{dt} = \frac{1}{c_m}\left[\frac{1}{r_i(\Delta x)^2}\left(V_{m,n-1} - 2V_{m,n} + V_{m,n+1} + V_{o,n-1} - 2V_{o,n} + V_{o,n+1}\right) - i_{mI}\right] \tag{1.22}$$

Again the ionic current i_{mI} is determined by a linear relation if the membrane is not activated and it is determined by the equations of Hodgkin and Huxley if it is activated. In the linear case this equation can be written in a more common form. Therefore we realize that for very small Δx the two terms in the equation are actually second order derivitives:

$$\frac{V_{n-1} - 2V_n + V_{n+1}}{(\Delta x)^2} \equiv \frac{V(a+2h) - 2V(a+h) + V(a)}{h^2} = \frac{d^2V}{dx^2} \tag{1.23}$$

Substituting this in the previous equation gives (for the linear subthreshold behaviour, where V_o is only dependent on the stimulation current and not on the activation mechanisms in the cell membrane):

$$\frac{dV_{m,n}}{dt} = \frac{1}{c_m}\left[\frac{1}{r_i}\frac{\partial^2 V_{m,n}}{\partial x^2} + \frac{1}{r_i}\frac{\partial^2 V_o}{\partial x^2} - \frac{V_{m,n}}{r_m}\right] \tag{1.24}$$

This means that the membrane voltage up to the threshold voltage can be described by this differential equation. In order to be able to activate the cell, this differential equation must satisfy $dV_{m,n}/dt > 0$.

Looking at the structure of the differential equation, this condition seems to be closely related to the d^2V_o/dx^2 term. It is often assumed that $dV_{m,n}/dt > 0$ if $d^2V_o/dx^2 > 0$. Although this is not true in general it gives a good indication. In Figure 1.16 d^2V_o/dx^2 is plotted as a function along the axon for both cathodal and anodal stimulation. In cathodal stimulation the potantial of the electrode is lowered, so the axon is depolarized at places closest to the axon (corresponding with node 0 in the myelinated case). In anodal stimulation, the potential is raised, so the membrane is only depolarized at places further away from the electrode.

It can be assumed now that depolarization (and maybe activation) takes place at those points where $d^2V_o/dx^2 > 0$, which corresponds to the shaded areas. As can be seen, the cathodal stimulation will have the biggest depolarization in the axon at the point 0, the closest to the stimulation site. This corresponds to the myelinated axon situation, where the membrane voltage is the largest at $n = 0$. Note that this figure only shows where activation might be possible. The stimulation current must still be high enough to reach the threshold voltage of the membrane.

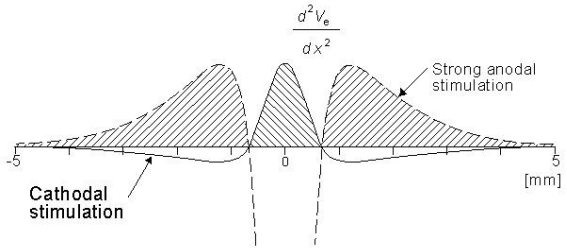


Figure 1.16: Areas of activation in an unmyelinated axon as a result from a step function in the electrode (from [48])

With anodic stimulation, the currents (and voltages) are all reversed and the $d^2V_o/dx^2 > 0$ occurs only at those points where it was negative in the cathodic stimulation. This is also depicted in the figure. However, it turns out the anodic stimulation requires the current to be 5 times as big as the cathodic stimulation to obtain the same fields. This is why it is stated 'strong anodal stimulation' in the figure. Again this figure is analogous to the myelinated axon situation, where the largest depolarization occurs in anodic stimulation at nodes ± 2.

Until now only the place at which stimulation might occur has been investigated. It is possible by using the equations obtained and the Hodgkin-Huxley equations to determine for which currents activation will occur. This is a mathematically complex operation and it is omitted here. The result however is depicted in Figure 1.17 for two different type of axons (in terms of size). The inner scale corresponds to a small axon (fiber diameter is $9.6\,\mu$m) and the outer scale to a large axon ($38.4\,\mu$m). The figure can be explained as follows.

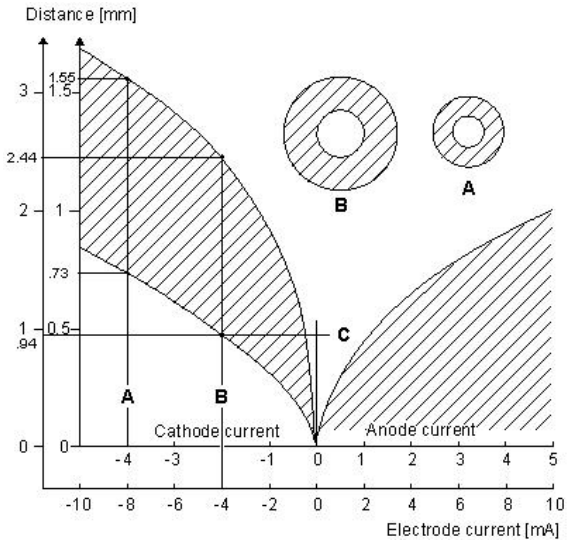


Figure 1.17: Activation areas (shaded) as a function of the electrode current and distance (from [48])

Cathodic pulse The figure is most easily read on a horizontal line, corresponding with a constant distance. In the cathodic stimulation case, the axon at a certain distance from the electrode is activated when the stimulation current has reached a certain threshold value (following the horizontal line from the center to the left). For higher currents then the threshold it will be activated as well, expect when the currents become really high. At this point the hyperpolarisation of the tissue further away then $|x| > h\sqrt{(2)}$ (the negative part of the

cathodal curve in Figure 1.17) will be too big, which prevents the activation pulse from propagating through the axon.

Anodic pulse In the anodic case there is a threshold current as well. Going to the right on a horizontal line shows that the membrane will be activated as soon as the current has reached the threshold. Because in the anodic case, there is no hyperpolarized membrane on the outer sides of the axon, the pulse can always propagate along the membrane, which means there is no maximum on the stimulation current. It is also seen that for the same distance the anodic current needs to be larger for activation then the cathodic current.

At this point the stimulation and activation of neural cells using electrodes has been described sufficiently. The basic mechanisms, required for the design of a stimulator system, are described both qualitatively and quantitatively. Therefore some of the concepts introduced here will be used in subsequent chapters on the design of the stimulator system. Furthermore this information will also be used in section 1.5 to define the boundaries for safe nerve stimulation.

1.4 Electrode Tissue interface modelling for electrical circuits

As was shown in section 1.1.3 the physical behavior and the generation of an activation pulse of a cell membrane is described quite accurate using the advanced membrance model, incorporating the Hodgkin-Huxely conductance, a membrane capacitance and a Nernst potential voltage source. This model was needed to understand the basic working principle of neural cells.

To design an electric circuit which is interacting with neural cells this model however is not suitable, since it does not describe the (external) electric properties of the cells. In this section a model is obtained for the impedance of the tissue seen from the terminals of the electrodes. As will be seen shortly, the interface between the electrodes and the tissue is the most challenging to model.

More then a century ago the first research has been conducted towards establishing a model for the electrode-tissue ystem In [73] it was discovered that the response of the interface was exponential and frequency dependent in nature and that it was therefore reasonable to model the system with a series RC circuit as depicted in Figure 1.18. Both components can be coupled to a physical meaning:

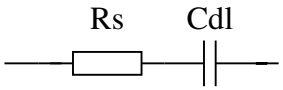


Figure 1.18: Simple RC equivalent model of the Electrode-tissue system

- *Double Layer Capacitor C_{dl}*
  The current (charge) in the electrode is a result of the movement of electrons. In the electrolyte the current originates due to the movement of ions. This means that at the electrode-electrolyte interface there is an interaction between two types of charged particles: electrons and ions. The interface which separates them is therefore capacitive in nature (C).

- *The series resistance R_s*
  The resistive component R corresponds to the resistance of the electrode leads and the tissue. In practice the resistance of the electrolyte will be much higher and is therefore the dominant component.

However, it was also discovered in [73] that the electrode-electrolyte interface is much more complicated then just a simple linear first order RC circuit. One of the additional mechanisms,

which need to be modeled, is the ionization of metal atoms at the electrode-electrolyte interface. The underlying electrochemical processes are quite complicated, especially due to the inhomogeneous surface of the electrode as described in [23]. These processes are modeled using an additional resistor, also called the leakage or charge transfer resistance R_{ct}.

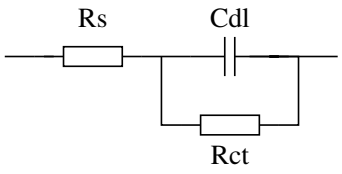


Figure 1.19: More extensive model of the Electrode-tissue system

The extended model is depicted in Figure 1.19 This model has long been considered as the most common way to represent the biomedical system. Many efforts have been made to quantitatively describe the electrode-electrolyte interface using this model ([60], [55], [56], [65], [20]). These experiments have shown that the component values are subject to many parameters:

- *Electrode material used*
  When using another type of metal, the ionization process will be different, as well as the value of the double layer capacitance.

- *Current density*
  Most materials show constant component values for low current densities. This means that the interface can be assumed linear when the current density is low enough (and all other parameters are constant). When the current exceeds the Limit Current of Linearity, the component values start of change dramaticly. Depending on the choice of the material C_{dl} is usually increasing and R_{ct} is decreasing.

- *Frequency* The values of C_{dl} and R_{ct} are also dependent on the frequency. For increasing frequencies both C_{dl} and R_{ct} will decrease approximately with $\sqrt{f}$. Also the Limit Current of Linearity is subject to frequency variations.

The dependencies described above show that the electrode-electrolyte interface is a highly non-linear system (except for low current densities and constant frequency). Based on the experimental results from [65], a theoretical model has been established in both [50] en [64]. The circuit is depicted in Figure 1.20.

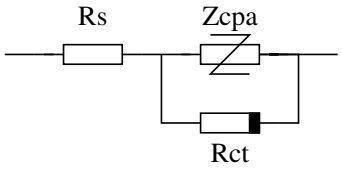


Figure 1.20: Complex model of the Electrode-tissue system

The Constant Phase Angle impedance Z_{cpa} is a replacement for the double-layer capacitance C_{dl} and is very much related to it:

$$Z_{cpa} = \frac{1}{(j\omega C_{dl})^{\beta}} \qquad 0 \leq \beta \leq 1 \tag{1.25}$$

Here β is a factor (usually around 0.8) which describes the deviation of Z_{cpa} from an ideal capacitance. This non ideality represents the distorted electrode area due to for example surface roughness. It is assumed the value of Z_{cpa} is more or less linear. This assumption is reasonable, since the non linearity of R_{ct} is much more apparent.

The resistor R_{ct} models the same physical phenomonom as in the model in Figure 1.19. This component accounts for the faradic current (due to ionization). This DC current component can be described using the Butler-Volmer equation (a basic equation from electrochemistry describing the current through an electrode resulting from both anodic and cathodic currents):

$$J = J_0 \left[\exp\left(\frac{(1-\alpha)nF\eta}{RT} \right) - \exp\left(\frac{-\alpha nF\eta}{RT} \right) \right] \tag{1.26}$$

Here n is the number of electrons per molecule oxidised of reduced, F is the Faraday constant (96 485 C/mol), η is the voltage deviation from the equillibrium voltage (v), R is the universal gas constant (8.3144 J/(K mol)), T is the absolute temperature (k) and J_0 is the exchange current desnity (a/ m^2).

To illustrate the highly non linear behavior of the faradic current as a function of the interface voltage, the faradic current is plotted in the same way as in [49] (using $n = 2$, $\alpha = 0.5$ and $i_o = 12.8\,\text{nA}$) in Figure 1.21.

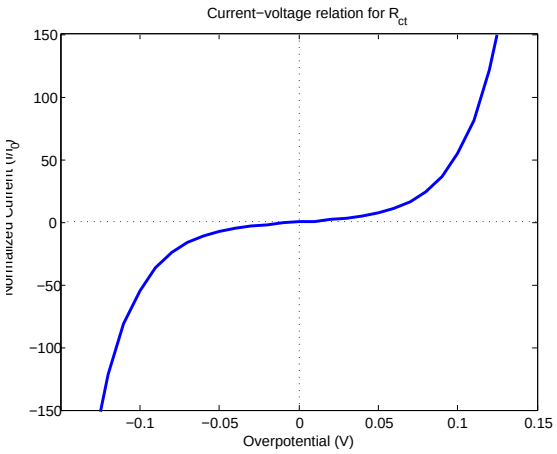


Figure 1.21: Current-voltage relation for the nonlinear charge transfer resistance

As can be seen the current increases rapidly in a nonlinear (exponential) way if the potential is increased above a few 100mV. The faradic current can be approximated as follows:

$$\eta >> \tfrac{RT}{\alpha nF} \qquad J = J_0 \exp\left(\frac{(1-\alpha)nF\eta}{RT} \right) \tag{1.27}$$

$$|\eta| << \tfrac{RT}{\alpha nF} \qquad J = \frac{J_0 nF\eta}{RT} \tag{1.28}$$

$$\eta << \tfrac{RT}{\alpha nF} \qquad J = J_0 \exp\left(\frac{-\alpha nF\eta}{RT} \right) \tag{1.29}$$

The faradic impedance is now given as the ratio of the overpotential η and the faradic current. In the exponential region of the current, the impedance can be found to be:

$$R_{ct} = \frac{RT \ln\left(\frac{J}{J_0}\right)}{(1-\alpha)nF} \frac{1}{J} = \frac{\eta}{I_0} \tag{1.30}$$

Here I_0 is the exchange current a $\cdot$ This shows the charge transfer resistance is indeed nonlinear. If the ln $\frac{J}{J_0}$ term is considered constant for varying currents, the resistance shows an inversely proportional dependence to the faradic current and an proportional dependence on the overpotential.

Having now described the two elements of the interface impedance, the total impedance can be considered. When only considering the interface itself, the impedance is the parallel combination

of Z_{cpa} and R_{ct}. To gain insight in the behavior of the interface, a plot is made in the R_s-X_s plane, the real and imaginaire parts of the interface impedance respectively in Figure 1.22. The plot comprises lines of constant impedance (absolute value), which show as halve circles in the plot.

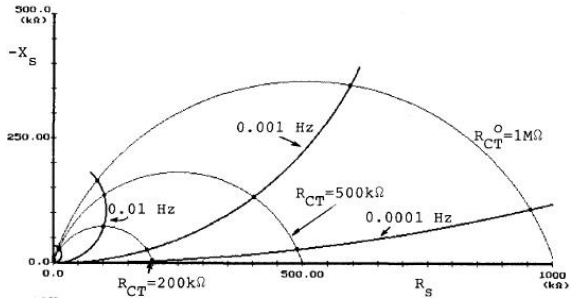


Figure 1.22: Plot of the interface impedance

Now over these lines of constant impedance are plotted the lines of constant frequency. The right part of the halve circle (of the constant impedance) is equivalent to the very low frequencies (the total impedance is almost equal to the R_{ct}, the DC impedance of the interface).

Remember now that the R_{ct} is the component which changes as a function of the applied current: it will decrease when the current intensity is increased. A decreasing R_{ct} is equivalent with a different (lower) constant impedance line. As can be seen from the figure R_s changes much more as a function of the current density then the high currents. The figure can be summarized as follows:

- If the current density is increased, R_{ct} is decreased.
- For low frequencies R_s is decreased very significantly due to the R_{ct} decrease.
  For high frequencies R_s is first increased slightly and then decreased.
- X_s is monotonically decreasing for all frequencies due to the R_{ct} decrease.

The behavior described above can also be understood differently: R_{ct} is highly nonlinear when the current density is increased. A change in R_{ct} affects the low frequencies first, since for those frequencies, the (non ideal) Z_{cpa} has a very high impedance. Higher frequencies are less effected by the change in R_{ct}, since for those frequencies Z_{cpa} has a lower impedance.

The current limit of non linearity I_l is defined as the current for which the impedance of the interface has changed with 10% compared to the linear impedance. Using this model it can be shown that

$$I_l \propto \omega^{\beta} \tag{1.31}$$

This result is also confirmed using experiments.

The model given in Figure 1.20 sufficiently describes the electrode-tissue system. In this section the behavior was discussed mostly from a qualitative point of view. In subsequent chapter on the design of the stimulator system the model will be used to investigate the currents and voltages at the output of the system when stimulating the tissue. In these chapters the model will therefore be used more quantitatively.

1.5 Safe nerve stimulation

Implanting and using a stimulator can result in neural damage. For some kind of damage the brain tissue is able to recover by regenerating cells, for other kind of damage this is not possible and the damage is irreversible. Damage can be divided in two main categories, of which the second is the most important from an electrical point of view.

In this section the mechanisms underlying tissue damage are described, such that safe stimulator design is possible.

1.5.1 Mechanically induced damage

Mechanical damage to a nerve can be the result of the incorrect placement of the electrode array, surgical trauma, pressure caused by swellings (postsurgical oedema), excessive scar formation (connective tissue) and tension on the electrode cables ([34]).

Many of these problems can be overcome if the device and electrodes are properly placed. For example the cables should always have some margin to allow for some stretching of the cables without the electrode to move.

Important factor in mechanically induced neural damage include ([34]):

- Interference of the blood supply of the cells due to the placement of the implant is not a problem, since the body will adapt and change the blood supply wherever necessary.
- Slight stretching of nerves is not a significant risk. Moderate stretching also does not result in chronic damage.
- Nerve constriction and compression is injurious.
- Intraneural electrodes involve more risks then cuff electrodes.

1.5.2 Electrically induced damage

Electrically induced damage can result in so called Early Axonal Degeneration (EAD). The myelin surrounding the axon collapses into the axonal space, preventing the axon from working normally. It is also shown that this type of damage will be partially irreversible. Furthermore there is not much late-onset injury, which means the EAD is a good indicator for neuronal damage due to electrical activity. In general EAD is assumed to result from two kinds of processes [34].

Electrochemical reactions

This type of damage is related to the passage of stimulus current across the interface between electrode and physiological fluid. This results in electrochemical reactions at the electrode-tissue interface. Examples of these reactions are given below for a platinum electrode in tissue [14]:

- Platinum electrode as anode
  - Electrolysis of water: $2H_20 \rightarrow O_2\uparrow + 4H^+ + 4e^-$
  - Oxidation of saline: e.g., $Cl^- + H_2O \rightarrow ClO^- + 2H^+ + 2e^-$
  - Oxidation of metal: e.g., $Pt + 6Cl^- \rightarrow PtCl_6^2 + 4e^-$
  - Oxidation of organics: e.g., $C_6H_{12}O_6 + 6H_2O \rightarrow 6C0_2 + 24H^+ + 24e^-$
- Platinum electrode as cathode
  - Reduction of hydrogen: $2e^- + 2H^+ \rightarrow H_2$.

As can be seen all these reactions are redox reactions and electrons are involved. This means that they indeed occur due to the passage of electrons through the electron-tissue interface. All these reactions are undesirable, because the products that result from the reactions can change the pH. A pH-change is very destructive for cells.

The equations above show that charge nullification (no net DC current) is very important to avoid the reactions from taking place. This fundamental safety issue was already discovered in 1955 ([44]). However, it is shown that at high current rates, exceeding the capabilities of the capacitance of the electrode-tissue interface, electrochemical reactions still occur. Some of them will be reversed in the charge cancellation phase, but not all of them. Therefore, even with charge balanced curves and noble metal electrodes, these reactions can still occur.

However, in [2] it is shown that, under some reasonable assumptions, the electrochemical reactions are not the major cause of damage in cells. In practice the charge density can be kept reasonably low ($100\,\mu\mathrm{C\,cm^{-2}}$ for platinum) while still reaching threshold for the nerve stimulation. If charge balancing is assured, the cells are not damaged by electrochemical reactions. This is proved by anaesthetizing the nerves (in order to remove damage resulting from activity of the cells). It was shown that damage does almost not occur then, so that it can be concluded that electrochemical reactions do not contribute significantly in damaging the tissue when stimulation parameters are kept in a reasonable range.

Passage of stimulus current through the tissue

This type of damaging process is found to be the most critical process. The damage is related with the axonal activity and or the depolarization and hyperpolarization of the cell membrane. However, it is not fully understood what process within the cells is responsible for the induced damage. It is only known that this type of damage is related to neuronal activity (due to the conclusions in [2]).

The best explanation for this phenomenon is that the damage is due to mass-activity in the axons. Due to the stimulation pulse a lot of axons are stimulated at the same moment. One of the consequences might be an accumulation of potassium outside the axons. This may lead to damage to the axons, but again this is not known precisely. Another 'strange' phenomenon is that the 'medium' sized axons seem to be the most vulnerable to this kind of damage, while the small and large axons remain undamaged. The large axons have a lower threshold and therefore more damage might be expected there. This is however not the case and the reason is not clear yet.

Although the physical principles are not understood yet, much research has been done in order to investigate the induced damage as a function of the electrical parameters. Goal of these studies was to correlate the stimulus parameters with the induced EAD in the axons. In contrast to the electrochemical reaction process, which can be characterized by limited charge density and charge per phase for a given electrode, this is not the case for activity related EAD.

Because the electrons are incorporated in the tissue, which is alive and time-variant the induced activity as a result of some current amplitude will vary among different cases. Therefore the activity needs to be normalized to some parameter.

A good parameter is found when the current is normalized to the current required to induce a certain activation (called the earliest α component of the compound action potential). It turns out a good correlation between several stimulation parameters can be found if normalized to the full α component [51].

- *Amplitude*
  Under a certain threshold almost no damage is observed. Above that threshold the amplitude has a more or less linear relationship with the amount of damage in the tissue ([52]).

- *Frequency*
  The frequency determines the slope of the linear relation between damage and amplitude. The slope increases for increasing frequency. This is depicted in Figure 1.23.

- *Pulse shape*
  When the pulse duration or the interphase delay is changed, the threshold of the amplitude/damage is changed as well. For example, when the pulse width is shortened, the amplitude threshold for damage becomes much larger. This supports the mass-activation theorem: a shorter pulse width activates the larger axons only, meaning less activity and therefore less damage due to mass-activity ([51]).

- *Continuity*
  If the period of continuous stimulation is shortened, the amount of damage is reduced as well. It is also possible to decrease damage if the stimulation duty cycle is lowered (for example 5 seconds of stimulation and then 5 second without stimulation). [1]

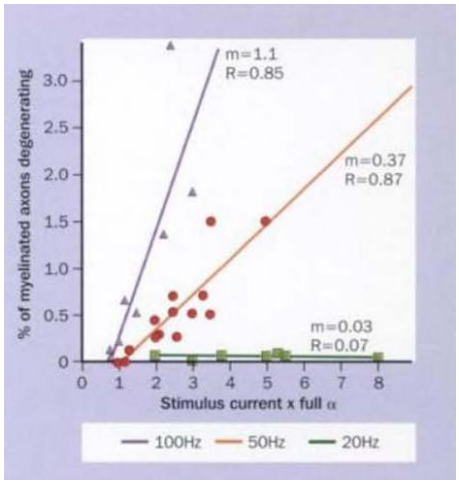


Figure 1.23: Neural damage as a function of amplitude and frequency (from [34]

In conclusion it can be stated that the underlying mechanisms of tissue damage are not yet fully understood. However emperical research has shown that neural damage is minimized if the stimulation uses as low an amplitude as possible, uses a low frequency and pulse width and stimulates as short as possible. Although it will not be possible to fullfill all requirements in a practical situation, the stimulation scheme can be adjusted in such a way the damage is minimised.

Chapter 2

The implantable brain stimulator: an overview

In this chapter a general overview of a brain stimulator system is given. In the first section the stimulator system is considered at a very high level of abstraction. In the subsequent section the emphasize will be on the design aspects of the output stage of the stimulator. Finally the technology in which the system will be realized is chosen. The choice for the technology is quite complicated, because the design of the output stage has certain special demands, such as high voltage capabilities.

Most of the content of this chapter is based on existing stimulator systems and references can be found throughout the chapter. The design aspects and challenges given in literature were ordered in categories presented in this chapter. Based on these categories some new concepts are introduced here as well.

The focus of the chapter is to outline the design choices which need to be made and to describe the advantages and disadvantages of these choices. The actual design choices are made in the next chapter.

2.1 General Stimulator system

In this section a general system level description of a stimulator system is given. The basic structure described here is similar to the structure described in [12]. Each stimulator system can be divided into the blocks depicted in Figure 2.1 Each block is treated shortly here.

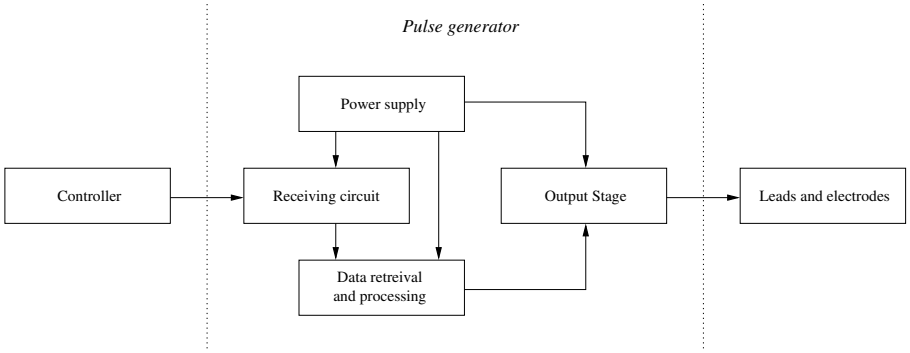


Figure 2.1: System level description of a stimulator

Controller During operation of the stimulator, it is controlled by means of an external controller. This controller can for example change stimulation parameters such as pulse width, frequency

and intensity or can turn the stimulator on and off. Depending on the application the controller must be able to control a certain amount of stimulation parameters.

Power supply This part of the system converts the energy from a certain power source into a stable power supply for the rest of the electrical circuit. The output of the circuit consists most of the time of several output voltages. A relatively high voltage is used to stimulate the tissue sufficiently strong. A lower voltage is used for all other electronics to reduce the power consumption.

The power source can be of many sorts. Some stimulators use an (integrated) battery, while others use telemetry (inductive coupling, for example [27], [9] and [18]) to wirelessly transmit energy transcutaneous (through the skin). A combination of telemetry and a (rechargeable) battery is also possible. Furthermore exotic power supplies such as acoustic waves are possible solutions as well [19]. The nature of the power source does however not change the fundamental function of the Power supply block.

Receiving circuit The receiving circuit is used to receive information from the external controller. If the energy source is telemetry, the receiving circuit also contains the receiving coil and some additional circuitry. In general the receiving circuit consists of all circuitry used to process incoming signals at the generator.

Data retrieval and processing The information received by the receiving circuit needs to be decoded using a certain demodulation technique. Furthermore this information needs to be interpreted and subsequently the stimulation process needs to be adjusted according to the command. Good data integrity and error checking is very important in the communication.

Output Stage This block is responsible for generating the actual stimulation pulses. The implementation of this block will be discussed more in depth in later chapters.

Lead wires and electrodes The lead wires and electrodes connect the pulse generator with the tissue. To minimize the chance for tissue damage the lead wires should be as short as possible. If the electrodes are located on the stimulator chip itself, there are no leads (this will be later referred to as a monolithic system).

Other important design choices for the electrodes include the electrode material and size. Both parameters determine the electrode capacitance, which effects the electric field produced by the electrode [16]. Electrode design however is a complicated research field on its own and is not discussed in depth ere.

2.1.1 Location of the system blocks

Based on the system block diagram defined in the previous section, a classification in systems can be made based on the location of the system blocks. In this section some of the possible solutions and the advantages and disadvantages are discussed.

First the degree of 'implantability' is discussed. What is meant here is which components of the system are implanted inside the body and which are located outside the body.

Surface of transcutaneous stimulation All components are placed outside the body. Stimulation is done from outside the body and the EM field is directed through the skin toward the stimulation location. Advantage is the fact this method is non invasive and the system has therefore no strict requirements in terms of size and bio compatibility. Disadvantages include the reduced reproducibility and accuracy and inconvenience for the patient (having the carry around an external stimulator).

Percutaneous stimulation Only the electrodes and (partially) the lead wires are implanted. The electrodes can be placed at exactly the right location, while the lead wires penetrate the skin towards the external pulse generator. Main advantage is the increased accuracy, while still having not severe size and bio compatibility constraints. Disadvantage is that the

penetration site is very vulnerable for infection, it is not robust and quite uncomfortable for the patient.

Implantable stimulation All parts of the system (except the wireless external controller) are implanted in the body. Advantages include high accuracy and high degree of comfort and aesthetics for the patient. Disadvantages include the high degree of invasion, placing severe constraints on the size (and therefore power consumption) and bio compatibility.

Based on the discussion above it can be concluded that the more components are implanted, the more severe the requirements on size and bio compatibility become, but also the more accuracy and patient comfort can be obtained.

One of the key requirements of an implantable solution is the power consumption. When the power consumption is low, two key requirements can be met:

- The energy source of the system can be smaller when power consumption is low. Either a smaller battery or a smaller telemetry coil (or a combination of these two) can be realized. In this way the system size decreases, yielding less implantation issues.

- When the power consumption is low, the heat generation within the device (due to power dissipation) is lower. It is important to keep the self heating of the device as low as possible, since temperature changes are destructive for neural cells. Therefore a low power consumption is also important from the safety point of view.

Although no design choices are made in this chapter, an exception is made hare, because the degree of implantability determines the design aspect of the system to a large degree. Because the stimulator is eventually to be designed for clinical use, the patient comfort is a very important constraint. Therefore the fully implanted system is chosen as the architecture used here.

Based on this choice still a few choices can be made about the relative position of the system blocks inside the body ([18]).

Monolithic All electronics are at the stimulation site. This means there are no lead wires. Main advantage is the body is invaded only at one side, meaning minimal damage. The main disadvantage are the extreme size constraints. The implant needs to be placed somewhere inside the brain, where space is very limited. The implant should therefore be extremely small.

Remote All electronics are at a remote location. A wire (lead) is connected between the stimulator and the electrode which stimulates the tissue. This is the way most practical stimulator systems work today. The advantage is a more suitable location can be found for the electronics. However, if this location is far away, the lead wires need to become very long, yielding a high degree of invasion for the body.

Modular Electronics are placed on the stimulation site as well as on a remote location, depending on the task of the specific module. For example the output stage is placed at the stimulation site, while all other blocks are at a remote location. This allows larger receiving circuits (antennas). The modules are connected via leads. Another advantage is the flexibility of this system: it is easy to connect an arbitrary number of stimulation modules to a single receiver.

Distributed This is a slightly different approach. Several independent and autonomous circuits perform stimulation at different locations, without having a link between them. The circuits are controlled by an external controller.

Most of the current clinical stimulators use the remote option. The pulse generator is placed in the chest of the patient and lead wires are placed (subcutaneously) towards the brain. The long lead wires can easily lead to infections or a wire break, yielding a malfunction of the system.

2.1.2 Stimulator with feedback

Almost all current stimulator designs use a 'direct' stimulation approach. This means the stimulation pulse is injected into the tissue without measuring the results or consequences in the tissue. This approach can be compared with early pacemaker systems.

Current state of the art pacemakers all make use of a feedback scheme: based on measurements of the heart pace it is decided if and how the pacemaker should stimulate the heart muscle. A similar approach can be incorporated in neural stimulators as well. The neural activity can be measured using neural amplifiers. Based on the measurements the stimulation scheme can be adjusted.

In Figure 2.2 a stimulator system is depicted including a feedback architecture. As can be seen the feedback chain is composed of 3 system blocks, which are treated shortly here.

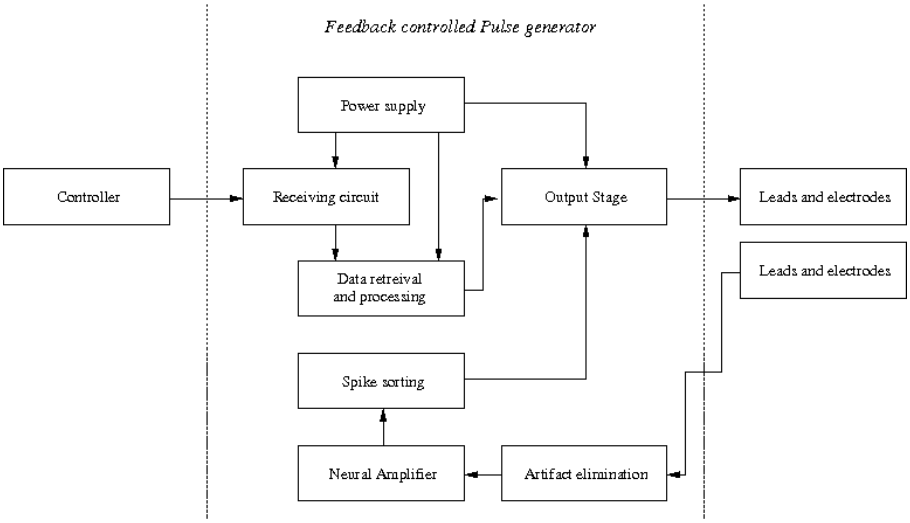


Figure 2.2: System level description of a stimulator with feedback

Artifact elimination

The signals the neural amplifier has to detect are generally very weak ([22], [31]) in the orders of several tens of micro volts. This means that the amplifiers which measure the neural signals must be very sensitive. However the output of the stimulator is a high amplitude stimulation pulse (several volts). This means that during a stimulation pulse the input of the sensitive neural amplifier would clip instantly when the stimulator is turned on.

This is of course undesirable, since no measurements would be possible during the stimulations. Considering the purpose of the system (stimulating the tissue), the immediate response of the tissue to the stimulation pulse is very important information. Therefore a method must be incorporated which allows measuring the tissue activity during and/or immediately after stimulation.

In literature two different methods exist. The first method tries to eliminate the stimulation artifact as fast as possible after the stimulation has ended ([22], [31], [10], [13], [33]). The result of a stimulation artifact is charge accumulation on the electrode. To understand this, take a look at the electrode-tissue interface model established in section 1.4. The interface is characterized using a (non ideal) capacitor. Due to the voltage impulse of the stimulation artifact the interface is charge with a relatively high voltage.

The artifact elimination technique tries to eliminate the accumulated charge as fast as possible by means active discharge circuit. Most of the times this circuit is an amplifier discharging the electrode interface. Most circuits are able to discharge the interface within several microseconds, which is about 100 times faster compared to the case when the interface discharges itself.

Another artifact elimination technique is presented in [29] and [35]. The idea is to use the information about the stimulation waveform, which can be extracted from the stimulator output stage, to subtract the stimulation artifact real time from the corrupted input signal. This results in a 'clean' neural activity signal again. To do this an adaptive filter is constructed similar as the wide spread Spectral Noise Cancellation technique.

The second technique has the advantage that the neural activity can be measured during the stimulation. In this way it can be determined exactly at what time the tissue is activated. At this point the stimulation can stop in order to avoid other cells to activate or to waste power on delivering useless stimulation pulses (the tissue was already activated).

Neural amplifier

As was outlined in the previous section the neural amplifier needs to be very sensitive because of the low amplitude of the neural signals. Literature reports many neural amplifier designs, the recent designs focusing more and more on power consumption [74]. Power consumption is particularly important if the amplifier is incorporated in big sensor arrays in which each single electrode has its own amplifier [8]. Furthermore the chip area is also important in these cases [30].

The bandwidth of the neural spike signals ranges from around 100 Hz to 1 kHz. In some applications the Local Field Potential (LPF) contains important information as well. The LPF is a very low frequency signal (100 mHz-100 Hz). One of the challenges in the bandwidth design of the amplifier is the chip area: because of the very low frequency large components (capacitors) are needed to suppress the DC signals. Active low frequency suppression (using a feedback control loop) proofs to be more area efficient.

Another important design aspect is the input referred noise of the amplifier. Because the neural signals are very weak, the input referred noise of the amplifier should be kept below the noise level of the background noise (around 5 μV-10 μV).

One of the interesting options in the amplifier design includes wavelet filters. In chapter 1.2 it was shown the shape of an activation impulse is known and can be described mathematically with good accuracy. The information about the shape of the pulse can be used to efficiently (especially in terms of power consumption) detect the neural spikes [36].

Spike sorting

The output of the neural amplifier comprises the amplified neural activity. The electrode which is used to monitor the neural activity is placed within the brain near the stimulation site. However in the vicinity of the electrode are many neural cells, which all produce neural spikes. Spike sorting is the process in which the spikes from the stimulation side are separated from the spikes from other cells. The separation is based on the amplitude and shape of the neural spikes.

Many types of spike sorting algorithms are developed [43]. The most simple spike sorting algorithm uses the amplitude information of the neural spikes. The electrode is positioned in such a way that the spikes from the cell of interest have the highest amplitude. Now the spikes can be easily discriminated using an amplitude threshold detection: only the spikes having a sufficiently high amplitude are considered to be the spikes of interest.

Main drawback of the amplitude threshold method is it cannot detect overlapping pulses and it cannot discriminate between different cells with the same activation pulse amplitude. Many more sophisticated spike sorting algorithms are developed, which are not treated in detail here. The main challenge in all these methods is to make them work under very low (0 dB) signal-to-noise ratios. Applied methods include the use of wavelet transforms in combination with neural networks [38] or using statistical properties of the activation pulse (Guassian Mixture Model) [66].

2.2 Output Stage

After the general description of a stimulator system the output stage is discussed in more detail in this section. The output stage is responsible for generating the pulses used for the tissue

stimulation. Various design aspects are treated in this chapter, based on both existing designs from literature as well as new ideas. The design aspects are summarized in table 2.1

2.2.1 Output quantity

The tissue is stimulated with electrical energy to either activate or deactivate particular areas of the brain. The amount of electrical energy delivered is to be controlled using an electrical quantity. The choice for which quantity is to be controlled is strongly related to the physical principles underlying the stimulation process.

As was shown in chapter 1, the electrode tissue interface can be modeled by an RC network. The stimulator is charging the (non ideal) capacitance, thereby changing the voltage in the tissue. When enough charge is delivered, the potential in the tissue reaches a certain threshold voltage, leading to (de)activation of the neural cells.

This means that the physical principles leading to activation can be best described using the quantity charge: the stimulator needs to deliver a certain amount of charge to the tissue in order to reach the threshold potential. However, most traditional stimulators don't use charge as the output steering quantity, but one of the following quantities:

Voltage steered Voltage steered output stages were applied in early stimulators, because of the easy implementation of voltage source. However, due to the highly time variant nature of the electrode-tissue interface impedance, the output current (and therefore the charge) of the stimulator is not easily controlled. This can easily lead to incorrect charges injected in the tissue. Furthermore charge cancellation (see section 2.2.3) is hard to achieve due to the unknown charge injection during both phases.

Current steered Current steered output stages are most often applied in state of the art stimulators (for example [18], [68], [9], [7], [75] and [57]). Using current control, the total charge is easily controlled by activating the current sources for a certain amount of time. Drawback is the high complexity of accurate current sources.

Both of these methods lack the direct charge control. Furthermore they both focus on keeping either the current or voltage constant, while the shape of both of these quantities is of no concern from the stimulation perspective; only the total charge injected matters. Especially for current control, it is not easy to implement an accurate and highly constant current source. Furthermore, lots of efforts need to be made to obtain charge cancellation through the control of these quantities. Therefore, purely charge controlled circuits would probably do a better job, being closer related to the underlying physical mechanisms.

Charge steered This is the ideal situation, since it is closest to the physical principles. Using this approach both the voltage and current waveforms are not important. Only the amount of charge injected is to be controlled.

The implementation of a charge controlled output stage is discussed further in subsequent chapters.

Note that regardless of which technique is chosen, the absolute value of the output quantity is not important. Since the electrode-tissue interface is very different from subject to subject (due to the incorporation of the electrode in the body by means of connective tissue), the absolute value of the stimulation parameter is of no significance. The subject should only indicate if the stimulation must be stronger or weaker.

For safety concerns the maximum allowable charge is important to prevent tissue damage. It is to be decided if the device should have a built-in protection against high charge (densities) or that the physician should prevent this from happening.

Table 2.1: Output stage design aspects

Output Quantity	**Pulse shape control**	**Charge Cancellation**	**Pulse Parameter Adjustability**	**Number of outputs**
Voltage	DAC	Coupling Capacitor	Amplitude and Pulse Width	Number of channels
Current	Analog processing	Electrode shortening	Interphase delay	Number of electrodes
Charge	DAC + Analog	High Frequency addition	Burst stimulation	Electrode arrangment
		Push/pull matching	Frequency	Push/pull stimulation
		Charge packet cancellation	Pulse shape	
		Charge metering	Pulse sequence	
			Subthreshold prepulses	
			Pulse symmetry	

2.2.2 Pulse shape control

With the output quantity defined, still design choices remain in terms of the output generation. Most likely a certain waveform is desired for stimulating and furthermore different output intensities are needed. Therefore simply connecting a source directly to the tissue is not possible.

The traditional way to construct a certain waveform is by using Digital to Analog Converters (DACs). The pulse shape is constructed using digital logic and is then converted to an analog signal to stimulate the tissue. In most traditional stimulators only square shaped waves are used. Using this scheme the DAC is set at a certain constant output intensity end subsequently the DAC is enabled for a certain period of time.

Several DAC based designs are reported in literature. A classical DAC based design can be found in [76]. Some modifications are found in literature, each focusing on a certain aspect of the DAC:

- To improve the *resolution* in [69] the design is modified to have a variable maximum current. When low intensities are required, the DAC current is reduced. In this way a high resolution can be obtained, even when the output current is small.
- When designing a stimulator with many output channels, the *area* of the stimulator becomes important. In [70] the area reduction was mainly obtained by introducing a more efficient current source implementation. In [21] the area reduction if obtained by introducing a multibias scheme: instead of using 2^N-1 transistors to generate the binary weighted currents, only N transistors are used, each of them biased differently to generate the binary weighted currents.
- To assure *monotonicity*, the DAC can be chosen to be made thermometer based instead of binary weighted [45].

An alternative to the use of a DAC is to do all signal processing in the analog domain. This technique can be used to obtain a very low power consumption. Recent publications mostly show applications in cochlear implants [28]. Input signals from a microphone is filtered and processed to create the stimulation pulses in an analog way. Publications show this can significantly decrease power consumption using sub-threshold operation compared to using DSPs.

The drawback of this scheme is the limited flexibility. An analog circuit is in most cases only applicable for a certain application. A little more flexibility while still having the low power consumption is to add a little digital control to the analog circuitry [27].

2.2.3 Charge Cancellation

In order to prevent electrolysis to happen at the electrode tissue interface, the net charge delivered to the tissue needs to be as close to zero as possible. This was shown in chapter 1.5. As a consequence almost all stimulators use a *biphasic* stimulation scheme: the stimulation pulse is followed by an inverted pulse of the same intensity and duration in order to compensate the injected charge.

However: due to mismatches and non linearities, the second pulse will never cancel out the injected charge perfectly. Therefore, additional circuitry needs to be designed to assure enough charge cancellation. Zero charge injection can be established with brute force by two methods.

Coupling capacitors By introducing series capacitors the DC signal is blocked [7]. The value of the coupling capacitor is determined by its constitutional relation:

$$I_{stim} = C\frac{dV}{dt} \tag{2.1}$$

If a stimulation current of 1 mA is assumed, the stimulation voltage is 1 V and the stimulation time is 1 ms, the required capacitor is already 1 μF. A capacitor of this size occupies a lot of area, yielding a large implant. Therefore this method is not very applicable.

Electrode shortening Zero charge injection can be obtained when the electrodes are short circuited in between stimulation pulses. During the shortening, the remaining charge on the electrodes gets a chance to leak away through the short.

The last method works fine, but in practice it turns out to require a lot of time to assure the charge has leaked away sufficiently. The combination of the equivalent electrode capacitance and resistance yields a fairly large time constant, as was discovered in chapter 1.4. This limits the maximal stimulation frequency. Therefore this method mostly applied after another technique for charge cancellation to cancel the very last bit of charge away.

Due to the limited functionality of these two 'brute force' charge cancellation techniques, most stimulators include other techniques to assure charge cancellation. Some techniques are described in this section.

High frequency addition Referring to equation 2.1 it is easily seen the size requirements of the capacitor can be reduced if the dt is reduced as well. To decrease the dt, the frequency of the pulse is increased. Subsequently two anti-phase high frequency pulse trains are added to produce a low frequency stimulation pulse [46], [47]. Each high frequency pulse trains needs its own coupling capacitor, but it the total capacitance area is much smaller because of the increased frequency.

Push/pull matching One of the most applied charge cancellation techniques is to try to match the second pulse in the biphasic stimulation scheme as much to the first pulse as possible [68], [41]. In this technique the positive and negative output current are compared with each other and by means of a certain internal feedback network they are matched as good as possible with each other. Perfect matching will never be possible, because of process variations in the feedback network. However, good results are reported in literature.

Charge packet cancellation Another charge cancellation method is reported in [57]. The result of charge remaining on the electrodes is a non zero voltage at the electrode (this is the result of the capacitance of the electrode/tissue interface: $V = Q/C$).

The idea of the charge packet cancellation technique is to measure the electrode voltage after stimulation. When the voltage is above a certain threshold value, a charge packet (a very small stimulation pulse) is injected in the tissue to lower the electrode voltage. After injection the voltage is measured again and another spike is injected if the voltage is still too high. In this way the electrode voltage (and thus the remaining charge) is brought below a certain safe value.

Although literature only reports the use of this system in biphasic schemes, it can also be used in a monophasic scheme. Note that the cancellation will take somewhat longer in this case: more charge packets will be needed to cancel the big initial voltage. However successive approximation schemes can improve the time needed to discharge the tissue interface.

Charge metering Using this method the physical quantity of interest is controlled directly. During the stimulation the injected charge is measured real time. The charge measuring mechanism can guarantee that during both phases of the biphasic stimulation the injected charge is equal. In [24] the charge is measured by integrating the current injected into the tissue. This method is essentially a charge steered output. The output current and voltage are of now interest anymore, only the injected charge is important. In subsequent chapters this method is discussed in more detail.

2.2.4 Pulse parameter adjustability

One of the main problems encountered in the clinical use of brain stimulators is the adaptive behavior of brain tissue. The impulses given by the stimulator are unnatural phenomena from the brain's perspective. The brain will therefore adapt itself in order to ignore the artificial pulses. This will eventually neutralize the beneficial effects of the brain stimulation.

One way to solve this problem is to increase the stimulation intensity. This will however also lead to more tissue damage, due to more mass activation, as explained in chapter 1.5. Another way to overcome the neural adaption is expected to be variation in pulse parameters. The idea is to frequently change pulse shape, duration, repetition rate and other parameters, so it is harder for the tissue to adapt itself.

Therefore the adjustability of the pulse parameters of the output stage is an important property. Besides the increased robustness against adaptation, the pulse parameter adjustability also determines the flexibility of the stimulator: the more parameters are adjustable, the more applications the stimulator will have. In this section the most important pulse parameter and their influence are discussed. An overview of the pulse parameters denoted in an example pulse is given in Figure 2.3.

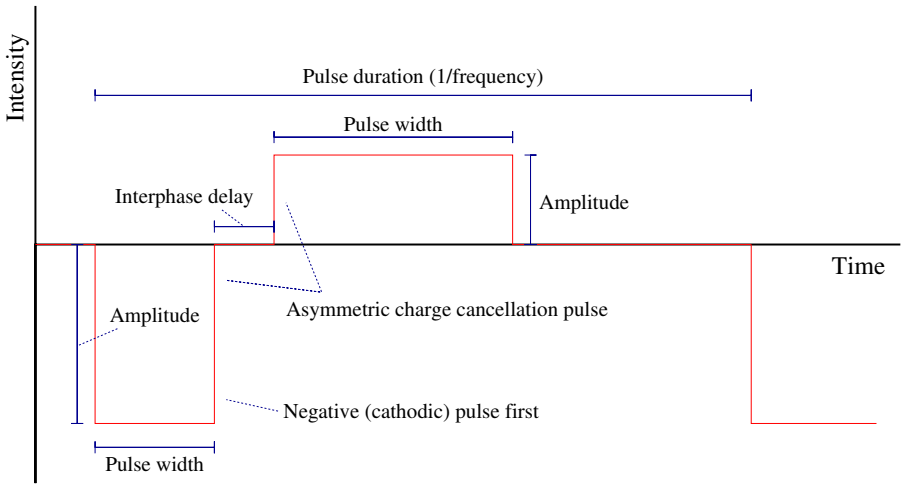


Figure 2.3: An example of a stimulation pulse with some pulse parameters denoted

Amplitude and pulse width The combination of the amplitude and pulse width of the stimulation pulse determines the charge applied to the tissue ($Q = \int Idt$). The more charge is injected, the higher the tissue voltage will become and the more cells will be activated. Both the maximum amplitude and pulse width (the maximum injectable charge) and the resolution determine the applicability of the device.

In terms of adaptation redundancy it is important to realize it is possible to vary the amplitude and pulse width, while still injecting the same charge into the tissue. This means that for different pulse shapes, still the same charge is injected, leading to the same tissue voltage.

As was already shown in chapter 1.2 shorter the pulse widths (and therefore higher the amplitudes) are preferred from an energy consumption perspective.

Interphase Delay The interphase delay is defined as the delay between the first and second pulse in a biphasic stimulation scheme. A small delay between the two pulses is required to allow the tissue to 'react' on the voltage change of the first stimulation pulse (due to the latency of the neural cells). The tissue must first be activated, before the tissue voltage can be lowered by the second charge cancellation pulse.

Changing the interphase delay changes the pulse 'shape' and therefore increases the robustness against adaptation. The minimum delay time is set by the time it takes for the tissue to activate and the maximum time is defined by safety constraints: the maximum allowed time to keep charge on the tissue.

Burst stimulation Some applications require the use of 'burst stimulation'. Instead of applying a single pulse to the tissue (which is subsequently canceled when using a biphasic stimulation scheme) a series of small pulses is applied shortly after each other. Not before this pulse train is finished the injected charge is canceled.

Frequency The frequency is defined as the repetition rate of the stimulation. Two types of frequency are distinguished:

Burst frequency, which is the repetition rate of the pulses within the burst pulse train.

Stimulation frequency, which is the repetition rate of one complete stimulation, including the charge cancellation pulse.

The frequency applied in stimulation is mostly application specific: each application requires more or less a fixed frequency. Therefore the frequency cannot be changed in order to increase the adaptation robustness, but it determines the number of applications the stimulator can be used for. It also has influence on the tissue damage as was seen in chapter 1.5.

Pulse shape The waveform is the shape of the output quantity of the pulse applied to the tissue. Most systems use an on-off characteristic and have therefore a square waveform. In case of a current steered device, this means the current has a square waveform, but the voltage can have any waveform, depending on the impedance of the electrodes.

There is not much known about the influence of the waveform. Most probably it is of not much influence on the activation process, since this only depends on the charging of the capacitor and the tissue potential. However, the pulse shape may have a relation with the amount of tissue damage involved with the stimulation and the robustness against tissue damage.

Therefore it can be chosen to design a stimulator where multiple waveforms can be chosen. Examples include square wave, triangles, exponentials, sinusoidal, etc.

Pulse sequence As was shown before the first pulse in a biphasic stimulation scheme is the pulse used to stimulate the tissue, while the second pulse is only used for charge cancellation. The polarity of the first pulse determines what kind of stimulation is used.

Using cathodic stimulation the voltage at the electrode is made more negative during the first stimulation pulse. In this case the cells are depolarized, yielding an activation mechanism. Cathodic stimulation is therefore used when a desired mechanism in the brains is absent or when a certain mechanism needs to be paced in a rhythm.

Using anodic stimulation the voltage at the electrode is made more positive during the first stimulation pulse. In this case the cells are hyperpolarized, yielding deactivation. This type of stimulation is used if a certain activation of the brain needs to be suppressed.

The stimulator can be configured either for one of these types of stimulation or for both types, in which case the stimulator will be applicable in more applications (flexibility).

Subthreshold prepulse Subthreshold prepulses are small (low amplitude) pulses which are excited just before the 'real' stimulation pulse. Using sub threshold prepulses some nerves at short distances from the electrodes can be effected, while due to the low amplitude the nerves further away will not experience any difference. The nerves nearby can be chosen to be either slightly depolarized or hyperpolarized. Due to this deviation from their equilibrium, they will respond different to a subsequent super threshold pulse.

Using a subthreshold cathodic pulse, the nerves are slightly depolarized. This means they will need a lower depolarizing pulse to activate them. This means that due to this lower amplitude less surrounding cells will be activated as well. Only cells more close to the electrode are activated.

Using a subthreshold anodic pulse, the nerves are slightly hyperpolarized. This means they will need a higher depolarizing pulse to activate them. This means that cells close to the

electrode will not be activated, but cells further away (which were not affected by the prepulse) will be activated.

Note that the same reasoning applies to a situation in which the cells need to be deactivated. Again using subthreshold prepulses the activation area can be either made smaller or wider (while not affecting the cells close by).

Pulse symmetry When using a biphasic stimulation scheme, the second pulse does not need to be of the same shape as the first pulse. The only requirement is to inject the same amount of charge into the tissue.

Reasons concerning minimizing the tissue damage or power consumption might lead to a different pulse shapes for the second pulse as for the first pulse.

Stimulation scheme

Stimulators in clinical use typically apply a certain stimulation program. A program is a series stimulation pulses for which the pulse parameters can be programmed. A program can consist for example of 20 pulses with alternating amplitudes and pulse width and a certain duty cycle in the repetition rate.

The variety in programming options for the stimulator greatly determines its effectiveness in clinical use. Each application will require a certain stimulation scheme, while even each individual patient will need slight modifications for optimal stimulation, because of the patient specific implantation in the brain.

In principle all pulse parameters discussed in this section can be controlled in a stimulation program. In terms of tissue damage it is very beneficial if a program can be repeated with a low duty cycle compared to continuous stimulation. Neural adaption is expected to decrease when using different pulse shapes.

2.2.5 Number of outputs

Another important property of the output stage is the number of electrodes attached to it. Again a few categories can be distinguished in the number of outputs.An example of a stimulator system with multiple outputs is given in Figure 2.4.

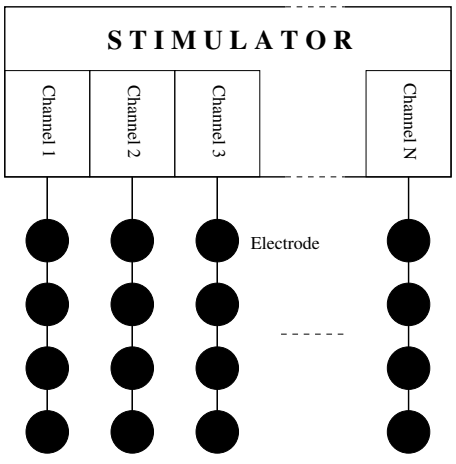


Figure 2.4: Multichannel stimulator system

Number of channels A channel is a set electrodes which can be controlled independent of another channel. In fact each channel is a small stimulator. Using multiple channels it is possible to stimulate at multiple electrodes simultaneously with different pulses.

Each channel needs its own output stage to stimulate independently of the other channels. The number of channels required depends on the application of the stimulator. Retinal implants need for example a high number of channels to stimulate the retina with enough 'pixels'.

Number of electrodes per channel Within each channel the number of electrodes can be varied as well. Using multiple electrodes, the tissue can be stimulated simultaneously with the same signal at multiple electrodes. The electrodes can also be stimulated successively with different signals (time multiplexed). Again the application determines the number of electrodes required.

The number of electrodes can also increase the spatial resolution of the stimulation. If multiple electrodes are implanted, the electrode which is the closest to the actual stimulation site can be chosen to be the active electrode. In this way the system is made more robust against implantation mistakes.

Furthermore the number of electrodes determine the possibilities for electrode arrangement, which is treated next.

Electrode arrangement The electrode arrangement is the spatial placement of the electrodes. When using only one electrode the stimulation is called monopolar. In this case the return electrode is at a distant location (usually at the stimulator).

When using two electrodes located close to each other the stimulation is bipolar. When using even more electrodes the stimulation is multipolar. In this case all kinds of arrangements can be made. In [75] and [42] a hexagonal arrangement is made. Using this setting pixels can be shifted around in the electrode array.

The consequences of the electrode arrangement for the stimulation are described in [40] using electric field simulations. In monopolar stimulation, the electric field is more spread out then in multipolar stimulation. In multipolar stimulation, the field is more confined to the area between the electrodes, yielding less side effects (in terms of damage) then monopolar stimulation.

Bipolar and monopolar stimulation have found to have comparable clinical benefits at low stimulation rates. At high stimulation intensities however, the monopolar stimulation induces more damage due to the higher spread area mentioned above.

However, monopolar stimulation is likely to be more selective then multipolar stimulation. The activation function is the second derivative of the electric potential. This means that for multipolar stimulation, cells are activated at each of the electrode-tissue interfaces. For monopolar this is only at the single interface of the electrode, yielding a higher selectivity.

Push/Pull stimulation Using a push-pull stimulation scheme the stimulator has sources in both the anodic as well as the cathodic branch. In this way the stimulation current is forced to flow through the selected electrodes.

In push or pull stimulation, the sources are only placed at the anodic or cathodic branch respectively. If a multipolar scheme is used leakage currents can more easily exist through electrodes located nearby. Therefore using a push-pull strategy the selectivity is increased.

2.3 Specifications of existing designs

Having defined the possible implementation choices for a stimulator system, it can be seen how the different existing stimulator systems perform. It turn out it is acutally quite difficult to compare different stimulator systems. First of all because they differ very much in implementation strategy (for example some are voltage controlled and others current controlled, which means the basic principle is quite different). Furthermore no clear figures of merit exist to compare the stimulator sytems.

Table 2.2: Existing stimmulator system specifications

System	Amplitude range	Pulse width range	Reptition rate
EON IPG [71]	$0 \sim 25.5\,\text{mA}$	$50 \sim 500\,\mu\text{s}$	$2 \sim 1\,200\,\text{Hz}$
Medtronic Resotre ULTRA [53]	$0 \sim 10.5\,\text{V}$	$60\,\mu\text{s} \sim 1\,\text{ms}$	$2 \sim 1\,200\,\text{Hz}$
Retinal Stimulator [18]	$< 140\,\mu\text{A}, < 3\,\text{V}$		
Stimulator [68]	$< 1\,\text{mA}$		
Cochlear Stimulator [9]	$< 500\,\mu\text{A}$	$> 4\,\mu\text{s}$	
Cochlear Stimulator [7]	$7.3 \sim 1\,800\,\mu\text{A}$	$8 \sim 58.1\,\mu\text{s}$	$1\,\text{kHz}$
Retinal Stimulator [75]	$2\,0 \sim 4\,030\,\mu\text{A}$		
Clinical values	$0.05 \sim 7\,\text{mA}$	$90 \sim 500\,\mu\text{s}$	$40.0 \sim 50\,\text{Hz}$

For example the power consumption of a stimulator is naturally a very important specification, since it determines battery life. However, some publications report the power consumption of the complete system, while others exclude the power associated with the stimulation pulses. A similar problem exist for specifications like efficiency. Often it is not clear what exactly is meant by efficiency. A natural way to define it, would be as the ratio between the power injected into the tissue divided by the total power consumed by the circuit. However very often this ratio heavily depends on for example the amplitude of the stimulation pulse chosen. Therefore this measure is most of the time not very meaningful.

When considering the power consumption and efficiency of the system designed in this project a clear definition is first made for the efficiency. This will be given in chapter 5.

For now simply a couple of systems are compared. The type of specifications that has none of the problems described above is the output range of the stimulator. These specifications include the amplitude range, pulse width range and repitition rate.

Some existing stimulators are investigted in Table 2.2. Note that the application areas for these stimulators are not strictly neural implants only. They include retinal stimulators, spinal cord stimulators, etcetera. However the output parameters are compared in order to get an idea of the scope of the output specifications required.

As can be seen the values for the amplitude reach up to several mA, while the voltage for most stimulators is high $\approx 10\,\text{V}$ as well (not depicted in the table). The pulse widths are maximum 1 ms and the maximum repitition rate is about 1 kHz. In the last row of the table some clinical values are depicted used in a treatment for chronical pain using Spinal Cord Stimulation. In this study a comparison was made between burst and tonic stimulation. The relatively high amplitudes of 7 mA were used for tonic stimulation, while burst stimulation needs lower amplitudes. It can be concluded that the required amplitudes for stimulation are rather high (in the order of several mA in combination with high voltages).

In Table 2.3 the power consumption of some existing systems is depicted. As explained before the values for the power consumption show a very large spread. Some of them (such as [7]) have a very high power consumption. This is due to the fact that this system also comprises an external device, which consumes quite a lot of power. For the system from [9] the power used in the stimulation waveform with an amplitude of 5 V is incorporated as well.

The quiscent power used by [75] is a parameter which gives a better view on the performance of the system. It means the system is always consuming $152\,\mu\text{W}$ at minimum, also when it is not stimulating. For the other systems it is not very clear which sources are exactly included in the determination of the power consumption.

From the previous discussion it can be concluded stimulator systems need high output values, both in terms of voltages as well as in terms of currents. The way in which the power consumption of a stimulator is defined is not very clear. When discussing the power consumption of the design made in this project it is compared to the values discussed here.

Table 2.3: Power consumption of some stimulator systems

System	Power consumption
Retinal Stimulator [18]	880 μW
Stimulator [68]	47 μW per channel
Cochlear Stimulator [9]	2.5 mW at 5 V
Cochlear Stimulator [7]	105 mW including external electronics
Retinal Stimulator [75]	9.8 mW (152 μW quiscent)

Table 2.4: Key parameters of Technologies offering high voltage capabilities

Manufacturer	Name	Size	Standard Voltage	Maximum voltage
AMIS (Alcatel)	I3T80	0.35 μm	3.3 V	80 V
AMIS (Alcatel)	I2T30	0.7 μm	5 V	30 V
AMIS (Alcatel)	I2T100	0.7 μm	5 V	100 V
AMS	CXZ	0.8 μm	3.3 V or 5 V	50 V
AMS	H35BxDx	0.35 μm		50 V

2.4 Technology choice

In this section considerations used for choosing the technology for the implementation of the system are discussed. This choice has big influences on the (im)possibilities of the system. To make the choice more complicated, the whole stimulator system needs to be implemented using this technology. This means not only the output stage described in this chapter, but also the digital parts, the communication part, etc. Digital circuitry has different requirements for the technology compared to the mostly analog circuitry designed in this report.

The starting point for the technology choice was availability: it was investigated which technologies were available and which of them provided the most fundamental requirements for the design. Availability was determined by both the processes provided by Europractice and some technologies provided by the Delft University of Technology (DIMES).

One of the most fundamental (and selective) requirements for the output stage is the compatibility of the technology with high voltages. For stimulation purposes the required voltage can be as high as 15 V. Standard technologies, especially with small feature sizes, cannot handle these high voltages. The number of available technologies with high voltage capabilities proved to be limited: from the available technologies only AMIS (Alcatel) and AMS (Austriamicrosystems) were offering high voltage devices. The technologies are listed in table 2.4 together with some key parameters. As can be seen all technologies offer maximum voltage rating which are high enough for the purposes in this project.

Next step is to compare the technologies on different aspects than high voltage compatibility. Therefore it is first required to know the requirements for the technologies from both an analog and digital perspective. At this stage of the decision trajectory it is sufficient to describe these requirements in a qualitative and high level way.

From an analog perspective the technology should offer enough options for the integration of passive components, such as capacitors, resistors and diodes. Although at this stage it is difficult to know precisely, it might be useful if the technology offers bipolar transistors as well. Of less importance is the speed of the system: maximum stimulation frequencies reach up to several kilohertz only.

From a digital perspective, the most important requirement is the power consumption. This power consumption includes both the static as well as the dynamic (switching) power consumption.

General requirements (both from analog as well as digital perspective) include reliability. One

aspect of reliability is the protection of the chip against ElectroStatic Discharge (ESD). Because the chip will have connections with the outside world via electrodes, electrostatic discharge is an issue. Another aspect might be temperature dependence of the components. Although the chip will be implanted and will therefore operate in an environment with almost constant temperature, the temperature dependence should be as small as possible. Most of the component parameters are specified at room temperature, which is different from body temperature. Therefore to find the parameters which will be valid for the system, the temperature dependence needs to be taken into account.

First the differences between both technologies (AMS and AMIS) are compared at a high level to make a first choice. This can be done using the data sheets of the technologies offered by Europractice. The following aspects were noticed:

- Both technologies offer components required for analog circuitry, such as Bipolar transistors, diodes, resistors and capacitors. However it is noted in the specification sheets of AMS, that the analog library of AMS is not available through Europractice, only directly through AMS. This is a drawback compared to the AMIS technologies, which are fully avaiable through Europractice.

- Both technologies are used in existing designs for stimulator systems. Examples of AMIS based systems include [68], [9] and [62], while AMS based systems are reported in [75] and [27]. All these references report working stimulator systems. This indicates that both technologies are suitable for implementing stimulator systems.

- Both technologies offer ESD protection comoponents and circuitry.

- Overall the documentation provided by AMIS is more open and more elaborate than the documentation from AMS. On the website of Europractice AMIS provides already a lot of transistor parameters, while in the design kits very detailed information can be found: from layout details, process variations to ESD protection. For AMS only a limited parameters are given at the Europractice website and the documentation of the technology can only be obtained via the website of AMS, where a password is required.

Based on the observations above it was chosen to investigate the AMIS technology in more detail. From both I3T80 and I2T100 the extensive diesign kits were readily available. This was not the case for the I2T30 technology. Therefore in the next section the I3T80 and I2T100 technologies are compared head to head. The I2T30 technology is omitted, but not forgotten. This technology is actually the same as I2T100. Only the high voltage components are different in the sense they are rated for a lower voltage. If the I2T100 technology turns out to be better then the I3T80 technology, the I2T30 technology should be compared to the I2T100 technology.

2.4.1 Comparing I2T100 and I3T80 technologies

In this section the I2T100 (a 0.7 μm technology) is compared to the I3T80 (a 0.35 μm technology). The technologies are compared based on the requirements set in the previous section, but this time in a quantitative way. The required quantitative parameters are mostly found in the design manuals provided with the technology ([5], [6], [3], [4]). In the following subsections each requirement is investigated in a more detailed way.

Analog components availability

Both technologies offer a variety of analog components in the form of resistors, capacitors and diodes. These components can be created with the help of both metal layers as well as diffusion and poly layers. This offers possibilities for high and low value components with low or high accuracy. Based on the basic documentation available there are no significant differences for the analog components between these two technologies.

In both technologies all analog components come in versions which can handle high voltages. Both technologies use so called DMOS technology to include high voltage transistors. The circuit symbols for these components are depicted in Figure 2.5. These particular type of transistors are designed to withstand a high voltage between the gate and drain terminals. In the I3T80 technology $V_{DS} < 80$ and in the I2T100 technology $V_{DS} < 100$. Note that the gate-source voltage is still limited by the 'normal' breakdown voltages (around 3 V for I3T80 and around 5 V for I2T100). This means the device is not symmetrical, in contrast to 'normal' CMOS devices.

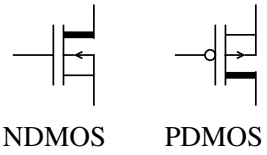


Figure 2.5: Circuit symbols for the High Voltage DMOS transistors

Furthermore these type of transistors take up quite some space on the chip area. As a rough estimate the following equations give the size of the transistors in μm^2 for the I3T80 technology:

$$\text{PDMOS}: \quad A = (40 + 8N_s)\left(\frac{W}{N_s} + 39\right) \tag{2.2}$$

$$\text{NDMOS}: \quad A = \left(\frac{W}{N_s} + 37\right)(55 + 8N_s) \tag{2.3}$$

Here W is the width of the transistors (which needs to be $> 20\mu m$ for reliable operation) and N_s is the number of fingers (which needs to be > 2 and preferably even). This means that the minimum size of these transistors is $2744\,\mu\text{m}^2$ and $3337\,\mu\text{m}^2$ for PDMOS and NDMOS respectively. When the I2T100 technology is chosen, these numbers will be even bigger. To keep the area of the chip as small as possible, the use of high voltage transistors should therefore be avoided as much as possible.

Besides the DMOS, both technologies also provide normal CMOS transistors with floating abilities. This means that the voltage over each terminals is still limited to the low voltage. However, the voltage with respect to the substrate can be much higher. The size of these floating transistors is much smaller then the DMOS transistors.

Static Leakage

For decreasing technology size, the static leakage current will increase [11]. For digital applications the static leakage is important. Most likely the device will be idle for a relatively long time, during which leakage is responsible for the power dissipation. Since this problem is especially important to the digital design, the leakage of the standard (low voltage) NMOS and PMOS transistors is compared in Table 2.5.

Table 2.5: Leakage current per transistor width in pA/μm for $V_g = 0\,\text{V}$ (From AMIS documentation)

Device	0.7 μm Typ/Worst case $V_g = 0\,\text{V}$, $V_d = 7\,\text{V}$	0.35 μm Typ/Worst case $V_g = 0\,\text{V}$, $V_d = 3.63\,\text{V}$
NMOS	/10	1/50
PMOS	/-10	-1/-50

For the 0.7μ technology no typical values were specified, only the worst case values were specified. Comparing the worst case values of the two technologies the 0.7μ technology performs

better, which is to be expected, since larger technologies have smaller leakage currents. Since the information of the typical values is not complete, the only comparison can be made for the worst case.

The power lost due to the leakage is however also dependent on the voltage used. This means for the 0.35μ technology the worst case static leakage power dissipation is $\mathrm{p} = \mathrm{i}\,\mathrm{v} = 5\,0 * 3.3 = 1\,65\,\mathrm{pW}/\mu\mathrm{m}$, while for the 0.7μ technology it is $\mathrm{p} = \mathrm{i}\,\mathrm{v} = 1\,0 * 5 = 50\,\mathrm{pW}/\mu\mathrm{m}$. This means the leakage is 3.3 times as bad for the 0.35μ as for the 0.7μ.

Switching leakage

The switching leakage in digital logic is mostly determined by the gate capacitance of the transistors. To compare the two technologies the gate capacitance is used. Other important capacitances include mainly the interconnect capacitance and less importantly the drain and source capacitances. However, here only the gate capacitance is compared.

Table 2.6: Some parameters related to the gate capacitance of a 0.35μ LV CMOS
(From AMIS documentation)

Device	Parameter	Unit	Low	Typical	High	Condition
Nchannel	Tox	nm	6.5	7.1	7.7	Optical measurement
		nm		7.4		Calculated from Cplate
	Cplate	F/m		4.66e-3		V=-4V
	VBD	V		7		I = 1 mA/cm2
Pchannel	Tox	nm	6.5	7.1	7.7	Optical measurement
		nm		7.4		Calculated from Cplate
	Cplate	F/m		4.66e-3		V=+4V
	VBD	V		7		I = 1 mA/cm2

Table 2.7: Some parameters related to the gate capacitance of a 0.7μ LV CMOS
(From AMIS documentation)

Device	Parameter	Unit	Low	Typical	High	Condition
Nchannel	Tox	nm	15.5	17.0	18.5	Cmax (Vdnom)
	Cplate	F/m2				Calc. or meas.
	Vbd	V	12	20		I = 1 mA/cm2
	CGDO	F/m	2.3e-10	3.1e-10	3.9e-10	TBD
	CGSO	F/m	2.3e-10	3.1e-10	3.9e-10	TBD
Pchannel	Tox	nm	15.5	17.0	18.5	Cmax (Vdnom)
	Cplate	F/m2				Calc. or meas.
	Vbd	V	12	20		I = 1 mA/cm2
	CGDO	F/m	1.9e-10	2.2e-10	2.6e-10	TBD
	CGSO	F/m	1.9e-10	2.2e-10	2.6e-10	TBD

For some reason the gate capacitance in the documentation for the 0.7μ process is omitted. However, if the parallel plate approach is used, it is seen the capacitance value is proportional to the area of the device and inversely proportional to the distance between the plates:

$$C = \frac{\epsilon A}{d} \tag{2.4}$$

Based on the oxide thickness, the distance d is approximately halved in the 0.35μ technology compared to the 0.7μ option. However, the minimum feature size is also halved (0.35μ compared

to 0.7μ). This means the area A is reduced by four times. Using the parallel plate approach, the gate capacitance of the 0.35μ process should be halved compared to the 0.7μ technology.

This means that the dynamic leakage for the 0.35μ technology is most likely smaller then the dynamic leakage for the 0.7μ technology. Again the power associated with this leakage depends on the voltage used. the energy required to charge a gate capacitor towards the supply voltage is:

$$E = \frac{Cv_{dd}^2}{2} \tag{2.5}$$

This means that charging a gate capacitance in the 0.35μ technology requires about $(Cv_{dd}^2)/(0.5C(0.66v_{dd})^2) = 4.6$ times less energy than charging the gate capacitance in the 0.7μ technology.

Temperature dependence

Although the transistors will be operated in an environment where the temperature will be constant (temperature change of brain tissue is very destructive), the temperature coefficients are important: most of the parameters in the datasheets are given for 25 degrees, while the system will operate around 37 degrees.

Table 2.8: Temperature dependence of a 0.35μ LV CMOS (W/L=10/0.35)
(From AMIS documentation)

Temperature coefficient	Unit	Value	Conditions
Vt(0)	mV/C	-1.0	Vds = 100 mV, Vbs = 0 V
β_{lin}	N/A	-1.6	Vds = 100 mV, Vbs = 0 V
Idsat	%/C	-0.16	Vds = Vgs = 3.3 V, Vbs = 0 V

Table 2.9: Temperature dependence of a 0.7μ LV CMOS (W/L=20/0.7)(From AMIS documentation)

Temperature coefficient	Unit	Value	Conditions
Vt(0)	mV/C	-1.5	V_d is linear regime
β_{lin}	$\log(\mu A/V^2)/\log(K)$	-1.83	V_d in linear regime
Idsat	μA/C	-13.8	$I_{d,sat}/W = 358\,\mu A/\mu m$
	%/C	-0.19	

In Table 2.8 and 2.9 some parameters are given related to the temperature dependence of the Low voltage CMOS transistors in the 0.35μ and 0.7μ technologies respectively. The temperature dependence of the threshold voltage, the current factor $\beta = \mu_n C_{ox} W/L$ (the factor in front of the expression for the drain current) and the saturation current are given. From these tables it can be concluded that the 0.7u technology is slightly more sensitive to temperature changes. The differences are quite small however, especially if considering the fact that the temperature variations in the tissue will be very low anyway.

ESD protection

Because the device will be connected to the outside world using electrodes, the chances for ElectroStatic Discharge (ESD) are big. ESD can potentially damage a chip severely. Therefore it is important that the technology provides means to protect the device from ESD.

Both technologies provide ESD protection libraries. The 0.35μ ESD protection library seems to be better documented than the 0.7μ technology. From both documentations however it is hard to extract comparing specifications of the ESD components.

Conclusions

Based on the different requirements investigated in the previous paragraphs a decision about which technology to be used is made. First of all it is clear that from an analog point of view both technologies can offer similar components.

From a digital point of view the static leakage is lower (3.3 times) for the I2T100 technology, while the switching leakage is lower (4.6 times) for the I3T80 technology. However, it's very hard to draw any conclusions from this. It's unkown what the ratio will be between the amount of static leakage and dynamic leakage. In terms of temperature dependence the I3T80 technology performs slightly better. Based upon these points the I3T80 technology has slight advantage over the I2T100 technology. However two additional points are important to consider:

- The smaller feature size of the I3T80 technology will result in a smaller chip area. This is a particularly important requirement of a stimulator, since this will lead to a smaller impact of the stimulator on the body. The minimum gate length of the I3T80 technology is 1.7 times smaller than the minimum gate length of the I2T100 technology. If this scaling factor could be used for both dimensions (which will in practice not be the case, but here it is used as an indicator), the chip could be $1.7^2 \approx 3$ times as small. This is a significant advantage.
- The I3T80 technology is a newer technology than the I2T100 technology. This means the most likely Alcatel will support the I3T80 technology for a longer time than the I2T100. Since it is expected that the technology used in this project will be used for several years, this is also an important factor. Having to redesign a complete circuit for a different technology is a lot of work.

Based on these additional points, together with everything else mentioned in the previous sections, it is decided to choose for the I3T80 technology.

Chapter 3

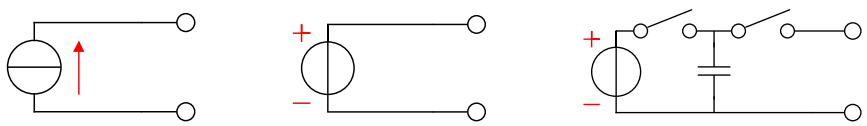
Design of a charge steered output stage

In this chapter the design of the output stage is treated. In the first section several alternative fundamental design choices are discussed. This will lead to a system level description of the output stage in terms of system blocks.

In the next section, a closer look is taken to the tissue model. The response of this model is quite important for the design of the various system blocks. Some of the tissue interface models discussed in the first chapter are compared here. Based on these comparison it is also decided what model is to be used for simulation purposes.

3.1 General layout of the output stage

As explained in chapter 2.2 a charge controlled implementation of the output stage is closest to the underlying physical principles of stimulation. This means that a charge controlled circuit does not suffer from drawbacks of the Voltage and Current stimulators such as keeping the voltage or current output well defined, while this is not necessary for stimulation. The most common charge source existing is a capacitor. This means that a charge controlled output stage will consist of a capacitor on which a certain amount of charge is stored. This charge is subsequently discharged into the tissue. In Figure 3.1 the fundamental three types of output stages are depicted. Note that a flux source is not included here (and was not discussed in the previous chapter as well). In principle it is possible to stimulate the tissue with a flux source. However, flux sources (for example an inductor) are very hard to include efficiently on a chip, especially if large amounts of flux are needed. Furthermore there is no physical relation between the stimulation of the tissue and flux.



(a) Current steered (b) Voltage steered (c) Charge steered

Figure 3.1: Three fundamental output stage types

When making design choices however also other requirements are important, such as power consumption and area. The area needed by the charge steered stimulator largely depends on the size of the capacitor. Comparing the specifications of the BION stimulator (yielding $I_{max} = 25\,\text{mA}$ and $t_{max} = 500\,\mu\text{s}$) the maximum amount of charge injected during one cycle is $Q = It = 12.75\,\mu\text{C}$.

When assuming a maximum stimulation voltage of 12 V, the capacitor needs to be around 1 μF. Furthermore this capacitor needs to be able to handle relatively high voltages of 12 V. This means it will take up a lot of area in the chip design.

Also power consumption is not promising for the charge steered output stage. In [32] a charge, voltage and current steered output stage are compared in terms of efficiency. With an reported efficiency of 77% the charge steered output stage performs better than the current controlled (65%), but worse than the voltage steered (92%) output stage. Therefore it can be concluded that although the purely charge steered output stage is closest to the physical principles, it is inefficient to implement in terms of power and area.

The results of [32] confirm the statements made in chapter 2.2: current controlled output stages are hard to realize efficiently due to the complex implementation of accurate current sources. Therefore a stimulator using voltage sources is probably the most efficient solution. As was mentioned in chapter 2.2 as well, the drawback of voltage controlled stimulation is the lack of charge control, due to the variable impedance (which results in variable currents) of the tissue.

The solution to the problem presented above is to use voltage controlled stimulation in which the current injected in the tissue is sensed and integrated to keep track of the charge inject in the tissue. In this way the system has an efficient implementation because of the voltage source and charge cancellation is still assured because of the current integrator. Additional advantages of this system include:

- It is easy to change the waveform injected in the tissue: by varying the shape of the voltage source in principle every desired waveform can be injected in the tissue. This greatly improves the abilities of the system to fight tissue habituation. Note that this flexibility includes the possibilities of asymmetric waveforms, subthreshold prepulses, etc.

- The value of the voltage source doesn't need to be accurate. The exact shape of the voltage source is of no importance, only the total injected charge. Since this is controlled by the integrator, not much attention needs to be paid to designing a very accurate voltage source. This further improves power consumption and area.

- The absolute accuracy of the integrator is not important. Only the relative accuracy needs to be high: the charge of both phases need to be exactly the same. The exact amount of charge injected per phase does not need to be known very accurately. This is because of the large spread of required charge injection among patients. In each patient the electrodes are incorporated in the body in a different manner. This means the required charge for activation of the same area differs significantly per patient. Tuning the parameters is required to find the charge threshold which is enough for each particular patient. Therefore the exact amount of charge injected does not need to be accurately known as long as the relative amount of charge is controlled exactly for charge cancellation purposes.

The basic concept of this output stage is similar to the concept introduced in [24]. However the way the current injected is sensed and integrated is reconsidered in the next section.

3.1.1 Methods for sensing voltage and current

As described in the previous section, the basic idea of the implementation is to make it voltage steered, while the injected current is measured and fed back to the input to control the injected charge. In this section some fundamental architectures for this type of system are discussed. The emphasis will be on the implementation of the feedback loop(s) in the system.

A current feedback loop is necessary for the system to measure the charge injected in the tissue. A voltage feedback loop is optional: this loop can control the voltage over the tissue if the system is implemented in such a way that the input voltage source cannot control it in a direct way anymore. This means the system will comprise one or two feedback loops. These feedback loops can be implemented in two fundamental ways: in a direct or indirect way. The fundamental system architectures are summarized in table 3.1 and are discussed in the following sections.

Table 3.1: Fundamental system implementations

	Voltage feedback		
	Direct	Indirect	No voltage control
Direct Current feedback	1	2	3
Indirect current feedback	4	5	6

1: Direct current and voltage feedback
2: Direct current and indirect voltage feedback
3: Direct current feedback only
4: Indirect current and direct voltage feedback
5: Indirect current and voltage feedback
6: Indirect current feedback only

In a direct feedback implementation the quantity to be controlled is measured by using this quantity itself. This means that the feedback circuitry will load and influence this output quantity. The advantage however is in general the relatively simple implementation of a direct feedback network.

In an indirect feedback loop implementation the quantity to be controlled is measured using another quantity which is related to it. This quantity might be the result of physical laws (such as the magnetic field resulting from a current), but the relation can also be established by additional circuitry (e.g. make a copy of the output quantity). The advantage is that the output quantity itself remains untouched by the feedback network. However when for example a copy of the output quantity is made, this involves additional circuitry and most likely more power consumption (assuming the need for very accurate replicas).

Furthermore each type of feedback can be established in a passive and active way. In a passive implementation the process of bringing the desired quantity towards the feedback network does not use any active circuitry. Examples of direct and indirect feedback (both passive and active) are given in subsequent chapters.

Voltage feedback loops

Measuring a voltage in a *direct way* is probably the most straight forward way to feedback an electrical quantity. The voltage is simply 'tapped off' by two wires. Of course the system is loaded in this way, depending on the input impedance of the feedback loop. Furthermore the voltage might be floating if none of the terminals is connected to ground. This means that the common mode rejection of the feedback loop becomes important as well.

The principle is depicted in the left side of Figure 3.2. In some way this type of feedback can be considered as passive direct voltage feedback. When the feedback network would load the output quantity too much, an active implementation can be considered. Now the voltage is first copied using a buffer with a much higher input impedance.

In contrast to the straightforward direct implementation, an *indirect way* for voltage feedback loops is not very trivial. According to the definition for indirect feedback the voltage is measured using a related quantity. The original voltage is fed into the load, while the other quantity is used as an input of the feedback network. In this way the voltage at the load is not influenced by the feedback network. The principle is depicted in the right side of Figure 3.2.

A passive indirect voltage feedback network would consist of measuring a quantity related to the voltage without the need of actively generate this quantity. A theoretical option would be to measure the electrical field generated by the voltage. This would require some kind of an antenna. It is clear it's very hard to integrate this on a chip.

Indirect voltage feedback using active circuitry improves the feasibility of the circuit. One option is to copy the voltage to be measured. Now the related quantity is again a voltage. The

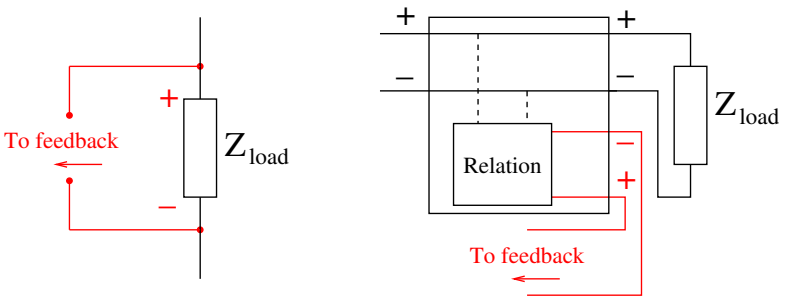


Figure 3.2: Principle of direct (left) and indirect (right) voltage feedback networks

output of the active circuit responsible for the copying consists of two voltages. The voltages are either equal or are a well defined fraction of each other. One of them is used for the load, while the other is fed back.

The voltage feedback for the stimulator system needs to control the voltage over the tissue. Using active circuitry a good copy can be obtained, however the additional circuitry will consume both power and chip area. Especially since the active circuitry will need High Voltage capabilities. Since power and area are two very important considerations and direct voltage feedback does not seem to pose any serious problems, the option with direct voltage feedback is preferred over indirect voltage feedback. Depending on the structure of the rest of the system, it needs to be decided if voltage feedback is necessary at all. Therefore at this point only solutions 2 and 5 from table 3.1 can be rejected.

Direct Current feedback loops

A current feedback loop is harder to implement than a voltage loop, because current sensors are not as straightforward as voltage sensors (simply tapping of the voltage using two wires). Sensing the current in a direct way involves inserting a device in the current path which senses the current. The principle is depicted in Figure 3.3.

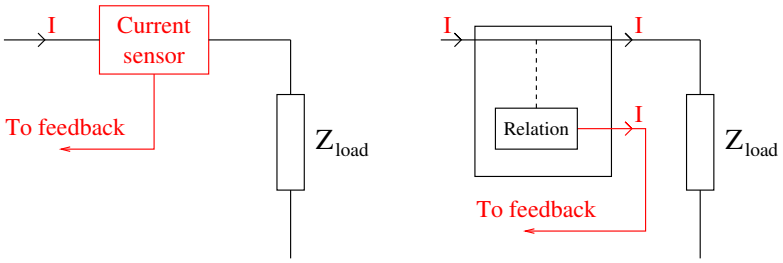


Figure 3.3: Principle of direct (left) and indirect (right) current feedback networks

First of all it is easily seen that the inserted device will introduce a voltage drop. This will influence the voltage across the load (in this system the tissue). When exciting with a voltage source this also influences the current injected into the tissue. As long as this influence is not very big, this does not yield too big problems: as was stated earlier the voltage over the tissue does not need to be very accurate. If required the voltage can be controlled with an additional voltage feedback loop. The current sensing device will however consume power.

It is assumed the tissue is always grounded. As can be seen in Figure 3.4 this leaves two possible implementations for the direct current feedback. When the integrator is placed at the negative terminal of the voltage source, the current sensor is grounded at one terminal. This makes it easy

to process the sensor signal. However, when multiple electrodes are connected to a single voltage source they have a common return potential (ground). This means that the individual electrode currents cannot be measured at this return potential. This means the current integrator cannot measure the individual charges injected, but instead only measures the cumulative charge. In this way, charge cancellation is not ensured, since electrode impedance variations can lead to charge imbalances in individual electrodes, while the cumulative charge is still balanced.

Another disadvantage of this placement is that a floating stimulation source is required. The implementation of this source is not straightforward. The voltage based stimulation was chosen because of its efficient and simple implementation. Having the need to implement a floating voltage stimulation source would therefore contradict one of the fundamental reasons to design this type of stimulator.

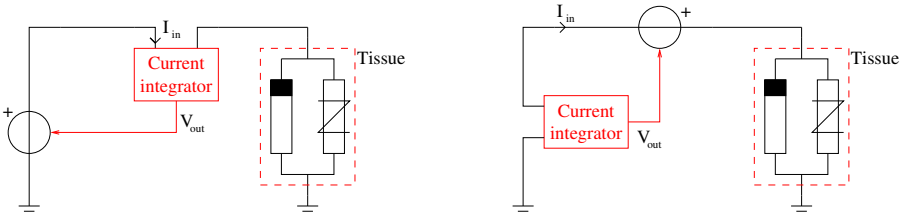


Figure 3.4: Two alternatives for a stimulator with direct current feedback

Therefore the sensor in a direct current feedback needs to be placed at the positive voltage source terminal. This will however require a floating sensor. First a couple of alternatives for the current sensing device are considered.

Passive solution: Sense resistor By placing a small resistor in series, the current through the resistor is related to the voltage over the resistor by means of Ohm's Law. This voltage is subsequently integrated, which then resembles the charged injected ($Q = R \int Idt = \int Udt$). The voltage over the sensing resistor can be easily fed back in a direct way as was explained in the previous section. The principle is depicted in Figure 3.5a.

Implementing the system with a sensing resistor is similar to the system described in [24]. Main advantage is the relatively easy implementation. Note that if the resistance spread in the technology is relatively big, this imposes no problems: the injected charge does not need to be accurate. Only the relative charge needs to be well controlled. Since the resistor value is constant, this is assured.

A disadvantage is the power dissipated by the resistor (as long as the resistor is not made small enough). In [24] a value of 200 Ω is chosen. If it is assumed the resistive part of the tissue impedance is about 1 kΩ (which is often considered as a standard value), the sensing resistor alone is dissipating 20% of the power which is used in the electrode to stimulate the tissue. This is not very efficient.

When choosing a smaller resistor value, the differential voltage of the resistor becomes smaller and because of the large common mode signal, it will be hard to design an accurate integrator. Note that the integrator needs a high common mode rejection. When it is not high enough, the integrator will be integrating a common mode signal, which will lead to a wrong charge value. This would be no problem if the common mode signal would be equal during the cathodic and anodic phase of the stimulator. However, to make the stimulator as flexible as possible, it is desired to change the shape of the stimulation signal during anodic and cathodic phase. When there is not enough common mode rejection, this will lead to charge mismatch errors.

Further disadvantages of the resistor includes noise. The noise injected in the tissue due to the resistor does not pose big problems, since the stimulation signal has a high amplitude. However, the noise imposed on the differential signal used by the integrator can pose problems if the differential signal has a low amplitude. All in all implementing the current sensor with a

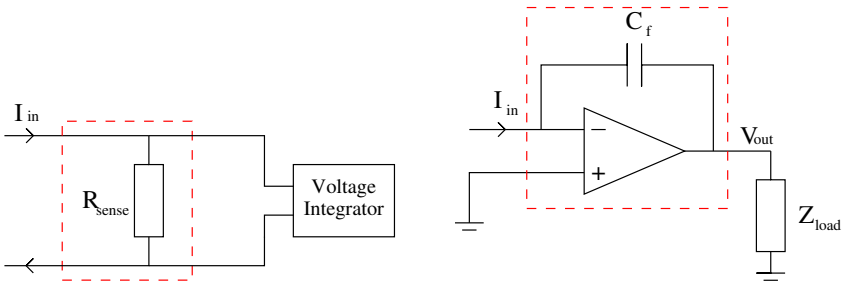
resistor poses some problems. Especially power consumption is a big issue.

Active solution: Current amplifier The main reason the resistor based solution consumes a lot of power is related to the fact that the relatively high stimulation current is flowing through a resistive component. Instead of using a passive device as a current sensor, an active implementation can be used. This will yield a current amplifier. The advantage of this implementation is that the input impedance of the amplifier can be made very small by means of for example a high loop gain. This means that the power consumption due to the stimulation current flowing through the device can be made very small.

Using an active circuit as the current sensing device however also leads to problems when looking at the implementation. Since the current needs to be integrated, the current amplifier can be implemented as an active current integrator directly. A basic implementation of a current integrator is given in Figure 3.5b. As can be seen from the figure, the feedback action only works properly if one of the input terminals of the integrator is grounded. However this is not possible in the direct current implementation, since the current sensing device needs to be floating as was stated before.

Another problem with the basic current integrator is that it is an inverting integrator. Therefore a negative voltage is built up over the capacitor. This means that the circuit will need a negative voltage supply as well or the capacitor needs to be precharged before every stimulation. A negative voltage will need to be generated separately, which will yield a significant increase in circuit area and power consumption. Precharging will mean that the capacitor needs to be charged with a certain amount of charge every single stimulation cycle. The charge required for this precharging will correspond to energy loss, yielding a higher power consumption.

Of course it is possible to design more elaborate implementations of the active integrator. Ideally a floating non inverting current integrator is needed. The design of such a device is however not straightforward. It will most likely lead to a significant increase in area and power consumption.



(a) Sense resistor

(b) Possible implementation of active current integrator

Figure 3.5: Implementation of direct current feedback systems

Summarizing it can be seen that direct current feedback introduces quite some problems for different kind of implementations of the current sensor. The two main disadvantages include:

- The sensor needs to be floating, which yields more complicated implementations and common mode issues.
- The sensor needs to handle the relatively large stimulation current directly. This means the power consumption of the sensor will be higher as well.

Indirect Current feedback loops

Having seen the problems related with a direct current feedback approach, the options 1, 2 and 3 from Table 3.1 are rejected as well. This means only options 4 and 6 remain. For these options,

the indirect current feedback approach is investigated. Measuring current in an indirect way involves relating the current to another quantity and using this quantity for the feedback system and therefore not using the current directly. The related quantity is then integrated to obtain the charge injected into the system. The principle is depicted in Figure 3.3 as well.

Advantage of this approach is that both currents can now be grounded, yielding no common mode problems and overcoming the problems associated with the implementation of the active current integrator. Furthermore the related quantity can be made much smaller then the stimulation current (but still an accurate fraction). Now the current sensor does not need to handle a big current anymore, which can decrease power consumption.

Disadvantage of the indirect current feedback includes the additional circuitry required for the generation or detection of the related quantity. This circuitry will consume chip area and power consumption. It will be seen however that this circuit can be very simple. In the following sections some ways to measure the current in an indirect way are treated.

Passive solution: current clamp A current clamp is a device which measures the magnetic field produced by the current through a wire. The principle is schematically depicted in Figure 3.6. The magnetic field is converted to a voltage, which can be integrated to obtain a measure for the charge injected. A current clamp does not introduce a voltage drop as is the case for the sense resistor (it is a non contact current measurement), but it does load the system: the magnetic field is influenced by the current clamp. The main drawback of a current clamp is that it is very hard to implement on a chip: it needs a coil around the wire through which the current is flowing to 'catch' the magnetic field. It therefore is not a realistic option.

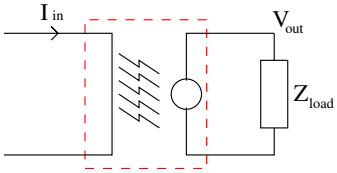


Figure 3.6: Passive indirect feedback: current clamp

Passive solution: transformer . A transformer uses the magnetic field of the tissue current to generate a second current with a well defined relation. A transformer creates a copy of the voltage and current from the input terminals at its output terminals. The way this component can be used in the stimulator system is depicted in Figure 3.7. Using the fuctionality of the transformer a low input current can be fed through the current sensor, while the high stimulation current is generated at the output terminals of the transformer. The drawback however is the realization of a transformer on a chip, especially for the low frequencies associated with stimulation. Furthermore, creating the high current at the output means a very high voltage at the input: nV_{tissue}. Since the tissue voltage is already quite high, the voltage at the input will be very high. Because of these two drawbacks it is not a realistic option.

Active solution: current conveyor . One way to actively generate a related quantity is to copy the current to be measured using an active circuit. The task of this current copier would be to let the stimulation current pass through, while a second current is generated which has a accurate relation with the stimulation current. This is exactly what happens inside a current conveyor. Since the current conveyor will be placed between the positive terminal of the voltage source and the tissue (just like the sense resistor is in the previous section), the input needs to be floating again.

Third generation Current Conveyors ([54]) have floating input capability. The principle of the CCIII in terms of nullators and norators is given in Figure 3.8. Its behavior can be described by

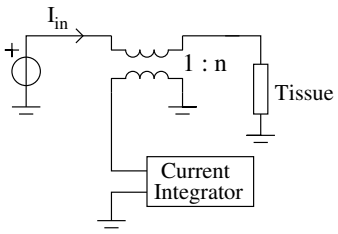


Figure 3.7: Using a transformer to generate the copy of the current

means of the following equation:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{3.1}$$

The input terminals (x and y) can be used as a floating input: the current flowing into x is equal to the current flowing out of y and the voltage difference between the two terminals is zero. Furthermore the third terminal z is producing a copy of the input current. However, when looking at the way the CCIII is producing the currents one can see this is inefficient: the input current i_x is grounded. Based on this grounded current the output currents are produced. This means that the grounded current is 'wasted' instead of put directly through to y.

Furthermore implementing the CCIII requires quite some circuitry as can be seen in for example [54]. Especially since this current conveyor needs to be able to handle high currents and voltages. It is therefore maybe not the most efficient way of generating a copy of the input signal.

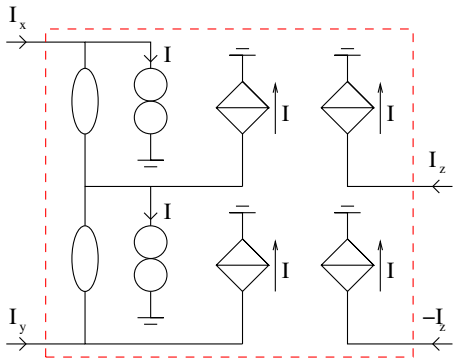


Figure 3.8: The principle of the third generation current conveyors

Active solution: v_{gs} copier . A current can be easily copied by means of a current mirror. The working principle is based on the fact that when the gate-source voltage of two transistors is kept the same, the drain current through both devices is equal (assuming both devices operate in saturation region and the channel length modulation effect can be ignored). By scaling the transistors in a certain way, an accurate fraction of the output current can be copied for feedback purposes. Main advantage of this network is the relatively easy implementation.

Current mirrors are usually used with a current as input (which is copied to the output). This current will generate a particular gate-source voltage, which is copied to a second transistor, which will then produce a similar current. The fundamental working principle is based around copying the gate-source voltage.

This principle is used in this particular application, where the input is voltage based. Two transistors are supplied with the same V_{gs}, which will result in two currents which are exact copies. When the transistor sizes are adjusted in a certain ratio, one current is an accurate fraction of the other. The principle is depicted in Figure 3.9. The large current is supplied to the tissue, while the smaller current is used for charge cancellation.

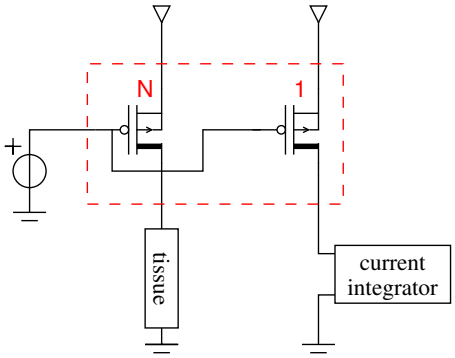


Figure 3.9: Using a current mirror to generate the copy of the current

Inaccuracy of the matching between the two transistors does not pose any problems: since the mismatch is constant, the mismatch in current is also constant. Although this will result in errors in the absolute value of the current, it does not result in relative errors. As long as the absolute error does not become extremely large, this does not pose any problems. Another advantage of this network is that the copied current, which is fed into the integrator can be very small. This can keep the power dissipation associated with the integrator relatively small.

Because the current through the tissue (and therefore the voltage over the tissue) is now controlled using a gate-source voltage, the input voltage does not correspond to the tissue voltage anymore (in fact: if the input voltage is chosen at the maximum value, the voltage over the tissue is zero, because the PMOS transistors are switched off). Therefore a voltage feedback loop is required to regulate the voltage over the tissue.

Using the indirect current feedback loop implemented with a current mirror the problems associated with the direct current feedback are overcome. The current integrator system is now grounded, yielding an easy implementation. Furthermore the current that needs to be integrated can be made small, which yields low power consumption of the integrator. Therefore option 4 is chosen from Table 3.1. In Figure 3.10 the complete diagram is depicted, including the voltage and charge control loops.

A drawback of this system is the limited support for multiple electrodes per channel. If an additional electrode is to be connected it cannot be simply parallel connected to the first electrode. Because of the time variant nature of the electrode impedance, not every electrode will get the same amount of current, which will lead to charge imbalance problems. Especially because of the highly non linear behavior of the tissue, it cannot be assumed that by using non symmetrical stimulation pulses the currents through the electrodes are a constant fraction of each other.

A solution is found in placing another 'N'-sized transistor in parallel with the additional electrode connected as depicted in Figure 3.11. Now the voltage of this additional electrodes cannot be controlled anymore, since this is already done for the first electrode. This means that the voltage over the additional electrode is not well defined. However, the current injected into the electrode is the same as the first electrode (because the gate-source voltages are equal). This also means that the charge injected into the additional electrode is equal. Since charge is the fundamental physical property the additional electrode can be still controlled in a proper way without the need of an additional integrator and stimulation voltage source. Depending on the variation in impedance, the stimulation waveform of an additional electrode might be very different, but the injected charge is equal. However, each additional electrode does require the

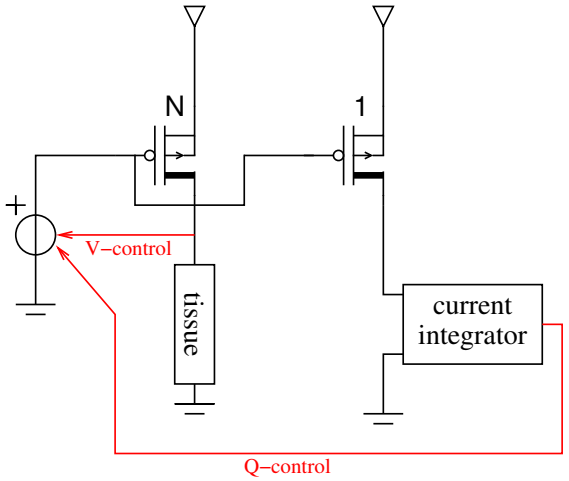


Figure 3.10: High level design of the output stage

relatively large transistor of size N, yielding more area consumption.

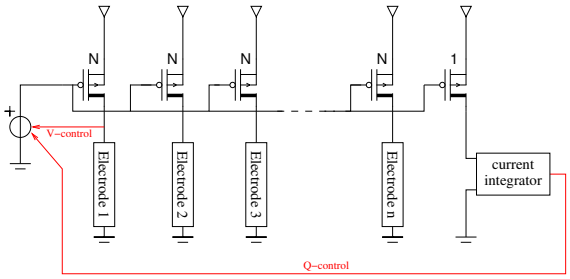


Figure 3.11: System configuration with multiple electrodes

Choosing for the indirect current feedback using the current mirror imposes important limitations on the power consumption of the system. The current used for integration purposes is not injected in the tissue and is therefore 'wasted' in terms of efficiency. This means that this system has the fundamental property that by choosing a certain N, a minimum efficiency is set:

$$\eta = \frac{N}{N+1} \tag{3.2}$$

By increasing N, the power efficiency will increase as well. However, increasing N will also increase area. This is a fundamental trade-off between power and area for this circuit. Depending on the area available and the size of the power transistors, a choice will need to be made.

3.1.2 System blocks definition

Now that the basic structure of the system is defined as depicted in Figure 3.10, it is possible to define some more high level system blocks. In this way the design process is simplified by subdividing the large system into smaller blocks which can be designed more or less independently from each other. First of all the two control loops can be made explicit using system blocks.

The voltage loop will be generating the gate voltage of the driver transistors based on the input voltage and the tissue voltage (the difference between these two must be brought towards zero). This means this block has two inputs and one output.

The charge loop needs some more attention. The integrator will keep track of the integrated charge and at some point a certain threshold will be reached. At this point the stimulation must stop. The question is how to stop the stimulation effectively. Making the stimulation voltage zero is not sufficient: due to the stimulation the tissue is charged to a certain voltage and by making the stimulation source zero subsequently, a discharge process will start: current will flow 'back' through the low impedance voltage source. Stopping the stimulation means no current is able to flow into the tissue. This can be accomplished by placing a switch between the driver and the tissue. However it's still possible for current to flow into the integrator then, destroying the matched conditions of the indirect feedback. Introducing yet another switch in the integrator path might solve this, but this implementation is becoming unnecessary complicated and is also vulnerable to mismatches between the two switches.

The problem can be solved more efficiently by forcing the gate-source voltage of the two driving transistors towards zero. In this way using only one switch, both driving transistors are switched off and stimulation is guaranteed to stop. In this way the charge feedback network is implemented in an efficient and easy way.

More blocks are needed. It needs to be decided in what way the anodic and cathodic phase are generated. Like most current based stimulators this can be done by including a second (negative) stimulation source. This means that using the chosen stimulation scheme a second scheme is needed which is connected to a negative voltage supply. Each of the two systems is active during one phase, making it possible to stimulate with both positive and negative voltages. However, this scheme is very inefficient. First of all, the stimulation scheme is almost doubled in area. Furthermore mismatches between these two systems in terms of the integrators (if it is chosen to copy the integrator as well) will result in charge mismatches. Finally there is a need of a negative voltage. This is not available from a battery and therefore will need to be generated separately, yielding additional circuitry or an additional battery.

Another option is to change the direction of the stimulation current using a switch array. The structure of this array is depicted in Figure 3.13 using switches S_1-S_4. The advantage is that only one stimulation source is required. This means the issues concerning mismatches during the two stimulation cycli are overcome, because the same integrator can be used during both phases (the current through the integrator is not reversed). Drawback compared to the other option is that each individual electrode needs two wires. When using the two source approach, multiple electrodes can share the same return wire. This reduces the impact on the body. However, for a brain stimulator most likely a limited amount of electrodes is required for stimulation purposes. Furthermore the advantage of the significant area reduction is considered more important.

Yet another block is to be defined if a closer look is taken to the integrator. The integrator actually is part of a bigger system block which is responsible for keeping track of the injected charge. This 'charge cancellation' block consists first of an integrator, but also a part which is responsible for the charge threshold detection. When the right amount of charge is injected, this circuit will be triggered in order to for example trigger the switch to stop stimulation.

The complete system in terms of system blocks is now presented in Figure 3.12. Note that using colors a distinction is made between the high and low voltage parts of the system. The tissue will need to be stimulated using a high voltage (<20V) in order to bring the tissue towards the activation threshold. Only the driving transistors and some switches need to have high voltage capabilities. The charge cancellation part can be limited to a lower supply voltage. This will significantly decrease power consumption and area.

However, at each interface between low and high voltages a level shifter is required. This is particularly important for the interface between the charge threshold detector and the stimulation enable switch. Here the voltage needs to be shifted up from the low voltage supply towards the high voltage. Therefore an additional block is included here: a level shifter.

Furthermore note that the stimulation voltage source is chosen to be low voltage as well. This means that in the feedback path from the tissue a voltage attenuator is required. Although the implementation of the stimulation source is outside the scope of this project, it is discussed shortly here. As presented before, the stimulation source needs to be as flexible in terms of waveforms as possible. One possible implementation with a lot of flexibility is a DAC. Using a bit pattern

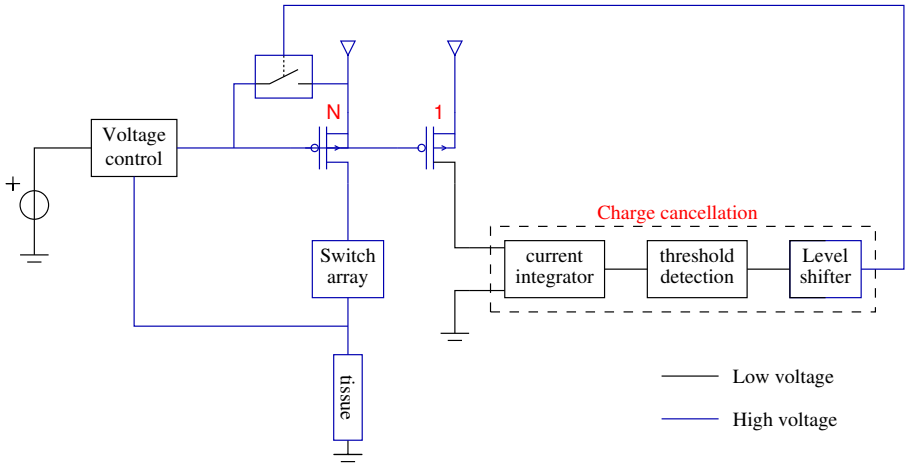


Figure 3.12: Block scheme of the output stage

the tissue can then be stimulated using any waveform shape (including burst stimulation, sub-threshold prepulses, etc). When implementing this DAC it's in terms of power consumption very beneficial using the low voltage supply voltage. That's why this source is considered low voltage in this design.

Having defined the overall scheme now, it is good to refer back to table 2.1 in which several design parameters of the output stage were discussed. The following parameters were chosen:

- Output quantity: Voltage
- Pulse shape control: Not included in this design. It's still considered as an ideal low voltage source.
- Charge cancellation: Charge metering
- Pulse parameter adjustability: all possible parameters can be adjusted by modifying the ideal low voltage source. Depending on its final implementation this might reduce the adjustability, but this is not included in this project.
- Number of outputs: Number of channels and electrodes can in principle be arbitrary. However, it's in terms of area not very efficient including an additional electrode in a channel, since the large N-sized driver transistor needs to be copied. The electrode arrangement is not discussed in this project.
  The chosen system structure is inherently a push stimulation: the voltage source is placed at the positive electrode and there is no source on the negative terminal.

As can be seen the focus during the design has been put on the flexibility of the waveform. This design has consequently a very high adjustability, which is beneficial for tissue habituation. Charge cancellation is still ensured due to the charge metering. Disadvantage is the limited number of electrodes which this system can support without occupying significant chip area.

3.1.3 System level simulations

To verify the correct functionality of the overall system, some high level simulations are done. The most important functionality to verify is the ability to achieve charge cancellation with the voltage based stimulation in combination with the high flexibility in waveforms. Using a simple (Pspice based) simulator, a basic circuit was implemented, as shown in Figure 3.13. Since the goal is to prove the system concept, only ideal components were used.

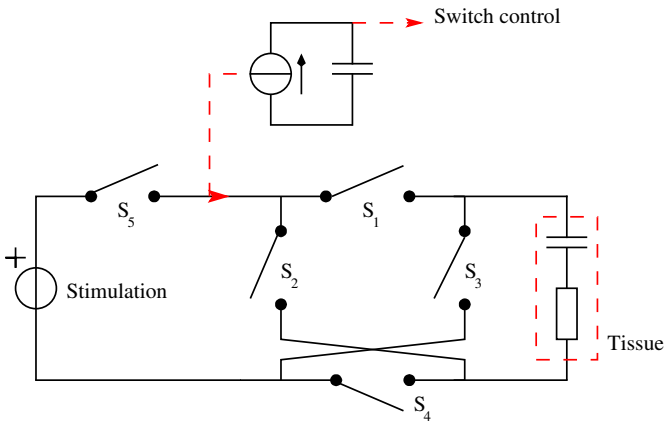


Figure 3.13: Simplified ideal circuit representing voltage based stimulation with charge cancellation

Note that in this figure the circuitry responsible for controlling the switches has been omitted for the sake of clarity. During the first stimulation phase Switches S_1 and S_4 are open, while in the second phase only S_2 and S_3 are open. When the output of the integrator reaches a certain threshold value, switch S_5 is opened, in order to stop the stimulation. Another thing to notice is that no explicit use of indirect current feedback is used here. Instead a more ideal situation using an ideal current controlled current source is used to measure the current.

The tissue is modeled using a combination of a capacitor and a resistor. In Section 3.2 more attention is given to the modelling of the tissue. For now it's enough to know that the combination of a resistor and capacitor can represent the response of the tissue accurately enough in most cases.

First a stimulation using a square shaped waveform is used. The result is depicted in Figure 3.14. As can been seen a voltage of 10 V is used to stimulate the tissue. After the first stimulation phase the tissue is charged up to approximately 4.5 V. After the second phase the voltage of the tissue is reduced again to 0 V, meaning charge balance is achieved.

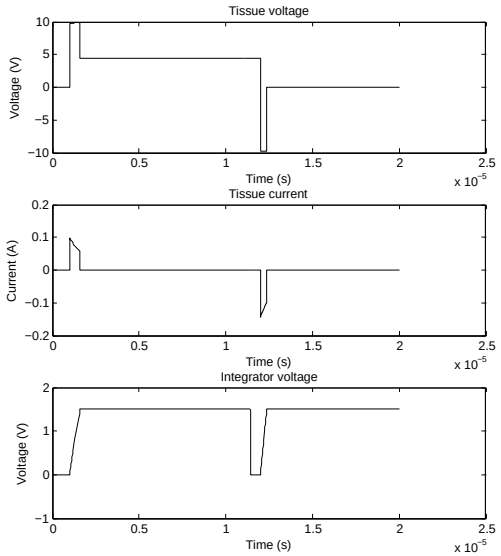


Figure 3.14: Square waveform stimulation

As expected from the tissue consisting of a capacitor and resistor, the current response has

an exponential decaying nature, as can be seen in the second subplot. It can also been seen the current during the second phase is higher than during the first phase. This is because of the fact the tissue is charged to 4.5 V at that point, yielding a total voltage difference of 14.5 V. This also explains why the second phase is much shorter than the first phase.

In the lowest subplot, the voltage over the capacitor (the integrator) is depicted. As can be seen the shape of the integrated voltage is exponential, corresponding to the current. The threshold voltage was chosen to be 1.5 V, explaining the fact why integration stops at the voltage. At 12 μs the voltage over the capacitor is reset to zero again, to make it possible to integrate the current during the second phase again.

To show the flexibility of the circuit two other stimulation waveforms are chosen. First a sinusoidal waveform is applied in Figure 3.15. An offset voltage of 7 V is added to a sinusoidal with an amplitude of 3 V. As can be seen, the current now becomes an exponential decaying sinusoid. Thanks to the integrator however, charge balancing is still achieved. For the same reasons as with the square waveform, the second phase results in a higher current and therefore smaller pulse width.

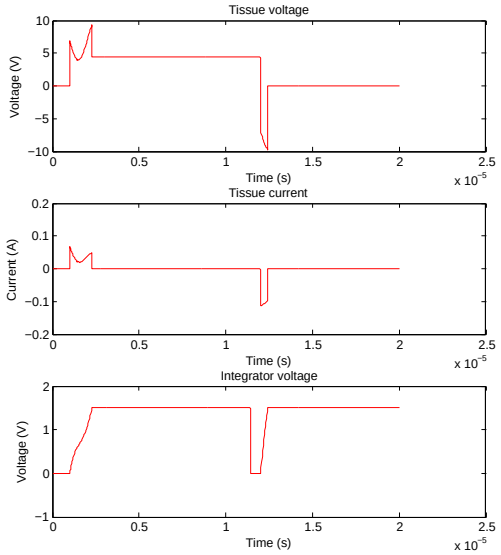


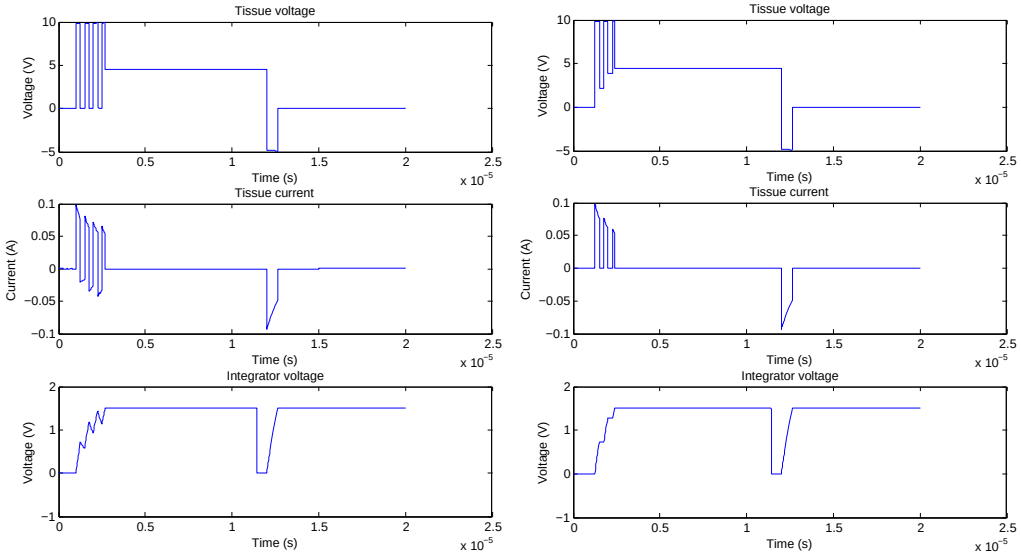
Figure 3.15: Sinusoidial waveform stimulation

Finally also a burst stimulation is applied: a pulse train. The voltage is switched between 0 and 10 V. As can be seen in Figure 3.16(a), the tissue is now charged with steps up to the threshold voltage. It can also be seen that when the voltage is 0 V, the tissue discharges. This is because the stimulation voltage is than lower than the voltage of the tissue. This means the tissue will discharge through the (low impedance) voltage source. Note that in practice this situation will not occur, since the driver transistors are high impedance, when the input voltage is set at 0 V.

In principle however the discharging does not matter for the stimulation purposes: the charging process is much faster (since the voltage of 10 V is much higher than the voltage of the tissue), which makes sure the tissue is still charged towards its threshold voltage. Furthermore charge balancing is still achieved. When the tissue is discharging a bit, the integrator still works fine (by decreasing its output). In the second phase a constant voltage instead of a pulse is applied. This is not necessary: a pulse train would work as well.

The simulation can be changed a bit to remove the discharging in between the burst pulses. The pulses can be generated alternatively by making a constant stimulation voltage and toggling switch S_5 on and off. In this case the stimulation is stopped, instead of forcing it to 0 V. As can be seen in Figure 3.16(b), the current is now on and off alternately. Again charge balancing is

achieved.



(a) Discharge in between burst pulses

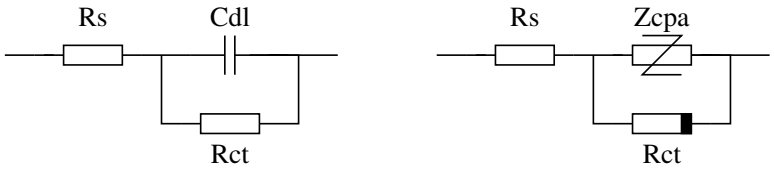
(b) No discharge

Figure 3.16: Pulsetrain waveform stimulation

The simulations above show that the chosen system architecture can indeed provide the safety and flexibility which is required. The implementation of for example the indirect current feedback will most likely introduce complications and or limitations, but this is not fundamental for the chosen architecture.

3.2 Current response of the tissue

The tissue will be stimulated with a certain voltage based waveform. As a result of this voltage, a certain current will flow into the tissue (and the same scaled current into the charge cancellation scheme). Important for the design of almost any system block is the shape of this current waveform. In order to predict the waveform of the current as function of a certain voltage applied to the tissue, the model for the tissue obtained in chapter 1.4 is analyzed when it is excited with a voltage source. For convenience the two most widely used models are depicted again in Figure 3.17.



(a) Linear model

(b) Nonlinear model

Figure 3.17: Two commonly used interface models (copied from chapter 1.4)

Extensive research has been done in analyzing both models when excited with current sources ([26], [50]). However, research about the case when excited with a voltage source is limited. The linear model is easy to analyse using any circuit simulator. However, the non linear model is much harder to analyse. Therefore this needs special attention.

3.2.1 Current response of the nonlinear interface model

Taking a closer look at the non linear interface model, a fundamental problem is discovered. The Charge Transfer resistance R_{ct} is a highly non linear component, characterised with an exponential relationship. The constant phase impedance Z_{cpa} however is a linear component described in the Laplace domain. The relations of both components are repeated here:

$$Z_{cpa} = \frac{1}{(j\omega C_{dl})^{\beta}} \qquad J_{R_{ct}} = J_0 \left[\exp\left(\frac{(1-\alpha)nF\eta}{RT} \right) - \exp\left(\frac{-\alpha nF\eta}{RT} \right) \right] \tag{3.3}$$

The combination of these two components leads to a problem finding any closed form expression for these components: the Laplace description of Z_{cpa} is *only* valid in a linear system.

One solution would be to solve the system using numerical methods. A closed form expression for Z_{cpa} needs to be found in the time domain. Because all components are then described in the same domain, numerical methods will be able to find the response of the system. In this derivation another approach is chosen. When the value of R_{ct} is assumed to be constant (and thus linear), the whole system can be described in the Laplace domain. Using the inverse Laplace transform the time response of the system can be found. This approach is used in many references in literature (for example [26] and [50]), however there only one fixed value for R_{ct} is used, although this is not explicitly mentioned. In reality however, R_{ct} is constantly changing as function of the voltage over the component. Furthermore in these references it is not mentioned that it is not correct to use non linear components in the Laplace domain.

In this work the system is described in the Laplace domain and then evaluated for multiple values of R_{ct}. The transient response is then a combination of these multiple linear responses. To keep things simple it was decided to limit the derivation of the circuit to the case of which the tissue is excited with a Heaviside step function: $V_{in} = V_{dc}\epsilon(t)$. In the subsequent sections the derivation for a couple of cases is described.

$i(t)$ **for** $t = 0$

For $t = 0$ the Heaviside step function changes from 0 to V_{dc}. However, the nature of Z_{cpa} is capacitive. This means that the voltage over this component will not change abruptly. Therefore it can be assumed at $t = 0$ the value of R_{ct} can be found assuming the voltage over this component is 0 V. Therefore the current at $t = 0$ is determined only by the value of R_s:

$$i(t=0) = \frac{V_{dc}}{R_s} \tag{3.4}$$

Right after $t = 0$ the voltage over Z_{cpa} and R_{ct} will start to increase. The rate at which the voltage will change depends on the value of all three components of the model. For $t \approx 0$ the value of R_{ct} can be assumed linear (as was explained before in section 1.4) according to:

$$R_{ct,0} = \frac{1}{nfI_0} \tag{3.5}$$

$i(t)$ **for** $t = \infty$

In case of a step function all transients will be attenuated for $t \to \infty$. This means the tissue is only excited with a DC signal. For DC the impedance of Z_{cpa} is infinity ($Z_{cpa} \to \infty$ for $\omega \to 0$). This means the tissue model only consists of the series resistance and the charge transfer resistance. The goal is now to find the current through these two components as a function of a DC voltage over both components. It holds:

$$V_{dc} = V_{R_s} + V_{R_{ct}} = I_{dc}R_s + V_{R_{ct}} \tag{3.6}$$

Because of the nonlinear relation of R_{ct} the voltage $V_{R_{ct}}$ needs to be found first:

$$V_{R_{ct}} = V_{dc} - I_{dc}R_s \tag{3.7}$$

To find an expression for I_{dc} a new parameter is introduced:

$$w = R_s(1-\alpha)nfI_{dc} \qquad \rightarrow \qquad w\exp(w) = R_s(1-\alpha)nfI_{dc}\exp\left(R_s(1-\alpha)nfI_{dc}\right) \tag{3.8}$$

The first I_{dc} in the equation is now replaced by the simplification in Equation 1.27: $I_{dc} = \exp\left((1-\alpha)nfV_{R_{ct}}\right)$, assuming the step voltage is large enough for this approximation to be valid. After rearranging terms, the expression becomes:

$$w\exp(w) = R_s(1-\alpha)nf\exp\left((1-\alpha)nfV_{dc}\right) \tag{3.9}$$

Now the Lambert 'W' function is used. This function is defined as:

$$x = w\exp(w) \rightarrow W[x] = w \tag{3.10}$$

Applying this to Equation 3.9 it is found:

$$w = R_s(1-\alpha)nfI_{dc} = W\left[R_s(1-\alpha)nf\exp\left((1-\alpha)nfV_{dc}\right)\right] \tag{3.11}$$

This lead to the expression for the current:

$$I_{dc} = \frac{W\left[R_s(1-\alpha)nf\exp\left((1-\alpha)nfV_{dc}\right)\right]}{R_s(1-\alpha)nf} \tag{3.12}$$

The Lambert function can be easily evaluated using Matlab. At this point the value of $i(t)$ for $t \rightarrow \infty$ is known.

$i(t)$ for $0 < t < \infty$

From the last two sections the initial and final values for the current were obtained. The reason this was possible is because for both situations the value system reduces to a linear system (in the case for $t = \infty$ the current was calculated, from which the (constant) R_{ct} can follow easily). In between $t = 0$ and $t = \infty$ the system is not linear, since the value of R_{ct} will change constantly. As explained before the system will now be analyzed assuming R_{ct} to be linear (and thus constant). The values of $R_{ct,0}$ and $R_{ct,\infty}$ found in the previous sections, will both be used to find two different responses of the system.

Laplace domain representation The response of the system can be described by the combination of R_s, Z_{cpa} and R_{ct} in the Laplace domain, since R_{ct} is assumed to be linear now. It holds:

$$I(s) = V_{in}(s)Y_{tissue}(s) = \frac{V_{in}}{s}\left[\frac{1}{R_s}||\left(Y_{cpa} + \frac{1}{R_{ct}}\right)\right] \tag{3.13}$$

Here the Heaviside step function is transformed to the Laplace domain. Furthermore $Y_{cpa} = Z_{cpa}^{-1}$ is the admittance of the constant phase impedance. First an expression is obtained for the admittance of the tissue (without the input signal). Rearranging terms leads to the following expression:

$$Y_{tissue}(s) = \frac{1 + R_{ct}Y_{cpa}}{R_s + R_{ct} + R_sR_{ct}Y_{cpa}} \tag{3.14}$$

In order to find the inverse Laplace transform, the equation is converted to partial fraction form. Therefore both the nominator and denominator are multiplied with $(R_{ct} + R_s)$, and then divided by $R_{ct}Y_{cpa}$:

$$Y_{tissue}(s) = \frac{(R_{ct}+R_s)(1+R_{ct}Y_{cpa})}{(R_s+R_{ct})^2 + R_sR_{ct}Y_{cpa}(R_{ct}+R_s)} = \frac{R_{ct} + R_s\left(1 + \frac{R_s+R_{ct}}{R_{ct}R_sY_{cpa}}\right)}{R_s\left(R_s+R_{ct}\right) + \frac{(R_s+R_{ct})^2}{R_{ct}Y_{cpa}}} \tag{3.15}$$

Now the equation can be put into partial fraction form:

$$Y_{tissue}(s) = \frac{1}{R_s + R_{ct}} + \frac{R_{ct}}{R_s\left(R_s + R_{ct}\right)\left(1 + \frac{R_s + R_{ct}}{R_{ct}R_s Y_{cpa}}\right)} \tag{3.16}$$

Substituting the equation $Y_{cpa} = K^{-1}s^{\beta}$ into this equation leads to:

$$Y_{tissue}(s) = \frac{1}{R_s + R_{ct}} + \frac{R_{ct}}{R_s\left(R_s + R_{ct}\right)\left(1 + \frac{(R_s + R_{ct})K}{R_{ct}R_s s^{\beta}}\right)} \tag{3.17}$$

Similar as in [26] a parameter is introduced:

$$T = \left[\frac{\left(R_s + R_{ct}\right)K}{R_{ct}R_s}\right]^{-1/\beta} \tag{3.18}$$

Substituting this into the equation finally leads to the following expression for the admittance of the tissue:

$$Y_{tissue}(s) = \frac{1}{R_s + R_{ct}} + \frac{R_{ct}}{R_s\left(R_s + R_{ct}\right)\left(1 + (Ts)^{-\beta}\right)} \tag{3.19}$$

Substituting this into equation 3.13 leads to the following:

$$I(s) = \frac{V_{in}}{s}Y_{tissue}(s) = \frac{V_{dc}}{s\left(R_s + R_{ct}\right)} + \frac{V_{dc}R_{ct}}{R_s\left(R_s + R_{ct}\right)s\left(1 + (Ts)^{-\beta}\right)} \tag{3.20}$$

Introducing now the function $F(s)$:

$$F(s) = \frac{1}{s\left(1 + s^{-\beta}\right)} \tag{3.21}$$

Substituting this into the equation leads to the expression for the system response in the Laplace domain:

$$I(s) = \frac{V_{dc}}{s\left(R_s + R_{ct}\right)} + \frac{V_{dc}R_{ct}}{R_s\left(R_s + R_{ct}\right)}TF(Ts) \tag{3.22}$$

General time domain representation The Laplace domain expression obtained in the previous section can now be transformed back to the time domain, assuming the value of R_{ct} is linear. Therefore the following Laplace transform rule is used:

$$\mathcal{L}^{-1}\left[\frac{1}{T}F\left(\frac{s}{T}\right)\right] = f(Tt) \tag{3.23}$$

Applying this to equation 3.22, the following equation results:

$$i(t) = \frac{V_{dc}\epsilon(t)}{R_s + R_{ct}} + \frac{V_{dc}R_{ct}}{R_s\left(R_s + R_{ct}\right)}f(\bar{t}) \qquad \bar{t} = \frac{t}{T} \tag{3.24}$$

Now a closed form expression for $f(\bar{t})$ needs to be obtained. Because of the complex mathematical operations related to this derivation, it was chosen to use the values from a table in [26]. In this table the values for $f(t)$ are given for several values of β. The interested reader is referred to [26] for a description of the mathematical derivation of $f(t)$.

In Figure 3.18 a plot is given of $f(t)$ for several values of β. The timescale here is the normalized time $\bar{t}$ as described in equation 3.24. As can be seen, the higher the β, the steeper the slope of the function becomes. This makes sense: high β means the component is more close to capacitive behavior, while low β makes the component closer to resistive behaviour (which would mean no slope at all).

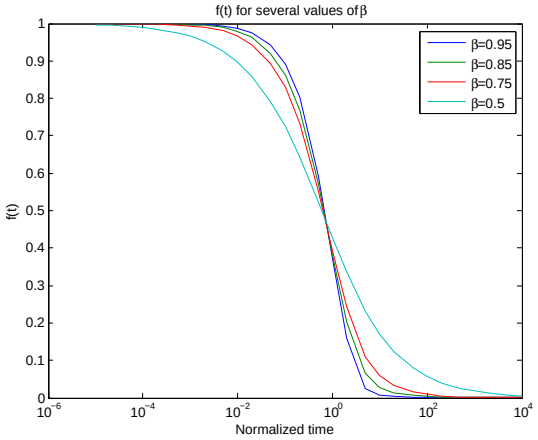


Figure 3.18: Plots of $f(t)$ for several values of β

Table 3.2: Numerical values of the model parameters

Parameter	Value	Unit
V_{dc}	1	V
R_s	1	kΩ
I_0	12.8	nA
K	22	$\text{k}\Omega\text{s}^{-\beta}$
β	0.75	
n	2	
α	0.5	

Examples of system response

Now that an expression for the time domain response of the system to a voltage step function has been obtained in equation 3.24, the system response can be obtained. As explained before the value for R_{ct} needs to be fixed in order to make the system linear. It is now chosen to evaluate the system for both $R_{ct,0}$ and $R_{ct,\infty}$, which both follow directly from the analysis of the system at $t = 0$ and $t = \infty$. Having obtained these two curves, the actual response of the system must begin with the curve for $R_{ct,0}$ and end with the curve for $R_{ct,\infty}$. In between the response is estimated by means of interpolation between these two curves.

First equation 3.24 is implemented in Matlab. To evaluate the model numerical values for the parameters are needed. However, to the best knowledge of the author, these values are not reported frequently in literature. It was chosen to take values used in [50] as a starting point. These values are summarized in table 3.2.

Using this values, the curves for $R_{ct,0}$ and $R_{ct,\infty}$ can be plotted, together with the computed values for $t = 0$ and $t = \infty$. The result is depicted in Figure 3.19. As can be seen the curve for $R_{ct,0}$ starts at $i(t = 0)$ and the curve for $R_{ct,\infty}$ ends at $i(t = \infty)$, just as expected. Note however that the time scale of this figure is still the normalized time. Since both curves use different values for R_{ct} ($R_{ct,0} = 0.976\,\text{M}\Omega$ and $R_{ct,\infty} = 377\,\Omega$) the values for T are different as well.

Hence, the next step is to denormalize the time scale and then interpolate both curves into the resulting curve. This is done by multiplying both timescales with their respective T. Next step is to choose two points at both curves in between which the interpolation takes place. For the sake of simplicity it is chosen to use linear interpolation and the two points are simply chosen by visual inspection of both curves. The result is depicted in Figure 3.20. As can be seen, due to

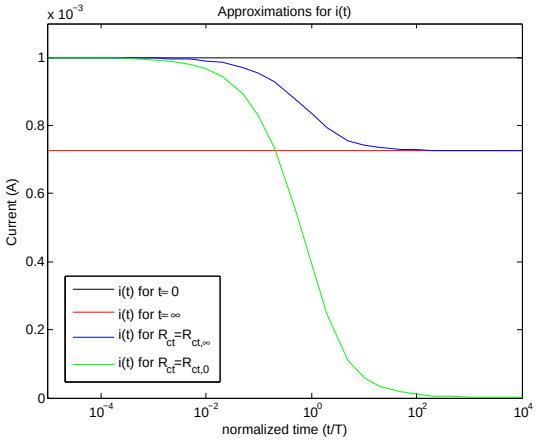


Figure 3.19: Plots of approximations $i(t)$ for several values of R_{ct}

the denormalized time scale, both curves are much closer to each other.

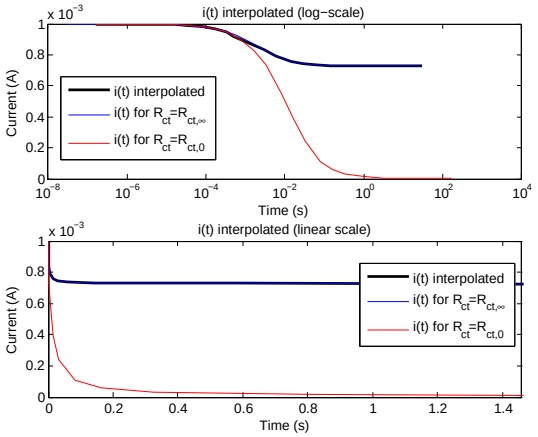


Figure 3.20: Plot of the interpolated step response with denormalized time scale

3.2.2 Compare with the simple model

Having found the transient response to a voltage step function, conclusions can be made about the waveform resulting from a particular stimulation pattern. This can subsequently determine the specifications of the integrator. However, due to the complicated nature of the model, it is not easy to find the resulting transient response for any possible waveform: analysis using the strategy described above is limited to step functions and furthermore the interpolation technique is not 'automated': the point at which interpolation takes place, needs to be set by hand.

Therefore, it is investigated first how much the response of the much simpler network (the left one in Figure 3.17) deviates from the response of the complicated network. The response of the linear network can be easily found using Matlab. For the component values in this model the following values were chosen:

C_{dl} This component is related to $Z_{cpa} = Ks^{-\beta}$. Because $Z_c = (C_{dl}s)^{-1}$, it is natural to make

$C_{dl} = K^{-1}$.

R_{ct} In the nonlinear model, the maximum and minimum values for R_{ct} were obtained: the one at $t = 0$ or the one at $t = \infty$. The worst case for the linear model is equivalent to $R_{ct,\infty}$, the lowest value. This value corresponds to the smallest time constant, which will result in the highest frequency response. The value has no influence on the maximum current. Therefore the value of $R_{ct,\infty}$ is chosen for R_{ct}.

R_s This component is the same as the component in the non linear model and is therefore chosen to be the same.

Now the response of the linear and non-linear model can be plotted in one figure, both in the time and frequency domain. To obtain plot of the frequency spectrum for the non linear model, it was necessary to make the time scale linear. Because of the combination of two denormalized curves, the time scale is non uniform. It was made uniform using linear interpolation. The spectrum is found using the fft transform. One of the properties of the fft transform is that the input signal is assumed to be the period of an infinitely periodic signal. Therefore at $t = 0^-$ a zero was added to account for the step in the transient response at $t = 0$.

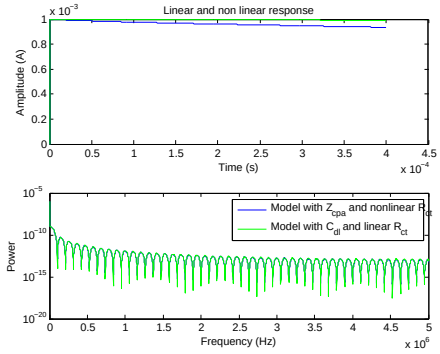
The results are plotted in Figure 3.21a. For this plot the same parameters as given in table 3.2 are used. Furthermore it was chosen to plot the time response in the interval $0 \leq t \leq 0.4$ms. Longer intervals were investigated as well, but proved not to produce significant differences and are omitted in this report for the sake of clarity.

The step at $t = 0$ can be clearly seen in the plot. From the plot it becomes obvious that both the time and frequency contents of the transient response are very similar for the non linear and the linear model. In Figures 3.21b-d some of the parameters of the model are varied. As can be seen this can have some more influence on the time signal, which is the clearest in case of a change in β in Figure 3.21b.

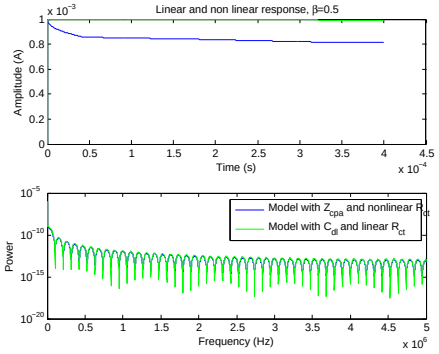
The question is now if the differences in transient responses are big enough to make it necessary to use the complicated non linear model instead of the simpler linear model. Two very important aspects for the design of the various blocks include the maximum peak current and the frequency contents of the current. The maximum current is determined by the value of R_s, which is the same for both models. As can be seen in Figure 3.21, the frequency contents of both signals are very similar for different model parameters.

Therefore the simple model is sufficient to simulate the current response of the tissue as a function of the voltage stimulus. This makes it easy to simulate the system in any circuit simulator, since it only comprises linear standard components. The exact current response however depends largely on the value of the resistors and capacitor, which are subject to large spread. Therefore the system should be ale to handle a large variety of combinations of resistors and capacitors.

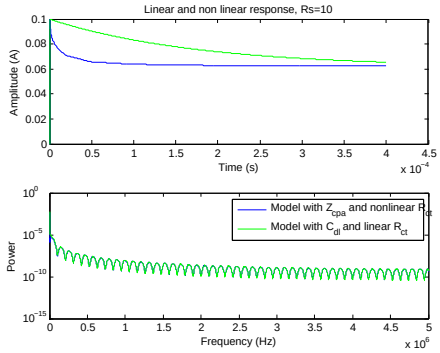
In the next sections the design of the various system blocks visualized in Figure 3.12 is treated. In the various subsections some design alternatives for each block are discussed and one of these is selected for implementation.



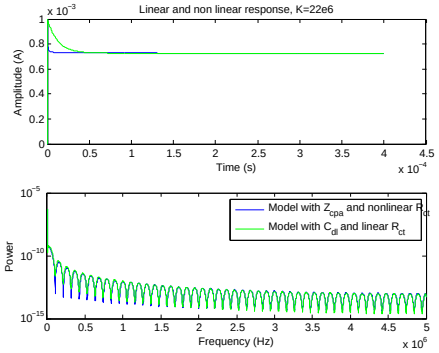
(a) $\beta = 0.75,\ R_s = 1\,\mathrm{k\Omega},\ K = 22\,\mathrm{k\Omega s}^{\beta}$



(b) $\beta = 0.5,\ R_s = 1\,\mathrm{k\Omega},\ K = 22\,\mathrm{k\Omega s}^{\beta}$



(c) $\beta = 0.75,\ R_s = 10\,\Omega,\ K = 22\,\mathrm{k\Omega s}^{\beta}$



(d) $\beta = 0.75,\ R_s = 1\,\mathrm{k\Omega},\ K = 22\,\mathrm{M\Omega s}^{\beta}$

Figure 3.21: Comparison between the linear and non linear model transient responses for different model parameters based on Table 3.2

Chapter 4

Design of the system blocks

In this chapter the design of the various system blocks defined in chapter 3 and visualized in Figure 3.12 is treated. In the various subsections some design alternatives for each block are discussed and one of them is chosen to implement. In the next chapter the performance of the various system blocks is verified using simulations. Although it has been tried to postpone as much discussion based on simulation results to the next chapter, in some cases it was more clear to include simulation results in this chapter already. The blocks to be discussed are subsequently:

- Stimulation enable switch
- Level shifter
- Driver
- Voltage control feedback
- Integrator
- Switch array

4.1 Stimulation enable switch

This switch is used to disable the stimulation when this is required. Either because the charge threshold is reached or because no stimulation is necessary at all. To stop stimulation, the gate and source of the driver transistors are shorted. This switches off the driver transistors, guaranteeing no stimulation current is fed into the tissue.

The tissue is stimulated using driver transistors as depicted in Figure 3.12. The transistors are also depicted in Figure 4.1. When stimulation needs to be stopped, the driver transistors need to be disabled. This means the gate voltage of these transistors need to be charged towards the high voltage supply voltage.

The simplest implementation for this functionality is a switch using a single transistor. This means the switch will need to pull the gate voltage up, yielding a PMOS transistor as the proper implementation. The implementation using only one PMOS transistor is depicted in Figure 4.1. Since the gate voltage of the driver transistors is limited to about $V_{dd} - 3\text{V}$ (in order not to exceed the gate source breakdown voltage), the voltage differences on the terminals of the switch do not exceed 3 V anywhere.

This means it is not necessary to use a transistor with high voltage capabilities to do the job. It is only necessary to isolate a normal transistor sufficiently from the gnd voltage, which is possible in the I3T80 technology. The voltage V_{switch} must switch between $V_{dd,high}$ and $V_{dd,high} - 3$ to turn stimulation on and off respectively.

Whether this single transistor implementation is good enough will need to be determined later, when other system blocks are designed. First of all the switch needs to be strong enough to pull up

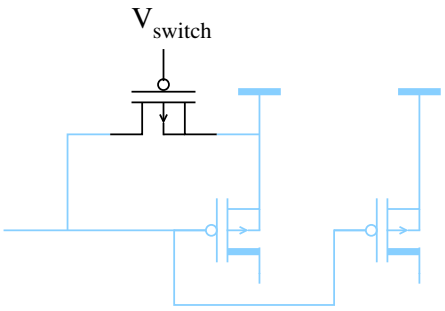


Figure 4.1: Single transistor implementation of the Stimulation enable switch

the gate voltage fast enough to switch off stimulation fast enough. This can be assured by making the transistor wider (stronger) if necessary. Furthermore the impedance of the switch when it's off must be high enough in order not to have too much influence on the Voltage control circuit. This circuit regulates the gate voltage of the driving transistors. If the off impedance of the switch is too low, it might drain too much current from the voltage control circuit. This will be checked when the voltage control circuit is completed.

4.2 Level shifter

The level shifter needs to convert the low voltage threshold detection output signal towards a high voltage signal, which controls the stimulation enable switch using V_{switch}. The ideal circuit equivalent of this circuit is a floating voltage source, shifting the voltage level of the signal with $V_{dd,high} - V_{dd,low}$. This is depicted in Figure 4.2. To implement this floating voltage source, 4 different topologies are considered:

- Resistor with current sources
- V_{be} multiplier
- Capacitor based level shifter
- Transistor-only level shifter

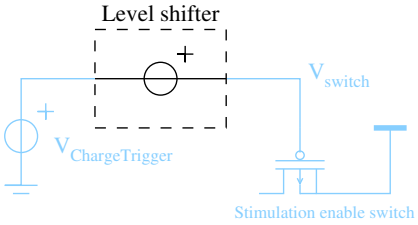


Figure 4.2: Ideal implementation of the level shifter

4.2.1 Resistor with current sources

The basic concept of this circuit is depicted in Figure 4.3. By forcing a certain current through a resistor, Ohm's law predicts a voltage drop of $V = IR$ over the resistor. Since the output impedance of the ideal current sources is $Z_{out} \rightarrow \infty$, the 'normal' signal flow from input to output is not influenced, except that the voltage is shifted by IR.

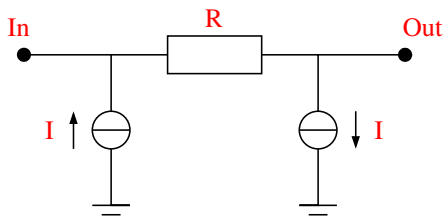


Figure 4.3: Implementation of the level shifter using a resistor and two current sources

This circuit implementation of a level shifter has quite some disadvantages. First of all it has a static power consumption which is equal to $P = I^2R$. The power consumption can be made smaller by increasing the resistor value (and thereby reducing the required current). Besides the practical problem of realizing a big resistor, this also puts high requirements on the output impedance of the current sources when they are realized.

Besides the power consumption also practical problems arise: it's not easy to integrate large resistors on chip. Especially in this case for which a resistor is needed which is able to handle the high voltage of $V_{dd,high} - V_{dd,low}$. One option to realise this is to replace the resistor by a diode chain. When the voltage drop over each diode is small enough, the current through them is very small, corresponding to a large resistance.

However, the circuit will still yield a static power consumption. therefore it is better to look for alternative implementations.

4.2.2 V_{be} multiplier

Another option is to generate the floating voltage using an active implementation. A very well known circuit for this is called a V_{be} multiplier. The circuit is depicted in Figure 4.4. It is based on the fact that the base-emitter voltage of a bipolar transistor is about constant (one diode voltage, usually around 0.6V). Using a feedback network this voltage is amplified (multiplied) towards the required voltage drop.

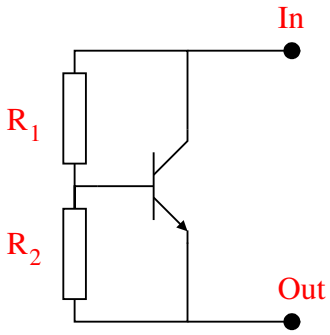


Figure 4.4: Implementation of the level shifter using a V_{be} multiplier

Assuming that there is no current into the base terminal, the current I through the resistors introduces a voltage drop over these resistors:

$$V_{out} - V_{in} = I(R_1 + R_2) \tag{4.1}$$

The current I can be described in terms of the base emitter voltage using $I = V_{be}/R_2$, yielding:

$$V_{out} - V_{in} = V_{be}\left(1 + \frac{R_1}{R_2}\right) \tag{4.2}$$

Assuming now that V_{be} is approximately constant, it's easy to generate the required floating voltage by choosing a certain ratio for R_1 and R_2. The advantage of this circuit compared to the passive implementation using the resistor with current sources is that there is more freedom to choose the resistors, since the output voltage is determined by a ratio.

Drawback of this circuit is again the need for resistors which are hard to implement on a chip. Furthermore this active implementation also dissipates a static current, corresponding to:

$$I = \frac{V_{out} - V_{in}}{R_1 + R_2} \tag{4.3}$$

It seems the active implementation has the same drawback as the passive implementation (static power consumption and hard to implement on a chip). Alternative implementations are therefore considered.

4.2.3 Capacitor based level shifter

Another well known way of introducing a voltage shift is by using a capacitor. A capacitor can be used to store a certain voltage on, which can be used for the floating voltage. The basic concept is shown in Figure 4.5. Consider the situation for which $V_{in} = V_{DDlow}$. Thanks to the diode clamp comprising D_1, D_2 and the source $V_{DDhigh} - V_{DDlow}$, the right terminal of the capacitor is charged towards $V_{DDhigh} - V_{DDlow}$. Since the left capacitor terminal is connected to ground, the voltage over the capacitor is exactly the required $V_{DDhigh} - V_{DDlow}$.

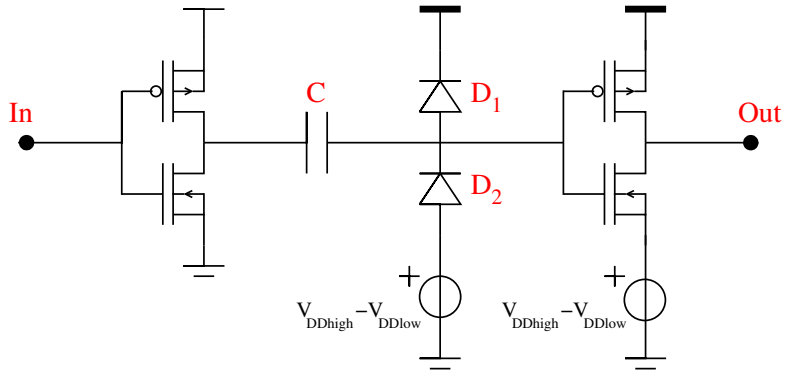


Figure 4.5: Implementation of the level shifter using a capacitor

When the input is switched from V_{DDlow} to 0, the left terminal of the capacitor is now connected to V_{DDlow}. Because of the nature of a capacitor the voltage over the capacitor is kept constant, meaning the right terminal will be V_{DDhigh}. This means the capacitor implements the required floating voltage source. Note that diode D_1 is not necessary for a correct functionality of the system. This diode only makes sure the voltage does not become higher than V_{DDhigh}.

A couple of aspects need some more attention. First of all the capacitor will start to discharge due to leakage when the right terminal is lifted towards V_{DDhigh}. The discharge rate depends on the value of the capacitor and the resistance of the diodes and inverter. It must be made sure that the right terminal voltage stays above the threshold voltage of the second inverter long enough. In case of the charge threshold detection, this means that the capacitor must be able to hold its value at least as long as the longest pulse possible.

Furthermore it must be noted that integrating a capacitor on a chip also requires quite some area. However, the big advantage of this circuit is that it does not consume any static power. When the capacitor is charged towards $V_{DDhigh} - V_{DDlow}$ it does not consume any power anymore (apart from small leakage). Also when switching no additional power is consumed, apart from the inverters which need to switch. Therefore the overall power consumption is expected to be very low.

4.2.4 Transistor only level shifter

Another way to implement a level shifter is to consider its operation from another point of veiw. The operation of the circuit is similar to what is happening in a level converter [59]. This circuit is used to interface between two digital circuits with different supply voltages. In contrast to the situation in this project the scope of the input signal is between 0 and V_{DDlow}, while the output signal is between 0 and V_{DDhigh}. However, by changing the circuit topology a bit, it is possible to get the desired behaviour in which the output signal is between $V_{DDhigh} - V_{DDlow}$ and V_{DDhigh}.

A commonly used circuit for a level converter is based around a cross coupled PMOS pair as is shown in Figure 4.6. If the low voltage signal would be connected to a high voltage inverter directly, the low voltage cannot turn off the high voltage PMOS, yielding a very high power consumption. Therefore a cross coupled PMOS pair (M_1 and M_2 in Figure 4.6) is used instead to prevent a direct path from V_{DDhigh} to *gnd* at any time.

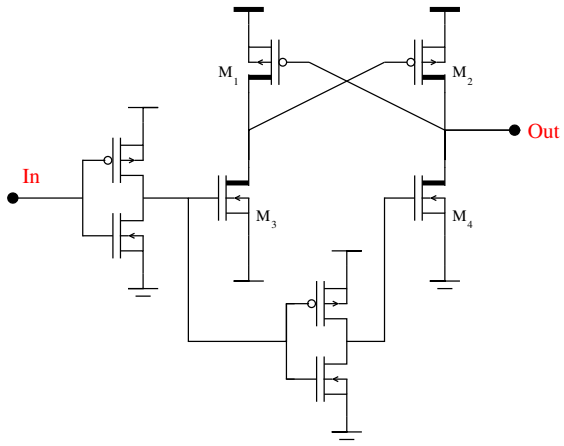


Figure 4.6: A conventional Level Converter circuit

This basic concept of a level converter can be used for a level *shifter* as well as is described in [58]. The only thing that should change is that the minimum output voltage should be limited to $V_{out} > V_{DDhigh} - V_{DDlow}$. This can be done by inserting two additional PMOS transistors with their gates biased to this particular voltage, as shown in Figure 4.7. This garantees that the voltage at node N_1 does never drop beneath $V_{bias} - V_{th}$ with V_{th} being the threshold voltage of M_3 and M_4. When N_1 does become smaller, M_3 and M_4 will be switched off, making sure the voltage cannot drop further.

Note that the cross coupled PMOS transistors M_1 and M_2 have been changed to low voltage transistors. The voltage drop over them is not bigger than V_{DDlow} thanks to M_3 and M_4. Changing them into low voltage transistors saves a lot of area. the output is buffered by another inverter, which can also consist of low voltage transistors. Depending on the need for either an inverting or non inverting level shifter, an additional inverter can be added at the input.

The advantage of this circuit is that no capacitor is needed. First of all this saves area, but it also means the dynamic nature of the circuit is gone, yielding no complications with the maximum time a high output can be hold. The static power consumption of this circuit is also very low, since no direct paths exist from the supply voltage to ground. Furthermore this circuit is not bound to a constant voltage shift of $V_{DDhigh} - V_{DDlow}$. The output voltage range can be chosen arbitrarily, by changing the bias voltage of transistor M_3 and M_4. In this particular application this will not be necessary (since the switching voltage of the stimulation enable switch is 3 V), but for other applications this might be beneficial.

Disadvantages of this circuit first of all include the use of 4 high voltage transistors, occupying quite some chip area. This might cancel the area reduction obtained by not using a capacitor. Furthermore the dynamic power consumption can be expected to be slightly higher. The voltages

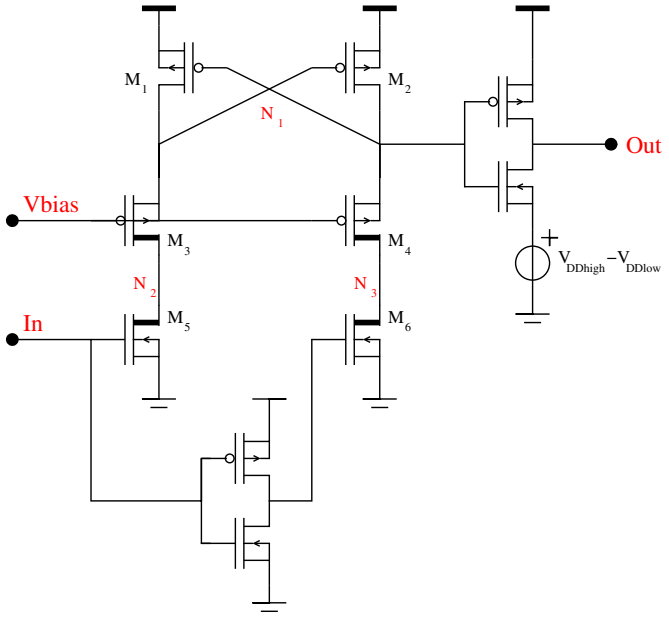


Figure 4.7: Design of a Level Shifter based on a Level Converter

at nodes N_2 and N_3 are switching between the full V_{DDhigh} and *gnd*. This large voltage swing means more current is required to charge and discharge these nodes.

4.3 Driver

The next block to be considered is the Driver. The task of this block is to generate the stimulation current (based on the gate voltage provided by the voltage feedback block) and an accurate copy of this current for the integrator. The working principle was already discussed in chapter 3: by copying the gate-source voltage, the output current is copied as well assuming both transistors operate in the saturation region and channel length modulation can be neglected. The basic idea is depicted in Figure 4.8.

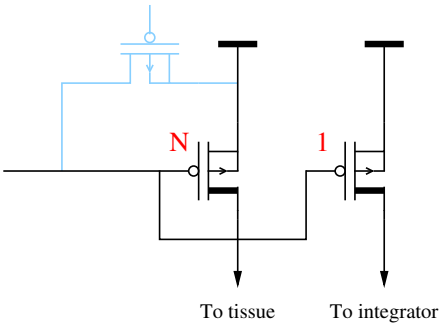


Figure 4.8: Basic design of the Driver transistors

First a choice needs to be made for the ratio N. The higher N is chosen, the higher is the power efficiency, as explained in equation 3.2. However, the bigger N, the more area is needed. This is important, because the transistors need to be high voltage transistors and they take up

quite some area. The choice of N is therefore based on a trade-off between power consumption and chip area.

At this point it's hard to predict how much area exactly is available for the stimulator on the chip. This depends on the total chip area available, but also on the chip area needed for the other components (digital circuitry, sense amplifiers, etc). For now it's important to realize the fundamental functionality of the circuit does not depend on N: the circuit will work for any value. Only the power efficiency of the circuit is affected. Therefore it is decided for now to take the arbitrary value of $N = 100$. This value is more or less considered as a maximum value: 100 DPMOS transistors take up a significant amount of space, while the theoretical efficiency now is as high as 99%.

If at any point it is decided to choose $N < 100$ (for example because of area occupation), it will decrease the power efficiency, but it does most likely not have any other negative issues. For example: when $N = 100$ the load for the voltage feedback circuit comprises 101 DMOS gates. When later it is decided to decrease N, this will only reduce the load, which is not a problem.

Most important for the driver circuit is that the two output currents are a constant fraction (N) of each other. Errors will be produced if this ratio varies for different output currents. For example consider the case for which in the positive phase a high current is injected for t_1 seconds for which the fraction is $N + \alpha$ and in the negative phase a low current with fraction N for t_2 seconds. Now in the first phase an additional charge of αt_1 C is injected and charge balance is not achieved anymore.

It therefore needs to be investigated under which conditions the ratio N is affected. Assuming the MOS transistors operate in the strong inversion saturation region, the current through the MOSFET is given by:

$$\frac{\mu_p C_{ox}}{2} \frac{W}{L} \left(V_{gs} - V_t\right)^2 \left(1 + \lambda V_{ds}\right) \tag{4.4}$$

Here μ_p is the mobility, C_{ox} the gate oxide capacitance per unit area, W is the width, L the length and λ is the channel length modulation index. Any mismatch between the two transistors in any of the quantities in the equation will lead to a deviation from the ideal current ratio N. Besides strong inversion, the transistors might also been driven into the weak inversion region. Here another relation is valid (assuming again saturation):

$$I_d = \frac{W}{L} I_t \exp\left(\frac{V_{gs} - V_T + \eta V_{ds}}{n U_T}\right) \tag{4.5}$$

Here U_T is the thermal voltage, n is the subthreshold current slope factor, which is ideally 1 and η is a parameter similar to λ in strong inversion, modelling a dependence for V_{DS}. The parameter I_t is a constant which is dependent on process parameters, much like μ_n and C_{ox} in strong inversion.

It needs to be investigated which quantities lead to actual charge cancellation mismatches. A distinction is made between errors resulting from process variations and errors resulting from voltage variations.

4.3.1 Effects of process mismatch

Process mismatch will lead to deviations of the transistor parameters. First, deviations in the first term for strong inversion (deviations in μ_n, C_{ox}, W and/or L) are investigated. An error will lead to a deviation of this first term: here a factor α is assumed. The current ratio is affected by it:

$$\frac{I_N}{I_1} = \frac{\alpha \frac{\mu_n C_{ox}}{2} \frac{NW}{L} \left(V_{gs} - V_t\right)^2 \left(1 + \lambda V_{ds}\right)}{\frac{\mu_n C_{ox}}{2} \frac{W}{L} \left(V_{gs} - V_t\right)^2 \left(1 + \lambda V_{ds}\right)} = \alpha N \tag{4.6}$$

As can be seen these mismatches change the current ratio N, but this ratio is constant. This means that charge cancellation is still achieved, since during both stimulation phases the current ratio is constant. In weak inversion a similar reasoning can be made for the parameters W, L and I_t.

Next parameter to be investigated is the threshold voltage V_t. Due to for example impurities in the doping concentrations, the threshold voltage of a device may vary within a single die. Assume again a multiplicative error of α in the threshold voltage, this will lead to the following current ratio in strong inversion:

$$\frac{I_N}{I_1} = \frac{\frac{\mu_n C_{ox}}{2}\frac{NW}{L}\left(V_{gs}-\alpha V_t\right)^2\left(1+\lambda V_{ds}\right)}{\frac{\mu_n C_{ox}}{2}\frac{W}{L}\left(V_{gs}-V_t\right)^2\left(1+\lambda V_{ds}\right)} = N\frac{\left(V_{gs}-\alpha V_t\right)^2}{\left(V_{gs}-V_t\right)^2} \tag{4.7}$$

There is some data about current matching in the datasheets of the technology. Based on some basic experiments, the standard deviation for V_t is provided. Assuming minimum width ($W = 20$), it holds for a PDMOS device ([5] and [6]):

$$\sigma = \frac{A_{vT}}{W} + C_{vT} = 0.9418\,\text{mV} \tag{4.8}$$

This means that in the 4σ corner, the V_t varies with about $\Delta V_t = 3.7\,\text{mV}$. Assuming now a $V_t = -0.56\,\text{V}$, as provided in the documentation for the PDMOS transistor, a plot can be made for the deviation in current ratio, which is depicted in Figure 4.9 using the dashed line.

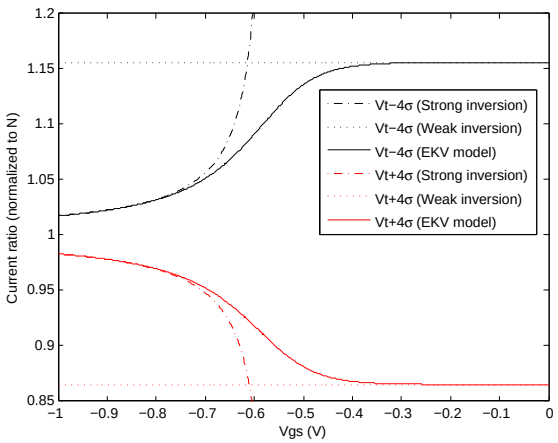


Figure 4.9: Normalized current ratio due to intra die V_t mismatches

Looking at the figure, the effect of the V_t mismatch looks quite dramatic for low currents (when V_{gs} is close to the threshold voltage). However, for low currents, the transistor is close to the Weak inversion region (subthreshold). Here 4.5 holds and the following current ratio results when the threshold voltage deviates (ignoring channel length modulation):

$$\frac{I_N}{I_1} = \frac{\frac{NW}{L} I_t \exp\left(\frac{V_{gs}-\alpha V_T+\eta V_{ds}}{nU_T}\right)}{\frac{W}{L} I_t \exp\left(\frac{V_{gs}-V_T+\eta V_{ds}}{nU_T}\right)} = \frac{\exp\left(\frac{V_{gs}-\alpha V_t}{U_T}\right)}{\exp\left(\frac{V_{gs}-V_t}{U_T}\right)} = \exp\left(\frac{(1-\alpha)V_t}{U_T}\right) \tag{4.9}$$

As can be seen in weak inversion the deviation of the current ratio is not dependent on the V_{gs}. This means that if the transistors would only operate in weak inversion, the threshold voltage deviation would be no problem. However, as already seen, this is not the case. The value for the weak inversion region is also depicted in Figure 4.9 using a dotted line. Clearly the current ratio resulting in practice will be a combination of both functions described above.

To describe the transition region between the strong and weak inversion, the EKV model can be used [17]. Here a transition function is used to 'bridge' the exponential and quadratic behaviour using the form of $F = \left[\ln\left(1+\exp\frac{v}{2}\right)\right]^2$. The following form can be used:

$$I_d = \beta U_T^2 \left[\ln\left(1+\exp\frac{V_{gs}-V_t}{2U_T}\right)\right]^2 \tag{4.10}$$

Here β is a scaling factor. Using this equation, the current ratio according to the EKV model can be calculated:

$$\frac{I_N}{I_1} = \frac{N\beta U_T^2 \left[\ln\left(1+\exp\frac{V_{gs}-\alpha V_t}{2U_T}\right)\right]^2}{\beta U_T^2 \left[\ln\left(1+\exp\frac{V_{gs}-V_t}{2U_T}\right)\right]^2} = \frac{N\ln\left(1+\exp\frac{V_{gs}-\alpha V_t}{2U_T}\right)^2}{\ln\left(1+\exp\frac{V_{gs}-V_t}{2U_T}\right)^2} \tag{4.11}$$

This equation is also plotted in Figure 4.9. As can be seen, this indeed bridges the gap between the weak and strong inversion regions. The weak inversion region specifies the worst case deviation, which is about 10% for the technology used. This is quite significant.

However the effect of the data provided in Figure 4.9 is worse than it will be in reality. The data provided in the datasheets assumed two equally sized transistors. However, in this case, one transistor is much bigger. This means that the V_t for this transistor is much better defined, which will reduce the standard deviation compared to the situation with two identical transistors. However, for this situation no data is provided. Since N will be chosen quite high (100 for now), the effect of threshold deviations will be much lower. For now it is decided to not change the design of the driver transistors based on the V_t mismatch. First more research is needed on the exact implications the large N-sized PDMOS transistor has on the V_t mismatch.

The final quantity from Equation 4.4 that can vary is the channel length modulation index λ (or η in the weak inversion). In the documentation of the technology, no experimental data about the spread of the channel length modulation index were found. As will be clear in the next section a lot of effort will be put in making the V_{ds} of both transistors equal. This will greatly decrease the influence of λ and η. Therefore the variation of λ and η is not taken into account.

4.3.2 Effects of Channel Length modulation

Channel Length modulation results in a dependence of the drain current on the Drain-Source voltage. It is represented in equation 4.4 by the last term $(1 + \lambda V_{ds})$. This means that although the V_{gs} of both transistors is the same, still the current ratio may deviate from N if the V_{ds} is different. Actually this is the case for the circuit as it is now. Although for the other blocks the simulation results are given in the next chapter, an exception is made for the driver transistors. The design choices made for this system block are clearer when simulation results are incorporated.

The big N-sized transistor has its drain connected to the tissue. The voltage over the tissue can be anything between 0 and V_{DDhigh}. The small transistor however has its drain connected to the integrator. As was pointed out before, this integrator is realized in low voltage technology. The exact voltage will depend on the implementation of the integrator, but at least it's known that the voltage will not exceed V_{DDlow}.

Therefore it is for sure that without any further adjustments the circuit will suffer from channel length modulation, which will result in charge mismatch. To illustrate this the response of two driver transistors is verified using simulations.

The goal is to simulate the current ratio of the transistors for various V_{ds}. To do this the big transistor is connected to the tissue which is modeled by a simple resistor, as depicted in Figure 4.10. A complicated model is not required; it's only important for the simulations to have a certain current flowing through the tissue. For $V_{DDhigh} = 12\,\mathrm{V}$, the tissue was modeled using $R = 1\,\mathrm{k\Omega}$, since this corresponds to a maximum current around 10 mA, which is consistent with many existing stimulators.

The small transistor is connected to the ground, in order to account for the worst case V_{ds}. The voltage over the tissue is controlled using an ideal voltage control loop, consisting of an ideal g_m cell. Using a DC sweep of the stimulation source, the tissue voltage can be swept over the complete 0 to V_{DDhigh} range. For the DC simulation an additional resistor of $1\,\mathrm{G\Omega}$ is added to have a DC connection to ground at the gates.

The result of the simulations using only the two driver transistors is depicted in Figure 4.11. As can be seen in Figure 4.11(b) the current ratio varies quite significantly over the voltage range. The deviation is very significant when $V_{tissue} \approx V_{DDhigh}$. This is because at this point the voltage

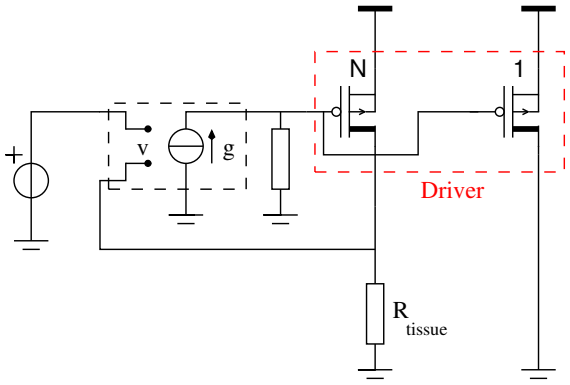


Figure 4.10: Circuit used to simulate the current ratio deviations due to Channel Length Modulation

drop over the transistor is small and eneters its triode region. In these operating regions V_{gs} becomes very large and the transistors are in breakdown, yielding unexpected behavior. In Figure 4.11(a) it can be clearly seen the Integrator current is increasing rapidly for high tissue voltages due to the high V_{gs}. Therefore in practice the tissue cannot be driven until the full V_{DDhigh} voltage, since the voltage drop over the driver needs to be taken into account.

However, from the figure it can be seen that already significant deviations exist in the current ratio at lower voltages as well. Therefore measures need to be taken to avoid this. To completely avoid the channel length modulation, the V_{ds} of both driver transistors should be made equal. One very common way for channel length modulation elimination in current mirrors is by using a cascode stage. Actually this cascode is an implementation of an active circuit with the functionality of a current follower. Therefore it was chosen to first explore an implementation with an ideal active circuit, to check if indeed channel length modulation is the only effect playing a role in the simulation of the current ratio mismatch.

CLM cancellation using an ideal active circuit

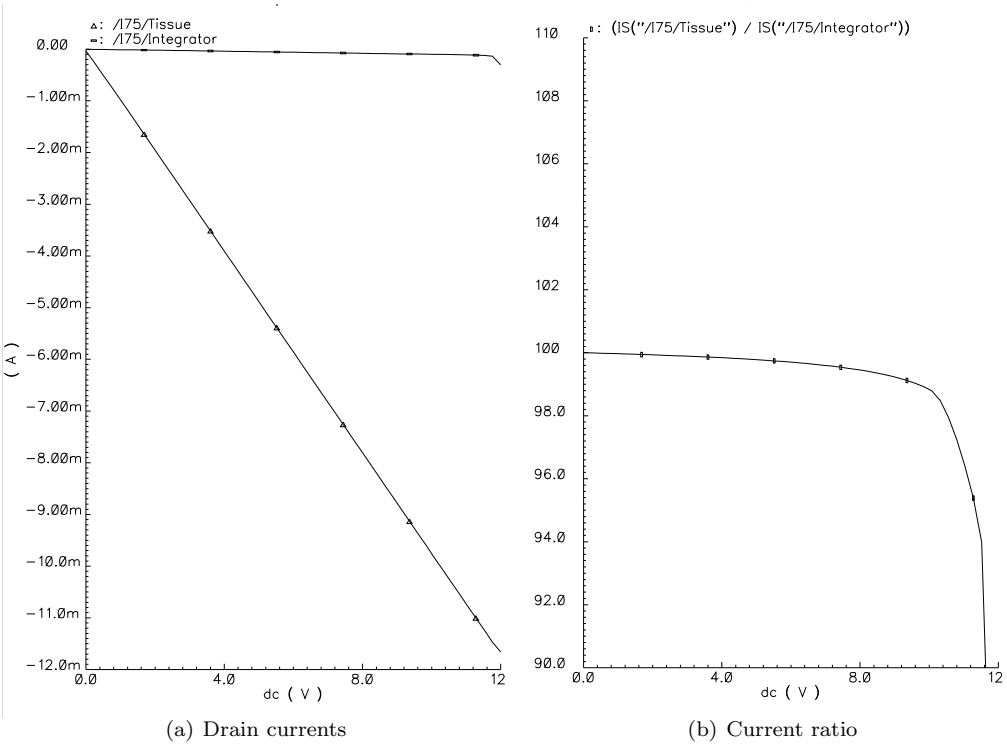
One way to make the V_{ds} of the two transistors equal is by using an active circuit. At the input the voltage of both drain terminals should be monitored. At the output, the voltage should be adjusted in such a way that the two Drain voltages are equal. It was chosen to implement the ideal active circuit using a voltage controlled current source. The circuit was implemented as shown in the Figure 4.12(a).

The simulation result is depicted in Figure 4.13(a) and 4.13(a). As can be seen the current ratio is now perfectly constant at N for all V_{gs}. This confirms that indeed channel length modulation was causing the current ratio mismatches found in Figure 4.11. A possible implementation of the ideal active circuit is given in Figure 4.12(b): using a differential CS stage. In this figure the bias sources are included as well.

As can be seen, biasing this circuit is not straightforward. All voltage sources depicted are floating. Furthermore, the bias current for these transistors needs to be at least the current which is flowing through the integrator. This will significantly increase the power consumption of the circuit. Using a modified biasing scheme it might be possible to use the integrator current as bias current, but then a more complex biasing scheme will be needed. Therefore the implementation of the Channel length modulation using a CS stage as active circuit is rejected.

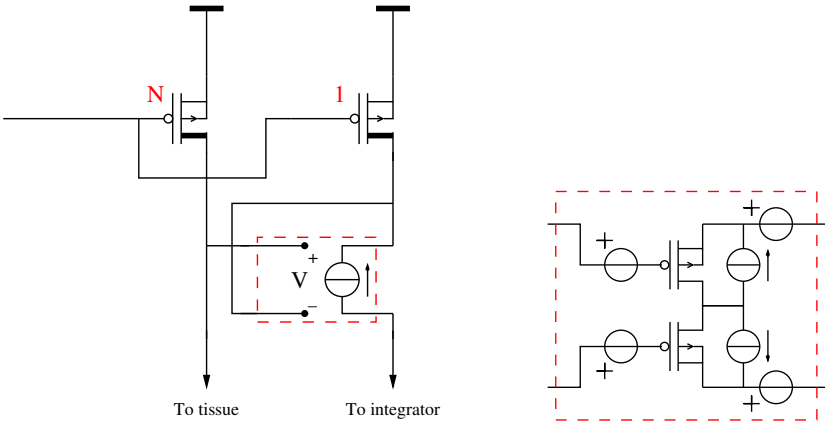
CLM cancellation using a cascode circuit

Another implementation of an active circuit keeping the drain voltages equal is a cascode stage. This actually is an implementation of a current follower: the input impedance is low, such that



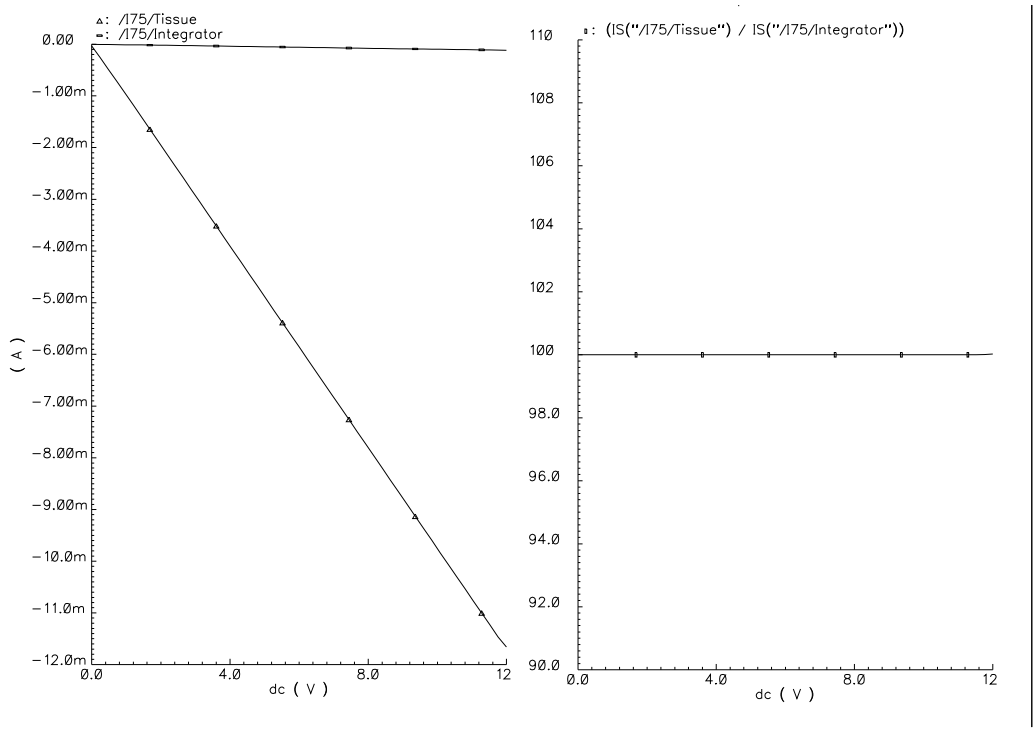
(a) Drain currents (b) Current ratio

Figure 4.11: Current response using the basic circuit implementation



(a) Circuit principle (b) Possible ative circuit implementation

Figure 4.12: Channel Length cancellation using an ideal active circuit



(a) Drain currents

(b) Current ratio

Figure 4.13: Current response using the active circuit for CLM cancellation

the voltage over the two drains becomes equal. The advantage of a cascode stage compared to the active implementation discussed above is, that it does not require any additional biasing circuitry.

The implementation of a cascode stage is depicted in Figure 4.14. The diode connected PMOS generates a particular V_{gs} over this transistor. This V_{gs} is copied to the other transistor in the cascode stage, because these transistors have the same size ratio as the driver transistors. This forces the drain voltages of the two driver transistors to be equal.

In Figure 4.15(a) and 4.15(b) the result of a simulation of the circuit depicted in Figure 4.14 is shown. As can be seen, the cascode stage is indeed able to keep the current ratio constant at 100. However, when the tissue voltage increases above a particular level, the current ratio is not constant anymore. This can be explained by the fact that there is an additional voltage drop over the diode connected transistor M_3 in the cascode stage. When the tissue voltage is increased at some point the voltage headroom will be too small. This means the current through the tissue cannot increase anymore (it clips). The voltage feedback circuit however will try to push more current through, to increase the tissue voltage. This will lower the gate voltage.

However, the output voltage of the voltage feedback is limited to prevent the $|V_{gs}|$ of M_1 and M_2 to become to large. While the V_{gs} is still decreasing, the current through the integrator is slightly increasing, yielding a lower current ratio. When the gate voltage reaches the limit, the current ratio becomes constant again, in this case around 97.65.

Besides the reduced voltage headroom due to the diode connected transistor, the circuit depicted in Figure 4.14 has one major drawback: it requires two additional High Voltage transistors, one of them being of size N. This will double the area needed for the driver, which already was significant. The problem is that the cascode stage needs to have the same ratio for the transistors as the driver transistors. Since the driver transistors already use the minimum width for the unit-sized transistors, this is a fundamental size limitation of the cascode stage.

A solution for this problem is found when realizing that for the diode connected transistor the voltage over each of its terminals will never exceed the breakdown voltages for a low voltage

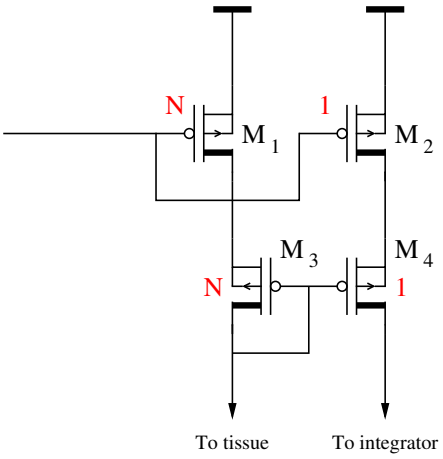
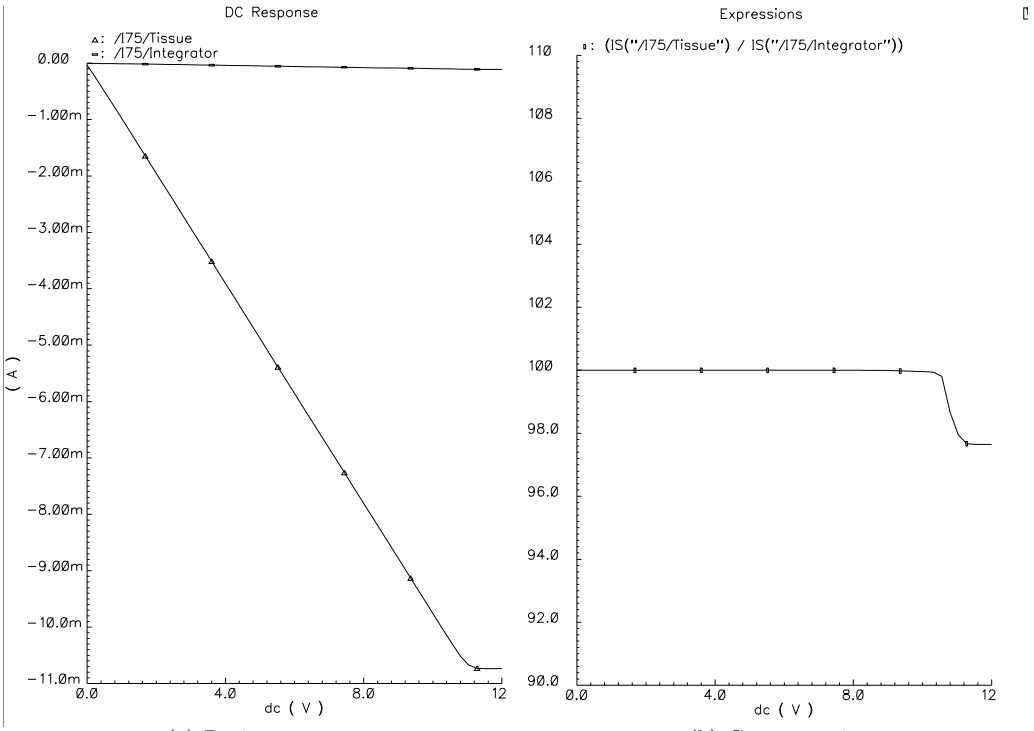


Figure 4.14: Channel Length cancellation using a cascode stage



(a) Drain currents (b) Current ratio

Figure 4.15: Current response using a cascode stage for CLM cancellation

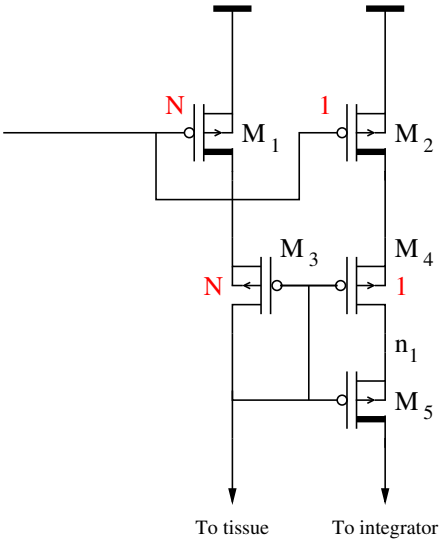


Figure 4.16: Channel Length cancellation using a low voltage cascode stage

transistor. Here a low voltage transistor can be used. This means that for correct operation of the cascode stage, the other transistor must be low voltage as well.

Now there is another problem. Since the voltage of the integrator is low, the voltage drop at the drain of the low voltage transistor will be too large. Therefore a single high voltage transistor is introduced to shield the drain from the low voltage. This is illustrated in Figure 4.16. This has however some consequences for the voltage headroom. In the circuit of Figure 4.14 $V_{ds,3}$ will be higher than using the high voltage cascode stage. the voltage at node n_1 depends on the $V_{ds,4}$ corresponding to the current flowing through it (I_{int}). The V_{tissue} is now found by adding $V_{gs,5}$ to it:

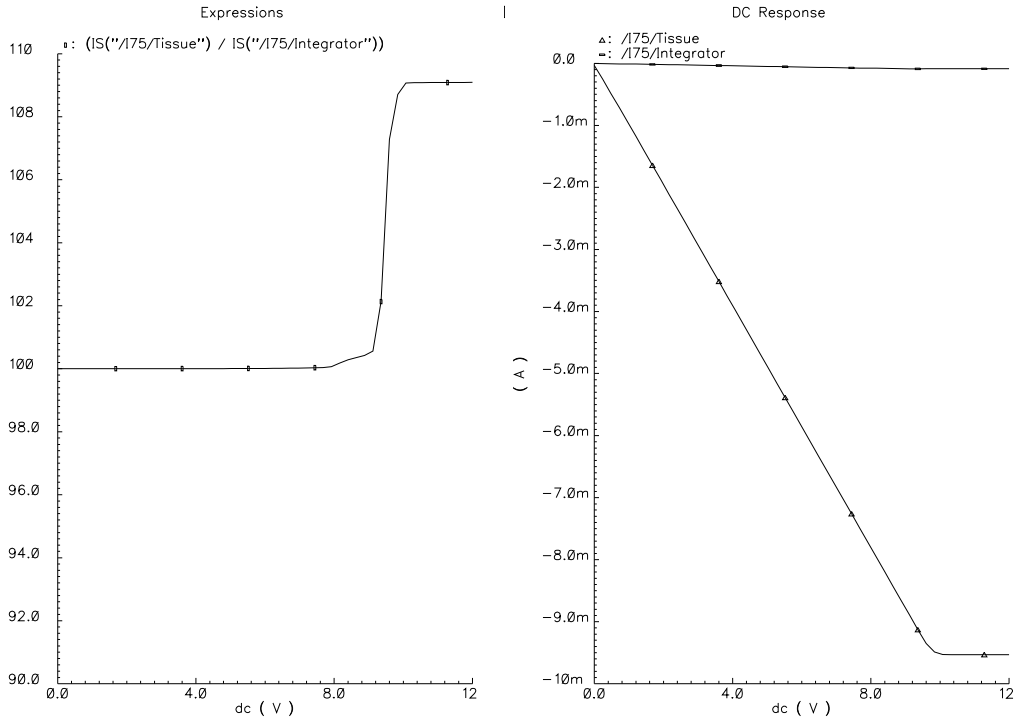
$$|V_{ds,3}| = |V_{ds,4}| + |V_{gs,5}| \tag{4.12}$$

This means that the additional high voltage transistor M_5 increases the voltage drop over transistor M_3. This voltage will not become bigger than the breakdown voltage. This is because $V_{gs,5}$ is not very big: the current through the integrator branch is 100 times smaller than the stimulation current. The higher $V_{ds,3}$ has however consequences for the voltage headroom for stimulation. Because of the decreased drain voltage, the tissue voltage will clip sooner. This can be seen indeed in Figure 4.17.

In this figure it's remarkable the current ratio is increasing this time when the voltage clips, instead of decreasing, as was the case in the previous designs. This can be understood easily: in the previous designs the tissue current was at some point limited, because the drain voltage was clipping to the supply voltage. This time however, it's the integrator current which is clipping first: it is node n_1 in Figure 4.16 which is pushing the drain voltages of M_1 and M_2 towards the supply voltage. Therefore the ratio $I_{tissue}/I_{integrator}$ is increasing in the latter case and increasing in the first case.

Note that the working principle depends on the fact that $V_{tissue} > V_{integrator}$. When $V_{integrator}$ becomes larger than V_{tissue} it can turn off transistor M_5. However, since the drain of this transistor is very well isolated from the rest of the transistor, the effect is minimal. Simulations show only very minor changes in the current ratio (when $V_{integrator} = 7\,\mathrm{V}$, the current ratio becomes 100.3 for $V_{tissue} = 0\,\mathrm{V}$, which is already much worse than will happen in practice where the integrator voltage is lower).

The reduced voltage swing for which the tissue can be stimulated with a constant current ratio is a drawback of the circuit: a much higher voltage needs to be generated, while only part of it is used efficiently. Due to the channel length cancellation circuitry, the voltage swing is reduced by two V_{gs} voltages.



(a) Drain currents (b) Current ratio

Figure 4.17: Current response using a low voltage cascode stage for CLM

One way to solve this would be by boosting the tissue voltage with respect to the gates of transistors M_3, M_4 and M_5 as illustrated in Figure 4.18. In this way, the tissue already reaches its maximum value before the voltage at node n_1 starts to clip. However, this source should be turned off if the tissue voltage is lowered under a certain voltage. Otherwise, the voltage at the gates will become negative.

To check the working principle of this circuit, a source is implemented which switches on or off, depending on the tissue voltage. The simulation results are depicted in Figure 4.19(a) and 4.19(b). As can be seen, the source is switched on when the tissue voltage reaches 8 V. Indeed the current ratio now stays constant much longer (it is increased by one V_{gs}, just like the situation with the 'simple' cascode stage).

Problem of this boosting source is to implement the floating dependent voltage source. For now the implementation of the source is not further considered. If in the future it becomes necessary to have a bigger voltage swing and the cascode circuit is actually chosen, the implementation of this floating voltage source can be reconsidered.

CLM cancellation using a cascode with increased voltage headroom

The last principle to cancel the charge cancellation which is discussed here, is by using again a cascode, but now with increased voltage headroom as depicted in Figure 4.20. First the drain voltages of the driver transistors are made equal by using a cascode stage similar to the first one discussed in the previous paragraph. However, this time two transistors of size 1 are used. the idea is to allow $(N-1)I$ through the tissue and $1I$ through the cascode. To ensure that exactly $1I$ is passing through the cascode, a second cascode stage (using NDMOS) is added, which matches the current to the integrator current, which is also $1I$. Now $(N-1)I$ is flowing through the tissue, while $2I$ is flowing through the integrator.

Benefit of this approach is that the tissue voltage swing is maximized. Also only 4 additional unit-size high voltage transistors are needed, which is much lower than the conventional cascode

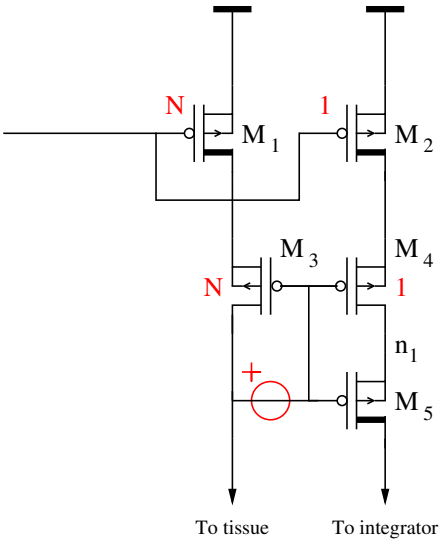
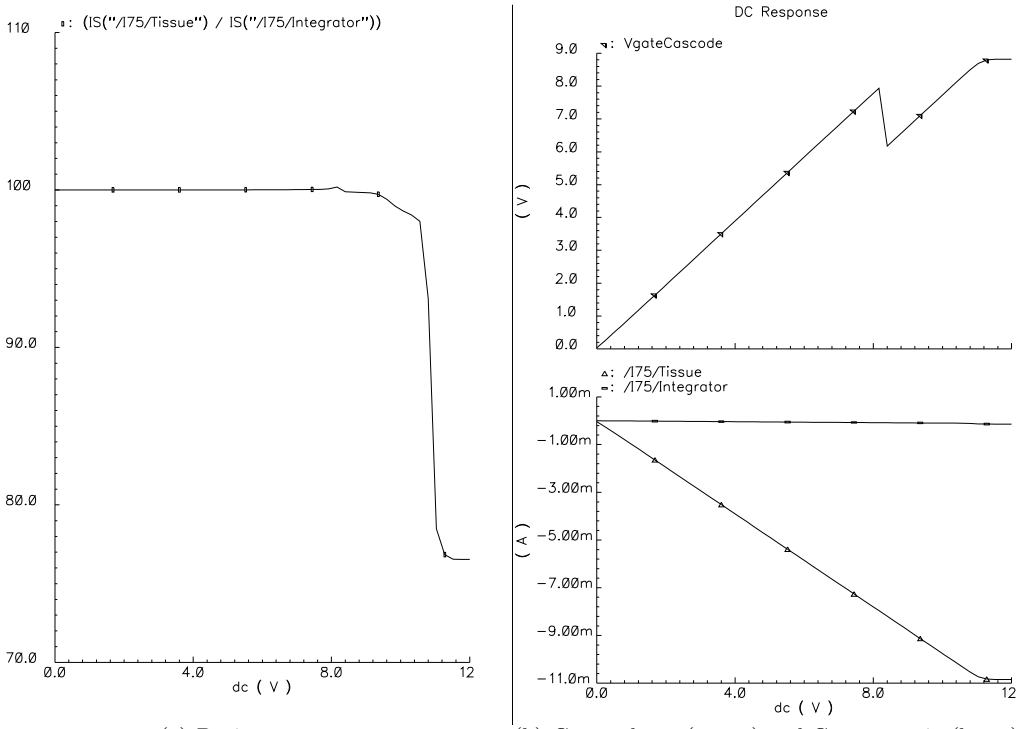


Figure 4.18: Increasing the Tissue voltage swing by boosting the voltage



(a) Drain currents

(b) Gate voltage (upper) and Current ratio (lower)

Figure 4.19: Current response using using a low voltage cascode stage with a boosted tissue voltage

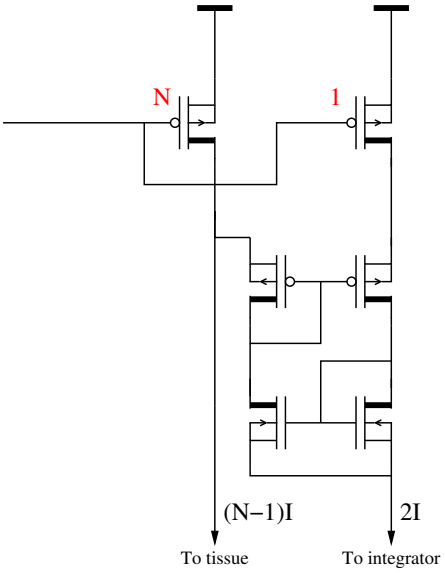


Figure 4.20: Channel length cancellation using a cascode with increased voltage headroom

stage. The major drawback is that the power efficiency is almost halved: twice as much current is 'wasted' in the integrator.

Simulations have shown this circuit is indeed working. However, there is another problem: the transistors used in the 'cascode' suffer from Channel Length modulation themselves. The diode connected transistor has a voltage drop of only V_{gs}, while the other has a voltage drop of almost the complete voltage swing. Including more circuitry to fight the channel length modulation is possible (and simulations confirm this once again), but this makes the circuit quite complicated.

Due to the reduced power efficiency combined with the complexity of the circuit, it was chosen not to use this design. Instead is was chosen to implement the cascode stage with the low voltage transistors. At this point a trade-off is made between area consumption and power efficiency (related to the reduced output voltage swing). The reduced area consumption of the low voltage transistors compared to the high voltage cascode stage was considered more valuable than the output voltage swing.

4.4 Voltage Control feedback

The function of the voltage feedback circuit is to adjust the gate voltage of the driver transistors in such a way that the tissue voltage is matched to the voltage of the stimulation source. For reasons mentioned before the stimulation voltage source is assumed to be low voltage. This means the voltage from the tissue needs to be attenuated first before it is matched to the stimulation source. Additional advantage of this approach is that the input voltage of the feedback network is low voltage, which makes the use of high voltage isolation at the input not necessary.

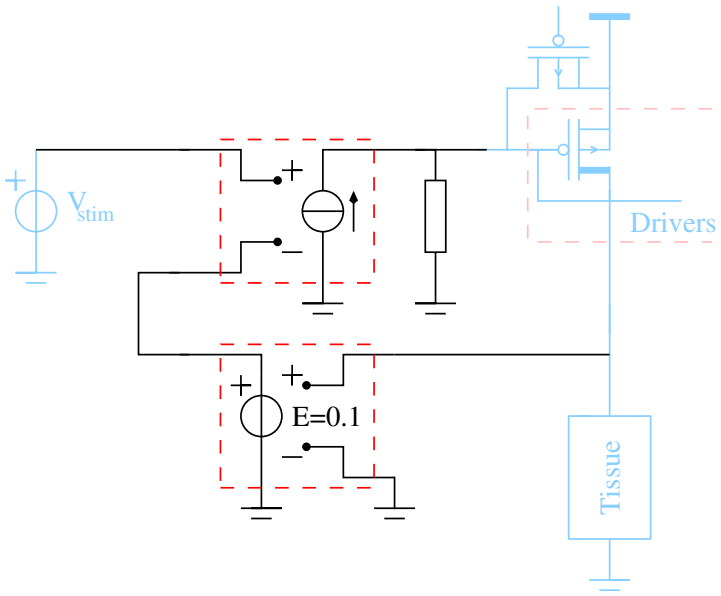


Figure 4.21: Ideal voltage feedback network

The ideal voltage control feedback network is depicted in Figure 4.21. First the voltage from the tissue is attenuated 10 times. The factor 10 was chosen quite arbitrarily. The only requirement is that the high voltage from the tissue is converted towards $< V_{DDlow}$. Using a factor 10, the maximum value for V_{DDhigh} is around 30 V now. After attenuation, a G_m cell is included, which contributes gain in the feedback loop. A g_m cell was chosen because it resembles a CS connected transistor best (for maximum gain), which is the most straight forward implementation.

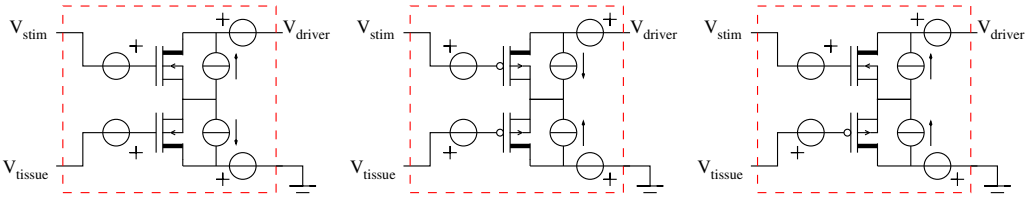
A resistor is added. This is done for simulation purposes in order to have a DC path to ground. This resistor is made very big. Simulation results show a correct operation of this ideal voltage control scheme. DC simulations are done to check if the tissue voltage is indeed made equal to the stimulation source. The results are not included here, but the ideal scheme was working as expected.

First the implementation of the G_m cell was considered. To obtain maximum gain, a CS stage was considered first. Since the transfer of the gain stage needs to be non inverting, a differential implementation was required. Furthermore, the gate voltage of the driver transistors is high voltage: the source of these transistors is connected to V_{DDhigh}. Therefore the transistors in the gain block also need to have high voltage capabilities. Choosing for the CS stage makes this easy: the drain of the DMOS transistors has high voltage capabilities, and it is exactly this drain which is connected to the driver.

It turned out that biasing the CS stage is not straight forward, because using standard circuits, there is a need for a negative voltage supply. Creating a negative voltage supply yields the need for extra circuitry and therefore additional power consumption. Therefore it is tried to bias the circuit with positive voltages only.

Let's first consider a NDMOS transistor pair, as depicted in the Figure 4.22(a). At first sight

not much problems seem to arise: all voltages are positive. However, the implementation of the circuit as depicted is not very practical. Especially the floating voltage source towards the tissue is very hard to implement. Therefore, this source should be shifted through the gain stage. When this happens, the tissue voltage is directly connected to the gate of the lower transistor. When the tissue voltage is now set to 0 V, the source voltage of both transistors is forced to $-V_{gs}$. This means that a negative voltage is required to keep the transistors biased properly. To implement the differential pair using NDMOS transistors, either a negative voltage is required, or the floating voltage source should be implemented.



(a) NMOS (b) PMOS (c) NMOS+PMOS

Figure 4.22: Three different biasing schemes for the differential CS stage

Next a PDMOS transistor pair is considered as depicted in Figure 4.22(b). Again the floating source from the tissue can be shifted into the rest of the circuit, eliminating the need for negative voltages here. However, the biasing of the drain of the lower transistor immediately shows the need for a negative voltage. This voltage can however be eliminated by shifting sources (as will be shown later during the actual implementation). Another disadvantage of this circuit is the difficult implementation of the floating source towards the driver. When using an NDMOS, this source can be omitted (as will be shown further on as well) because the bias of the gate itself can be used. This is however not possible with the PDMOS: here a (floating) bias source is required. This floating source will also need high voltage capabilities, yielding a difficult and large implementation.

Since problems arise in the lower transistor for a NMOS implementation and in the upper transistor for the PMOS transistor, it makes sense to use a combination of a NDMOS and PDMOS transistor. This is depicted in Figure 4.22(c). One obvious issue with this schematic is that the cell is not purely differential anymore. This means the output is not symmetrical anymore. However, this is not very important for this application: the circuit only needs to deliver enough gain. There are not many issues related to for example non linearity, since the exact shape of the voltage waveform is not very important, as pointed out before.

Now the biasing is considered. In Figure 4.23 the different biasing steps are depicted. First the drain current sources are shifted. Now the drain currents of both transistors are chosen to be equal, so the middle current source can be omitted. Furthermore the current source in the bottom can be omitted as well, assuming the voltage source is able to deliver the current.

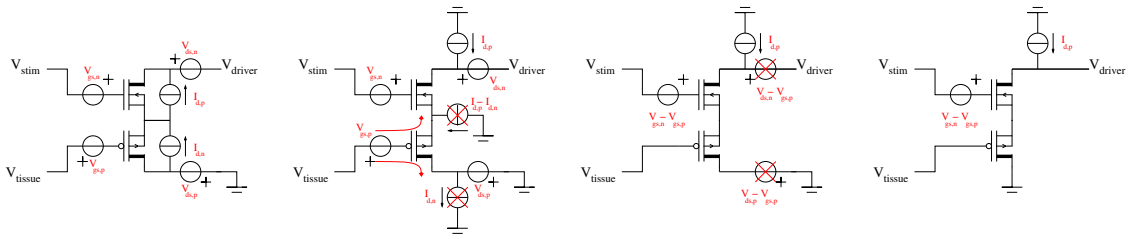


Figure 4.23: Biasing of the CS stage

Next step is to shift $V_{gs,p}$ into the differential stage. Now the source $V_{ds,p} - V_{gs,p}$ is considered. The $V_{ds,p}$ biasing voltage of the PMOS transistor can be chosen arbitrarily, since the NMOS transistor will take care of the high voltage needed by the gate. Now it is chosen $V_{ds,p} = V_{gs,p}$, which will eliminate this source. Note that this choice makes the differential stage even more

unbalanced, since the two transistors have a completely different V_{ds}. However, this is most likely not a big problem, since again the accuracy of this stage is not very important, it only needs to deliver enough gain.

The source $V_{ds,n} - V_{gs,p}$ can also be omitted. The drain of the NMOS must be able to deliver up to V_{DDhigh} to the gate of the driver transistors. Since the driver transistors are already biased at this voltage and the current source is also connected to this high voltage, a voltage shift is not necessary anymore. The resulting circuit shows a biasing scheme with only two sources. The floating voltage source is added to the stimulation source. As pointed out before, this source will most likely implemented using a DAC. It is easy to include a little offset in this source. Alternatively the offset can be canceled using some simple circuitry. Including a copy of both transistors with the appropriate bias, the offset introduced can be substracted quite easily.

Next step is to decide on the bias current and voltages. When deciding on the bias, four factors are important: noise, bandwidth, distortion and slew rate. An additional factor which is partly related to the bias as well is the stability of the system. When considering all these factors one very important thing to realize here is that the system is non linear. The voltage swing over the tissue is very large, which means that the driver transistors operate in the large signal domain. This implies that it is not possible to calculate a loop gain or system poles. Therefore it is also impossible to define a certain bandwidth of the system (it depends on the voltage over the tissue) or to prove the stability by showing the system poles. However, as will be shown next there are ways to deal with this problem.

Noise Noise is of not much consideration here: a noisy gate voltage would yield some fluctuations on the tissue voltage, but this is not of big concern: the signals levels used are quite high, which makes the signal to noise ratio high. Furthermore it is not very problematic to send a noisy signal into the tissue, because the voltage waveform does not need to be very accurate.

Distortion Distortion is also not very important. First let's consider clipping distortion. The biasing of the drain was already discussed and it was assured here that the output stage is able to deliver the maximum voltage of V_{DDhigh} to the gates.

Harmonic distortion is also not a very big problem, since again the output voltage does not need to be very accurate. Slight variation in the tissue voltage do not pose a big problem for the functionality of the device. Furthermore the loop gain is reasonably high due to the CS stage, which will result in a relatively low harmonic distortion. If at some point the distortion needs to be reduced, this can be done by increasing the loop gain (for example increase the bias current or add an extra stage).

Slew rate Slew rate is a large signal parameter and therefore it is no problem for the consideration of this parameter that the system is non linear. The slew rate is the maximum slope of the output voltage (in this case the gate voltage). It is determined by the gate capacitance and the maximum current which can be used to charge it:

$$\frac{dV}{dt} = \frac{I}{C} \tag{4.13}$$

In this case the C_{gs} of the driver transistors form the main capacitance. Again, the exact value of the gate capacitance depends on the bias voltages. However, from the data sheet it was found that the $C_{gs} = 0.0175\,\mathrm{pF}/\mu\mathrm{m}$. Having set $N = 100$ and using the minimum width of $20\,\mu\mathrm{m}$ for a single transistor, the total capacitance is about $35.35\,\mathrm{pF}$.

The fastest signals the system must handle are formed by the burst stimulation pulses with a frequency of about $1\,\mathrm{kHz}$. This means the pulse width is around $500\,\mu\mathrm{s}$. When the tissue voltage needs to switch from $0\,\mathrm{V}$ to V_{DDhigh}, the required gate voltage swing depends on the current, but is usually around $\Delta V_{gs} = 1\,\mathrm{V}$. Assuming now the voltage needs to reach its maximum value within 10% of the total pulse width, a slew rate of $1\,\mathrm{V}/50\,\mu\mathrm{s} = 0.02\,\mathrm{V}/\mu\mathrm{s}$. This means a current of $0.02 \cdot 10^6 \cdot 35.35 \cdot 10^{-12} = 707\,\mathrm{nA}$ is required.

Therefore a bias current of $700\,\mathrm{nA}$ is chosen and the required V_{gs} for this current is found.

'Bandwidth' As explained before the bandwidth of this system is very hard to define, since it is a non linear system. In the next chapter a measure will be given for the 'bandwidth' of the system using simulations.

Stability The stability of the system is also hard to analyse. Since there are no 'fixed' system poles, it is not possible to show (in)stability by defining the poles of the system. A qualitative description can be given however. In some way it is possible to distinguish two time constants (note they are specifically not called poles): one at the tissue and one at the output of the differential pair. The tissue time constant is very variant and cannot be changed. The time constant at the differential pair output consist of the capacitance of the driver transistors together with the output resistance of the differential pair and the current source.

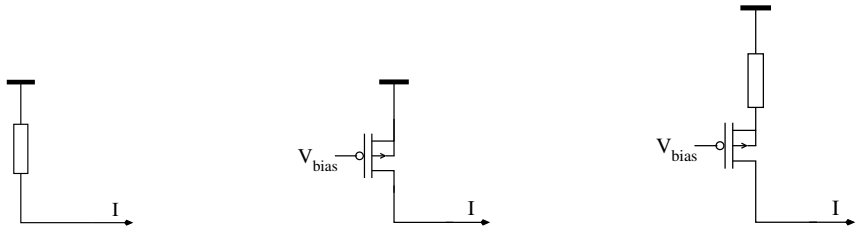
If the frequencies of these time constants are far away from each other, no stability problems are to be expected, since both system 'poles' will be real. If the tissue time constant is getting closer to the time constant of the differential pair (when the time constant becomes smaller, for example due to a smaller C), the poles come closer together and might 'split', yielding complex poles and possible overshoot.

Therefore it is beneficial to make time constant at the output of the diff-pair small. One way would be to implement the current source with a relatively small output impedance. In this way the time constant is kept small. This actually is equivalent to resistive broadbanding. This strategy is paid with a reduced loopgain, but simulations have shown this is not a big problem.

Besides this qualitative approach, it is also possible to make the stability plausible using simulations. A series of transient simulation can be done with different realistic values for the tissue impedance. During these simulations, the stimulation voltage is switched on and off, to account for the switching actions. If all simulations show stable responses, the system is likely to be stable. This does of course not prove stability, but it is a way to make stability plausible in a non linear system. The simulations are discussed in the next chapter.

4.4.1 Current source implementation

For the current source $I_{d,p}$ in Figure 4.23 various implementations are considered. One important criterium is to have an as low voltage drop as possible across the current source. This makes it possible to drive the gates as close to V_{DDhigh} as possible turning them off as much as possible. Therefore an implementation with a single resistor (as depicted in Figure 4.24(a)) is not feasible, since the resistor will introduce a voltage drop. The same holds for a simple transconductance using negative feedback as depicted in Figure 4.24(c). Again a resistor is used, which will lead to a voltage drop.



(a) Resistor (b) Single PMOS (c) Feedback resistor

Figure 4.24: Three alternative current source implementations

The advantage of the feedback implementation is in general the increased output impedance. However, as was seen before, the output impedance can be quite low for stability purposes. Therefore a transconductance without feedback (only a simple CS connected transistor) is considered as depicted in Figure 4.24(b). Drawback compared with the feedback implementation is the reduced output impedance, which is actually beneficial for the stability. Furthermore the accuracy of the

current source is reduced: some fluctuations in the gate voltage will lead to significant fluctuations in the output current.

It is possible to increase the accuracy by introducing a current mirror. The current can then be generated using another current source with a lot of voltage headroom, which makes an accurate implementation possible. For now this source is chosen to be implemented using an ideal current source. In this way the current source together with the current mirror resembles an accurate model for the final current source implementation. The implementation of the current source together with the rest of the stage is depicted in Figure 4.25.

4.4.2 Implementation of the voltage attenuator

The voltage attenuator needs to divide the tissue voltage by a factor 10. This circuit is most easily implemented using a passive circuit. The only thing to consider here is that the tissue voltage can be as high as V_{DDhigh}. This means that the circuit must be able to handle high voltages.

The easiest way to implement a voltage divider is by means of a voltage division over two impedances. Inductors are hard to implement on chip and capacitors do not have a well defined DC voltage division, which means these two options are rejected. Resistors are the only remaining option.

For power consumption, the resistors need to be as large as possible. The highest resistors per unit area available in the technology are called 'pwrne'. This is a diffused resistor formed in the poly area of a pmos transistor. By putting some resistors in series the voltage drop over each individual resistor can be kept in the low voltage regime. the drawback of integrating resistors is that they take up quite a significant space. For now it was decided to implement a $1\,\mathrm{k\Omega}$ and a $9\,\mathrm{k\Omega}$ equivalent resistor. This does not yet consume a lot of chip area.

When it turns out during simulations this value is too small, a voltage division using non linear components can be considered. The complete implementation of the voltage feedback network is depicted in Figure 4.25.

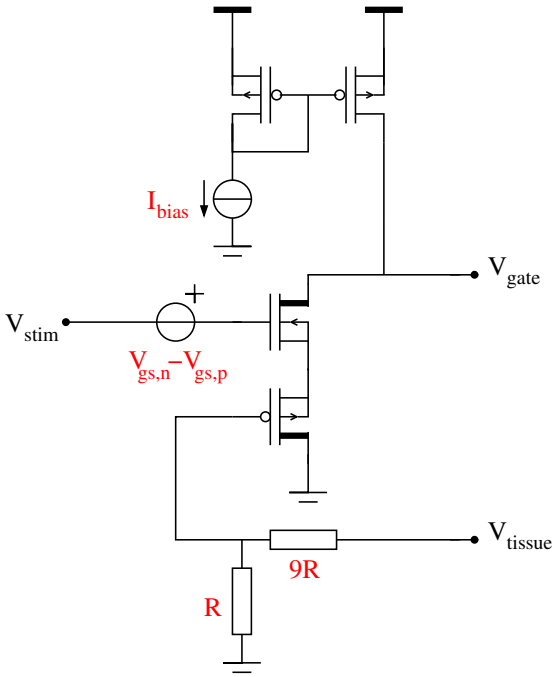


Figure 4.25: Design of the voltage feedback network

4.5 Integrator

The integrator needs to integrate the copy of the stimulation current. Its output is a measure of the amount of charge injected into the tissue. Subsequently a comparator is used to determine at which point a particular amount of charge is injected.

One of the major design challenges of the integrator turns out to be the dynamic range. The input of the integrator consists of the copy of the stimulation current. Most existing stimulators offer a stimulation current range of about 50 μA up to 7 mA as was summarized in table 2.2. Furthermore the pulse width also has a big spread, since it can be chosen somewhere between 1 μs and 1 ms.

If a constant stimulation current is assumed, the injected charge is easily found to be $Q = It$. In the worst case scenario, this would mean that the output can have a dynamic range of 6 decades. Although in practice the high amplitude pulses will most likely have a shorter period, the dynamic range is still very high (for the clinical values entry in Table 2.2 the range is between 90 nC and 8000 nC. If the output of the integrator is a voltage and when assuming only 3 decades of magnitude, on a 3 volt scale a 3 mV resolution at the comparator is required, which is very hard to realize. Therefore a solution needs to be found. Some possibilities are discussed here, each of which can be used in combination with one another.

4.5.1 Integrator architecture

Almost all implementations of integrators somehow use a capacitor as the integrating element (either in an active or passive implementation). The voltage over the capacitor is a measure for the integrated current: $V = C^{-1} \int idt$. To handle the large dynamic range some form of scaling is required. Looking at the equation, the scaling can be done for i, C and V. In the following subsections, this will be treated.

Scaling at the input of the integrator

First of all the input current can be scaled, before it is fed to the integrator. Inputting only a fraction of the current into the integrator and discarding the remaining part will decrease the output voltage with the same ratio. Some advantages and disadvantages are discussed here.

+ The implementation of a current divider is quite simple and efficient. An accurate implementation can be made using the MOCD technique, which is discussed later
+ The scaling factor of the current can be easily controlled using a binary and/or thermometer scheme. This means that a digital circuit can determine the scaling factor required for a certain stimulation voltage.
+ If during the anodic and cathodic phase the same current splitting ratio is used, any static errors in the current splitting will have no influence on the accuracy. If for example the current splitting factor has a particular mismatch, this mismatch is equal for both phases, yielding the same charge injected.
- When a certain part of the current is discarded, this current is wasted. This means an increase in power and heat dissipation. The efficiency in terms of power of the stimulator will not decrease: the copy of the stimulation current was already considered as a 'wasted' current, so by discarding part of it, the efficiency is still the same.

Scaling by changing the integrator itself

Scaling in the integrator itself, can be achieved by changing the value of the capacitor. When the capacitance is increased, the output voltage will be smaller. One way to increase the capacitance is by placing multiple capacitors in parallel.

+ Easy implementation by switching on or off multiple capacitors

+ If during the anodic and cathodic phase the same capacitor is used, no accuracy is lost. If for example due to mismatch a particular capacitor value has a particular deviation, this deviation is the same during both phases.

- Very large area consumption required when C needs a large range. When the C needs to be scaled over 3 decades of magnitude, the area required will be quite significant.

Scaling at the output of the integrator

As pointed out before, the large dynamic range at the output of the integrator will make it very hard to implement a 'simple' voltage threshold detector. By making a tunable voltage comparator, the amount of charge can be decided. However, due to the dynamic range, the resolution required is very high and in combination with tunability this is very hard to realize.

Therefore other ways of converting the voltage at the output of the integrator need to be considered. One quantity that can be implemented in a chip with high accuracy is time. By converting the voltage signal to a quantity related with time, a high accuracy over a large dynamic range can be achieved.

One way to do this is to convert the output voltage into a periodic signal. Each time the integrator reaches a certain threshold, the output is 'flipped'. The output will now consist of a square wave signal of which the frequency is related to the rate of charge injected in the tissue. Each period of the periodic signal corresponds to a certain amount of charge: a charge packet. This periodic signal is subsequently fed into a counter to be able to detect a particular amount of charge packets.

+ The detectable quantity is now converted to time (counting periods). Provided the resolution (charge packet size) is high enough, the accuracy of this method can be very high.

+ The threshold voltage which determines when another charge packet has been injected does not need to be tunable. This means that using a fixed threshold voltage (yielding a simple implementation), still a variable amount of charge can be injected.

+ Static tolerances and mismatches (for example a mismatch in the size of a charge packet) have the same influence during the two stimulation phases, yielding no charge mismatch errors.

- The maximum resolution of this method is bounded by the size of the charge packet. A charge packet must be small enough to be able to have a high enough resolution. On the other hand it cannot be too small, since this would require a large counter, which is also fast enough to count the small packets which are injected fast after each other.

- It is expected that this method has a higher power consumption due to continuous switching of the output signal.

Other techniques

The time constant of the tissue is very large. This means the injected current can be assumed to be relatively constant over time. Therefore the integrator can be turned on and off with a certain duty cycle. For high charge values, the capacitor is turned off relatively long to keep the output voltage low. For example, using a duty cycle of 20% the amount of charge injected is 5 times higher than the output voltage of the integrator.

+ Accuracy is relatively high, given the available clock frequency used for generating the duty cycle is high enough

+ Easy implementation: integrator only needs to be turned on and off

+ Power friendly: when the integrator is turned off, it does not consume power.

- Depending on the time constant of the tissue (which is time variant) and the current waveform, errors can be made when the duty cycle is low. This method assumes a constant current during the off-times. Especially if a non constant voltage waveform is used, the current is also varying. This will lead to errors in the output and in some way the flexibility of the system is therefore decreased: it is not possible to use fast varying waveforms.

Based on the advantages and disadvantages given above, two methods provide high accuracy with an easy implementation: the current splitting and the periodic signal converter. Other methods introduce either errors (time division multiplexing) or yield a complex or inefficient implementation. The two promising methods can actually be used together. The current splitting can be used to make sure the dynamic range of the input current is reduced somewhat. This can also compensate for the large variations in the tissue impedance. Subsequently the periodic signal converter can detect with high accuracy the charge injected by counting the charge packets. An overview is given in Figure 4.26 and the implementation of these systems is considered in more detail now.

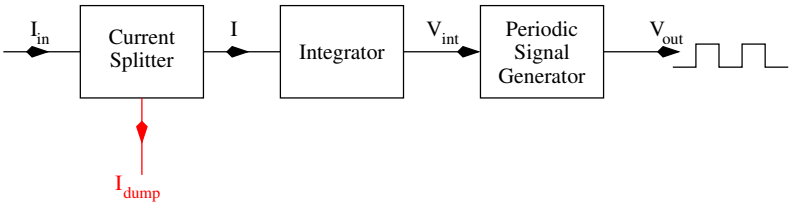


Figure 4.26: integrator system architecture

4.5.2 Current Splitter (MOCD)

A well known and easy implementation of a Current Splitter is called the MOS Only Current Divider (MOCD) [15]. Its principle is based around the circuit depicted in Figure 4.27. Independent of the values of V_{in}, V_a, V_b or the operating regions of the transistors, it holds:

$$\Delta I_{d1} = \frac{-I_{in}}{1 + \frac{W_1}{L_1}\frac{L_2}{W_2}} \qquad \Delta I_{d2} = \frac{-I_{in}}{1 - \frac{W_1}{L_1}\frac{L_2}{W_2}} \tag{4.14}$$

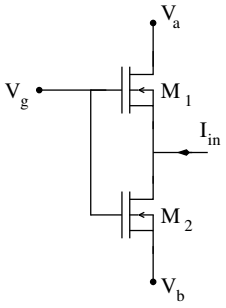


Figure 4.27: Basic principle of the MOCD

Here ΔI_d is the increase in drain current compared to the situation when no input current is inserted (any DC current). Basically the equations show the current division between the two transistors is completely linear and only dependent on the relative sizes of the transistors.

Mismatches in geometry and or gate oxide thickness will lead to static mismatches and not to distortion. This is not important as long as during both stimulation phases the same current division ratio is used: the two phases will now have the same static mismatch. Mismatch in

threshold voltage and channel length modulation will lead to non static errors, much similar as has been seen in the design of the driver stage. These effects need to be taken into account.

First two fundamental implementations are considered for the MOCD. The binary coded implementation is taken from [15]. The thermometer based implementation is a novel implementation.

Binary coded implementation

A binary coded implementation consists of several MOCD stages. In each stage it can be chosen to either attenuate the current with a certain factor or to have no attenuation. In [15] it was chosen to implement a 12 dB attenuation per stage. In principle each attenuation is possible. The principle is depicted in Figure 4.28.

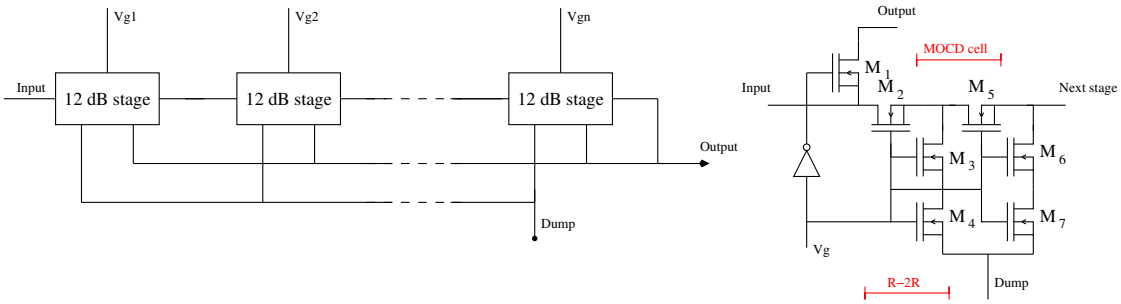


Figure 4.28: Implementation of a binary coded MOCD (block scheme left and implementation of a single block right)

In fact each stage acts as two R-2R ladder network stages. When V_g is enabled, the ladder is turned 'on' and the current will be attenuated with 12 dB before it is fed to the next stage. The 'wasted' current is fed to the dump line. When V_g is disabled, then all the current is fed to the output directly. This means there is no attenuation in this particular stage and the current is fed to the output. Note that each stage can be considered as two R-2R ladder network stages, but it consist of only one complete MOCD stage. At the source of transistor M_2 the current is split between M_5 and $M_3 + M_4$. The second MOCD stage is formed by $M_6 + M_7$ and M_1 or M_2 from the next stage.

Note that in order to make this particular implementation work properly, the output needs to be terminated with two transistors, corresponding to 2R. This can be considered as the characteristic impedance of the ladder network. At the output there should be a transistor with an equivalent size compared to the two transistors ($M_3 + M_4$ or $M_6 + M_7$) from the 12 dB cell.

Thermometer coded implementation

In this implementation only one MOCD stage is used. The principle is depicted in Figure 4.29. The size of the first transistor, which is connected to the dumpline, is fixed (M_2 in the Figure). The second transistor (used for passing on the current) is composed of a number of transistors in series. Depending on how many transistors are switched on, the length of this transistor can be adjusted. Using a number of stages composed of two transistors either an additional transistor can be added, or the current can be fed directly to the output.

This scheme is a thermometer coded scheme (when all transistors are equally sized). Each additional transistor linearly increase the current ratio. Transistor M_1 is a pass transistor and can be used to feed all the current directly to the output, without any attenuation.

The advantage of a thermometer coded scheme over a binary weighted scheme is in general an increased linearity, guaranteed monotonicity and the reduction of glitches. However, for this application, the MOCD does not need to switch during operation of the stimulation. Before the stimulation pulse is applied the MOCD is set to a particular value. This means that no issues are to be expected with glitches.

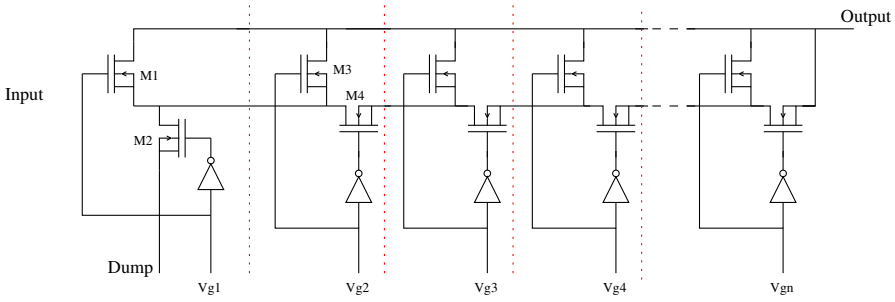


Figure 4.29: Implementation of a thermometer coded MOCD

Furthermore the thermometer based scheme uses more transistors than the binary scheme if the current ratio becomes large. As pointed out, the input current ratio can easily reach 3 decades of magnitude. Using a thermometer coded implementation, 1000 stages are required to reach such a attenuation. To bring down the amplitude this far with the (12 dB) binary coded scheme presented, only 5 stages are required.

On the other hand, using a thermometer coded implementation, the current can be regulated more accurately. The binary coded scheme can only decrease the current by a factor 4 each time, yielding an exponential decrease. Any values 'in between' are not possible. The thermometer coded scheme offers a linear decrease and therefore more values to choose from in the same range.

However, it is not required to adjust the output current so accurate. It is only required to reduce the current to a value low enough so that it can be handled by the integrator. If that means the current is 4 times lower than the maximum current the integrator can handle, this is not a big problem. The 'resolution' will reduce by a factor 4 (since the charge package corresponding to a period of the output also multiplies with a factor 4), but the charge also does not need to be adjusted very accurate.

Therefore it is chosen to opt for the area efficient binary implementation. If it later appears necessary to include a more accurate adjustment, it is always possible to include a thermometer based design.

Output stage

In the discussion of the MOCD as depicted in Figure 4.27 it was assumed a certain DC current is flowing through both transistors, causing a certain V_a and V_b. In this case the *change* in current due to the injection of I_{in} is determined by the relative sizes of the transistors. However, in the discussion of the MOCD as depicted in Figure 4.28, no DC bias current was considered. When the output and dump line voltages however are not equal, this will yield a certain DC current. This can be easily understood by considering the MOCD as being a R-2R ladder network: the output voltage now needs to be equal to the dump line as well.Clearly, a DC current offset is a problem, since it will yield in the integration of current, which is not going through the tissue.

Therefore it needs to be assured the dump line potential is equal to the output line potential of the MOCD. One way to assure this, is by implementing an active integrator block, which will follow the MOCD. An active current integrator has a very low input impedance, yielding a $V_{in} \approx 0\,\mathrm{V}$ when it is grounded. Now the dump line can also be connected to the ground, yielding an equal voltage. However, as will be shown in the next section, an active integrator yields a more complicated implementation and requires biasing, which yields a static power consumption.

Therefore in this section a circuit is considered which is able to assure an equal voltage for both the dump and output line. This circuit requires biasing as well. However, this biasing can be much smaller than the current going through the MOCD, yielding a much lower power consumption compared with the active integrator implementation.

The basic circuit principle used for keeping the dump and output line voltages equal is depicted in Figure 4.30. Transistors M_1 and M_2 conduct the currents through the dump line and the output

line of the MOCD (which actually is an input of this circuit) to ground. The rest of the circuit will make sure that $V_{ds,1} = V_{ds,2}$.

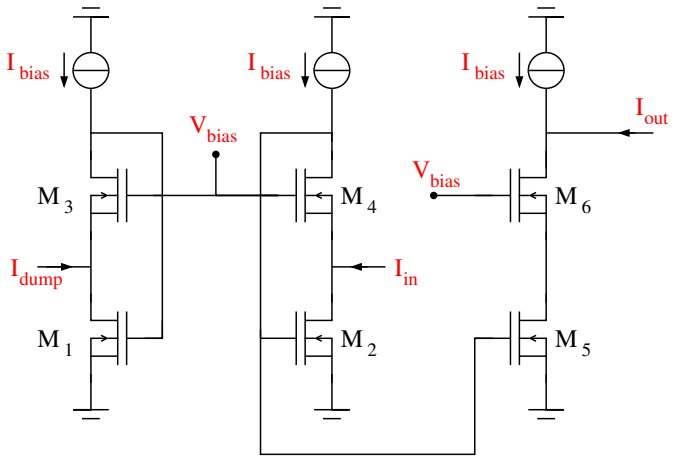


Figure 4.30: Circuit principle used at the output of the MOCD

The gate voltage of transistors M_3 and M_4 is chosen such that the V_{gs} of the transistor corresponds to the value required for conducting I_{bias}. This means that the source voltage of M_3 and M_4 is also fixed, yielding a constant $V_{ds,1}$ and $V_{ds,2}$. The dump and output current of the MOCD need to be conducted by transistor M_1 and M_2, for which the required gate voltage is set by the current source. Since I_{dump} and I_{in} are assumed to be much bigger than I_{bias}, the $V_g > V_d$ for M_1 and M_2, leaving them in the triode region. Note that the drain voltage of these transistors cannot increase, because it is bounded by M_3 and M_4.

The gate voltages of transistors M_2 and M_4 are subsequently copied to transistors M_5 and M_6. In combination with also copying the bias current, the input current of the circuit is copied to the output here. This basically completes the principle of the circuit: the voltage of the input and dump lines are equal, while the input current is copied to the output.

Most important for this circuit is to keep the dump and input voltages equal. Three different situations can be distinguished:

- $I_{bias} < I_{in}$
  This is the operating region intended for this circuit. The gate voltages of M_1 and M_2 are much higher than their drain voltages, yielding a triode operating region. The drain voltages $V_{ds,1}$ and $V_{ds,2}$ are therefore completely determined by the V_{gs} of M_3 and M_4, yielding a constant voltage at the dump and input.

- $I_{bias} \approx I_{in}$ and $I_{bias} > I_{in}$
  When I_{in} becomes comparable to I_{bias}, the situation changes. The gate voltages of M_1 and M_2 are not much higher as their drain voltages. This means these transistors will either not be in triode at all or are at the boundary of being in triode. This also means that the drain voltage is not completely determined aymore by the V_{gs} of transistors M_3 and M_4. Therefore it will in general not hold that $V_{in} = V_{dump}$. This will eventually lead to errors in the MOCD ratio and moreover, the current will not be copied accurately to the output (M_5 and M_6).

- $I_{bias} \ll I_{in}$
  Yet another situation occurs when I_{in} becomes very big compared to I_{bias}. Now a problem starts to occur at transistor M_6. Transistor M_6, being biased with I_{bias} is not able to conduct the very large I_{out} towards the output anymore. This will also destroy the required relation of this block.

This means that only a correct functionality of the system is to be expected when the bias current is small compared to the input current, but not too small neither too big. To be able to handle the large spread in input current that can be expected, it is required to adapt the bias current to the input current. Therefore this circuit will get a variable bias circuit.

The bias voltage V_g from Figure 4.30 is generated by making a copy of transistors M_1 and M_2 which are both diode connected. The gate voltage of the upper transistor is the bias voltage required for this particular transistor. In Figure 4.31 the complete circuit is depicted. For example transistors M_7 and M_8 are used for this purpose: they are biasing the gate voltage of transistors M_3 and M_4. The same holds for transistors M_9 or M_{10}, biasing M_6. It is explained later why not transistor M_7 and M_8 are used for transistor M_6 as well.

The adaptive character of the bias is realized using transistors $M_{11} - M_{17}$. As can be seen, the input current through M_1 is copied at transistor M_{11} and M_{12} using a certain ratio. Subsequently this current is used for biasing by copying it to transistors $M_{13} - M_{17}$, realizing the adaptive biasing.

Next aspect to consider is the stability of the system. Simple simulations quickly showed the system is showing an oscillatory behaviour. Analyzing the stability of the system in a quantitative way is however not straightforward, since the system is nonlinear. The biasing depends on the input current and this will make the poles of the system shift when the input current varies.

One loop which leads to instability can be easily eliminated. When the gate of M_6 is biased using M_7 and M_8, a loop is created via the C_{gs} of M_6, M_4, M_2 and M_5 back to M_6. Therefore the gate of M_6 is biased using two additional transistors M_9 and M_{10}.

Transistors M_1 and M_3 form a loop, just like transistors M_2 and M_4. These loops also give rise to instability. One way to solve this is by applying pole splitting at transistor M_1 and M_2 by inserting a capacitor between the gate and drain terminals. This is also shown in Figure 4.31. Due to the non linear nature of the circuit the value of this capacitor needs to be found using simulations.

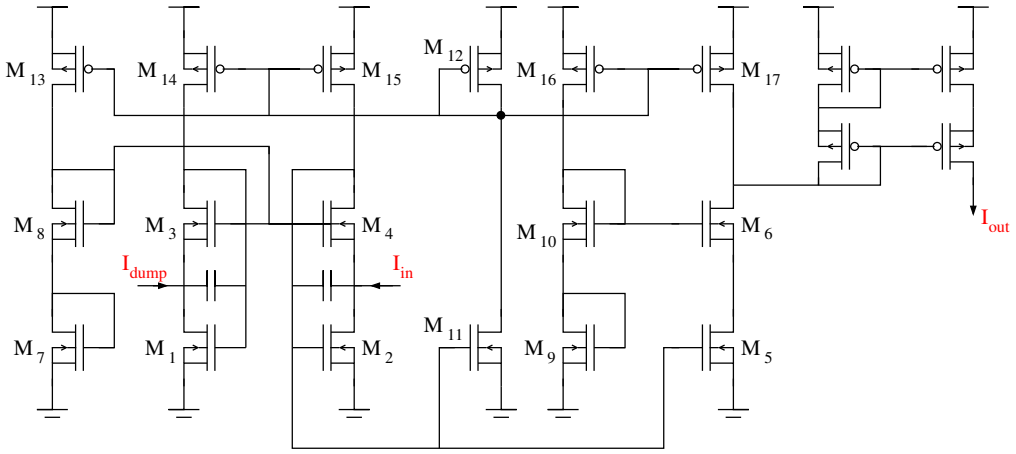


Figure 4.31: Complete circuit of the MOCD output stage

Note that the copying of the output is not perfect. The drain voltages of transistors M_4 and M_6 are not equal and the output current needs to be conducted by transistor M_6 and not by M_4, which yields errors. Using simulations it needs to be found how big this error is and if it is tolerated.

Second order effects

As pointed out before both threshold voltage mismatch and channel length modulation will have influence on the performance of the MOCD. For reasons similar to the ones described while

discussing the driver block, it was chosen not to account for the threshold voltage mismatch in the design. The channel length modulation was however taken into account.

In the binary based MOCD implementation, channel length modulation has some influence, despite the fact that the dump and output line voltages are equal. Since the circuit is based around a R-2R ladder network, the voltage over the individual components varies. This means the current division is slightly influenced by the channel length modulation. Using simulations the severity of this problem needs to be found. It is possible to reduce its effect by increasing the length of the transistors.

Note that a thermometer based MOCD has no channel length modulation effects (as long as the dump and output line voltages are equal). A thermometer based MOCD effectively consists of only one stage, yielding the same V_{ds} over the two transistors.

4.5.3 Integrator and periodic signal generator

The purpose of this circuit is to create a periodic signal based on the current injected by the input signal. The principle of the system should be to integrate the input current towards a certain (fixed) threshold. This threshold should be detected by a comparator which then triggers a mechanism to create the periodic signal. Since the input signal is fixed, the design parameters for this circuit include the threshold and the way the periodic signal is realized.

Single threshold design

If a design is chosen with a single threshold it has certain implications for the architecture to the rest of the integrator. The basic idea is that the integrator will integrate up to a threshold value. At this point the integrator is reset in order to be able to integrate towards the threshold again. It is important that the integrator is able to integrate continuously in order not to 'miss' any current injected in the tissue. This means that it is not possible to reset the integrator once the threshold is reached without having another mechanism which is able to integrate during the reset time. This basically means a single threshold design needs two integrating elements at least if a reset is required.

Single threshold, two integrators One way to realize this system is using two separate integrators, as depicted in Figure 4.32(a). One of them is reset, while the other one is integrating the input current until the threshold voltage is reached. At this point both integrators swap tasks: the first one will integrate the input current, while the other one is reset again.

The output voltage of this circuit is sawtooth shaped for a constant current input: the integrator output is a slope until the threshold voltage. At this point a step is made towards the reset voltage of the second integrator. This is depicted in Figure 4.32(d).

Single threshold, multiple capacitors Instead of having two integrators, it is also possible to only copy the capacitor itself, as depicted in Figure 4.32(b), but without the upper capacitor. Instead of switching between integrators, the switch is made between capacitors. While one capacitor is integrating, the other one is disconnected from the circuit and reset. Once the first capacitor has reached threshold, the positions are swapped. Again this will result in a sawtooth shaped output voltage (as in 4.32(d).

Drawback of both designs is that during the switching action, it is not sure how the integrator will behave. If the integrator or capacitor which has reached threshold is switched off before the second integrator or capacitor is enabled, the input current cannot be integrated for a short period of time.

In case of the capacitor this can be solved by placing a third capacitor which is permanently connected to the integrator, as shown in Figure 4.32(b). During switching this third capacitor makes sure the integration is continuously. When the cleared integrator is connected somewhat later charge redistribution takes place and the system can integrate correctly towards the threshold again. Note that using this third capacitor the output voltage swing is reduced. With two

capacitors the output voltage is swinging between the threshold and reset voltage. However due to the third capacitor the output is not reaching the reset voltage anymore, but an intermediate voltage, depending on the ratio between the two capacitors and the third capacitor. This is depicted in Figure 4.32(e).

The concept of the third capacitor is harder to implement for the system with two integrators. This is due to the fact the multiple capacitors are placed in parallel. It is not possible to place a third integrator in parallel with the other two, since the output is voltage based.

Another fundamental problem with a single threshold system is timing. When a comparator is detecting the threshold is reached, its output flips. This flipping can trigger a couple of switches which make sure the element which has been reset is connected and the other one is disconnected in order to get reset. However as soon as the new element is connected, the output voltage is stepped down.

This will make the comparator to flip back, since the output voltage is now under the threshold again. At this point it must be prevented that the switches which control the integrator or capacitor also flip back. This means there is a memory element required to store the state of the system (which element is connected and which one is being reset).

The situation described above can yield timing problems. It must be made sure that the new state of the memory is completely switched and does not accidentally 'flip back', although the output of the comparator might have switched back earlier.

Single threshold, flip single capacitor One way to overcome the need of a second integrating element is by reversing the terminals of the capacitor as soon as the output reached threshold, as depicted in Figure 4.32(c). This will also flip the voltage. This is actually equivalent to resetting the integrator, but now the capacitor is able to continue integrating immediately, ignoring the time it takes to switch the terminals of the capacitor. It is assumed this time can be very short, yielding only minor errors. The output is depicted in Figure 4.32(f) in which the negative voltage is clearly visible..

The big problem however is that this system requires negative voltages. Since the rest of the system is designed for positive voltage only, this is a sincere disadvantage. Furthermore this implementation does not solve the timing issues. Therefore a closer look is taken at systems with multiple thresholds.

Multiple threshold design

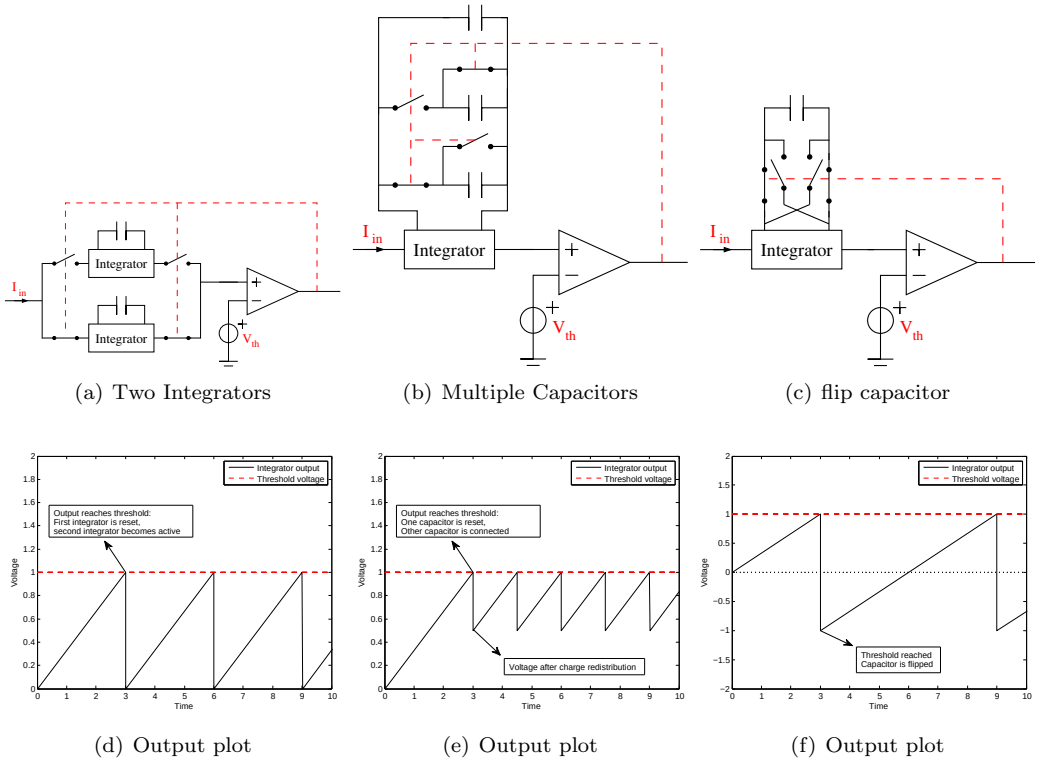
If a system is designed with multiple threshold voltages, the situation is slightly different. There is no need anymore for multiple integrating elements. When one threshold is reached, the system can start integrating towards a second threshold, without the need for having it reset. This means it can operate constantly, eliminating the need for a second integrating element.

Since two thresholds are enough to eliminate the need for multiple integrating elements, only systems with two threshold levels are considered here. The output waveform is triangular, assuming constant current input: the voltage is continuously switching between the two thresholds.

One way to have the system switch between two thresholds is to flip the input current of the integrator as soon as a threshold has been reached. This flipping can be done easily by using a current mirror. The two threshold voltages can be easily implemented using a Schmitt Trigger circuit.

The advantage of this system is that the timing problem described in the previous section is solved. When the first threshold voltage is reached, the comparator will switch. However, it will not switch back before the second threshold is reached.

Because of the easy implementation and the advantage of having no timing issues, the system with two thresholds is chosen. An overview of this implementation is given in Figure 4.33.



(a) Two Integrators (b) Multiple Capacitors (c) flip capacitor

(d) Output plot (e) Output plot (f) Output plot

Figure 4.32: Three different integrator implementations using a single threshold level

Implementation of the integrator

As described above the integrator can be implemented using a passive or active implementation. The passive implementation is the easiest, since it consists of simply one capacitor. An active implementation needs an op-amp implementation and yields an inverting transfer, although this last aspect is not important anymore in the schmitt trigger based design.

Because of the sake of simplicity it is decided to implement the integrator in a passive way first. The drawback is that the input voltage is varying now (depending on the threshold voltages of the Schmitt Trigger). When this imposes a problem later in the design, the integrator can be made active.

The value of the capacitor determines, together with the input current and the threshold levels, the output frequency. To determine the capacitor value, all these quantities need to be known. For now some assumptions are made and an example calculation is done. The speed of the digital circuit which will count the periods determines the maximum possible frequency. It is assumed the maximum frequency is set quite low at 10 kHz. First of all this is done to be 'on the safe side'. Furthermore it is to be expected that the frequency of the digital network will be quite low to safe power consumption. Assume further that the Schmitt Trigger threshold values are about 2 V from each other. This means the capacitor needs to overcome a 4 V difference each period (charging and discharging). If the maximum current through the integrator is assumed to be 1 μA (reasons for this will become clear later), the capacitor value is:

$$C = \frac{It}{2\Delta V} = \frac{1\,\mu\text{A} \cdot 100\,\mu\text{S}}{2 \cdot 2\,\text{V}} = 50\,\text{pF} \tag{4.15}$$

This capacitor value can be implemented on chip without too much difficulties and area consumption. Chosen was to use a 'MIMC'-cap, the capacitor with the largest capacitor value per unit area. A 50 pF MIMC capacitor uses an area of about 80 μmx80 μm.

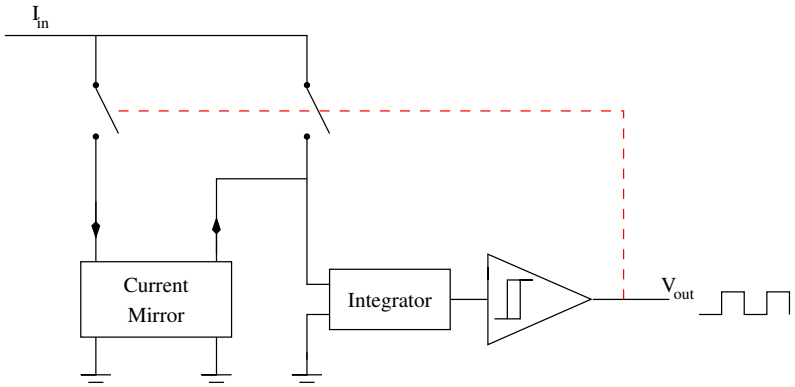


Figure 4.33: Block scheme of the integrator and comparator combination

Implementation of the current mirror

A basic current mirror is easily implemented using two transistors. Any static errors in mismatch do not play a role here, very similar as in the case of the driver transistors. Therefore size mismatches do not play an important role, since they cancel each other during the two phases.

Threshold voltage mismatch plays a similar role as in the driver transistors. A similar graph as depicted in Figure 4.9 holds for this current mirror. Therefore mismatches of around 10% can be expected. For now it is decided not to take any design measures for this.

Channel Length modulation is investigated in more detail. First it has to be decided if channel length modulation has a negative effect at all. The output of the current mirror is connected to the integrating capacitor. This means the output voltage will continuously swing between the two threshold voltages. The output current of the current mirror can be expressed as follows:

$$I_d(t) = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \left(V_{gs} - V_t\right)^2 \left(1 + \lambda V_{ds}\right) = I(t) \left[1 + V_{ds}\lambda\right] \tag{4.16}$$

this current is fed into the integrator. The output voltage V_{out} of the integrator is also the V_{ds} of the current mirror output. This yields the following equation:

$$V_{out} = \int I_d(t)dt = \int I(t) \left[1 + V_{out}\lambda\right] dt = \int I(t)dt + \int I(t)\lambda V_{out}dt \tag{4.17}$$

This equation cannot be solved analytically, since no closed form for V_{out} can be obtained. Therefore a numerical approach is used to investigate the effect of channel length modulation. The equations are implemented in a Simulink blockscheme, as depicted in Figure 4.34.

Using the two identical blocks on the left side, the function $\int I(t) \left[1 + V_{out}\lambda\right] dt$ is implemented. The constant at the most left part represents the input current $I(t)$ and can be given any value (or other shapes, using different source blocks). In the right part a threshold detection is implemented. Different waveforms can be injected and it can be seen when a certain threshold is reached. Various simulations show that the threshold is reached at the moment which is expected, independent of the channel length modulation. To illustrate this, a couple of voltage outputs of the integrator are depicted in Figure 4.35.

All plots in the figure contain the simulation result of a DC input signal. As can be seen,the effect of channel length modulation is very clear: the current increases for increasing output voltages. In the first figure the voltage is compared with the case of a sinus wave, which has the same DC value and an amplitude equal to the DC voltage. Despite of the large variations of the sinus, the integrator still reaches the same values. The same holds for a block shaped wave with a duty cycle of 10% and an amplitude of 10 times the DC current.

In the last plot the DC current is compared with the same DC current to which strong noise is added. The noise varies the signal almost between 0 A and 2 A. As can be seen, still the integrator is integrating towards the same value, despite of the channel length modulation.

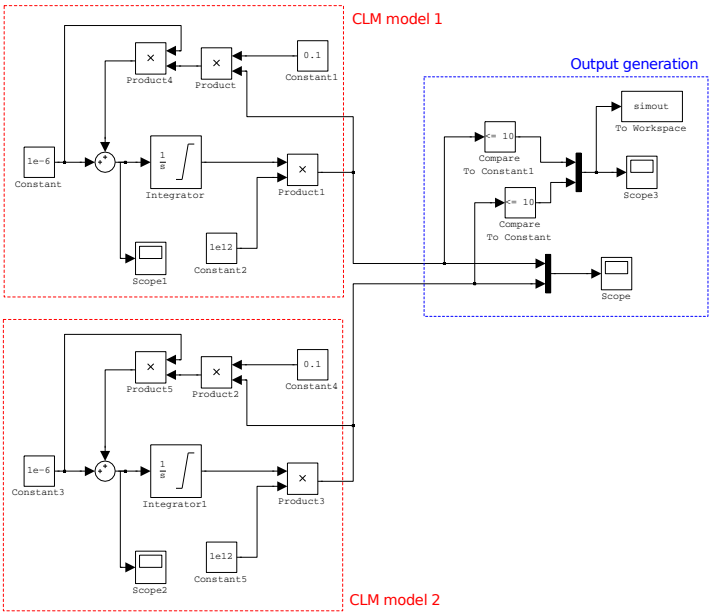
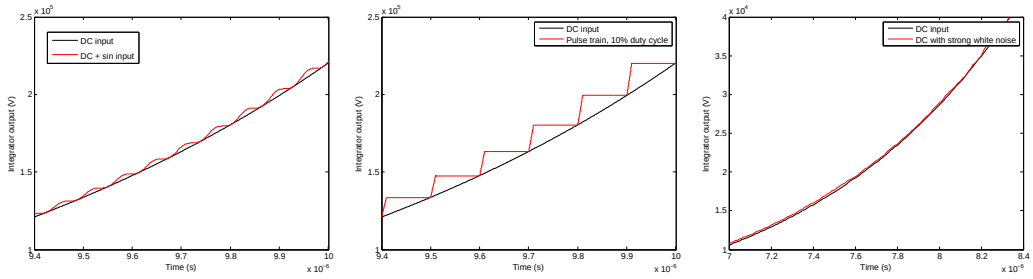


Figure 4.34: Simulink block scheme to compare the effect of channel length modulation for two inputs



(a) Sinusoidal shape (b) Pulse train (c) Noise

Figure 4.35: Some outputs of the Simulink simulation shown in Figure 4.34

From the simulations it can be concluded that channel length modulation has no influence on the integration. This can also be understood qualitatively. Channel length modulation will increase the output current while integrating, thereby introducing mismatches in the current. However, because of the periodic nature, each period, the same mismatch will be generated. When large currents are injected, the effect of the channel length contribution is larger. However, the output of the integrator will also increase quicker, which means the increased effect takes place for a shorter amount of time. The simulations show these two effects exactly cancel each other.

Therefore it is not necessary to include any measures to fight channel length modulation.

Implementation of the switches

The switches are used to reverse the current which is sent into the integrator. The switch needs to conduct voltages over the complete spectrum of almost 0 up to V_{dd}. Consider for example when the current is not going towards the current mirror, but directly in the capacitor. Now the voltage can be anywhere between the two threshold values, which are most likely chosen to be close to 0 and V_{dd} to have maximum voltage swing. This implies that a single transistor cannot handle

this voltage range and instead transmission gates are required (NMOS transistors are for example turned off when they need to conduct a value close to $V_{dd} = V_g$).

The voltage over the capacitor is bounded between the two threshold voltages. This is ensured by the Schmitt trigger. The voltage at the input of the current mirror is determined by the V_{gs} of the input transistor, which is dependent on the input current.

Implementation of the Schmitt trigger

For the design of the Schmitt trigger various designs are considered. Two well known fundamentally different designs are treated, which are also discussed in [63]. The first one uses an op-amp based implementation. The second one is based around cross connected CMOS inverters.

Op-amp based design The function of a Schmitt trigger is defined as being a comparator type of circuit of which the threshold voltage depends on the 'state' of the schmitt trigger. Therefore a straight forward implementation would be using a comparator circuit based around an op-amp. The threshold voltage is made dependent on the output state by adding positive feedback in the form of an additional resistor. This is resistor R_3 in the left part of Figure 4.36.

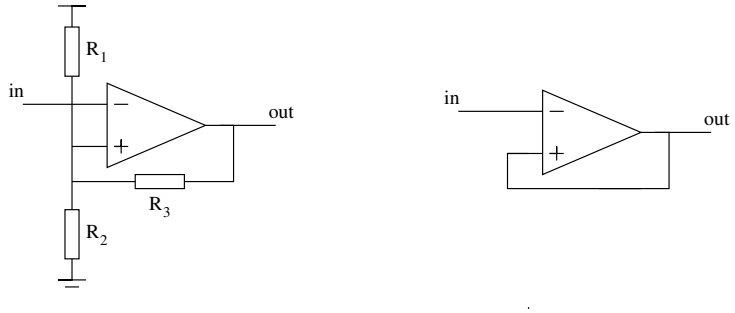


Figure 4.36: Opamp based Schmitt trigger implementation with tunable threshold voltages (left) and fixed (right)

Analysing the circuit in its two states (when $V_{out} = 0$ and $V_{out} = V_{dd}$), the values for the two threshold voltages V_L and V_H are found easily:

$$V_L = \frac{R_2||R_3}{R_1 + R_2||R_3} V_{DD} \qquad V_H = \frac{R_2}{R_2 + R_1||R_3} V_{DD} \tag{4.18}$$

Since resistors with a high value are hard to implement on chip, it is seen what happens with the threshold voltages when they are omitted. Subsequently $R_2 \to \infty$, $R_3 \to 0$ and $R_1 \to \infty$, which will lead to the circuit depicted in the right part of Figure 4.36. For this circuit $V_L = 0$ and $V_H = V_{DD}$. For the application in the stimulator this is a perfect situation: the voltage swing over the capacitor is maximum. This means the full range of the capacitor is used, which means this area hungry component is optimally used.

The implementation of the op-amp is realized using a differential pair. This differential pair needs to be biased. However, since the opamp is used in a positive feedback scheme, it is not operating in a linear regime. Instead it is always pushed into one of the two states: one of the transistors in the differential pair will be turned on and one will be off all the time. Realizing this it is still possible to consider the differential pair from a bias point of view, as depicted in Figure 4.37.

In the first subfigure a completely biased stage is depicted. After I-shifting the current sources, the current source parallel to the lower drain voltage source can be omitted. The upper drain voltage can be set zero: it only determines a voltage shift between the source voltage and the the output voltage when the upper transistor is turned on. The source voltage can be made equal to the output voltage. Furthermore the gate bias voltages can be omitted as well. The input voltages

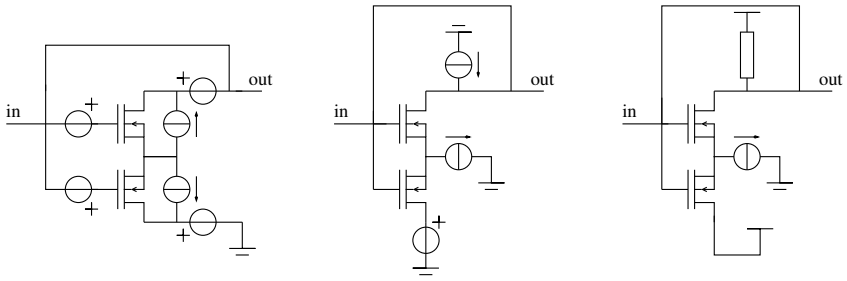


Figure 4.37: 'Biasing' of the differential pair to implement the Schimtt trigger

of the circuit itself can be used to bias these transistors. This means the source voltage is shifted with respect to the input voltage. This also means that when the input voltage is zero, the source voltage might become negative. This will be 'fixed' in a later design step.

Implementing the simplifications described above will lead to the circuit in the middle of Figure 4.37. The drain bias voltage of the lower transistor needs to be V_{dd}, since the output voltage switches between 0 and V_{dd}. Furthermore the upper current source is implemented using a single resistor. This will result in the circuit depicted in the right part of Figure 4.37. This circuit is equivalent to the one which is presented in [63].

The advantage of considering the circuit using the bias approach is that more insight is given in the way the circuit works. Discarding the gate biasing, means a voltage shift is created between the input of the transistor and the source. When the upper transistor is turned off, the output voltage is high (no current flows through the resistor). Since the gate bias source is omitted, the source voltage is equal to $V_{dd} - V_{th}$, enough to keep the lower transistor turned on. This can be seen in the plot of Figure 4.38, a simulation result of the circuit. When the input voltage becomes high enough to turn on the upper transistor, the output voltage flips towards $V_{dd} - IR$. The source voltage gets the same value (since the upper transistor is turned on).

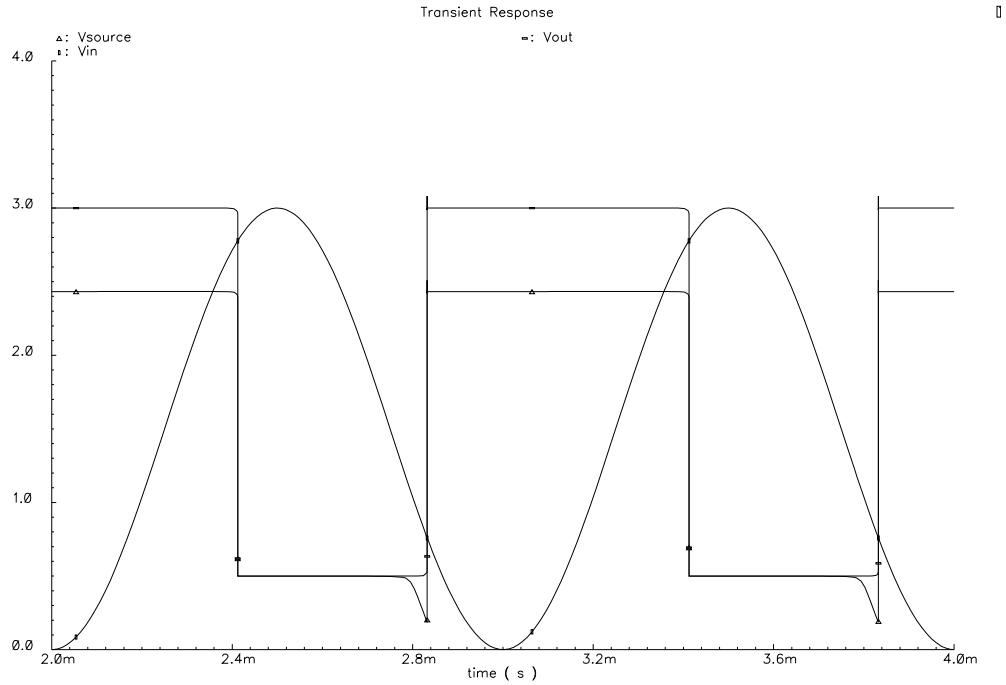


Figure 4.38: Simulation results of the right circuit from Figure 4.37

When the input voltage decreases towards $V_{in} < V_{out} + V_{th}$, the source voltage is pushed lower.

This is to keep the upper transistor turned on. However, when the source voltage becomes small enough to turn on the lower transistor on (of which the gate voltage is fixed at V_{out}), the circuit flips back to the beginning of the cycle: the output voltage becomes $V_{out} = V_{dd}$ again. As can be seen from the simulations, the threshold voltages of this design are:

$$V_L = V_{DD} - IR - V_{th} \qquad V_H = V_{DD} - IV_{gs,on} + V_{th} \tag{4.19}$$

Here $V_{gs,on}$ is the gate source voltage over the lower transistor when it is turned on.

As is clear the circuit can only switch back if the source voltage can be pushed far enough under V_{out} in order to switch on the lower transistor. This means the circuit relies on the fact that the output is not pushed down towards 0 V, but towards $V_{dd} - IR$. In [63] the voltage at the gate is pushed towards 0 using inverters as depicted in Figure 4.39. The only reason this circuit still works is because of the non ideal implementation of the current source (using a single transistor as a transconductance). This will push the source voltage slightly higher, which makes it possible to turn on the lower transistor. This means the lower threshold of this circuit is not very well controlled anymore, but instead relies on the non ideality of the current source implementation.

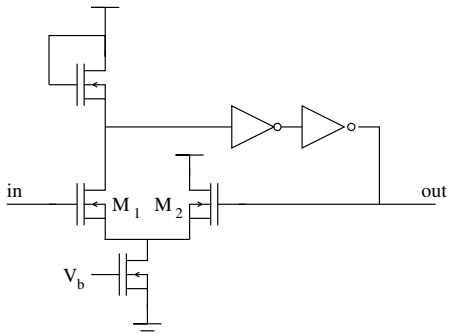


Figure 4.39: Possible implementation of the Schmitt trigger [63]

Furthermore, it is found that the design quite heavily relies on the relative sizing of the transistors. The resistor is implemented using a diode connected MOSFET to reduce the need for a large area resistor. This means the current must be matched to the diode well enough to achieve the required voltage swing. Furthermore the voltage swing allowed is also affected by mismatch in the inverters which were added to increase the output voltage swing: the voltage at the diode must cross the threshold voltage of the inverter. This means there is a lot of interdependency of component parameters in this design. Although this does not pose any limitations on the feasibility of the system, it makes designing this circuit more complicated. To illustrate this: simulations have shown that for a bias current of 1 μA, the sizing of the inverter only works on a size interval of 0.5 μm.

Another problem with this circuit is speed. When transistor M_1 is switched on, the voltage at the diode decreases. However, it takes a while before this decrease is translated towards the output. First of all it needs to propagate through both inverters. Furthermore the current which needs to discharge the node at the drain of M_1 is limited. At the moment M_1 switches, M_2 is also still on, since the voltage at its gate needs to wait for the inverters to propagate the decrease. This means that the current from the current source splits between M_1 and M_2. Since M_1 is connected in series with the diode, most current will still flow through M_2, while it should flow through M_1 to discharge the diode. Therefore switching takes a relatively long time.

This is also illustrated using a simulation. The complete integrator circuit is simulated using the above mentioned Schmitt trigger. Three different DC currents are chosen as the input: 10 nA, 100 nA and 1 μA. The voltages over the capacitor are plotted in Figure 4.40. A more detailed description about how exactly this simulation results were obtained can be found in the next chapter. For now it's important that when there is a delay in the switching action, the capacitor will continue integrating for a while, before the current is switching polarity. When the current

is relatively high, this extra delay will result in quite significant increase in voltage. This can be clearly seen in the figure: when the input current is high (high frequency), the amplitude of the capacitor voltage is much higher.

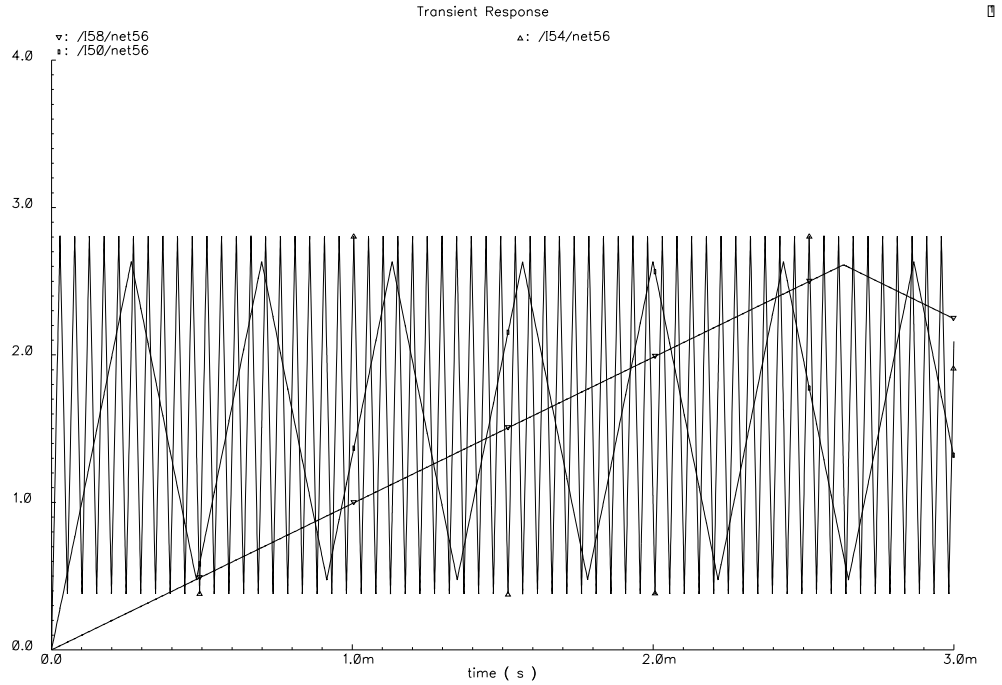


Figure 4.40: Capacitor voltages in the integrator using three DC current inputs

This will result in a longer period and therefore relatively lower frequency for high input currents. To illustrate this: the 100 nA input current will result in a 2.3 kHz signal, while the 1 mA current results in a 20.5 kHz signal. This means the schmitt trigger introduces a delay which is too large to have an accurate periodic signal conversion.

Taking a step back, there is also a more fundamental limitation of this design: it needs a constant bias source to operate. This means the circuit has a static power consumption. The minimum bias current is hard to calculate exactly, but the bias current determines the loopgain of the Schmitt trigger and therefore its speed. The current also determines the voltage drop over the diode. This voltage drop needs to be sufficient to let the input of the inverter fall under its threshold.

Despite its simple implementation discussed here, this circuit poses some problems in terms of accuracy. Therefore other circuits are discussed as well.

CMOS inverter based design

The basic concept of a CMOS inverter based design is depicted in Figure 4.41 and is also discussed in [63]. The basic operation is formed by the cross coupled inverters. A single inverter has a certain V_{th} for which the output is switched. In the cross coupled inverter pair, the effective threshold is changed, depending on the value of the output. This will change the threshold value, yielding a Schmitt trigger functionality.

Consider the case when a low voltage is at the input of the cross coupled inverter pair (V_x in Figure 4.41). M_3 is on, yielding a high output voltage. This output voltage will activate M_6. This will further push down the voltage at V_x. This will make it harder for the input inverter (consisting of M_1 and M_2) to pull up this node and switch the cross coupled inverter pair. This means M_1 needs to be activated 'stronger' (a lower input voltage) before it can overcome the power of M_6 in the cross coupled pair. This effectively reduces the V_{th} of the complete circuit. For a low input

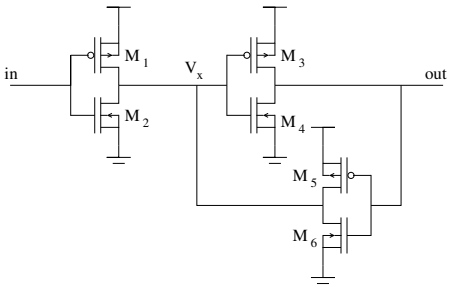


Figure 4.41: Inverter based Schmitt trigger

signal a similar reasoning holds, which wil lead to an increase of the V_{th}. For proper operation of this type of Schmitt trigger it is obvious the input inverter needs to be stronger than the cross coupled inverter pair.

The big advantage of this type of Schmitt trigger is that no static bias current is required. This means the static power consumption is very low. Especially if the input voltage is made 0 while the Schmitt trigger is inactive, there is no DC patch to ground.

The V_L is determined by the voltage division at V_x between M_2 and M_5 in combination with the threshold voltage of the inverter M_3+M_4. It has to be determined for which input voltage ($V_{gs,M2}$) V_x will cross the threshold voltage of the inverter M_3+M_4. M_5 is assumed to be in the linear region ($V_{gs} = V_{dd}$), while M_2 is assumed to be in the saturation region ($V_x \approx V_{dd}/2$). Stating $I_{d,m2} = I_{d,m5}$, this yields:

$$\frac{\mu_n C_{ox}}{2}\frac{W_n}{L_n}\left(V_{gs}-V_t\right)^2\left(1+\lambda V_x\right) = \frac{\mu_n C_{ox}}{2}\frac{W_p}{L_p}\left[2(V_{dd}-V_t)(V_{dd}-V_x)-(V_{dd}-V_x)^2\right] \tag{4.20}$$

Now discarding channel length modulation ($\lambda = 0$) and assuming $V_{dd} - V_x \ll 2(V_{dd} - V_t)$, the following expression is found:

$$V_x = \frac{W_n L_p}{L_n W_p}\frac{(V_{gs}-V_t)^2}{2(V_{dd}-V_t)} \tag{4.21}$$

It can now be found for which V_{gs} the V_x is equal to the threshold voltage of the inverter M_3+M_4. A similar derivation can be done for V_H. It is easily seen the value of the threshold voltages is very dependent on the size of the transistors, the threshold voltages and the power supply.

This means that mismatch in any of these quantities will lead to a shift in the threshold voltages of the Schmitt trigger. All static errors are in principle no problem (they will not lead to charge mismatch), since it will only affect the period, but this is equal during both stimulation phases. Other dependencies, such as the supply voltage, will affect strongly the period of the output of the schmitt trigger. Therefore this design is considered to be not robust enough for this application.

Threshold compensated inverter based design

A new Schmitt trigger design is based on the threshold compensated inverter introduced in [72] and used for different applications in [37] and [25]. The basic idea is to have an inverter for which the threshold voltage can be set. In all applications described this was used to design an inverter with a fixed threshold voltage which is robust for process variations. In this design the threshold is not only set, it is also varied to construct the functionality of a Schmitt trigger. Remember that in fact a Schmitt trigger is nothing else than a comparator with two threshold voltages.

The basic circuit implementing the threshold compensated inverter is depicted in Figure 4.44. The basic inverter is formed by transistors M_1 and M_2. Transistors M_3 and M_4 are duplicates of M_1 and M_2 with the required V_t at its input. The output of these transistors V_g determines the gate voltage of transistors M_5-M_8. Transistors M_7 and M_8 form a feedback loopt with M_3 and M_4 and are biased in such a way that their equivalent resistance R_{ds} will set the threshold of the inverter formed by M_3 and M_4 exactly at V_t.

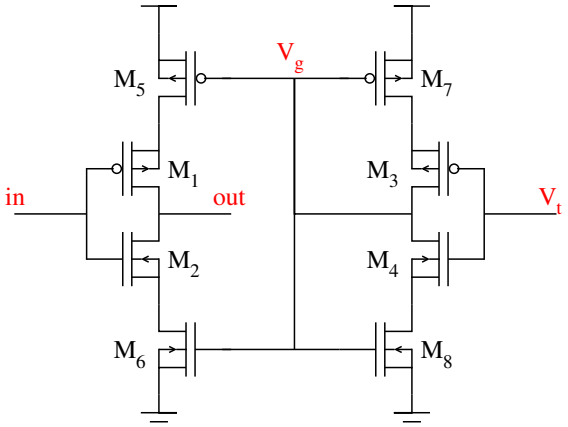


Figure 4.42: Threshold compensated inverter [72]

For example, if V_t is set at $V_{dd}/2$ and both M_3 and M_4 are equally strong, transistors M_7 and M_8 will have the same R_{ds}. However if due to for example mismatch M_3 is much stronger, the power of this transistor is decreased by biasing M_7 with a much higher R_{ds} than M_8. This will weaken M_3 again, bringing the threshold at $V_{dd}/2$.

Transistors M_5 and M_6 are copies of M_7 and M_8. This means they will affect the inverter formed by M_1 and M_2 in the same way as M_3 and M_4. Since these inverters are identical, the threshold voltage set by V_t will also be transferred to M_1 and M_2. Note that the correct working principle of this circuit relies on the matching of the transistors M_1-M_3, M_2-M_4, M_5-M_7 and M_6-M_8. It is still possible that mismatches will be present, but it is already a big improvement compared to the cross coupled 'normal' inverter.

As explained this circuit can be used in a Schmitt trigger when the threshold voltage is made dependent on the output voltage. This is depicted in Figure 4.43. The threshold compensated inverter is the first inverter in the chain and has an additional input, representing the V_t. As can be seen, the threshold compensated inverter is followed by a normal inverter first. This is done to make the output square shaped, since the output of the threshold compensated inverter is not completely square shaped. This is due to the fact that the slope of the input voltage may be quite low, which will lead to some transition effects around the threshold voltage. This is unwanted for the switch which controls the threshold voltages.

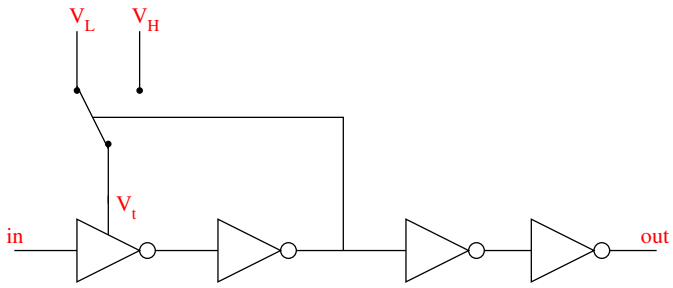


Figure 4.43: Threshold compensated inverter based Schmitt trigger

Subsequently this square shaped voltage is used to control the threshold voltage of the first inverter. The threshold voltages can in principle be freely chosen to be $0 < V_L, V_H < V_{dd}$. The two additional inverters are added for timing purposes. It is important for the Schmitt Trigger that the threshold voltage is changed before the output (and with that the direction of the current) is reversed. If the current is reversed before the threshold voltage is changed, the Schmitt trigger will switch back immediately. Therefore two inverters are added to introduce a small delay to

guarantee the schmitt trigger first changes its threshold voltage and then switches its output.

The main advantages of this design include its simplicity and the robustness against process variations.

Power consumption When considering the power consumption of the threshold compensated inverter a problem is found. Consider the situation in which the threshold is set at a value close to $0.5V_{dd}$. In this case the inverter M_3 and M_4 is close to its 'natural' threshold, which means both the NMOS and PMOS transistor are 'on'. This means there exists a DC path from V_{dd} to gnd through M_7, M_3, M_4 and M_8, yielding a very high static power consumption. Two possible solutions exist:

- Choose V_t to be close to gnd or V_{dd}. In this case the V_t set will be far away from the 'natural' V_t of the inverter. This means that the equivalent resistance of M_7 or M_8 will need to become very large to compensate for this. A large resistance means a low current.

  For this particular application, a V_t which is close to V_{dd} or gnd is beneficial. As explained before in this way the full voltage range of the capacitor is used and therefore the capacitor is used at its maximum efficiency.

- The length of transistors M_5, M_6, M_7 and M_8 can be increased. In this way the resistance of these transistors increases, yielding a lower static current through the right branch of the circuit.

These methods can be used in combination with each other. However, they will have some negative consequences on the performance of the circuit. By increasing the resistance of transistors M_5 and M_6, the output current will decrease. This will decrease the speed of the circuit: it will take longer to switch the output ((dis)charging the next inverter).

Increasing the length also increases the capacitive load at node V_g. This means it will take longer before the V_g required for the new V_t is reached. If the input current is high, it might reach this threshold before V_g reaches its final value. This means the Schmitt Trigger will switch back sooner, which will effect the period of the output signal. Note that due to the fact 4 transistors are affected by the increase of the length, this effect is quite strong.

Simulations confirm the statements made above. Using a combination of the methods described above, the amplitude of the capacitor voltage is very much dependent on the input current, similar to the results found in Figure 4.40. This indicates a lack of speed at the output.

Therefore a redesign of the threshold compensated inverter is required. The fundamental reason the length of the transistors was increased, was to increase the resistance in the right branch of the circuit formed by M_3, M_4, M_7 and M_8. The fact that this also decreased the maximum output current of the circuit was because it was assumed M_5 and M_6 need to have the same size as M_7 and M_8. It is considered now if M_5 and M_6 indeed need to be the same length.

The principle of the circuit is such that the *relative* equivalent resistances of M_7 and M_8 are adjusted using feedback in such a way that the threshold voltage is shifted. This principle works for any transistor length. This means that, ignoring any second order effects for now, that M_4 and M_5 can be given a much smaller length. They will have the same gate voltage and will therefore lead to the same equivalent resistance ratio. As will be clear shortly, this is a very simplified way of looking at the circuit. In practice many non linear effects will influence the working principle. However it will also be clear that for this particular application, the reasoning will be valid.

In Table 4.1 the operating regions of M_7 and M_8 are shown for some operating regions. It basically shows that usually one of these transistors is in triode, while one is in saturation. Since for the value of V_t, the equivalent resistances for these transistors is important, an equation is found for these two regions. For triode holds:

$$I_d = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \left[2(V_{dd} - V_t)V_{ds} - V_{ds}^2 \right] \tag{4.22}$$

Table 4.1: Operating regions of M_7 and M_8 for a symmetrically sized V_t compensated inverter

V_t	$V_{gs,8} = V_g$	$V_{ds,8}$	Region	$V_{gs,7}$	$V_{ds,7}$	Region
0.5	1.77	27.95m	triode	-1.23	-1.36	saturation
1	1.136	0.443	triode	-1.864	-1.221	saturation
1.5	1.132	0.691	saturation	-1.868	-0.868	triode
2	1.046	0.930	saturation	-1.954	-0.395	triode
2.5	0.691	1.044	saturation	-2.309	24m	triode

Assuming $V_{ds} \ll 2(V_{gs} - V_t)$, it holds:

$$\frac{V_{ds}}{I_d} = \frac{L}{\mu C_{ox} W (V_{gs} - V_t)} \tag{4.23}$$

This shows that the equivalent resistance decreases approximately proportional when L is decreased. For the saturation region it holds:

$$I_d = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{gs} - V_t)^2 (1 + \lambda V_{ds}) \tag{4.24}$$

When ignoring channel length modulation ($\lambda = 0$), the current is independent on V_{ds}. However the current is inversely proportional to the transistor length L. This means that for the same V_g (which is generated by the right side of the circuit and therefore does not change), the current is increased proportionally with the decrease in transistor length. The equivalent resistance of the triode operating transistor will decrease proportionally as well, yielding the same voltage drop over this transistor as with the long transistor. This means that ignoring all the effects mentioned, the threshold voltage should still be the same.

In Figure 4.44 the DC response is given for several values for V_t for both a symmetric circuit as an asymmetric circuit. In the upper plot, transistors M_5, M_6, M_7 and M_8 all have $L - 20\,\mu$m, while in the lower plot M_5 and M_6 were given $L - 1\,\mu$m. As can be seen, the threshold voltages of the symmetrically sized circuit indeed correspond to the values set. For the asymmetrical circuit some obvious deviations are clear. However, the values relatively close to V_{dd} and *gnd* show only minor deviations. The deviations are explained using some second order effects which were ignored in the equations.

When the V_{ds} of the triode connected transistor becomes relatively large, the linear relation between the equivalent resistance and the length does not hold anymore. This is the major reason of the big deviation when for example $V_t = 1.5$. The V_{ds} of the triode connected transistor is relatively big then, yielding a very non linear behaviour.

When the V_{ds} of the triode connected transistor is small (when $V_t = 0.5$ or $V_t = 2.5$), this transistor can assumed to behave linearly. Still there is a small deviation from the symmetric circuit. this can be explained by the channel length modulation of the saturated transistor. This transistor will have a relatively large V_{ds}, which makes the current depend a bit more on V_{ds}, destroying the proportional relation.

However, this effect is relatively small and the deviation is acceptable. The simulated V_t is relatively close to the value set by V_t and since it is a static deviation, it does not lead to charge mismatch. This makes it possible to operate this threshold compensated inverter with low power consumption and still making it fast enough to switch. The only design trade-off that needs to be made is between power consumption and speed of (dis)charging node V_g. When the length of M_7 and M_8 becomes very large, the power consumption is very low, but it would take long to (dis)charge V_g. Considering the maximum frequency of the capacitor voltage, the maximum length for M_7 and M_8 can be found.

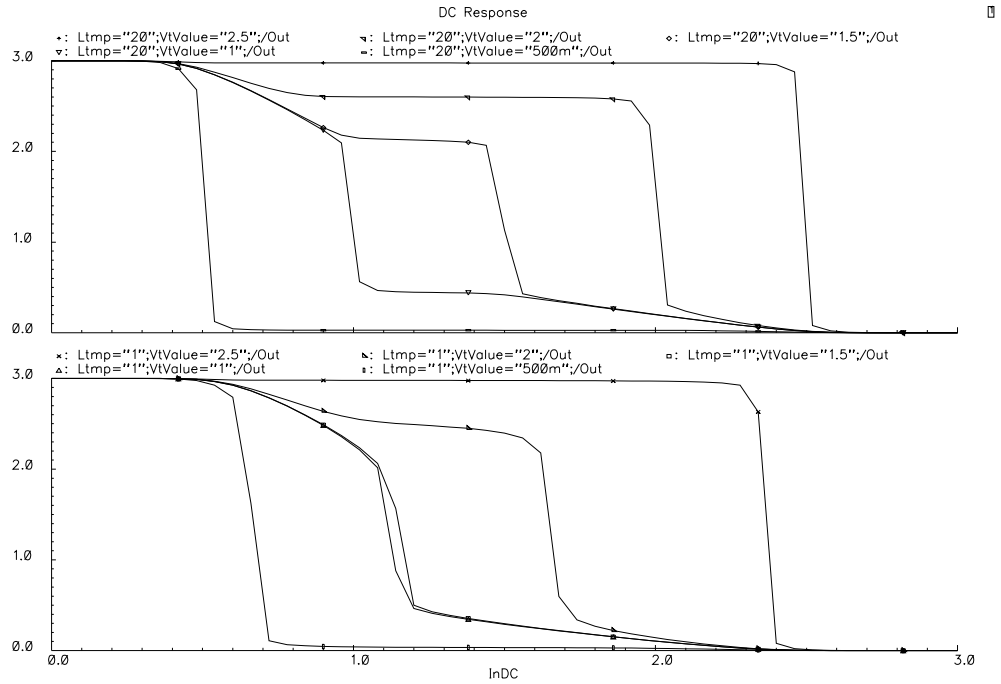


Figure 4.44: DC response of a symmetric (upper plot) and asymmetric (lower plot) threshold compensated inverter

4.6 Switch array

The switch array is used to control the direction of the current injected into the tissue. The ideal implementation of these switches is depicted in Figure 4.45. During one stimulation phase, switches S_1 and S_2 are closed and during the other phase S_3 and S_4 are closed. This will invert the direction of he current during the two phases. A few important remarks can be made from this figure.

First of all the voltage levels are considered. When a switch is closed, it needs to be able to conduct voltages ranging from 0 to $V_{dd,high}$: the complete voltage span. This means care has to be taken that no voltages exceed the breakdown at any point. When a switch is open, both sides need to be able to handle a large range of voltages. The side connected to the driver transistor may again need to handle the complete voltage spectrum, similar to when the switch is closed. The other end of the switch is connected to the tissue. The tissue might be charged, which means that also this terminal must be able to handle all voltages.

Furthermore, care has to be taken of in what order the switches are opened and closed. After a stimulation pulse, the tissue is charged. Now it's important not to (semi-)close all switches simultaneously, because this will lead to charge redistribution, which will lead to charge imbalances after the second stimulation phase. Therefore after a stimulation pulse, first all switches need to open. After that the other two switches can be closed (switched on) and a second stimulation pulse can be applied.

Because of the large voltage swings the switches need to handle, a straightforward implementation might be using transmission gates. Because of the high voltages DMOS transistors would be used. However, the V_{gs} of DMOS transistors is still limited to about 3.3 V. Since a closed switch conducts voltages over the complete voltage span, a fixed gate voltage will lead to breakdown.

Therefore V_g needs to be a floating voltage source which can be set to a certain value with respect to the source terminal. Using this approach it is not necessary anymore to use a transmission gate. Because of the floating voltage source, the transistor will always stay on when it is supposed to be on, independent on the source voltage.

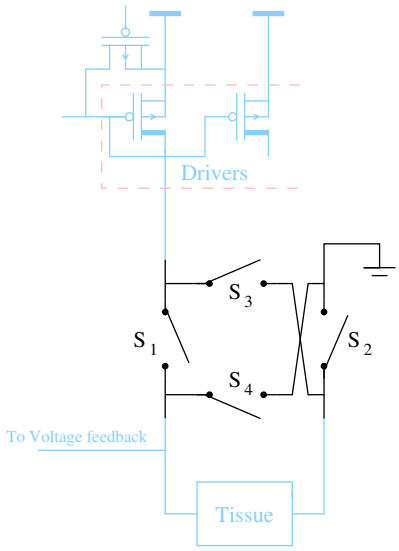


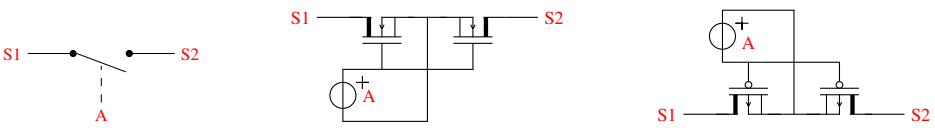
Figure 4.45: Ideal implementation of the switch array

However, it is not sufficient to use only one transistor. Consider the case in which the tissue is charged by using switches S_1 and S_2. A particular voltage is built up over the tissue. When S_3 and S_4 are subsequently switched on, the voltage which was built up is maintained. Seen from the terminals of switches S_1 and S_2, this voltage is now 'reversed'.

Consider now the case in which the switches are implemented using a single NDMOS switch. Problems will arise due to negative V_{ds} of the switches. The drain of switch S_2 for example will now be connected to a negative voltage. This means that although $V_{gs} = 0$, an inversion layer is still created because of the positive V_{gd} of the transistor. Note this effect is reduced for DMOS transistors compared to normal MOS transistors, due to the nonsymmetrical structure. However, any leakage should be prevented. For a PDMOS transistor a similar reasoning can be done, in which case the drain voltage will be positive compared to the gate.

This means that a single transistor is not enough to implement the switch. Two transistors are at least required. Using this approach the value for the source and gate can be kept independent of the tissue voltages (the voltage is floating), yielding no leakages anymore. This is depicted in Figure 4.46. The NDMOS transistors (4.46(b)) have a lower equivalent resistance than the PDMOS transistors (4.46(c)), so first an implementation using NDMOS transistor pairs as switches is considered.

Soon another problem however pops up, related to the bulk of the transistors. As discussed before, one terminal of S_2 becomes negative after stimulation. For NDMOS transistors, the bulk is connected to the source terminal. This means that in order to have the bulk connected to the lowest voltage, it would be necessary to generate a negative voltage at the source of the NDMOS transistors to prevent leakage via the bulk. Since no negative voltage supply is available this would be very hard to implement. Note that this is a fundamental problem for the NDMOS transistors and that therefore NDMOS transistors are not the best option.



(a) Ideal (b) NDMOS (c) PDMOS

Figure 4.46: Implementations of the switch

PMOS transistors have a separate bulk terminal, which makes it possible to bias this terminal with the highest voltage available. This will guarantee that no bulk leakage will exist. Next question is how to implement the floating voltage source. Three alternatives are discussed:

Resistor based This method is similar of what was discussed in the level shifter. A grounded current is fed through a resistance and subsequently is fed back to the ground. The voltage drop over the resistor $V = IR$ is floating. The major drawback is, as was discussed, the static power consumption and the hard to realize large resistance.

Capacitance A capacitor can be used as a floating voltage source, as also discussed in the level shifter design. Drawback is that care has to be taken of leakage effects which will discharge the capacitor.

Voltage-current-voltage converter Another possible implementation is to generate the required gate voltage using a current conversion. First convert the voltage at the source to a current. Subsequently the current is increased with a certain value corresponding to the required voltage shift. Subsequently this current is converted to a voltage again and fed to the gate. The floating voltage source is thus implemented using a current addition.

This method has the drawback that there is a static current and that the two conversions will most likely yield power consumption as well.

For all these methods it needs to be understood that the voltage source must be able to handle high voltages (the switches need to conduct the complete voltage spectrum). This means that the implementation using the voltage-current-voltage converter is not feasible: both converters would need to be implemented using high voltage transistors, yielding large area.

The implementation with a capacitor has similar problems. The capacitor would need to be switched 'on' and 'off' to the transistors in order to preload the capacitor with a particular voltage before it is connected. That means high voltage switches are required for this purpose. Besides the fact that these switches would require a big area (more high voltage transistors are needed), there is also a more fundamental problem: these switches have the same problem as the two switching transistors: a floating V_{gs} is required. That means that using a capacitor as the floating voltage source, the problem is actually transferred to the switches controlling the capacitor.

Therefore an implementation using a resistor and two current sources is considered. To keep the power consumption as low as possible, the resistance should be as low as possible. Implementations using 'ordinary' resistances have been implemented and tested. They work very well, but the drawback is the feasibility of the large resistances on chip. Therefore alternatives are considered.

A diode biased with a small current can yield a high equivalent resistance. Due to that exponential nature of the diodes, a very small current already can result in a quite significant voltage drop. This voltage is by far not enough to turn the switches on (about 3 V is required). To generate a voltage which is high enough, multiple diodes are put in series. The bias current needs to be chosen based on the maximum time it takes to charge the parasitic capacitances when the current sources are switched on.

Based on some simulations, it was chosen to introduce a current of 100 nA, which yields a 500 mV voltage drop over a diode connected NMOS transistors. To turn the PDMOS devices used for switching completely on, a $V_{gs} = 3$ V is required. Therefore a total of 6 diodes are connected in series. This is depicted in Figure 4.47. Now a floating voltage source is created between the gate and source of both switching transistors. The transistors can be switched on and off by switching the current sources on and off.

Simulations showed a new problem: when the current source is switched off, the diodes keep charge in their parasitic capacitance. This charge needs to flow away, which is problematic. The equivalent resistance connected to the charge is very high: it consists of diodes with only a small voltage drop (which means they are turned off and have a very high equivalent resistance) and current sources, which also have a high output resistance. This means that discharging the diodes takes quite a lot of time, which means that switching off the switches will take a lot of time.

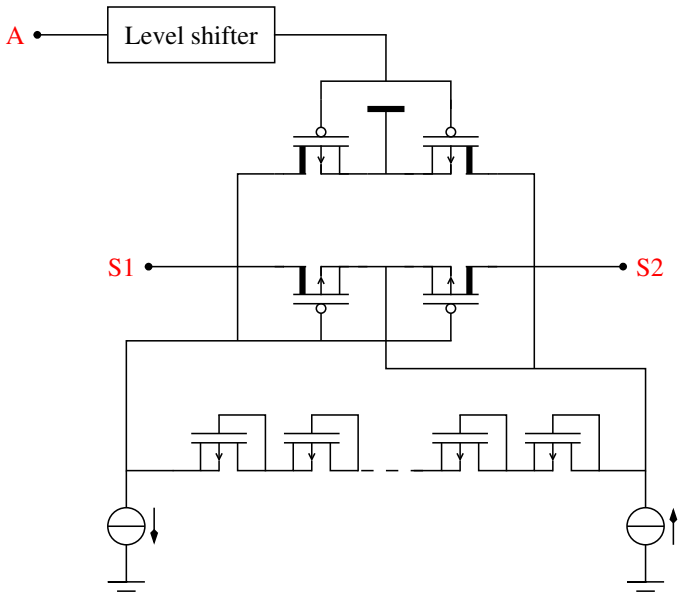


Figure 4.47: Final implementation of the switch

Therefore alternatives need to be considered. One is to actively discharge the diodes. This could be done using a voltage controlled current source. The voltage V_{gs} is monitored and as long as this voltage is above a certain threshold, the discharge process is accelerated using the output current. This approach was shown to be working, however the implementation is quite complicated. A (floating) high voltage needs to be monitored, yielding the need for additional high voltage transistors.

Another principle is depicted in Figure 4.47. When the switch needs to be turned off, two additional transistors connect both the gate and source terminal of the switching transistors to V_{DDhigh}. In this way the transistor is guaranteed to be off (the gate and source are shorted) and since both terminals are connected to the highest voltage available, the drain cannot turn the transistors on either. The advantage of connecting these transistors to the fixed voltage V_{DDhigh} is that this means the two additional transistors can be switched with a fixed gate voltage as well. Since the source is connected to V_{DDhigh}, the gate must switch between V_{DDhigh} and $V_{DDhigh} - 3$, which explains the use of the level shifter depicted in Figure 4.47. This level shifter uses the same implementation as the block discussed before.

Note that when the gate and source are shorted, the current sources still dissipate power. This is a drawback compared to the case when the current sources would be turned off when the switch needs to be open. However, since the current is chosen to be relatively small, the power consumption is acceptable. The current sources are implemented using a simple single transistor implementation comparable with the one used in the voltage feedback network. Of course these transistors need to be high voltage transistors as well. This means that apart from the level shifter, each switch uses 6 high voltage transistors.

Chapter 5

Simulation Results

In this chapter simulation results of the various blocks discussed in the previous chapter are discussed. In the first sections the correct functionality of the individual system blocks is verified. Some blocks are also combined into smaller subsystems (such as the voltage feedback loop) and simulated as such.

Subsequently a testbench is constructed to simulate the complete system. For this simulation the output stage as designed needs to be controlled using some digital logic and the charge cancellation loop needs to be completed using a counter. After the construction the complete system is simulated. Besides correct functionality also power consumption and robustness are considered.

All simulations were done in the Cadence environment using the spectre simulator. The models for the AMIS I3T80u technology are version Rev2.15.

5.1 Level shifter

All level shifters discussed were implemented in a circuit simulator to check for the correct functionality. Because of the issues related with the integration of resistances, only the capacitor based as well as the level converter based level shifter are investigated in more detail here.

First the capacitor based level converter was implemented. For the capacitor the high voltage capacitor MMCHB (Metal-Metal "Finger"/Bar Capacitor) [6] was chosen. Since the impedance seen by the capacitor (consisting of the gates of the second inverter and the reversed biased diodes) is very high, the capacitor does not need to be very big. When taking a look at the various commercial stimulators available, for example the EON IPG or some stimulators from Medtronic, it can be seen the maximum stimulation pulse width is about 1 ms (See table 2.2).

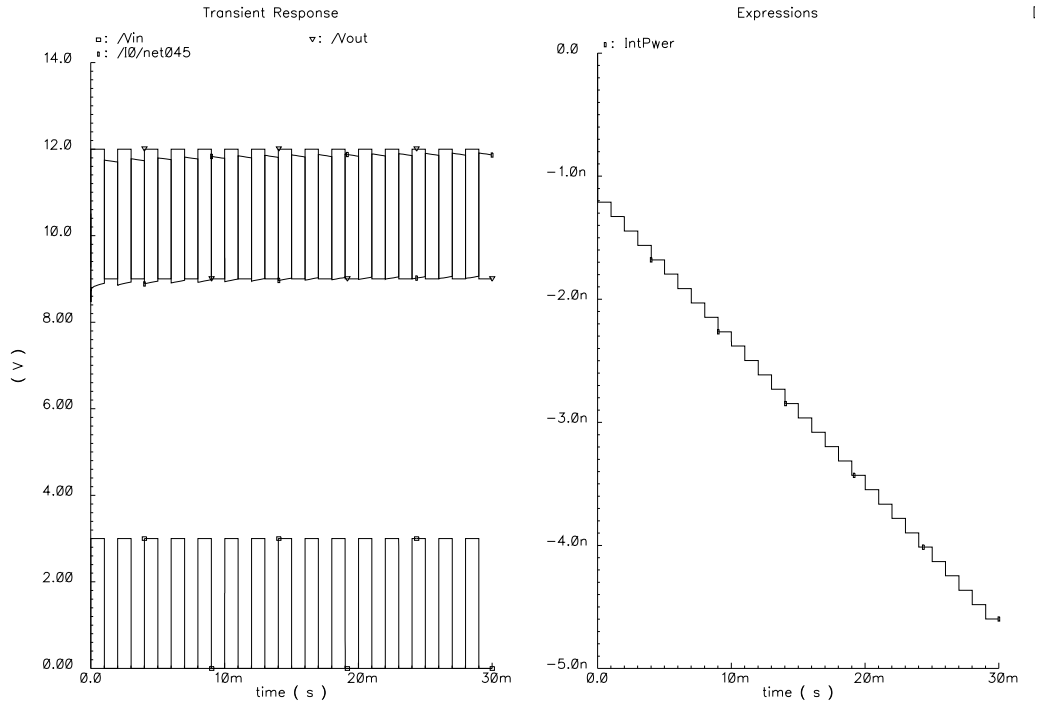
To test the functionality, the input of the circuit is chosen to be a 1 kHz square waveform. Subsequently the capacitor is tuned to assure it does not discharge too much. It turns out indeed the values of the capacitor can be very small: 100 fF is more than enough to keep the output stable for 1 ms. From the AMIS technology files it was found the capacitor value of a MMCHB capacitor is:

$$C = \text{Length}\,(C0 + Nf * C1) \tag{5.1}$$

In which Nf is the number of fingers and $C0 = -9.9 \cdot 10^{-11}$ and $C1 = 3.3 \cdot 10^{-10}$ are constants. It was found a capacitor with Length $= 20\,\mu$m and $Nf = 10$ corresponds to about 64 fF, which is large enough. The capacitor now has an area of $20\,\mu$mx$13.4\,\mu$m.

In Figure 5.1 the simulation results are depicted. In Figure 5.1(a) the transient response is depicted. As can be seen the output is indeed a shifted version of the input. Here it was chosen to have $V_{DDlow} = 3$ and $V_{DDhigh} = 12$. The voltage at the right side of the capacitor is depicted as well and the slight discharge is clearly visible.

In Figure 5.1(b) the energy consumption (the time integral over the power consumption) is depicted. As expected the power consumption is very low. In static mode the power consumption



(a) Transient

(b) Energy consumption

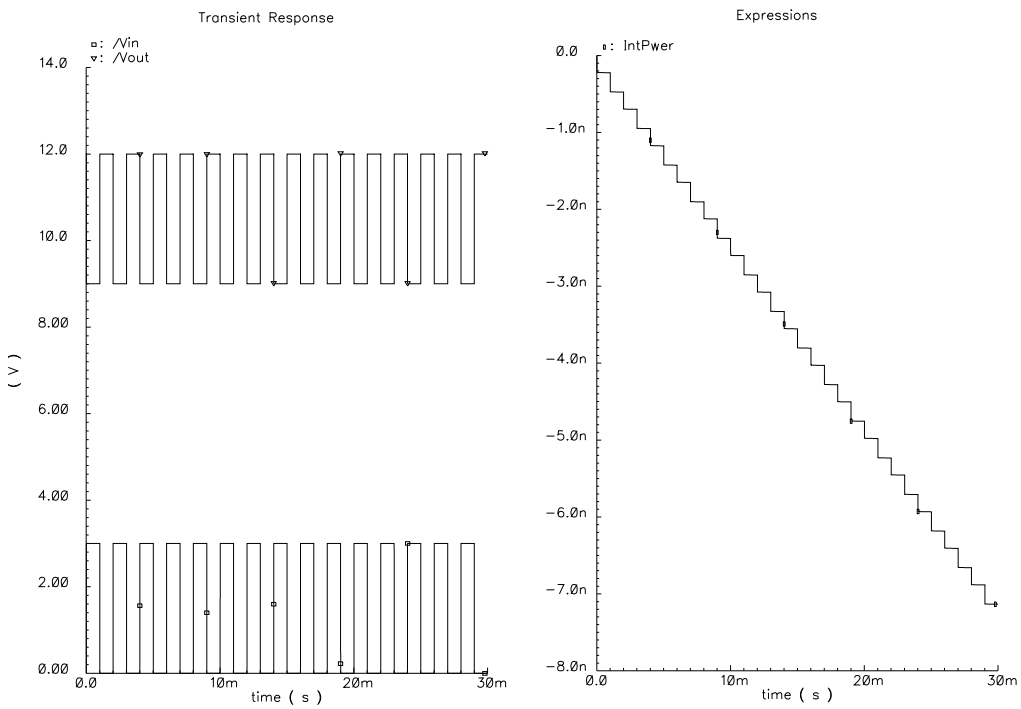
Figure 5.1: Simulation results of the capacitor based level shifter

is almost zero. Each switch consumes about 0.117 nJ of energy. As stated before this is mainly due to the energy related with switching the inverters.

The same has been done for the other level shifter: the one based on the level converter. The same parameters were chosen ($V_{DDlow} = 3$ and $V_{DDhigh} = 12$). The bias voltage of transistors M_3 and M_4 was chosen to be $V_{bias} = 8$. The simulation results are depicted in Figure 5.2. In Figure 5.2(a)the input and output voltages are depicted, showing the correct functionality of the circuit.

Figure 5.2(b) shows the static power consumption is again close to zero, as was expected. The dynamic energy consumption (when switching) is about 0.3 nJ per switch, which is quite a lot more than the capacitor based circuit. This was to be expected because of the large voltage swing at nodes N_2 and N_3.

Based on the simulation results, it can be concluded the capacitor based circuit consumes less energy. Furthermore, the area of this circuit is also lower, because of the very low size of the capacitor. The level converter based circuit needs 4 high voltage transistors, which take up much more space. Therefore it's chosen to use the capacitor based circuit in the design.



(a) Transient (b) Energy consumption

Figure 5.2: Simulation results of the level converter based level shifter

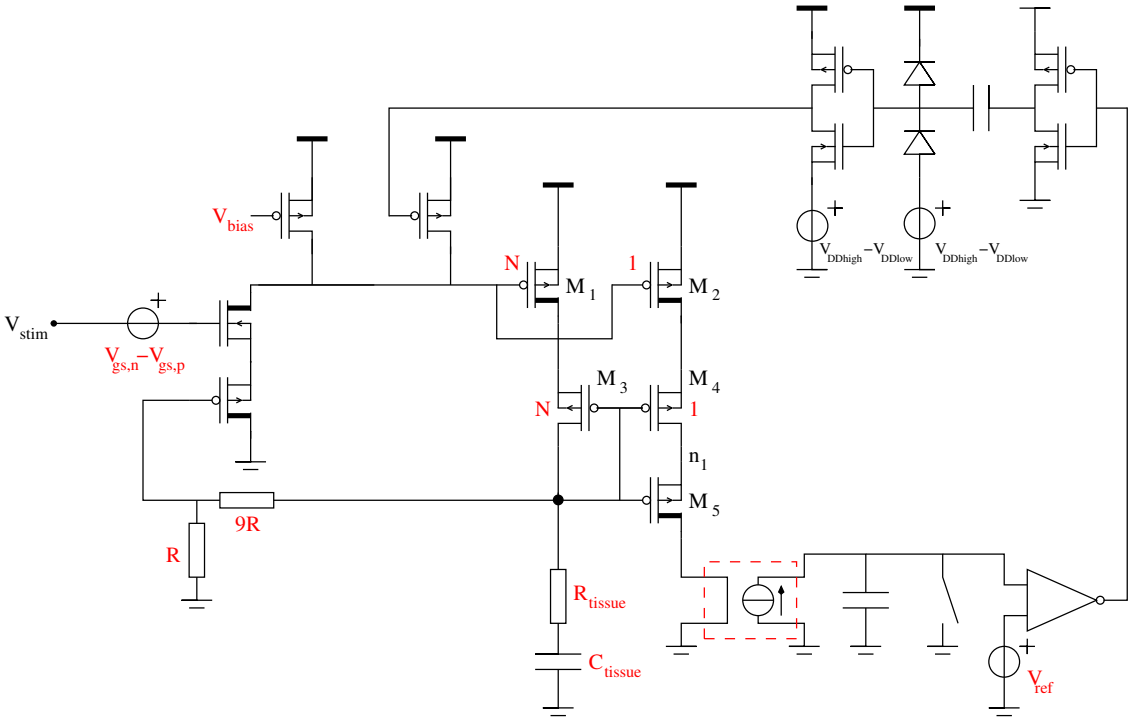


Figure 5.3: Circuit used to simulate the working principle of the stimulation circuit

5.2 Voltage feedback loop

The voltage feedback loop comprises all circuitry except the charge cancellation part. The circuit as depicted in Figure 5.3 was implemented in the simulator. As can be seen the circuits for the driver, stimulation enable switch, level shifter and voltage feedback circuit are included. An ideal version of both the integrator as well as the (inverting) comparator were included. The capacitor is integrating a copy of the stimulation current. When reaching a particular threshold, using the level shifter, the stimulation switch is enabled, which will stop the simulation. In this way all components in the circuit are simulated.

To check the stability of the feedback system a lot of transient simulations were done, each with varying tissue impedance values. During the simulations, the stimulation voltage was switched on and off, to take into account the switching actions. The waveform used is depicted in Figure 5.4. As can be seen a tissue voltage of 5 V is used for stimulation. In the same figure it is also shown the integrator is reset at about 500 μs. If the charge threshold was reached before that time, the stimulation can continue after the reset.

First the tissue resistance was varied from 10 Ω and 100 kΩ. This is depicted in Figure 5.5. In the response of the system the resistance determines the maximum current at the switching action. This means that for low resistances a very high peak current is to be expected. Also for low resistances, the time constant is low. This means the capacitor is charged faster and threshold will be reached earlier.

For high resistance values the current injected is small. This means the integrator does not reach its threshold. For lower resistance values (from 1 kΩ on) the current is large enough and the time constant is small enough to reach the threshold.

For very low resistance values, the current is very high. For $R = 10\,\Omega$ the current corresponding with the voltage (5 V) would be so high (0.5 A), that the gate potential of M_1 and M_2 will become lower than 9 V to have the impedance of the driver transistors low enough. Because this would result in damage at the driver transistors, the gate voltage is limited to 9 V at minimum. This also means that the current is lower, which means the voltage over the tissue is also lower. The

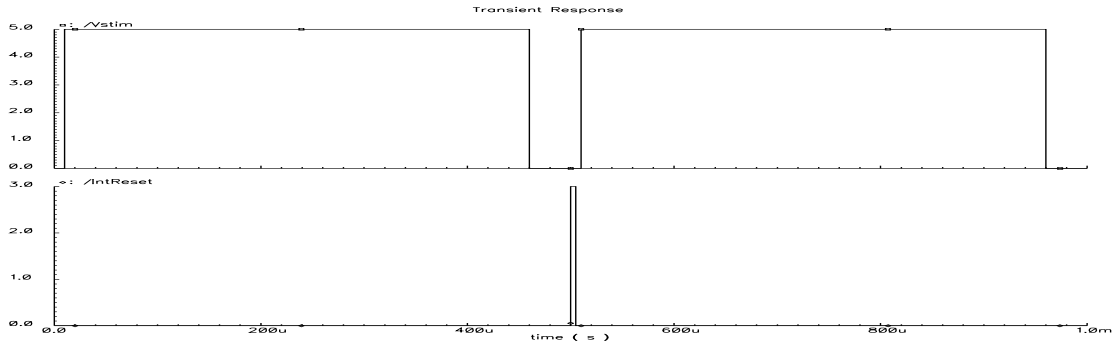


Figure 5.4: Input waveforms used for transient simulations

feedback action is therefore clipped in this case.

Limiting the gate voltage effectively means that the current injected in the tissue is also limited, which is good. This means that when a failure occurs at the electrodes, resulting in a short circuit, the current will not explode, which prevents tissue damage.

Furthermore the simulations show a stable behaviour for all values of R. No oscillations or 'exploding' signals are perceived.

Next the tissue capacitor is varied. The capacitor determines the amount of charge which needs to be stored on it to fully charge it to the voltage set by the stimulation source. A small capacitor needs less charge and will therefore maybe not reach the threshold. A smaller capacitor also yields a smaller time constant, which means the capacitor is charged faster.

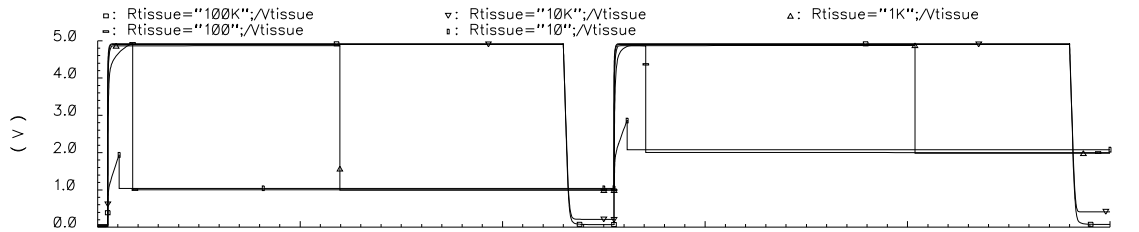
The results are depicted in Figure 5.6 for the capacitor range 1 nF up to 1 mF. For very low capacitor values (up to 100 nF in this case), the capacitor is fully charged without reaching the threshold. After resetting the integrator there is no additional current injected anymore, because the capacitor is already charged. This is different for bigger capacitors: here threshold is reached before the capacitor is fully charged. This means that after the integrator reset, the tissue is charged further.

For very low values of the capacitor an oscillatory behaviour is seen. As explained before this is due to the fact that the time constant of the tissue is now so small, that it comes close to the 'time constant' which is located at the gate terminal. The 'poles' will split and this will lead to oscillatory behaviour. As can be seen in the figure this oscillating behaviour is not leading to an unstable response. The only thing is that the tissue voltage is not completely constant anymore, which is not a very big problem, since the voltage does not need to be very accurate. Furthermore, a capacitance value of 1 nF is very small for tissue. Usually a value of around 1 μF is reported. Therefore no problems are to be expected.

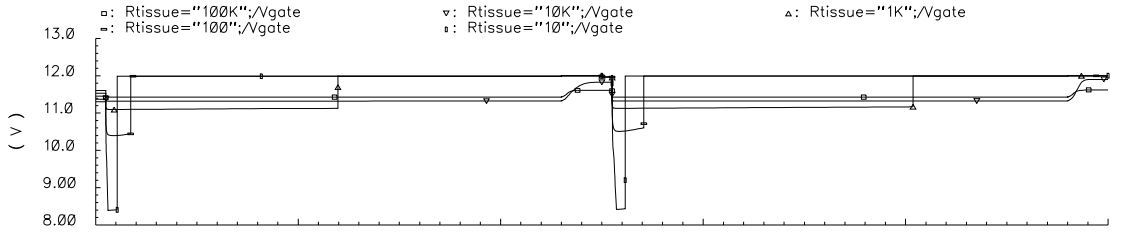
5.2.1 'Bandwidth'

As explained before it is actually not possible to discuss the bandwidth of the system, since it is nonlinear. However, it is possible to do AC simulations for the circuit. These simulations show in some way a measure for the loop gain of the system for increasingly fast transitions. For simulation purposes, the capacitor in the tissue model was shorted in order to account for the maximum current delivered by the drivers. Simulation results are depicted in Figure 5.7.

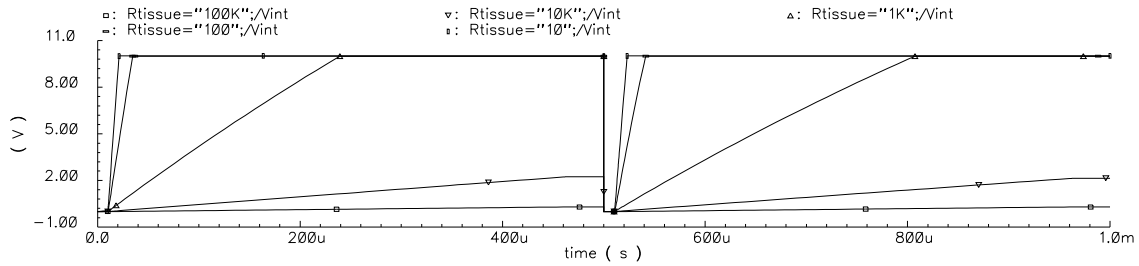
From the figure it can be seen the tissue voltage has been simulated for 4 different input voltages: 2 V, 4.7 V, 7.3 V and 10 V. Keep in mind this is a non linear system, so the result does not say anything about stability or the real output levels. However it gives an indication for at which frequencies (fast transitions), the loop gain is lowered. The output is constant up to about 5 kHz and then decreases. This means that at this point a 'pole' is decreasing the loopgain. The frequency of 5 kHz is high enough for stimulation waveforms, which have (in burst mode) a maximum frequency of 1 kHz.



(a) Tissue Voltage

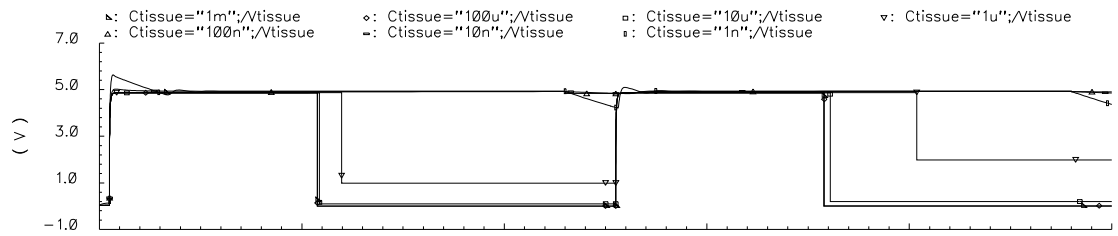


(b) Gate voltage (Driver transistors)

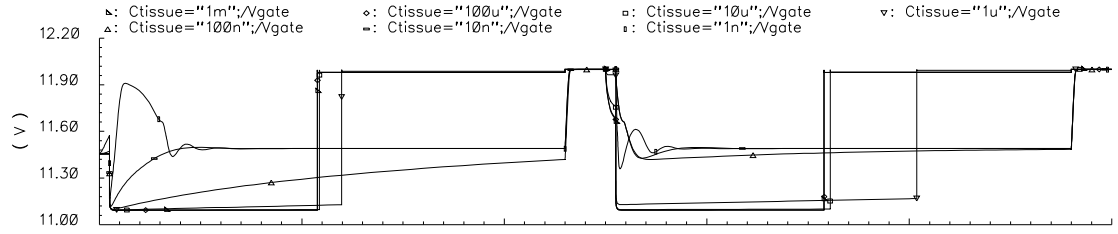


(c) Integrator voltage

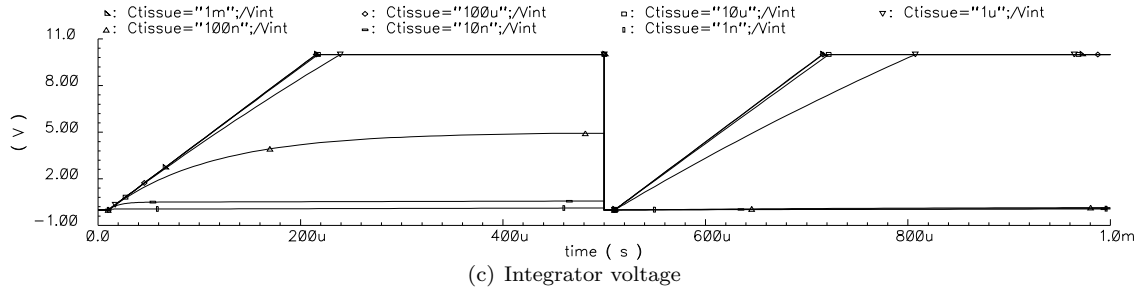
Figure 5.5: Transient simulations for varying tissue resistance



(a) Tissue Voltage



(b) Gate voltage (Driver transistors)



(c) Integrator voltage

Figure 5.6: Transient simulations for varying tissue capacitance

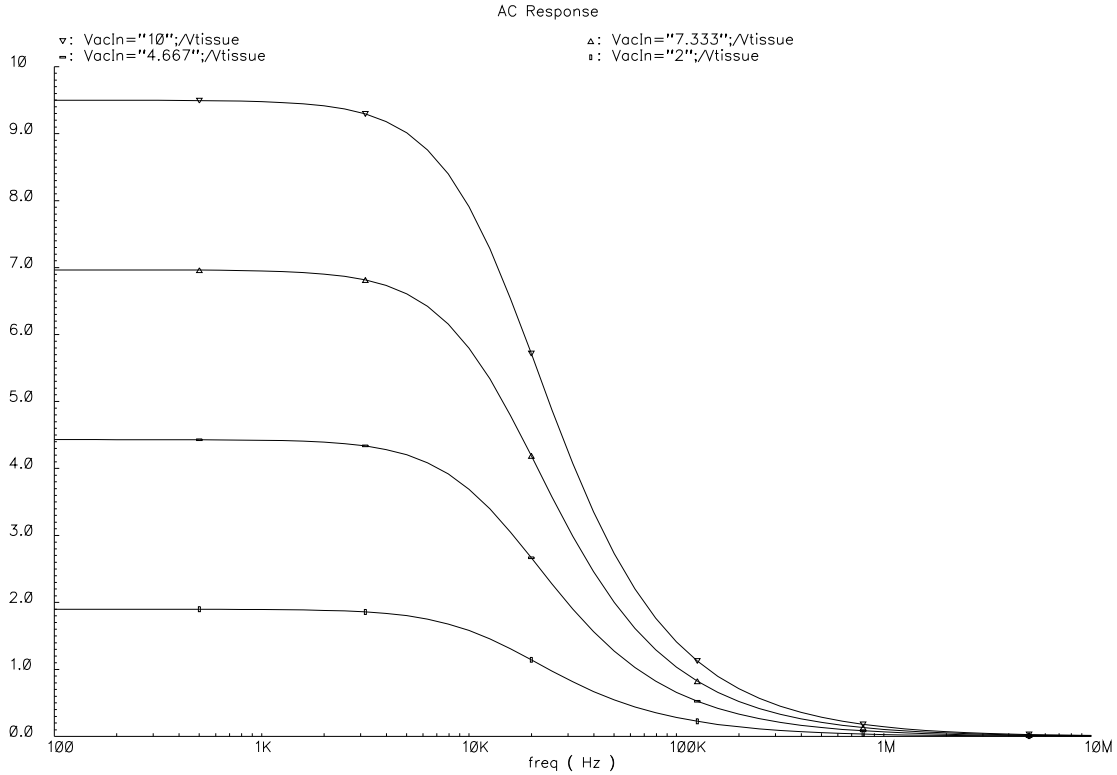


Figure 5.7: AC simulations of the tissue voltage for various input voltages

5.3 charge cancellation circuit

The charge cancellation circuit consists of the current divider and integrator. These two circuits are treated separately here.

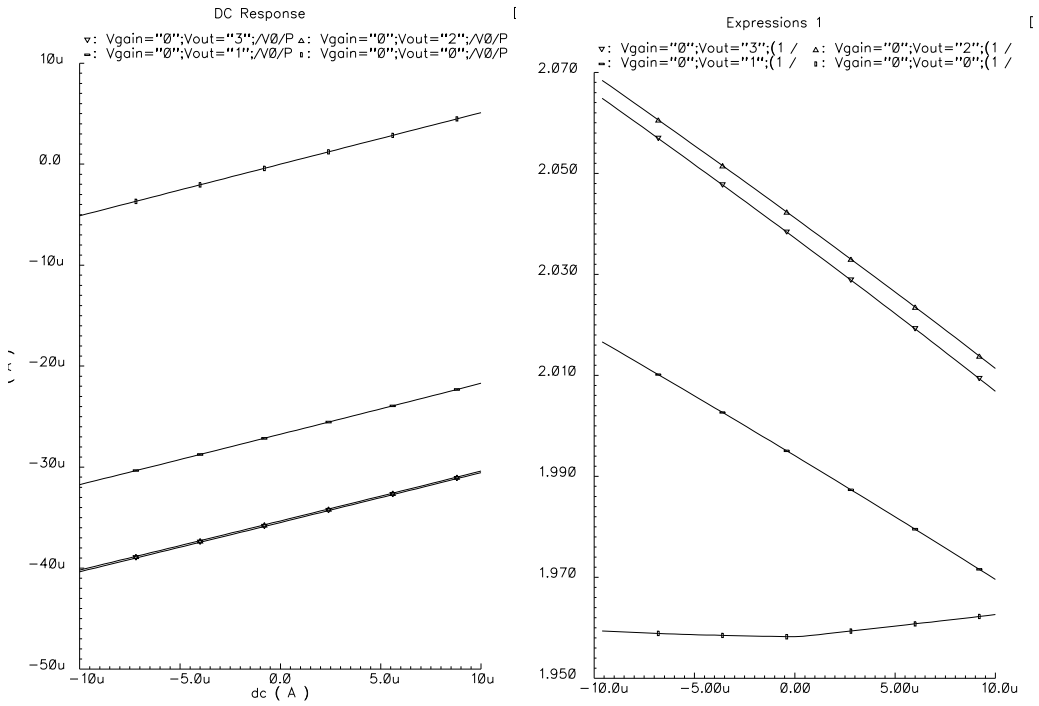
5.3.1 Current divider

The binary controlled current divider was implemented in the circuit simulator. Chosen was for a 4 stage MOCD with a 6 dB attenuation per stage. This means that each stage includes a single R-2R stage. The circuit is to be controlled now using 4 bits. Furthermore it was chosen to have $V_{dd} = 3\,\mathrm{V}$. The correct functionality of the current divider will be investigated in the following subsections:

- Operation of the MOCD without an output stage
- Operation of the output stage only
- Operation of the MOCD with output stage
- Dynamic behaviour

Operation of the MOCD without an output stage

First the operation of the MOCD itself is checked, without the output stage which can be used to keep the dump and output line voltages equal. The dump line is connected to ground, while the output line is connected to a DC voltage source, for which the value can be varied. A DC sweep simulation was used to sweep the input current over the range $-10\,\mu\mathrm{A} < I_{in} < 10\,\mu\mathrm{A}$.



(a) Output current (b) Current gain

Figure 5.8: Operation of the MOCD without the output stage

Furthermore only the first stage of the MOCD is active, which means the dump line current should be twice as big as the output current.

In Figure 5.8 the results are depicted. In Figure 5.8(b) it can be seen the current attenuation indeed is $I_{in}/I_{out} \approx 2$. For reasons becoming clear soon, the current gain was found by calculating the derivative of the output current, while realizing the derivative of the input current is always 1 (it is the parameter being swept). The variations in the current gain can be explained due to channel length modulation, as explained in the previous chapter. By changing the output voltage the V_{ds} of the transistors varies, yielding a slightly different current division. The same holds when the input current is varied: since the input consists of a current source, the input voltage will vary, yielding channel length modulation effects as well. When the length of the transistors is increased, it is seen both effects become smaller.

In Figure 5.8(a), an effect also described in the previous chapter is found. Besides the expected current swing of $-5\,\mu$A to $5\,\mu$A, there is a static DC current flowing from the output to the dump line, depending on the DC output voltage. Of course this will yield problems in the system. This DC current was the reason to use the derivative to calculate the current gain, because it cancels the DC and shows clearly the effect of channel length modulation.

The results from Figure 5.8 show that it is necessary to have the voltages of the output and dump line equal. Only in this way there will be no DC current which can destroy the transfer of the MOCD. Therefore the output stage described in the previous chapter is investigated now.

Operation of the output stage only

First the performance of the output stage only is investigated. Therefore the MOCD and its output stage are separated from each other using an ideal current buffer.

First an output stage with a *fixed* bias scheme is investigated. A DC sweep over the input current is simulated with four different settings for the MOCD (each time an additional stage is enabled, thereby halving the total gain of the system). In Figure 5.9 the simulation results are

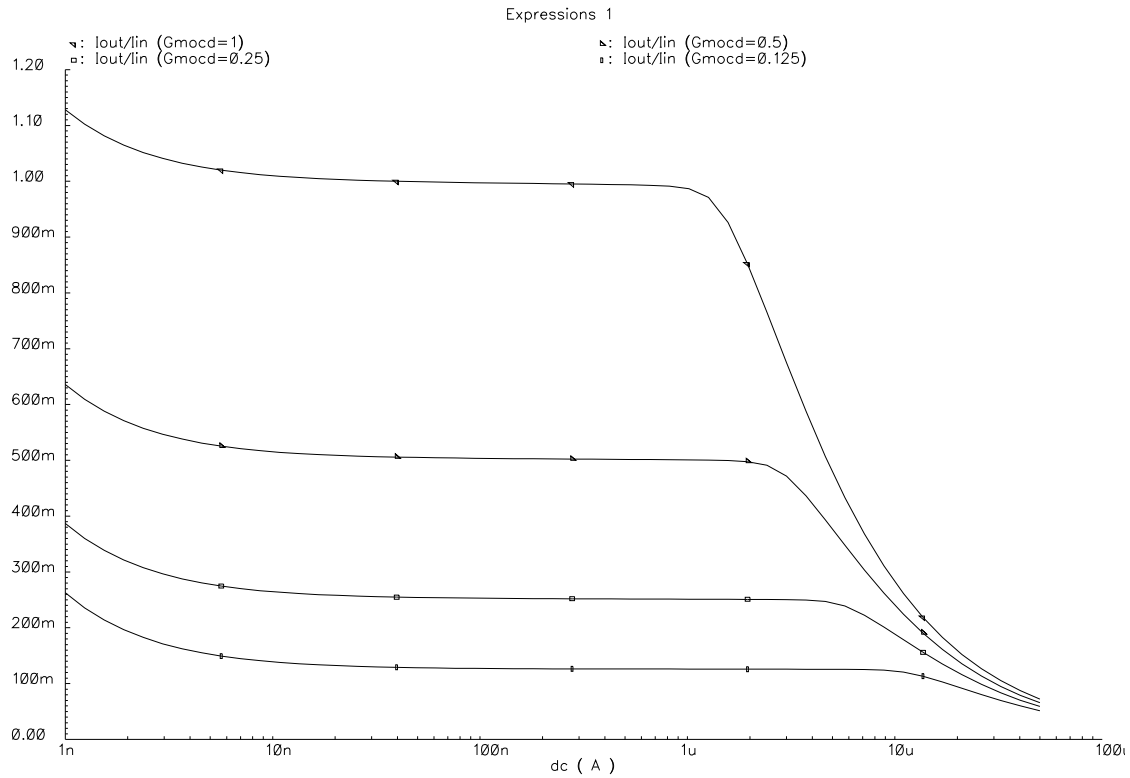


Figure 5.9: MOCD current gain using a buffered output stage with fixed bias (10 nA)

depicted. It was chosen to have $I_{bias} = 10\,\text{nA}$. In the figure the three regions defined in the previous chapter can be easily found:

- When $I_{bias} \approx I_{in}$ the current gain is higher then expected, since the drain voltages of the two input transistors are not completely equal.
- When $I_{bias} \ll I_{in}$ the gain has exactly the expected value
- When I_{in} is very large, the output transistor cannot conduct the large output current anymore, yielding a decrease in the current gain.

The output stage is subsequently changed by including the adaptive bias scheme introduced in the previous chapter. The same simulation is run and the results are depicted in Figure 5.10. As can be seen the three regions have disappeared and the gain is just as expected. Only when the MOCD itself is disabled (a gain of 1), the total system gain reduces for high currents. This decrease can be explained by the fact that the bias current becomes so large, the gate voltage of the upper transistors (in particular transistor M_6 in Figure 4.31) becomes very large. This will reduce the voltage headroom of the current mirror at the output, used to invert the output current. When the current becomes too large the voltage headroom becomes too small and the output current will decrease. This is not a big problem, since for high currents the MOCD will be set using a large attenuation and in this case no problems are expected, due to a smaller bias current.

Operation of the MOCD with output stage

Since both the MOCD and the output stage of the MOCD are working fine, the current buffer in between the two blocks is removed. The simulation results are depicted in Figure 5.11. As can be

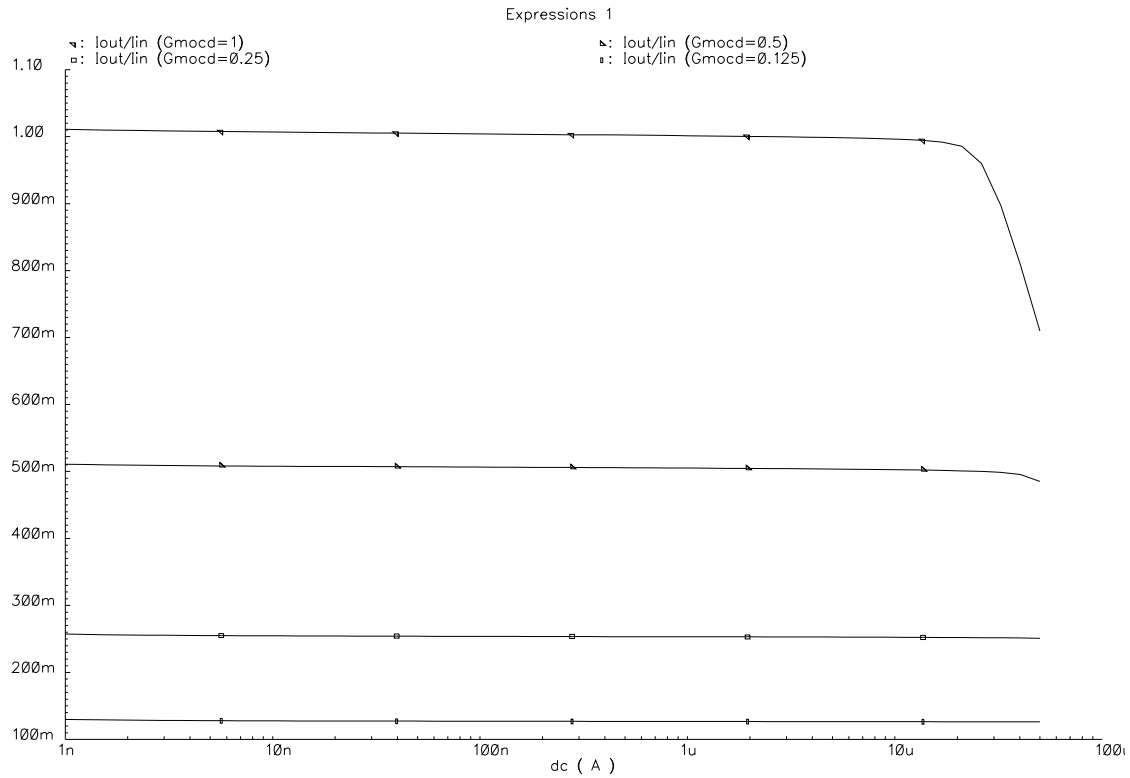


Figure 5.10: MOCD current gain using a buffered output stage with adaptive bias

seen the results are quite different from when a current buffer is used. Two effects are important here:

- When the MOCD gain is set 0.125 or 0.25 and the input current is low, the actual MOCD gain becomes close to 0.5
- At high currents ($> 15\,\mu$A), the current gain decreases rapidly

. These two effects are discussed in the following paragraphs.

Gain error for low currents When the input current of the output stage is small, the gate voltage of transistor M_2 (Figure 4.31) is relatively small. This means the impedance of this transistor (Z_{ds}) is relatively high. When this impedance increases too much, it becomes the dominating impedance for the current, instead of the impedances from the MOCD stages. In this case transistors M_1 and M_2 are dominating, which explains why the current gain goes towards 0.5, since they are the same for the dump and output line of the MOCD.

One obvious way to decrease the input resistance of the output stage is to increase the bias current. Note however that in this case the input current becomes comparable to the bias current and the circuit will operate in a wrong region. To illustrate that indeed the input impedance is the problem, a circuit with a high (fixed) bias current ($10\,\mu$A) is implemented. The simulation results are depicted in Figure 5.12.

In Figure 5.12(a) the gain from the input of the MOCD to the input of the output stage is depicted. Indeed the gain is constant now for low currents (meaning the impedance problem is solved), but it does not correspond to the gain set by the MOCD. This is because the circuit is operating mostly in the region for which the input current is comparable to the bias current. This will mean the current gain will not be very accurate anymore.

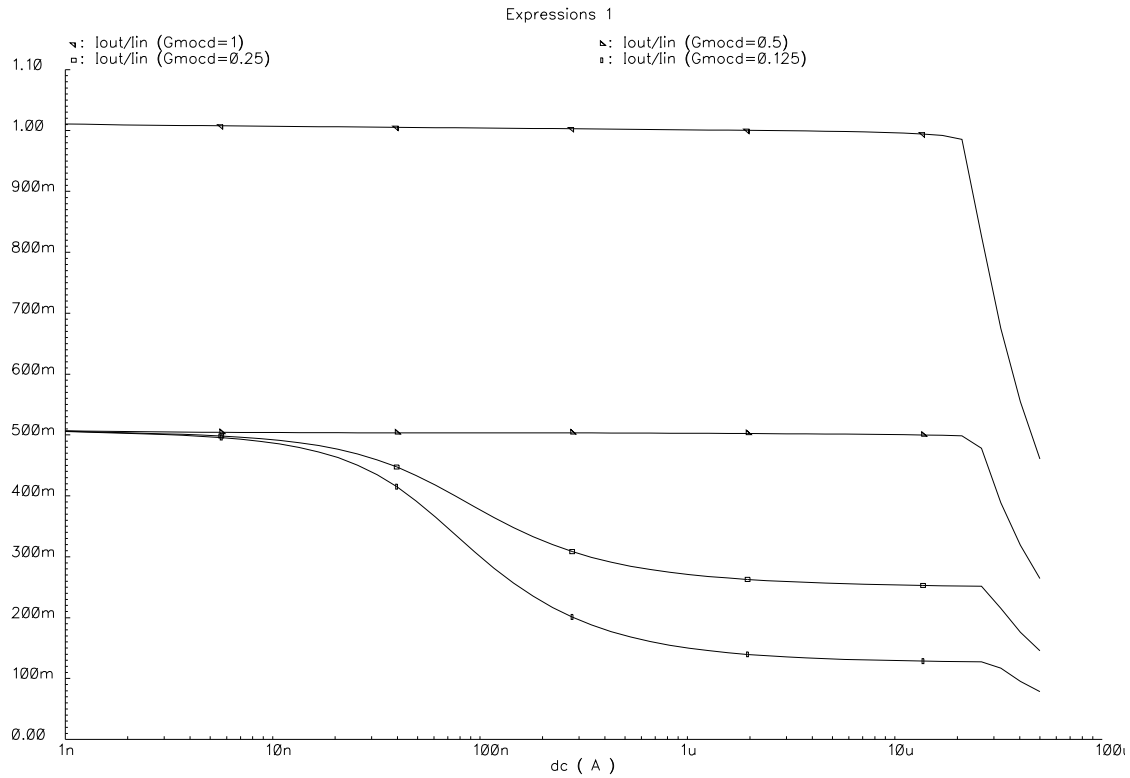


Figure 5.11: MOCD current gain using an output stage with adaptive bias

Furthermore it can be seen the copying of the output current towards the output does not work anymore using a high fixed bias current as can be seen in Figure 5.12(b). Because in this case the input transistors are not sufficiently in triode, the current is not copied accurately anymore.

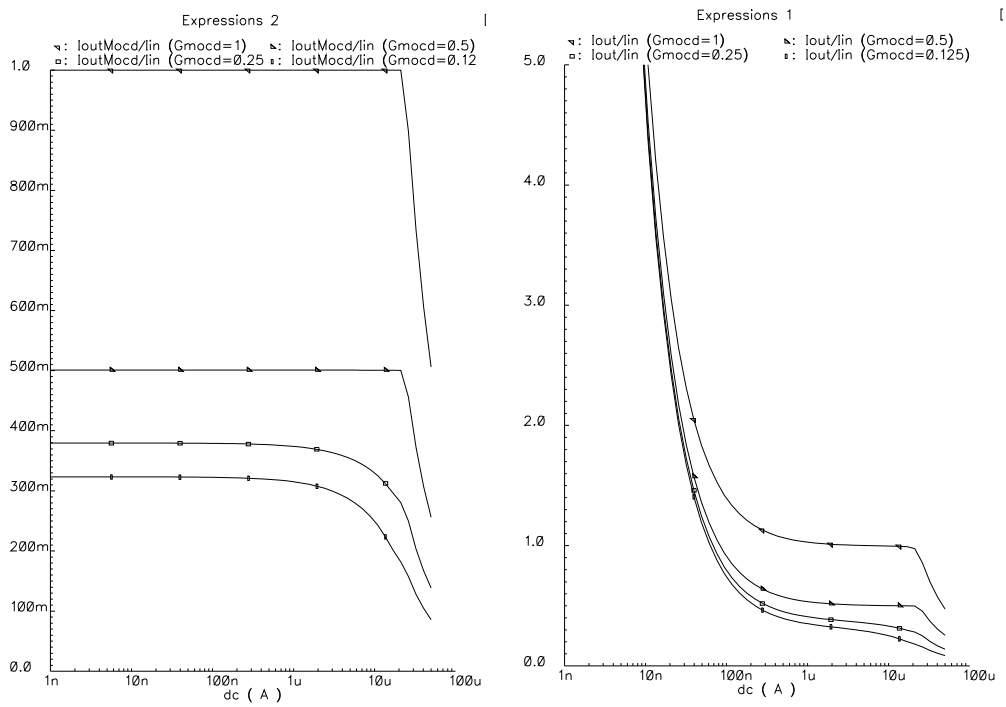
At first the problems associated with low input currents described here might seem to yield problems for the operation of the circuit. However, the circuit works fine in the regions which will be used in practice. When the current is low, the MOCD gain will be large (1 or 0.5) and in these cases the circuit is working fine. When the current is high, the gain of the MOCD is decreased and again for these regions the circuit is working fine. Note the x-axis in Figure 5.11 is logarithmic. In Figure 5.13 the same plot is depicted with linear axes and here it can be seen the circuit is indeed working fine for a large current range.

Gain error for high currents The decrease in current gain for high currents ($I > 15\,\mu$A) is due to the fact that the voltage at the MOCD input becomes too high. The impedance of the MOCD stages needs to be high enough to overcome the gain errors for low currents. However this will lead to a higher voltage over the MOCD when the current becomes large (a higher impedance means a higher voltage drop over each MOCD stage). In this case the transistors will reach breakdown yielding gain errors. This is the effect which can be seen in Figure 5.11.

Therefore the transistor size for the MOCD should be chosen such that it is large to handle low currents. At the same time the size cannot be too large, since it will not be able to handle the big currents. A trade-off was found using a size of $W/L = 1/5\mu$m.

Dynamic behaviour

Next aspect to investigate is the stability of the MOCD output stage. As pointed out in the previous chapter, the loops in the output stage give rise to oscillatory behaviour. One of the



(a) $I_{outMOCD}/I_{in}$ (b) I_{out}/I_{in}

Figure 5.12: MOCD current gain using an output stage with a fixed bias (10 μA)

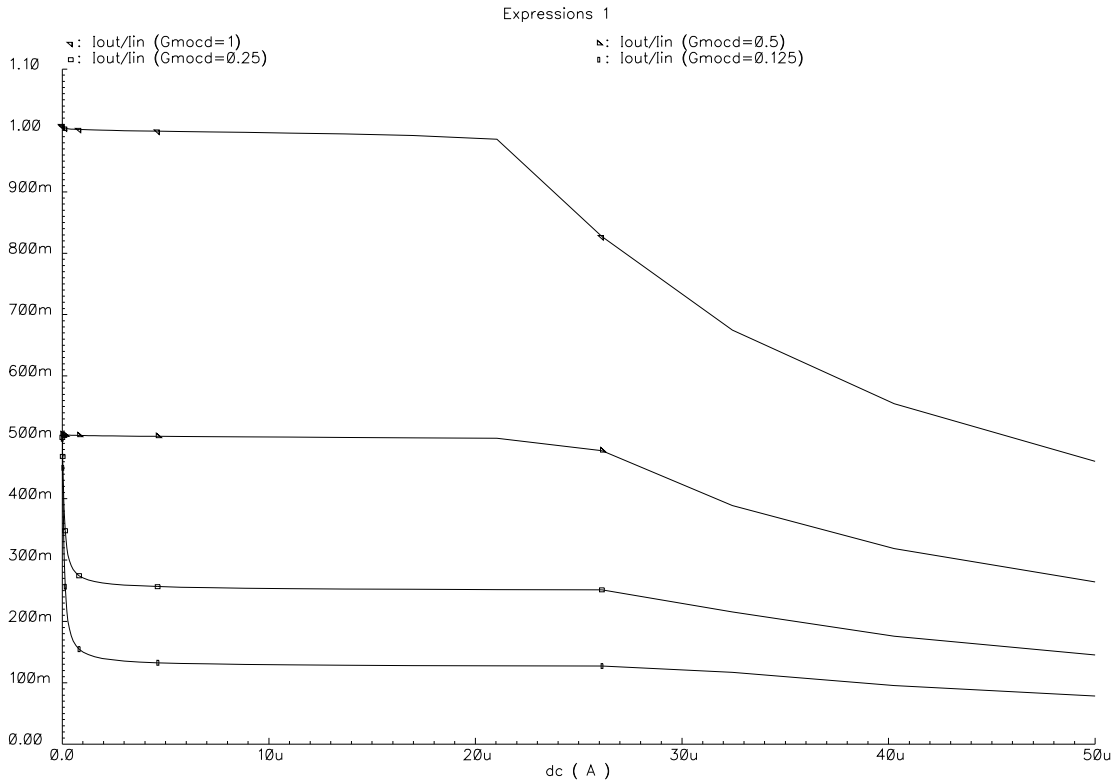


Figure 5.13: MOCD current gain using an output stage with adaptive bias (linear scales)

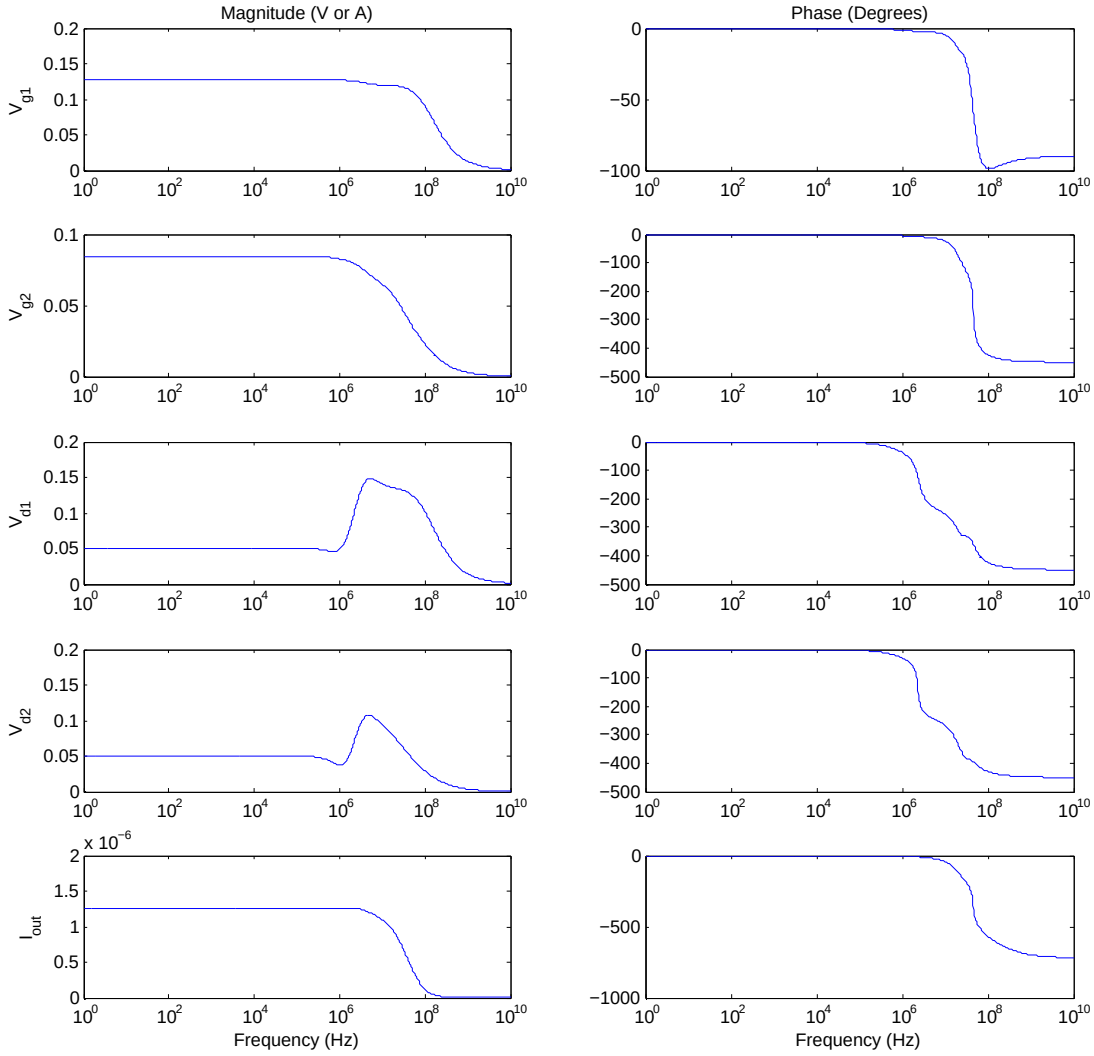


Figure 5.14: AC simulations of the MOCD output stage without stabilization network

problems in analyzing the circuit is that due to the adaptive biasing scheme the circuit is not linear. This means the AC response depends heavily on the input signal.

In Figure 5.14 the magnitude and phase of some voltage nodes in the circuit is depicted as well as the output current. It was chosen to have a $5\,\mu$A current as input here. As can be clearly seen, the phase of the voltage nodes exceeds $-180\,°$, which can give rise to instable situations.

One way to solve this is by introducing a pole splitting capacitor. This capacitor will now determine the phase shift for high frequencies, yielding a maximum of $-90\,°$. Using some simulations it was found that two capacitors of 300 fF are enough to reduce the phase shift of the voltage nodes. In Figure 5.15 simulation results are depicted. Two input currents were used: 10 nA and $5\,\mu$A. As can be seen the phase shift is now only $-90\,°$ for the voltage nodes. The non linear behaviour is also clearly seen: the speed of the circuit is much lower for a lower input current, since the bias current is much lower as well, yielding slower transistors.

In the lowest plot the output current is depicted. The output current for $I_{in} = 10\,$nA is multiplied with 1000 in order to be able to plot it together with the $I_{in} = 5\,\mu$A case. The

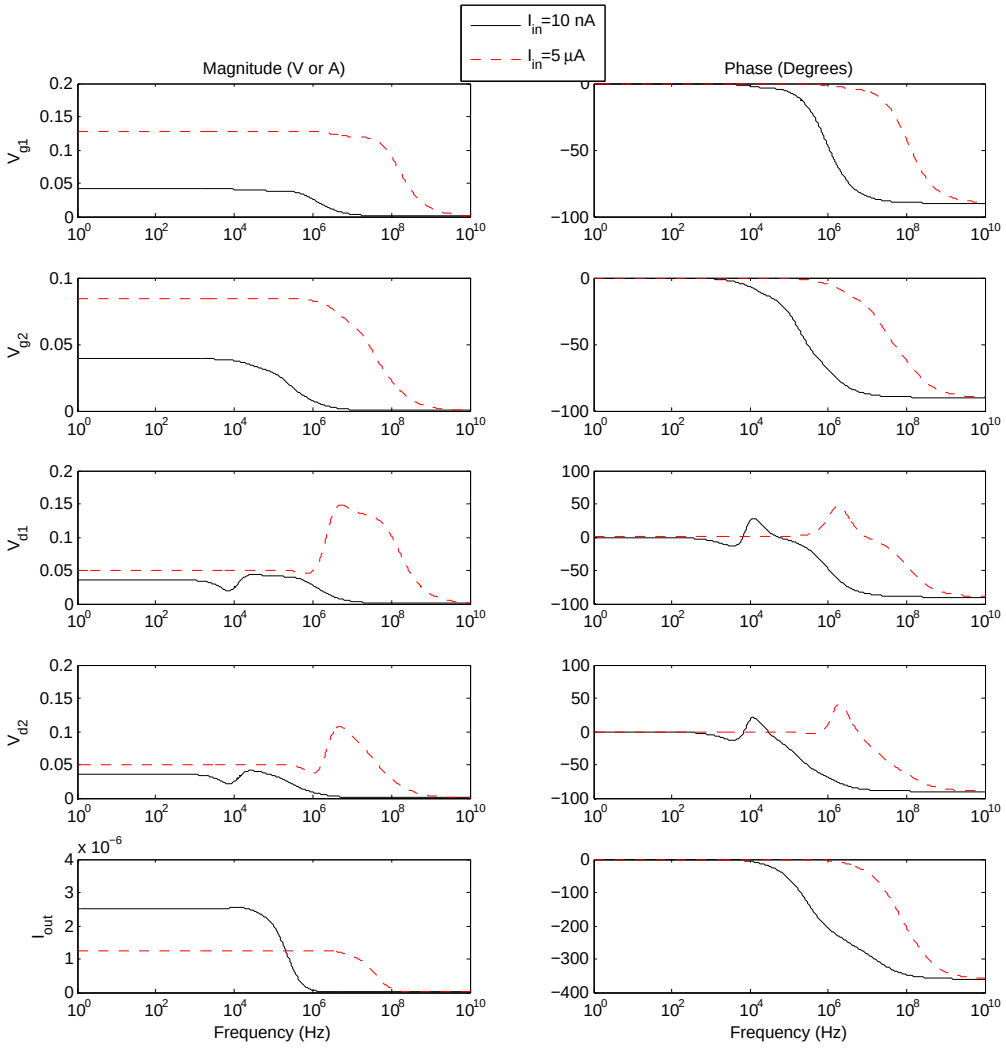


Figure 5.15: AC simulations of the MOCD output stage with two 300 fF pole splitting capacitors

phase shift of the current is clearly still more than 180 °. However, the phase at this point is not important, since there is no loop from the output current back to the input. Only the gain is important here and it is found that until about 10 kHz the expected current is at the output (for a 10 nA input current).

Therefore it is concluded that the MOCD system is working fine. First of all it is stable and when the gain of the MOCD is chosen carefully the transfer is also accurate enough.

5.3.2 Integrator

The circuit for the integrator as depicted in Figure 4.33 is implemented in the simulator. A complete overview of this circuit is depicted in Figure 5.16. The various components from Figure 4.33 are referred in this figure. Note that for the current mirror a cascoded current mirror is used. In the previous chapter was found this is not required to cancel channel length modulation. In the following discussion it will become clear why this cascoded mirror will be used anyway.

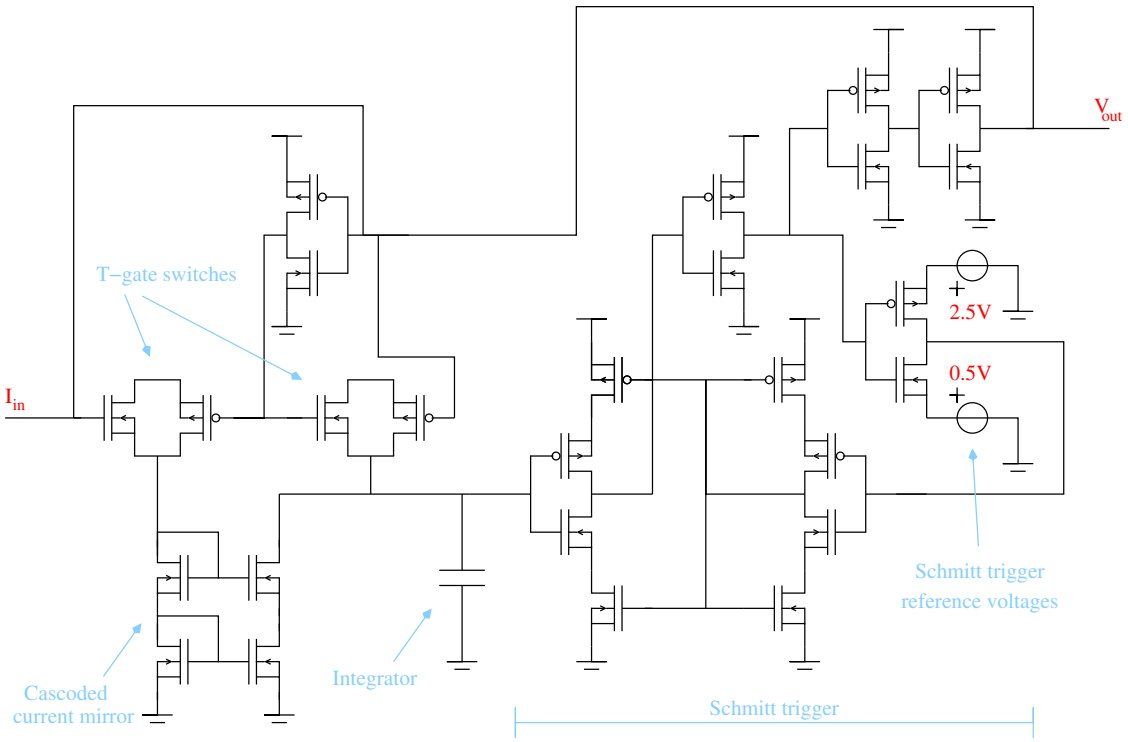


Figure 5.16: Block scheme of the integrator and comparator combination

The circuit is simulated by injecting a certain current. The output of the circuit consists of the block shaped periodical signal. To check the accuracy of the circuit, various input currents are used (10 nA, 100 nA and 1 μA). The frequency at the output should be a linear function of the input current. In Figure 5.17 the voltage at the capacitor is depicted for these three different input currents. The frequency of these triangular shaped is calculated and is found to be 305 Hz, 3.01 kHz and 29.4 kHz for 10 nA, 100 nA and 1 μA respectively.

Although these values clearly show a trend, they still are not completely linear. This will result in errors in the charge cancellation. Although it has been shown that the channel length modulation should not introduce any errors, it might be possible that the relatively simple model used in the previous chapter (using λ only), was not sufficient enough. Therefore it was decided to replace the simple current mirror by a cascoded version, as depicted in Figure 5.16. Running the same simulation, a comparable figure results, but this time the frequencies are 288 Hz, 2.88 kHz and 28.6 kHz for 10 nA, 100 nA and 1 μA respectively. This is a big improvement, which explains why it was chosen to use the cascoded version.

The drawback of the cascoded version is an increased input voltage. However, simulations show that for currents up to 1 μA, the input voltage does not increase above 1.5 V for transistor sizes $W/L = 2/1$. Therefore no errors are to be expected using the cascoded stage instead.

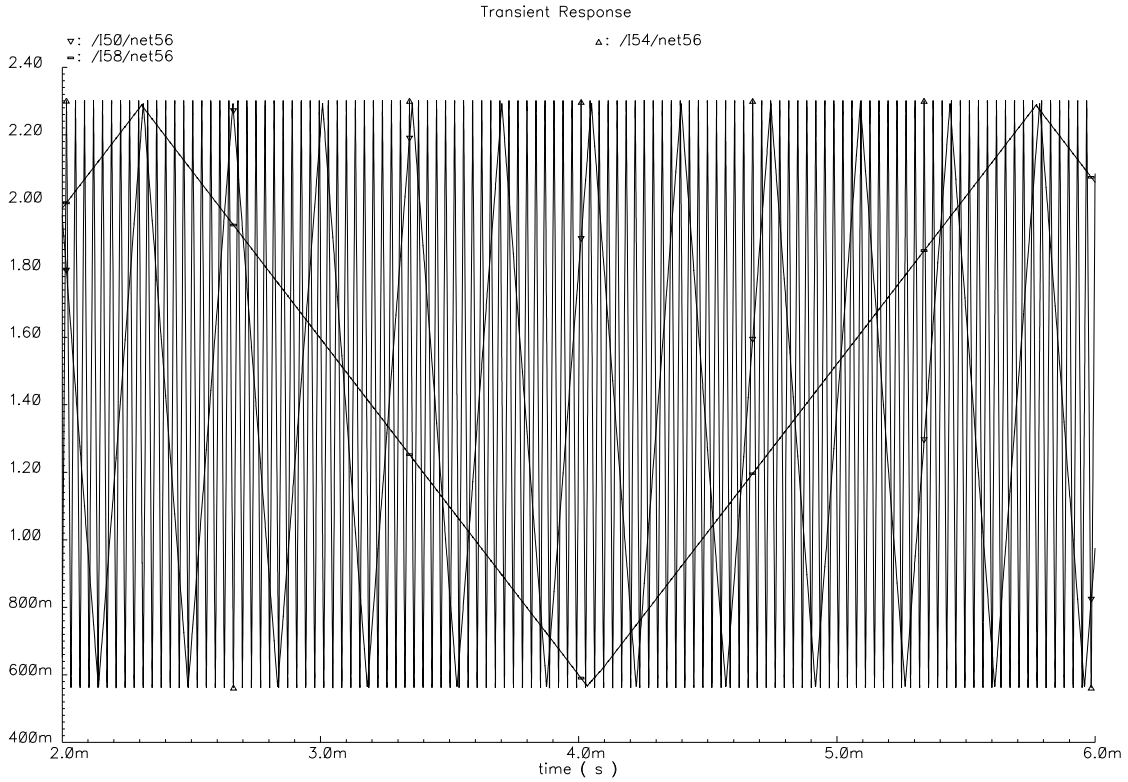


Figure 5.17: Voltage over the capacitor in the integrator for different input currents

5.4 Switch Array

The switches as discussed in the previous chapter and as depicted in Figure 4.47 are implemented in the simulator. The performance of the switch is checked using a simulation. The input side of the switches is connected to a current source, which can be disconnected in order to create a high impedance node when the current source is not active. The output side of the switches is connected to a simple tissue model consisting of a capacitor and resistor, in order to be able to charge the tissue.

It is now important to have the stimulation procedure in the right order. When the system is 'in rest', all switches are enabled. This means that the tissue is shorted and no charge can be injected. From this situation, the stimulation procedure is as follows:

- Disable switch 3 and 4
- Enable stimulation by connecting the current source to the switch array
- Stop stimulation by disabling the current source (since no charge cancellation is implemented (we are only testing the switches), the stimulation is stopped after a certain period of time.
- Disable switch 1 and 2
- Enable switch 3 and 4 (note that it is important to first disable switch 1 and 2 before enabling 3 and 4 to prevent charge redistribution).
- Enable stimulation by connecting the current source
- Stop stimulation by disabling the current source
- Enable switch 1 and 2 to short circuit the tissue again.

This cycle is implemented in the simulator. The stimulation source waveform was chosen to be a shifted sinus with equal amplitude and offset. The voltage swing was chosen to be maximum in order to test the switches over the full range.

The simulation results are depicted in Figure 5.18. In the lower left corner it is clearly seen the tissue is charged to about 6 V and subsequently discharged to 0 V again. A number of things are important from this figure.

First of all it can be clearly seen from the tissue potential voltage in the right part that switches which are enabled still have a certain voltage drop. This means their impedance is still quite high. For the injected current of 6 mA a voltage of 3 V is lost over the switch. This impedance can be decreased by increasing the size of the transistor. This means a trade-off needs to be made between area consumption and power efficiency. In this simulation a rather big transistor size was chosen (minimum PMOS size with a multiplier of 10).

Another important feature is the speed of switching. This is depicted in the upper left plot by the gate-source voltage of the switching transistors. As can be seen the voltage switches rather quick: the voltage of -3 V is reached within 39 μs. This time is determined by the value of the current source and the parasitic capacitance of the diodes which needs to be charged.

Switching off is a very quick process, since the Gate and Source are shorted to V_{DDhigh}, which is a low impedance source, the equivalent RC time is very small (the 10% to 90% charging time is shorter than 1 ns). The two transistors connecting the V_{DDhigh} to the gate and source of the switches are chosen to be single minimum size transistors.

One remarkable aspect to be noticed from Figure 5.18 is the fact that the V_{gs} of the switches is first charged towards $\approx$ 0.5 V and after a while to 3 V. When the voltage is $\approx$ 0.5 V, the stimulation source is not yet active and the voltage at both terminals is almost 0 V, as can be seen in the right part of the figure. This means that in order to reach $V_{gs} = -3$ V, the source would need to become up to -3 V. Since no negative potential is available, this is impossible.

This has important implications for the system. It is not possible for the switches to be enabled completely for voltages lower than 3 V. In this case the gate cannot be brought to a potential low

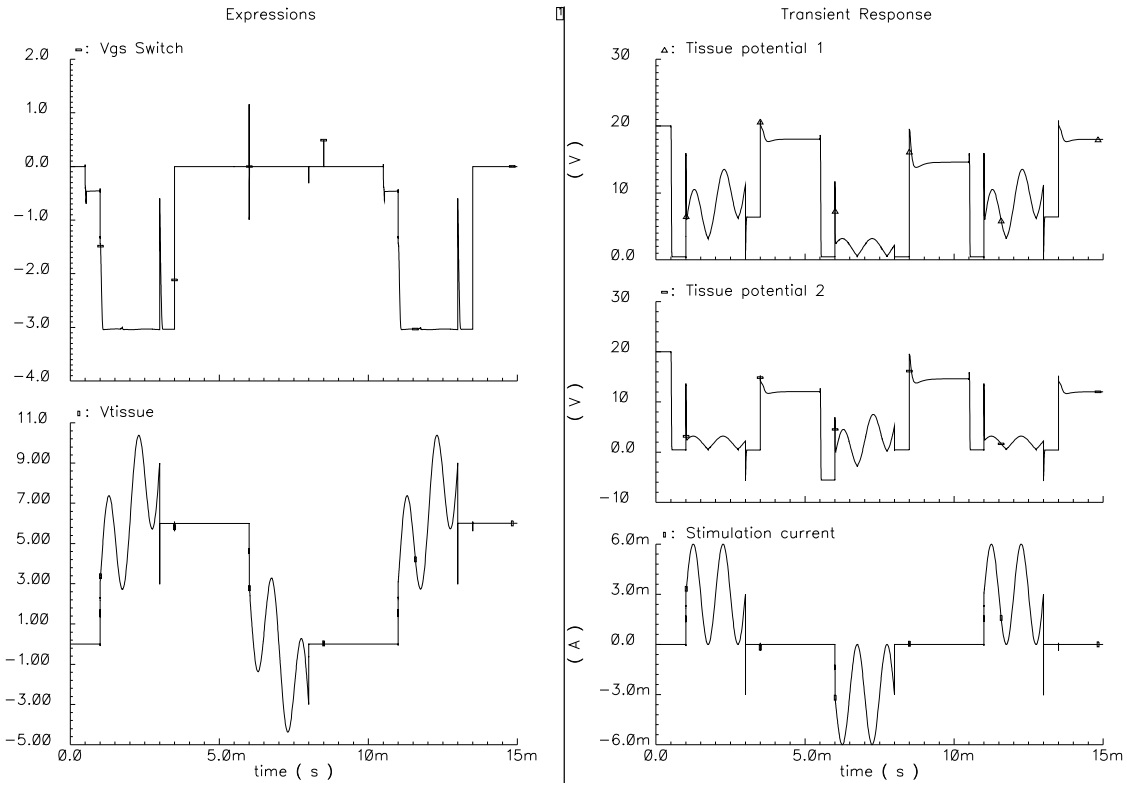


Figure 5.18: Simulation results of the switch array

enough to enable the switch. This is a fundamental limitation of using PMOS transistors only in the switch. It could be solved by adding NMOS transistors (which can only conduct values $< V_{DDhigh} - 3$), however it was already seen NMOS transistors have the fundamental limitation of having the bulk and source connected to each other, yielding leakage. Therefore using the chosen set up the voltages set at the tissue must be > 3.

In practice the voltages used for stimulation are usually much higher than 3 V, which means no problems are expected. Furthermore, when the voltage is lower than 3 V, the only thing that happens is that the injected current decreases, because the switches switch off. However, the decreased current is still copied to the charge cancellation circuitry with the same ratio. This means no charge mismatch errors are created. Therefore the switches are considered to be working well enough.

5.5 Complete system simulations

In this section simulation results of the complete system are discussed. First a testbench is created which is able to perform a complete stimulation cycle. This means it must be able to control all the system blocks and the charge cancellation functionality. Subsequently the correct functionality of the system if verified and the system performance is evaluated.

5.5.1 Testbench construction

Using all the blocks defined in the previous chapter and verified in the previous sections, the complete system can be constructed. First of all the inputs and outputs of the system need to be defined. An overview of the inputs and outputs is given in Table 5.1.

The input is the voltage source used to control the stimulation voltage for the tissue. As

Table 5.1: Inputs and outputs of the system

Inputs		Outputs	
Input	Stimulation Voltage source	Tissue	Tissue terminals
MOCD	MOCD control lines	SchmittOut	Output Schmitt Trigger
StimEnable	Enable stimulation		
ResetInt	Reset integrator		
Switches	Switch array control		
Internal signals			
Threshold	Charge threshold setting		
Reset	General reset (both counter and integrator)		
Enable	Override Enable signal from threshold		

mentioned before the implementation of this voltage source is outside the scope of this project and instead an ideal source is used. The input MOCD is the binary control of the MOCD. In this system it was chosen to implement 4 stages, which means this is a 4 bits signal. The Stim Enable signal is connected to the level shifter, which is subsequently connected to the gate of the stimulation enable switch. When this signal is high, the voltage set at the input voltage source is transferred to the tissue. On the other hand, when this signal is low, the stimulator is guaranteed to be off.

The reset signal is used to reset the integrator. Each stimulation cycle, the integrator must start with the same value in order to have exactly the same amount of charge injected. The signal switch is used to control the switch array. Since this array consists of 4 switches, this is a 4 bits signal. It might be considered in later designs to reduce this to a two bit signal and use a binary decoder to convert it back to 4 separate signals. For now simply 4 separate signals are used.

At the output first the tissue is found. Furthermore there is the output from the Schmitt trigger: a block shaped periodic signal, representing the number of charge packets inserted into the tissue.

The complete testbench is now depicted in Figure 5.19. The upper block is the block controlling the stimulator output stage, which is the lower block. Furthermore the tissue and the stimulation voltage source are easily recognized.

When the system is to be used in a complete stimulator system, more control signals would be needed. These signals are represented as 'internal signals' in Table 5.1. These signals are generated inside the control block. This is why they cannot be seen in Figure 5.19, but they are still required to control the stimulator. First it is required to set the charge threshold. It is a binary code representing a certain binary number of the counter. The counter was chosen to be implemented using 4 bits, which means the threshold is a 4 bits signal. The threshold is now set inside the threshold block.

In the final system one reset signal can be combined to reset both the counter as well as the integrator. Furthermore the StimEnable signal does need to be overrated by an additional signal called 'enable'. This will be explained later.

An overview of the control block (the upper block in Figure 5.19) is given in Figure 5.20. On the right the control sources for the signals MOCD and Switches are depicted. In the left part the charge cancellation scheme is depicted, consisting of a counter and a threshold block.

As can be seen, the output of the charge threshold circuit is connected to the StimEnable signal. when a certain threshold is reached, it can turn off the stimulation. However, the additional 'enable' signal is able to control this signal as well. This is required to turn off stimulation manually or when the charge threshold is not reached within a certain time.

The implementation of the charge cancellation scheme, consisting of the counter and threshold block are discussed a bit more in detail in the next section.

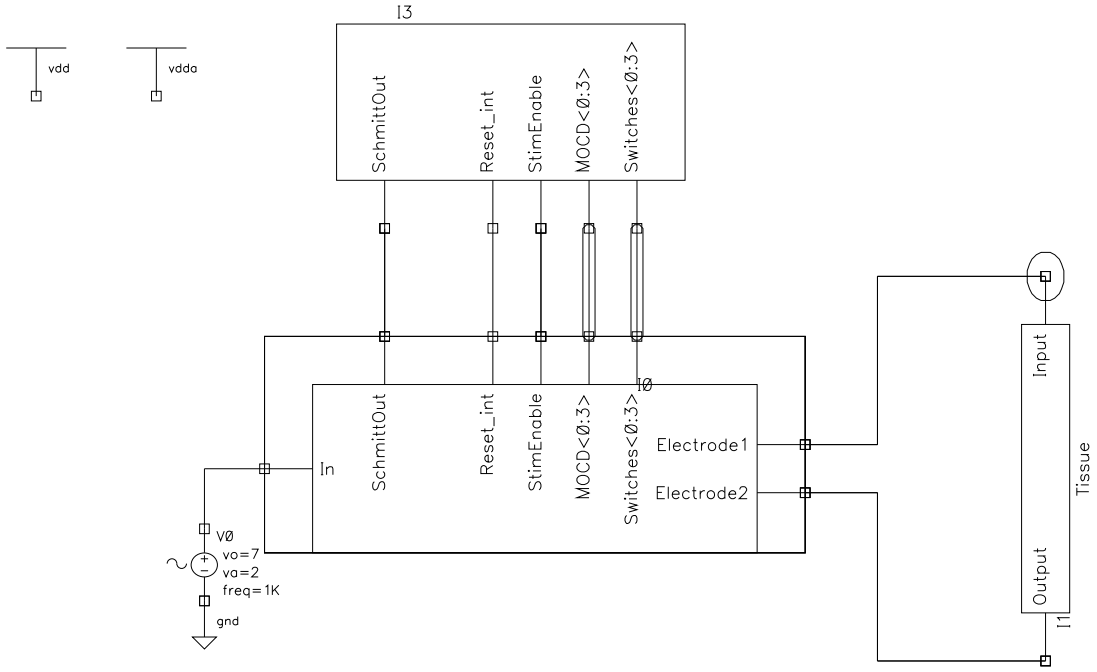


Figure 5.19: Overview of the testbench

Charge cancellation scheme

The task of this block is to count the number of periods outputted by the schmitt trigger. When a certain threshold of periods is reached, this should be detected. Therefore this part actually consists of 2 subparts: the counter and the threshold detector.

The counter is constructed with a well known scheme using T-flipflops [67]. A T-flipflop has only one input. Assuming the flipflop is positive edge triggered, the output of the T-flipflop is switched everytime a positive edge is detected at the input. This effectively means the output changes once every period, yielding a doubling of the period at the output. Cascading multiple T-flipflops will half the frequency every stage and effectively implements a counter.

A normal T-flipflop however is not quite good enough, since the counter must be reset. A T-Flipflop is constructed using a JK-flipflop with both inputs connected to one and the input connected to the CLK. The T-flipflop is tweaked by making it possible to set the J input to '0' as well. Any positive edge will then reset this flipflop. This means that when the flipflop is reset, a clock signal needs to be feeded into the T-flipflop input.

This means that during normal operation, the periods of the Schmitt trigger need to be passed, while during reset, the artificial clock needs to be passed to reset the flipflops. Solving a simple truth table yield the simple logic circuit representing this functionality. The complete circuit of the counter is depicted in Figure 5.21, while the implementation of the two blocks used are depicted in figure 5.22. In the left part the small block is depicted (responsible for feeding through the schmitt trigger output or the artificial clock signal) and in the right part the modified T flipflop.

Note that no special attention is paid to for example optimize this design, for example by sizing the transistors properly. The focus of this design was not on the digital part.

The threshold part was implemented simply by ideal voltage controlled voltage sources, as depicted in Figure 5.23. One input terminal is set to $0.5V_{dd}$, the gain is very high (1000) and the output voltage is bounded between 0 and V_{dd}. The threshold for each source can be set at '0' or '1' by changing the sign of the gain (In Figure 5.23 the threshold for the most significant bit ($In < 3 >$) is set at '0'). Subsequently the outputs of these sources are combined into a NAND

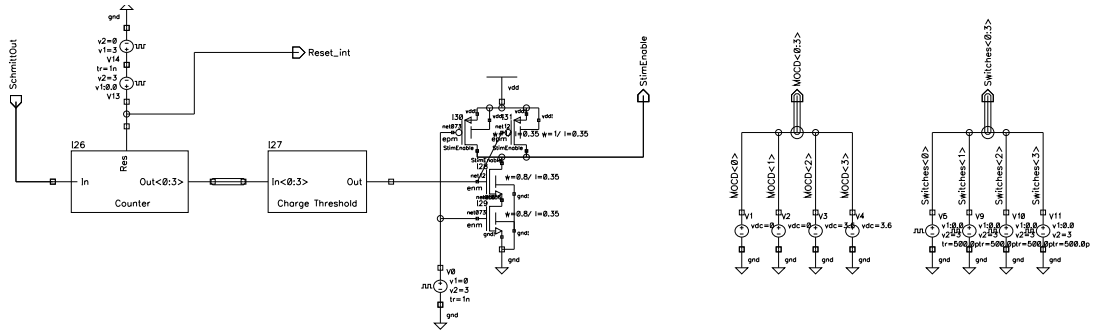


Figure 5.20: Implementation of the control block in the testbench

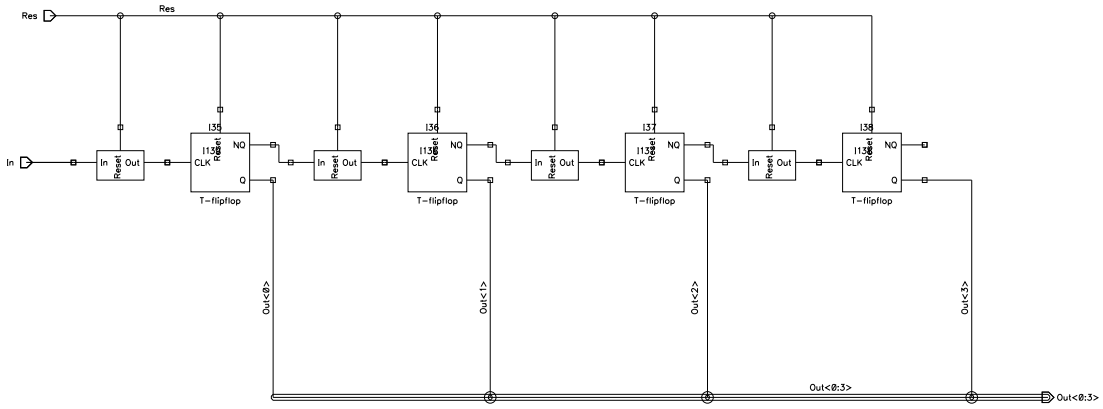


Figure 5.21: Implementation of the counter in the testbench

gate. When all the controlled sources have a high input, the output of this circuit will switch from high to low, indicating that the required threshold is reached.

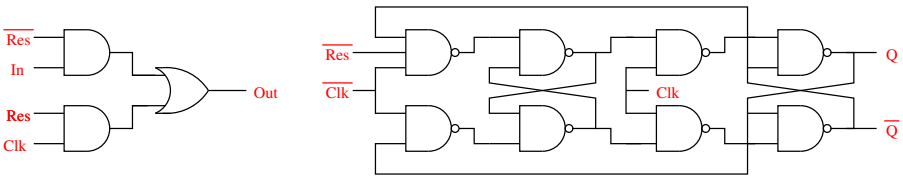


Figure 5.22: Implementation of the two blocks from Figure 5.21

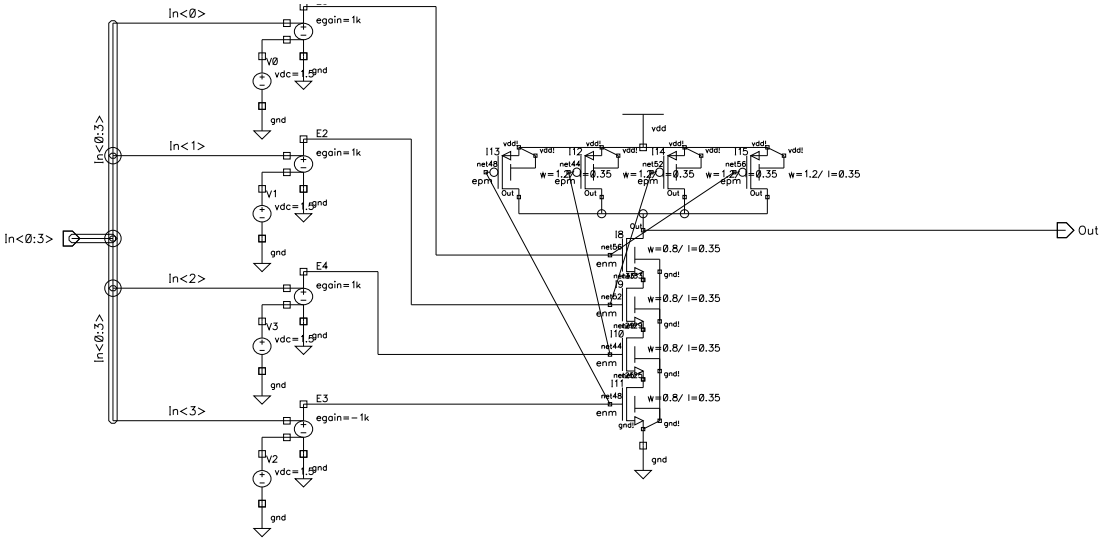


Figure 5.23: Implementation of the charge threshold block in the testbench

Stimulation cycle

To test the functionality of the system, a complete stimulation cycle is created. This means first a positive pulse is injected into the tissue with a certain threshold. Subsequently the direction of the current is reversed and the a second pulse is injected, while the charge threshold circuit will take care of the charge cancellation.

In Figure 5.24 the control signals used during the cycle are depicted. First the system is reset (note the signal depicted here is the internal reset, yielding a reset of the integrator as well as the counter). After the reset, the first two switches are enabled. Subsequently the enable signal is set high. This will lower the gate voltage of the stimulation enable switch, which will start the stimulation. The counter will count the injected charge packets until the charge threshold set (in the case of Figure 5.23 this is '0111') is reached.

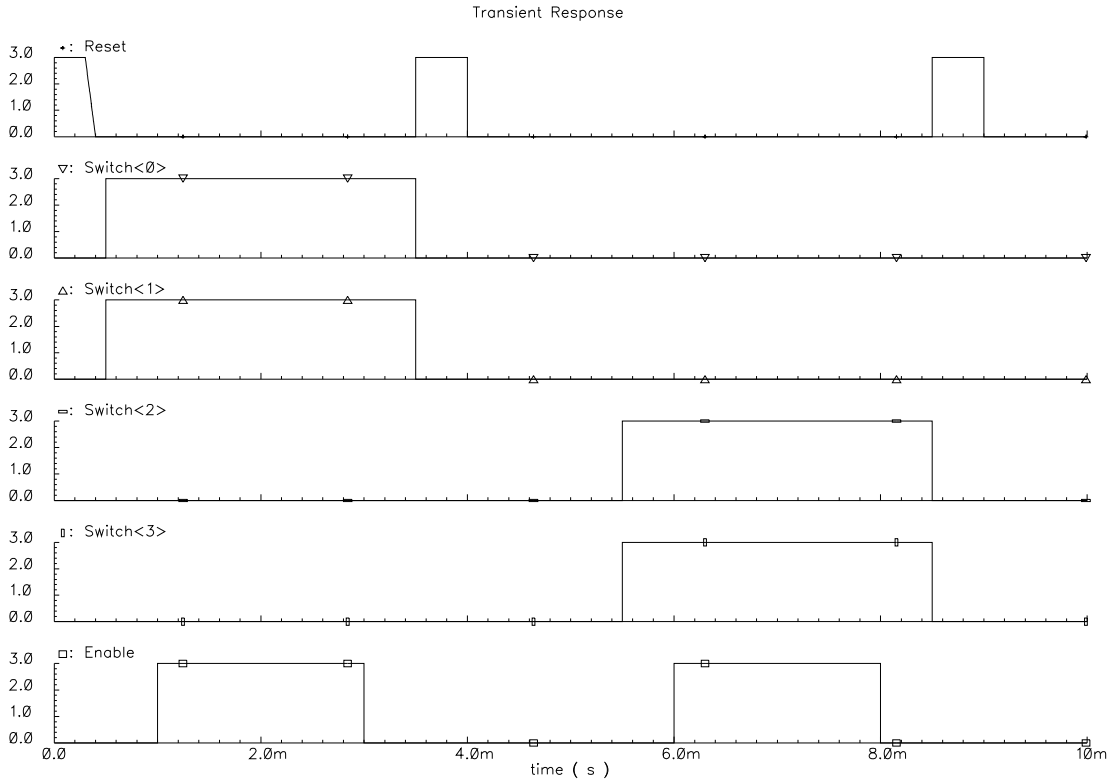


Figure 5.24: Control signals used for a simulation cycle

When the output of the threshold block becomes low this will make the StimEnable signal high again, stopping the stimulation. The system is given 2 ms of time to reach the threshold. After this time, the enable signal is made low again, which manually disables the stimulation. After this first signal all switches are closed and subsequently the system is reset again. The other two switches are enabled and the next inverse stimulation pulse is started by the enable signal.

The signals for the MOCD are kept constant during the complete stimulation cycle to cancel any static errors made by this block. For the input signal any type of waveform can be chosen. It is even possible to change the waveform for the second pulse while charge cancellation is still assured.

5.5.2 Simulation results

Using the testbench described above in combination with the stimulation cycle the system is tested. For the stimulation waveform a 1 kHz sinusoid is chosen with a DC offset voltage of 7 V

and an amplitude of 2 V. The tissue was modeled with a resistance of 10 kΩ and a capacitor of 75 nF. In later simulations these values will be changed.

The result of a complete stimulation cycle is depicted in Figure 5.25. In plot the voltage over the tissue is depicted. As can be seen during the first stimulation pulse the tissue is charged up to about −2.3 V. After the second stimulation pulse the charge stored at the tissue is almost canceled, yielding a remaining voltage of only 23 mV. This indicates that the principle of the circuit is working.

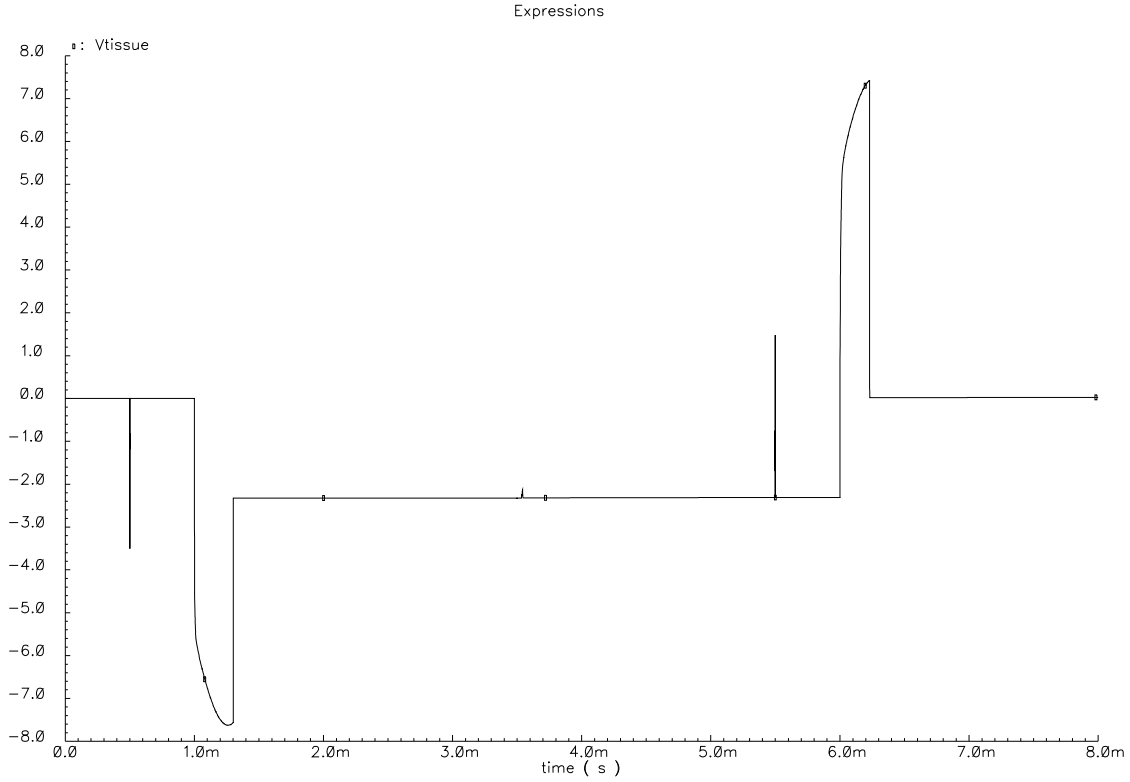


Figure 5.25: Tissue voltage during a complete stimulation cycle

In Figure 5.26 a detail of the first stimulation pulse is depicted. In the upper right plot the tissue voltage is again depicted. In the lower left plot the tissue current is depicted. As expected for a voltage of about 7 V the maximum current is almost 700 μA through the tissue with resistance of 10 kΩ.

In the upper right plot the output current of the MOCD is plotted. This is the current which will be fed into the integrator. As can be seen this current has a lot of spikes and some oscillations. Most spikes are very short, which means they don't have much influence on the output of the integrator. The spikes and oscillations are explained by the switching in the integrator (reversing the current to generate the periodic signal), which influences the output stage of the MOCD. The influence of these spikes on the total charge mismatch is treated later.

In the same subplot the output of the integrator (the schmitt trigger block shaped output) is depicted as well. Since the current does not vary a lot during this particular waveform, the output frequency is quite constant as well.

Finally in the lower right plot the ratio between the tissue current and integrator current is depicted. As can be seen the ratio is very constant around the expected value of 100. In the beginning some oscillations are still visible. These are the result of charging the capacitors in the MOCD output stage. It takes some time before the output stage is biased correctly. Again these oscillations do not cause any serious problems for the charge cancellation.

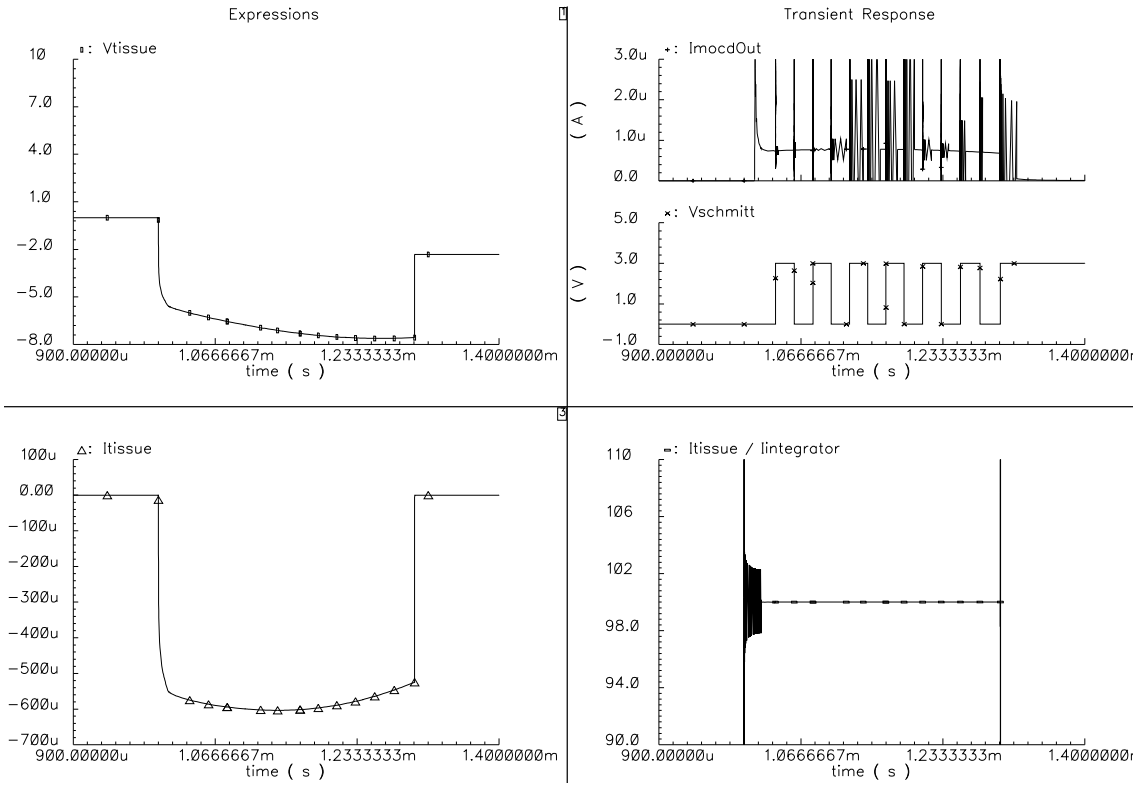


Figure 5.26: Detail of Figure 5.25 for one stimulation pulse (upper left: Tissue voltage, upper right: MOCD output current and Schmitt trigger output, lower left: Tissue current, lower right: Tissue/integrator ratio)

Sources of the remaining charge mismatch

The question is now what the main reason is for the remaining charge mismatch. In Table 5.2 an overview is given of the charge injected at various points in the circuit. This charge is obtained by integrating the current through the specific node over time. As can be seen from the table the charge at the driver nodes is very good matched to each other (the factor N is very accurate here).

However at the tissue something else happens. After the first stimulation pulse the tissue is charged up to 171.4 nC, corresponding to the charge injected via the driver. However, when the second pulse is injected, the tissue charge has changed to 170.6 nC. This means the tissue has discharged a bit. This can be explained by the finite impedance of the switch array when all switches are closed. During this time a very small discharge current is discharging the tissue with about 0.8 nC. When the second pulse is applied with the same amount of charge as the first pulse, this will mean the tissue has a charge mismatch, since the discharge of the tissue is not accounted for. Indeed a large part of the charge mismatch (1.5 nC) can be explained by the self discharge.

The fact that the closed switches indeed conduct a bit of current is confirmed using simulations. This means that about 50% of the remaining charge mismatch is due to the self discharge of the tissue. Note that in practice this value will most likely be much smaller. The interpulse delay is in this case quite long: more than 3.5 times as long as the pulse itself. When this period is made smaller, the charge mismatch will be smaller as well. Furthermore note that the bigger the tissue voltage after the first stimulation pulse, the higher the discharge current will be and thus a bigger charge mismatch.

In practice the charge mismatch due to self discharge poses no problem. Note that there is only a very small time for the tissue to discharge (only between the two pulses). After the second pulse the tissue is shorted and thereby given some time to discharge any remaining charge. Since

Table 5.2: Charge injection at different places in the stimulator

	$t = 0.5\,\text{ms}$	$t = 3.5\,\text{ms}$	$t = 5.5\,\text{ms}$	$t = 8\,\text{ms}$
Driver (tissue terminal)	1.14 pC	171.2 nC	171.2 nC	343.2 nC
Driver (integrator terminal)	2.79 pC	1.712 nC	1.712 nC	3.432 nC
Tissue	65.29 pC	171.4 nC	170.6 nC	1.583 nC

the shorted condition means the time constant of the tissue is greatly reduced compared to the situation in between the two pulses, the tissue should be able to discharge the remaining charge mismatch very quickly.

The other 50% of the charge mismatch is due to other factors. First of all note that this other 50% is also very easily discharged after the second stimulation pulse by shortening the tissue. Therefore it should not pose any problems to the functionality of the system. However it is investigated what is the most important source of the remaining error.

Based on the spiky response of the MOCD output showed in Figure 5.26 the MOCD can be expected to cause some errors. The biasing circuit of the output stage of the MOCD needs time to settle and the switching in the integrator causes some oscillations in this part. Furthermore it was already found that the gain of the MOCD circuit is not very constant over the complete current spectrum. The MOCD gain was set to be 0.125, which means the current gain has quite some variations (see Figure 5.11). Since the tissue current during the second pulse is much higher, this also causes mismatches.

Therefore the MOCD is most likely the component responsible for some of the remaining charge mismatch. When the MOCD is replaced by an ideal current divider the charge mismatch reduces to 12.87 mV, corresponding to 0.95 nC. This will also eliminate the settling time and spiking visible in Figure 5.26. This is illustrated in Figure 5.27. This figure is exactly the same as Figure 5.26, but this time the MOCD has been replaced by an ideal current divider. Since the self discharge during the interpulse delay is still present in this stimulation, the remaining charge mismatch due to the circuit itself is reduced to only 0.15 nC, yielding a mismatch as small as 0.08%.

From the simulation results discussed in this section it can be concluded the circuit as designed is working. The remaining charge mismatch is small and can easily be canceled out by shortening the tissue for a short period. The two main sources of remaining charge mismatch result from self discharge of the tissue and the MOCD.

5.5.3 Power consumption and efficiency

In literature a wide variety of power and efficiency measures are found. In some cases the total power consumption of the circuit is used, including used for stimulating the tissue. Is other cases the power used for stimulating the tissue is omitted. Furthermore in some circuits parts can be switched off, yielding a much lower power consumption.

First of all the total power consumption is obtained by measuring the current through the power supply, multiplying and multiplying it by the voltage. Two voltage supplies are required: V_{DDlow} and V_{DDhigh}. A third power supply with the same voltage as V_{DDlow} is used to power the control block. In this way the power consumed by the control block can be omitted. Furthermore the power injected in the tissue is found by multiplying the current through the tissue with the voltage over the tissue.

During a stimulation cycle the average power consumption can be obtained by integrating the instantaneous power consumption over time and subsequently dividing by the total time. The efficiency of the circuit is divided by the power injected to the tissue divided by the average power consumption.

First a closer look is taken at the maximum efficiency possible. It was already seen the maximum theoretical efficiency is determined by the factor N: the current used for integration and charge cancellation is not injected into the tissue and therefore 'wasted'. This limits the power

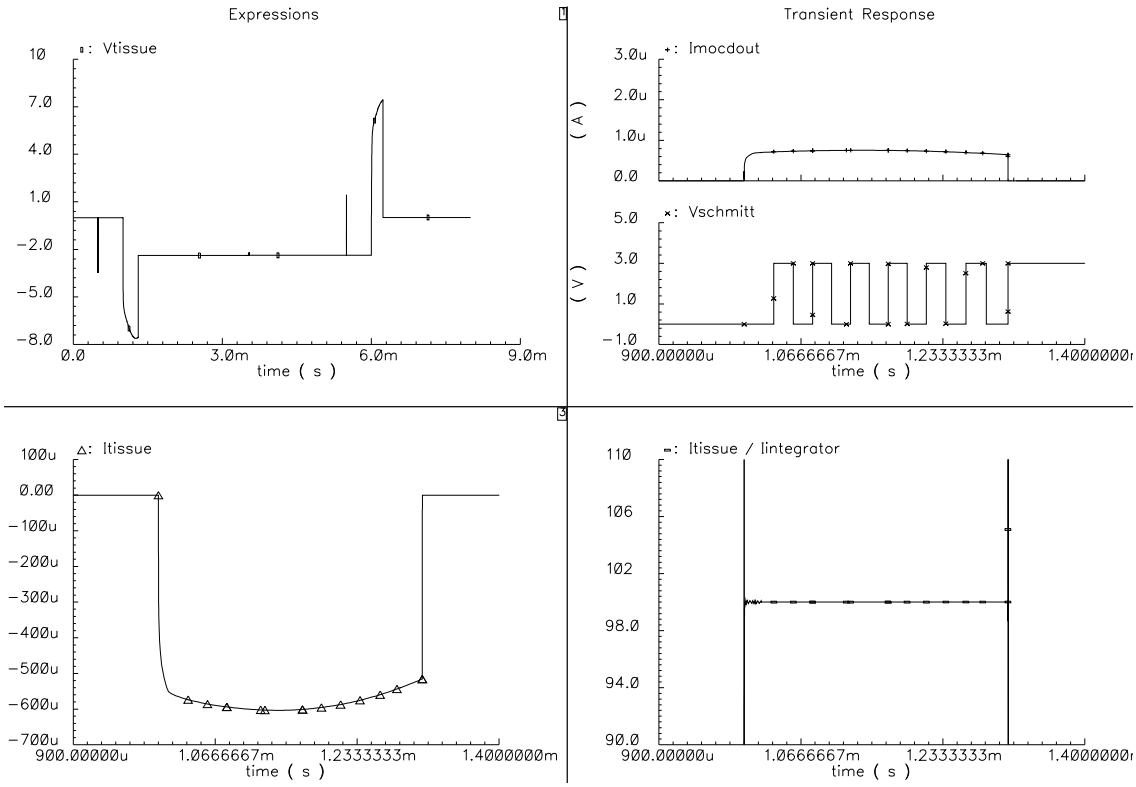


Figure 5.27: Detail of a stimulation pulse using the system with an ideal current divider (upper left: Tissue voltage, upper right: MOCD output current and Schmitt trigger output, lower left: Tissue current, lower right: Tissue/integrator ratio)

efficiency to 99% if $N = 100$. Furthermore the power efficiency is very much dependent on the voltage used for stimulation. When the tissue voltage is low, this will yield a large voltage drop over the driver transistors. This means quite a lot of power is 'wasted' in this transistors. When the tissue voltage is high, the voltage drop over the driver is small, and most power is injected into the tissue.

It is however important to note that when the voltage over the tissue is low, the current injected in the tissue is also low. This means that the total power wasted in the driver transistors is much lower as well. To see this the circuit is considered as follows: the voltage from V_{DDhigh} is divided between two impedances: Z_{tissue} and Z_{driver}. When the voltage over the tissue needs to be high, the value of Z_{driver} is made very small, which will lead to a small voltage drop over this impedance. When the voltage over the tissue needs to be low, Z_{driver} is large. For the tissue voltage it holds:

$$V_{tissue} = \frac{Z_{tissue}}{Z_{driver} + Z_{tissue}} V_{DDhigh} \qquad \rightarrow \qquad Z_{driver} = \left(\frac{V_{DDhigh}}{V_{tissue}} - 1 \right) Z_{tissue} \tag{5.2}$$

The total impedance can now be expressed as function of V_{tissue}:

$$Z_{total} = \left(\frac{V_{DDhigh}}{V_{tissue}} - 1 \right) Z_{tissue} + Z_{tissue} = \frac{V_{DDhigh}}{V_{tissue}} Z_{tissue} \tag{5.3}$$

The power consumption can now be easily found. Noting the power consumption in the tissue is $P_{tissue} = V_{tissue}^2 / Z_{tissue}$, it is found:

$$P_{total} = \frac{V_{dd}^2}{Z_{total}} = \frac{V_{tissue}}{Z_{tissue}} V_{DDhigh} \qquad P_{loss} = \frac{V_{tissue}}{Z_{tissue}} V_{DDhigh} - \frac{V_{tissue}^2}{Z_{tissue}} \tag{5.4}$$

These equation are plotted in Figure 5.28 for $V_{DDhigh} = 10$ and $Z_{tissue} = 1\,\text{k}\Omega$. Furthermore the efficiency is plotted by $\eta = 100P_{tissue}/P_{total}$.

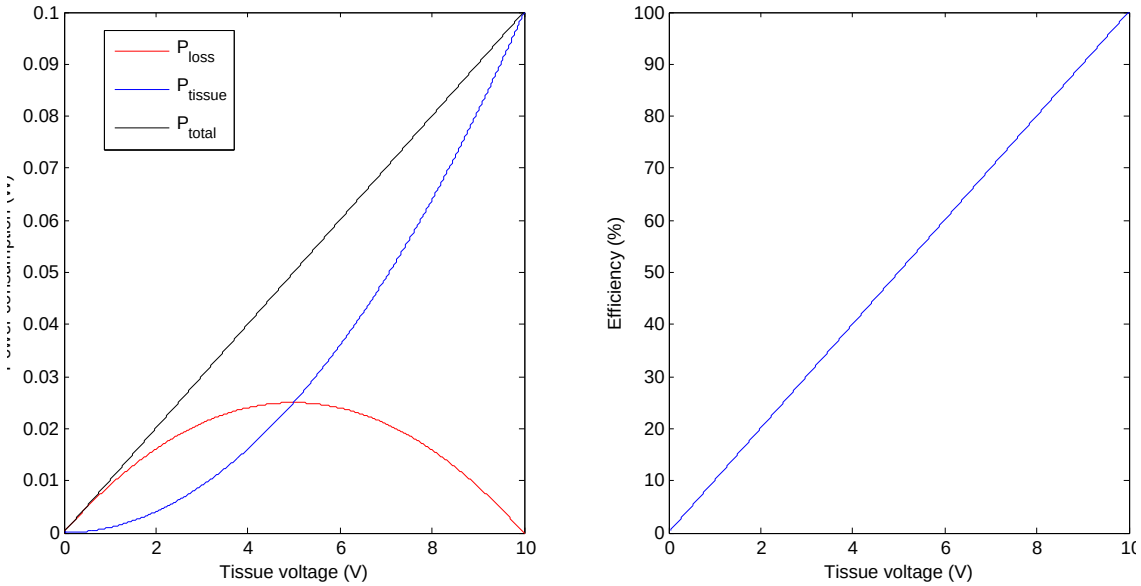


Figure 5.28: Power consumption of the tissue compared to the driver as a function of V_{tissue}

From this figure it is seen the efficiency is indeed a linear function of the tissue voltage. However, the absolute power loss is maximum when $V_{tissue} = 0.5V_{DDhigh}$. Therefore for the voltage based stimulation as proposed the efficiency only is not a very meaningful quantity. Therefore in order to investigate the worst case, the stimulation voltage should be chosen around $0.5V_{DDhigh}$. In this case the efficiency is only 50%, but the absolute power loss is maximum. Note that in the equations above the influence of the switch array is ignored. There will be a voltage drop over these switches as well, yielding power a power loss as well.

In order to increase the efficiency the value of V_{DDhigh} can be made dependent on the stimulation waveform. When the maximum stimulation voltage sued is for example only 5 V, the efficiency of the system can be improved a lot when $V_{DDhigh} = 5\,\text{V}$ only. When the V_{DDhigh} would follow the stimulation voltage exactly this would theoretically bring the efficiency of the system close to 99%, determined by the factor N.

Note that a varying V_{DDhigh} requires no significant redesign of any of the components of this output stage. Only the required bias voltages of the level converter ($V_{DDhigh} - V_{DDlow}$) will need to be made dependent as well. The functionality remains unchanged.

Realizing the statements made before the power consumption of the circuit can be analysed. In Figure 5.29 the power consumption of V_{DDhigh} and V_{DDlow} are depicted for a stimulation cycle. The plots are obtained by integrating the current from the supplies multiplied with the voltage over time. What is actually plotted is therefore the energy delivered by the power supply over time. An average power consumption can be obtained by dividing a certain energy difference by the time it took to deliver this energy.

Contribution of V_{DDhigh}

First a closer look is taken at the V_{DDhigh}. Note that in the plot the power used by the driver circuit and the enable switch are omitted. These are discussed later. The power consumption depicted now is mainly dominated by the static power consumption by the current sources in the voltage feedback network and the high voltage switches in the switch array. The average power

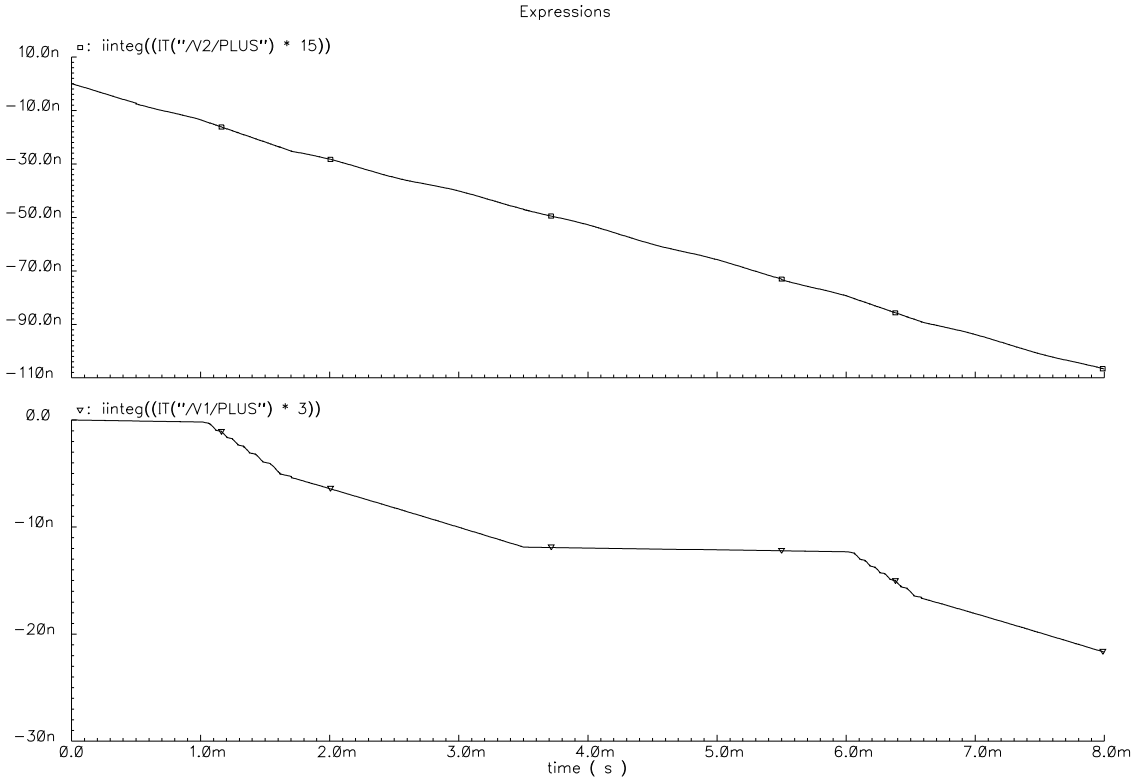


Figure 5.29: Power consumption of V_{DDhigh} (upper plot, excluding driver and enable switch) and V_{DDlow} (lower)

Table 5.3: Energy and Power consumption of the Driver and Tissue

V_{tissue}	Pulse width	E_{total}	E_{tissue}	E_{loss}	$\bar{P}_{total}$	$\bar{P}_{tissue}$	$\bar{P}_{loss}$	η_{ideal}	η
3.5 V	2.89 ms	1.36 μJ	0.245 μJ	1.12 μJ	471 μW	84.8 μW	386 μW	0.23	0.18
7.5 V	1.72 ms	1.34 μJ	0.584 μJ	0.759 μJ	783 μW	341 μW	442 μW	0.5	0.44
11.5 V	1.45 ms	1.34 μJ	0.926 μJ	0.413 μJ	926 μW	640 μW	285 μW	0.77	0.69

consumption over the 8 ms simulation is 13.25 μW. Biggest part of this is due to the 600 nA biasing of the voltage feedback stage, which corresponds to 9 μW at $V_{DDhigh} = 15$ V. However, the current from this source is decreased when the stimulation enable switch is enabled, because the source is 'shorted' to V_{DDhigh}. The current now depends on the gate voltage: the closer it is kept to V_{DDhigh}, the lower the current is from this source.

Therefore: the contribution of this source is determined by the combination of the current when stimulation is enabled and disabled. The current consumed by the high voltage switch is constant at about 100 nA corresponding to 1.5 μW. Having 4 switches this totals to 6 μW.

The power consumed by the driver depends very much on the waveform as was discussed before and summarized in Figure 5.28. This is verified by comparing the power injected by V_{DDhigh} in the driver stage and the power actually injected into the tissue. To compare different tissue amplitudes, the stimulation waveform is changed to a DC shape with three different amplitudes: 3.5 V, 7.5 V, 11.5 V. Since $V_{DDhigh} = 15$ it is expected to have the highest power consumption in the driver (P_{loss}) when $V_{in} = 7.5$ V. The simulation results are depicted in Table 5.3.

Since the charge threshold is the same for all simulations the total energy used is the same for

all simulations (the injected charge times V_{DDhigh} is constant). Because the voltage over the tissue and driver is different, this corresponds to different energy distributions. When this is translated to the average power consumption (divide it with the pulse width) it can be seen the observations made in Figure 5.28 are correct: $\bar{P}_{loss}$ is maximum when $V_{in} = V_{DDhigh}/2$.

In the last two columns of Table 5.3 the ideal efficiency corresponding to the right plot of Figure 5.28 is showed ($\eta_{ideal} = V_{in}/V_{DDhigh}$) and it is compared to the efficiency from simulations. The difference between the two in mainly due to the power lost in the switch array, which was neglected in the calculation of η_{ideal}. It can be concluded that from the point of efficiency it is better to use an as high amplitude as possible. The amount of energy injected in the tissue can then be adjusted by charge threshold.

Finally the contribution of the stimulation enable switch is checked. When this switch is disabled, the stimulation is on and the current through the switch is very small. At this point the power is consumed by the driver stage as discussed before. However, when the switch is enabled, it tries to keep the gate voltage at V_{DDhigh} by shorting it to V_{DDhigh}. This breaks the voltage feedback loop.

However, the differential pair at the input will still try to make pull the gate voltage to the value which will make the difference between the stimulation source and the tissue voltage towards zero. This means the transistors in the differential stage will still be biased and enabled, yielding a DC path towards ground. Therefore a large current will flow from V_{DDhigh} trough the stimulation enable switch and through the differential pair towards ground. This current might be as big as $200\,\mu$A, yielding a power consumption of 3 mW. This of course is not desired.

One way to solve this is to set the stimulation voltage to the value corresponding to the situation in which $V_{gate} = V_{DDhigh}$, yielding $V_{in} = 0$ V. This means the stimulation voltage source will need to be controlled as well: only when the stimulation is enabled, the stimulation voltage source needs to be on, in all other cases it needs to be 0 V to keep the power consumption low.

This does not mean the stimulation enable switch has become obsolete: it is still an extra safety measure to grantee no charge is injected in the tissue. If anything in the stimulator would go wrong, yielding an incorrect control of the stimulation voltage source, the stimulation enable switch can still assure no charge is injected in the tissue when it is not supposed to be injected.

Contribution of V_{DDlow}

The contribution in the power consumption of V_{DDlow} is plotted in the lower part of Figure 5.29. The largest contribution in the power consumption is due to the Schmitt Trigger. Three different 'phases' can be clearly distinguished:

Integrator reset In this phase the integrator is reset, which means the input voltage of the Schmitt trigger is 0 V. the power consumption is very low now. The main static component is the current flowing through the threshold compensating inverter (in branch M_7-M_3-M_4-M_8 from Figure 4.44). The Schmitt trigger is in this phase during $t < 1$ ms and 3.5 ms$t < 6$ ms and the power consumption is ≈ 200 nW.

Note that the MOCD is not consuming energy, since when no current is flowing into the MOCD, the bias current of the output stage is also 0 A. meaning no static power consumption.

Integrator is integrating In this phase the Schmitt trigger consumes the most power. The power consumption is very dependent on the input current (which determines the frequency of the output signal). However, the total energy required to generate the amount of periods required to reach a certain charge threshold is more or less equal. For the charge threshold set in the simulation, the required energy was about 3 nJ and the average power consumption during the pulse was about $7.2\,\mu$W.

The MOCD is also consuming energy. Again this is very much dependent on the amount of current through the MOCD, since that will also determine the biasing of the MOCD output

stage. In this particular case the MOCD has used about 0.7 nJ of energy. Therefore it is not the main energy consuming component (which is the schmitt trigger).

Integrator reached threshold When the integrator has reached its threshold, but is not yet reset, the power consumption is slightly different. In this case the voltage over the capacitor is, depending on the sign of the counter either 0.5 V or 2.5 V, the threshold levels of the Schmitt trigger. Assuming it is 2.5 V, the PMOS transistor of the threshold compensated inverter is slightly 'on'. Therefore a static path will exist between V_{DDlow} and ground. This yields an average power consumption of about 3.6 μW.

Total power consumption

Summarizing it can be stated the power consumption is very dependent on the stimulation waveform and timing used. There are however a few sources yielding static (quiescent) power consumption. The biggest contribution is formed by the voltage feedback biasing and the switches, yielding a quiescent power consumption of 15 μW at maximum. Compared to the quiescent power consumption reported in [75] (see table 2.3). The rest of the power consumption is dependent on the charge threshold, the stimulation current. Furthermore the timing is also important: the time difference between the moment the charge threshold is reached and the moment the integrator is reset determines the duration of the Schmitt Trigger being in phase 3.

5.5.4 Waveform flexibility

One of the major design criteria for this design was the ability to use a wide variety of waveforms. while still assuring charge cancellation. In this section a couple of simulation results are depicted for different waveforms. Note that in principle every waveform shape can be used by adjusting the stimulation voltage source to the desired shape.

In Figure 5.30 a square shaped and sinusoidal shaped stimulation waveform is used. In each figure the tissue voltage, the tissue current and the output of the Schmitt Trigger is depicted. It can be clearly seen the current is an exponentially decaying current with a relatively large time constant and the frequency of the Schmitt Trigger is clearly a function of the current. Furthermore for both waveforms charge cancellation is assured as can be seen from the fact the final tissue voltage is about 0 V.

Both simulations from Figure 5.30 use a symmetrical waveform for the two simulations. This is no requirement as shown in Figure 5.31. Here a burst type of stimulation is shown in the left part and a triangular waveform in the right part. The charge cancellation pulse consists of a DC pulse, yielding an asymmetrical stimulation. Again charge cancellation is assured as can be seen by the final voltage of the tissue after stimulation.

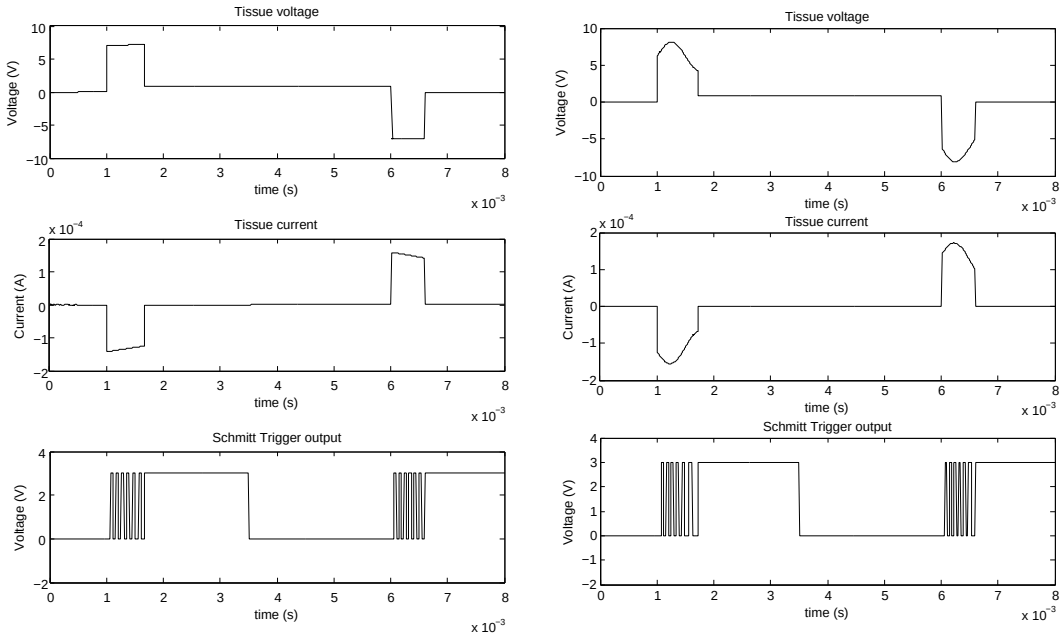
Figures 5.30 and 5.31 show that the system is very flexible in terms of waveforms. In principle any waveform can be injected in the tissue. The most important limitation is formed by the voltage feedback network, which has finite frequency characteristics and slew rate. If these limitations are exceeded, the tissue voltage might be different from what was expected. However the charge cancellation is still assured.

5.5.5 Tissue Variations

As explained before the parameters for the tissue impedance can vary significantly from patient to patient. The stimulator system must be able to cope with these changes. Therefore it is checked how the system responds to varying values for R_{tissue} and C_{tissue}.

Variations in R_{tissue}

As seen in the simulations of the voltage feedback loop, the value of R_{tissue} determines the maximum stimulation current upon switching the stimulator on. Furthermore it also determines the



(a) Block shape

(b) Sinus shape

Figure 5.30: System response for a block (left) and shifted sinusoid (right) shaped stimulation

time required to reach threshold. It was chosen to do a simulation for the system for values values of $1\,\mathrm{k\Omega} < R < 100\,\mathrm{k\Omega}$. The results are depicted in the left part of Figure **??**.

A couple of important this are to be noticed from this figure. First of all the final tissue voltage for all values of R is the same and close to zero (except for $R_{tissue} = 100\,\mathrm{k\Omega}$). This indicates the charge cancellation in the system still works properly for variations in R. Note that the settings for the MOCD and the charge threshold are the same for all simulations, explaining why the pulse width varies a lot when R varies.

Clearly for $R = 100\,\mathrm{k\Omega}$ the system shows a different response. Due to the small current injected the charge threshold is not reached before the system is reset again at $t = 3\,\mathrm{ms}$. Therefore the charge cancellation cannot be achieved anymore and the final voltage will be different. This can be solved by either changing the charge threshold or by giving the system more time to reach threshold.

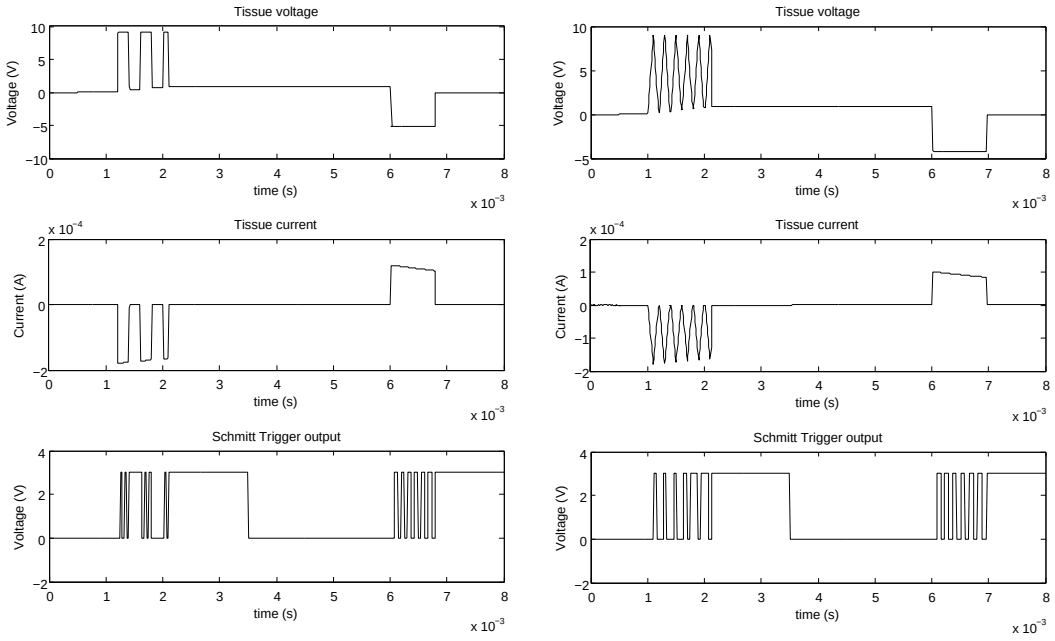
Furthermore it is remarkable the tissue voltage is different during stimulation. During stimulation the tissue voltage is determined by the voltage feedback loop and due to this it is expected the tissue voltage should not depend on the value of R. The voltage feedback loop is measuring the tissue voltage with respect to ground. However, one side of the tissue is connected to a switch which is connected to ground. Due to a non zero equivalent impedance of the switch, the voltage over the tissue will not be equal to the voltage set by the voltage feedback.

The voltage drop over the switch is dependent on the current through the switch. This explains why for different values of R, the voltage over the feedback network changes. For low values of R, the current is high, yielding a higher voltage loss over the switches, yielding a lower voltage over the tissue.

Variations in C_{tissue}

The capacitor determines the amount of charge required to charge the tissue to a certain voltage as discussed before as well. In the right part of Figure 5.32 the system response is depicted for varying tissue capacitor values ($10\,\mathrm{nF} < C < 100\,\mu\mathrm{F}$).

As can be seen the voltage the tissue is charged to after the first stimulation pulse is decreasing



(a) Block shape burst

(b) Triangle shape burst

Figure 5.31: System response for a burst (left) and triangular (right) stimulation

while C_{tissue} is increasing, just as expected (when $Q = CV$ is constant and C is increasing, V must decrease). Furthermore it can also be seen the voltage over the tissue is now almost constant. This confirms the statements about the current dependent voltage drop over the switches in the previous section: for varying C_{tissue} the current is constant and therefore also the voltage drop over the switches.

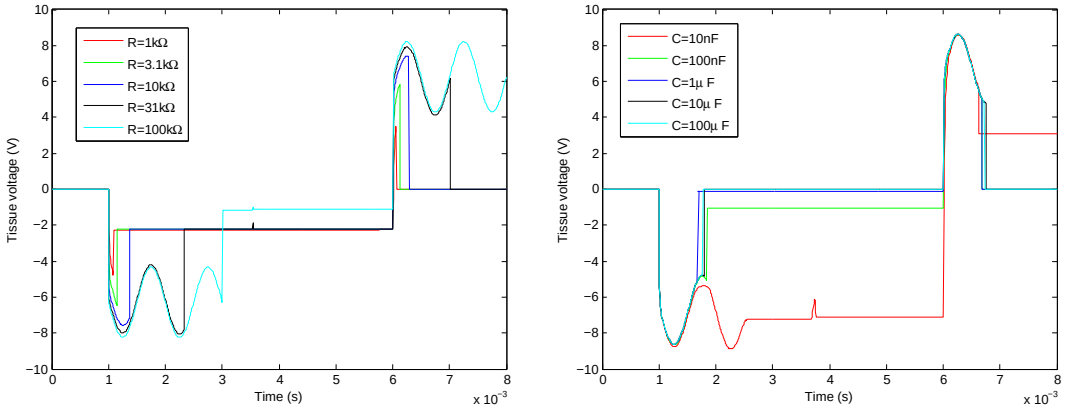
Furthermore it can be seen the final tissue value is almost constant and very close to 0 V among the different values for C_{tissue}. This means the charge cancellation is working as expected. It is noted that for $C = 10\,\text{nF}$ the charge is not canceled. This is due to the fact that after the first stimulation pulse the charge threshold is not yet reached. Due to the small value of the capacitor, the tissue voltage is increasing quite rapidly, without injecting a lot of charge. During the second pulse the threshold is reached, because at the pulse start the tissue is charged to a very negative voltage. The voltage can now change enough in order to reach the threshold, but of course now a different amount of charge is injected compared to the first pulse.

5.5.6 Process Variations

The robustness of the system is a very important constraint for biomedical applications as has been pointed out before. This also means the system needs to be able to handle process variations properly. When it comes to process variations, two important measures can be distinguished: process corners and process mismatch. They are treated separately here.

Process Corners

The process corners are defined as the statistical maximum inter-die variations. These variations occur due to many aspects such as the die position on a wafer or atmospheric variations during the manufacturing. The consequences of these variations is that all transistors and parameters on a single dire have the same variations. For example: the doping of all NMOS transistors in die A is such that they become much stronger compared to the transistors in die B. The process corners are now defined as the statistical maximum deviations of these parameters. For



(a) Resistance variations

(b) Capacitance variations

Figure 5.32: System response for tissue variations

Table 5.4: Process Corners

Corner type	4σ corner	6σ corner
Typical	typ	typ
Strong N, Strong P	wcp	awcp
Weak N, Weak P	wcs	awcs
Weak N, Strong P	wc0	awc0
Strong N, Weak P	wc1	swc1

the I3T80U technology 4 different corners are specified compared to the 'typical' corner with two different standard deviations as depicted in Table 5.4.

The names for the process corners are 'worst case power' (when both N and P are strong, the static leakage current is relatively high), 'worst case speed', 'worst case 0' and 'worst case 1'. When adjusting the corners the parameters for all transistors (both the MOS and DMOS types) are changed. The parameters for the passive components are not changed. The system is now tested for all process corners with the 4σ deviations. For the tissue is was chosen $R_{tissue} = 10\,\mathrm{k\Omega}$ and $C_{tissue} = 75\,\mathrm{nF}$, the stimulation voltage was a sinusoid with a 2 V amplitude on top of a 7 V DC voltage (the same parameters while testing the complete system in the typical corner).

The simulation results are depicted in Figure 5.33. As can be seen the stimulation waveform for the different process corners is quite different. However, the resulting voltage over the tissue after the two stimulation pulses is still close to zero. This means the charge cancellation is still assured.

Note that the voltage over the tissue is quite different for each process corner. This is mainly due to a combination of factors. First of all it was chosen to implement the biasing of the voltage feedback stage without biasing loops. This means that when the transistor parameters change, the bias current and voltages correspond not with the transistor anymore. This will lead to DC voltages at the output of the stage. These offsets will subsequently lead to an offset at the driver gate, which will lead to an offset in the tissue current and therefore at the tissue voltage.

This effect is further enhanced by the switch array. When the current is changed, the voltage drop over the switches (for which the parameters also changed) will change as well. Both effects will clearly yield a voltage deviation over the tissue as depicted in the figure.

Note that in the 'wcp' corner the discharge of the tissue during the interpulse delay is the

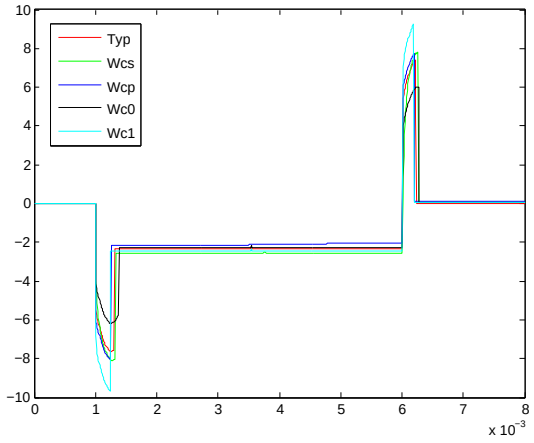


Figure 5.33: Simulation results of the system for different process corners

largest. This is explained quite easily, since in this corner the impedance of the switches is the lowest. This means the RC time is the lowest, yielding the fastest discharge. This will also mean in this corner the charge mismatch is the largest (about 0.1 V). However, this can of course be reduced significantly if a shorter interphase delay is chosen.

It can be therefore concluded that the system is working fine for all 4 process corners.

Mismatch

Mismatch is in contrast to the process corners the deviation in component parameters on a single die, which means it is an intra-die phenomenon. This means the parameters of components have slight variations with respect to each other. This type of variations is most easily simulated using a Monte Carlo simulation for which each run the parameters of the components are slightly changed according to statistical models.

A Monte Carlo simulation with 100 runs is performed for the circuit. In Figure 5.34 the results are depicted. The effect of the mismatch is clearly visible: the stimulation waveform is clearly affected by the mismatches introduced. It is investigated if the system is still working properly.

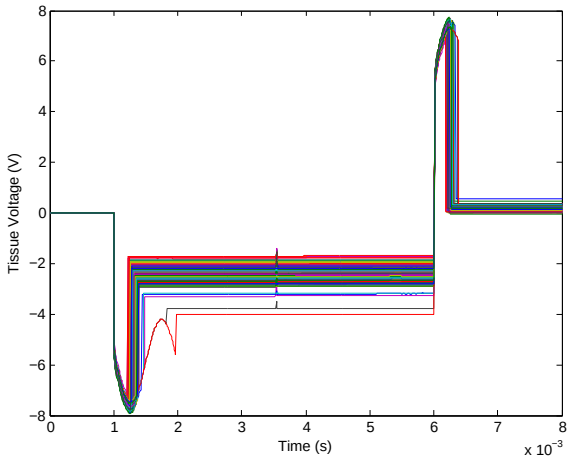


Figure 5.34: 100 run Monte Carlo simulation of the stimulator

First of all the voltage over the tissue after the first stimulus varies quite a lot. This can be

explained easily by the mismatches: when for example the two driver transistors have a mismatch, the total amount of charge injected varies. The amount of variation in the tissue voltage after the first stimulation waveform is depicted in the left histogram in Figure 5.35. As can be seen the variation is quite significant, reaching from almost $-4\,\mathrm{V}$ towards $-1.5\,\mathrm{V}$. In principle this is not a very big problem, as long as the charge is exactly canceled in the end.

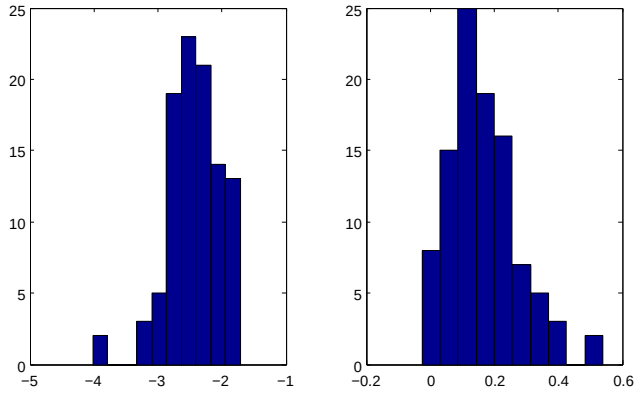


Figure 5.35: The tissue voltage at two different time instances during a 64 run Monte Carlo simulation

In the right part of Figure 5.35 the final tissue voltage is depicted for all runs. Here it is clear that quite a large variation is found in the final tissue voltage. The tissue voltage can reach as far as $\pm 0.5\,\mathrm{V}$. Clearly this is not a desired situation and it can be concluded that the system as designed now has some problems with internal mismatches.

The most likely component that is having problems is the current splitter (MOCD). Actually two factors play a role in the errors resulting from the monte carlo simulation. First of all the MOCD is only working with a constant current gain in a limited current range. This means that when the current changes due to process mismatches, the MOCD might not be working in the optimal range anymore.

Furthermore the output stage in this circuit used to keep the output and dump line voltages equal partly operates in the triode region. In this region the transistors are quite susceptible to process variations. This means that this easily results in large spreads in this part of the system. To check the influence, a Monte Carlo simulation is done for the MOCD. The MOCD was given a gain of 0.125 (three active MOCD stages) and the ratio I_{out}/I_{in} was simulated for 100 monte carlo mismatch runs. The results are depicted in Figure 5.36.

As can be seen the spread in current gain is quite significantly (ranging from about 0.05 towards almost 0.2). Furthermore the influence becomes even bigger when the current injected becomes small (the current gain ranging from 0 up to 1.2). This might lead to significant mismatches. Consider the situation in which the injected current in the first pulse is due to mismatches too small, which will lead to a very unpredictable current gain of the MOCD. In the second phase the current is higher (due to the fact the tissue has been precharged) and the current gain of the MOCD will now be significantly different. This will lead to charge mismatches.

To further illustrate the influence of the mismatches in the MOCD (output stage), a monte carlo simulation for the integrator is run. A block shaped input current is used, which consists of a current of $5\,\mu\mathrm{A}$ which is on between $10\,\mu\mathrm{s} < t < 80\,\mu\mathrm{s}$. The voltage over the integrating capacitor is depicted in Figure 5.37(a). As can be seen the frequency has a fairly large spread. Without mismatch the output frequency is 28 kHz, while now the frequency is between 15 kHz and 50 kHz.

The reason for this is mainly the mismatch in the in triode operating input transistors of the output stage of the MOCD. This is depicted in Figure 5.37(b). Here the differential voltage of the input and dump line of the MOCD is depicted. This voltage should ideally be 0, but as can be seen a significant spread is found here.

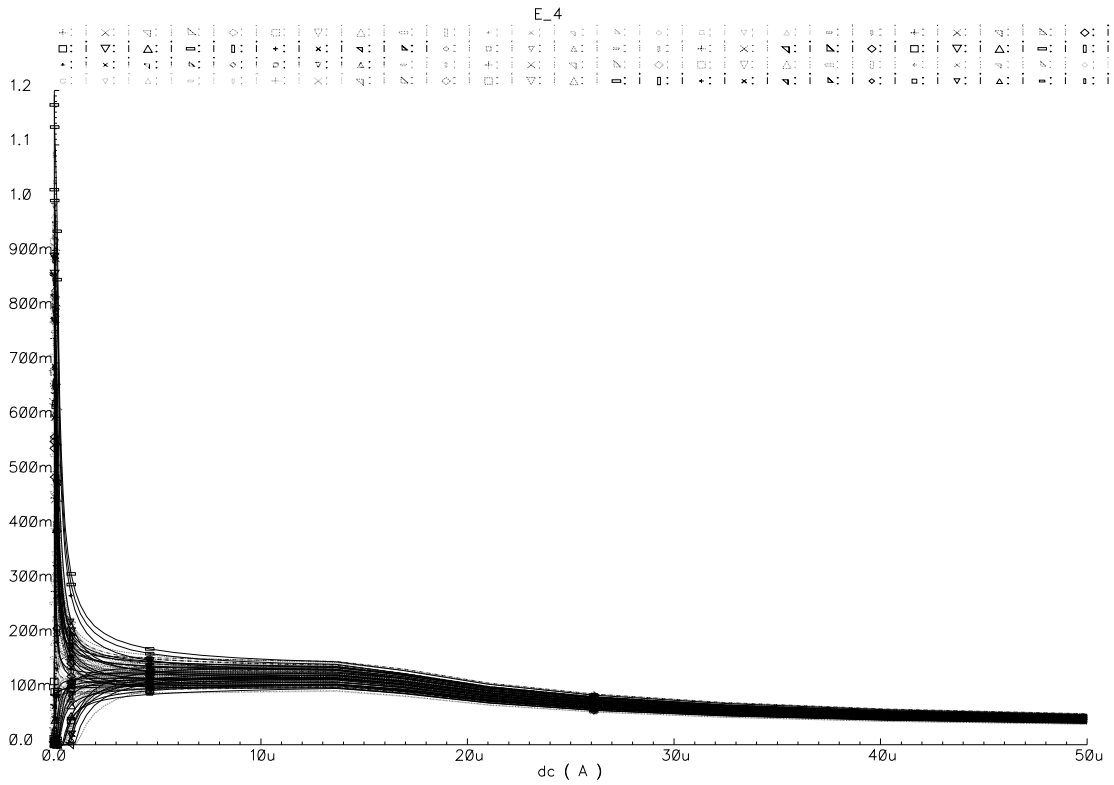


Figure 5.36: 100 run Monte Carlo mismatch simulation for the MOCD current gain

Therefore it is concluded that the MOCD is most likely the main source of mismatch errors in the system. To check whether the MOCD is indeed the component responsible for the problems during the monte carlo simulation of the complete system, the component is replaced by an ideal current splitter (a current controlled current source) and the monte carlo simulation is done again. The results are depicted in Figure 5.38. It can be clearly seen the deviations are much smaller.

In Figure 5.39 a similar plot is made as in Figure 5.35 for the stimulator with the ideal MOCD. In the left figure it can be seen a smaller spread for the voltage after the first stimulation pulse is now achieved. Also the shape of this histogram (close to a normal distribution) indicates a more expected behaviour. Furthermore note that a bit of spread in the injected charge is not a big problem for the functionality of the system as explained before.

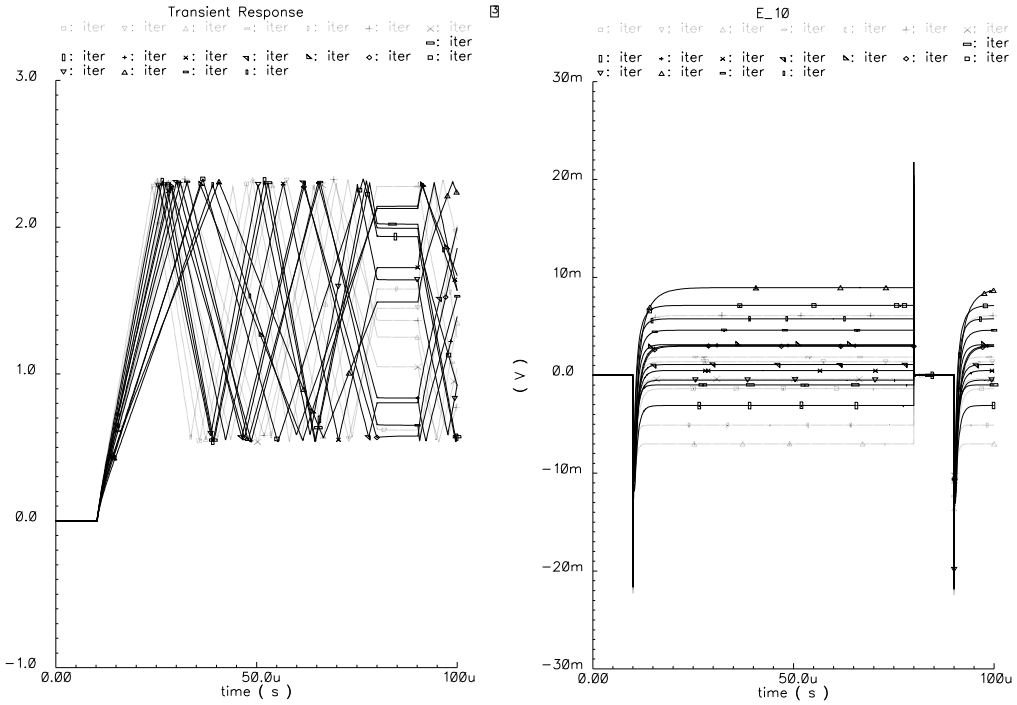
In the right part of Figure 5.39 it is also clear the charge cancellation is working properly again: the resulting voltage at the tissue has a much smaller spread. This indicates that indeed the MOCD was the problem in the robustness against process mismatch.

Note that in Figure 5.38 still the voltage over the tissue is not constant during the different monte carlo runs. This can be explained by the same reasoning as before: due to mismatches the biasing of the voltage feedback stage is affected yielding to offset at the gate. Furthermore the equivalent resistance of the switches is affected as well.

Conclusions

Based on the observations made in the previous sections it can be concluded that a stimulator output stage has been designed with a very high flexibility, a quite accurate charge cancellation scheme which is very robust in terms of process and tissue variations. The quiescent power consumption is reasonably low of about $15\,\mu$W.

The complete circuit was designed, except the reference voltages required for for example the current sources. The only component that is not very robust in terms of process variations is the



(a) Capacitor voltage

(b) MOCD output stage differential input voltage

Figure 5.37: 25 run Monte Carlo mismatch simulation for the integrator

current splitter (MOCD). This component needs a redesign in order to have an accurate system.

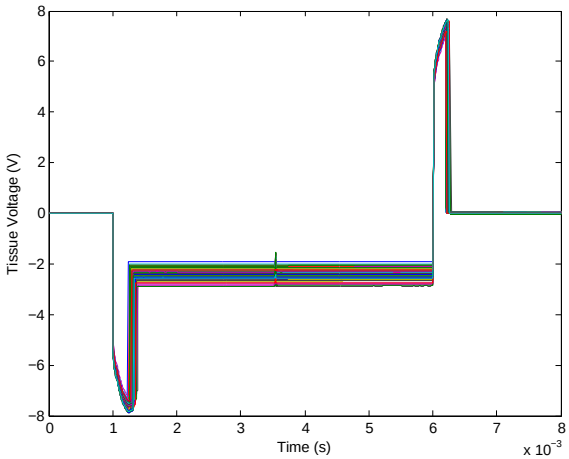


Figure 5.38: 64 run Monte Carlo simulation of the stimulator with ideal current splitter

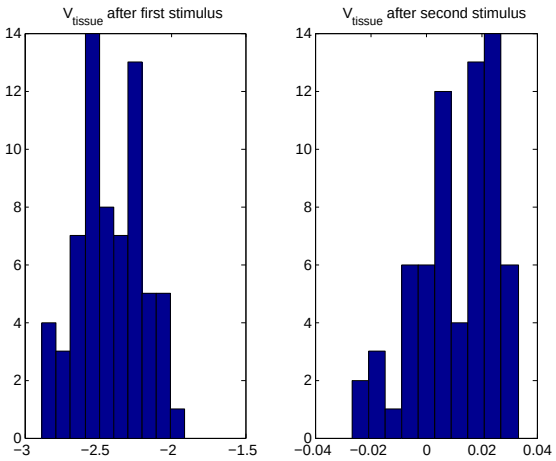


Figure 5.39: The tissue voltage at two different time instances during a 64 run Monte Carlo simulation with ideal current splitter

Conclusions and recommendations

In this chapter the results from the project are summarized in the conclusions. After the conclusions an overview of the scientific contributions made during this project is given. Subsequently in the next section a series of recommendations is made for further research. These recommendations include not only possible improvements of the design of the output stage, but also important aspects on the design of the digital part.

Conclusions

Functional electrical stimulation is an effective tool for the treatment of various diseases and has the potential of becoming applicable for a wide variety of diseases originating in the brain. Current stimulators have two major drawbacks. First of all the freedom in waveform shapes is very limited. This results in a decreased effectiveness of the stimulation and a limited immunity against tissue habituation. When the tissue is stimulated with the same stimulation pattern for a long time, the brain will habituate in order to ignore the stimulus. Therefore more flexibility is required for the stimulation waveform.

The second of the main problems is the limitted implantability of current stimulators. They are too bulky to be implanted in the head, which leads to long subcutaneous wires, yielding an increased risc of wire failure or medical complications. In order to minimize the size, the power consumption should be kept as small as possible in order to make the battery as small as possible.

Neural cells communicate using action potentials: the cell membrane voltage changes due to a change in the ion fluxes through its membrane. It is possible to evoke these potentials in an artificial way using functional electrical stimulation. Electrodes are implanted close to the cells and generate a particular potential, yielding a change in the outer cell membrane potential. This potential changes the memrane voltage and when this change is large enough an action potential is either generated or blocked (depending on the sign of the voltage change).

The interface between the electrode and the tissue can electrically be modeled using a combination of a constant phase impedance and a highly non linear resistor. It is shown that from an electrical point of view the error made by linearizing this model using a capacitor and resistor is neglectable. It can now be seen that elevating the tissue potential up to a certain level essentially means injecting a particular amount of *charge* in the tissue. Therefore it can be concluded that the important quantity for stimulation from a physical point of view is charge.

Charge is important for another reason as well. When large amounts of charge are injected into the tissue, electrolysis will occur, which will damage the neural cells. To prevent electrolysis at the electrode interface, charge built-up should be prevented. Electrolysis will damage the tissue and therefore it is important that every charge injection is followed by a negative pulse with the same charge. This means the charge of both pulses should be matched very well to prevent charge mismatch.

First a system level description is given for a complete stimulator system. The most important analog blocks include the communication block with the outside world, the voltage regulator for the power supply and the output stage, responsible for generating the stimulation signal. All these blocks are controlled by a digital processor. To significantly improve the functionality a feedback loop can be added. This loop records the brain activity and based on this activity the stimulation

program is generated. This feedback loop includes both analog circuitry (recording and amplifying the neural signal) and probably digital or analog processing of the signal.

Subsequently the focus is put on the design of the output stage responsible for the generation of the stimulation signal. To minimize power consumption the system was chosen to use only positive power supplies, corresponding to a system using only one battery. Furthermore the system was chosen to be voltage based, since this type of system was shown to have the highest power efficiency. Most existing systems use a current based stimulation in order to have easy control over the charge injected. This however comes at the price of a significant power efficiency reduction (accurate current sources are hard to implement). Since the current based approach is not a fundemental requirement the more power efficient voltage based approach was chosen.

To keep track of the charge injected, the tissue current is monitored using a feedback loop. It was shown that an indirect current feedback loop in which a fraction of the current is copied to the feedback network yields the most efficient implementation. This current is subsequently integrated to obtain the charge injected in the tissue. In this way it is possible to inject any arbritary waveform into the tissue, while still keeping track of the charge injected. Because of the architecture chosen a voltage feedback loop is required as well to control the tissue voltage.

Clinical applications show a very high spread in stimulation parameters among patients. The injected charge has a very high dynamic range, in the order of 4 decades of magnitude. To obtain an integrator which is able to accurately cover such a dynamic range, two systems are designed: the current is first scaled using a MOCD and subsequently the integrator converts the output signal to a periodic signal. To obtain this conversion in a power efficient way a new type of Schmitt trigger is proposed.

The complete system was designed to be implemented in a simulator using the AMIS 0.35μ I3T80 high voltage technology. Two power supplies were used: 3 V for the low voltage circuitry and 15 V for the high voltage part. A digital part controlling the system was implemented as well. The feasability of the system was proven using a series of simulations. Charge mismatch was in the order of 1% and can be improved to 0.1% if the design of the MOCD is either improved or omitted and the interpulse delay is minimized.

The quiescent power consumption of the system is smaller than $15\,\mu$W. The power efficiency is very dependent on the waveform shape, to what degree the high voltage supply will be adjustable and how exactly the circuit is to be controlled digitally.

The system is proven to be very versatile by showing endless possibilities for the waveform adjustability. The system is shown to be working for tonic shapes (sinusoids, block shaped), various burst stimulation shapes, symmetric stimulation and asymmetric stimulation.

Furthermore the system is shown to be very robust. It can handle a wide variety of resistance and capacitance values of the tissue impedance. Furthermore it is shown to be working for all process corners as well as process mismatches. Finally the system is also able to detect failures in the electrodes, since the tissue current can be limited using two independent mechanisms.

Summary of contributions

The following scientific contributions are made in this thesis:

- *New stimulator architecture*
  A fundamentally new stimulator output stage architecture is provided, consisting of voltage based stimulation with indirect current feedback. The architecture is based on a thorough understanding of the physical principles underlying functional electrical stimulation of neural cells. This architecture has the following advantages:
  - Power efficient stimulation (quiscent power among the lowest reported: $15\,\mu$W)
  - Very high waveform adjustability (any waveform possible)
  - Safe stimulation is assured by an accurate charge cancellation scheme (0.1% mismtach).

  Simulations have confirmed the feasability of this approach.

- *Very high dynamic range current integrator*
  A current integrator is designed which can handle a very high dynamic range (several decades of magnitude). The input signal is converted to a periodic signal using a Schmitt trigger. For the Schmitt trigger a new design is proposed to allow a low static power consumption (no bias sources), while it is still fast and accurate enough for this particular application. Its design is based on a threshold compensated invertor.

- *Very robust operation*
  It is made clear that the absolute value of the stimulation parameters does not need to be accurate. Therefore only efforts are made to make the relative values between positive and negative pulses accurate to assure charge cancellation. It was shown the system is very robust over all process corners and mismatches. Furthermore the system is also working for a wide range of tissue variations ($1\,\mathrm{k\Omega} < R_{tissue} < 100\,\mathrm{k\Omega}$ and $10\,\mathrm{nF} < C_{tissue} < 100\,\mu\mathrm{F}$).

- *Only single ended supply voltages used*
  The system is designed in such a way that no negative voltage supply is required. The system is able to inject and handle both positive and negative pulses from a single ended supply. This makes the system suitable for operation using a single battery.

- *Non linear tissue model linearized*
  The current response of the non linear tissue model is investigated for a voltage step input. In contrast to previous publications, the non linearity of the model was accounted for in the complete analysis. It was found that the current respons can be described with only minor deviations using a linear model as well. This greatly simplifies the incorporation of the tissue model in a circuit simulator.

Recommendations

Based on the results found in this project a couple of recommendations can be made for further research. Some recommendations are specific for the output stage design, while others are more general recommendations for the complete stimulator system.

System level

- *Medium Voltage Technology*
  While working on this project a couple of new technologies have come available through the Europractice program. Two of them include the I3T25 and I3T50 technologies. They are equivalent to the I3T80 technology used in this project, however the High Voltage transistors can now handle voltages up to 25 V and 40 V respectively. Since the 80 V was slightly overkill for the biomedical application, these medium voltages might suit the application better. Most likely these transistors are much smaller, yielding a smaller area for the complete chip. The low voltage transistors are most likely equivalent (it's based on the same C035U technology), which means all the low voltage circuit design does not need to be repeated.

  Therefore the use of this medium voltage technologies instead of the current high voltage technology should definitely be considered.

- *Heat generation*
  In the design of the system no special attention has been paid to heat generation. Any power burnt in the stimulator will lead to heat generation. The brain is very sensitive to temperature variations and therefore the heat dissipation in the stimulator should be as limited as possible.

  Since static power consumption is fairly low, no big problems are to be expected here. However, when the tissue voltage is 50% of the supply voltage the power dissipation in the stimulator is shown to be maximum and this situation needs special attention. One way to solve this is to make the power supply variable, as will be discussed in another recommendation.

- *ESD protection*
  This aspect was briefly touched upon in the discussion of the technology choice. Because of the large number of contacts to the outside world (using electrodes) protection against ElectroStatic Discharge is an important requirement for the system. In the current design no attention was paid to ESD protection, but the technology provides libraries which are especially designed to protect the circuit against ESD. Therefore this is an additional point that should be investigated.

- *Make the power supply variable*
  As was discussed in the report already, the power efficiency depends largely on the ratio between the power supply voltage and the stimulation voltage. The smaller the stimulation voltage compared to the supply voltage, the lower the efficiency.

  In order to keep the efficiency high, the supply voltage can be chosen to be adjusted to the stimulation voltage (for example to tune the high voltage supply to the highest stimulation voltage value during the stimulation cycle).

  In order to generate this variable voltage supply probably some analog circuits need to be designed, which are controlled by the digital part. This part is also generating the stimulation cycle and therefore knows the maximum stimulation voltage.

Analog part of the output stage

- *Investigate the intra-die V_t mismatches*
  In this report the intra die threshold voltage mismatches between transistors were not considered. The threshold voltage mismatches become important especially for the driver block

as mentioned in the report, but also for example for the MOCD. Although the monte carlo simulations have shown that (apart from the MOCD output stage) the charge cancellation is working good enough, it might increase the accuracy of the circuit even more if circuit techniques are used to fight the intra-die threshold voltage mismatch.

- *Include more control over the Tissue current for safety*
  In the current circuit the current injected in the tissue is controlled only up to a certain degree. By changing the tissue voltage, the tissue current is changed as well. Variations in tissue impedance however can significantly change the current injected, while this is not 'noticed'. Also short circuit or open circuit conditions at the electrodes are not yet monitored by the circuit.

  An open circuit means no current will flow into the tissue. This will also mean the charge threshold is not reached. This can easily be detected by the digital circuitry which is controlling the output stage. This circuitry can signal back the faulty situation towards the user.

  For a short circuit condition the situation is more dangerous. When no precautions are taken the current injected might become very high. This can damage the tissue and/or the circuitry. Therefore it is desired to limit the output current. This can be quite easily done in two ways. First of all the gate voltage of the driver transistors should be given a lower limit. This will not only make sure the maximum V_{gs} of these transistors is not exceeded, it will also limit the input current. This will however not yet signal the faulty condition.

  A second way to monitor the current is to monitor the output of the integrator. In the digital circuitry the output frequency of the schmitt trigger can be monitored. When this frequency becomes too high for a certain MOCD setting the tissue current is too high. This can be detected and signaled back to the user. In this way a double protection can be included against the potentially dangerous short circuit condition of the electrodes.

- *Use a better MOCD implementation to decrease charge mismatch*
  As seen in the last chapter of the report, the largest mismatch error results from the discharge of the tissue during the interpulse delay. Besides this error which can only be improved by improving the off impedance of the switches, the most significant source of errors results from the MOCD.

  One way to improve the MOCD would be by increasing its accuracy and robustness. The focus should then be on the output stage, which is a source for deviations due to process mismatch. In order to improve this, probably a complete redesign of this component is required. Yet another option might be to opt for a different approach than an MOCD, for example another type of current attenuator.

  However it should also be considered to eliminate the MOCD block completely in the circuit. This means that the output of the driver block is connected directly to the integrator. This would mean the range at the output of the schmitt trigger is much bigger then when using an MOCD. This mainly puts higher requirements on the digital part of the charge cancellation circuit: the counter must count up to a much broader range. This might however not be a very big problem.

  First of all in practice high values for charge injection are used not very often. Usually relatively low stimulation parameters can be used to obtain stimulation. This means the counter does not need to count up to very high values in most cases.

  Furthermore it might be possible to ignore the least significant bits if the counter is required to count up to a high value. In this way the rest of the digital circuit can still operate using a small number of bits (yielding smaller area an power consumption), while the counter can still count up to higher values. Of course ignoring the least significant bits reduces the resolution of the charge threshold. However this might not be a very big problem for these high charge values.

- *Increase the accuracy even more*
  When it should be required to increase the efficiency of the circuit even more after the current divider has been implemented, the focus should be on the discharge of the tissue during the interpulse delay. It has become clear that this effect can be responsible for the largest charge mismatches if the interpulse delay is high.

  Because of the highly non linear nature of the tissue it is not possible to say anything about the amount of leakage by just monitoring the voltage over the tissue. Therefore the only way to compensate for this would be to measure the current flowing from the tissue during the interpulse delay in a direct way. It has been seen in this report that measuring the current from the tissue in a direct way yields a complicated implementation. Since however this is the only way to get an accurate measure of the charge leaking away, this implementation should be considered if a higher accuracy is required.

Digital part of the output stage

- *Optimize the digital part*
  The digital part of the charge cancellation circuit has not yet been optimized. Mainly for the counter a lot of better implementations might exist. In order to for example minimize the power consumption a different counting scheme might be used. An option might be to use so called 'gray coding' in which the bit sequence changes with only one bit each next cycle. This minimizes power consumption, since each bit change is associated with additional power consumption. Each change yields the charging or discharging of certain nodes in the circuit.

  Other optimalisations might include a more efficient reset scheme for the counter. In the scheme used in this report an additional clock signal is used to reset the counter. This clock signal uses power as well.

- *Implement different stimulation strategies*
  In the current report the digital electronics were assumed to be working as follows: a voltage waveform was constructed and a certain charge threshold was selected on beforehand. When the charge threshold was reached, stimulation was stopped and a counterpulse was applied to exactly cancel the charge injected.

  It might be that in practice the required charge threshold is not yet known very well. Another possibility is that the physicians simply want to inject a certain waveform (with a certain length) without bothering about the total amount of charge. In this case a different stimulation strategy can be used. A certain voltage waveform is constructed with a certain length. While injecting this pulse, the corresponding charge is calculated by counting the periods from the Schmitt trigger and this number is stored. Subsequently the injected pulse is canceled by injecting a counter pulse with the same number of periods.

  In this way the charge is omitted as a parameter from the stimulation strategy. Although this is not in correspondence with the underlying physical principles, it might be a helpful operation mode for physicians.

- *Increase the power efficiency of stimulation*
  The control circuitry needs to be adjusted a bit to achieve maximum power efficiency for stimulation. It was seen the circuit has a fairly high power consumption when the charge threshold has been reached, but the stimulation source is not equal to 0. In this case a static current will flow through the voltage feedback network. Therefore from a power consumption perspective the stimulation source should be made 0 as soon as the charge threshold has been reached.

  This should be relatively easy to implement in the digital part of the circuit. This part also registers when a charge threshold is reached, which means it is also able to make the stimulation source 0.

Recommendations for the user

- *Point out how stimulation can be achieved most efficiently*
  The goal is to make the circuit as efficient and accurate as possible. A lot of different measures are taken using circuit techniques to meet these goals as close as possible. However it should be noted that also the end user of the device should be made aware of how this device can be operated as efficient and accurate as possible.

  First of all the accuracy increases when the interpulse delay is as short as possible. It was seen that during this delay the tissue slightly discharges. Since this discharge is not measured by the integrator, it cannot be compensated during the charge cancellation pulse. Therefore in order to get an as accurate result as possible, the leakage should be minimized.

  The only way to do this is to minimize the interpulse delay. When a certain application has a need for a relatively large interpulse delay, the charge mismatch might be reduced by shortening the tissue after stimulation a bit longer. In this way the tissue is given some more time to fully discharge itself and to eliminate the remaining charge.

  A second aspect that needs to be kept in mind by the end user is that in order to have a maximum power efficiency, the stimulation waveform should be as close to the power supply as possible. The circuit is dissipating the most power when the stimulation waveform is chosen to be half of the power supply.

  As pointed out before the efficiency might be increase by making the power supply adjustable. Still it needs to be known by the physician that a waveform in which the value is chosen to be half of the maximum value for a long time, yields a high power dissipation in the circuit. This means the battery is not used in an efficient way and heat will be generated in the circuit.

Appendix A

Derivations of equations

A.1 The Nernst potential equation

The ion flux resulting from an electric field depends on the magnitude of the field, the concentrations of ions and the mobility of the ions:

$$J_e = -\mu \frac{z}{|z|} c \nabla \Phi \tag{A.1}$$

Here J_e is the ionic flux due to the electric field [mol/cm^2 s], μ is the mobility [cm^2/V s], z is the valence of the ion, c is the ionic concentration [mol/cm^3] and $\nabla\Phi = -E$ is the electric potential gradient [V/m].

The ion flux resulting from the concentration gradient is due to diffusion and is described by Fick's law:

$$J_d = -D \nabla \Phi \tag{A.2}$$

Here J_d is the ionic flux due to diffusion [mol/cm^2 s] and D is the diffusion constant [cm^2/s]. The Diffusion constant is related to the mobility by the following equation (foudn by Nernst and Einstein):

$$D = \frac{\mu R T}{|z| F} \tag{A.3}$$

The total ion flux is then found to be the sum of those two fluxes. By using equations A.1, A.2 and A.3 the total ion flux is found:

$$J = J_d + J_e = -D \left(\nabla c + \frac{czF}{RT} \nabla \Phi \right) \tag{A.4}$$

This equation is called the Nernst-Planck equation in which R is the gas constant [8.314 J/mol K], T is the temperature [K] and F is Faraday's constant [$9.6 \cdot 1\,0^4$ C/mol]. In equilibrium, the net current is zero. By applying this condition to equation A.4 and considering the membrane voltage as a one dimensional quantity (along the normal of the membrane), the equation becomes an ordinary differential equation. Solving the differential equation by integrating over the membrane (this operation is omitted here and can be found in [48]), one can find for the equilibrium voltage (also called the Nernst voltage):

$$V = \frac{RT}{zF} \ln \frac{c_i}{c_o} \tag{A.5}$$

Here V is the Nernst voltage [V], c_i is the intracellular concentration of the ion and c_o is the extracellular concentration of the ion. The Nerst Voltage sets the membrane voltage for one particular type of ion sets the voltage for which no ions of that type flow through the membrane.

A.2 The Goldman-Hodgkin-Katz equation

Starting from equation A.4, which describes the total membrane ion flux for one particular type of ion, some assumptions are made. First of all the membrane is again assumed to be one dimensional, leading to $\nabla\Phi = d\Phi/dx$ and $\nabla c = dc/dx$:

$$J_k = -D_k \left(\frac{dc_k}{dx} + \frac{c_k z_k F}{RT} \frac{d\Phi}{dx} \right) \tag{A.6}$$

Note that all parameters are now denoted with the k-subscript, indicating the k^{th} ion type (in general $k = 1..3$ for potassium, sodium and chloride ions). If now furhtermore i t is assumed the electric field is constant over the membrane ($d\Phi/dx = V_m/h$ with h is the membrane thickness), the equation becomes:

$$\frac{dc_k}{dx} = -\frac{J_k}{D_k} - \frac{V_m z_k F}{RTh} c_k \tag{A.7}$$

This differential equation can be solved by integrating over the membrane ($x = 0..h$) and realising steady state conditions ($J_k(x)$ is constant) the following equation can be obtained:

$$J_k = -\frac{D_k V_m z_k F}{RTh} \frac{c_k^h - c_k^0 \exp\left(-\frac{V_m z_k F}{RT}\right)}{1 - \exp\left(-\frac{V_m z_k F}{RT}\right)} \tag{A.8}$$

Here c_k^h and c_k^0 correspond to the concentration of the k^{th} ion at $x = h$ and $x = 0$ subsequently. These quantities can be described more convenient, by realizing these values correspond exactly to the intercellular and extracellular ionic centrentrations: $c_k^h = \beta_k c_i$ and $c_k^0 = \beta_k c_o$. Here β_k is the partition coefficient, describing the ratio between the concentration of the x^{th} ion and the total ion concentration. Furthermore the permeability of the membrane is defined as:

$$P_k = \frac{D_k \beta_k}{h} \tag{A.9}$$

Substituting these notation changes exitin equation A.8 yields:

$$J_k = -\frac{P_k V_m z_k^2 F^2}{RT} \frac{c_i - c_0 \exp\left(-\frac{V_m z_k F}{RT}\right)}{1 - \exp\left(-\frac{V_m z_k F}{RT}\right)} \tag{A.10}$$

This equation describes the membrane current for one particular type of ion. This equation can be substituted in $J_{tot} = J_K + J_{Na} + J_{Cl} = 0$ and by incorporating the correct valences of the ions, the following equation results:Ach at j

$$-P_K \frac{c_{i,K} - c_{o,K} \exp\left(\frac{-V_m F}{RT}\right)}{1 - \exp\left(\frac{-V_m F}{RT}\right)} - P_{Na} \frac{c_{i,Na} - c_{o,Na} \exp\left(\frac{-V_m F}{RT}\right)}{1 - \exp\left(\frac{-V_m F}{RT}\right)} - P_{Cl} \frac{c_{i,Cl} - c_{o,Cl} \exp\left(\frac{-V_m F}{RT}\right)}{1 - \exp\left(\frac{-V_m F}{RT}\right)} = 0 \tag{A.11}$$

This equation can be rearranged and solved for V_m, yielding the Goldman-Hodgkin-Katz equation:

$$V_m = -\frac{RT}{F} \ln\left(\frac{P_K c_{i,K} + P_{Na} c_{i,Na} + P_{Cl} c_{o,Cl}}{P_K c_{o,K} + P_{Na} c_{o,Na} + P_{Cl} c_{i,Cl}} \right) \tag{A.12}$$

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