Design and Development of Active Baseband Load-pull
MSc Thesis (ELCA)

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Design and Development of Active Baseband Load-pull MSc Thesis (ELCA)

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Abstract

3G and 4G modulation standards have non constant amplitude modulation to suffice the needs of high bandwidth. These signals show high peak to average power ratio increasing the dynamic range of the RF signals. This translates into very stringent linearity requirements for the power amplifiers at the RF front end. Linearization techniques are employed to linearize the power amplifiers instead of backing off from peak output power. Memory effects, which are the amplitude and phase deviations of intermodulation products caused by tone spacing, may limit the maximum achievable cancellation performance of the pre-distortion method. Studies have shown that, the baseband impedance is the major contributor of these memory effects. In order to understand the behavior of these memory effects over a bandwidth, it becomes necessary to have the capability to load-pull the baseband impedance of a system. Systems with such a capability to load-pull the baseband, are not commercially available yet. The objective of this thesis was to design and develop such a baseband load-pull system and integrate it into an existing active harmonic load-pull system.

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Last but not the least, I dedicate this thesis to my family, to my mom, my dad, my granny, my brother Deepu and my girlfriend Arnica.

Ajay Kumar Manjanna
Delft, the Netherlands
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Chapter 1

Introduction

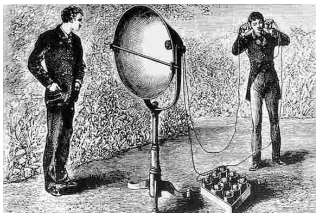
"From the top floor of this building was sent on June 3, 1880 over a beam of light to 1325 'L' street the first wireless telephone message in the history of the world. The apparatus used in sending the message was the photophone invented by Alexander Graham Bell, inventor of the telephone" [1]

June 3, 1880 was the day when Alexander Graham Bell and Charles Sumner Tainter succeeded in communicating over a distance of 213 meters using plain sunlight as their modulated signal using a device called *photophone*, Figure 1.1(a). This marked the first wireless telephone communication ever made by man. In 1899 Nikola Tesla setup a tower on Long island 187 feet high, having a spherical terminal of about 68 feet in diameter, Figure 1.1(b), to demonstrate the radio transmission through air. These attempts focussed on achieving wireless communication over greater distances but not on optimizing the performance, cost and efficiency of such systems.

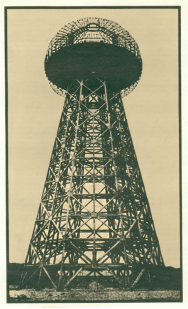
The desire to communicate anytime and anyplace has always been an important technology driver. Since the idea was conceived, the mobile phone from being a luxury has become a necessity, changing its status in less than 25 years. Mobile phones are no longer used only to make and receive calls, instead, they are also used as wireless TV, high speed wireless internet browsers, hi-definition multimedia and gaming stations. For this reason, large bandwidth, high efficiency (e.g. long battery life) and low cost have become crucial requirements for today's handsets.

Figure 1.2 shows a simplified block diagram of a transceiver system which performs both the receiving and transmitting function of a wireless (mobile) unit. In the transmitter chain, the application specific signals are processed and delivered to the antenna to be broadcasted to the nearest base station. In order to overcome the environment losses the signal delivered

[1] Plaque on the exterior of the Franklin School at 13th & K Streets NW in Washington, D.C.



(a) Photophone receiver and headset [1]



(b) Tesla tower in Long island (1901 - 1917) [2]

Figure 1.1: Photographs showing Graham Bell with photophone and Tesla tower in Long island.

to the antenna has to be large enough to compensate for the path losses. These high level signals are delivered by power amplifiers (PA) which represent a critical[2] building block of transmitter chain.

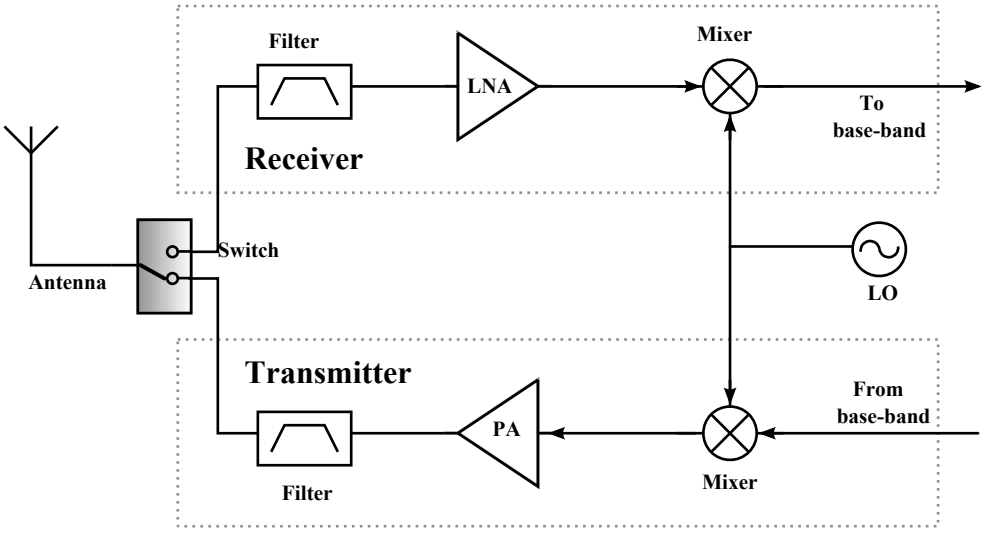


Figure 1.2: Transceiver chain.

In order to cater to the need of high data rates and to accommodate ever increasing mobile subscribers which seek the need of large bandwidths, the industry has developed and implemented third generation (3G) wireless networks. Fourth generation (4G) networks are

[2]Critical in order to ensure optimal system level performances in terms of linearity and power efficiency.

under development to accommodate higher data rates and bandwidth. Most of the 3G and 4G standards utilize some sort of Code Division Multiple Access (CDMA) format, such as Wide-band CDMA (WCDMA), Orthogonal Frequency Division Multiplexing (OFDM) or Time Division Synchronous CDMA (TD-SCDMA), flash OFDM, etc. Unlike GSM, a 2G standard, these new modulation standards have non constant amplitude modulation with peak to average power ratios of 6dB - 12dB, increasing the dynamic range of the RF signals tremendously. This translates into very stringent linearity requirements of the RF front end that are getting more and more difficult to meet from the manufacturer. Moreover, the slow progress on the battery technology compared to RF technology calls for highly efficient power amplifiers. All these factors lead to more complex PA design challenges.

The linearity and efficiency are more critical in base stations. Base station power amplifiers have much more stringent requirements on efficiency and linearity compared to handset PAs. Earlier, the amplifiers were typically designed for 30-60W and for two carriers, but recent deployments require three or even four carriers with up to 60 MHz bandwidth. The resulting signals from the above mentioned standards have very high Peak-to-Average Ratio (PAR[3]) and are wide-band. As a result, these multiple carrier power amplifiers have higher linearity and bandwidth requirements, and the tradeoff between power-added efficiency and linearity is a major challenge. The PAR for a typical 3G waveform transmitted by a base station power amplifier can be as high as 12 dB. As a result, the amplifiers are typically operated at an average power backed-off from the peak output power by at least 12dB [3]. The resulting efficiency, which depends on the class of amplifier operation as well as the transistor, can be quite poor. Thus it becomes more important in the case of base station power amplifiers, that high linearity and high efficiency co-exists.

In order to meet these challenges, not only advanced design techniques but also advanced testing techniques are crucial in understanding the circuit and device level characteristics. Sophisticated measurement tools and procedures enable fast time to market and avoid costly redesign process.

[3]is defined as the ratio of the peak amplitude of the waveform to its RMS value.

1.1 Characterization

The final transmitted RF signal is expected to meet some minimum criteria in order to be discernible at the receiver. Owing to the need of higher data rates, multi carrier systems have emerged over recent years. Due to high peak to average ratio (PAR) exhibited by these signals, power amplifiers will have to cope with high power levels and may be driven into the unwanted nonlinear operating region. The effect manifests itself through a severe bit-error-rate (BER[4]) degradation of the system [4]. S. Merchan in [5] shows that, the symbol error rate performance degrades as a function of clipping and nonlinear distortions in 16-QAM/OFDM systems. This is one of the reasons to have a highly linear power amplifier at the output stage when transmitting an amplitude modulated signal.

Nonlinear behavior of a system is detrimental to the signals that pass through it. Such is the case with distortion in a RF power amplifier. So, it becomes very important that these nonlinear effects on various input signals are measured, characterized and understood. A nonlinear behavior can manifest itself as all or one of the following:

- Distortion effects
  - Gain Compression
  - Phase Distortion
  - Harmonic Distortion
  - Intermodulation Distortion
- In/Out of band non-linear characteristics
  - Error Vector Magnitude
  - Adjacent Channel Interference

The following section reviews most used figure of merits (FoMs) to characterize PAs.

1.1.1 Figure of merits (FoMs)

From power series (see below) analysis it can be shown that the signal gain in microwave circuits is dependent on the input signal amplitude. Generally, the signal gain decreases with increasing amplitude or input signal power level. So, it becomes important to characterize the gain compression characteristics of microwave components. Figure 1.3 will be used to show the following FoMs graphically. In this figure, the output power is plotted against

[4] is the percentage of bits that have errors relative to the total number of bits received in a transmission.

input power in log-log scale. The linear/small-signal gain exhibit a 1:1 slope, whereas, n^{th} harmonics or intermodulation[5] terms will have an n:1 slope.

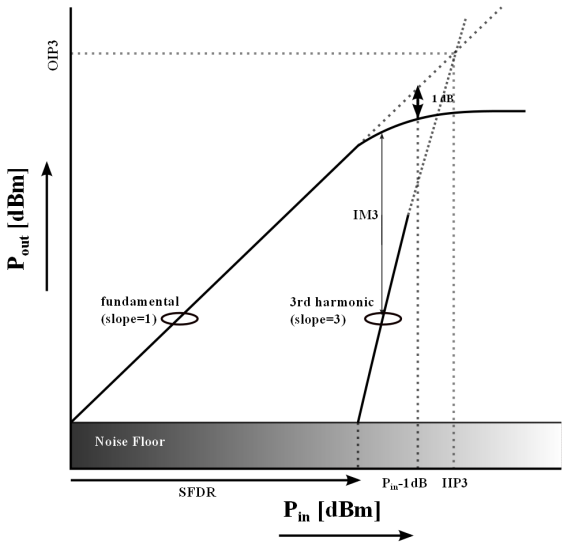


Figure 1.3: Pout Vs Pin showing IIP3, OIP3, SFDR & P-1dB points.

The relationship between an input signal S_{in} and S_{out} of a memoryless non-linear system can be expressed by a power series as below:

$$S_{out} = a_1 S_{in} + a_2 S_{in}^2 + a_3 S_{in}^3 + ... \tag{1.1}$$

Substituting $S_{in} = A.cos(\omega t)$ in Equation 1.1, yields :

$$S_{out} = \overbrace{\frac{1}{2}a_2A^2}^{\text{DC}} + \overbrace{\left(a_1A + \frac{3}{4}a_3A^3\right)cos(\omega t)}^{\text{Fundamental}} + \overbrace{\frac{1}{2}a_2A^2cos(2\omega t)}^{2^{nd}\ harmonic} + \overbrace{\frac{1}{4}a_3A^3cos(3\omega t)}^{3^{rd}\ harmonic} + ... \tag{1.2}$$

Gain 1dB compression point (P_{1dB})

From the Equation 1.2, it is seen that the amplitude of the fundamental signal consists of a linear and a third degree terms. If the system is operating at relatively large input amplitude, term $\left(\frac{3}{4}a_3A^3\right)$ cannot be ignored. Depending on the sign of this term the

[5]Intermodulation Products occur at the output of a non-linear system when the input signal to such a system consists of multiple frequencies.

system can experience gain expansion or gain compression. For a two tone input signal, the amplitude of the fundamental signal is given by $\left(a_1 A + \frac{9}{4} a_3 A^3\right)$.

An important FoM to measure linearity of a system is called *1-dB compression point* P_{1dB}. P_{1dB} compression point is defined as the input or output power level where the gain drops by 1dB in respect to its small signal value.

Third Order Intercept point (TOI)

Input (output) TOI is defined as the input (output) power level where the extrapolated undesired third-order intermodulation response (IM3) intersects the desired first-order response, as shown in Figure 1.3. The relation between IM3 products (Δ IM3) output third order intercept point is given by [6]:

$$P_{OIP3} = P_{out} + \frac{\Delta IM3}{2} \tag{1.3}$$

Input third order intercept (IIP3) can be calculated by subtracting the power gain (G_P) of the device from P_{OIP3}

$$P_{IIP3} = P_{OIP3} - G_P \tag{1.4}$$

Spurious Free Dynamic Range (SFDR)

SFDR is defined as the difference between the power levels at which the input power level is equal to the noise floor and the input power level at which the IM3 products start to rise above the noise floor.

$$SFDR = \frac{2P_{IIP3} + NF}{3} - SNR_{min} \tag{1.5}$$

where NF is the noise factor and SNR is signal to noise ratio.

Power Added Efficiency (PAE)

PAE is a metric used to define the efficiency of a Power Amplifier and is defined as below.

$$PAE = \frac{P_{RFout} - P_{RFin}}{P_{DC}} \tag{1.6}$$

where $P_{RFout}, P_{RFin}, P_{DC}$ are output RF power, input RF power and input DC power respectively.

1.1.2 Load-pull technique

Advanced design testing techniques are instrumental in circuit performance enhancement as they allow rapid analysis and interpretation of design tradeoffs. Advanced testing capability can form a bridge between improvement of technology and new circuit topologies, so that optimization can be done at both transistor and circuit level to tailor for optimum overall RF circuit performance [7].

The power amplifier is the single source of most power consumption in a radio. With modern modulation techniques, the input to the power amplifier is a non constant envelope signal. This demands the power amplifier to be highly linear[6]. In classical PA design an inevitable tradeoff exists between linearity and efficiency. Significant effort is devoted in developing high performance RF transistors and circuits to improve power amplifier efficiency. In this case, it is necessary to determine the source and load impedance for best tradeoff in overall performance. Such a measurement where source/load impedance is varied to characterize the large signal behavior of the RF device (under test) is called *"load-pull measurement"*.

Load-pull as a design tool is based on measuring the performance of a transistor at various source and/or load impedances and drawing contours of measured quantities, in the gamma-domain; measurements at various bias and frequency conditions may also be done. Several parameters can be superimposed over each other on a Smith chart and tradeoffs in performance can be determined. From this analysis, optimal source and load impedances can be determined [8].

The easiest way to achieve the variable impedance is to use a mechanical tuner to set the impedance at source and load. This is called passive load-pull. This method suffers from unavoidable losses in the measurement setup because of which, the maximum achievable reflection coefficient is much lower than 1. Also, it is difficult to design a passive system to control harmonic impedances along with the fundamental impedance. As a method to overcome these limitations, in the late seventies, Takayama introduced the concept of active load-pull measurement technique [9]. Since then there have been continuous attempts to perfect the art of load-pulling. The concept is based on simple definition of reflection coefficient.

$$\Gamma = \frac{a_2}{b_2} \tag{1.7}$$

[6] A constant envelope can be amplified using a device operating in compression region without increasing significant amount of distortion. But, for a non-constant envelope signal the PA has to operate in linear region to avoid distorted signal at the output.

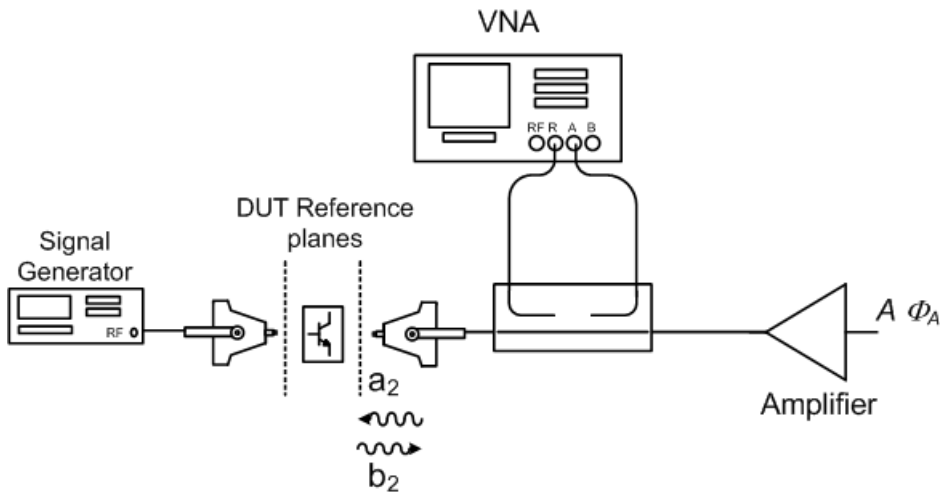


Figure 1.4: Active load-pull setup showing signal generator, DUT and open loop amplifier to set the fundamental load impedance.

where $a_2(=A.e^{(-j\phi_A)})$ and $b_2(=B.e^{(-j\phi_B)})$ are the reflected and incident waves at the output of the DUT when looking into the load, respectively. By controlling the amplitude (A) and phase (ϕ_A) of the a_2 wave, the Γ at the output of the DUT can be controlled. This can be achieved by injecting a signal of known amplitude and phase into the device as shown in Figure 1.4. The process can be iterated changing the amplitude and phase of the injected signal to converge on the desired reflection coefficient.

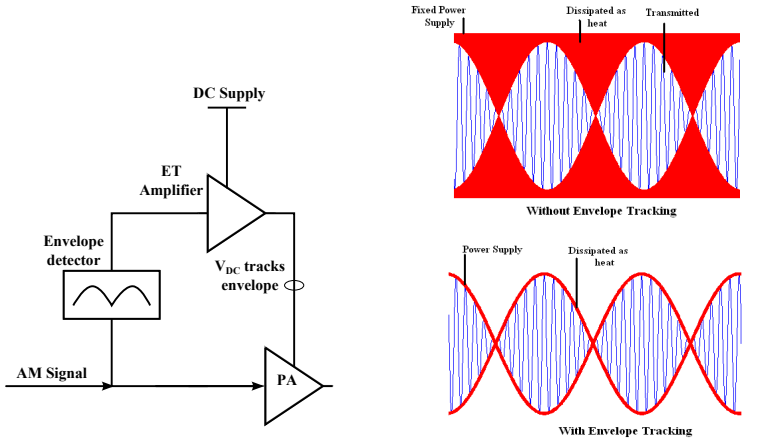
1.2 Efficiency enhanced power amplifiers

The efficiency of classical power amplifiers is dependent upon the *crest factor*[7] of the signal being amplified. The advent of complex modulation techniques have made a power amplifier designed in conventional way to be inefficient. This is because, a conventional power amplifier design gives maximum efficiency at a single power level, usually near maximum rated power for the device, whereas, the PAR in an amplitude modulated signal is about 6dB-12dB. As Cripps mentions [10], effective *efficiency enhancement* techniques are available since many years. Literature [10] mentions three classical techniques; the Doherty Amplifier, the Outphasing Amplifier initially proposed by Chireix, and the Envelope Elimination and Restoration (EER) technique demonstrated by Kahn. In this section we will look into one of the recent derivatives, viz. *Envelope Tracking (ET)* Amplifier architecture.

[7] same as PAR or PAPR.

1.2.1 Envelope tracking (ET) power amplifier

The principle of ET has been known for many years [11]. In a nutshell, in the ET power amplifier architecture, the bias voltage supplied to the final RF stage power transistor is changed dynamically, synchronized with the RF signal passing through the device ensuring that the output device remains in most efficient operating region. Figure 1.5(a) shows the generalized ET power amplifier structure. The envelope from the incoming RF signal is extracted and is given as input to the ET amplifier which regulates the DC supply to the final RF stage according to the envelope signal. The supply voltage is reduced from its maximum value so that it tracks the envelope of the signal, and this reduces the energy dissipated as seen in Figure 1.5(b). This figure compares the signal at the output without and with ET, in the time domain.



(a) ET amplifier Architecture

(b) Waveforms showing power dissipated when constant DC supply is applied and when dynamic bias, i.e., ET is employed.

Figure 1.5: Envelope tracking amplifier.

ET architecture can be used with digital pre-distortion techniques to improve linearity of the PA along with the efficiency [12, 13]. Even though the concept of ET is more than 50 years old, implementing a power supply modulator capable of having the accuracy, bandwidth and noise specifications necessary for wide-band signals has been difficult until recent works in this field [12–17].

1.3 Memory effects

When considering an amplifier excited with two tone input signals, the IM3 terms (resultants due to nonlinear transfer function of the amplifier) are expected to be symmetric in amplitude and constant over tone spacing of the input signals. But, in reality the phase and amplitude of IM3 components vary with the tone spacing and the IM3 components tend to be asymmetric. Figure 1.6 shows these artifacts[8].

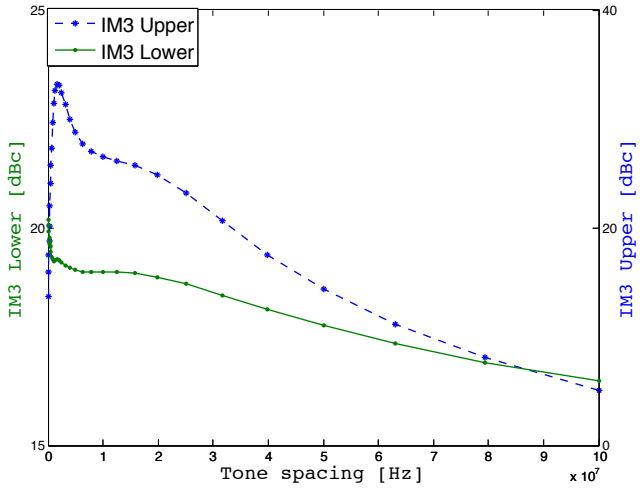


Figure 1.6: Simulation results showing behavior of IM3 tones as a function of tone spacing

Such modulation bandwidth limitations that are amplitude deviations of intermodulation (IM) responses caused by the tone difference of a two-tone signal are called ***Memory Effects***. Thus, memory effects can be defined as changes in the amplitude and phase of distortion components caused by changes in modulation/difference frequency. It is important to emphasize that the distortion itself is not a memory effect, but any non-constant distortion behavior at different tone-spacings can be regarded as one [18].

These effects are generally attributable to thermal, electrical and/or packaging effects. This behaviour in turn impacts overall linearity. It is observed that electrical memory introduced by the low-frequency baseband impedance represents a significant contributor to overall observed memory effects in high-power PA design as will be shown in the following section. This baseband impedance is associated with the power amplifier bias networks being frequency dependent [19].

[8] An experimental simulation was run where a NXP LDMOS (BLF66G22) model was excited with 2 tone signal with constant amplitude but varying tone space(from 100kHz to 100MHz). The device was operated at its full power rating.

Memory effects of lower magnitude with amplitude change (in IM3 tones with tone spacing) less than 0.5dB and phase rotation of $10^0 - 20^0$, are not detrimental to the amplifier performance [18]. They do not have a dramatic effect on the device's ACPR performance. However, its a different scenario when linearization technique is used to cancel the IM3 sidebands. Pre-distortion, for example, is a linearization method that produces signals of equal magnitude and opposite phase relative to distortion products. Since IM3 components rotate with changes in baseband frequency as opposed to pre-distortion signals which maintain a constant phase, it becomes immediately evident that the maximum achievable IM3 cancellation performance using this method gets limited. Also, many other linearization methods suffer from the same problem. As a result, memory effects render use of linearization ineffective for a number of applications [18].

1.3.1 Role of baseband impedance

This section analyzes the role of baseband impedance in causing memory effects. Detailed analysis of FET intermodulation dependence on baseband impedance has been made in [20]. Following text shows two tone analysis of a FET biased in saturation region.

Consider a circuit with common source FET biased in saturation region, with nonlinear gate-source capacitance controlled by gate v_g and drain current controlled by gate v_g and drain v_d voltage signals. These signals result in nonlinear currents through the drain and gate.

Assuming that the lower and upper input tones are at ω_1 and ω_2 respectively, the lower and upper third order IMD products will be at $(2\omega_1 - \omega_2)$ and $(2\omega_2 - \omega_1)$. The baseband frequencies at $\pm(\omega_2 - \omega_1)$. It is often the case that the baseband frequency is small compared to midband carrier frequency ω_c so that $\omega_c \approx \omega_1 \approx \omega_2 \approx (2\omega_2 - \omega_1) \approx (2\omega_1 - \omega_2)$. This approximation does not hold when the envelope frequency is not small. Based on this approximation the equations representing the lower and upper third order intermodulation levels can be given as [20]:

$$IM3_{Lower} = V_s^3 Z_o(\omega_c) r^2 r^* (c_0 Z_o(\omega_1 - \omega_2) + c_1 + c_2 Z_o(2\omega_c)) \tag{1.8}$$

$$IM3_{Upper} = V_s^3 Z_o(\omega_c) r^2 r^* (c_0 Z_o(\omega_2 - \omega_1) + c_1 + c_2 Z_o(2\omega_c)) \tag{1.9}$$

The term r is a pole due to gate-source capacitance. The asterisk * denotes a complex conjugate, which corresponds to negative frequencies. $Z_o(\omega)$ denotes the effective linear drain impedance.

If the expressions for lower (1.8) and upper (1.9) intermodulation products are observed carefully, the only difference is the presence of $Z_o(\omega_1 - \omega_2)$ in 1.8 and its conjugate $Z_o(\omega_2 - \omega_1)$ in 1.9. $Z_o(\omega_1 - \omega_2)$ is the only term in (1.8) that will change with the baseband frequency as it is determined by the baseband impedance at drain terminal. ***This significant result reasons the change in levels of intermodulation levels with the change in baseband frequency. Also, the imaginary part of*** $Z_o(\omega_1 - \omega_2)$ ***in (1.8) is in opposite sign as compared to its conjugate in (1.9). This results in asymmetry of the intermodulation terms.***

1.3.2 Observations

From the above discussion, the following observations can be made:

- Frequency dependent bias networks set the baseband impedance.
- IM3 asymmetry and magnitude variation with tone spacing is a resultant of impedance seen by baseband signals.
- This effect is detrimental when using pre-distortion techniques for linearization.
- A good control over baseband impedance can have an impact on linearity improvement of the circuit[9].

1.4 Thesis objectives

The work of this thesis involves designing, simulating and realizing a power modulator and implementing the realized modulator into existing active harmonic load-pull (AHLP) system. The designed modulator should be capable of:

- DC biasing both low (i.e., 14V) and high power devices (i.e., 28V).
- Controlling the impedance at baseband frequency by injecting the amplitude and phase controlled high power signal (about 50W[10]) towards the device over a wide bandwidth (about 40MHz).
- Operating in pulsed mode to enable pulsed DC testing of the device.

[9] Baseband and second harmonic impedances can be controlled to generate indirect mixing terms which can be equal and opposite to IM3 tones, thus improving linearity.

[10] This number will be justified in the next chapter.

- Tracking the envelope of the input signal and bias the device accordingly. Such an envelope tracking biasing solution for load-pull system does not exist. This would enable a realistic testing of devices for ET power amplifiers.

1.5 Thesis organization

Outline of the thesis can be summarized as follows:

Chapter 2 deals with the simulation setup and simulation results used to derive the specifications for the designed baseband modulator. *Chapter 3* details the design of the modulator. In this chapter the design steps, simulation results, board layout and design issues, real component selection and the realized modulator prototype results are discussed, *Chapter 4* describes the method used for baseband calibration and measurement. The results are also discussed. *Chapter 5* details the integration of the designed modulator with the active loadpull system. Tests and results done on a real device are discussed. The thesis concludes with *Chapter 6* giving conclusions and recommendations for future work.

Chapter 2

Active Baseband Tuning

In this chapter, the concept of active baseband impedance[1] control is introduced and the system requirements to achieve this are translated into specifications for the baseband modulator. The specifications will be derived from nonlinear large signal simulation and theoretical understandings. The desired baseband power modulator will hereafter be termed as **"BB modulator"**.

2.1 Introduction

As discussed in section 1.1.2, in an active load-pull system, the load seen by the DUT at a given frequency can be set by injecting an amplitude and phase controlled signal of the same frequency towards the DUT. This is true at baseband frequency as well, i.e., the baseband impedance seen by the device can be set by injecting an amplitude and phase controlled baseband signal.

Since the frequency dependent bias networks set the baseband impedance, it is desirable to build a system that is capable of biasing the DUT and actively controlling the baseband impedance simultaneously by injecting a signal towards the DUT at baseband frequency. Realization of such a system would enable us to study and understand the device behavior when presented with different baseband impedances.

The optimal baseband impedance may in general be complex, in contrast to the commonly held belief that the envelope termination must be a short. James Brinkhoff in [21] gives an empirical formula to calculate such an optimal baseband impedance in order to minimize the IMD levels for a given bias, for a FET. Various studies have shown that, not only FETs [20–23], but also other devices like GaN HEMTs [24,25], HBTs [26,27], LDMOSs [19,28]

[1] impedance seen by the DUT at baseband frequency.

and BJTs [29–31] demonstrate memory effects as a function of baseband impedance. For these reasons, it becomes important to control the baseband impedance across the whole Smith chart, in order to study and optimize the linear behavior of RF devices. In order to realize such a solution, it is clear from the previous section that there is a need of a system capable of

- Injecting a signal at baseband frequencies over a wide bandwidth starting from DC to control the baseband impedance.
- Providing a constant (or envelope tracking or pulsed) DC biasing.

However, such a solution has to satisfy an explicit set of requirements called specifications. Specifications such as

- Range of constant voltage levels required to bias the DUT[2]
- Maximum deliverable current
- Bandwidth, i.e., the range of frequencies over which it must operate
- Maximum signal swing, required to set the desired baseband impedance

In this chapter, quantified values of such specifications will be identified based on certain simulation and theoretical understandings.

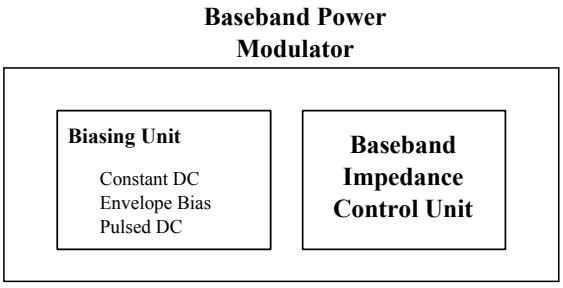


Figure 2.1: Functional Block diagram representing BB modulator.

Deriving specifications for the BB modulator defined as a single entity becomes cumbersome. So, it is split up into two functional blocks, viz. biasing and baseband impedance control units, see Figure 2.1. The biasing unit is subdivided into constant, envelope and pulsed biasing. Specifications are quantified for each of the two units and at the end of the chapter all the specifications are combined to give the overall specifications for the BB modulator.

[2]Low/high power RF devices such as LDMOSs, GaN/GaAs HBTs etc.

2.2 Biasing unit

Depending on the characterization requirement, the DUT can be biased in one of the following configurations (see Figure 2.2):

- Constant biasing
- Envelope biasing
- Pulsed biasing

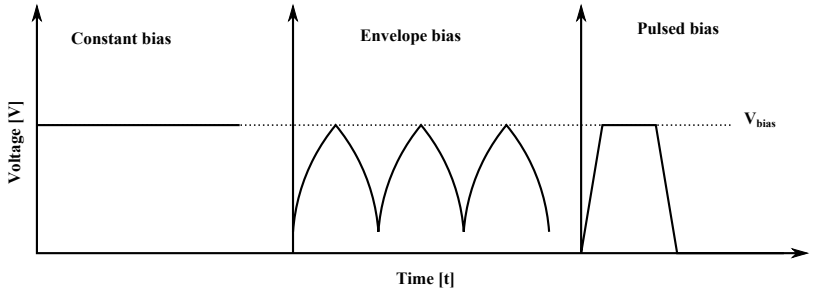


Figure 2.2: Bias Configurations showing constant, pulsed and DC biasing requirements.

2.2.1 Constant DC biasing

A wide range of RF devices are available today to satisfy the application needs in the market. The drain (collector) bias/supply for these devices vary with the power rating of these devices. As discussed, Load-pull setup is used to characterize these devices. Table 2.1 shows a list of low to high power RF devices, their typical drain (collector) bias voltages and their maximum current rating.

Devices	Drain Bias [V]	Max Current [A]
LDMOS(upto 100W)[NXP]	12.5 - 32	12(45W) - 20(100W)
CMOS(0.16um)[Skyworks]	2.9 - 5.5	1.5
GaAs HBT[Skyworks]	2.9 - 4.6	2
GaN HEMT[CREE]	28	28(120W)
BJT[NXP]	2 - 50	15A(250W)

Table 2.1: Typical bias Voltages and maximum current of different RF devices.

The BB modulator should be able to provide constant DC voltage to bias these devices. It should be capable of outputting a desired DC voltage which is load[3] and line[4] regulated. The modulator should not only be able to supply sufficient DC voltage but also be capable of providing sufficient current. For example, a typical 45W LDMOS device has an absolute maximum current rating of 12A when operated with 28V on its drain.

2.2.2 Envelope biasing

With the requirement of high data rate capability, the amplitude modulated signals become inevitable. This means that a PA cannot be operated in power compression region anymore. PAs have to be operated at an average power, backed-off from the peak output power. Thus, the efficiency of the PA becomes an important scale of performance measure in PA design. As discussed in section 1.2.1, an envelope tracking amplifier is one such efficiency enhancement technique for PA design. Envelope tracking power amplifiers dynamically adjust the drain bias voltage of the RF power amplifiers according to the input power level, so that the RF power amplifiers operate in saturation region for all input amplitudes. A RF device used in envelope tracking configuration is best characterized under varying drain bias. So, it becomes necessary that the load-pull systems incorporate such a varying drain (collector) bias solution.

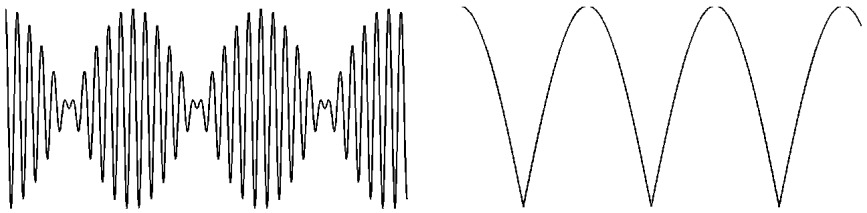
Consider a two tone signal as shown in Figure 2.3(a). The envelope of such a signal is shown in Figure 2.3(b). So, the BB modulator should be capable of outputting a DC voltage similar to Figure 2.3(b). Depending on modulation scheme and the power rating of RF device, the envelope peak voltage can be in the region of breakdown voltage for a given RF device. So, the BB modulator should be capable of dynamically changing its output DC voltage from knee voltage (2V-6V) of the biased RF device to at least half of its breakdown voltage (25V-50V) in the case of an LDMOS device.

2.2.3 Pulsed DC bias

Even though memory effects are majorly caused by the variation of baseband impedance as discussed in section 1.3.1, it is not limited to it, thermal [32] and charge trapping effects [33] also contribute to memory effects. This subsection explores the role of thermal effects in causing memory effects and the need of pulsed characterization.

[3]Load regulation is the measure of ability of the modulator to maintain a constant voltage at its output irrespective of changes in load.

[4]Line regulation is the measure of ability to of the modulator to maintain a constant output voltage at its output irrespective of variations in the input voltage level.



(a) 2-tone signal (b) Envelope signal

Figure 2.3: Wave form showing time domain 2-Tone signal and its envelope.

Thermal and trapping effects

The on state voltage and the current gain of power FETs, LDMOSs, HBTs and BJTs are temperature dependent and vary due to *self heating* where the process of *self heating* can be seen as the temperature change caused by the power dissipation which is a function of drain (or collector in case of BJTs/HBTs) current, that has a frequency response determined by the physical structure of the transistor and its packaging.

This heating process can be considered as a feedback mechanism which influences the drain or collector current due to temperature dependency of carrier mobility, threshold voltage, and carrier saturation velocity [32]. Anthony Parker [32], represents this process as a feedback system and in his measurements while maintaining baseband impedance constant, shows that the variations and asymmetries in intermodulation levels with tone spacing are also attributed to the self heating process within the device.

Dispersion effects such as current collapse, g_m dispersion etc. observed in large bandgap RF devices (GaN, AlGaN, GaAs, SiC) have been attributed to *surface trapping* effects [34, 35]. These phenomena affect the output performance of the RF devices. These *trapping effects* arise from the capture and emission of electrons injected in the semi-insulated substrate by deep level traps [36]. The related time constants to these effects are in μs and ms regime [33].

The charge trapping and self-heating mechanisms are not considered significant at high frequencies as they have slow time constants. However, the baseband frequencies, being slow, interact with slow time constants and have been linked to the generation of intermodulation products and the asymmetry in intermodulation products [37].

Need of pulsed bias system

- Pulsed measurements have been and continue to be used for small signal iso-thermal

characterization to gain an insight about the device linearity, which is useful for circuit designing and as well for device model verification [38].

- The trapping process results in strong dependencies of I-V characteristics in drain-source voltage slow dynamics. This makes the modeling process difficult to be carried out as the RF I-V characteristics strongly differ from DC ones [36]. This drawback can be eliminated by using pulsed measurements which allow to derive a set of output characteristics for a particular quiescent bias point, as long as the pulse duration is much smaller than the emission process time constant. It was shown that device performance could be accurately predicted by using the pulsed characteristics in small and large signal models [39, 40].

- The S-parameters extracted by characterizing a device with constant DC bias and in continuous wave (CW) mode will not accurately predict the operation of that device under pulsed condition[5]. And, it becomes necessary to have information of various parameters in pulsed mode when the devices operating outside the safe operating area are to be tested, for e.g. for radar system applications. So, the pulsed measurements are used to measure the device parameters to assist in the design of circuits for pulsed operation.

- Gate oxide tends to be few angstroms thick in latest CMOS technologies. These oxide layers cannot be characterized by applying large constant DC biasing, which would result in high electric fields that injects large amount of charge into the device. The hot electron might cause permanent damage to the film rendering subsequent I-V chracterizations futile. Pulsed I-V characterization techniques are used to avoid such problems by limiting the number of hot electrons injected into the device [41].

2.3 Baseband impedance control unit

As discussed in section 1.1.2, in an active load-pull system, the load seen by the DUT at a given frequency can be set by injecting amplitude and phase controlled signal of same frequency towards the DUT. It is required to know the minimum/maximum power that the BB modulator has to inject at a certain baseband frequency to be able to control the baseband impedance over the whole Smith chart. [42] gives an equation (eqn 2.1) to calculate the amount of power that has to be injected towards the DUT to achieve a specific load impedance.

[5] Because of the onset of thermal effects.

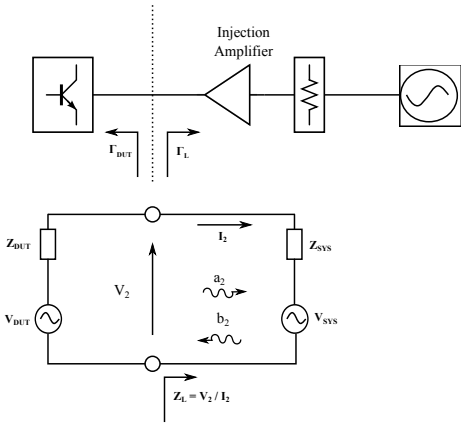


Figure 2.4: Injection amplifier and DUT

$$P_{inj} = P_{b2} = P_{a2}.\frac{1-|\Gamma_{DUT}|^2}{1-|\Gamma_{SYS}|^2}.\frac{|Z_{DUT}+Z_0|^2}{|Z_{SYS}+Z_0|^2}.\frac{|Z_L-Z_{SYS}|^2}{|Z_{DUT}+Z_L|^2} \tag{2.1}$$

From Figure 2.4 and equation 2.1 it can be seen that the power injected in order to set a desired gamma depends on the power generated by the DUT and the impedance seen by the injection amplifier at that frequency. These parameters depend on the power capability of the DUT and the technology used to construct it.

Following subsection details the simulations performed, in order to obtain the power levels and voltage swings the injection amplifier must support and the bandwidth it should have in order to control the baseband impedance of an NXP LDMOS[6].

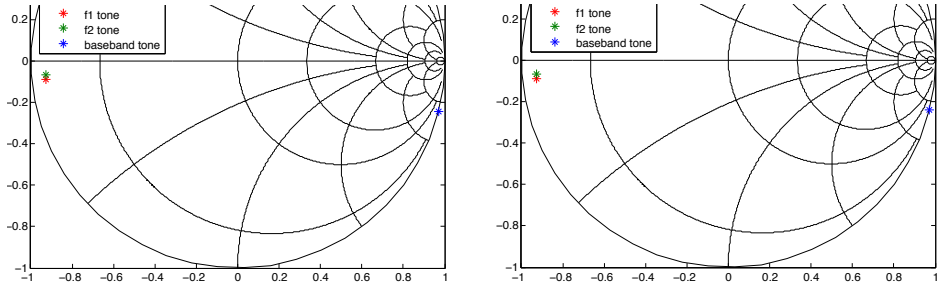
2.3.1 Desired signal swing

The results in this subsection are resultant of the simulations performed using NXP BLF6G22_45 LDMOS model, a typical 45W device used in base station applications.

Passive matching

To begin with, the selected device was biased at $I_{dq} = 405mA$, $V_{DS} = 28V$ with $R_L = 50\Omega$. Harmonic Balance simulation was performed by exciting the device with a two tone continuos RF signal having centre frequency of 2.14GHz and a tone spacing of 20MHz. Input and output matching networks were designed using passive components to power match (10W per tone) the device. Figure 2.5(a) shows the output reflection coefficients (Γ_L) of fundamental and baseband tones under power matched conditions.

[6]NXP BLF6G22 45 ADS model.



(a) Γ*s* when power matched passively (b) Γ*s* when power matched actively

Figure 2.5: Reflection coefficients with active and passive matching networks for power match condition

Active matching

Figure 2.6 shows the device under same bias conditions as above but power matched actively by injecting power at fundamental and baseband tones. Figure 2.5(b) shows that the reflection coefficients of fundamental and baseband tones are set close to the corresponding reflection coefficients with passive matching network, to power match the device to 10W per tone.

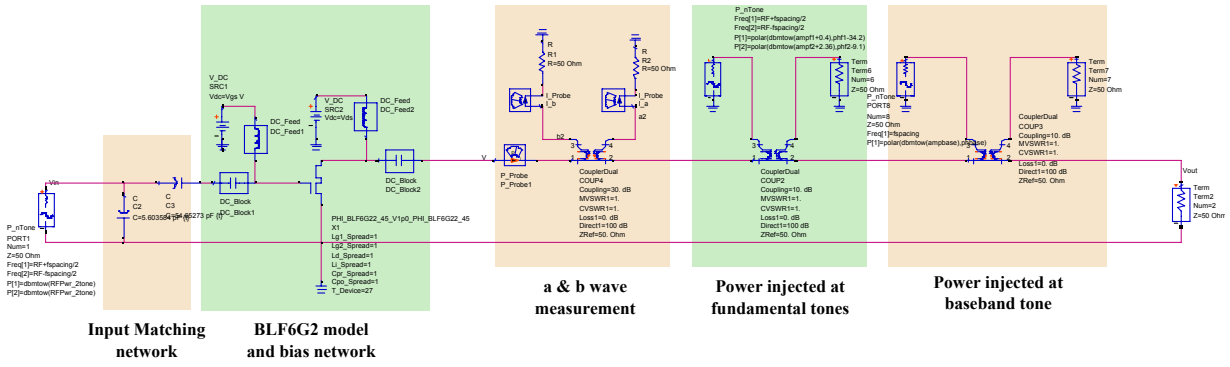


Figure 2.6: ADS simulation setup showing input matching network, DUT and actively power matched at the output.

Controlling Baseband Impedance

The amplitude and phase of the injected power at the baseband is varied to set the baseband impedance to seven different impedances as shown in Figure 2.7 (*Z_{BB}). The power injected to place the baseband impedance at these points were observed and are given in Table 2.2. This table compares the simulated and theoretical values of *'power to be injected'* to set the

baseband impedance. Theoretical values are calculated using the Equation 2.1, where Z_{DUT} was calculated by doing large signal S-parameter (LSSP) simulation and Z_{SYS} is assumed to be 50Ω. Table 2.2 also gives the magnitudes of the signals that were injected at baseband in simulation. Simulated P_{inj} numbers in the table are corrected for the 10dB coupler used to couple the baseband signals. In reality a coupler would not be used to inject the baseband signals.

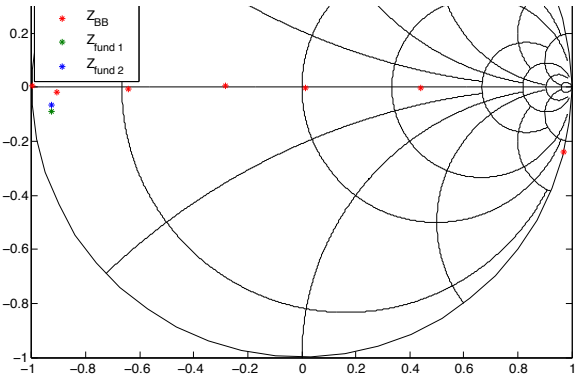


Figure 2.7: Keeping the fundamental load impedances fixed, the baseband impedance was varied across the Smith chart as shown.

Impedance [Ω]	**Simulated P_{inj}[dBm]**	**Theoretical P_{inj}[dBm]**	**Voltage [V_{p-p}]**
0 - 415j	38.59	29.71	32.1
128 - 0.8j	34.03	27.71	31.2
51 - 0.3j	06.88	04.17	28.0
28 + 0.25j	34.03	31.36	24.4
14 - 0.2j	43.15	42.77	15.2
2.4 - 0.4j	47.05	46.91	04.4
0.05 + 0.01j	48.14	48.26	01.2

Table 2.2: Simulated vs Theoretical injected power

The differences seen in the theoretical and simulated injection power is due to the assumption of one Z_{DUT} value for all the calculations, whereas the Z_{DUT} depends on the injected signal. From the Table 2.2, it can be understood that, the BB modulator should be capable of providing a swing of 35V and about 60W in the worst case in order to be capable of placing the baseband impedance at desired location over the Smithchart for a 45W device.

2.3.2 Desired bandwidth

Following details were considered to define the bandwidth to quantify the bandwidth specification :

- It is desired to control and correct baseband impedances of at least two WCDMA channels including guard and ACPR bands, each 5MHz wide. This results in a total bandwidth of 35MHz

  ACPR2 - ACPR1 - Channel1 - Guard band - Channel2 - ACPR1 - ACPR2 = 7*5 = 35MHz

- With a 40MHz bandwidth, the system should be capable of generating pulses with rising time as low as 10ns (≈8.75ns). This would enable the BB modulator to pulse bias the DUT with fast well settled pulses in less than 100ns.

2.4 Set of specifications

In this chapter, from the simulation and theoretical understandings, quantified specifications are derived for the BB modulator. These specifications are summed up as below :

- DC Capability[7]
  - Range of DC Voltage : 0V - 50V
  - Maximum current : 15A
- AC Delivering Capability
  - Maximum signal swing : 50 V_{p-p}
  - Bandwidth : 40MHz

2.5 Conclusion

In this chapter, reasoned derivations of specifications for the BB modulator were made based on theoretical and simulation understandings. In the next chapter a BB modulator design procedure to achieve the derived specifications will be explained.

[7] Load and Line regulated.

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