A Non-galvanic Chip-to-Waveguide Transition For Mm-Wave Characterisation Probes

Cyrus Tirband

Master Thesis
Delft University of Technology

Student:
Cyrus Tirband
Programme: Master
Telecommunications &
Sensing Systems

Supervisors:
Dr. M. Spirito
Dr. D. Cavallo
Terahertz Sensing Group
Faculty of EEMCS

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Abstract

To solve extant complications with standard wafer-probing techniques, such as probe-to-probe coupling and probe-tip deterioration, a novel probe tip device has been designed and verified by means of 3D EM-simulation for the 220-325 GHz frequency band. The new probing technique uses an on-wafer cavity-backed slot to couple the signal to a tapered structure in an open-ended waveguide which is held above the cavity, and acts as a fully shielded transition from the transverse electromagnetic mode of the planar stripline to the fundamental transverse electric mode of the waveguide. The on-wafer structure used for the transition is limited to the back-end-of-line of the process, and is shielded from the ill-characterised substrate. The transition achieves an insertion loss of <1.8 dB across the entire 220-325 GHz band and does not require galvanic contact with the die.
The layout for the on-wafer structure has been designed for a 0.25 µm SiGe process and a simplified version has been used for a simulated sample measurement using the thru-reflect-line calibration algorithm. Due to coupling to nearby structures, the novel probing technique show significant improvement over the standard coplanar probes only when a chip area greater than the cross-section of the open-ended waveguide is reserved. Simulated measurement of an independent passive structure show a reduction of the average worst case bound from 0.041 to 0.017 in the 220-325 GHz band.

1

Introduction

1.1. Motivation

In recent years, millimeter-wave (mm-wave) frequencies have become a key spectrum to enable applications such as imaging, automotive radar and ultra-fast wireless communications [1–3]. Design of circuits in these frequencies is no simple task, and it is for this reason that accurate models must be known to aid the design and verification procedure of active and passive devices. This is where device characterisation fills the gap: if an accurate model of the device parameters can be extracted, the development time and cost of designing integrated circuits will decrease substantially.

Measuring and characterising active and passive components mm-wave frequencies comes with many challenges. When the operating wavelength is relatively short compared to the signal path, the systematic error introduced by the instrumentation must be removed in a process called calibration.

1.2. Difficulties of calibration

Calibration is used to remove unwanted parasitics, capacitances, and transitions from the network leading up to the device. If the calibration is performed poorly, the quality of the measurement will suffer, which is why a lot of effort in device metrology is put into exactly this topic.

Calibration requires the measurement of a set of standards that can be found on an impedance standard substrate (ISS), on the same wafer on which the device is placed, or with two-tier procedure that uses a combination of the two. The SOLT (SHORT-OPEN-LOAD-THRU) calibration algorithm requires fully characterised standards. When dealing with frequencies well into the mm-wave spectrum, the parasitic capacitances and inductances of these standards are extremely difficult to characterise. Moreover, the parasitics may even change depending on where the

probe is placed. In these cases, the thru-reflect-line (TRL) algorithm [4] which requires precise knowledge of only the characteristic impedance of the transmission line used, is the most commonly employed algorithm [5].

Despite not needing the exact knowledge of the standards, TRL calibration is still a cumbersome task. Often, a two-tier calibration is used where the test set-up is first calibrated to the tips of the probe first. At this point, the parasitics of the contact pads and all other transitions leading up to the devices are not yet accounted for. Then, the calibration is transferred to an on-wafer environment where the rest is accounted for.

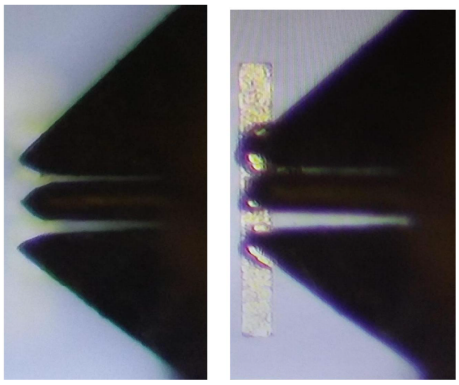
Performing calibration in this way introduces several inaccuracies. ISSs typically use a thick alumina substrate with relatively high dielectric permittivity ($\varepsilon_r = 9.6$), which supports higher order surface wave modes, especially the TE mode [6]. If the ISS is directly placed on the metallic chuck of the wafer probing environment, parallel-plate waveguide modes are also supported [7] [8]. On top of this, the difference in dielectric permittivity between the ISS and the BEOL of the wafer causes probe tips to couple differently, which in turn introduces more inaccuracies when transferring the calibration to an on-wafer environment [9]. For all of the aforementioned reasons, the calibration standards should be implemented on the BEOL which is the same as the one belonging to the wafer of the device. By using the bottom metal layers of the BEOL as a ground plane, the standards are shielded from the lossy, electrically thick, and ill-defined substrate. The top metal layer is then usually used to carry the signal. This top metal layer is often the thickest, which in turn makes it the least lossy when used as a transmission lines. It is also the most distant from the ground plane, which makes impedance matching easier.

However, if the intent is to measure an active device, placing the transmission line at the top metal layer may be a disadvantage. If the line standard is at the top metal layer, then so will be the plane of reference of the calibration. This means that the terminals of the device, which are found at the bottom of the BEOL, are still displaced from this reference location and connected with a transition made of vias. In [10], the substrate is unshielded but the layers above are capacitively loaded so as to increase the effective permittivity above the bottom metal line. In this way, more energy flows above the line and the impact of the substrate is reduced.

After calibration, the error-terms can be extracted and can be used to correct a measurement of a device under test (DUT). The error terms represent residuals introduced by the test set-up. Although a term that would describe crosstalk, direct coupling from one measurement port to the other without passing through the DUT, is present, it is usually omitted as it tends to worsen the measurement rather than improve it [11]. One reason for this is that the crosstalk is dependent on the distance between the probes amongst other things and, since the standards are not all of the same length, the error will not be consistent between each measurement. For this reason, the calibrations performed in this thesis will use the 10-term

error model. This makes crosstalk between probes a large complication, especially at higher frequencies where a larger portion of the energy is present in substrate modes and even direct probe-to-probe coupling.

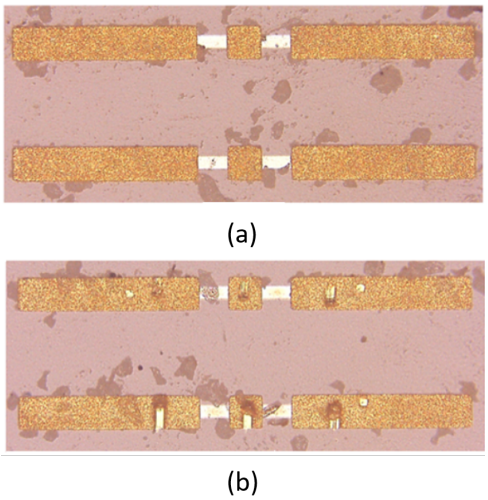
This is not the only inconsistency in the measurement of calibration standards. Measuring higher frequencies implies using a smaller probe pitch (distance between the pins of the probe tip), making them less rigid and more prone to damage and breaking. Deformations caused may bring the central conductor and the ground of the probe tips closer together, changing the characteristic impedance of the transmission line on the probe. An example of this is shown in Fig. 1.1.



(a) **(b)**

Figure 1.1: A coplanar probe before (a) and after (b) landing on an alumina substrate standard. After landing, the center pin has bent a certain distance towards the upper ground pin, affecting the characteristic impedance of the probe. Image taken from [12].

The landing pads on the die are also deformed when landed on by a probe: in a process called 'skating', in order to ensure proper conductive contact the probe tips flex and scratch a certain distance along the landing pads after touching down. This creates grooves in the metal pads, shown in Fig. 1.2. Though not much of an issue at lower frequencies, in the mm-wave range these deformations become electrically large and bring parasitics with them that are distributed in nature. When performing broadband measurements, several landings must be performed on the same test pad as each frequency range has its own probe. This exacerbates the problem further, creating discontinuities between the measurements of each frequency band.



(a)

(b)

Figure 1.2: Photograph of the landing pad before (a) and after (b) being touched down on by a coplanar probe. Notable grooves can be seen in the photograph that is taken post landing.

Skating also wears out the tips of the probe, even when performed by a skilled operator. With typical wafer probes for the WR-3 frequency band costing upwards of 5000 euros, this constitutes a need for innovation.

1.3. Goal of this study

And so, the need for a new method of probing has hopefully become clear. The goal of this thesis is to design a transition from a planar environment to a waveguide for mm-wave characterisation probes that addresses calibration problems by having the following properties:

- The transition is limited to the BEOL so as to prevent excitation of higher order modes and not be exposed to an ill-defined substrate;
- The transition is as much as possible shielded from outside sources, so that coupling to surrounding structures on the chip and direct probe-to-probe coupling is mitigated;
- The probe is robust and does not need to skate along the die to function.

All the while, the probe should not sacrifice dynamic range (power transmission). IC-to-waveguide transitions that do not use landing pads have been proposed in literature [13–19], but never in a back-end-of-line as thin as 10 µm, a typical value for BiCMOS RF processes, while simultaneously covering a large portion of the waveguide band.
This thesis will focus on the verification of the design for the WR-3 frequency band, although the design procedure itself is not intrinsically limited to this band.

1.4. Proposed structure

The total probe consists of two distinct parts: a waveguide section and a cavity-backed slot. The concepts builds on an idea introduced in [20]. The waveguide section is an open-ended waveguide with a metallic structure that converts the fundamental transverse electric (TE) mode of the waveguide into a transverse electromagnetic (TEM) mode at the waveguide end, which interfaces with the chip (Fig. 1.3).

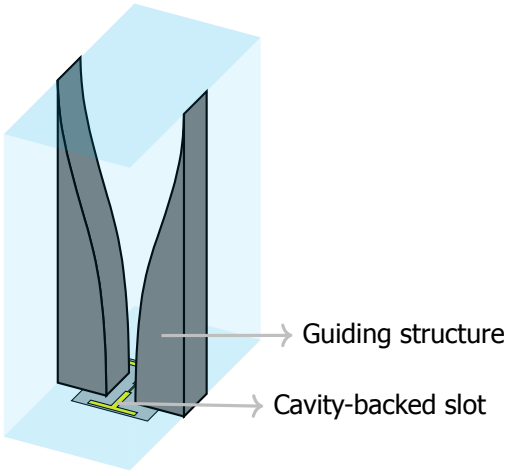


Figure 1.3: Overview of the transition. The rectangular waveguide containing the guiding structure is placed on top of the cavity backed slot, and shapes the field to match those of the fundamental mode of the waveguide.

The metallic structure can be realized with different approaches, such as continuous tapers or stepped transitions, symmetric or asymmetric with respect to the central axis of the waveguide, with one or two metal flares (see Fig. 1.4). The taper is necessary to efficiently excite the fundamental mode of the rectangular waveguide in a wideband manner. Smaller widths of the gaps and increased lengths of the tapered structure can be used to increase the bandwidth. The probe may lightly touch the surface of the chip or hover slightly above it without galvanic contact.

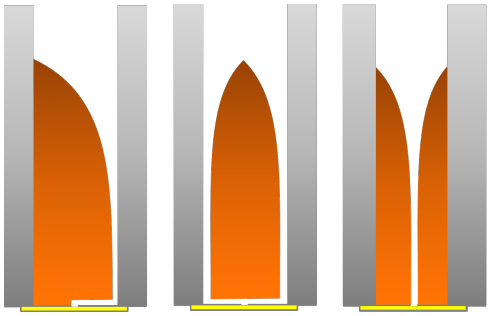


Figure 1.4: Three possible tapered guiding structures. Each of these tapers could also be realised as a discrete stepped taper.

The on-chip structure is a resonant cavity-backed slot fed by a stripline in the middle. The stripline can be either terminated by a shorting pin or a radial open stub. The cavity-backed slot antenna is realized in the BEOL of the integrated circuit, using the bottom metal layer as the backing short for the slot, with the slot being in the top metal layer. The stripline will be implemented with an intermediate metal layers. However different metal layers for slot, cavity and stripline may be used. The walls are implemented by means of via fences. A schematic overview of the on-chip structure is shown in Fig. 1.5.

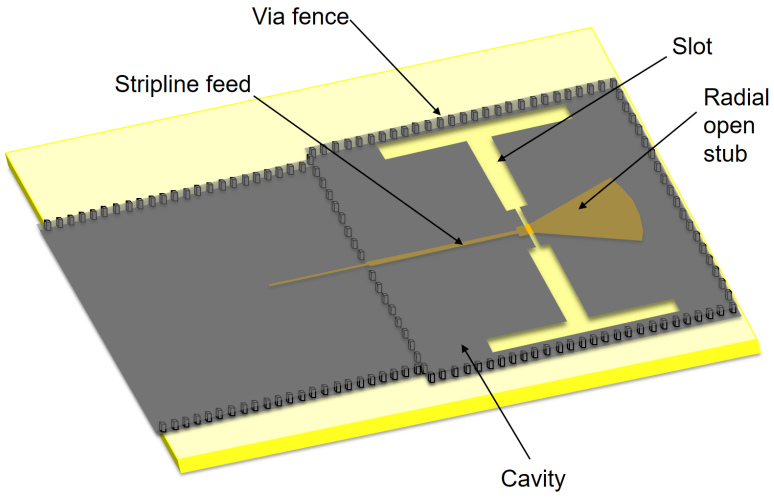


Figure 1.5: Schematic overview of the chip section of the transition.

1.5. Outline of this thesis

In chapters 2 and 3, the design steps of the entire probe will be presented. Chapter 2 will focus on the design of the waveguide section of the probe, whereas chapter 3 will be about the on-wafer structure. In chapter 4, the performance of the design will be gauged aswell as its tolerance to displacement. In chapter 5, a layout is presented of an on-wafer calibration kit and a simulation study is performed to verify its workings. Chapter 5 finishes the report by providing conclusions.

2

Waveguide section

In this chapter the design of the waveguide section will be discussed. The main function of the waveguide section is to couple the tranverse electromagnetic (TEM) mode supplied by the feed to the transverse electric (TE) mode of the rectangular waveguide (RWG) with minimal reflections.

2.1. Tapered lines

In order to efficiently excite the TE_{10} mode of the RWG, a tapered transmission line is used. This line propagates a (mostly) TEM mode and tapers out until it eventually continues into the TE_{10} mode of the RWG. A guiding structure is used to support this tapered line. The electric field lines of the TEM mode supported by the guiding structure run either between the walls of the waveguide and the sides of the guiding structure or between the two separate metal parts of the guiding structure, as is made clear in Fig. 2.1, where two possible realisations for such a guiding structure are shown. As the metal part tapers, the TE_{10} mode can be excited, because its field lines are parallel to that of the TEM mode.

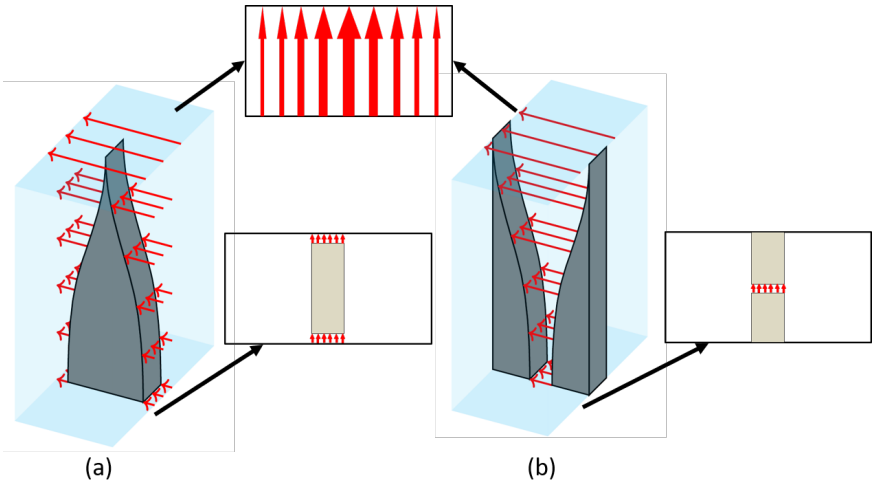


Figure 2.1: Two guiding structure possibilities for a vertical transition from a TEM mode (insets to the right of the structures) to the TE_{10} mode of the waveguide (inset above). In **(a)**, the tapered TEM-line propagates between the walls of the waveguide and the sides of the guiding structure. In **(b)**, the tapered TEM-line propagates between the two metal parts.

For the analysis of the tapered line in this section, the theory of small reflections is used as described in [21].

The taper is allowed to be several wavelengths long at the center frequency of 272.5 GHz (one wavelength being 1.1 mm in the WR3 band) and the reflection coefficient should ideally be as low and stable as possible throughout the frequency band. To this end, a triangular taper is chosen. That is, a taper with the following profile for the line impedance versus position:

$$Z(z) = \begin{cases} Z_0 e^{2z^2/L^2 \ln(Z_L/Z_0)} & \text{for } 0 \le z \le L/2 \\ Z_0 e^{(4z/L - 2z^2/L^2 - 1)\ln(Z_L/Z_0)} & \text{for } L/2 \le z \le L \end{cases} \tag{2.1}$$

Here, Z_0 is the line impedance at position $z = 0$ (the start of the tapered line), and Z_L is the line impedance at position $z = L$ (the end of the tapered line). The name *triangular taper* can be misleading, but it is aptly named because $\frac{d\ln Z}{dz}$ is a triangular function.

Compared to other typically used continuous taper profiles, the triangular reaches the first null of its reflection coefficient later. However, at higher frequencies it has a lower value for its reflection coefficient and on top of this it stays more stable in the frequency band. The triangular taper shall in theory result in the reflection coefficient $\Gamma(\beta L)$ given by the equation below:

$$\Gamma(\beta L) = \frac{1}{2} e^{-j\beta L} \ln\left(\frac{Z_L}{Z_0}\right) \left[\frac{\sin(\beta L/2)}{\beta L/2}\right]^2 \tag{2.2}$$

where β is $\frac{2\pi}{\lambda}$, the propagation constant of the tapered line. The magnitude of the reflection coefficient can be seen in Fig. 2.2. For comparison, the magnitude reflection coefficient of an exponentially tapered line is also shown. The values on the vertical axis are omitted because they depend on the specific values of Z_L and Z_0 for the transformer. Moreover, Equation 2.2 is not valid for small values of βL. At βL =, the equation predicts $\Gamma = \frac{1}{2}(\ln \frac{Z_L}{Z_0})$ while in this limit it should tend to $\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}$.

It can be seen that the exponential taper reaches its first null earlier, but has a higher value for the reflection coefficient in for larger values of βL. Since the maximum length of the structure is not a real concern, no trade-off needs to be made in other to choose the triangular taper of the exponential taper or any other taper.

However, it should be noted that the first null of the reflection coefficient should be reached, which occurs at $\beta L = 2\pi$. For this reason, it is preferred that the tapered line is at least as long as the longest wavelength in the frequency band (1.4 mm in the WR3 band).

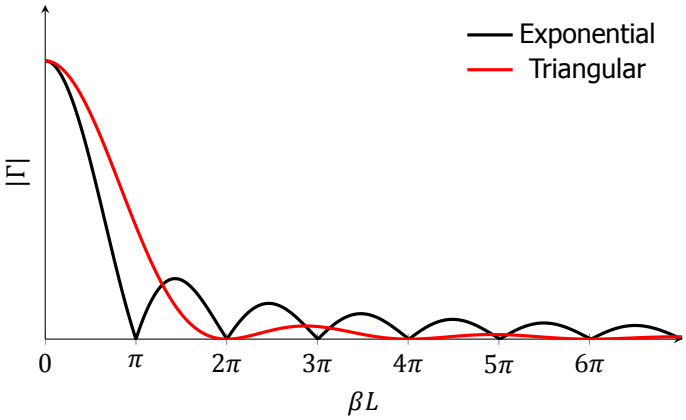


Figure 2.2: Magnitude of the reflection coefficient of a triangularly and exponentially tapered line.

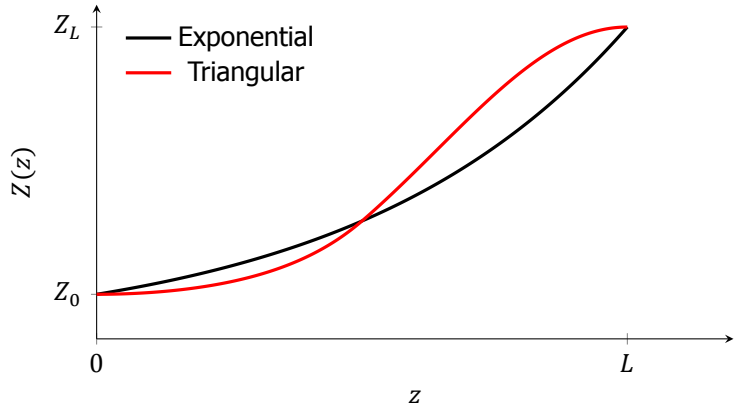


Figure 2.3: Impedance versus position for a triangularly and exponentially tapered line.

2.2. Guiding structure

One could apply this taper to the transition by shaping a guiding structure so that the distance from the wall of the RWG to the guiding structure follows the same profile as the impedance in (2.1). This approach makes two notable assumptions about the transition:

- The distance between the guiding structure and the RWG wall is proportional to the characteristic impedance of the mode that travels through this line.
- The propagating mode is a (quasi-)TEM mode. This latter assumption is less intuitive but important. The theory of small reflections on which the decision to use a triangular taper is based, is valid only for TEM lines. However, near the end of the line when the conducting parts are far from each other, a TE mode may already be propagating. At this point the electric field will be a hybrid TEM-TE mode of which the characteristic impedance is not well-defined.

2.3. Distance-impedance relation

In order to achieve the desired variation of the line's characteristic impedance throughout the transition, the relationship between the geometrical properties of the taper and the impedance must be found. Once a one-to-one relation between these two quantities is defined, the guiding structure can be shaped to achieve the required taper in impedance.

However, no such relation is documented for the pertinent geometry, whether it be analytical or empirical. The following section describes how such a relation is obtained for a guiding structure as in Fig. 2.1a. A very similar procedure can be done to obtain a relation for a guiding structure as in Fig. 2.1b, by changing the

simulation geometry.

As a first approximation, one could model the line as a microstrip, for which this relation is known [21]. This approximation is most accurate when the distance is either small or large. When the distance is small, most of the electric field will be concentrated between the guiding structure and the wall, and the fringe fields are negligible. When the distance is large, the guiding structure is thin and resembles a microstrip, since the height of the guiding structure decreases with increasing distance. A comparison between the geometry of a microstrip and that of the real line is shown in Fig. 2.4.

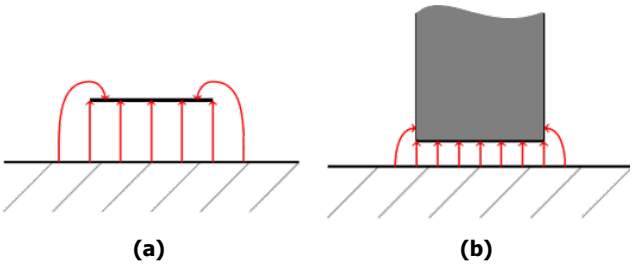


Figure 2.4: Comparison between the geometry of the microstrip (a) and that of the relevant line for the proposed structure (b). If the fringe fields were not present, the electromagnetic behaviour would've been identical.

The distance-impedance relation can be obtained by simulating the structure in CST for different values of the distance d as in Fig. 2.5.

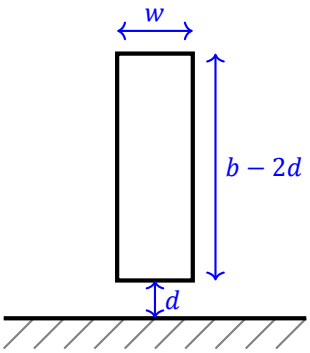


Figure 2.5: Schematic of the geometry used to obtain the line impedance of the quasi-TEM mode between the guiding structure and the waveguide wall. The height of the guiding structure is equal to $b - 2d$, where b is the length of the short waveguide wall (431.8 µm) and d is the distance between the guiding structure and the wall. w denotes the width of the structure.

In Fig. 2.6 the simulated results are shown for width $w = 150$ µm, and d ranging

from 20 µm to 210 µm. The figure also shows a direct comparison with the characteristic impedance of a microstrip line, for which the following equation is used [21]:

$$Z_0 = \begin{cases} \frac{60}{\sqrt{\varepsilon_e}} \ln\left(\frac{8d}{w} + \frac{w}{4d}\right) & \text{for } w/d \leq 1 \\ \frac{120\pi}{\varepsilon_e} \left[w/d + 1.393 + 0.667 \ln(w/d + 1.444)\right] & \text{for } w/d \geq 1 \end{cases} \tag{2.3}$$

The first thing that stands out is that the fringe fields are not to be neglected, and the height of the guiding structure has a significant effect on the impedance of the TEM-mode. Clearly it is inaccurate to use the microstrip approximation.

A function is then constructed which closely follows the simulation results. In Fig. 2.6, the simulation is fitted to the function $d = a_0 + a_1 \cos(Z_0\omega) + b_1 \sin(Z_0\omega)$ using the non-linear least squares method, with a_0, a_1, b_1, and ω being the parameters which are fitted for, and d given in mm. The function was chosen for its wide availability in curve fitting packages, and because it accurately describes the simulation results in this case with relatively few variables. The values that were found are $a_0 = 0.109$, $a_1 = -0.108$, $b_1 = 0.0046$, and $\omega = 0.01882$.

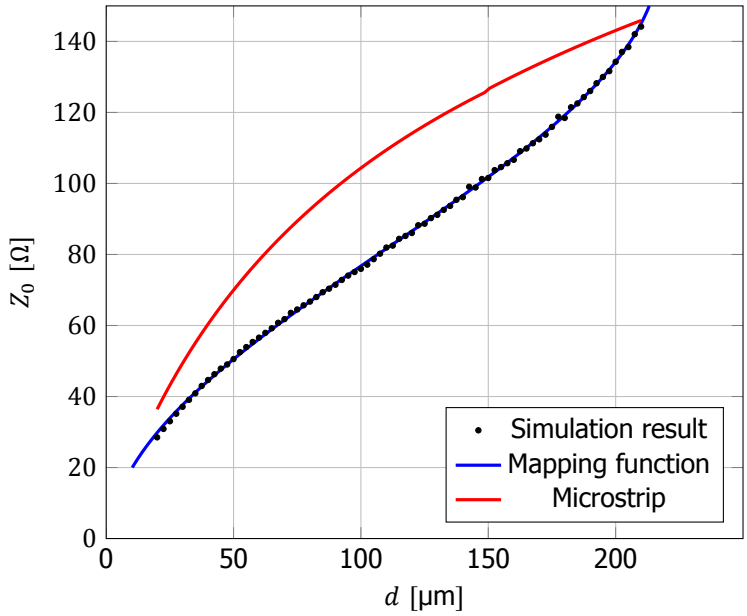


Figure 2.6: Result of the simulation using the geometry shown in Fig. 2.5 for $w = 150$ µm. The black dots shows the simulation results, the blue curve shows the mapping function constructed based on this result, and the red line shows the known curve for a microstrip.

To summarise, shaping the guiding structure is done according to the following

steps:

1. A simulation of the geometry is done for different distances d from the guiding structure to the waveguide wall, and a function is fitted which closely follows the data points that relate Z_0 to d.
2. An impedance profile is defined for the guiding structure which is triangularly tapered between the lowest and highest Z_0 recorded in the simulation.
3. The fitted function is used to map this impedance profile to a shape for the guiding structure.

In Fig. 2.7, the effect on the shape of the guiding structure due to mapping is shown when compared to the shape that would be obtained if the triangular taper were applied to the distance directly.

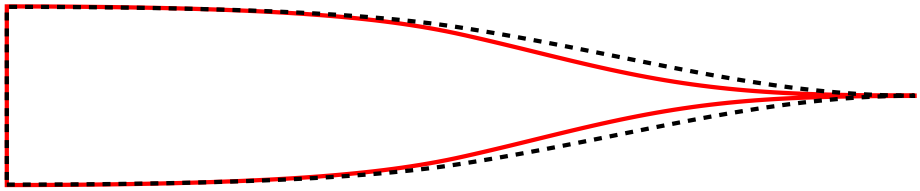


Figure 2.7: The difference in shape due to mapping of the distance d of the geometry in 2.5 to the line impedance of the TEM mode. The red outline shows the unmapped shape, and the the black dotted outline shows the shape that is adjusted by the mapping function in 2.6.

A 3D model of the tapered structure has been made in 3D electromagnetic simulation software, and its reflectivity has been directly simulated. In Fig. 2.8 the reflection coefficient of the tapered transmission line is shown . Using a triangular taper, a reflectivity of $< -20dB$ over the entire frequency band is obtained.

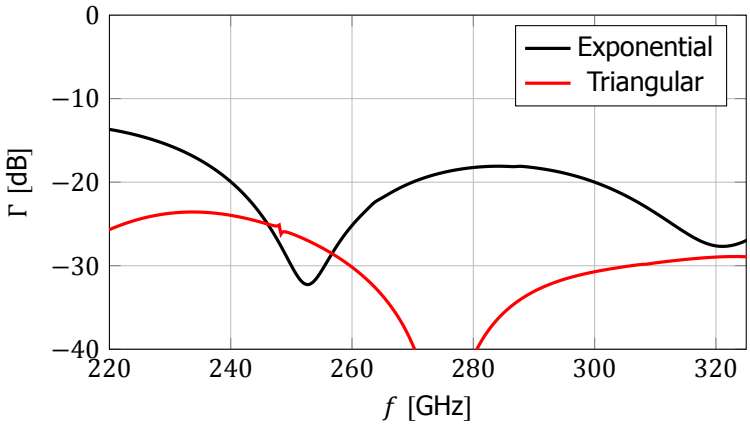


Figure 2.8: Reflectivity of the tapered transformer, obtained through 3D EM simulation. The exponential taper (red) notacibly performs worse than the triangular taper (black) as is expected in this frequency band.

2.4. Placement of dielectric

The coupling to the waveguide can be increased by placing a dielectric brick between the metal parts of the guiding structure, as shown in Fig. 2.9. By placing this dielectric just above the feed, the field will flow more in the direction of higher dielectric permittivity. The advantage is twofold: not only is the coupling to the waveguide stronger, the input impedance Z_{in} of the waveguide will also reduce, so that the distance between the two parts of the metal guiding structure can be increased while keeping the input impedance the same. This is analogous to the reduction in the characteristic impedance of a parallel plate waveguide by a factor of $\sqrt{\varepsilon_r}$ when a dielectric is introduced in between the plates. However, unless the entire waveguide is filled with this dielectric material, reflections will occur at the dielectric-air interface where the dielectric stops. In order to prevent this, the height of the brick should be chosen so that it is a quarter-wave transformer at the center frequency. Initial designs used a 80 µm tall silicon ($\varepsilon_r = 11.9$) brick, for example.

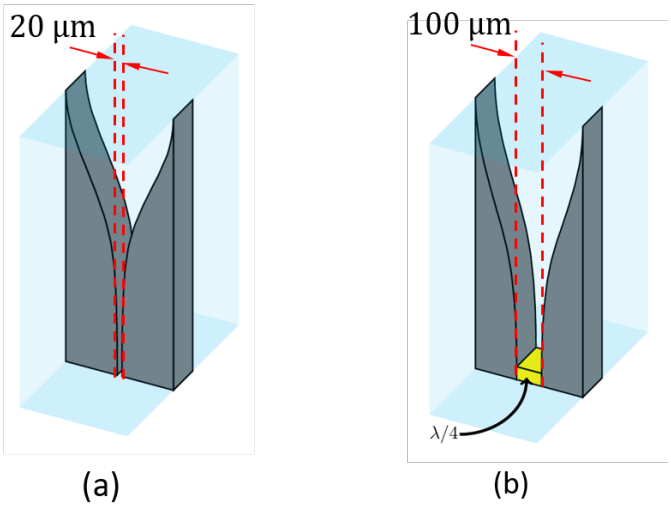


Figure 2.9: Schematic showing the placement of a dielectric inside the waveguide to improve coupling to the waveguide. When the dielectric is placed, the metal parts can be placed further apart.

Relaxing the requirements on the distance between the metal parts of the guiding structure also improves the robustness of the transition to placement inaccuracies. The transition functions well when the feed of the guiding structure is placed above the feed of the slot, and none of the metal parts of the guiding structure cover and short parts of the slot. Fig. 2.11 shows how placement inaccuracies lead to shorting of the slot.

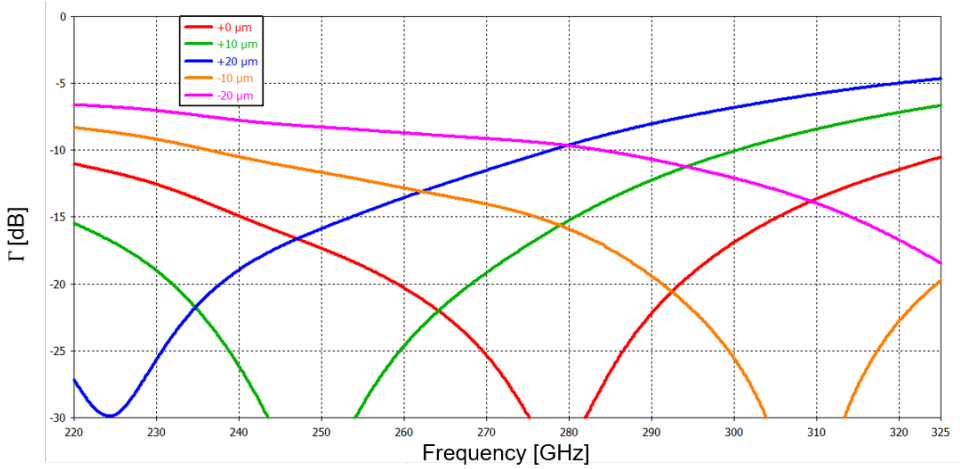


Figure 2.10: Plot showing the effect of deviations from the nominal value of the dielectric height on the reflection coefficient of the probe.

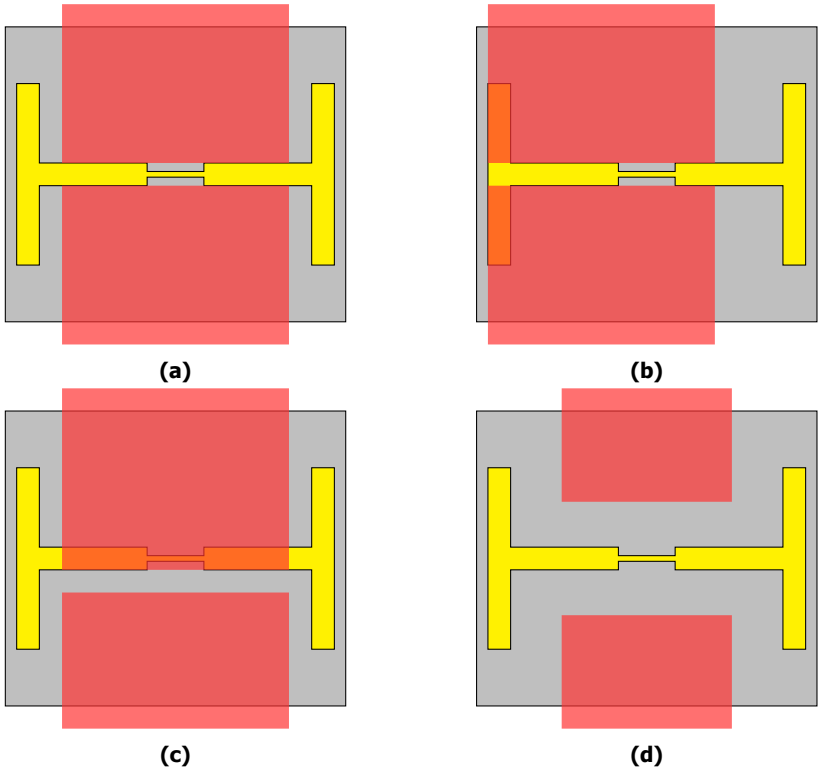


Figure 2.11: Images of the base of the guiding structure (in red) on top of the IC-section of the probe. **(a)** The base of the fins perfectly aligned on the IC-section of the waveguide probe. **(b)** Misalignment in the x-direction short circuiting part of the slot, causing the resonant frequency of the slot to shift to higher frequency and damaging the transmission at lower frequencies of the band. **(c)** Complete failure of the probe due to misalignment in the y-direction, short-circuiting the slot altogether. **(d)** A larger gap and narrower fins increase the margins before the malfunctions outlined in (c) and (d) occur.

Despite the aforementioned advantages of placing dielectric at the tip of the waveguide, it will not be included in the final design. The reasons for this being the difficulty of fabricating such a dielectric brick and placing it. On top of this, the dimensions of the brick must be accurate, since its height is equal to a quarter-wavelength. Even though in perfect conditions the transition performs better with the dielectric brick present, the height of the dielectric would become the main critical parameter affecting the bandwidth of the probe. The dependence of the reflection coefficient on the tolerance of the height of the dielectric has been simulated in the case of a silicon brick, and is shown in Fig. 2.10.

3

On-wafer structure

This chapter will detail the design steps and considerations for designing the on-wafer structure that couples the signal to the waveguide tip. To this end, an equivalent model is discussed which gives insight into how the coupling can be maximised. Then, the slot feeding network is presented. Finally, the transmissive properties of the entire design is shown.

3.1. Equivalent circuit

To understand what conditions must be met to satisfy wideband performance, an equivalent circuit model is used [22].

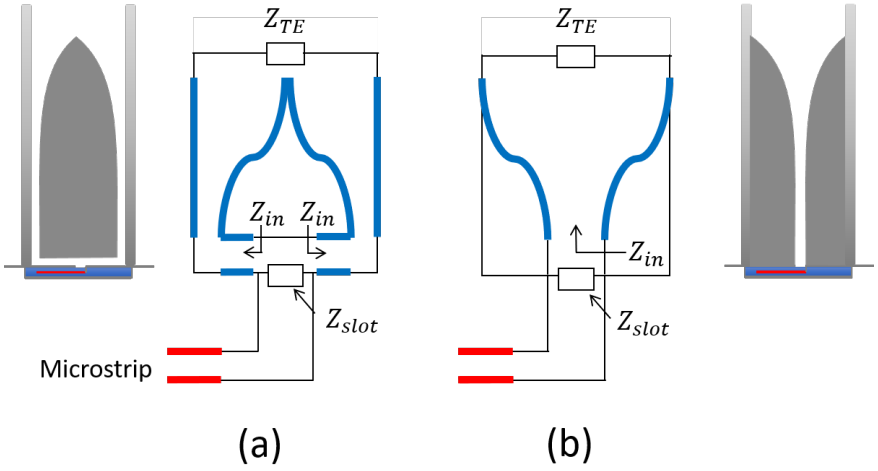


Figure 3.1: Two guiding structure possibilities. The schematic shows that the input impedance is parallel to the impedance of the slot Z_{slot}. **(a)** Schematic of a guiding structure which floats in the middle of the RWG, fed symmetrically between the RWG walls and the guiding structure. **(b)** Schematic of a guiding structure which is fed in the middle, effectively halving the total input impedance of the structure.

Consider the simplified circuit model shown in Fig. 3.1a. A stripline, with a certain characteristic impedance Z_0, couples to the slot with impedance Z_{slot} and to the rectangular waveguide which can be modelled as two series impedances Z_{in} when seen from where it is fed. The intent is to maximise the amount of power that is coupled to the waveguide. In order to achieve this, power coupled to the slot must be avoided. Since Z_{slot} is parallel to the impedances Z_{in} in the equivalent circuit model, the condition to couple most of the power to the waveguide is that Z_{slot} must be significantly large compared to $2Z_{in}$. Furthermore, $2Z_{in}$ must be equal to the characteristic impedance Z_0 of the stripline to prevent reflections due to impedance mismatch.

Now consider the simplified circuit model shown in Fig. 3.1b. By feeding the waveguide in a single location the middle, the impedance parallel to Z_{slot} is now Z_{in} rather than $2Z_{in}$. This relaxes the requirement on the impedance of the slot, which now becomes $Z_{slot} \gg Z_{in}$. Z_{slot} is high when the slot is resonant. This makes intuitive sense: it essentially means that the slot couples to the waveguide more effectively at the frequencies at which it would radiate if the waveguide were not present.

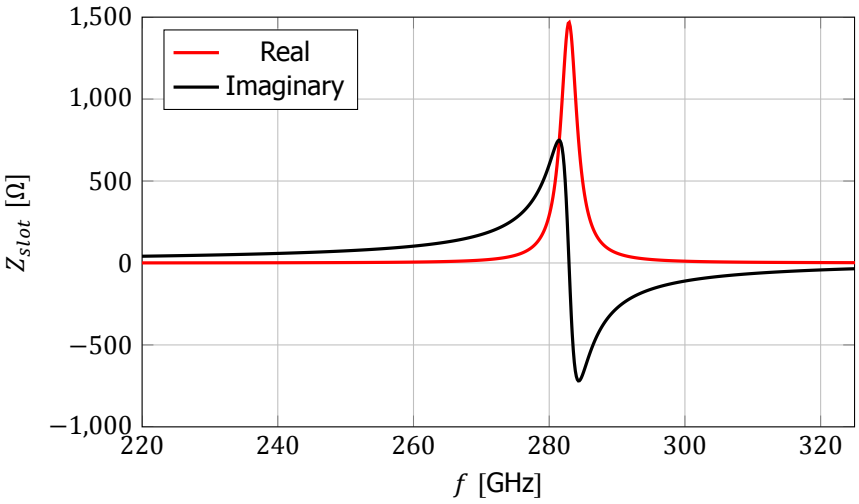


Figure 3.2: Real part (red) and imaginary part (black) of the impedance of the cavity-backed slot.

Keeping in mind the impedance of the cavity backed slot in Fig. 3.2, the real part Z_{slot} is only high over a very narrow bandwidth, which is typical for slots backed by very thin cavities. For this design, it is in fact the greatest limitation on the bandwidth of the transition. The imaginary part also shows narrow resonance behaviour, but less so, dropping to roughly $\pm 70j\Omega$ at the edge of the band. If Z_{in} can be made small compared to this value of $\pm 70j\Omega$, then the transition couples to the waveguide over the entire frequency band.

Furthermore, the structure shown in Fig. 3.1b is more robust to fabrication tolerances; if the structure from Fig. 3.1a is not perfectly symmetric, the waves arriving from either side of the metal may not join with the same phase, which hurts the performance. Lastly, fabrication itself is also made easier by having a single feed. When comparing Fig. 2.1a to 2.1b, it is clear that the former cannot exist without a slab holding it in its place, since the metal is floating and not attached to the waveguide walls. Accurate placement of this slab is then critical for the performance of the transition, and the electromagnetic properties of the slab itself affect the transition as well. It is for all of the above-mentioned reasons that for this design, a single feed guiding structure is used as in Fig. 2.1b, which is fed in the middle and tapers outwards towards the long sides of the waveguide wall.

3.2. Integrated circuit section

The integrated circuit section consists of a cavity-backed slot antenna (CBSA). The cavity exists to prevent fields from leaking into the silicon substrate and other areas of integrated circuit by completely shielding the signal by metal.

3.2.1. Cavity-backed slot antenna

The cavity-backed slot antenna is realised in the BEOL of the integrated circuit, using the bottom metal layer as the backing short for the slot, with the slot being in the top metal layer. The walls are implemented by means of via fences.

The main challenge in designing a CBSA on a chip for high-frequency CMOS processes is the narrowband characteristic as a result of the height h of the cavity being very small ($h = 12\,\mu\text{m} < \lambda/50$).

The type of slot used for the CBSA is H-shaped in order to prevent the guiding structure from covering any parts of the slot like in 2.11, while still having a relatively large resonance wavelength by extending the slot in the other direction. Other slot types such as a bow-tie, dogbone, and rectangular shaped slots, all observable in Fig. 3.3 have been been simulated as well, but the type of slot does not appear to change the performance of the entire structure.

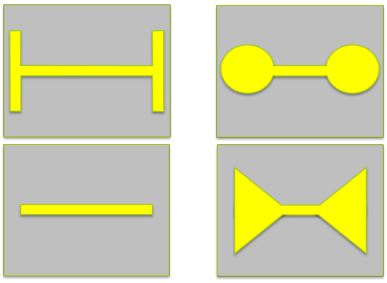


Figure 3.3: Possibilities for the shape of the cavity backed slot. The performance difference between each of the shapes is negligible.

The geometry of the H-slot can be seen in Fig. 3.4.

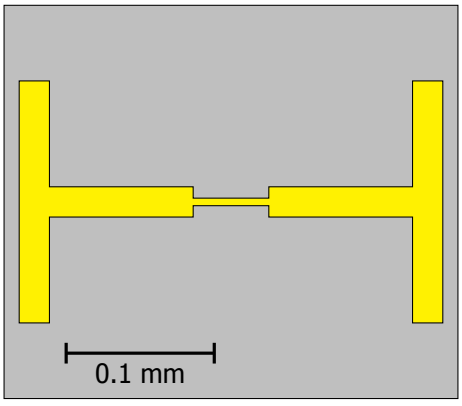
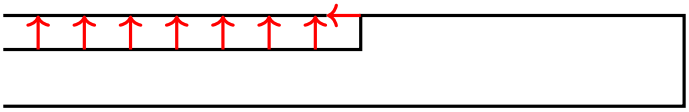


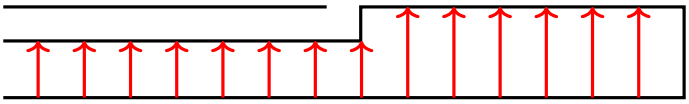
Figure 3.4: Top-view of the H-slot.

3.2.2. Slot feed

The slot is fed using a stripline in metal layer M5. The stripline is terminated with a quarter-wavelength radial stub. This quarter-wavelength stub is chosen instead of a shorting pin in order to prevent an unwanted resonance in the cavity. This resonance, shown schematically in Fig. 3.5b, occurs due to the short distance between the stripline and the cavity's bottom metal plane. Replacing the shorting pin by a quarter-wavelength stub dampens this resonance significantly, and it disappears completely when ohmic and dielectric losses are also taken into account.



(a) Preferable mode in which the stripline efficiently couples to the gap in the slot.



(b) Field orientation when the stripline couples to the cavity. This may happen when the stripline is terminated with a shorting pin.

Figure 3.5: Two different modes that are excited in the cavity are shown. Arrows indicate electric field orientation, not field strength.

The input impedance of the transition generally differs from the 50 Ω standard. A quarter-wave transformer section is used to match the input impedance of the transition ($Z_{in} \approx 20\,\Omega$) to a 50 Ω input.

Lastly, the 50 Ω stripline must be changed to a configuration where a grounded coplanar waveguide is on the top metal layer with the ground plane being the bottom metal layer. This configuration is the one that has the lowest losses possible for a given impedance, due to the fact that the top metal layer is relatively thick and has the best quality metal for transporting the signal to the terminals of the device to be tested

This stripline-to-coplanar waveguide (CPW) transition is done as shown in Fig. 3.7. While the signal approaches along the microstrip from the left, the conductor on the metal plane closes in to create a coplanar waveguide-like mode before the electric field flips as the signal-carrying metal changes layers to metal layer M5.

The stripline-to-CPW transition is preferably as close as possible to the cavity, so that the relatively lossy stripline is as short as possible. It cannot be arbitrarily close to the cavity, as the waveguide walls will then short the CPW and prevent any transmission. For this reason, the waveguide part is tilted, so that the part of the waveguide wall that is pointing towards the device under test is as far as

possible from the device, while still being able to provide mechanical stability for the waveguide, shown in Fig 3.6.

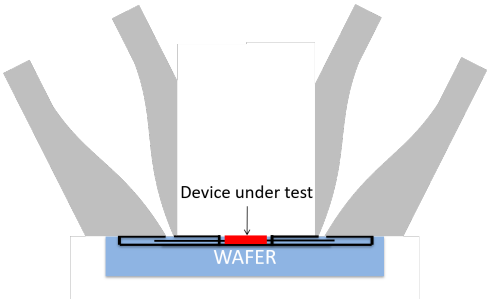


Figure 3.6: Schematic showing that if the probes are designed to be angled, the waveguide wall does not need to stick out towards the device under test, so stripline feeding the slot can be made shorter.

Figure 3.7: (a) Top and **(b)** side view of the stripline-to-CPW transition. On the left side, the CPW is in metal layer M6, with the ground plane being metal layer M1, on the right side, the stripline is inside the silicon oxide on metal layer M5.

The final feeding structure is shown together with the CBSA in Fig. 3.8.

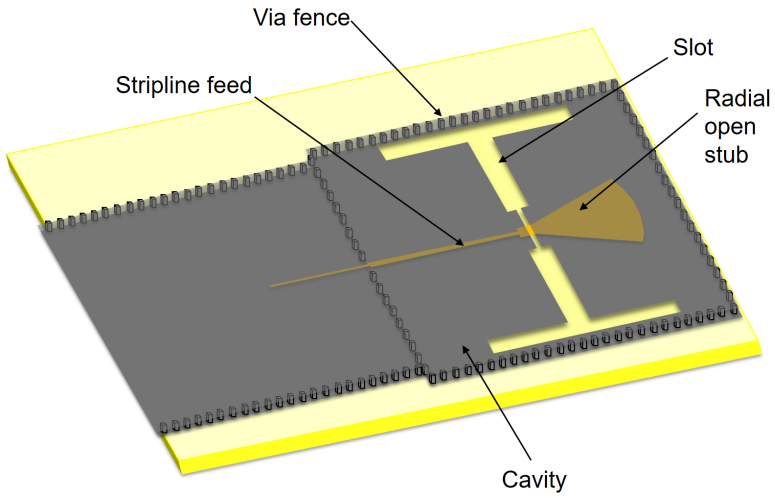


Figure 3.8: The complete feeding structure of the slot. The feed, the 50 Ω stripline, the quarter-wave transformer, and the radial stub are indicated in the picture.

3.3. Losses

The structure cannot be compared with other probing techniques without also assessing the losses. For a fair comparison, the losses of the entire structure should be taken into account, including the guiding structure, the cavity, and the microstrip feed leading to the 50 Ω microstrip on the top metal layer outside the cavity.

Metal layers 5 and 6 are 3 µm thick and made of aluminium ($\sigma = 3.67 \times 10^7$ S/m). All the other metal layers are made of aluminium as well. The cavity walls are modelled by a thick sheet of aluminium instead of via fences, in order to prevent unnecessary increase of computational load on the commercial electromagnetic software. The host structure, SiO_2 ($\varepsilon_r = 4.2$), is given a loss tangent $\tan\delta = 0.001$. This loss tangent is assumed constant over the entire frequency band. The guiding structure inside the waveguide section is modelled as being made of copper.

The resulting S_{12}-parameter is shown in Fig. 3.9. The structure achieves $S_{12} > -1.8$dB over the entire band. This result is an improvement over [20], where the S_{12} parameter varies between -2.1 dB and -2.8 dB in the desired band.
The unwanted cavity resonance present in the lossless curve at 313 GHz is seen to almost disappear in the lossy structure.

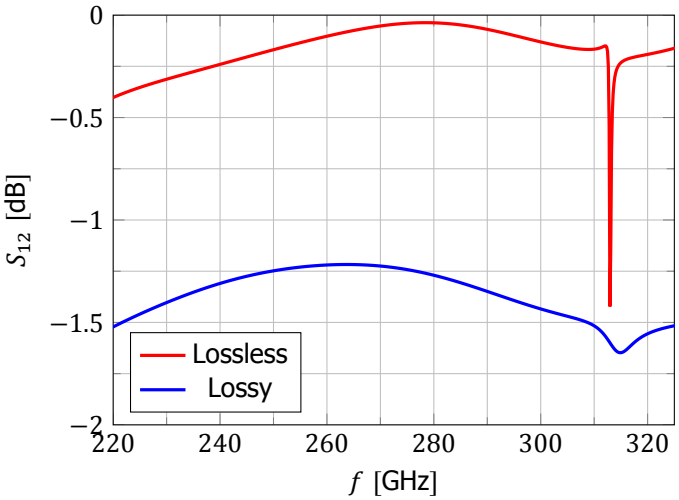


Figure 3.9: S_{12}-parameter of the entire structure with and without losses.

In order to study the origin of the losses, each loss mechanism (be it ohmic or dielectric) in the probe is enabled separately in the simulation software. The loss mechanisms are split into the following categories:

- Microstrip. This includes most of the feeding network including the radial stub, the quarter-wave transformer, and the feed.
- Cavity walls and bottom. These are the copper walls of the cavity and the bottom metal layer of the IC.
- Top metal layer.
- Guiding structure.
- All metals. This includes all of the above.
- Dielectric losses. These are the losses inside the SiO_2 host material.

The result of the loss study is shown in Fig. 3.10. In this plot, the loss (in dB) is defined as:

$$\text{Loss [dB]} = -10\log_{10}\left(|S_{11}|^2 + |S_{12}|^2\right) \tag{3.1}$$

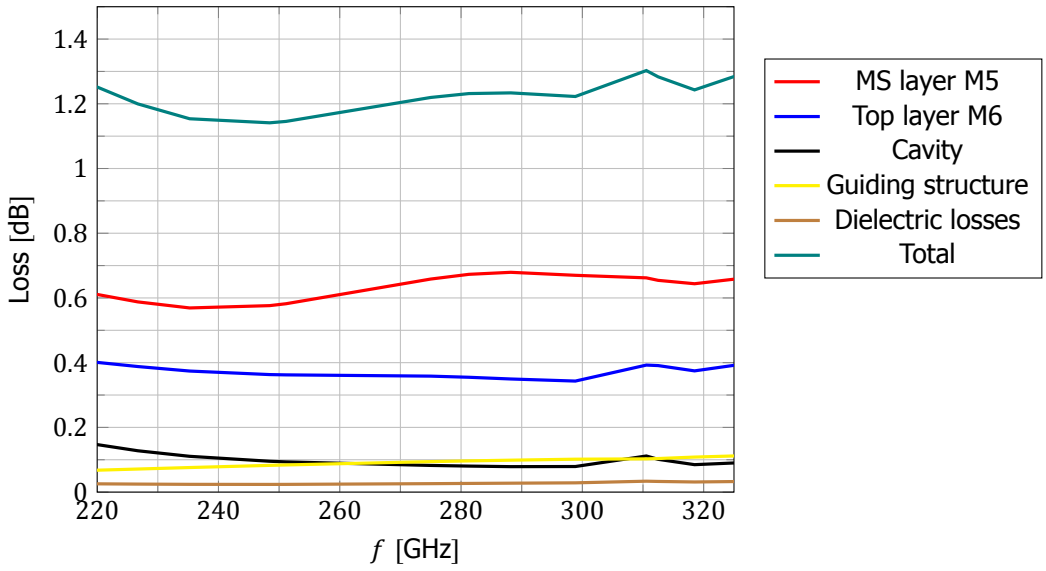


Figure 3.10: Plot showing the power lost due to either ohmic or dielectric losses versus frequency.

The figure clearly shows that the losses in the waveguide section are negligible. Most of the losses are due to the feed: the microstrip and stripline in combination with their ground plane. When looking to reduce losses, the geometry of the feed should be looked at first.

3.4. Usage in other frequency bands

Although the design and simulations are done for the 220-325 GHz band, the approach can be extended to other bands as well. By scaling all the frequency-dependent parameters with the wavelength (width and length of cavity, length of guiding structure, length of radial stub) and keeping all frequency-independent parameters (size of the gap between the metal parts of the guiding structure, width of the stripline, height of the cavity) identical, the same concept can be applied. The most notable parameter here is the maximum height of the cavity, which is constrained by the BEOL of the process that is used. When moving to higher frequencies, the height of the cavity relative to the wavelength will increase, which results in more wideband performance.

In order to test the performance at higher frequencies, the design was parametrised and simulated again for the WR-8, WR-3, and WR-2.2 waveguides and frequency bands, without any further tweaking of the values for optimisation. Losses were not included in this simulation. The result can be observed in Fig. 3.11.

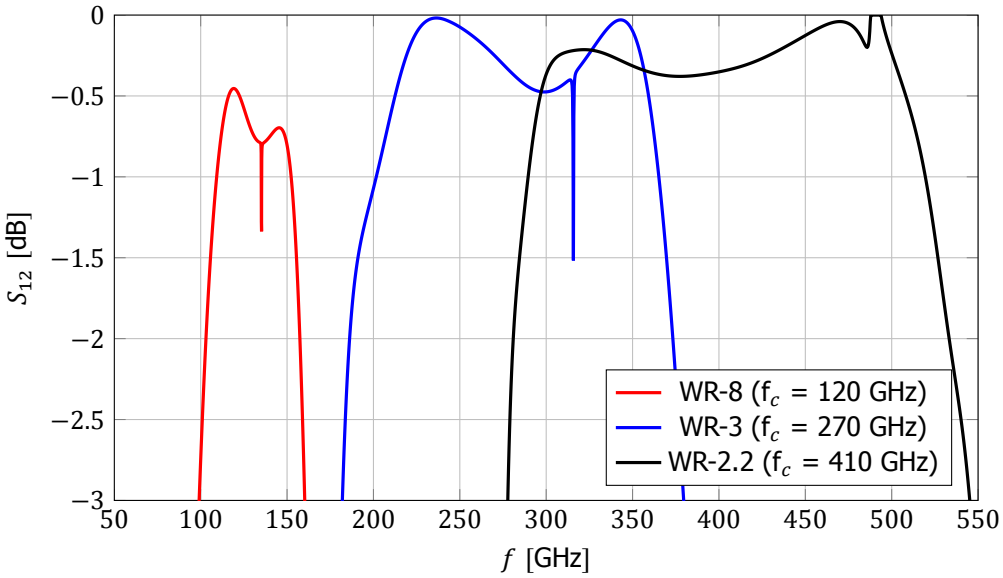


Figure 3.11: Lossless S_{12}-parameters of the parametrised design for three selected frequency bands, without further optimisation of the dimensions of the structure.

The most prominent thing that can be observed is the poor performance in the lower frequency bands. Although the transition was not originally meant to be used for these frequency bands where traditional probing methods achieve reasonable performance, this plot reinforces the idea that the height of the BEOL limits its use in these frequencies. At higher frequencies, where the height of the BEOL is relatively large, the transition has no issue covering the entire band of the WR-2.2 waveguide. It should be noted that the transition does not perform better at these frequencies if losses are taken into account, since losses increase with increasing frequency too.

An extensive list of the final parameters of the design and whether or not they were scaled to the frequency band can be found in appendix A.

4

Design verification and tolerances

The previous chapter focused largely on maximising the *transmissivity* and minimising the *reflectivity* of the transition. In this chapter, the effect of placement tolerances on the calibration accuracy will be studied by using 3D EM simulation software, thus providing a first order validation of the design process for the aimed application, i.e. mm-wave wafer level characterization.

4.1. EM validation

While transmissivity and reflectivity are very important aspect of a characterisation probe, they are not the only figures of merit. After all, the transitions leading up to the device terminal are in theory removed by an accurate calibration of the measurement set-up. This does not mean the transmissivity does not hold value at all. If the power transmitted through the device comes close to the noise floor of the measurement, even an accurate calibration procedure cannot salvage the result. This is because a low transmission implies a large multiplicative scaling factor from the calibration, which will also amplify the readout noise.

When examining the effect of inaccuracies such as displacement, it is not enough to study just the dependence of the transmission on these inaccuracies. For example, a displacement may significantly alter the phase response of the transition, without affecting the power that is transmitted, which can still heavily alter the result of a measurement. Thus, a new figure of merit is needed, which is called the worst case bound (WCB, also called error bound or upper bound), defined as:

$$\mathrm{WCB}(f) = \max_{i,j} |S'_{i,j}(f) - S_{i,j}(f)|, \tag{4.1}$$

where S' is the reference scattering matrix of the DUT, which will be obtained through direct simulation at the DUT terminals in this case and S is the scattering matrix of the DUT obtained after calibration with $i, j \in \{1, 2\}$.

The WCB gives the largest deviations between all the S-parameters for every frequency point, and was introduced in [23]. The WCB will be the main figure to characterise the quality of a calibration.

The calibration algorithm that is used here is the TRL algorithm [4], which requires three standards:

- a thru, directly connecting the planes of reference of the measurement.
- a reflect, a structure with a high reflection coefficient of which it is known whether it behaves like an open or like a short, placed at the reference plane.
- a line, a section of matched transmission line between the planes of reference.

The TRL algorithm requires only precise knowledge of the characteristic impedance of the line section that is used, which is extracted through 3D EM-based simulation. For the device under test (DUT) an independent line is used with length 600 µm.

If the probes are is positioned perfectly during calibration and measurement, the WCB should stay zero across the entire frequency band, numerical errors aside. A change in placement will then cause the S-parameters of the measurement to change, and in turn increase the WCB.

As an example, Fig. 4.1 below shows the WCB for perfect positioning on the calibration structures, but a misplacement in the z-direction (orthogonal to the planar chip environment) of 0.5 µm of both measurement probes. This means the tip of the waveguide containing the guiding structure if floating 0.5 µm above the slot.

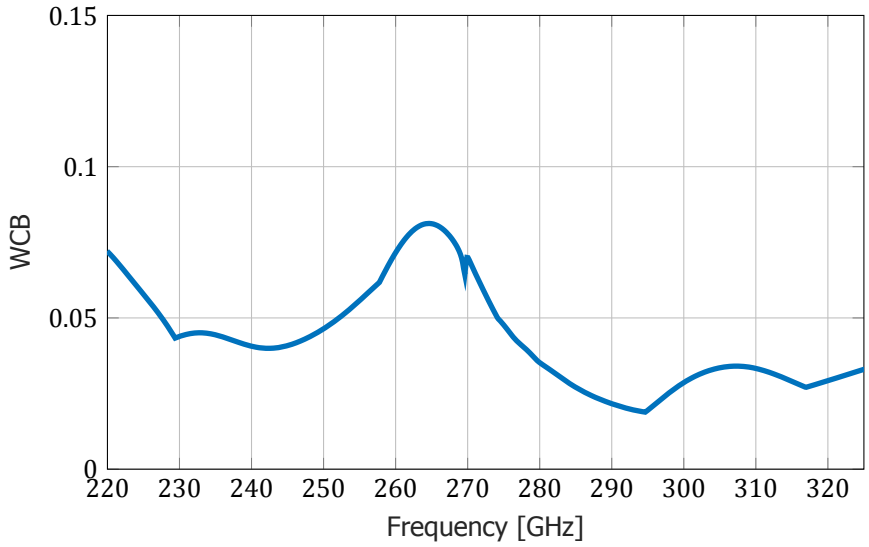


Figure 4.1: Example plot of the WCB showing the result of displacing both probes by 0.5 µm in the z-direction after non-displaced calibration.

4.2. Placement tolerances

In this section, the tolerance of the proposed probe to displacements in the x-, y-, and z-displacement are quantified. In order to show the displacement dependency of the WCB, the value is averaged over all frequency points and plotted against the displacement value. Again, the calibration is assumed ideal and non-displaced, and the probes are only displaced when measuring the DUT.

This mean value of the WCB plotted against x-, y-, and z-displacement is shown in Fig. 4.2, Fig. 4.3 and Fig. 4.4 respectively. X-displacement is along the long side of the rectangular waveguide, and y-displacement is along the short side of the rectangular waveguide.

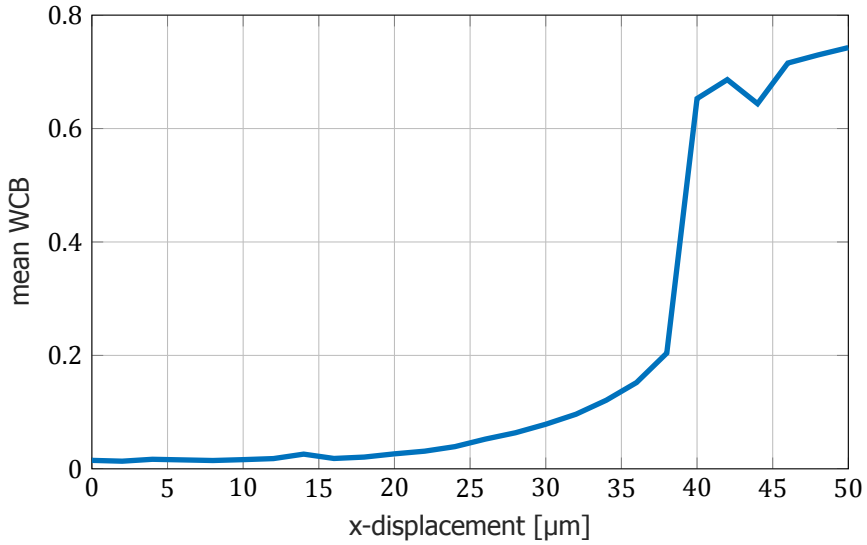


Figure 4.2: WCB versus x-displacement when simulating the measurement of the DUT. The curve is very well behaved until roughly 35 µm, when the curve shows a rapid increase.

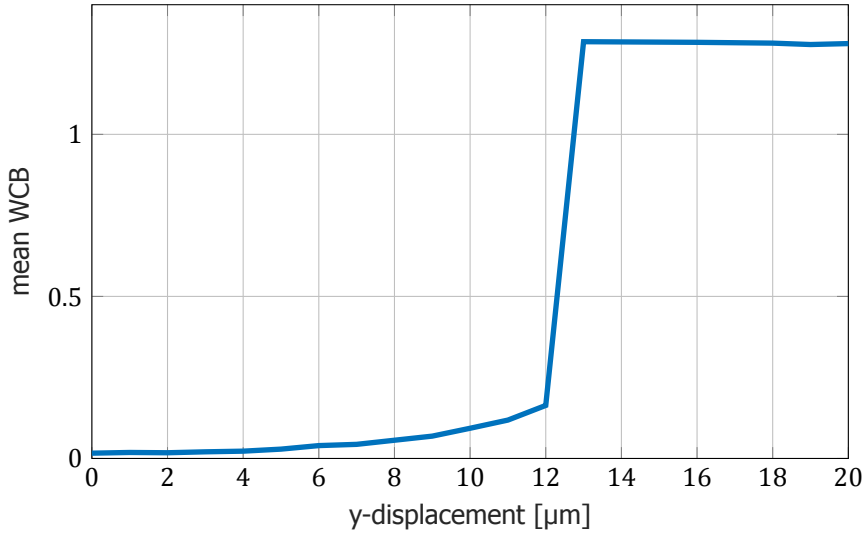


Figure 4.3: WCB versus y-displacement when simulating the measurement of the DUT. The curve shows a sudden jump at 12 µm due to shorting of the slot.

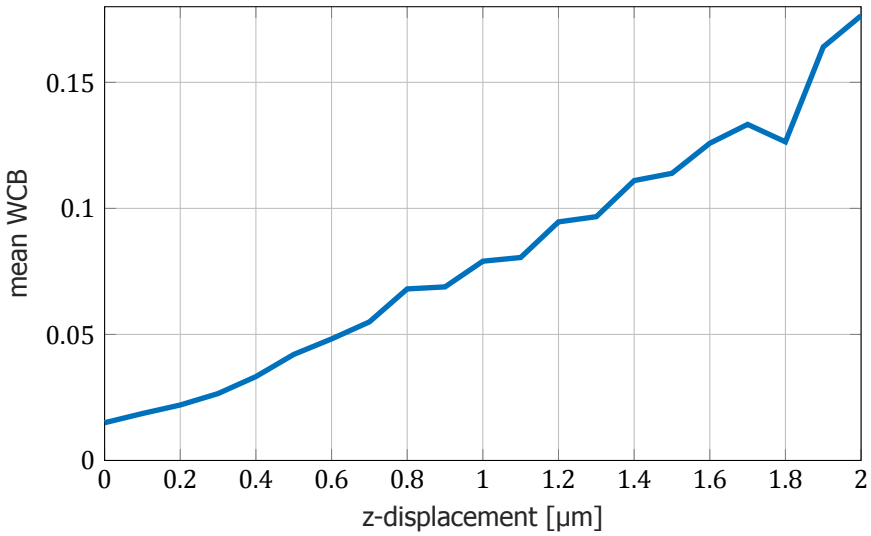


Figure 4.4: WCB versus z-displacement when simulating the measurement of the DUT.

Both the curve for the x-displacement and the curve for the y-displacement show a sudden increase at a certain displacement level, as opposed to the curve for z-displacement which shows a steady increase. This is due to the failure modes outlined in Fig. 2.11. When the probe is displaced too much in the x-direction, e.g. 35 µm in the considered example, the slot will resonate at a higher frequency due to part of it being shorted. This will not result in zero transmission, and might even increase the transmissivity at higher portions of the band. It will, however, change the resulting S-parameters of the measurement and render the it pointless. If the probe is displaced more than 12 µm in the y-direction, the feed of the slot is shorted and the transmission will drop to zero.

The above plots show only what will happen when the probes are displaced during measurement of the DUT. What would happen if the probes are displaced during each of the calibration steps? To quantify this, a simulation is done where each of the probes, during each of the calibration steps as well as during the measurement is given a z-displacement value which is uniformly distributed between 0 and 2 µm. When averaged over many calibrations, this should given an indication on how well the probe performs when a maximum displacement of 2 µm. The result is shown in Fig. 4.5.

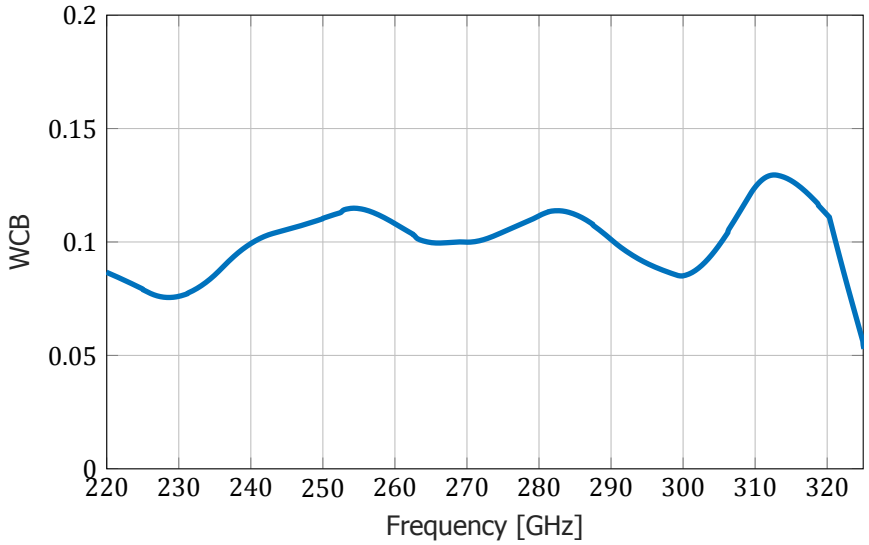


Figure 4.5: WCB verus frequency averaged for probes with z-displacements uniformly distributed between 0 and 2 µm during each of the calibration steps.

The WCB for this simulation is between 0.05 and 0.14 over the entire WR-3 band, and does not show any unusual extremities.

4.3. Conclusion

In this chapter, the effect of displacement tolerances on the measurement quality for the non-galvanic probe has been studied. The probe can be seen to be especially sensitive to displacements transverse to the plane of the slot; in a measurement where the probe hovers an average of 1 µm above the slot, the worst case bound averages 0.1 across the WR-3 frequency band. For comparison, in literature the WCB for this frequency range has been measured at 0.12 using conventional probing techniques [24]. The probe's intolerance to displacements in the plane of the slot is largely due to shorting of the slot by the metal of the probe tip. In order for the calibration quality to be in line with those of conventional probes, the displacements in this plane should not exceed 10 µm. This could prove to be challenging, given that the slot will be covered by the probe during measurement and not visible to an operator. Ideally, operation shall be automated to ensure placement that is precise enough to warrant the probe's use.

5

Layout design and simulation

An on-wafer calibration kit has been designed for a 0.25 µm SiGe process. The approximate layer stack for this process is shown in Figure 5.1. Two versions of the layout are made: one which conforms all the design rule checks (DRC) and will be taped out and sent to the foundry, and the other is a simplified version which will exported for use in commercial EM simulation software for verification. In the simplified version, all meshed surfaces and blocks are replaced by equivalent solid metal structures to reduce the computational load for the solver.

5.1. Floor plan

The die with the on-wafer calibration kit serves the purpose of allowing experimental verification of the non-galvanic probe. On the same die, there will also be a calibration kit for a standard WR-3 probe. Performing a measurement with both types of probe on the same die should illustrate the differences in calibration quality. The non-galvanic probe, being shielded from probe-to-probe coupling and without the problem of deformed landing pads or probe tips should give more consistent results. This is exacerbated when multiple landings are performed on the same calibration standard and the parasitics associated with the scratching of the landing pads worsen.

The die should then have the space to accommodate at least eight structures for a TRL-calibration experiment. For both the coplanar probe and the non-galvanic probe it should have: a thru, a reflect, and a line standard for the calibration, as well as a known DUT for verification. The DUT that is used here is a transmission line of length 320 µm between the planes of references of the calibration. This line is well defined as its characteristics can easily be extracted using a 3D EM-solver and its cross-section is the exact same as the one used for the thru and line standards.

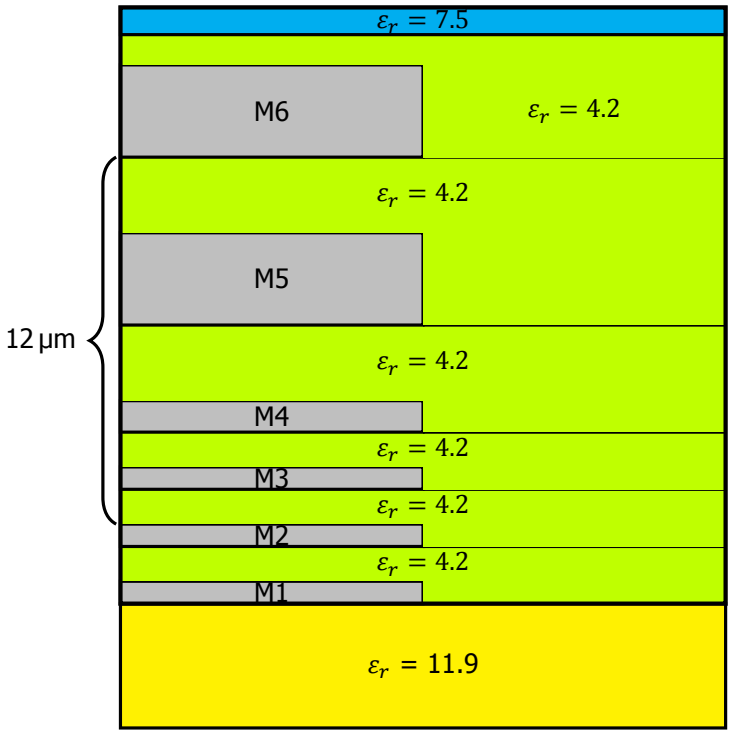


Figure 5.1: BEOL layer stack of the 0.25 µm process that was used. The silicon substrate on the bottom is 300 µm thick and out of scale. This is a typical SiGe BiCMOS stack for RF purposes.

Since the calibration standards for the coplanar probe are expected to suffer more from coupling through neighbouring structures, two verification lines are placed for this probe. One of the lines is placed on a location on the die where the surrounding real estate is more or less symmetric with respect to the centre of the structure, from now on referred to as ”symmetrically loaded”. The other is placed at the edge of the die, from now on referred to as ”asymmetrically loaded”. The asymmetrically loaded DUT is expected to behave in a less-defined way which should be reflected in worse calibration performance.

In order to gauge the transmissive properties of the non-galvanic probe, a power detector is also placed [25]. The power detector houses two test pads that connect to the termination of the line, so that the transmitted power can be calibrated and the transmission of the non-galvanic probe can measured. The remaining chip area is filled with power detectors for the coplanar probes.

The final floor plan of the die can be observed in Fig. 5.2.
It can be immediately observed that one large drawback of the non-galvanic probe

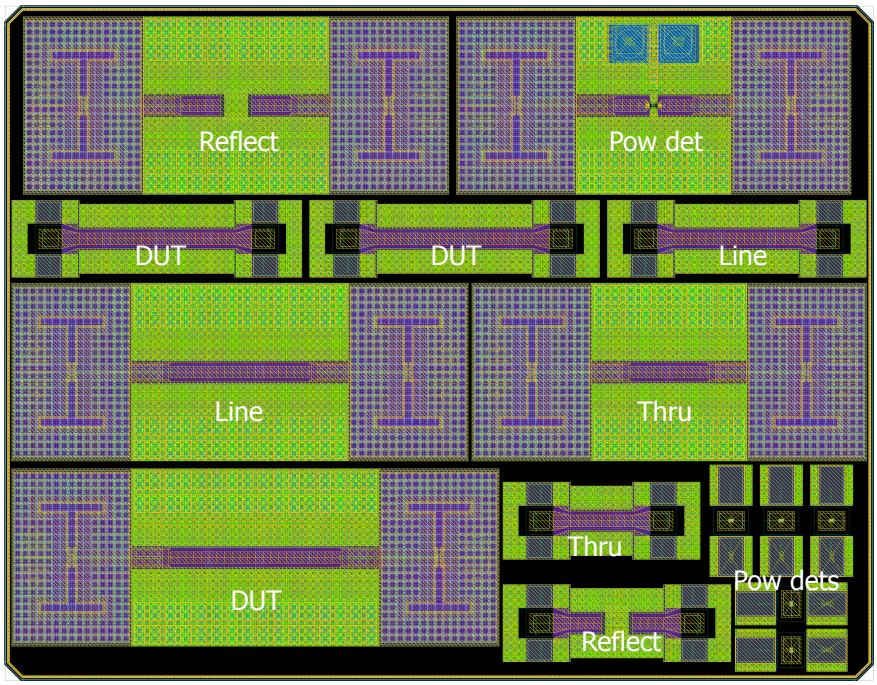


Figure 5.2: Floor plan of the die. The image is a screenshot of the GDSII file that is sent to be taped out.

pad is that the size of the on-wafer structures is large compared to those of the coplanar probe. As an example, the thru standard on the die is 510 x 200 µm^2 for the coplanar probe, compared to the 1020 x 450 µm^2 of the non-galvanic probe.

5.1.1. Calibration lines

The transmission line used for the calibration structures and the DUT is a grounded coplanar waveguide (CPWG), similar to the line used in [24]. The highest metal layer (M6) is used for the line, so as to minimise the metal losses in the line since it is also the thickest metal layer. The line is 30 µm wide, 3 µm thick, and the gap between the signal and side grounds is 10 µm. Metal layers 1 and 2 are meshed to form the ground plane. A cross section of the line is shown in Fig. 5.3.
The characteristic impedance Z_0 of the line is obtained through direct 3D simulation of the line, and through use of (5.1) presented in [26].

$$Z_0 = Z_{sys}\sqrt{\frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2}}, \tag{5.1}$$

where Z_{sys} is the reference impedance of the system, in this case the 50 Ω to which the excitation ports are set. Z_0 was left frequency dependent in the calculations,

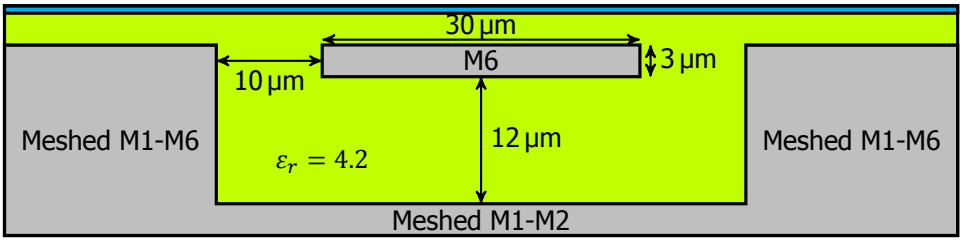


Figure 5.3: Cross-section of the line used in the test structures.

but was found to be an almost constant 33.5 Ω.

For both the non-galvanic and the coplanar probe calibration kits, the length of the thru line is 100 µm ($\approx \lambda/5$) between the nearest transition and the reference plane, to ensure that the mode at the plane of reference is the desired propagating mode. The line standard must be chosen so that the the phase shift of the line between the planes of reference is no less than 20° and no more than 160°. The line is chosen to be 160 µm long, which with the effective relative permittivity of 3.8 of the line translates to a phase shift of 82° at the lowest frequency in the band and 122° at the highest frequency. The reflects are shorts placed at the plane of reference which ensures that the sign of the reflect for the TRL algorithm remains constant throughout the entire band. The DUT is a line of length 240 µm between the planes of reference.

5.2. Landing pads

All calibration structures for the coplanar probes are equipped with aluminium landing pads. They are made to handle probes with a pitch of 75 µm for use in the WR3-band. In order to satisfy the process design rules, the signal pad is made 50 µm wide, which is wider than the 30 µm width of the CPWG central line. For this reason, a taper is introduced to reach the required width. This introduces additional mismatch and reflections, which will lower the dynamic range of the measurement. However, since the behaviour of the pads and the taper is all included in the calibration, this mismatch will not affect the goal of the experiment.

Additionally, the pads also employ a back short which connects the two ground pads. This back short is placed at a distance of 20 µm from the signal pad, and is made in an effort to reduce the coupling to nearby structures and achieve a performance of the coplanar probe which is as good as possible to use for comparison with the non-galvanic probe. A schematic of the landing pads can be observed in Fig.5.4.

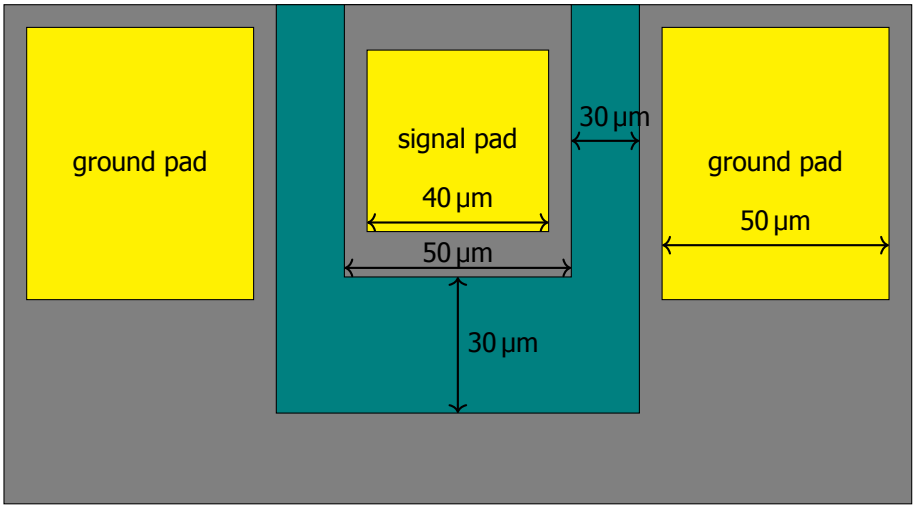


Figure 5.4: Schematic showing the most important dimensions of the landing pads for the coplanar probe. Grey shows the placement of metal, with the yellowing rectangles being the cuts in the nitride made for landing.

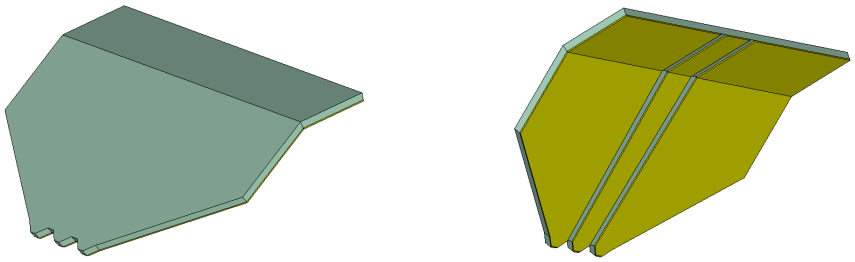
5.3. Simulation set-up

The simplified version of the chip layout is imported to CST, and all the metal layers are merged to a single object with a conductivity of 32 MS. This value is roughly equivalent to the average specified conductivity of all metal layers in the BEOL stack. Creating a single object significantly reduces the computational strain on the solver. In the simulation environment, the chip is surrounded by an air box from all sides which is terminated by a perfectly matched radiation boundary at a distance of 500 µm from the edges of the die.

No information has been found on the dielectric loss tangent of the silicon dioxide at this frequency; a conservative loss tangent of 10^{-3} was used. A mesh for the on-wafer calibration kit and each of the probes was made and kept unchanged throughout each of the simulations.

5.3.1. Coplanar probe tip model

A model of an RF probe tip was used for simulation of the coplanar probe calibration structures. The probe tip is coplanar waveguide with a characteristic line impedance of 50 Ω. The line is 650 µm in length, covered by a silicon ($\varepsilon_r = 11.9$) substrate and the pitch of the tips is 75 µm. The probe is visually similar to the probe shown in [27], but the transition to a coaxial waveguide is not included. Instead, the probe tip is directly excited by a modal waveguide port at its termination.



(a) (b)

Figure 5.5: Top view (a) and bottom view (b) of the 3D Model of the coplanar probe.

The probes are placed precisely on the centre of the landing pads, touching the top metal layer of the chip.

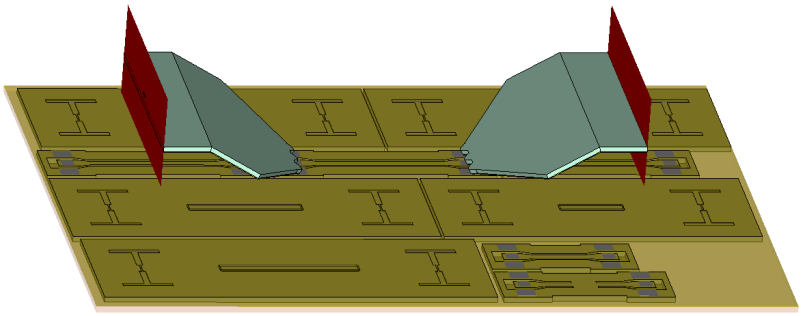


Figure 5.6: 3D model of the entire simulation using the coplanar probe. The (modal) excitation ports of the coplanar probe are shown in red.

5.4. Non-galvanic probes

The non-galvanic probe model used in the simulation is of the tilted probe without a dielectric in between the metal parts. Its walls are modelled as a metal sheet, and the probe is excited by a waveguide port at the top. The simulation geometry for one of the calibration structures is shown in Fig. 5.7.

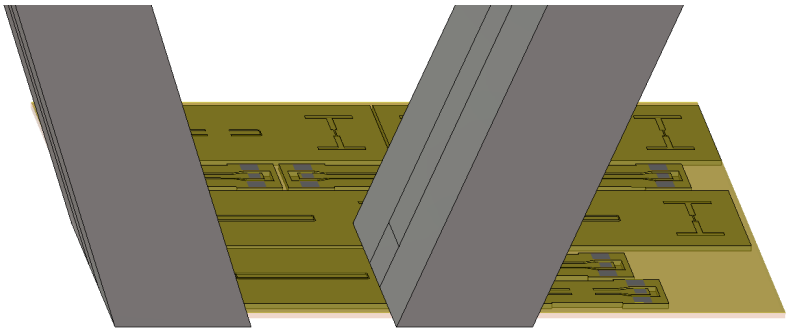


Figure 5.7: 3D model of the die and non-galvanic probe used in simulation.

It should be noted that the opening of the waveguide is larger than the cavity on-chip. While both the slot and the long side of the waveguide are made to resonate at $\lambda/2$, the cavity is filled with a dielectric (ε_r = 4.2) so that it is smaller. The calibration structures on the chip are packed very closely together, in order to minimize the area used by the calibration kit. As a result, the opening of the non-galvanic probe covers more than just the calibration kit structure which it is placed on. If energy from the probe couples to other structures, it may hamper the calibration accuracy. Though direct simulations done on the isolated non-galvanic probe suggest that the probe tip is insensitive to what takes places outside of the narrow feed, the effect may become more pronounced in a calibration. The size of the waveguide opening relative to the cavity on the slot can be seen in Fig. 5.8.

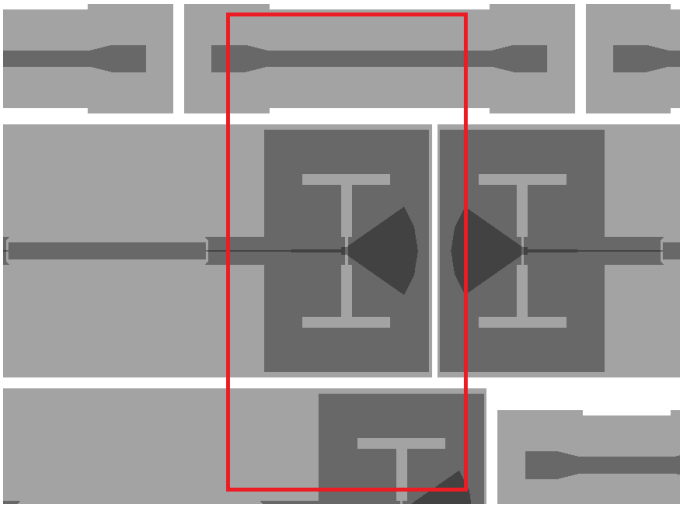


Figure 5.8: Schematic figure showing the relative size of the waveguide cross-section (red rectangle). The opening covers more than just the structure it measures, extending to other structures on the same chip.

5.5. Simulation results

The results of the calibration are shown in Fig. 5.9, where the WCB is plotted against a frequency for three calibration simulations.

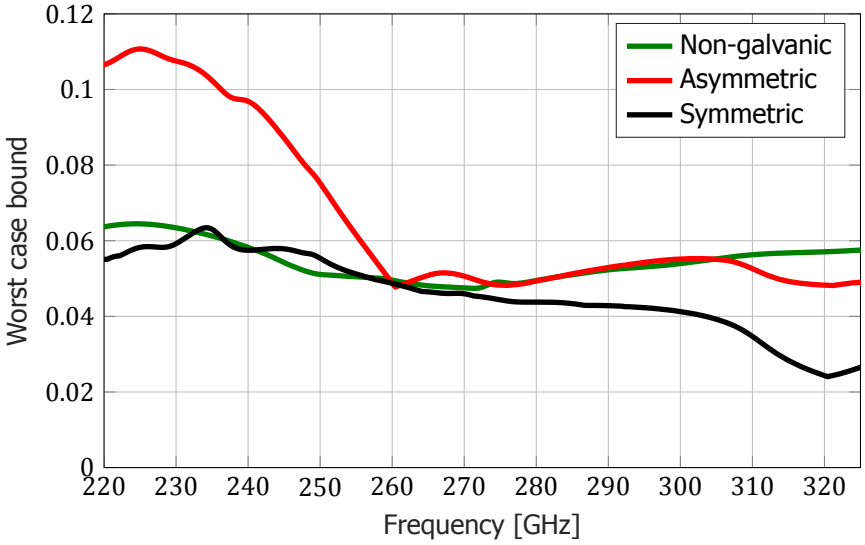


Figure 5.9: Worst case bound against frequency for the non-galvanic probe (green), the coplanar probe with the symmetrically loaded DUT located in the middle of the chip (black), and the coplanar probe with the asymmetrically loaded DUT located at the edge of the chip (red).

The first thing that stands out is that the asymmetrically loaded DUT performs worse than the symmetrically loaded DUT over the entire frequency band. Most notably, the asymmetric DUT has a a large 'bump' in the calibration inaccuracy in the lower portion of the band, not present in the other simulations. A contour plot of the electric field, depicted in Fig. , highlights the reason for this discrepancy. As expected, the coplanar probe shows significant coupling to the substrate, which is different for the two differently placed DUTs.

Furthermore, the calibration with the non-galvanic probe does not outperform the symmetrically loaded coplanar probe, despite the expectation that the unshielded coplanar probe tips suffer more from coupling to nearby structures. Crucially, the probe performance is degraded when compared to a calibration simulation on isolated structures, such as in Fig. 4.4 where a mean WCB of 0.015 was obtained compared to the mean WCB of 0.057 in the simulation of the calibration with surrounding structures.

Evidently, the effect of placing the structures so close together that the waveguide covers other structures on the same chip, shown in Fig. 5.8 is enough to noticeably

degrade the performance of the non-galvanic probe. This suspicion is confirmed by viewing the electric field distribution of the chip during one of the measurements steps, shown in Fig. 5.10.

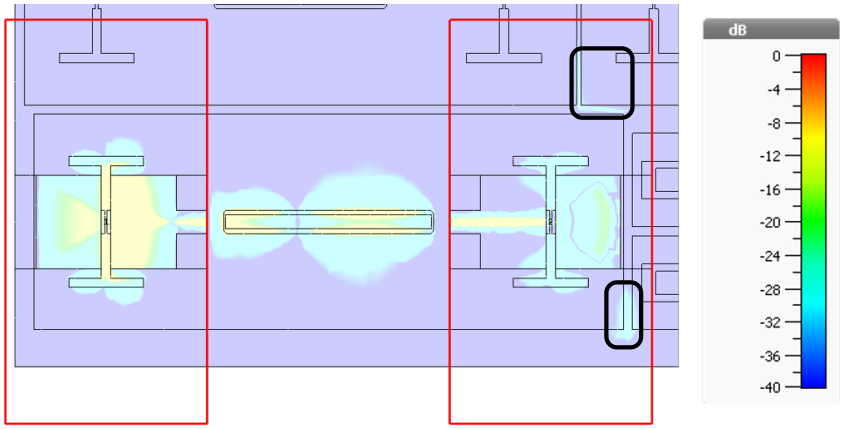


Figure 5.10: Electric field distribution on the die during simulated measurement of the DUT. Undesired excitation of fields can be observed in surrounding structures. Red outline shows the footprint of the waveguide, black outlines show the undesired excited fields.

To mitigate this effect, an area on the die should be reserved at least as large as the opening of the waveguide for each landing location of the non-galvanic probe. This amounts to 0.864 x 0.432 mm^2 in the WR-3 frequency band for each landing spot.

5.6. Isolated comparison

Although the non-galvanic probe performs slightly worse than the coplanar probe across almost the entire WR-3 band, the performance is expected to be better in an isolated comparison where the surrounding structures on the chip are removed and the area around the cavities of the non-galvanic calibration kit are controlled, so that no coupling to surrounding structures takes place. Probe-to-probe coupling will still be possible in the case of the coplanar probe, which is assumed to be the greatest source of inaccuracy of the calbration. The results of this comparison is shown in Fig. 5.11.

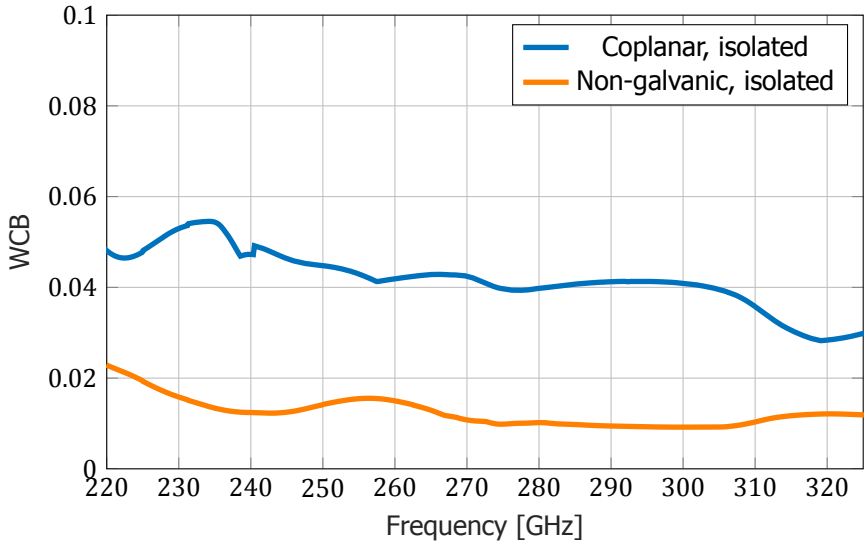


Figure 5.11: Comparison of the WCB of the coplanar probe and the non-galvanic probe of the calibration lines and DUT without the presence of surrounding structures.

As is expected, the WCB of the non-galvanic probe on a calibration kit without surrounding structures is lower than that of the coplanar probe. The WCB of the coplanar probe did not significantly decrease compared to the calibration and measurement of the symmetrically loaded line in Fig. 5.9.

6

Conclusion

In this thesis, a design for a chip-to-waveguide transition for use in mm-wave probes is presented, and commercial 3D electromagnetic solvers have been used to verify its performance.
In chapter 2, all the design steps have been layed out that were used to reach the proposed design. The transition comprises a tapered structure at the tip of an open-ended waveguide to transform a TEM mode to the fundamental TE mode of the waveguide. The signal is coupled through a resonant on-wafer slot backed by a cavity. Despite the inherently narrowband behaviour slot, the transition achieves $S_{12} > -1.8$dB over the entire bandwidth specified for the WR-3 waveguide (220-325 GHz). The limitation of the bandwidth is caused mostly by the electrically thin cavity; if the same transition is designed for a higher frequency, the relative bandwidth increases. The dominant source of losses are those of the on-wafer structure, where the stripline and slot account for over 70% of all losses in the transition.

In chapter 3, the design has been verified in a simulation of a calibration procedure, of which the results as well as a tolerance study are shown The main tolerances which are discussed are a displacement of the waveguide in the x, y, and z-direction with respect to the center of the cavity-backed slot. The figure of merit used in the worst case bound. The transition showed good resistance to lateral (x or y) displacement, but failing when the metal at the tip of the waveguide shorts covers part of the slot due to displacement. The performance deteriorates when the waveguide is displaced vertically, reaching a WCB of 0.1 when for a z-displacement of 1.3 µm, while it is 0.17 when no displacement is taken into account.

In chapter 4, the implementation of the chip layout is presented. The die contains a calibration kit for TRL-calibration of the non-galvanic probe as well as for a standard coplanar probe. Because the non-galvanic transition is completely shielded, it should be unaffected by loading due to nearby structures. To exemplify this, the calibration kit for the coplanar probe contains two identical devices for testing, but

loaded differently.

In chapter 5, the expected results of a measurement on the chip are shown by comparing the performance of the presented design with that of the coplanar probe. The simulation predicts a WCB averaging 0.06 for the non-galvanic probe, significantly higher than the 0.17 that was simulated in the isolated measurement in chapter 3, which did not take the neighbouring structures into consideration. A field monitor of the die showed that the non-galvanic probe still coupled to nearby structures because the relatively large open-ended waveguide covered more than just the cavity it is meant to couple to. This is expected to be the reason for the discrepancy with the results of chapter 3. To combat this, one would have to reserve an area for each landing location on-chip which is equal or larger than the cross-section of the waveguide. For the coplanar probe, there was a significant difference between the symmetrically and asymetrically loaded device, with the symetrically loaded device performing better than the non-galvanic probe.

While the transition promises to be more robust and have better performance than contemporary industry-standard probing techniques, it comes with a drawback of requiring significantly more chip area. In the layout of the chip presented in chapter 4, the size of the thru standard for the non-galvanic probe was $1280\,\mu m^2 \times 460\,\mu m^2$ compared to the $440\,\mu m^2 \times 280\,\mu m^2$ of the coplanar probe thru standard. This makes the novel concept more fit for use in higher frequency bands, where the resonant wavelength of both the cavity-backed slot and the waveguide are smaller. For future work, more research can be done into miniaturizing the waveguide to combat this drawback.

Fabrication of the probe is difficult, due to the small features of the tip for which no straightforward method is available. One promising technique is 3D stereolithography, where a photosensitive polymer is shined by lasers to create a print with high resolution. The accuracy of this technique can be appreciated in Fig. 6.1 which shows a microscope image of the tapered structure produced by this technique.
If this print can be metallised, it can be placed into a metal holder which would constitute the larger part of the probe, as shown in Fig. 6.2.

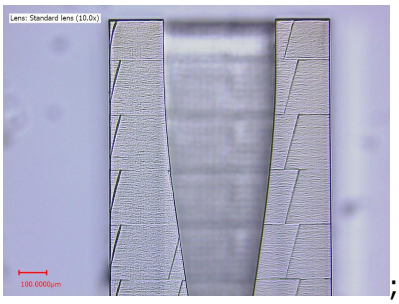


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Figure 6.1: A microscope scan of the tip of the waveguide, containing the tapered guiding structure, printed by means of 3D stereolithography.

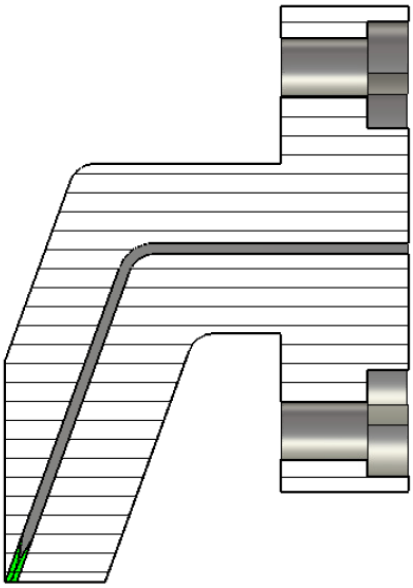
;

Figure 6.2: A cross-sectional view of the holder including waveguide flange that would case the tip.

A

Parameters

Table A.1: List of parameters used for simulation of the transition for the 220-325 GHz band, description of the parameters, and whether or not they should scale proportionally to the wavelength if the design is used for a difference frequency.

Parameter	Dimension [mm]	Description	Frequency scaling
l_g	2	Length of the guiding structure	yes
gap	0.02	Gap between metal parts of guiding structure	no
w_g	0.20	Width of the guiding structure	no
w_{cavity}	0.44	Width of the cavity (parallel to the long side of the RWG)	yes
l_{cavity}	0.30	Length of the cavity (parallel to the short side of the RWG)	yes
h_{cavity}	0.012	Height of the cavity	no
l_{slot}	0.28	Total length of the H-slot (parallel to the long side of the RWG)	yes
w_{slot}	0.16	Total width of the H-slot (parallel to the width of the RWG)	yes
w_{cuts}	0.02	Width of the slot cuts, outside of the feed part	yes
l_{feed}	0.05	Length of the feed part of the slot (along the slot)	no
w_{feed}	0.005	Width of the feed part of the slot	no
w_{sl}	0.013	Width of the stripline where it crosses the slot	no
r_{stub}	0.13	Radius of the radial stub	yes
ang_{stub}	70 [°]	Angle of the radial stub in degrees	no
h_{sl}	0.007	Distance from the groud plane (M2) to the strip line	no
t_{sl}	0.003	Thickness of the stripline metal	no
w_{qwave}	0.008	Width of the quarter-wave stripline	no
w_{fl}	0.004	Width of the stripline matched to the CPW	no

B

Layout generation

When transfering the original intended design to a layout that is sent to the foundry, some changes must be made due to the certain design rules outlined in the process' development kit. These rules can encompass parameters such as the maximum width of the metal patches, minimum spacing between two neighbouring metals, and minimum or maximum density of metal in a layer. To ensure that the entire layout satisfies these rules, the structures on the chip are made out of tiles that pass the design rule checker (DRC).
The unit cell of the tiling pattern is shown Fig. B.1. For subsequent layers, the unit cell is shifted half a unit vector in the x-direction as well as in the y-direction, and vias are placed in the intersections. When these tiles are repeated periodically, a metallic mesh is created of which the electromagnetic behaviour is similar to that of a solid block of metal.

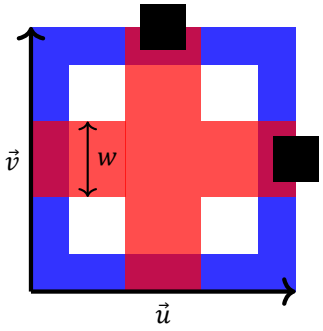

Figure B.1: Schematic of the square unit cell for tiling two subsequent layers, blue and red. Black shows the vias interconnecting the metals. The red metal is shifted $+\frac{1}{2}(\vec{u}+\vec{v})$ with respect to the blue metal, where $\vec{u}$ and $\vec{v}$ are the two unit vectors for the pattern. The minimum value of the dimension w is determined by the design rules. The length u of the unit vectors must satisfy $\frac{(u-w)^2}{u^2} > 1-\rho$, with ρ being the maximum metal density of the layer.

The size u of the unit cell is chosen so that the w is at least as large as the minimum metal thickness according to the design rules, and the density of the metal is made equal to the maximum allowed metal density. The size of the unit cell is then rounded up to a suitable number which is a divisor for many other numbers, such as 2, 5, or 10 µm. In this implementation, the unit cell size of the bottom metal layers is 5 µm. The unit cell size of the top metal layers, which use different design rules, was set to 20 µm. The final unit cell containing all of the process' layers is shown in Fig. B.2

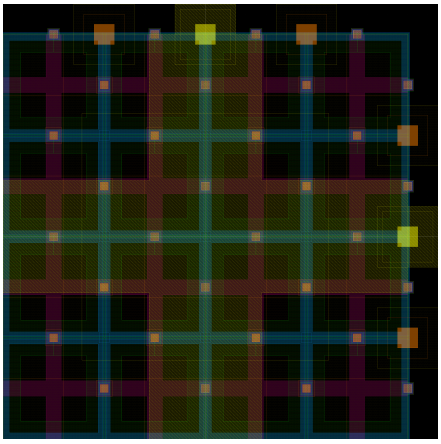

Figure B.2: Screenshot of the unit cell used where solid metal equivalent is required in the design, as shown in the layout generation program. This unit cell comprises all of the process' metal layers.

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