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Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology,
by the authority of the Rector Magnificus, prof. dr. ir. T.H.J.J. van der Hagen,
chair of the Board for Doctorates,
to be defended publicly on Tuesday 22 April 2025 at 15:00 o'clock

By

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Born in Changchun, China.

This dissertation has been approved by the promoters

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If the mountain will not come to me
Then, I will go to the mountain

Contents

Summary

The future power grid must accommodate large-scale integration of variable renewable energy sources. Power electronic (PE)-based components, e.g. converters, will play an essential role in the operation of the power system. However, the harmonics and transients generated by these PE-based components can significantly affect the lifetime and reliability of various power system components. These disturbances, particularly harmonics and transients, are challenging to eliminate. Thus, a more effective strategy is to assess the effects and enhance the durability and performance of the system components. To ensure the reliability of critical system components, these should meet stringent specifications and undergo rigorous testing prior to installation. Using a modular cascaded H-bridge (CHB) based high-voltage arbitrary waveform generator (HV-AWG), capable of replicating the dielectric stresses induced by PE components, enables a more accurate assessment of component resilience under operational conditions.

The CHB-based HV-AWG can be divided into several submodules; each module consists of three key components: a driver, a medium-frequency transformer, and an H-bridge equipped with HV rectifiers. Although various types of HV-AWGs exist, the modular CHB-based HV-AWG excels due to its superior high-voltage capability, broad operating frequency bandwidth, simple topology, compact size and low manufacturing costs. To successfully realize the CHB-based HV-AWG design, several technical challenges must be addressed, including the development of the insulation system for the medium-frequency transformer and the design of the high-voltage switch within the H-bridge.

The objective of the PhD project is to design and prototype a CHB-based HV-AWG, aiming for testing the insulation specimens of HV system equipment at voltages up to 8 kV to further enhance the power grid reliability. The primary functions of this prototype are outlined as follows: The CHB-based HV-AWG starts with a low-voltage (LV) DC input, which is supplied to the ZVS driver. The ZVS driver employs a soft-switching technique to drive a medium-frequency transformer, whose primary function is to elevate the input voltage to the required level. The transformer's output is rectified, generating a high-voltage DC (HVDC) output that serves as input for the HV H-bridge. The HV H-bridge then converts this HVDC input into HV pulses, which can be manipulated and controlled via a sophisticated algorithm that cascades the HV pulses to generate a variety of desired waveform shapes. This scalable modular approach, along with the precise control of pulse generation, enables the HV-AWG to create complex waveforms suited for various applications.

The main scientific challenges associated with the realization of a modular cascaded H-bridge-based high-voltage arbitrary waveform generator are:

- **Medium Frequency Transformer Design** with the considerations of trans-

former insulation material and winding configuration selection and transformer secondary design: To ensure sufficient creepage and clearance between the transformer windings, a split-winding configuration is implemented, where the windings are distributed across the two limbs of a U-U core. This configuration allows for more insulation materials between the windings. The secondary winding employs a disc-winding arrangement to enhance its high-voltage capability. Furthermore, an isolation turn is introduced between adjacent winding discs to mitigate the risk of disc-to-disc discharges. Based on Novo-control measurement method, the insulation dielectric properties are measured. After the analysis of the dielectric properties of various insulating materials, including transformer oil, silicone oil, epoxy resin, and silicone rubber, the heat-resistant TFC silicone rubber is selected for the construction of the transformer's insulation system.

- **HV H-Bridge Design** with the considerations of power-electronic component selection, HV gate driver design and the voltage sharing of the series-connected MOSFETs. To build the HV H-bridge, SiC MOSFETs are generally preferable owing to their superior performance in high-temperature environments, lower on-resistance, reduced switching losses, and enhanced thermal conductivity. However, SiC MOSFETs have a maximum blocking voltage limitation of 3.3 kV. To meet higher voltage demands, the most straightforward and effective approach is to connect multiple SiC MOSFETs in series. This introduces the challenge of unbalanced drain-source voltage sharing. The voltage balancing techniques — such as gate balancing core method, improved RC snubber methods, and optimized zener clamping method can mitigate this as is demonstrated in this thesis, which is verified by LTSpice simulations. However, they introduce additional costs and result in a bulky prototype due to the need for auxiliary components.

  For the prototype, Si MOSFETs, which can offer a maximum blocking voltage of 4.5 kV, are used. To further accommodate high voltage requirements, isolated gate drivers are replaced by non-isolated gate drivers and optocouplers. This modification allows the high voltage to be shifted away from the insulation system of the isolated gate driver to the optocoupler.

Based on the performed research on the key components, a three-stage modular CHB-based HV-AWG prototype, capable of producing a maximum output voltage of approximately 8.1 kV is realized, constrained by the insulation limits of the optocouplers and DC/DC converters. The generator can produce a variety of waveform shapes, including pulse, sawtooth, and stair patterns by modifying the control algorithm of the HV-AWG. This arbitrary waveform generator serves a platform for insulation samples' aging tests at TU Delft HV lab. To enhance the scalability of the HV-AWG, future research includes cascading the HV H-bridge submodules using fiber optics and integrating control through advanced platforms such as the Typhoon HIL system. Additionally, replacing the medium-frequency transformer with a planar transformer can be considered to achieve a more compact device design.

Preface

During the journey of research, I had a thousand of thoughts to quit. Luckily, I also had a thousand and one thoughts to continue.

Weichuan ZHAO
Delft, July 2024

1

Introduction

1.1. Background

The global economic growth has intensified concerns about the availability of the resources and environmental sustainability, both of which are emerging as significant barriers to the energy transition and sustainable development. The climate change and massive utilization of fossil fuels present a major challenge of achieving a sustainable energy power system. Consequently, the energy sector is undergoing a major global shift, moving from traditional fossil-based energy production to renewable sources such as wind, solar, bioenergy and hydropower, illustrated in Fig. 1.1 [1]. Also, electricity consumption is rising exponentially owing to the increasing electrification of transportation, such as electric vehicles and industry. As a result, the demand for a greener, more affordable, and more accessible high-voltage (HV) power system is expected to gain significant momentum over time.

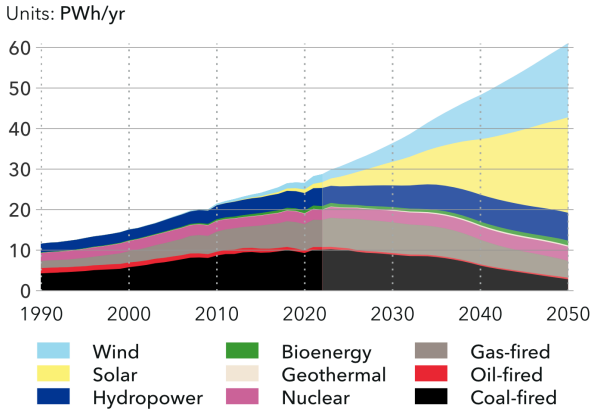

Figure 1.1: World grid-connected electricity generation by power station type [1]

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As a large number of renewable energy sources are integrated into various levels of the power grid – HV for generation layer, medium voltage (MV) for transmission layer, and low voltage (LV) for consumption layer, as shown in Fig. 1.2, there will be a substantial growth in the use of power-electronic (PE) based converters for electric power conversion (e.g. DC-to-AC, AC-to-DC), which will gradually dominate the grid. However, due to the fast switching (high $\mathrm{dv/dt}$ and $\mathrm{di/dt}$), the PE-based modules will generate a significant amount of high-frequency (HF) harmonics, voltage transients and steep current spikes, which create new electric field stresses on the insulation systems of HV components. Thus, the HV equipment insulation can degrade faster and jeopardize the reliability of grid assets.

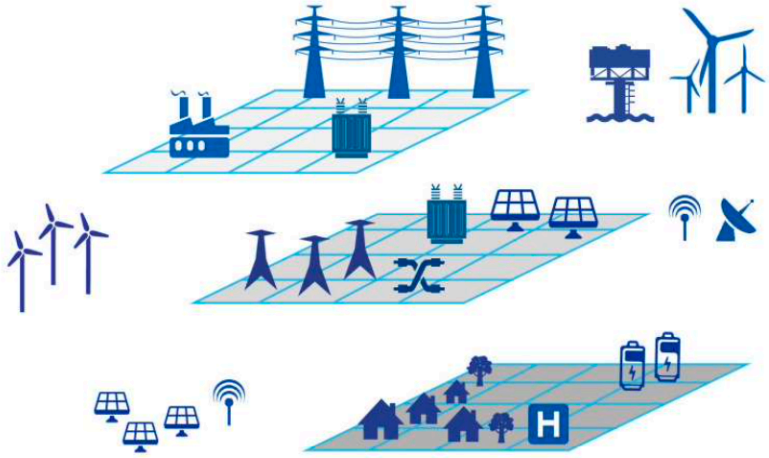

Figure 1.2: Renewables in different power grid layers (DNV energy transition outlook 2023)

It is commonly known that the mitigation of these harmonics, transients, spikes and oscillations is complicated because of the unavoidable parasitic parameters present in the PE based converters, which can rapidly charge or discharge owing to the solid-state switching and HF circulating current harmonics [2]. The most economical and practical solution is to improve the insulation quality of the HV components. Before installation, these HV components should be tested under specific and customized HV and HF field strength, which is similar to that occurring in the real power grid. A reliable HV arbitrary waveform generator (HV-AWG) that has the capability to generate such required test signal is highly-required for insulation testing.

The PhD project general objective is to enhance the reliability of HV system components in future power grids by testing their insulation systems under realistic dielectric stress conditions. The specific objective is to design and prototype a modular cascaded H-Bridge (CHB) based HV-AWG for testing the insulation specimens up to 8 kV. The design guidelines will address all critical factors relevant to the full-scale implementation of the HV-AWG. The prototype will consist of three compact

submodules, facilitating ease of integration and storage. Additionally, the expected output performance and the associated control system will be demonstrated.

1.2. HV Arbitrary Waveform Generator Topologies

Nowadays, with concerted effort, the researchers worldwide have already provided a number of effective approaches for the realization of the HV-AWG, which are listed below. Detailed explanation and comparison of these methods will be provided in Chapter 2.

- The use of commercial-available function generator and HV Trek amplifier
- Non-modular cascaded H-bridge based HV-AWG with medium-frequency transformer (MFT)
- Modular cascaded H-bridge based HV-AWG with MFT
- Modular multilevel converter [3]
- Modular cascaded H-bridge based HV-AWG with flyback supply [4] and [5]
- Modular cascaded H-bridge based HV-AWG with boost supply [6]

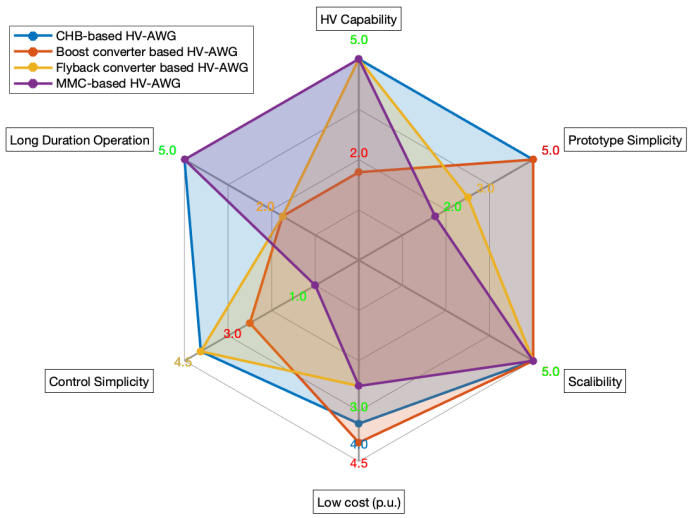

Figure 1.3: Comparison of different HV-AWG topologies

These HV-AWG topologies can be evaluated according to six different criteria: High-Voltage Capability, Prototype Simplicity, Scalability, Low Cost per Unit, Control Algorithm Simplicity and Long Duration Operation Capability. The comparison results are summarized in Fig. 1.3.

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Fig. 1.4 illustrates the schematic of the envisioned modular cascaded H-bridge based HV-AWG with 2 stages, highlighting three critical components: MFT, standard H-bridge or zero-voltage switching (ZVS) driver, and HV H-bridge. To fulfill the design of these components, the following scientific challenges must be tackled.

- MFT design: insulation material selection, winding configuration selection, transformer secondary winding design
- HV H-bridge: PE-based component selection, unbalanced voltage sharing of the series-connected SiC MOSFETs, protection systems, HV gate driver design

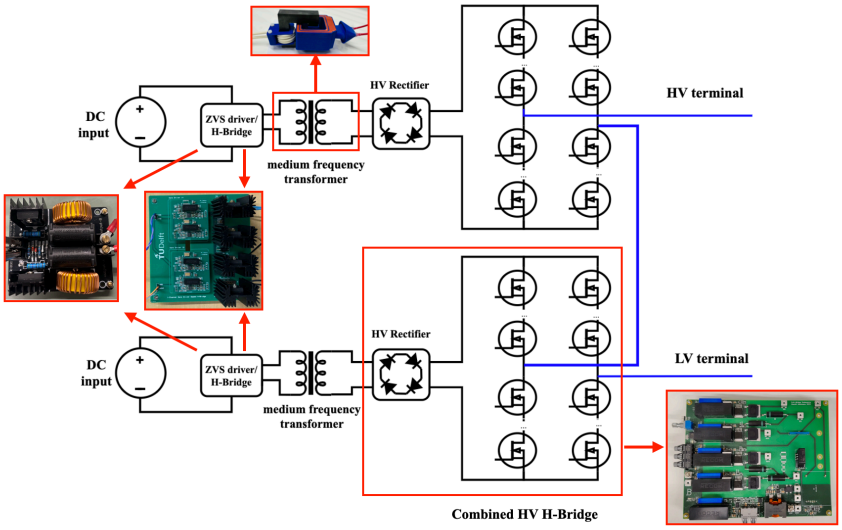


Figure 1.4: Modular cascaded H-bridge based HV-AWG topology schematic with indication of the critical components

1.3. PhD Research Questions

According to the background and the aforementioned research challenges, the PhD research questions can be defined as follows:

- **"What are the important considerations of the 10 kV class insulation system design of the medium frequency transformer (25-40 kHz)"**

  The following medium frequency transformer design items should be covered: insulation material type selection (HV accelerated aging and ramp breakdown tests under various frequencies and temperatures), MFT core type selection, MFT winding configuration design, thermal management, MFT (HV) secondary winding design and MFT (HV) bushing design.

- **"Which type of winding configuration is suitable for the medium frequency transformer inside the HV arbitrary waveform generator"**

  The following items should be covered: the transformer winding arrangements (core, side-by-side shell, concentric and sandwich type [7]), transformer terminal location (double-side placement or middle placement), transformer bushing design, transformer bobbin or bobbin cup design.

  Suitable transformer winding configuration should have higher winding breakdown voltage U_{bk}, higher partial discharge inception voltage U_{pd}, lower transformer temperature increment, lower manufacturing cost, compact transformer size and ease of implementation.

- **"What is the best method to deal with the unbalanced voltage sharing of the series-connected switches (e.g. SiC MOSFETs)"**

  Generally, the HV H-bridge module contains four HV switches (each comprised of series-connected MOSFETs). Due to the variation in the electrical characteristics of the PE-based components such as gate drivers, MOSFETs, optocouplers, regulators and the presence of the unavoidable parasitic capacitances (associated within switches or with respect to ground), unbalanced drain-source voltage sharing occurs.

  The improved RC snubber (IMS) methods, zener clamping (ZC) method, gate balancing core (GBC) method and the static balancing method are described and evaluated. The best balancing method should have the following properties: evident improvement of the V_{DS} sharing of the series-connected MOSFETs, ease of circuit implementation, simple circuit design, low cost and compact prototype size.

- **"How to properly design and prototype the HV gate drivers of the series-connected MOSFETs or the Si MOSFETs within the HV H-bridge"**

  The voltage potential of the gate terminal $V_{G(i)}$ is similar as that of the source terminal $V_{S(i)}$. If the number of the series-connected MOSFETs is large, the gate voltage of the topmost switches close to the input lead are quite high and almost equal to the main input voltage. To avoid breakdown and overheating of the gate drivers, the HV gate drivers are required. The simplest method is to use the non-isolated gate drivers together with the optocouplers and isolated DC/DC converters to built the HV gate driver circuits. The optocouplers and isolated DC/DC converters provide galvanic isolation for the HV and LV. Additionally, the magnetically isolated gate driver represents another method, utilizing two gate-coupled transformers to simultaneously turn on and off the series-connected MOSFETs. However, this technique is still under development in our research group and has not yet reached full maturity.

- **"Which switching topology is suitable to generate the input voltage of the medium frequency transformer"**

  Soft-switching topology: The output voltage and current waveforms of a standard H-bridge are square-shaped. By incorporating additional capacitors and inductors, such as an LLC or LCC resonant tank, between the standard H-bridge and the primary winding of the MFT, the current output waveform can be transformed from square-shaped to sinusoidal. This conversion significantly reduces the $\mathrm{di/dt}$, leading to fewer voltage transients and spikes, which in turn minimizes losses. Additionally, the presence of resonant tank can increase the transformer's output voltage. As an alternative, the zero-voltage switching (ZVS) driver could also be used for soft-switching.

  Hard-switching topology: If a hard-switching topology is employed, the MFT input will consist of square pulses. This can lead to potential distortion in the MFT output voltage waveform as well as the standard H-bridge waveform. The distortion is caused by (reflected) transients and spikes induced by the high $\mathrm{di/dt}$ on the transformer's primary voltage. Consequently, the use of a hard-switching topology is not recommended.

For the MFT design, a thorough review of relevant literature is necessary to establish a clear transformer design procedure. During the design process, COMSOL simulations are required to calculate transformer leakage inductance and the electric field distribution of the HV winding. Additionally, Novo-control measurements should be used to measure the dielectric characteristics (e.g. $tan\delta$ and ϵ_r) of potential insulation materials such as transformer oil, silicone oil, silicone rubber, and epoxy resin. For the design of the LV and HV H-bridge, Altium Designer are used to create the PCB, and LTspice simulations will be employed to analyze the H-bridge circuit and various balancing methods for the HV switch.

1.4. PhD Contributions

- A PhD thesis that contains comprehensive design guidelines of the cascaded H-bridge based HV-AWG – three key components: HV H-bridge, LV H-bridge, medium frequency transformer.

- A validated HV and HF insulation (ramp sinusoidal breakdown and accelerated aging) test platform using a ferrite-based resonant transformer (max. $23\,\mathrm{kV_{pk}}$ limited by the voltage level of DC source) **(Chapter 4)**

- A reliable and validated medium frequency transformer designed in a compact size with the specifications: $20-30\,\mathrm{kV_{pk}}$ isolation level and 25-45 kHz working frequency level **(Chapter 4)**

- A validated medium frequency transformer (25–45 kHz) with at least $10\,\mathrm{kV_{pk}}$ insulation level **(Chapter 6)**

- A validated and calibrated $2.7\,\mathrm{kV_{pk}}$ and $0.2\,\mathrm{A_{rms}}$ HV H-bridge (Si-MOSFET based) PCB with corresponding current, voltage measurements and over-current, over-voltage protections and a validated standard H-bridge (max. $1\,\mathrm{kV_{pk}}$) **(Chapter 5 and 6)**
- A validated 8 kV-level modular cascaded H-bridge based HV-AWG prototype (3 submodules and 7 voltage levels) **(Chapter 6)**

1.5. PhD Thesis Layout

This PhD thesis presents a comprehensive design guidelines for a 3-stage modular cascaded H-bridge-based high-voltage arbitrary waveform generator. The structure of the thesis is shown in Fig. 1.5:

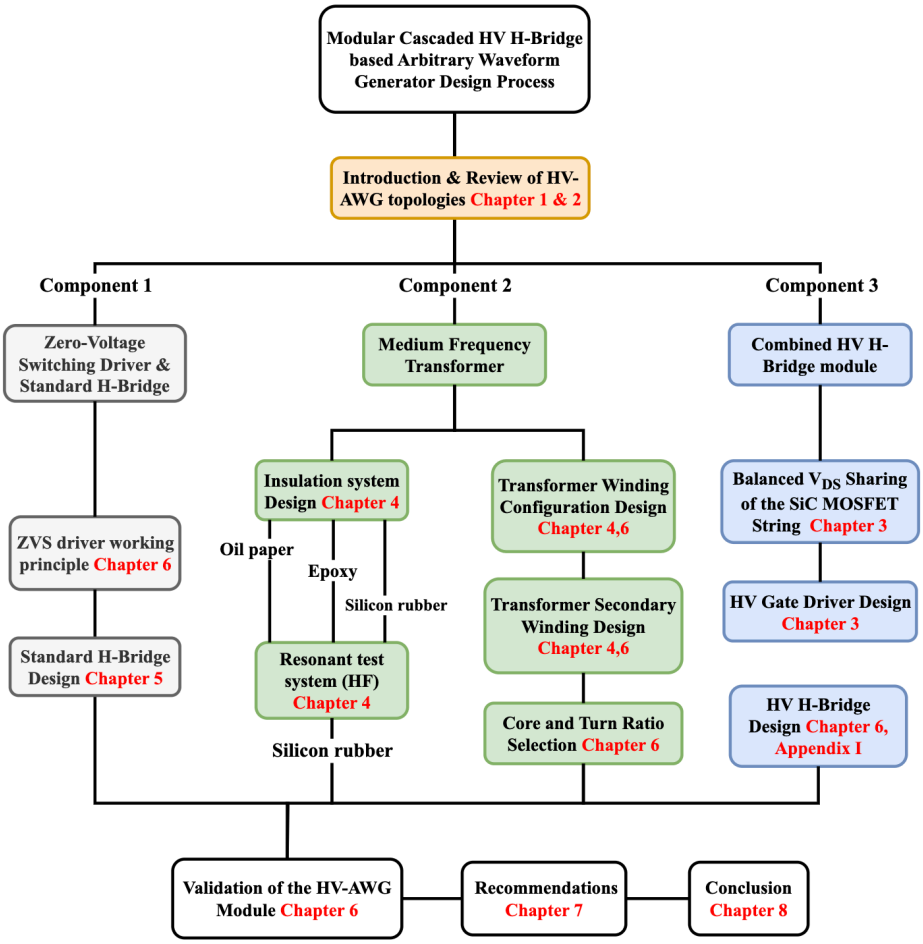


Figure 1.5: The flow chart of the PhD thesis outlines

The **first chapter** outlines the context of energy transition and the motivation for developing an arbitrary waveform generator, aimed at testing the insulation systems of HV equipment under realistic electric field strength conditions. **Chapter 2** reviews and compares various existing types of HV arbitrary waveform generators, leading to the identification of the CHB-based HV-AWG as the optimal topology based on performance metrics.

In **Chapter 3**, different methods for balancing the drain-source voltage of SiC MOSFETs in series-connected configurations are explored, evaluated, and compared to assess their suitability for constructing the HV switch of the H-bridge. This research reveals that, although the voltage sharing condition can be improved significantly, the implementation of balancing techniques significantly complicates the HV H-bridge design, ultimately leading to the selection of Si MOSFETs with higher blocking voltages. Additionally, the design of the HV gate driver for triggering the corresponding switch is elaborated in this chapter.

Chapter 4 focuses on the insulation selection for the required medium-frequency transformer. The dielectric properties of oil-impregnated paper and neat epoxy resin are investigated at relatively low frequencies. However, since the medium-frequency transformer is required to operate above 25 kHz, an alternative test platform capable of performing ramp sinusoidal tests at the target frequency is needed. This chapter introduces the design and prototyping of a resonant test system that meets these specifications. **Chapter 5** presents the design of the standard H-bridge inverter, a key component of the resonant test system.

Chapter 6 synthesizes the dielectric data obtained through the resonant test system, concluding that silicon rubber is the most suitable insulation material for the medium-frequency transformer. This chapter also details the design process of the medium-frequency transformer, including the selection of the transformer core, turn ratio, winding configuration, and secondary winding, as well as the design of the HV H-bridge, Si MOSFET selection, and protection circuit development. Additionally, validation results are provided, demonstrating that the designed prototype HV-AWG successfully generates arbitrary waveforms.

Finally, **Chapter 7** provides the future recommendations, which discusses the challenges in transformer manufacturing, specifically the labor-intensive processes involved in insulation casting and winding wrapping. The planar transformer is explored as a potential alternative to conventional medium-frequency transformers, and preliminary investigations into the insulation properties of FR-4 are conducted. This research may be continued in future work. **Chapter 8** presents a detailed conclusion of the PhD thesis.

2

Existing HV Arbitrary Waveform Generator Topologies

2.1. Function Generator with Linear HV Amplifier

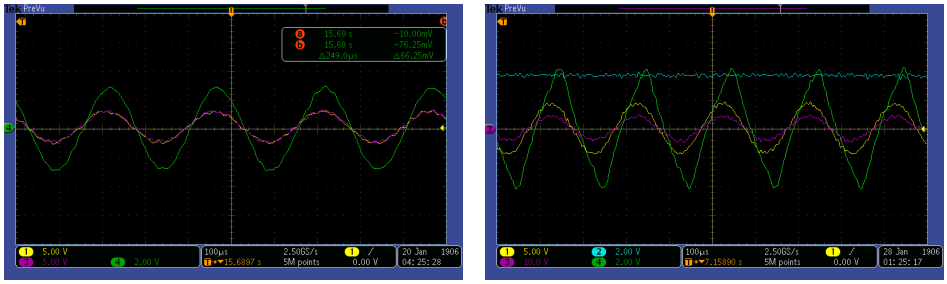
The simplest method to generate the HV and HF arbitrary waveforms is to directly connect a function generator to an HV amplifier. However, the commercially available HV amplifiers have limited frequency bandwidth and voltage ratings [2]. For instance, the HV TREK amplifier in TU Delft HV lab has a maximum voltage limit of $30\,\mathrm{kV_{pk}}$ and a maximum current limit of $20\,\mathrm{mA_{rms}}$. According to formula (2.1), if the sample under test is selected, its equivalent capacitance C_{DUT} can be considered as a fixed value. The permissible ranges of I_{amp} and U_{amp} are also known. As a result, the feasible frequency bandwidth f_{max} of the TREK amplifier can be obtained.

$$f_{max} = \frac{I_{amp}}{2\pi \cdot U_{amp} \cdot C_{DUT}} \tag{2.1}$$

Furthermore, while the function generator of type TENMA 72-14111 can continuously provide the HF arbitrary waveforms at LV levels, sending an HF (>5 kHz) input signal to the TREK amplifier results in a significant distortion of the amplified signal, as illustrated in Fig. 2.1. Due to these limitations and drawbacks, this method is not recommended for producing HF and HV pulses for testing the insulation of HV grid components.

2.2. Cascaded H-Bridge with Flyback Supply

This subsection details the advantages, disadvantages, and working principle of the flyback converter-based HV-AWG. As described in [4] and [5], the HV-AWG is designed using a multi-level cascaded H-bridge topology, as illustrated in Fig. 2.2.



(a) Original sinusoidal waveform (b) Distorted waveform

Figure 2.1: Output performance of the Trek amplifier based HV-AWG

The primary advantage of this topology is its modular structure, which relies on duplicating elementary modules. This allows for significant scalability of the AWG output voltage and greatly simplifies the manufacturing process. Additionally, the modular design enhances the reliability of the AWG. The schematic shows that only 600 V H-bridges are required, simplifying the prototype design but limiting the output voltage of each submodule. In the referenced work, 24 submodules are connected in series, achieving a maximum output voltage of ±14.4 kV and producing up to 49 output voltage levels. However, this results in a really complicated control algorithm for the cascaded H-bridges. In Fig. 2.2, the battery stack serves as the

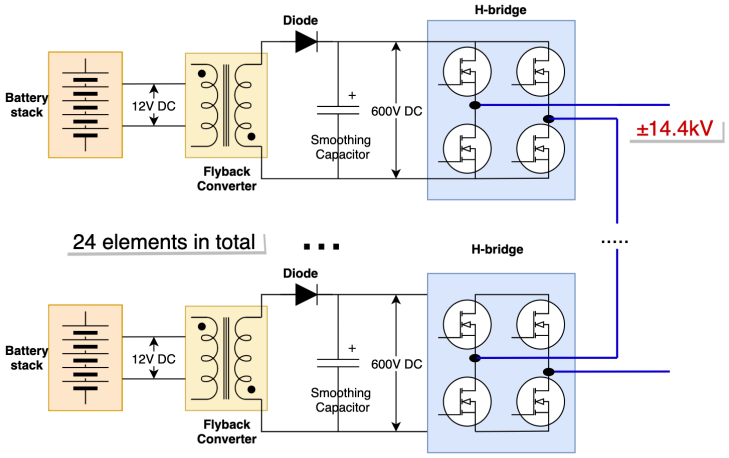


Figure 2.2: The topology of the modular multilevel flyback converter based HV-AWG

input voltage source for the HV-AWG, providing 12 V that is then boosted to 600 V DC by the flyback converter. However, the battery stack has a notable limitation: its finite energy storage, which restricts its ability to supply continuous power for a long duration. The crucial component of the flyback converter is the HF trans-

former, which includes one primary winding, six separate secondary windings, and two tertiary windings, as depicted in Fig. 2.3. Designing such a multi-secondary transformer is quite challenging. Without a primary compensation capacitor, the energy transfer efficiency of the transformer is significantly reduced to less than 50 % due to the low coupling factor k. An alternative solution is to use a matrix transformer, described in [8].

To achieve a stable flyback output, as shown in Fig. 2.3, the secondary winding is regulated using a robust closed-loop control mode. An auxiliary secondary feedback winding W_1, is required for modular output voltage measurement. Additionally, the shunt resistor R_1 measures the primary current. If a voltage drop ΔV is detected on the secondary output by W_1, the duty cycle of the power switch S_1 can be adjusted to stabilize the 600 V DC output. Furthermore, a seventh secondary winding W_2, set to 40 V DC output, supplies power to the H-bridge auxiliary control circuits.

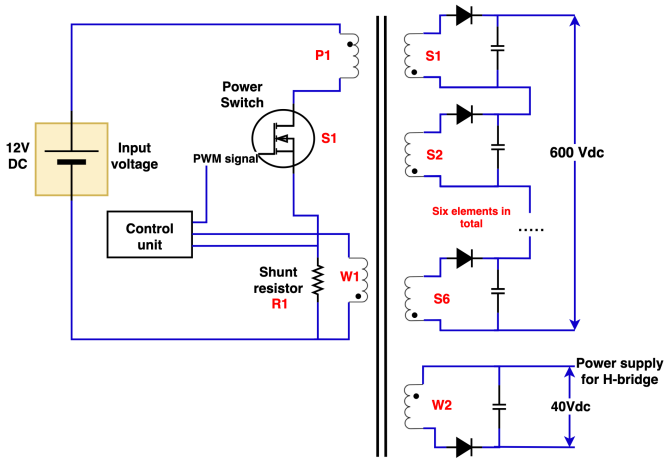


Figure 2.3: The flyback converter used to feed the H-bridge block

The HV-AWG consisting of 24 submodules complicates the control algorithm for the cascaded HV H-bridges. To achieve the desired HV output with fewer submodules, the target output voltage for each AWG submodule is designed to be approximately 2-3 kV, with three submodule elements anticipated. The input battery stack (12 V) is replaced by a commercially-available DC source, which offers continuous power and higher voltage amplitude. If the AWG submodule output voltage increases from 600 V to 2-3 kV, the power switches within the H-bridge may reach their maximum blocking voltage, potentially causing breakdown (commercially-available SiC MOSFETs have a voltage limit of 1.7 kV). To mitigate this, multiple switches could be connected in series to distribute the blocking voltage across the switches. However, unbalanced voltage sharing may occur due to unsynchronized gating signals, variations in PE-based component parasitic parameters, and different electrical characteristics. This specific problem will be thoroughly discussed in Chapter 3.

2.3. Cascaded H-Bridge with Boost Supply

In [6], a boost converter-based HV-AWG was introduced and designed also using a multilevel cascaded H-bridge topology. This subsection elaborates on the AWG working principle, along with its advantages and disadvantages. Contrasting with the topology discussed in Chapter 2.2, the complicated flyback converter is replaced by a simple boost converter, and the HF transformer is eliminated. As a result, the boost converter-based topology, depicted in Fig. 2.4, offers a more compact device size, reduced weight and ease of assembly and integration.

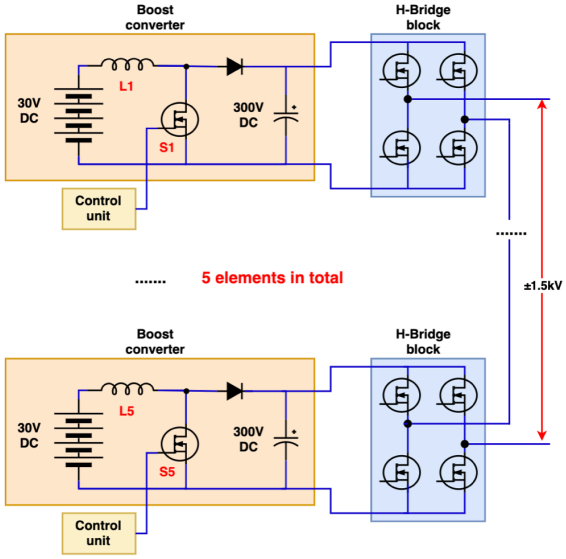


Figure 2.4: The topology of the modular multilevel boost converter based HV-AWG

The initial power source of the HV-AWG prototype is a 30 V DC lithium-ion battery stack. Additionally, the introduced DC-DC boost converter amplifies the original input DC voltage 10 times to 300 V DC (with a duty cycle of 0.9). A large HV smoothing capacitor C_{smooth} is connected at the end of the boost converter to stabilize the DC output. The final output voltage of this 5-stage prototype is only 1.5 kV. In fact, removing the HF transformer did achieve a more compact prototype size compared to the topology shown in Fig. 2.2. However, the boost converter has a limitation in its amplification capacity. If a higher HV-AWG output voltage is required, a larger number of submodules must be cascaded, complicating the control algorithm for the H-bridges. Additionally, the HF transformer provides galvanic isolation between the primary and secondary windings. Without this isolation, a significant voltage difference between the boost converter's input and output increases the risk of breakdown due to discharges and sparks from the secondary to the primary side. For the PhD project, around 8 kV HV-AWG output is desired. Thus, this method is not suitable.

2.4. Modular Multilevel Converter (MMC)

Fig. 2.5 depicts the schematic of the MMC-based HV-AWG [2]. It includes a split DC source V_{dc}, an AC filter composed of the upper and lower arm inductance L_a, a capacitive load C_{load} representing the equivalent electrical model of the HV object, and multiple MMC modules, which can be in either an on-state or off-state. When a module is in the on-state (T_1 ON and T_2 OFF), it generates V_{Cs} as output. When the module is in the off-state (T_1 OFF and T_2 ON), it is bypassed. By properly controlling the MMC modules through the algorithm, a specific number of V_{Cs} outputs can be cascaded, generating the HV arbitrary waveform. Notably, there is a series resistance R_a along with the arm inductances L_a. This is needed to damp the oscillations caused by the resonance between the arm inductances and the load capacitance.

Advantages of the modular multilevel converter based HV-AWG:

- **Flexibility:** MMC-based HV-AWG offers high flexibility in generating arbitrary voltage waveforms. Users can specify various parameters such as amplitude, frequency, phase, and waveform shape.
- **High Voltage Capability:** MMCs are well-suited for HV applications. They operate at high voltages efficiently, making them suitable for testing and simulation in high voltage power systems.
- **Low Harmonic Distortion:** MMC-based HV-AWG exhibits low harmonic distortion in the output voltage waveform. This characteristic is advantageous in applications where low distortion is critical.
- **Modularity:** MMCs are modular in nature, which means they can be easily scaled up or down depending on the application requirements. This modularity facilitates easier maintenance, repair, and expansion compared to traditional converter topologies.
- **High Efficiency:** MMCs can achieve high efficiency levels, especially at higher voltage levels. This efficiency is crucial in power systems where minimizing losses is essential for overall system performance and energy conservation.

Disadvantages of the modular multilevel converter based HV-AWG:

- **Complexity:** The control and operation of the MMC-based converters can be more complex compared to traditional converter topologies. This complexity arises owing to the need for sophisticated control algorithms to manage the multiple modular units and ensure proper voltage balancing.
- **Cost:** MMC-based converters are more expensive to manufacture and implement compared to conventional converter topologies. The higher cost is mainly attributed to the use of multiple power semiconductor devices and complex control systems.

- **Component Count:** MMCs consist of a large number of PE-based devices (e.g. IGBTs or IGCTs) and passive components like capacitors and inductors. Managing and maintaining a large number of components can increase the risk of component failures and require more extensive monitoring and maintenance procedures.
- **Voltage Balancing:** Achieving proper voltage balancing across the modular units in an MMC can be challenging, especially under dynamic operating conditions. Imbalances in voltage levels can degrade converter performance and lead to increased losses and further leads the converter breakdown.

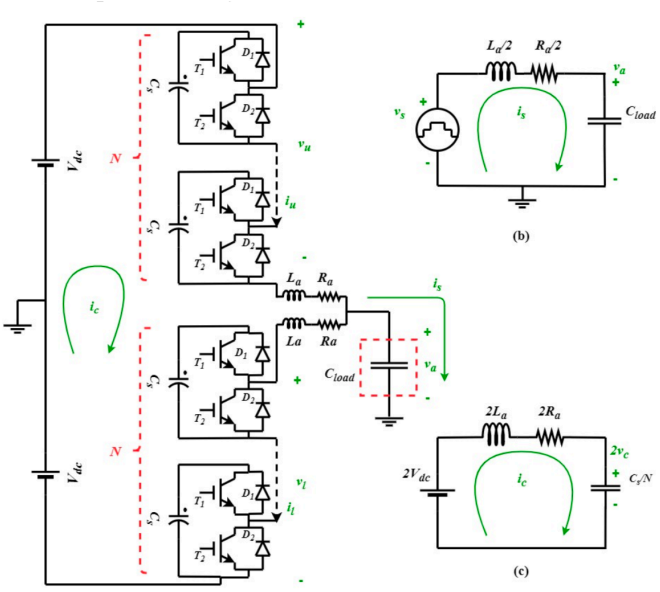


Figure 2.5: The topology of the modular multilevel converter based HV-AWG [9]

In conclusion, chapters 2.2 to 2.4 present three types of the designed HV-AWG topologies using different modular multilevel converters. Compared to the non-modular case, described in [10], the modular HV-AWG topology offers several significant advantages: high voltage capability, excellent submodule interchangeability, enhanced scalability and reliability of the HV-AWG prototype, as well as ease of integration and manufacturing.

2.5. Modular Cascaded HV H-Bridge

Fig. 2.6 presents the schematic of a submodule of the modular cascaded H-bridge-based HV-AWG, while Fig. 2.7 depicts the full-scale HV-AWG. The transformer can be driven by either a ZVS driver (soft-switching) or a standard H-bridge (hard-switching). Operating at 20-30 kHz, the medium frequency transformer provides

isolation level above 10 kV and steps up its input signal amplitude by a factor of 50. The HF output signals from the transformer are rectified to generate the DC signal (2-3 kV), which is then sent to the HV H-bridge input. This cascaded H-bridge-based HV-AWG design has a similar topology as the solid-state transformer (SST), decipted in Fig. 2.8 [11].

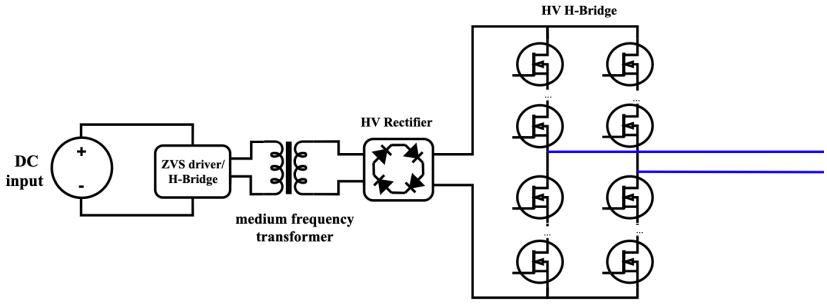


Figure 2.6: Desired cascaded H-bridge based HV-AWG submodule in a soft-switching topology

The modular CHB-based HV-AWG is used to test the insulation of system components, which can be considered as capacitive loads. Consequently, there is only a low output current requirement, up to 5 A [2]. With this low current, less heat is generated in the submodules, allowing for a potentially compact size. However, the transformer insulation system is quite vulnerable, as its permissible electric field strength significantly decreases if the input frequency increases to 20-30 kHz. Therefore, more insulation material is needed to withstand the high voltage, which conflicts with the goal of maintaining a compact size.

Compared to the CHB-based HV-AWG in a soft-switching topology, the hard-switching topology is simpler and cheaper to design owing to its circuit simplicity. Additionally, the hard-switching topology allows for a wider transformer operating frequency f_s, ranging from several kHz to tens of kHz. However, if the hard-switching topology is chosen, several considerations need to be addressed:

- The severity of LC oscillations caused by the leakage inductance $L_{k(p)}$ or $L_{k(s)}$ and parasitic capacitance C_p on both sides should be manageable. To reduce the resonance severity, the simplest method is to minimize the primary and secondary leakage inductance and improve the flux linkage coupling by using the coaxial primary and secondary winding layout as described in [11].
- The switching energy loss P_{loss} of the power switches within the standard H-bridge should be considered. The input parasitic capacitances of the power switches (e.g. MOSFETs) can be hundreds of pF, and some leakage inductance L_k may also arise from the H-bridge PCB. Electrical energy will dissipate owing to these parasitic parameters within the H-bridge. Although, the CHB-based HV-AWG is used to test HV device insulation systems (capacitive loads), its output current I_{HV} can reach a few amperes. Under HF applications, the switching energy losses would be considerable.

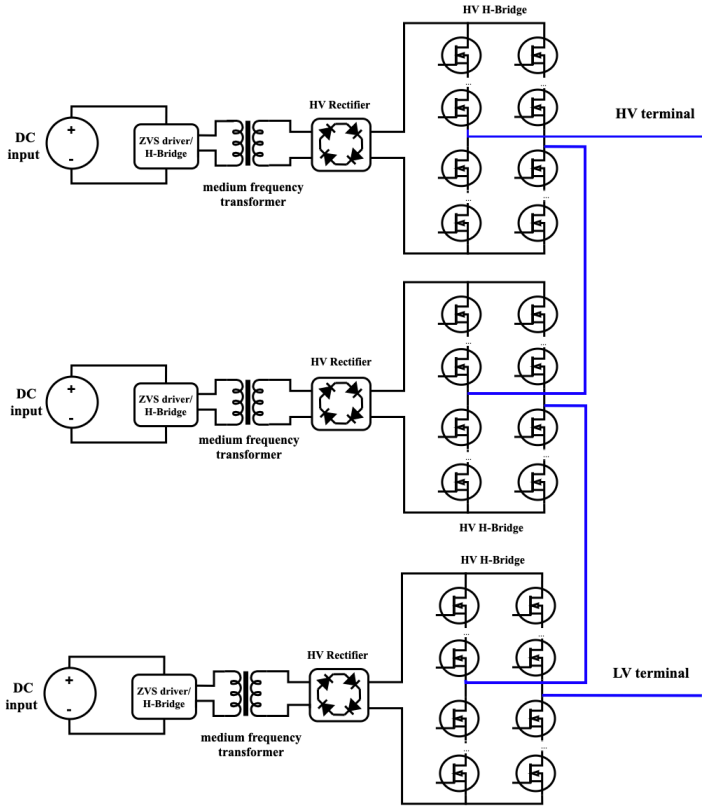


Figure 2.7: Modular cascaded H-bridge based HV AWG with three submodules in series

- To achieve the same amount of HV-AWG submodule output voltage, a MFT with soft-switching (ZVS driver) can utilize an amplitude-enhanced input signal compared to the one with hard-switching (standard H-bridge). Consequently, fewer transformer secondary turns are needed because the resonant circuit boosts its output gain. This allows for a more compact transformer size.
- If the hard-switching topology is used in HF applications, there will be a large $\mathrm{di/dt}$ during the H-bridge transient period, causing significant voltage spikes and disturbances. This results in distortion of the H-bridge output waveform.

Inspired by the transformer inside the flyback converter shown in Fig. 2.3, the non-modular CHB-based HV-AWG topology is proposed, as illustrated in Fig. 2.9. This non-modular topology is suitable only for lower output voltages owing to the limitations of the transformer insulation system. In this schematic, the transformer has one primary and multiple secondary windings, which presents the biggest challenge for this topology. The advantages and drawbacks of this non-modular CHB-based HV-AWG are as follows:

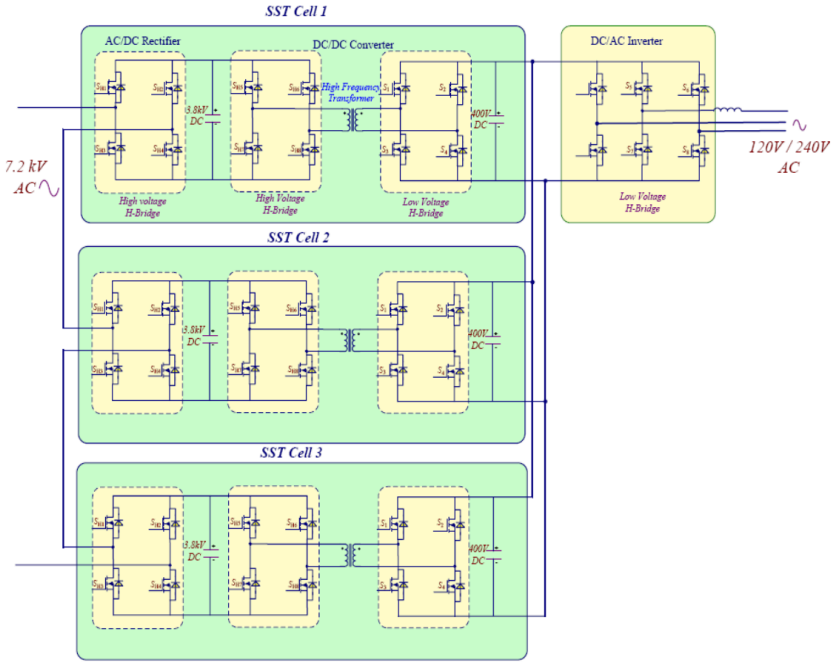


Figure 2.8: The schematic of the solid state transformer [11] with similar scheme as the CHB-based HV-AWG

- **Advantages:** As shown in Fig. 2.9, the MFT has only one primary winding but several secondary windings. This design allows the manufacturer to reduce the cost associated with multiple primary circuits. Additionally, the output voltage from each transformer secondary winding, which will be rectified and fed to the HV H-bridge, can have exactly identical value.

- **Drawbacks:** The reliability of this non-modular topology is low. If the primary winding of the MFT fails, the entire arbitrary waveform generator will cease to function. Additionally, heat dissipation in the transformer core and windings will pose a significant problem. Furthermore, the high total output from the secondary windings necessitates a superior transformer insulation system. Last but not least, the coupling between the primary and secondary windings will be very low, requiring an additional primary compensation capacitor.

In conclusion, compared to the non-modular CHB based HV-AWG, the modular one has more advantages and should be eventually selected. Compared to the modular boost converter based HV-AWG, the CHB based HV-AWG submodule has higher voltage capability owing to the utilization of the MFT (galvanic isolation between LV and HV side). Also, the battery stack is replaced by the rectified 230 V, which can continuous power the HV-AWG and allow performing long-duration HV

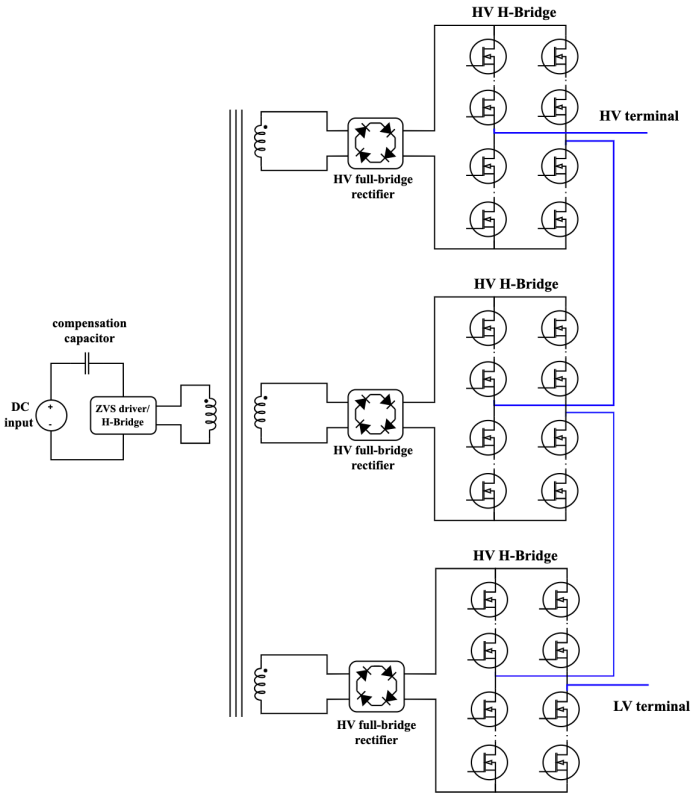


Figure 2.9: Non-modular CHB based HV-AWG with soft-switching topology

and HF insulation aging tests. Comparing to the modular flyback converter based HV-AWG, apart from the replacement of the battery stack, the flyback converter is simplified to a compact MFT together with a LV H-bridge or ZVS driver and the prototype design cost can be reduced. The modular cascaded H-bridge based HV-AWG is selected. The following chapters address the corresponding research questions, with the design details presented in Chapters 4, 5, 6, and Appendix I.

3

Balancing Techniques for the H-Bridge HV Switch[1]

3.1. Background

As the integration of renewables into the power grid continues to increase, the deployment of medium-voltage high-power converters, modular multilevel converters [2, 12], and solid-state transformers [13, 14] will become numerous in the near future. For the next generation of these PE-based systems, high efficiency, high voltage, and high power are essential for a wide range of applications, as summarized in Fig. 3.1. In this context, the role of semiconductor devices with the capability to operate at high switching frequencies, withstand elevated temperatures, and exhibit low switching losses becomes even more important.

Compared to silicon (Si), silicon carbide (SiC) excels in several properties, such as reasonable electron mobility, higher critical field strength and thermal conductivity. Moreover, SiC MOSFETs may have lower on-resistance $R_{DS(on)}$, higher blocking voltage, higher operation temperature, and can be used at higher switching frequencies [32]. Compared to IGBTs, SiC MOSFETs have no tail-current characteristics during the turn-off period, which contributes to lower switching losses and shorter turn-off delay.

Currently, MV SiC devices with a maximum blocking voltage of 10-15 kV have sparked significant interest for use in HV applications, although they have not yet been commercialized [33], [34]. The main limitations are the costs and the complexity of device manufacturing and packaging, which currently restrict the commercially available SiC MOSFETs to a maximum blocking voltage of 3.3 kV [35]. Whereas, to overcome this blocking voltage limitation and achieve higher system voltages, it is possible to connect multiple commercially available SiC MOSFETs in

[1] W. Zhao, S. Ghafoor, G. W. Lagerweij, G. Rietveld, P. Vaessen, M. G. Niasar, "Comprehensive Investigation of Promising Techniques to Enhance the Voltage Sharing among SiC MOSFET Strings, Supported by Experimental and Simulation Validations", Electronics 13, 1481 (2024).

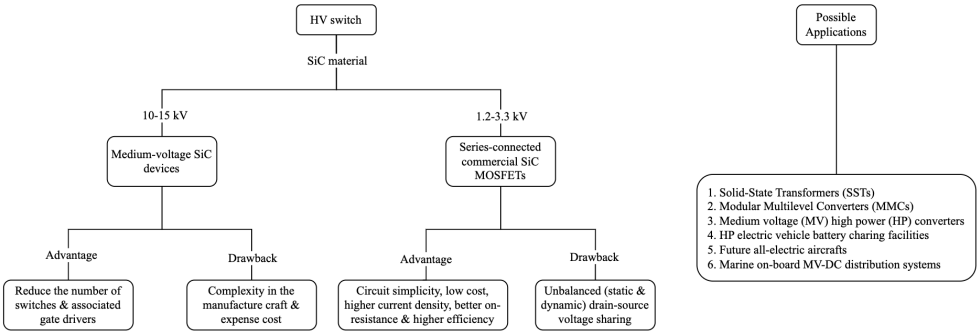


Figure 3.1: Properties for different types of HV switches (left) and their possible applications (right) [12, 15–31]

series. Figure 3.1 provides a detailed overview of the advantages and drawbacks of such SiC MOSFET strings and MV SiC MOSFETs.

Using multiple low-cost and commercially available SiC MOSFETs in series allows the required HV operation with simple yet mature gate-driving techniques. The major obstacle to implementing the series-connected operation is maintaining an equal voltage distribution across the SiC MOSFET string under all operating and transient conditions. Voltage balancing is essential to achieve equal stressing of the MOSFETs, and consequently high reliability and higher operating voltages without voltage derating. The voltage imbalance is primarily caused by mismatched gate driving signals, the existence of SiC MOSFET intrinsic and external parasitic capacitances and inductances [36], and the variation in SiC MOSFET off-resistance. These factors result in switching delays or time shifts (several ns to tens of ns), variation in $\mathrm{dV_{GS}/dt}$, and voltage imbalance across the MOSFET string.

3.1.1. Factors Influencing Drain-Source Voltage Distribution

The factors that can cause unequal drain-source voltage sharing of the SiC MOSFET string are elaborated in this subsection. A testing circuit composed of two series-connected SiC MOSFETs and one current-limiting resistor is shown in Fig. 3.2, which is used to analyze the impact of various factors on the voltage sharing among the SiC MOSFET string.

Variation in MOSFET switching delay $\delta\, t_d$: According to the measured results shown in Table. 3.1, ignoring the other possible factors, the intrinsic variation in the switching delay is not the dominant factor causing V_{DS} imbalance. Also, part of the variation in $t_{d(on)}$ and $t_{d(off)}$ between the measured values and the typical values from datasheets may be due to different measuring conditions. Generally, the variation in MOSFET parasitic parameters is limited if the devices are bought from good manufacturers and selected from the same production batch. However, gate threshold voltage of SiC MOSFET may vary with temperature, and from device

to device. This can contribute to a larger $\delta\, t_d$.

Fifteen measurements of switch type IMW120R220M1H (Infineon) or C3M0280-090D (Wolfspeed) are performed based on [37] and the median is taken as the typical value of $t_{d(on)}$ and $t_{d(off)}$. Among all of the obtained data, the intrinsic variation in $t_{d(on)}$ and $t_{d(off)}$ are 2.0 and 2.4 ns (IMW120R220M1H), and 2.3 and 1.6 ns (C3M0280090D).

Table 3.1: The turn-on and -off delay of two types of commercially available SiC MOSFETs

SiC MOSFET	Datasheet		Measurement			
	$t_{d(on)}$	$t_{d(off)}$	$t_{d(on)}$	$\delta\, t_{d(on)}$	$t_{d(off)}$	$\delta\, t_{d(off)}$
IMW120R220M1H	5.0 ns	10.0 ns	6.8 ns	±2.0 ns	12.8 ns	±2.4 ns
C3M0280090D	5.3 ns	8.5 ns	7.7 ns	±2.3 ns	11.6 ns	±1.6 ns

Variation in gate driver switching delay $\delta\, t_d$: The variation in switching delay that arises due to variations in the gate driver circuitry, components, and layout (i.e., the external factors) are much more significant than the intrinsic variation of the MOSFET. For example, the maximum switching delay variation $\delta\, t_{d(max)}$ reported in [38, 39] of the isolated gate driver type STGAP2SICSN (e.g.) and that of the non-isolated gate driver type IXDD630MCI (e.g.) is around 40 ns. Moreover, according to [40], that of the opto-coupler type FOD3182 (e.g.) can even reach 160 ns. The value of $\delta\, t_{d(max)}$ can be reduced by sorting, binning, and matching components, thus reducing the voltage imbalance.

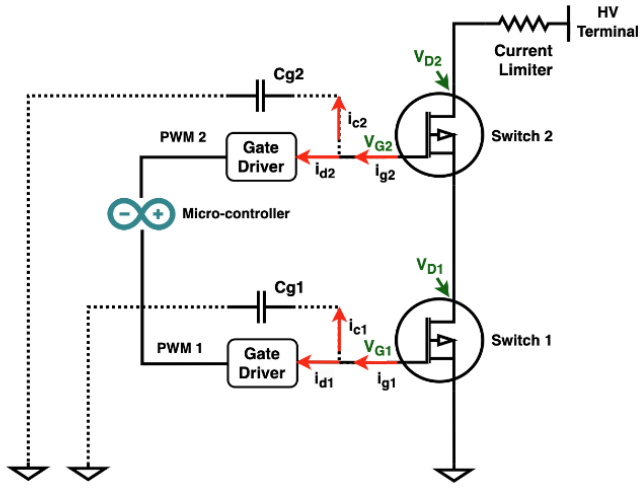


Figure 3.2: Basic schematic for testing two series-connected SiC MOSFETs

Parasitic capacitances from MOSFET gates to ground: According to [41], as seen in Fig. 3.2, the C_{gi} existing from respective gates to ground is observed as the dominating factor contributing to the unbalanced V_{DS} sharing among the MOSFET string. If the MOSFETs and driving components were identical, identical sink currents would flow to the drivers (i_{di}=i_{d2}). However, due to the difference between the voltages V_{Gi} with respect to ground, a variation in the gate voltage slopes occurs, which results in a different magnitude of capacitive currents i_{ci} and creates a difference in total gate currents i_{gi}, leading to voltage imbalance.

In Fig. 3.2, the total gate current i_{gi} is the sum of the gate sink current i_{di} and capacitive current i_{ci} from the gate to ground. The dv/dt at the gate of the top MOSFET is equal to that at the drain of the bottom MOSFET ($V_{G2} \approx V_{D1}$), while the gate of the bottom MOSFET is almost at ground potential. Thus, dv_{G2}/dt is higher than dv_{G1}/dt and the resultant capacitive current i_{c2} is also larger than i_{c1}. Moreover, the difference in C_{gi} from the stacked gate terminals to ground will also play a role in altering the intensity of the total gate current i_g when the number of the involved MOSFETs is large. For a small number of MOSFETs, the difference in C_{gi} can be neglected. This shows that even with perfectly matched gate drivers, $i_{g2} > i_{g1}$, resulting in faster turn-off of the top MOSFET.

Variation in MOSFET off-resistance $R_{DS(off)}$: Owing to the presence of the variation in SiC MOSFET $R_{DS(off)}$, the static V_{DS} sharing of the series-connected MOSFETs may be unbalanced. Balancing resistors ought to be connected in parallel with the SiC MOSFETs to achieve balanced static voltage sharing. Furthermore, during the V_{DS} measurement, the impedance of the differential probes will influence the balancing resistor network, and thus should also be considered.

3.1.2. State-of-the-Art Solutions

Over the past decades, various solutions have been proposed to improve the voltage sharing between series-connected MOSFETs. These methods can be categorized into static and dynamic balancing. Most challenges are encountered in the dynamic balancing. Some of the proposed solutions are: Zener clamping circuits, passive snubber circuits, and gate signal delay adjustment methods.

To avoid the SiC MOSFET breakdown caused by the unbalanced voltage sharing, the Zener clamping circuit is introduced in [42] and evaluated in [43]. The overvoltage across the MOSFET is eliminated by clamping V_{DG} through the series-connected Zener diodes whose equivalent reverse breakdown voltage V_Z is chosen based on the blocking voltage of the MOSFET. In [44], four types of passive snubbers are summarized with thorough principle elaboration. The purpose of introducing these passive snubbers is either to reduce the rise slew rate dv_{DS}/dt or to clamp the V_{DS} in such a way that the series-connected MOSFETs can share identical voltages.

The gate signal delay adjustment methods can compensate the delay time variation without slowing down the switching speed. In [45], Kiyoaki reports an important technique named the gate-balancing core (GBC) method which uses gate-coupled magnetic cores to synchronize the SiC MOSFET gate drive currents. In [46], an improved RC snubber method is proposed by S.Chen, which has a combination of the passive snubbers and the gate signal delay adjustment methods. The key

point of this method is the use of a three-port inductor whose primary windings are coupled within two snubber circuits and whose secondary winding is in series with the gate. The induced voltages from the secondary windings will be added to the gate circuits to tune V_{GS} and achieve identical gate currents.

Reliable and robust voltage balancing techniques must achieve effective voltage balancing, minimize the number of components within the balancing circuit, simplify the gate-side control circuits and introduce minimal switching losses [47]. The purpose of this chapter is to provide a detailed and concise evaluation of various approaches dealing with the unbalanced voltage sharing among the SiC MOSFET string. The pros and cons of each method are discussed and the suitable conditions for the application of each method are provided.

3.2. Static Voltage Balancing Method

The factors that can lead to the static voltage imbalance are thoroughly examined, underscoring the significance of this issue. A promising solution is then proposed and validated, to improve the static voltage sharing of the SiC MOSFET string. Additionally, the correct use of differential probes to measure the SiC MOSFET drain-source voltage is explained, an important aspect that can significantly influence the static voltage sharing of the MOSFET string while performing drain-source voltage measurements.

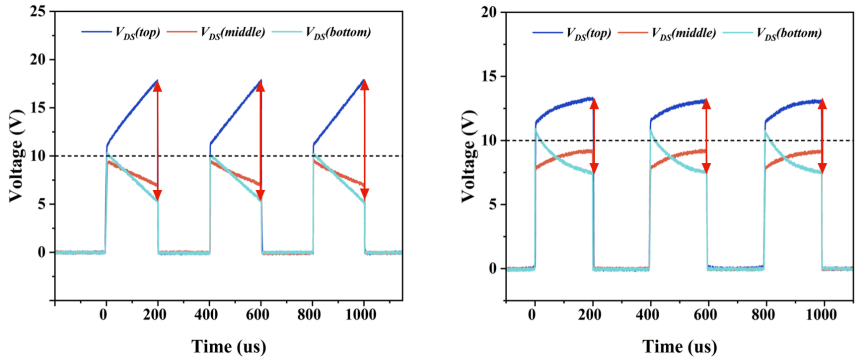


Figure 3.3: Measured unbalanced V_{DS} sharing of the SiC MOSFET string without (left) and with (right) the identical balancing resistors (500 $k\Omega$)

As seen in Fig. 3.3 (left), an unbalanced static voltage sharing issue occurs on the three series-connected MOSFETs. This phenomenon can occur due to variation of the off-resistance $R_{DS(off)}$ of the MOSFETs or the impact of the measurement probe. This issue can be effectively addressed through the utilization of static balancing resistors R_{st}, which equalizes the voltage stress in the series-connected devices at the cost of increased static power dissipation. The MOSFETs chosen for experiments are of type IMW120R220M1H. From its datasheet, if the applied drain-source voltage is 1.2 kV, the drain leakage current I_{DSS} varies over two decades (0.2 μA to 95 μA) at an ambient temperature of 25 °C. Therefore, the corresponding MOSFET

off-resistance $R_{DS(off)}$ varies from 6 $G\Omega$ to 12.6 $M\Omega$.

Generally, the value of the parallel balancing resistor R_{st} should be selected at least 10 times smaller than the minimum $R_{DS(off)}$. The parallel combination of R_{st} and $R_{DS(off)}$ will then be dominated by the balancing resistor, reducing the effect of variation in $R_{DS(off)}$. The power loss in each balancing resistor is calculated using (3.1). With a derating of 40% and a maximum dissipation of 1 W, a minimum R_{st} of 500 $k\Omega$ is calculated.

$$P_{st} = \frac{U_{max}^2}{R_{st}} = \frac{(0.6 * V_{DSS})^2}{R_{st}} = \frac{(0.6 * 1200)^2}{500 * 10^3} \approx 1\,W \tag{3.1}$$

During the measurement of MOSFET drain-source voltages, even though the static balancing resistors ($R_{st} = 500\,k\Omega$) are applied, the static voltages along the SiC MOSFET string are not yet balanced, as shown in Fig. 3.3 (right).

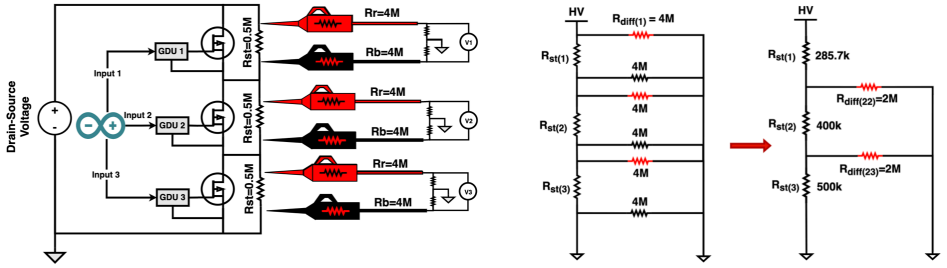


Figure 3.4: Schematic of the V_{DS} measurement of the three series-connected SiC MOSFETs (left) and the corresponding resistance ladder network (right)

The reason for this phenomenon is that the impedance of the differential probes $R_r = 4\,M\Omega$ and $R_b = 4\,M\Omega$ must be considered as part of the balancing resistor network, as shown in Fig. 3.4 (left), which influences the static voltage sharing. Hence, while observing the drain-source voltage, R_{st} should be fine-tuned only during the tests to prevent static voltage imbalance. Fig. 3.4 (right) shows the simplification of the resistive network during V_{DS} measurement. Assuming the value of $R_{st(3)}$ that is applied across the bottom MOSFET is 500 $k\Omega$, the presence of the probe impedance $R_{diff(23)}$ changes the required value of $R_{st(2)}$ for the middle switch to 400 $k\Omega$, using (3.2). Similarly, the total equivalent resistance for the bottom two MOSFETs combined with $R_{diff(22)}$ and $R_{diff(23)}$ is about 571.4 $k\Omega$. Therefore, the magnitude of $R_{st(1)}$ should be half the value of the obtained total equivalent resistance, calculated using (3.3).

$$R_{st(2)} = R_{st(3)} || R_{diff(23)} = 400\,k\Omega \tag{3.2}$$

$$R_{st(1)} = \frac{1}{2} * \left[(2 \cdot R_{st(2)}) || R_{diff(22)}\right] = 285.7\,k\Omega \tag{3.3}$$

After the application of the tuned static balancing resistors as shown in Fig. 3.4 (right), the balanced static voltage sharing of the MOSFET string can be achieved

(Fig. 3.5). However, due to the existence of the parasitic capacitances and inductances, the unmatched MOSFETs and gate drivers, balanced dynamic voltage sharing is not yet achieved.

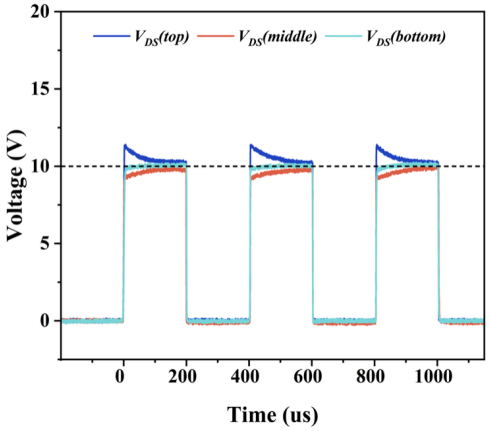


Figure 3.5: Measured overall V_{DS} sharing of the MOSFET string with tuned balancing resistors

The balancing resistors with tuned values are only used to observe the statically balanced V_{DS} waveforms on the oscilloscope during experiments. If the SiC MOSFET string is used under HV applications, the value of the required balancing resistors should be identical since there is no requirement to measure the drain-source voltages during normal operation.

3.3. Gate-Balancing Core (GBC) Method

This section evaluates the GBC method to improve the dynamic V_{DS} sharing in a string of series-connected MOSFETs. This method is based on gate signal delay adjustment. The method is validated by experiments, which are relevant for a SiC MOSFET string with a considerable variation in the turn-off delay $t_{d(off)}$. In [45,48], the GBC method is proposed to synchronize mismatched gate currents. The key point of this method is the use of a coupled inductor with a high coupling factor k, which is well-coupled within the adjacent gate circuits of the SiC MOSFET string. The magnetic coupling will impose almost identical gate sink currents ($I_{g1} \approx I_{g2}$), even if a considerable turn-off delay time variation $\delta t_{d(off)}$ exists.

When a slight turn-off delay $\delta t_{d(off)}$ is present in the bottom MOSFET, as depicted in Fig. 3.6, the top MOSFET switches off faster. Its gate current I_{g1} flows through the upper winding of the coupled inductor and returns to the gate driver. The induced current I_{g2} occurs simultaneously with I_{g1} on the lower winding through magnetic coupling. If the turns ratio is 1:1 and k is close to 1, the magnitudes of the induced gate current I_{g2} and the initial sink current I_{g1} are identical. This synchronization of the gate currents leads to balanced voltage sharing among the series-connected MOSFETs. Fig. 3.7 further illustrates the extension of the GBC method to a higher number of series-connected SiC MOSFETs. The inter-winding

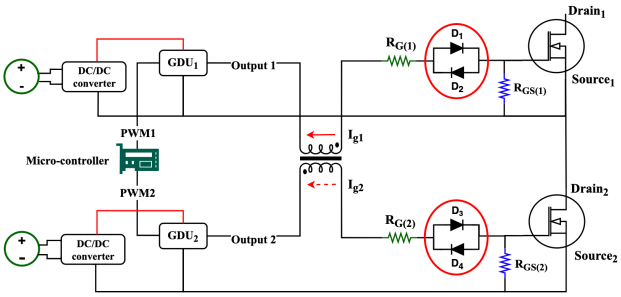


Figure 3.6: Schematic of the two series-connected SiC MOSFETs using the GBC method

insulation requirements are relaxed since inductors are only coupled between consecutive MOSFETs.

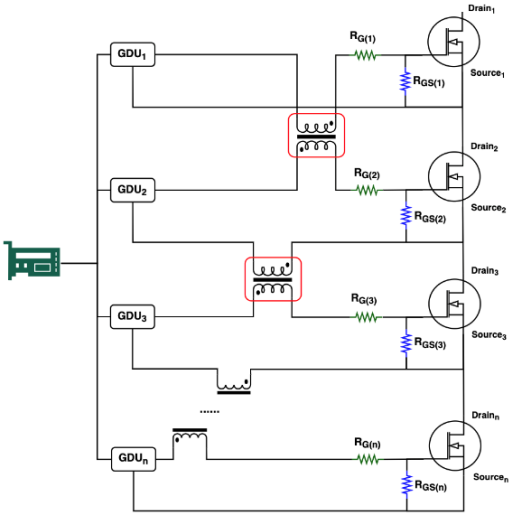


Figure 3.7: Schematic of the multiple series-connected SiC MOSFETs using the GBC method

The coupled inductor leakage inductance L_k can resonate with the dynamic input capacitance C_{iss} of the MOSFET. It should be minimized to avoid excessive ringing or oscillations on the transient parts of the gate pulses, which influences the output performance of the MOSFET string. Thus, interleaved inductor construction is recommended. Equations (3.4) and (3.6) are derived to calculate the required magnetizing inductance L_m and leakage inductance L_k in case of a particular variation in $\delta t_{d(off)}$ among the series-connected MOSFETs [45, 48].

In (3.4), $\delta t_{d(off)}$ is the turn-off delay variation of the corresponding SiC MOSFETs, and C_{iss} stands for the MOSFET input capacitance. Equation (3.4) is derived based on the assumption that the gate voltage variation δV_{GS} is smaller than 1%

of the input gate voltage V_{GS}.

$$L_m > \frac{1}{2} \cdot \frac{\delta\, t_{d(off)}^2}{0.01 \cdot C_{iss}} \tag{3.4}$$

The magnitude of δV_{GS} depends on the amount of discharge δQ_m of C_{iss} (undelayed) by the magnetizing current i_m shown in (3.5). Based on the equivalent inductor circuit model, the C_{iss} of the undelayed switch is discharged by the present magnetizing current i_m and the gate sink current i_g. However, the C_{iss} of the delayed switch is discharged only by i_g. To synchronize the gate discharge currents, the value of L_m should be sufficiently large to suppress the magnetizing current i_m. It should be noted that the total voltage applied on the magnetizing inductance L_m is V_{GS} during the turn-off delay period.

$$\begin{aligned} \delta V_{GS} &= \frac{\delta Q_m}{C_{iss(undelayed)}} = \frac{i_{m(pk)} \cdot \delta t_{d(off)}}{2 \cdot C_{iss(undelayed)}} \\ i_{m(pk)} &= \frac{\delta t_{d(off)} \cdot V_{GS}}{L_m} \end{aligned} \tag{3.5}$$

Combining the formulas in (3.5) eventually leads to (3.4). If the value of $\delta t_{d(off)}$ is relatively small (e.g., 50 ns), the assumption that δV_{GS} should be smaller than 1% of V_{GS} leads to a reasonable size of L_m. However, if the value of $\delta t_{d(off)}$ is quite large (e.g., 250 ns), the allowable gate voltage mismatch should be increased to avoid having an unrealistically large L_m. The magnitude of δV_{GS} should then be smaller than 5% of V_{GS}. Therefore, the denominator of (3.4) is modified as $0.1 C_{iss}$. Moreover, R_g stands for the total gate resistance, including the internal resistance of the gate driver.

$$L_k \leq \frac{C_{iss} R_g^2}{4\zeta^2} = \frac{C_{iss} R_g^2}{0.64} \tag{3.6}$$

The leakage inductance L_k of the gate-coupled inductors can be seen as parasitic inductances in the wires between the gate drivers and MOSFETs. The value of L_k should be designed to prevent the initial and induced gate currents from severe oscillations generated by L_k and C_{iss}. The desired tiny L_k can be difficult to realize if the damping factor ζ is chosen to be relatively large ($\geq$0.7 in [48]). Usually, the integrated gate driver IC has some internal output resistance of around $5\,\Omega$, and an external gate resistance of $10\,\Omega$ is suggested, leading to a total value of $R_g = 15\,\Omega$. Assuming ζ equals or exceeds 0.4, the required leakage can be realized and the computed k is more than 0.9999.

3.3.1. Experiments with Two Series-Connected MOSFETs Using the Gate Balancing Core Method

In [45], it is shown that for the case of two series-connected power switches, dynamic V_{DS} sharing can be achieved with a turn-off delay variation $\delta t_{d(off)}$ of up

to 80 ns using the GBC method. Experiments are performed to investigate the V_{DS} sharing when a longer $\delta t_{d(off)}$ of up to 560 ns exists, further demonstrating the robustness of the GBC method.

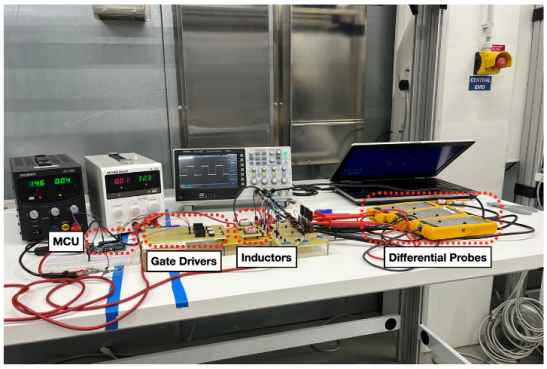


Figure 3.8: Experimental set-up of the series-connected SiC MOSFETs using the GBC method

Fig. 3.8 shows the experimental set-up with a two-switch MOSFET string using the GBC method. The switching frequency of this prototype is 2.5 kHz. For the case of two MOSFETs operating in series, compared with the bottom switch, the top one has an additional 560 ns turn-off delay, as shown in Fig. 3.9 (left). The coupled inductor is constructed with interleaved windings, resulting in a coupling factor of $k = 99.99\%$. The winding inductances L_{se} are 4.71 mH (white) and 4.56 mH (red), while the leakage inductances L_k are 390 nH (white) and 373 nH (red), shown as detail in Fig. 3.9 (right).

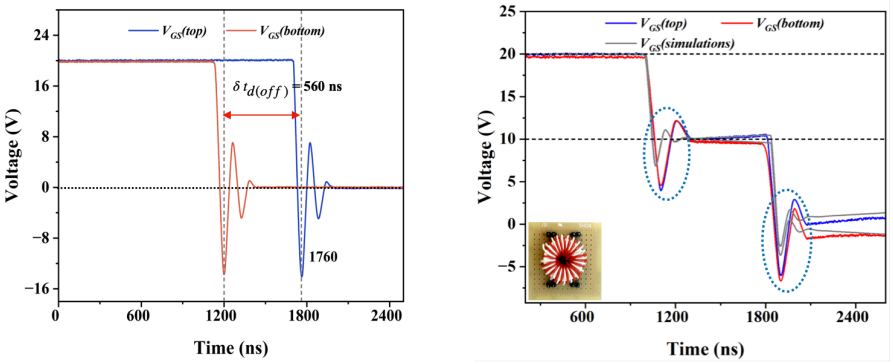


Figure 3.9: Measured V_{GS} waveforms of the two series-connected MOSFETs during turn-off period without (left) and with the gate-coupled inductor with simulation verification (right)

Fig. 3.9 illustrates how the presence of the gate-coupled inductor influences the gate voltages. Before using the coupled inductor, an extra 560 ns delay results in a noticeable difference in turn-off time. After inserting the coupled inductor in the gate circuits, the gate voltages of the MOSFET string are almost perfectly

synchronized and balanced at half of the input gate voltage. At the end of the delay $\delta t_{d(off)}$, $V_{GS(top)}$ (delayed) is slightly higher than $V_{GS(bottom)}$ (undelayed). This will be further explained in Section 3.3.2 using analytical calculations.

The gate voltages balance at $0.5V_{GS}$ during $\delta t_{d(off)}$ because the magnetizing inductance is sufficiently large to suppress i_m. This limits the gate voltage variation to less than 5% of V_{GS} and $V_{GS(top)} \approx V_{GS(bottom)}$. Since the value of i_m is negligible, if the turns ratio is set to be 1:1, the C_{iss} of the delayed MOSFET and that of the undelayed MOSFET are discharged by identical gate currents i_g. Hence, the gate currents of all MOSFETs are synchronized, and the induced voltage $V_{T(top)}$ is equal to the lower winding voltage $V_{T(bottom)}$. According to (3.7), the sum of $V_{GS(top)}$ and $V_{GS(bottom)}$ is the input gate voltage. Therefore, the final balance point is $0.5V_{GS}$.

$$\begin{aligned} Delayed &: V_{GS} = V_{GS(top)} + V_{T(top)} \\ Undelayed &: 0 = V_{GS(bottom)} - V_{T(bottom)} \end{aligned} \tag{3.7}$$

The parasitic parameters slightly distort the obtained V_{GS} waveforms. However, this issue can be tackled by using two reverse-biased placed diodes in series with the external gate resistors [49] circled in red in Fig. 3.6. Moreover, the comparison in Fig. 3.10 demonstrates that the GBC method can significantly improve the V_{DS} sharing of the SiC MOSFET string in case of the presence of a large $\delta t_{d(off)}$.

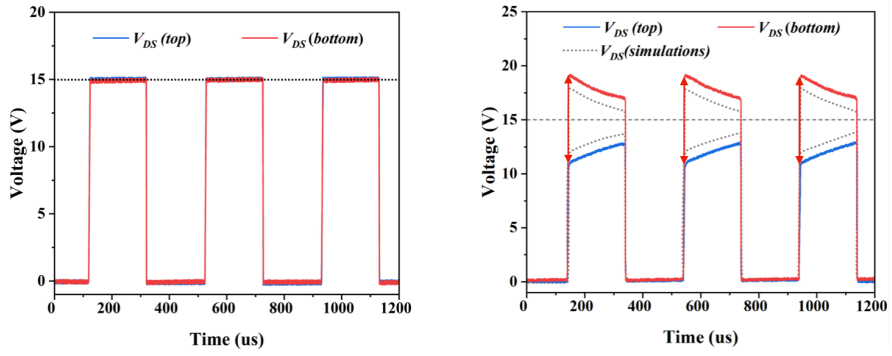


Figure 3.10: Measured V_{DS} of the MOSFET string with (left) and without coupled inductor with simulation verification (right)

From a commercial perspective, N series-connected SiC MOSFETs require $(N-1)$ coupled inductors, which can be expensive and result in a bulky solution. However, the circuit and gate-side routing are simple, which reduces the cost of components and manufacturing. Moreover, the required insulation level of the gate-coupled coupled inductor is low (V_{input}/N); thus, the cost of each component is reasonable. This means that the GBC method is quite commercially attractive.

3.3.2. Analytical Analysis of Dynamic Voltage Sharing Using the GBC Method

Balanced dynamic voltage sharing of the MOSFET string can be achieved through the GBC method in case of a large $\delta t_{d(off)}$, as shown in Fig. 3.10 (left). To better understand the performance of the MOSFET V_{GS} waveforms during $\delta t_{d(off)}$ with the gate-coupled inductors, an analytical method is derived based on the equivalent gate circuits of the two series-connected SiC MOSFETs during $\delta t_{d(off)}$, as shown in Fig. 3.11.

Compared with the top MOSFET, the bottom one is assumed to have some extra turn-off delay. Therefore, from Fig. 3.11, the bottom MOSFET remains in the on-state. Meanwhile, the top MOSFET is switched off. It can also be noted that the MOSFET gate circuits are simplified as the charged dynamic input capacitors ($C_{iss(1)}$ and $C_{iss(2)}$) circled by black dotted lines. The analytical method is derived for the case with perfect coupling ($k = 1$, similar to the previous experimental case). Consequently, the self-inductance of the windings will become equal to the magnetizing and mutual inductance ($L_{se} = L_m = M$).

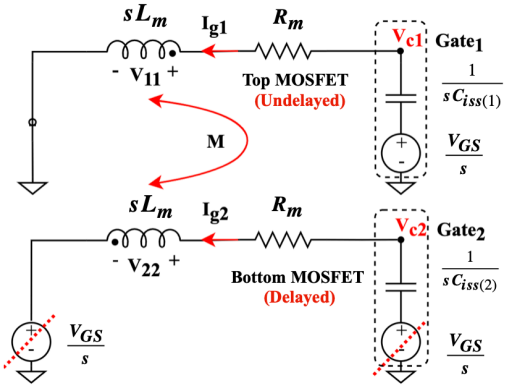


Figure 3.11: Equivalent gate circuits of the two series-connected SiC MOSFETs using GBC method

Fig. 3.11 indicates the propagation direction of the gate discharge currents (I_{g1} and I_{g2}) and the polarity of the inductor winding voltages. Due to the difference in polarity, the voltages across the upper (V_{11}) and lower (V_{22}) winding can be calculated from (3.8).

$$\begin{aligned} V_{11} &= sL_m I_{g1} - sMI_{g2} = sL_m(I_{g1} - I_{g2}) \\ V_{22} &= sL_m I_{g2} - sMI_{g1} = sL_m(I_{g2} - I_{g1}) \end{aligned} \tag{3.8}$$

The input voltage of the bottom MOSFET gate circuit is provided by the gate driver (left), and the remaining voltage on $C_{iss(2)}$ (right) is canceled. Hence, the voltage across the inductor lower winding can be calculated as: $V_{22} = -I_{g2} \cdot$

$\left(R_m + \frac{1}{sC_{iss}}\right)$. The relationship between the gate sink currents I_{g1} and I_{g2} is shown in (3.9). Also, the MOSFET gate voltages are calculated using (3.10).

$$\frac{I_{g2}}{I_{g1}} = \frac{sL_m}{sL_m + R_m + \frac{1}{sC_{iss}}} \tag{3.9}$$

$$V_{c(i)} = \frac{V_{GS}}{s} - \frac{I_{g(i)}}{sC_{iss(i)}} (i = 1, 2) \tag{3.10}$$

If the winding resistance R_m is neglected, the gate discharge current I_{g1} for the gate circuit of the top switch (undelayed) can be derived using (3.11) and (3.12).

$$\frac{V_{GS}}{s} = V_{11} + I_{g1} \cdot R_m + \frac{I_{g1}}{sC_{iss}} \tag{3.11}$$

$$I_{g1} = V_{GS} \cdot \frac{C_{iss}(1 + s^2 L_m C_{iss})}{1 + 2s^2 L_m C_{iss}} \tag{3.12}$$

According to (3.9) and (3.12), the formula of I_{g2} can be derived as shown in (3.13). After the combination of (3.10) and (3.12), (3.10) and (3.13), the gate voltages of two involved MOSFETs can be derived as (3.14).

$$I_{g2} = V_{GS} \cdot \frac{s^2 L_m C_{iss}^2}{1 + 2s^2 L_m C_{iss}} \tag{3.13}$$

$$V_{c1} = V_{GS} \cdot \frac{sL_m C_{iss}}{1 + 2s^2 L_m C_{iss}} V_{c2} = V_{GS}\left(\frac{1}{s} - \frac{sL_m C_{iss}}{1 + 2s^2 L_m C_{iss}}\right) \tag{3.14}$$

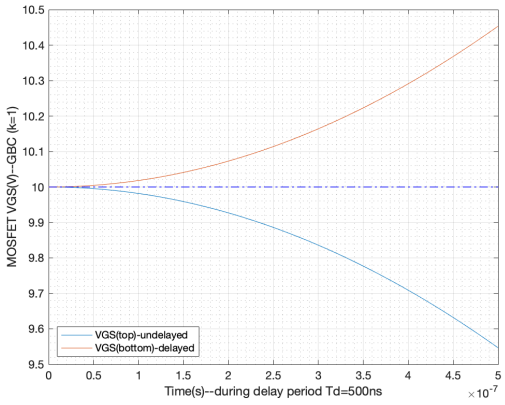


Figure 3.12: V_{GS} curves of the MOSFET string during the turn-off delay with coupled inductor ($k = 1$)

At the beginning of $\delta t_{d(off)}$, the frequency content of the gate voltage waveforms ($V_{GS(top)}$ and $V_{GS(bottom)}$) is large, and the gate current I_{g1} is almost the same as I_{g2} based on (3.9). Thus, based on (3.10), the value of $V_{GS(top)}$ should also be the same as $V_{GS(bottom)}$. On the other hand, when the high-frequency harmonics decay, the magnitude of I_{g2} will become smaller than I_{g1}, and $V_{GS(bottom)}$ will be larger than $V_{GS(top)}$. These obtained results verify that during $\delta t_{d(off)}$, $V_{GS(bottom)}$ (delayed) first resonates synchronously with $V_{GS(top)}$ (undelayed) but becomes larger than $V_{GS(top)}$ after the oscillations, as shown in Fig. 3.12. As a result, the experimental result shown in Fig. 3.9 (right) matches the analytical results.

If the coupling factor k of the inductor is close to 1, the leakage inductance L_k will be minimal, and the corresponding V_{GS} oscillation period will also be small. When the oscillations decay, the gate voltage variation δV_{GS} will occur. Conversely, if k is relatively low, the oscillation period T_o will be much larger, and the gate voltages can be precisely synchronized during the entire period of $\delta t_{d(off)}$.

3.3.3. Simulation Verification of Dynamic Voltage Sharing Using the GBC Method

The analytical calculations are verified against the obtained experimental results. The behavior of the V_{GS} waveforms during the entire $\delta t_{d(off)}$ is verified using Simulink based on Fig. 3.11, which only focuses on the gate circuits of the SiC MOSFET string. The parameters of the simulation model are all extracted from the experiments: The bottom SiC MOSFET has an extra 500 ns turn-off delay compared to the top MOSFET, and the self-inductance of both inductor windings is 4.56 mH. The dynamic input capacitance of the MOSFETs is 289 pF (IMW120R220M1H).

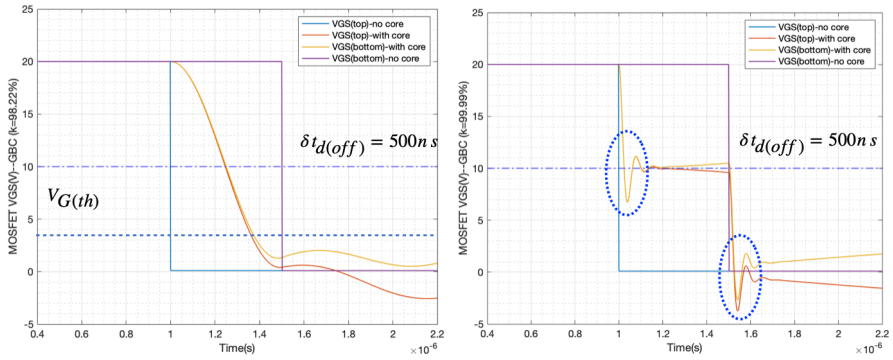


Figure 3.13: V_{GS} waveforms of the two series-connected SiC MOSFETs using GBC method during off-period with inductor k = 98.22% (left) and k = 99.99% (right) performed in MATLAB Simulink

If the coupling factor k has a relatively low value, the leakage inductance L_k has a larger value. Therefore, in Fig. 3.13 (left), the resonant frequency of the gate waveforms f_o is lower than in Fig. 3.13 (right). During the period of $\delta t_{d(off)}$, the resonances (generated by L_k and C_{iss}) will last; thus, both $V_{GS(top)}$ and $V_{GS(bottom)}$ will be dominated by the HF harmonics and react synchronously. If the value of k

is large, almost identical V_{GS} sharing can be observed. The simulated waveforms match quite well with those measured in Fig. 3.9.

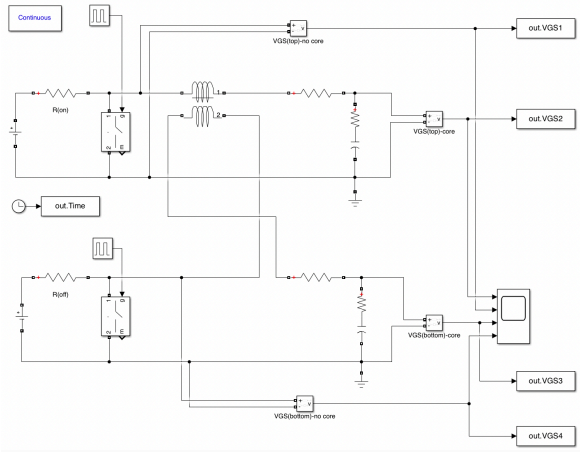


Figure 3.14: The MATLAB Simulink model (gate circuits of two series-connected SiC MOSFETs) built based on the schematic of Fig. 3.11

The balance point at $0.5V_{GS}$ can only appear if L_k is sufficiently small. If k is poor, the gate pulse resonances will last for the entire duration of $\delta t_{d(off)}$, and thus, the $0.5V_{GS}$ balance point is obscured by the oscillations. If k is close to perfect, the resulting f_o is larger. During the period of $\delta t_{d(off)}$, the gate waveforms will first resonate synchronously, but they may deviate for a short period of time after the oscillations have attenuated.

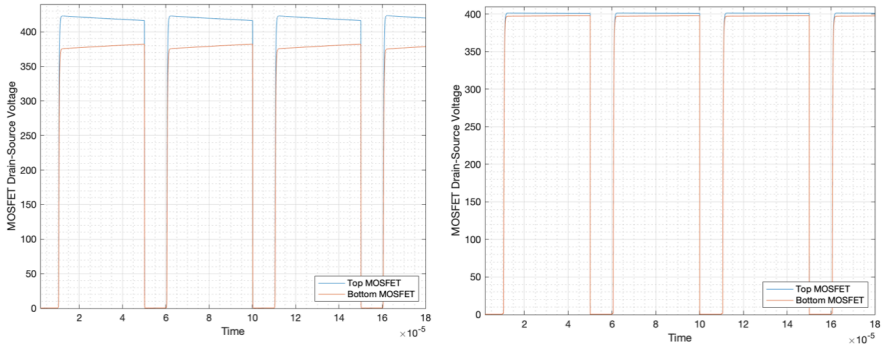


Figure 3.15: V_{DS} waveforms of the SiC MOSFET string using GBC method during off-period with coupled inductor $k = 98.22\%$ (left) and $k = 99.99\%$ (right) in case of $\delta t_{d(off)}$=500 ns (LTspice)

An LTspice simulation model, decipted in Fig. 3.14 is also built based on the schematic of Fig. 3.6 to verify the V_{DS} waveforms. The component parameters are the same as those of the experiments and Simulink simulations. Again, there is an

extra 500 ns turn-off delay in the bottom SiC MOSFET.

The LTspice simulation results show V_{GS} behavior similar to the Simulink model in Fig. 3.13. It should be noted that, if the coupling factor of the gate-coupled inductor is low, the V_{DS} sharing of the SiC MOSFET string is poor. Despite the synchronous gate voltages, the V_{DS} rising slew rates of the MOSFETs are different due to the non-identical gate sink currents ($I_{g(delayed)}$<$I_{g(undelayed)}$), which causes an imbalance in V_{DS}. However, if the value of k is close to 1, the gate sink currents are almost identical. Therefore, balanced V_{DS} sharing can be achieved.

3.4. Hybrid Gate Signal Delay Adjustment Method – Improved RC Snubber Method

The GBC method is solely based on gate signal delay adjustment. Combining GBC with a passive snubber yields the improved RC snubber method. Two different types of improved RC snubber methods are evaluated and validated by experiments and LTspice simulations. Based on the obtained results, the strengths and weaknesses of each method are provided, and a comparison of these two methods is given.

3.4.1. Passive Snubber Circuits

To enhance the V_{DS} sharing of the SiC MOSFET string, passive snubber circuits (e.g., RC and RCD snubbers, as shown in Fig. 3.16) are commonly employed alongside the static balancing resistors R_{st}. While the RCD snubber may increase cost, it offers significantly lower snubber losses than the RC snubber. During MOSFET turn-off, the snubber capacitor C_{sn} is charged through the low-impedance diode D_{sn}. During MOSFET turn-on, it is discharged through the snubber resistor and MOSFET. Thus, the losses induced during turn-off are nearly eliminated. It is important to note that the snubber resistor R_{sn} can provide damping of ringing and voltage spikes on V_{DS} and prevents discharging C_{sn} directly through the MOSFET itself.

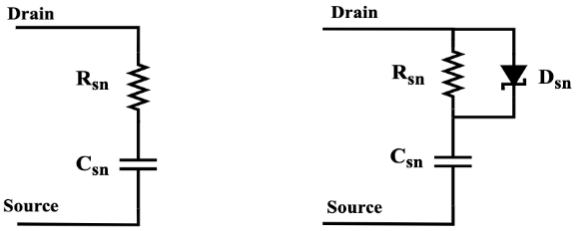


Figure 3.16: RC snubber circuit (left) and RCD snubber circuit (right)

Usually, the tail-current characteristics, shown in Fig. 3.17, will exist in IGBTs during the off-period. These tail currents impact the voltage sharing of the series-connected IGBTs as the value of the tail-period T_{tail} is unpredictable and deviates from one device to another. Since the SiC MOSFETs do not exhibit a tail-current characteristic, no further discussion related to this factor will be provided.

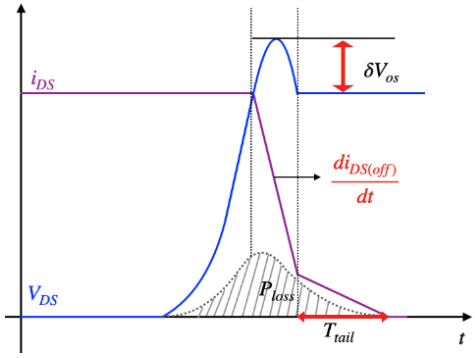


Figure 3.17: V_{DS} and i_{DS} waveform of a IGBT during turn-off period

If the series-connected SiC MOSFETs run under HF applications, the high drain-current slew rate $di_{DS(off)}/dt$ during turn-off period results in a significant voltage overshoot δV_{os}, as shown in Fig. 3.17. The formula for the magnitude of the overshoot is given in (3.15), where L_s stands for the total parasitic inductance of the commutation loop.

$$\delta V_{os} = L_s \cdot \frac{di_{DS(off)}}{dt} \tag{3.15}$$

In [50], Baraia introduces the passive clamping snubber shown in Fig. 3.18 (left). In this passive clamping snubber circuit, the snubber capacitor C_{sn} reduces the V_{DS} rising slew rate, and the presence of R_a accelerates the discharging process of C_{sn}. During the MOSFET off-period, if V_{DS} exceeds the Zener voltage V_z, it gets clamped at V_z. This clamping action is crucial in maintaining the drain-source voltage below the device breakdown.

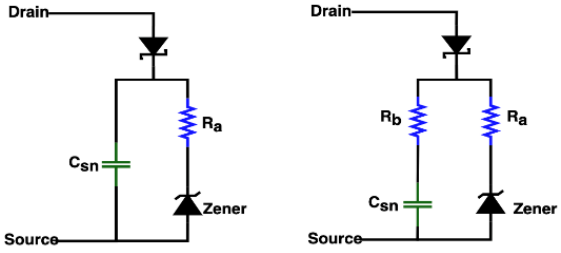


Figure 3.18: Schematic of two types of passive clamping snubber circuit

Furthermore, in [51], Zhang introduces another resistor, R_b, in series with C_{sn}, as shown in Fig. 3.18 (right), which assists in reducing the magnitude of the peak voltage across the snubber capacitor. The Zener diode keeps the voltage imbalance δV_{DS} within the limits, making the entire circuit more reliable and robust.

The four types of passive snubber circuits discussed and evaluated in the following paragraphs all slow down the V_{DS} slew rate of the series-connected SiC MOSFETs to reduce the δV_{DS} generated by $\delta t_{d(off)}$. Usually, better suppression of δV_{DS} can be reached for larger snubber capacitance values. However, to ensure sufficient switching speed and lower switching losses of the SiC MOSFETs, the gate signal delay adjustment method should be combined with the passive snubber circuit.

3.4.2. Improved RC Snubber Method (a)

In [46] and [52], the improved RC snubber method (a) was described. The critical part of this technique is to use a coupled inductor whose primary windings are coupled with the passive snubber circuits to generate a compensation voltage on the secondary winding, which behaves as feedback to the gate, as shown in Fig. 3.19. Through the change in gate voltage, the MOSFET V_{DS} rise slew rate can be altered, and balanced voltage sharing of the SiC MOSFET string can be achieved.

In Fig. 3.19, two coupled inductors are connected to the RC snubber and gate circuits of the SiC MOSFET string. Note that the polarities of the two secondary windings are different. If the bottom SiC MOSFET has an extra 200 ns turn-off delay, the top one will turn off faster, and some capacitive currents will flow through the top snubber circuit. Feedback voltages will be induced on both secondary windings, which are added to the original gate voltages. The feedback voltage of the top SiC MOSFET enhances its overall gate voltage but decreases the slew rate of V_{DS}. In contrast, the feedback voltage of the bottom MOSFET decreases its overall gate voltage but increases the slew rate of V_{DS}.

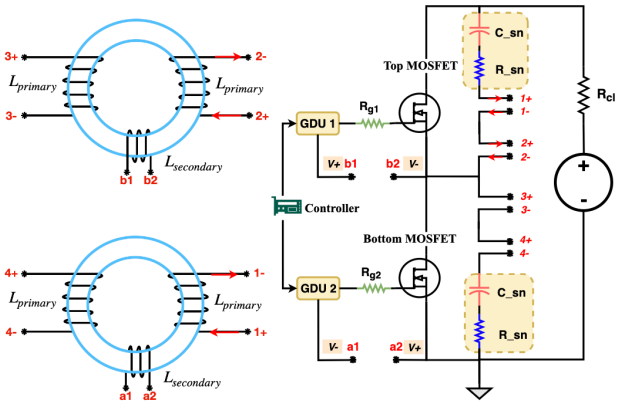


Figure 3.19: Schematic of two series-connected MOSFETs using improved RC snubber method (a)

An LTspice simulation model is built according to the schematic of Fig. 3.19 to verify the voltage-sharing performance. Both coupled inductors have a primary inductance L_p of 880 µH and a secondary inductance L_s of 24 µH with a high coupling factor. The external gate resistance $R_{g(i)}$ is 25 Ω, and the snubber capacitance C_{sn} and resistance R_{sn} are selected as 330 pF and 50 Ω, respectively.

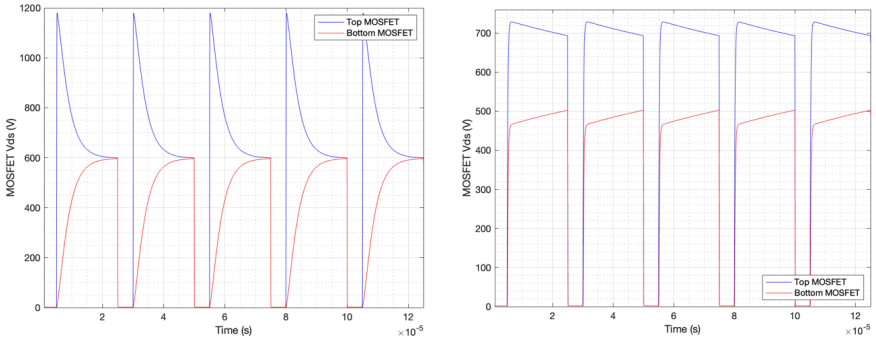


Figure 3.20: V_{DS} sharing of the SiC MOSFET string using a passive RC snubber with an extra 200 ns turn-off delay in the bottom switch without snubber (left) and with snubber (right)

The passive RC snubber circuit can improve the V_{DS} sharing of the two series-connected SiC MOSFETs in case of a large turn-off delay variation. Nevertheless, a considerable voltage imbalance δV_{DS} still remains. With the adoption of RC snubber method (a) in Fig. 3.21, good V_{DS} sharing can be achieved with a maximum imbalance voltage of just 2% of V_{DS}. Comparing Fig. 3.20 to Fig. 3.21 (left), the improved RC snubber (a) shows a significantly improved V_{DS} sharing capability.

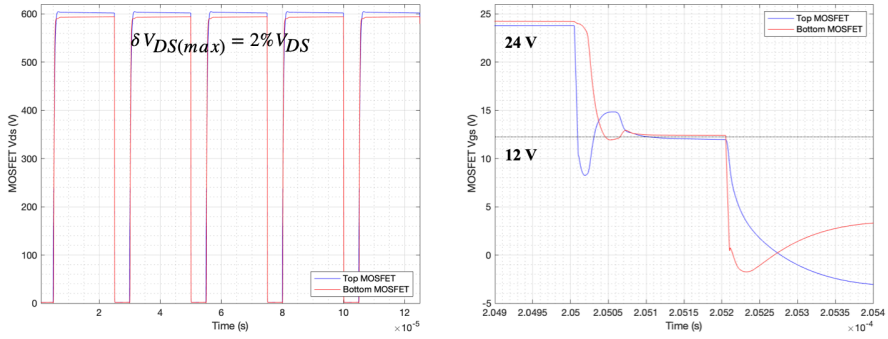


Figure 3.21: V_{DS} (left) and V_{GS} during off-period (right) sharing of the MOSFET string using the improved RC snubber method (a) with an extra 200 ns turn-off delay in the bottom switch with inductor

Fig. 3.21 (right) demonstrates the V_{GS} waveforms of the SiC MOSFET string during the turn-off transition. The variation in gate-source voltage δV_{GS} is almost eliminated using the coupled inductors. Despite slight V_{GS} waveform distortion due to parasitic oscillations, the gate voltages switch almost synchronously and are balanced at $0.5V_{GS}$. If the feedback voltages induced on the secondaries are sufficient, the gate currents can be synchronized. Thus, the gate charge movement velocity of the MOSFET from the string is almost identical and δV_{GS} is suppressed.

In conclusion, the improved RC snubber method (a) results in good V_{DS} sharing of the SiC MOSFET string. The disadvantage, however, is the relatively large number

of required components, which leads to a higher cost (N series-connected MOSFETs require N coupled inductors) and complicated snubber circuit routing. Finally, the scalability of this method (a) is low, which limits the usable input voltage.

3.4.3. Improved RC Snubber Method (b)

Fig. 3.22 shows the schematic of the improved RC snubber method (b), an optimized variant of method (a), applied to two series-connected MOSFET. A four-port coupled inductor links two snubber circuits and two gate circuits. The main difference with method (a) is that only one primary winding is coupled within one snubber branch. Hence, the circuit layout and routing of method (b) are much more straightforward. Moreover, one fewer inductor is required, reducing the total material cost. The polarity of the inductor secondary windings still needs to be different to generate the gate feedback voltages with opposing polarity.

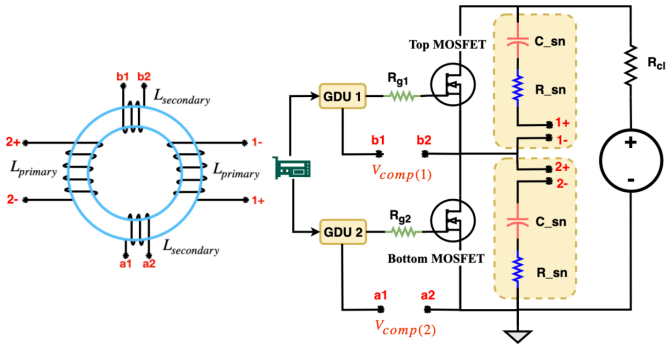


Figure 3.22: Schematic of the two series-connected MOSFETs using improved RC snubber method (b)

Comparing the LTspice simulation results shown in Fig. 3.23 to Fig. 3.24 (left), in case of an additional 200 ns turn-off delay existing on the bottom switch, with the utilization of the four-port inductor, the V_{DS} sharing of the SiC MOSFET string is again excellent. The maximum voltage imbalance is just 1.5% of V_{DS}, which is slightly better than that obtained using method (a). This degree of voltage imbalance is negligible and cannot lead to a device breakdown.

Fig. 3.24 (right) shows the V_{DS} sharing of the SiC MOSFET string during the turn-off delay. After the turn-off of the top MOSFET during the delay period $\delta t_{d(off)}$, the slew rate of $V_{DS(top)}$ (blue) is quite large at the very beginning and then decreases due to the gate feedback voltage $V_{comp(1)}$. Meanwhile, $V_{DS(bottom)}$ (red) remains turned on for around 15 ns and then increases considerably due to the presence of $V_{comp(2)}$. After the delay period, at t_1, the bottom switch will be fully turned off, and the slew rate of V_{DS} will grow significantly. The actual turn-off delay period of the bottom switch has been shortened drastically from 200 ns to 15 ns due to the gate compensation circuits (coupled inductor secondaries).

To conclude, both improved RC snubber methods can achieve near-perfect voltage balancing. Also, the maximum imbalance voltage δV_{DS} is well within the safety

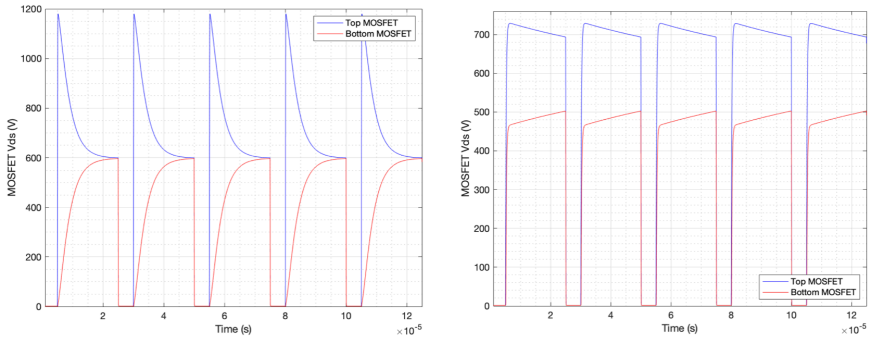


Figure 3.23: V_{DS} sharing of the SiC MOSFET string using the improved RC snubber method (b) with an extra 200 ns turn-off delay in the bottom switch without snubber (left) and with snubber without inductor (right). Repeated from Fig. 3.20 for better comparison with Fig. 3.24.

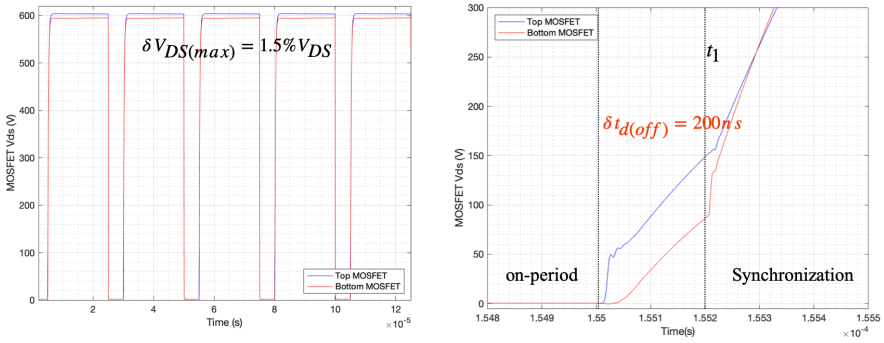


Figure 3.24: V_{DS} (left) and V_{DS} during off-period (right) sharing of the SiC MOSFET string using improved RC snubber method (b) with a 200 ns turn-off delay in the bottom switch with inductor

margin and cannot cause the devices to break down. In [46, 52], the feasibility of the proposed improved RC snubber method (a) has already been verified by experiments, although the applied MOSFET switching delay variation is only 5 ns. Hence, to obtain convincing evidence that the improved RC snubber method (b) also works well, it is validated through experiments with a larger turn-off delay variation.

3.4.4. Experiments Using Improved RC Snubber Method (b) on Four Series-Connected SiC MOSFETs

The schematic of four series-connected SiC MOSFETs using improved RC snubber method (b) is shown in Fig. 3.25. The top two and bottom two MOSFETs can be regarded as equivalent HV switches. Then, these two equivalent HV switches are connected in series. Apart from the four-port coupled inductors, a two-port inductor is also coupled within the RC snubber circuits of those two equivalent switches.

According to the schematic of Fig. 3.25, an LTspice simulation model is built for four series-connected SiC MOSFETs using the improved RC snubber method (b).

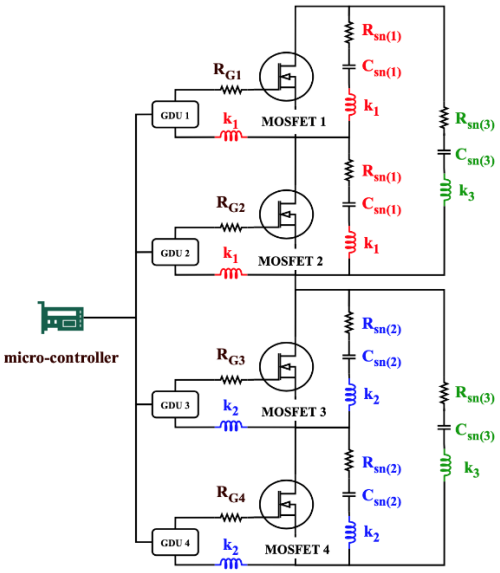


Figure 3.25: Schematic of four series-connected MOSFETs using improved RC snubber method (b)

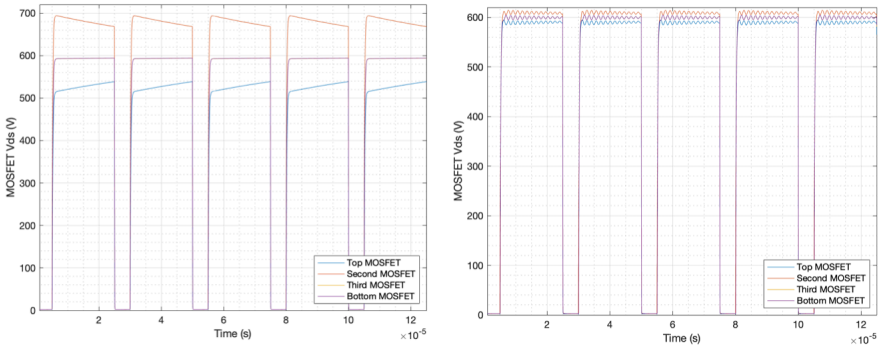


Figure 3.26: V_{DS} sharing of the SiC MOSFET string using improved RC snubber method (b) with snubber but without inductors (left) and with snubber and inductor (right)

The coupling factors of the inductors are set to 99.99%. The primary inductance associated with the snubber circuit is 800 µH, and the secondary inductance associated with the gate circuit is 24 µH. The capacitance of $C_{sn(1)}$ and $C_{sn(2)}$ is 330 pF, and that of $C_{sn(3)}$ is 200 pF to guarantee a sufficient voltage slew rate. MOSFETs 3 and 4 have an extra 125 ns turn-off delay, and MOSFET 1 has an additional 250 ns turn-off delay compared to MOSFET 2. Furthermore, the external gate resistance is $25\,\Omega$, and the snubber resistance of the snubber circuits is $50\,\Omega$.

Fig. 3.26 indicates the V_{DS} sharing of the four series-connected SiC MOSFETs before and after the connection of the three inductors, performed in LTspice simu-

lations. Comparing Fig. 3.26 (right) to (left) shows that nearly perfect drain-source voltage sharing can be achieved by means of these three coupled inductors. Therefore, the improved RC snubber method (b) is verified to have significantly improved the voltage-sharing capability, even for more than two series-connected MOSFETs.

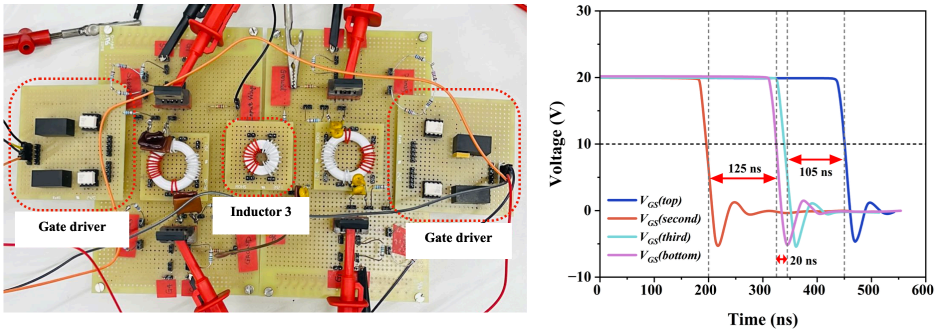


Figure 3.27: Experimental set-up of the four series-connected SiC MOSFETs (left) using improved RC snubber method (b) and measured V_{GS} waveforms during off-period (right)

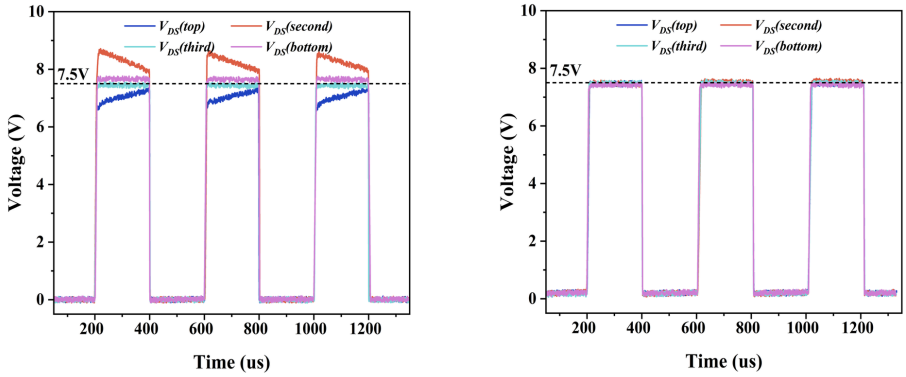


Figure 3.28: Measured V_{DS} sharing of the four series-connected SiC MOSFETs using the improved RC snubber (b) method without coupled inductors (left) and with coupled inductors (right)

Fig. 3.27 (left) illustrates the experimental implementation of the same circuit. The gate triggering pulses are shown in Fig. 3.27 (right): MOSFETs 3 and 4 both have two micro-controller clock cycles' turn-off delay variation (125 ns), and MOSFET 1 has four extra micro-controller clock cycles' turn-off delay (250 ns) compared to MOSFET 2. An extra 20 ns switching delay variation is found between the V_{GS} waveforms of MOSFETs 3 and 4. This delay difference is generated by the parameter variation in the gate drivers, the difference in the connection wire length, and the parasitic parameters. Therefore, the MOSFETs have different switching delays.

Comparing Fig. 3.28 (left) to (right), it can be concluded that the coupled inductors can help to significantly improve the V_{DS} sharing of the four series-connected

SiC MOSFETs, even though there is turn-off delay variation. From Fig. 3.28 (right), the V_{DS} sharing among the MOSFET string is nearly perfect, proving the functionality of the improved RC snubber method (b) and validating the feasibility of the circuit in Fig. 3.25.

As a result, based on Fig. 3.26 (right) and Fig. 3.28 (right), the balanced voltage sharing among the series-connected SiC MOSFETs can be implemented by means of the improved RC snubber method (b). However, the biggest challenge is the insulation design of the coupled inductors, as shown in Fig. 3.25. Inductor 3 must withstand the whole input voltage V_{in}, and thus is more sensitive to breakdown. Another drawback of this method is that the number of series-connected MOSFETs cannot be arbitrary but should be a power of two ($N = 2^x$). This imposes strict limitations on the applied voltage of the HV switch.

3.5. Gate-Drain Zener Clamping Circuits

The Zener clamping method is one of the most effective solutions for the unbalanced V_{DS} sharing of the series-connected SiC MOSFETs. Generally, the Zener clamping circuit comprises Zener diodes and some passive components, which are applied between the gate-drain terminals to limit the overvoltage across the SiC MOSFET. The Zener clamping method only addresses the overvoltages caused by voltage imbalance, thereby protecting the semiconductor devices. For optimal results, it is recommended to use this method in conjunction with passive snubber circuits to achieve superior static and dynamic voltage sharing.

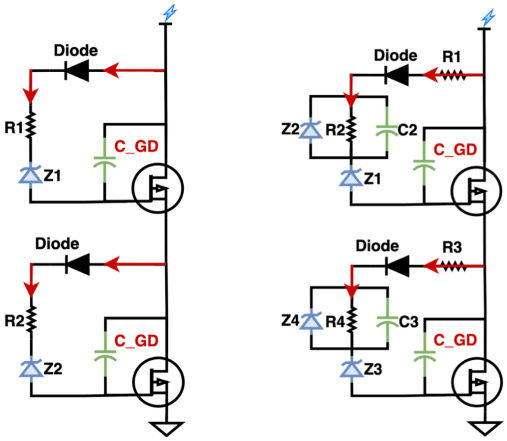


Figure 3.29: Schematic of two series-connected SiC MOSFETs using the basic (left) and optimized (right) Zener clamping circuits

The basic Zener clamping method was first proposed in [53], requiring a Zener diode to clamp the V_{DG} of the corresponding MOSFET as a means of overvoltage control. An optimized Zener clamping method was suggested in [54] to achieve satisfactory operation with a high input voltage for the MOSFET string. Multiple Zener

diodes are connected in series to increase the clamping voltage of every Zener branch. Multiple series-connected diodes are used because the commercially available Zener diodes are limited to about 400 V. It can be noted that a 400 V Zener diode has a maximum continuous current of 7 mA with a power loss of approximately 0.25 W.

In the basic Zener clamping method, as depicted in Fig. 3.29 (left), the Zener diodes Z_1 and Z_2 clamp the drain-gate voltages of their respective MOSFETs to the Zener voltage. If the bottom MOSFET experiences some extra turn-off delay, $V_{DG(top)}$ will rise faster than $V_{DG(bottom)}$, while the top MOSFET is switching off. When the value of $V_{DG(top)}$ exceeds the Zener voltage, it gets clamped to V_{Z1}, thus preventing the breakdown of the top MOSFET.

In practice, the SiC MOSFET reverse capacitance C_{rss} decreases drastically with increasing V_{DS} [55, 56]. Since the bottom SiC MOSFET has some extra turn-off delay, after the delay period $\delta t_{d(off)}$, $V_{DG(top)}$ is larger than $V_{DG(bottom)}$, but $C_{DG(top)}$ is smaller than $C_{DG(bottom)}$. Hence, $dV_{DG(top)}/dt$ gradually increases, and the variation between $V_{DG(bottom)}$ and $V_{DG(top)}$ becomes more noticeable.

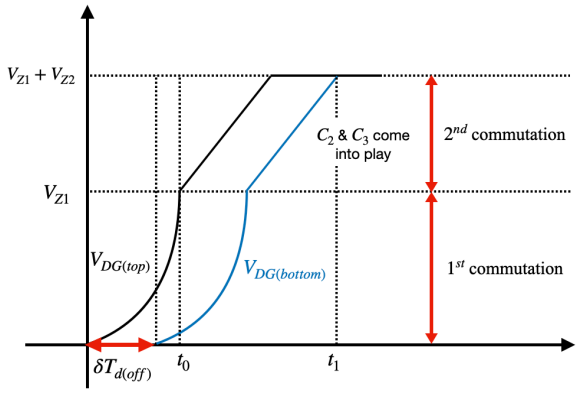


Figure 3.30: Operation principle of two series-connected MOSFETs for optimized Zener clamping method (bottom switch delayed)

In [57, 58], an optimized Zener clamping method was proposed, see Fig. 3.29 (right). Suppose the bottom MOSFET still has some $\delta t_{d(off)}$ during the 1^{st} commutation period, shown in Fig. 3.30. In that case, the $dV_{DG(top)}/dt$ will grow rapidly before reaching the first-step Zener clamping voltage V_{Z1} because $C_{rss(top)}$ reduces when $V_{DG(top)}$ increases. If the value of $V_{DG(top)}$ is larger than V_{Z1}, during the 2^{nd} commutation period, the capacitor C_2 plays a crucial role in slowing down the $dV_{DG(top)}/dt$ to 'wait' for the growth of $V_{DG(bottom)}$. Thus, the variation between $V_{DG(top)}$ and $V_{DG(bottom)}$ will decrease. The optimized Zener clamping method allows the beginning of the commutation to be as quick as possible and slow down at the end. Furthermore, using capacitors C_2 and C_3 can minimize the effect of varying C_{DG} with voltage and between MOSFET devices. During the 2^{nd} commutation period, the total capacitor C_{tot} used for slowing down the dV_{DS}/dt (dV_{DG}/dt) is (C_2+$C_{DG(top)}$) or (C_3+$C_{DG(bottom)}$).

Proper component selection is critical when using the optimized Zener clamping method. Referring to Fig. 3.29 (right), if the expected applied voltage of each SiC MOSFET under balanced V_{DS} sharing is V_a, which is 60% of the MOSFET maximum blocking voltage ($V_{DG} \approx V_a = V_{DS}$), the voltage of Z_1 should be slightly smaller but close to $0.5V_a$. Additionally, the sum of V_{Z1} and V_{Z2} is the total Zener voltage $V_{Z(tot)}$, which should be slightly smaller but close to V_a. These selection criteria are such because some voltage will be dropped over the resistor R_1 and R_3, connected in series with the Zener diodes. Generally, the value of $V_{Z(tot)}$ is chosen as V_a.

During the static balancing period (after t_1), the resistors R_2 and R_4 shown in Fig. 3.29 (right) are dominant and limit the current through the Zener branch. The current I_r that flows through R_2 or R_4 should be at least 10 times the drain leakage current I_{DSS} found on the datasheet of the selected SiC MOSFET.

$$R_2 = \frac{V_a - V_{Z1}}{I_r} = \frac{V_a - V_{Z1}}{10 \cdot I_{DSS}} \tag{3.16}$$

$$C_2 \leq \frac{T_{on}}{(3or5) \cdot R_2} \tag{3.17}$$

During the 2^{nd} commutation period (from t_0 to t_1), the capacitors C_2 and C_3 become dominant and slow down the $dV_{DG(top)}/dt$ and $dV_{DG(bottom)}/dt$, if V_{DG} is larger than V_{Z1}. When the values of R_2 and R_4 are determined based on (3.16), the capacitance of C_2 and C_3 can be calculated from (3.17). The time constant of the branch is chosen to be less than 3-5 times the on-period T_{on}.

3.5.1. Experiments with the Optimized Zener Clamping Method and Three Series-Connected MOSFETs

Fig. 3.31 illustrates the experimental setup used to verify the aforementioned optimized Zener clamping method. The top SiC MOSFET has an additional 560 ns (8 micro-controller clock cycles) turn-off delay compared to the other SiC MOSFETs, and a switching frequency of 2.5 kHz.

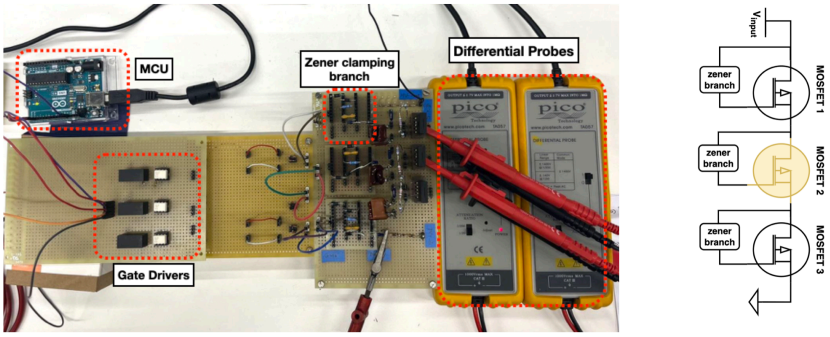


Figure 3.31: Set-up of the three series-connected MOSFETs using Zener clamping method

As seen in Fig. 3.32 (left), balanced static V_{DS} sharing can be achieved with Zener clamping in case of a large $\delta t_{d(off)}$. However, as shown in Fig. 3.32 (right), completely balanced dynamic V_{DS} sharing has yet to be achieved. The performance of the V_{DS} wavefronts matches the working principle of the optimized Zener clamping method: the V_{DS} first grows rapidly with a high slew rate when it is lower than the first Zener voltage V_Z. After this, the slew rate decreases considerably if the value of V_{DS} is larger than V_Z owing to the capacitors present in the Zener branches. If the value of V_{DG} climbs above $V_{Z(tot)}$, it will be clamped, preventing the destruction of the MOSFET due to overvoltage.

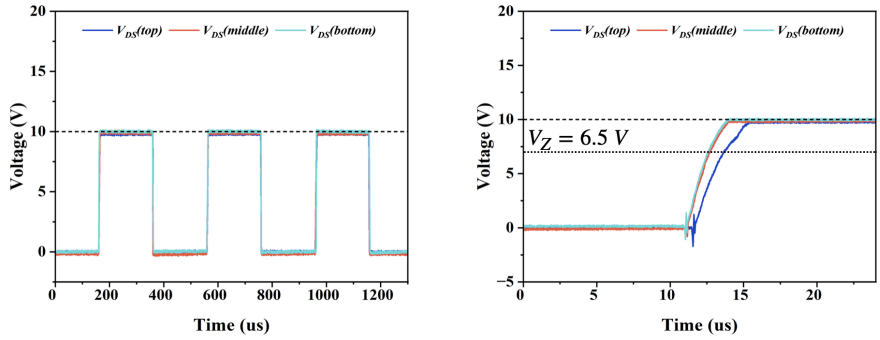


Figure 3.32: V_{DS} overall waveforms (left) and V_{DS} waveforms during off-period (right) of the SiC MOSFET string with optimized Zener clamping circuits ($\delta t_{d(off)}$ = 560 ns)

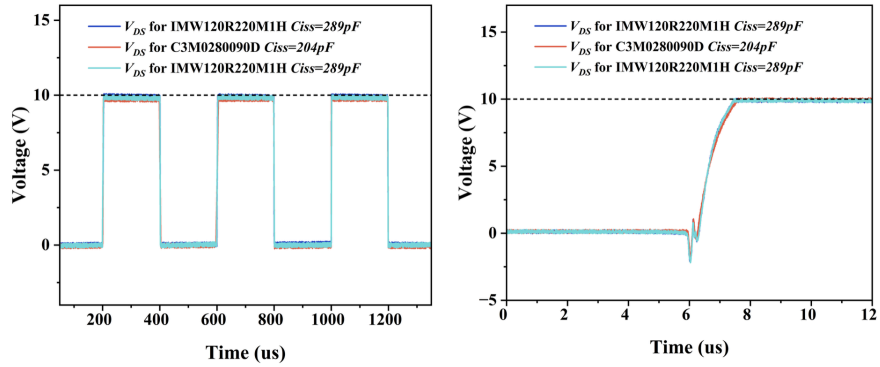


Figure 3.33: V_{DS} overall waveforms (left) and V_{DS} waveforms during off-period (right) of the SiC MOSFET string with optimized Zener clamping circuits (δC_{iss} = 85 pF)

Among the SiC MOSFET string, if there is no $\delta t_{d(on)}$ or $\delta t_{d(off)}$ but some parasitic parameter variation δC_{iss} exists, balanced V_{DS} sharing can still be achieved. Figure. 3.33(left) illustrates this in the case of $\delta C_{iss} = 85\,pF$, where the middle SiC MOSFET is replaced by another type, C3M0280090D, with a smaller C_{iss} compared to the selected switch type IMW120R220M1H. From Fig. 3.33 (right), it should be

noted that during the MOSFET off-period, the slew rates of $V_{DS(top)}$, $V_{DS(middle)}$, and $V_{DS(bottom)}$ are almost identical, guaranteeing balanced voltage sharing. Thus, the small amount of δC_{iss} in the MOSFET string is not considered as the leading cause of voltage sharing imbalance.

To summarize, the optimized Zener clamping method can successfully clamp the overvoltage caused by $\delta t_{d(off)}$ to avoid SiC MOSFET breakdown. However, this method cannot improve the dynamic voltage sharing of the SiC MOSFET string. This method only requires low-cost components, which results in low material costs. As the voltage level increases, more losses will be induced in the Zener branch, consisting of some static dissipation during the off-time, as well as (larger) dynamic losses associated with the clamping current.

3.6. Design of Isolated HV Gate Drivers

While presented methods can indeed achieve statically and dynamically balanced voltage sharing, another big challenge must be addressed. When N MOSFETs are connected in series, as shown in Fig. 3.34, the required gate driving potential for each consecutive switch increases. The gate terminal voltage potential is given in formula (3.18). For each MOSFET, the potential of the gate $V_{G(i)}$ and source $V_{S(i)}$ terminals is almost the same. From (3.18), it is clear that the gate potential of the MOSFETs close to the input lead is high, comparable to the HV input voltage V_{input}.

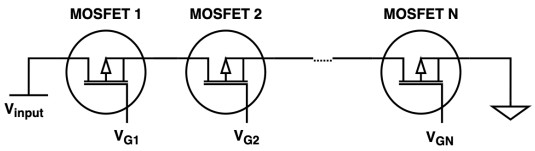


Figure 3.34: Basic schematic of multiple (N) series-connected SiC MOSFETs

In this scenario, to avoid the breakdown of the gate drivers, those with a high isolation voltage level are required. The HV gate drivers (e.g., 8-10 kV level) are not yet commercialized, and the price of the commercial available ones are excessively high. Therefore, the design of such a HV gate driver is essential to achieve a cost-effective HV switch with series-connected MOSFETs.

$$V_{G(i)} = \frac{N-i}{N} \cdot V_{input}; (i = 1...N) \tag{3.18}$$

The proposed solution for enhancing the isolation voltage of the gate driving circuit is to replace the isolated gate driver with a non-isolated driver, shifting the isolation barrier to an optocoupler and isolated DC/DC converter. Commercial optocouplers are available with an isolation voltage that is much higher than that of isolated gate drivers (beyond 20 kVDC). In addition, the propagation delay variation of non-isolated drivers is typically better. This concept is illustrated in Fig. 3.35, where the non-isolated gate drivers are implemented using a BJT push-pull stage with split output.

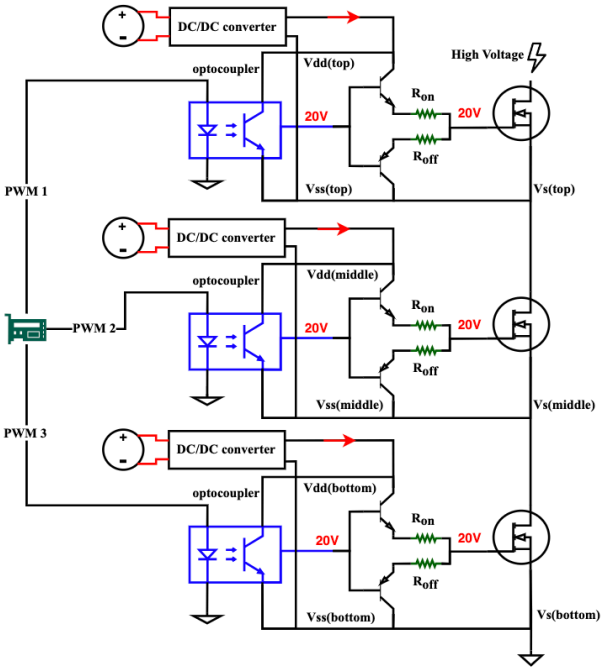


Figure 3.35: Schematic of the SiC MOSFET string driven by the general HV gate driver circuits

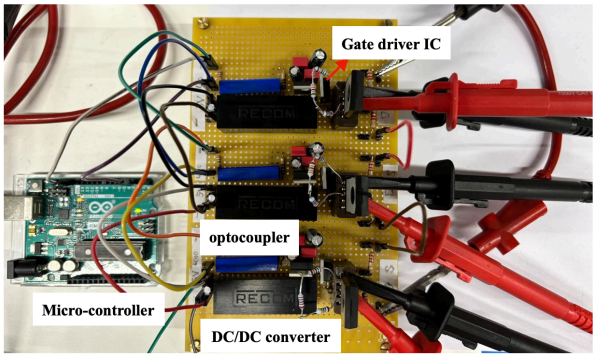


Figure 3.36: The prototype of the three series-connected MOSFETs controlled by HV gate driving circuit

A prototype (Fig. 3.36) is built with three series-connected SiC MOSFETs and optically isolated HV gate drivers according to the schematic in Fig. 3.35, using an IXDD630MXI non-isolated driver, OPI1268S optocoupler, and RHV2-0512D isolated DC/DC converter. While the DC/DC converter has an isolation level of 20 kV for 1 s, destructive tests have shown that its maximum continuous working voltage is about 8 kV, thus limiting the input voltage of the SiC MOSFET string.

As shown in Fig. 3.37 (left), the static and dynamic voltage sharing is relatively good during the SiC MOSFET off-period, but some imbalance remains. This is due to the delay variation in the input PWM signal propagation (e.g., wire length differences) and the variation in gate circuit parameters and component characteristics. Hence, it is still recommended to use one of the previously described dynamic balancing techniques. Alternatively, the gate circuit components could be binned and matched during production, allowing for the operation without a dynamic balancing technique.

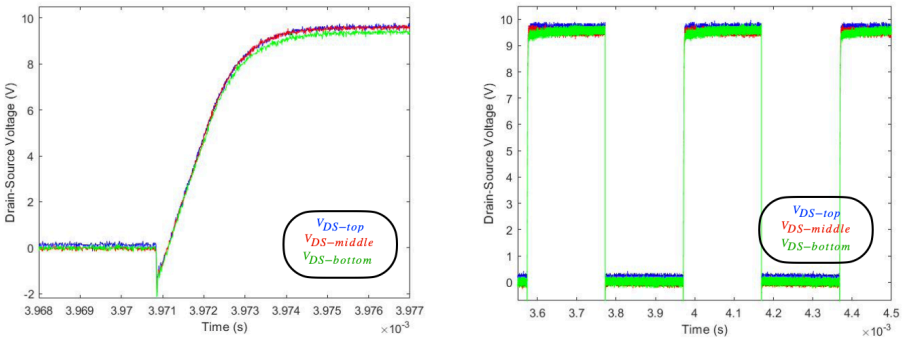


Figure 3.37: Measured V_{DS} waveforms during off-period (left) and overall V_{DS} waveforms (right)

The results shown in Fig. 3.37 are obtained from low-voltage tests. Tests are also performed with an input voltage of 2.8 kV (no current limiting resistors), and satisfactory output performance is obtained, as shown in Fig. 3.38. The output voltage was measured using an HV probe. Performing drain voltage measurement on every SiC MOSFET during HV operation was not possible because the commercial differential probes were limited to an isolation level of 1.4 kV.

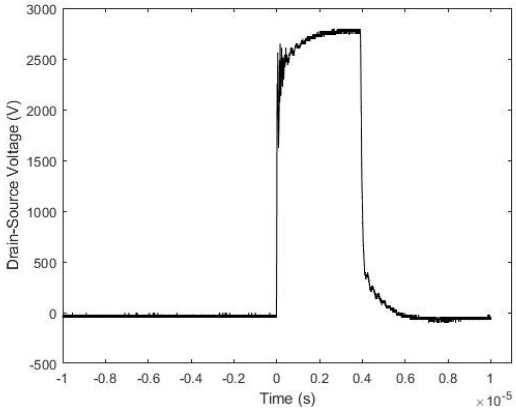


Figure 3.38: Measured V_{DS} waveform of the entire SiC MOSFET string with a voltage of 2.8 kV

3.7. A Magnetically Isolated HV Gate Driver

The optically isolated gate driver concept is quite simple and provides robust control of the MOSFET string. If the number of series-connected MOSFETs is large and the input voltage is high, the optocouplers and DC/DC converters must have a high insulation level, which results in a bulky and expensive construction. A magnetically isolated gate driver is proposed to address these issues [59]. Similar approaches have resulted in HV switches with blocking voltages of 5 to 15 kV [60, 61].

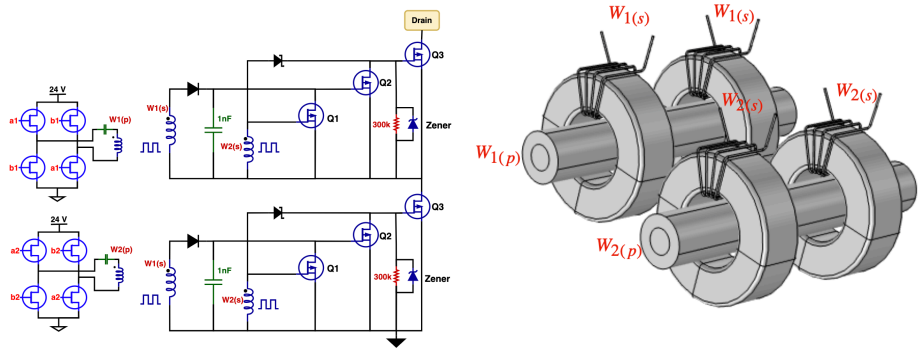


Figure 3.39: Schematic of the magnetically isolated gate driver based two series-connected MOSFETs (left) and two gate-coupled transformers (right)

Fig. 3.39 (left) presents the schematic of the magnetically isolated driver. The key element of this method is the use of two gate-coupled transformers. One transformer is for turning on, while the other is for turning off the HV MOSFET. Each transformer features an HV-insulated wire as the primary winding, with the secondary winding wound on the toroidal cores as shown in Fig. 3.39 (right).

The construction shown in Fig. 3.39 allows for the synchronous delivery of the gate pulses to the corresponding auxiliary switches (Q_1 or Q_2). Therefore, the contribution of turn-on and turn-off delay variation δt_d caused by propagation path differences is eliminated. As with the optically isolated gate driver, the isolation barrier is moved from the driver circuitry to the transformers. If an HV-insulated wire is used for the primary winding, it can handle high input voltages applied to the HV switch.

To avoid saturation of the toroidal cores, the pulses applied to the transformer primary wires $W_{1(p)}$ and $W_{2(p)}$ should be bipolar. Furthermore, for the proper operation of the HV MOSFETs (Q_3), the transformer input pulses delivered to their corresponding auxiliary switches Q_1 and Q_2 should be complementary. That is, the turn-on and turn-off signals are modulated using on-off keying, as shown in Fig. 3.40. Because the waveform is bipolar with a frequency that is independent of the desired on/off timing, there is no risk of core saturation and arbitrarily long on-times can be achieved.

In a practical implementation, the coupling factor k of the transformers is poor, measured at around 50%. The value of k will reduce for an increasing number of

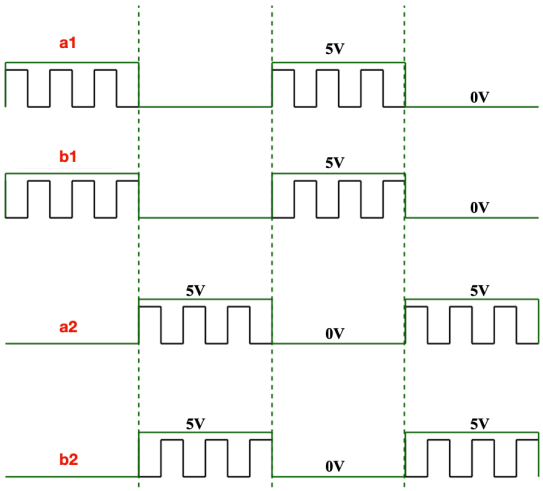


Figure 3.40: Modulation waveforms for the generation of the transformer input pulses. The desired output waveform (in green) is modulated with on-off keying.

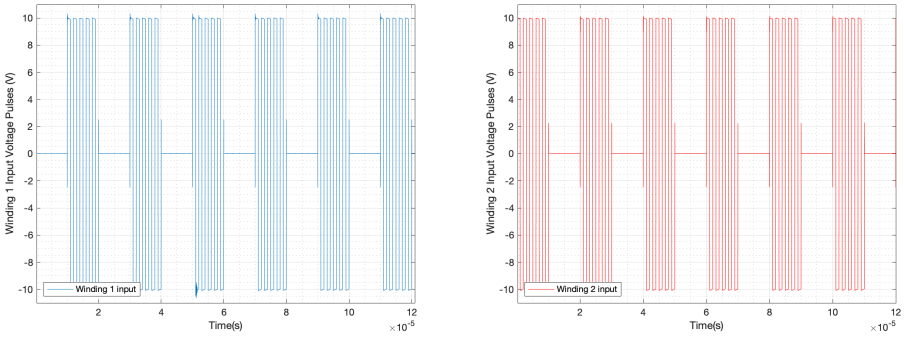


Figure 3.41: The desired bipolar and complementary modulation waveforms (the input pulses of the gate-coupled transformers shown in 3.39)

switches (increasing primary winding length). For each gate-coupled transformer, the coupling of the primary wire to the toroidal cores will also vary slightly owing to geometrical differences. Therefore, a compensation capacitor C_p should be connected in series with the primary wire to compensate for the leakage inductance L_k. This increases the transformer efficiency and allows the transformer to be operated at high frequency in the resonance mode.

The modulation waveforms (a_1, b_1, a_2, and b_2) created by the micro-controller, as depicted in Fig. 3.40, will be delivered to the low-voltage H-bridges of Fig. 3.39 (left) to convert these unipolar waveforms into bipolar waveforms with the amplitude of 24 V. After that, these resulted waveforms will become complementary

shown in Fig. 3.41, which are filtered to recover the desired gate waveform and applied to the auxiliary switches.

The modulated waveforms applied to the primary windings 1 and 2 are complementary, meaning that pulses will be present on $W_{1(s)}$ or $W_{2(s)}$, but not both simultaneously. When pulses are present on $W_{1(s)}$, these are rectified and sent to Q_2, which forces the HV MOSFET Q_3 to be in the off-state by pulling its gate low. On the other hand, when pulses are present on $W_{2(s)}$, these force Q_2 to be off and simultaneously deliver charge to the gate capacitor C_{iss} to turn on Q_3. This allows for synchronous switching of the HV MOSFETs with only a minor impact by the parasitic properties of the circuit.

3.7.1. LTspice Simulations of the Magnetically Isolated HV Gate Driver

Fig. 3.42 illustrates the schematic of the magnetically isolated gate driver with three series-connected SiC MOSFETs in LTspice. The two gate-coupled transformers are utilized to trigger the three series-connected SiC MOSFETs with complementary bipolar gate pulses. In the LTspice simulation model, L_7 denotes the primary, and L_4, L_5, L_6 are the secondary windings of transformer W_1; L_8 denotes the primary, and L_1, L_2, L_3 are the secondary windings of W_2. For each transformer, the driving pulses will be sent to its primary winding and then transferred to the secondary windings synchronously. These driving pulses in the secondary windings control the auxiliary gate-side power switches (U_1, U_4, U_7 and U_2, U_5, U_8) for switching the main MOSFETs. As shown in Fig. 3.42, the coupling factors of the windings corresponding to different main MOSFETs are not identical (k_{top} is 0.5, k_{middle} is 0.49 and k_{bottom} is 0.51). This non-ideality results in a slight imbalance in the drain-source voltages.

Consequently, the magnetically isolated gate driver-based SiC MOSFET string requires fewer components than other balancing methods, and therefore, a compact HV switch size can be achieved. Moreover, the scalability of this method is high since only two transformers with an arbitrary number of secondaries are required. The main disadvantage of this method is the poor coupling factor k of the transformers, which may generate some losses. However, applying a compensation capacitor at the primary side of the transformer can solve this issue. As shown in Fig. 3.43, good V_{DS} balancing can still be achieved with a poor transformer coupling factor. The experimental results based on this type of gate driver will be presented in future paper [59].

Similar to the optically isolated HV gate driver, other balancing techniques can be applied to further improve voltage sharing among the MOSFET string. However, the parameter variation ($\delta t_{d(on)}$, $\delta t_{d(off)}$ and δC_{iss}) of the circuit components is usually too low to generate a voltage imbalance on a level that would be destructive to the MOSFETs.

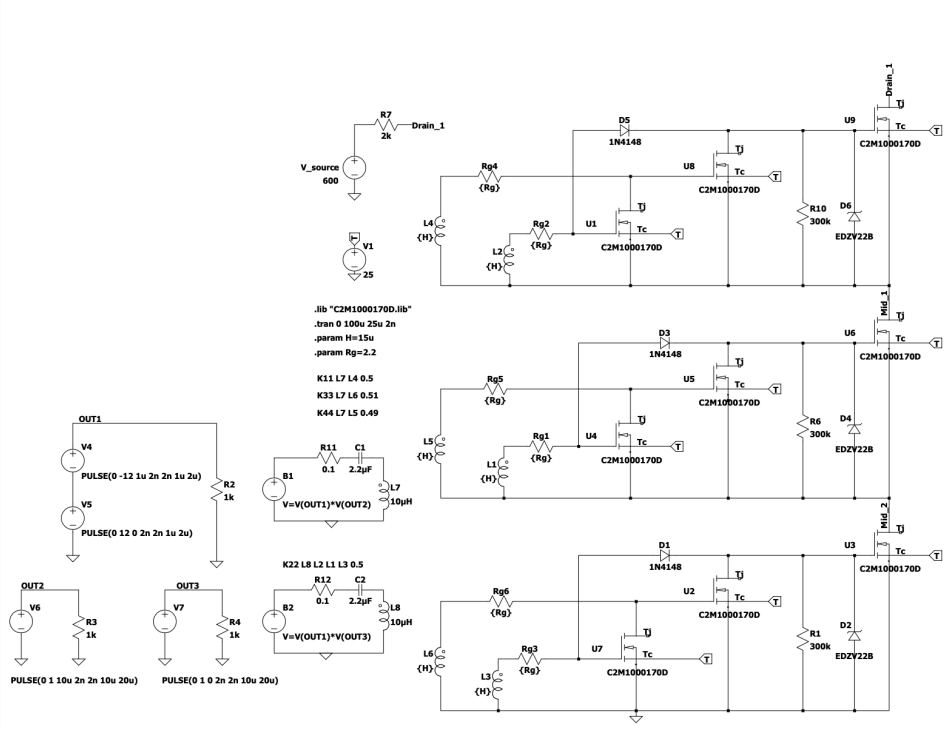


Figure 3.42: Schematic of the magnetically isolated HV gate driver based three series-connected SiC MOSFETs

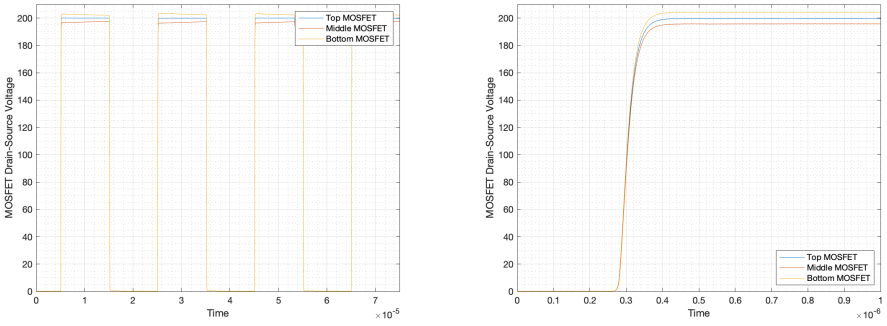


Figure 3.43: V_{DS} overall waveforms (left) and V_{DS} during turn-off period (right) of the magnetically isolated gate driver based SiC MOSFET string

3.8. Summary of Chapter 3

In this chapter, four techniques have been discussed to ensure balanced V_{DS} sharing of the series-connected SiC MOSFETs. Satisfactory static balancing is achieved

using balancing resistors at the cost of additional static power dissipation. The following methods were evaluated to achieve dynamic balancing during the switching transients: (i) the gate-balancing core method, (ii) improved RC snubbers, and (iii) the Zener clamping method.

For HV applications, the gate-balancing core method proves to be a practical solution, offering good output performance. It ensures a short V_{DS} rise time and excellent V_{DS} sharing, even in the presence of a considerable $\delta t_{d(off)}$. The GBC method and the improved RC snubber method (b) can perform well in relatively low-voltage applications owing to their excellent voltage-balancing capability. However, it must be noted that improved RC snubber methods face challenges at higher input voltage levels owing to the insulation requirements on the balancing transformer, which must withstand the entire stage voltage.

Furthermore, the research evaluates two types of high-voltage gate drivers and their ability to maintain balanced voltage sharing, even at high input voltage levels. The suitability of the techniques are assessed through experiments and LTspice simulations. For series-connected SiC MOSFETs with an input voltage lower than 8 kV, the optically isolated gate drivers discussed in Section 3.6 are recommended due to its lower propagation delay and ease of implementation. If the delay times of the gate driver components are not matched, one of the V_{DS} balancing techniques should be used in conjunction with the HV gate driver to ensure balanced drain-source voltage sharing. For input voltages exceeding 8 kV, the magnetically isolated gate driver demonstrated in Section 3.7 is recommended due to its small size and lower material cost. This is mainly because the gate coupling transformers can easily be extended to such voltage levels. Despite its potential, this gate driving technique is still in the developmental stages and is not currently suitable for immediate implementation in the required H-bridge. In the design of the HV H-bridge module, the aforementioned optically isolated gate drivers are employed. The maximum output voltage (U_{out}^{max}) of the CHB based HV-AWG is approximated at 8 kV.

To further simplify the SiC MOSFET string and ensure balanced static and dynamic drain-source voltage sharing, careful sorting, binning, and matching of the SiC MOSFETs, optocouplers, non-isolated gate drivers, and other passive components could be undertaken prior to assembly. If executed correctly, this process could eliminate the need for V_{DS} balancing, leading to a reduction in size and cost of the series-connected MOSFET. Finally, it is recommended to cast the series-connected SiC MOSFETs in epoxy resin to prevent the occurrence of partial discharges that may otherwise occur at various locations in the circuit.

4

MFT Insulation System Design

To design a reliable insulation system of the MFT integrated within the HV-AWG, it is essential to first obtain the lifetime curves of the insulation material for different frequencies. These curves help determine the permissible field strength and the appropriate thickness of the insulation material. Additionally, they assist in selecting sufficient electric field grading for the MFT design. Although the breakdown and lifetime curves of various insulation materials have been extensively studied for 50 Hz AC [62, 63], the effects of frequency and voltage waveform on insulation degradation still remain inconclusive.

In general, it is concluded that when partial discharges (PDs) are present, the insulation lifetime L_f decreases with the increase of working frequency ($L_f \propto f^{-k}$). Factor k is obtained to be 1 according to [62] and less than 1 (typically between 0.6-0.8) based on [64]. Faster rise time of the voltage pulses, in case PDs are present, results in lower lifetime and higher amplitude of PDs [63, 65]. When PDs exist, the lifetime increases if the duty cycle of the applied voltage decreases [66, 67]. When PDs are not present, there are number of other factors that impact the lifetime, such as peak and rms value of the voltage waveform, frequency, temperature, harmonics content. In [68], Cavallani proposed formula (4.1) that relates the lifetime to the voltage peak, voltage rms and harmonics content. According to experimental results, **peak voltage** has the most significant impact on insulation lifetime.

$$L_f = L_0 \cdot K_p^{-n_p} \cdot K_{rms}^{-n_{rms}} \cdot K_s^{-n_s} \tag{4.1}$$

Higher frequencies or harmonic content result in additional dielectric loss, potentially leading to overheating [65, 69, 70]. A comparison of the impact of overtemperature and the peak-to-peak voltage value is presented in [68], revealing that temperature has a lesser effect compared to the peak-to-peak applied voltage. The lifetime of insulation decreases with increasing frequency [71] and slew rate. Reference [72] proposed a formula (4.2) that relates lifetime and frequency, where

L_1 and f_1 are the reference lifetime and frequency, respectively. To accurately determine the aging curves, **ramp sinusoidal breakdown** tests are conducted on the insulation samples (DUTs) to identify the range of breakdown strength. Subsequently, specific field strengths, close to the range median, are selected for HV accelerated aging tests of the insulation samples.

$$L_f = L_1 \cdot \left(\frac{f_1}{f}\right)^{\gamma} \tag{4.2}$$

4.1. Oil-Impregnated Paper Dielectric Investigation[1]

Various types of insulation materials, such as paper insulation, epoxy, polyamide film, and polypropylene, are potential candidates for the insulation system of MFT [73]. However, designing an insulation system for MFT using dry-type insulation materials poses significant challenges owing to the heat dissipation issues. A viable alternative is the liquid-immersed MFT. The properties of oil-impregnated paper (OIP) insulation systems have been thoroughly investigated at 50 Hz and DC in the existing literature [74]. In this section, the breakdown strength and lifetime of OIP are examined and compared at 50 Hz and 1500 Hz. The lifetime curves of OIP are plotted, and the parameters of these curves (slope and y-intercept) are compared between the two target frequencies.

4.1.1. OIP Sample Preparation

In this study, mineral oil, type Nynas Nytro Taurus is used as the impregnating medium. The paper used is Tervakovski cable paper with an average thickness of 0.15 mm. The paper samples were impregnated inside a BINDER VD 53 vacuum oven. A large paper sheet was first cut into small circular pieces suitable for the test set-up. The detailed impregnation procedure is as follow:

- Paper samples were dried at $120°C$ for 24 h
- Oven temperature was reduced gradually to $60°C$, the chamber was filled with dry nitrogen and oil container was placed into the chamber. Vacuum pump was turned on and the pressure of chamber was lowered to 5 mbar and kept at that level. Both oil and paper samples were vacuum dried (5 mbar) at $60°C$ for another 24 h.
- The chamber was filled with dry nitrogen and the paper samples were placed inside oil container. The paper samples were impregnated under vacuum at $60°C$ for 24 h.
- The heater was turned off and the oil paper samples were left inside vacuum chamber to cool down.

[1] W. Zhao and M. G. Niasar, "Aging of oil-impregnated paper at different frequencies," 2021 IEEE International Conference on the Properties and Applications of Dielectric Materials (ICPADM), Johor Bahru, Malaysia, 2021, pp. 430-433, doi: 10.1109/ICPADM49635.2021.9493911.

After the impregnation processes, the OIP samples should always be kept below the oil level inside a sealed desiccator to limit moisture ingress. Prior to each experiment, required number of samples together with sufficient amount of oil were transferred to another glass container from which the samples were taken and placed between the electrodes of the test setup.

4.1.2. Experimental Set-up Preparation

A 30 kV Trek amplifier is used to generate high voltage at different frequencies. The Trek amplifier is equipped with an internal voltage divider which is used to measure its output voltage. The input signal is produced by a TENUMA 72-14111 function generator. The electrodes are made of stainless steel with a diameter of 40 mm and rounded edges of 3 mm radius. The support structure is made of Teflon and is held together by Nylon screws and bolts. Fig. 4.1 illustrates the experimental set-up.

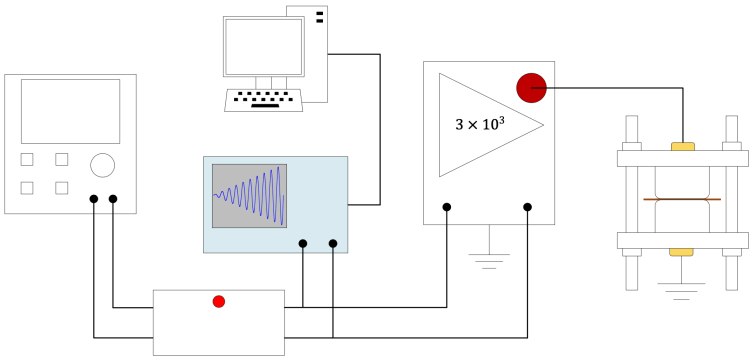


Figure 4.1: Experimental setup used to perform the ramp sinusoidal breakdown and HV accelerated aging tests of the OIP samples

Even though the Trek amplifier has its in-built fault detection circuitry, due to the small thickness of the OIP samples, in many cases, the amplifier fault detection mechanism takes many cycles to operate especially at higher frequencies. This causes the formation of carbonized spots on the surface of electrodes after each experiment which may change the electric field at those positions for the next experiments. These spots can be removed by polishing the electrodes. To minimize this effect, a control box is added between the function generator and the amplifier. The output voltage measured by the amplifier is fed back to this control box and as soon as voltage drops below a threshold over a pre-defined time period, this control box stops the input signal to the amplifier. The control box is made with an Arduino and is capable of detection of breakdown within a few cycles at different frequencies, which is much faster than in-built fault detection system of the amplifier. Using this approach, discharge spots were almost eliminated. Thus, the electrodes were polished only after each set of experiments rather than after each individual experiment.

For the ramp sinusoidal breakdown tests, the sine waveform was modulated by a

ramp signal in the function generator. The function generator produced continuous ramp sinusoidal waveform. To force the ramp breakdown test to start exactly at the beginning of a ramp, the synchronization signal of the function generator is fed to the control box. When a user pushes the button on the control box, the Arduino detects the beginning of the next ramp by means of the synchronization signal, a relay inside the control box is activated and the output of function generator is connected to the amplifier. In this way, it was ensured that all ramp sinusoidal breakdown tests were started from the beginning of a ramp and increased with an exact $1\,kV_p/s$ slew rate.

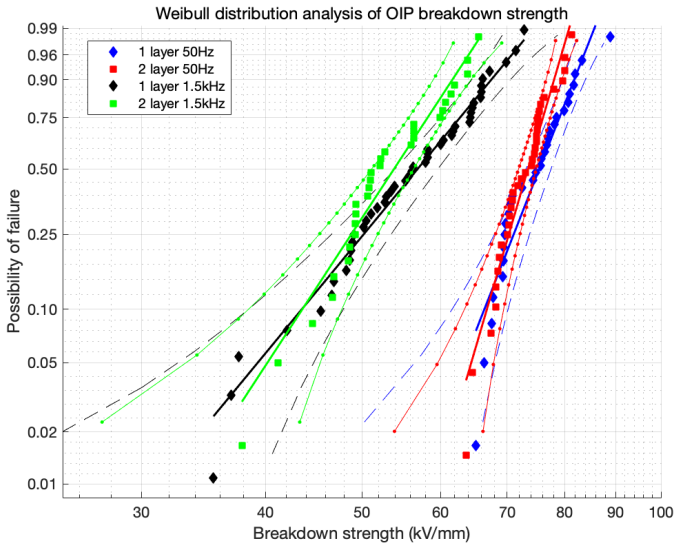


Figure 4.2: Comparison of Weibull plots for 1 and 2 layers of OIP at 50 and 1500 Hz

4.1.3. Ramp Sinusoidal Breakdown Tests

The ramp breakdown tests were performed on the OIP samples made of one or two layers. A ramp sinusoidal voltage with the slope of $1\,kV_p/s$ is applied to the electrodes, once at 50 Hz and once at 1500 Hz. To have a good statistics, at least 30 experiments were performed for each case study. After each experiment, the thickness of OIP sample was measured at the point of breakdown. Breakdown strength is measured by dividing the applied voltage to the corresponding sample thickness at the point of breakdown. It is important to notice that since here we have a two phase system (oil and paper), and because oil has also high breakdown strength, in many cases the point of breakdown has even higher thickness compared with other parts of the sample under electrodes.

$$F(E) = 1 - e^{-\left(\frac{E}{\eta}^{\beta}\right)} \tag{4.3}$$

The 2-parameter Weibull distribution formula shown in (4.3) is used to analyse the data. In (4.3), E stands for the DUT breakdown strength, $F(E)$ is the cumulative probability of breakdown, β is the shape parameter which reflects the slope of regression line in the probability plot, and η is the scale parameter. Probability of breakdown (failure) for the DUT is 63.2% at an electric field strength equal to η. Furthermore, in Weibull distribution plot there is another important parameter named correlation factor ρ, which is an indicator showing how well the linear regression line fits the data. Weibull plots of ramp sinusoidal breakdown for one and two layers of OIP at 50 Hz and 1500 Hz is shown in Fig. 4.2. Table. 4.1 shows a summary of Weibull distribution parameters for the plots illustrated in Fig. 4.2. A number of important observations can be made.

Parameter	β	η $[kV_p/mm]$	ρ
One layer 50 Hz	16.85	77.0	0.9468
Two layers 50 Hz	21.28	74.8	0.9750
One layer 1500 Hz	7.29	59.9	0.9907
Two layers 1500 Hz	9.51	56.0	0.9771

Table 4.1: Weibull distribution parameters of plots in Fig. 4.1

First of all, the breakdown strength at 50 Hz is considerably higher than that at 1500 Hz (also visible in parameter η shown in Table. 4.1). The slope of the Weibull plot is steeper at 50 Hz compared with that at 1500 Hz (also visible in parameter β). It can be seen that at 50 Hz, the spread of breakdown strength is narrower. Within a span of 25 kV/mm (65-90 kV/mm), all samples undergo breakdown. However, at 1500 Hz, the spread is wider and all of the DUTs break down within a span of 40 kV/mm (35-75 kV/mm). This means that weaker samples at higher frequencies behave poorly, which is very important since insulation system is designed such that even the weakest point of dielectric should handle the electric field stress. If the weakest samples has far lower breakdown strength, it means more insulation material is needed to achieve a reliable design.

Secondly, compared with the plots of one-layer breakdown test, it can be seen that for both 50 and 1500 Hz, the slope of the regression lines for two layers become sharper (also visible in parameter β). This is because with more OIP layers it is less likely that two weak points on each OIP layer align. As a consequence, the breakdown strength of material becomes less dependent on each individual sample layer and its weak points. Hence, the breakdown strength is less spread.

Thirdly, for both 50 and 1500 Hz, it can be seen that samples made of two layers of OIP have in general lower breakdown strength than those with one layer. This observation can be referred to the volume effect which is usually observed in insulation material. According to this effect, thinner and smaller sample of a piece of insulation material has higher breakdown strength than the thicker and larger ones. The effect is attributed to the number of defects in a given volume of insulation sample. The thicker the sample is, the more likely of the presence of defects inside the sample would be. Thus, it is more likely that breakdown occurs.

However, when considering the lower parts of the curves (probability of failure <20%) which belongs to those samples that have severe weak points (breakdown occurs at the lower range of electric field), there is no clear observation of volume effect and if regression lines are considered, actually the opposite effect is observed. This is because when severe weak points are present (which is true for this part of the curve), for one layer sample, the severe weak point directly lead to breakdown of one layer samples. However, for two layer OIP samples, two severe weak points on each layer is unlikely to be right on top of each other. Therefore, for this part of the curve, the breakdown strength of one layer sample is lower than sample with 2 layers (or multi layers in general).

4.1.4. HV Accelerated Aging Tests (Lifetime Tests)

Time to breakdown was measured for 50 and 1500 Hz at different level of electric field stress. At each field strength level, the experiment was repeated at least 21 times (in some cases up to 31 times) to get good statistics. For each electric field strength, the median of the measurements (coloured blue in Fig. 4.3) was selected to represent the trend of data and to draw the lifetime curve. By fitting the medians into the well-known empirical inverse power low, (4.4), the lifetime curve can be obtained. Fig. 4.3 shows the time to breakdown measurement data and the fitted lifetime curves at 50 Hz and 1500 Hz.

$$t = k \cdot \left(\frac{E}{E_0}\right)^{-n} \tag{4.4}$$

In (4.4), E stands for the field strength with the unit of kV/mm. The reference field strength, E_0, is defined as $1.0\,kV/mm$. The variable t denotes the time to breakdown at the field strength E, while k indicates the time to breakdown at E_0. It can be seen that the slope of lifetime curve increases considerably from 50 to 1500 Hz. This indicates a lower lifetime for OIP samples that are exposed to higher frequency stress.

Table. 4.2 shows the parameters of lifetime curves for the two target frequencies. For 50 Hz, parameters are very sensitive and even small change of the medians along each electric field stress will influence the value of n and k considerably. In general, to obtain more reliable parameters, experiments at lower field strengths are required to be done and the resulted time to breakdown is expected to be much longer.

Parameter	n	k
One layer 50 Hz	25.6	$5 * 10^{46}$
One layer 1500 Hz	7.15	$7 * 10^{12}$

Table 4.2: Parameters of the lifetime curves shown in Fig. 4.3

It was also observed that through the whole experiments, for both ramp sinusoidal breakdown and lifetime tests, breakdown happens at both polarities, most

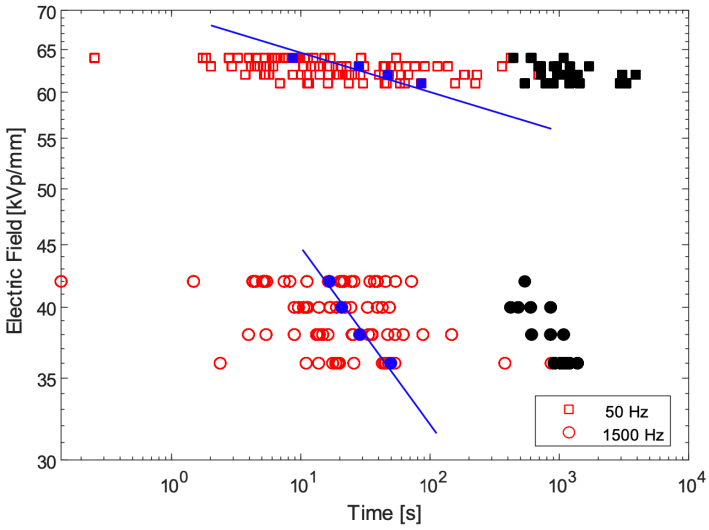


Figure 4.3: Lifetime curves for one layer of OIP at 50 and 1500 Hz. Black dots represent the halted experiments. n is equal to 7.15 for 1500 Hz and 25.64 for 50 Hz.

of them take place close to the peak of voltage waveform for both polarities and sometimes off the peak.

4.1.5. Summary of Chapter 4.1

In this research, the breakdown strength and lifetime of OIP samples were investigated both at 50 and 1500 Hz. For the ramp sinusoidal breakdown tests, it can be concluded that the breakdown strength is lower and at the same time more spread at 1500 Hz, compared with 50 Hz. To obtain lifetime curves, step sinusoidal voltage waveform was used. It was found that the slope of lifetime curve for 1500 Hz is much lower than that at 50 Hz. This indicates that for a desired lifetime, the permissible field strength at 1500 Hz must be much lower than at 50 Hz, which means more insulation material for a given design is required at 1500 Hz.

For the design of the MFT within HV-AWG, the expected operating frequency is around 30 kHz. However, the Trek amplifier has a limited frequency bandwidth ($\leq$ 5 kHz). Therefore, a new testing platform needs to be developed to test the DUTs at higher frequencies (will be explained in Section 4.3).

The future plan is to extend this work by conducting similar experiments at a higher frequency range, around 30 kHz. This will enhance the understanding of OIP aging under high-frequency, high-voltage stress, and provide insights into selecting suitable insulation materials for the MFT.

4.2. Epoxy Resin Dielectric Investigation[2]

In Section 4.1, the dielectric characteristics of OIPs are thoroughly investigated. If the OIP is chosen as the insulation material of MFT, the transformer must be fully immersed in oil. However, the oil-based transformers are typically bulky and heavy, making integration with the desired CHB-based HV-AWG challenging. Transformer oil can also become contaminated with impurities such as water, particulate matter, and gases, reducing its dielectric strength and potentially leading to electrical failures. The costs associated with oil replacement, purification, and degassing can increase operational expenses. Additionally, transformer oil poses environmental hazards in the event of leaks or spills. Therefore, solid-type materials can be considered as alternative insulation options for MFTs.

As discussed in Section 1.4, the MFTs are designed to be more compact. Achieving a smaller size and higher energy transmission efficiency requires an increase in the frequency level of the MFT input signal. According to equation (4.4), it is well-established that insulation materials exposed to higher frequencies experience accelerated aging. Consequently, studying the performance of insulation at high frequencies is crucial for ensuring the stable operation of dry-type MFTs and their associated power electronic equipments.

Epoxy resin is regarded as one of the most competitive insulation materials for MFT due to its superior electrical, thermal, and mechanical properties [75], as well as its relatively low dissipation factor. These properties can be significantly enhanced by incorporating a specific amount of nano-fillers, such as hexagonal boron nitride (hBN) particles [76,77]. In [78], N. Awang concluded that increasing the amount of BN nano-fillers leads to a reduction in PD magnitude, PD number, and PD charge compared to the neat epoxy sample.

Moreover, the breakdown strength of pure epoxy resin is influenced by several factors, including material thickness, the slope of the applied AC voltage ramp, field stress duration, temperature, humidity, and the condition of the dielectric (whether aged or brand-new) [79]. To obtain reliable and convincing results, the slope of the sinusoidal input voltage ramp is set to be $1\,kV_p/s$. In this study, the breakdown strength of neat epoxy resin is investigated and compared at frequencies of 50, 500, and 5000 Hz at room temperature ($20°C$).

4.2.1. Epoxy Resin Sample Preparation

In [80], Z. Xu has introduced a pre-made mould to create the thin epoxy resin samples. The spacers are placed within the mould to adjust the sample thickness. However, owing to the large viscosity of epoxy resin, the removal of the sample from the mould after curing will be a big issue. Also, in [81], H. Fu provided the detailed interpretations for the preparation of the epoxy samples with the thickness of around 5 mm. However, due to the limited HV capability of the Trek amplifier (maximum 30 kV), the epoxy resin samples with 5 mm thickness are too thick to break down.

[2] W. Zhao, T. Luo and M. G. Niasar, "Ramp sinusoidal breakdown of epoxy resin under high voltage waveforms at different frequencies", 22nd International Symposium on High Voltage Engineering (ISH 2021), Hybrid Conference, Xi'an, China, 2021, pp. 2083-2088, doi: 10.1049/icp.2022.0291.

In this study, epoxy resin type CY225 and hardener type HY925 are the original materials used for sample preparation. Initially, Teflon plates were used as the mould for samples because the cured epoxy resin wouldn't stick tightly on Teflon. However, after the curing process, Teflon material penetrated the epoxy resin sample and make it non-transparent. To reach more accurate results, the Teflon-base mould was abandoned. If the epoxy resin material was poured in an open mould, the epoxy surface will be curved and shrinked and thin samples cannot be made. It is worth mentioning that the pure epoxy needs hardener to create tightly cross-linked molecular structures that impart incredible strength into the cured film. Based on above information, the epoxy sample preparation processes with a thickness between 0.1 and 0.2 mm are as follow:

- Epoxy resin (CY225) and hardener (HY925) were both degassed at $60°C$ for 1 h in the chamber of BINDER VD 53 vacuum oven to remove air and moisture inside the original materials.

- The degassed hardener (liquid-type) was added to epoxy resin and mixed thoroughly for 30 mins. Then, the mixture was placed inside BINDER VD 53 vacuum oven to remove the trapped air at $60°C$ for 2.5 h.

- Two large Aluminum plates were machined to fit the BINDER oven and used as the mould for epoxy resin sample casting and curing. For easier sample removal, a thin layer of silicon rubber with the thickness of 0.3 mm was casted on the plates, shown in Fig. 4.4 (left). (The silicon rubber layer is made of TFC Silicon Kautschuk TYP3- Basis and Catalyst.)

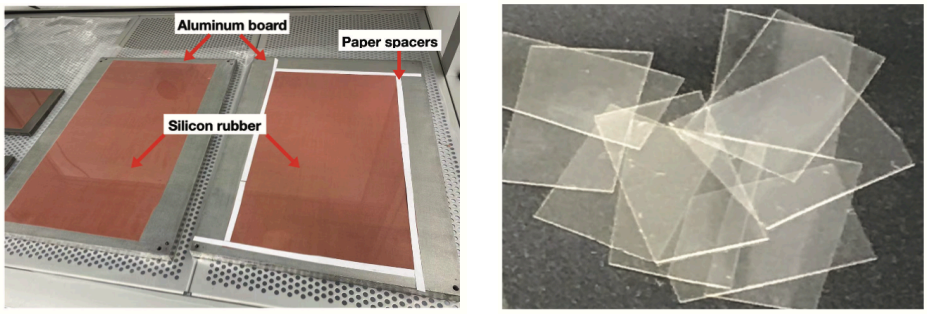


Figure 4.4: Pre-made mould for epoxy resin preparation (left) and thin epoxy sample pieces (right)

- Paper spacers were placed at the edge of silicon rubber area, shown in Fig 4.4 (left) and used to control the thickness of pure epoxy sample. The thickness for one layer of paper spacer is around 0.10 mm. To acquire thicker samples, multiple layers of paper could be used. The degassed epoxy-hardener mixture was casted on the silicon rubber region and spread uniformly by the universal applicator.

- Epoxy resin sample was cured inside the oven at $120°C$ for 4 h. Then, the sample was cooled down and cut into pieces for ramp breakdown tests. The thickness of the sample ranges from 0.08 to 0.20 mm shown in Fig 4.4 (right).

4.2.2. Experimental Set-up Preparation

Similar to the experimental setup described in Section 4.1.2 for testing OIPs, this setup primarily consists of a Trek amplifier and a function generator. The sphere electrodes are immersed in clean mineral oil to prevent the occurrence of surface discharges. In [82, 83], double-sphere electrodes were utilized to generate homogeneous field strength for ramp sinusoidal breakdown tests. Conversely, in [72], cylinder electrodes are implemented for AC tests. According to [84], cylinder electrodes are predominantly used for DC breakdown tests. Consequently, this study employs double-sphere electrodes made of brass, each with a diameter of 10 mm. The schematic of the entire experimental setup is illustrated in Fig. 4.5.

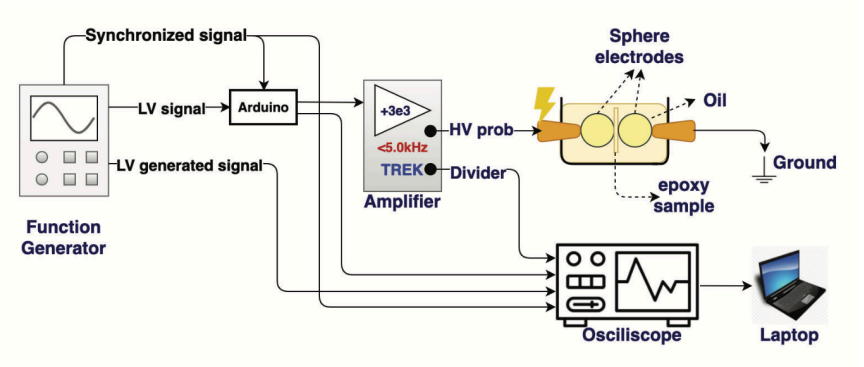


Figure 4.5: Experimental setup for ramp sinusoidal breakdown tests

The Arduino, relay and some other accessories formed the control box of the set-up. The control box is connected between the function generator and Trek amplifier. The relay within the control box could only be turned on at the instant when the synchronization signal sent from function generator to Arduino dropped from 'High' to 'Low' level. Therefore, the ramp voltage signal would definitely start at the very beginning and be sent to the Trek amplifier. In this way, all ramp breakdown tests were ensured to have same waveform start-point with an exact $1\,kV_p/s$ rate.

4.2.3. Ramp Sinusoidal Breakdown Tests

The tests were conducted on thin epoxy resin samples with thicknesses ranging from 0.1 to 0.2 mm. A ramp sinusoidal voltage input signal with a slope of $1\,kV_p/s$ at frequencies of 50, 500, or 5000 Hz was applied to one of the sphere electrodes. The breakdown strength was determined by dividing the applied voltage by the sample thickness near the breakdown perforation.

In [85], G. Chen observed that the electrical breakdown strength of solid dielectrics decreases with increasing sample thickness, a phenomenon that can be

explained by the inverse power law shown in equation (4.5). Here, E represents the breakdown strength of the insulation material at a given thickness, while n and k are constants specific to the testing material. This phenomenon is also attributed to the volume effect: thicker samples contain more defects (such as cavities and cracks), which can induce discharges and significantly reduce the breakdown strength.

$$E(d) = k \cdot d^{-n} \tag{4.5}$$

In this research, the epoxy resin samples are categorized into three different thickness groups. Group one ranges from 0.105 to 0.135 mm (0.12 ± 0.015 mm). Group two ranges from 0.135 to 0.165 mm (0.15 ± 0.015 mm), and group three ranges from 0.165 to 0.195 mm (0.18 ± 0.015 mm). The 2-parameter Weibull distribution analysis formula, as presented in equation (4.3), is employed to analyze the data obtained from the breakdown tests. Fig. 4.6 displays the Weibull plots for the breakdown strength of epoxy samples across these three thickness groups at 50, 500, and 5000 Hz, respectively.

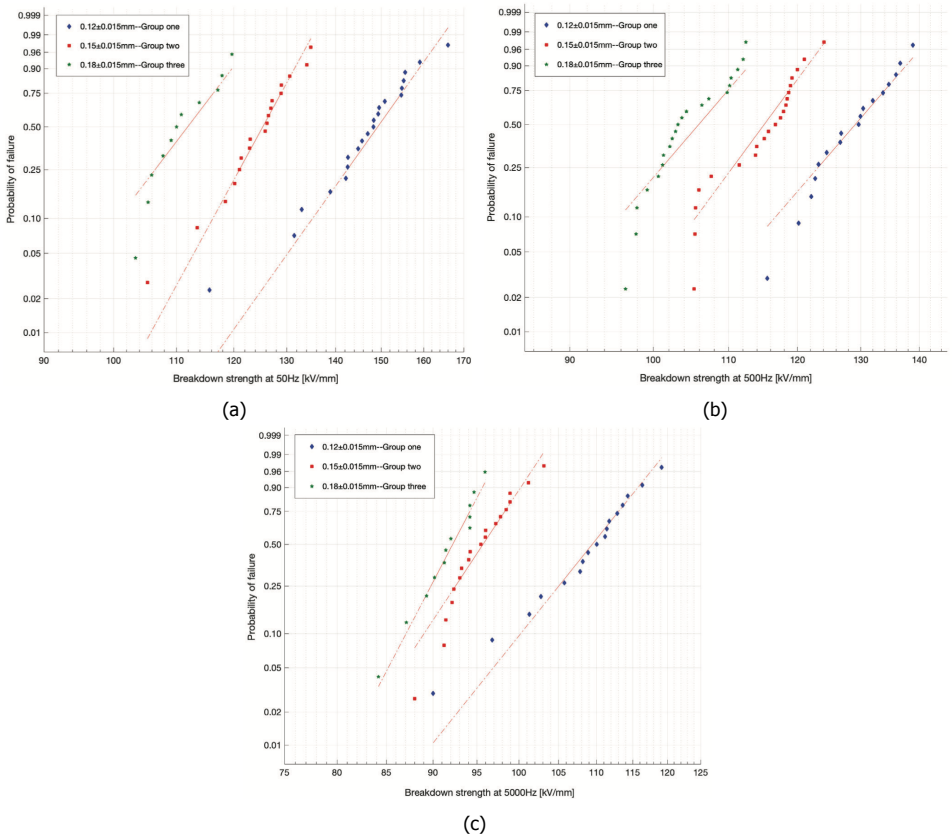


Figure 4.6: Weibull plots of the ramp sinusoidal breakdown data of epoxy resin samples (a) at 50 Hz, (b) at 500 Hz, (c) at 5000 Hz

According to Fig. 4.6, it is quite obvious that the thinnest thickness group (blue dots) has considerable larger breakdown strength compared with that for thicker groups owing to the volume effect. Moreover, at higher frequency level, the surface discharges that can cause cumulative heating with higher repetition rate might also contribute to the reduction of sample breakdown strength. According to Fig. 4.6 (a) and (c), it seems that the spread of ramp breakdown field strength at 5 kHz is relatively smaller than that at 50 Hz. To properly fulfill the statistical analysis, for each thickness group, at certain frequency, at least 12 experiments were performed for the ramp sinusoidal breakdown tests.

4.2.4. Summary of Chapter 4.2

For the obtained ramp breakdown results, depicted in Fig. 4.6, it can be concluded that the breakdown strength of pure epoxy resin is highly sensitive to thickness. The breakdown strength is much higher for thinner samples compared to thicker samples. Additionally, for the same sample thickness, the breakdown strength decreases with increasing frequency. When compared to the ramp breakdown results of OIP samples, illustrated in Fig. 4.2, at the same frequency level (e.g., 50 Hz), the minimum breakdown strength of a single piece of epoxy resin is considerably higher than the maximum breakdown strength of a single layer of OIP.

The ramp breakdown results demonstrate that the breakdown strength of pure epoxy resin is highly dependent on material thickness. Notably, thinner samples exhibit significantly higher breakdown strength compared to thicker ones. Furthermore, for a given sample thickness, the breakdown strength reduces as the frequency increases. When these results are compared with those of OIP samples at the same frequency (e.g., 50 Hz), the breakdown strength of a single epoxy resin sample is markedly higher than that of a single layer of OIP. However, additional investigation at higher frequencies (e.g., around 30 kHz) is still required.

4.3. Design of a HV & HF Insulation Test System Using a Ferrite-Based Resonant Transformer[3]

With the increasing introduction of PE-based systems in the electricity grid, both medium- and high-voltage insulation systems are subjected to voltage waveforms containing high-frequency components in the kHz and MHz range. This HF content results in an accelerated insulation degradation, potentially reducing the lifetime by orders of magnitude. Consequently, insulation materials must be characterized and tested using HF waveforms. The major challenge in generating the HV and HF waveforms is the enormous reactive power associated with the dv/dt, even for capacitances in the range of hundreds of pF [86].

Although the PE-based insulation systems typically endure pulsed stress, they can be effectively characterized using HV and HF sinusoidal waveforms, which are easier to be generated at the necessary frequencies. Additionally, the insulation systems of various system components, such as transformers, circuit breakers, and

[3] W. Zhao, G. W. Lagerweij, M. G. Niasar, "Design of a High-Voltage High-Frequency Insulation Test System using a Ferrite-Based Resonant Transformer", IET High Voltage, accepted.

disconnectors, can also be evaluated using HV and HF sinusoidal waveforms. The following methods have been employed to generate these waveforms:

- Linear HV amplifier: Linear amplifiers are limited in the available output current (HV side) and, thus, cannot be used beyond several kHz. For example, with an HV power amplifier of type Trek Model 30-20 A, voltage levels up to about $25\,\mathrm{kV_{pk}}$ can be attained at frequencies less than 2.5 kHz with acceptable distortion [87]. (The HV linear-amplifier-based experimental setup is utilized for conducting HV ramp breakdown and accelerated aging tests on OIP and epoxy resin samples, as detailed in Sections 4.1 and 4.2.)
- PE based HV source: HV arbitrary waveform generators for insulation testing are currently under development. The permissible bandwidth and output voltage level are still limited by the available hardware [31, 88, 89].
- Vacuum tube oscillator: An oscillator with HV output can be built with a high-power vacuum tube and resonant anode circuit. Frequencies up to 5 MHz may be achieved, but the voltage is limited by the tube and losses in the resonant circuit. [90, 91]
- Inverter- or amplifier-driven transformer: Linear power amplifiers and inverters are easy to obtain. In combination with a simple resonant transformer, high voltages (approx. $10\,\mathrm{kV_{pk}}$) at frequencies in the range of 10 to 100 kHz could be generated. [86, 92]

For decades, the HV test systems for power-frequency AC have utilised (quasi-) resonant circuits to compensate (a part of) the current drawn by large capacitive loads presented by, e.g., cables and transformers [93, 94]. This concept can be applied to achieve full resonance at any desired testing frequency [95, 96]. In this section, a resonant system is developed which can be driven by an inverter or power amplifier for HV testing at high frequencies ranging from 25-45 kHz.

State-of-the-Art

An air-coupled (or Tesla) transformer has sometimes been used for HV HF testing [96]. These transformers are rather big and less easily controlled than, e.g., a transformer using a ferrite core. Ferrite-based resonant transformers are small, easy to build and drive, and cheap [92]. However, ferrite-based resonance transformers are usually not chosen due to (i) the nonlinearity of the core material at high flux density and (ii) the parasitic capacitance of the transformer, which can restrict the tunable frequency range compared to a Tesla transformer-based solution. The advantages and disadvantages will be further explored in HF insulation testing.

The general architecture of the described resonant test system is shown in Fig. 4.7. The key component is a ferrite-core transformer whose secondary leakage inductance L_σ creates a resonant circuit with the insulation sample (DUT), modeled as the capacitance C_{DUT}. The resonance frequency can be tuned using an additional adjustable capacitor C_{res}. The losses in the resonant transformer and DUT have a significant effect on the gain of this system. Due to its resonant nature,

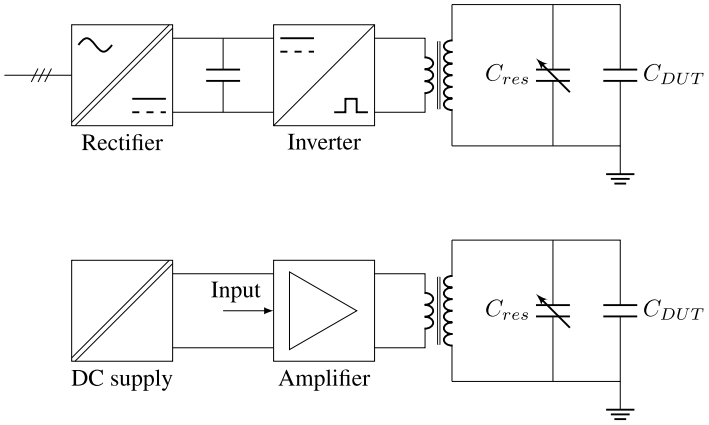


Figure 4.7: Insulation test system with an HV resonant transformer utilizing PE-based pulse generator and power amplifier.

the test system can be driven with any waveform as long as it has a frequency component at the resonant frequency. Therefore, it is possible to drive the system with a switching (PE-based) pulse generator or a (linear) power amplifier.

Most available literature on HF ageing of insulating materials is limited to high frequency and medium voltage (several kV), or medium frequency and high voltage (several tens of kV). A series-resonant test system is proposed to extend the testable range. The design of such resonant test systems up to a voltage of $10\,\mathrm{kV_{pk}}$ and several tens to 100 kHz can be achieved using extremely simple means, as demonstrated in [86, 92]. To increase the output voltage to around $23\,\mathrm{kV_{pk}}$, while maintaining the same test frequency, several big challenges must be overcome.

In the next chapter, two analytical models are derived for the test system to explain the effect of the various circuit parameters on the gain of the system. The resonant transformer design is discussed in Section 4.3.2 using a model-based approach. When increasing the frequency, the current drawn by the DUT will naturally increase. Even for very small DUTs, the reactive power may exceed the single-digit kVAs. The combination of high current and high voltage in the limited window area results in a complex secondary winding design. Section 4.3.3 addresses the implications for the bobbin and insulation design. A transformer prototype is built and evaluated in Section 4.3.4. The prototype is then used to perform breakdown tests, which show the importance of the dielectric loss and cooling performance of the insulation.

4.3.1. Resonant Test System Circuit Analysis

Resonant Transformer with Ideal DUT

Ideally, the DUT could be modelled as a lossless capacitor C_{DUT}. Substituting the well-known equivalent circuit for the transformer (leakage inductances L_{11} and L_{22}, magnetising inductance L_m, winding resistances R_{11} and R_{21}) and referring all the components to the secondary side yields the circuit in Fig 4.8.

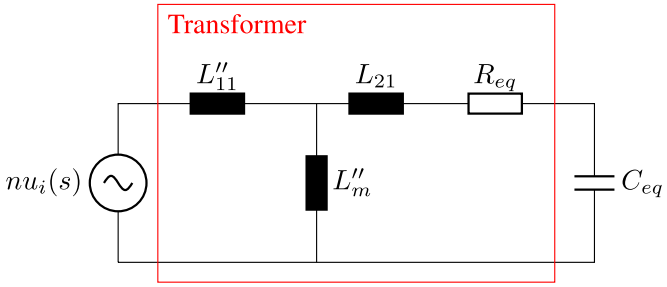


Figure 4.8: Equivalent circuit of the resonant transformer-based test system. L''_m and L''_{11} are referred to the secondary side.

These components can be lumped together into an effective transfer ratio m and a damped series RLC circuit composed of L_{eq}, C_{eq}, and R_{eq}.

$$m = \frac{nL''_m}{L''_m + L''_{11}} \tag{4.6a}$$

$$L_{eq} = L_{21} + L''_m \parallel L''_{11} \tag{4.6b}$$

$$R_{eq} = R_{21} + R''_{11} \tag{4.6c}$$

$$C_{eq} = C_{DUT} + C_{res} + C_\sigma \tag{4.6d}$$

Usually $L_m \gg L_{11}$. Therefore, the resonant system can be modelled using the second-order transfer function (4.7a).

$$\frac{u_o(s)}{u_i(s)} = \frac{m\omega_0^2}{s^2 + 2\zeta\omega_0 + \omega_0^2} \tag{4.7a}$$

$$\omega_0 = \frac{1}{\sqrt{L_{eq}C_{eq}}} \tag{4.7b}$$

$$\zeta = \frac{R_{eq}}{2\omega_0 L_{eq}} = \frac{R_{eq}}{2}\sqrt{\frac{C_{eq}}{L_{eq}}} \tag{4.7c}$$

Resonant Transformer with Lossy DUT

In practice, the DUT is not perfectly capacitive, and an additional loss component must be considered. The origin of this loss can be the dielectric loss ($\tan\delta$), partial discharges, or conductivity of the dielectric. The loss is modelled with an additional resistance R_p in parallel with the DUT capacitance C_{eq}.

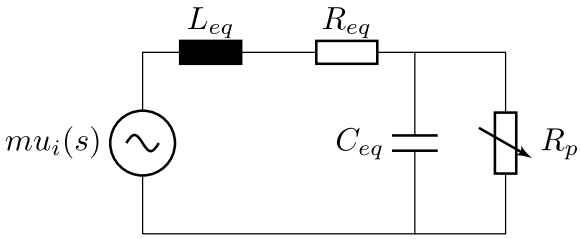


Figure 4.9: Equivalent circuit of the resonant transformer-based test system. The lossy DUT is modelled as a parallel RC circuit.

The transfer function of the equivalent circuit shown in Fig. 4.9 is given in (4.8). With reducing the value of R_p (i.e., increasing loss), the damping of the circuit is increased, and the resonance frequency decreases.

$$\frac{u_o(s)}{u_i(s)} = \frac{m\omega_0^2}{s^2 + s\left(\frac{R_{eq}}{L_{eq}} + \frac{1}{R_p C_{eq}}\right) + \omega_0^2\left(\frac{R_{eq}}{R_p} + 1\right)} \tag{4.8}$$

In the most general case, R_p will be a function of frequency, voltage, temperature, and other environmental influences. To accurately predict the output voltage of the test system, dielectric loss, and partial discharges should be accounted for.

4.3.2. Transformer Design Procedure

The capabilities of the resonant test system are limited in part by the resonant transformer design. They may be evaluated in terms of the load diagram (Figure. 4.10), which is also typically provided for low-frequency resonant test systems [94]. The transformer design aspects influencing this diagram are:

- Quality factor (i.e., losses) of the transformer,
- Thermal performance,
- Insulation system and secondary winding design.

The limiting curves of the load diagram should be designed to allow for the insulation testing at the desired voltage U_{max} with a maximum load capacitance C_{max} and test frequency f_{max}.

The following subsections describe the design of a ferrite-based resonant transformer, aiming to generate an output voltage of at least $20\,\mathrm{kV_{pk}}$ with high frequencies (25-45 kHz).

Parameter Calculation

The required leakage inductance of the resonant transformer follows directly from the range of the test frequency and the available load capacitance consisting of the DUT capacitance C_{DUT} and the optional variable capacitor C_{res} using (4.9).

$$L_{eq} = \frac{1}{(2\pi f)^2 C_{eq}} \tag{4.9}$$

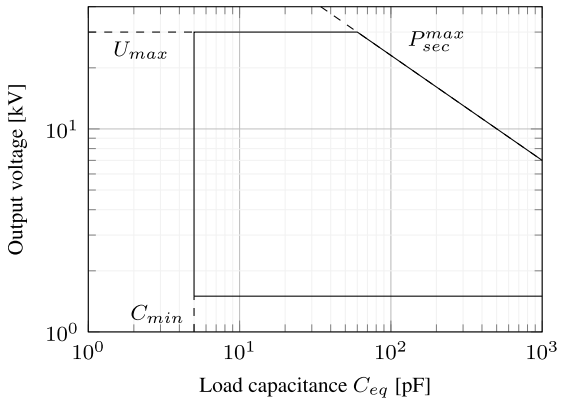


Figure 4.10: Load diagram of the designed transformer system (parameters given in Section 4.3.4). Operation outside the indicated operating area may be possible with waveform distortion or partial discharges.

The secondary current increases with frequency and capacitive load, and is given by (4.10) when the resistive component of the DUT is neglected.

$$I_s = 2\pi f C_{eq} U_o \tag{4.10}$$

Core Selection

A split transformer winding configuration (core-type) creates a large leakage inductance, with the windings on two legs of a UU core. The desired leakage inductance can be realised with a large number of secondary turns. In addition, a large window area is needed to ensure sufficient clearance between the secondary winding and core. The split configuration aids in increasing the clearance between the primary and secondary winding.

Core saturation is not a major concern because the voltage applied to the primary is low (gain is on the order of 10^3), and the number of turns is relatively high. The flux density in the core is calculated using the primary volt-seconds in (4.11), where U_p is the primary peak voltage, N_p is the primary turns, and A_e is the effective core area.

$$B = \frac{U_p}{\sqrt{2}\pi f N_p A_e} \tag{4.11}$$

Leakage Inductance Estimation

No analytical formulas are currently available for the split transformer winding configuration chosen for the resonant transformer. Attempts have been made, but are generally inaccurate [97, 98]. Therefore, the leakage inductance is simulated using a finite element model (FEM), as shown in Fig. 4.11.

The model uses a single homogenised volume to model the secondary winding. This approach has been verified against more detailed models for a low number of turns (multiple layers and each winding modelled as a realistic wire). The simplified

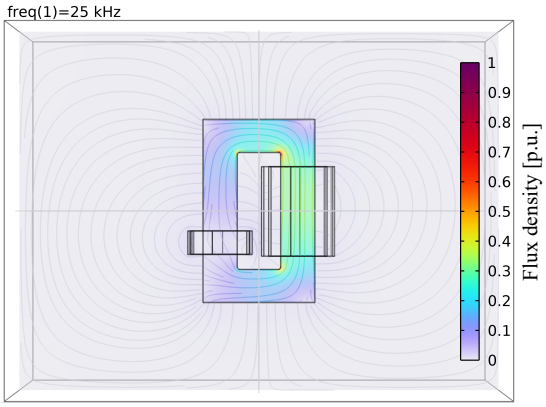


Figure 4.11: FEM model for leakage inductance with excitation current in the secondary winding and short-circuited primary winding (50:600). The contour and colour map show the H and B-field, respectively. The colour is given in p.u. since its magnitude depends on the excitation.

model has an error of below 6 % in a fraction of the computation time, which is satisfactory for the leakage inductance estimate. The obtained results are compared and shown in Figure 4.11 and Table 4.3.

Table 4.3: Comparison of detailed and simplified FEM simulation results

Turns ratio $N_p : N_s$	$10:10$	$10:20$	$10:30$
Detailed winding	$3.9\,\mu H$	$11.3\,\mu H$	$19.9\,\mu H$
Simplified winding	$4.1\,\mu H$	$11.5\,\mu H$	$20.1\,\mu H$
Error	$+5.1\,\%$	$+1.8\,\%$	$+1.0\,\%$

AC Resistance Estimation

Because many turns can be required to obtain the desired resonance frequency and leakage inductance, multi-layer windings are usually necessary. If the designs are limited to a single layer, very thin windings must be created, negatively impacting the corona inception voltage and winding resistance. Since the desired operating frequencies are in the range of 25 to 45 kHz, the skin and proximity effect should be taken into account to determine the gain of the system correctly. The AC resistance can be estimated using the procedure presented by Biela [99, pp. 235-240].

$$R_{AC}(f) = 2R_{DC}\left[F_R(f) + N^2 G_R(f)\frac{4M^2-1}{12b_F^2}\right] \tag{4.12}$$

where $F_R(f)$ and $G_R(f)$ represent the skin and proximity effect, N is the number of turns per layer, M is the number of layers, and b_F is the winding height. The DC resistance R_{DC} is calculated from the winding geometry. The results given in Fig. 4.12 show good agreement between the measured and calculated AC resistance. For

multi-layer windings, the resistance increases significantly with frequency due to the skin and proximity effect.

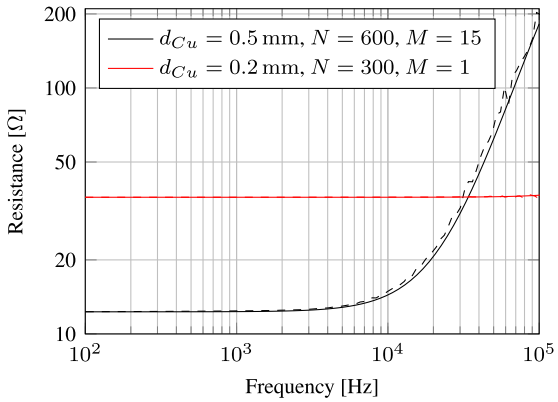


Figure 4.12: AC resistance calculation (solid line) and measurement (dashed line) on two secondary winding designs. Using a small wire in a single-layer winding results in less variation with frequency but limits the number of turns.

Resonant System Gain

The gain of the resonant system depends on the turns ratio n of the transformer, as well as the quality factor Q of the system (e.g., the resonant gain). The latter is determined by the combination of the transformer and the load (DUT and resonant capacitor), as calculated in (4.13) derived from (4.8).

$$Q = Q_T \parallel Q_{load} = \left[\frac{1}{Q_T} + \frac{1}{Q_{load}}\right]^{-1} \tag{4.13}$$

The gain can then be expressed as $G = nQ$. With a well-designed transformer (i.e., with high Q_T), the DUT usually determines the value of Q.

Transformer Turns Ratio

The secondary number of turns is selected based on the FEM simulation discussed in Section 4.3.2. With the preceding calculation results, the turns ratio and number of primary turns can be chosen. To achieve the desired output voltage from a DC source with limited output voltage, a minimum n is required. On the other hand, the secondary current is reflected back to the primary, leading to a maximum n for a current-limited source.

$$n \geq \frac{1}{Q}\frac{U_o^{max}}{U_i^{max}} \tag{4.14a}$$

$$n \leq \frac{I_{src}^{max}}{I_s^{max}} \tag{4.14b}$$

where U_i and U_o are the input and output voltage, I_s is the secondary current, and I_{src} is the current from the DC source.

Core Grounding

If the potential of the transformer core is not defined, it will be determined by the parasitic capacitances between the windings and the core. This may cause the core to attain a high potential [100]. For testing at voltages below $10\,\mathrm{kV_{pk}}$, this is not typically a problem. However, to avoid PDs between the core and LV winding, the core should be grounded [101].

If the core halves of the transformer are grounded by the copper foils, as shown in Fig. 4.13, the output gain of the resonant transformer is reduced significantly. This phenomenon can be explained as follows: Due to the large secondary leakage magnetic field, eddy currents are induced in the copper foils. The losses generated by these eddy currents can significantly reduce the quality factor of the transformer.

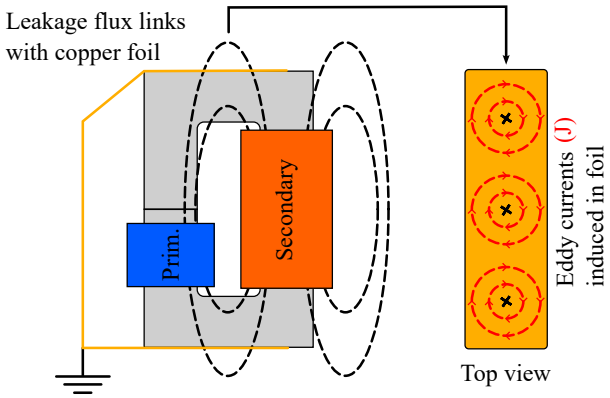


Figure 4.13: Schematic of transformer grounding using copper foil.

Two methods are implemented to reduce the eddy current losses: First, the cross-sectional area in which the eddy current can circulate is reduced by using thin copper wires instead of a wide foil, as illustrated in Fig 4.14. Second, these wires are placed far from the secondary winding to reduce the linking leakage flux.

4.3.3. Secondary Insulation Design

Special attention must be paid to the transformer secondary winding design. Due to the relatively small window area of the core halves, the desired HV output voltage may have the possibility to flash over across the winding or to the core.

Bobbin Design

A disc-type structure is chosen for the secondary winding, with the number of discs selected to limit the maximum turn-to-turn voltage. A single isolation turn between adjacent discs separates the wire bundles and eliminates disc-to-disc discharges. Fig. 4.15 illustrates the designed secondary bobbin with rounded corners and sufficient disc-to-disc distance to prevent flashovers.

The wire used to construct the secondary winding has a breakdown voltage of $3.3\,\mathrm{kV_{pk}}$. Since the winding turns are wound manually in a semi-random pattern,

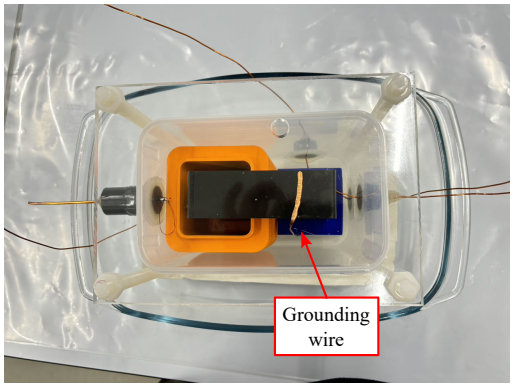


Figure 4.14: Resonant transformer grounded by thin wires to the top and bottom core half.

the chance of the disc voltage occurring between neighbouring turns is small. Nevertheless, to minimise the discharges between the turns, the secondary winding is divided into 12 segments to limit the disc voltage to $1.7\,\mathrm{kV_{pk}}$ at an output voltage of $20\,\mathrm{kV_{pk}}$. Although this is around $50\,\%$ of the breakdown voltage of the wire, this potential difference will never occur in practice.

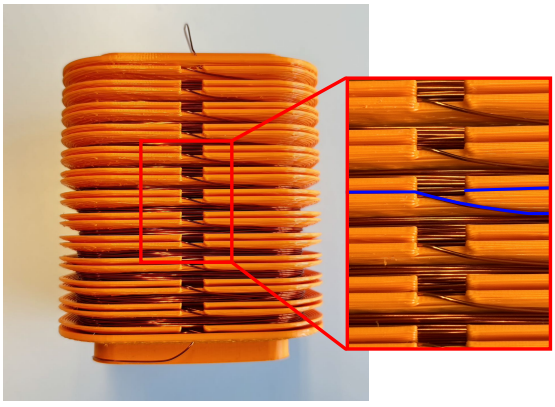


Figure 4.15: Resonant transformer secondary winding with isolation turns in the inter-segment slots. One of the isolation turns is highlighted in blue.

Insulation Design

When using the designed bobbin in air, discharges may occur in the winding and between the winding and the grounded core at relatively low voltages due to the sharp edges of the core. An additional insulating material prevents these discharges while providing adequate heat dissipation from the secondary winding. For the desired output of $20\,\mathrm{kV_{pk}}$, the required secondary power is already 10 kVA at $C_{eq} = 180\,\mathrm{pF}$ and $f = 45\,\mathrm{kHz}$. Some inspiration for the insulation design is taken from high-power solid-state transformers. In the power range of 15–60 kVA, several

different types of insulating materials are used: silicone gel [102], oil-impregnated paper [103], silicone rubber [104], and epoxy resin [104,105]. The insulator should provide good thermal conductivity.

Therefore, two types of dielectrics are considered for the design of the HF resonant transformer: liquid (transformer oil and silicone oil) and solid (epoxy CY225, and silicone rubber). Liquid dielectrics offer good breakdown strength, recovery after breakdown, and provide excellent cooling by convection of the insulated equipment [93]. According to the measurement results in Table. 4.4, they have a very low $\tan\delta$ at high frequency. Solid insulation offers several benefits over liquid dielectrics: they allow for compact insulation systems, are easy to work with and maintain, and are environmentally friendly. The dielectric properties of the solid dielectrics are typically better and more stable over temperature. Solid insulation can only provide cooling by conduction and is typically modified with fillers to increase the thermal conductivity κ. In addition, they can be more resistant to environmental factors such as moisture and contaminants [106].

Table 4.4: Insulation Material Properties (refer to Fig. 4.22)

Material	ε_r	$\tan\delta$ [10^{-4}] @ 10 kHz	κ [W/(mK)]
Transformer oil	3.2	1.6	0.14
Silicone oil	2.7	3.0	0.15
Epoxy CY225+HY925	2.8	100	0.21
Silicone rubber	3.1	25	0.30

After careful considerations, transformer oil is chosen as the insulating liquid for the prototype transformer because of the good insulation properties, low dielectric losses and good cooling performance.

4.3.4. Experimental Results

Prototype Transformer

A prototype transformer was designed for the parameters presented in Table 4.5. Parameters with an asterisk are design targets. The maximum required test power is around 10 kVA and the secondary output current is $0.71\,\mathrm{A_{rms}}$. The transformer uses two U93/76/30 core halves of material 3C90 ($\mu_i \approx 1900$) owing to sufficient window area. A 26 AWG MW35-C wire was chosen for the HV winding, resulting in a current density of $5.1\,\mathrm{A/mm^2}$. According to the FEM simulation result, the number of secondary turns should be 600 to reach the desired leakage inductance of approximately 130-140 mH, which is computed based on the frequency and load capacitance C_{eq} range. Based on the primary source limitations, a turns ratio of 12 was chosen, resulting in 50 primary turns. The winding bobbin is 3D printed according to the design presented in Section 4.3.3. Transformer oil of type MIDEL 7131 is used as the insulating liquid. The prototype transformer is depicted in Fig. 4.16.

Table 4.5: Prototype System Parameters

Parameter	Value
U_o^*	$20\,\mathrm{kV_{pk}}$
f^*	$25 - 45\,\mathrm{kHz}$
C_{load}	$100 - 180\,\mathrm{pF}$
Q_{load}	≥ 55
U_i	$\leq 30\,\mathrm{V_{pk}}$
I_{src}	$\leq 9\,\mathrm{A}$

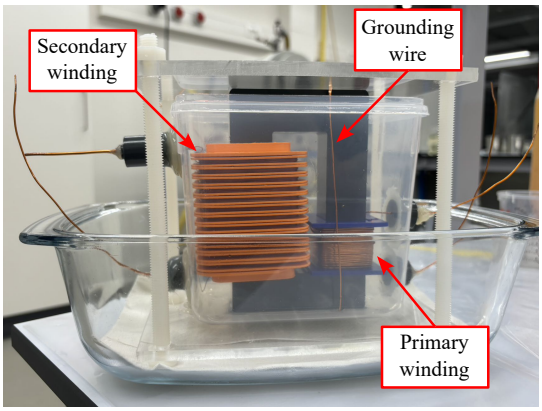


Figure 4.16: Transformer prototype with a plastic tank for transformer oil.

Transformer Parameter Extraction

The equivalent circuit parameters of the designed resonant transformers are extracted using the procedure of [86] and presented in Table 4.6. The winding resistances are measured at 25 kHz. The secondary leakage inductance L_{21} obtained from the FEM simulation described in Section 4.3.2 is 139.2 mH, which has an error of less than 5 % compared to the measurement. Both results lie within the range of the required L_{eq}. Using the extracted parameters and characteristics of the driving circuit, the load diagram of Fig. 4.10 is derived.

Although the physical construction is small, the parasitic capacitance C_σ is extremely small compared to the capacitance of typical DUT, which is usually more than 50 pF.

Resonant Transformer Response

Next, the response of the resonant transformer is measured by exciting the primary with a small square wave voltage and measuring the peak output voltage of the transformer. The gain is calculated from the output voltage and the fundamental component of the input voltage. The measured resonance peak is compared to the analytical results of (4.7a) and (4.8) and shown in Fig. 4.17. When dielectric loss is accounted for, the measured result matches the response predicted by (4.8). The

Table 4.6: Extracted Transformer Parameters

	Measured	Calculated	Error
L_m	3.3 mH	3.5 mH	+6.0 %
L_{21}	133.8 mH	139.2 mH	+4.0 %
R_{11}	0.11 Ω	0.12 Ω	+9.1 %
R_{21}	27.3 Ω	25.3 Ω	−7.3 %
C_σ	5.8 pF		

measured gain corresponds well to the calculated $G = nQ \approx 12 \times 57 = 680$, where Q is predominantly determined by Q_{load}.

The harmonic content of the output waveform has an important effect on the insulation lifetime. Ideally, a pure sinusoidal voltage should be obtained from the resonant transformer. In Fig. 4.18, the harmonic content is shown in the case of (i) sinusoidal primary voltage and (ii) square-wave primary voltage. As expected, the harmonics produced by the resonant test system are negligible.

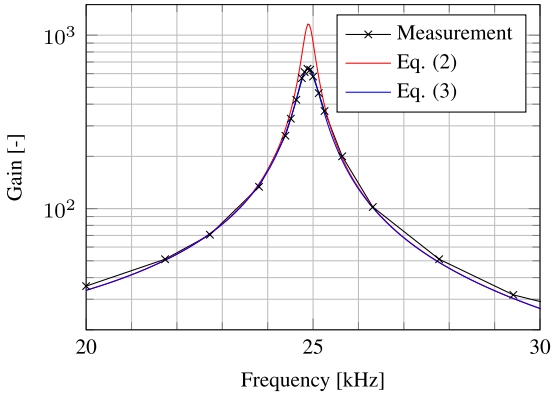


Figure 4.17: Response of the transformer with a load consisting of the DUT (C_{DUT} = 170 pF, $\tan\delta = 300 \cdot 10^{-4}$ @ 25 kHz) and an additional C_{res} = 120 pF with no dielectric loss.

The output voltage of the resonant transformer is approximately linear with the input voltage, as shown in the input-output characteristic in Fig. 4.19. The gain of the linear fit is $G \approx 790\,\mathrm{V/V}$. Experiments on various materials have shown that the gain and linearity are strongly dependent on the properties of the DUT.

Breakdown Characteristics of Insulated Twisted Wires

In transformer and electrical machine applications, enamelled copper wires are wound on a coil former or magnetic core. In this configuration, there will be contact points between neighbouring turns with a potential difference between them. To evaluate the breakdown behaviour of such a configuration at high frequencies, the twisted-wire samples shown in Fig. 4.20 are made of 26 AWG enamelled copper wire

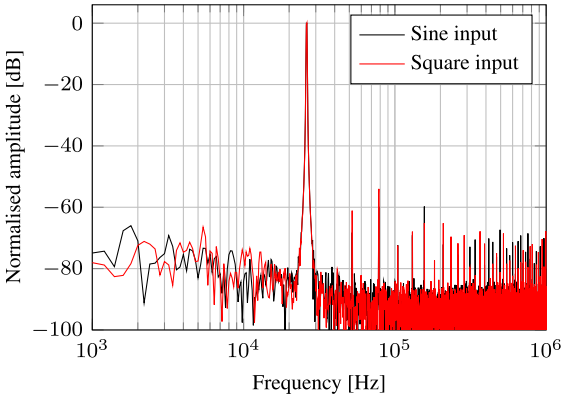


Figure 4.18: Frequency spectrum of the output voltage of the resonant transformer driven by a square-wave (red, THD = 0.3 %) and sinusoidal voltage (black, THD = 0.2 %).

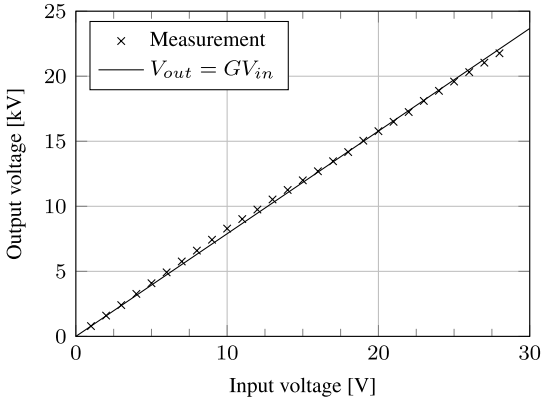


Figure 4.19: Input-output characteristic of the resonant transformer system when driven with an inverter with variable DC link voltage.

(MW35-C heavy film). To homogeneously distribute the contact points, strands are finely twisted. To prevent the partial discharges between the non-insulated ends of the wire, these are physically separated.

Twisted wire samples are submerged in oil or cast in one of the solid dielectrics. The samples are then subjected to a 35 kHz sinusoidal voltage waveform with linearly increasing amplitude. The sample ramp sinusoidal breakdown voltages are analyzed using Weibull statistics shown in Fig. 4.21.

The ramp breakdown results show two interesting conclusions: First of all, transformer oil has the highest breakdown voltage, even though it is one of the most lossy materials under consideration. Secondly, silicone rubber performs better than epoxy, which agrees with the general idea that lower-loss material should perform better under HF electrical stress. In the next paragraph, these statements are con-

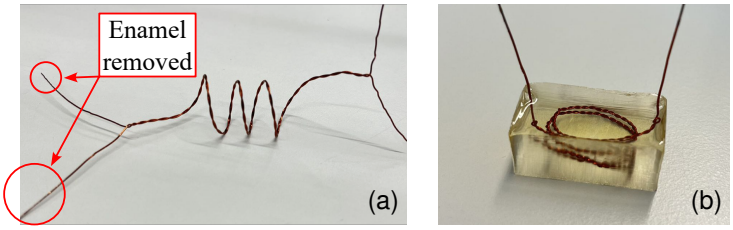


Figure 4.20: Twisted-wire samples used for breakdown tests in (a) liquid dielectric and (b) epoxy/silicon rubber.

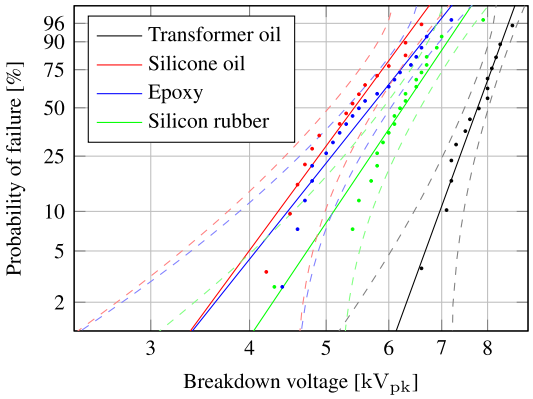


Figure 4.21: Weibull analysis of the breakdown voltage of the twisted wires

firmed through dielectric spectroscopy. Besides a low dielectric loss, high thermal conductivity is also desired for insulation materials used at high frequencies.

Relation to material properties The dielectric spectrum of cylindrical raw material samples was recorded using Novocontrol dielectric spectrometer, shown in Fig. 4.22. The linear behavior of the permittivity of transformer oil and silicon oil versus frequency is due to their simple molecular structures and minimal dipolar relaxation mechanisms, resulting in stable dielectric properties over a wide frequency range. In contrast, epoxy resin and silicon rubber exhibit non-linear permittivity and loss behavior after 1 kHz due to their complex molecular structures, leading to frequency-dependent dielectric relaxation processes that become prominent at higher frequencies.

Both dielectric liquids have a low $\tan\delta$ in the range of interest (10–100 kHz). The big difference in viscosity causes the significant difference in breakdown voltage between transformer and silicone oil: transformer oil is much less viscous and, therefore, provides better convective cooling. In the range of interest, the dielectric loss $\tan\delta$ of epoxy (1.0 %) is significantly higher than that of silicone rubber (0.2 %). Since the two materials have similar thermal conductivity, silicone rubber is less prone to thermal runaway breakdown.

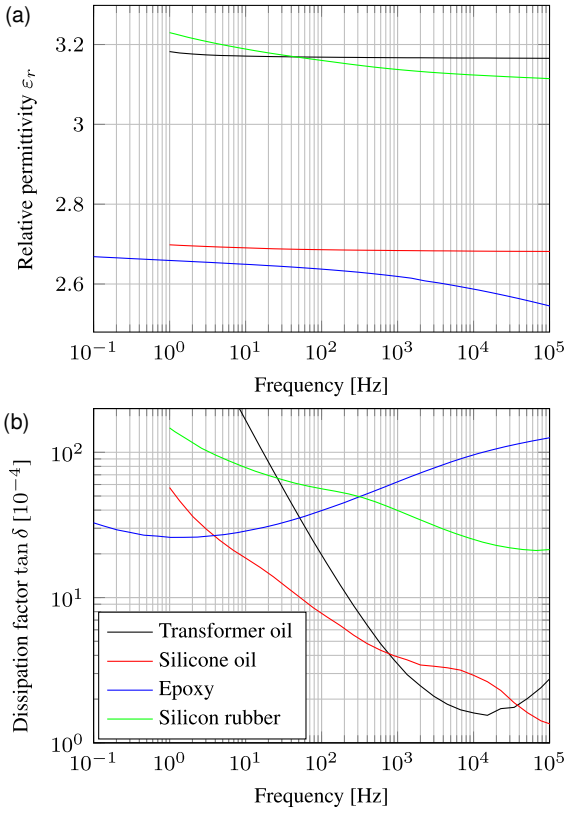


Figure 4.22: Dielectric spectrum of evaluated insulation materials. (a) Dielectric constant ε_r, and (b) dissipation factor $\tan\delta$.

The permittivity ε_r of the materials is similar, meaning that there will not be a significant difference in parasitic capacitance of the transformer. This property has a minor influence on the resonance frequency.

4.3.5. Discussion

A resonant test system is designed to generate a high-voltage, high-frequency sinusoidal waveform for insulation sample testing. The system topology, transformer secondary winding design, and insulation material selection are crucial to achieving efficient and steady test system operation.

Transformer secondary winding optimisation: The secondary voltage distributes non-uniformly along the disc winding, and the winding discs adjacent to the HV input take most of the voltage drop, meaning discharges and breakdown are more likely to occur [107]. Thus, an extra isolation turn is introduced; see Fig 4.15. This isolation turn is wrapped around the bobbin once to ensure that the last turn of the upper disc segment does not touch the adjacent lower disc segment. With-

out this single isolation turn, the disc-to-disc discharges will likely occur between adjacent discs at the HV side. Sufficient distance is also provided to reduce the probability of flashover.

Loss considerations: The losses generated in the resonant test system decrease the system output gain G and could lead to thermal breakdown of the system components. The losses are categorised into dielectric losses (e.g., the DUT and transformer insulation) and losses in system components (e.g., amplifier and resonant capacitor). Measurement results shown in Fig. 4.17 have shown that the DUT can be lossy. Also, analytical results illustrated in Fig 4.12 confirm that the AC resistance of the secondary winding will be large at high frequency due to the skin and proximity effect, which results in a large amount of secondary winding losses. An insulation material with low $\tan\delta$ is chosen for the resonant transformer to reduce the losses. Based on Fig. 4.22, the transformer oil of type MIDEL 7131 is selected due to its low $\tan\delta$ in the 10–100 kHz range.

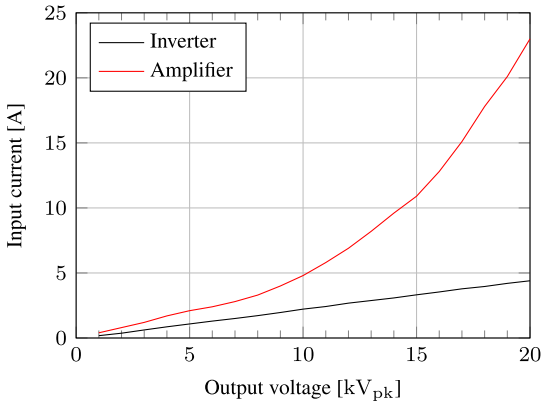


Figure 4.23: Low-voltage current draw versus output voltage for the inverter and linear amplifier-based test systems.

Of the two resonant test systems presented in Fig. 4.7, the inverter-based system requires much less driving current than that based on a linear power amplifier, as illustrated in Figure 4.23. Therefore, the inverter-based system is preferred. As illustrated in Fig. 4.19, a stable system output gain G can be achieved with the inverter-based test system.

System topology considerations: The frequency of the proposed test system is tuned using a variable capacitance. The mechanical construction of such a system is more straightforward than an inductance-tuned system, which is more common for 50/60 Hz testing. The fringing losses associated with the variable air-gap are eliminated. The secondary transformer leakage is utilized as the resonant inductance. As shown in Fig. 4.18, the quality of the output waveform is excellent, with negligible system-induced harmonics.

In the current implementation, the stability of the output amplitude and system resonant frequency is not yet guaranteed. Dielectric losses and temperature fluctu-

ations in the DUT and variable capacitor can influence these parameters. Therefore, a closed-loop control system should be implemented to ensure a stable output voltage over time.

Due to the losses in the transformer, changing the leakage inductance is easier than increasing the capacitive tuning range to achieve a larger test frequency range. This variable leakage inductance can be realized using separate transformers or by switching segments of the secondary winding (i.e., tuning the number of secondary turns via a tap-changer).

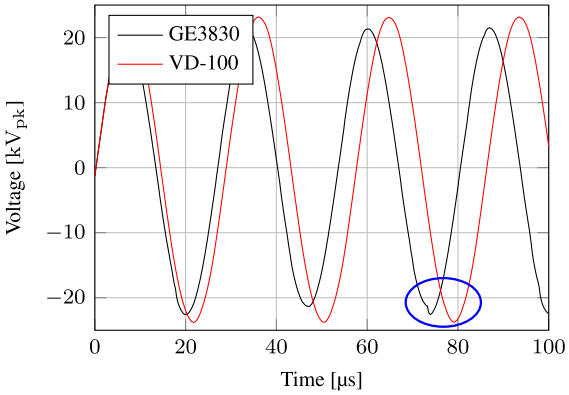


Figure 4.24: Output voltage waveforms measured with two high-voltage probes: Elditest GE3830 and North Star VD-100. Note the PD distortion at the peaks of the waveform captured using GE3830.

Resonant test system output limitations: The maximum output voltage of the system depends on many factors related to the transformer and the load, as described in the load diagram in Fig. 4.10. The auxiliary components, such as insulators, tuning capacitors, and HV probes, can also have a considerable impact. All auxiliary components must be PD-free at the desired frequency and voltage. In Fig. 4.24, HV waveforms captured using two different probes (Elditest GE3830 and North Star VD-100) are shown. Some distortion is present on the GE3830 waveform, which is attributed to PDs: The voltage amplitude on the negative half-cycle is reduced from the zero crossing until the peak, indicating that PDs take energy from the resonant circuit during this period. With a suitable, PD-free high-voltage probe, operation up to 23 kV$_{pk}$ was achieved at approx. 35 kHz (red waveform). The waveform is perfectly sinusoidal without any distortion. Higher voltages could be achieved if a DC supply with a larger output voltage capability is used.

4.4. Summary of Chapter 4

A capacitance-tuned resonant test system based on a ferrite transformer has been designed and validated in Section 4.3. This resonant test system can successfully generate an HV and HF sinusoidal output waveform with an amplitude up to $23\,\mathrm{kV_{pk}}$ in the frequency range of 25–45 kHz. The obtained waveform has very low distortion. The system can be driven either with a power electronic inverter or a linear

power amplifier, although the latter has a comparable larger current draw. The resonant transformer within the system is insulated by the transformer oil of type MIDEL 7131, which has excellent dielectric characteristics. Also, its secondary winding has been optimized using an extra isolation turn to separate the adjacent disc segments and avoid the occurrence of disc-to-disc discharges. PD-free auxiliary components are required to obtain a stable, undistorted, high-voltage output. This specific resonant testing platform enables the characterization of insulation materials under high-frequency conditions.

In Section 4.3.4, the twisted-wire samples insulated with silicon rubber (type TFC) exhibited higher breakdown voltages compared to those cast in neat epoxy resin of type CY 225. In Section 4.1 and 4.2, the neat epoxy resin also demonstrated superior dielectric properties relative to the oil-impregnated paper (under low frequency levels: 50 Hz and 1 kHz). Given the various advantages of solid-type insulation materials, it is determined that heat-resistant silicon rubber is the most suitable choice for the insulation system design of MFT. According to the results presented in Figure. 4.21, transformer oil, as a liquid-type insulation, exhibited the highest breakdown voltage, making it appropriate for use as insulation of the resonant transformer within the resonant test platform.

5

PCB Design of a Standard H-Bridge

5.1. Standard H-Bridge Design

The standard H-bridge can serve as the inverter (DC-to-AC) within the aforementioned resonant test platform, as detailed in Section 4.3. Additionally, it can also drive the medium-frequency transformer within the modular CHB-based HV-AWG. This H-bridge is designed to achieve an output voltage with an amplitude of 300 V. Commercially available MOSFETs can easily meet this requirement. As discussed in Section 3.1, SiC MOSFETs excel in high-power and high-temperature applications and are therefore recommended. According to component availability and cost considerations, the SiC MOSFET type IMW120R220M1H has been chosen. This SiC MOSFET offers a maximum blocking voltage V_{DS}^{max} of 1.2 kV and a maximum current rating I_D^{max} of 13 A, which are adequate to meet the design specifications.

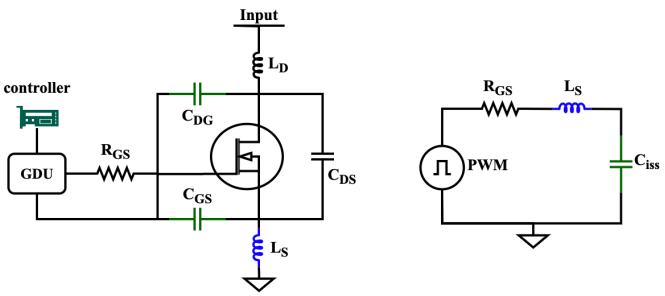


Figure 5.1: SiC MOSFET electric model (left) and its equivalent ringing circuit (right)

Figure 5.1 depicts the electrical model of a commercial SiC MOSFET, incorporating parasitic capacitances (C_{GS}, C_{DG}, C_{DS}) and inductances (L_D, L_S). Oscillations

and overshoots observed in the gate voltage V_{GS} are primarily attributed to the dynamic input capacitance C_{iss} and source inductance L_S. Notably, C_{iss} is defined as the sum of C_{DG} and C_{GS}. The presence of these intrinsic parasitic elements leads to the following two significant issues. However, implementing external gate resistors ($R_{G(on)}$ and $R_{G(off)}$) can effectively mitigate these problems.

- Due to the presence of the MOSFET input parasitic capacitance C_{iss}, initial current spike will occur when the gate pin goes from 'LOW' to 'HIGH'.
- Ringings will initially occur on the gate signal V_{GS} and consequently on V_{DS}.

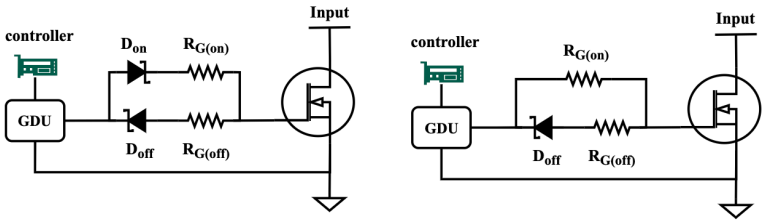


Figure 5.2: External gate circuits with two Schottky diodes (left) and one Schottky diode (right)

Notably, increasing the gate resistor's value reduces the SiC MOSFET switching speed, thereby increasing its switching losses. Conversely, decreasing the gate resistor value enhances the MOSFET switching speed but may induce surge voltages on V_{DS} and V_{GS} due to parasitic inductances and capacitances. Therefore, the external gate resistance must be optimized to balance switching speed and voltage surges.

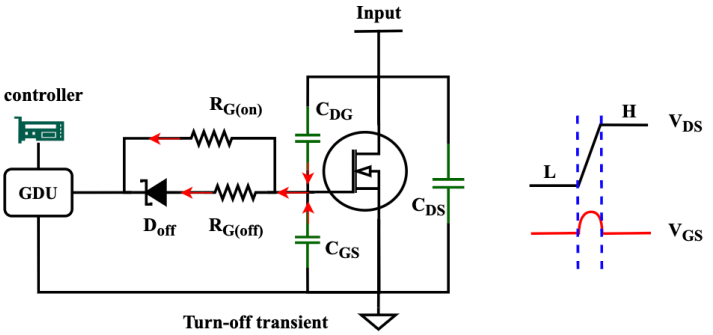


Figure 5.3: Miller current explanation - SiC MOSFET **turn-off** transient process

In [49], it is demonstrated that the reverse-biased placed Schottky diodes D_{on} and D_{off}, depicted in Fig. 5.2 (left), effectively attenuate oscillations on V_{GS}. Also, D_{on} and D_{off} enable the adjustment of the SiC MOSFET's turn-on and turn-off slew

rates. Additionally, the use of external gate circuits can mitigate electromagnetic interference and fine-tune the gate drive strength. Furthermore, gate resistors can function as current regulators, thereby reducing the intensity of inrush current spikes. Due to the presence of Miller current flow, the values of $R_{G(on)}$ and $R_{G(off)}$ cannot be excessively large, as this would induce negative and positive spikes in V_{GS}, potentially causing MOSFET misoperation.

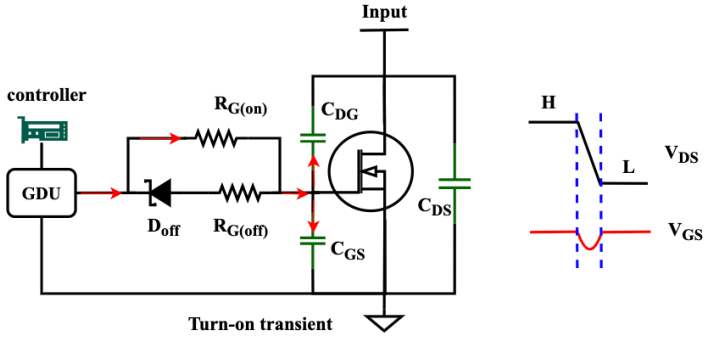


Figure 5.4: Miller current explanation - SiC MOSFET **turn-on** transient process

During the SiC MOSFET **turn-off** transient, as depicted in Fig. 5.3, C_{DG} begins charging and C_{GS} starts discharging. The magnitude of V_{DG} is approximately equal to V_{DS}. Furthermore, the charging current i_c of C_{DG} is larger than the discharging current i_d of C_{GS} owing to V_{DG} being much larger than V_{GS}. Consequently, the Miller current flowing through the gate resistor circuit is predominantly determined by i_c, resulting in a positive voltage surge in the V_{GS} waveform. If the total gate resistance is sufficiently large, this positive voltage spike can exceed the gate threshold voltage $V_{GS(th)}$, potentially causing misoperation of the SiC MOSFET.

$$i_c = C_{DG} * \frac{dV_{DS}}{dt} \approx C_{DG} * \frac{dV_{DG}}{dt} \gg i_d = C_{GS} * \frac{dV_{GS}}{dt} \tag{5.1}$$

During the MOSFET **turn-on** transient, illustrated in Fig. 5.4, C_{DG} discharges while C_{GS} charges until the gate voltage reaches its final value. Based on (5.1), the magnitude of i_d which flows from $R_{G(on)}$ to C_{DG} is much larger than that of i_c flowing through C_{GS}. Thus, the Miller current magnitude is nearly the same as that of i_d. If the value of $R_{G(on)}$ is large, a substantial negative spike will be generated on V_{GS} waveform. If the negative surge peak reach below the gate off-threshold voltage, the MOSFET will misoperate. Therefore, the resistance of 2.2 Ω is selected to be the value of $R_{G(on)}$ and $R_{G(off)}$.

The gate resistor circuit shown in Fig. 5.2 (right) was eventually selected. Comparing to the left one, one Schottky diode is saved and the total cost can be slightly reduced. Besides, the PCB footprint layout is simplified as well. Moreover, the total power consumption is reduced because a diode can generate some switching energy losses. Last but not least, due to this gate driver resistor structure, the sink

current faces less resistance and the peak sink current magnitude can be large. (Smaller $R_{G(off)}$ could provide strong pull-down for robust gate drive.) Therefore, the requirement for a fast switch-off process is fulfilled.

According to the output requirements of this H-bridge, an isolated gate driver is necessary. Two suitable options are the UCC21521, a 2-channel gate driver, and the STGAP2SiCSN, a 1-channel gate driver. Given the availability of components, the STGAP2SiCSN was selected. This gate driver provides a maximum isolation of 4.8 kV DC and 1.7 kV AC, and has a sink/source current capability of 4 A. An isolated DC/DC converter is employed to power the components (gate drivers) integrated on the PCB.

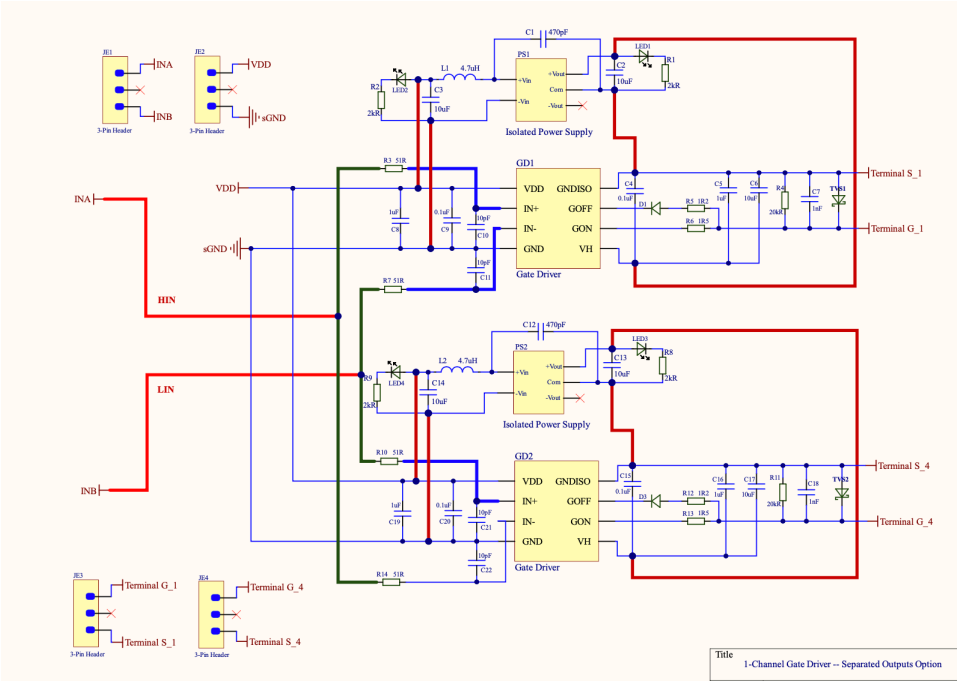


Figure 5.5: Schematic of the gate driver circuits for a half H-bridge

Figure. 5.5 illustrates the schematic of the gate drivers for a half H-bridge. The input signals INA and INB are designed to be complementary to prevent short-circuiting within the half bridge. These input signals are typically generated by the micro-controller, and a small input $R_{in} - C_{in}$ filter can be employed to mitigate ringings caused by non-ideal layouts or long PCB traces due to parasitic effects. However, this filter may introduce a delay or slow down the signal at the output. According to the gate driver datasheet, the recommended values for R_{in} and C_{in} are 51 Ω and 10 pF, respectively. The selection of other components is guided by the specifications detailed in the gate driver datasheet.

Fig. 5.6 illustrates the 3D version of the gate driver PCB board designed in Altium designer. Based on the schematic shown in Fig. 5.5, the footprints of the

gate driver components were positioned. After proper wire routing and placement of the components, the gate driver PCB could be finally designed.

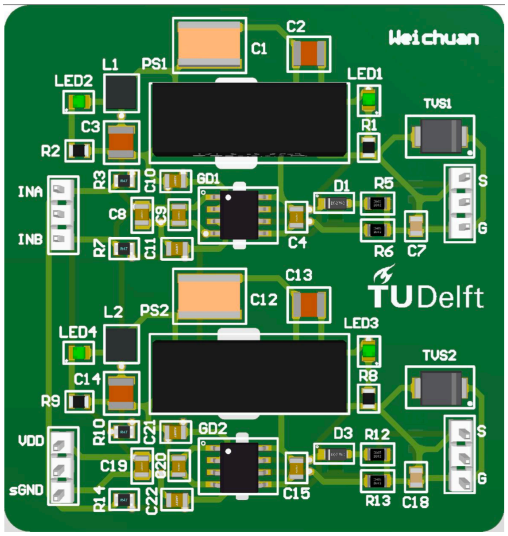


Figure 5.6: PCB board of the gate driver for half H-bridge designed in Altium Designer

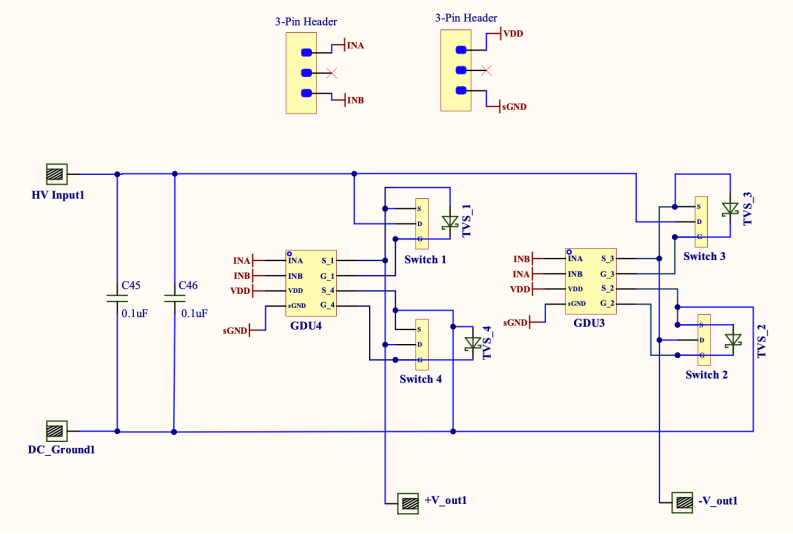


Figure 5.7: Schematic of the main board of the standard H-bridge

Figures 5.7 and 5.8 present the schematic and PCB layout of the standard H-bridge design created in Altium Designer. To improve thermal management, heat sinks are attached to the SiC MOSFETs. Additionally, Zener diodes are placed be-

tween the drain and source terminals of the SiC MOSFETs to prevent breakdown of the MOSFETs owing to large voltage overshoots.

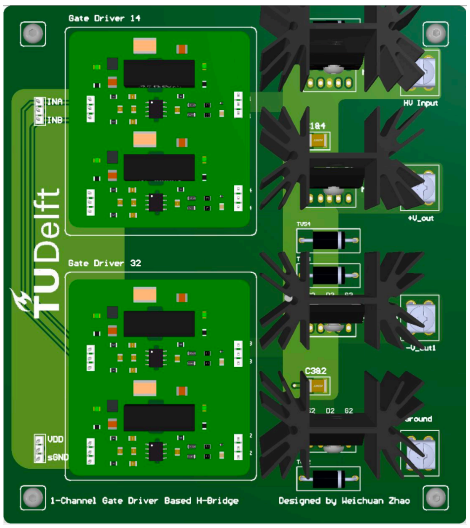


Figure 5.8: The PCB board of the H-bridge designed in Altium Designer

5.2. Standard H-Bridge Validations

The output voltage of the gate driver PCB (half H-bridge driver) depicted in Fig. 5.6 exhibits a complementary behavior, as shown in Fig. 5.9. Also, a magnified view of these waveforms is provided in Fig. 5.10 for detailed analysis. The gate drivers are designed to supply a 20 V signal to the SiC MOSFET gate terminal, a voltage level that is adequate to fully activate and drive these devices efficiently.

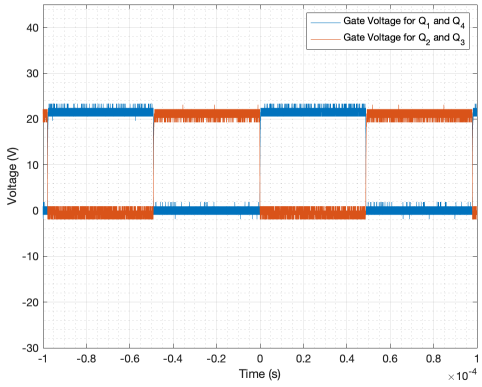


Figure 5.9: Output voltage of the gate driver PCB (half standard H-bridge)

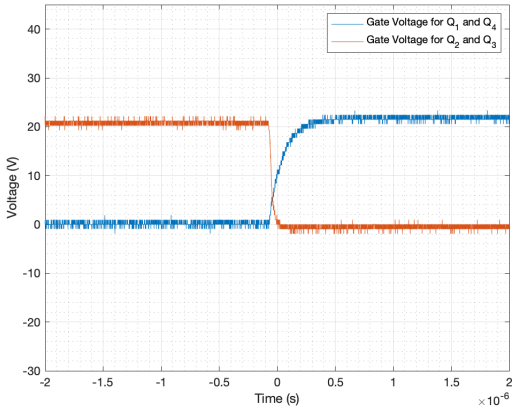


Figure 5.10: Output voltage of the gate driver PCB (zoom-in version)

The output voltage waveform of a standard H-bridge is presented in Fig. 5.11, with a zoom-in view during the switching transients shown in Fig. 5.12. The output waveform exhibits a bipolar nature, with observable ringing, overshoot, and undershoot occurring during the high-speed switching events. These transient effects are primarily attributed to the parasitic inductances and capacitances in the PCB layout. Additionally, the high rates of change in current (di/dt) and voltage (dv/dt) during switching transitions further exacerbate these effects, exciting the parasitic elements and contributing to the overshoot and undershoot phenomena.

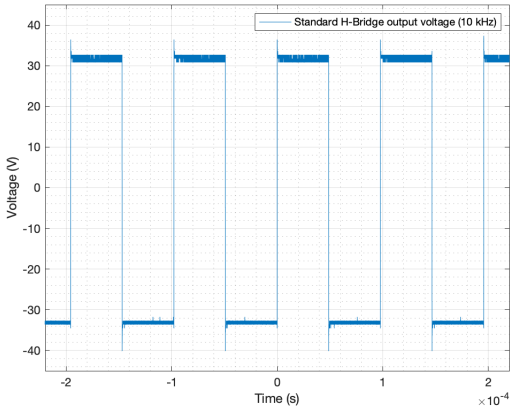


Figure 5.11: Output voltage of the standard H-bridge

From some performed destructive tests, the prototyped H-bridge circuit, decipted in 5.13, successfully generates a bipolar output waveform with an amplitude of maximum 300 V, which is lower than the expected output voltage 80% V_{DS}^{max}.

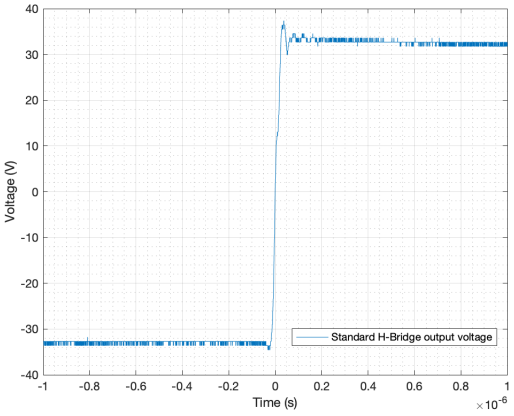


Figure 5.12: Output voltage of the standard H-bridge (Zoom-in version)

5

To enhance its performance, several improvements should be considered. Firstly, a visible dead-time needs to be introduced between the gate signals of the SiC MOSFETs Q_1, Q_4 and Q_2, Q_3 to reduce switching losses. Secondly, the width of the PCB traces should be increased, or a ground plane should be implemented to minimize parasitic inductance and capacitance, which can adversely affect the circuit's efficiency and reliability.

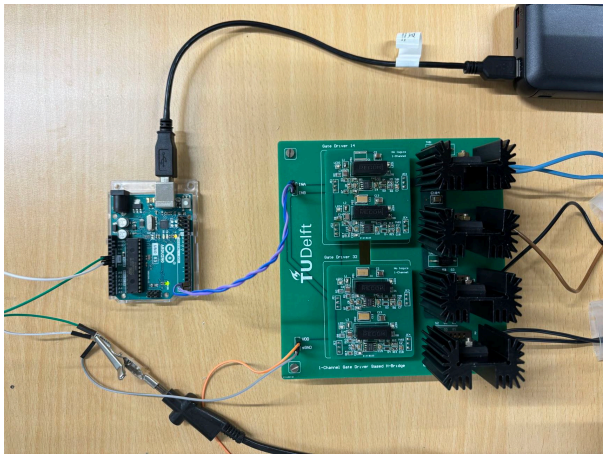


Figure 5.13: Prototyped standard H-bridge driven by the micro-controller (Arduino)

6

Design of a HV Arbitrary Waveform Generator Using a Modular Cascaded H-Bridge Topology[1]

In this chapter, the design guidelines of the HV arbitrary waveform generator are given. As introduced in Chapter 2, the general architecture of the envisioned modular CHB-based HV-AWG with multiple stages is illustrated in Fig. 6.1, highlighting two critical components: the isolated DC/DC supply and the HV H-bridge. Next, the experimental validation results of the designed generator are presented. Finally, recommendations for further improvements to the generator are discussed.

The low-voltage DC input, supplied by a commercial DC source, is converted into either HF AC pulses (hard-switching) or sinusoidal waveforms (soft-switching) to drive a MFT operating at frequencies around 30 kHz. The transformer is designed to provide a galvanic isolation for more than 10 kV between its primary and secondary sides, requiring careful insulation and winding configuration design. The MFT's output voltage is rectified into a high DC voltage and supplied to the HV H-bridge module. By precisely controlling the multiple HV H-bridge modules, the output waveform of this modular CHB-based HV-AWG can be customized.

6.1. H-Bridge Design

For the H-bridge design, the number of output voltage levels N_{level} can be calculated from (6.1) by considering that each H-bridge stage has three states ($+V_{DC}$,

[1]W. Zhao, G. W. Lagerweij, B. P. M. Hurkmans, M. G. Niasar, "Design of a High-Voltage Arbitrary Waveform Generator using a Modular Cascaded H-Bridge Topology, Electronics 13, 4390 (2024).

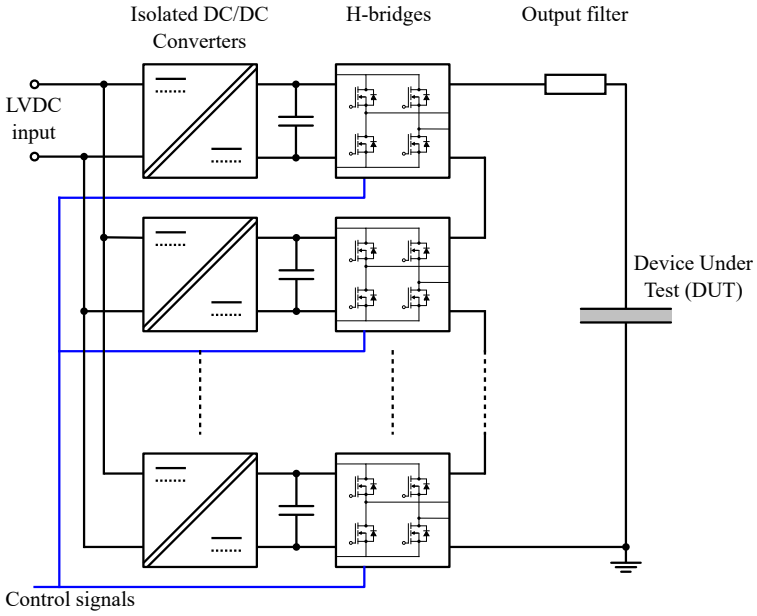


Figure 6.1: Modular cascaded H-bridge topology for HV AWG showing three cascaded stages.

0, and $-V_{DC}$). The number of cascaded H-bridge submodules is N.

$$N_{level} = 2N + 1 \tag{6.1}$$

The number of CHB stages depends on generator output voltage, circuit complexity and cost. With a low number of stages, to fulfill a desired output voltage, the voltage per stage is high, adding cost and complexity to the semiconductor devices. Additionally, the output waveform will have a smaller number of levels. On the other hand, with a large number of stages, more isolated DC/DC converters and control circuits are required. The number of stages is related to the maximum output voltage U_{out}^{max} by formula (6.2), where U_{stage}^{max} is the maximum stage voltage.

$$N = \frac{U_{out}^{max}}{U_{stage}^{max}} \tag{6.2}$$

The limited number of N_{level} in the HV-AWG restricts its ability to accurately approximate arbitrary waveforms, resulting in relatively coarse and rough approximations. Increasing the number of stages would enhance resolution and produce smoother waveforms, particularly important for generating complex shapes such as impulse waveform. However, adding stages increases the HV-AWG system complexity, requiring more auxiliary circuitry. This design demonstrates the feasibility of a cascaded H-bridge based HV-AWG with 3 H-bridge modules. U_{out}^{max} is limited to 8 kV due to the insulation level of the components integrated on H-bridges (e.g. optocouplers). The scalability of the system also depends on the control architecture;

for example, the Typhoon HIL 604 controller could support up to 32 digital outputs. Future work will explore scalability through fiber-optic connections to increase the number of cascaded H-bridges.

6.1.1. Semiconductor Device Selection

In the semiconductor device selection, a trade-off must be made between its breakdown voltage and current capacity (or on-resistance $R_{DS,on}$). In general, the on-resistance increases more than quadratically with increasing breakdown voltage due to the required die thickness [108]. Silicon carbide (SiC) devices with voltage ratings up to 3.3 kV and excellent current ratings are available. However, this restricts the maximum voltage per stage to about 2 kV (considering a 40 % safety factor). Placing multiple low-voltage (e.g., 1.2 kV) devices in series is possible, but this introduces additional complexity to maintain equal voltage sharing across the devices [109], (introduced in Chapter 3). Silicon (Si) devices with higher voltage ratings are commercially available because the technology is more mature than SiC, resulting in a low price. However, they typically have much larger on resistances than an equivalent SiC MOSFET would have.

The current rating of the applied switches can be divided into repetitive peak current $I_{d,pk}$ (during switching transients) and the RMS current $I_{d,rms}$, which determines the thermal performance. For the proposed HV-AWG, the generator drives an RC load, and a considerable amount of current will only be drawn during the switching transients. To accurately replicate the fast transient overvoltages that insulation materials might encounter in real applications, the waveform generated by the HV-AWG must have a relatively short voltage rise time t_r. The peak current through the HV H-bridge module is given by (6.3). Considering the HV-AWG stage output U_{out}^{max} of 3 kV, for a rise time of about 0.6 µs and a maximum load C_{DUT}^{max} of 60 pF (extra 20 pF for parasitics C_{par}), the permissible pulsed drain current I_{DM} of the selected MOSFET should be larger than 0.4 A ($I_{d,pk}^{max}$).

$$I_{d,pk}^{max} = (C_{DUT} + C_{par})\frac{dU}{dt} \approx (C_{DUT}^{max} + C_{par})\frac{U_{stage}^{max}}{t_r} \tag{6.3}$$

$$I_{d,rms}^{max} \approx 2\pi f_s^{max} \cdot U_{stage}^{max} \cdot (C_{DUT}^{max} + C_{par}) \tag{6.4}$$

If the HV-AWG device is used to perform sample breakdown tests, to obtain the required t_r, the total resistance in the circuit (MOSFET $R_{DS,on}$ and external resistance R_{ext}) should be limited. For an RC output circuit, the 10–90 % rise time can be approximated by 2.2τ, where τ stands for RC time constant. For the prototype HV-AWG, the value of R_{tot} is selected as 14 kΩ, resulting a maximum fault current of 0.57 A, when the maximum sample voltage U_{out}^{max} 8 kV is applied. Owing to the low capacitive load application, for an AWG output frequency f_s of 1-10 kHz, the permissible continuous current of the selected MOSFET should be above $I_{d,rms}^{max}$ (0.04 A), which is easily achievable.

Considering the component's price and availability, the Si MOSFET of type IXTT0-2N450HV is selected, which has a continuous current capability of 0.2 A (0.6 A for I_{DM}) and voltage limitation of 4.5 kV, with an $R_{DS,on}$ of around 625 Ω. Thus, U_{stage}^{max}

is decided as 2.7 kV, considering a 40% safety margin and the number of stages N should be 3.

During the HV testing, if the insulation sample breaks down, the HV-AWG output is momentarily short-circuited, causing a large current pulse to be drawn either once or multiple times in a quick succession. This short-circuit current can be limited by the resistance in the 3-stage CHB circuit, which includes the Si MOSFET $R_{DS,on}$ multiplied by two times the number of stages N, and an external current limiting resistor R_{ext} with a value of 10.25 kΩ, calculated by (6.5).

$$R_{ext} = R_{tot} - 2NR_{DS,on} \tag{6.5}$$

For breakdown testing of insulation samples, a smaller t_r and faster switching performance can be ensured by selecting a smaller external resistance R_{ext}, particularly when the HV H-Bridge utilizes the semiconductor devices with higher current ratings or when the required output voltage U_{out} for sample breakdown is lower. Additionally, if the current measurement sensor exhibits extremely high sensitivity, R_{ext} can potentially be eliminated. In cases where the arbitrary waveform generator is employed solely for aging insulation samples over a fixed duration, rather than for breakdown testing, R_{ext} can also be omitted, allowing the generation of waveforms with exceptionally short t_r values. As R_{ext} can be significantly reduced in these scenarios, the achievable t_r can be improved, thus expanding the applicable range of sample loads C_{DUT} for testing.

6.1.2. Gate Driver Circuit

Because the HV H-bridge circuits' reference potentials are switching with the output voltage, high isolation is required between the HV H-bridge and control circuit. This isolation concerns the gate signals, gate driver supply voltages, and optional feedback signals such as measurements or status signals. Optical signal isolation is one of the feasible choices for the considered output voltage levels, either using a high-isolation optocoupler or fiber optics. The rest of the gate drive circuitry must only withstand the voltages inside a single HV H-bridge stage. This concept is shown schematically in Fig. 6.2, where the non-isolated gate driver, red enclosed, is implemented using a BJT push-pull stage with split output and the isolation barrier is shifted towards the optocoupler and isolated DC/DC converter. Comparing to the core-isolation method [110, 111], the optical-isolation method excels in its superior high-voltage performance, faster signal transmission and response, reduced electromagnetic interface and enhanced safety and reliability.

The isolated DC/DC converter generating the gate drive voltages has a limited isolation voltage. In HV converters, the auxiliary power supply is usually derived from the submodule voltage, eliminating the need for full isolation to earth [112]. It is also possible to add a tertiary winding to the transformer to power the PE-based components integrated on the HV H-bridge PCB, described in Section 6.4

6.1.3. Over-Current Protection

Typically, during insulation testing, the fast-switching capability of the HV-AWG is crucial due to noise reduction, improved thermal management, and accurate simu-

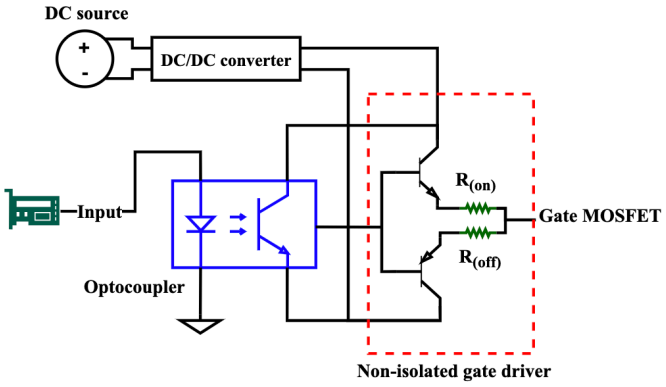


Figure 6.2: High-voltage gate driver using a high-isolation optocoupler & DC/DC converter, and a non-isolated driver circuit.

lation of field strength. Using an R_{ext} with approximately 10 kΩ would significantly slow down the t_r of the generated arbitrary waveform. An over-current protection circuit should be designed and implemented to prevent the breakdown of HV H-bridge components caused by the high dv/dt and current spikes during sample testing failure.

The current measurement sensor of the H-bridges and protection circuitry are integrated and used to address the issue of over-current. If the selected current sensor has a wide measurement range (e.g., -20 to $+20$ A), the measured signal will be noisy, with an inaccuracy of several 100 mA. Since the current rating of the designed HV H-bridge is only 0.2 A, a current sensor with a lower measurement range should be selected. Moreover, the current sensor must provide enough space for the connection cable to pass through and have sufficient sensitivity to detect the over-current pulses. Consequently, the current sensor of type LEM CTSR 0.6-P has been selected, which features a low measurement range of -0.85 A to 0.85 A and a relatively fast response time of 3.5 µs (0 to 90 % response time). The detailed and complete HV H-bridge design process is elaborated in Appendix I.

6.2. Isolated DC/DC Converter Design

6.2.1. Transformer ZVS Driving Circuit

The ZVS driver was selected for the transformer driving circuit to address the issues of power losses and operational instability associated with hard switching. In hard-switching circuits, MOSFETs switch at high voltage and current levels, leading to significant switching losses and electromagnetic interference. These losses can degrade performance, especially under varying load conditions. ZVS, on the other hand, ensures that the MOSFETs switch at zero voltage, which reduces the di/dt during the transient period, minimizing EMI and power losses. This contributes to better thermal management and overall system stability. Therefore, the transformer

driving circuit should employ a ZVS driver that generates a sinusoidal waveform. This significantly reduces the di/dt during transient period, thereby decreasing the disturbances on the voltage waveform, which is crucial for accurate HV waveform generation. Additionally, the ZVS driver offers a voltage amplification factor of π.

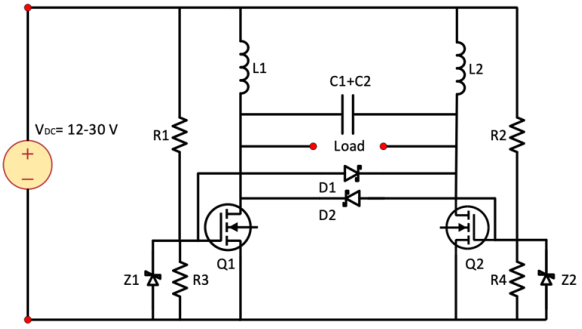


Figure 6.3: Schematic of the ZVS driver before self-oscillation

The ZVS driver is self-oscillating if sufficient input voltage is applied. As the driving circuit starts, one of the MOSFETs is turned on first due to the resistance tolerance range variation in the divider resistors and the difference in MOSFET gate threshold voltages. According to Figure 6.3, if $V_{GS(1)}$ rises faster than $V_{GS(2)}$, Q_1 reaches its threshold voltage earlier and is triggered faster. Then, $V_{DS(1)}$ reduces and the charges flow through the Schottky diode D_2 instead of the gate of MOSFET Q_2. As a result, $V_{GS(2)}$ is pulled low and $V_{DS(2)}$ becomes larger. Therefore, Q_2 remains off. Due to the LCR resonant circuit shown in Figure 6.4, at a particular instant, $V_{DS(2)}$ will also be pulled low. The charges will then flow through D_1. Conversely, $V_{GS(1)}$ will be pulled low and Q_1 will be switched off, resulting the increase of $V_{DS(1)}$. D_2 will be switched-off and the charges will be added on the gate of Q_2 through the voltage divider. Thus, $V_{GS(2)}$ rises and Q_2 will be triggered and the oscillation continues.

In Figure 6.4, the driver capacitors C_1, C_2 have a value of 0.3 µF, leading to a total capacitance C of 0.6 µF. The internal inductances L_1, L_2 are approximated at 98 µH. When Q_1 is ON and Q_2 is OFF, the resonant circuit can be simplified as shown in Figure 6.5, assuming the load resistance R is negligible. Its resonant frequency f_o can be derived as (6.7):

$$V_{out} = \frac{Z_2}{Z_1 + Z_2} \cdot \frac{V_{DC}}{s} = \frac{\frac{1}{L_1 C}}{\left(s + \frac{1}{2RC}\right)^2 + \frac{1}{L_{load}C} + \frac{1}{L_1 C} - \frac{1}{4R^2C^2}} \cdot \frac{V_{DC}}{s} \tag{6.6}$$

$$\omega_o^2 = \frac{1}{L_{load}C} + \frac{1}{L_1 C} - \frac{1}{4R^2C^2} \tag{6.7}$$

In this study, the input voltage of the ZVS circuit is V_{in}, limited by 35 V_{rms}. The waveform polarity of $V_{DS(1)}$ and $V_{DS(2)}$ is complementary. The average value V_{avg} of the obtained $V_{DS(i)}$ (half-sine waveform) is V_{in}, resulting a peak value of πV_{in}. The

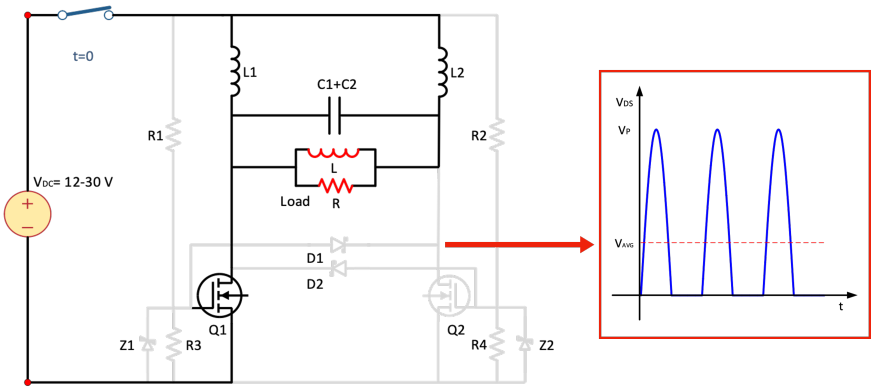


Figure 6.4: **Left**: Schematic of the ZVS driver while MOSFET Q_1 is ON and Q_2 is OFF. **Right**: Drain-source V_{DS} waveform of MOSFET Q_2

voltage applied to the inductive load (transformer primary winding) is a complete sinusoidal waveform. For continuous operation, the input voltage of the ZVS driver should be limited within 80 % of $V_{in(max)}$. As a result, the peak value of the driver output U_p should be 28π.

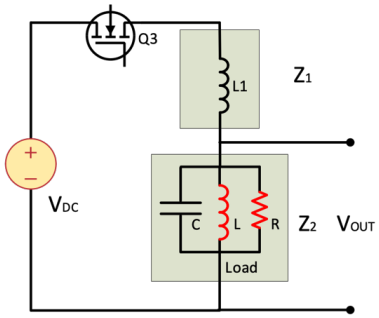


Figure 6.5: Schematic of the simplified resonant circuit of the ZVS driver when $Q_{1(on)}$ and $Q_{2(off)}$ are present

6.2.2. Medium-Frequency Transformer Design

A medium-frequency transformer is used to step up the voltage generated by the ZVS driver and provide high isolation between the H-bridge stages and the LV driving circuitry. The output of the transformer is rectified to generate the DC link voltage. The target output voltage is 10 kV, which is higher than $N \cdot U_{stage}^{max}$. The working frequency of the transformer is determined by the ZVS driver, which is tuned to operate above the audible threshold at 25 kHz.

Table 6.1: MF transformer requirements

Parameter	Value	Unit
Working frequency f_s	≥ 25	kHz
Secondary voltage U_{sec}	2.7	kV
Isolation voltage U_{iso}	≥ 10	kV

Transformer Winding Configuration and Core Selection

The split winding configuration, where the windings are placed on two legs of a U-U core, provides several advantages. It offers sufficient creepage and clearance distance between windings, allowing more winding design flexibility and facilitating the placement of additional insulation material to achieve the required isolation level, U_{iso}. Compared to other configurations, the split winding configuration significantly reduces the proximity effect, which is responsible for increased AC losses. By physically separating the windings on different core arms, AC resistance and power losses are minimized. This configuration also enhances airflow and heat dissipation, leading to lower operating temperatures and improved transformer reliability. Furthermore, in HF applications, the reduced parasitic capacitance between the windings helps mitigate unwanted resonances and losses, thereby improving HF performance. However, this configuration has a large leakage inductance, so the secondary voltage drop ΔV is significant. The transformer core should have a large window area but small outer dimensions. According to Table 6.2, two Ferroxcube U100/57/25 core halves of material 3C90 ($\mu_i \approx 1900$) are used due to its relatively large window area, compact size, and low price.

Table 6.2: MF transformer ferrite-core comparison

Core shape	Ferroxcube UU100/114/25	TDK UU93/152/30	EPCOS UU126/182/20	
Core size	100×114	93×152	126×182	mm^2
Window area A_w	52×68	34.6×96	63×140	mm^2
Price	33	51	62	EUR/pc

Transformer Primary Number Selection

After selecting the core, the primary number of turns N_p can be selected based on the effective area A_e and saturation flux density B_{sat} of the magnetic core, and the primary voltage $U_{p(max)}$ using (6.8-6.9). The parameters chosen for the prototype are shown in Table 6.3.

An HV-insulated cable is selected as the primary winding for robust transformer isolation to avoid winding-to-winding and winding-to-core discharges. The cable diameter D_{cable} is 3 mm and the core inner height H_{inner} is measured as 68 mm.

Table 6.3: MF transformer prototype parameters

Parameter	Value	Unit
Source maximum current I_{source}^{max}	≤ 10	A
H-bridge maximum current I_{B}^{max}	160	mA
Transformer maximum primary voltage U_{p}^{max}	$28 \cdot \pi$	V
Minimum saturation flux density B_{sat}^{min}	320	mT

As a result, N_p should be larger than 3 but lower than 22. Thus, N_p is set to 5.

$$N_p \geq \frac{U_p^{max}}{2\pi f_s A_e B_{sat}^{min}} = 3 \tag{6.8}$$

$$N_p \leq \frac{H_{inner}}{D_{cable}} = 22 \tag{6.9}$$

The measured inductance of the primary winding is 106 µH with core (L_{load}). The internal capacitance and inductance of the ZVS driver are 0.6 µF (C) and 98 µH (L_1), resulting in a transformer operating frequency of around 28 kHz according to (6.7).

Transformer Turn Ratio Selection

To achieve the desired secondary output voltage from a ZVS driver with limited input voltage, a minimum turns ratio n is required. On the other hand, the transformer secondary current is reflected back to the primary, leading to a maximum n for a current-limited source. From (6.10), n can be selected as 50. Thus, the number of the secondary turns N_s is 250. Referring to (6.11), the core remains unsaturated with N_s of 250 turns and the resulted flux density is only 96 mT.

$$\frac{U_{sec}\,[\mathrm{kV_{pk}}]}{U_p\,[\mathrm{kV_{pk}}]} \leq n \leq \frac{I_{source(max)}}{I_{s(max)}} \tag{6.10}$$

$$\hat{B}_{sec} = \frac{\hat{U}_{sec}}{2\pi f_s \cdot N_s A_e} < B_{sat(min)} \tag{6.11}$$

Transformer Secondary Winding (Bobbin) Design

To simulate the breakdown performance of the MFT's insulated winding, insulated twisted-wire samples are selected. As depicted in Figure 4.21, the minimum breakdown voltage of a single insulated wire layer is approximately at $3.5\,\mathrm{kV_{pk}}$, with a testing frequency of around 33 kHz. Considering that the maximum required U_{sec} is only $2.7\,\mathrm{kV_{pk}}$, and assuming a derated permissible breakdown voltage of a single wire layer at $1.5\,\mathrm{kV_{pk}}$, a winding comprising more than two layers can safely withstand the desired voltage. As a result, both the disc-type and layer-type windings are viable options. The disc-type winding is favored due to its superior high voltage capabilities. For the MFT secondary winding, every disc segment is expected to

handle around 1.5 kV. In total, 6 discs should be provided (to satisfy the desired U_{iso}). Moreover, seen from Figure 6.6, an isolation turn is introduced to be added between adjacent winding discs to avoid the disc-to-disc discharges. By wrapping this isolation turn around the bobbin, it separates the adjacent discs and makes sure that the last turn of the upper disc segment does not touch all the other layers of the adjacent lower disc segment. The designed bobbin has rounded corners and sufficient disc-to-disc creepage distance to prevent flashovers.

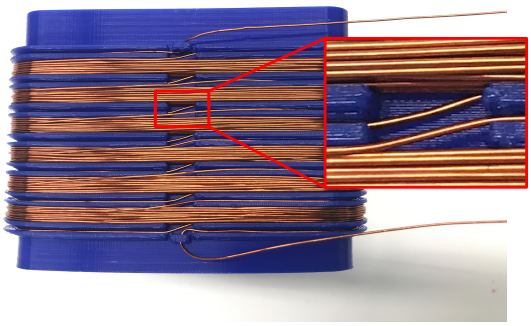


Figure 6.6: Medium frequency transformer secondary winding with isolation turns

Transformer Insulation Selection

Typically, transformer insulation system design involves two types of dielectrics: liquid (e.g. transformer or silicone oil) and solid (e.g. epoxy or silicone rubber). While liquid dielectrics offer lower loss and efficient cooling, the solid dielectrics present advantages such as allowing for compact insulation systems, resistant to environmental factors (e.g. moisture and contaminants), cleanliness and eco-friendliness, along with higher thermal conductivity κ.

Table 6.4: MF transformer insulation material properties

Material	ϵ_r	$\tan\delta\,[10^{-4}]$ @ 10 kHz	κ [W/(mK)]
Epoxy CY225	2.8	100	0.21
Silicone rubber	3.1	25	0.30

Based on the Steinmetz equation (6.12), the loss of the transformer core of type 3C90 can be calculated. The value of the parameters ($k = 5.69$, $\alpha = 1.46$, and $\beta = 2.75$) are all obtained from the manufacturer. The obtained maximum core loss

at room temperature $25°C$ is around 7 W.

$$P_{l(core)} = k f_s^{\alpha} B_{sec}^{\beta} V_e \tag{6.12}$$

$$P_{l(winding)} = R_{AC} I_{s(max)}^2 \approx 0.4\,W \tag{6.13}$$

The total transformer winding loss can be calculated by (6.13). It can be noted that R_{AC} is measured from Bode-100 with a value of 15 Ω and the obtained loss is around 0.4 W. Since the total power rating of the designed transformer is around 7.4 W, the considerations regarding to loss and heat dissipation cannot be simply disregarded. According to the findings shown in Table 6.4, if the solid-type dielectrics are favored, silicone rubber emerges as the preferred choice owing to its comparable lower loss $\tan\delta$ [113], superior thermal conductivity, and ease of preparation and casting. These properties make it an ideal choice for the MFT used in the arbitrary waveform generator. In HV applications, ensuring sufficient creepage and clearance distances between the windings is crucial, and silicone rubber's flexibility and ease of preparation allow for compact insulation systems while still providing the necessary dielectric strength.

In [113], the twisted-wire samples insulated with silicone rubber are verified to exhibit higher breakdown voltages compared to those cast in epoxy resin. This result substantiates the appropriateness of silicone rubber as the preferred insulation material. The twisted-wire samples are employed to simulate transformer disc wires, which have multiple points of contact, thereby simulating real-world operational conditions.

Transformer Bobbin Cup and Bushings

The transformer secondary winding is positioned within the bobbin cup, illustrated in Figure 6.7, which features grooves to accommodate the secondary turns and guides for the connection cables and secondary wire terminals. The bobbin cup geometry has an inner cavity designed to accommodate the core. Additionally, an air gap of 17 mm is maintained between the core and the main compartment, which houses the secondary windings. According to the findings in [114], the breakdown voltage of air at 57 kHz is reduced to 66% of the standard air breakdown voltage of 3 kV/mm. Under the assumption of worst-case operating conditions, the air breakdown voltage is conservatively set at 0.6 kV/mm. The designated air gap is sufficient to sustain the insulation requirement of 10 kV, when the core is grounded. This gap plays a critical role in minimizing the risk of discharge between the windings and the core. The output terminals of the secondary windings are attached with the connection cables, going through the extended part of the bobbin cup. The main compartment is filled with silicone rubber to generate the required isolation.

6.3. Experimental Results

Figure 6.8 illustrates the non-breakdown experimental configuration of the 3-stage CHB based HV-AWG. The setup includes a 10 kV MFT that provides galvanic isolation between primary and secondary sides. The output voltage from the MFT is subsequently rectified by the 6 kV, 1 A rectifiers and then stabilized using a 3 kV,

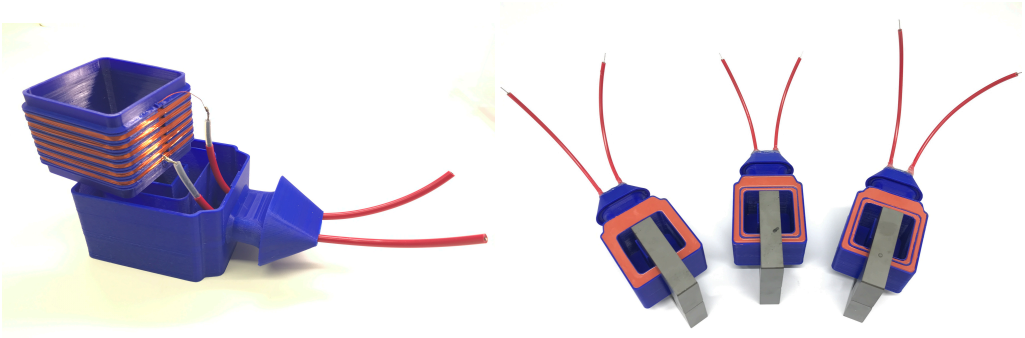


Figure 6.7: MFT secondary winding before silicon rubber casting (left) and after casting (right)

1.0 μF capacitor. This stabilized voltage is then supplied to a series of cascaded HV H-bridge modules, which are responsible for synthesizing the desired arbitrary waveforms.

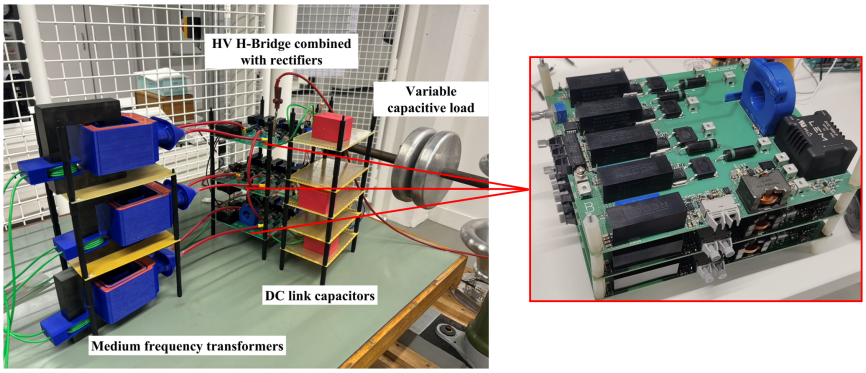
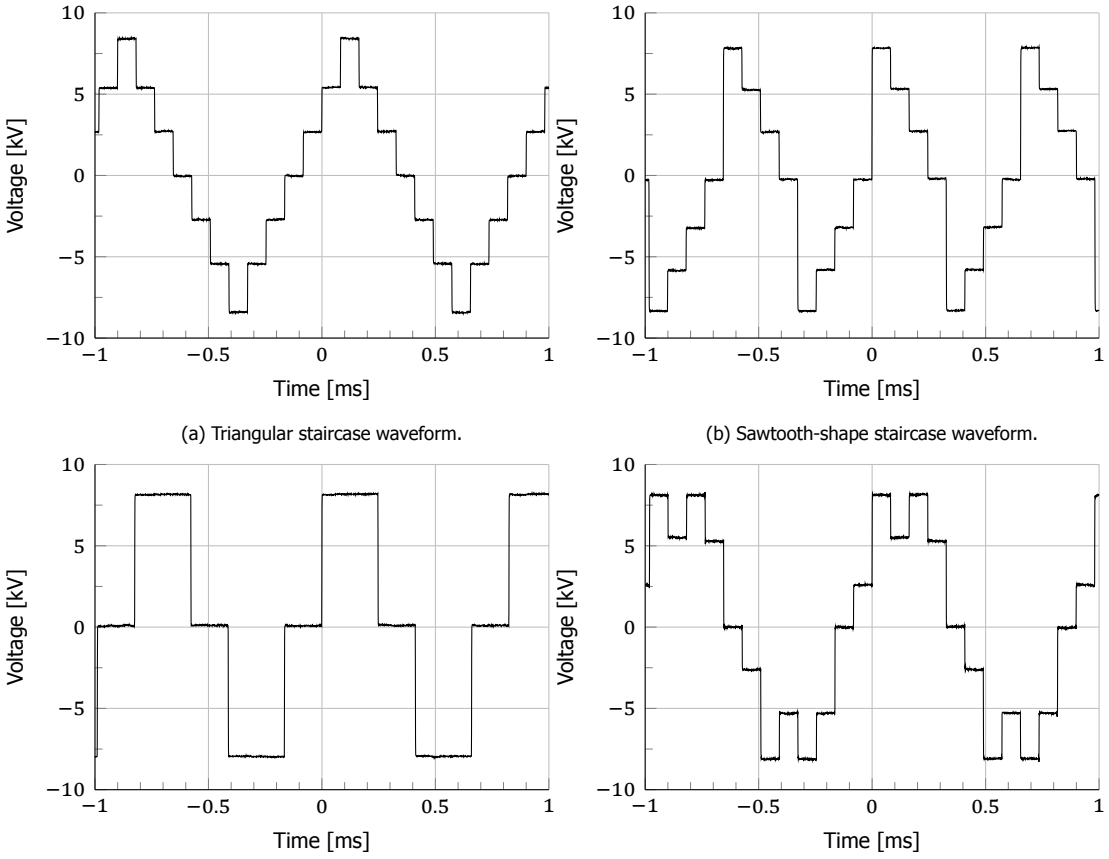


Figure 6.8: The experimental set-up of the 3-stage modular CHB based HV-AWG

In this configuration, the medium frequency transformers ensure safety and isolation by preventing direct electrical connection between the high-voltage output and the low-voltage control circuitry, thereby protecting sensitive components. The rectification and stabilization process involving the capacitor smooths out voltage fluctuations, ensuring a consistent HV output for subsequent stages. The cascaded HV H-bridge modules then modulate this HVDC into complex AC waveforms as required for the application, leveraging the high switching speed.

As illustrated in Figure 6.9, the customized waveforms – namely stair (triangle), saw-tooth, pulse and complex shapes are generated with a peak voltage of around 8.1 kV. The output waveforms exhibit up to 7 distinct voltage levels. According to Figure 6.10, achieving an output voltage range from 0 to 8.1 kV with a load of 40 pF (plus an additional 20 pF for the measuring probe) results in a rise time of



(a) Triangular staircase waveform.

(b) Sawtooth-shape staircase waveform.

(c) Three-level square waveform.

(d) Complex-shape staircase waveform.

Figure 6.9: Customized output waveforms of the 3-stage modular CHB based HV-AWG. For waveform (c), three H-bridge stages are controlled as a single stage.

approximately 1.2 µs. In contrast, under no-load conditions, the rise time is reduced to approximately 800 ns. By modifying the input signals, it is possible to obtain the desired high-voltage waveforms with specific shapes.

Switching and conduction power loss analysis: The output waveform of this 3-stage CHB-based HV-AWG is determined as centro-symmetric and repetitive. The total switching energy loss per half cycle $E_{tot,0.5pt}$ can be computed using formula (6.14), where K represents the number of switching transients per half cycle. V_i denotes a specific step voltage in the HV-AWG output waveform, while $V_{(i+1)}$ stands for the adjacent step voltage following V_i.

$$E_{tot,0.5pt} = \frac{1}{2} * \left(C_{DUT} + C_{par}\right) * \sum_{i=1}^{K} |V_{(i+1)}^2 - V_i^2| \tag{6.14}$$

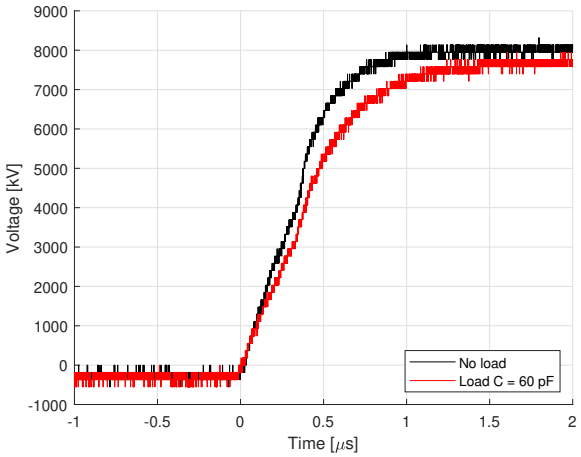


Figure 6.10: Comparison of the case in Figure 6.9 (b) and (c) without load and with 60 pF load

The total switching power loss of the Si MOSFETs $P_{tot(sw,MOS)}$ can be calculated using formula (6.15), where $E_{tot,pt}$ denotes the total switching energy loss per cycle.

$$P_{tot(sw,MOS)} = E_{tot,pt} * f_{sw} = 2 * E_{tot,0.5pt} * f_{sw} \tag{6.15}$$

$$P^{max}_{tot(cd,MOS)} = 2N * R_{DS,on} * \left[2\pi * f_{sw} * (C_{DUT} + C_{par}) * U^{max}_{out}\right]^2 ; N = 3 \tag{6.16}$$

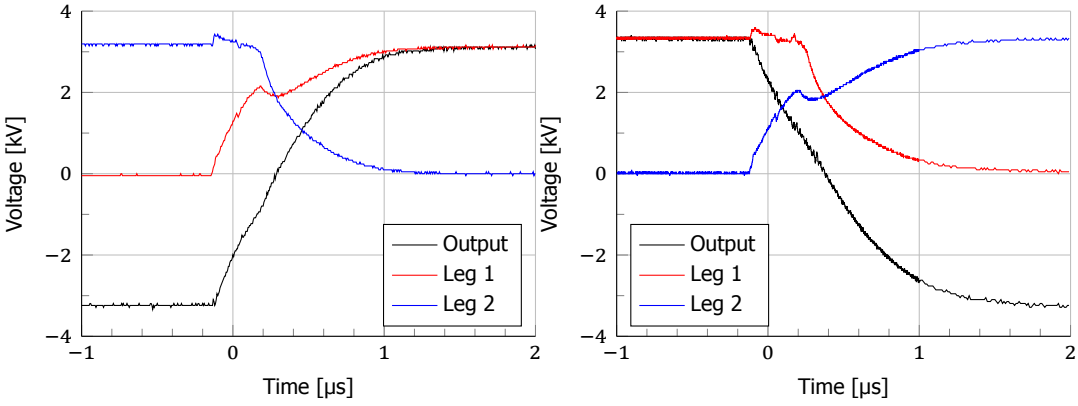
The maximum total conduction power loss $P^{max}_{tot(cd,MOS)}$ can be calculated according to formula (6.16), where N is the number of stages within HV-AWG. Based on the obtained experimental results, the value of $P^{max}_{tot(cd,MOS)}$ is computed as 79 mW.

During the half-switching cycle, if the output waveform of the HV-AWG is designed to rise from 0 V, reach its peak value U^{max}_{out}, and then return to 0 V, as illustrated in cases (a-c) of Fig. 6.9, these configurations result in a lower $P_{tot(sw,MOS)}$, compared to case (d). The $P_{tot(sw,MOS)}$ for cases (a-c) is calculated to be 11.8 W. However, that for case (d) is 18.37 W. Consequently, the conduction loss in the Si MOSFETs is negligible in comparison to the switching loss. To prevent thermal breakdown during switching, it is critical to employ a heat sink with low thermal resistance to ensure effective heat dissipation.

6.4. Discussion

For each individual HV H-bridge module, with a total load C_{DUT} of 60 pF (including 20 pF for the measuring probe), the voltage applied to the test object can be increased to $\pm$3.2 kV. As shown in Figure 6.11, the rise and fall times of the HV H-bridge are approximately 800 ns (without R_{ext}), resulting in a maximum current

peak adjacent to, but less than 0.6 A. Therefore, the H-bridge validation voltage is limited to 3.2 kV. Exceeding this voltage during switching transients causes the current to surpass the $I_{DM(max)}$, potentially damaging the MOSFET layout.



(a) HV H-bridge output voltage rise duration

(b) HV H-bridge output voltage fall duration

Figure 6.11: Output and phase leg waveforms for one H-bridge with 3.2 kV DC voltage and 80 pF load (60 pF for C_{DUT} and 20 pF for C_{par}).

Output voltage scalability: In the prototype design, the optocouplers and auxiliary DC/DC converters are subjected to the entire output voltage U_{out}, if the H-bridge module is positioned near the HV output and the submodules are all connected with copper wires to a controller. Typically, the selected DC/DC converters and optocouplers provide isolation up to 12.5 kV AC for only 1 minute. For extended insulation testing periods, the U_{out}^{max} of the HV-AWG should be around 7.5-8 kV, considering a 40 % safety factor. Therefore, even though the HV-AWG submodule has been validated to achieve a higher output voltage (3.2 kV per submodule, corresponding to an output voltage of almost 10 kV), it is not yet possible to run it at this voltage for prolonged periods.

To achieve a higher HV-AWG output voltage, isolated DC/DC converters and optocouplers with higher isolation ratings are required. However, such components are expensive and bulky. Connecting the H-bridge submodules via fibre optics provides galvanic isolation from the low-voltage control system. For example, using a Typhoon HIL to control all the H-bridge submodules in the HV-AWG removes the need for the optocouplers to withstand the high voltage. Additionally, a tertiary winding can be incorporated on the MFT and encapsulated in silicone rubber. When combined with a rectifier and a buck converter or linear regulator, this tertiary winding provides power to the control circuitry of the H-bridge. This modification eliminates the need for an auxiliary DC/DC converter with a higher insulation level (the selected DC/DC converter only needs to handle the maximum stage voltage U_{stage}^{max}). As a result, the scalability of the CHB-based HV-AWG system can be significantly improved. But all the MFTs should be able to handle the full output voltage

U_{out}.

Semiconductor device selection: Choosing another type of HV MOSFET with larger pulsed and continuous drain current ratings is advisable. This choice accommodates a broader range of the testing load C_{DUT}^{max}. Additionally, it allows for achieving lower values of R_{tot} and t_r. For the lifetime considerations of the HV-AWG, the MOSFETs with lower $R_{DS,on}$ are recommended. Higher $R_{DS,on}$ values result in large losses within the semiconductor device, making heat dissipation more challenging. An external current limiting resistor R_{ext} is recommended to limit the rise time and current since this can be cooled more effectively. For example, the Si MOSFETs of type IXTT1N450HV with $I_{D25(max)} = 1\,A$, $I_{DM(max)} = 3\,A$, and $R_{DS(on)} = 85\,\Omega$ could be selected.

Current sensor selection and protection circuit design: Faulty operation of the protection circuitry can be prevented by selecting a current sensor with reduced sensitivity, particularly when the maximum allowable current of the H-bridge protection circuit (I_{HB}^{max}) is less than the peak drain current of the H-bridge during switching transient ($I_{d,pk}^{max}$). However, with the availability of a Si MOSFET that possesses a higher maximum drain current (I_{DM}), the I_{HB}^{max} can be increased. Consequently, this adjustment mitigates the risk of mis-operation, provided that the maximum capacitance (C_{DUT}^{max}) and maximum output voltage (U_{out}^{max}) remain unchanged. It is advisable to select a current sensor with higher sensitivity to enhance fault detection speed and prevent thermal breakdown of the H-bridge components.

6.5. Summary of Chapter 6

A three-stage CHB-based HV-AWG has been designed and validated to generate customized arbitrary waveforms (saw-tooth, triangular, pulse and complex) with peak voltages of around 8 kV, which forms a platform for insulation material high-frequency tests. The prototype stands out for its simple design, low manufacturing cost, excellent HV performance, and potential for extending the number of stages. Silicon MOSFETs with a maximum blocking voltage of 4.5 kV are used to simplify the design of the HV H-bridge module and reduce cost. Optocouplers and non-isolated gate drivers are utilized to create the corresponding HV gate drivers. A transformer with a split winding configuration, insulated with silicon rubber, creates the isolated DC link voltage of the CHB modules. An isolation turn is placed between adjacent transformer secondary discs to prevent disc-to-disc discharges, effectively mitigating discharges and allowing the transformer to withstand more than 10 kV. A commercially available ZVS driver is also selected to drive the transformer properly. PD-free measurement equipment is necessary to achieve a non-distorted and stable HV output. Measurements show rise times on the order of 1.5 µs when switching all CHBs as a single stage. Switching waveforms are smooth and without overshoot, allowing accurate waveform reconstruction.

7

Planar Transformers[1]

The medium frequency transformer within the aforementioned CHB-based HV-AWG has the potential to be substituted with a PCB planar transformer. Compared to traditional MV wire-wound transformers, MV PCB planar transformers offer several superior properties, including higher power density, enhanced energy transfer efficiency due to reduced copper and core losses, improved thermal management (easy for heat sink application), increased reliability, and easier integration. The planar design of PCB transformers provides a larger surface area for heat dissipation, while the compact size shortens the winding length, leading to reduced magnetic flux leakage and lower electromagnetic interference (EMI).

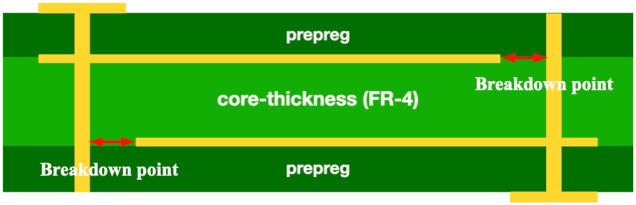


Figure 7.1: Cross-section of the PCB electrode used for interlayer breakdown

In [115], C. Spro conducted comprehensive research on the electrical performance of various planar transformer winding types, offering valuable insights to optimize the winding design. Furthermore, in [116], R. Wang presented a detailed design methodology for MV PCB transformers. This study demonstrated that applying a semiconductive coating to the winding surface effectively mitigates severe electric field stress at the winding edges. Furthermore, the treatment of the winding terminals successfully eliminated surface partial discharge in the transformer.

[1] W. Zhao, M. G. Niasar, Aging Characteristics of FR-4 at Different Frequencies, 2025 IEEE Conference on Electrical Insulation and Dielectric Phenomena, submitted.

The winding turns of the planar transformer are insulated with Flame Retardant 4 (FR-4) and embedded within the prepreg, similar to the PCB electrode samples depicted in Figure 7.1. In addition to its affordability, FR-4 exhibits robust mechanical strength and thermal conductivity, making it suitable for high-power applications. According to Ampere's force law, the substantial currents involved can induce significant mechanical stress on the transformer windings. Despite these advantages, the electrical properties of FR-4 remain underexplored.

In [117], Albert performed both short- and long-term breakdown tests on PCB electrodes at frequencies of 50 Hz, 130 kHz, and 190 kHz to investigate interlayer and layer-to-layer breakdown phenomena. However, the analysis of short-term breakdown voltages did not include a Weibull distribution analysis to assess failure rate probabilities. Furthermore, the long-term tests lacked effective accelerated aging results, as none of the PCB electrodes tested experienced breakdown. Consequently, additional experiments are required to conduct a more thorough investigation of the PCB insulation material FR-4.

7.1. Interlayer Breakdown Tests of PCB Electrodes at 50 Hz

The PCB electrodes in the cross-sectional version, depicted in Fig. 7.1, were designed specifically for interlayer breakdown tests. The core material, FR-4, was chosen with a thickness of 0.71 mm, adhering to standard specifications to ensure cost effectiveness. Additionally, the distance from the edge of the electrode layer to the via is precisely 4.0 mm, as indicated by the red arrows.

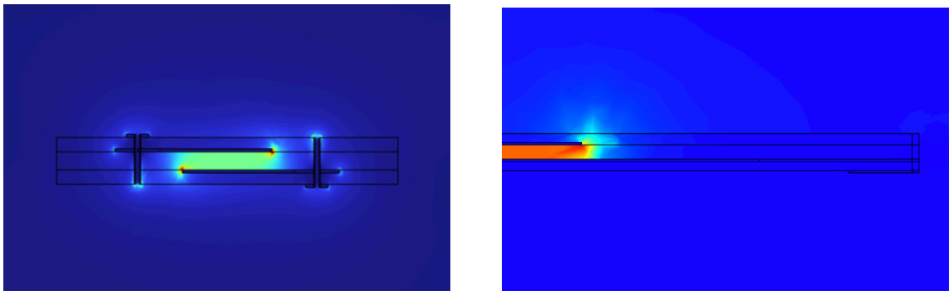


Figure 7.2: Overall electric field strength distribution (Color red symbolizes high field strength.)

Figure 7.2 presents the field strength distribution of the PCB electrodes under HV conditions, derived through numerical simulations. Notably, the field strength peaks at the edges of the electrode layers, known as the triple points. If the core thickness (FR-4 thickness) is sufficiently large, interlayer breakdown is more likely to occur along the interface between the prepreg and core material.

Figure 7.3 and 7.4 illustrate the schematic and experimental set-up, used to study the interlayer breakdown of the 4 mm PCB electrodes. This setup is employed for both HV ramp sinusoidal breakdown and HV accelerated aging tests. A current-

limiting resistor with a resistance of 75 kΩ is added to limit the current following a breakdown event. Upon breakdown, surge currents with high rise rates can occur, and the inclusion of this resistor increases the circuit's time constant, τ. Additionally, the PCB electrodes are submerged in silicone oil to prevent the occurrence of partial discharges.

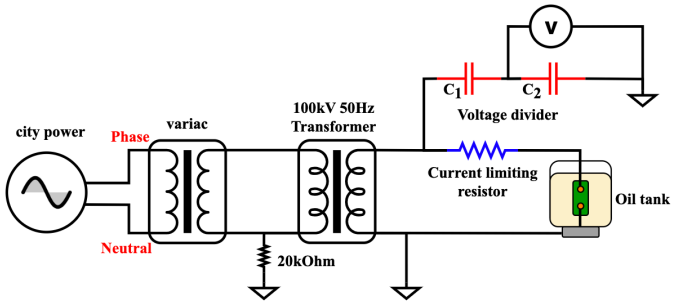


Figure 7.3: Schematic of the experimental set-up at 50 Hz

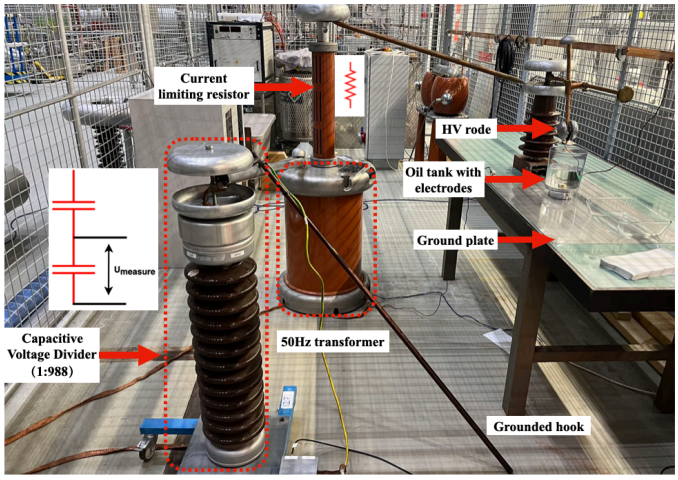


Figure 7.4: Experimental setup for PCB electrode breakdown tests at 50 Hz

Figure 7.5 illustrates various cases of interlayer PCB breakdown. Based on the obtained ramp sinusoidal breakdown data, if the median value is considered as the interlayer breakdown voltage, the PCB electrode breakdown voltage is determined to be 28.6 kV_{rms}, as shown in Fig 7.6. This corresponds to a field strength of approximately 7.2 kV/mm. However, this value is much lower compared to the breakdown results presented in Sections 4.1 and 4.2 for OIP and epoxy samples.

The power law equation governing the accelerated aging experiments is given in Equation (7.1). Additionally, the median time to breakdown is utilized for con-

structing the aging curve.

$$t = k\left(\frac{E}{E_0}\right)^{-n} \tag{7.1}$$

$$\log(t) = -n \cdot \log\left(E/E_0\right) + \log k \tag{7.2}$$

where t is the time to breakdown, k denotes the time to breakdown when the tested PCB sample is subjected to the reference field strength, E is the actual electric field strength in kilovolts per millimeter (kV/mm), and E_0 represents the reference field strength, which is 1.0 kV/mm. Formula (7.2) provides the logarithmic transformation of formula (7.1).

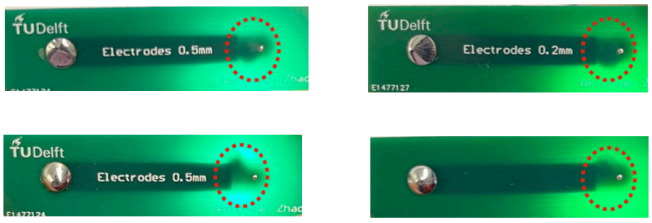


Figure 7.5: The interlayer (edge-to-via) breakdown points at different sides

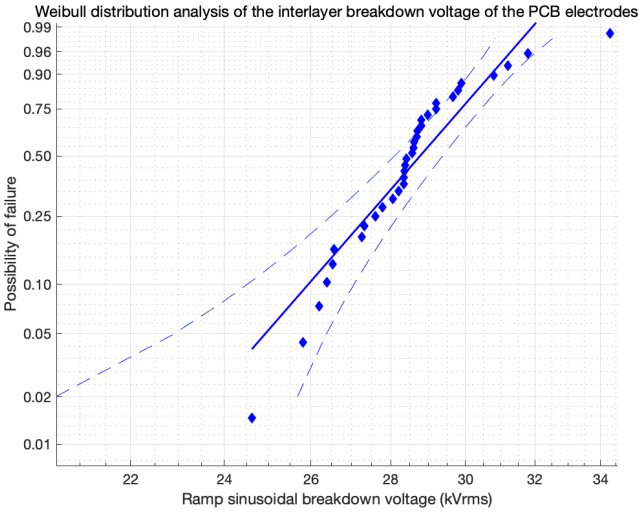


Figure 7.6: Weibull distribution analysis of the PCB electrode interlayer ramp sinusoidal breakdown voltage at 50 Hz

Figure 7.7 presents the HV accelerated inter-layer aging curve for PCB electrodes with a 4 mm gap, tested at a frequency of 50 Hz. In the experiments, the inter-layer

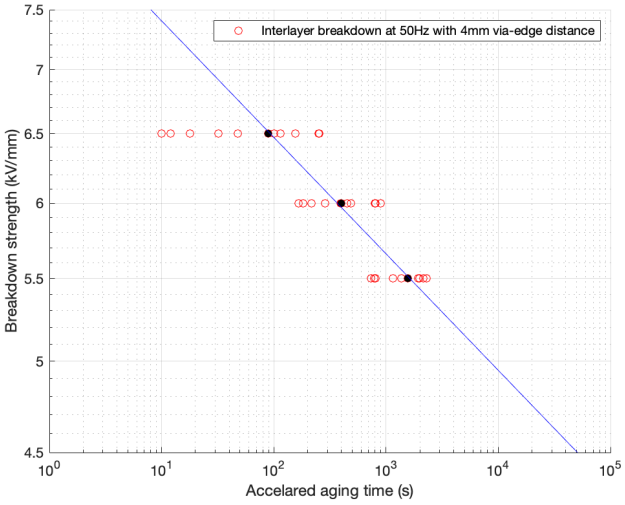


Figure 7.7: The HV accelerated inter-layer aging curve of the PCB electrodes obtained at 50 Hz

field strength of the PCB electrodes was held constant at 5.5 kV/mm, 6 kV/mm, and 6.5 kV/mm. The corresponding time to breakdown values ($t_{5.5}$, t_6, and $t_{6.5}$) were measured for each field strength. However, when the field strength was increased to 7 kV/mm, the time to breakdown (t_7) was observed to be significantly shorter, rendering it unsuitable for inclusion in the aging curve. From the aging curve, the value of n is obtained as 17.14 and that of k is $10^{36.61}$.

7.2. Layer-Layer Breakdown Tests of PCB Electrodes at 50 Hz

During the electrode layer-layer ramp sinusoidal breakdown tests, two types of electrodes were selected: one with a relatively narrow electrode width of 5 mm and the other with a wider electrode width of 10 mm, as depicted in Figure 7.8. Additionally, the thickness of all PCB electrode samples was 0.36 mm. The breakdown results indicated that the layer-layer breakdown voltage for both the narrower and wider electrodes was similar, approximately 21.5 kV_{rms}, corresponding to a breakdown strength of 59 kV/mm, shown in Figure 7.9. Comparing to the interlayer ramp breakdown results, interlayer breakdown occurs more readily because its permissible breakdown strength is 8 times lower than that of layer-layer breakdown.

According to Figure 7.9, a comparative analysis of the ramp breakdown results for wider and narrow PCB electrodes reveals the volume effect. Specifically, for the same probability of failure, the breakdown strength of the narrower PCB electrode samples is marginally higher than that of the wider electrode samples. This phenomenon can be explained using the scaling laws (7.5) and (7.6). Additionally, the permissible field strength of material FR-4 is comparable to, but slightly lower than,

Figure 7.8: PCB electrodes with wider (10 mm) & narrower (5 mm) copper layer

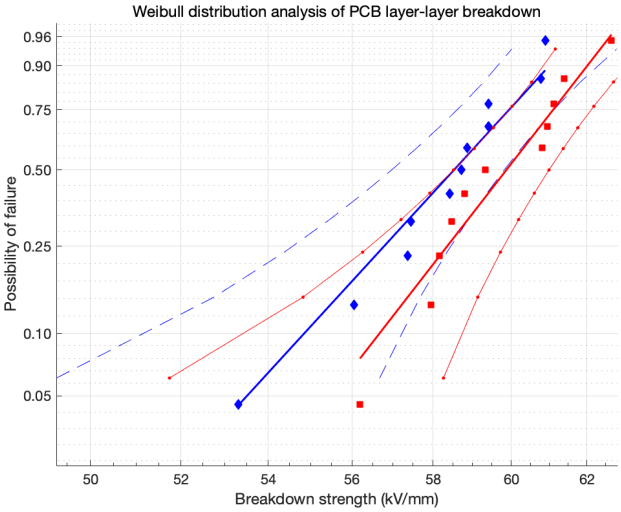


Figure 7.9: Weibull analysis of the electrode layer-layer ramp breakdown strength at 50 Hz (blue for wider electrodes and red for narrow electrodes)

that of OIP.

$$F_1(U) = 1 - \exp\left[-\left(\frac{U}{\eta_1}\right)^{\beta}\right] \tag{7.3}$$

$$R_1(U) = 1 - F_1(U) = \exp\left[-\left(\frac{U}{\eta_1}\right)^{\beta}\right] \tag{7.4}$$

If the value of the applied voltage on the tested electrode is U, its possibility of breakdown or failure $F(U)$ can be expressed by a two-parameter Weibull distribution (7.3). Furthermore, the reliability $R(U)$ of the electrodes under U can be derived using (7.4). Symbol η_1 denotes the scale parameter and β represents the shape parameter. If U equals to η_1, the PCB sample's possibility of failure is 63.2 %.

$$F_n(U) = 1 - R_1(U)^n = 1 - \exp\left[-n\left(\frac{U}{\eta_1}\right)^{\beta}\right] = 1 - \exp\left[-\left(\frac{U}{\eta_n}\right)^{\beta}\right] \tag{7.5}$$

$$\eta_n = \frac{\eta_1}{n^{\frac{1}{\beta}}};\ \ \eta_2 = \frac{\eta_1}{2^{\frac{1}{\beta}}} \tag{7.6}$$

If the surface area of the copper layers in the PCB electrodes is increased by a factor of n, and the applied voltage remains constant at U, the possibility of PCB sample breakdown $F_n(U)$ can be described by equation (7.5). The corresponding scale parameter, denoted as η_n, is given by equation (7.6). Consequently, to achieve a failure rate of 63.2 %, the value of η_2 will be less than η_1.

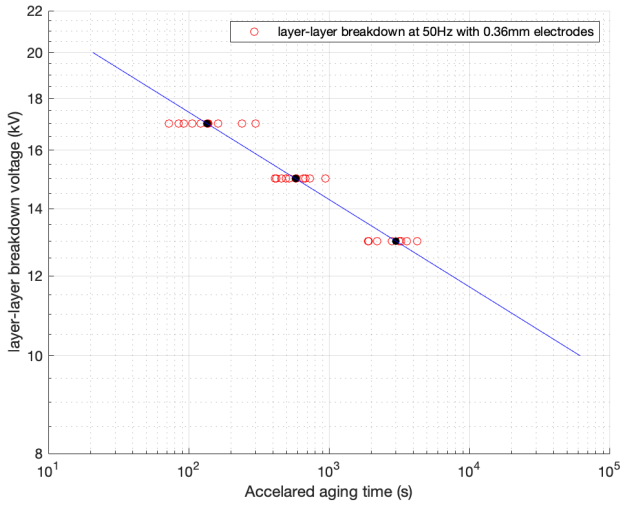


Figure 7.10: The HV accelerated layer-layer aging curve obtained at 50 Hz

During the HV accelerated aging tests of the PCB electrodes, samples were tested at voltages of 17, 15, and 13 kV. For each set of experiments, the median time to breakdown was used as the representative value. Specifically, the PCB electrode samples were subjected to field strengths of 47.22 kV/mm, 41.67 kV/mm, and 36.11 kV/mm, respectively. The resulting aging curve is presented in Figure 7.10. The obtained value of the parameter n_{50Hz} is 11.5.

7.3. Layer-Layer Breakdown Tests of PCB Electrodes at 1 kHz

Figure 7.11 illustrates the schematic of the experimental setup used to investigate the layer-layer breakdown of 0.36 mm PCB electrodes at a frequency of 1 kHz. In

this configuration, the input signal generated by the function generator is initially directed to the Arduino A_0 pin for preliminary analysis. Subsequently, the signal is transmitted to the TREK amplifier, where it undergoes amplification by a factor of 3000. The amplifier is also capable of returning the measured voltage signal, reduced by a factor of 3000, to the Arduino A_1 pin for further analysis.

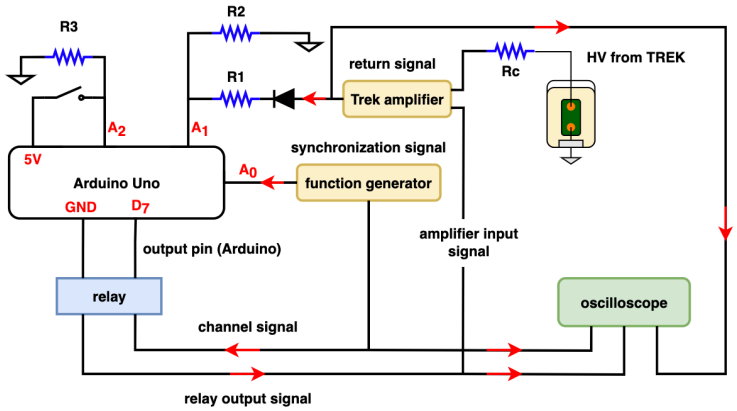


Figure 7.11: Schematic of the HV accelerated layer-layer aging tests of the 0.36 mm thickness PCB electrodes at 1 kHz

Before the breakdown of the PCB sample, the return signal from the TREK amplifier maintains a higher amplitude, preventing the Arduino from triggering the relay. Upon breakdown, the Arduino's A_1 pin detects a significant decrease in the return signal amplitude. If this return voltage falls below a predefined threshold, the Arduino's D_7 pin sends a control signal to deactivate the relay. Consequently, the duration of the circuit's short-circuited state is minimized.

Figure 7.12 illustrates the HV accelerated layer-layer aging curves of the PCB electrodes at frequencies of 50 Hz and 1 kHz. The aging curves are presented with the median time to breakdown at a specified field strength. It is evident that, at the same field strength, the PCB electrodes subjected to the higher frequency of 1 kHz exhibit a shorter time to breakdown compared to those tested at 50 Hz. The value of the aging exponent n is 11.38 for 1 kHz and 11.5 for 50 Hz.

The PCB planar transformer is also anticipated to be integrated into the modular CHB-based HV-AWG, operating at frequencies ranging from 25 to 40 kHz. Furthermore, HV accelerated layer-layer and interlayer aging, as well as the ramp breakdown experiments, can be conducted using the resonant test system described in Section 4.3. However, to achieve the 4 mm interlayer breakdown tests, a minimum of 40 kV_p is required. To meet this requirement, the resonant transformer within the test system should be enhanced, for example, by adding more secondary winding discs or using a larger transformer core.

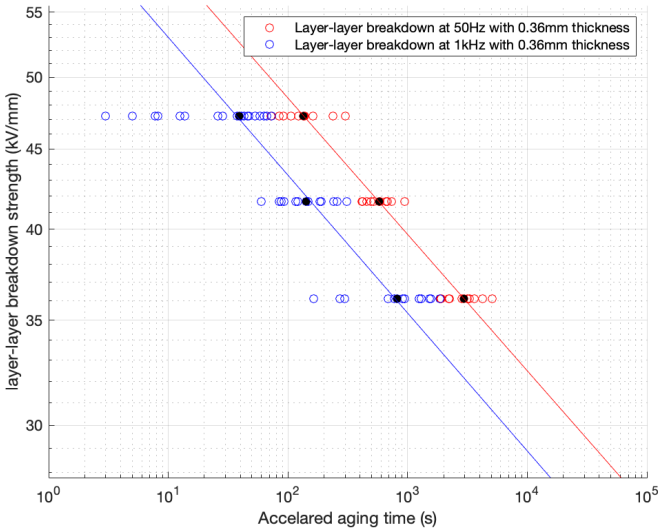


Figure 7.12: The HV accelerated layer-layer aging curve of the PCB samples obtained both at 50 Hz and 1 kHz

7.4. Summary of Chapter 7

Based on the obtained experimental results, it is clear that the layer-layer time to breakdown of the FR-4 samples decreases with increasing frequency of its applied voltage. Additionally, interlayer failure, specifically from PCB vias to copper edges, needs close attention since the the breakdown strength at 50 Hz is just approximately 7.2 kV/mm. When operating the planar transformer at higher frequencies, the interlayer breakdown strength is expected to diminish significantly. Therefore, further research is necessary, involving additional experiments on high-frequency interlayer aging and ramp breakdown of the FR-4 samples. Furthermore, an HV & HF generator must be prepared to conduct the required tests effectively. The resonant test platform, as described in Section 4.3, can be employed to carry out the necessary tests. However, further investigation is required to increase the output voltage of this resonant platform to approximately 35–40 kV. Following an in-depth analysis of the FR-4 material, a planar transformer prototype can be designed, constructed, subjected to validation testing and serve as an alternative for the wire-wound medium frequency transformer.

8

Conclusion

The global energy transition and grid modernization have led to an increased use of power electronics in the power grid, driven by the rise of variable renewable energy sources such as solar and wind. These sources often produce DC power, requiring converters for grid integration. Power electronics, such as inverters and rectifiers, introduce harmonics and transients that can harm and degrade key grid components like transformers, cables and switchgears. Addressing these issues is vital for grid reliability and resilience.

Harmonics and transients from power electronics are complex and unpredictable, making them difficult to mitigate. Enhancing the quality of key grid components is crucial. Before installation, the grid components must undergo rigorous insulation testing to ensure reliability under operational stress. A high-voltage arbitrary waveform generator is essential for testing these components in the future grid, as it can replicate the dielectric stresses caused by power electronic systems. However, developing a reliable arbitrary waveform generator remains challenging, particularly in achieving precise waveform control and high-voltage performance.

This thesis focuses on the design of a 8 kV modular cascaded H-bridge based high-voltage arbitrary waveform generator, which has been tested and validated. The proposed arbitrary waveform generator comprises three core components: a high-voltage H-bridge, a zero-voltage switching driver or standard H-bridge, and a medium-frequency transformer. To achieve an optimized AWG design, five key research questions were identified and systematically addressed.

- **Q1. What are the important considerations of the 10 kV class insulation system design of the medium frequency transformer (25-40 kHz)**

  The identified key considerations in the design of the 10 kV medium-frequency transformer are outlined below, followed by the detailed elaboration.

  - Transformer insulation material selection

- Transformer winding configuration layout and selection
- Transformer secondary winding design
- Transformer core grounding method
- Transformer bushing and bobbin cup design

In the design of medium frequency transformers, the selection of insulation materials plays a critical role. Extensive research and experiments are essential to identify materials with superior dielectric properties that perform optimally within the desired frequency range. Utilizing the Novo-Control for dielectric spectroscopy measurements, combined with breakdown voltage testing of insulated twisted wire samples provided key insights. The experimental results reveal that twisted wires insulated with silicon rubber exhibit higher breakdown voltages compared to those insulated with epoxy resin. Additionally, silicon rubber demonstrates a much lower dissipation factor ($\tan\delta$) across the expected frequency range, indicating reduced energy loss. Based on these findings, silicon rubber was selected as the preferred insulation material.

The configuration layout of the transformer windings and the secondary winding design, are equally important. The transformer secondary output is designed to deliver a high voltage of approximately 10 kV, while the primary side operates with a limited voltage amplitude. To achieve this, a high turns ratio is employed. The secondary winding utilizes a disc-winding configuration with an additional isolation (separation) turn present between adjacent discs to prevent the disc-to-disc discharges. Furthermore, a split-winding configuration is used. The windings across two legs of a U-U core provide adequate creepage and clearance distance between the primary and secondary windings. This design not only improves the integrity of the insulation, but also allows for inclusion of more insulation material. Meanwhile, this configuration creates sufficient leakage inductance, which enhances the output gain and reduces the circuit's power consumption when excited at resonance with the capacitance of the test object. Consequently, the split winding configuration (core-type configuration) is selected for the transformer. To prevent discharges from occurring between the transformer core and the primary winding, the transformer core should be grounded. This is necessary because the secondary winding of the transformer is well-insulated and encapsulated but the primary winding not. In addition to these considerations, the choice of transformer core, the design of transformer bushings and secondary bobbin holder, are critical factors that have also been addressed in Chapter 6, journal publication 3.

- **Q2. Which type of winding configuration is suitable for the medium frequency transformer integrated inside the HV arbitrary waveform generator**

  The split transformer winding configuration is selected owing to its improved heat dissipation (good thermal management), reduced proximity effect and losses, minimized parasitic capacitance and flexibility in design.

- **Q3. What is the best method to deal with the unbalanced voltage sharing of the series-connected switches (e.g. SiC MOSFETs)**

  - For high-voltage applications, the gate balancing core method is typically the preferred approach.
  - For low-voltage applications, the gate balancing core and the improved RC snubber method (b) are the preferred approaches.

  For HV applications, the gate-balancing core (GBC) method emerges as an effective and practical solution, delivering superior output performance. This method is particularly advantageous due to its ability to achieve a short drain-source voltage V_{DS} rise time and maintain precise V_{DS} sharing, even in the presence of significant differences in turn-off delay time $\delta t_{d(off)}$. Furthermore, both the GBC method and improved RC snubber method (b) demonstrate excellent voltage-balancing capabilities, making them suitable for LV applications. However, at higher input voltage levels of the series-connected MOSFETs, the improved RC snubber method (b) encounters limitations, primarily due to the insulation requirements for the balancing inductor, which must be designed to withstand the full stage voltage. This insulation demand poses a challenge for maintaining reliable performance at elevated voltage levels as mentioned in Chapter 3, journal publication 1.

  However, these aforementioned methods introduce additional complexity to maintain equal voltage sharing across the SiC MOSFETs. Extra components and costs are required to build the series-connected SiC MOSFETs. As an alternative, silicon devices with higher voltage ratings are eventually selected owing to its commercial availability and low price.

- **Q4. How to properly design and prototype the HV gate drivers of the series-connected MOSFETs or the Si MOSFETs within the HV H-bridge**

  For the case of the series-connected SiC MOSFETs:

  - If the input voltage of the SiC MOSFET string is below 8 kV, both optically isolated and magnetically isolated gate drivers are viable design options for operation.
  - If the input voltage exceeds 8 kV, the magnetically isolated gate driver design can be employed.

  For the case of the Si MOSFET within the HV H-bridge:

  - If the input voltage is below 8 kV and the HV H-bridge modules are interconnected using copper conductors, the optically isolated gate driver design is selected.
  - If the input voltage exceeds 8 kV, the optically isolated gate driver remains applicable. However, the H-bridge modules should be cascaded using fiber-optics and controlled via a Typhoon HIL system.

For series-connected SiC MOSFETs operating at input voltages below 8 kV, optically isolated gate drivers are recommended due to their shorter propagation delays and ease of integration into high-voltage circuits. Destructive testing has shown that the maximum continuous blocking voltage of commercially available DC/DC converters and optocouplers is limited to 8 kV. When the propagation delays of the gate driver components are not matched, voltage imbalances can occur in the MOSFETs. In such cases, V_{DS} balancing techniques should be applied in conjunction with high-voltage gate drivers to ensure uniform distribution of the V_{DS} across the series-connected devices.

For input voltages exceeding 8 kV, magnetically isolated gate drivers are recommended due to their compact size and lower material cost. This is mainly because gate coupling transformers can be readily designed to operate at higher voltage levels, making them more scalable. However, despite the potential advantages of magnetically isolated gate drivers, this technology is still under development and is not yet commercialized at an affordable price for immediate application in HV H-bridge designs.

For the design of the HV H-bridge module, optically isolated gate drivers are employed. The maximum output voltage of the cascaded H-bridge based HV arbitrary waveform generator is also approximately 8 kV, in alignment with the voltage-handling capabilities of the optocouplers and isolated DC/DC converters. To enhance the voltage capability, fiber optic connections between the HV H-bridge submodules and the control system provide galvanic isolation. For instance, employing a Typhoon HIL for submodule control eliminates the necessity for optocouplers to withstand high voltages. Additionally, a tertiary winding can be integrated on the secondary side of the MFT encapsulated in silicone rubber. This tertiary winding, in conjunction with a rectifier and either a buck converter or linear regulator, supplies power to the H-bridge control circuitry. Consequently, this design modification eliminates the need for an auxiliary DC/DC converter with high insulation requirements, as the selected DC/DC converter only needs to accommodate the maximum voltage of the submodules.

- **Q5. Which switching topology is suitable to generate the input voltage of the medium frequency transformer**

  - Soft-switching topology is preferred.

Using a standard H-bridge in a hard-switching topology to generate the transformer driving signal introduces low-voltage AC pulses directly to the primary winding of the medium-frequency transformer. This can lead to significant disturbances during the transient periods of the waveform, primarily due to abrupt changes in current, high di/dt. The resulting output signal from the transformer often exhibits amplitude fluctuations that follow a saw-tooth pattern, which can lead to instability in the high-voltage arbitrary waveform generator when a load is applied.

To mitigate these issues, the transformer driving circuit should incorporate a Zero-Voltage Switching driver that operates in a soft-switching topology, producing a quasi-sinusoidal waveform. By minimizing the di/dt during transitions, this approach reduces the electromagnetic interference and voltage spikes, leading to a more stable and efficient system. Additionally, soft-switching reduces switching losses and thermal stress on the components, enhancing the overall reliability of the system.

A

Appendix I

Appendix I provides a comprehensive explanation of the HV H-bridge PCB design process. This section outlines the design principles and guidelines applied in developing the HV H-bridge, which also incorporates high-voltage full-bridge rectifiers.

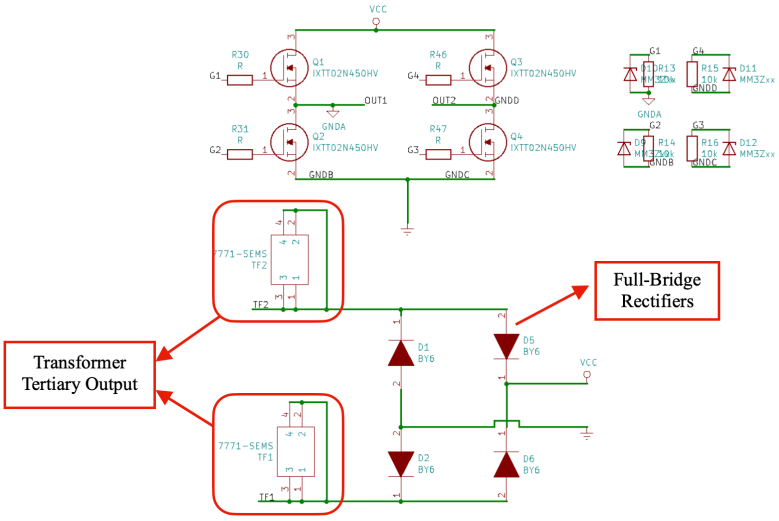


Figure A.1: Schematic of the HV H-bridge as well as the HV full-bridge rectifiers

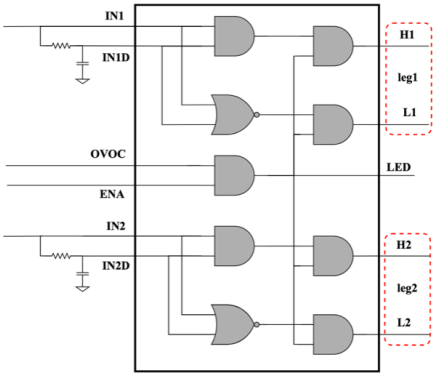
Figure. A.1 depicts the schematic of the HV H-bridge alongside the HV full-bridge rectifiers, designed in KiCad. The high-frequency output from the transformer undergoes rectification before being supplied to the input of the HV H-bridge. The Si MOSFETs of type IXTH02N450HV are chosen, possessing a blocking voltage of up to 4.5 kV with a current limit of 0.2 A. (In the schematic, Q_1 and Q_2 belong to leg1. Q_3 and Q_4 are for leg2.) Additionally, gate-protecting zener diodes and gate discharge

A

resistors are also implemented. It is worth mentioning that the gate resistance R_g and load capacitance C_{load} should be carefully defined. According to [118], the selected Si MOSFETs have low rise time (several 10s of ns), resulting a large dV_{DS}/dt. If C_{load} is large, during the transient period, a huge current spike will be induced and break the MOSFETs. Thus, the value of R_g should be larger and that of C_{load} should be carefully chosen to keep the current within limits.

A.1. Input Controller & Dead-Time Generation

In Figure. A.3, the programmable logic device (PLD) and the optocouplers of type OPI1268S are illustrated. The dead time t_d of the input signal IN1 and IN2 is regulated using a maximum 1 kΩ two-gang potentiometer and two 470 pF capacitors, allowing for a t_d adjustment within the range of 0-1 µs. The PLD is programmed from the logic circuit depicted in Fig. A.2, with input signal IN1 controlling HV H-bridge leg1 and IN2 governing leg2. (Due to the control logic, besides setting t_d, it is critical for the output of the upper switch H_i and that of the lower switch L_i to be complementary.) The potentiometer facilitates the availability of two resistors with identical resistance, ensuring that the dead time of both HV H-bridge legs can be synchronized.



IN_1	IN_2	ENA	OVOC	Output
1	0	1	1	$+V_{DC}$
0	1	1	1	$-V_{DC}$
1	1	1	1	0 (high)
0	0	1	1	0 (low)

Figure A.2: Programmed logic circuit to control the HV H-bridge with corresponding truth table

A.2. Design of the HV H-Bridge Gate Driving Circuit

Within the HV H-bridge module, only lower-side MOSFETs (L_i) feature grounded source terminals. Conversely, to turn-on the upper-side MOSFETs (H_i), the required gate voltages ought to be referred to their source voltages, instead of ground. Consequently, the gate drivers need to be isolated. Otherwise, they need to generate the threshold voltages above the upper MOSFET source voltages, which can be several kilo-volts. As shown in Fig. A.4, to achieve sufficient isolation, isolated DC/DC converters and optocouplers can be employed. The optocoupler and DC/DC converter are capable of offering the isolation up to 20 kV and are employed to

separate the LV side from HV side. As decipted in Fig. A.3, the optocoupler's low side input is toggled because the PLD can draw more current than it can source. A current-limiting resistor of 150 Ω is included to restrict the optocoupler primary current. Its output is elevated by a 560 Ω resistor. The optocoupler output signal will be directed to the non-isolated gate driver.

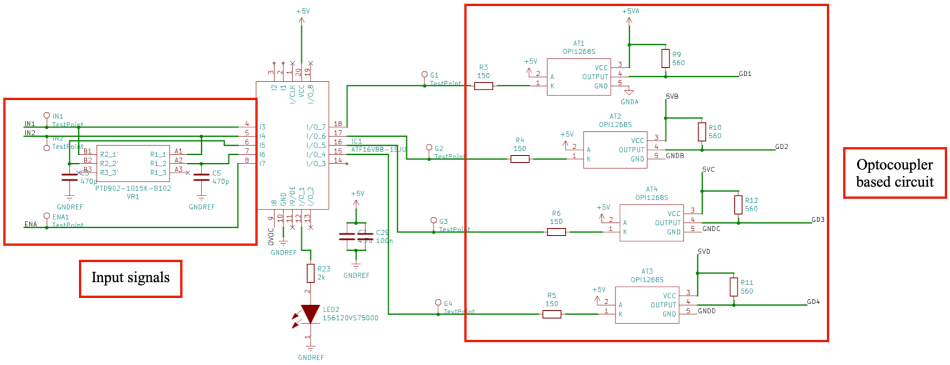


Figure A.3: Schematic of the PLD system and optocouplers (from input signals to MOSFET gate pulses)

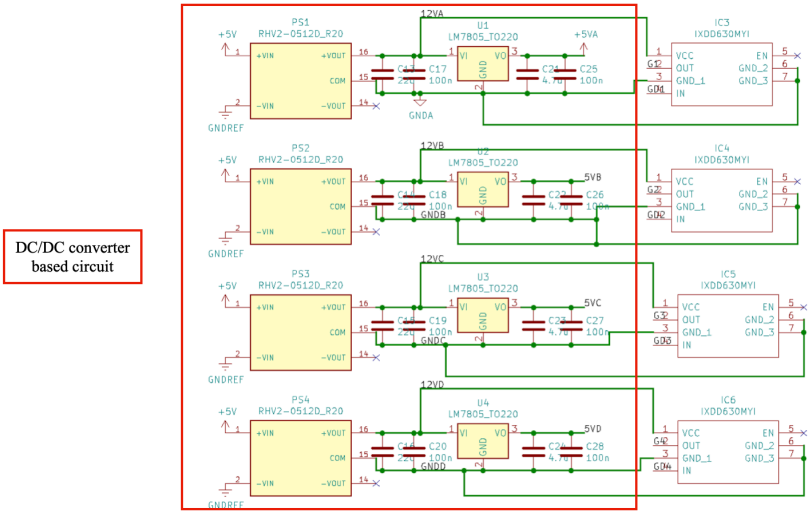


Figure A.4: Schematic of the non-isolated gate drivers powered by DC/DC converters

A.3. Voltage and Current Measurement Circuit

Voltage measurement sensor of type DVC 1000-P is chosen owing to its wider input range and fast measuring speed, which can measure the voltage ranging ±1.5 kV ($U_{sen(max)}$). Actually, the HV H-bridge module is supposed to work up to 4.5 kV

(VCC). Therefore, a voltage divider is introduced to measure VCC (H-bridge input voltage). DVC 1000-P has an internal resistance R_{in} of 12.6 $M\Omega$. A series resistor R_{24} with the value of 40 $M\Omega$ is connected and thus, it is able to measure the voltage from 0 to 6.2 kV, calculated based on (A.1). However, adding a series resistor R_{24} has the impact on the speed of sensor, since the input capacitance of the sensor is charged through the high resistance.

$$\frac{U_{max}}{R_{in} + R_{24}} = \frac{U_{sen(max)}}{R_{in}}; U_{max} \approx 6.2\,kV \tag{A.1}$$

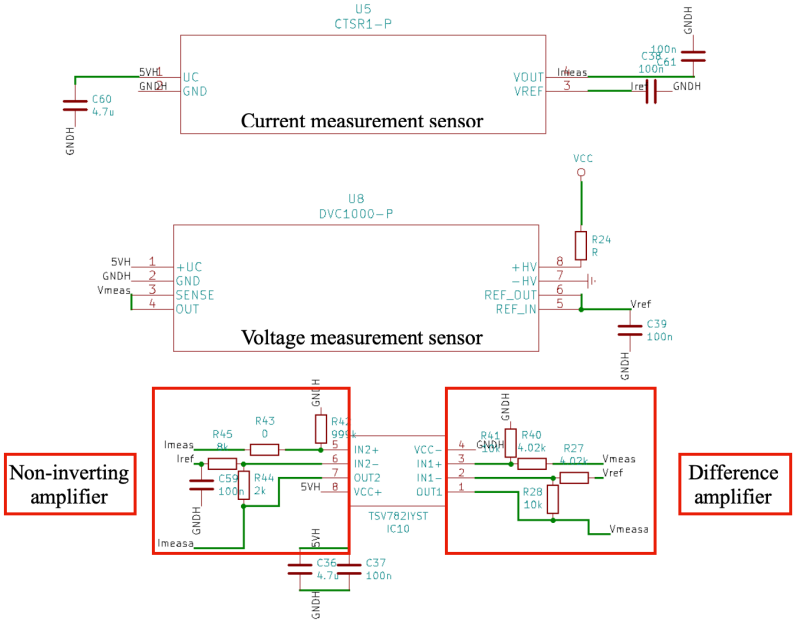


Figure A.5: Schematic of the voltage (current) measurement sensor with difference (non-inverting) amplifier

From [119], if the input of DVC 1000-P ranges ±1.5 kV. Its output voltage V_{meas} ranges from 0.5 to 4.5 V. For the voltage measurement sensor, only positive voltages can be measured (0-1.5 kV). Thus, the V_{meas} range will be shortened as 2.5-4.5 V. Notably, DVC 1000-P has an internal reference voltage of 2.5 V. By means of the difference amplifier of type TSV7821YST, shown in Fig. A.5, the reference voltage value is subtracted from V_{meas} and the obtained voltage should be multiplied by 2.5 times. As a result, the optimized output measurement voltage V_{measa} ranges from 0 to 5 V referring the input voltage VCC from 0 to 6.2 kV.

$$V_{measa(min)} = (V_{meas(min)} - 2.5) * 2.5 = 0\,V; \tag{A.2}$$

$$V_{measa(max)} = (V_{meas(max)} - 2.5) * 2.5 = 5\,V \tag{A.3}$$

Since Si MOSFET of type IXTT02N450HV has the maximum current rating of 0.2 A at 25°C, the HV H-bridge module also has a maximum current range of ±0.2 A (both directions). The selected current measurement sensor of type CTSR1-P has the theoretical sensitivity of 1.2 V/A. Similarly, CTSR1-P has a reference voltage of 2.5 V (I_{ref}). As a result, the output voltage of the current sensor I_{meas} varies from 2.26 to 2.74 V. By means of the non-inverting amplifier (1.25x), the I_{measa} varies from 2.2 to 2.8 V.

$$I_{measa(min)} = I_{ref} + I_{meas(min)} * 1.25 = 2.2\,V; \tag{A.4}$$

$$I_{measa(max)} = I_{ref} + I_{meas(max)} * 1.25 = 2.8\,V \tag{A.5}$$

A.4. HV H-Bridge Fault Detection

Seen from Fig. A.6, the fault detection circuit is formed by a single (voltage) comparator, a dual (current) comparator and a NAND gate. There is only an upper limit for the voltage, and an upper and a lower limit for the current which flows in both directions. The voltage limit is set as 4.5 kV, resulting in around 3.63 V for V_{measa} and the current limit is ±0.2 A, resulting in 2.2 to 2.8 V for I_{measa}. To fully avoid the HV H-bridge breakdown, a 0.3 kV margin voltage of the MOSFETs is considered, the maximum measured voltage should be 4.2 kV, resulting a V_{measa} of 3.4 V. Moreover, if the current limitation is modified as ±0.16 A, I_{measa} varies from 2.26 to 2.74 V. If the measured voltage V_{measa} or current I_{measa} exceeds these pre-set values, the output of the present comparators will be pulled low. As a result, the output of NAND gate will be pulled high but the optocoupler output will be pulled low.

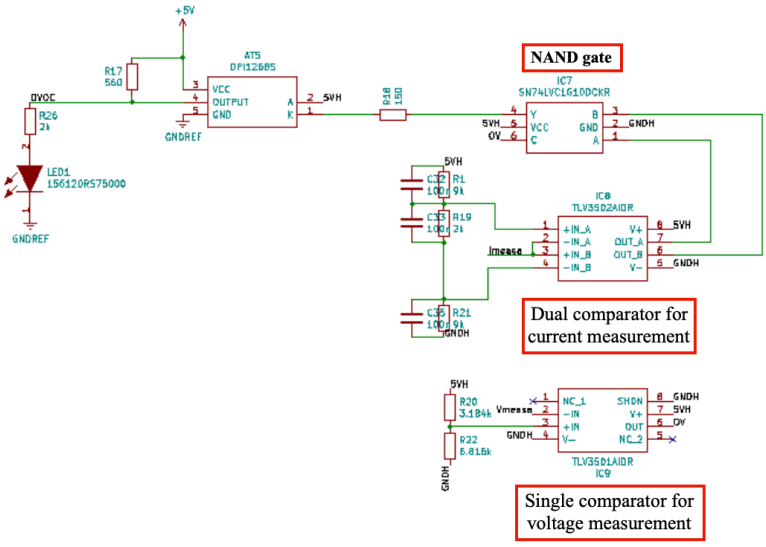


Figure A.6: Schematic of the fault detection circuit with LED indication

Epilogue

Not work harder, work smarter and manage expectations.

– Peter Vaessen

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A

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Curriculum Vitæ

Weichuan Zhao was born at 10^{th} of July, 1995, in Changchun, Jilin, China. He received his B.sc degree in Electrical Engineering and its Automation in Sichuan University (SCU) in 2018. Also, in 2020, he received his M.sc degree with cum laude from Delft University of Technology in the expertise of High-Voltage Technology. In 2020, he joined in the High Voltage Technology Group from the Electrical Sustainable Department at Delft University of Technology as a PhD candidate. His research topic is "Design of a Modular Cascaded H-Bridge Based High-Voltage Arbitrary Waveform Generator". Currently, Weichuan Zhao is a High-Voltage Engineer in Optics11.

List of Publications

Journal Publications:

1. **W. Zhao**, S. Ghafoor, G. W. Lagerweij, G. Rietveld, P. Vaessen, M. G. Niasar, *Comprehensive Investigation of Promising Techniques to Enhance the Voltage Sharing among SiC MOSFET Strings, Supported by Experimental and Simulation Validations*, Electronics **13**, 1481 (2024).

2. **W. Zhao**, G. W. Lagerweij, M. G. Niasar, *Design of a High-Voltage High-Frequency Insulation Test System using a Ferrite-Based Resonant Transformer*, IET High Voltage, accepted.

3. **W. Zhao**, G. W. Lagerweij, B. P. M. Hurkmans, M. G. Niasar, *Design of a High-Voltage Arbitrary Waveform Generator using a Modular Cascaded H-Bridge Topology*, Electronics **13**, 4390 (2024).

4. Z. Wang, X. Wei, M. G. Niasar, **W. Zhao**, T. Luo, P. Vaessen, H. Sørensen, C. L. Bak, *Partial Discharge Behavior of High Frequency Transformer Insulation under High-Voltage PWM Stress*, IEEE Transactions on Power Electronics, accepted.

Conference Publications:

1. **W. Zhao**, P. Vaessen, G. Rietveld, M. G. Niasar, *Voltage sharing improvement methods in series-connected MOSFETs for future grid high voltage applications*, 23rd International Symposium on High Voltage Engineering, pp. 85-91, (2023).

2. **W. Zhao**, T. Luo, M. G. Niasar, *Ramp sinusoidal breakdown of epoxy resin under high voltage waveforms at different frequencies*, 22nd International Symposium on High Voltage Engineering, pp. 2083-2088, (2021).

3. **W. Zhao**, M. G. Niasar, *Aging of oil-impregnated paper at different frequencies*, 2021 IEEE International Conference on the Properties and Applications of Dielectric Materials, pp. 430-433, (2021).

4. T. Luo, **W. Zhao**, M. G. Niasar, *Experimental study of epoxy surface discharge under different frequencies*, 2021 IEEE Conference on Electrical Insulation and Dielectric Phenomena, pp. 574-577, (2021).

5. **W. Zhao**, M. G. Niasar, *Aging Characteristics of FR-4 at Different Frequencies*, 2025 IEEE Conference on Electrical Insulation and Dielectric Phenomena, submitted.

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