Department of Precision and Microsystems Engineering

Modelling of the Initial Deformation of TriPleX Based Bimorph Actuators Used in Alignment of Optical Waveguides

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Abstract

This thesis presents an investigation of the initial deformation of micro-machined bimorph beams used in the alignment of flexible optical waveguides, due to residual stresses present in the material layers after processing. A material stack called TriPleX, a platform for planar lightwave circuits, forms the basis of the bimorph beam; a layer of polysilicon is deposited on top to create a bilayer. By varying the length of the polysilicon layer the initial deformation of the bimorph can be tuned to achieve a desired vertical deflection of the endpoint of the beam at room temperature. This initial deflection serves a 'starting point' from which the bimorph actuator fine tunes the position of the waveguide endpoint to achieve alignment to another waveguide.

A finite element model is constructed using COMSOL Multiphysics Modeling Software to simulate the behavior of the bimorph beam as it cools down from processing temperature to room temperature. Modelling the bilayer bending during cooling down is achieved using physics modules within the finite element package based on the difference in coefficient of thermal expansion (CTE) of the two layers, but this is only part of the residual stress found in the structure at room temperature. Another part is the so-called intrinsic stress: stress introduced in the material during deposition caused by imperfections in structure and lattice spacing mismatch at the interface between layers of different materials, among other causes. To account for this intrinsic stress in the finite element model, monolayer beams with lengths of 500 µm, 750 µm and 1000 µm, thicknesses of 3 µm and 5 µm, and widths ranging from 10 to 54 µm are fabricated and their initial deformation is studied to obtain a stress distribution referred to as the 'equivalent stress' distribution. This simplified distribution is meant just to reproduce the measured deformation, but does not represent the actual intrinsic stress distribution within the material. The equivalent stress is used to extend the finite element model to account for the effect the intrinsic stress has on the initial deformation of the bimorph beam.

The method of incorporating the equivalent stress into the finite element model produces simulation results that accurately match the deformations found in the fabricated monolayer beams, comparing different aspects such as the radius of curvature and the initial slope of the cantilever at its anchor point to the substrate. The complexity of the geometry of the anchor point of the cantilever, caused by underetching of supporting layers, is found to play an important role in the overall deflection of the cantilever. Refining the modelled geometry in this area reduces the average initial slope of a polysilicon cantilever with a length of

500 µm, a thickness of 3 µm and a width of 38 µm from roughly 0.91 mm/m to 0.15 mm/m, the measured slope being 0.12 mm/m. For cantilevers of different dimensions similar improvements in simulation accuracy are observed.

Verification of simulation results using structures that employ multiple bimorph beams to actuate an array of flexible waveguides show that the measured deformation in these structures can also be approximated using the extended finite element model and that introduction of the equivalent stress improves simulation results. However, for one bimorph beam 1000 µm in length the difference in the vertical deflection of the endpoint between simulated results and the measured profile is 3.56 µm. The same comparison for a bimorph beam 525 µm in length yielded a difference of 1.45 µm. Since the desired vertical endpoint deflection is only 8 µm, the simulation results provide a first approximation of the realzied deformation.

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Chapter 1

Introduction

The research presented in this paper was performed as part of the Flex-O-Guides project, under the umbrella of the PHASTFlex initiative. The Flex-O-Guides project aims to develop a concept for the alignment of multichannel photonic integrated circuits (PICs) using flexible waveguide beams integrated in the PICs that are positionable by integrated actuators. This research focuses specifically on the vertical component of the integrated actuating function. This chapter will discuss the background of this research by introducing the field of photonics, discussing the need for accurate optical alignment in packaging and presenting the proposed concept to achieve this alignment, as well as formulate the set of problems that underly the present research along with the concrete design goals.

1.1 Context

1.1.1 Photonic Systems

The term photonics in its broadest sense is used to denote the technical application of light. Photonic systems are systems that fulfill one or more optical functions, for instance the emission, amplification or detection of light, using optical components such as lasers, optical amplifiers or photodetectors. The most important field of application for photonic systems is the field of telecommunications, exploiting the advantages of using light as a carrier of information as opposed to electricity; light has the beneficial properties of having a very broad bandwidth, low transmission losses, no heat dissipation and not being susceptible to electro-magnetic interference [1]. The parallel between photonic and electrical systems is an important characteristic that distinguishes photonics from conventional optics; the field of photonics has benefited from the advances in

semiconductor fabrication technology, which has lead to photonic functions being miniaturized and combined to form so-called photonic integrated circuits (PICs), analogous to the way electrical functions are combined in electrical integrated circuits (ICs). Developments in photonics have lagged behind those in electrical IC fabrication, due to the complexity of controlling light within a circuit compared to the relative ease of controlling electrical currents. Nevertheless, ever-increasing requirements in performance of telecommunication technology, as well as the emerging of fields such as optical computing [2] and novel use in medical sensing [3], have recently spurred interest in its application.

Most commonly PICs are fabricated on an indium phosphide (InP) substrate due to its optical qualities, but recently breakthroughs in research are clearing the way for silicon [4] or silicon dioxide based circuits. Optical connections within a PIC are formed by so-called waveguides, which transmit light from one component to another, performing a function equivalent to electrical interconnects in regular electrical ICs. To allow communication between the PIC and outside systems these waveguides have to be coupled to optical fibres at the boundary of the PIC; a non-trivial task presently responsible for a large share in the overall production cost.

1.1.2 Optical Packaging

Optical packaging describes the process of incorporating photonic systems into a platform that can be easily handled and allows it to be used in conjunction with other optical or electrical systems, as well as provides power and means of heat dissipation to the system [5]. With electrical ICs this package takes the form of a chip carrier, which main function is to connect the terminals of the IC to larger leads suitable for conventional soldering. In much the same way, a PIC needs to be provided with a means to transmit its optical signals to larger conventional optical fibres, which are used in communication between different optical systems. The coupling between the PIC waveguides and optical fibres raises two issues.

Firstly, the mismatch in dimensions between the PIC waveguides and the optical fibres introduces severe optical losses. PICs are manufactured by means of semiconductor fabrication technology, in a similar process used to fabricate electrical ICs, resulting in a monolithic structure with highly miniaturized features. The waveguides within the PIC have sub-micrometer cross-sectional dimensions, while the average optical fibre has a diameter of 125 μm. The diameter of the beam of light, the so-called spot-size, traveling through the PIC waveguide

is therefore significantly smaller, than the spot-size of the optical fibre. Moreover, the pitch between waveguides on a PIC is insufficient to accommodate the optical. To overcome the difference in dimensions between the waveguides on the PIC and the optical fibres, a so-called interposer chip is introduced between the and the optical fibres. This interposer chip serves two functions: firstly it acts as a spot-size converter, matching the spot-size of the PIC waveguide on one end, and gradually increasing the diameter to match the spot-size of the optical fibre on the other end. Secondly, it increases the pitch between the waveguides, matching the pitch of the PIC waveguides on one end, and gradually increasing the pitch to the desired amount on the side of the optical fibres.

Secondly, the alignment between waveguides is highly critical in ensuring efficient optical coupling [5], often requiring sub-micrometer accuracy.

Methods of aligning waveguides or optical fibres largely fall into two categories: active and passive alignment.
When actively aligning waveguides, a beam of light is sent through one of the waveguides, which is fixed, while measuring the intensity of light that is transmitted to the other waveguide, which is manipulated. When the measured intensity reaches an optimum, both waveguides are fixed permanently, resulting in the most efficient coupling. This form of alignment is often performed using (robotic) manipulation where micro-grippers are used to position the fibres or waveguides; a time-consuming process that is highly serial in nature, making it expensive and unsuitable for use in high-throughput industrialized processes.
Passive alignment does not involve monitoring the coupling efficiency, but solely relies on prefabricated alignment markers or structures to position two waveguides. Components are either positioned manually using a microscope to visually align the waveguides, or structures are fabricated that physically guide the components to a predetermined position. Passive alignment is less time consuming, but generally yields less precise results compared to active alignment. An example of passive alignment is a process reported by Van Gurp et al. [6] in which a PIC and an interposer chip are mounted on a shared optical bench, using alignment features to serve as mechanical end-stops allowing precise alignment of waveguides on both chips.

As a result of the complexity of the alignment process in optical packaging, it is usually accountable for the largest portion of production costs. Reducing the cost of alignment therefore has the potential to significantly lower the overall cost of production of PICs [7]. Factors that determine packaging costs include the time per individual packaging operation, and the through-put of the pack-

aging process. Therefore reducing packaging time and increasing the number of simultaneous operations will reduce the overall packaging costs.

The Flex-O-Guides project aims to do so by removing the need for external micro-manipulators in active alignment. This is achieved by actuating arrays of flexible waveguide beams from the PIC itself using actuators integrated into the PIC. These actuators should be capable of manipulating the position of the endpoint of the waveguide to align to a waveguide of another PIC. In this case specifically, the waveguides of an interposer chip need to be coupled to waveguides on an InP PIC. The interposer chip acts as a spot-size converter to allow connection of the InP PIC waveguides to optical fibres. The interposer chip and the InP PIC are mounted on a shared substrate and aligned using complementary alignment features on both of the chips and the substrate. As a result of the fabrication of these alignment features the chips are mounted onto the substrate upside down (so-called Flip-Chip). The flip-chip step ensures an initial alignment of the waveguides of the interposer chip and the InP PIC, which can subsequently be refined through use of the integrated actuators on the interposer chip. An array of four interposer waveguide beams connected rigidly through a crossbar at the end of the beams will be manipulated simultaneously. Using thermal actuation the horizontal and vertical deflection of the endpoint of the waveguides can be adjusted to align them with the ends of the waveguides of the InP PIC, which are fixed. This research focuses on a concept of realizing vertical actuation.

1.1.3 Bimorph Waveguide Beam

Vertical actuation of the waveguide endpoint will be realized by fabricating the waveguide as a part of a bimorph actuator. A bimorph actuator consists of a stack of two layers of different materials bonded together which, due to the difference in their coefficient of thermal expansion (CTE), will curve when heated. Another possibility is creating a bimorph actuator parallel to the waveguide beam. By mechanically connecting the bimorph actuator to the waveguide beam, the bimorph can create a deflection in the waveguide beam. For the sake simplicity, only the first concept will be investigated. However, the theory can easily be extended to cover the second concept.
The waveguide beam itself consists of a 130 nm thick silicon nitride core surrounded by 8 µm silicon oxide cladding (a structure called TriPleX), the bottom half of which is thermally grown and the top half deposited using plasma enhanced chemical vapour deposition (PECVD). To create a bimorph, a layer of another material needs to be added with a CTE different from that of silicon dioxide.

In this case the material of choice is polysilicon, which will be deposited on top of the TriPleX stack. The polysilicon can be heated to induce a bending moment that will create a curvature in the waveguide beam. The complete waveguide beam is released from the substrate by underetching the silicon to form freely suspended beams, 1000 µm in length. The underetching happens in two stages; first the silicon is etched anisotropically using Deep Reactive Ion Etching (DRIE), effectively using the waveguide beam itself as a mask, after which the exposed silicon walls are coated in a passivation layer to protect them from the second isotropic etch step which releases the waveguide beam from the substrate by underetching the silicon at greater depth (see Figure 1.1). The goal of this two-stage etch process is to leave a layer of silicon attached to the bottom of the waveguide beam during the release to provide extra support. Without this support, many waveguide beams were observed to have fractured during the underetching process [8]. Whether or not this layer of silicon is removed after the beam is released, is determined by the duration of the second (isotropic) etch; if desirable the layer can be kept permanently to increase the rigidity of the waveguide beam.
A number of dimensions of the bimorph waveguide beam are fixed due to demands placed on the design by other facets of the Flex-O-Guides project. The optical workings of the spot-size converting interposer chip, for instance, dictate the dimensions of the core and the thickness of the cladding of the waveguide, thereby defining the cross-sectional dimensions. Since the waveguide also needs to be actuated in the horizontal direction, its in-plane stiffness cannot be too high. For this reason the intended length of the waveguide beam lies between 500 µm and 1000 µm. Dimensions that aren't fixed beforehand are mainly found in the dimensions of the layer of polysilicon deposited on top of the waveguide and the layer of silicon that can be left underneath the waveguide. The dimensions of the layer of polysilicon on top can be precisely controlled; its length and width through the mask design, its thickness through deposition time, while the dimensions of the layer of silicon underneath are limited by the sequence of isotropic and anisotropic etch steps (see figure 1.2).

1.2 Problem Statement

In designing the bimorph waveguide beam, certain limitations have to be understood and respected. These limitations are posed by the fabrication methods used to create the beams, as well as the performance that is demanded by other aspects of the design within the Flex-O-Guides project.

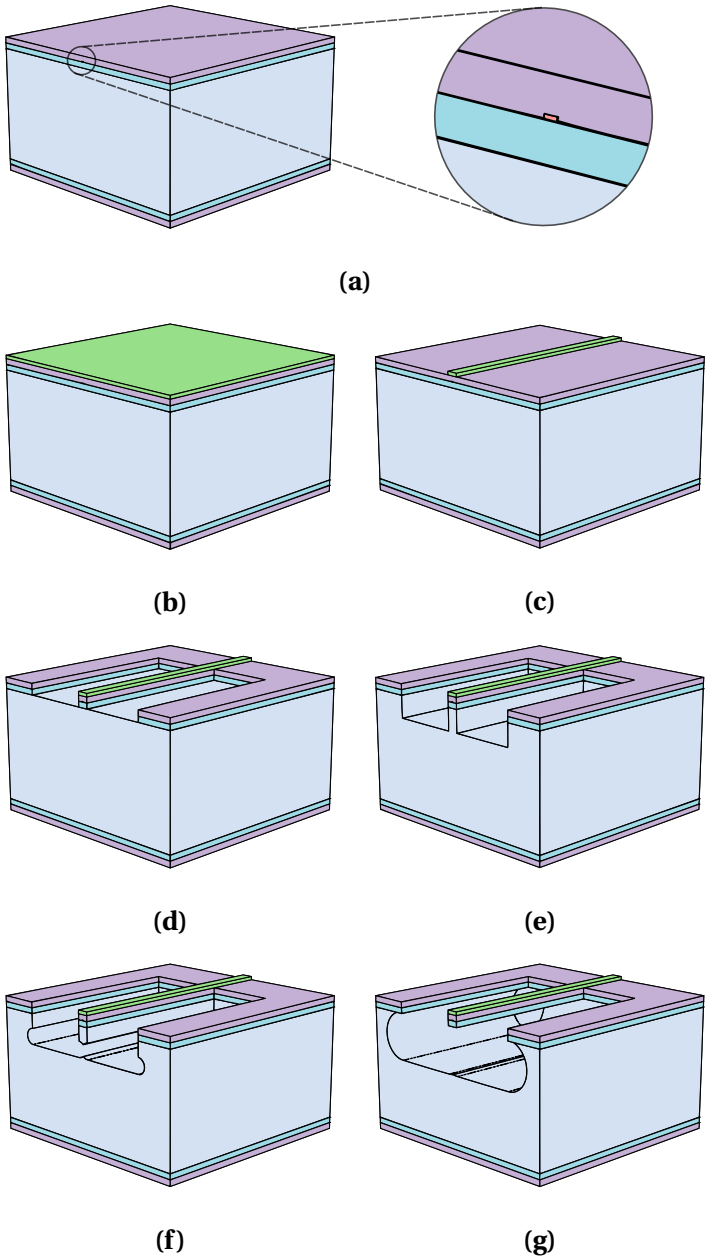


Figure 1.1: Fabrication of single bimorph waveguide beam: (a) Wafer with TriPleX stack already present (note the Si_3N_4 waveguide core), (b) deposition polysilicon (epitaxially grown from LPCVD seedlayer), (c) etch of polysilicon, (d) plasma etch of SiO_2, (e) DRIE of silicon, (f) isotropic etch of silicon to release waveguide beam, (g) isotropic etch of silicon to remove bottom layer of silicon underneath the bimorph waveguide beam

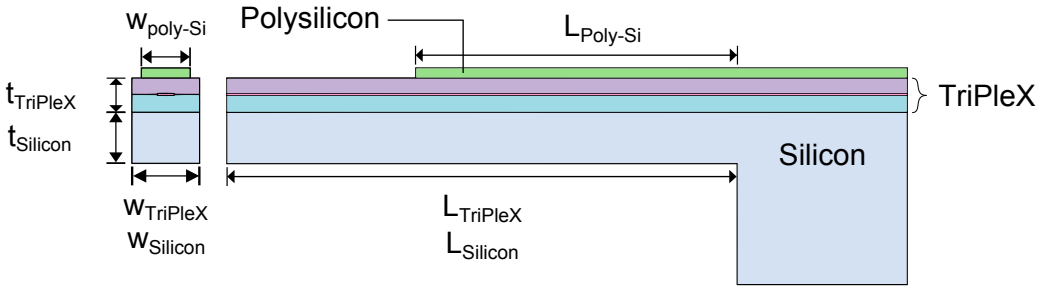


Figure 1.2: Schematic cross-section of the bimorph waveguide beam design showing the dimensions of different layers

1.2.1 Residual Stress

In previous research [8], freely suspended TriPleX waveguide beams were observed to have deformed from their desired straight geometry after fabrication; the waveguide beams had developed a curvature away from the substrate. This deformation indicates the presence of a stress gradient throughout the thickness of the waveguide beam. This stress-gradient is introduced into the material during fabrication and is called residual stress. The origins of residual stress in a thin layer can be varied and are often comprised of the effect of multiple phenomena, often dependent on factors such as material properties, fabrication parameters, layer thicknesses and doping levels. As a layered structure becomes more complex and more layers are introduced, the added effect of the residual stresses found in each layer results in a complex stress profile throughout the thickness of the structure.

Two types of stress can be defined within thin films; thermal and intrinsic stress [9]. Thermal stress is found in any system consisting of a rigid bond of two materials with different thermal expansion coefficients that undergoes heating or cooling. In this case a system of silicon oxide bonded to a silicon substrate is cooled down from the process temperature at which the oxide deposition takes place to room temperature.

Any stress that cannot be attributed to the thermal expansion mismatch between substrate and thin film can be grouped under so-called intrinsic stress [10, 11]. These stresses manifest themselves before cooling down, therefore thermal expansion (or in this case contraction) cannot be the cause of these stresses. Intrinsic stress is a product of the particular mechanism of deposition and the molecular structure of the resulting thin layer, as well as crystallographic or structural flaws introduced during deposition [9]. The added effect of thermal- and

intrinsic stress make up the total stress profile found within the film.

In the case of the bimorph waveguide beam, the introduced curvature causes the position of the endpoint of the waveguide beam to be displaced by an unknown amount. Since this system is supposed to realize alignment of this endpoint with sub-micrometer accuracy, it is necessary to know beforehand the stresses that will develop in the structure and the resulting deformations.

1.2.2 Offset Waveguides in Flip-Chip Configuration

Alignment between the interposer waveguides and the InP PIC waveguides happens in two stages. The first stage involves mounting the interposer chip as well as the InP PIC onto a shared substrate, while the second stage covers the active alignment using the integrated actuators of the interposer waveguides. The first stage offers pre-alignment of the interposer chip and the InP PIC by passively aligning the two chips using complementary alignment features present on the surface of the optical bench and on the surface of both chips. These alignment features are fabricated in the same fabrication steps that produce the waveguides themselves, so that the relative position of the waveguides to the alignment features can be accurately controlled. Since the features are fabricated on the top side of the chips, they need to be mounted onto the optical bench upside down to access the complementary features on the top of the optical bench, an approach called the flip-chip method (see Figure 1.3). Once the chips are bonded to the optical bench, the micro-actuators integrated into the interposer waveguide beams allow for fine-tuning of the alignment (see Figure 1.4).

The flip-chip method is not only used to achieve in-plane alignment, but also offers out-of-plane alignment. This out-of-plane alignment is based on the fact that the thickness of each deposited layers that make up a chip is accurately known. Therefore, the vertical position of a waveguide on a chip is accurately known with respect to the top surface. By mounting both the interposer and the InP PIC upside-down, aligning the top surface of both chips, the relative vertical distance between the waveguides on both chips is accurately known. This principle is used to realize an initial vertical alignment between the interposer waveguide and the PIC waveguide. Due to the difference in the way the interposer waveguides and the InP PIC waveguides are fabricated, the centerline of both waveguides are offset by 8 µm with respect to their top surface (see figure 1.5). The bimorph waveguide beam should be designed to ensure this distance is within its actuation range.

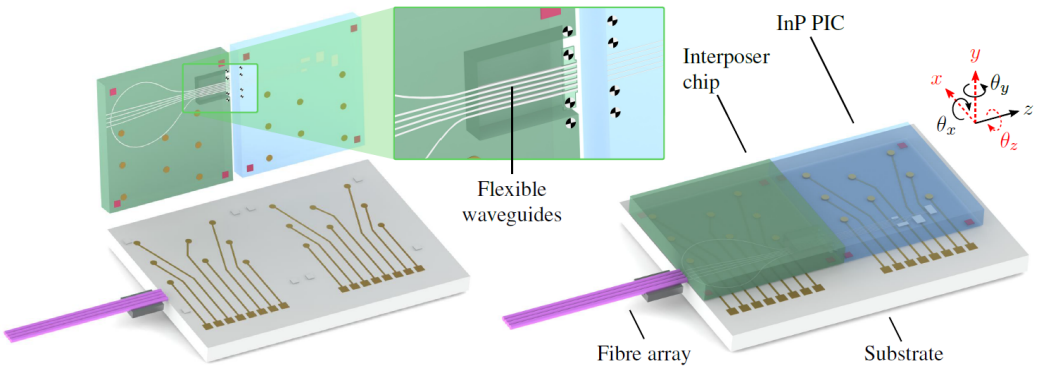


Figure 1.3: Representation of the pre-alignment step of the Flip-Chip method, showing the interposer chip and the InP PIC being mounted up-side-down on a shared substrate, guided by alignment features on each of the four corners of each chip, in order to provide pre-alignment of the flexible waveguide beams of the interposer to the waveguides of the InP PIC [8].

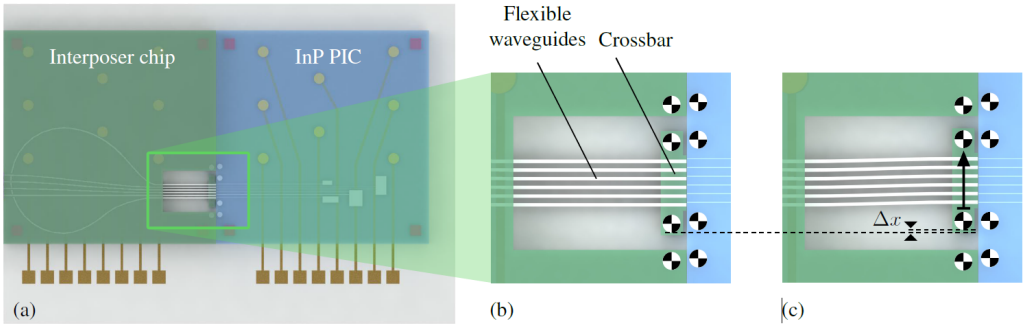


Figure 1.4: Representation of the fine alignment step of the Flip-Chip method, showing the array of flexible waveguide beams on the interposer chip being translated by a distance $\triangle x$ to finely align them to the waveguides of the InP PIC [8].

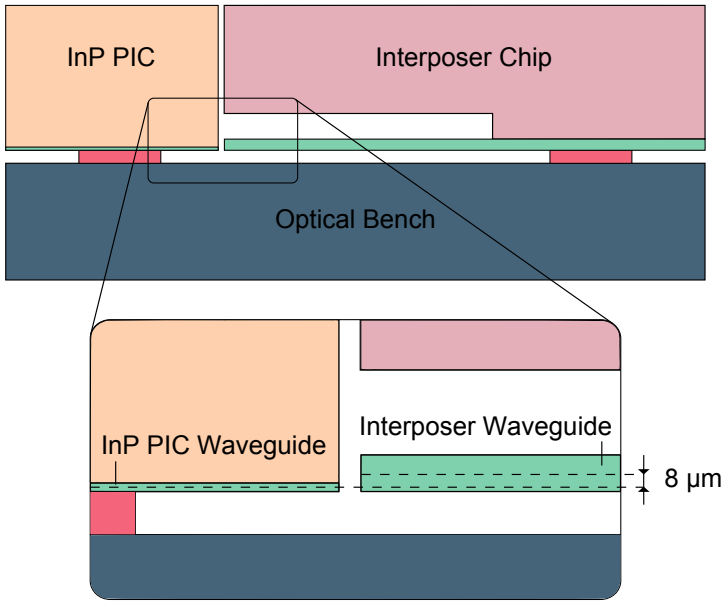


Figure 1.5: Vertical offset between InP PIC waveguide and interposer waveguide caused by flip-chip mounting of both chips on a shard optical bench

1.3 Thesis Goal

The goal of this research project is to construct a model that is able to predict the behavior of a bimorph waveguide beam, and use this model to propose a viable design capable of vertical alignment to an InP PIC waveguide. The model must include information on residual stresses present in the different layers that make up the bimorph waveguide beam, as well as predict the general bimorph behavior. Present knowledge of the origin of residual stresses needs to be assessed to determine the extent to which these stresses can be predicted analytically, or otherwise determined empirically. The proposed design resulting from the model has to perform as an integral part of the overarching Flex-O-Guides project and therefore has to respect the conditions and parameters set by other functions of the alignment concept and not conflict with their operation.

1.4 Report Structure

The main body of this report is structured as follows:
In the second chapter the present knowledge of causes of residual stresses and subsequent deformation or failure in micro-fabricated beams is reviewed, as well

as current attempts at modelling and predicting these phenomena. An assessment is made as to which approach would be applicable to the specific case of arrays of flexible TriPleX waveguide beams.
The third chapter documents the method used to gather relevant data and combine this data into a model.
In the fourth chapter the obtained results are presented and discussed.
Chapter 5 discusses the conclusions that can be drawn from the obtained results and provides recommendations on future work that could build on the present thesis research.

Chapter 2

Literature Review

This chapter presents a broad overview of the current knowledge on the origin, magnitude and consequences of residual stresses found in deposited layers as reported in literature, as well as efforts made to measure and simulate these stresses, with specific interest in silicon dioxide layers and beam structures. It is concluded by a summary of methods and approaches that will be used in this specific research.

Section 2.1 covers the causes of residual stress, specifically in thermally grown silicon dioxide, as well as in silicon dioxide deposited using chemical vapour deposition (CVD). Section 2.2 discusses the effects of residual stress in the form of deformations and possible failure in thin suspended features. Section 2.3 presents some attempts at measuring residual stresses, as well as modelling various aspects of these stresses and predicting subsequent deformations, as found in literature.

2.1 Causes of Stress

In this section the stress that remains in a thin film after deposition, the so-called residual stress, is investigated, focusing on silicon oxide. Firstly the basic structure of this residual stress is discussed, after which stresses found in thermally grown oxide and oxide formed using CVD are examined respectively. This section restricts itself to the analysis of thin films of infinite in-plane dimensions, the specific beam geometry will be discussed in the next section.

2.1.1 Residual Stress

The deformation and failure of (partially) released waveguide beams indicate the existence of stresses within the waveguide material. Upon release of the waveguide beam from the substrate these stresses are relieved and the structure deforms or in some cases fails. From the particular shape of the deformed beam (a slope at the base and constant curvature along the length of the beam) it is clear that the stress distribution within the material of the beam is complex, and it is insufficient to assume a simple average compressive or tensile stress.

2.1.2 Residual Stress Found in Thermally Grown Oxide

Thermally grown silicon dioxide films have been shown to generally be in a state of compression [10]. The cause for this compressive stress is the thermal expansion mismatch between the silicon substrate and the oxide layer on top. Since the thermal growth of silicon oxide occurs at relatively high temperatures (800-1200 °C), the difference in thermal expansion coefficient between the oxide and the silicon substrate causes stresses in both film and substrate when the system is cooled down to room temperature. The lower thermal expansion coefficient of the oxide (0.6×10^{-6}/°C) compared to the silicon (4.5×10^{-6}/°C) in the range of 0 to 1000 °C explains the compressive nature of the induced stress [12, 13].

In thermally grown oxide the intrinsic stress has its origin in the mechanism of oxidation and the atomic structure of the formed layer. The growth of thermal oxide depends on the diffusion of oxidizing species (O_2, H_2O, OH) through the oxide layer towards the interface, where the oxidizing reaction takes place [14]. Oxygen diffusing into the oxide layer, either in ionic or in molecular form, forms the main defect in the oxide structure and contributes to the compressive nature of the intrinsic stress [13]. Besides oxygen, hydrogen is an important contaminant in the oxide structure, introducing OH and Si-H bonds. Since OH has a higher thermal expansion coefficient than the oxide, hydrogen may actually help reduce thermal stress in the oxide when cooling down to room temperature; the effective thermal expansion coefficient will be closer to that of silicon [15]. For this reason overall stresses in thermal oxide grown in a wet environment are lower than those grown in a dry environment. The presence of SiH has been shown to decrease the strength of the oxide, since the Si-H bond is weaker than the Si-O bond [15].
Evidence of a reactive interfacial layer between silicon and oxide has been found by Stoneham et al. [16]. As oxygen diffuses from the ambient into the oxide, silicon diffuses from the substrate through this reactive layer and silicon oxide is

formed at the upper boundary of this layer. High stress concentrations in this layer serve to relieve the dynamic stress generated in thermal oxidation. The peak stresses in this interfacial layer can reach values of up to 0.47 GPa at the interface [11, 17].
Another source of intrinsic stress is found in the difference in molar volume between silicon and silicon oxide [11]. A volume increase of 126 % occurs when silicon is oxidized and this volume needs to be accommodated somehow. Elastic strain alone cannot account for this phenomenon; some structural rearrangement has to take place [18].
The last source of intrinsic stress is found in the structural mismatch between the silicon and the oxide at the interface. Mrstik et al. [18] suggested that silicon oxide grows in a relatively highly ordered state (coesite structure) near the interface, to satisfy the electrical bonds, leaving it in a state of strain. The mechanical properties of this ordered state of the oxide near the interface have been shown to differ from those of bulk non-crystalline silicon oxide. For instance, the Young's modulus was found to be more like that of silicon. The oxide loses its ordered structure as it moves away from the interface, being displaced by newly formed oxide below.

Stresses accumulating in the oxide layer as a result of the phenomena discussed above can be relieved through thermal annealing. Visco-elastic relaxation is the proposed mechanism behind this stress relieve [11]. Annealing can be done following the deposition process, as an intentional part of fabrication, but it also takes place during deposition, since these processes require relatively high temperatures. It follows that oxide at the outer surface (which is the 'oldest') of the growing layer has annealed for a longer period than newly formed oxide at the silicon/oxide interface, which implies stresses must decrease away from the interface. This concept is known as inhomogeneous thermal history [11]. This inhomogeneous thermal history causes intrinsic stress to form a gradient along the thickness coordinate. Since the visco-elastic relaxation during annealing is driven by temperature, it makes sense that a higher process temperature leads to a higher amount of stress relieve and therefore a larger gradient [11]. It was shown that annealing cannot completely relieve all intrinsic stress within the oxide. The part that remains can mainly be attributed to contaminants within the oxide structure, which cannot be removed through annealing. These contaminants consist mainly of oxygen, but depending on the process characteristics also hydrogen or dopants such as boron of phosphorus may be present.

2.1.3 Residual Stress Found in CVD Oxide

Silicon oxide deposited using low pressure chemical vapor deposition (CVD) methods has generally been found to develop tensile intrinsic stress [13], contrary to the compressive intrinsic stress in thermally grown oxide. This tensile stress can be lowered by doping with boron or phosphorus and annealing. Using low pressure chemical vapor deposition (LPCVD) and 2.5 % boron and phosphorus doping, the stress was even shown to change from an initial tensile state to compressive after a half hour anneal (see figure 2.1). It is important to note that the overall stress after deposition and cooling down will still generally be compressive due to the thermal mismatch induced compressive stress.
Bulla et al. [19] report compressive stress levels of $\sim 1.4 \times 10^2$ MPa in layers of oxide $\sim 4.2\,\mu$m thick deposited using plasma enhanced chemical vapour deposition (PECVD) 0.5 µm at a time. These thin layers were initially under tensile stress ($\sim -0.75 \times 10^2$ MPa), but after a rapid thermal annealing process this stress was observed to have changed to compressive ($\sim 0.9 \times 10^2$ MPa).
Tarraf et al. [20] describe intrinsic stress levels for layers of PECVD oxide deposited at low temperatures (60 °C as well as high temperatures (300 °C. At low temperatures they report a average compressive stress of ~ 150 MPa, while at low temperatures only ~ 17 MPa of compressive stress was measured.

2.2 Deformation and Failure

The combination of thermal and intrinsic stress discussed in the previous section causes some of the micro-fabricated beams to fail and others to deform. The typical deformation consists of a slope at the beam's anchor point to the substrate and a constant curvature along its length. Both effects will be examined separately.

2.2.1 Rotation at base

The slope at the anchor point of the waveguide beam is caused by the stresses present in the part of the beam that is still bonded to the substrate [21]. Most of the thermal stress in this part cannot be relieved, but the oxide still deforms close to a free edge. In this case it causes the oxide to bulge slightly over the edge at the base of the beam. This means the beam's clamped end is deformed in such a way that a downward initial slope is realized. Thermal stresses seem to generally dominate over intrinsic stresses [10], so the effect of intrinsic stress in deforming the base of the beam is not taken into account.

2.2.2 Curvature

In monolayer beams fabricated from a single material, the curvature along the length can be attributed to intrinsic stresses alone. Since thermal stress is uniform by nature [22], it is relieved completely upon release of the waveguide beam from the substrate, causing only an elongation of the beam. The intrinsic stresses form a gradient profile along the thickness of the beam and therefore induce a constant moment which causes the beam to curve [21].
In the specific case of TriPleX waveguide beams, the beams consist of PECVD oxide on top of thermal oxide with a silicon nitride core. It is therefore not possible to assume all thermal stress is relieved and only intrinsic stress remains to produce the curvature of the beam. The thermal expansion coefficient may differ between PECVD and thermal oxide, causing residual thermal stress. The nitride core of course also adds to the stress profile, though its dimensions are relatively small. It is therefore the combination of thermal and intrinsic stress in all three elements that determines the curvature.

2.2.3 Failure

During fabrication high stress concentrations can occur in the waveguide beams, causing some to fail. Longer beams were observed to fail more often [8].
One source of failure due to high stress concentrations is buckling. During underetching of the silicon to release the waveguide beams, the situation may occur where the center part of the beam is already released from the substrate while the endpoint is still connected. This causes the beam to behave like a doubly-clamped beam and the residual stresses may then cause it to buckle. The way the buckling occurs depends on the magnitude of the thermal- and intrinsic stresses as well as their ratio [23]. As mentioned before, thermal stresses cause a deformation of the boundaries of the beam resulting in an initial downward slope. If thermal stresses are dominant, buckling would be expected to be in a downward direction. Intrinsic stresses cause the beam to curve upward. Therefore, if intrinsic stresses are dominant, buckling would be expected in an upward direction [23]. Evidence of downward buckling in [8] suggests dominant thermal stresses.

2.3 Modelling

This section presents attempts at determining stresses in thin films and microfabricated structures through measurement or predictive modelling. First, the determination of material properties is discussed. Secondly, some common methods of measuring stresses are summerized. Thirdly, attempts at modelling these

stresses are discussed. Lastly, some comments are made on the effect of boundary conditions on the stress distribution in micro-fabricated structures.

2.3.1 Material properties

Any attempt at modelling stress and strain related phenomena relies on an accurate knowledge of material properties. Bulk values of, for instance, the Young's modulus or Poisson's ratio are readily available, but on micro scale these bulk values may not always be accurate. Furthermore, in thin films these material properties may not be isotropic throughout the thickness or towards free edges [18].

Early research into the Young's modulus of thin thermal oxide layers (2000–20 000 Å) was done by Jaccodine et al. [10]. In this research, stress-strain relations were obtained using two methods: firstly, a thin silicon substrate was oxidized and used as a beam, removing the thermal oxide from one face of the substrate and measuring the resulting deflection. Secondly, a silicon oxide film was created by etching away all silicon supporting it. The film was then fixed in a frame. By increasing the pressure on one side of the film, deflection of the surface could be measured. The setup for both methods is illustrated in figure 2.2. From the relation between pressure and deflection, the strength of the film could be determined. These methods yielded an average Young's modulus of 66 GPa. The fragility of the thin oxide films made measurements using these methods difficult.

Petersen et al. [24] provided a new method of determining the Young's modulus of various materials, based on vibrational analysis of thin beams (8.3 µm x 2 µm x 950 Å). Their values for thermal oxide grown in a dry environment (67 GPa) are in agreement with the value found by Jaccodine et al.[10]. Of interest is their value found for thermal oxide grown in a wet environment (57 GPa) which is significantly lower than that of dry oxide. The higher concentration of OH in the oxide is given as an explanation for the lower strength in wet oxide. This also affirms the theory stated by Mrstik et al. [18] that the weaker SiH bonds found in "wet oxide" are detrimental to the strength of the oxide.

Mrstik et al. [18] furthermore provide a Young's modulus value for bulk non-crystalline silicon oxide of 73 GPa, as well as a value of 161 GPa for the ordered silicon oxide near the surface, which they state is structurally similar to coesite.

2.3.2 Measuring stresses

The first substantial contribution to the analytical determination of stresses in thin films was made by Stoney in 1909 [25]. Stoney presents a formulation to de-

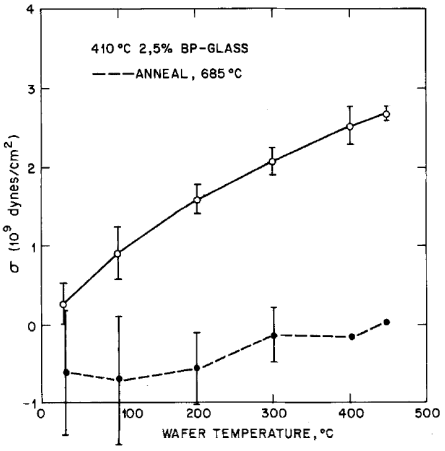


Figure 2.1: Plots of the measured stress as a function of temperature of a 410 °C, 2.5 % B,P-glass. The solid line shows data for the as-deposited film, while the ditted line is for data from this film after a 0.5h anneal at 685 °C [13].

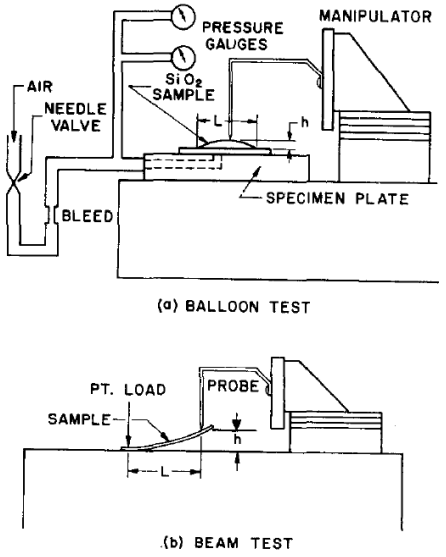


Figure 2.2: Schematic of test apparatus used to determine the strains in SiO_2 [10]. (a) shows the setup of the balloon method, while (b) illustrates the cantilever beam method.

termine the average stresses in a substrate coated with a thin film by measuring the radius of curvature of the deformed system. As an example he describes a flat steel bar onto which a nickel film is deposited. Nickel was used because its Young's modulus is almost equal to that of steel, which simplifies calculations. The deflection of the end of the bar was measured to determine the curvature and subsequently the stress in the bar as well as the film could be determined. This method is still the most prevalent means of determining stress on wafer level. By measuring the curvature of the wafer before and after deposition, the stress in the deposited layer can be determined if the thickness is known.
Important assumptions were made in Stoney's formulation; firstly, the thickness of the substrate and film are assumed to be small compared to the in-plane dimensions. Also, the thickness of the film is assumed to be small compared to the substrate thickness. Furthermore, the materials are assumed to be homogeneous, isotropic and linearly elastic. The curvature of the deformed laminate is assumed to be small. Most importantly, the stresses throughout the thickness of both substrate and film are assumed to be uniform. This last assumption makes Stoney's formulation less suitable to apply when dealing with material layers that are subject to high intrinsic stresses, since these intrinsic stresses are often anisotropic in nature.

An extension to the formulation presented by Stoney was made by Huang et al. [26]. Huang modified the formulation to allow arbitrary gradients in residual stresses in film and substrate. These gradients are represented by n-degree polynomials.

Brotherton et al. [27]used a similar bi-metallic strip model to find a linear approximation of the stress distribution in both the silicon oxide film and the silicon substrate as a function of the oxidation temperature and the thickness of the oxide and substrate, based on the radius of curvature of a strained oxidized silicon slice. The behavior was assumed to be elastic and materials to be isotropic. The writer concludes that the oxide is completely in compression, while the substrate is in tension near the oxide interface and in compression near the bottom free surface.

Drieenhuizen et al. [28] present methods of determining both compressive as well as tensile stresses in thin films. The first method is based on buckling. An array of doubly-clamped beams of increasing length is constructed. Since longer beams buckle more easily than shorter ones, the shortest of the doubly-clamped beams to buckle is indicative of the stress present in the beams (see figure 2.3).
The second method is based on a rotating beam, or pointer, which is supported only by two perpendicular beams with offset centerlines. If these two supporting beams expand (compressive stress) or retract (tensile stress) the pointer assumes an angle from which the magnitude of the stress in the supporting beams can be

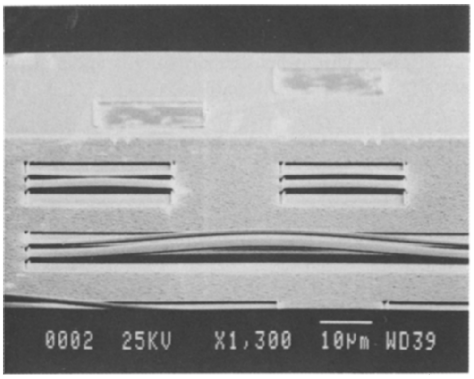


Figure 2.3: SEM photograph of buckled beams under compressive strain. The form of the buckling indicates that the clamped beam assumption is valid. [28]

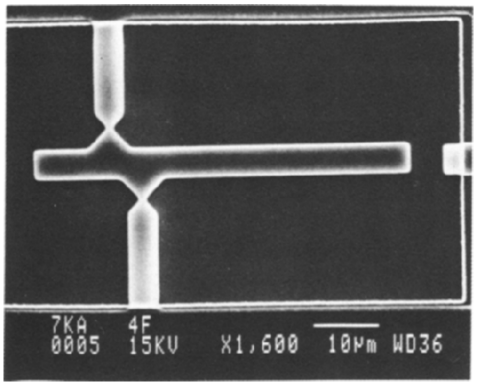


Figure 2.4: SEM photograph of the pointer under compressive strain.[28]

determined (see figure 2.4).
The buckling method has some shortcomings. Firstly, the fact that this method requires a large number of structures to determine the shortest beam that will buckle. Secondly, the resolution of the stress measurement is determined by the incremental increase in length of successive beams. Furthermore, it is relatively difficult to determine whether or not a beam has buckled, since deformations are small. Lastly, a simple doubly-clamped beam can only buckle under compressive stress; more complex structures are necessary to show buckling as a result of tensile stress.
The rotating beam, in contrast, requires only one structure capable of determining both compressive and tensile stress, and has a continuous response with greater magnitude, which makes measurements easier and more reliable.
Both methods still are only capable of determining mean stresses. No knowledge is gathered in stress gradients.

One approach that does attempt to determine the stress gradients in thin films is presented by Prime [29]. Prime cuts a structure, subject to a certain stress profile, and from the deformed surface of this newly formed cross-section, the stresses can be retraced. The method is limited to determining normal stresses and relies on the assumption that all deformations after cutting are elastic, i.e., no plastic deformations occur. Furthermore, only a pure gradient stress can be retraced, since the reference used to determine the deformed profile is arbitrary.

Any pure elongation due to average stress is therefore not taken into account.

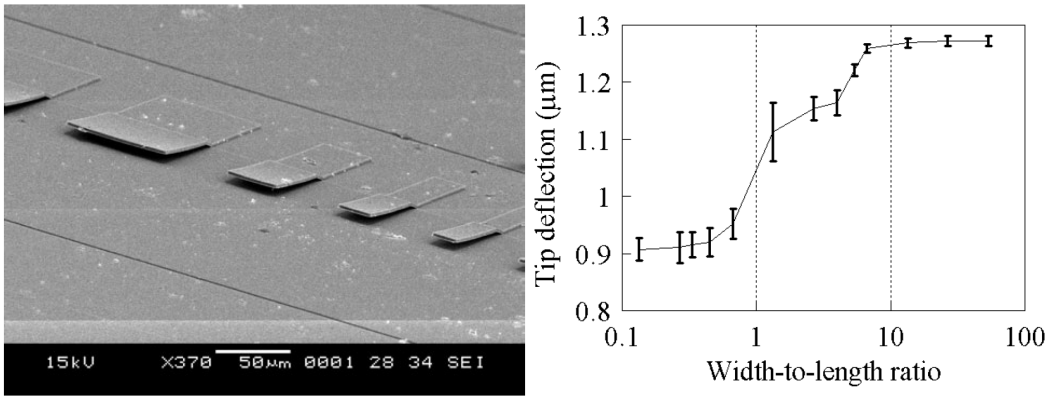
2.3.3 Modelling stresses

The only research found dealing with the modelling of intrinsic stresses in microfabricated beams is by Fang et al. [21]. Fang utilizes a two-dimensional model to predict deformations in silicon oxide beams. He assumes a mean stress in the material attributed to the thermal expansion mismatch between the silicon substrate and the silicon oxide film, and a linear stress gradient through the thickness of the film approximating the intrinsic stress profile. The mean stress causes a slope at the anchor point of the beam which is positive or negative depending on the sign of the mean stress, while the stress gradient causes the beam to curve upwards or downwards, again depending on the sign of the gradient. Fang demonstrates that the slope at the anchor point is directly proportional to the magnitude of the mean stress and linearly dependent on both the Poisson's ratio of silicon oxide and the beam thickness. Furthermore, he demonstrates that the angle caused by the curvature along the length of the beam is quadratically dependent on the thickness of the beam. Fang uses these dependencies along with experimental data to arrive at an empirical formulation of the two angles by fitting a curve. A two-dimensional finite element model (FEM) is used to verify the results, showing general agreement.

Very little research has been found on the actual prediction of intrinsic stress distributions in thin films. The only attempt at doing so is presented by Cheng et al. [30]. The method proposed utilizes a revised Thomas-Fermi-Dirac model, which is based on the condition of continuity of electron densities at the interface as a source of large internal stresses within thin films. Two methods to come to the intrinsic stress are presented; the first is a power series expansion which only considers first-order terms with respect to coordinates and disregards boundary conditions at the outer surface of the layer. This method is therefore only valid near the interface. The second method is based on a Laplace expansion, which takes higher order terms into account and thereby fulfills most boundary conditions. This method therefore holds more validity further away from the interface. Since these methods are highly theoretical and their validity is limited by a very specific set of conditions, they are not deemed suitable for use in the present research.

2.3.4 Free-Edge effects

The majority of work describing stresses in thin films is based on infinite in-plane dimensions, that is; no edge effects are taken into account. In this thesis the



(a) **(b)**

Figure 2.5: (a) A SEM photomicrograph of several surface micro-machined bilayer beams with same lengths L = 30 µm and various widths W = 13.3, 20, 40 and 80 µm. (b) Measured tip deflections versus width-to-length ratio of the surface-micro-machined bilayer beam with constant length L = 30 µm and various widths W = 4, 8, 10, 13.3, 20, 40, 80, 120, 160, 200, 400, 800 and 1600 µm. [31]

interest lies in the modelling of micro-fabricated beams for use as waveguides. Unlike the infinite plates often studied, these beams have finite dimensions in width, and it is to be expected that this finite width has some effect on the stresses and strains present.

The effect of width on the curvature of bi-layer beams was studied by Hou et al. [31]. Hou reports on an increasing tip deflection with increasing width, until a width-to-length ratio of approximately 7 is reached, after which the beam can be regarded as infinitely wide and no further increase in deflection is observed. Below this ratio the width negatively affects the tip deflection. For wide beams, the effect of the plane-strain in the center strip, away from the edges, dominates over the effect of the more complex strain at the edges. Vice versa, in narrow beams the strain at the edges dominates, since there is no plane-strain area or this part is very small (see figure 2.5).

2.4 Conclusion

An assessment of the current understanding of stress development in thin films has made clear that a substantial amount of qualitative knowledge exists on the causes of residual stresses, but a lack of quantitative understanding makes it virtually impossible to make accurate estimates of the magnitude and gradient of

these stresses [32]. The ease with which stresses can be measured through methods described above, for a large part takes away the necessity to deepen the fundamental understanding. The fact that the development of stress and the resulting stress profile is highly dependent on process parameters, but is easily reproducible if these parameters are matched, further add to the validity of measuring stresses in stead of predicting them.

The current research is focused on simulating the behavior of a bimorph beam, and therefore the actual residual stresses that develop within each deposited layer that make up this bimorph are not of specific interest. Only the influence of these residual stresses on the behavior and initial deformation of the structure are of importance. For this reason it is sufficient to empirically determine the stresses within the different material layers and use the obtained data in combination with a FEM simulation to come to a useful method of predicting the bimorph behavior.

The method to determine the magnitude of the residual stress used in this research is the one proposed by Fang et al. (see section 2.3.3), based on the deformation of monolayer beams. A number of monolayer beams will be fabricated, consisting of TriPleX and polysilicon material, and their curvature will give insight into the residual stress present in the different material layers.

Chapter 3

Method

This section covers the method used to investigate the initial deformation of the bimorph beam. First the fundamental design is presented in more detail, discussing limitations on design variables and effects of fabrication methods on specific features. Also an initial analysis of fundamental design choices is performed, used to narrow down the design space. Secondly an in-depth look at the framework of the finite element model is given. Lastly, the method used to determine the intrinsic stress present in different layers of the bimorph beam is explained.

3.1 Bimorph Beam Design

A simplified description of the design of the bimorph beam was presented in section 1.1.3 (Figure 1.2). As discussed, the dimensions of the beam itself are fixed; its width and thickness are dictated by the desired optical characteristics, while its length is determined by the need for a sufficiently high in-plane compliancy. The optical performance demands 8 µm of cladding surrounding the silicon nitride core, adding up to a minimum total width and thickness of 16 µm. The need for sufficiently low in-plane stiffness of the bimorph beam, necessary to facilitate in-plane actuation, results in a relatively long beam (lengths of 500, 750 and 1000 µm are being used in the Flex-O-Guides project). For simplicity reasons, in this thesis the length of the bimorph beam is fixed at 1000 µm.

The dimensions that have not yet been set will form the design space: the length, width and thickness of the layer of polysilicon on top and the thickness of the layer of silicon underneath the beam. It should be noted that the thickness of both the layer of polysilicon on top, as well as the silicon layer underneath the beam can be set to zero, therefore completely eliminating it from the design.

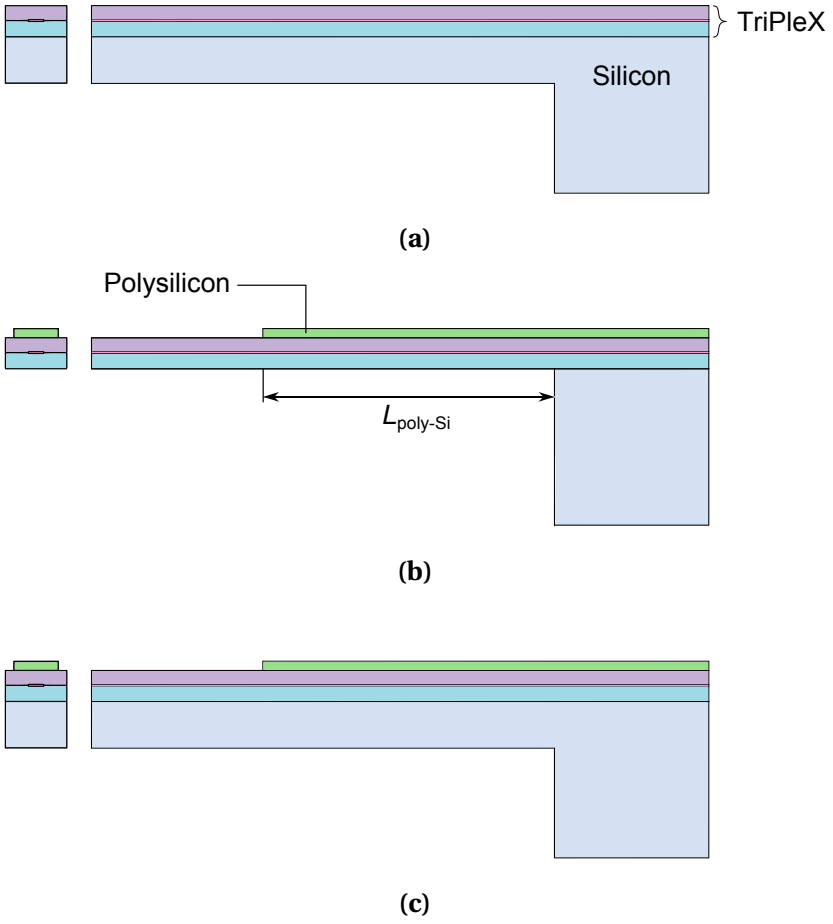


Figure 3.1: Three possible concepts of the bimorph beam design: leaving a layer of silicon underneath the TriPleX beam (a), adding a layer of polysilicon on top of the beam (b), combining both options (c)

Maintaining or omitting one of these layers yields three general concepts to be investigated (see figure: 3.1).

The first concept features the layer of silicon underneath the beam, but leaves out the layer of polysilicon on top. A number of problems arise from this design: first, the created silicon/silicon dioxide bimorph needs to be heated from a heating element on top of the beam, which requires more steps and masks to fabricate, increasing complexity and production costs. More importantly, the bimorph is fabricated at a maximum process temperature of around 1100 °C; the operating temperature of the PECVD process used to deposit silicon dioxide. At this temperature the bimorph beam is straight as intended, but when the system

cools down to room temperature, the difference in thermal expansion coefficient between the silicon and silicon dioxide will cause the bimorph to curve. Both layers will contract, but since the thermal expansion coefficient of silicon is higher than that of silicon dioxide, the silicon will contract more, causing a curvature of the bimorph towards the substrate. When looking at the consequences of this curvature in the flip-chip stage in relation to the desired position of the endpoint of the beam, it's clear that the endpoint of the beam has actually moved away from the desired position of 8 µm above the reference line. The range of motion of the bimorph will not be enough the overcome its initial deformation plus the initial 8 µm offset it has to traverse from there. Heating the system to 1100 °C would only return the bimorph beam to its undeformed state, with even higher temperatures needed for the endpoint to reach the height of the InP PIC waveguide. This concept will therefore not be investigated further.

The second concept trades in the layer of silicon underneath the beam for a layer of polysilicon on top. The first advantage of this concept is the fact that the polysilicon layer, as opposed to the silicon layer, can easily be made conductive during the fabrication process. The amount of doping applied to the polysilicon will determine its resistivity, which is used to create a thermo-electric heating element. This eliminates the need for a separate heating element on top, resulting in a simpler design. The second advantage is the direction of the initial curvature of the bimorph beam after it has cooled down from process temperature. Since the layer of polysilicon is positioned on top of the beam and it will contract more than the silicon dioxide due to its higher thermal expansion coefficient, the entire bimorph will curve away from the substrate. This is opposite from the first case where the silicon underneath caused a curvature towards the substrate. In the flip-chip situation, this results in an initial deflection of the endpoint of the interposer beam towards the desired position, instead of away from it. This initial deflection can be tuned by decreasing the length over which polysilicon is deposited along the beam ($L_{\text{poly-Si}}$). A shorter length of polysilicon leads to a smaller portion of the beam that will curve during cooling down, which decreases the deflection of the endpoint. This principle could be used to fine-tune the initial deformation of the bimorph beam, yielding a deformed state that already positions the endpoint of the beam close to its desired position. Reducing the effective bimorph length will however reduce the overall actuation range.

The third concept combines the layer of silicon underneath the beam with the layer of polysilicon on top. Having more parameters to vary might increase the control over the initial deformation of the bimorph beam, although the overall compliancy will have to be kept in check. Since silicon and polysilicon have

roughly the same thermal expansion coefficient, the stresses induced in both layers during cooling down will counteract each other, providing a possibility to effectively tune the initial curvature of the bimorph beam. At the same time, the counteraction of both layers reduces the bimorph effect, reducing its actuation range.

While some of the features and dimensions of the bimorph beam are fixed by external demands, others are the result of the fabrication methods used to deposit and etch each layer.
As shown in figure 1.1 the layer of polysilicon on top of the beam is formed by depositing a layer of a specified thickness across the entire waver, and etching away the majority, leaving a thin strip. The photolithography used in the etching of the polysilicon is performed using a contact mask; a mask that is placed directly onto the substrate. A contact aligner is used to manually align the mask to the substrate using a microscope. This method is accurate to within about 1 µm. To ensure the layer of polysilicon lies entirely within the edges of the beam, a margin to the edge of the beam has to be kept minimally equal to the alignment accuracy of 1 µm. This means the width of the layer of polysilicon will always be 2 µm less than the entire width of the beam.
After etching of the polysilicon, the TriPleX layer is etched to create the bimorph beam geometry. This step is performed using a photoresist mask. Since this mask is also slightly affected by the etchant, the width of the polymer mask will decrease during etching. This results in sidewalls that are not perfectly vertical, but tapered towards the top (see Figure 3.2).

As described in section 1.1.3, the release of the bimorph beam is performed in two steps; first the silicon is etched straight down using Bosch process, secondly the silicon is etched isotropically to release the beam. This two-step process is designed to leave a layer of silicon attached to the bottom of the beam to provide structural support during the release, minimizing the chances of fracture in the beam. The Bosch process etches the silicon in small increments: the desired area is etched isotropically using a plasma etch for a short amount of time, after which a passivation layer is deposited designed to protect the silicon from the isotropic plasma etch. Vertically directed ions in the isotropic plasma etch subsequently remove the passivation layer, but only on the bottom of the etched trench, leaving the passivation layer on the sidewalls intact. These steps are repeated to create holes and trenches with high aspect ratios. Depending on the setup of the process parameters these trenches can have walls at an angle of 90°, but larger angles are also possible. The process in this case is set up to create angles larger than 90°, resulting in a silicon layer that is tapered towards the bottom

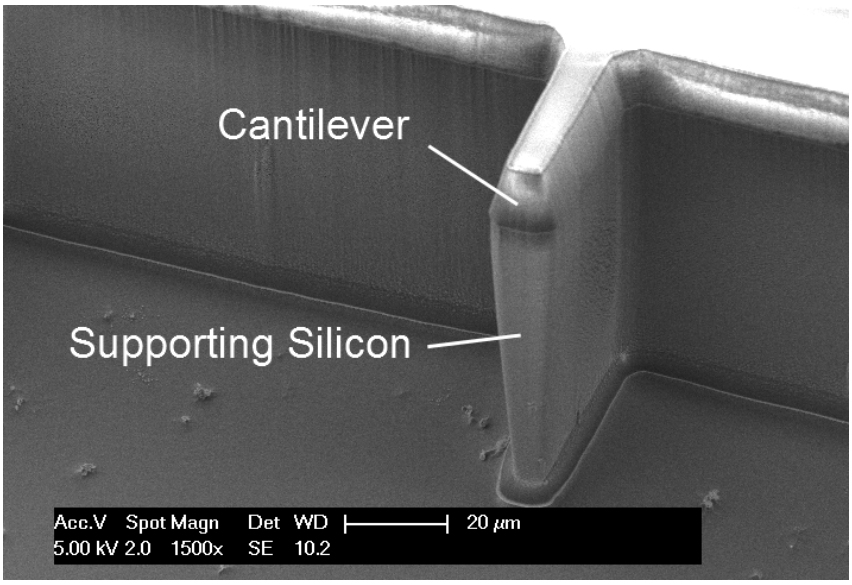


Figure 3.2: Scanning Electron Microscope (SEM) picture of a short TriPleX beam not yet released from the substrate. Indicated are the TriPleX beam, as well as the layer of silicon underneath that is designed to offer support to the beam during release. This picture shows clearly the tapered cross-section of both the TriPleX beam and the silicon layer, as a result of their respective etch processes.

(see Figure 3.2).

3.2 Finite Element Model

This section will present the framework of the finite element model used in simulating the initial deformation of the bimorph beam within the COMSOL finite element software package. It covers the geometry, material properties, meshing and solving methods. The model will simulate the behavior of the bimorph as it cools down from its fabrication process temperature to determine its initial deformation, and subsequently simulate its actuating behavior.

3.2.1 Geometry

To effectively simulate the initial deformation of the bimorph beam it is important to assess which parts of the geometry should be included in the finite element model and to which extend they contribute to the accuracy of the simulation results. This ensures the available processing power is used most efficiently, allowing for higher accuracy and decreased solving times. The assessment is made by focusing on the key elements that dominate the behavior of the system.
The initial deformation of the bimorph beam stems from two parts; most importantly is the out-of-plane bending of the bimorph itself, which is responsible for the induced curvature. Besides the effect of the bimorph bending, complex deformations occur at the anchor point of the beam to the substrate, which are responsible for the initial angle at the base of the beam, as discussed in section 2.2.1. The model therefore needs to consist not only of the bimorph beam, but also of a sufficiently large part of the substrate near the beam.

To ensure the geometry is as simple as possible and the load on the processor while solving is minimized, two observations are important to make; first, the entire system is symmetrical along the length of the bimorph beam. This means only half of the bimorph has to be modeled, using a mirror constraint to simulate the other half. This cuts the number of elements in half, resulting in half the load on the processor. Secondly, even though a large part of the substrate near the bimorph beam contributes to the initial deformation of the system, it is mainly the material in a direct line behind the beam that is of interest; its expansion causes the deformations at the anchor point of the beam. Therefore a relatively narrow but long slice of the substrate is sufficient to accurately determine its effect on the behavior of the bimorph. Not having to model a large portion of the sub-

strate minimizes the amount of elements used.

The basis of the geometry is formed by the TriPleX beam, attached to the substrate at the anchor point. It consists of two layers of silicon dioxide with a thin strip of silicon nitride in the middle. On top of the TriPleX beam a layer of polysilicon is added. Due to the inaccuracy in the manual alignment of the masks used in etching the polysilicon, the polysilicon layer is less wide than the top surface of the TriPleX beam to allow for some uncertainty in its lateral position.

The final geometry created in COMSOL is presented in figure 3.4.

3.2.2 Material Properties

A large selection of properties of materials commonly used in MEMS is available within the COMSOL Materials database, listing constant values. When dealing with a large variation in temperature however, it is necessary to look at the temperature dependence of certain properties, since these properties can vary significantly with changing temperatures.

In this work four materials are used: silicon, polysilicon, silicon dioxide (both thermally grown and deposited using PECVD) and silicon nitride. For each of these materials, the following thermal and mechanical properties need to be assessed:

- Thermal properties:
  - Coefficient of thermal expansion (CTE) (α)
  - Heat capacity at constant pressure (C_p)
  - Thermal conductivity (λ)
- Mechanical properties:
  - Young's modulus (E)
  - Poisson's ratio (ν)
  - Density (ρ)

The thermal behavior is of specific interest, since it forms the basis of the principle behind the bimorph actuator, therefore the thermal properties and their temperature dependence will be investigated in detail for each material. The mechanical properties are assumed to be constants. All material properties that were used are listed in table 3.1.

Silicon

Since silicon forms the basis of most MEMS devices, a lot of its mechanical and thermal properties have been extensively documented. Most applications do not require thermal dependencies to be taken into account, however a significant amount of work reporting on thermal dependent material properties has been found.

COMSOL lists a value of the CTE of silicon of 2.6×10^{-6}/K, valid at 298 K. However, values as high as 4.56×10^{-6}/K at 1500 K and even negative values as low as -0.51×10^{-6}/K at 100 K have been reported [33, 34]. Okada et al. [33] provide a fit to empirical values of the thermal expansion coefficient using a least-squares approach:

$$\alpha(T) = (3.7251 - \exp[-5.88 \times 10^{-3}(T - 124)] + 5.548 \times 10^{-4} T) \times 10^{-6} \tag{3.1}$$

where T is the temperature in Kelvin. This equation is incorporated into the materials list of the COMSOL model to ensure accurate behavior of thermal expansion at different temperatures.

The heat capacity of silicon is also well documented. Gurvich et al. [35] provide provide experimental values of the heat capacity of pure silicon between 100 and 1600 K, combining data of a number of researches. More recently Glazov et al. [36] provide a fit to new empirical data, agreeing with the data provided by Gurvich et al.:

$$C_p = 23.698 + 3.305 \times 10^{-3} T - 4.354 \times 10^{5} T^{-2} \tag{3.2}$$

where T is the temperature in Kelvin. This empirical function will be included in the COMSOL materials list.

Values of the thermal conductivity of silicon at different temperatures have also been found. Yamasue et al. [37] report average values of the thermal conductivity of silicon of 139.4 W m/K at 293 K, up to 19.0 W m/K at 1673 K. The tabulated data they provide will be used to interpolate values of the thermal conductivity within COMSOL. The data can be found in appendix A.

Polysilicon

COMSOL provides a value of the CTE of polysilicon of 2.6×10^{-6}/°C, equal to the provided value for single-crystal silicon. In literature however, large variations

in the value for the CTE are reported. Oh et al.[38] report values ranging from 3.7×10^{-6} to 6.4×10^{-6}/°C, while Tada et al. [39] report an increase in CTE from 2.9×10^{-6}/°C at room temperature to 5.8×10^{-6}/°C at 900 °C. Both authors draw no definite conclusions due to high uncertainty resulting from the method used, other than the fact that the CTE for polysilicon may be significantly higher than that of bulk single-crystal silicon. Because of this high uncertainty, the value provided by COMSOL will be used in simulation.

No useful data on the temperature dependence of the heat capacity and the thermal conductivity of polysilicon have been found, therefore the values provided in the COMSOL materials list are used.

Silicon Dioxide

Silicon dioxide has not received the same attention that silicon has when it comes to research into its (thermo)mechanical properties. The use of silicon dioxide as a structural material, as opposed to an optical medium or electrical insulator, is fairly limited and therefore not much effort has been given to the determination of its thermal and mechanical properties. For this reason no useful information on the thermal dependence of the thermal properties of silicon dioxide has been found. COMSOL provides a value for the CTE of silicon dioxide of 0.5×10^{-6}/°C, and similar values are found in literature: El-Kareh [40] reports a value of 5.6×10^{-7}/°C.

No useful data on the temperature dependence of the heat capacity and the thermal conductivity of silicon dioxide have been found, therefore the values provided in the COMSOL materials list are used.

Silicon Nitride

COMSOL provides a value for the CTE of Silicon Nitride of 2.3×10^{-6}/°C, however in literature higher and lower values can be found: Tokuyama et al. [41] report a value of 3.85×10^{-6}/°C for silicon nitride deposited at 800 °C, while Retajczyk et al. [42] reports a value of 1.5×10^{-6}/°C. For this reason the value provided by COMSOL is taken as a suitable average.

No useful data on the temperature dependence of the heat capacity and the thermal conductivity of silicon nitride have been found, therefore the values provided in the COMSOL materials list are used.

Table 3.1: Material properties used in finite element modeling of the bimorph beam using the COMSOL finite element package. Values without reference are imported from the COMSOL materials list.

	Silicon	Polysilicon	Silicon Dioxide	Silicon Nitride
Coefficient of Thermal Expansion (CTE)	Eq. 3.1 [33]	2.6×10^{-6}/K	0.5×10^{-6}/K	2.3×10^{-6}/K
Heat Capacity	Eq. 3.2 [36]	678 J/(kg K)	730 J/(kg K)	700 J/(kg K)
Thermal Conductivity	Tab. data [37]	34 W/(m K)	1.4 W/(m K)	20 W/(m K)
Young's Modulus	170 GPa	160 GPa	70 GPa	250 GPa
Poisson's Ratio	0.28	0.22	0.17	0.23
Density	2329 kg/m^3	2320 kg/m^3	2200 kg/m^3	3100 kg/m^3

3.2.3 Physics

Two physics modules are used to model the thermo-mechanical behavior of the bimorph beam: the "Solid Mechanics" module covers the mechanical aspect of the behavior, while the "Heat Transfer in Solids" simulates the thermal aspect. The two modules are coupled by the "Thermal Expansion" and the "Thermal Coupling" module. This coupling is one-way, meaning only temperature data is passed on from the "Heat Transfer in Solids" module to the "Solid Mechanics" module. The effect of the mechanical behavior on the temperature is assumed to be negligible, so the reverse coupling is not taken intro account.

The "Solid Mechanics" module most importantly contains the mechanical boundary conditions. As mentioned previously, to optimize the use of the available processing power, only one half of the bimorph actuator is modelled. This modelling choice means a "symmetry" constraint has to be used on each face on its symmetry plane.

To fix the x, y and z-translation of the entire geometry, a "fixed" constraint was applied to a corner furthest away from the beam.

To prevent rotation of the geometry around the x and y-axes a "roller" constraint was applied to the bottom surface of the substrate. The "roller" constraint constrains translation and rotation along two axes, while allowing translation and rotation along the third.

The modelled geometry is essentially a 'slice' taken from the substrate, meaning in reality the cut surfaces will not be visible as they are part of the substrate. To prevent the cut surface itself from deforming, e.g. bulging of the oxide layer on top of the silicon, yet allowing the entire surface to translate, a "forced displacement" constraint is used. These forced displacements are given as vari-

ables, COMSOL subsequently solves for these variables, making sure that the total displacement of the cut surface is equal for each part of the cut surface. This guarantees the cut surface remains plane after deformation, but the entire surface is allowed to displace.

The use of constraints is illustrated in figure 3.3.

The "Heat transfer in Solids" contains the initial values for temperature, in this case the process temperature, as well as a "Heat Flux" module used to subsequently cool the system down to room temperature.

The "Thermal Expansion" module covers the properties pertaining thermal expansion, requiring a coefficient of thermal expansion, as well as a strain reference temperature. The coefficient of thermal expansion is found in the materials list, while the strain reference temperature is taken to be the initial temperature of the system. At the initial temperature (the process temperature) no stresses, and therefore no strains, have been generated in the layers of the bimorph beam. Therefore it serves as the "reference" temperature for subsequent strains.

3.2.4 Meshing

Meshing can be a tricky part of finite element modelling, especially when dealing with a large variation in dimensions. In the case of the bimorph beam the smallest dimension is the thickness of the silicon nitride strip that forms the core of the waveguide (130 nm), while the largest dimension is the length of the waveguide beam itself (1000 µm). Features of small dimensions obviously require a fine mesh, but even more so since they can often be subject to high stresses and deformations. Larger bodies that do not contain fine features can be accurately modelled using a coarser mesh since no high stress concentrations are expected. To optimize the accuracy of the overall model it is crucial to assess which parts require fine meshing and which parts suffice with a courser mesh. This allows the available processing power to be distributed most effectively.

The highest mesh density is found within and surrounding the silicon nitride waveguide core (see figure 3.4). Since this core is of such small dimensions compared to the waveguide beam itself, it pays to investigate its significance on the simulation results; if its impact on the overall results is small, it might not be desirable to omit it from the model. Figure 3.5 shows the results of a simulation of a bimorph waveguide beam of arbitrary dimensions for different lengths of the polysilicon layer on top of the beam, looking at the initial vertical endpoint deflection, with and without the silicon nitride core. The results show clearly that the core is of little significance to the simulation results, with an average differ-

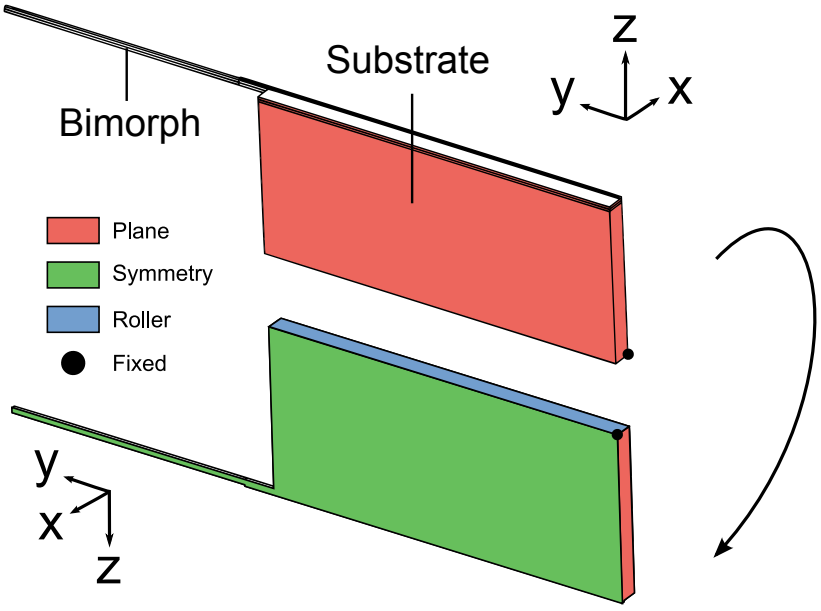


Figure 3.3: Schematic drawing of the constraints used in the FEM model in COMSOL. Indicated are: cut surfaces forced to remain plane (red), surfaces part of the symmetry plane (green), bottom surface of the substrate subject to a roller constraint (blue) and the corner of the geometry that is entirely translationally fixed in space (dot). These constraints guarantee the geometry is allowed to contract freely during cooling down, yet all surfaces that are in reality an internal part of the wafer will remain plane.

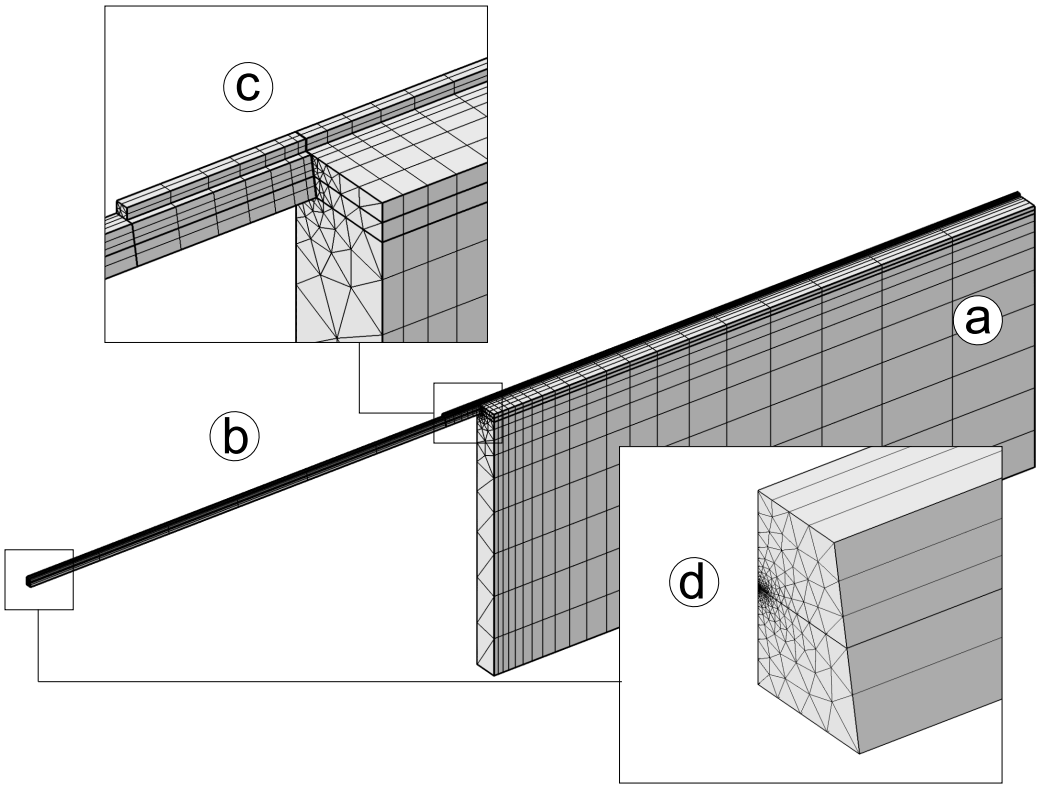


Figure 3.4: Isometric view of the finite element model geometry, showing: the substrate (a), the bimorph beam (b), layer of polysilicon that extends onto the beam showing increasing mesh element density near the anchor point(c), meshing of the face of the beam showing extremely fine mesh surrounding the beam core (d)

ence of only 0.024 % of the simulation without core compared to the simulation with core. For this reason the core will not be used in general, yet the option to include it remains present in case the stresses or strains near or within the nitride core are of interest.

Omitting the silicon nitride core results in a less dense mesh. A free triangular mesh is subsequently used to mesh the face of the endpoint of the beam, while a swept mesh is used to extend the mesh along the length of the beam. The way the swept mesh operates in COMSOL dictates that two separate swept meshes are needed: one for the part that is covered by polysilicon and one for the part that is not. A custom distribution is used to determine the number of elements generated by the swept mesh on both parts. Depending on the length of the polysilicon layer more of fewer elements are needed on both parts. To ensure a

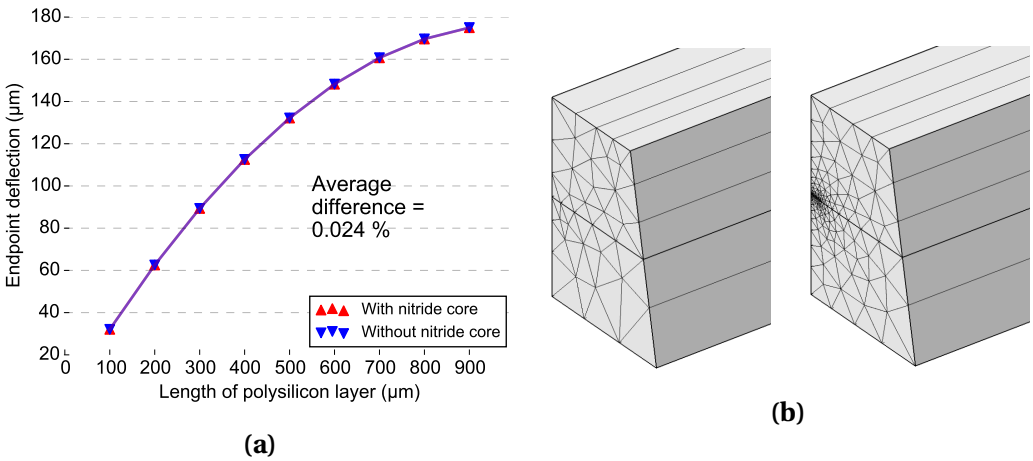


Figure 3.5: (a) shows a comparison of simulation results of the length of the polysilicon layer versus the initial endpoint deflection of the bimorph waveguide beam for a bimorph of arbitrary dimensions. The graph illustrates the significance of including the silicon nitride core in the FEM model on simulation results. The difference is deemed too small to justify the extra computational load inclusion of the silicon nitride core demands. (b) shows the difference in mesh density on the face of the TriPleX waveguide beam, with the increase in the number of elements caused by the core clearly visible.

more or less constant distribution of elements along the entire beam the number of elements for each part is determined by

$$n_1 = \lceil \frac{1}{2} L_{\text{polySi}} \times 10^4 \rceil + 7 \tag{3.3a}$$

$$n_2 = \lceil \frac{1}{2} (1 - L_{\text{polySi}} \times 10^4) \rceil + 5 \tag{3.3b}$$

where n_1 is the number of elements on the first part of the beam, nearest the substrate, covered by polysilicon, n_2 is the number of elements on the second part of the beam, not covered by polysilicon, L_{polySi} is the length of the polysilicon layer and the $\lceil x \rceil$ operator is used to indicate rounding off to the nearest integer larger than x. Equation 3.3 guarantees a minimum of 7 elements for the first part and a minimum of 5 elements for the second part of the beam. An "arithmetic sequence" with a ratio of 40 is used on the first part of the beam to generate more elements near the base of the beam, since a finer mesh is required. An equally spaced distribution is used for the second part.

The same approach is used for the substrate: the face of the substrate is meshed using a free triangular mesh, while a swept mesh extends the mesh along the length of the substrate. A "geometric sequence" is used to create more elements near the base of the beam, as shown in figure 3.4.

3.2.5 Solving Method

The behavior of the bimorph beam can be split into two parts. Firstly, the bimorph beam cools down from the process temperature, causing the initial deformation. A stationary solver is used to study this behavior. Secondly, the bimorph actuator is operated by heating the polysilicon. A second stationary solver is used to study the actuating behavior, taking the solution of the first solver as initial conditions.

3.3 Measuring Intrinsic Stress

The finite element model at this stage is capable of simulating the effect of changes in temperature on the behavior of the bimorph beam; it uses just the difference in CTE between layers of different materials to determine the stresses that are induced by a change in temperature and the bending moment they generate. Simulating the effect of the difference in CTE should provide accurate results for

the pure bimorph bending of the bimorph beam, as well as for the initial slope at the anchor. However, the so-called thermal stress is only part of the total residual stress that the layers are subject to, the other part being the intrinsic stress (as discussed in section 2), responsible for the curvature observed in single-material beams. Since the origin of intrinsic stress specifically lies in the structure of a material on a crystallographic level, and is therefore very complex in nature, there is no way of simulating its effects in a finite element modelling environment. For this reason the intrinsic stress will be determined empirically for each material layer and incorporated into the finite element model.

A common method of gaining insight into the intrinsic stress present in thin layers is to examine the deformation of freely suspended features fabricated from the layer of interest. These deformations give information on bending moments generated by the non-uniform distribution through the thickness of the layer of the in-plane intrinsic stresses. A simple feature used to examine intrinsic stress is the freely suspended beam. Due to the moments generated by the intrinsic stress, a beam fabricated from a thin layer will curve out-of-plane when released from the substrate. The curvature of the beam can be determined and used to find the bending moment that is generated by the intrinsic stress. To incorporate the effect of the intrinsic stress into the finite element model a simple linear stress distribution is assumed that would generate the same bending moment. Although in an ideal situation the actual stress distribution throughout the thickness of the layer would be known, this is not necessary for the present modelling purposes.

Since only small deflections of the beam endpoint (<1% of the beam's length) are expected, simple beam theory is used to determine the equivalent linear stress distribution throughout the thickness of the beam. The assumptions that are made to allow the use of beam theory are:

1. Strains in out-of-plane direction are negligible
2. Cross-sectional planes will remain perpendicular to the neutral axis of the beam
3. The beam material is isotropic and linear elastic

The assumed stress distribution throughout the thickness of the beam is a simple linear one, ranging from a maximum tensile stress $\sigma_{\max}$ at the top surface to a maximum compressive stress -$\sigma_{\max}$ at the bottom surface and zero stress at the neutral axis, as shown in figure 3.6. The value of $\sigma_{\max}$ is what is of interest

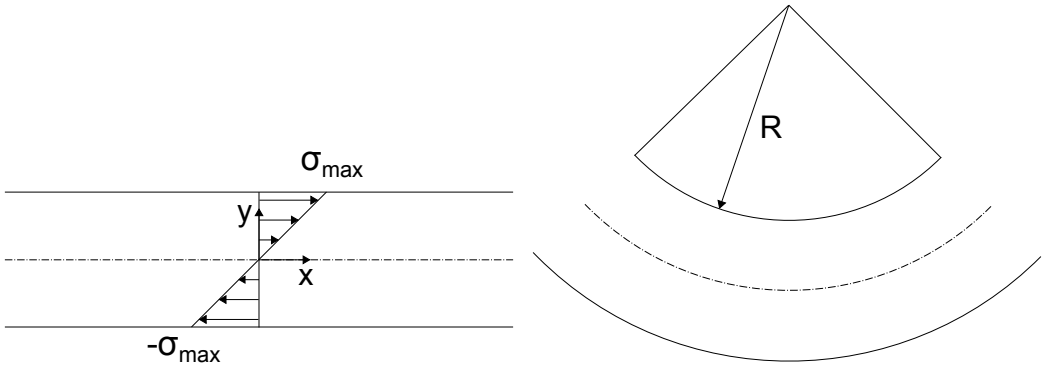


Figure 3.6: Schematic cross-section of a beam, illustrating the extracted equivalent stress profile that reproduces the measured curvature (a). (b) indicates the measured radius of curvature of a beam.

here, since it can be used to enter the stress profile into the COMSOL model. Mathematically the normal stress can be described by:

$$\sigma(y) = \frac{2\sigma_{\max}}{t} y \tag{3.4}$$

Where t is the thickness of the beam and y is the vertical coordinate with origin lying in the middle of the beam's cross-section. The moment generated by the normal stress can be determined by integrating the stress multiplied by the distance to the neutral axis over the cross-section:

$$\begin{aligned} M &= \int_{-\frac{t}{2}}^{\frac{t}{2}} \sigma(y) y w dy \\ &= \frac{1}{6}\sigma_{\max} w t^2 \end{aligned} \tag{3.5}$$

Where w is the beam width. The moment generated by the normal stress can be related to the radius of curvature of the beam through the following equation:

$$M = \frac{EI}{R} \tag{3.6}$$

Where E is the Young's modulus of the beam material and I is its moment of inertia. The moment of inertia is given by:

$$I = \frac{w t^3}{12} \tag{3.7}$$

Combining 3.5 and 3.6 yields the relation between the maximum stress $\sigma_{\max}$ and the curvature of the beam:

$$\sigma_{\max} = \frac{6EI}{wt^2R} \tag{3.8}$$

This equation is used to determine the maximum stress found in the equivalent stress distribution of 3.4 from the measured curvature of the beam.

3.3.1 Design of Experiment

As discussed before, freely suspended beams can be used to determine the magnitude of the intrinsic stress present within a thin layer. Each layer that makes up the bimorph beam is either of a different material or deposited using a different process than all the other layers. Therefore each layer develops a distinct intrinsic stress profile, which can be experimentally determined.

The bimorph beam consists of a number of layers: first there is the TriPleX beam itself, consisting of a layer of thermally grown silicon oxide with a small silicon nitride strip on top covered by another layer of PECVD silicon oxide. Secondly a layer of polysilicon is deposited on top of the TriPleX beam. Ideally the intrinsic stress in each material layer would be known, to most accurately model the behavior of these layers. This would mean at least four different experiments would have had to be conducted, each requiring an individual test wafer. Moreover, the polysilicon layer is of particular interest, since design choices will have to be made regarding layer thickness and doping specifications. Therefore different test wafers had to be fabricated to vary the design parameters of the polysilicon layer. To limit the amount of test wafers necessary, the decision was made to treat the entire TriPleX stack as one layer, reducing the number of test wafers from three to one. Since the ultimate aim of the measurements is to more accurately model the stresses in the bimorph beam, it is not necessary to obtain the stress distribution within the layers that make up the TriPleX beam. Determining the intrinsic stress for the TriPleX stack as a whole provides a means to model its effect on the behavior of the bimorph beam, and since the dimensions of the TriPleX are fixed, the intrinsic stress does not vary.

Reducing the number of test wafers used in determining the intrinsic stress in the TriPleX stack leaves room to investigate the intrinsic stress present in the polysilicon layer. The expected thickness of the polysilicon layer needed to achieve sufficient actuating capabilities with the bimorph beam lies between 3 µm-5 µm. To study the effect of layer thickness on the intrinsic stress, both 3 µm and 5 µm

thick layers will be investigated. Besides layer thickness, doping may have a significant influence on the development of intrinsic stress. For this reason both doped and undoped polysilicon will be investigated.

Since the intrinsic stress generated during deposition is dependent on process parameters and the layer thickness, the in-plane dimensions of the beam do not influence the intrinsic stress, i.e., an equal curvature is expected for each beam, regardless of its width or length. Nevertheless it is likely that the stress distribution near the edges of the beam is different from the stress distribution at the center. In a slender beam the stress on the edges will dominate the total stress distribution, while a wide beam will have a larger contribution of stress at the center. Differently sized beams may therefore experience different deformations as a result of the same intrinsic stress. To study this effect, beams of different lengths and widths are investigated. The minimum width of the TriPleX beam is around 18 µm, as dictated by the desired wave propagating qualities, nonetheless widths smaller than 18 µm will be investigated to extend the knowledge on very slender beams. There is of course virtually no limit to the maximum width of a beam. The minimum width is set to 10 µm, to guarantee sufficient beams survive the fabrication process, while the maximum width is 54 µm, 50 % wider than the widest TriPleX beam produced within the Flex-O-Guides project [8]. The width of subsequent beams will increase by an increment of 4 µm. Besides the width, three different lengths of the beam will be investigated, 500 µm, 750 µm and 1000 µm.

3.3.2 Fabrication of Test Structures

Five wafers containing test structures are fabricated: four wafers containing polysilicon beams and one wafer containing TriPleX beams.

The wafers containing polysilicon beams are fabricated using the following process steps, starting from a silicon wafer with a diameter of 10 cm and a thickness of 525 µm:

1. Top and bottom surface of wafer are thermally oxidized to form a layer of 2 µm thick silicon dioxide
2. Polysilicon is deposited on top of the oxide on the top surface of the wafer
    - Deposition time determines layer thickness. Either 3 µm or 5 µm is desired.

- Two of the four wafers are doped to a sheet resistance of 30 Ω/□

3. DRIE is used to etch through the polysilicon layer, creating the beam shape

4. An isotropic vapour HF etch process is used to remove the oxide underneath the beam, creating a freely suspended beam

The wafers containing TriPleX test structures required fewer process steps, since the wafers are shipped with the TriPleX stack already present. The following process steps were subsequently used to fabricate freely suspended beams:

1. DRIE is used to etch through the TriPleX layer, creating the beam shape

2. The silicon is etched anisotropically to a depth of 60 µm

3. The silicon is etched isotropically to release the TriPleX beam and remove all silicon underneath

Both descriptions of the process steps are simplified. The full process flowchart can be found in appendix B.

3.3.3 Measuring Curvature

Height Map

To determine the curvature of the beams a white-light interferometer[1] is used to extract a height map. This height map is a two-dimensional grid of points containing height data. A visual example is shown in figure 3.9a. From this height map two height profiles are extracted: the first along the length of the beam, the second across the trench next to the beam, as shown in figure 3.9b. These height profiles are used to calculate the radius of the curvature of each beam.

Algorithm

An algorithm was employed to automatically fit a curve to the beam height profile and determine its radius. This algorithm is designed to isolate the curved part of the beam from its height profile and subsequently fit a circle trough this curve using a least-squares approach, yielding its radius of curvature. The process is illustrated in figure 3.10

[1] Bruker Contour GT-K 3D Optical Profilometer

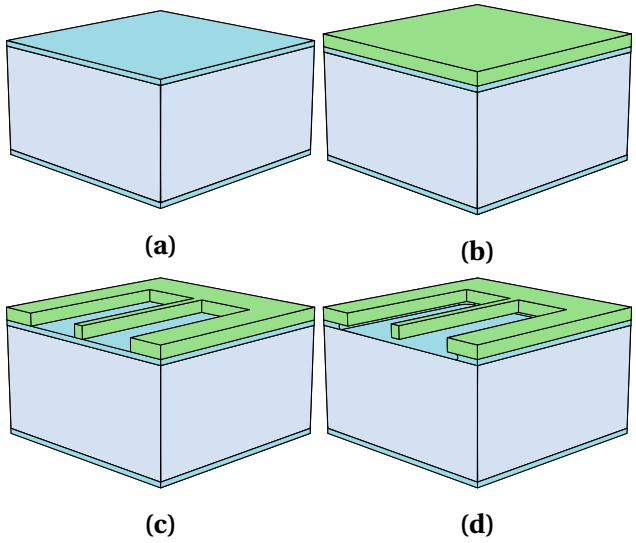


Figure 3.7: Schematic illustrating the fabrication of the polysilicon beam test structure. Fabrication starts with thermally oxidizing the silicon wafer to create a 2 µm thick silicon dioxide layer (a). A layer of polysilicon is then deposited on top of the oxide, with a thickness of 3 µm or 5 µm (b). Doping, if desired, is applied during deposition. The polysilicon is etched to create a beam shape (c). Finally, the silicon dioxide layer is etched isotropically to release the beam from the substrate (d).

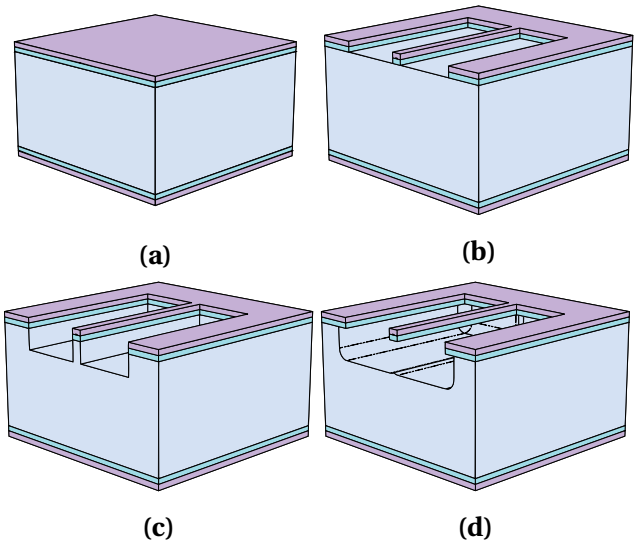
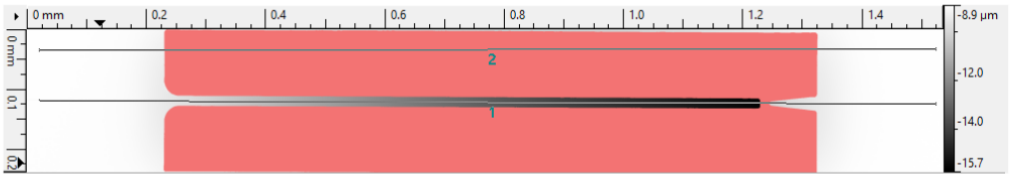
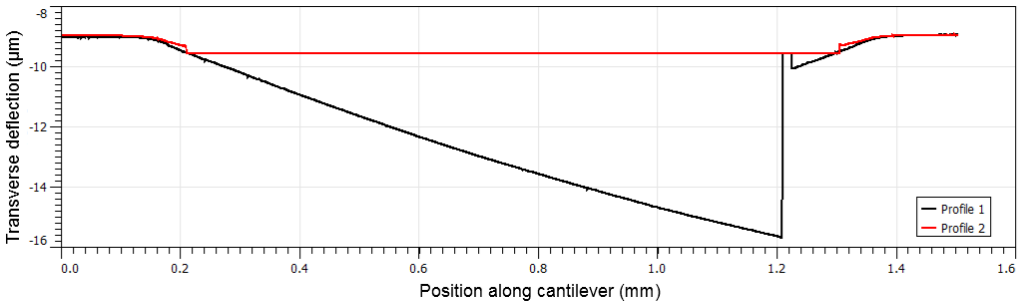


Figure 3.8: Schematic illustrating the fabrication of the TriPleX beam test structure. Fabrication starts with a silicon wafer with the TriPleX material stack already present (a). The TriPleX is etched to reveal the silicon substrate below, creating a beam shape (b). The silicon is etched anisotropically, leaving a layer of silicon attached to the TriPleX beam (c). Finally, the silicon is etched isotropically, releasing the beam from the substrate and removing all silicon attached to it (d).



(a)



(b)

Figure 3.9: Example of the height map of a single beam as obtained from the white-light interferometer (a). Also shown are the positions of two parallel height profiles: one along the beam itself, the other across the trench. The actual height profiles are shown in (b).

The algorithm firstly uses the height profile across the trench next to the beam to determine roughly where the trench starts, equating this to the position of the base of the beam. The position of the endpoint of the beam is then accurately determined by finding the minimum value of the beam height profile. The position of the base of the beam and the position of the endpoint are used to crop the height profile to cover just the beam itself. To ensure the actual curved part of the beam is isolated, the coordinates of the beginning and end of the beam are extended inwards by a constant factor.

Now that the desired portion of the beam height profile has been isolated, the algorithm attempts to fit a circle through the remaining data points using the least-squares approach to find an optimal fit. The method starts by determining the average of the x and y-components of all data points:

$$\bar{x} = \frac{1}{N}\sum_i x_i \tag{3.9a}$$

$$\bar{y} = \frac{1}{N}\sum_i y_i \tag{3.9b}$$

where N is the number of datapoints in the extracted height profile. A new set of coördinates is defined relative to the average of the coördinates:

$$u_i = x_i - \bar{x} \tag{3.10a}$$

$$v_i = y_i - \bar{y} \tag{3.10b}$$

A system of two equations is then solved simultaneously:

$$u_c S_{uu} + v_c S_{uv} = \frac{1}{2}(S_{uuu} + S_{uvv}) \tag{3.11a}$$

$$u_c S_{uv} + v_c S_{vv} = \frac{1}{2}(S_{vvv} + S_{vuu}) \tag{3.11b}$$

where (u_c, v_c) are the coördinates of the center of the circle and the following definitions are used:

$$S_{uu} = \sum_i u_i^2 \tag{3.12a}$$

$$S_{uv} = \sum_i u_i v_i \tag{3.12b}$$

$$S_{vv} = \sum_i v_i^2 \tag{3.12c}$$

$$S_{uuu} = \sum_i u_i^3 \tag{3.12d}$$

$$S_{uvv} = \sum_i u_i v_i^2 \tag{3.12e}$$

$$S_{vvv} = \sum_i v_i^3 \tag{3.12f}$$

$$S_{vuu} = \sum_i u_i^2 v_i \tag{3.12g}$$

Solving equations (3.11a) and (3.11b) using the definitions from (3.12) yields (u_c, v_c). The radius of the circle can now be found as follows:

$$R^2 = u_c^2 + v_c^2 + \frac{S_{uu} + S_{vv}}{N} \tag{3.13}$$

where R is the radius of curvature of the fitted circle.

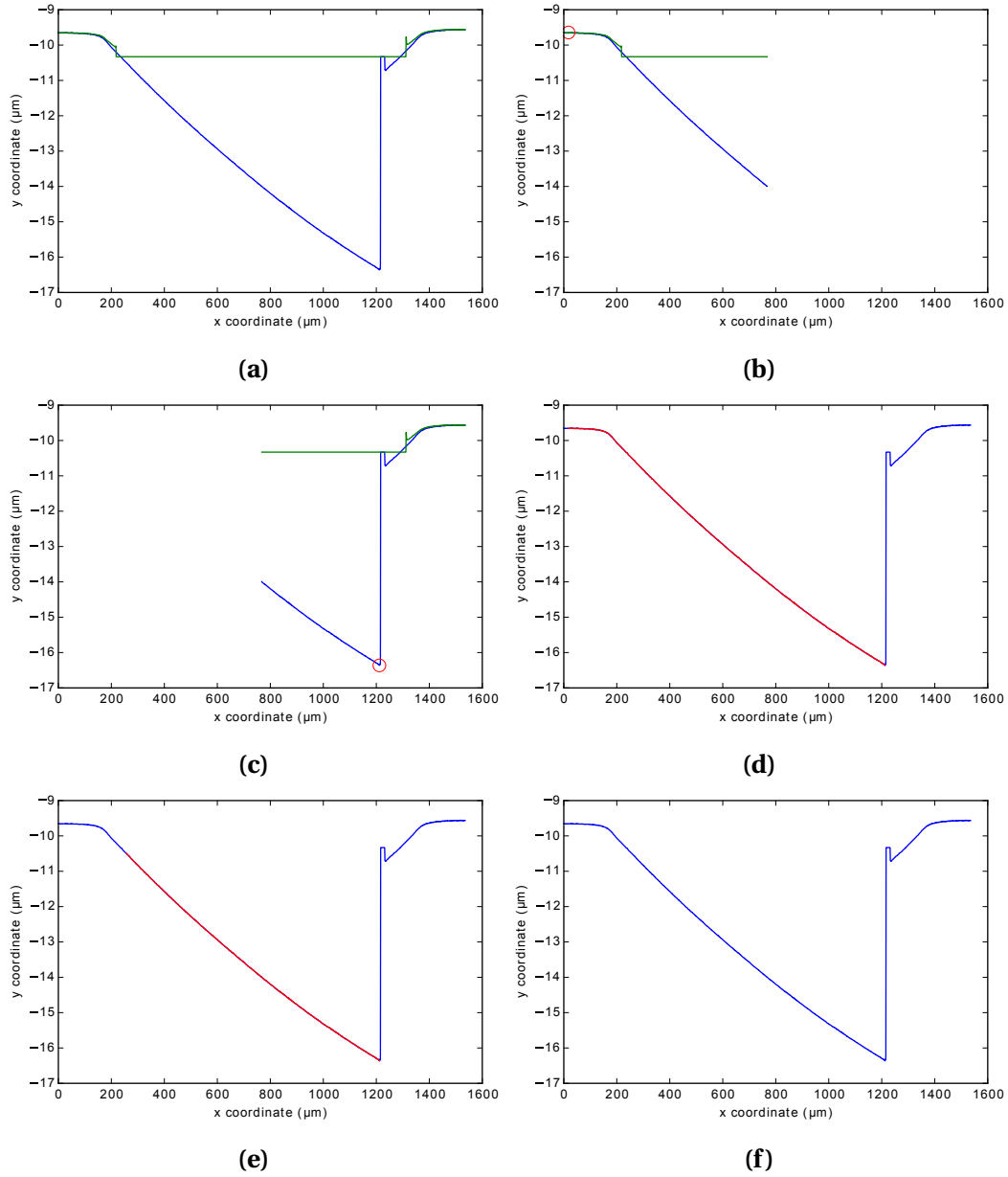


Figure 3.10: Circle fitting algorithm shown operating on the height profile of a freely suspended TriPleX beam: (a) Height profile of the beam (blue) and trench (green), (b) left half of both profiles, maximum value of trench profile encircled in red, (c) right half of both profiles, minimum value of beam profile encircled in red, (d) first crop of beam height profile using determined minimum and maximum, (e) second crop to ensure isolation of curvature, (f) circle fitted to final cropped profile

Chapter 4

Results & Discussion

This section presents the results of the measurements of intrinsic stress discussed in chapter 3. Section 4.1 discusses the results of the fabricated test structures, indicating which parts were usable and which were not. Section 4.2 presents the primary results of the measurements of the intrinsic stress for the TriPleX and polysilicon material layers. In section 4.3 the accuracy of the model complemented by the measured intrinsic stress is verified by comparing the simulation results with the measured data. Section 4.4 presents the results of the completed model of the bimorph waveguide, indicating values for the length of the layer of polysilicon that would yield the desired endpoint deflection of 8 µm. Finally, section 4.5 discusses an approach at verifying the accuracy of the completed model of the bimorph waveguide through realized structures that implement the use of a bimorph with polysilicon deposited along a part of the beam's length.

4.1 Results Fabrication

The fabrication of the beams used to determine the intrinsic stress in TriPleX and polysilicon layers, as discussed in section 4.1, came with some complications, yielding only a fraction of the desired chips for measurement. While the wafer containing TriPleX beams provided all the desired results, the polysilicon beams were often found to be stuck to the substrate, either because the silicon dioxide etch duration was insufficient to release them from the substrate, or because the intrinsic bending stresses were of such magnitude that they cause the beam to curve downwards and stick to the substrate. This resulted in a limited number of chips suitable for measurement.

Using a scanning electron microscope, cross-sections of polysilicon beams

were investigated, showing clearly a layer of silicon dioxide remaining between the beam and the substrate on wider beams, where it would ideally have been etched away completely (see figure 4.1). For for a particular polysilicon beam of 3 µm thickness the underetch was found to be 18.8 µm, for a particular 5 µm thick beam this was 16.2 µm, where at least 27 µm is necessary to completely release the widest beam of 54 µm width. The etching was performed using a vapour HF etch, so the difference in underetch between beams of 3 µm and 5 µm thickness is hard to justify. Investigation of the height-profile of beams on different chips showed beams up to a width of 38 µm were either all completely released, or at least eight released beams of the same length were found.

Of the polysilicon beams that were released successfully, some were observed to be stuck to the substrate below. The intrinsic stress in polysilicon causes a curvature towards the substrate, causing a sufficiently long beam to be able to actually touch the substrate and stick to it, as illustrated in figure 4.2.

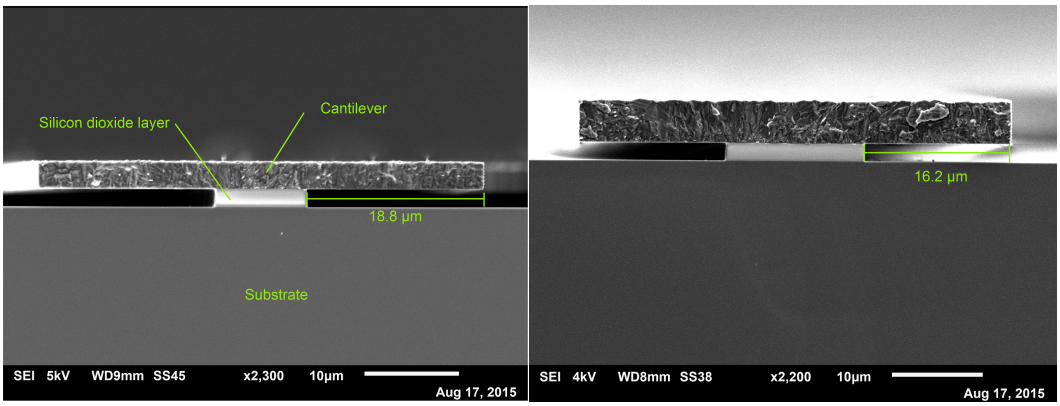
This was observed in the 3 µm thick undoped polysilicon beams 1000 µm in length. Beams 750 µm in length were sometimes observed to be stuck to the substrate, but enough freely suspended beams were found on each chip to obtain the desired eight measurements. Beams 500 µm in length were all free from the substrate.

The 5 µm thick beams of undoped polysilicon which were all freely suspended (unless not released in the vapour HF etch as described above). Very little curvature was observed in these beams, causing none to touch the substrate below. The beams on wafer #109, containing 3 µm thick doped polysilicon, were all observed to be stuck to the substrate, indicating a higher intrinsic stress causing a larger downward curvature.

The final wafer was supposed to contain doped polysilicon beams of 5 µm thickness, however fabrication of this wafer was unsuccessful and it yielded no usable test structures.

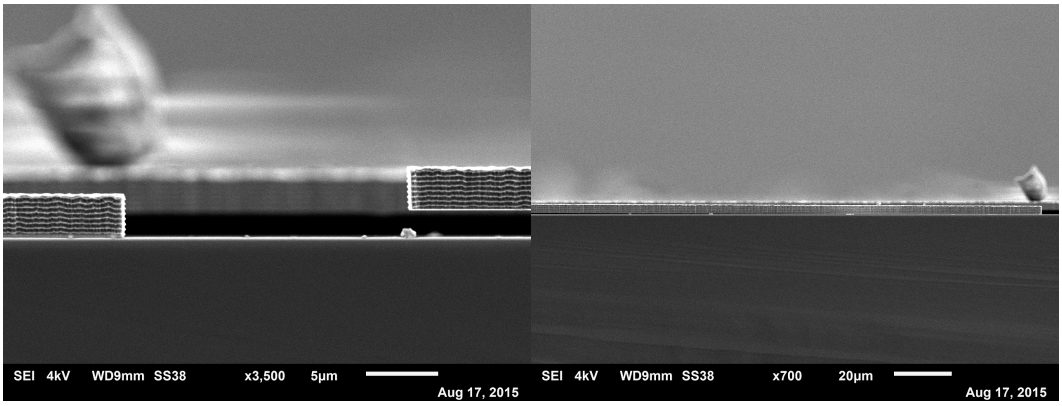
An overview of the status of the chips on each wafer is presented in figure 4.3.

The limited number of chips yielding useful results means measurements on polysilicon beams are limited to the wafer containing 3 µm thick beams of undoped polysilicon and the wafer containing 5 µm thick beams of undoped silicon up to a width of 38 µm for lengths of 500 µm and 750 µm. All other beams were either not released or suffered from stiction. In case of TriPleX beams, beams of 1000 µm were measured.



(a) **(b)**

Figure 4.1: Scanning electron microscope image of the cross-section of polysilicon beams not released from the substrate, showing the underetch of the silicon dioxide layer. For beams of 3 µm thick an underetch of 18.8 µm was found (a), while for beams of 5 µm thickness this is only 16.2 µm (b).



(a) **(b)**

Figure 4.2: Another phenomenon encountered in fabrication of the polysilicon beams: stiction. Most beams of 1000 µm in length were found to be stuck to the substrate, while doped polysilicon beams were all found to be stuck, indicating large bending stresses introduced by doping. (a) shows the endpoints of two beams opposite each other, one stuck to the substrate, the other still freely suspended. (b) shows the same beam on a different scale.

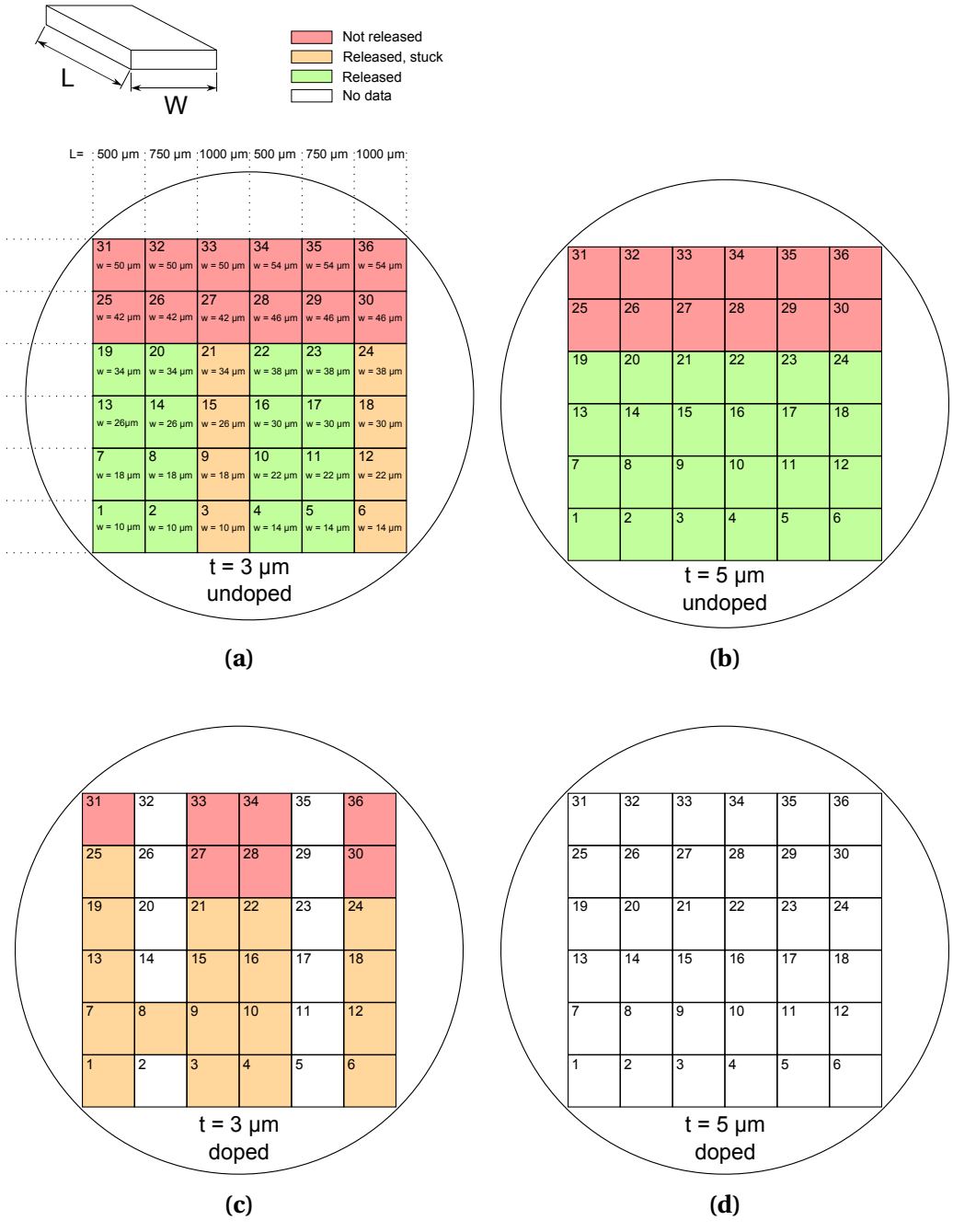


Figure 4.3: Overview of the status of polysilicon beams four wafers, showing chips with usable released beams in green. (a) top view of the wafer with undoped 3 µm thick polysilicon beams. (b) top view of the wafer with undoped 5 µm thick polysilicon beams. (c) top view of the wafer with doped 3 µm thick polysilicon beams. (d) top view of the wafer with doped 5 µm thick polysilicon beams, which yielded no usable data.

4.2 Results Measurements

4.2.1 TriPleX Beams

For each beam, TriPleX and polysilicon, the radius of curvature is determined, from which a theoretical stress is derived. This stress is the maximum of a hypothetical linear stress profile through the thickness of the beam, that would produce the measured radius of curvature, found on the top and bottom surface of the beam, as discussed in section 3.3. The results for the measurements of 1000 µm long TriPleX beams are shown in figure 4.4. The radius is shown in general to increase with increasing beam width, reaching a constant value of around 0.4 m at a width of 30 µm. The larger radius for lower beam width can be attributed to the effect of the stress near the beam's edges. Stress development near discontinuities is complex and not well-understood. It is possible that the edge-effects, that are dominant in slender beams, in combination with a low area of inertia produce smaller radii of curvature. In wider beams, these edge-effects are less dominant compared to the part of the beam away from the edges which behaves more like a perfect beam in plane-strain. Therefore it makes sense there is some maximum radius of curvature that is approached with increasing beam width. Similar conclusions were drawn by Hou et al. [31], who reported on the effect of beam width in bilayers (see section 2.3.4). Differences in width were observed to be of great influence on the endpoint deflection of the bilayer beams if the width of the beam was small compared to its length, yet in beams that were wide compared to their length, differences in width were of no real significance.

4.2.2 Polysilicon Beams

The measurements of the 3 µm thick undoped polysilicon beams show generally the same results as the TriPleX beams before: increasing width means increasing radius of curvature, as shown in figure 4.5. Both 500 µm as well as 750 µm long beams show roughly the same radius of curvature, except for widths of 30 µm and 38 µm where the radius decreases for beams 500 µm in length, yet increases for beams 750 µm in length. Since these measurements form the last two data points, there is no reason to believe this difference represents an actual opposite trend. Most likely the difference is to be attributed to measurement inaccuracies.

The results of the 5 µm thick undoped polysilicon beams show a significantly larger radius of curvature than the ones found in 3 µm thick beams, as shown in figure 4.6. The most likely conclusion to be drawn from this observation is that the increase in area moment of inertia between 3 µm and 5 µm thick polysilicon

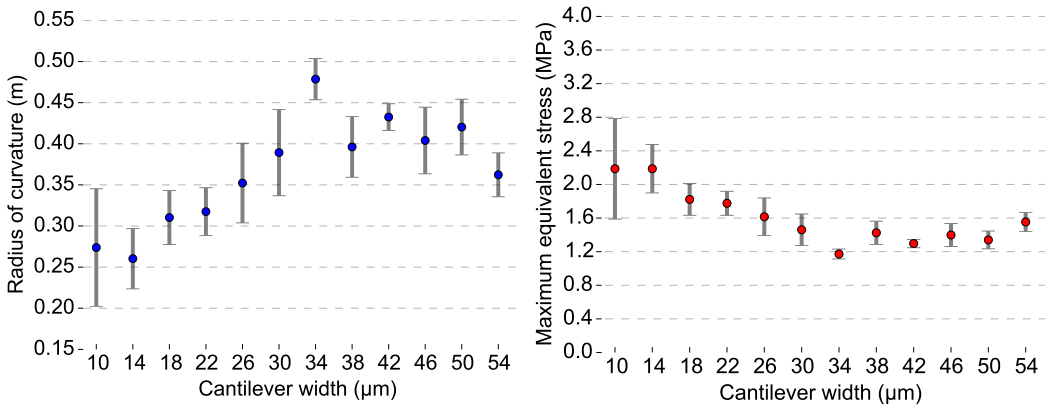


Figure 4.4: Measured radius of curvature of TriPleX beams of different widths (a) and the determined stress used to produce an equivalent curvature (b) for different beam widths. Shown are the average values along with standard deviation.

is not matched by the increase in intrinsic bending stress introduced into the added thickness during deposition. A strong increase in area moment of inertia, put against only a slight increase in bending stress, results in a larger radius of curvature.

The relatively large radius of curvature caused the spread in measurements to be relatively large, yet the same trend as before is observed: increasing beam width means increasing radius of curvature.

4.3 Verification of Measurement Results

The determined stress profile obtained from measured data presented in this section is used to complement a FEM model of a bimorph structure that has no initial "knowledge" of intrinsic stress present in its different material layers. Adding information on intrinsic stress will hopefully increase the accuracy of the results of FEM simulations, since it will provide a closer match to reality.

An initial verification of the validity of implementing the determined intrinsic stress would be to recreate the deformation observed in the measured beams. Since these beams are, for all present intents and purposes, single-material (TriPleX is of course a compound material, however this fact is not of interest in the present analysis of the problem), they provide a simple opportunity to verify the most basic intended purpose of implementing intrinsic stress into a FEM model.

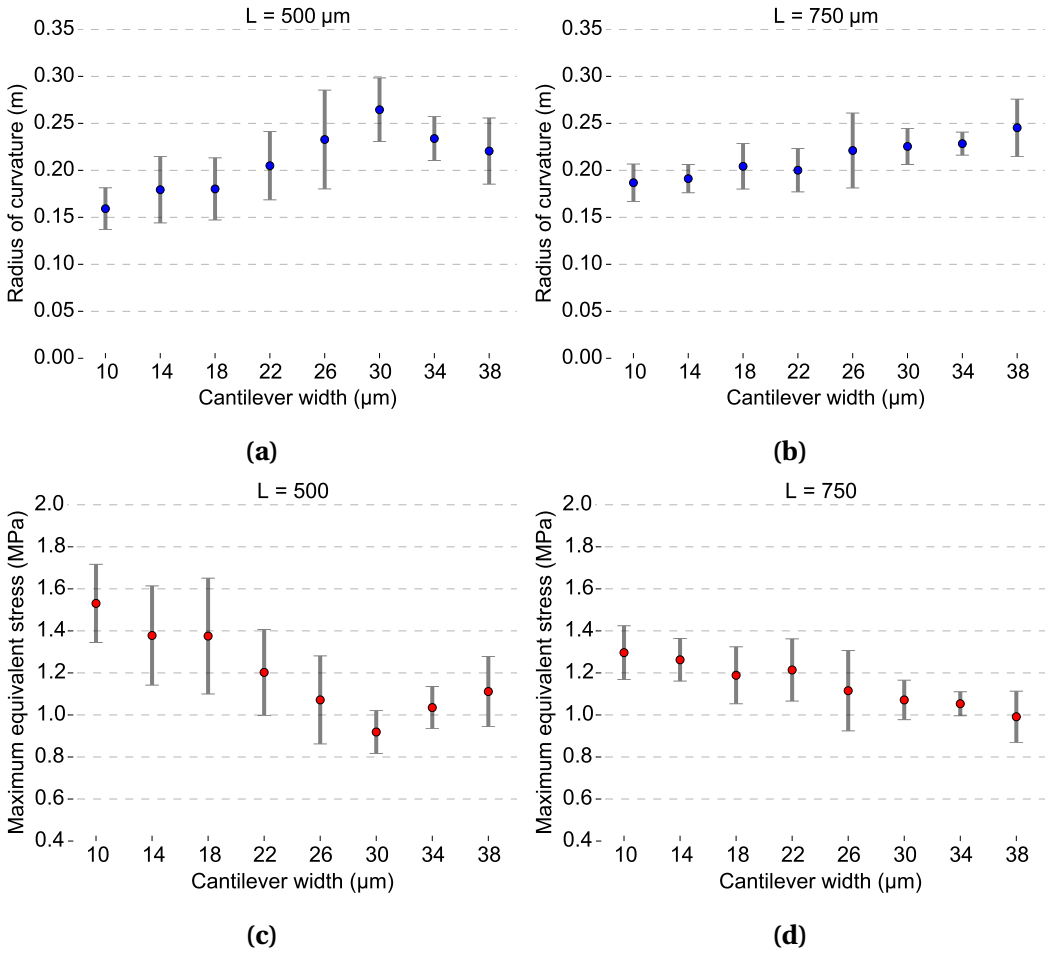


Figure 4.5: Measured radius of curvature of 3 µm thick polysilicon beams of increasing width for a length of 500 µm (a) and 750 µm (b), and the maximum determined stress used to produce an equivalent curvature ((c) and (d) respectively). Shown are the average values along with standard deviation.

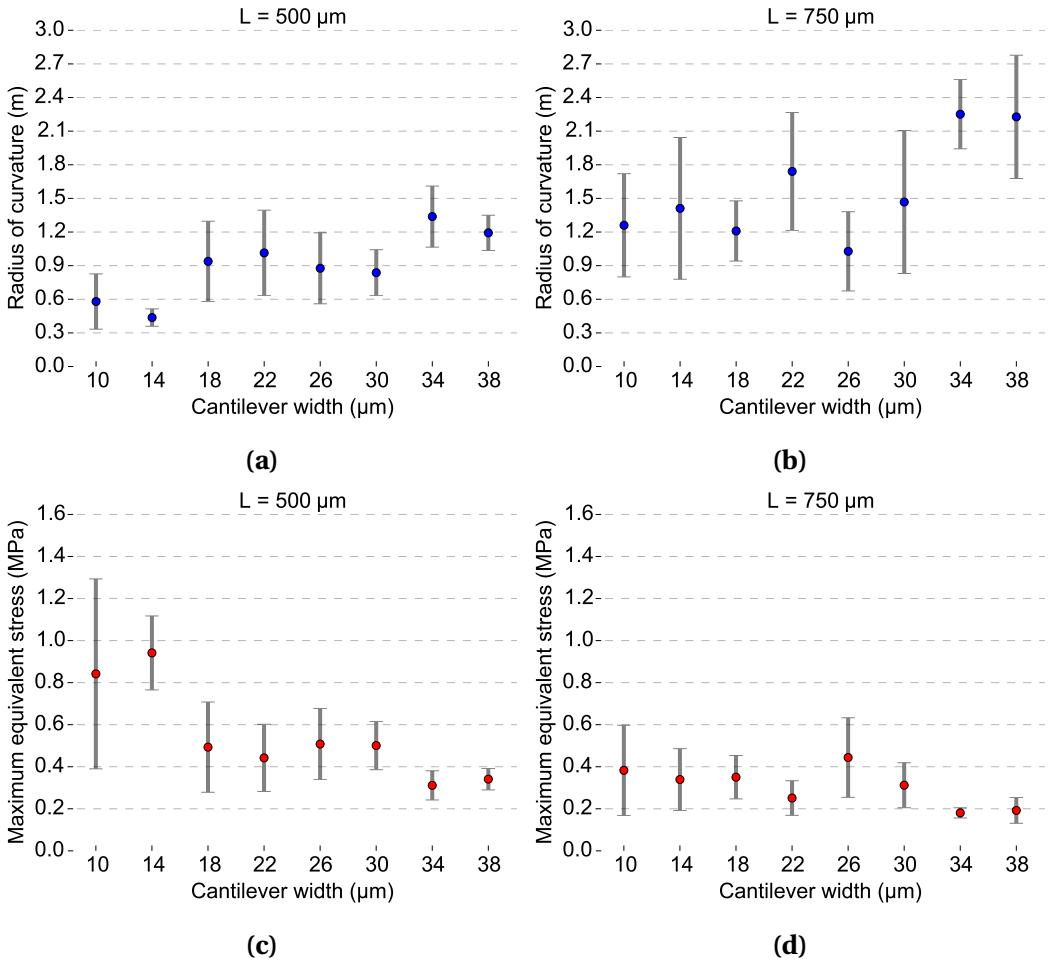


Figure 4.6: Measured radius of curvature of 5 µm thick polysilicon beams of increasing width for a length of 500 µm (a) and 750 µm (b), and the maximum determined stress used to produce an equivalent curvature ((c) and (d) respectively). Shown are the average values along with standard deviation.

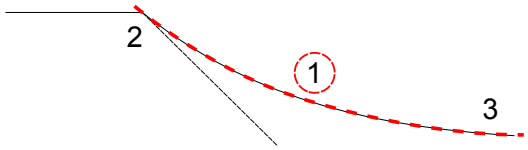


Figure 4.7: Schematic side view of a single beam indicating the aspect of its initial deformation that is discussed in section 4.3.1, which is the beam's radius of curvature.

As described in section 2, the deformation of a monolayer beam is comprised of two parts: firstly the curvature generated by the intrinsic stress profile throughout the beam's thickness, and secondly the initial slope of the beam generated at its anchor point by the thermal behavior of the beam material being bonded to the substrate during cooling down after processing. Both characteristic deformations will be analyzed from the realized beams and compared with the FEM results. Finally the combination of the two deformations determines the endpoint deflection of the beam, which is the ultimate goal of this thesis. Therefore the endpoint deflection will also be verified.

4.3.1 Verification of Radius

The most simple aspect to verify is the curvature generated by the intrinsic stress (see figure 4.7). The method that is used relies on measuring the curvature of a physical beam, deriving a hypothetical stress profile from this curvature and implementing that curvature into a FEM beam. Logically the curvature generated by the beam in the FEM environment should be the same as that of its physical counterpart.

For each type of beam that was measured, the measured curvature is compared to the curvature of an identical beam modelled in a FEM environment. The results of the comparison are presented in figure 4.8.

The curvature extracted from FEM analysis closely matches the measured curvatures for the 3 µm and the 5 µm thick undoped polysilicon beams, as well as for the TriPleX beams, all be it that the measured radius of curvature is slightly larger than determined from FEM analysis in all cases.

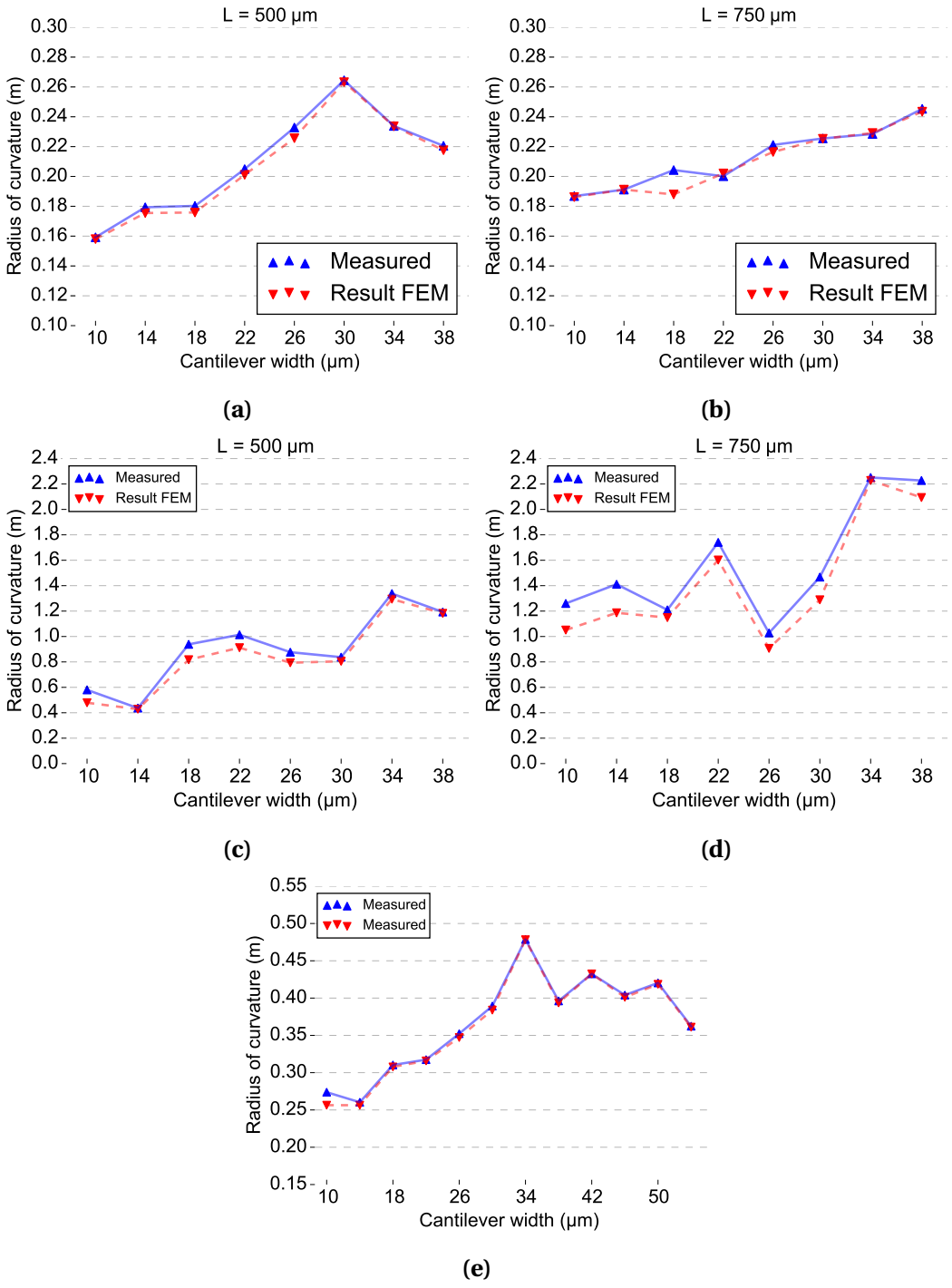


Figure 4.8: Comparison of radius obtained by FEM analysis with the radius that was measured for 3 µm thick polysilicon beams of 500 µm (a) and 750 µm in length (b), 5 µm thick polysilicon beams of 500 µm (c) and 750 µm in length (d) and TriPleX beams 1000 µm in length (e) for different beam widths.

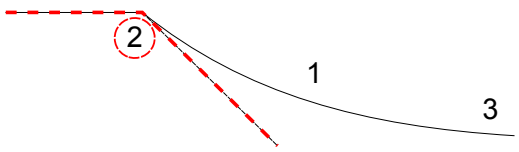


Figure 4.9: Schematic side view of a single beam indicating the aspect of its initial deformation that is discussed in section 4.3.2, which is the beam's initial slope.

4.3.2 Verification of Initial Slope

Besides the curvature, the initial slope of the beam is an important part of its deformation. Analogous to the comparison of the curvature in section 4.3.1, the initial slope of the physical beams is compared to the initial slope as determined in the FEM analysis (see figure 4.9). The results are presented in figure 4.10.

It is clear from figure 4.10 that the initial slope of the beam is more difficult to compare. Extracting the slope from the height-profile of the beam is to some extent an arbitrary process, since the angle is not clearly defined; it gradually increases over a length of roughly 50 µm. This is reflected in the more erratic behavior of the measured slope as the width of the beam increases. Remarkable is the trend that is visible for each type of polysilicon beam: a wider beam has a lower initial angle. TriPleX beam do not follow this trend, showing a relatively constant initial slope for each beam width. It is important to note that the TriPleX beams are 16 µm thick, where the polysilicon beams are 3 µm and 5 µm thick. At a thickness of 16 µm it might well be that the beam width is of no influence on the initial slope. This would imply a certain 'thickness-to-width ratio' exists for which the width is no longer a factor in the deformation at the anchor point of the beam.

The comparison also shows that the initial FEM analysis results do not agree with measured data. Even though for narrow beams its predictions are acceptable, for wider beams the results quickly diverge. This led to a new iteration of the representation of the anchor point of the beam, taking into account the underetching that would occur, which should offer more realistic results.

In the case of the TriPleX beams, the etch process causes a large underetch of the silicon at the anchor point creating an overhang, as illustrated in figure 4.11. This influences the initial slope of the beam itself immensely, increasing it to match the measured slope. The explanation for this effect lies in the fact that the overhang created by underetching acts as a bilayer itself, with the silicon dioxide based TriPleX on top and silicon underneath. As discussed before, the silicon contracts more than the oxide creating a downward curvature, which is

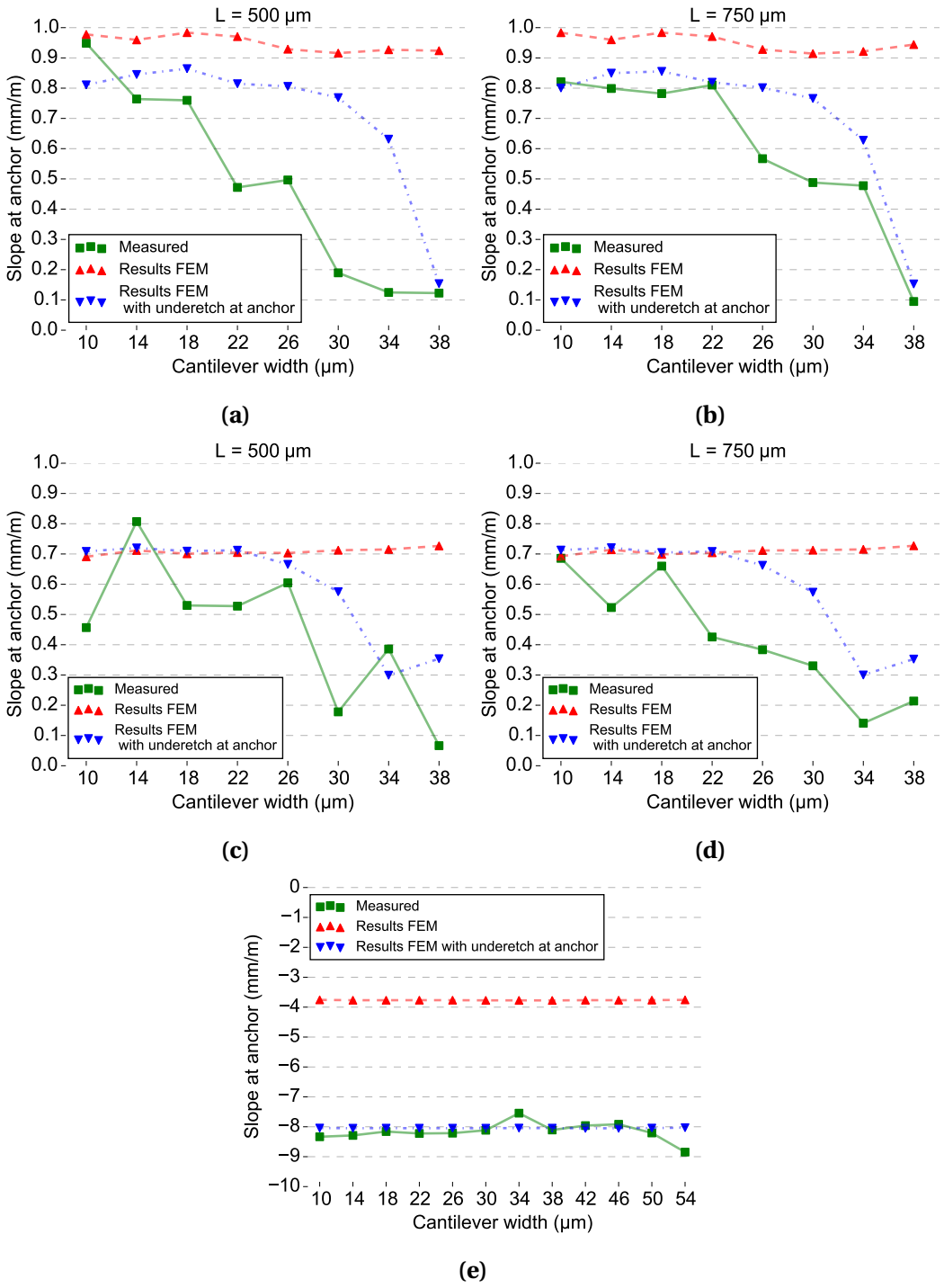


Figure 4.10: Comparison of the initial slope obtained by FEM analysis with the slope that was measured for 3 µm thick polysilicon beams of 500 µm (a) and 750 µm in length (b), 5 µm thick polysilicon beams of 500 µm (c) and 750 µm in length (d) and TriPleX beams 1000 µm in length (e).

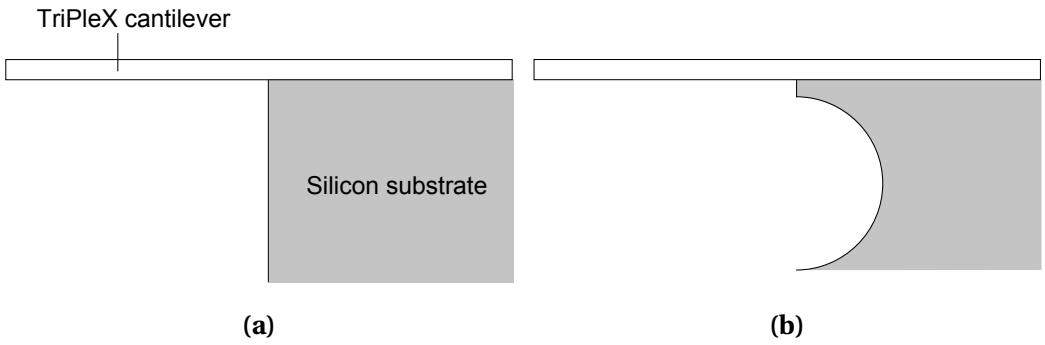


Figure 4.11: Schematic side view of a TriPleX beam showing the initial FEM representation of the beam's anchor point (a), and the modified anchor point taking into account underetching of the silicon substrate (b). The modified anchor point yields results that more closely resemble measured data.

responsible for the increased (negative) initial slope of the beam.

For the polysilicon beams, taking into account the underetch of the silicon dioxide layer that separates the polysilicon from the silicon substrate, as illustrated in figure 4.12, brought the initial slope closer to the measured data. Even though the exact values do not match, at least the trend of decreasing initial slope with increasing beam width is achieved. As explained previously, the initial slope is caused by the difference in CTE between the polysilicon layer and the oxide it is deposited on. On the interface the oxide 'restrains' the polysilicon, preventing it from contracting, while away from the interface the polysilicon can contract more freely. This means the free sidewalls of the polysilicon are slightly angled, causing the initial slope in the beam. Underetching of the oxide layer means there is less oxide to 'restrain' the polysilicon at the interface, leading to a decreased angle of the free sidewalls. This in turn decreases the initial slope of the beam.

4.3.3 Verification Endpoint Deflection

The main goal of this research is to predict the endpoint deflection of a bimorph waveguide, therefore the last verification is on the realized endpoint deflection (see figure 4.13). Again the measured endpoint deflection is compared to the endpoint deflection resulting from the FEM analysis. The result of this comparison is presented in figure 4.14.

The first thing to note about the measured endpoint deflection is the fact that, despite the curvature and initial slope varying for different beam widths, the endpoint deflection of each beam is relatively constant between different

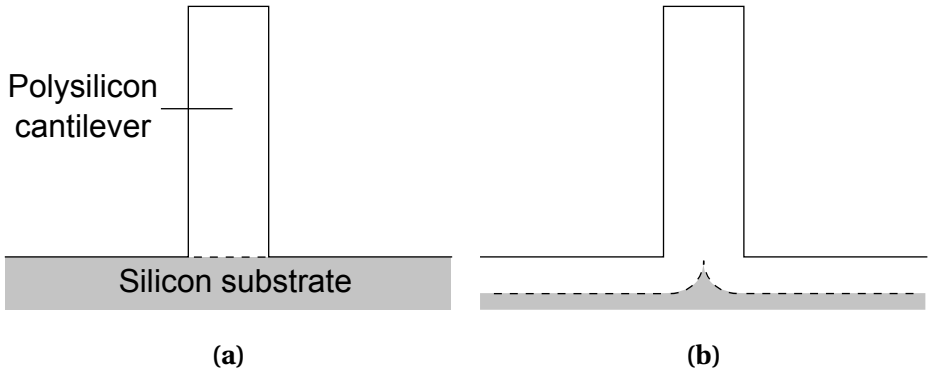


Figure 4.12: Schematic top view of a polysilicon beam showing the initial FEM representation of the beam's anchor point (a), and the modified anchor point taking into account underetching of the oxide layer that separates the polysilicon beam from the silicon substrate (b). The modified anchor point yields results that more closely resemble measured data.

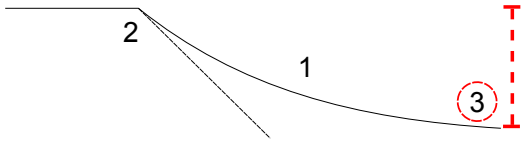


Figure 4.13: Schematic side view of a single beam indicating the aspect of its initial deformation that is discussed in section 4.3.3, which is the deflection at the beam's endpoint.

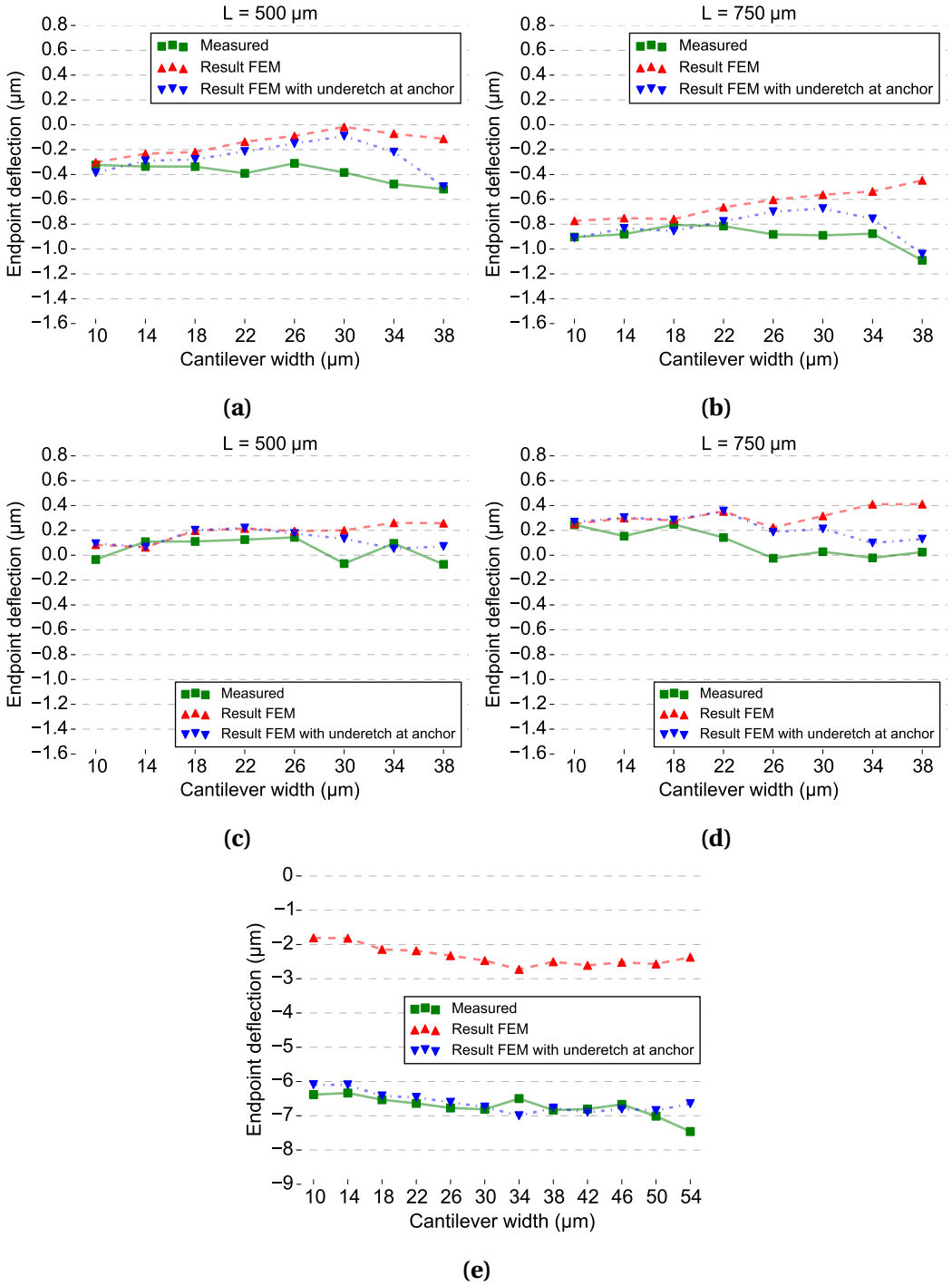


Figure 4.14: Comparison of the vertical endpoint deflection obtained by FEM analysis with the deflection that was measured for 3 µm thick polysilicon beams of 500 µm (a) and 750 µm in length (b), 5 µm thick polysilicon beams of 500 µm (c) and 750 µm in length (d) and TriPleX beams 1000 µm in length (e).

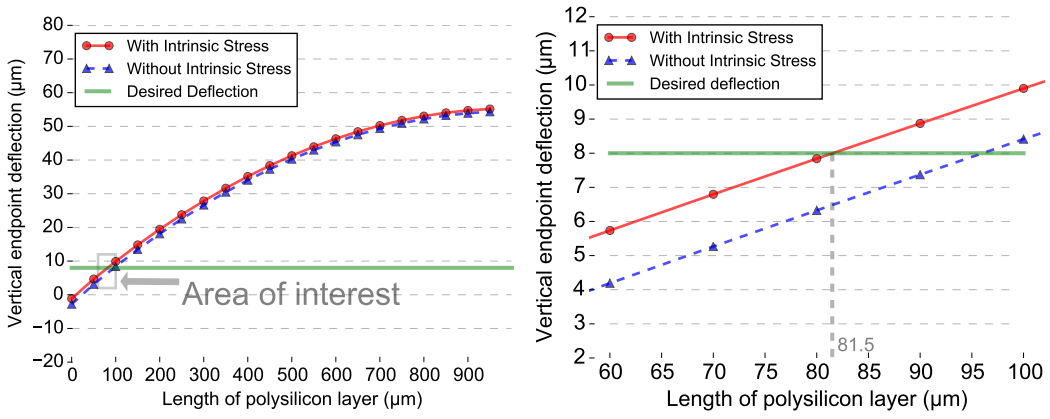


Figure 4.15: Vertical endpoint deflection of the bimorph waveguide for increasing length of the polysilicon layer on top, with and without the incorporation of the measured intrinsic stress (a). (b) shows a more detailed look at the area around the desired endpoint deflection. A length of the polysilicon layer of 81.5 µm is required to realize the desired initial endpoint deflection of 8 µm. The waveguide is 1000 µm in length and 18 µminwidth, while the polysilicon layer is 14 µm in width and 3 µm thick.

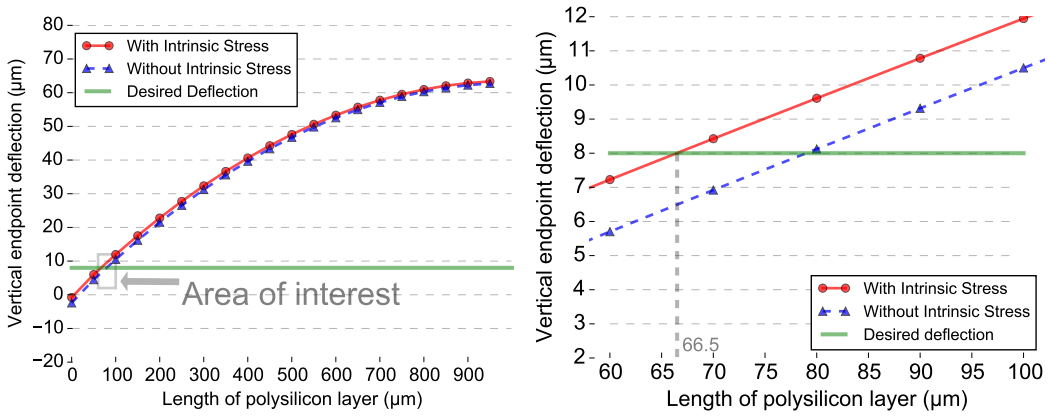
beam widths. The initial FEM analysis does not accurately follow the measured endpoint deflection, but modifying the anchor point to include the effect of underetching yields results matching the measurements more closely.

4.4 Results of Bimorph Beam Simulations

Having verified the validity of the determined intrinsic stresses for each material layer of the bimorph waveguide in a FEM analysis, the complete model can now be assessed. To determine the initial length of the polysilicon layer on top of the TriPleX waveguide needed to realize an initial endpoint deflection of 8 µm a simulation is run using a swept analysis increasing the length of polysilicon from 0 µm to the full length of the waveguide, which varies from 500 µm to 1000 µm, and determining the endpoint deflection for each configuration. This is done both with and without the added intrinsic stress to determine the magnitude of its effect. The results of this simulation are presented in figure 4.15 and 4.16.

The results indicate the required length of the polysilicon layer is 81.5 µm for a thickness of 3 µm and 66.5 µm for a thickness of 5 µm.

It is also shown that the addition of the intrinsic stress does alter the results



(a) **(b)**

Figure 4.16: Vertical endpoint deflection of the bimorph waveguide for increasing length of the polysilicon layer on top, with and without the incorporation of the measured intrinsic stress (a). (b) shows a more detailed look at the area around the desired endpoint deflection. A length of the polysilicon layer of 66.5 µm is required to realize the desired initial endpoint deflection of 8 µm. The waveguide is 1000 µm in length and 18 µm in width, while the polysilicon layer is 14 µm in width and 5 µm thick.

of the simulation, though it seems only a small amount. When inspecting the area around the desired endpoint deflection of 8 µm, it is clear that the effect of the addition of the intrinsic stress on the prediction of the endpoint deflection is roughly 1.5 µm which might be quite significant when dealing with sub micrometer alignment accuracy.

4.5 Verification of Simulation Results

Besides verifying the accuracy of a FEM model of a monolayer beam, as presented in previous sections, the accuracy of the model of the bimorph waveguide itself should also be verified. Due to budget and time constraints, the actual bimorph waveguide that was modelled could not be fabricated, making a direct verification impossible. However, similar structures have recently been fabricated that can be used to verify the models results to some extent.

Within the PHASTFlex project a new set of test structures have been fabricated using multiple actuation concepts to manipulate an array of four waveguides. One of the actuation features is the bimorph, six of which have been positioned on either side of the array of waveguides, twelve bimorph actuators in

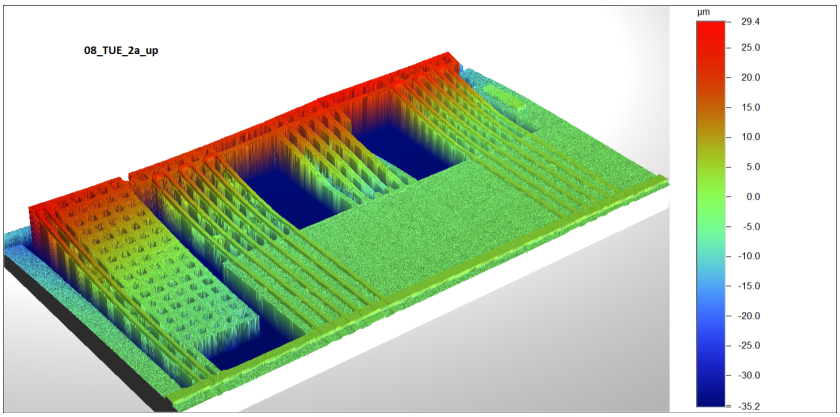
total. The bimorph actuators are fabricated with a layer of polysilicon along the entire length of the waveguide, as well as in a "short loop" configuration, where the polysilicon extends only a certain distance onto the TriPleX beam, as can be seen in figure 4.17.

The main issue is the fact that the FEM analysis performed in this thesis only concerns a single bimorph actuator, while the newly fabricated structures deal with arrays of bimorph actuators connected to an array of waveguides and different actuators. Structures were selected that showed fractures in the cross-beam connecting the bimorph actuators to the array of waveguides and the other actuators, to eliminate as much influence of these structures on the deformation of the bimorph actuator itself. Still it was not possible to ensure these structures were completely decoupled, making it difficult to draw any solid conclusions from a comparison between the two.

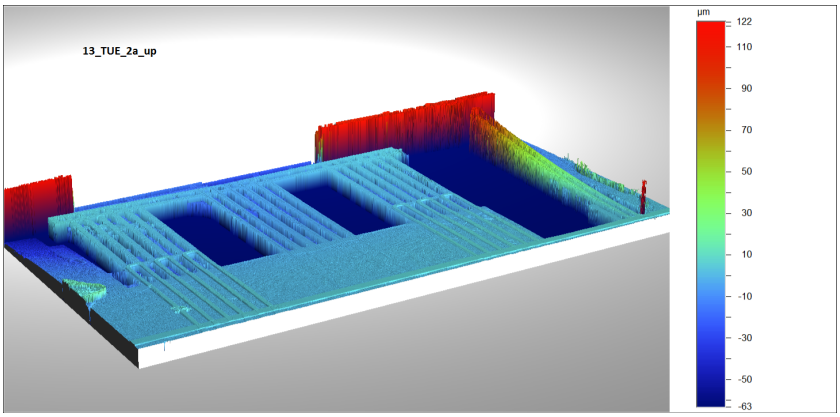
Figure 4.18 shows a comparison between the measured height profile of a bimorph beam 1000 µm in length with polysilicon along its entire length and simulation results. At first glance the profiles seem to match reasonably well: the difference in endpoint deflection between the measured profile and the profile obtained by FEM simulation with addition of intrinsic stress is 3.56 µm. However, since the desired endpoint deflection of the bimorph waveguide is only 8 µm, this is a significant error. It must be mentioned that the model is not an accurate representation of the measured structure. Furthermore, the measured height profile needed to be filtered to remove large spikes, as well as tilted to ensure the wafer surface was parallel to the horizontal axis in order to be able to compare the profile to the FEM results. These factors contribute to the difference between measured data and simulated results. The simulation results do approach the measured profile slightly better when the intrinsic stress is included. Furthermore, it is interesting to note that the simulation results diverge from the measured data when taking into account underetching at the anchor point. In previous analyses modification of the anchor point yielded results that were more in concurrence with measurements.

Figure 4.19 shows a comparison between the measured height profile of a bimorph beam 525 µm in length with the 'short-loop' polysilicon layer extending 200 µm along its length and simulation results. Again, the profiles seem to match reasonably well: the difference in endpoint deflection between the measured profile and the profile obtained by FEM simulation with addition of intrinsic stress is 1.45 µm. However, since this waveguide is significantly shorter than the one shown in figure 4.18, this is still a significant error. The simulation results approach the measured profile better when the intrinsic stress is included,

the simulation results diverge from the measured data when taking into account underetching at the anchor point.



(a)



(b)

Figure 4.17: Interferometer height-map of the latest PHASTFlex test structures, illustrating the concept of using two arrays of six bimorph beams on each side of an array of four waveguides in combination with a u-beam actuator to realize displacement of the array of waveguides in two directions. (a) shows the concept using bimorph actuators with polysilicon along the entire length of the beam, while (b) illustrates the short loop concept of only extending the polysilicon a short distance along the beam (K. Wu, kai.wu@tudelft.nl).

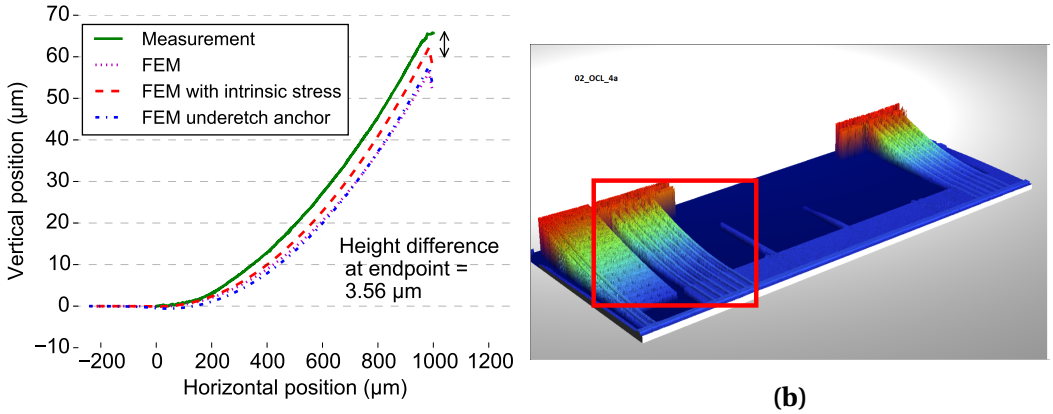


Figure 4.18: Measured bimorph beam profile compared to FEM predictions for a bimorph beam 1000 µm in length with polysilicon along its entire length. FEM analysis was done without the addition of intrinsic stress, with the addition of intrinsic stress, and with both the addition of the intrinsic stress and the effect of underetching at the anchor point (a). (b) shows the height map of the entire structure, indicating the measured beam with a red rectangle (K. Wu, kai.wu@tudelft.nl).

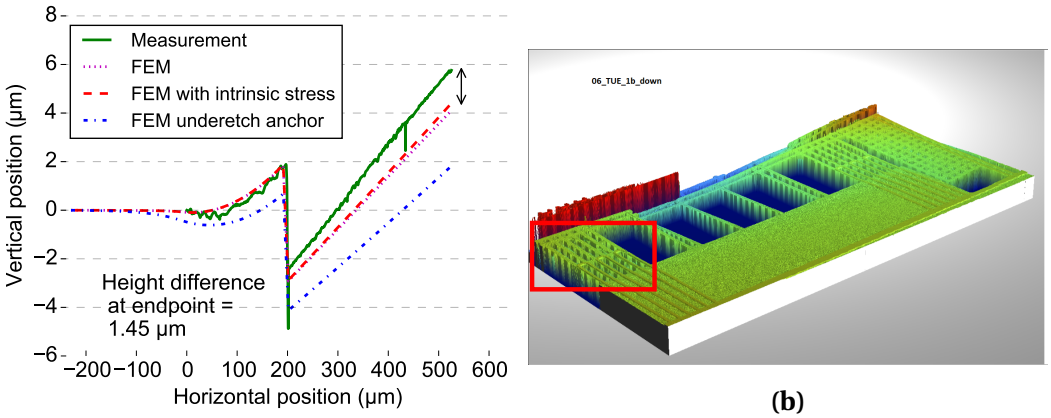


Figure 4.19: Measured bimorph beam profile compared to FEM predictions for a bimorph beam 525 µm in length with the 'short-loop' polysilicon layer extending 200 µm along its length. FEM analysis was done without the addition of intrinsic stress, with the addition of intrinsic stress, and with both the addition of the intrinsic stress and the effect of underetching at the anchor point (a) (Note the step in the profiles due to the height of the polysilicon layer). (b) shows the height map of the entire structure, indicating the measured beam with a red rectangle (K. Wu, kai.wu@tudelft.nl).

Chapter 5

Conclusions and recommendations

This thesis has presented a method of simulating the initial deformation of micromachined bimorph beams as a result of residual stress that is introduced into the different material layers during processing. Both the intrinsic and the thermal stress that make up the residual stress have been investigated for the two materials that make up the bimorph; TriPleX and polysilicon. The basis of this simulation is a finite element model built using COMSOL Multiphysics Modeling Software. Since the finite element method is only capable of simulating the thermal part of the residual stress, experiments were designed to measure the intrinsic stress in the TriPleX and polysilicon layers separately in the form of an 'equivalent stress', not designed to accurately represent the intrinsic stress distribution within the beam material; it aims just to reproduce the initial deformation the intrinsic stress generates. Measurements were performed on TriPleX and polysilicon beams of different dimensions, emphasizing the effect of beam width on the initial deformation. The obtained equivalent stress has been incorporated into the finite element model to improve the accuracy of the simulation results.

Verification of the simulation results of TriPleX and polysilicon monolayer beams have shown that the method of 'equivalent stress' is a valid way of including the influence of intrinsic stress on the initial deformation of these beams. The initial slope of the beam at its anchor point, its radius and the vertical deflection of its endpoint obtained through simulation shown general agreement with measurements. Results for narrow beams seem to match better than results for wider beams.

The representation of the anchor point of the bimorph beam has proven to be a key element in simulating the initial deformation of a beam. Taking into

account the effect of underetching of supporting layers on the geometry of the anchor point improves simulation results, especially for wider beams. Refining the modelled geometry in this area reduced the average initial slope of a polysilicon beam with a length of 500 µm, a thickness of 3 µm and a width of 38 µm from roughly 0.91 mm/m to 0.15 mm/m, the measured slope being 0.12 mm/m. For beams of different length and thickness similar improvements in simulation accuracy are observed. The simulation results for more narrow beams already showed greater concurrence with measured data, therefore modifying the anchor point did not change the simulation accuracy as drastically. The average initial slope of a polysilicon beam with a length of 750 µm, a thickness of 3 µm and a width of 10 µm was reduced from roughly 0.98 mm/m to 0.81 mm/m, the measured slope being 0.82 mm/m.

Incorporating the 'equivalent stress' into the finite element model has a significant effect on simulation results of the bimorph beam. Verification of these results using measurements of deformations of realized structures that incorporated multiple bimorph beams has shown the predicted deformations match the measurements quite well. However, for one bimorph beam 1000 µm in length the difference in the vertical deflection of the endpoint between simulated results and the measured profile is 3.56 µm. The same comparison for a bimorph beam 525 µm in length yielded a difference of 1.45 µm. Comparing these values to the desired vertical endpoint deflection of 8 µm, it is clear that he simulation results at this point are not accurate enough to make predictions on the exact specifications necessary to achieve the desired initial deformation.

Accurate geometrical representation of the bimorph beam's anchor point was found to be difficult to achieve, yet its influence on the initial deformation is relatively large. A more in-depth investigation of the factors that influence the geometry of the anchor point, such as underetching of supporting layers, could lead to improved accuracy of simulation results. This is especially true for TriPleX beams due to the complexity of the method used to release the beams from the substrate.

More extensively documenting the effect of the dimensions of a beam on its initial deformation might yield an empirical way of predicting the intrinsic stress in a beam of arbitrary dimensions, varying more than just the width of the beam.

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Appendix A

Thermal Conductiviy of Silicon at Increasing Temperature

Table A.1: Average value, standard deviation and scatter for the thermal conductivity of silicon at increasing temperature as provided by Yamasue et al.[37]

Temperature (K)	Average value (W m/K)	Standard Deviation (W m/K)	Scatter (%)
293	139.4	1.4	1.0
373	105.8	2.4	2.2
473	82.4	0.9	1.0
573	65.6	1.8	2.8
673	50.3	1.1	2.1
773	42.4	1.4	3.3
873	36.7	0.5	1.4
973	30.9	0.8	2.6
1073	27.4	0.7	2.5
1173	24.8	1.1	4.6
1273	23.7	0.5	1.9
1373	22.3	1.2	5.4
1473	20.1	0.8	3.8
1573	20.4	0.5	2.5
1673	19.0	0.9	4.7

Appendix B

Fabrication Flowcharts

PROCESS FLOW FOR FLEXIBLE TRIPLEX WAVEGUIDES FOR CURVATURE MEASUREMENTS

Tim Nooren

(April 29, 2015)

DIMES PROCESS NUMBER WB1993

General rules

Cleanroom behaviour

- Always follow the **'Security and Behaviour'** rules when working in the Dimes cleanrooms.
- Always handle wafers with care during processing. Use cleanroom gloves and work as clean as possible !!
- Always check equipment and process conditions before starting a process. Do NOT make unauthorized changes !
- Directly notify the responsible staff member(s) when there are problems with equipment (like malfunction or contamination). Always leave a note on the equipment to warn other users.
- Do not try to repair or clean equipment yourself, and never try to refresh a contaminated etch or cleaning bath! Only authorized staff members are allowed to do this.

Cleaning of wafers

After several hours of storage, wafers must always be cleaned before performing a *coating*, *furnace*, *epitaxy* or *deposition* step. Use the correct cleaning procedure:

- Acetone or Tepla stripper ⇒ for photoresist removal (Use Tepla for implanted or plasma etched resist)
- HNO_3 99% (Si) ⇒ for wafers which do not need a HNO_3 69.5% step
- HNO_3 99% ('green' metals) ⇒ for wafers which are or have been in contact with a 'green' metal layer
- HNO_3 99% (Si) + HNO_3 69.5% (Si) ⇒ for all other wafers

Wafers do not have to be cleaned after a furnace, epitaxy or deposition step if the next process step will be performed immediately (unless the wafers are covered with particles).

Furnace restrictions

Wafers that are covered with photoresist or a metal layer may NEVER be processed in any of the furnaces. This also applies to wafers from which a metal layer has been removed by etching. Only alloying in tube C4 is allowed for wafers with an aluminium layer.

Measurements

Always perform all the measurement and inspection steps, and **write down the results in your journal and in the result tables that can be found at some of the equipment** !! The results are used to check the condition of processes and/or equipment. It is allowed to use the following equipment to perform measurements directly onto your process wafers:

- The Leitz MPV-SP, the WOOLLAM and the SAGAX. These systems are used for thickness measurements of transparent layers. The measurements are non-destructive and without contact to the wafer surface.
- The Dektak 8 surface profilometer. This system is used for step height measurements. In this case a needle will physically scan over the wafer surface (contact measurement), which can be destructive for structures.
- The XL50 SEM. It can be used for inspection of your wafers and for width, depth or thickness measurements.

! Note that after certain (mainly contact) measurements cleaning of wafers may be required for further processing.

An extra wafer must be processed when other measurement methods will be used (like sheet resistance and junction depth measurements). These wafers can not be used for further processing.

PAC rules

- All substrates, layers and chemicals which are not standard being used in the Dimes 01/02/03/04 or Dimos 01 production processes are considered to be "NON-STANDARD" materials, and may be contaminating.
- The use of "non-standard" materials for processing in the class100 and SAL cleanroom must ALWAYS BE EVALUATED AND APPROVED by the Process Approval Committee. It is strictly forbidden to use these materials without permission.
- Wafers that are contaminated may NEVER be processed in any of the equipment without permission of the PAC committee. Special precautions may have to be taken, like the use of a special substrate holder or container.
- Check the PAC 'Rules & Instructions' - available on the internet - for more details.

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Starting Material

Use single side polished wafers with the following specifications:

Type:	p-type
Orientation:	{100}
Resistivity:	31
Thickness:	525 ± 2 µm
Diameter:	100.0 ± 0.2 mm

Deposit TriPleX stack

Processing is done by LioniX.
Layer stack on frontside:

- Bottom cladding layer: thermal oxide, thickness = 8 µm
- Waveguide core: silicon nitride, thickness = 200 nm
- Top cladding: PECVD oxide, thickness = 8 µm

Stack on backside of wafer is either similar to frontside or without the (complete) top cladding layer. We'll find out by measuring.
Zero layer alignment markers for contact aligner (FWAMs) are patterned in the silicon nitride layer!

Cleaning of wafers from outside Dimes

1 Cleaning in MEMS lab: HNO_3 100% and 65%

Cleaning	10 minutes in fuming nitric acid (Merck: HNO_3 100% selectipur) at ambient temperature. This will dissolve organic materials. Fill the container with HNO_3 100%
Rinse	Rinse in DI water
Cleaning	10 minutes in concentrated nitric acid (Merck: HNO_3 65% selectipur) at 110 °C. This will dissolve metal particles. Fill the container with HNO_3 65%.
Rinse	Rinse in DI water
Drying	Use the dry-spinner.

2 Enter Class 100 Cleanroom

Change waferbox to a standard Dimes black box.

3 Cleaning Procedure: HNO_3 100% and 65%

Cleaning	10 minutes in fuming nitric acid (Merck: HNO_3 100% selectipur) at ambient temperature. This will dissolve organic materials. Use wet bench 'HNO_3 (100%)' and the carrier with the red dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Cleaning	10 minutes in concentrated nitric acid (Merck: HNO_3 65% selectipur) at 110 °C. This will dissolve metal particles. Use wet bench 'HNO_3 (65%)' and the carrier with the red dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the Semitool 'rinser/dryer' with the standard program, and the white carrier with a red dot.

4 Measurement: curvature

Use Tencor Flexus instrument to measure the curvature of the wafer. If a previous measurement is available, the stress can be determined.
This is a reference measurement.

5 Measurement: thickness (frontside and backside)

Use the Leitz MPV-SP measurement system to measure the oxide thickness on the *frontside* of Lionix wafers:
Program: Th. Sio2 on Si >50 nm auto5pts
Expected oxide thickness: 16 µm

Use the Leitz MPV-SP measurement system to measure the oxide thickness on the *backside* of Lionix wafers:
Program: Th. Sio2 on Si >50 nm auto5pts
Expected oxide thickness: in the range of 8 µm to 16 µm

Pattern and release waveguide beams @ frontside

6 Spincoat (frontside)

On top of the spraycoated resist, spincoat a layer of AZ9260. Thickness: ~8 µm
Use the EVG120 system to coat the wafers with photoresist, and follow the instructions specified for this equipment.
The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with AZ9260 positive resist, and a soft bake at 95 °C for 90 seconds. The resist is dispensed with a pump. Always check the relative humidity (48 ± 2 %) in the room before coating.

Use coating program **...** on the coating system (resist thickness: ... µm at 48% RH).
After coating, check on the back part of the wafers that there are no resist residues. If there are, clean them with a cotton bud and acetone.
! Wait at least 30 minutes after coating for dehydration before exposure!

7 Alignment and exposure (frontside)

Processing will be performed on ELVIS / EVG420 contact aligner.
Follow the operating instructions from the manual when using this machine.

Expose mask 'WB1839_V4 OX' (located in box 464) using an exposure energy of ... mJ. This is achieved with a duration of ... seconds.
! Wait at least 30 minutes after coating for dehydration before exposure!

8 Developing

Manual developing of photoresist. Use 1 part of AZ400K diluted with 2 parts of DI water. For development time: start with 1 min 30 sec. Depending of the result (optical inspection) another 30 sec.

9 Inspection: Linewidth and overlay

Visually inspect the wafers through a microscope, and check the linewidth and overlay. No resist residues are allowed.

10 Etch Oxide (16 µm, stop on Silicon)

Drytek Triode for RIE
Recipe: StdOxide
Etchrate SiO_2: 500 nm/min
Etchrate AZ9260: 145 nm/min

Drytek Triode T384 etch parameters. Recipe: **'StdOxide'**

Step	**Gasses & flows**	**Pressure**	**RF power**	**He pressure**	**Etch time**
1. Oxide (RIE)	C_2F_6 @ 36 sccm CHF_3 @ 144 sccm	180 mTorr	300 W	12 Torr	~ 32 min

Etch Silicon @ frontside

11 Etch Silicon anisotropically (60 µm)

Use the SPTS Rapier Omega i2L plasma etcher. Follow the operating instructions from the manual when using this machine.
The process conditions of the etch and passivation program may not be changed!
Use recipe 'DTC_Smooth_20C' to anisotropically etch the pattern into the silicon.
Etch rate: ~ 6 µm/min.
Etching 60 µm of Si requires around 300 loops.

SPTS Rapier Omega i2L etch parameters. Recipe: **'DTC_Smooth_20C'**

Step	**Gasses & flows**	**Pressure**	**Source 1 Power**	**Source 2 power**	**Platen HF power**	**Process time**
1. Strike	Ar @ 300 sccm	40 mTorr	2500 W	500 W	0 W	2.0 s
	C_4F_8 @ 220 sccm					
2. Depo	C_4F_8 @ 220 sccm	40 mTorr	2500 W	500 W	0 W	1.2 s
3. Etch_1a	SF_6 @ 400 sccm	30 mTorr	2500 W	500 W	175 W	1.0 s
4. Etch_1b	SF_6 @ 400 sccm	30 mTorr	2500 W	500 W	60 W	2.5 s

12 Deposit passivation layer and locally remove it

Use the SPTS Rapier Omega i2L plasma etcher. Follow the operating instructions from the manual when using this machine.
The process conditions of the etch and passivation program may not be changed!
Use recipe 'DTC_Depo_And_Pasiv_Etch' to deposit and subsequently locally remove the passivation layer.

SPTS Rapier Omega i2L etch parameters. Recipe: **'DTC_Depo_And_Pasiv_Etch'**

Step	**Gasses & flows**	**Pressure**	**Source 1 Power**	**Source 2 power**	**Platen HF power**	**Process time**
1. Strike	Ar @ 300 sccm	40 mTorr	2500 W	500 W	0 W	2.0 s
	C_4F_8 @ 220 sccm					
2. d1	C_4F_8 @ 220 sccm	40 mTorr	2500 W	500 W	0 W	400.0 s
3. E1	SF_6 @ 350 sccm	25 mTorr	2500 W	0 W	75 W	100.0 s

Etch silicon @ frontside

13 Etch Silicon isotropically (35 µm): release

Use the SPTS Rapier Omega i2L plasma etcher. Follow the operating instructions from the manual when using this machine.
The process conditions of the etch and passivation program may not be changed!
Use recipe 'DTC_IsoEtch_PS_01' to isotropically etch the silicon.
Etch rate: ~ 7 µm/min.

SPTS Rapier Omega i2L etch parameters. Recipe: **'DTC_IsoEtch_PS_01'**

Step	**Gasses & flows**	**Pressure**	**Source 1 Power**	**Source 2 power**	**Platen HF power**	**Process time**
1. Strike1	Ar @ 250 sccm	50 mTorr	2500 W	0 W	0 W	5.0 s
	C_4F_8 @ 1 sccm					
2. Strike2	Ar @ 250 sccm	75 mTorr	2500 W	0 W	0 W	5.0 s
	C_4F_8 @ 250 sccm					
3. IsoEtch1	SF_6 @ 500 sccm	100 mTorr	2500 W	0 W	0 W	300.0 s

14 Strip photoresist and passivation layer using Tepla

Strip resist — Use the Tepla plasma system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use **'program . . . '**: 1000 W power and 30 min etching.

15 Etch Silicon isotropically (35 µm): remove supporting Silicon

Use the SPTS Rapier Omega i2L plasma etcher. Follow the operating instructions from the manual when using this machine.
The process conditions of the etch and passivation program may not be changed!
Use recipe 'DTC_IsoEtch_PS_01' to isotropically etch the silicon.
! Put process wafer on top of a carrier wafer to prevent etching into the chuck.
Etch rate: ~ 7 µm/min.

SPTS Rapier Omega i2L etch parameters. Recipe: **'DTC_IsoEtch_PS_01'**

Step	**Gasses & flows**	**Pressure**	**Source 1 Power**	**Source 2 power**	**Platen HF power**	**Process time**
1. Strike1	Ar @ 250 sccm C_4F_8 @ 1 sccm	50 mTorr	2500 W	0 W	0 W	5.0 s
2. Strike2	Ar @ 250 sccm C_4F_8 @ 250 sccm	75 mTorr	2500 W	0 W	0 W	5.0 s
3. IsoEtch1	SF_6 @ 500 sccm	100 mTorr	2500 W	0 W	0 W	250.0 s

Finished

16 Inspection with SEM

Inspect the end-result using the SEM.

Tim Nooren
(April 29, 2015)

DIMES PROCESS NUMBER WB1993

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- HNO_3 99% (Si) ⇒ for wafers which do not need a HNO_3 69.5% step
- HNO_3 99% ('green' metals) ⇒ for wafers which are or have been in contact with a 'green' metal layer
- HNO_3 99% (Si) + HNO_3 69.5% (Si) ⇒ for all other wafers

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- The Dektak 8 surface profilometer. This system is used for step height measurements. In this case a needle will physically scan over the wafer surface (contact measurement), which can be destructive for structures.
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- Check the PAC 'Rules & Instructions' - available on the internet - for more details.

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16 Inspection with SEM . . . 7

Starting Material

Use single side polished wafers with the following specifications:

Type:	p-type
Number of wafers:	4
Orientation:	{100}
Thickness:	525 ± 2 µm
Diameter:	100.0 ± 0.2 mm

Measurements before processing

1 Measurement: curvature

Use Tencor Flexus instrument to measure the curvature of the wafer. If a previous measurement is available, the stress can be determined.
This is a reference measurement.

Grow 2 µm silicon oxide

Use Tempress furnace C1.
Recipe: 'wetox'. Duration: 8 hours 16 minutes. Temperature: 1100 °C. This grows 2 µm of silicon oxide.

Deposit poly-Si @ frontside

2 LPCVD of poly-Si: seedlayer

Tempress LPCVD tube E3 poly, recipe: LPolyBin.
Duration: 1 h. Expected thickness: 130 nm.

3 Remove LPCVD poly-Si from backside

Trikon Omega 201 plasma etcher.
Follow the operating instructions from the manual when using this machine. The process parameters of the etch program may not be changed. Recipe: 'Leon_1'. Duration: 1 min 00.

4 Cleaning Procedure: HNO_3 100% and 65%

Cleaning	10 minutes in fuming nitric acid (Merck: HNO_3 100% selectipur) at ambient temperature. This will dissolve organic materials. Use wet bench 'HNO_3 (100%)' and the carrier with the red dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Cleaning	10 minutes in concentrated nitric acid (Merck: HNO_3 65% selectipur) at 110 °C. This will dissolve metal particles. Use wet bench 'HNO_3 (65%)' and the carrier with the red dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the Semitool 'rinser/dryer' with the standard program, and the white carrier with a red dot.

5 Remove native oxide from poly-Si

! Perform this step right before starting the epitaxy. After waiting for too long, native oxide will reappear.

Etching	4 minutes in 0.55 % HF solution (Merck: HF 0.55 % VLSI selectipur) at ambient temperature. Use wet bench 'HF (0.55 %)' and the carrier with the black dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the Semitool 'rinser/dryer' with the standard program, and the orange carrier with a red dot.

6 Epitaxy of 3 µm or 5 µm thick poly-Si

Use ASMI Epsilon One

	Thickness	Target sheet resistance
Wafer 1:	3 µm	undoped
Wafer 2:	3 µm	30 Ω/□
Wafer 3:	5 µm	undoped
Wafer 4:	5 µm	30 Ω/□

Pattern poly-Si @ frontside

7 Coating (frontside)

Use the EVG120 system to coat the wafers with photoresist, and follow the instructions specified for this equipment.
The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with Shipley SPR3027 positive resist, and a soft bake at 95 °C for 90 seconds. The resist is dispensed with a pump. Always check the relative humidity (48 ± 2 %) in the room before coating.

Use coating program **'Co-edg-3027-4.0um'** on the coating system (resist thickness: 3.1 µm at 48% RH).
After coating, check on the back part of the wafers that there are no resist residues. If there are, clean them with a cotton bud and acetone.

8 Alignment and exposure (frontside)

Processing will be performed on ELVIS / EVG420 contact aligner.
Follow the operating instructions from the manual when using this machine.

Expose mask 'WB1839_V4 OX' (located in box 464) using an exposure energy of ... mW. This is achieved with a duration of ... seconds. Check table!

9 Developing

The wafers are developed by a combination of EVG120 processes and manual development.
When using the EVG120 system, follow the instructions specified for this equipment.

(i) Use program 'Dev_PEB' on the developer station. This performs a post-exposure bake at 115 °C for 90 seconds.

(ii) Manually develop in MF322. Duration: 1 min

(iii) Rinse thoroughly with DI water

(iv) Use program 'Dev_HB' on the developer station. This performs a hard bake at 100 °C for 90 seconds.

10 Inspection: Linewidth and overlay

Visually inspect the wafers through a microscope, and check the linewidth and overlay. No resist residues are allowed.

11 Etch poly-Si

Use the Trikon Omega 201 plasma etcher.
Follow the operating instructions from the manual when using this machine.
The process parameters of the etch program may not be changed!

Use recipe 'Poly3000'

! Include several dummy wafers for tests!

12 Strip photoresist using Tepla

Strip resist — Use the Tepla plasma system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use **'program 23'**: plasma with CF_4 gas. Duration: 3 min.

13 Cleaning Procedure: HNO_3 100% and 65%

Cleaning	10 minutes in fuming nitric acid (Merck: HNO_3 100% selectipur) at ambient temperature. This will dissolve organic materials. Use wet bench 'HNO_3 (100%)' and the carrier with the red dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Cleaning	10 minutes in concentrated nitric acid (Merck: HNO_3 65% selectipur) at 110 °C. This will dissolve metal particles. Use wet bench 'HNO_3 (65%)' and the carrier with the red dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the Semitool 'rinser/dryer' with the standard program, and the white carrier with a red dot.

Etch Silicon Oxide @ frontside

14 Etch Silicon Oxide isotropically (27 µm): release

Use the SPTS UEtch HF Vapour Etcher.
Follow the operating instructions from the manual when using this machine.
Recipe 5. Duration:....

Measurements after processing

15 Measure sheet resistance

Use test wafer

Use the CDE Resmap 4-points probe with the silicon probe (ask Tom for help).
Expected sheet resistance for: 30 Ω/□ (wafers 2 and 4)

Finished

16 Inspection with SEM

Inspect the end-result using the SEM.