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Pedro Martín García-Vite[1] ✉, Julio C. Rosas-Caro[2], Ana Lidia Martínez-Salazar[1], Jose de Jesus Chavez[3], Antonio Valderrábano-González[2], Victor M. Sánchez-Huerta[4]

[1]*TECNM/Instituto Tecnológico de Ciudad Madero, CP. 89440, Tamaulipas., Mexico*
[2]*Universidad Panamericana-Guadalajara, CP. 45010 Zapopan, Jalisco, Mexico*
[3]*Delft University of Technology, CP 2628 CD Delft, The Netherlands*
[4]*Universidad de Quintana Roo, CP. 77019, Chetumal, Quintana Roo, Mexico*
✉ *E-mail: pedro.vite@itcm.edu.mx*

Abstract: This study introduces an advanced DC–DC power converter with two main objectives, (i) to achieve a wide range of voltage gain, which means the converter may work over a wide range of input voltage for a fixed desired output voltage and (ii) to achieve a reduced input current ripple. Those features are highly desired in renewable energy applications, for example with photovoltaic panels and fuel cells. The proposed converter was designed in a structure in which the input voltage is composed by the difference of two inductor currents, the currents through inductors are driven with transistors that may have different duty cycle, this allows the current ripple cancellation. In addition, the structure of the converter provides a quadratic type voltage gain, which leads to a wide range of operation voltage. The converter achieves both the wire range of voltage gain and current ripple cancellation, nonetheless, the buck–boost capability is also provided. The input current ripple reduction helps preserve the renewable energy sources since they suffer deterioration when current with considerable ripple is drawn from them. Dynamic and steady-state analysis are performed along with the components sizing. Simulation and experimental results are provided to demonstrate the principle of the proposition.

Nomenclature

V_{Cj}	average voltage of capacitor C_j
I_{Lj}	average current through inductor L_j
Δi_{Lj}	current ripple of the inductor L_j
Δv_{Cj}	voltage ripple of the capacitor C_j
r_{Lj}	equivalent series resistance of inductor L_j
r_{onj}	on-resistance of transistors Q_j
r'_j	ratio of the load resistor and the r_j: R/r_j
D	duty cycle applied to transistor Q_j
D_n	complement of the duty cycle $(1 - D)$ applied to Q_j
QBC	quadratic boost converter
G_B^2	voltage gain of the QBC
G_B	voltage gain of the conventional boost converter
Q_j	transistor jth with $j = 1, 2$
D_j	diode jth with $j = 1, p, n$
C_j	capacitor jth with $j = 1, p, n, o$
L_j	inductor jth with $j = 1, 2, o$
v_{Cj}	instantaneous voltage of the capacitor C_j
i_{Lj}	instantaneous current of the inductor L_j

1 Introduction

It is indisputable that power electronics converters are essential for processing the generated power from renewable sources. Among the DC renewable power sources, proton exchange membrane fuel cell (PEMFC) systems [1–3] and photovoltaic (PV) panels [4–6] are the most remarkable. In the design of an energy management system, there are two main requirements, besides traditional needs of the power electronics converters; (i) the wide voltage-range of operation and (ii) the requirements on the input current harmonic distortion.

The voltage-range of operation might be wide because renewable sources usually generate power at low and variable DC voltage; in the case of PV panels, issues concerned with the voltage gain can be alleviated if configurations of series-connected panels are employed [4, 7]. This approach can increase the voltage, nevertheless, the MPPT algorithms can be affected under partial shading conditions. In PEMFC applications, it is slightly more complicated to achieve a useful voltage level by means of several fuel cells. In this case, a power electronics converter is suited for obtaining the required voltage level, therefore some power processors have been already proposed, such as those reported in [1, 2]. In [7] a scheme, suited for renewable energy applications, incorporating battery-integrated DC–DC converters and derived from the basic power converters, has been proposed. Out of several studies, it can be observed that the concept of multi-input is taking significant relevance for schemes with more than one renewable power source; this kind of configurations gives the possibility of hybrid microgrids [8]. The study reported in [9] presented several multi-input converters, showing a well performance of two sources. Nonetheless, in the aforementioned approaches the input current ripple is still presented.

On the other hand, it is evident that the output voltage has to be regulated over a wide range, given the different levels. For example, the output voltage of the FC in [10] varies from 43 V at open circuit to 26 V at maximum load. This voltage is relatively low if it is considered that a grid-tie inverter may be fed with 200 V, the DC–DC converter must boost the voltage in the full operation range and regulate the output voltage under variations of the input voltage. The required voltage gain for such an application varies from 4.6 (43 V input and 200 V output) to 7.7 (26 V input and 200 V output).

The most common topology employed to increase the voltage is the traditional boost converter [11–13] whose static gain is well-known $G_B = 1/(1 - D)$. However, there are certain cases when it does not comply with the requirement of high voltage gain since its actual gain is limited due to the equivalent series resistance (ESR) of inductors and on-state resistance of MOSFETs as well as the commutation phenomena [3]. The problem of high gain can be partially alleviated by employing coupled inductors to extend the

static gain, such as in [14–16]. In [17] a converter based on two switches and a three-winding coupled inductor with a transformation ratio of n is presented. It possesses high efficiency and has an extra gain of $(n+1)$. This gain is even increased by means of a voltage extension cell for recycling inductor energy by a factor of $(n+2)$ [15]. Another interesting topology based on coupled inductors is the quasi-Z-source configuration [16] which provides an extra gain of $G_B = (1-D)/(1-2D)$. Besides, the efficiency can be increased employing soft-switching strategies [15] but a high number of components is required.

Most brands of commercial pulse width modulation (PWM) circuits do not warrantee a duty cycle >0.85 [13]. In that case, the voltage gain cannot be >6.67 for the conventional boost converter. Therefore, the discussed example, in which the maximum gain is 7.7 cannot be achieved with the traditional boost converter. Alternatively, a great number of topologies has been proposed [1, 18–22]; the key idea consists of incorporating an extra gain in cascade connection at the output of the conventional boost converter. Typically, the multiplier cells, constituted by pairs of diode–capacitor [18], have been employed, however as the number of cells increases so do the power losses [18]. The converter proposed in [19] is able to draw reduced input current ripple by adding extra components to the single-transistor conventional boost converter. However, its gain is only doubled, nonetheless the semiconductor stress is also kept low. The converter proposed in [22] is able to extract ripple-free current from the power source, however it does not possess the buck–boost capability. Other converter topologies with the capability of cancelling part of the switching ripple, are available in the literature, for example [20] presents a buck–boost and [22] presents a boost converter, both with the capability of cancelling part of the input current ripple, with the switching functions of their transistors. Some exiting topologies, belonging to the same member of the converter family, along with the proposed topology are presented in Fig. 1.

Another plausible solution is the use of quadratic converters [23–28], in which the voltage gain contains a quadratic term (G_B^2) and then a larger gain is expected for the same duty cycle. A recently observed tendency shows that when the power rating of FC is increasing, the output voltage reaches larger levels, too. There are FCs that exhibit nominal voltages >100 V, see e.g. [29, 30]. If the tendency continues, the development of converters with the capability of either increasing or decreasing the output voltage may be required for FC applications. Those reasons make a convert with buck–boost operation capability very convenient. The single-switch circuit proposed in [23] employs a buffer capacitor for coupling two converter obtaining a quadratic gain, however no current ripple-free is achieved. The circuit presented in [24] employs the concept of reduced redundant power processing which consists of cascading two three-port cells for obtaining a family of quadratic converters. Even though the converter's gain is quadratic, its terms are rather more elaborated than the classical. Nevertheless, the control strategy was successfully tested in [25]. The coupled inductor configuration also has been covered, providing an extra degree of freedom, such as in [27]. For applications where the step-down conversion is required, the topology showed in [31] is suited, since it contains a single quadratic term in the numerator.

After the wide voltage-range operation, the second big challenge for renewable energy harvesting is the need of draining a current with low harmonic distortion, since a large current ripple drawn from a renewable source reduces its efficiency and lifespan [32]. Therefore, it is highly advised to employ a power converter whose input current ripple is as small as possible. There are solutions based on magnetic coupling [33–36], either a passive filter [33] or the modification of a converter by combining it with the coupled inductor [34–36], but this manuscript focusses on non-coupled solutions which can be implemented with devices off-the-shelves. Converter proposed in [37] offers a non-coupled solution, however, it does not have quadratic gain and it cannot achieve ripple-free input current. Furthermore, the proposed topology can be also combined with a passive filter to have a further reduction of the input current ripple.

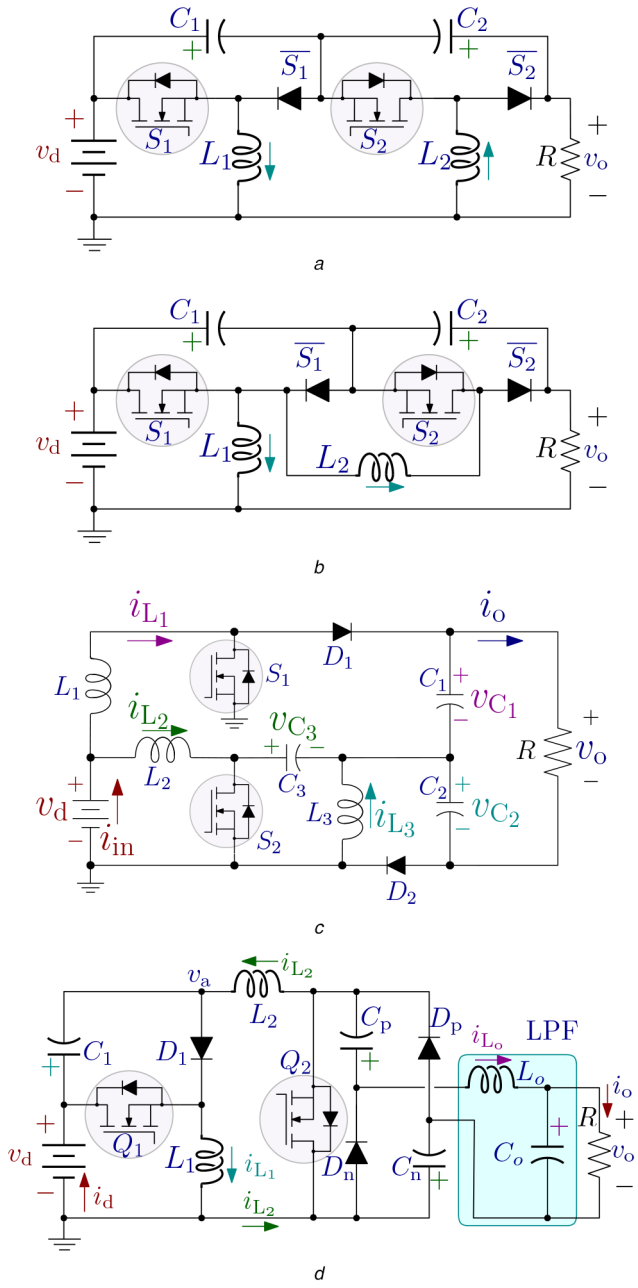

Fig. 1 *Quadratic boost converter topologies*
(a) Topology presented in [20], ***(b)*** Topology presented in [21], ***(c)*** Topology presented in [22], ***(d)*** Proposed topology

This work proposed a converter with wide voltage range of operation and low input current ripple. The main contribution of the manuscript is the proposition of the topology and the definition of switching functions in transistors, to perform a cancellation in an important percentage of the input current ripple, this allows to reduce the size of inductors compared to converters without current ripple cancellation capability.

The rest of the paper contains the proposed topology in Section 2 and then it is analysed in order to validate its effectiveness in Section 3. Although major design considerations are provided on Section 4. An efficiency comparison with existing power converters is performed in Section 5. The theoretical analysis is validated via simulation and experimentation whose results are reported in Sections 6 and 7, respectively. Finally, conclusions close the paper.

2 Proposed converter topology

The proposed structure of the converter, shown in Fig. 1*d*, is derived from the cascade configuration of a modified version of the traditional boost converter [38, 39] constituted by Q_1, D_1, L_1 and C_1,

and a modified boost converter which has been hybridised with a voltage multiplier and a low pass filter (LPF), and is constituted by Q_2, L_2, C_p, C_n D_p, D_n, L_o, and C_o. Although the first part of the converter is a boost-type, it feeds the rest of the converter, which is the voltage at the node $v_a = v_d - v_{C_1}$. This latter capability is very useful when the variable output voltage from a renewable source overpasses the voltage required by the load.

Both switches, Q_1 and Q_2 in Fig. 1*d*, are activated synchronously. The direction of currents and polarities of voltages are indicated in the positive direction.

2.1 Equivalent circuit states

Since switches are simultaneously controlled only two different equivalent circuits states are obtained. Due to the operation of the converter, the capacitors of the voltage multiplier C_p and C_n have the same voltage, therefore their voltage can be indicated as v_C, see Fig. 2.

Active state: When transistors are turned on, diodes get reverse biased; D_1 is reverse biased with the voltage across capacitor C_1. Diodes D_p and D_n get reverse biased with the voltage across C_p and C_n, respectively. Considering that the transistors behave as short circuits in this state, and diodes as open circuits, the converter can be represented with the equivalent circuit shown in Fig. 2*a*. The inductor L_1 is directly connected to the input voltage v_d. Therefore, its currents is increasing at rate of (v_d/L_1). As will be shown in Section 3, in steady state, the voltage across C_1 is larger than the input voltage, this causes that the current through L_2 also rises with a slope of $(v_{C_1} - v_d)/L_2$. Moreover, capacitors of the voltage multiplier (C_p and C_n) are connected in series, feeding the LPF with $(2v_C)$ volts.

Inactive state: During this time interval, transistors are turned off, which makes all diodes conduct. Diode D_1 closes to drain the current through L_1, and diodes D_p and D_n close to drain the current through L_o. Since transistors behave as open circuits and diodes as short circuits in this state, the converter can be represented with the equivalent circuit in Fig. 2*b*. In this case, capacitors of the voltage multiplier are getting charged and connected in parallel, this justifies the statement of $v_{C_p} = v_{C_n}$. Note that the load resistor has been drawn oppositely for a better appreciation.

By applying the Kirchhoff current law in the lower or ground node, the input current can be expressed as (1).

$$i_d = i_{L_1} - i_{L_2}. \tag{1}$$

Equation (1) makes the input current ripple cancellation possible.

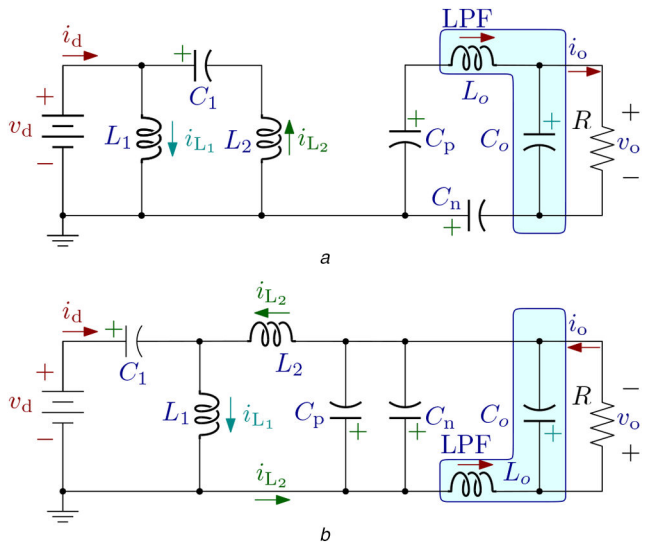

Fig. 2 *Equivalent circuits of the proposed topology*
(a) For the active state, ***(b)*** For the inactive state

3 Analysis of the proposed converter

Since one of the main contributions of the proposed topology is to draw free-ripple input current from the renewable source, only the continuous conduction mode (CCM) is suggested for achieving the lowest possible input current ripple at nominal operation. Therefore, the analysis of the proposed converter is explained next. If zero value of the input current ripple is desired, currents through inductors may feature triangular waveforms, that is, with a non-zero value. Thus, CCM is only taken into account for the analysis of the proposed topology. In order to obtain the mathematical expressions, the elements are taken as ideal components. For the CCM, inductors equations are:

$$L_1 \frac{\mathrm{d}i_{L_1}}{\mathrm{d}t} = d(v_d) + (1-d)(v_d - v_{C_1}), \tag{2a}$$

$$L_2 \frac{\mathrm{d}i_{L_2}}{\mathrm{d}t} = d(v_{C_1} - v_d) + (1-d)(v_{C_1} - v_d - v_C), \tag{2b}$$

$$L_o \frac{\mathrm{d}i_{L_o}}{\mathrm{d}t} = d(2 \cdot v_C - v_o) + (1-d)(v_C - v_o), \tag{2c}$$

where the voltage v_C is the voltage across C_p and C_n.

Equations (2a)–(2c) are obtained by applying the averaging technique [11]. The first term is the duty cycle d multiplied by the voltage across each inductor during the active state, see Fig. 2*a*. And the second term is the complement of the duty cycle $(1-d)$ multiplied by the voltage of the inductor during the inactive state, see Fig. 2*b*.

Since the average voltage, over a commutation period, on each inductor is zero, (2a)–(2c) can be reorganised in order to obtain the voltage across each capacitor which depends on the values of v_d and d, as (3a)–(3c), shows. Following a convenient notation, those variables for the input voltage, v_d, and the duty cycle, d, are capitalised which indicates average values.

$$V_{C_1} = V_d \cdot \frac{1}{(1-D)}, \tag{3a}$$

$$V_C = V_d \cdot \frac{D}{(1-D)^2}, \tag{3b}$$

$$V_{C_o} = V_d \cdot D \cdot \frac{(1+D)}{(1-D)^2}. \tag{3c}$$

As can be seen from (3a), the voltage across C_1 has the same gain as that of the conventional boost converter (G_B). The voltage from the upper node of the first converter indicated as v_a in Fig. 1*d*, is measured from that point to the ground, it is equal to $(v_d - v_{C_1})$, since v_{C_1} is larger than v_d [see (3a)], v_a is a negative voltage. Capacitors C_p and C_n contain a voltage produced by the cascade connection of a boost and a buck–boost G_{bB} converters (3b). Finally, the total output voltage is the cascade connection of a boost, a buck–boost, and a factor of $(D+1)$ as presented in (3c). This connection is not totally arbitrary but they are properly accommodated such that the input current ripple can be reduced or even totally cancelled which is analysed in Section 4.1. In this manner, the state space equations can be written as in (4).

(see (4))

(see (5a))

$$\begin{aligned} L_2 \frac{\mathrm{d}i_{L_2}}{\mathrm{d}t} &= d(v_{C_1} - r_{L_2} i_{L_2} - r_{on_2} i_{S_2} - v_d) \\ &\quad + (1-d)(v_{C_1} - v_d - v_C - r_{L_2} i_{L_2}), \end{aligned} \tag{5b}$$

$$\begin{aligned} L_o \frac{\mathrm{d}i_{L_o}}{\mathrm{d}t} &= d(2 \cdot v_C - r_{L_o} i_{L_o} - r_{on_2} i_{S_2} - v_o) \\ &\quad + (1-d)(v_C - r_{L_o} i_{L_o} - v_o). \end{aligned} \tag{5c}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{L_1} \\ i_{L_2} \\ i_{L_o} \\ v_{C_1} \\ v_C \\ v_{C_o} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -\frac{(1-d)}{L_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & -\frac{(1-d)}{L_2} & 0 \\ 0 & 0 & 0 & 0 & \frac{(1+d)}{L_o} & -\frac{1}{L_o} \\ \frac{(1-d)}{C_1} & -\frac{1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & \frac{(1-d)}{C} & -\frac{1}{C} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_o} & 0 & 0 & -\frac{1}{RC_o} \end{bmatrix} \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ i_{L_o} \\ v_{C_1} \\ v_C \\ v_{C_o} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ -\frac{1}{L_2} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{\mathrm{d}} \tag{4}$$

$$L_1 \frac{\mathrm{d}i_{L_1}}{\mathrm{d}t} = d(v_{\mathrm{d}} - (r_{\mathrm{on}_1} + r_{L_1}) \cdot i_{L_1}) + (1-d)(v_{\mathrm{d}} - v_{C_1} - r_{L_1} \cdot i_{L_1}), \tag{5a}$$

Among the several techniques of getting a dynamic model of converter [11, 40, 41], the simplified analysis of the converter using the model of PWM switches is used, this method consists of substituting transistors and diodes with controlled current and voltage sources, according to their respective average current and voltage in terms of the duty cycle and the state variables of the converter [11, 40, 41]. In this case, the application of the method leads to the dynamical model in Fig. 3. This model can be further manipulated to get the model with the equivalent DC-transformers [11] if required.

3.1 Comparison with similar topologies

Topologies that share the input current ripple capability are taken for comparison proposes. The conventional interleaved boost converter has the same gain as that of the traditional boost converter [42]. However, it does not possess the buck conversion capability which is disadvantageous in some applications. The converter with multiplier cells is an alternative option for obtaining a high gain, according to the number of cells. Depending on the number of stages, the input voltage can be a multiplier by an n factor. Nevertheless, conduction losses significantly increase [18]. The QBB proposed in [43] that possesses higher gain given its quadratic term besides the buck–boost conversion and input current ripple cancellation capabilities is taken as reference. Converters presented in [20, 21] possess the buck–boost (BB) conversion capability, as well as, the input current ripple cancellation. Their main features are taken as comparison. Fig. 4 shows the ideal voltage gains for the various converters employed for comparison, the proposed converter can both buck and boost the input voltage, allowing a wider voltage operating range besides it possesses a quadratic gain which increases more rapidly than that of the others. Additionally, Table 1 shows the comparison of converters in terms of number of components and their capability of cancelling the input current ripple. Similarly, Table 2 presents the comparison of converters in terms of voltage gain, and voltage and current stress on switches and diodes. For a specific value of $D = 50\%$, the QBB converter presented in [43] reaches a gain of two whereas the proposed converter can reach a gain of three. However, for values of duty cycle beyond 50% of the proposed converter has the highest gain of all of them.

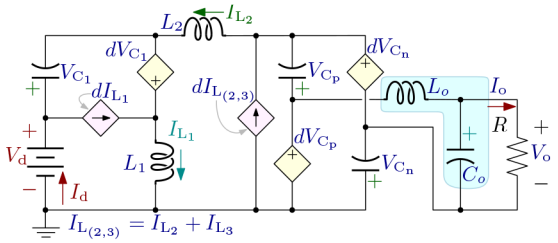

Fig. 3 *Average equivalent circuit of the proposed converter*

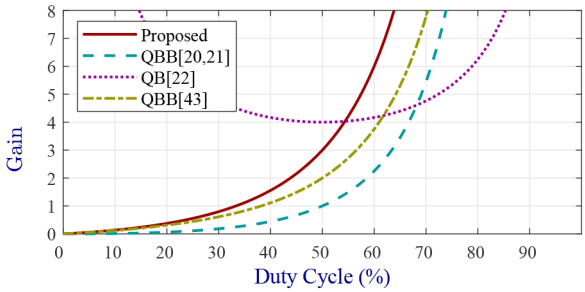

Fig. 4 *Comparison of the voltage of the proposed converter against other existing topologies*

Table 1 Elements quantity comparison

Parameter	Quadratic buck–boost in [20]	Quadratic buck–boost in [21]	Boost converter in [22]	Proposed quadratic buck–boost
inductors	2	2	3	3
capacitors	2	2	3	4
transistors	2	2	2	2
diodes	2	2	2	3
input current ripple cancellation	yes	no	yes	yes

3.2 Analysis under real conditions

Even though the output voltage can be calculated by means of (3a–3c), a more realistic approximation is needed for estimating the actual output voltage. Therefore, the parasitic elements of the inductors (r_{L_s}) as well as the on-resistance of the transistors (r_{on}) are taken into account. From the equivalent circuits of the different states, expressions of (2a)–(2c) can be rewritten considering the aforementioned resistive elements, resulting (5a)–(5c).

Note that $i_{S_2} = i_{L_2} + i_{L_o}$, which is readily deduced from the scheme of Fig. 1*d* during the on-state or equivalently $q(t) = 1$.

Moreover, for obtaining the average inductors currents a procedure described in [11] can be followed. Therefore, the dynamic capacitors currents can be employed, as described below

$$C_1\frac{\mathrm{d}v_{C_1}}{\mathrm{d}t} = d(-i_{L_2}) + (1-d)(i_{L_1} - i_{L_2}), \tag{6a}$$

$$C_p\frac{\mathrm{d}v_{C_p}}{\mathrm{d}t} = d(-i_{L_o}) + (1-d)(i_{L_2} - i_{C_n} - i_{L_o}), \tag{6b}$$

$$C_n\frac{\mathrm{d}v_{C_n}}{\mathrm{d}t} = d(-i_{L_o}) + (1-d)(i_{L_2} - i_{C_p} - i_{L_o}), \tag{6c}$$

$$C_o\frac{\mathrm{d}v_{C_o}}{\mathrm{d}t} = d(i_{L_o} - i_o) + (1-d)(i_{L_o} - i_o)\,. \tag{6d}$$

It can be readily seen from (6d) that $I_{L_o} = I_o$, averaging the rest of the inductors currents over a period in (7a)–(7c) results

$$I_{L_1} = \frac{1+D}{(1-D)^2}\cdot I_o, \tag{7a}$$

$$I_{L_2} = \frac{1+D}{(1-D)}\cdot I_o, \tag{7b}$$

$$I_{L_o} = I_o\,. \tag{7c}$$

Besides, the ideal inductors currents are found as a function of the output voltage V_o and the load resistor R. By recognising that the output current is found given the input and output voltages, as below

$$I_o = \frac{V_o}{R}, \tag{8a}$$

$$I_o = \frac{V_d}{R}\cdot\frac{(1+D)}{(1-D)^2}\cdot D\,. \tag{8b}$$

The variables $D_p = (1+D)$ and $D_n = (1-D)$ will be introduced in order to avoid notational clutter. By substituting (8a) and (8b) into (5), averaging over a switching period T_s, and solving for the capacitor's voltages, results in

$$V_{C_1} = \frac{1}{D_n}\left[V_d - (r_{L_1} + r_{On_1}D)\cdot I_{L_1}\right], \tag{9a}$$

$$V_C = \frac{1}{D_n}\left[V_{C_1} - V_d - (r_{L_2} + r_{On_2}D)I_{L_2} - r_{On_2}DI_{L_o}\right], \tag{9b}$$

$$V_o = V_C\cdot D_p - (r_{L_o} + r_{On_2}D)\cdot I_{L_o} - r_{On_2}D\cdot I_{L_o}\,. \tag{9c}$$

Finally, the actual output voltage is found by substituting the corresponding values of capacitor voltages into (9c), as shown below

$$V_o = V_d\frac{D\cdot D_p}{D_n^2}\left(1 - r'_{L_1}\frac{D_p^2}{D_n^4} - r'_{L_2}\frac{D_p^2}{D_n^2} - r'_{L_o} - r'_{On_1}\frac{D_p^2}{D_n^4}D - r'_{On_2}\frac{4D}{D_n^2}\right) \tag{10}$$

Where the parasitic elements have been defined as $r'_j = (r_j/R)$ with $j = L_1$, L_2, L_o, On_1, and On_2 for the inductors L_1, L_2, and L_o, and transistors S_1 and S_2, respectively. It is worth mentioning that the ideal gain, expressed in (3c), is retrieved when the resistive elements are set to zero, ($r'_j = 0$).

4 Design considerations

From Fig. 1*d*, by applying the Kirchhoff current law in the lower node, it can be observed that the input current i_d is equal to the inductor L_1 current i_{L_1} minus the inductor L_2 current i_{L_2}, also indicated in (1). An interesting behaviour can be observed in Fig. 2, when switches are On [see Fig. 2*a*]. The current i_{L_1} rises, getting charged with a slope equal to (v_d/L_1), while the current in inductor L_2 decreases, its voltage is equal to ($v_d - v_{C_1}$). However, as can be seen in (3a), v_{C_1} is larger than v_d. It is worth mentioning that when one inductor current ripple increases, the other one decreases. They are 180° out of phase from the input point of view (1)

$$\Delta i_d = \Delta i_{L_1} - \Delta i_{L_2}\,. \tag{11}$$

The strategy for getting null (low) input current ripple consists of employing the current slopes of inductors L_1 and L_2 in such a way that they are cancelled (reduced) with each other.

4.1 Input current with low ripple

From Fig. 2, the current ripple in L_1 can be expressed from the current slope when switches are On. The voltage across L_1 is equal to V_d (considering the small ripple approximation [11]) and, its current slope is V_d/L_1. Fig. 2*a* holds during a time DTs, then, the peak-to-peak current or total variation in the current of L_1 can be expressed by (12a).

Table 2 Comparison of topologies parameters

Parameter	Quadratic buck–boost in [20]	Quadratic buck–boost in [21]	Boost converter in [22]	Proposed quadratic buck–boost
voltage gain	$\left(\frac{D}{1-D}\right)^2$	$\left(\frac{D}{1-D}\right)^2$	$\frac{1}{D(1-D)}$	$\frac{D(1+D)}{(1-D)^2}$
voltage stress				
switch 1	$\frac{1}{1-D}V_d$	$\frac{1}{1-D}V_d$	$\frac{1}{D}V_d$	$\frac{1}{1-D}V_d$
switch 2	$\frac{D}{(1-D)^2}V_d$	$\frac{D}{(1-D)^2}V_d$	$\frac{1}{1-D}V_d$	$\frac{D}{(1-D)^2}V_d$
diode 1	$\frac{1}{1-D}V_d$	$\frac{1}{1-D}V_d$	$\frac{1}{D(1-D)}V_d$	$\frac{1}{1-D}V_d$
diode 2	$\frac{D}{(1-D)^2}V_d$	$\frac{D}{(1-D)^2}V_d$	$\frac{1}{1-D}V_d$	$\frac{D}{(1-D)^2}V_d$
diode 3	—	—	—	$\frac{D}{(1-D)^2}V_d$
current stress				
switch 1	$\frac{1}{1-D}I_o$	$\frac{D}{(1-D)^2}I_o$	$\frac{1}{D}I_o$	$\frac{1+D}{(1-D)^2}I_o$
switch 2	$\frac{D}{(1-D)^2}I_o$	$\frac{1}{1-D}I_o$	$\frac{1}{1-D}I_o$	$\frac{1+D}{1-D}I_o$
diode 1	$\frac{1}{1-D}I_o$	$\frac{D}{(1-D)^2}I_o$	$\frac{1}{D}I_o$	$\frac{1+D}{(1-D)^2}I_o$
diode 2	$\frac{D}{(1-D)^2}I_o$	$\frac{1}{1-D}I_o$	$\frac{1}{1-D}I_o$	$\frac{D}{1-D}I_o$
diode 3	—	—	—	$\frac{D}{1-D}I_o$

Similarly, the current ripple in L_2 can be expressed from its current slope when switches are on, see Fig. 2*a*. In this case, the voltage across L_2 is equal to $V_d - V_{C_2}$ (considering the small ripple approximation [11]) and, its current slope is equal to $(V_d - V_{C_2})/L_2$. Fig. 2*a* holds during a time DT_s, the peak-to-peak current or total variation in the current of L_2 can be expressed by (12b).

$$\Delta i_{L_1} = \frac{V_d}{L_1} D T_s, \tag{12a}$$

$$\Delta i_{L_2} = \frac{V_d}{L_2} \cdot \frac{D^2}{(1-D)} T_s. \tag{12b}$$

The current ripples expressed in (12a and 12b) can be used to compute the current ripple at the input side as expressed in (11). Moreover, the duty cycle $D^\star$, at which the input current ripple is zero ($\Delta i_d = 0$), can be found my making (12a) equal to (12b), which leads to

$$D^\star = \frac{L_2}{L_1 + L_2}. \tag{13}$$

4.1.1 Sizing of inductors: Inductors are usually calculated according to a desired current ripple, with expressions similar to (12a and 12b). In this case, before choosing them, the relation among them can be calculated with (13). The operation of the converter is usually limited to a range of duty cycle; it is highly desirable than the duty cycle $D^\star$ holds within the operation range. From (13) a relation among inductors can be established in terms of the duty cycle $D^\star$ as

$$\frac{L_1}{L_2} = \frac{1 - D^\star}{D^\star}. \tag{14}$$

It can be noticed that one inductor value can be freely proposed, whereas the other needs to be found by employing (14). Note that as the duty ratio moves away from the optimal value $D^\star$, the current ripple will be increased as well. Nevertheless, a static operating point is expected in the steady state, having zero current ripples during normal operation. Current ripple in other operation points can be calculated from (11) and (12).

4.1.2 Continuous conduction mode: As explained in Section 2.1, the current through diodes D_p and D_n are equal during the entire switching period. During the off-state interval, the current of L_2

$$i_{L_2} = i_{D_p} + i_{C_p}, \tag{15a}$$

$$i_{L_2} = i_{D_p} + (i_{D_n} - i_{L_o}). \tag{15b}$$

Moreover, defining $i_D = i_{D_n} = i_{D_p}$ and solving for each diode current, results:

$$i_D = \frac{i_{L_2} + i_{L_o}}{2}. \tag{16}$$

Averaging (16) over a switching period and employing the average inductor currents given in (7) and taking the current ripples into account, produces, respectively

$$I_D = \frac{I_o}{(1-D)}, \tag{17a}$$

$$\Delta i_D = -\frac{D^2 V_d \cdot T_s}{2 \cdot (1-D)} \left(\frac{1}{L_o} + \frac{1}{L_2} \right). \tag{17b}$$

Similarly as occurred in [22], the CCM is ensured on the assumption that i_D is positive for the turn-off interval, that is $[(1-D) \cdot T_s]$. The current (i_B) represents the load current for the boundary condition, note that it decreases to zero at the end of the $(1-D) \cdot T_s$ interval, observe Fig. 5. The converter will enter in the discontinuous conduction mode if the load is reduced.

Furthermore, (16) is expressed in terms of current ripples of L_o and L_2, such as

$$\Delta i_D = \frac{\Delta i_{L_o} + \Delta i_{L_2}}{2}. \tag{18}$$

The minimum value of inductors L_o and L_2, for guaranteeing the CCM, are found by employing (2a)–(2c), (3a)–(3c), (17a) and (17b) and (18).

$$L_{eq} \geq \frac{D \cdot (1-D)^2 \cdot R}{4 \cdot (1+D) \cdot F_s}. \tag{19}$$

where L_{eq} is the parallel equivalent of L_o with L_2 which can be computed as $L_{eq} = ((L_o \cdot L_2)/(L_o + L_2))$ and $F_s = 1/T_s$ is the switching frequency.

4.2 Sizing of capacitors

For specific voltage ripple on capacitors, (6a)–(6d) and (7a)–(7c) are used to calculate the various capacitor values

$$\Delta V_{C_1} = \frac{V_o}{R \cdot C_1} \cdot \frac{D \cdot (1+D)}{(1-D) \cdot F_s}, \tag{20a}$$

$$\Delta V_C = \frac{V_o}{R \cdot C} \cdot \frac{D}{F_s}. \tag{20b}$$

where C has been defined for the capacitors of the multiplier stage as $C = C_p = C_n$.

5 Power loss analysis

Converters with similar features are taken for comparison. Therefore, converters presented in [20, 43] are simulated under the same conditions and power rating.

By following the procedure describe in the literature [11, 37], the power losses distributed in the various components are summarised in Table 3. Where $P_{Loss}^{SW,cond}$, $P_{Loss}^{SW,switch}$, P_{Loss}^{D}, P_{Loss}^{L}, and P_{Loss}^{C} are the conduction losses for transistors, switching losses for transistors, conduction losses of diodes, losses due to the ESR on inductors and capacitors, respectively.

As can be observed, the proposed converter takes advantage over the QBB of [20] since the low ripple input current makes the inductors loss keep at minimum. However, for low values of duty ratio, the conducting losses on D_1 are increased, since it has to conduct the current during the interval $(1-D)T_s$. Compared to the QBB of [43], with identical values of inductors (L_1 and L_2), the proposed converter is able to deliver the same amount of power at lower duty ratio. This is possible due to the multiplier cell. Moreover, if inductors were properly selected, by means of (13),

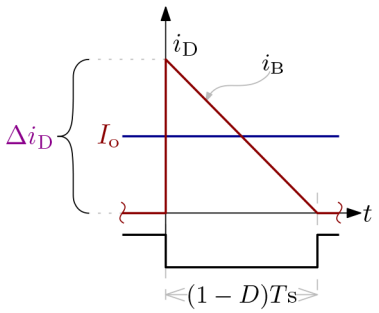

Fig. 5 *Current through diodes at the boundary condition*

Table 3 Efficiency and loss comparison: rated at an output power of 250 W, and $R = 270\,\Omega$

Loss	QBB [20]		QBB [43]		Proposed	
	$\eta = 92.23\%$		$\eta = 93.12\%$		$\eta = 94.9\%$	
	(%)	(W)	(%)	(W)	(%)	(W)
$P_{\text{Loss}}^{\text{SW, cond}}$	0.70	1.75	0.6	1.50	0.7	1.75
$P_{\text{Loss}}^{\text{SW, switch}}$	2.10	5.25	1.13	2.82	1.1	2.75
$P_{\text{Loss}}^{\text{D}}$	1.10	2.75	1.15	2.87	1.4	3.5
$P_{\text{Loss}}^{\text{L}}$	3.50	8.75	3.6	9.00	1.6	4.0
$P_{\text{Loss}}^{\text{C}}$	0.37	0.92	0.4	1.00	0.3	0.75
$P_{\text{Loss}}^{\text{Total}}$	7.77	19.42	6.88	17.2	5.10	12.75

Table 4 Parameters of the various devices

Symbol	Value
power components	
v_{d}	10 V
L_1	33 µH (1140-330K-RC)
L_2	82 µH (1140-820K-RC)
L_{o}	100 µH (1140-101K-RC)
C_1, $C_{(\text{p, n})}$, C_{o}	100 µF
R	65 Ω
ESRs	
r_{L_1}, r_{L_2}	15, 11 mΩ
$r_{L_{\text{o}}}$	25 mΩ
r_{onT1}	5.9 mΩ
r_{onT2}	6.2 mΩ
commanding signal	
D	71.3%
F_{s}	50 kHz
devices	
MCU	ATmega328p
S_1	IPA075N15N3
S_2	TK56A12N1
D_1	DSS16-01A
$D_{(\text{p, n})}$	NTST20U100CTG
gate drivers	A3120

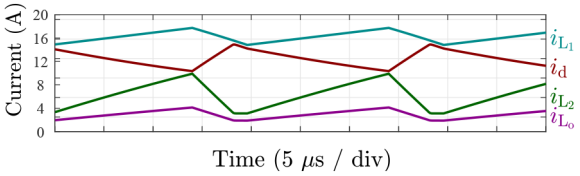

Fig. 6 *Presence of ripple in the current ripple*

with a higher value of the duty ratio ($D > D^{\star}$), zero input current ripple would not be possible.

6 Numerical validation

The proposed converter has been simulated in the SimPowerSystems environment of Matlab, with the aim of proving the theoretical approach. Also, a laboratory-scale prototype was set up, considering the parameters listed in Table 4. First, a simulation was run by setting values of inductors $L_1 = L_2 = 33\,\mu$H and with $D = 73\%$. Voltages keep without changes, therefore only currents are presented in Fig. 6. Clearly, there is no cancellation ripple at the input current.

In order to corroborate the effectiveness of the proposed switching strategy, inductors have been selected as $L_1 = 33\,\mu$H and $L_2 = 82\,\mu$H. Fig. 7 shows the simulation results for a specific duty ratio of about 71.3%, found by (13).

Fig. 7 contains the inductors and input currents. The input current does not possess ripple while i_{L_1} and i_{L_2} are represented by triangular waveforms. The current through the LPF inductor has been included as well. At the bottom of the figure, the commanding signals with 71.3% of the duty cycle. Note that current of inductors L_1 and L_2 have the same triangular waveform. According to (1), the instantaneous value of the input current ripple is zero all the time. Also, that $i_{L_{\text{o}}}$ can become negative.

The remaining waveforms are presented in Figs. 8 and 9; Fig. 8*a*: capacitors voltages – the output voltage, taken from the output filter capacitor C_{o} reaches about 130 V, feeding a load resistor of 200 Ω. v_{C_1} is ∼30 V, and $v_C = v_{C_{\text{p}}} = v_{C_{\text{n}}}$ is 70 V. Voltage and current on the switches 1 and 2 are indicated in Figs. 8*b* and *c*. Note that I_{S_1} is higher than I_{S_2} by a factor of $1/(1 - D)$. Inductors voltages are shown in Fig. 9*a*. Since both transistors share the same switching function, voltages across the three inductors have the same polarity. Note that inductors L_2 and L_{o} have the same voltage magnitude. Voltages and currents on diodes are also presented in Figs. 9*b* and *c*. Similarly, diodes D_{p} and D_{n} share the same parameters of voltage and current.

7 Experimental results

As previously said, the simulation results were validated by means of a laboratory prototype, presented in Fig. 10, with the main devices highlighted.

Experimentation was carried out utilising identical values for the simulation, given in Table 4. As can be observed in the upper oscillogram Fig. 11, both inductors current ripples have the same magnitude ($\Delta i_{L_1} = \Delta i_{L_2}$), therefore the input current ripple is successfully cancelled, producing a flat or pure DC waveform. Also, it is important to note that the average values of such currents are different, even though ($I_{L_1} > I_{L_2}$), it is possible to cancel their ripples at the input side, for a specific duty cycle $D^{\star}$. Both results match, as expected, however, little spikes on the voltage appear due to the commutation phenomena and the high-frequency noise, which can be eliminated employing some snubber nets or omitted.

Figs. 12 and 13 show the rest of the registered parameters. Fig. 12*a* contains the capacitors and input voltage. As expected, C_{p} and C_{n} have the same magnitude voltage, output capacitor voltage matches the predicted value by means the simulation, as well. However, small voltage spikes appeared on switches 1 and 2, even though nets snubbers were employed, Figs. 12*b* and *c*. Inductors voltage and parameters diodes D_1 and $D_{(\text{p, n})}$ are shown in Figs. 13*b* and *c*, respectively. As predicted, losses are concentrated on D_1. Whereas diodes $D_{(p,n)}$ do not contribute significatively with the power losses.

8 Conclusion

A buck–boost power converter that possesses the main features of a wide voltage range of operation and low input current ripple was proposed. The converter has the quadratic gain which is further increased by a multiplier cell that shares a diode–capacitor pair as part of a conventional boost converter. The proposed topology also possesses the bucking capability which results convenient for

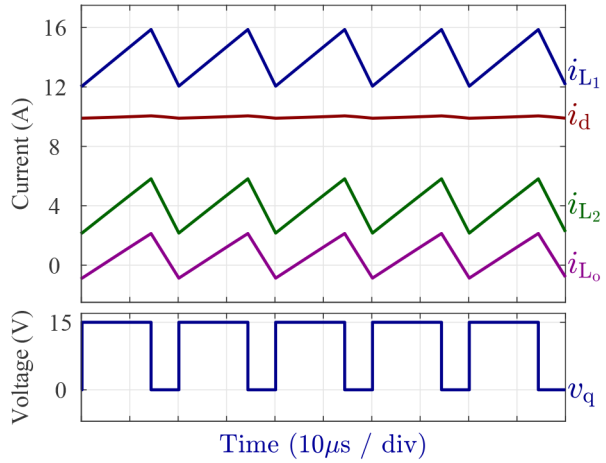

Fig. 7 *Simulation key waveforms of the proposed converter*

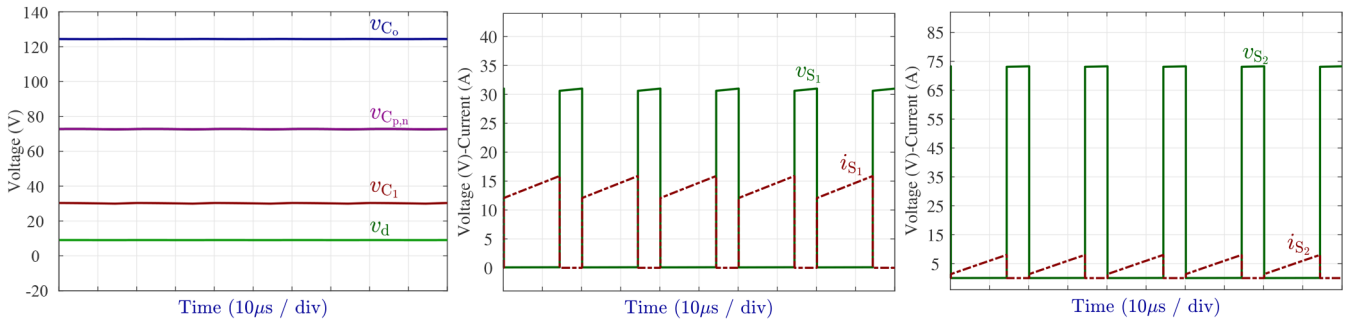

Fig. 8 *Simulation waveforms of capacitors and switches*
(a) Capacitors and input voltage, ***(b)*** Voltage and current of switch 1, (v_{S_1}, i_{S_1}), ***(c)*** Voltage and current of switch 2, (v_{S_2}, i_{S_2})

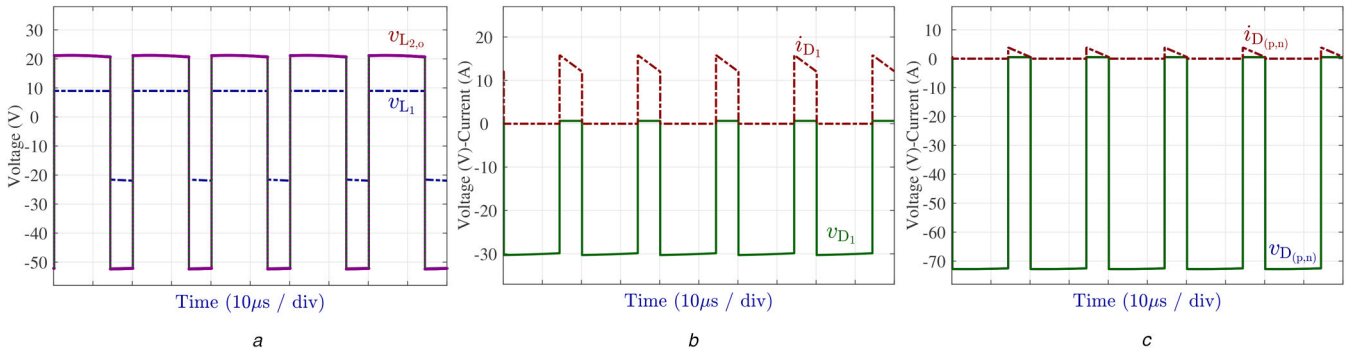

Fig. 9 *Simulation waveforms of inductors and diodes*
(a) Inductors voltage, (v_{L_1}, v_{L_2}, i_{L_o}), ***(b)*** Voltage and current of diode D_1, ***(c)*** Voltage and current of diodes $D_{(p,n)}$

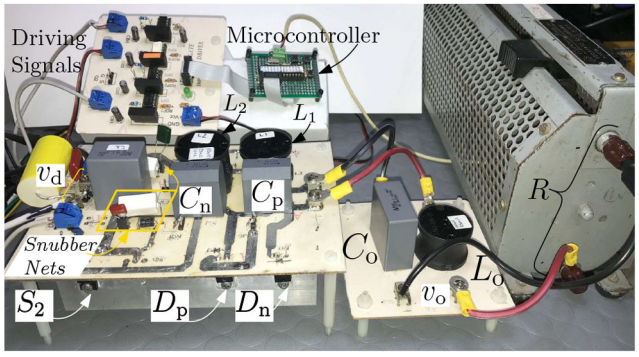

Fig. 10 *Picture of the prototype*

renewable energy applications. The topology was deeply analysed to deduce the voltage gain. The corresponding equations for computing the various components ratings were determined. The key waveforms for cancelling the input current ripple were presented as well. Simulation and experimental results corroborated the well performance of the proposal, showing a great matching each other. The proposal is an alternative for renewable applications, as was evidenced by the comparison performed.

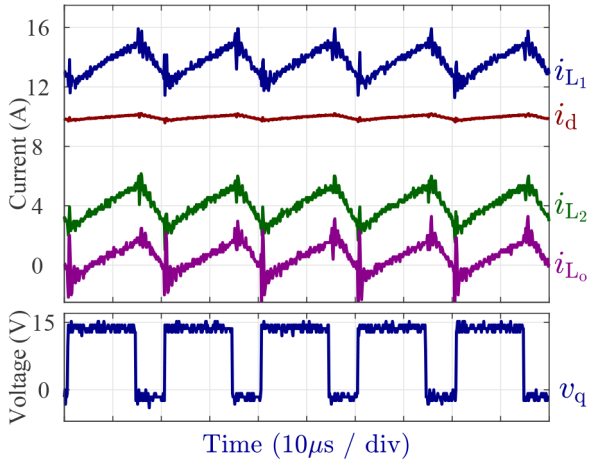

Fig. 11 *Experimental key waveforms of the proposed converter*

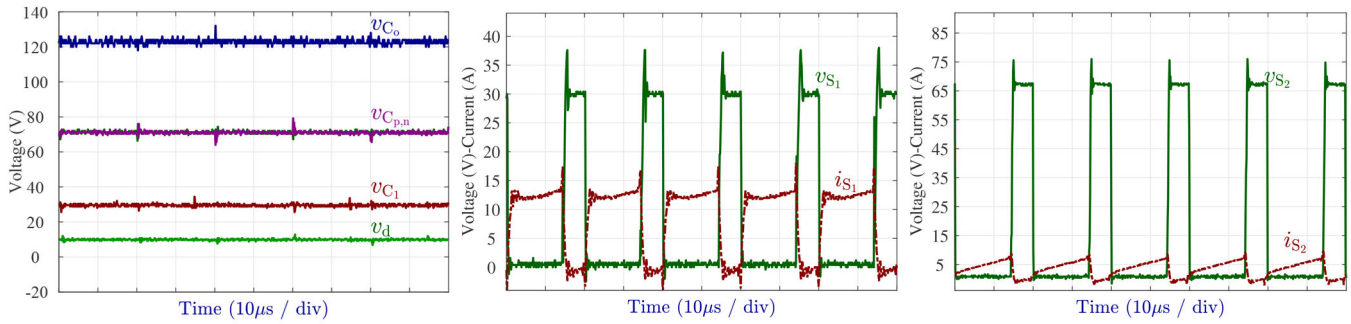

Fig. 12 *Experimental waveforms of capacitors and switches*
(a) Capacitors and input voltage, ***(b)*** Voltage and current of switch 1, (v_{S_1}, i_{S_1}), ***(c)*** Voltage and current of switch 2, (v_{S_2}, i_{S_2})

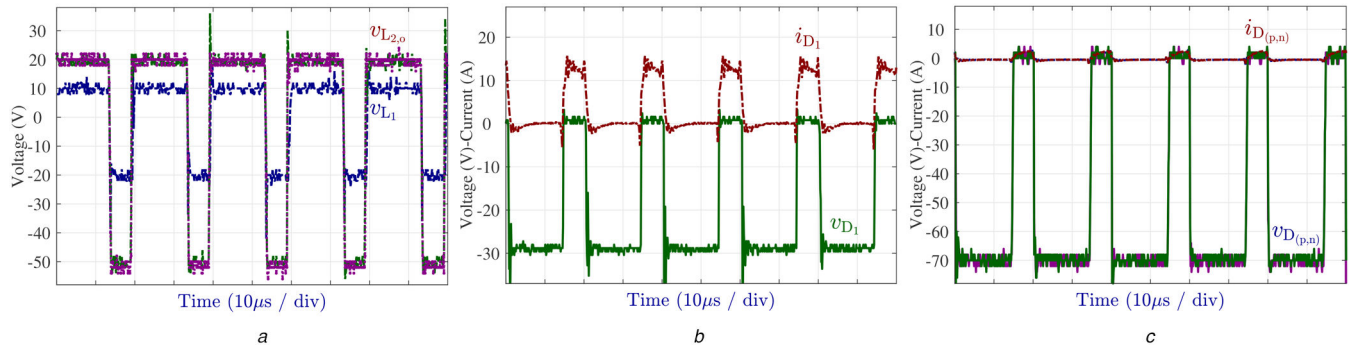

Fig. 13 *Experimental waveforms of inductors and diodes*
(a) Inductors voltage, (v_{L_1}, v_{L_2}, i_{L_o}), ***(b)*** Voltage and current of Diode D_1, ***(c)*** Voltage and current of Diodes $D_{(p,n)}$

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