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Compact and Scalable Capacitorless Linear Voltage Regulator for Power Management Integrated Circuits

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Compact and Scalable Capacitorless Linear Voltage Regulator for Power Management Integrated Circuits

by

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Abstract

The current generation of power management integrated circuits require fully integrated, low cost and low power solutions for voltage regulation. As final blocks in the internal power supply chain, excellent performance linear voltage regulators are required, especially in terms of dynamic response and stability. Since many voltage regulators are used, the chip area consumed by the regulators is a point of attention. Additionally, for some internal voltages the load current or capacitive loading is much lower, such that a scalable compact solution would be preferred. This project focuses on minimizing the on-chip area of voltage regulators while maximizing their performance.

The proposed design incorporates a novel circuit technique for improving the dynamic response of linear voltage regulators. In this thesis, the theory and analysis of current amplifier-based NMOST linear voltage regulators is introduced. In order to maximize the dynamic performance, multiple implementations are analyzed and their drawbacks are presented. Adaptive biasing has been implemented in order to improve the slew rate at the gate of the pass transistor and to increase the voltage loop gain bandwidth. The current loop is stabilized by means of bandwidth enhancement resistors, reaching a unity gain frequency of over 500MHz at maximum load current condition.

The linear voltage regulator occupies an area of 0.0078 mm^2, consumes a quiescent current of 8.5μA and has a current capability of 10 mA. The circuit operates at supply levels varying between 7 to 18V, provides an output regulated voltage of 1.8V and is scalable in terms of the load capacitance and the load current. This design achieves a FOM of 0.613ps and is comparable to state-of-the-art designs.

Acknowledgements

I still remember the day I arrived in the Netherlands and glanced at its wonders as if it were yesterday. Looking back at the last two years I realize that I have met wonderful, amazing people, teachers, colleagues, and friends, that have shaped me even further as a person. I could not be more grateful for the experiences that have been presented to me and I will never forget the memories that were born here.

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I want to express my most sincere gratitude to my parents, for their love, appreciation, and support, and to my close friends, who have always been there for me, supportive, and positive. I could not have done this as easily without you.

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1 Introduction

1.1. Background

Power management integrated circuits (power management ICs or PMICs) are solid-state devices that control the flow and direction of electrical power. Many electrical devices have multiple internal voltages (e.g., 5 V, 3.3 V, 1.8 V, etc.) and sources of external power (e.g., wall outlet, battery, etc.), meaning that the power design of the device has multiple requirements for operation.

PMICs are used to control external power MOSFETs that are used in power converters such as boost converters, buck converters, buck/boost converters, and half-bridges. Power management ICs add smart power functions to the converters that aim to maximize the efficiency of the product in which it is being used, such as:

1. Protections:
   (a) Overvoltage protection.
   (b) Undervoltage protection.
   (c) Overtemperature protection.
   (d) Short-circuit protection.
   (e) Overcurrent protection.
2. Dedicated control techniques that allow for different modes of operation, e.g., low-/high-power modes of operation.

Several improvements to the overall design can be made by incorporating these functions into one IC, such as: better conversion efficiency, smaller solution size, and better heat dissipation [1].

The PMIC unit requires many linear voltage regulators (LVRs) with different output voltages and load current capacities to support many applications, for example, tablet PC applications, laptops, adapters, video game consoles and many others.

The current generation of PMICs requires low area and therefore low cost solutions for voltage regulation. This had the immediate effect of highlighting the need for an alternative implementation of LVRs that can eliminate the conventional bulky off-chip capacitor. As the

final blocks in the internal power supply chain, excellent performance linear voltage regulators are required, especially in terms of dynamic response, such as line and load regulation, startup time, and stability [2] .

Recent research focuses on the development of fully integrated LVRs, or output capacitor-less LVRs, that target a higher integration level of System-on-Chip (SoC) power management. Eliminating the bulky external capacitor saves pin count, and board space, reduces bond-wire induced noise, and saves chip area as the number of pads is reduced. However, the trade-offs among stability, regulation precision, quiescent current consumption, loop bandwidth, and transient responses have imposed critical challenges on the design of CL LVRs [3] .

1.2. Application

An example of an application for which the proposed LVRs are meant to be integrated in is a digital, configurable LLC & PFC (power factor control) combo controller for high-efficiency resonant power supplies [4]. The targeted applications for this product are:

1. Industrial: Printers.
2. Mobile: Notebook Adapter.
3. Smart Home:
   (a) Desktop and all-in-one Personal Computers.
   (b) Video Game Consoles.

A simplified application diagram is illustrated in Fig. 1.1 [4].

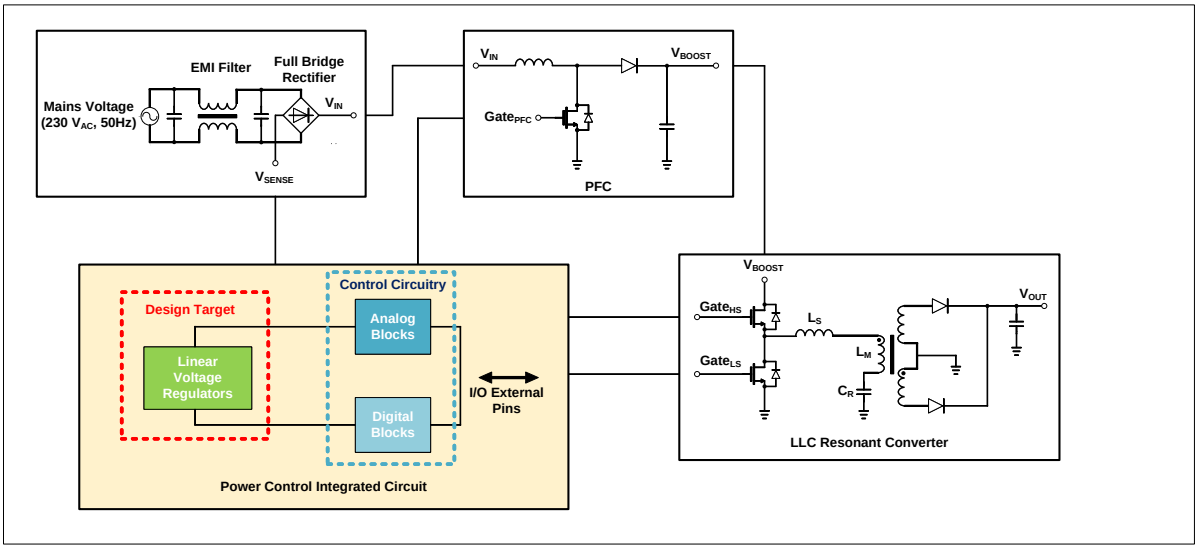

Figure 1.1: Simplified Application Diagram

A brief introduction to the principles behind PFC circuitry and LLC resonant converters is given in the following subsections.

1.2.1. Power Factor Control Principle

Three types of power, e.g., active, reactive, and apparent, relate to one another in a trigonometric form known as the power triangle. The relation between the triangles is illustrated in Fig. [5].

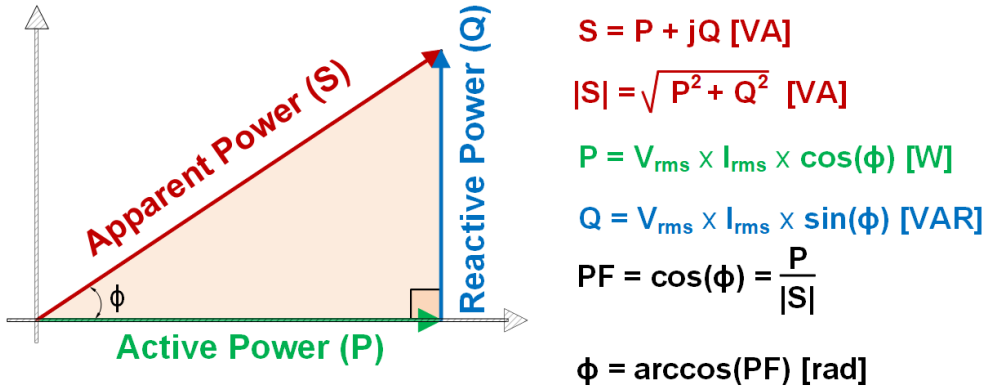

Figure 1.2: Power Triangle [5]

- Real power (or active power), P, is the amount of power consumed by a load and is measured in Watts.
- Reactive loads such as inductors and capacitors do not dissipate power, yet they drop voltage and draw current. This is called reactive power, Q, and is measured in Volt-Amps-Reactive (VAR).
- The combination of reactive power and active power is called apparent power, S, and it denotes the amount of power transferred from a power supply. The unit of measure for apparent power is Volt-Amps (VA).

The power factor (PF) is defined as the cosine of the phase angle between apparent and active power:

$$PF = cos(\phi) = \frac{P}{|S|} \tag{1.1}$$

The phase shift between the voltage and current waveforms can be computed as:

$$\phi = arccos(PF)[rad] \tag{1.2}$$

According to Fig. , the active power is given by:

$$P = V_{rms} I_{rms} cos(\phi)[W] \tag{1.3}$$

For a DC input, the input current and input voltage are in phase and, as such, maintain a PF equal to one.

For an electronic application that is powered from the AC grid, the input current does not naturally follow the instantaneous AC line voltage. For a PF less than 1, a significant portion of the generated power circulates in the system instead of being consumed by the load. More

apparent power, i.e., more circulating current would be required to deliver the same amount of real power to the load.

To achieve a PF equal to unity, yielding maximum efficiency, the phase shift between voltage and current must be zero. However, it is not sufficient to bring the current and voltage into phase. As described in the international standard, EN 61000-3-2 [6], there are limits imposed on the values of harmonic currents up to the 40th harmonic current. Therefore, to comply with the standard, the current and voltage waveforms must not only be in phase but also the current needs to be sinusoidal.

The most common topology choice for active power factor correction is the DC-DC boost converter [7]. In this topology, the inductor is on the input side of the converter, meaning that the input current does not experience high dI/dt, making the topology better equipped to achieve low input current distortion. European mains voltage is presently specified as being 230 V_{rms} ± 10% and since the PF control circuit is a boost converter, the output voltage must be higher than the maximum input voltage, e.g., 253 V_{rms} or 356.73V. The industry standard for the boosted voltage is 400V.

1.2.2. LLC Resonant Converter Principle

Safety regulations impose that the apparatus must be isolated from the mains pins. This is achieved using an isolation transformer (safety regulations) in combination with a LLC tank (harmonic current regulations).

A LLC converter is a resonant inverter with three reactive elements where the boosted DC input voltage is turned into a square wave by a switch network arranged as a half-bridge that feeds the resonant LLC tank, effectively filtering out harmonics, providing sinusoidal-like voltage and current waveforms [8].

Based on Fig. 1.1, the linear relationship between the input power and energy stored in capacitor C_r is briefly described as [4]:

- When the high-side switch is on, a primary current is flowing through the transformer and resonant capacitor C_r, as indicated by the red line.
- Half the energy the input delivers is transferred to the output. The other half charges resonant capacitor C_r $\implies$ the voltage across the resonant capacitor increases.
- When the high-side switch is off and the low-side switch is on, the energy which is stored in resonant capacitor, C_r, is transferred to the output and its voltage decreases.

The input power has a lienar relationship with the capacitor voltage difference, ΔC_r [4]:

$$P_{IN} = V_{BOOST} \cdot I_{BOOST} = V_{BOOST} \cdot \Delta V_{C_r} \cdot C_r \cdot f_{sw} \tag{1.4}$$

1.3. Technology

For this design, the chosen technology process is CMOS14P of NXP Semiconductors. CMOS14P is a 140nm process family for power applications up to 30V. The key technology features of CMOS14P are:

1. Low-resistive substrate.

2. Deep N-wells (can eliminate substrate crosstalk/noise by placing a shield layer below critical analog circuits).
3. Multiple gate oxides.
4. Low-k dielectric materials.
5. High-density logic.
6. Low- and high-voltage transistors (from 1.8V up to 30V).
7. Low leakage transistors (which enables high-temperature operation).

A key advantage of CMOS14P technology process is that it benefits from multiple wells which can shield sensitive analog blocks from substrate crosstalk or noise. Cross-sections of both NMOS and PMOS low-voltage transistors is illustrated in Fig. 1.3.

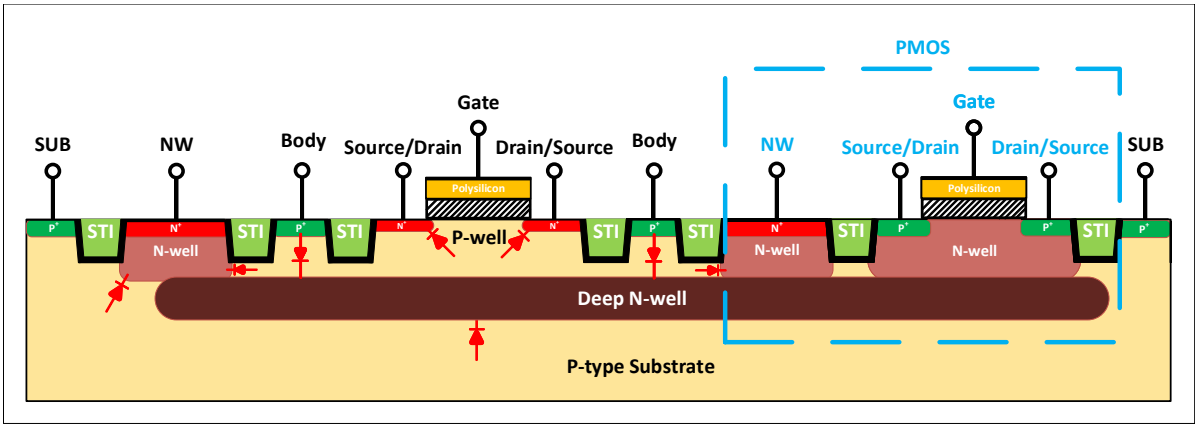

Figure 1.3: Low-voltage Deep N-well NMOS and PMOS Transistors Cross-Section

The P-type substrate is shared by all the circuits on the respective wafer and any noise coming from the switching activity of the digital blocks can affect sensitive analog blocks, such as current mirrors or differential pairs. It is important to note that only NMOS transistors are affected by the aforementioned effects, as a PMOS transistor is already shielded by the N-well that serves as its substrate (or body). To fix this issue, a deep N-well (DNW) is used to shield (or isolate) the NMOS from the noisy P-type substrate. An isolated P-well serves then as a noise-free substrate for the NMOS transistor. It can also be observed in Fig. 1.3 that the DNW is connected to the N-well body of the PMOS transistor. Additionally, this feature allows the bulk of the NMOS to be connected to arbitrary potentials, i.e., usually ground or tied to the source such that the body effect is eliminated. Shallow trench isolation (STI) is applied to isolate transistors from each other.

Parasitic diodes are also highlighted in Fig. 1.3. DNW is typically connected to a high voltage potential to ensure that the diodes are reverse-biased. The P-type substrate is always connected to the lowest potential available. Since the P-type substrate is shared by all the circuits on the wafer, it is crucial to reverse-bias the parasitic diodes to isolate the devices between each other.

It is important to mention that the CMOS14P process includes high-voltage PMOS transistors up to 16V whereas the high-voltage NMOS transistors includes a 30V model. The cross-section of a high-voltage NMOS transistor is illustrated in Fig. 1.4.

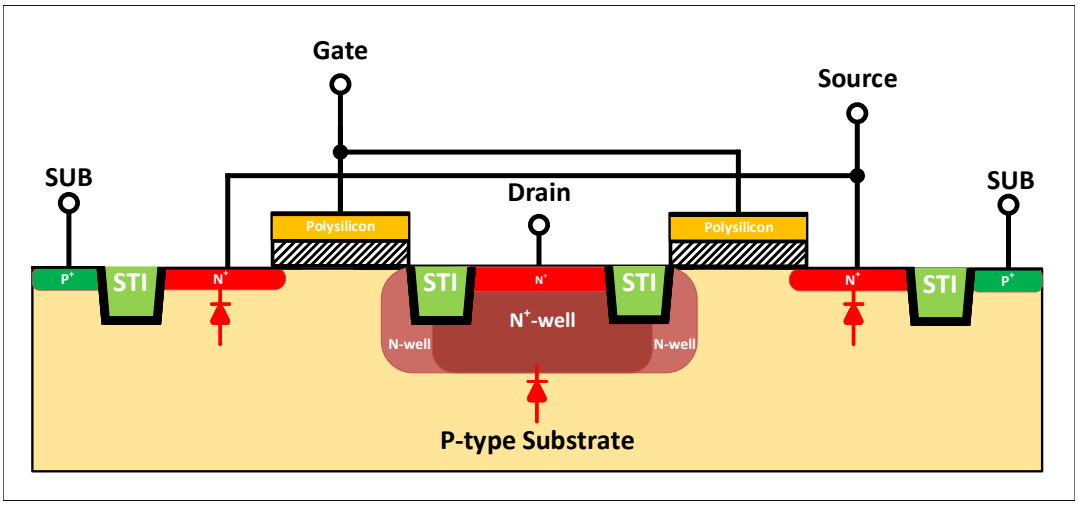

Figure 1.4: High-voltage NMOS Transistor Cross-Section

Low-voltage transistors are symmetrical, meaning that the source and drain can be exchanged without changing the behavior of the transistor. The construction of a high-voltage transistor is different. The drain is now separated from the channel by a lightly doped N-well that prevents the voltage on the drain to appear across the sensitive gate oxide. Therefore, high-voltage transistors are not symmetrical.

In the CMOS14P process, 20V/30V NMOS transistors do not benefit from shielding layers. Thus, the aforementioned devices will always have their body, the P-type substrate, connected to the lowest available potential meaning that the transistors will suffer from the body effect.

1.4. Research Objectives & Targets

A higher integration level of LVRs requires eliminating the large external (off-chip) capacitor. Although beneficial for the area, the key parameters that describe the performance of a LVR (i.e., stability, quiescent current consumption, loop bandwidth, and transient response, described in Chapter 2, Section 2.6.3, have all been degraded.

The correct functionality of the LLC resonant converter imposes a limited supply voltage variation for the power control integrated circuit between 7V and 18V. Current generations of NXP Semiconductors power control integrated circuits for PF control and resonant control use multiple integrated LVRs for generation of 1.8V up to 5V regulated voltages.

The objectives of this work are summarized in the following:

- Multiple voltage levels are required:
  - Aiming to reduce the chip area consumed by the LVRs is the first objective of this work.
  - To meet efficiency regulations during standby/low-power mode, a limited amount of quiescent current is allowed for each LVR. An architecture that has a fast transient response with a low quiescent current reveals the second objective of this work.

- For some internal voltages, the load current or capacitive loading can vary significantly. To achieve maximum area efficiency, providing an architecture that is scalable in terms of the load current and the load capacitance highlights the third objective of this work.

According to the requirements, the targeted design specifications are listed in Table 1.1.

Table 1.1: Table of Specifications

Symbol	Parameter	Min	Typ.	Max	Unit
V_{IN}	Input Voltage	7.0	–	18	V
V_{OUT}	Output Voltage	1.65	1.8	1.95	V
ΔV_{OUT}	Dynamic Load Regulation	-8.33	–	8.33	%
I_Q	Quiescent Current (I_L = 0, w/o band-gap)	–	–	10μ	A
I_L	Load Current	0	–	10m	A
Area	–	–	–	0.0353	mm^2
C_L	Load Capacitance	50	–	300	pF

1.5. Thesis Outline

This thesis project entails the conceptual analysis, architecture design, and circuit design of the proposed linear voltage regulator. The rest of this thesis report is organized as follows:

Chapter 2 introduces the working principle of fully integrated linear voltage regulators, followed by a detailed description of the key parameters, and ends with the associated output stage choice problems, and solutions.

Chapter 3 presents the novelty of this work, i.e., a comprehensive mathematical description of current amplifier-based LVRs, comprising design limitations, improvements and conclusions.

Chapter 4 provides the final schematic implementation of the LVR, highlights the compactness and scalability of the design, presents the simulation results and the comparison with state-of-the-art designs.

Chapter 5 summarizes this project, offers conclusions, and proposes a research direction for future works.

2

Fully Integrated Linear Voltage Regulators

In this chapter, the generic NMOS and PMOS topologies of LVRs will be used as a mean to introduce the static and dynamic state specifications. At the end of the chapter, the main design challenge of the target LVR is addressed. Small-signal derivations are detailed in Appendix B.1.

2.1. Static State Specifications

Generic LVR static state specifications are described in this section.

2.1.1. Quiescent Current

The quiescent current, I_Q, is defined as the current consumed by the LVR's control circuits.

The power efficiency, η, of a linear voltage regulator can be expressed as in Eq. (2.1), where I_{LOAD} is the current flowing into the load and V_{DO} = V_{IN} - V_{OUT} is the dropout voltage.

$$\eta = \frac{E_{DELIVERED}}{E_{SUPPLIED}} = \frac{V_{OUT} \cdot I_{LOAD}}{V_{IN} \cdot (I_{LOAD} + I_Q)} = \left(1 - \frac{V_{DO}}{V_{IN}}\right) \cdot \frac{I_{LOAD}}{I_{LOAD} + I_Q} \tag{2.1}$$

It can be observed that the efficiency can be increased by reducing V_{DO} and/or I_Q.

2.1.2. Line Regulation

Line regulation represents the ability of a regulator to withstand static variations from its supply. It is defined as the gain between the regulated output and input supply $\Delta V_{OUT}/\Delta V_{IN}$.

2.1.3. Load Regulation

The load regulation is defined as the static output voltage variation, V_X, in response to static load current changes, I_X.

2.2. Dynamic State Specifications

The ability of a LVR to withstand supply voltage and load current transients is the defining quality factor of a regulator. The output voltage spike and recovery time directly affect the LVR's output accuracy, therefore, small output voltage variations, i.e., voltage overshoot, voltage undershoot and fast recovery time are desired and must be within the specified limits in order to prevent causing permanent damage to the IC.

The output voltage spikes occur in large signal domain, where strong non-linear slewing effects occur and this makes the analysis not trivial and difficult to accurately define the transient behavior [9].

2.2.1. Load Transient Response

Load transient response is defined as the LVR's ability to regulate the output voltage during fast load transients. The circuits loaded by the LVRs can unpredictably fast draw large currents. Therefore, it is crucial that the LVR's load transient response does not cause large overshoot/undershoot peak voltages, which could permanently damage the IC. A fast settling time is also desired due to its dependency on the overshoot/undershoot peaks [9].

2.2.2. Line Transient Response

Line transient response is the regulated output voltage variation in response to sudden changes in the the supply voltage (V_{IN}). The most important parameters that describe the line transient response are the settling time of the output voltage when a line transient occurs and overshoot/undershoot peak of the output voltage.

2.3. High Frequency Behavior

2.3.1. Power Supply Rejection

The power supply rejection (PSR) of a LVR can be defined as the ability to maintain a constant output voltage, V_{OUT}, in the presence of a noisy supply voltage, V_{IN}.

In comparison with static state line regulation specification, power supply rejection ratio is in AC domain and can be defined as:

$$PSRR = \left| 20log_{10}\left(\frac{V_{OUT}}{V_{IN}}\right)\right| \tag{2.2}$$

In the low frequency range, the supply variation that appears at the output can be treated as a DC component, which is actually represented by the line regulation ability of the LVR. As frequency increases, more noise or ripple from the supply line will show up at the output of the regulator [9]. Using a cascode transistor between the supply line and the pass device not only improve line regulation and the line transient response, it also improves PSR.

2.3.2. Noise

The output noise is an important specification when the LVR is driving a noise sensitive analog/RF block. In this design, the noise requirement is included in the output voltage accuracy. The equivalent input referred voltage noise spectral density sources are portrayed in Fig. 2.1.

The noise of a LVR consists of three main contributors:

1. Band gap reference power spectral density (PSD), $\overline{V^2_{n,BG}}$,
2. Feedback elements PSD, $\overline{V^2_{n,R_{EQ}}}$,
3. LVR circuit PSD, $\overline{V^2_{n,LVR}}$.

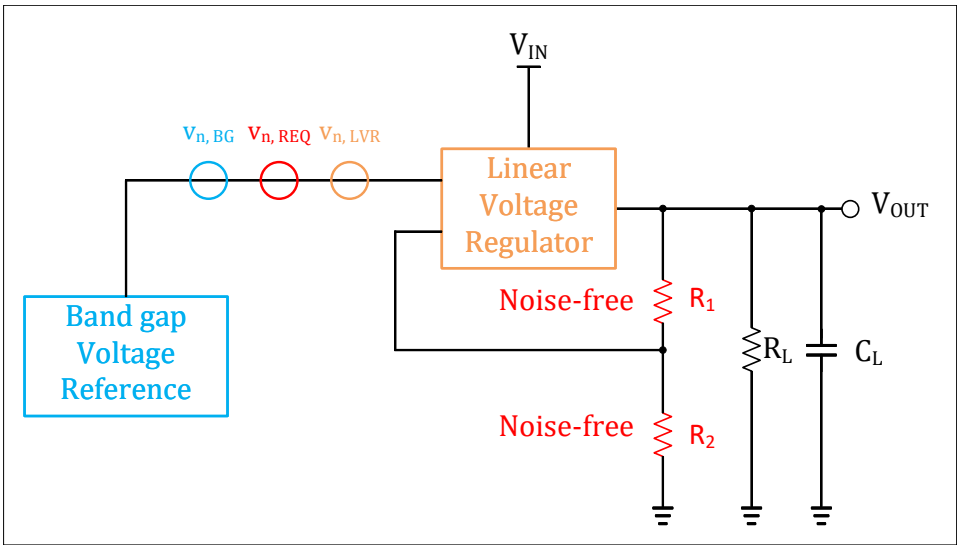

Figure 2.1: Equivalent Input Referred Voltage Noise Spectral Density Sources of a LVR

In LVRs, the most commonly used feedback elements are resistors, and in that case, their thermal noise contribution to the input are accounted for as if their parallel connection is in series with the reference voltage source [10]. For a properly designed LVR, the main contributor to noise should be the first stage of the OTA within the LVR [10].

2.4. Frequency Behavior

A LVR employs voltage negative feedback (series-shunt) in order to achieve the desired output voltage level. The main consideration that needs to be taken into account for the LVR design is that stability should be assured for the entire load current range. In other words, the voltage loop gain magnitude should intersect the unity gain bandwidth (UGBW) with a slope of -20dB/decade.

2.4.1. Output Impedance

The small-signal circuits for analyzing the output impedance (or dynamic load regulation) for both pass device options is depicted in Fig. 2.2. The overlap capacitances, C_{GS} and C_{GD}, have been omitted.

The output impedances of the LVRs are given by:

$$Z_{OUT,NMOST}(s) = \frac{\Delta V_X}{\Delta I_X}(s) = \frac{1}{\frac{1}{r_{ds,N}} + \frac{1}{R_1+R_2} + sC_L + \frac{A_V \beta g_{mN} + (1+sR_G C_G) g_{mN}}{1+sR_G C_G}} \tag{2.3}$$

$$Z_{OUT,PMOST}(s) = \frac{\Delta V_X}{\Delta I_X}(s) = \frac{1}{\frac{1}{r_{ds,P}} + \frac{1}{R_1+R_2} + sC_L + \frac{A_V \beta g_{mP}}{1+sR_G C_G}} \tag{2.4}$$

Assuming a very fast load current pulse ($s \to \infty$), the output impedances can be approximated by:

$$\lim_{s\to\infty} Z_{OUT,NMOST}(s) = \lim_{s\to\infty} \frac{\Delta V_X}{\Delta I_X}(s) \approx \frac{1}{sC_L + g_{mN}} \tag{2.5}$$

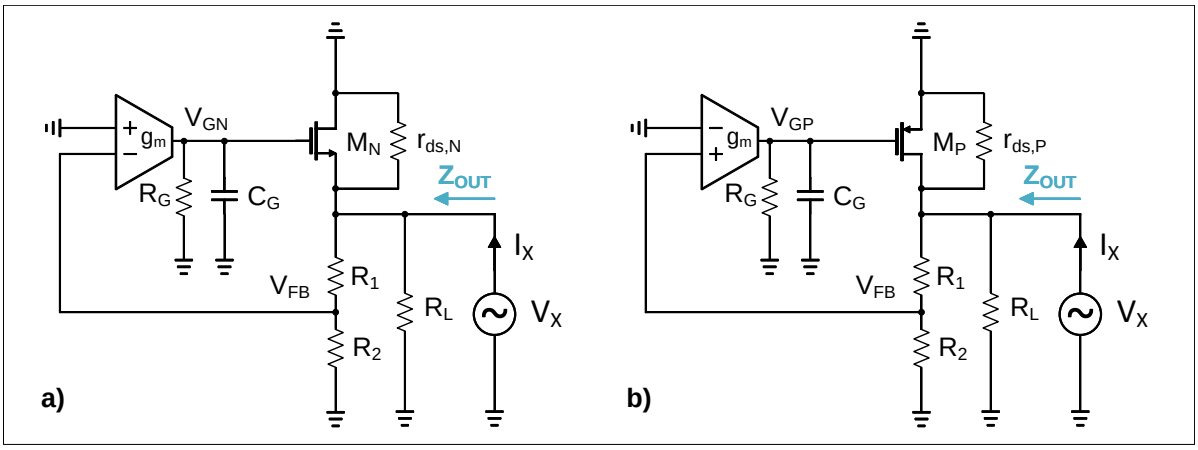

Figure 2.2: Small-signal circuits for output impedance analysis. a) NMOS-based LVR & b) PMOS-based LVR

$$\lim_{s\to\infty} Z_{OUT,PMOST}(s) = \lim_{s\to\infty} \frac{\Delta V_X}{\Delta I_X}(s) \approx \frac{1}{sC_L} \tag{2.6}$$

It can be observed that for the NMOST LVR, the output impedance is much smaller, enabling the regulator to respond faster to load current steps.

2.4.2. NMOST Output Stage

A NMOST output stage LVR with annotated poles and zeros is depicted in Fig. 2.3. The voltage loop gain is sufficient to describe the stability of the system. The calculations are detailed in Appendix B.2.

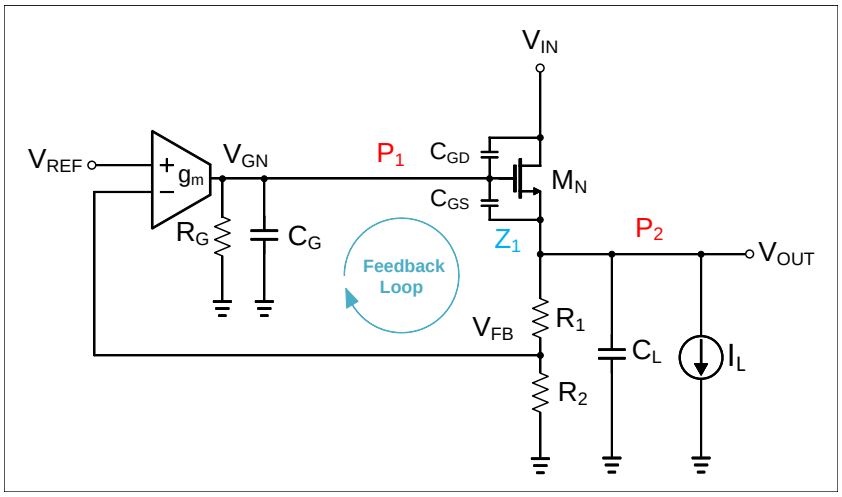

Figure 2.3: NMOS-based LVR

A left half plane zero, Z_1, is generated by the transconductance of transistor M_N and the overlap capacitance, C_{GS}. Its position is given by:

$$\omega_{Z_1} = -\frac{g_{mN}}{C_{GS}}[rad/s] \tag{2.7}$$

The first dominant pole, P_1, is due to the high output impedance of the operational transconductance amplifier (OTA) stage and the capacitance at the gate of the pass transistor and is

located at:

$$\omega_{P_1} = -\frac{1}{R_G C_G}[rad/s] \tag{2.8}$$

By using Miller's approximation, we can define C_G as:

$$C_G = C_{OTA} + C_{GD} + (1 - A_{V,CD}) \cdot C_{GS}[F] \tag{2.9}$$

If the body of M_N is connected to the source of M_N, the body effect can be neglected ($A_{V,CD} = 1$), therefore $C_G = C_{OTA} + C_{GD}$.

The second dominant pole, P_2, is located at:

$$\omega_{P_2} = -\frac{1}{1/g_{mN}||(R_1 + R_2)||R_L \cdot C_L}[rad/s] \tag{2.10}$$

Eq. (2.10) can be further simplified if we assume that:

$$\frac{1}{g_{mN}}||R_L << R_1 + R_2[\Omega] \tag{2.11}$$

Condition (2.11) is true most of the time because both resistors, R_1 and R_2, are in the range of hundreds of kΩ to units of MΩ. Usually, resistor R_2 is chosen in order to bias transistor M_N at a certain current:

$$I_{Q_{M_N}} = \frac{V_{REF}}{R_2}[A] \tag{2.12}$$

Whereas resistor R_1 is chosen in order to meet the desired output voltage:

$$V_{OUT} = \left(1 + \frac{R_1}{R_2}\right) \cdot V_{REF}[V] \tag{2.13}$$

By comparing $1/g_{mN}$ to R_L, we can deduce that:

$$\frac{1}{g_{mN}} = \frac{V_{GS} - V_{TH}}{2I_L} = \frac{V_{OV}}{2I_L} << \frac{V_{OUT}}{I_L} = R_L[\Omega] \tag{2.14}$$

Where V_{OV} is the overdrive voltage of transistor M_N and V_{TH} is the threshold voltage of transistor M_N.

Therefore, Eq. (2.10) can be simplified to:

$$\omega_{P_2} \approx -\frac{g_{mN}}{C_L}[rad/s] \tag{2.15}$$

Comparing ω_{Z_1} with ω_{P_2} and considering that C_{GS} is much smaller than C_L, it can be concluded that Z_1 is a non-dominant zero, making the system a second-order all pole system.

Therefore, we have the first dominant pole located at the gate of the pass transistor and a second dominant pole at the output of the LVR. The position of the output pole, P_2, increases with the load current as given by Eq. (2.15).

The DC loop gain is given by:

$$L_{DC} = -A_V \beta g_{mN} r_{out} = -g_m R_G \cdot \frac{R_2}{R_1 + R_2} \cdot \frac{g_{mN}}{g_{mN} + \frac{1}{r_{ds,N}} + \frac{1}{R_L} + \frac{1}{R_1 + R_2}} \tag{2.16}$$

The last term in Eq. (2.16) can be approximated to 1, meaning that the DC loop gain is given only by the feedback network and the OTA, hence, increasing I_L from $I_{L,min}$ to $I_{L,max}$ does not affect the DC loop gain.

A conceptual bode plot of the voltage loop gain magnitude is depicted in Fig. 2.4.

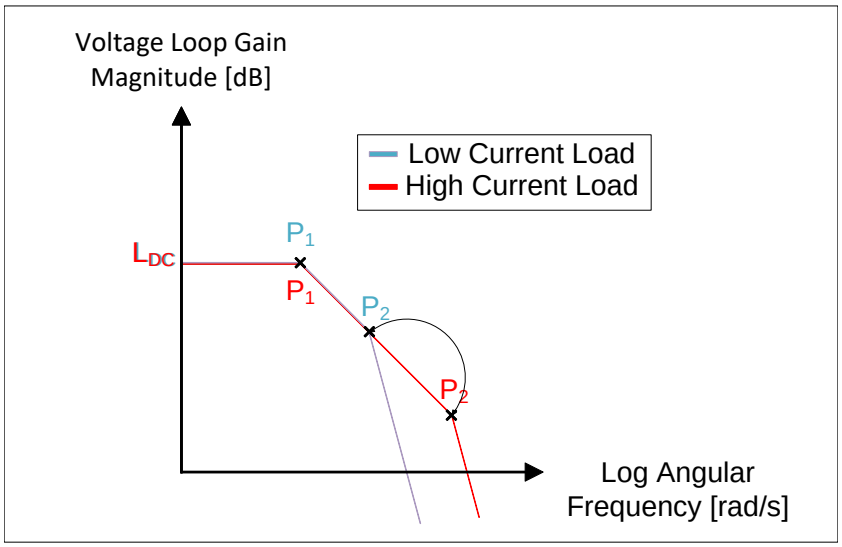

Figure 2.4: NMOS-based LVR - Conceptual Loop Gain Bode Plot - Poles Movement

2.4.3. PMOST Output Stage

A PMOST output stage LVR with annotated poles and zeros is depicted in Fig. 2.5.

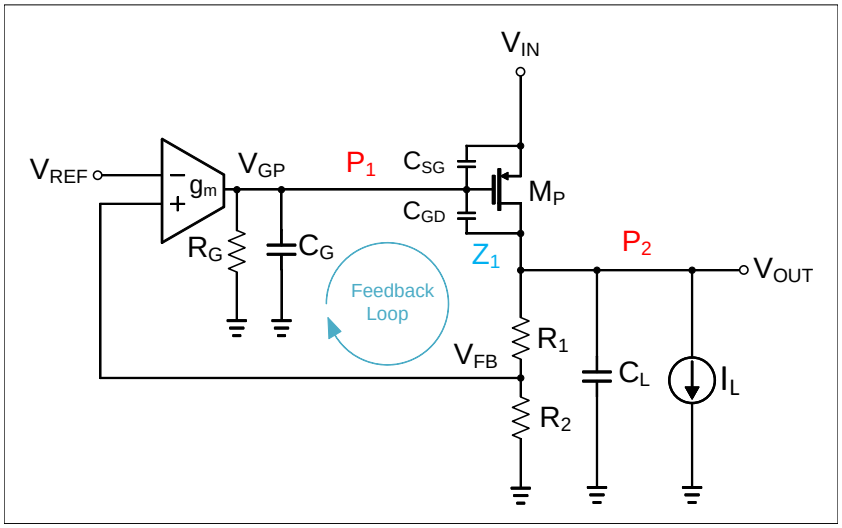

Figure 2.5: PMOS-based LVR

A right half plane zero, Z_1, is generated by the transconductance of transistor M_P and the overlap capacitance, C_{GD}. Its position is given by:

$$\omega_{Z_1} = \frac{g_{mP}}{C_{GD}} [rad/s] \tag{2.17}$$

The first dominant pole, P_1, is due to the high output impedance of the OTA stage and the capacitance at the gate of the pass transistor and is located at:

$$\omega_{P_1} = -\frac{1}{R_G C_G}[rad/s] \tag{2.18}$$

By using Miller's approximation, we can define C_G as:

$$C_G = C_{OTA} + C_{GS} + (1 - A_{V,CS}) \cdot C_{GD} = C_{OTA} + C_{GS} + (1 + g_{mP} r_{ds,P}) \cdot C_{GD}[F] \tag{2.19}$$

C_{GD} will be found at the output node as:

$$C_{GD,OUT} = C_{GD} \cdot \left(1 - \frac{1}{A_{V,CS}}\right) \approx C_{GD}[F] \tag{2.20}$$

The second dominant pole, P_2, (neglecting C_{DB}) is located at:

$$\omega_{P_2} = -\frac{1}{r_{ds,P} C_L}[rad/s] \tag{2.21}$$

The output impedance of transistor M_P can be written as:

$$r_{ds,P} = \frac{\partial V_{DS,P}}{\partial I_{DS,P}} = \frac{L_P}{\lambda I_{DS,P}}[\Omega] \tag{2.22}$$

Where: λ is a process dependent parameter and denotes the channel length modulation effect.

Therefore, Eq. (2.21) can be rewritten as:

$$\omega_{P_2} = -\frac{\lambda I_L}{L_P \cdot C_L}[rad/s] \tag{2.23}$$

Similar to the NMOST LVR, the second pole's location moves with the load current. Considering that $C_{GD} << C_L$, it can be concluded that Z_1 is a non-dominant zero, making the system a second-order all pole system.

The DC loop gain is given by:

$$L_{DC} = -A_V \beta g_{mP} r_{out} = -g_m R_G \frac{R_2}{R_1 + R_2} \cdot g_{mP} \cdot r_{ds,p} || R_L || (R_1 + R_2) \tag{2.24}$$

Usually, in PMOST LVR designs, the PMOS transistor is designed for very low $r_{ds,P}$, which allows for low-dropout regulation, therefore, Eq. (2.24) can be simplified to:

$$L_{DC} = -g_m R_G \frac{R_2}{R_1 + R_2} \cdot g_{mP} \cdot r_{ds,P} \tag{2.25}$$

In order to analyze the effect of the load current on the loop gain, we can substitute $g_{mP} = \sqrt{2KI_L}$ and $r_{ds,P} = L/(\lambda I_L)$ in Eq. (2.25):

$$L_{DC} = -g_m R_G \frac{R_2}{R_1 + R_2} \cdot \sqrt{2K} \cdot \frac{1}{\lambda \sqrt{I_L}} \tag{2.26}$$

Eq. (2.26) reveals that the loop gain reaches the highest value at low current load and that it reaches the lowest value at high current load, effect that is illustrated in Fig. 2.5.

A conceptual bode plot of the voltage loop gain magnitude is depicted in Fig. 2.6.

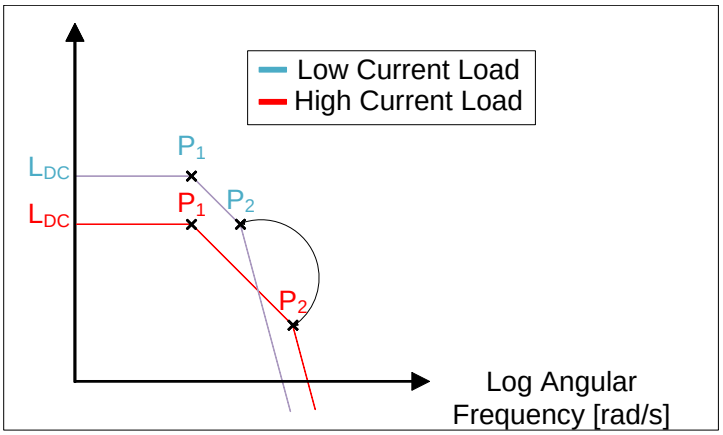

Figure 2.6: PMOS-based LVR - Conceptual Loop Gain Bode Plot - Poles Movement

2.5. Pass Device Choice

The performance and characteristics of both NMOST and PMOST implementations for the pass device are given in Table 2.1.

Table 2.1: Pass Devices Comparison

Pass Device	NMOST	PMOST
Configuration	Common Drain	Common Source
Line Regulation $\left[\frac{V}{V}\right]$	$\frac{1}{A_V \beta g_{m,pass} r_{ds,pass}}$	$\frac{1}{A_V \beta}$
Load Regulation $\left[\frac{V}{A}\right]$	$-\frac{1}{A_V \beta g_{m,pass}}$	$-\frac{1}{A_V \beta g_{m,pass}}$
DC Loop Gain	$-A_V \beta$	$-A_V \beta g_{m,pass} r_{ds,P}$
P_1 [rad/s]	$-\frac{1}{R_G C_G}$	$-\frac{1}{R_G C_G}$
P_2 [rad/s]	$\approx -\frac{g_{m,pass}}{C_L}$	$-\frac{1}{r_{ds,pass} C_L}$
(Non-dominant) Z_1 [rad/s]	$-\frac{g_{m,pass}}{C_{GS}}$	$\frac{g_{m,pass}}{C_{GD}}$

A NMOST is chosen as the pass device for this design because it offers improved line regulation, lower output impedance, no accuracy degradation in the voltage feedback loop gain along with higher current capability ($\mu_{e^-} > \mu_{e^+}$) for a smaller area.

2.6. Transient Behavior

2.6.1. Capacitive Division

In addition to output voltage variation caused by load current steps, there is an additional voltage step caused by a capacitive division between C_G and C_{GS}. The effect is illustrated in Fig. 2.7. Because of the capacitive division, node V_{GN} will move in the same direction as V_{OUT} before recovering.

This effect can be mitigated by placing an additional capacitor in order to increase C_G. The equation that governs this effect (detailed in Appendix B.3) is given by:

$$\lim_{s \to \infty} \frac{\Delta V_{GN}}{\Delta V_{OUT}}(s) = \frac{C_{GS}}{C_G + C_{GS}} \tag{2.27}$$

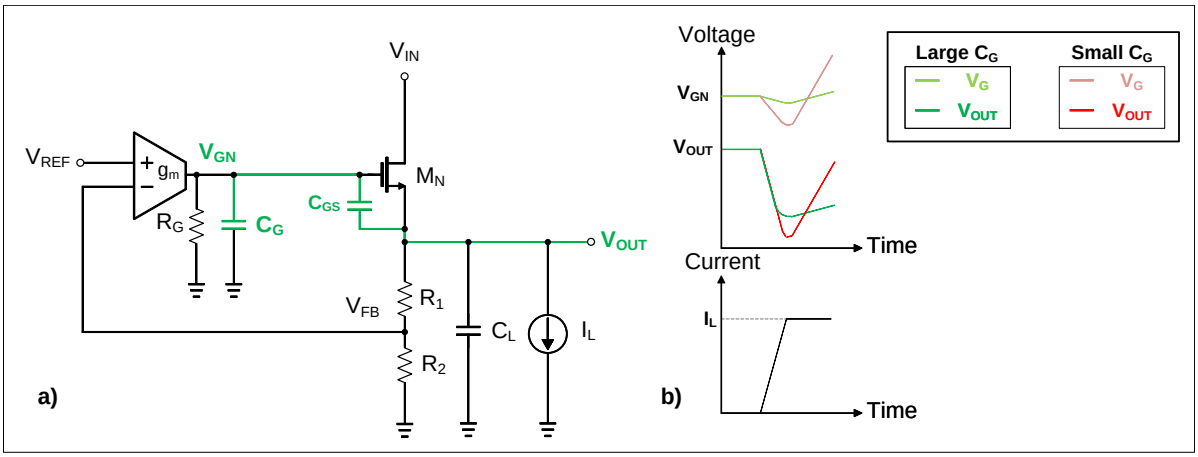

Figure 2.7: a) NMOS-based LVR- Capacitive Division & b) Capacitive Division Transient Waveforms

The trade-offs for this method are:

- The slew rate at node V_{GN} will decrease, according to:

$$\frac{\Delta V_{GN}}{\Delta t} = \frac{I_{SR}}{C_G}\left[\frac{V}{s}\right] \tag{2.28}$$

- In addition, the bandwidth of the voltage loop is effectively decreased, as illustrated in Fig. 2.8.

Fortunately, the performance degrading consequences of mitigating the capacitive division effect can be improved by applying the adaptive biasing technique, which will be discussed in detail in Chapter 3.

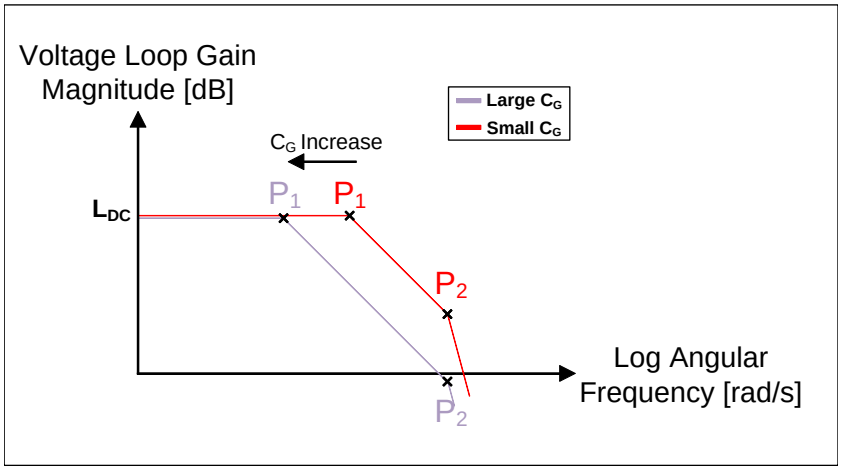

Figure 2.8: Capacitive Division Mitigation - Loop Bandwidth Reduction Effect

2.6.2. Consecutive Load Current Steps

Because of the limited amount of quiescent current allowed for this design, the feedback resistors, R_1 and R_2 along with the load capacitance, C_L, can constitute a large time constant, $\tau = (R_1 + R_2) \cdot C_L$, in the order of tens of μs.

An undesired effect might happen in the following scenario: assuming that the LVR is recovering from a negative load current step and that the time constant is very large, the gate potential, V_G, will be discharged, in some cases, below V_{OUT}, effectively turning transistor M_N OFF. If a positive load current step then occurs at the point where V_G is at its minimum value, V_{OUT} will face a very large undershoot voltage peak. This effect is illustrated in Fig. 2.9.

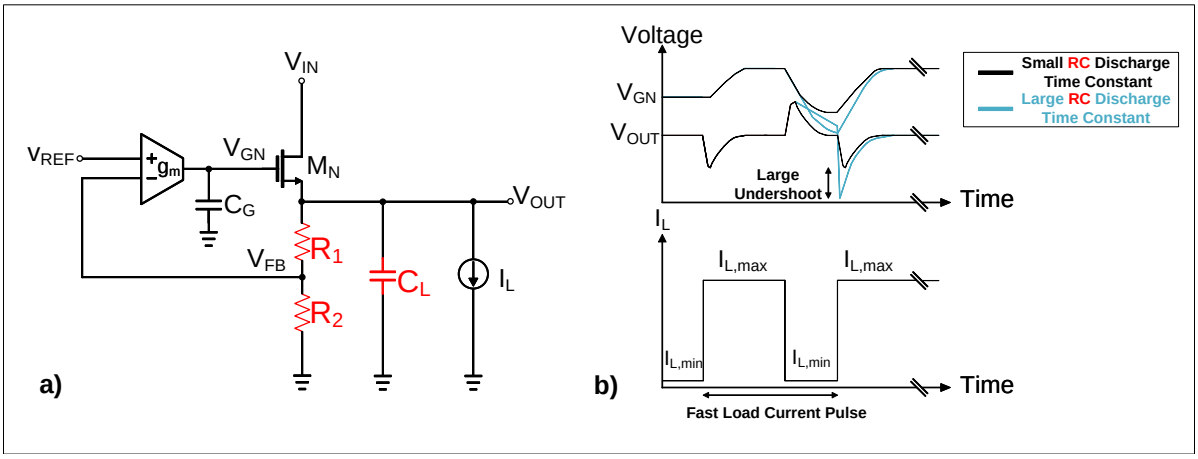

Figure 2.9: a) NMOS-based LVR & b) RC Time Constant - Transient Waveforms

A LVR that consists only of an OTA, the feedback network and a NMOST output stage does not have any other discharge path besides R_1, R_2 and C_L. Therefore, in order to mitigate this effect, another discharge path ought to be implemented. One possible implementation is to replace the NMOST common drain output stage with a common drain push-pull output stage. In this way, the output node, V_{OUT}, will be discharged via the PMOST only during negative load current stepts, as shown in Fig. 2.10.

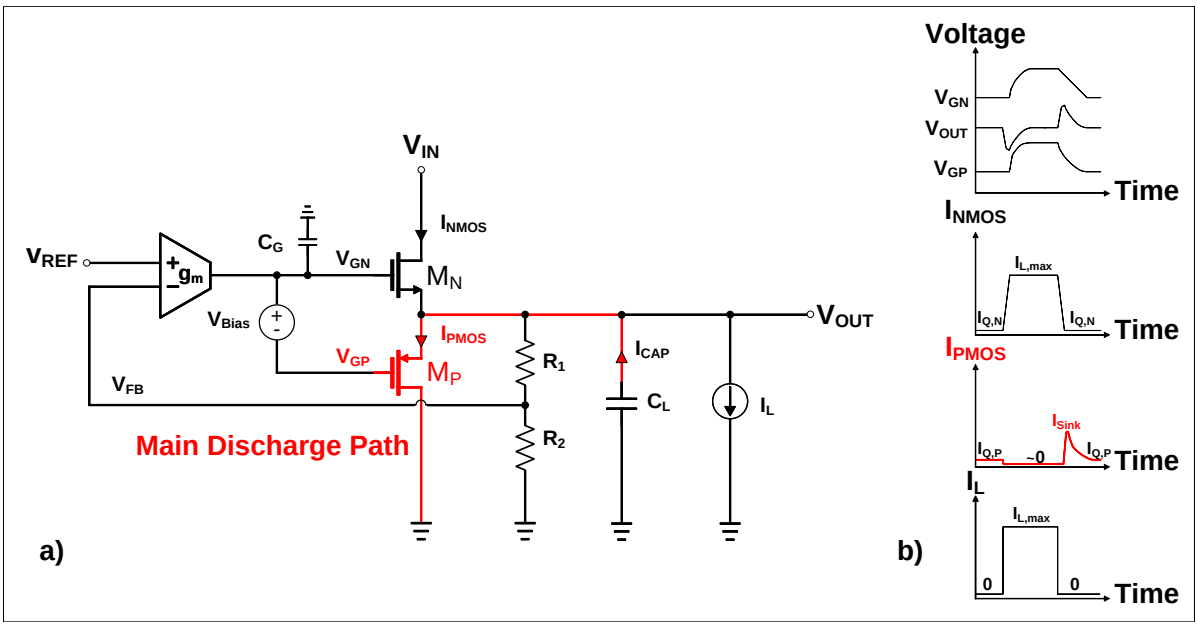

Figure 2.10: a) NMOS-based LVR with Push-Pull Stage & b) Transient Waveforms

The classical CMOS implementation for the common-drain class AB push-pull stage is depicted in Fig. 2.11 [11]:

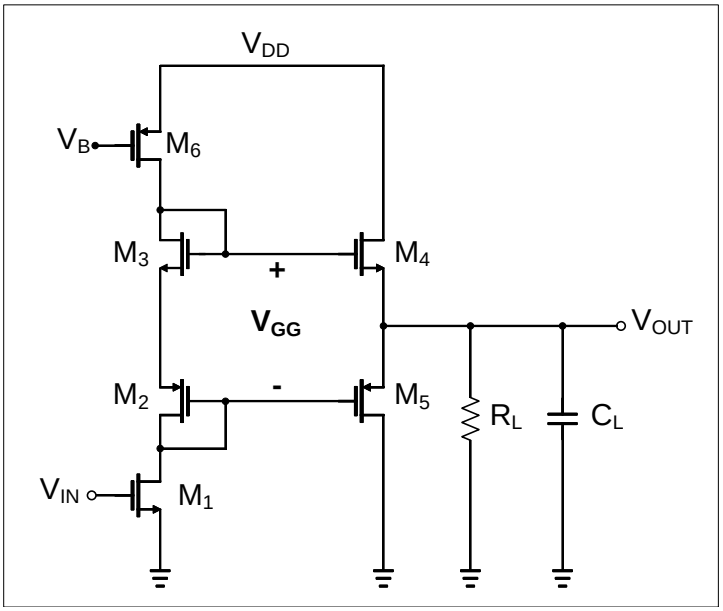

Figure 2.11: Common-Drain Class AB Output Stage

Where:

$$V_{GG} = V_{GS3} + V_{SG2} = V_{GS4} + V_{SG5} \tag{2.29}$$

$$V_{GS3} + V_{SG2} = \sqrt{\frac{2I_B}{\mu_n C_{ox}\left(\frac{W}{L}\right)_3}} + V_{TH3} + \sqrt{\frac{2I_B}{\mu_p C_{ox}\left(\frac{W}{L}\right)_2}} + V_{TH2} \tag{2.30}$$

$$V_{GS4} + V_{SG5} = \sqrt{\frac{2I_{M4}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_4}} + V_{TH4} + \sqrt{\frac{2I_{M5}}{\mu_p C_{ox}\left(\frac{W}{L}\right)_5}} + V_{TH5} \tag{2.31}$$

Equating the previous two equations yields:

$$\sqrt{\frac{2I_B}{\mu_n C_{ox}\left(\frac{W}{L}\right)_3}} + \sqrt{\frac{2I_B}{\mu_p C_{ox}\left(\frac{W}{L}\right)_2}} = \sqrt{\frac{2I_{M4}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_4}} + \sqrt{\frac{2I_{M5}}{\mu_p C_{ox}\left(\frac{W}{L}\right)_5}} \tag{2.32}$$

Assuming quiescent point operation, that is $I_{M4} = I_{M5} = I_Q$ and $V_{OUT} = 0$, then:

$$I_Q = I_B \cdot \left[\frac{1/\sqrt{\mu_n C_{ox}(W/L)_3} + 1/\sqrt{\mu_p C_{ox}(W/L)_2}}{1/\sqrt{\mu_n C_{ox}(W/L)_4} + 1/\sqrt{\mu_p C_{ox}(W/L)_5}} \right]^2 \tag{2.33}$$

If we also assume that the transistors are matched, that is:

$$\mu_n C_{ox}(W/L)_3 = \mu_p C_{ox}(W/L)_2 \tag{2.34}$$

$$\mu_n C_{ox}(W/L)_4 = \mu_p C_{ox}(W/L)_5 \tag{2.35}$$

Then:

$$I_Q = I_B \cdot \frac{(W/L)_4}{(W/L)_3} \tag{2.36}$$

In this design, the quiescent current of transistor M_5 in Fig. 2.11 is chosen to be twice as large ($\approx 1\mu A$) as the bias current ($0.5\mu A$) supplied by transistor M_6. It should be noted that the effective transconductance of the output stage becomes $G_m = g_{m5} + g_{m4}$. The push-pull stage slightly increases the transconductance of the second stage of the OTA [10].

2.6.3. Response Time

The most challenging aspect of the design is to achieve a load current step response with minimal overshoot/undershoot peaks in the output voltage with the following constraints:

- Small load capacitance (C_L = 50pF),
- Limited quiescent current ($I_{Q,max}$ = 10μA),
- Minimal controller area.

In [12], the response time has been defined as:

$$T_R = \frac{C_L \cdot \Delta V_{OUT}}{\Delta I_L}[s] \tag{2.37}$$

Where:

- ΔV_{OUT} represents the change in V_{OUT}, i.e, either the undershoot or overshoot peak voltage,
- ΔI_L represents the change in the output current, I_L.

Eq. (2.37) highlights the transient performance degradation for fully integrated LVRs, as opposed to an external load capacitor LVR (up to 10^6 order of magnitude difference in C_L: pF $\implies$ μF) and is usually used to determine the required response time in order to achieve a certain undershoot/overshoot in V_{OUT} for a given load current step variation.

In [13], the response time of a LVR has been further detailed as:

$$T_R \approx \frac{1}{BW_{CL}} + C_G \cdot \frac{\Delta V_G}{I_{SR}}[s] \tag{2.38}$$

Where:

- BW_{CL} represents the closed-loop bandwidth of the LVR negative feedback,
- ΔV_G represents the voltage variation at the gate of the power transistor,
- I_{SR} represents the slew rate current of the output stage of the EA that drives the capacitance at the gate of the pass device, C_G.

The slew rate current, I_{SR}, can be enhanced by using a push-pull stage, making use of the current amplification ability [14]. The response time, T_R, can be improved (i.e., reduced) by using an adaptive biasing scheme in order to enhance the closed-loop bandwidth of the LVR during load step transients while also increasing the slew rate current, I_{SR}.

3

Current Amplifier-based Linear Voltage Regulator

The work presented in this chapter is complementary to a patented implementation of a current amplifier-based LVR (CA LVR) [15], in the sense that it develops a theoretical framework that contains comprehensive mathematical insight(i.e., provides design equations) and proposes suggestions for improvements.

This chapter starts with the generalized concept of CA LVRs, an overview of the prior art and its application. The subsequent sections introduce the working principle of CA LVRs and its simplest implementation. Various implementations are all built on the previous, highlighting the performance improvement and their associated design trade-offs (where applicable). The last two sections of this chapter describe the working principle and the implementation of a technique called adaptive biasing, that can be applied to all CA implementations, followed by the conclusions of this chapter.

3.1. Concept & Prior Art

The concept of a current amplifier-based LVR is illustrated in Fig. 3.1 [15].

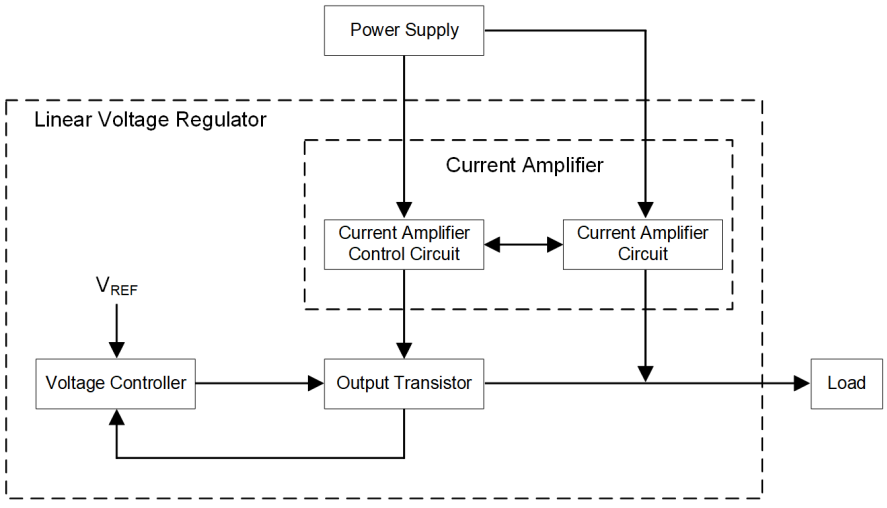

Figure 3.1: Current Amplifier-based LVR - Concept

The concept was initially implemented via external, discrete components, around an integrated LVR, as illustrated in Fig. 3.2 [16], in order to boost the current capability of the LVR in cases where the output capability of the integrated LVR was insufficient (for example, the load requires 10x more current than what the LVR can handle). Transistor Q_1 is controlled by the voltage drop generated across the sense resistor, R_1. The voltage drop is caused by the current that the regulator is supplying to the load. When the regulator current, I_{REG} in Fig. 3.2, is high enough (i.e., $I_{REG} > V_{BE,Q1}/R_1$), transistor Q_1 will become biased and will be able to provide the extra current that the load requires.

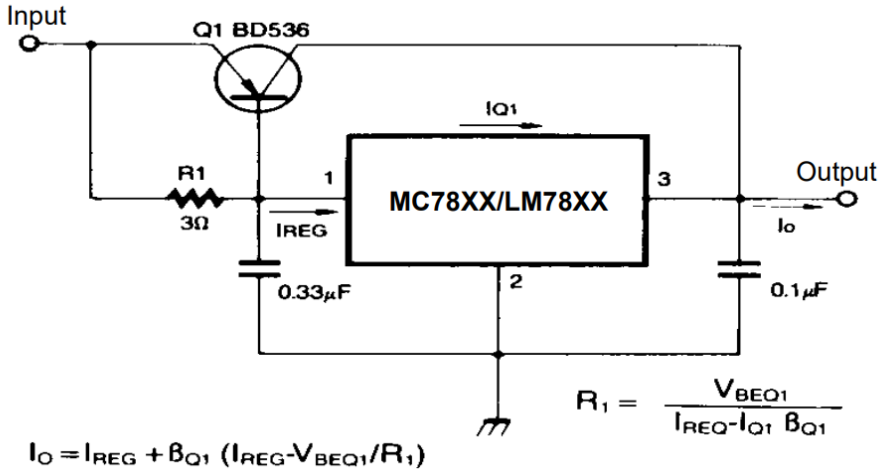

Figure 3.2: Current Boosted LVR [16]

The value of the sense resistor can be chosen such that, when the integrated LVR reaches its maximum current capability, the voltage drop generated across the sense resistor would turn transistor Q_1 ON, providing the additional required current.

3.2. Principle of Operation

Taking the idea further, integrating the current amplifier and using a local feedback output stage (NMOST in the common drain configuration) can greatly improve the transient response of the LVR. The idea, using a 180nm GPDK, is illustrated in Fig. 3.3. The overshoot/undershoot voltage spikes in V_{OUT} depend on the $I_{DS}vs.V_{GS}$ curve of the output NMOST. The transient performance is enhanced by the fact that the current variation ΔI_{DS} in transistor M_N can be reduced by a factor equal to the CA gain, which in turn decreases the amount of ΔV_{GS} required to sustain ΔI_{DS}/K, and therefore, reduces the amount of undershoot and overshoot that the LVR suffers from during load current steps. The condition for the CA to be effective is to design a threshold below which the CA loop gain is zero.

A first design consideration can be derived from the I_{DS} vs. V_{GS} plot of transistor M_N in Fig. 3.3, i.e., transistor M_N should be designed to operate in the deep weak inversion / subthreshold in order to maximize the transconductance efficiency (g_m/I_{DS}). In the following sections, practical implementations of CA LVRs will be presented in detail.

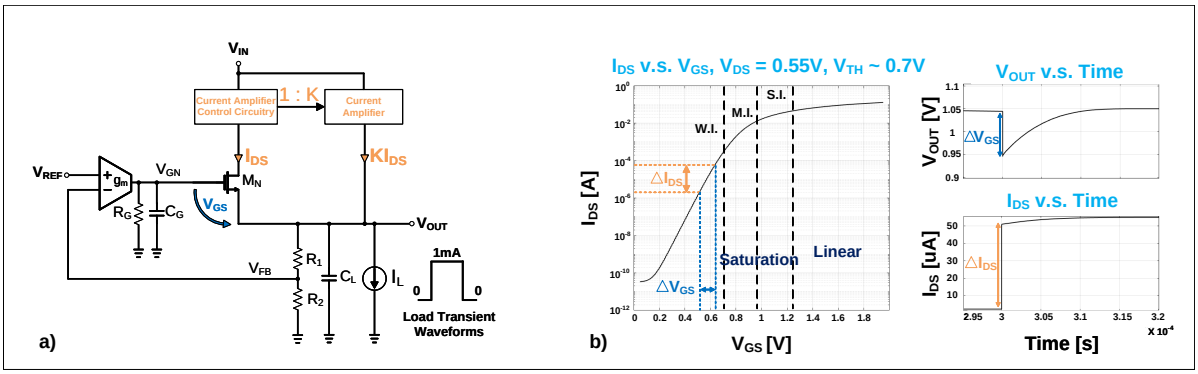

Figure 3.3: a) Current Amplifier-based NMOST LVR & b) Mechanism Illustrated for Current Gain = 20

3.3. Current Amplifier - Type I

The simplest CMOS implementation of a current amplifier-based LVR is depicted in Fig. 3.4. The sense resistor, R_A, and transistor M_2 form the additional current path from the supply to the load.

3.3.1. Qualitative Analysis

The current loop formed by M_N, M_2 and R_A is able to react very fast to sudden changes in I_L, greatly aiding the transient response of the LVR.

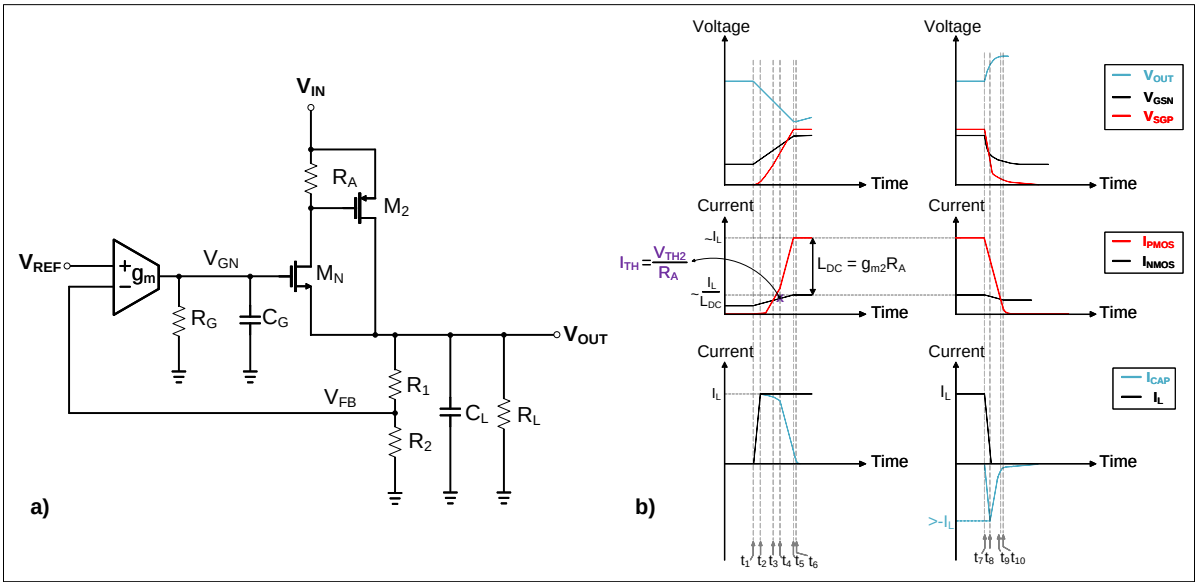

Figure 3.4: a) Current Amplifier-based LVR - Type I & b) Conceptual Transient Waveforms

Load Current Step Transient Response:

1. t ≤ t_1:
   - At t < t_1, the LVR is in its quiescent state: $I_L = 0$.
   - At t_1 a very high speed load current pulse is being applied.
2. t ≤ t_2

- At t = t_2, the load current, I_L, reaches its maximum value.
- The LVR is unable to react to such fast current pulses. The load current will be provided by the charge stored on C_L.
- Node V_{OUT} will be discharged with a current that has the same rate of change as I_L.
- Node V_{GN}, apart from the capacitive crosstalk between C_G and C_{GS}, remains constant. V_{GSN} thus increases.

3. t ≤ t_3

   - At t < t_3, the current through transistor M_1 increases causing a voltage drop across resistor R_A, which in turn causes a current to flow through transistor M_2.
   - At t = t_3, $I_{M1} = I_{M2}$.

4. t ≤ t_4

   - At t = t_4, the current through transistor M_1 is large enough to generate a voltage drop across R_A that is equal to the treshold voltage of transistor M_2, therefore biasing M_2 in weak inversion, saturation.

5. t ≤ t_5

   - At t < t_5, the current through transistor M_2 greatly increases as V_{SGP} is increased, delivering most of the load current, I_L.
   - At t = t_5, the current of transistors M_1 and M_2 stabilize according to:

$$I_{M1} + I_{M2} = I_L + I_{CAP} \tag{3.1}$$

   - I_{CAP} is very small at this point and can be neglected in the equation above.
   - The load current distribution between transistors M_1 and M_2 is governed by the current loop gain of the fast loop, $L_{DC} = g_{m2} \cdot R_A$.

$$I_{M1} \approx \frac{I_L}{L_{DC}} \tag{3.2}$$

$$I_{M2} = I_L - I_{M1} \approx I_L - \frac{I_L}{L_{DC}} \tag{3.3}$$

6. t ≤ t_6

   - At t < t_6, the load capacitance, C_L, does no longer have any contribution to I_L.
   - At t = t_6, depending on the speed of the slow loop, V_{OUT} will be brought up to its nominal value.
   - The recovery time of V_{OUT} is governed by the slew rate at node V_{GN}:

$$\frac{\Delta V_{GN}}{\Delta t} = \frac{I_{TAIL}}{C_G} \tag{3.4}$$

   - Where: I_{TAIL} is the bias current of the g_m stage.

7. t ≤ t_7

   - At t < t_7, the LVR is supplying a load current equal to I_L.
   - At t = t_7, the load current suddenly starts to decrease.

8. t ≤ t_8

   - At t < t_8, the LVR is not fast enough to react to the negative load current step (from $I_L \implies 0$) and transistors M_1 and M_2 are charging the output load capacitance resulting in an increase of V_{OUT}.
   - Node V_{GN}, apart from the capacitive crosstalk between C_G and C_{GS}, remains constant. V_{GSN} thus decreases.
   - At t = t_8, the load current reaches its minimum value. It can be observed that the current flowing into the load capacitance reaches a peak at a value lower than $|I_L|$ and can be approximated by a value lower than $|I_{PMOS}|$.

9. t ≤ t_9

   - At t < t_9, the current supplied by M_1 and M_2 decreases significantly.
   - At t = t_9, the current in transistors M_1 and M_2 are equal. The rate at which V_{OUT} is charged decreases.

10. t_{10}

    - At t = t_{10}, V_{OUT} reaches its maximum value.
    - At t > t_{10}, if no discharge circuitry exists, V_{OUT} will recover to its nominal value by discharging via R_1, R_2 and C_L.

The qualitative analysis is similar for all the subsequent CA implementations.

3.3.2. Stability Analysis

In order to deduce design equations, the stability and interaction of the voltage loop and the current loop is analyzed in this subsection, based on the circuit from Fig. 3.5.

- The poles and zeros of the current loop are found at much higher frequencies than the poles and zeros of the voltage loop and therefore, do not interact with the voltage loop.
- Therefore, the voltage loop gain (denoted as L_V) (deduced in Appendix B.4) can be approximated by a simplified expression, given by:

$$L_V(s) = \frac{\beta A_V g_{mN} R_{eq}}{(1 + sC_G R_G) \cdot \left[1 + (sC_L + g_{mN} R_{eq})\right]} \tag{3.5}$$

With:

$$L_{V,DC} \approx \beta A_V \tag{3.6}$$

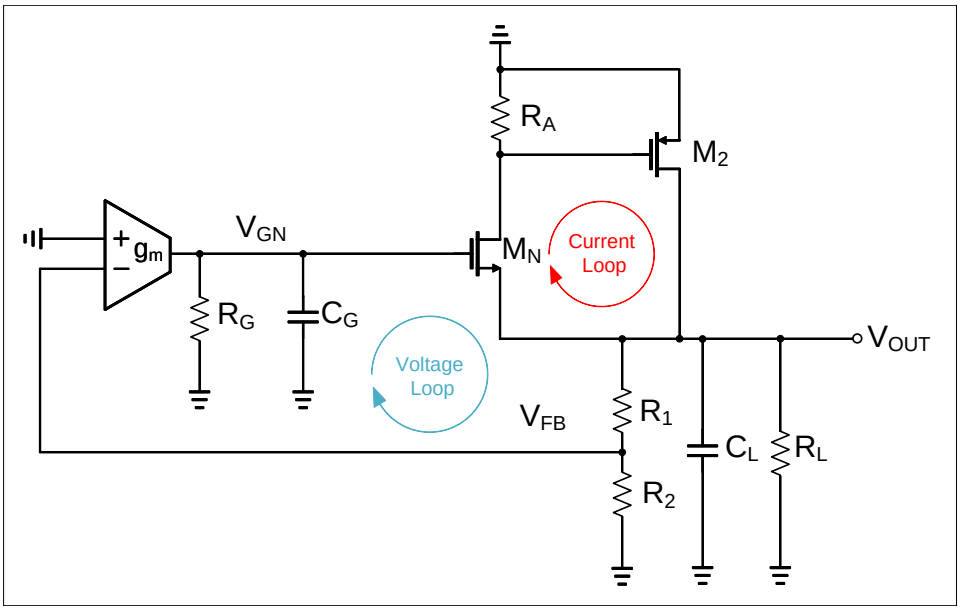

Figure 3.5: CA LVR Type I - Stability Analysis

Where:

- β is the negative feedback gain:

$$\beta = \frac{R_2}{R_1 + R_2} \tag{3.7}$$

- A_V is the voltage gain of the OTA stage:

$$A_V = g_m \cdot R_G \tag{3.8}$$

- R_G is the output impedance of the g_m stage.
- R_{eq} is the equivalent output resistance, given by:

$$R_{eq} = (R_1 + R_2)||R_L||r_{ds2}[\Omega] \tag{3.9}$$

- C_A is the total capacitance between the gate and source of transistor M_2:

$$C_A = C_{sg2}[F] \tag{3.10}$$

The current loop gain (denoted as L_I) (detailed in Appendix B.4) is given by:

$$L_I(s) = \frac{\beta A_V g_{mN} R_{eq} + (1 + sC_G R_G) g_{mN} R_{eq}}{(1 + sC_G R_G)(1 + sC_L R_{eq} + g_{mN} R_{eq}) + \beta A_V g_{mN} R_{eq}} \cdot \frac{g_{m2} R_A}{1 + sC_A R_A} \tag{3.11}$$

With:

$$L_{I,DC} \approx g_{m2} R_A \tag{3.12}$$

Where:

- The first pole is given by:

$$\omega_{P1} = -\frac{\beta g_m g_{mN} R_{eq}}{C_G(1 + g_{mN} R_{eq})}[rad/s] \tag{3.13}$$

- The first zero is given by:

$$\omega_{Z1} = -\frac{1 + \beta A_V}{C_G R_G}[rad/s] \tag{3.14}$$

- The second pole is given by:

$$\omega_{P2} = -\frac{g_{mN} R_{eq} + 1}{C_L R_{eq}}[rad/s] \tag{3.15}$$

- The third, non-dominant, pole is given by:

$$\omega_{P3} = -\frac{1}{C_A R_A}[rad/s] \tag{3.16}$$

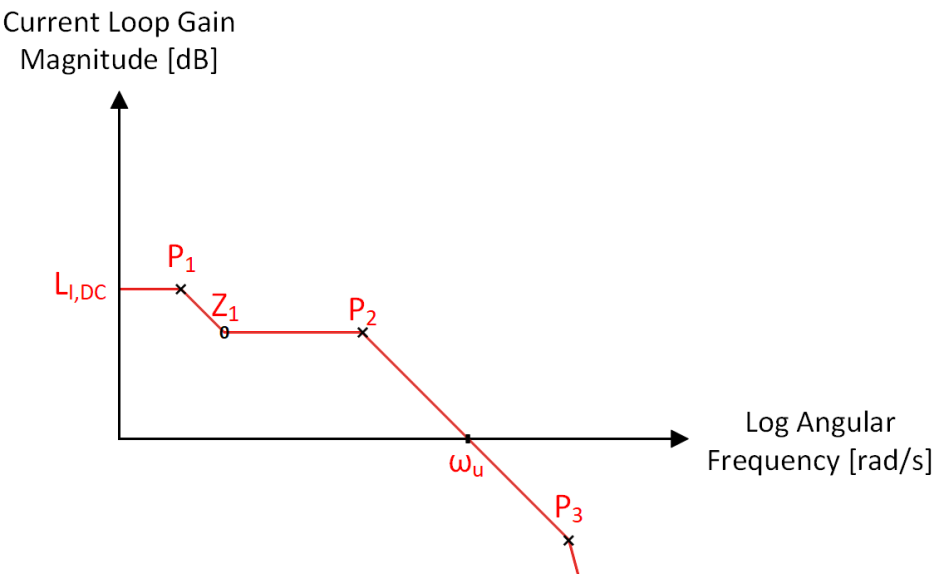

Figure 3.6: CA LVR Type I - Loop Gain Bode Plot

Based on the bode plot from Fig. 3.6, the unity gain frequency can be written as:

$$\omega_u = -L_{I,DC} \cdot \frac{\omega_{P1}}{\omega_{Z1}} \cdot \omega_{P2}[rad/s] \tag{3.17}$$

A phase margin design equation is deduced:

$$PM = 90° - tan^{-1}\left(\frac{\omega_u}{\omega_{P3}}\right) \cdot \frac{180°}{\pi} \tag{3.18}$$

For a phase margin of 60°:

$$30° = tan^{-1}\left(\frac{\omega_u}{\omega_{P3}}\right) \cdot \frac{180°}{\pi} \implies \frac{\pi}{6} = tan^{-1}\left(\frac{\omega_u}{\omega_{P3}}\right) \tag{3.19}$$

Leading to:

$$\frac{\omega_{P3}}{\omega_u} = \sqrt{3} \implies L_{I,DC} = \frac{1}{\sqrt{3}} \cdot \frac{\omega_{P3}}{\omega_{P2}} \cdot \frac{\omega_{Z1}}{\omega_{P1}} \tag{3.20}$$

Or its equivalent expression:

$$L_{I,DC} = \frac{1}{\sqrt{3}} \cdot \frac{C_L}{g_{mN}} \cdot \frac{1}{C_A R_A} \cdot \frac{\omega_{Z1}}{\omega_{P1}} \tag{3.21}$$

Several conclusions can be drawn:

1. The performance of the CA is dependent on both the DC loop gain and the unity gain frequency.
2. In order to increase the loop gain:
   - Sense resistor, R_A, can be increased, pulling pole P_3 closer to the unity gain frequency, decreasing stability.
   - Transistor M_2 can be made wider in order to increase g_{m2}. However, this choice has the effect that it will decrease stability $\implies$ capacitance C_A is dependent on the width of M_2:
   $$C_A = C_{sg2} \approx \frac{2}{3} W_2 L_2 C_{ox}[F] \tag{3.22}$$
   - Both methods successfully increase the DC loop gain of the CA at the expense of a lower overall bandwidth.
3. Generally, the DC loop gain of this implementation is large, but suffers from bandwidth limitation $\implies$ the non-dominant pole, P_3, is given by two fixed parameters, C_A and R_A.
4. Transistor M_2 must be designed such that it can sustain the load current without causing reliability issues (for example, self-heating), meaning that capacitance C_A will be relatively large.

The voltage loop has a direct effect on the current loop, as can be seen that pole P_1 and zero Z_1 are dependent on the voltage feedback gain and on the voltage gain of the g_m stage. A modified implementation is presented in the following section, aiming to solve the speed limitation of CA Type I.

3.4. Current Amplifier - Type II

A solution to CA Type I's bandwidth limitation is to utilize a simple current mirror, as depicted in Fig. 3.7.

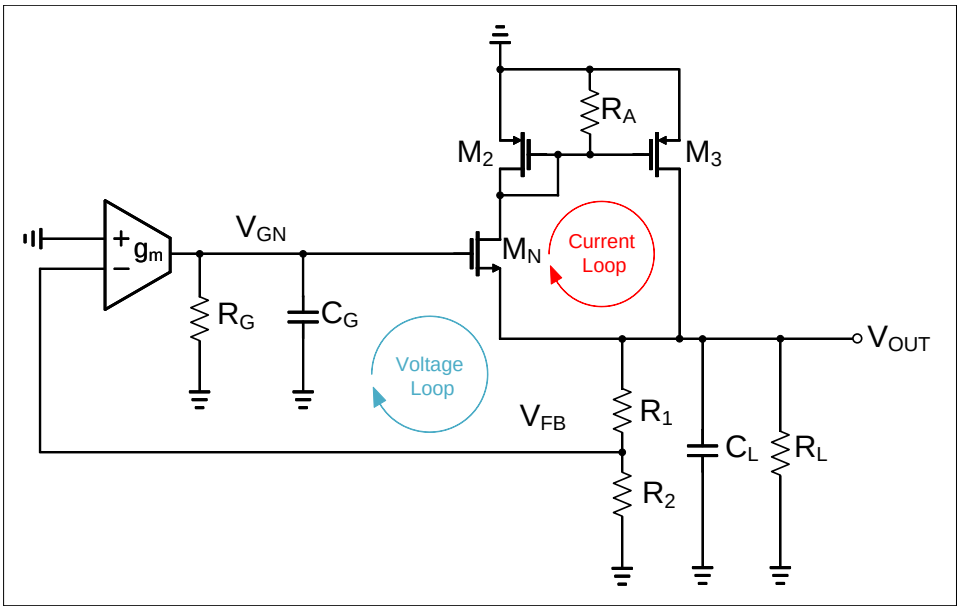

Figure 3.7: Current Amplifier-based LVR - Type II - Stability Analysis

3.4.1. Stability Analysis

The current loop gain (denoted as L_I) (detailed in Appendix B.5) is given by:

$$L_I(s) = \frac{\beta A_V g_{mN} R_{eq} + (1 + sC_G R_G) g_{mN} R_{eq}}{(1 + sC_G R_G)(1 + sC_L R_{eq} + g_{mN} R_{eq}) + \beta A_V g_{mN} R_{eq}} \cdot \frac{g_{m3} R_{A,tot}}{1 + s(C_A + g_{m3}) R_{A,tot}} \tag{3.23}$$

With:

$$L_{I,DC} \approx \frac{g_{m3}}{g_{m2}} \tag{3.24}$$

It can be observed that the first term of Eq. (3.23) is the same as the first term of Eq. (3.5) and is responsible for P_1, P_2 and Z_1. It describes the voltage loop influence on the current loop and will be, therefore, denoted by $H_I(s)$, for simplicity.

$$H_I(s) = \frac{\beta A_V g_{mN} R_{eq} + (1 + sC_G R_G) g_{mN} R_{eq}}{(1 + sC_G R_G)(1 + sC_L R_{eq} + g_{mN} R_{eq}) + \beta A_V g_{mN} R_{eq}} \tag{3.25}$$

Where:

- Capacitance C_A is now given by:

$$C_A = C_{sg2} + C_{sg3}[F] \tag{3.26}$$

- The total resistance between the source and gate of transistor M_3 is now given by:

$$R_{A,tot} = \frac{1}{g_{m2}} || r_{ds2} || R_A [\Omega] \tag{3.27}$$

- The third, non-dominant, pole is given by:

$$\omega_{P3} = -\frac{g_{m2}}{C_A}[rad/s] \tag{3.28}$$

A similar procedure as for the CA Type I, for a phase margin equal to 60° is done, leading to:

$$L_{I,DC} = \frac{1}{\sqrt{3}} \cdot \frac{\omega_{P3}}{\omega_{P2}} \cdot \frac{\omega_{Z1}}{\omega_{P1}} \tag{3.29}$$

Or its equivalent expression:

$$L_{I,DC} = \frac{1}{\sqrt{3}} \cdot \frac{C_L}{g_{mN}} \cdot \frac{g_{m2}}{C_A} \cdot \frac{\omega_{Z1}}{\omega_{P1}} \tag{3.30}$$

Several conclusions can be drawn:

1. The DC loop gain can now be approximated by the ratio of the transconductances of the current mirror formed by transistors M_2 and M_3.
2. The non-dominant pole is now a function of the load current, eliminating the bandwidth limitation caused by the fixed non-dominant pole for CA Type I.
3. Sense resistor, R_A, is necessary to be placed in order to limit the quiescent current of the current mirror transistors, M_2 and M_3.
4. The only method to increase the DC loop gain is to increase the $\frac{g_{m3}}{g_{m2}}$ ratio. However, capacitance C_A will be increased, via making transistor M_3 wider, marking the limitation of this CA Type II.
5. This implementation has a faster reaction time than CA Type I. However, the DC loop gain is limited by the total capacitance between the source and the gate of the current mirror, $C_A \propto W_2, W_3$.

The next section aims to introduce a configuration that overcomes the DC loop gain limitation.

3.5. Current Amplifier - Type III

A solution to CA Type II's DC loop gain limitation is to utilize another current mirror, as depicted in Fig. 3.8 [15].

3.5.1. Stability Analysis

The current loop gain (denoted as L_I) (detailed in Appendix B.6) is given by:

$$L_I(s) = H_I(s) \cdot \frac{g_{m3}R_{A,tot} \cdot \left[1 + (sC_B + g_{m4} + g_{m5})R_{B,tot}\right]}{\left[1 + s(C_A + g_{m3})R_{A,tot}\right] \cdot \left[1 + (sC_B + g_{m4})R_{B,tot}\right]} \tag{3.31}$$

With:

$$L_{I,DC} \approx \frac{g_{m3}}{g_{m2}} \cdot \left(1 + \frac{g_{m5}}{g_{m4}}\right) \approx \frac{g_{m3}}{g_{m2}} \cdot \frac{g_{m5}}{g_{m4}} \tag{3.32}$$

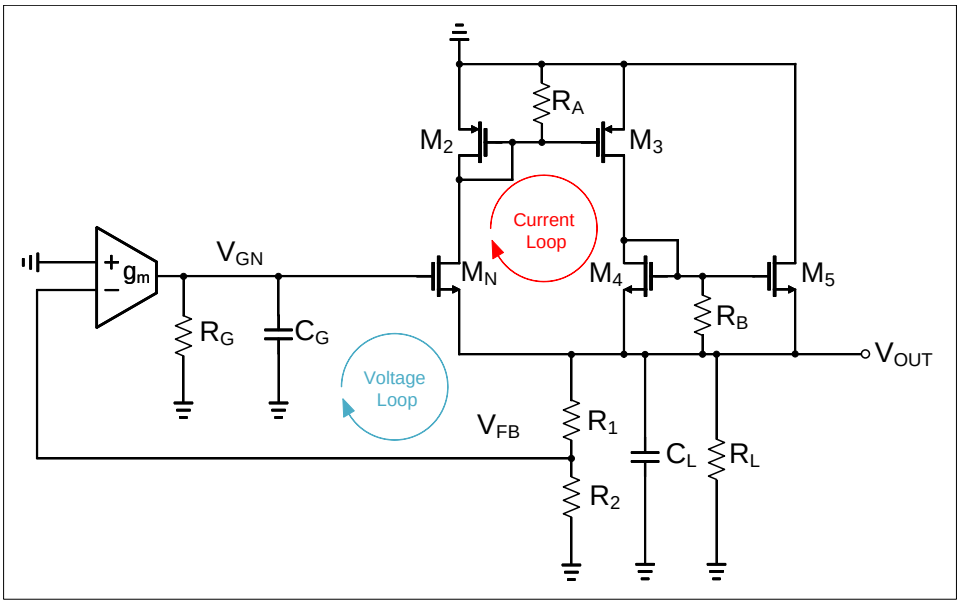

Figure 3.8: Current Amplifier-based LVR - Type III [15] - Stability Analysis

Where:

- Capacitance C_B is given by the total capacitance between the gate and source of transistor M_5:

$$C_B = C_{gs4} + C_{gs5}[F] \tag{3.33}$$

- The total resistance between the source and gate of transistor M_5 is given by:

$$R_{B,tot} = \frac{1}{g_{m4}} || r_{ds4} || R_B [\Omega] \tag{3.34}$$

- This configuration adds a fourth non-dominant pole, given by:

$$\omega_{P4} = -\frac{g_{m4}}{C_B}[rad/s] \tag{3.35}$$

- This configuration adds a non-dominant zero, located at:

$$\omega_{Z_2} = -\frac{(g_{m4} + g_{m5})R_{B,tot} + 1}{C_B R_{B,tot}} \approx -\frac{g_{m4} + g_{m5}}{C_B}[rad/s] \tag{3.36}$$

Based on the bode plot from Fig. 3.9, a phase margin design equation is deduced:

$$PM = 90° - tan^{-1}\left(\frac{\omega_u}{\omega_{P3}}\right) \cdot \frac{180°}{\pi} - tan^{-1}\left(\frac{\omega_u}{\omega_{P4}}\right) \cdot \frac{180°}{\pi} \tag{3.37}$$

For a phase margin of 60°:

$$L_{I,DC} = \frac{1}{\sqrt{3}} \cdot \frac{1}{\omega_{P2}} \cdot \frac{\omega_{P3}\omega_{P4}}{\omega_{P3} + \omega_{P4}} \cdot \frac{\omega_{Z1}}{\omega_{P1}} \tag{3.38}$$

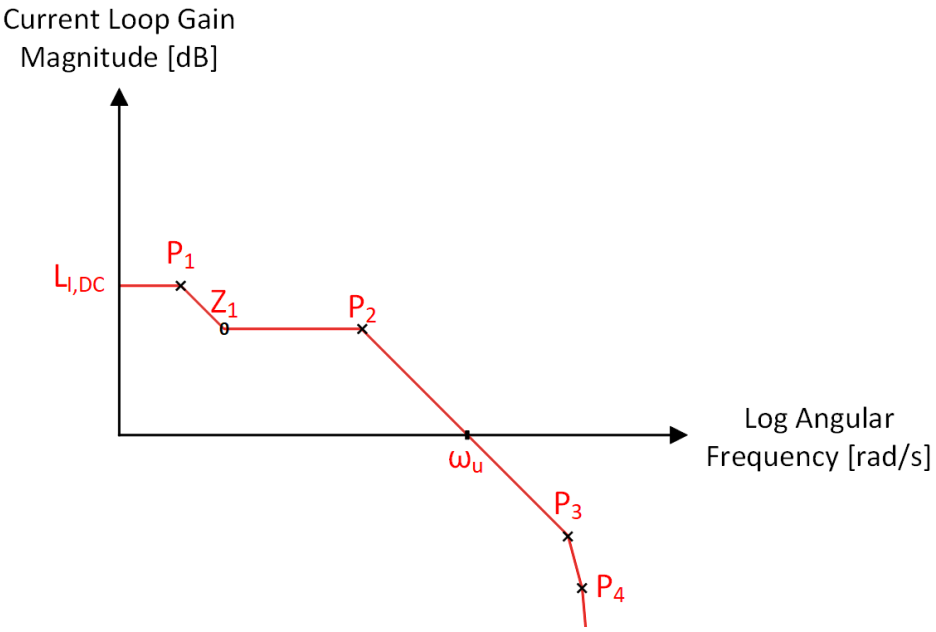

Figure 3.9: Current Amplifier-based LVR - Type III - Loop Gain Bode Plot

Or its equivalent expression:

$$L_{I,DC} = \frac{1}{\sqrt{3}} \cdot \frac{C_L}{g_{mN}} \cdot \frac{g_{m2}g_{m4}}{g_{m2}C_A + g_{m4}C_B} \cdot \frac{\omega_{Z1}}{\omega_{P1}} \tag{3.39}$$

Several conclusions can be drawn:

1. Placing another current mirror introduces an out of band zero, Z_2, and another non-dominant pole, P_4.
2. The DC loop gain can now be approximated by the ratio of the transconductances of the current mirror formed by transistors M_2, M_3 and M_4, M_5, respectively.
3. Sense resistor R_B is necessary to be placed in order to reduce the overshoot in V_{OUT} after a negative load current step.
4. Spreading the current gain among two current mirrors allows for smaller sizes for transistors M_2, M_3, M_4, M_5, meaning that the capacitances C_A and C_B are also much smaller implying an improved frequency and transient behavior.
5. This implementation offers a good compromise between current gain and bandwidth.

A brief mathematical description that explains the benefits of spreading the current gain across multiple current mirrors is given below:

- Suppose another current mirror is added, consisting of two PMOS transistors, M_6 and M_7.
- Each current mirror gain is denoted by F_1, F_2 and F_3.
- The new current mirror will add both a non-dominant zero and a non-dominant pole.

- Assume that the new current gain is designed to be the same as the old one:

$$F_{1,O} \cdot F_{2,O} = F_{1,N} \cdot F_{2,N} \cdot F_{3,N} \tag{3.40}$$

- Choose $F_{1,O}$ such that it is equal to $F_{1,N}$. This implies that:

$$F_{2,O} = F_{2,N} \cdot F_{3,N} \tag{3.41}$$

- Therefore, the new capacitance between the gate and source of the second current mirror is effectively decreased.

$$C_{A,O} = C_{A,N}[F] \tag{3.42}$$

$$C_{B,O} < C_{B,N}[F] \tag{3.43}$$

- More detailed:

$$C_{B,O} = (1 + F_{2,O}) \cdot C_{gs,unit}[F] \tag{3.44}$$

$$C_{B,N} = (1 + F_{2,N}) \cdot C_{gs,unit}[F] \tag{3.45}$$

- Furthermore, an analysis of the non-approximated DC loop gains of a CA with two current mirrors (denoted $L_{I,O,DC}$) with a CA with three current mirrors (denoted $L_{I,N,DC}$) yields the following:

$$L_{I,O,DC} = \frac{g_{m3}}{g_{m2}} \cdot \left(1 + \frac{g_{m5}}{g_{m4}}\right) \tag{3.46}$$

$$L_{I,N,DC} = \frac{g_{m3}}{g_{m2}} \cdot \left[1 + \frac{g_{m5}}{g_{m4}} \cdot \left(1 + \frac{g_{m7}}{g_{m6}}\right)\right] \tag{3.47}$$

  - Unless the ratios are not greater than 10, the + 1 terms are not negligible.
  - Therefore, $L_{I,N,DC} > L_{I,O,DC}$ with current mirror ratios that respect the following equation:

$$F_{1,O} \cdot F_{2,O} = F_{1,N} \cdot F_{2,N} \cdot F_{3,N} \tag{3.48}$$

- The same current gain but with improved stability, or, a higher current gain for the same stability can be achieved.

3.6. Current Amplifier - Type IV

An extension to CA Type III that aims to improve both gain and bandwidth of the current loop is presented in this section and is illustrated in Fig.3.10.

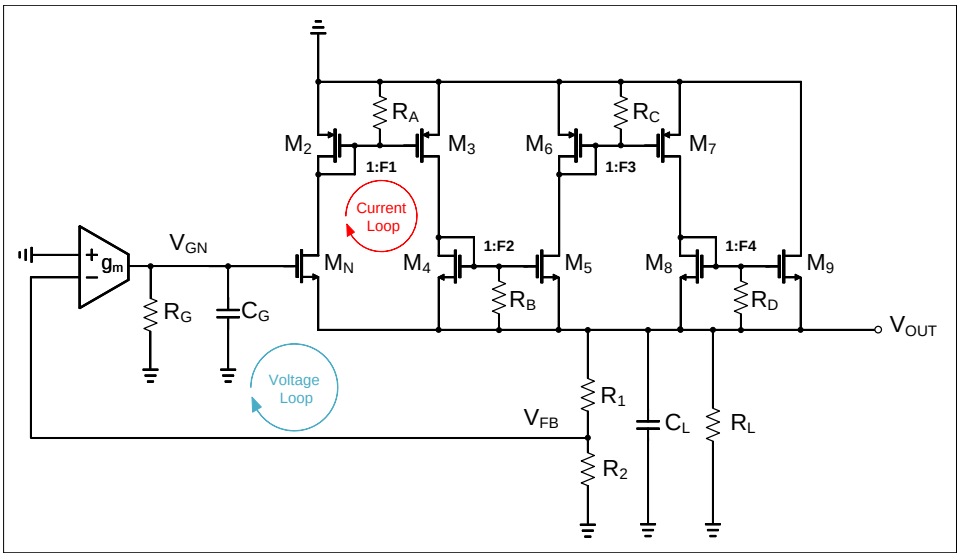

Figure 3.10: Current Amplifier-based LVR - Type IV - Stability Analysis

3.6.1. Stability Analysis

The current loop gain (denoted as L_I) (detailed in Appendix B.7) is given by:

$$L_I(s) = H_I(s) \cdot g_{m3} R_{A,tot} \cdot \frac{T_1(s) + T_2(s)}{T_3(s)} \tag{3.49}$$

With:

$$T_1(s) = \left[(g_{m4} + g_{m5} + sC_B)R_{B,tot} + 1\right]\left[(g_{m6} + sC_C)R_{C,tot} + 1\right]\left[(g_{m8} + sC_D)R_{D,tot} + 1\right] \tag{3.50}$$

$$T_2(s) = g_{m3} R_{A,tot} g_{m5} R_{B,tot} g_{m7} R_{C,tot} \cdot \left[(g_{m8} + g_{m9} + sC_D)R_{D,tot} + 1\right] \tag{3.51}$$

$$T_3(s) = \left[(g_{m2} + sC_A)R_{A,tot} + 1\right]\left[(g_{m4} + sC_B)R_{B,tot} + 1\right]\left[(g_{m6} + sC_C)R_{C,tot} + 1\right]\left[(g_{m8} + sC_D)R_{D,tot} + 1\right] \tag{3.52}$$

$$L_{I,DC} \approx \frac{g_{m3}}{g_{m2}} \cdot \left\{1 + \frac{g_{m5}}{g_{m4}} \cdot \left[1 + \frac{g_{m7}}{g_{m6}} \cdot \left(1 + \frac{g_{m9}}{g_{m8}}\right)\right]\right\} \tag{3.53}$$

Where:

- Capacitance C_C is given by the total capacitance between the gate and source of transistor M_7:

$$C_C = C_{gs6} + C_{gs7}[F] \tag{3.54}$$

- Capacitance C_D is given by the total capacitance between the gate and source of transistor M_9:

$$C_D = C_{gs8} + C_{gs9}[F] \tag{3.55}$$

- The total resistance between the source and gate of transistor M_7 is given by:

$$R_{C,tot} = \frac{1}{g_{m6}} || r_{ds6} || R_C [\Omega] \tag{3.56}$$

- The total resistance between the source and gate of transistor M_9 is given by:

$$R_{D,tot} = \frac{1}{g_{m8}} || r_{ds8} || R_D [\Omega] \tag{3.57}$$

- Two poles are added:

$$\omega_{P5} = -\frac{g_{m6}}{C_C} [rad/s] \tag{3.58}$$

$$\omega_{P6} = -\frac{g_{m8}}{C_D} [rad/s] \tag{3.59}$$

- The zeros that are introduced are out of band.

As described in the previous subsection, multiple current mirrors allow for smaller gate-source capacitances, increasing the bandwidth of the CA. The limitation on the number of current mirrors used is given by the voltage headroom of the structure.

3.6.2. Voltage Headroom

Voltage headroom issues are most likely to occur in the branch that contains the PMOST diode that conducts the most current (compared to the other PMOST diodes) because of the lower mobility of holes. An example is the branch containing transistors M_6 and M_7 in Fig. 3.10.

$$V_{IN,min} - V_{OUT} = V_{SG6} + V_{OV5} \implies V_{IN,min} - V_{OUT} = V_{TH6} + V_{OV6} + V_{OV5} \tag{3.60}$$

$$V_{IN,min} - V_{OUT} - V_{TH6} = V_{OV5} + V_{OV6} = \sqrt{\frac{2\frac{I_L}{F_3F_4}}{\mu_N C_{OX}\left(\frac{W}{L}\right)_5}} + \sqrt{\frac{2\frac{I_L}{F_3F_4}}{\mu_P C_{OX}\left(\frac{W}{L}\right)_6}} \tag{3.61}$$

For simplicity, consider that every transistor in the CA has an unit size $\left(\frac{W}{L}\right)_u$. Then the following relation holds:

$$\left(\frac{W}{L}\right)_5 = F_2 \cdot \left(\frac{W}{L}\right)_6 = F_2 \cdot \left(\frac{W}{L}\right)_u \tag{3.62}$$

$$V_{IN,min} - V_{OUT} - V_{TH6} = \sqrt{\frac{2I_L}{F_2F_3F_4\mu_N C_{OX}\left(\frac{W}{L}\right)_u}} + \sqrt{\frac{2I_L}{F_3F_4\mu_P C_{OX}\left(\frac{W}{L}\right)_u}} \tag{3.63}$$

Further calculations yield:

$$\left(\frac{W}{L}\right)_u = \frac{2I_L}{F_3F_4C_{OX}} \cdot \left(\frac{1}{\sqrt{\mu_P}} + \frac{1}{\sqrt{F_2\mu_N}}\right)^2 \cdot \frac{1}{(V_{IN,min} - V_{OUT} - V_{TH,P})^2} \tag{3.64}$$

The headroom voltage issue can be overcome by either increasing the current mirror gains, F_3 and F_4 or by increasing the unit size width of the transistors.

In the following subsection, an effect of improper values for the sense resistors will be discussed.

3.6.3. Sense Resistors Discussion

The sense resistors are essential, as they set current thresholds for each current mirror:

$$I_{TH} = \frac{V_{TH}}{R}[A] \tag{3.65}$$

However, large resistor values can bias the current mirrors at low load currents implying that the non-dominant poles will be found below or near the unity gain frequency of the loop, risking instability. Smaller resistor values should be chosen in order to mitigate this effect, as shown in Fig. 3.11.

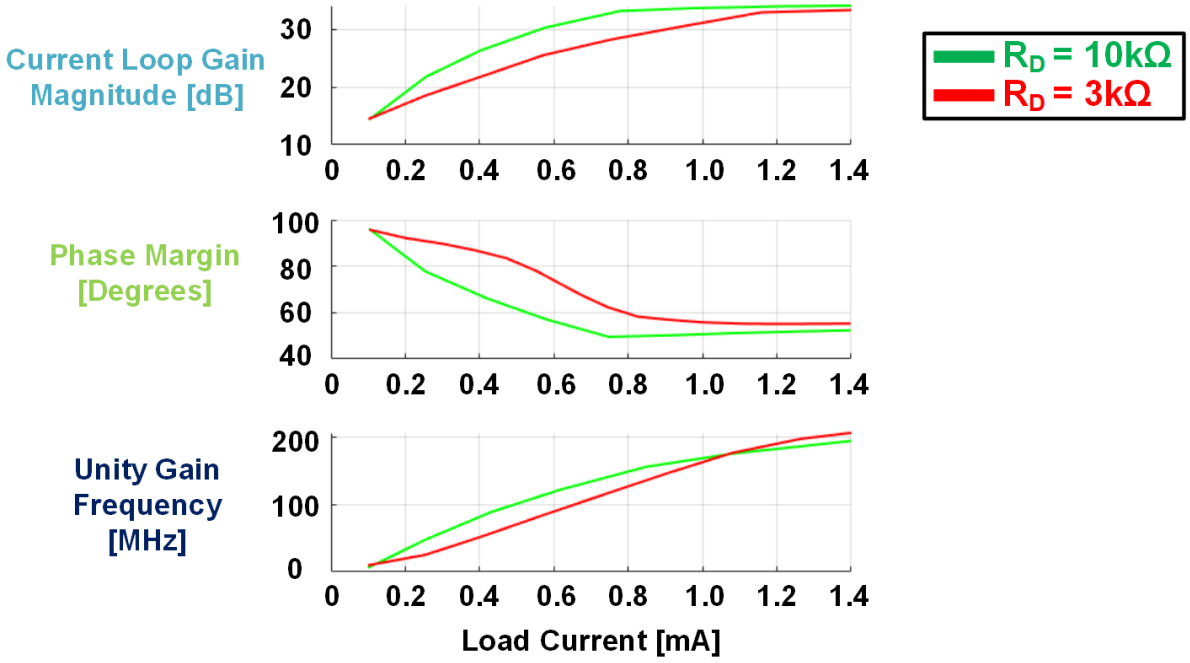

Figure 3.11: CA LVR - Type IV - Sense Resistors Stability Effects - Simulation Results

3.7. Improvements

3.7.1. Bandwidth Enhanced Current Mirror [17]

A well known technique to enhance the bandwidth of current mirrors is via a resistor placed between the gate and drain of the diode connected transistor [17], as depicted in Fig. 3.12, for a simple NMOST current mirror.

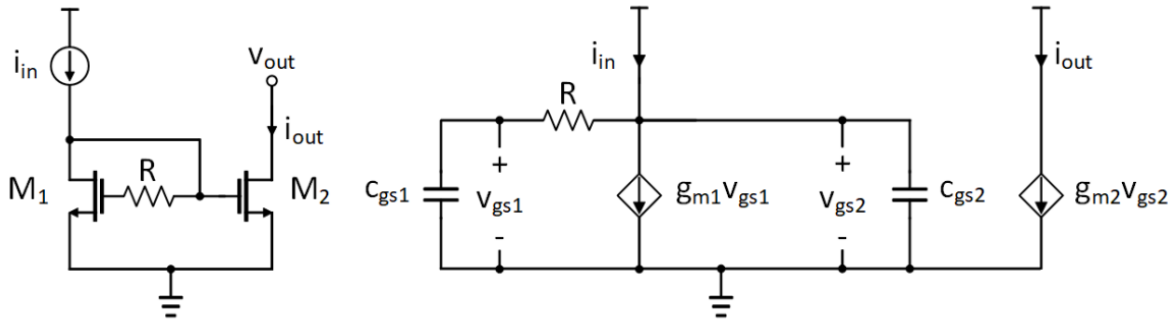

Figure 3.12: Current Mirror Compensation [17]

The resistor adds a zero, Z_1, at:

$$\omega_{Z1} = -\frac{1}{RC_{gs1}}[rad/s] \tag{3.66}$$

The resistor also generates a complex pair of poles, $P_{1,2}$, at:

$$\omega_{P1,2} = \frac{C_{gs1}+C_{gs2}}{2RC_{gs1}C_{gs2}} \cdot \left[-1 \pm \sqrt{1-\frac{4g_{m1}RC_{gs1}C_{gs2}}{(C_{gs1}+C_{gs2})^2}}\right][rad/s] \tag{3.67}$$

The compensated current mirror current gain transfer function can be described by a general second-order system transfer function [17]:

$$H(s) = \frac{\omega_0^2}{Z} \cdot \frac{s+Z}{s^2+2\zeta\omega_0 s+\omega_0^2} \tag{3.68}$$

With:

$$\omega_0 = \frac{g_{m1}}{RC_{gs1}C_{gs2}}[rad/s] \tag{3.69}$$

$$\zeta = \frac{C_{gs1}+C_{gs2}}{2\sqrt{g_{m1}RC_{gs1}C_{gs2}}} \tag{3.70}$$

Where:

- ω_0 represents the resonant (or natural) frequency,
- ζ represents the damping factor.

It can be seen from Eq. (3.70) that increasing the resistor's value, the system becomes underdamped ($0 < \zeta < 1$) and thus it becomes faster. The compensation resistors can be used in the CA LVR current mirrors, enhancing the CA transient response. This technique can also be used to stabilize the system via the zero that it adds.

3.7.2. Adaptive Biasing

Adaptive biasing aims to increase the voltage loop bandwidth (by increasing the transconductance of the error amplifier), increase the slew rate at the gate of the pass transistor (by increasing the bias current of the error amplifier) without affecting the no-load condition quiescent current, but at the expense of decreasing the voltage loop DC gain. The discussion below is based on a NMOST LVR.

A conceptual voltage loop bode plot is illustrated in Fig. 3.13.

- The voltage loop DC gain for a NMOST LVR is equal to:

$$L_{V,DC} = \beta A_V = \frac{R_2}{R_1 + R_2} \cdot g_m R_G \tag{3.71}$$

- g_m represents the transconductance of the OTA and is proportional to $\sqrt{I_{DS}}$.
- Resistor R_G represents the output impedance of the OTA and is proportional to $\frac{1}{I_{DS}}$.
- Where I_{DS} is the bias current of the OTA.
- Therefore, the voltage gain, $A_V = g_m R_G \propto \frac{\sqrt{I_{DS}}}{I_{DS}}$, will decrease with an increase in I_{DS}.

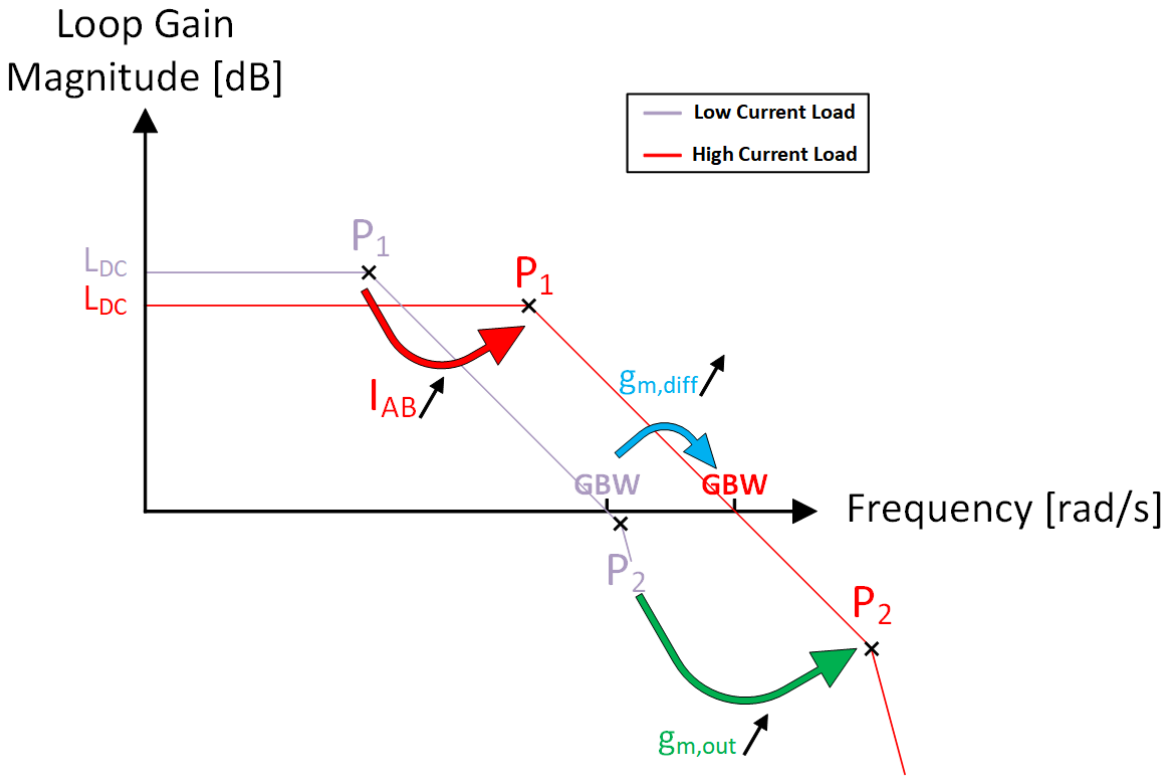

Figure 3.13: Adaptive Biasing - Conceptual Voltage Loop Bode Plot

Principle of operation:

1. For low load currents, adaptive biasing is not active and the system is compensated by a large capacitor, C_G (that also reduces the capacitive coupling effect).

2. For high load currents, adaptive biasing is active and an additional bias current (I_{AB}) is supplied to the OTA (denoted by $g_{m,diff}$).

   (a) Pole P_1, given by $1/R_G C_G$ [rad/s], is pushed to higher frequencies due to the decrease of the output impedance of the $g_{m,diff}$ stage, R_G, because of the increase in the bias current.

   (b) The unity gain frequency, denoted as GBW (gain bandwidth product) in Fig. 3.13, given by $g_{m,diff}/C_G$ [rad/s], is also pushed to higher frequencies, because of the increase of $g_{m,diff} \propto \sqrt{I_{AB}}$.

   (c) Non-dominant output pole, P_2, approximated by $g_{m,out}/C_L$ [rad/s] is inherently pushed to higher frequencies because of the increase of I_L, $g_{m,out} \propto \sqrt{I_L}$.

Adaptive biasing can be implemented in the CA using any PMOST current mirror, as depicted in Fig. 3.14, for CA Type II.

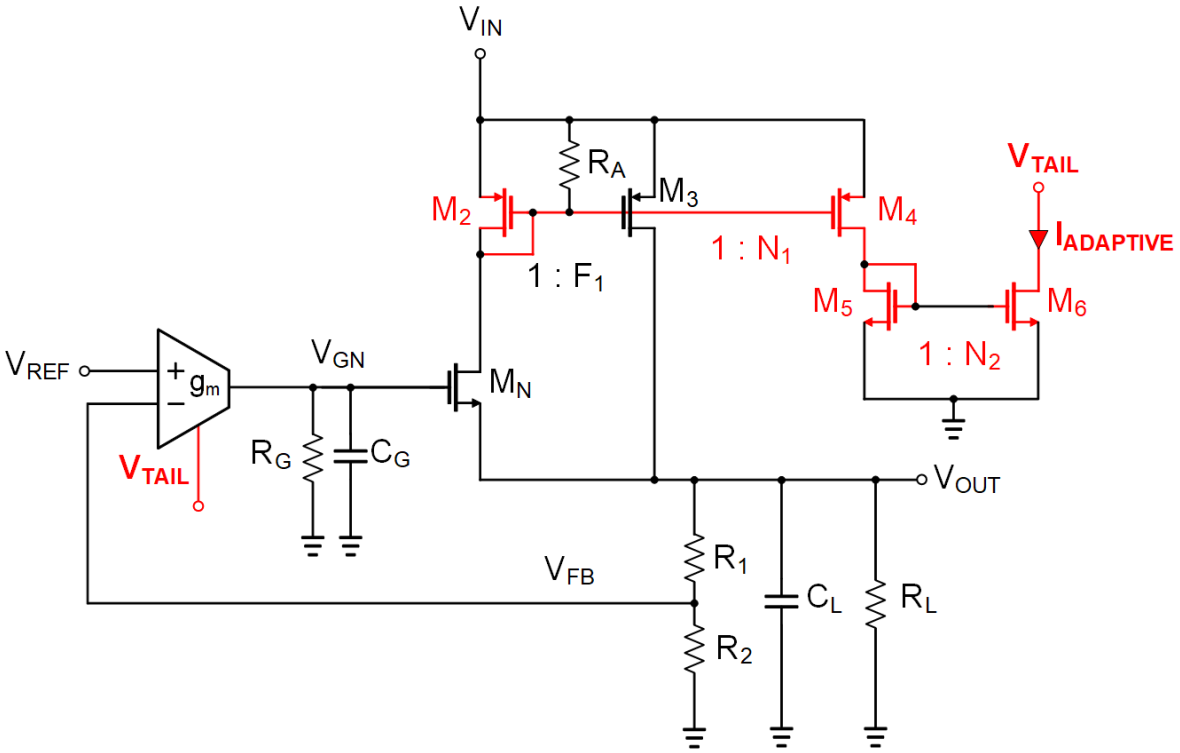

Figure 3.14: Current Amplifier-based LVR - Type II - Adaptive Biasing

The amount of extra bias current supplied to the g_m stage can be fixed by ratios N_1 and N_2:

- The current in transistor M_2 is $I_{M2} = I_L/L_{I,DC} = I_L/(g_{m3}/g_{m2})$.
- The current in transistor M_6 can then be written as:

$$I_{M6} = I_{M2} \cdot N_1 \cdot N_2 [A] \tag{3.72}$$

Several conclusions can be drawn:

1. The widths of transistors M_2 and M_4 should be chosen small, $W_4 < W_2 \implies I_{M4} < I_{M2}$, in order to maintain a high current efficiency at a non-zero load condition:

$$\eta_I = \frac{I_L}{I_L + I_Q} \tag{3.73}$$

   Where I_Q represents the sum of the bias current of the g_m stage and the bias current of M_N.

2. The adaptive biasing loop does not require frequency compensation because of the small sizes of the additional transistors: M_4, M_5 and M_6.

3. Adaptive biasing increases the slew rate at node V_{GN} and enhances the bandwidth of the voltage loop, overcoming the limitations initally caused by capacitor C_G.

3.8. Conclusions

Four types of current amplifier-based LVRs have been introduced, analyzed and discussed. CA Type I provides a large amount of current gain at the expense of slow reaction to load current steps. The subsequent implementation, CA Type II, proposes a solution to enhance the reaction time of the CA, however, at the expense of small DC loop gain, limited by stability. A good compromise between current gain and bandwidth was presented as CA Type III, and based on the same principle applied to extend CA Type II to CA Type III, CA Type IV was introduced. Limitations that occur in each CA have been discussed.

Techniques to improve the transient behavior have been proposed. Current mirror compensation decreases the reaction time of the CA. Adaptive biasing provides a solution to overcome the voltage loop bandwidth reduction due to the necessity of C_G. CA Type IV benefits from enhanced bandwidth for similar (or larger) current gain as CA Type III.

4

1.8V NMOST Current Amplifier-based Linear Voltage Regulator

4.1. Final Schematic

The final schematic is shown in Fig. 4.1.

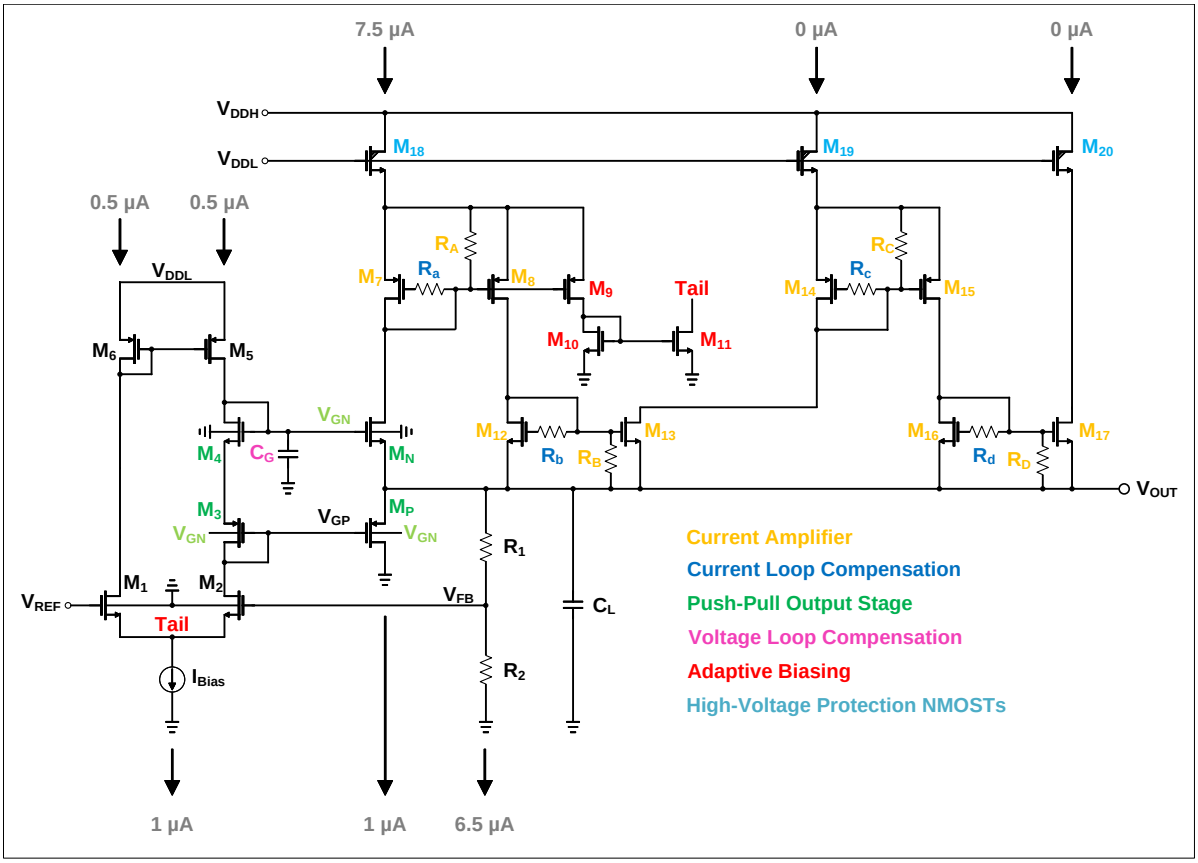

Figure 4.1: Current Amplifier-based LVR - Architecture

The operational amplifier formed by the OTA and the common-drain push-pull stage operates at a low voltage supply. The power transistors, M_{18}, M_{19} and M_{20} enable the circuit

to operate at a high-voltage supply. Apart from high-voltage operation, the power transistors also increase the power supply rejection of the LVR.

The body connections of transistors M_1 and M_2 are tied to ground in order to increase the unity gain bandwidth of the voltage loop (proven in Appendix B.2.1). The body of transistor M_N is connected to ground in order to push the bandwidth of the current loop to higher frequencies (proven in Appendix B.4.2) and also pushing the non-dominant pole of the voltage loop to higher frequencies. The body of transistor M_P is connected to node V_{GN} in order to increase the threshold voltage, limiting its quiescent current.

4.2. Compactness

Due to the low current variation through the output NMOS transistor, M_N, its size can be very small. This in turn has the immediate effect of requiring only a small 3pF gate capacitance to mitigate the capacitive coupling effect and to compensate the voltage loop. The transistors that form the current amplifier are also designed with small unit sizes in order to minimize the gate-source capacitances of the current mirror.

4.3. Scalability

4.3.1. Load Capacitance Scalability

A method to scale the design is to scale the current amplifier according to the load capacitance. A larger load capacitance will allow for a larger loop gain without sacrificing stability. This, in turn, increases the current capability of the current amplifier:

- Increase the load capacitance to shift the second dominant pole to lower frequencies.
- Increase the current mirror gain, F_4, of the current mirror formed by transistors M_{16} - M_{17}, to shift the non-dominant pole to lower frequencies.
- Therefore, the loop gain can be increased without stability issues and also relieves the voltage headroom of the CA as most of the load current will be conducted by transistor M_{17}.
- For simplicity, consider the loop gain bode plot of CA Type III, as illustrated in Fig. 4.2.
  - The relation between the load capacitance and the loop gain, for a phase margin equal to 60°, can be described as:

$$L_{I,DC} = \frac{1}{\sqrt{3}} \cdot \frac{1}{\omega_{P2}} \cdot \frac{\omega_{P3}\omega_{P4}}{\omega_{P3}+\omega_{P4}} \cdot \frac{\omega_{Z1}}{\omega_{P1}} = \frac{1}{\sqrt{3}} \cdot \frac{C_L}{g_{mN}} \cdot \frac{g_{m2}g_{m4}}{g_{m2}C_A + g_{m4}C_B} \cdot \frac{\omega_{Z1}}{\omega_{P1}} \quad (4.1)$$

- It can be observed that as C_L is increased, a higher loop gain can be achieved for the same phase margin of 60°.

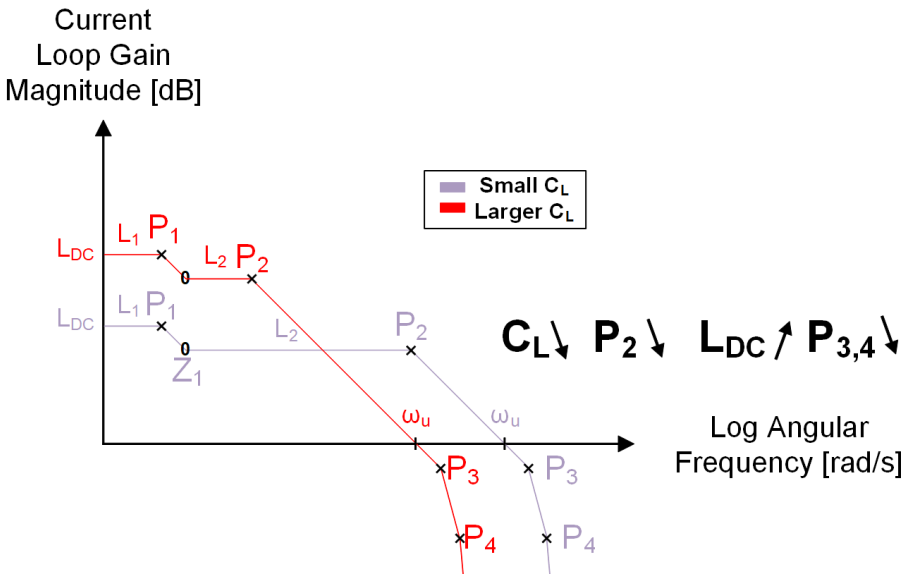

Figure 4.2: Load Capacitance Scalability - Bode Plot

4.3.2. Load Current Scalability

It is possible to scale the design up to effectively double the current (or any number of times) at the expense of extra area and stability degradation. To avoid headroom problems, the transistors that constitute the current amplifier (and the high-voltage NMOS transistors) should be designed twice as large $\left(V_{GS} \propto \sqrt{\frac{I_{DS}}{W}}\right)$, however, stability will be affected. To better illustrate the effect of scaling, consider the schematic illustrated in Fig. 4.1. The pole of the current mirror constituted by tranistors M_7 and M_8 is located at:

$$\omega = -\frac{g_{m7}}{C_{sg7} + C_{sg8}} = -\frac{g_{m7}}{C_{sg7} + F_1 C_{sg7}} [rad/s] \tag{4.2}$$

In Eq. (4.2), F_1 represents the current mirror gain. The gate-source capacitance can be approximated by:

$$C_{sg} \approx \frac{2}{3} W L C_{OX} [F] \tag{4.3}$$

Where:

- C_{OX} represents the gate oxide capacitance.

$$C_{OX} = \frac{\epsilon_0 \epsilon_r}{t_{ox}} [F/m^2] \tag{4.4}$$

- ϵ_0 represents the electric permittivity in free space and is approximately equal to 8.85 $\cdot 10^{-12}$ [F/m]
- ϵ_r represents the relative permittivity of silicon dioxide and is equal to 3.9
- t_{ox} represents the gate oxide thickness

The transconductance can be approximated as:

$$g_{m7} = \sqrt{2\mu_{e^+} C_{OX} \left(\frac{W}{L}\right)_7 \frac{I_L}{L_{I,DC}}} [S] \tag{4.5}$$

Therefore, a LVR that operates at twice the load current and with CA transistors sized twice as large would theoretically result in unchanged pole positions for the system.

However, the stability of the loop will be affected at smaller load currents. Even though the transconductances of the transistors will increase with $\sqrt{W}$, the capacitance remains fixed and proportional to 2W, meaning that the poles position are degraded (shifted to lower frequencies) by a factor equal to $\frac{\sqrt{W}}{2W} = \frac{1}{2\sqrt{W}}$, highlighting the necessity of increasing the load capacitance in order to maintain stability.

4.4. Performance Evaluation

Performance of the proposed design is evaluated and the results are reported in this section under the following simulation conditions:

- Load Capacitance = 50pF
- Temperature = 27°C
- Typical Corner

4.4.1. Line Regulation

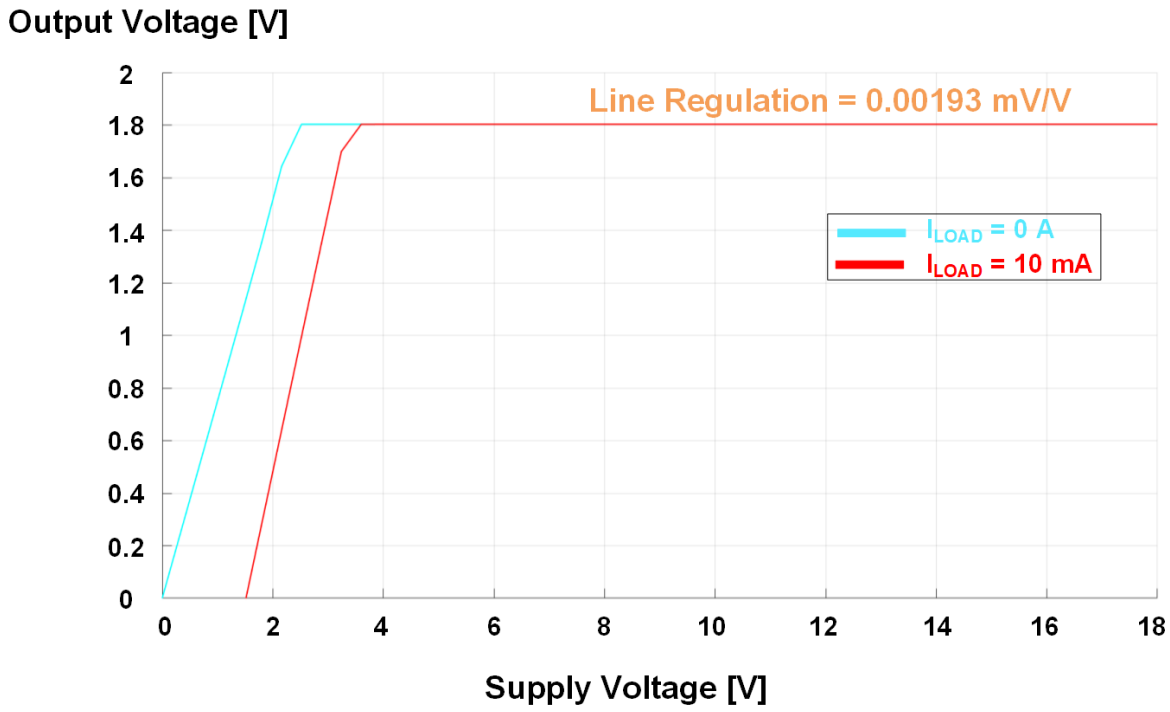

Figure 4.3: NMOST CA LVR - DC Line Regulation

As can be seen in Fig. 4.3, the LVR is able to operate at a minimum supply of 4V while providing a current of 10mA to the load.

4.4.2. Load Regulation

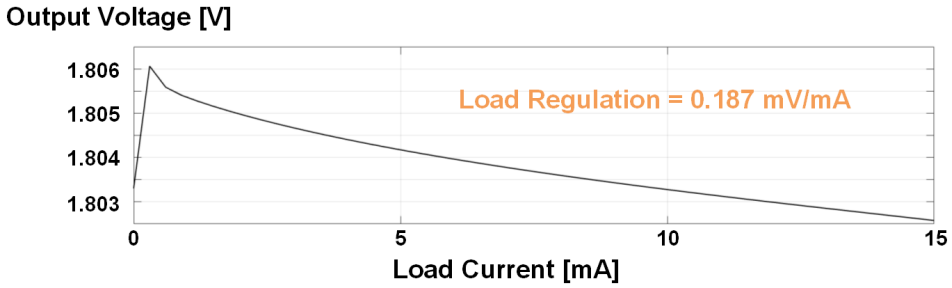

Figure 4.4: NMOST CA LVR - DC Load Regulation

As can be seen in Fig. 4.4, the LVR is able to provide load currents up to at least 15mA, providing a good margin that covers corner variations and temperature variations.

4.4.3. Voltage Loop Stability

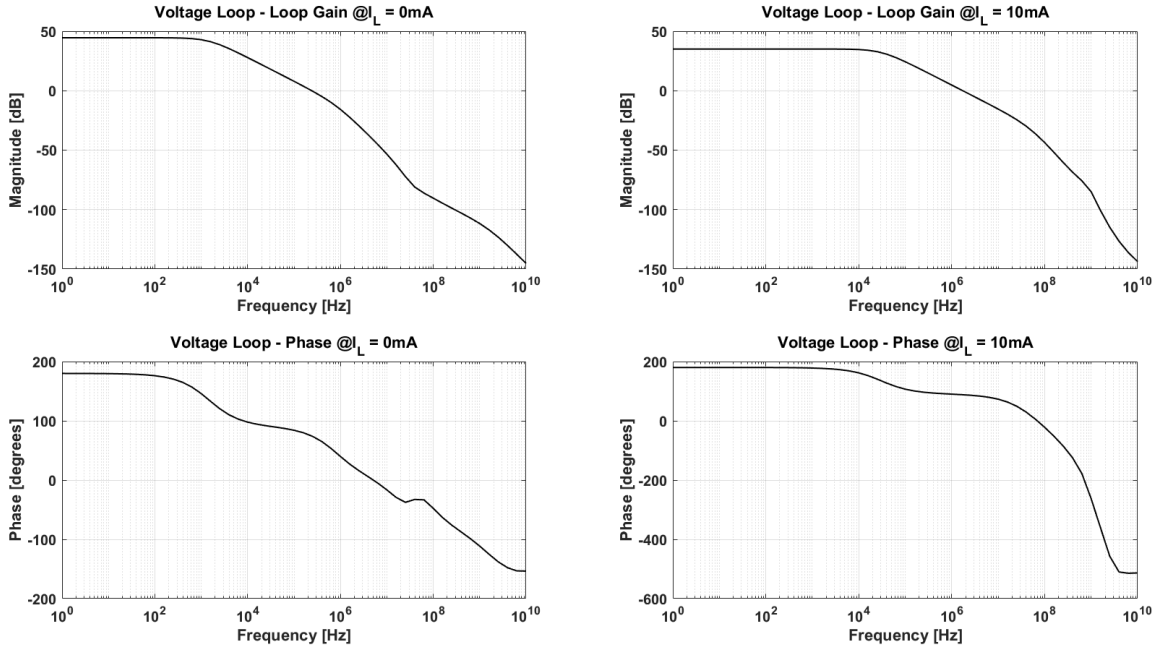

Figure 4.5: NMOST CA LVR - Voltage Loop Stability

The voltage loop bode plots for loop gain and phase, at no load condition, are depicted in the first column of Fig. 4.5. The DC loop gain is around 44 dB, the unity gain frequency is around 250kHz with a phase margin of above 60°.

The voltage loop bode plots for loop gain and phase, at maximum load condition, are depicted in the second column of Fig. 4.5. Because of adaptive biasing, the DC loop gain drops from 44 dB to around 35 dB, the new unity gain frequency is 1.6MHz, with a phase margin of above 85°.

4.4.4. Current Loop Stability

Fig. 4.6 presents the current loop bode plots for loop gain magnitude and phase. At a maximum load current of 10mA, the current loop has a current gain of 34 dB, achieving a unity gain frequency of 539MHz, with a phase margin of 54°.

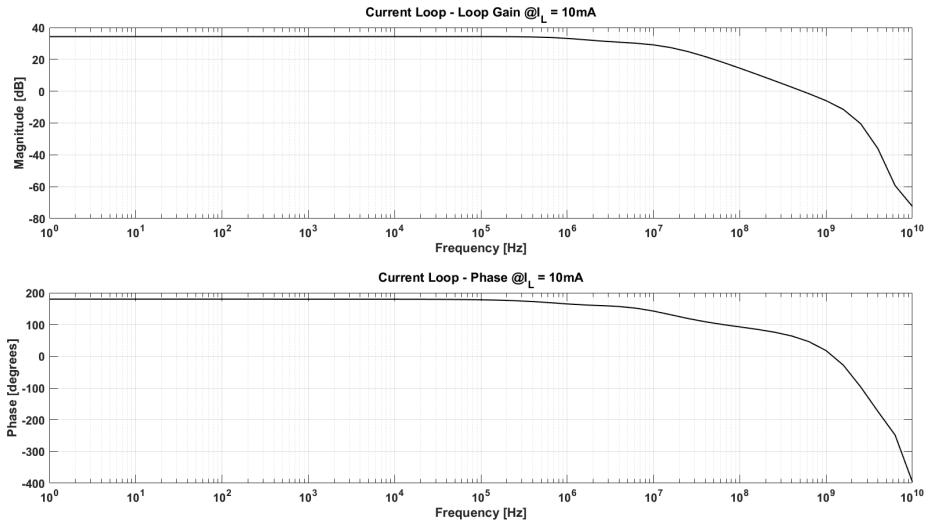

Figure 4.6: NMOST CA LVR - Current Loop Stability

Fig. 4.7 summarizes the current loop performance over the load current range. A minimum phase margin of 49.587° is reached at I_L = 1.074mA. The phase margin at I_L = 10mA is 54.3°.

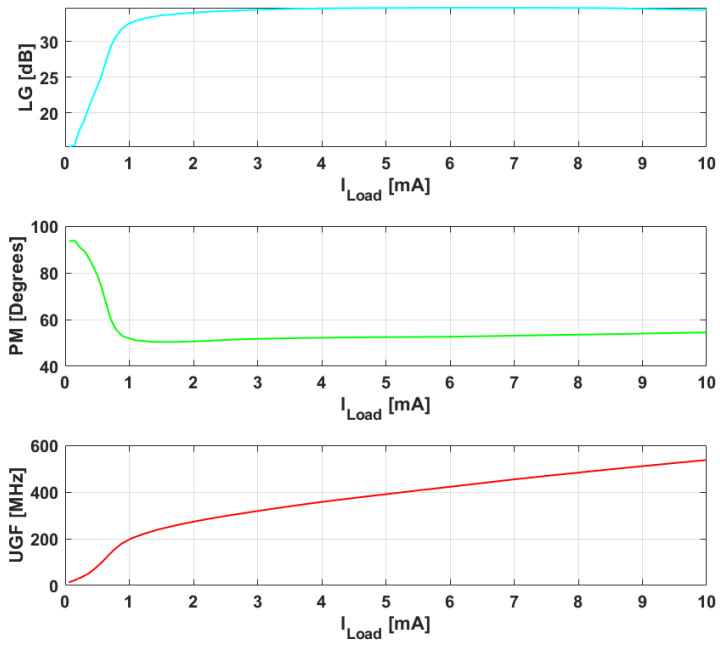

Figure 4.7: NMOST CA LVR - Current Loop - Performance

4.4.5. Load Current Step

In order to verify the LVR's performance during load current step transients:

- 10ns, 0A → 10mA and 10mA → 0A current pulses are applied in the top plot of Fig.4.6.
  - For a load current step of 0-10mA with rise time of 10ns, the LVR suffers from an undershoot of 143mV. The recovery time is approximately 1.4μs.
  - For a load current step of 10mA-0 with fall time of 10ns, the LVR suffers from an overshoot of 117mV. The recovery time is approximately 1.7μs.

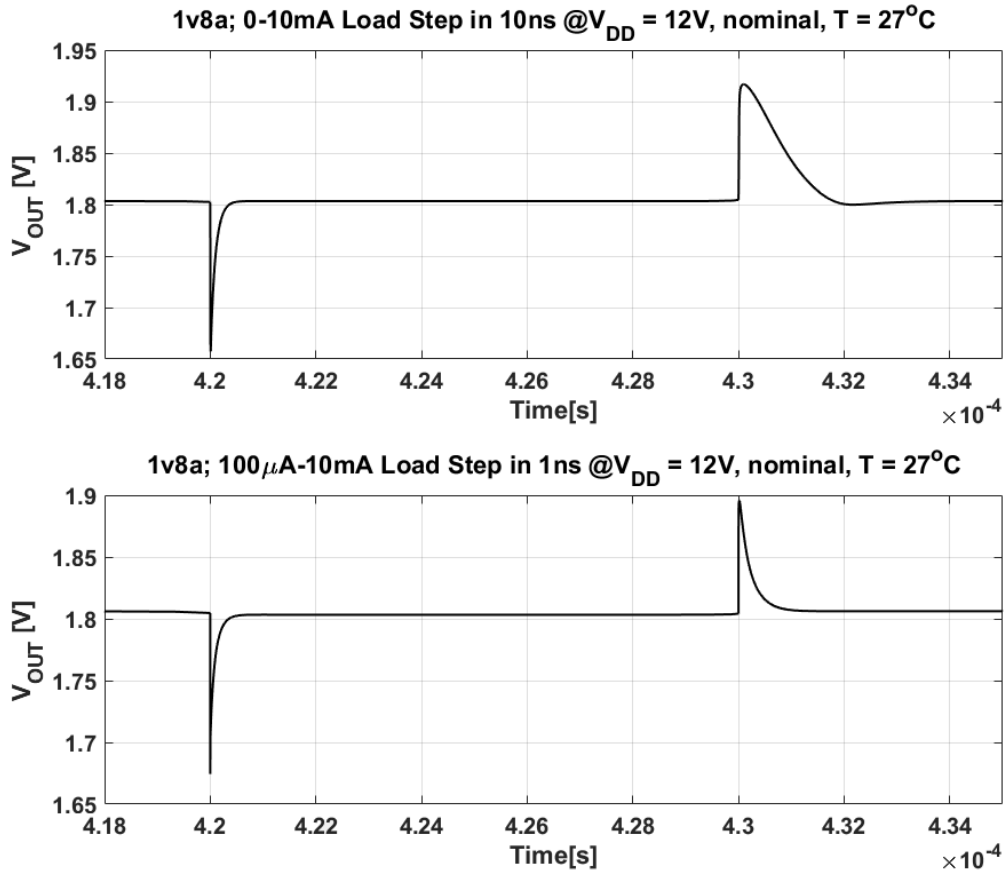

Figure 4.8: NMOST CA LVR - Load Current Step Transient

- 1ns, 100μA → 10mA and 10mA → 100μA current pulses are applied in the bottom plot of Fig. 4.6.
  - For a load current step of 100μA-10mA with rise time of 1ns, the LVR suffers from an undershoot of 122mV. The recovery time is approximately 600ns.
  - For a load current step of 10mA-100μA with fall time of 1ns, the LVR suffers from an overshoot of 96mV. The recovery time is approximately 900ns.

4.4.6. Supply Voltage Transient

In order to verify the power supply rejection of the LVR, a 100mV amplitude, 10MHz square wave signal has been superimposed on a supply voltage of 12V. The results are shown in Fig. 4.9.

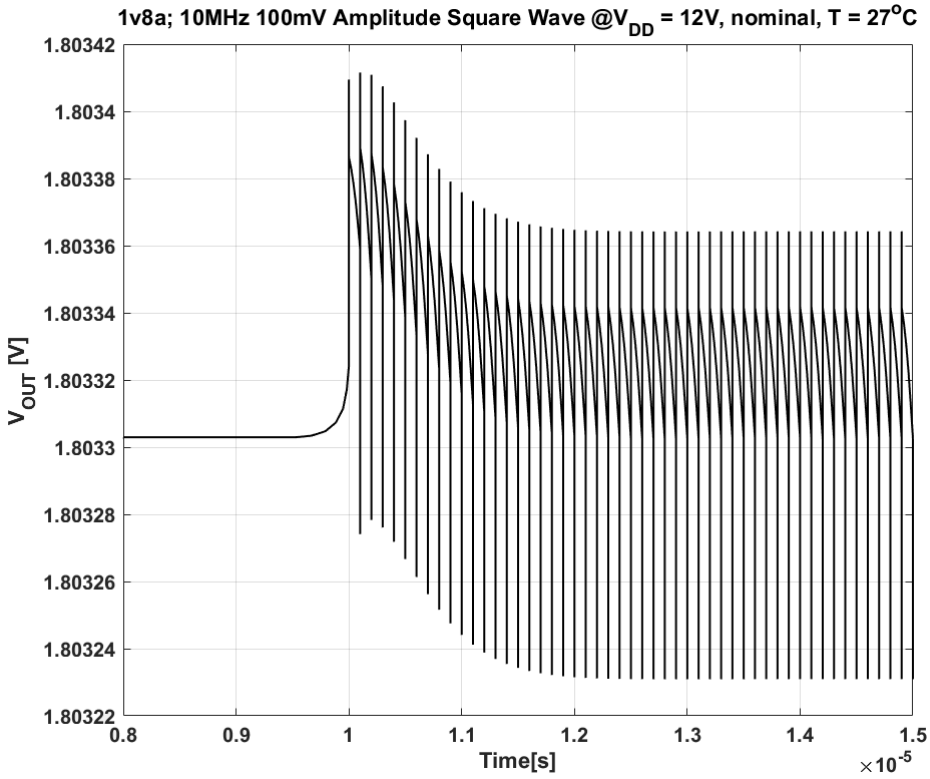

Figure 4.9: NMOST CA LVR - 100mV Amplitude 10 MHz Square Wave at V_{DD} = 12V

4.5. Performance Summary

Table 4.1: Overall Performance Summary of NMOST Current Amplifier-based Linear Voltage Regulator

Symbol	Parameter	Min	Typ.	Max	Unit
V_{IN}	Regulator Input Voltage	7.0	–	18	V
V_{OUT}	Output Voltage	1.65	1.8	1.95	V
ΔV_{OUT}	Dynamic Load Regulation	-8.33	–	8.33	%
I_Q	Quiescent Current (I_L = 0, w/o band-gap)	–	8.5μ	–	A
I_L	Load Current	0	–	10m	A
Area	–	–	0.0078	–	mm^2
C_L	Load Capacitance	–	50	–	pF

The regulator is fully scalable and can be accommodated for any combination of load capacitance and load current, according to the scalability features explained previously.

Due to the mathematical analysis, the limitation of the CA has been understood and the design has been optimized by proper sizing of the transistors, allowing for an obtained estimated area of ≈ four times smaller than the specification.

4.5.1. Comparison with State-of-the-Art

Table 4.2: Comparison with State-of-the-Art

Parameter	**This Work**	[18]	[19]	[20]	[21]	[22]	[23]
Technology [nm]	**140**	130	350	65	65	65	65
Chip Area [mm^2]	**0.0078**	0.008	0.077	0.01	0.017	0.0105	0.02^{est}
Quiescent Current I_Q [μA]	**8.5 - 39**	112	66	50-190	0.9	14	27-82
Max Output Current $I_{L,max}$ [mA]	**10**	25	100	50	100	100	20
Min Output Current $I_{L,min}$ [μA]	**0**	120	10 (for PM > 30°)	100 (for PM> 37°)	0	0	5
On-chip Cap [pF]	**3**	0.73	14	0.4	4.5	6	16.75
Load Capacitance C_L [pF]	**50**	0-25	0-100	0-2000	0-100 (PM drops for $C_L > 100pF$)	0-100	300
T_{Edge} [ns]	**10**	0.3	400	2	300	220 rising, 45 falling	0.8
Response Time (T_R) [ns]^X	**0.721**	0.2	14	0.113 ($C_L = 2pF$)	6.25 ($C_L = 100pF$)	10	0.9
Undershoot [mV]	**143**	322	255	80	65.1	230	59
Overshoot [mV]	**117**	227	170	77	0	133	71
ΔI_L [mA]	**0 $\Longrightarrow$ 10**	0.12 $\Longrightarrow$ 25	0.01 $\Longrightarrow$ 100	0.1 $\Longrightarrow$ 50	0 $\Longrightarrow$ 100	0 $\Longrightarrow$ 100	0.1 $\Longrightarrow$ 20
Load Regulation [mV/mA]	**0.187**	0.173	0.06	0.04	0.3	0.09	0.015
Line Regulation [mV/V]	**0.00193**	2.25	0.8	1	4.7	12	N/A
Recovery Time [μs]	**1.7**	0.19	0.7	1.25^{est}	6	3.2	0.2
FoM = $T_R \cdot \frac{I_Q}{I_{L,max}}$ [ps]	**0.613**	1.86	462	0.11	0.0562	1.4	1.45

The time response, T_R, has been computed as:

$$T_R = \frac{\Delta V_{OUT} C_L}{\Delta I_L}[s], T_R \gg T_{Edge} \tag{4.6}$$

And as [18]:

$$T_R = \sqrt{\frac{2C_L \Delta V_{OUT} T_{Edge}}{\Delta I_L}}[s], T_R < T_{Edge} \tag{4.7}$$

Eq. (4.7) is used to correct the initial T_R estimation from Eq. (4.6), in cases where the measured waveform respected the condition that $T_R < T_{Edge}$. In this design, T_R has been computed with Eq. (4.6). Several state-of-the-art designs are listed in Table 4.2 and a number of conclusions can be drawn:

1. One advantage of this design is that it does not require a minimum amount of load current in order for the LVR to be stable, such as [18], [19], [20] and [23].

2. Another advantage is that the design does not require an excessive amount of quiescent current, such as [18], [19] and [20].

3. A feature of this work is that it is scalable, both in terms of the load capacitance and of the load current. Some state-of-the-art designs are unstable for high load capacitances. The recovery time is also scalable, by accurately controlling the amount of current fed into the error amplifier via adaptive biasing, at the expense of degraded accuracy.

4. Design [21] has truly state-of-the-art performance in all aspects, except for degraded stability when driving high capacitive loads.

5. This design is comparable to state-of-the-art in terms of small area, low amount of quiescent current consumption and fast transient response.

5

Conclusions

5.1. Summary

This paper presents a current amplifier-based linear voltage regulator. In order to find an optimum architecture for the system, unwanted transient effects, i.e., capacitive coupling and consecutive load current steps limitation, have been identified and solutions have been implemented in order to overcome these effects. The current amplifier technique is introduced, different current amplifier implementations are discussed and analyzed, highlighting design trade-offs. The design focuses on minimizing the controller area and on maximizing the transient performance. Since the current amplifier concept is based on the I_{DS} vs V_{GS} curve of the output transistor, maximizing the current gain minimizes the required size of the NMOST output stage, which in turn minimizes the capacitance required both for decoupling and for stability. The interaction between the voltage and current loops is analyzed, offering a simple design procedure. The performance of the current amplifier is enhanced via the compensation resistors and an adaptive biasing technique has been proposed to overcome the bandwidth limitation caused by the decoupling capacitance.

This design has been implemented in a 140nm high voltage CMOS process and occupies an estimated area of 0.0078 mm^2. The simplicity of the architecture makes the system robust against PVT and the performance is comparable to state-of-the-art, fully integrated LDOs.

5.2. Future Work

The current amplifier technique is proven to be very powerful in aiding the transient response of the linear voltage regulator. A future study that would focus on a low voltage implementation of a current amplifier that will allow low dropout operation would extend the applicability of the current amplifier technique from usage in power control ICs to low voltage applications, ideally resulting in a simple, robust, fast transient and area efficient LDO.

A

Loop Gain Analysis Method

The measurement of loop gain in a closed loop by voltage injection or by current injection, as described by Middlebrook [24], provide a simple method to analyze the loop gain transfer function of a given circuit, taking into account the loading effects. Equations for the unilateral loop analysis have been used.

The voltage loop gain is given by:

$$\Pi_V := -\frac{v_y}{v_x}\Big|_{i_y=0} \tag{A.1}$$

Condition $i_y = 0$ means that node y is an open.

The current loop gain is given by:

$$\Pi_I := -\frac{i_y}{i_x}\Big|_{v_y=0} \tag{A.2}$$

Condition $v_y = 0$ means that node y is shorted to ground.

The loop gain is then given by:

$$\frac{1}{\Pi} = \frac{1}{\Pi_V} + \frac{1}{\Pi_I} \tag{A.3}$$

A.1. Approximations

Consider the cases from Fig. A.1.

Case 1:

- Neglecting C_{gs}, C_{gd}, a current source into the gate of a MOSFET (infinite impedance) will generate a potential $V_G = \infty$.
- This in turn will lead to $i_y = \infty$, where $i_x \neq 0$.

$$\Pi_I = -\frac{i_y}{i_x} = -\infty \tag{A.4}$$

$$\frac{1}{\Pi} = \frac{1}{\Pi_V} + \frac{1}{\Pi_I} = \frac{1}{\Pi_V} \tag{A.5}$$

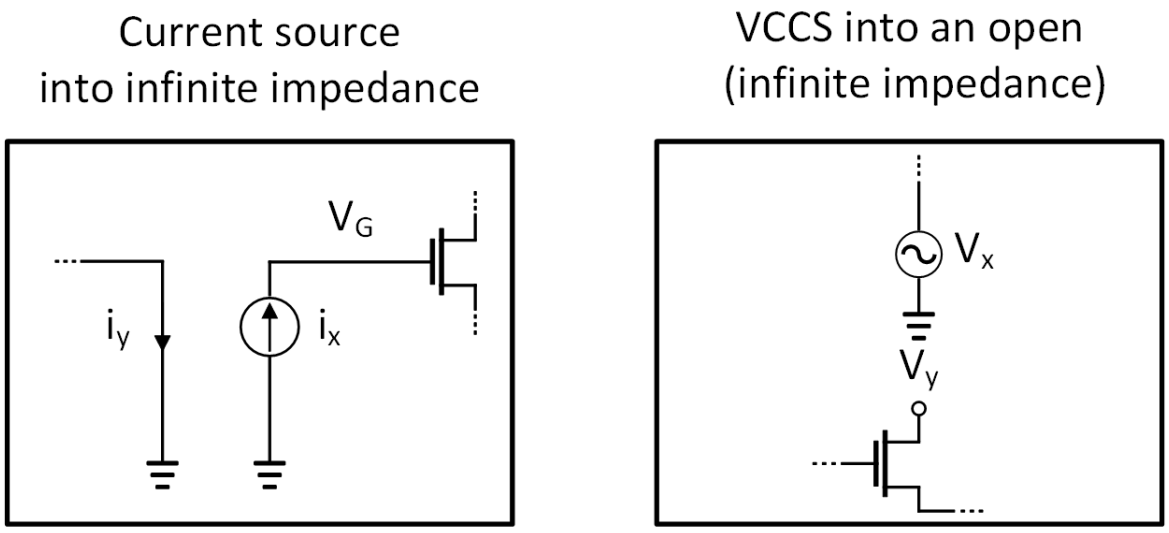

Figure A.1: Loop Breaking Points - Approximations

- Therefore, the loop gain is approximated by the voltage loop gain.

Case 2:

- A voltage controlled current source into an open (infinite impedance) will generate a potential $v_y = \infty$, where $v_x \neq 0$.
- This in turn will lead to:

$$\Pi_V = -\frac{v_y}{v_x} = -\infty \tag{A.6}$$

$$\frac{1}{\Pi} = \frac{1}{\Pi_V} + \frac{1}{\Pi_I} = \frac{1}{\Pi_I} \tag{A.7}$$

- Therefore, the loop gain is approximated by the current loop gain.

Voltage loop gain is sufficient to evaluate the loop gain of the LVR voltage loop.
Current loop gain is sufficient to evaluate the loop gain of the LVR CA loop.

B

Small-signal Derivations

B.1. Static Parameters

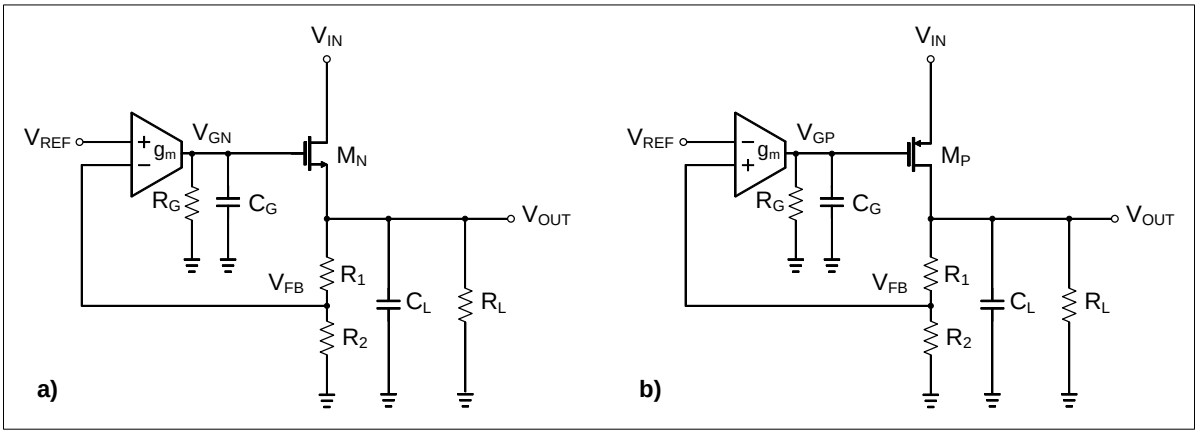

Figure B.1: a) NMOS-based LVR & b) PMOS-based LVR

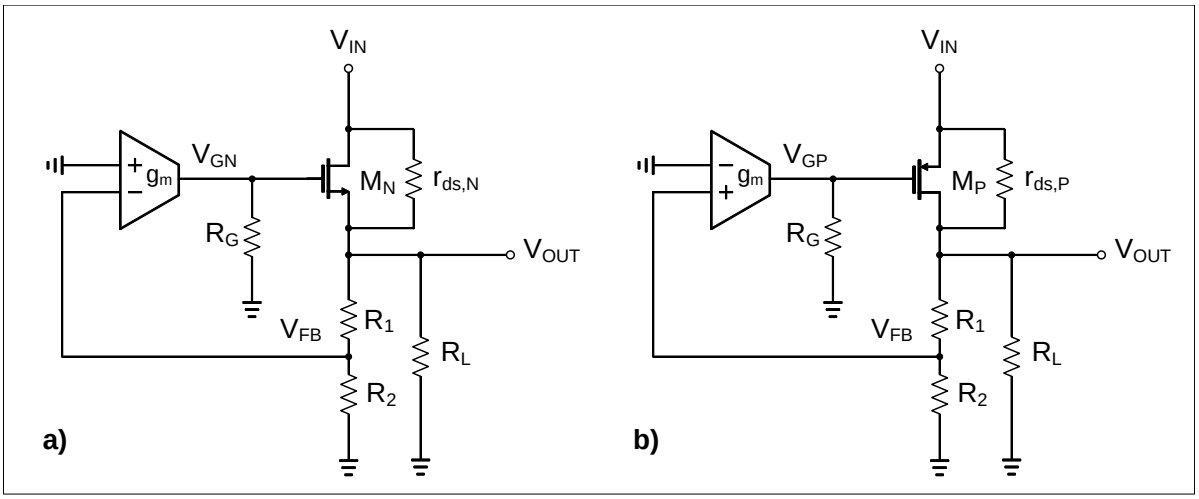

Figure B.2: Small-signal circuits for static line regulation analysis. a) NMOS-based LVR & b) PMOS-based LVR

B.1.1. NMOS Topology - Line Regulation

The small-signal analysis corresponding to Fig. B.1 a) can be done based on the small circuit domain circuit illustrated in Fig. B.2 a).

$$\Delta V_{GN} = -g_m R_G \cdot \Delta V_{FB} = -A_V \cdot \frac{R_2}{R_1 + R_2} \cdot \Delta V_{OUT} = -A_V \beta \Delta V_{OUT} \tag{B.1}$$

$$\Delta V_{GS} = \Delta V_{GN} - \Delta V_{OUT} = -A_V \beta \Delta V_{OUT} - \Delta V_{OUT} = -\Delta V_{OUT} \cdot \left(\beta A_V + 1\right) \tag{B.2}$$

Applying Kirchhoff's current law (KCL) at the output node yields:

$$g_{mN} \Delta V_{GS} + \frac{\Delta V_{IN} - \Delta V_{OUT}}{r_{ds,N}} = \Delta V_{OUT} \cdot \left(\frac{1}{R_1 + R_2} + \frac{1}{R_L}\right) = \frac{\Delta V_{OUT}}{R_{eq}} \tag{B.3}$$

Where:

$$R_{eq} = R_L || (R_1 + R_2) [\Omega] \tag{B.4}$$

Rearranging the equations:

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} = \frac{1}{1 + r_{ds,N} \cdot \left[\frac{1}{R_{eq}} + g_{mN} \cdot \left(\beta A_V + 1\right)\right]} \tag{B.5}$$

A_V represents the open loop gain of the error amplifier and is assumed large enough such that the following simplification can be made in Eq. (B.5):

$$g_{mN} \beta A_V >> \frac{1}{R_{eq}} + g_{mN} \tag{B.6}$$

Therefore:

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} \approx \frac{1}{\beta A_V \cdot g_{mN} \cdot r_{ds,N}} \tag{B.7}$$

B.1.2. PMOS Topology - Line Regulation

Therefore, based on Fig. B.1 b), the corresponding small-signal domain circuit is presented in Fig B.2 b). The $\Delta V_{OUT} / \Delta V_{IN}$ relationship can be derived as:

$$\Delta V_{GP} = g_m \cdot R_G \cdot \Delta V_{FB} = g_m R_G \frac{R_2}{R_1 + R_2} \Delta V_{OUT} = A_V \beta \Delta V_{OUT} \tag{B.8}$$

$$\Delta V_{SG} = \Delta V_{IN} - \Delta V_{GP} = \Delta V_{IN} - \beta A_V \Delta V_{OUT} \tag{B.9}$$

KCL at the output node yields:

$$g_{mP} \Delta V_{SG} + \frac{\Delta V_{IN} - \Delta V_{OUT}}{r_{ds,P}} = \frac{\Delta V_{OUT}}{R_{eq}} \tag{B.10}$$

Where:

$$R_{eq} = R_L || (R_1 + R_2) [\Omega] \tag{B.11}$$

Rearranging the equations, we arrive at:

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} = \frac{1 + g_{mP} r_{ds,P}}{r_{ds,P} \cdot \left(\frac{1}{R_{eq}} + \frac{1}{r_{ds,P}} + g_{mP} \beta A_V \right)} \tag{B.12}$$

A_V represents the open loop gain of the error amplifier and is assumed large enough such that the following simplifications can be made in Eq. (B.15):

$$g_{mP} \beta A_V >> \frac{1}{R_{eq}} + \frac{1}{r_{ds,P}} \tag{B.13}$$

$$g_{mP} r_{ds,P} >> 1 \tag{B.14}$$

Therefore:

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} \approx \frac{1}{\beta A_V} \tag{B.15}$$

It can be concluded that for the NMOS topology, the line regulation, given by Eq. (B.7), is improved by a factor equal to the intrinsic gain of the NMOS transistor, compared to the line regulation for the PMOS topology, given by Eq. (B.15).

The conclusion can also be reached by inspection. In the case of the NMOS topology, the pass device acts as a common gate (CG), or in other words, as a cascode device. Any voltage variation on the drain of the device will be attenuated by a factor equal to the intrinsic gain of the transistor when referred to the source of the device. Similarly, in the case of the PMOS topology, the pass device also acts as a CG or as a cascode device. Any voltage variation on the source of the device will be amplified by a factor equal to the intrinsic gain of the transistor when referred to the drain of the device.

B.1.3. NMOS Topology - Load Regulation

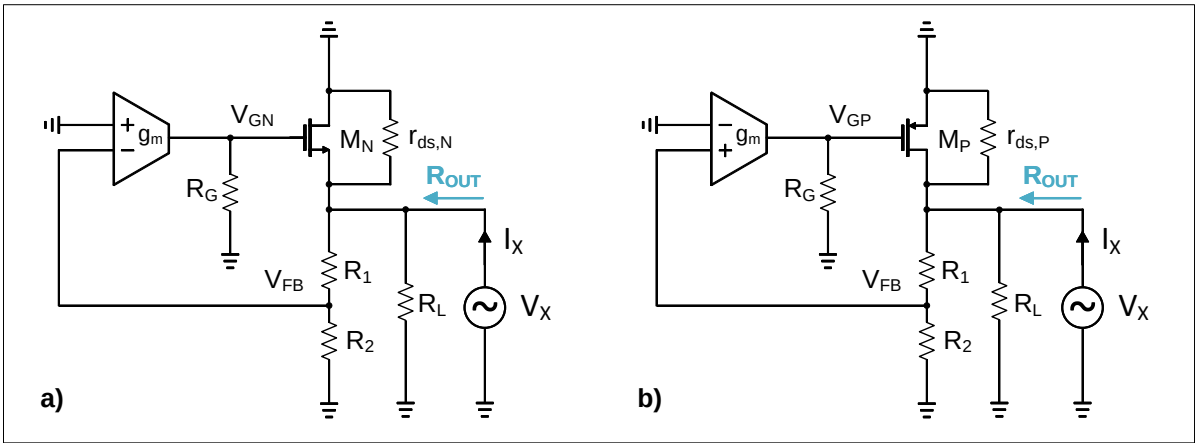

Figure B.3: Small-signal circuits for static load regulation analysis. a) NMOS-based LVR & b) PMOS-based LVR

Based on Fig. B.1 a), the corresponding small-signal domain circuit is presented in Fig. B.3 a). The $\Delta V_X / \Delta I_X$ relationship can be derived as:

$$\Delta V_{GN} = -g_m R_G \cdot \Delta V_{FB} = -A_V \cdot \frac{R_2}{R_1 + R_2} \cdot \Delta V_X = -A_V \beta \Delta V_X \tag{B.16}$$

$$\Delta V_{GS} = \Delta V_{GN} - \Delta V_X = -A_V \beta \Delta V_X - \Delta V_X = -\Delta V_X \cdot \left(\beta A_V + 1\right) \tag{B.17}$$

KCL at the output node yields:

$$\Delta I_X = \Delta V_X \cdot \left(\frac{1}{R_1 + R_2} + \frac{1}{R_L} + \frac{1}{r_{ds,N}}\right) - g_{mN} \Delta V_{GS} \tag{B.18}$$

$$\Delta I_X = \frac{\Delta V_X}{R_{eq}} + g_{mN} \Delta V_X (\beta A_V + 1) \tag{B.19}$$

Rearranging the equations:

$$\frac{\Delta V_X}{\Delta I_X} = \frac{1}{1 + \frac{1}{R_{eq}} + g_{mN} \beta A_V} \approx \frac{1}{g_{mN} \beta A_V} \tag{B.20}$$

B.1.4. PMOS Topology - Load Regulation

In a similar fashion, the small-signal analysis corresponding to Fig. B.1 b) can be done based on the small-signal domain circuit illustrated in Fig. B.3 b).

$$\Delta V_{GP} = g_m \cdot R_G \cdot \Delta V_{FB} = g_m R_G \frac{R_2}{R_1 + R_2} \Delta V_X = A_V \beta \Delta V_X \tag{B.21}$$

$$\Delta V_{SG} = 0 - \Delta V_{GP} = -\beta A_V \Delta V_X \tag{B.22}$$

KCL at the output node yields:

$$\Delta I_X = \Delta V_X \cdot \left(\frac{1}{R_1 + R_2} + \frac{1}{R_L} + \frac{1}{r_{ds,P}}\right) - g_{mP} \Delta V_{SG} \tag{B.23}$$

$$\Delta I_X = \Delta V_X \cdot \left(\frac{1}{R_{eq}} + g_{mP} \beta A_V\right) \tag{B.24}$$

Where:

$$R_{eq} = R_L || (R_1 + R_2) || r_{ds,P} \tag{B.25}$$

Rearranging the equations:

$$\frac{\Delta V_X}{\Delta I_X} = \frac{1}{\frac{1}{R_{eq}} + g_{mP} \beta A_V} \approx \frac{1}{g_{mP} \beta A_V} \tag{B.26}$$

Based on the obtained results, it can be concluded that the static load regulation for either the NMOS topology or the PMOS topology is the same.

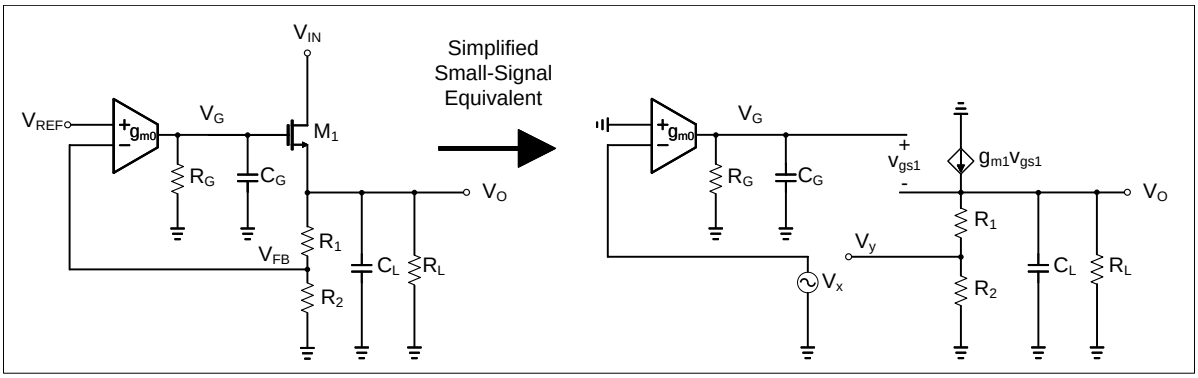

Figure B.4: NMOST-based LVR - Loop Gain Derivation

B.2. NMOST-based LVR - Loop Gain

KCL at node V_G yields:

$$-g_{m0} \cdot V_x = V_G \cdot \left(\frac{1}{R_G} + sC_G \right) \tag{B.27}$$

From which V_G can be written as:

$$V_G = -g_{m0} \cdot V_x \cdot \frac{R_G}{1 + sC_G R_G} \tag{B.28}$$

$$v_{gs1} = V_G - V_O = -g_{m0} \cdot V_x \cdot \frac{R_G}{1 + sC_G R_G} - V_O \tag{B.29}$$

KCL at the output node yields:

$$g_{m1} \cdot V_{GO} = V_O \cdot \left(\frac{1}{R_{eq}} + sC_L \right) \tag{B.30}$$

Where:

$$R_{eq} = (R_1 + R_2) || R_L \tag{B.31}$$

V_O can be extracted:

$$V_O = -V_x g_{m0} g_{m1} R_{eq} \frac{R_G}{1 + sR_G C_G} \cdot \frac{1}{1 + (sC_L + g_{m1}) R_{eq}} \tag{B.32}$$

$$V_y = V_O \cdot \frac{R_2}{R_1 + R_2} \tag{B.33}$$

The voltage loop gain is therefore given by:

$$L(s) = \frac{V_y}{V_x} = -g_{m0} R_G \frac{R_2}{R_1 + R_2} g_{m1} R_{eq} \cdot \frac{1}{(1 + sC_G R_G) \cdot \left[1 + (sC_L + g_{m1}) R_{eq} \right]} \tag{B.34}$$

Yielding two poles:

$$\omega_{P_1} = \frac{1}{C_G R_G} [rad/s] \tag{B.35}$$

$$\omega_{P_2} \approx \frac{g_{m1}}{C_L}[rad/s] \tag{B.36}$$

$$L_{DC} = -g_{m0}R_G\frac{R_2}{R_1+R_2}g_{m1}R_{eq} \tag{B.37}$$

B.2.1. Body Effect on Poles Position

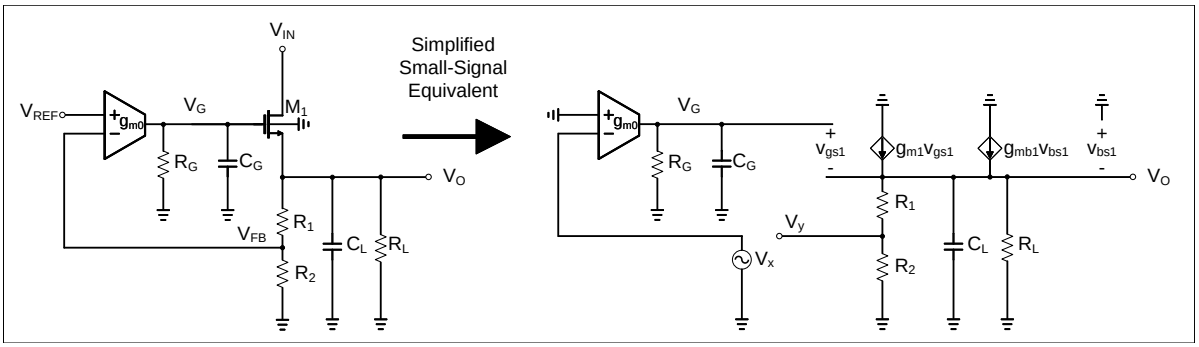

Figure B.5: NMOST-based LVR - Body Effect on Poles Position

KCL at node V_G yields:

$$-g_m V_X = V_G \cdot \left(\frac{1}{R_G} + sC_G\right) \tag{B.38}$$

This results in:

$$V_G = -\frac{A_V V_X}{1+sC_G R_G} \tag{B.39}$$

Where:

$$A_V = g_m \cdot R_G \tag{B.40}$$

Therefore:

$$\upsilon_{gs1} = V_G - V_O = -\frac{A_V V_X}{1+sC_G R_G} - V_O \tag{B.41}$$

$$\upsilon_{bs1} = 0 - V_O = -V_O \tag{B.42}$$

KCL at the output node yields:

$$g_{m1}\upsilon_{gs1} + g_{mb}\upsilon_{bs1} = V_O \cdot \left(\frac{1}{R_1+R_2} + \frac{1}{R_L} + sC_L\right) \tag{B.43}$$

Substituting υ_{gs1} and υ_{bs1}:

$$-g_{m1}\frac{A_V V_X}{1+sC_G R_G} - g_{m1}V_O - g_{mb1}V_O = V_O \cdot \left(\frac{1}{R_1+R_2} + \frac{1}{R_L} + sC_L\right) \tag{B.44}$$

Therefore:

$$-g_{m1}\frac{A_V V_X}{1+sC_G R_G} = V_O \cdot \left(\frac{1}{R_1+R_2}+\frac{1}{R_L}+sC_L+g_{m1}+g_{mb1}\right) \tag{B.45}$$

Multiply by $(R_1+R_2)R_L$:

$$-g_{m1}\frac{A_V V_X}{1+sC_G R_G}\cdot(R_1+R_2)R_L = V_O \cdot \left[R_L+(R_1+R_2)+(R_1+R_2)R_L\cdot(sC_L+g_{m1}+g_{mb1})\right] \tag{B.46}$$

$$V_y = \frac{R_2}{R_1+R_2}V_O = \beta V_O \implies V_O = \frac{V_y}{\beta} \tag{B.47}$$

Then:

$$-g_{m1}\frac{A_V V_X}{1+sC_G R_G}\cdot(R_1+R_2)R_L = \frac{V_y}{\beta} \cdot \left[R_L+(R_1+R_2)+(R_1+R_2)R_L\cdot(sC_L+g_{m1}+g_{mb1})\right] \tag{B.48}$$

Multiply by β:

$$-g_{m1}\frac{\beta A_V V_X}{1+sC_G R_G}\cdot(R_1+R_2)R_L = V_y \cdot \left[R_L+(R_1+R_2)+(R_1+R_2)R_L\cdot(sC_L+g_{m1}+g_{mb1})\right] \tag{B.49}$$

Then V_y/V_x can be found as:

$$\frac{V_y}{V_x} = -\frac{\beta A_V}{1+sC_G R_G}\cdot\frac{g_{m1}(R_1+R_2)R_L}{R_L+(R_1+R_2)+(R_1+R_2)R_L\cdot(sC_L+g_{m1}+g_{mb1})} \tag{B.50}$$

The DC loop gain is given by:

$$L_{DC} = -\beta A_V \cdot \frac{g_{m1}(R_1+R_2)R_L}{R_L+(R_1+R_2)+(R_1+R_2)R_L\cdot(g_{m1}+g_{mb1})} \tag{B.51}$$

Which can be approximated by:

$$L_{DC} = -\beta A_V \cdot \frac{g_{m1}}{g_{m1}+g_{mb1}} \tag{B.52}$$

Dominant pole given by:

$$\omega_{P_1} = -\frac{1}{C_G R_G}[rad/s] \tag{B.53}$$

Second, non-dominant pole deduction:

$$R_L+(R_1+R_2)+(R_1+R_2)R_L\cdot(sC_L+g_{m1}+g_{mb1}) = 0 \tag{B.54}$$

$$(R_1+R_2)R_L\cdot(sC_L+g_{m1}+g_{mb1}) = -R_L-(R_1+R_2) \tag{B.55}$$

$$(sC_L+g_{m1}+g_{mb1}) = -\frac{1}{R_1+R_2}-\frac{1}{R_L} \tag{B.56}$$

Then:

$$sC_L = -\frac{1}{R_1+R_2}-\frac{1}{R_L}-g_{m1}-g_{mb1} \approx -(g_{m1}+g_{mb1}) \implies \omega_{P_2} = -\frac{g_{m1}+g_{mb1}}{C_L}[rad/s] \tag{B.57}$$

B.3. NMOST-based LVR - Capacitive Division

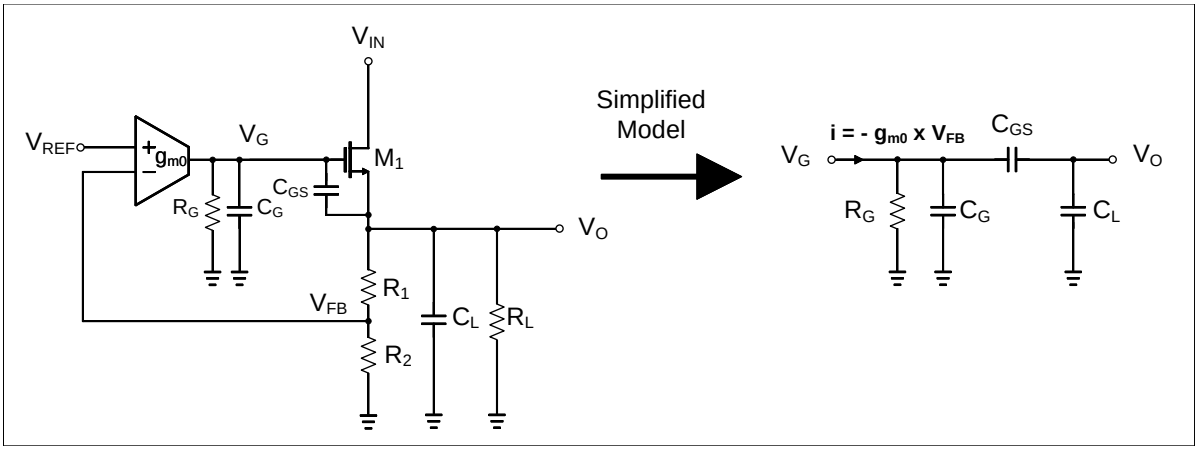

Figure B.6: NMOST-based LVR - Capacitive Division

$$\Delta V_{FB} = \frac{R_2}{R_1 + R_2} \cdot \Delta V_O \tag{B.58}$$

$$-g_{m0}\frac{R_2}{R_1 + R_2}\Delta V_O = \Delta V_G \cdot \left(\frac{1}{R_G} + sC_G\right) + \Delta V_{GO} sC_{GS} \tag{B.59}$$

$$\frac{\Delta V_G}{\Delta V_O}(s) = -\frac{g_{m0}R_2R_G + (R_1 + R_2)sC_{GS}R_G}{(R_1 + R_2)\cdot[1 + s(C_G + C_{GS})R_G]} \tag{B.60}$$

By considering a very fast voltage variation at the output, we obtain:

$$\lim_{s\to\infty}\frac{\Delta V_G}{\Delta V_O}(s) = -\frac{C_{GS}}{C_G + C_{GS}} \tag{B.61}$$

B.4. CA - Type I - Loop Gain

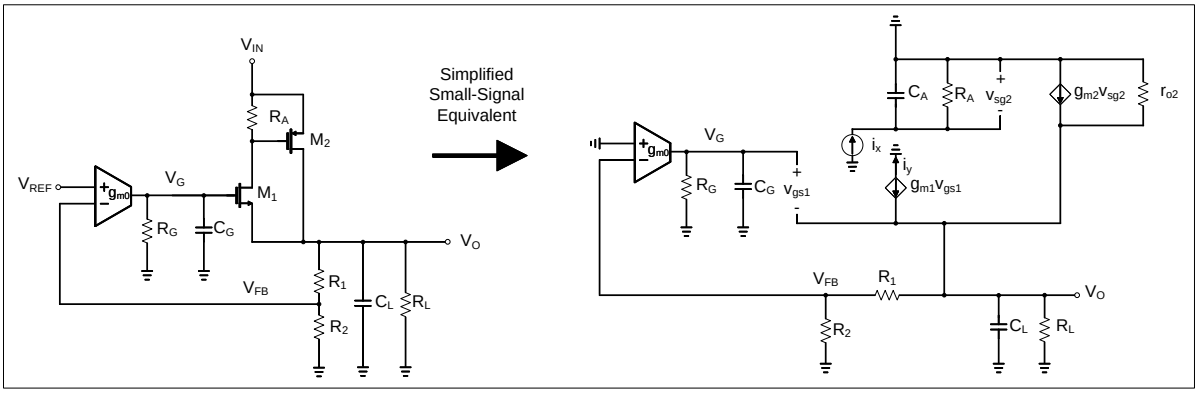

Figure B.7: Current Amplifier-based LVR - Type I - Loop Gain Derivation

Neglecting CLM of transistor M_1, the loop can be analyzed by measuring the current loop gain between the drain of transistor M_1 and the gate of transistor M_2.

$$i_x = V_A \cdot \left(\frac{1}{R_A} + sC_A \right) \tag{B.62}$$

$$V_A = i_x \cdot \frac{R_A}{1 + sC_A R_A} \tag{B.63}$$

Where:

$$V_A = -v_{sg2} \tag{B.64}$$

Potential V_{FB} is given by:

$$V_{FB} = \frac{R_2}{R_1 + R_2} \cdot V_O \tag{B.65}$$

The potential V_G can be found as:

$$(0 - V_{FB}) \cdot g_{m0} = V_G \cdot \left(\frac{1}{R_G} + sC_G \right) \tag{B.66}$$

$$V_G = -g_{m0} \cdot \frac{R_2}{R_1 + R_2} \cdot \frac{R_G}{1 + sC_G R_G} \cdot V_O \tag{B.67}$$

Therefore, $v_{gs1} = V_{GO}$ is given by:

$$v_{gs1} = V_{GO} = V_G - V_O = -\frac{g_{m0} R_G \frac{R_2}{R_1 + R_2} + (1 + sC_G R_G)}{1 + sC_G R_G} \cdot V_O \tag{B.68}$$

It can be noticed that:

$$i_{M1} = g_{m1} \cdot v_{gs1} = -i_y \tag{B.69}$$

$$i_{M2} = g_{m2} \cdot v_{sg2} = -i_x \cdot \frac{g_{m2} R_A}{1 + sC_A R_A} \tag{B.70}$$

From Equation (B.69):

$$V_O = -\frac{i_{M1}}{g_{m1}} \cdot \frac{1 + sC_G R_G}{g_{m0} R_G \frac{R_2}{R_1 + R_2} + (1 + sC_G R_G)} \tag{B.71}$$

By applying KCL at node V_O we find:

$$i_{M1} + i_{M2} = V_O \cdot \left(sC_L + \frac{1}{R_1 + R_2} + \frac{1}{r_{o2}} + \frac{1}{R_L} \right) \tag{B.72}$$

Where:

$$R_{eq} = R_L || r_{o2} || (R_1 + R_2) \tag{B.73}$$

Current i_{M1} and potential V_O are described in terms of i_y. Current i_{M2} is described in terms of i_x. Therefore, the current loop gain can be found from Equation (B.71) as:

$$\frac{i_y}{i_x} = -\frac{g_{m0}g_{m1}\frac{R_2}{R_1+R_2}R_GR_{eq} + (1+sC_GR_G)g_{m1}R_{eq}}{(1+sC_GR_G)(1+sC_LR_{eq}+g_{m1}R_{eq}) + g_{m0}g_{m1}\frac{R_2}{R_1+R_2}R_GR_{eq}} \cdot \frac{g_{m2}R_A}{1+sC_AR_A} \tag{B.74}$$

Where:

$$C_A = C_{gs2} + C_{gd2} \tag{B.75}$$

$$R_L = \frac{V_O}{I_L} \tag{B.76}$$

$$L_{DC} \approx -g_{m2} \cdot R_A \tag{B.77}$$

B.4.1. Poles/Zeros Approximation

Taking the denominator of the first term in Equation (B.74), expanding the equation and making it equal to 0 results in:

$$s^2C_LR_{eq}C_GR_G + s(C_LR_{eq} + C_GR_G + C_GR_Gg_{m1}R_{eq}) + 1 + g_{m1}R_{eq} + g_{m1}g_{m0}\frac{R_2}{R_1+R_2}R_GR_{eq} = 0 \tag{B.78}$$

With:

$$a = C_LR_{eq}C_GR_G \tag{B.79}$$

$$b = C_LR_{eq} + C_GR_G + C_GR_Gg_{m1}R_{eq} \tag{B.80}$$

$$c = 1 + g_{m1}R_{eq} + g_{m1}g_{m0}\frac{R_2}{R_1+R_2}R_GR_{eq} \tag{B.81}$$

The following approximations hold:

- $C_L \approx$ pF
- $C_G \approx$ pF
- $C_L \gg C_G$
- $R_{eq} \approx \Omega$
- $R_G \approx \text{M}\Omega$
- $g_{m0} \approx \mu$S
- $g_{m1} \approx$ mS

Sum of the poles is:

$$P_1 + P_2 = -\frac{b}{a} = -\frac{C_L R_{eq} + C_G R_G + C_G R_G g_{m1} R_{eq}}{C_L R_{eq} C_G R_G} \tag{B.82}$$

Making use of the previously mentioned approximations:

$$P_1 + P_2 \approx -\frac{C_G R_G + C_G R_G g_{m1} R_{eq}}{C_L R_{eq} C_G R_G} = -\frac{g_{m1} R_{eq} + 1}{C_L R_{eq}} \tag{B.83}$$

Product of the poles is:

$$P_1 P_2 = \frac{c}{a} = \frac{1 + g_{m1} R_{eq} + g_{m1} g_{m0} \frac{R_2}{R_1 + R_2} R_G R_{eq}}{C_L R_{eq} C_G R_G} \tag{B.84}$$

Making use of the previously mentioned approximations:

$$P_1 P_2 \approx \frac{g_{m1} g_{m0} \frac{R_2}{R_1 + R_2} R_G R_{eq}}{C_L R_{eq} C_G R_G} = \frac{g_{m1} g_{m0} \frac{R_2}{R_1 + R_2}}{C_L C_G} \tag{B.85}$$

Assuming that one of the poles is much larger than the other, then:

$$P_1 + P_2 \approx P_1 = -\frac{g_{m1} R_{eq} + 1}{C_L R_{eq}} \tag{B.86}$$

From the product of the poles P_2 can be found as:

$$P_2 \approx -\frac{g_{m1} g_{m0} R_2 R_{eq}}{C_G (R_1 + R_2)(1 + g_{m1} R_{eq})} \tag{B.87}$$

B.4.2. Body Effect on Poles Position

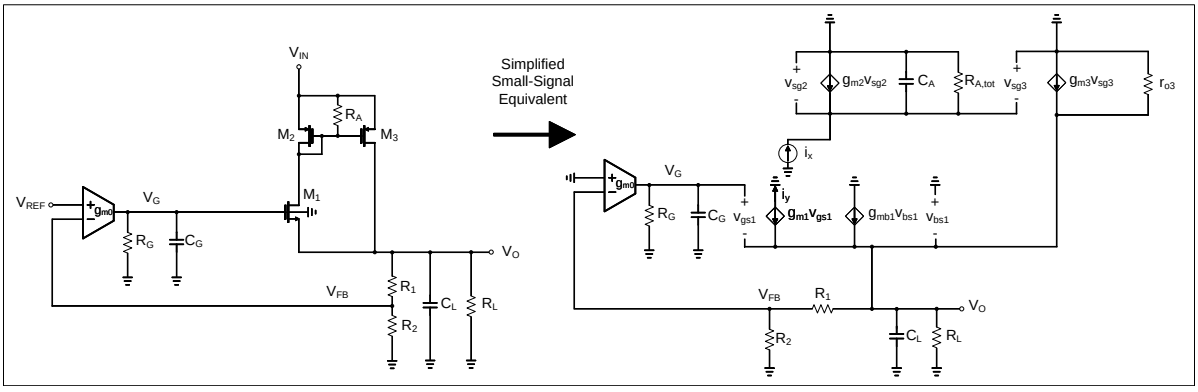

Figure B.8: Current Amplifier-based LVR - Type I - Body Effect on Poles Position

KCL at node V_G yields:

$$-g_m V_{FB} = V_G \cdot \left(\frac{1}{R_G} + sC_G \right) \tag{B.88}$$

Where:

$$V_{FB} = \frac{R_2}{R_1 + R_2} V_O = \beta V_O \tag{B.89}$$

This results in:

$$V_G = -\frac{\beta A_V V_O}{1 + sC_G R_G} \tag{B.90}$$

Where:

$$A_V = g_m \cdot R_G \tag{B.91}$$

Therefore:

$$v_{gs1} = V_G - V_O = -\frac{\beta A_V V_O}{1 + sC_G R_G} - V_O = -V_O \cdot \left(\frac{\beta A_V}{1 + sC_G R_G} + 1 \right) \tag{B.92}$$

$$v_{gs1} = -V_O \cdot \frac{\beta A_V + (1 + sC_G R_G)}{1 + sC_G R_G} \tag{B.93}$$

$$v_{bs1} = 0 - V_O = -V_O \tag{B.94}$$

Current I_{M1} is:

$$I_{M1} = -I_Y = -(g_{m1} v_{gs1} + g_{mb1} v_{bs1}) \tag{B.95}$$

$$I_{M1} = g_{m1} V_O \cdot \frac{\beta A_V + (1 + sC_G R_G)}{1 + sC_G R_G} + g_{mb1} V_O \implies I_{M1} = V_O \cdot \left(g_{m1} \frac{\beta A_V + (1 + sC_G R_G)}{1 + sC_G R_G} + g_{mb1} \right) \tag{B.96}$$

$$I_{M1} = V_O \cdot \frac{\beta A_V g_{m1} + (g_{m1} + g_{mb1}) \cdot (1 + sC_G R_G)}{1 + sC_G R_G} \tag{B.97}$$

From which V_O is obtained:

$$V_O = -i_Y \cdot \frac{1 + sC_G R_G}{\beta A_V g_{m1} + (g_{m1} + g_{mb1}) \cdot (1 + sC_G R_G)} \tag{B.98}$$

$$i_X = V_{G2} \cdot \left(sC_A + \frac{1}{R_A} \right) = V_{G2} \frac{1 + sC_A R_A}{R_A} \tag{B.99}$$

$$V_{G2} = i_X \cdot \frac{R_A}{1 + sC_A R_A} \tag{B.100}$$

$$v_{sg2} = -V_{G2} = -i_X \cdot \frac{R_A}{1 + sC_A R_A} \tag{B.101}$$

$$i_{M2} = -i_X \cdot \frac{g_{m2} R_A}{1 + sC_A R_A} \tag{B.102}$$

KCL at the output node yields:

$$i_{M1} + i_{M2} = V_O \cdot \left(\frac{1}{R_{eq}} + sC_L \right) \tag{B.103}$$

Where:

$$R_{eq} = R_L || (R_1 + R_2) || r_{ds2} [\Omega] \tag{B.104}$$

Substituting i_{M1}:

$$i_{M2} = V_O \cdot \left(\frac{1}{R_{eq}} + sC_L \right) - i_Y \tag{B.105}$$

$$i_{M2} = -i_Y \cdot \frac{1 + sC_G R_G}{\beta A_V g_{m1} + (g_{m1} + g_{mb1}) \cdot (1 + sC_G R_G)} \cdot \left(\frac{1 + sC_L R_{eq}}{R_{eq}} \right) - i_Y \tag{B.106}$$

$$i_{M2} = -i_Y \cdot \frac{(1 + sC_G R_G)(1 + sC_L R_{eq}) + R_{eq} \left[\beta A_V g_{m1} + (g_{m1} + g_{mb1}) \cdot (1 + sC_G R_G) \right]}{R_{eq} \left[\beta A_V g_{m1} + (g_{m1} + g_{mb1}) \cdot (1 + sC_G R_G) \right]} \tag{B.107}$$

$$i_{M2} = -i_Y \cdot \frac{(1 + sC_G R_G)(1 + sC_L R_{eq}) + R_{eq} \beta A_V g_{m1} + R_{eq} (g_{m1} + g_{mb1}) \cdot (1 + sC_G R_G)}{R_{eq} \left[\beta A_V g_{m1} + (g_{m1} + g_{mb1}) \cdot (1 + sC_G R_G) \right]} \tag{B.108}$$

$$i_{M2} = -i_Y \cdot \frac{(1 + sC_G R_G)(1 + sC_L R_{eq} + R_{eq} g_{m1} + R_{eq} g_{mb1}) + R_{eq} \beta A_V g_{m1}}{R_{eq} \left[\beta A_V g_{m1} + (g_{m1} + g_{mb1}) \cdot (1 + sC_G R_G) \right]} \tag{B.109}$$

Substituting i_{M2}:

$$-i_X \cdot \frac{g_{m2} R_A}{1 + sC_A R_A} = -i_Y \cdot \frac{(1 + sC_G R_G)(1 + sC_L R_{eq} + R_{eq} g_{m1} + R_{eq} g_{mb1}) + R_{eq} \beta A_V g_{m1}}{R_{eq} \left[\beta A_V g_{m1} + (g_{m1} + g_{mb1}) \cdot (1 + sC_G R_G) \right]} \tag{B.110}$$

Therefore:

$$\frac{i_Y}{i_X} = \frac{g_{m2} R_A}{1 + sC_A R_A} \cdot \frac{R_{eq} \beta A_V g_{m1} + R_{eq} (g_{m1} + g_{mb1}) \cdot (1 + sC_G R_G)}{(1 + sC_G R_G)(1 + sC_L R_{eq} + R_{eq} g_{m1} + R_{eq} g_{mb1}) + R_{eq} \beta A_V g_{m1}} \tag{B.111}$$

The pole will be pushed to higher frequencies because of the body effect, increasing stability. The pole position is approximated using the procedure from CA - Type I loop gain derivation.

$$\omega_{P_2} \approx -\frac{1 + (g_{m1} + g_{mb1}) R_{eq}}{C_L R_{eq}} [rad/s] \tag{B.112}$$

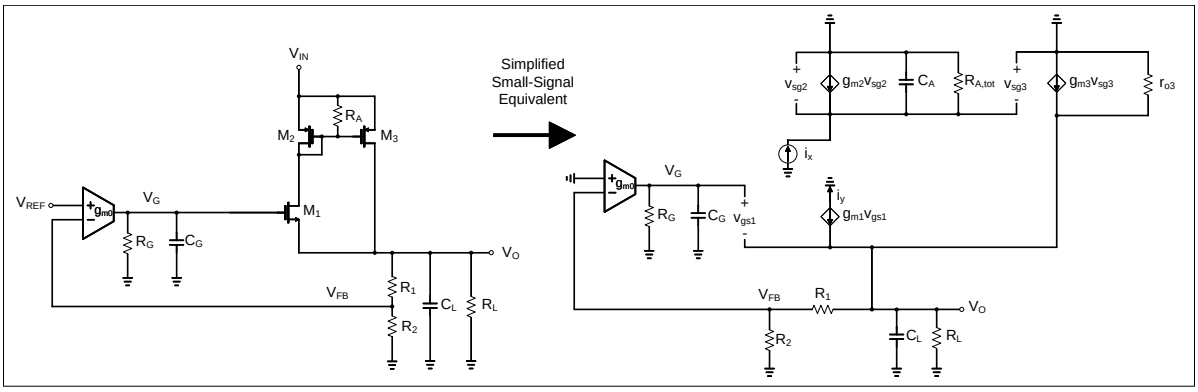

Figure B.9: Current Amplifier-based LVR - Type II - Loop Gain Derivation

B.5. CA - Type II - Loop Gain

Potential V_{FB} is given by:

$$V_{FB} = \frac{R_2}{R_1 + R_2} \cdot V_O \tag{B.113}$$

The potential V_G can be found as:

$$(0 - V_{FB}) \cdot g_{m0} = V_G \cdot \left(\frac{1}{R_G} + sC_G \right) \tag{B.114}$$

$$V_G = -g_{m0} \cdot \frac{R_2}{R_1 + R_2} \cdot \frac{R_G}{1 + sC_G R_G} \cdot V_O \tag{B.115}$$

Therefore, $v_{gs1} = V_{GO}$ is given by:

$$v_{gs1} = V_{GO} = V_G - V_O = -\frac{g_{m0} R_G \frac{R_2}{R_1 + R_2} + (1 + sC_G R_G)}{1 + sC_G R_G} \cdot V_O \tag{B.116}$$

It can be noticed that:

$$i_x = V_A \cdot \left(\frac{1}{R_{A,tot}} + sC_A \right) - g_{m2} v_{sg2} \tag{B.117}$$

$$V_A = i_x \cdot \frac{R_{A,tot}}{1 + s(C_A + g_{m2}) R_{A,tot}} \tag{B.118}$$

Where:

$$V_A = -v_{sg2} = -v_{sg3} \tag{B.119}$$

$$R_{A,tot} = r_{o2} || R_A \tag{B.120}$$

$$i_{M1} = g_{m1} \cdot v_{gs1} = -i_y \tag{B.121}$$

$$i_{M3} = g_{m3} \cdot v_{sg3} = -i_x \cdot \frac{g_{m3} R_{A,tot}}{1 + s(C_A + g_{m2}) R_{A,tot}} \tag{B.122}$$

From Equation (B.121):

$$V_O = -\frac{i_{M1}}{g_{m1}} \cdot \frac{1 + sC_G R_G}{g_{m0} R_G \frac{R_2}{R_1+R_2} + (1 + sC_G R_G)} \tag{B.123}$$

By applying KCL at node V_O we find:

$$i_{M1} + i_{M3} = V_O \cdot \left(sC_L + \frac{1}{R_1 + R_2} + \frac{1}{r_{o3}} + \frac{1}{R_L} \right) \tag{B.124}$$

Where:

$$R_{eq} = R_L || r_{o3} || (R_1 + R_2) \tag{B.125}$$

Current i_{M1} and potential V_O are described in terms of i_y. Current i_{M3} is described in terms of i_x. Therefore, the current loop gain can be found from Equation (B.123) as:

$$L(s) = \frac{i_y}{i_x} = -\frac{g_{m0} g_{m1} \frac{R_2}{R_1+R_2} R_G R_{eq} + (1 + sC_G R_G) g_{m1} R_{eq}}{(1 + sC_G R_G)(1 + sC_L R_{eq} + g_{m1} R_{eq}) + g_{m0} g_{m1} \frac{R_2}{R_1+R_2} R_G R_{eq}} \cdot \frac{g_{m3} R_{A,tot}}{1 + s(C_A + g_{m2}) R_{A,tot}} \tag{B.126}$$

Where:

$$C_A = C_{gs2} + C_{gs3} + C_{gd3} \tag{B.127}$$

$$R_L = \frac{V_O}{I_L} \tag{B.128}$$

$$L_{DC} \approx -\frac{g_{m3}}{g_{m2}} \tag{B.129}$$

B.5.1. Poles/Zeros Approximation

Since only the non-dominant pole is now shifted in frequency, the poles/zeros approximation is the same as for CA - Type I.

Non-dominant pole:

$$1 + (sC_A + g_{m2}) R_{A,tot} = 0 \tag{B.130}$$

From which:

$$s = -\frac{1 + g_{m2} R_{A,tot}}{C_A R_{A,tot}} \tag{B.131}$$

The following approximations hold:

- $R_{A,tot} \approx \text{k}\Omega$
- $g_{m2} \approx \text{mS}$

Therefore:

$$\omega_{P_3} \approx -\frac{g_{m2}}{C_A} [rad/s] \tag{B.132}$$

The non-dominant pole is now pushed further away in frequency.

B.6. CA - Type III - Loop Gain

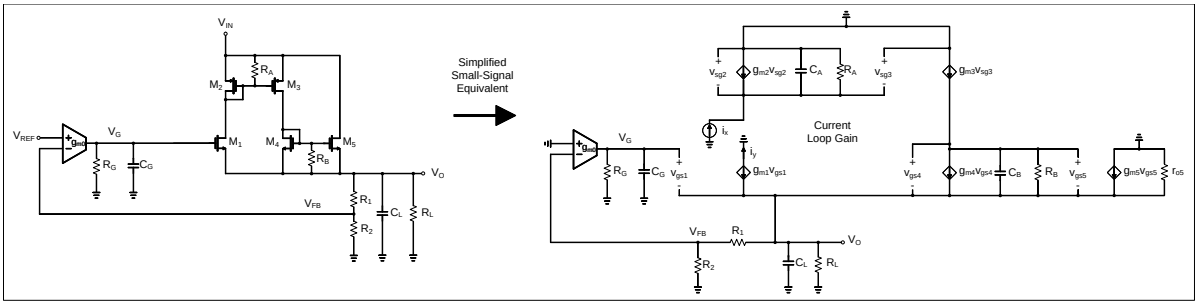

Figure B.10: Current Amplifier-based LVR - Type III - Loop Gain Derivation

Neglecting CLM of transistor M_1, the loop can be analyzed by measuring the current loop gain between the drain of transistor M_1 and the gate of transistor M_2.

Following a similar procedure as for Current Amplifier I and II:

Potential V_{FB} is given by:

$$V_{FB} = \frac{R_2}{R_1 + R_2} \cdot V_O \tag{B.133}$$

The potential V_G can be found as:

$$(0 - V_{FB}) \cdot g_{m0} = V_G \cdot \left(\frac{1}{R_G} + sC_G \right) \tag{B.134}$$

$$V_G = -g_{m0} \cdot \frac{R_2}{R_1 + R_2} \cdot \frac{R_G}{1 + sC_G R_G} \cdot V_O \tag{B.135}$$

Therefore, $v_{gs1} = V_{GO}$ is given by:

$$v_{gs1} = V_{GO} = V_G - V_O = -\frac{g_{m0} R_G \frac{R_2}{R_1 + R_2} + (1 + sC_G R_G)}{1 + sC_G R_G} \cdot V_O \tag{B.136}$$

It can be noticed that:

$$i_x = V_A \cdot \left(\frac{1}{R_{A,tot}} + sC_A \right) - g_{m2} v_{sg2} \tag{B.137}$$

$$V_A = i_x \cdot \frac{R_{A,tot}}{1 + s(C_A + g_{m2}) R_{A,tot}} \tag{B.138}$$

Where:

$$V_A = -v_{sg2} = -v_{sg3} \tag{B.139}$$

$$R_{A,tot} = r_{o2} || R_A \tag{B.140}$$

$$i_{M1} = g_{m1} \cdot v_{gs1} = g_{m1} \cdot V_{GO} = -i_y \tag{B.141}$$

$$i_{M3} = g_{m3} \cdot v_{sg3} = -g_{m3} \cdot V_A = -i_x \cdot \frac{g_{m3} R_{A,tot}}{1 + (sC_A + g_{m2}) R_{A,tot}} \tag{B.142}$$

$$i_{M3} = v_{gs4} \cdot \left(g_{m4} + \frac{1}{R_{B,tot}} + sC_B \right) \tag{B.143}$$

From which we can extract v_{gs4}:

$$v_{gs4} = i_{M3} \cdot \frac{R_{B,tot}}{1 + (sC_B + g_{m4}) R_{B,tot}} \tag{B.144}$$

Current i_{M5} can be found as:

$$i_{M5} = g_{m5} \cdot v_{gs5} = i_{M3} \cdot \frac{g_{m5} R_{B,tot}}{1 + (sC_B + g_{m4}) R_{B,tot}} = -i_x \cdot \frac{g_{m3} R_{A,tot}}{1 + (sC_A + g_{m2}) R_{A,tot}} \cdot \frac{g_{m5} R_{B,tot}}{1 + (sC_B + g_{m4}) R_{B,tot}} \tag{B.145}$$

From Equation (B.141):

$$V_O = -\frac{i_{M1}}{g_{m1}} \cdot \frac{1 + sC_G R_G}{g_{m0} R_G \frac{R_2}{R_1 + R_2} + (1 + sC_G R_G)} \tag{B.146}$$

By applying KCL at node V_O we find:

$$i_{M1} + i_{M3} + i_{M5} = V_O \cdot \left(sC_L + \frac{1}{R_1 + R_2} + \frac{1}{r_{o5}} + \frac{1}{R_L} \right) \tag{B.147}$$

Where:

$$R_{eq} = R_L || r_{o5} || (R_1 + R_2) \tag{B.148}$$

The sum of currents i_{M3}, i_{M5} can be found as:

$$i_{M3} + i_{M5} = -i_x \cdot \frac{g_{m3} R_{A,tot} \cdot \left[1 + (sC_B + g_{m4} + g_{m5}) R_{B,tot} \right]}{\left[1 + (sC_A + g_{m2}) R_{A,tot} \right] \cdot \left[1 + (sC_B + g_{m4}) R_{B,tot} \right]} \tag{B.149}$$

Current i_{M1} and potential V_O are described in terms of i_y. Current i_{M3} and current i_{M5} are described in terms of i_x. Therefore, the current loop gain can be found from Equation (B.147) as:

$$L(s) = \frac{i_y}{i_x} = -\frac{g_{m0} g_{m1} \frac{R_2}{R_1 + R_2} R_G R_{eq} + (1 + sC_G R_G) g_{m1} R_{eq}}{(1 + sC_G R_G)(1 + sC_L R_{eq} + g_{m1} R_{eq}) + g_{m0} g_{m1} \frac{R_2}{R_1 + R_2} R_G R_{eq}} \cdot \frac{g_{m3} R_{A,tot} \cdot \left[1 + (sC_B + g_{m4} + g_{m5}) \right.}{\left[1 + (sC_A + g_{m2}) R_{A,tot} \right] \cdot \left[1 + (sC_B + g \right.} \tag{B.150}$$

Where:

$$C_A = C_{gs2} + C_{gs3} + C_{gd3} \tag{B.151}$$

$$C_B = C_{gs4} + C_{gs5} + C_{gd5} \tag{B.152}$$

$$R_L = \frac{V_O}{I_L} \tag{B.153}$$

$$L_{DC} = -\frac{g_{m3}}{g_{m2}} \cdot \left(1 + \frac{g_{m5}}{g_{m4}}\right) \approx -\frac{g_{m3}}{g_{m2}} \cdot \frac{g_{m5}}{g_{m4}} \tag{B.154}$$

$$R_{A,tot} = R_A || r_{o2} \tag{B.155}$$

$$R_{B,tot} = R_B || r_{o4} \tag{B.156}$$

B.6.1. Poles/Zeros Approximation

An extra pole and an extra zero are obtained:

$$\omega_{P_4} = -\frac{g_{m4} R_{B,tot} + 1}{C_B R_B} \approx -\frac{g_{m4}}{C_B} [rad/s] \tag{B.157}$$

$$\omega_{Z_2} = -\frac{(g_{m4} + g_{m5}) R_{B,tot} + 1}{C_B R_B} \approx -\frac{g_{m4} + g_{m5}}{C_B} [rad/s] \tag{B.158}$$

The following approximations hold:

- $R_{B,tot} \approx$ hundreds of Ω kΩ
- $g_{m4}, g_{m5} \approx$ mS
- $g_{m4} R_{B,tot} \gg 1$
- $g_{m5} R_{B,tot} \gg 1$

B.7. CA - Type IV - Loop Gain

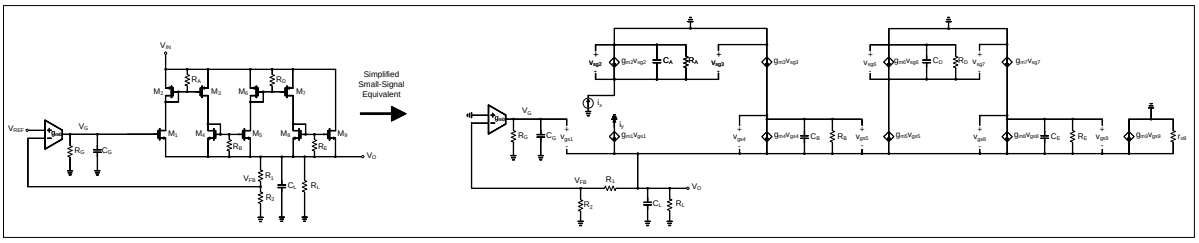

Figure B.11: Current Amplifier-based LVR - Type IV - Loop Gain Derivation

Neglecting CLM of transistor M_1, the loop can be analyzed by measuring the current loop gain between the drain of transistor M_1 and the gate of transistor M_2.

Following a similar procedure as for CA - Type I, II, & III:

$$R_{A,tot} = r_{o2} || R_A \tag{B.159}$$

$$R_{B,tot} = r_{o4} || R_B \tag{B.160}$$

$$R_{D,tot} = r_{o6} || R_D \tag{B.161}$$

$$R_{E,tot} = r_{o8} || R_E \tag{B.162}$$

$$i_x = V_A \cdot \left(\frac{1}{R_{A,tot}} + sC_A \right) - g_{m2} v_{sg2} \tag{B.163}$$

$$V_A = i_x \cdot \frac{R_{A,tot}}{1 + s(C_A + g_{m2}) R_{A,tot}} \tag{B.164}$$

Where:

$$V_A = -v_{sg2} = -v_{sg3} \tag{B.165}$$

Potential V_{FB} is given by:

$$V_{FB} = \frac{R_2}{R_1 + R_2} \cdot V_O \tag{B.166}$$

The potential V_G can be found as:

$$(0 - V_{FB}) \cdot g_{m0} = V_G \cdot \left(\frac{1}{R_G} + sC_G \right) \tag{B.167}$$

$$V_G = -g_{m0} \cdot \frac{R_2}{R_1 + R_2} \cdot \frac{R_G}{1 + sC_G R_G} \cdot V_O \tag{B.168}$$

Therefore, $v_{gs1} = V_{GO}$ is given by:

$$v_{gs1} = V_{GO} = V_G - V_O = -\frac{g_{m0} R_G \frac{R_2}{R_1 + R_2} + (1 + sC_G R_G)}{1 + sC_G R_G} \cdot V_O \tag{B.169}$$

It can be noticed that:

$$i_{M1} = g_{m1} \cdot v_{gs1} = g_{m1} \cdot V_{GO} = -i_y \tag{B.170}$$

$$i_{M3} = g_{m3} \cdot v_{sg3} = -g_{m3} \cdot V_A = -i_x \cdot \frac{g_{m3} R_{A,tot}}{1 + (sC_A + g_{m2}) R_{A,tot}} \tag{B.171}$$

$$i_{M3} = v_{gs4} \cdot \left(g_{m4} + \frac{1}{R_{B,tot}} + sC_B \right) \tag{B.172}$$

From which v_{gs4} can be extracted as:

$$v_{gs4} = i_{M3} \cdot \frac{R_{B,tot}}{1 + (sC_B + g_{m4}) R_{B,tot}} \tag{B.173}$$

Current i_{M5} can be found as:

$$i_{M5} = g_{m5} \cdot v_{gs5} = i_{M3} \cdot \frac{g_{m5} R_{B,tot}}{1 + (sC_B + g_{m4}) R_{B,tot}} = -i_x \cdot \frac{g_{m3} R_{A,tot}}{1 + (sC_A + g_{m2}) R_{A,tot}} \cdot \frac{g_{m5} R_{B,tot}}{1 + (sC_B + g_{m4}) R_{B,tot}} \tag{B.174}$$

$$-i_{M5} = -g_{m6} v_{sg6} + V_D \left(\frac{1}{R_D} + sC_D \right) \tag{B.175}$$

Where:

$$V_D = -v_{sg6} \tag{B.176}$$

From which v_{sg6} can be extracted as:

$$v_{sg6} = -V_D = i_{M5} \cdot \frac{R_D}{\left[1 + (sC_D + g_{m6})R_D\right]} \tag{B.177}$$

Current i_{M7} can be found as:

$$i_{M7} = g_{m7} \cdot v_{sg6} = i_{M5} \cdot \frac{g_{m7}R_D}{1 + (sC_D + g_{m6})R_D} \tag{B.178}$$

$$i_{M7} = -i_x \cdot \frac{g_{m3}R_{A,tot}}{1 + (sC_A + g_{m2})R_{A,tot}} \cdot \frac{g_{m5}R_{B,tot}}{1 + (sC_B + g_{m4})R_{B,tot}} \cdot \frac{g_{m7}R_D}{\left[1 + (sC_D + g_{m6})R_D\right]} \tag{B.179}$$

$$i_{M7} = g_{m8}v_{gs8} + v_{gs8} \cdot \left(\frac{1}{R_E} + sC_E\right) \tag{B.180}$$

From which v_{gs8} can be extracted as:

$$v_{gs8} = i_{M7} \cdot \frac{R_E}{\left[1 + (sC_E + g_{m8})R_E\right]} \tag{B.181}$$

Current i_{M9} can be found as:

$$i_{M9} = g_{m9}v_{gs9} = i_{M7} \cdot \frac{g_{m9}R_E}{\left[1 + (sC_E + g_{m8})R_E\right]} \tag{B.182}$$

$$i_{M9} = -i_x \cdot \frac{g_{m3}R_{A,tot}}{1 + (sC_A + g_{m2})R_{A,tot}} \cdot \frac{g_{m5}R_{B,tot}}{1 + (sC_B + g_{m4})R_{B,tot}} \cdot \frac{g_{m7}R_D}{\left[1 + (sC_D + g_{m6})R_D\right]} \cdot \frac{g_{m9}R_E}{\left[1 + (sC_E + g_{m8})R_E\right]} \tag{B.183}$$

From Equation (B.170):

$$V_O = -\frac{i_{M1}}{g_{m1}} \cdot \frac{1 + sC_GR_G}{g_{m0}R_G\frac{R_2}{R_1+R_2} + (1 + sC_GR_G)} \tag{B.184}$$

By applying KCL at node V_O we find:

$$i_{M1} + i_{M3} + i_{M5} + i_{M7} + i_{M9} = V_O \cdot \left(sC_L + \frac{1}{R_1 + R_2} + \frac{1}{r_{o9}} + \frac{1}{R_L}\right) \tag{B.185}$$

Where:

$$R_{eq} = R_L||r_{o9}||(R_1 + R_2) \tag{B.186}$$

The sum of currents i_{M3}, i_{M5}, i_{M7} and i_{M9} can be found as:

$$i_{M3} + i_{M5} + i_{M7} + i_{M9} = -i_x \cdot g_{m3}R_{A,tot} \cdot \frac{T_1 + T_2}{T_3} \tag{B.187}$$

$$T_1 = g_{m3}R_{A,tot} \cdot \left[(g_{m4} + g_{m5} + sC_B)R_B + 1\right] \cdot \left[(g_{m6} + sC_D)R_D + 1\right] \cdot \left[(g_{m8} + sC_E)R_E + 1\right] \tag{B.188}$$

$$T_2 = g_{m3}R_{A,tot}g_{m5}R_B g_{m7}R_D \cdot \left[(g_{m8} + g_{m9} + sC_E)R_E + 1\right] \tag{B.189}$$

$$T_3 = \left[(g_{m2} + sC_A)R_{A,tot} + 1\right] \cdot \left[(g_{m4} + sC_B)R_B + 1\right] \cdot \left[(g_{m6} + sC_D)R_D + 1\right] \cdot \left[(g_{m8} + sC_E)R_E + 1\right] \tag{B.190}$$

Current i_{M1} and potential V_O are described in terms of i_y. Currents i_{M3}, i_{M5}, i_{M7} and i_{M9} are described in terms of i_x. Therefore, the current loop gain can be found from Equation (B.185) as:

We can call:

$$TF_1(s) = \frac{g_{m0}g_{m1}\frac{R_2}{R_1+R_2}R_G R_{eq} + (1 + sC_G R_G)g_{m1}R_{eq}}{(1 + sC_G R_G)(1 + sC_L R_{eq} + g_{m1}R_{eq}) + g_{m0}g_{m1}\frac{R_2}{R_1+R_2}R_G R_{eq}} \tag{B.191}$$

$$L(s) = \frac{i_y}{i_x} = -TF_1(s) \cdot g_{m3}R_{A,tot} \cdot \frac{T_1 + T_2}{T_3} \tag{B.192}$$

Where:

$$C_A = C_{gs2} + C_{gs3} + C_{gd3} \tag{B.193}$$

$$C_B = C_{gs4} + C_{gs5} + C_{gd5} \tag{B.194}$$

$$C_D = C_{gs6} + C_{gs7} + C_{gd7} \tag{B.195}$$

$$C_E = C_{gs8} + C_{gs9} + C_{gd9} \tag{B.196}$$

$$R_L = \frac{V_O}{I_L} \tag{B.197}$$

$$L_{DC} = -\frac{g_{m3}}{g_{m2}} \cdot \left\{1 + \frac{g_{m5}}{g_{m4}} \cdot \left[1 + \frac{g_{m7}}{g_{m6}} \cdot \left(1 + \frac{g_{m9}}{g_{m8}}\right)\right]\right\} \approx -\frac{g_{m3}}{g_{m2}} \cdot \frac{g_{m5}}{g_{m4}} \cdot \frac{g_{m7}}{g_{m6}} \cdot \frac{g_{m9}}{g_{m8}} \tag{B.198}$$

B.7.1. Poles/Zeros Approximation

We obtain an extra pole and an extra zero:

$$\omega_{P_3} = -\frac{g_{m2}R_{A,tot} + 1}{C_A R_{A,tot}} \approx -\frac{g_{m2}}{C_A}[rad/s] \tag{B.199}$$

$$\omega_{P_4} = -\frac{g_{m4}R_{B,tot} + 1}{C_B R_{B,tot}} \approx -\frac{g_{m4}}{C_B}[rad/s] \tag{B.200}$$

$$\omega_{P_5} = -\frac{g_{m6}R_{D,tot}+1}{C_D R_{D,tot}} \approx -\frac{g_{m6}}{C_D}[rad/s] \tag{B.201}$$

$$\omega_{P_6} = -\frac{g_{m8}R_{E,tot}+1}{C_E R_{E,tot}} \approx -\frac{g_{m8}}{C_E}[rad/s] \tag{B.202}$$

The following approximations hold:

- $g_{mi} \approx$ mS
- $R_i \approx$ kΩ
- $g_{m2}R_{A,tot} \gg 1$
- $g_{m4}R_{B,tot} \gg 1$
- $g_{m6}R_{D,tot} \gg 1$
- $g_{m8}R_{E,tot} \gg 1$

B.7.2. Matlab Simulation

The loop gain equation has been implemented in Matlab and verified against the Cadence simulation for C_L = 50pF, I_L = 10mA, V_{OUT} = 1.8V, V_{IN} = 5V. It is important to mention that R_L requires to be modified to 320Ω from 180Ω in order to properly match the pole-zero pair caused by the voltage loop. This could be caused by the simplified small-signal model. The parameters are:

g_{m0} = 1.78μS; g_{m1}=3.78mS; g_{m2}=783μS; g_{m3}=1.69mS; g_{m4}=2.06mS; g_{m5}=4.505mS; g_{m6}=2.38mS; g_{m7}=5.008mS; g_{m8}=4.190mS; g_{m9}=8.884mS;

r_{o1}=22.38kΩ; r_{o2}=96kΩ; r_{o3}=126.257kΩ; r_{o4}=28.217kΩ; r_{o5}=17.439kΩ; r_{o6}=21.889kΩ; r_{o7}=26.739kΩ; r_{o8}=10.31kΩ; r_{o9}=8.038kΩ; R_A = 50kΩ; $R_B = r_{o4}$; $R_D = r_{o6}$; $R_E = r_{o8}$; R_1 = 77kΩ; R_2 = 200kΩ; R_G = 394.288MΩ;

$Cgs2$ = 18fF; $Cgs3$ = 36.28fF; $Cgd3$ = 9.135fF; $Cgs4$ = 18.878fF; $Cgd4$ = 4.886fF; $Cgs5$ = 37.72fF;

$Cgd5$ = 9.931fF; $Cgs6$ = 38.1fF; $Cgd6$ = 9.796fF; $Cgs7$ = 76.18fF; $Cgd7$ = 19.64fF; $Cgs8$ = 28.45fF;

$Cgs9$ = 55.96fF; $Cgd9$ = 15.8fF; C_A = 63.5fF; C_B = 66.529fF; C_D = 133.92fF; C_E = 100.21fF; C_G = 3pF;

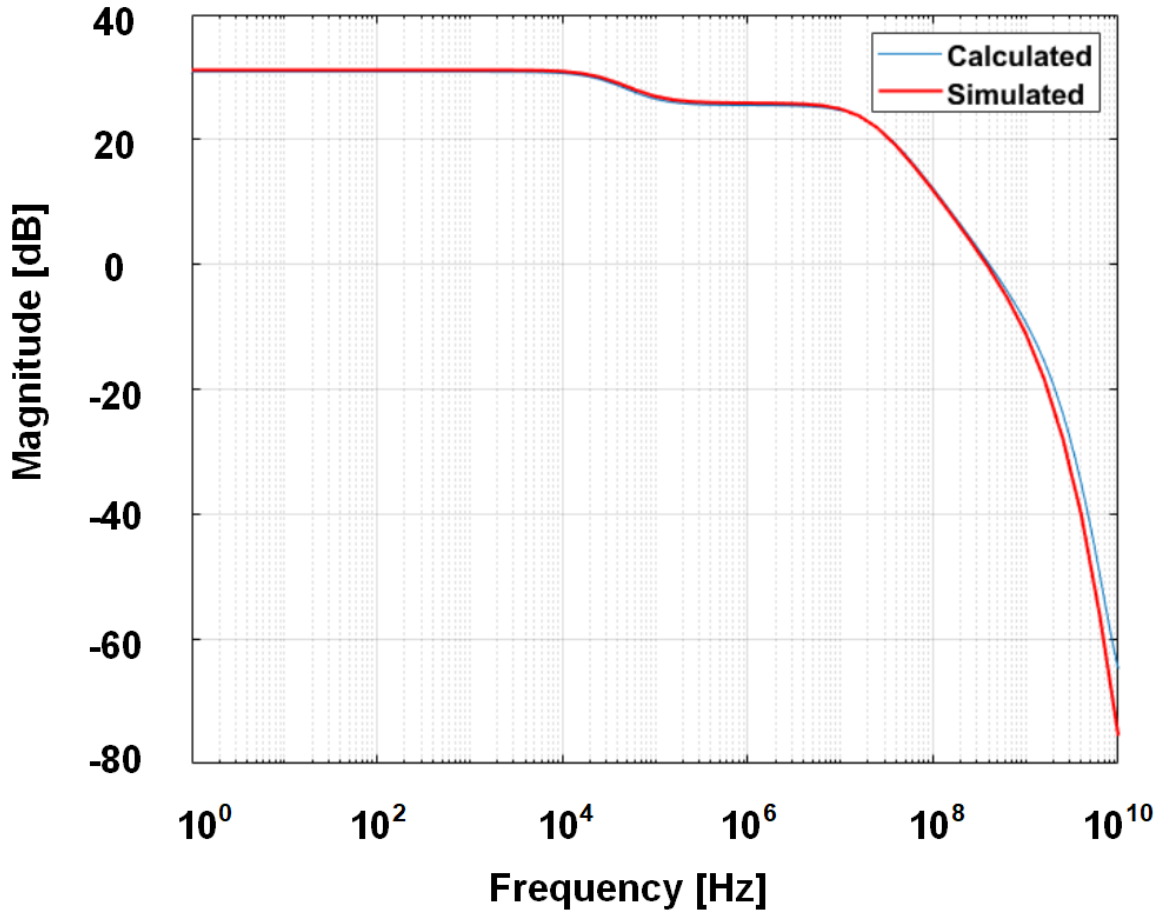

Figure B.12: Current Amplifier-based LVR - Type IV - Matlab Simulation

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