Fabrication of Transfer-free Corrugated Graphene Electrodes for Neuroelectronic Applications

Master of Science in Biomedical Engineering
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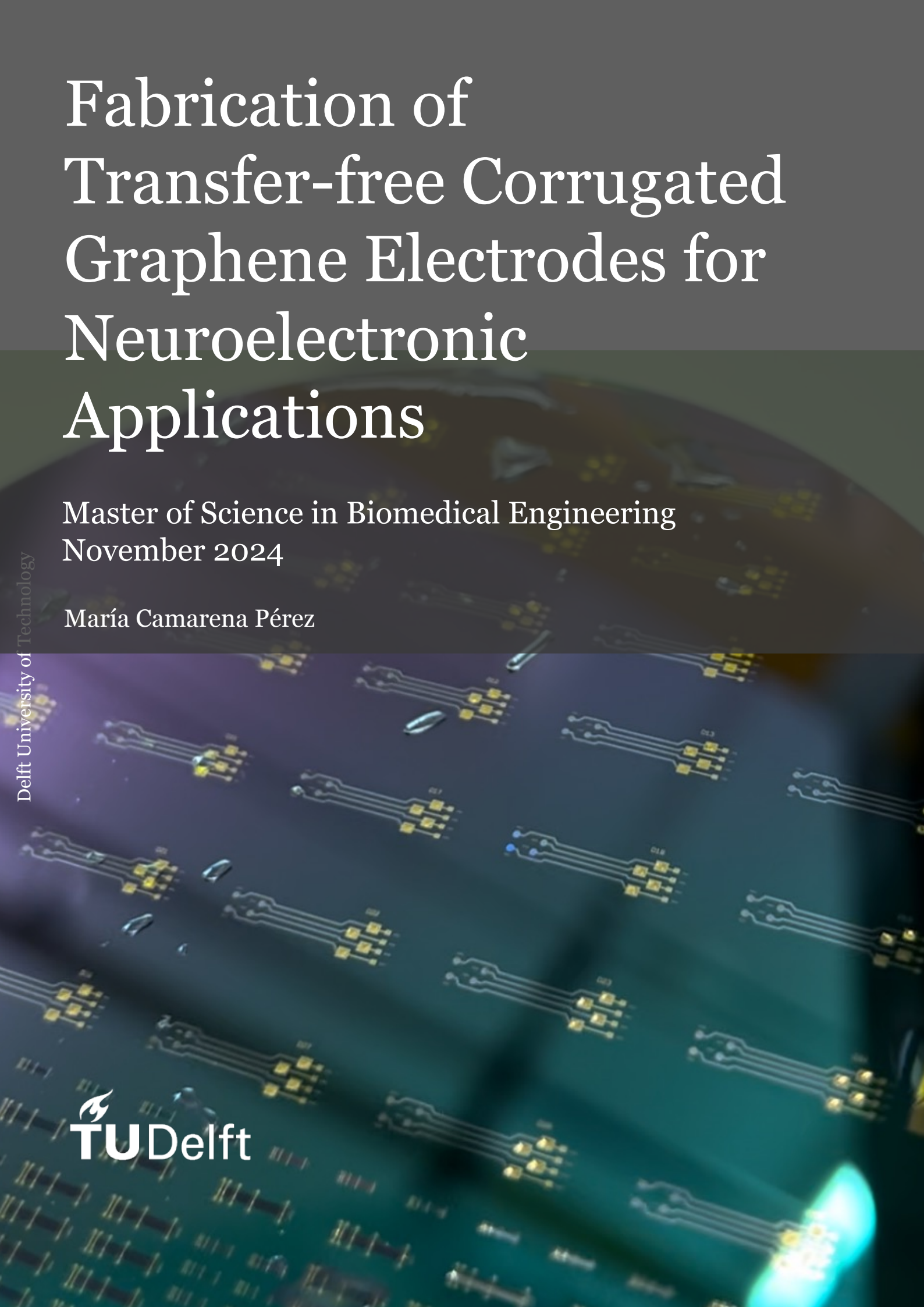

TU Delft

Fabrication of Transfer-free Corrugated Graphene Electrodes

for Neuroelectronic Applications

by

M. Camarena

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Abstract

Graphene-based neural interfaces offer an innovative solution to surpass the resolution limit of traditional neural recording, integrating neuroelectronics with optogenetics for combined electrophysiological and optical neural monitoring, among others. Three important factors in these interfaces are achieving a high signal-to-noise ratio (SNR), maintaining effective stimulation properties, and ensuring strong cell adhesion to neural tissue, which can be enhanced through surface topography modifications. This work explores two main approaches to enhance graphene-based neural interfaces: (1) exploring the creation of thin graphene films on molybdenum to integrate transistors and electrodes within a single fabrication process, which can potentially enhance the signal-to-noise ratio (SNR) while maintaining stimulation efficacy; and (2) creating corrugated graphene structures that increase surface area and improve cell adhesion. A major challenge in this work is establishing a transfer-free chemical vapor deposition (CVD) process on molybdenum for both approaches. While this method offers significant benefits, such as reducing defects and contamination, the challenge lies in the limited understanding of the mechanisms behind graphene growth on this catalyst. Exploring new molybdenum configurations to provide a better understanding of the graphene growth mechanism on this catalyst is also a relevant part of this work.

Experiments revealed that graphene grown on thick, unpatterned molybdenum produced high quality few layer graphene (FLG), while patterned thick molybdenum produced multilayer structures with high defect density. Based on the results obtained, a mechanism for graphene growth on thick molybdenum catalysts is proposed. However, the decision was made to proceed with the second research approach due to time limitations. Considering corrugated graphene structures, Raman analysis showed higher-quality graphene layers within the valleys, fact that supports the proposed growth model. sheet resistance values ranged from 60 Ω/sq – 180 Ω/sq, being these values among the lowest reported in the literature for undoped graphene. These low values are attributed to the combination of an FLG graphene with good interlayer electronic coupling, which is possible because of the low number of defects in the material. Results are promising for enabling high-density optically transparent neural interfaces with graphene tracks. Additionally, small and denser corrugations enhanced the electrode surface area, showing reduced impedance at 1 kHz compared to flat electrodes. Electrodes with 1 µm, 5 µm, and 20 µm corrugations shown impedance reductions in comparison to flat electrode, demonstrating an increased surface area. The area normalized impedance decreased from 35.5 kΩ ± 0.7 kΩ for flat electrodes to a minimum of 26.2 kΩ ± 1.1 kΩ. The electrodes achieved a maximum charge storage ca- pacity (CSC) of 80.6 µC/cm^2 and a maximum charge injection capacity (CIC) of 7.71 µC/cm^2, which are lower than the threshold for stimulation applications. However, these values could be potentially optimized through fabrication refinement. Furthermore, the biocompatibility tests indicated that corrugated graphene patterns are biocompatible have the potential to actively influence stem cell cytoskeleton dynamics, highlighting their promise as a safe and novel inclusion in interfaces for next-generation neural applications.

M. Camarena
Delft, November 2024

Acknowledgments

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Mamá, Papá, I am grateful for every second we spend together, physically and remotely. From you I have learned that every moment we have in this reality is a gift. You are the perfect example of taking the most out of life daily and unconditionally. You are my life inspiration. You are, and always will be, the loves of my life.

M. Camarena
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1 Introduction

Analysing the neuronal signals is of particular relevance for understanding the physiological performance of the nervous system and for identifying diseases associated with neurological malfunctioning, such as Parkinson's and Alzheimer's Diseases [1]. For this, it is of particular interest to understand the communication mechanisms of neurons. Transmission of information between neurons is mediated by changes in the polarity of the cell membrane, which is typically between -65 mV and -85 mV at rest for neurons. Threshold stimuli can cause depolarisation of the cell membrane, shifting the potential to positive values (usually +30 mV) and generating what are known as action potentials. Once the stimulus reaches the neuronal axon, neutrotransmitters are released as a consequence of Ca2+ ions influx during depolarization, transmitting the stimulus to the following neuron [2]. This way, electrical impulses can be transmitted between neurons, and information can be spread throughout a neuronal network. Conversely, considering a single neuron, minor alterations in membrane polarity may occur due to small, local changes in the ion concentration, temperature and pH changes, and even intrinsic neuronal activity. These small changes in the membrane potential are known as graded potentials, and although individual ones are not large enough to completely depolarise the membrane, their combination in time can lead to membrane depolarization and a consequent action potential, and may even mediate information transmission [3, 4]. Therefore, graded potentials can function as a mechanism for modulating information transmission and preventing excessive neuronal firing under certain conditions [5].

Neuronal signals can be recorded using extracellular recording techniques, employing electrodes or transistors to detect changes in extracellular voltage; in the case of transistors, the gate is responsible for sensing these variations. Both types of interfaces are particularly useful for understanding neuronal functioning without infiltrating the cells [6, 7]. Additionally, neural stimulation using electrodes has become increasingly relevant for treating pathologies related to the nervous system [8, 9]. Materials and structures used for recording electrodes should provide the lowest possible impedance to provide optimal signal to noise ratio (SNR). The SNR of an electrode is directly affected by its impedance, as higher impedance values generate higher thermal noise [10]. Typically, impedance values present in vivo values between 50 kΩ and 1MΩ [11]. Moreover, the electrodes used for stimulation must have a large charge injection capacity and a large charge storage capacity. Usually, materials that can provide all three characteristics are used, such as titanium nitride, iridium oxide, platinum and tantalum [11]. Considering transistors for neural recording, high transconductance and small gate capacitance are required parameters [12]. Typically, combining both recording and stimulation modalities are necessary to investigate the underlying mechanisms of neurological diseases and provide personalised treatment, being therefore crucial that both modalities work effectively simultaneously. Interfaces based solely on electrodes are typically used to offer both modalities (recording and stimulation in a single device). Alternatively, since transistor configurations offer higher SNR in reduced dimensions [13], integrating electrodes and transistors as neural interfaces in the same device could offer a solution for supporting both recording and stimulation modalities. An schematic example of this proposed neural interface is depicted in the Figure 1.1.

Despite achieving satisfactory results, electrophysiological recordings still have an intrinsic limitation: the specific neurons generating the recorded signal might not be sensed. The same issue arises

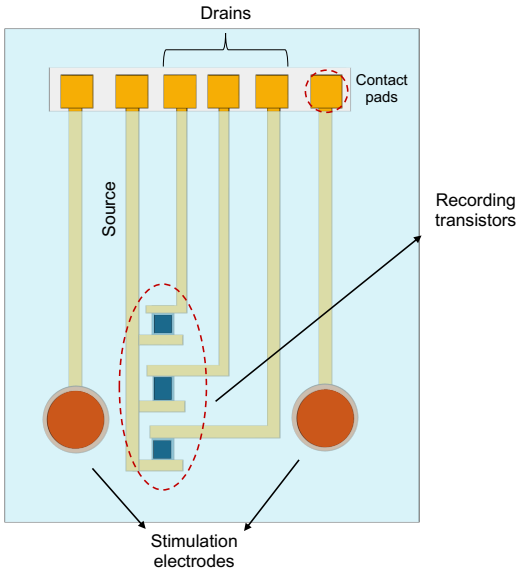

Figure 1.1: Schematic representation of a possible neural interface constitued by transistors and electrodes.

with stimulation: large interface sizes make it impossible to determine which specific neuron is being stimulated. This is known as the spatial resolution limit of the neural interfaces [14]. For this reason, there is an emerging necessity to combine neuroelectronic interfaces with techniques that allow the accurate identification of the specific neural region. Additionally, to ensure correct adaptation to the tissue, it is also necessary to improve the characteristics of the interfaces, such as flexibility and topography [15, 16]. It is therefore essential to explore materials and structures that offer the possibility of addressing all these challenges.

1.1. Strategies to Overcome the Resolution Limit

As mentioned, brain neuroelectronic interfaces have a limitation related to the spacial resolution due to the micrometric scale required. One of the most promising strategies to overcome this drawback is to combine them with image-based techniques and methods, which can provide a high accurate monitoring of cells with high spacial resolution. To achieve this, it becomes essential to have efficient transparent neuroelectronic interfaces that can be potentially integrated with optical imaging methods.

Over the last decades, effort has been made in integrating efficient transparent electronics in high technology applications. In the context of neuroelectronic interfaces, two of the most relevant material requirements are its biocompatibility and its adaptability to the tissue (therefore, its flexibility). Transparent electronics based on oxides such as zinc oxide (ZnO) and indium-tin oxide (ITO) are successfully used in industrial applications [17, 18]. However, the application of ITO and ZnO to the biomedical field is limited due to possible cytotoxic effects and poor mechanical properties, respectively [19, 20]. This has led the scientific community to study other types of materials with better biocompatibility and mechanical properties, such as conductive polymers and carbon-based materials. Carbon nanotubes (CNTs) have excelent conductive and mechanical properties, and can therefofe be considered as potential material for surface functionalization. However, its cytotoxicity remains under investigation, as it appears to interfere with the normal functioning of certain types of cell groups [21]. On the other hand, PEDOT:PSS and graphene as conductive, transparent materials are being successfully used to fabricate state of the art neural interfaces, with graphene being an outstanding material since its properties are not significantly impacted by humidity or high temperatures [22, 23]. The positive results in electrical performance, biocompatibility and mechanical properties of transparent electronics based on graphene enable the combination of these with optical imaging techniques that help improving the spatial resolution.

Examples of optical imaging techniques that can be potentially used to overcome the spatial resolution limit are intrinsic optical signal (IOS), voltage sensitive dyes (VSDs) based images and optical coherence tomography (OCT). IOS imaging is based on the hemodynamic variations in the neurons

related to their activity, allowing the indirect recording of neuronal performance in a non-invasive way with a spatial resolution of around 100 μm [24]. On the other hand, VSDs based techniques make use of molecules that respond to a change in voltage by emitting signals in certain ranges of the visible spectrum. An example of VSDs are certain molecules that emit light after binding to calcium, which makes them particularly powerful in detecting neuronal activity with resolutions in some cases lower than 50 μm [25, 26]. Lastly, OCT is based on measuring the light backscattering caused by the sample. From those mentioned, this technique provides the highest spatial resolution, achieving values between 1 μm and 15 μm [27]. Figure 1.2 shows the difference in capabilities that a transparent interface can offer compared to an opaque interface in a situation when both modalities are combines. As can be seen, transparent interfaces offer the possibility of obtaining OCT images seamlessly [28].

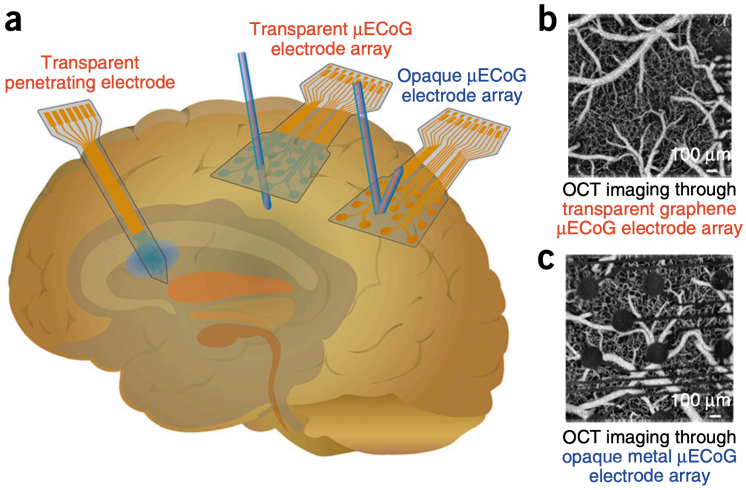

Figure 1.2: Comparison between transparent and opaque electrode interfaces. a) Schematic representation of a transparent penetrating electrode, a transparent electrode array and a opaque electrode array. As can be observed, the transparent interfaces would allow light to penetrate the tissue. b) OCT image obtained through a transparent graphene electrode array. c) OCT image obtained through a transparent graphene electrode array, where electrodes do not allow the image to be seen completely [28].

Additionally, another approach that employs light as a core tool is optogenetics which, by means of combining optics with genetics, can provide both high temporal and cellular precision. The central component of this technology are light-sensitive proteins known as opsins, which are microbial transmembrane channels that, when exposed to specific wavelengths of light, can directly or indirectly generate ionic currents in cells [29]. These currents can cause depolarisation, as in the case of Channelrhodopsin-2 after activation by blue light (460 nm), or hyperpolarisation of the cell membrane, as in the case of Halorhodopsin when stimulated by green light (570 nm) [30, 31]. For practical applications of optogenetic techniques, target cells are modified by introducing the transmembrane protein expression gene via a virus vector. As a result, diseases can be studied in genetically modified animal models, which can help in understanding the functioning of neurodegenerative diseases and unlock new insights that may lead to more effective treatments [32]. Despite significant advancements, applying optogenetics in human therapeutics remains a challenge, as it requires several factors that might generate a risk for the patient [33].

All the above mentioned light-based techniques can be integrated with transparent electronics. Selecting materials that allow this integration, while ensuring proper tissue interaction and adequate device performance, is therefore essential for achieving successful diagnoses and treatments. As mentioned above, graphene is a potentially promising material due to its electrical, mechanical and biocompatible properties [34]. Graphene-based transparent neuroelectronic devices combined with optics-based imaging techniques have already been successfully implemented [35, 36]. However, one of the current challenges is the efficient integration of graphene into microfabrication processes.

1.2. Graphene and Microfabrication Processes: the Transfer Issue

Since the isolation and identification of monolayer graphene in 2004 [37], many advances have been made in the technology and techniques used to produce graphene. One of the most reliable ways for its production is by chemical vapour deposition (CVD) using transition metals as catalysts, usually Ni or Cu, which offers excellent possibilities for the large-scale, controlled synthesis of graphene [38]. However, most processes require transferring the graphene from the catalyst to the substrate of interest using usually a support material. The process generally requires three fundamental steps: 1) adhesion of graphene to the transfer substrate, 2) delamination of the graphene from the catalytic substrate, and 3) deposition of the graphene on the target substrate [39]. A sacrificial material is typically used to assist this procedure, being usually a polymer, such as polymethyl methacrylate (PMMA), due to their excellent conformability. However, the transfer process introduces imperfections and contamination in the material. Figure 1.3 shows a schematic representation of some of the possible adverse consequences resulting from the transfer process. Undesired particles such as polymer debris, polymer etchant or water itself can get adhered to graphene and remain attached even after removing the sacrificial material. In addition, transferring a material to a different substrate may create mechanical stresses that may depend on the target material, its topography and surface treatments, which can lead to wrinkles and cracks on the graphene sheet. Other problems can also stem from the interface created between the graphene and the polymer, such as the creation of bubbles and the extreme flexibility of the polymer, which can lead to cracks in the graphene [40]. Due to the significant reduction of the graphene quality and practicality caused by these issues, effort is being applied by the scientific community to avoid as much as possible the adverse effects of the transfer.

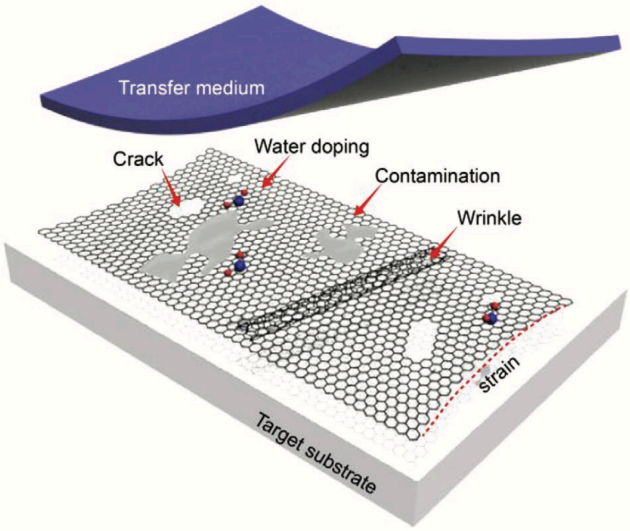

Figure 1.3: Schematic representation of a CVD graphene transfer process using a transfer substrate, where the adverse implications intrinsic to the transfer process are highlighted [40].

Despite all efforts, transferring graphene in a residue-free way and avoiding quality-degrading modifications of the material remains a challenge. Additionally, when considering microfabrication processes, it is usually desirable to carry out all processes on the same initial wafer in order to ensure compatibility with industrial-level production and improve cost-efficiency. Therefore, the ideal scenario is to synthesize CVD graphene directly on a catalyst that is part of the same wafer, avoiding transfer processes. For this, it is necessary to consider catalysts compatible with all the microfabrication processes. In addition, catalyst removal must be carried out safely to ensure the integrity of the wafer structures and materials. Molybdenum can potentially be considered for this particular scenario, as it can offer very exotic properties for this application, such as its high melting point and similar thermal expansion coefficient to that of silicon [41]. Production of CVD graphene using molybdenum has already been successfully implemented in neural interfaces manufacturing [42], but the graphene growth process is not as widely understood as in the case of Cu or Ni. Nevertheless, considering all the advantages of using molybdenum, this material will be used as a catalyst for graphene synthesis. More

detail information related to CVD graphene grown on this catalyst will be provided in Section 2.2.2. Part of this work will therefore involve exploring CVD graphene growth on a SiO2 substrate.

1.3. Objectives of the Project

This work pursues one main, general objective: contribute to the performance enhancement and optimization of graphene-based neural interfaces. For this, two main research lines have been established.

Considering the motivation behind the first research line, combining components that operate effectively in both recording and stimulation modalities is fundamental to create accurate, high-performance interfaces. A promising solution would be to combine the creation of transistors for recording with electrodes for stimulation by considering a single fabrication flowchart and using graphene as the material for both structures. However, as will be further explained in Section 2.3, single layer graphene (SLG) or few layer graphene (FLG) is usually preferred for a transistor structure, while multilayer graphene (MLG) is more suitable for stimulation electrodes. In addition, this work aims to work with transfer-free graphene using a molybdenum catalyst. Multilayer graphene can be manufactured in the laboratory, and it has already been used to create graphene electrodes [42]. However, the fabrication of SLG and MLG strucutres on the same die is a challenge considering a transfer-free process. Therefore, one of the fundamental questions is: can FLG/SLG-based transistors and MLG-based electrodes be created in the same transfer-free process, in the same die? The exploration of available technology can be summarized in the following objectives:

- Explore the catalyst characteristics needed to produce monolayer and few layer graphene.
- Use substrates (molybdenum structures) with different thicknesses to explore the possibility of creating graphene with different properties using the same wafer.
- Analyse and understand the differences between the graphene obtained on a molybdenum patterned before and after the CVD process.
- Characterise the fabricated materials.

An alternative approach towards the enhancement of graphene-based neural interfaces involves modifying the electrode topography by developing corrugated graphene surfaces, which defines the second line of research. Modifications in electrode surface have the potential to improve the cell adhesion and increase the electrode surface area. Additionally, graphene corrugated structures have proven to offer enhanced mechanical properties. All these points are supported by literature (see sections 2.1.3 and 2.2.1). Although information on corrugated graphene and graphene transferred to a previously corrugated pattern can be found in the literature, there are no studies on transfer free CVD graphene produced using molybdenum that consider a corrugated pattern. Compared to graphene grown on a flat surface, variations in the properties of graphene manufactured on corrugated structures are to be expected, requiring careful analysis of the obtained material. To address these challenges, this work introduces the following research question: can transfer-free, corrugated graphene surfaces be created? Can corrugated surfaces change graphene growth and impact the electrode properties? The following objectives are associated with these main questions:

- Design corrugated graphene electrodes and corrugated graphene test structures to analyse the electrical and material properties.
- Develope a process flow for the manufacturing of corrugated graphene electrodes.
- Investigate the impact of the microfabrication parameters and corrugation patterns variations on graphene properties.
- Characterise the electrochemical properties of the electrodes.
- Evaluate the material biocompatibility using in vitro cardiomyocyte cells.

1.4. Outline of the Report

This work is divided into seven Chapters. Chapter 2 provides an overview of the conventional implantable devices used for neural recording and stimulation, as well as the role of topography in cell adhesion and the improvement of electrode efficiency through topography modifications. Graphene and its properties will also be discussed, as well as graphene-based technology for neural interfaces.

In this work, two different although related lines of research have been followed. The first focuses on exploring the available technology for fabricating graphene-based structures, while the second addresses the process of manufacturing the actual electrical interfaces. Materials, methodologies and characerisation techniques used in both of the lines will be described in Chapter 3.

The results of the technology exploration and discussion will be addressed in Chapter 4, where the main reason for choosing electrodes as a neural interface component will also be presented. The corrugated electrode manufacturing process itself required its own optimisation logic and decision-making procedures based on outcomes. Chapter 5 highlights the results obtained and the reason behind the final parameters selection. Chapter 6 provides the results obtained for the final devices fabrication, assembly and characterisation, and the analysis of the outcomes.

Finally, general conclusions and recommendations are stated in Chapter 7.

2

Literature Review

The purpose of Chapter 2 is to understand the working principles of electrodes and transistors and their interfaces with the tissue, as well as the necessary specifications for each structure that are related to their application as neural interfaces. The properties of graphene, different configurations, its synthesis and characterisation techniques, as well as and promising state-of-the-art technologies based on this material are also addressed in this chapter.

2.1. Neural Interfaces for Recording and Stimulation

Neural interfaces are physical means of exchanging information with neurons, which typically consist of an array of electrodes or transistors. In this section, a comprehensive definition for each structure is given, and the required performance parameters and characterisation methods commonly used are documented. Additionally, examples of possible topography modifications that may enhance cell adhesion and increase the effective surface area of the interfaces are studied.

2.1.1. Electrodes for Neural Applications

An electrode is a passive structure consisting of a conductive material that allows the exchange of electrical signals with the medium. When applied to a biological tissue, they can be used as a two-way communication link, allowing to record electrical events and introduce stimulation signals. Since the electrode interacts with the electrolytes in the tissue, the interaction is mediated by the electrode-electrolyte interface, at which faradic and non-faradic reactions can occur [43]. During faradic processes, the reaction generates a direct transfer of charge, as can be interpreted from Figure 2.1.a. Non-faradic reactions are conversely due to the accumulation of ionic charges on the electrode surface, generating a double-layer capacitance (see Figure 2.1.b). Both reactions can occur at the same interface, depending on the electrode material and the electrolyte [43].

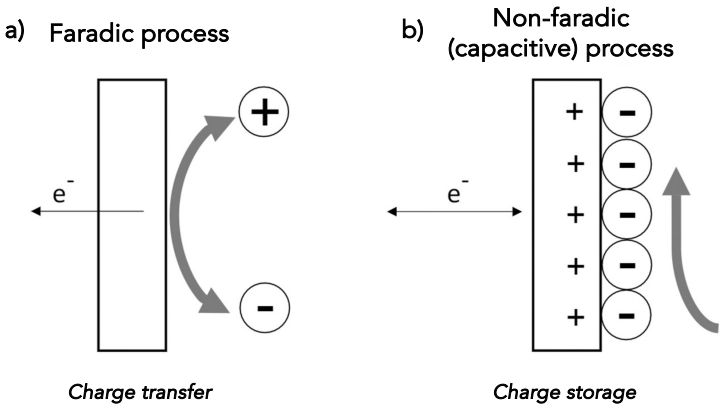

Figure 2.1: Schematic representation of a) Faradic process, b) Non-faradic process. Adapted from [43].

The single electrode-electrolyte interface can be modeled using basic circuit elements, such as resistances (R), impedances (Z), capacitances (C) and voltage sources (E). A half-cell potential, E, is an intrinsic association of every electrode immersed in an electrolyte. The intrinsic resistance of the electrode, as well as of the interface itself with the tissue, can be represented as R_u. The electrode-electrolyte interface model must take into account both faradic and non-faradic leakage reactions: the resistance associated with the charge transfer resistance is represented as R_{ct}, while the double layer is represented by a capacitor C_{dl}. Finally, an impedance related to diffusion phenomena that can affect the ionic transport is represented as Z_W, called Warburg impedance. [44]. Typically, to record or introduce a signal into a biological system a two-electrode setup is required. Figure 2.2 shows the equivalent circuit of a two-electrode-electrolyte interface configuration, which considers E_b as biological voltage source and the generic subject impedance Z_s [44].

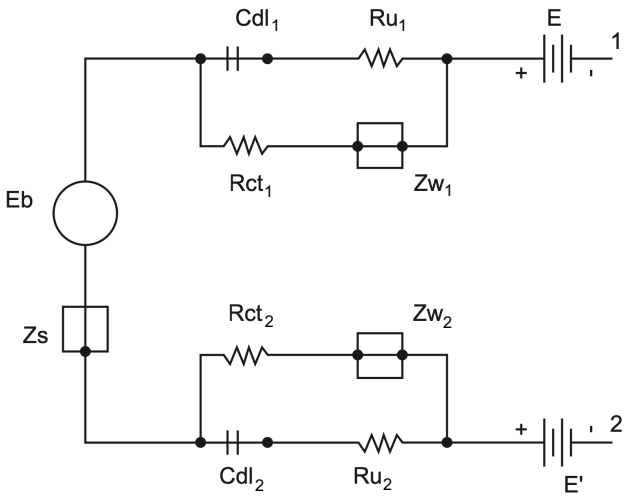

Figure 2.2: Equivalent circuit for a two electrode-tissue interface interacting with a biological system [44].

The electrode material as well as its geometry directly influence R_u and C_{dl} values. Therefore, the application has to be conscientiously considered during the material and design selection process. For recording, electrodes must be characterised by a low impedance, usually ranging between 1 MΩ and 50 kΩ at 1 kHz. This is necessary to have a convenient SNR and a faster response time, as well as better coupling to amplifiers [11]. In order to obtain signals originating from a single neuron, it is necessary to minimise the electrode area, which at the same time increases its impedance and reduces the SNR, so a trade-off is necessary. Regarding electrodes for stimulation, an ionic current is applied between two electrodes, where one of the electrodes is in close contact with the tissue. The stimulation electrode must withstand large enough charge injections to evoke a response in the tissue. At the same time, the charge injection must be limited so as not to generate irreversible reactions that could damage the tissue. The surface topography and shape of the electrode play a crucial role in fine-tuning the impedance and charge injection capacity [44, 45].

An accurate characterisation is crucial to ensure that the electrodes meet the characteristics described above. The electrochemical characterisation of neural interface eletrodes can be performed by means of a three electrode setup, which consists of the reference electrode (RE), the working electrode to be characterised (WE) and the counter electrode (CE). Typically, electrochemical impedance spectroscopy (EIS), cyclic voltametry (CV) and voltage transient (VT) tests are used to measure the impedance of the electrode, the charge storage capacity (CSC) and the charge injection capacity (CIC) of the electrode, respectively.

Electrochemical Impedance Spectroscopy

An EIS procedure implies applying a low-amplitude voltage or current between the WE and the CE and measuring the response of the system (in current or voltage, respectively) over a range of frequencies. Usually, sinusoidal signals typically ranging from 0.1 Hz to 100 kHz are employed. As an example, in case of applying a voltage, the impedance of the electrode-electrolyte system is calculated after

measuring the current, having also the information about the phase shift of the output signal with respect to the input signal [46]. The impedance can be represented as a combination of two components, as:

$$Z = R + jX \tag{2.1}$$

where R is the real part and X is the imaginary part.

Figure 2.3 shows the phasor diagrams and the sinusoidal signals of v(t), an applied voltage, and i(t), the output signal. The response of a pure resistive system is represented in Figure 2.3.a, where the output signal is in phase with the input one, being φ = 0. The impedance is considered pure real, and is represented by R. On the other hand, a pure capacitive system has a response shift caused by the charge stored in the capacitor. Therefore, this type of system is represented only by the imaginary part X [46].

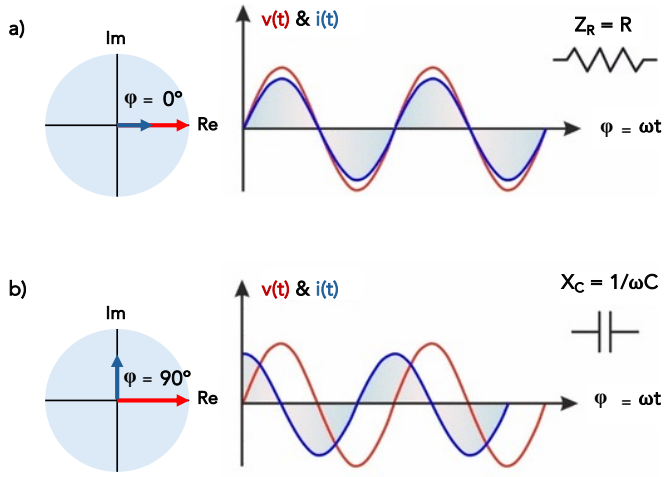

Figure 2.3: Phasor diagrams and sinusoidal signals for an applied voltage v(t) and the current response i(t) for a a) pure resistive system, and b) pure capacitive system. Adapted from [46].

Considering the electrode-tissue interface equivalent circuit, the system can be represented by a series of resistors and capacitors. Therefore, the phasors obtained as a result of EIS measurements will be in the range between 0° and 90°, although values up to 130° are possible depending on the circuit design and the influence of possible non-capacitive behaviour. The total magnitude of the impedance can be represented as $|Z| = \sqrt{R^2 + X^2}$, and usually is represented using the logaritmic values of both frequencies and impedance values. By obtaining $|Z|$ and the phasor values, information can be extracted about which behaviour dominates in a system (capacitive or resistive) given a particular frequency, and also how much resistance it opposes to the flow of electrons for particular sinusoidal signals [46].

Cyclic Voltammetry

A CV measurement implies applying a linear, ramped potential to the electrode over time. After reaching a specific potential value, the potential sweep is reversed, subjecting the electrode to the same ramped potential but in the opposite direction, as can be seen in Figure 2.4.a [47]. The water window, or range between oxidation and reduction potentials, is typically used as voltage range for performing CV tests. Representations of a cyclic voltammograms, which are I vs V, show usually an hysteresis behaviour as a consequence of the electrochemical processes succeeding at the WE, that generates charge transfer and capacitive charging [48]. The currents generated are representative of the reactions occurring in the WE as a result of applying the ramped voltages. The information from this test is therefore relevant for characterising the stimulation electrodes, as the hysteresis cycle obtained can be used to calculate the charge storage capacity (CSC) of the electrode. This parameter depends on the charge stored in reversible processes occurring during stimulation [48]. Figure 2.4.b shows an example CV of AIROF, in which the CSC is calculated using the integral of the cathodic current [11]. CSC can be calculated as:

$$CSC = \frac{\int_{V_{min}}^{V_{max}} I(V)dV}{A} \tag{2.2}$$

where V_{min} and V_{max} are defined by the water window, $I(V)$ is the cathodic current and A is the electrode area.

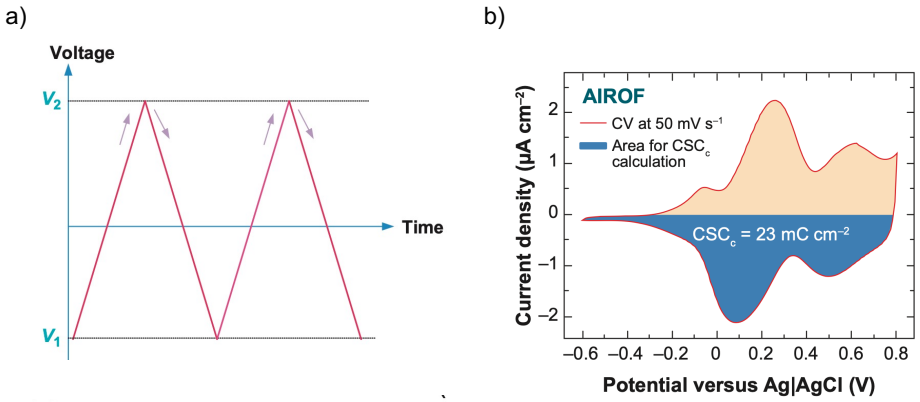

Figure 2.4: a) Cyclic voltammetry waveform, where V1 and V2 are typically the redjuction and oxidation potential, respectively [47]. b) CSC calculated from the cathodic current of the AIROF CV [11].

Voltage Transient

Considering a stimulation pulse, VT is used to calculate the maximum charge injection capacity of the electrode. This is known as the charge injection capacity (CIC) of the electrode. VT measures the polarisation of the electrode when a two-phase current is applied. The biphasic shape of the impulse is considered to maintain the net charge transfer as zero [47]. The maximum negative polarization E_{mc} and maximum positive polarization E_{ma} are considered as the limit potentials which, if transferred, can generate damage to the tissue and electrode. An initial voltage drop is represented at the start of the cathodic stimulus, V_a, due to the resistive components of the circuit. This is compensated by leaving a few ms between the cathodic and anodic current [11]. The CIC can be calculated as:

$$CIC = \frac{I_{max} t_c}{Area} \tag{2.3}$$

where I_{max} is the maximum current that can be applied within wafer window values for E_{mc} and E_{ma}, and t_c is the pulse duration.

2.1.2. Transistors for Neural Applications

A transistor is an active device that can amplify and switch an electrical signal. Depending on the structure of the transistor, it can generate an amplified current from a certain smaller current, or it can create a current by applying a certain voltage. While the first type is known as a bipolar junction transistor (BJT), the second is referred as field effect transistor (FET). Both are based on the combination of p-type materials, where the majority of charge carriers are holes, and n-type materials, which have electrons as the majority of charge carriers [49].

Figure 2.5 shows a simple, schematic representation of how a BJT and a metal oxide semiconductor FET (MOSFET) operates. Both structures are essentially composed by three main terminals or electrodes. In a BJT structure, a small current is applied between the emitter and the base, as can be seen in Figure 2.5.a. The electrons flow from the n-type (emitter, E) to the narrow, low doped p-type (base, B), being this current I_B (note that, for convention, the current is represented in the opposite direction to the flow of electrons). As the p-type region (B) has low concentration of holes, all of them recombine with electrons, leaving the material charged negatively. Electrons are now available at the p-type, so if a power source is applied between the collector (C) and the emitter (E) considering the positive terminal connected to the C, electrons will be able to flow from E to C, creating what is known as the collector current, I_C [49]. On the other hand, a MOSFET (and FETs in general) uses a voltage to regulate a current. The structure of a MOSFET as an example of a FET has been selected for ease of representation. Figure 2.5.b shows the schematic operation of an n-type channel MOSFET, where a voltage V_{GS} is applied between the gate (G) and the source (S). Since S and the substrate are connected, the voltage between G and S is the same as the voltage between G and the p-type substrate.

When enough voltage is applied, the presence of an insulator between G and the p-type substrate creates the accumulation of the available negative charges of the p-type substrate close to the gate, but the insulator prevents the electrons to flow through the gate. In this scenario, the depletion region in the areas close to the gate between the p-type and n-type substrates decreases and electrons can flow through the created channel, provided that a sufficient voltage V_{DS} is also applied between drain and source [49].

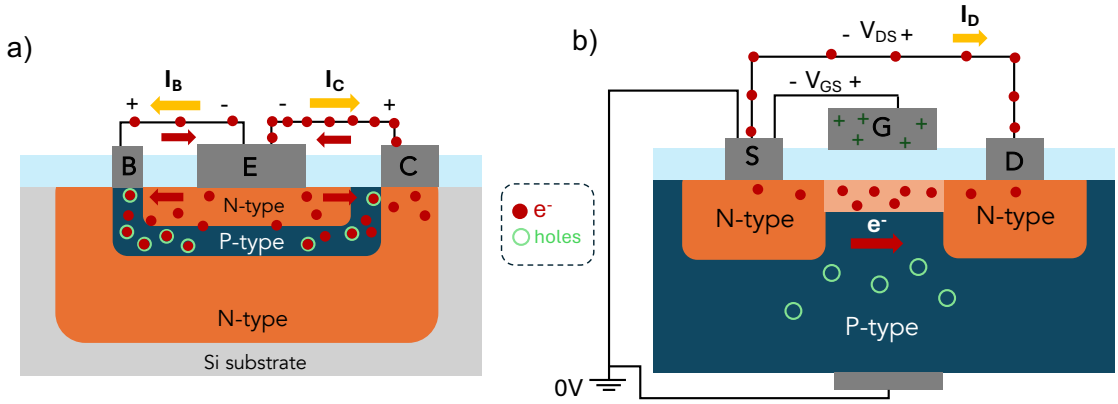

Figure 2.5: a) Schematic representation of BJT operation. B is the base, a narrow, low doped p-type region. As can be seen, once a current is applied between the emitter (E) and the base, the major part of the holes in B are recombined with electrons. C is the collector, where electrons are collected and the current is amplified. I_B controls I_C. b) Schematic representation of MOSFET operation. S is the source, which provides electrons. G is the gate, where the control voltage is applied. D is the drain, which collects the electrons. V_{GS} controls I_D for a specific V_{DS}.

Due to differences in their structure, BJTs and FETs have different characteristics. As mentioned, one of the main differences is that BJTs are current controlled while FETs are voltage controlled. This results in higher energy consumption in BJTs than in FETs because it requires a constant current application. In addition, FETs provide higher input impedance (so they draw minimal current from the input signal source) and lower noise levels [50]. All these features support the use of FETs structures (and variatons) over BJTs for the recording of biological signals, as they favour both a high SNR recording and a safer interface with the tissue.

The next question to address is how to properly characterise a transistor for neural interface applications. In general, the neural activity generates a variation in the gate-source voltage V_{GS}, which is translated into a change in I_D. The sensitivity of the channel in response to an electric field can be evaluated by means of several parameters, such as transconductance g_m, carrier mobility, threshold voltage and ON/OFF ratio [51]. These parameters can be extracted by means of the characteristic curves of the transistors, which are representations of I_D vs V_{DS}, and I_D vs V_{GS}. Figure 2.6 shows an example of both characteristic transistor curves of an n-type MOSFET. Considering the left curve, I_D vs V_{GS}, the transconductance g_m can be calculated from the linear region as $g_m = \frac{dI_D}{dV_{GS}}$. High values of g_m mean high sensitivities, which is a required feature for neural recording interfaces. The threshold voltage, V_{th}, can also be extracted from this curve as the minimum V_{GS} needed to create the channel. Furthermore, the ON/OFF ratio can be extracted considering the ratio between a current at high V_{GS} values vs the current at low V_{GS} values. Taking into account the right curve, I_D vs V_{DS}, the carrier mobility value can also be extracted, calculated as a function of V_{GS}, V_{th}, V_{DS} and the dimensions of the transistor.

Considering the application of transistors for neural interfaces, the values of the mentioned parameters documented in the literature are variable and depend on the type of structure and materials used. For the transconductance g_m, values raging from 10 µS to 180 mS have been obtained taking into account silicon-based, organic (OCTS and OECTS, for instance) and carbon-based transistors [51, 52, 53]. The carrier mobility is also highly dependent on the material used, and depending on the way the transistor operates, the values can vary from 1 to 1000 cm²/V-s [51, 54, 55, 56]. Additionally, SNR in the between 5 dB and 30 dB at the frequencies of interest should be provided [55, 57].

As signal recording interfaces, transistors offer some advantages over electrodes. By reducing the size of the electrodes (necessary to increase the spatial resolution) their impedance increases, which

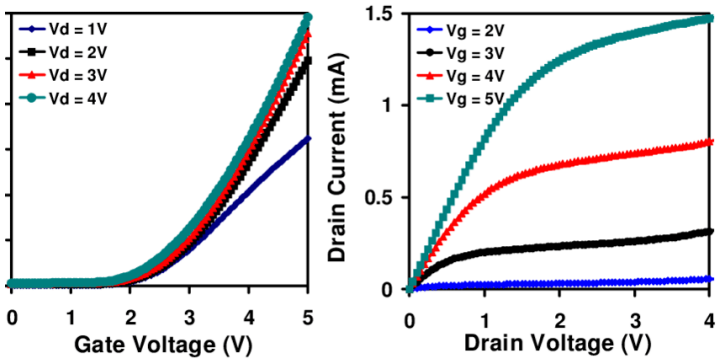

Figure 2.6: Left: I_D vs V_{GS}. Right: I_D vs V_{DS}. Curves extracted for a MOSFET at different drain and gate voltages, respectively [58].

reduces the SNR due to thermal noise generation. Transistors use *in situ* amplification of the signal, therefore when comparing electrodes and transistors of the same size, transistors provide better SNR [51, 12]. However, transistors are limited to recording applications, as they are specially designed to perform with small currents and provide a low CIC. Furthermore, in the case of FETs, the current is unidirectional, therefore they are not optimised for two-phase current generation [51, 12].

2.1.3. The Role of Surface Topography

Ensuring that the above parameters satisfy the required performance criteria is essential to obtain reliable neural interfaces. The capability of the devices not only depends on the materials used, but also on the interface created between the recording/stimulation structure and the electrolyte (or tissue), making their surface properties critically important. Studies show that surface modifications can improve both the electrochemical performance of the electrodes and the interaction and adhesion of the cells [59]. Research efforts on surface architecture are mainly focused on enhancing electrodes topography rather than transistors surface, since the intrinsic design of transistors is already complex and their optimization focuses more on modifying their component configurations instead of their surfaces. Therefore, this subsection highlights strategies to improve the electrode performance and the electrode-tissue interface through topography modifications.

Electrode performance enhanced by surface modifications

As mentioned, reducing electrode surface is a requirement for improving the spatial resolution. However this leads to an increase in the electrode impedance, which can lead to a reduction in the SNR and the increase of harmful events for the tissue. Reducing the area while maintaining electrical performance of electrodes is possible through surface modifications and the development of new concepts such as 3D electrodes.

Studies has shown electrode performance optimization by modifying the surface morphology. Li et. al [60] showed an increase in the surface area of the electrode by creating a series of micro/nano structures, patterned using laser irradiation. Comparing the electrodes with a higher groove microstructures density with the smooth surface electrodes, the first ones showed a significant reduction of impedance along with the increase of CSC, obtaining CSC values of 128.2 mC/cm^2 for the electrodes with the highest density of patterned microstructures and a CSC of 4.6 mC/cm2^2 for the smooth ones. Other studies show how grooving the surface of conductive polymers such as PEDOT using as coating of metal electrodes can also improve electrical characteristics of electrodes [61]. Chung et al [62] showed a similar approach, increasing the surface roughness of gold electrodes using tetrafluoromethane (CF4) plasma. Not only grooved structures or the increment in random roughness has proven to increase impedance. Other structures such as mushrooms-like shapes (see Figure 2.7.a) have also been investigated as surface increasment of electrodes, proving to be effective in reducing impedance and increasing SNR [63, 64]. Other studies show how considering the electrode itself as a three-dimensional structure decreases its impedance by increasing the active surface area [65, 66]. In addition, coatings with Pt NPs have also proved to increase the surface area of the electrode, reducing therefore the impedance and increasing the CSC [67, 42].

Electrode-cell interaction enhanced by topography modifications

A successful performance of the neural interface is directly dependent on its interaction with the tissue. However, the number of neurons in the vicinity of the neural interface tends to decrease after the interface implantation due to inflammatory response. Modifications on the electrode surface have proven to enhance neural guidance and neural homeostasis [59]. Additionally, the creation of continuous patterns at the surface of the electrodes can potentially reduce the immune response [68]. Different structures and sizes, patterned on materials used for neural electrodes, and their interaction with neurons are shown in the literature. To create the patterns, different litographic methods have been reported, being UV litography the most commonly used [69].

One of the most researched topographies is the anisotropic continous geometry of alternating grooves. In general, studies have used depth sizes ranging from 0.1 to 60 µm [70, 71]. For instance, an studied conduected on polypyrrole, a conductive polymer, showed a succesfully micropatterned grooves (or microchannels) structure (see Figure 2.7.b and 2.7.c) [72]. This surface configuration allowed neurons to define and polarize their axons more rapidly in comparison to a non-patterned substrate, implying a better stabilization of the neuron to the interface. Considering other type of patterns, Dowell-Mesfin et al [73] showed how topographycally modified surfaces using square micropilars can affect the orientation and growth of neurons (see Figures 2.7.d, 2.7.e, 2.7.f and 2.7.g), indicating that topographic features can contribute to the organization of neurons and growth of axons. This can be directly applied to the topography of neural interfaces, helping to improve the electrode-cell interaction. Lunghi et al. [74] presented a flexible neural interface based on PEDOT:PSS and gold micropillar arrays (see Figure 2.7.h). This structure exhibits hydrophobicity, which is beneficial for cell adhesion. In addition, the cell-topography interaction also showed an effect on the directionality of the neurons.

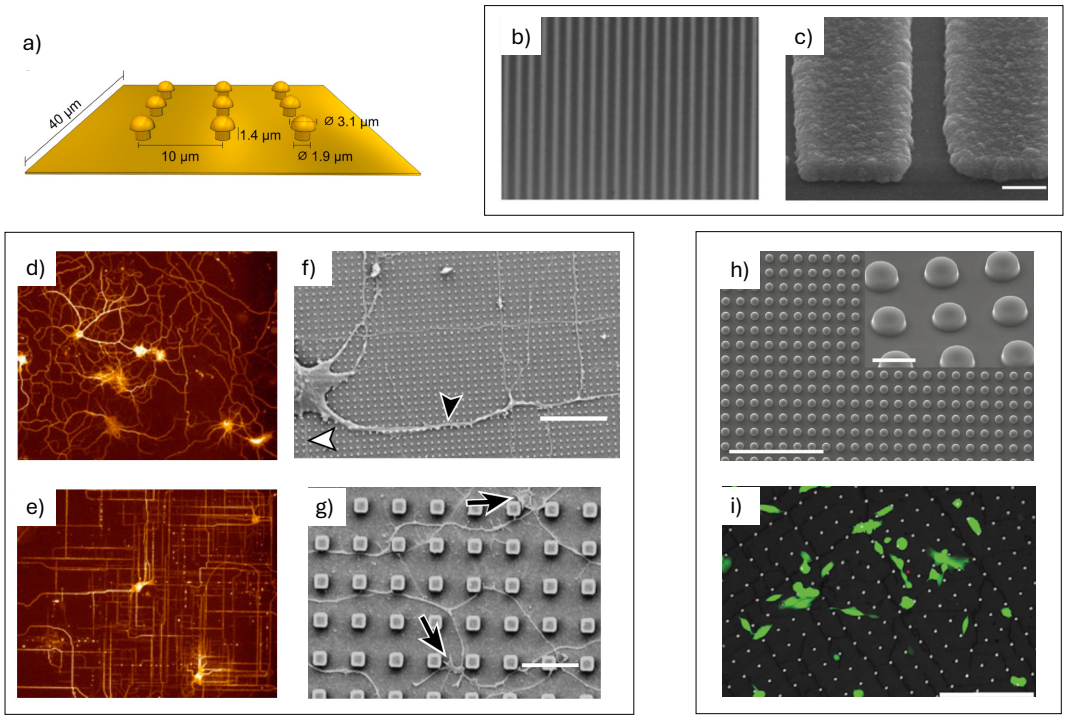

Figure 2.7: Different patterned surface topographies. a) Schematic representation of mushroom-like shapes patterned for enhacing both electrode electrical performance and neural adhesion [63]. b) & c): SEM images of anisotropic continous geometry of alternating grooves. Size: 1µm wide, 900 nm thick. Adapted from [72]. d) & e): Fluorescence images of neurons in a smooth surface (d) and in a square-shape pilars pattern (width: 2µm, gap size: 1.5µm, depth: 1µm). f) SEM images of a neuron on squared-shape pilars (width: 2µm, gap size: 4.5µm, depth: 1µm). g) Zoom of image in f). Adapted from [73]. h) SEM image of PEDOT:PSS and gold micropillar arrays (diameter size: 8.3 µm, depth: 3µm; pitch: 15µm) i) Fluorescence image of neurons in PEDOT:PSS micropillar arrays. Adapted from [74].

2.2. Graphene: a Potential Material for Neural Applications

2.2.1. Properties and Configurations

A single layer of graphene can be considered as a two dimensional crystal of carbon atoms arranged in a honeycomb shape. Each carbon atom creates three covalent σ bonds with the adjacent atoms as a result of the sp^2 hybridisation, which gives rise to the hexagonal and planar arrangement of the material. This configuration generates an unpaired electron in the p orbital, responsible for the π and π* energy bands, related to the valence and the conduction bands of the graphene respectively, which intersect [75, 76]. As a consequence of this intersection, graphene has a zero band gap, like metals. One can consider graphene as a semi-metallic material [77]. This configuration endows single layer graphene with exceptional electrical properties, such as an ultrahigh mobility of $2x10^5$ $cm^2V^{-1}s^{-1}$, a high conductivity of 10^6 Sm^{-1} and a sheet resistance of 31 Ω [78]. The σ bond, on the other hand, is responsible for the mechanical properties of graphene. Pure single layer graphene is one of the strongest materials known, achiving a tensile strength of 130 GPa and a intrinsic strength of 42 Nm^{-1} of the single membrane. Additionally, the Young's modulus of graphene is 1.0 TPa, so it is considered to be an elastic material that can withstand high loads before permanently deforming and fracturing [79]. With a light absorbance of 2.3% single layer graphene is almost transparent to the human eye, allowing 97.7% of the light to pass through the 2D structure. All the above mentioned properties are strongly dependent on the sheet defects and the number of graphene layers [80].

Graphene is a very versatile material that can be used in different configurations depending on its application. The above mentioned properties apply for a single layer graphene (SLG), but other configurations considering a higher amount of layers such as few-layer graphene (FLG; up to 10 layers) and multilayer graphene (MLG) also offer interesting features [81]. Compared to SLG, MLG offers a higher electrochemical capacitance and reduced sheet resistance as a result of interlayer interactions, which makes it an interesting material in stimulation modalities as it has more CSC than SLG. However, the significant reduction in the optical transmittance with the increase of the number of layers should be also considered [42]. In addition to the number of layers, the arrangement of the layers also plays an important role in the properties of graphene. Figure 2.8 shows the possible stacking sequences of two graphene layers. As can be seen, graphene layers can be: exactly superimposed (AA stacking, Figure 2.8.a); superimposed while their lattices being shifted in a way that a third layer is exactly superimposed to the first layer (ABA, Bernal stacking, Figure 2.8.b); superimposed and shifted over a distance equal to one C-C bond (ABC); turbostratic, superimposed while being randomly rotated (Figure 2.8.c) [82]. AB stacking is more energetically stable than AA and ABC arrangements. However, although being energetically metastable, the most frequent stacking is the turbostratic configuration, with graphene created by CVD usually being of this type [83]. As a result of a lower layer interaction, this turbostratic graphene has exotic electrical properties [84].

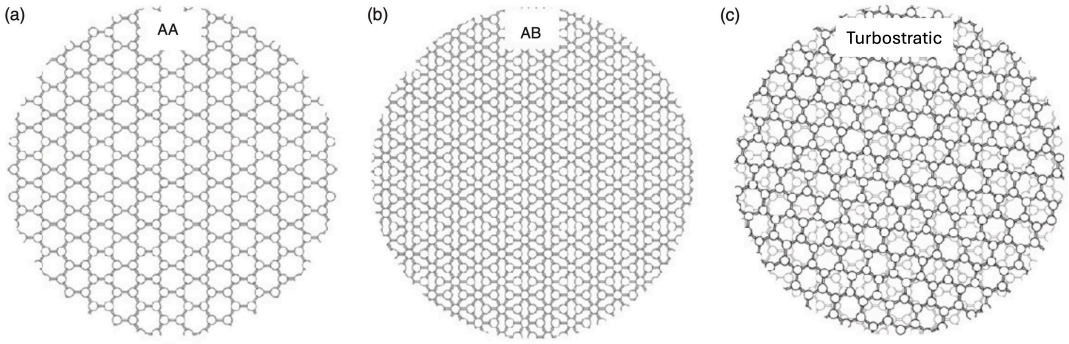

Figure 2.8: Stacking configurations of two graphene layers. a) AA stacking, b) AB (Bernal) stacking, c) Turbostratic graphene, for a 13º rotation angle. Adapted from [82].

Alternatively to the planar sheet configuration, corrugated graphene exhibits regular or irregular undulations and therefore structures outside the 2D plane. These sheet ripples, that can be nano and micrometric, can generate significant changes in mechanical and electrical properties of graphene. Ding et al. [85] showed how micrometric undulations allowed graphene to maintain its electrical properties under mechanical stress. In this study, a Cu substrate with micrometric ripples was used to grow

CDV graphene, which was succesfully transferred to a PDMS substrate (see Figure 2.9.a). Plantey et al. [86] presented another approach, transferring the graphene to a nanometric corrugated SiO_2 substrate (see Figure 2.9.b). This study supported also the ability to control strain through substrate design. The improvement in mechanical properties offered by corrugated graphene can benefit the implantation process of neural interfaces. Additionaly, electron mobility along the corrugation has been proven to be slightly larger than the mobility normal to the corrugation [87]. This anisotropy can also be taken into account for device design.

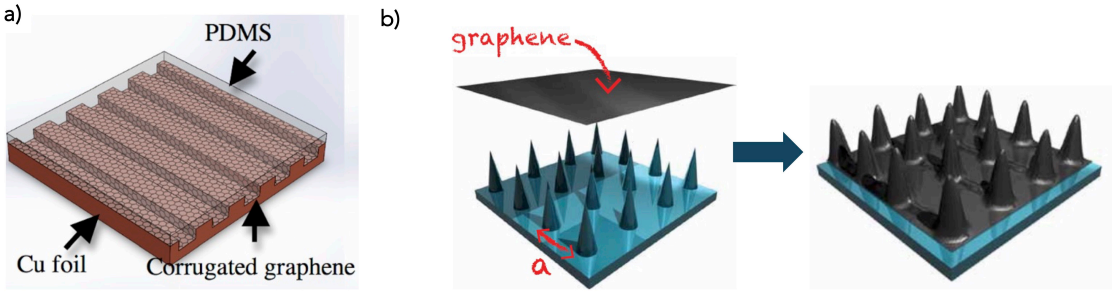

Figure 2.9: Corrugated graphene configurations. a) Growth of graphene on corrugated Cu, being transferred to a PDMS substrate. Adapted from [85]. b) Graphene transfer to a SiO_2 corrugated pattern. Adapted from [86].

2.2.2. Synthesis of Graphene

The production method of graphene is a relevant aspect to consider, as it directly affects the quality of the material and, consequently, its properties. Two different approaches can be considered for graphene synthess: bottom-up generation techniques are based on the generation of graphene from carbon compounds, while the top-down methodology usually involves the exfoliation of graphite [75]. As a top-down approach, mechanical exfoliation of graphene from graphite can be performed using the Scotch tape method. However, this methodology does not allow to control the number of layers, making it non-scalable [88]. Another top-down method is Liquid Phase Exfoliation (LPE), which main limitation is associated with a low uniformity of the resulting graphene together with the challenge of removing the solvent [89].

The most widely used method for graphene synthesis is chemical vapour deposition (CVD), as mentioned in Chapter 1. This bottom-up approach allows the synthesis of graphene in a controlled manner using a catalytic agent, usually Cu or Ni [90]. CVD graphene growth depends directly on the solubility of the carbon atoms in the material, and is a well-understood process for Cu and Ni. Considering Cu, graphene growth is a ”surface self-limiting” process due to the low solubility on Cu (7.4 at.ppm at 1020º), which tends to produce monolayer graphene. In the case of Ni, a segregation/precipitation process generates multilayer graphene (or thick graphene), resulting from the high solubility of cabron in Ni (9000 at.ppm at 900ºC) [91]. Graphene growth mechanism is not as well studied for other metals such as molybdenum (Mo), whose solubility of carbon atoms is from 700 ppm at 1500 ºC. In the latter case, a combination of both growth processes may occur, depending on both substrate thickness and process temperature [91].

Not only the synthesis but also the post processing of graphene is crucial to ensure that its properties are maintained. As mentioned in Chapter 1, the most common post processing procedure is graphene transfer from the catalyst to the substrate target. Material-assisted transfer processes are the most commonly used, although, as mentioned in the previous chapter, they tend to leave residues [40]. To improve the transfer process, some methods of sacrificial material-assisted transfer include the application of heat-sensitive materials, which can be peeled off when heat is applied, such as thermal sensitive tapes. This process is, however, not suitable if the substrate is rigid, which is the case of silicon wafers [92]. Another approach is the use of metals as a transfer material, which tends to leave less residues than polymeric materials after the metal is etched [93]. However, the counter side of this method is the cost-effectiveness in terms of production cost-effectiveness. Other techniques include transfer using solid thin films and liquid phase organic solvents. Yet, these methods have drawbacks: solid films lack flexibility, while liquids can negatively impact the final substrate [94]. In a completely different line of transfer, there are transfer processes that do not consider a supporting material or layer,

which usually make use of the surface tension of a liquid, avoiding having polymeric or metal residues. Nevertheless, the absence of support makes graphene more susceptible to cracking [94].

All these disadvantages of the transfer process divert the focus to developing transfer-free processes, in which graphene growth is produced in a catalyst deposited in the substrate of interest. Transfer-free processes on Cu have been studied and successfully performed [95, 96]. Nevertheless, the use of copper directly on silicon wafers is not ideal due to several factors, including the low melting point of Cu, difference in thermal expansion coefficients between Cu and Si which can generate stresses in the silicon, and the limited compatibility with standard semiconductor processing, as copper diffuses easily into the silicon, generating unwanted doping [97, 98]. For this reason, other metals such as molybdenum have begun to gain prominence, as it is compatible with CMOS technology and has an expansion coefficient more similar to Si and a higher melting point than Cu and Ni [41]. Ricardella et al. [99] shows a reliable way of fabricating transfer-free MLG using a Mo catalyst. In this work, Mo is etched away after graphene growth using a hydrogen peroxide solution, allowing the graphene to be deposited on the SiO_2 substrate. For this transition metal, graphene growth mechanism appears to be mediated by its carbide, Mo_2C, in situ created during the CVD process. Although the main growth is mediated by molybdenum carbide, the catalyst/substrate interface might also play a role. A model of MLG growth mechanism mediated by a thin Mo film (70 nm) is proposed by Kizir et al. [100], where the formation of the carbide and the effect of the Mo_2C/SiO_2 are emphasized, as can be seen in Figure 2.10. In the proposed theory, graphene growth could be mediated by 4 steps. Step 1 involves the formation of radicals, which is mediated by the interaction of the carbon precursor gas (CH4) and the catalyst, Mo. During step 2, carbon and hydrogen species diffuse through the metal carbide. Hydrogen atoms create activation O-H sites on the SiO_2. Some CH_x radicals will be chemically adsorbed by the O-H activation sites on the SiO_2, which creates graphene nucleation on SiO_2 substrates (step 3). Step 4 considers the growth of multilayer graphene, which is mainly mediated by the Mo2C, but can be also affected by the Mo_2C/SiO_2 interface. Although the growth mechanism in this specific scenario seems to be well reflected, this depends on other factors such as temperature, exposure time to the carbon precursor, the thickness of the catalyst, and the substrate and its characteristics [100]. Even though its mechanism is not fully understood, transfer-free MLG on thin Mo has already been successfully applied for neural interfaces applications [42, 101].

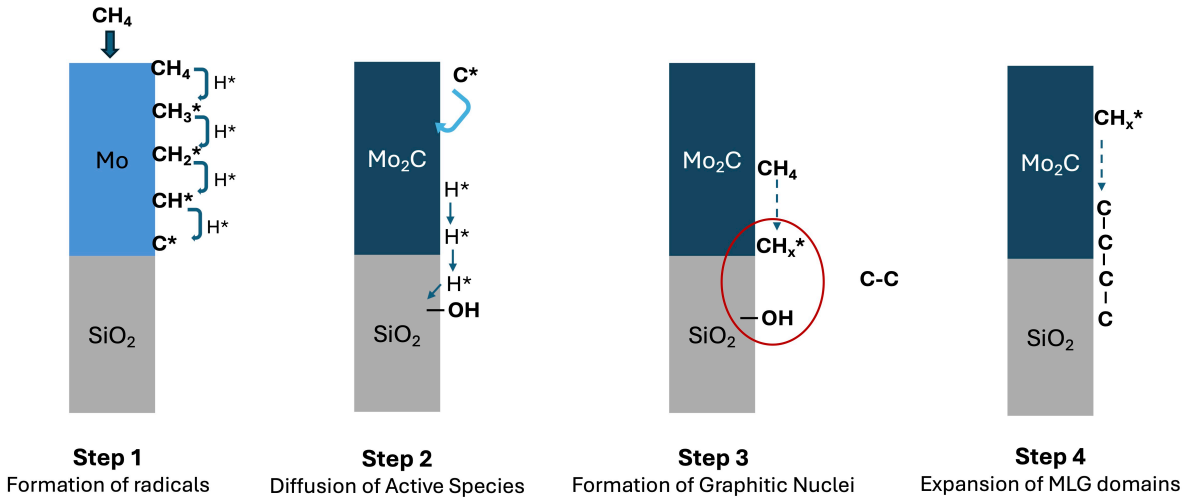

Figure 2.10: Schematic representation of the proposed MLG growth mediated by the Mo_2C and SiO_2 interface. Adapted from [100].

2.2.3. Graphene Characterisation

Raman Spectroscopy

Raman spectroscopy is a non-destructive technique which is widely used for the characterisation of 2D materials. During a Raman measurement, a sample is exposed to a monochromatic beam at a certain wavelength λ_i and energy E_0. The photons of the beam interacts with the molecules composing the material, which results in two different types of scattering [102]. Most photons present elastic scattering,

meaning that the photon is scattered with an energy equal to the incidence energy. This is known as Rayleigh scattering, where the energy of the scattered photon is $E_{Rayleigh} = E_0$. On the other hand, a small part of the photons will present a higher or lower energy, which is directly related to the molecular vibrational modes of the sample. This is known as Raman scattering, where the energy of the scattered photon is $E_{Raman} = E_0 + E_{vm}$, being E_{vm} dependent on the frequency associated to vibrational motions of molecular bonds [102]. The Raman spectrum is represented as a shift of the inverse of the input wavelength with respect to the output wavelength of the photon. This shift is kwown as wavenumber, and can be calulated as:

$$v = \left(\frac{1}{\lambda_0} - \frac{1}{\lambda_{Scattered}}\right) \times 10^7 \tag{2.4}$$

where λ_0 is the frequency of the incident photon, $\lambda_{Scattered}$ is the frequency of the scattered Raman photon [102].

Raman spectroscopy offers a *fingerprint* of a chemical specimen, meaning that a particular material and configuration has its unique Raman spectrum. Figure 2.11 shows the raman spectrum of SLG and MLG. As can be distinguish, graphene presents three main Raman peaks: D, at ~ 1350 cm^{-1}; G, at ~ 1582 cm^{-1}; and 2D, at ~ 2700 cm^{-1} [103]. The D band is product of breathing modes of the sp^2 carbon atoms, and it is typically associated with graphene quality, with a strong D peak usually indicating defects in the graphene. G band is generated by the in-plane vibrational modes of the sp^2 carbon atoms. Lastly, the D band originates from a two phonon double resonance process [104]. Usually, the ratios I_D/I_G and I_{2D}/I_G give information about the number of layers and the graphene quality, respectively. High I_D/I_G ratios imply higher number of defects, while a I_{2D}/I_G higher than 1 is usually an indicator of SLG [105]. Overall, Raman spectroscopy is a powerful tool to characterise graphene and graphene based compounds.

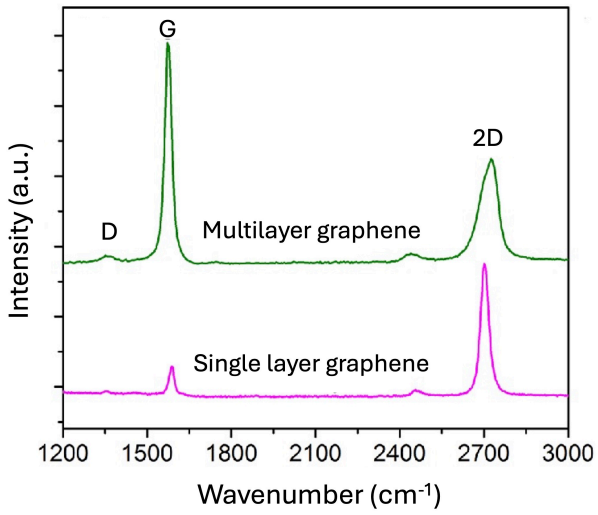

Figure 2.11: Raman spectrum of FLG and MLG. Adapted from [106].

Optical Transmittance

Optical transmittance (OT) is a technique used to determine the fraction of incident light that is successfully transmitted through a sample. During a OT measurement, the transmittance values are determined over a specific range of wavelengths, typically being between 300 nm and 1200 nm. Typically, the OT value at 550 nm is used to characterise graphene, being this value ~ 97,7% for SLG [107]. Zhu et al. [108] proposed a simple formula to determine the number of graphene layers using the transmittance value:

$$T = (1 + 1.13\pi\alpha N/2)^{-2} \tag{2.5}$$

where α is the fine-structure constant, which value is $\frac{1}{137}$ and N is the number of graphene layers. Usually, the graphene sample to be characterised is transferred to a transparent substrate, such as glass, making it important to properly extract the influence of the substrate after the measurements to

obtain a reliable OT value [42].

Atomic Force microscopy

Atomic force microscopy (AFM) is a high resolution characterization technique used to obtain high resolution images from a specific surface. The principle of operation is based on measuring the forces created between the tip of a cantilever and the surface of the sample and record the changes in the reflection of a laser beam. Figure 2.12 shows a representation of the main AFM components. The cantilever tip interacts with the sample by electrostatic, van der Waals or mechanical forces, which generates its oscillation. A laser beam is projected on the cantilever, which reflects to a photodetector. Variations in topography translates in cantilever oscillations, which result on a shift in the laser reflection. Finally, a feedback loop is necessary to adjust the vertical position of the cantilever [109].

In practice, there are three main modes of operation. In contact mode, the tip remains in physical contact with the surface of the sample. Considering the tapping mode, the cantilever tip intermittently contacts the surface, which reduces the lateral forces. Lastly, in non-contact mode the oscillations on the cantilever are consequence of the attractive forces between the tip and the sample surface [110]. Considering graphene characterization, tapping mode is usually preferred due to the reduced surface damage in comparison to contact mode, and enhanced imaging resolution than non-contact mode [109]. Generally, AFM is used both to measure the surface roughness of graphene and to measure its thickness relative to that of the substrate, the latter being relevant for determining the number of layers. Gupta et al. determined that the height of single-layer graphene (SLG) on a SiO_2 substrate measures $\sim$ 0.7 nm [111], although other reports have measured variations from 0.4 to 1.8 nm [112]. This reflects how sensitive this technique is to noise, which can originate from multiple factors, including the substrate's roughness, as well as the condition of the cantilever and the tip, among other variables [109].

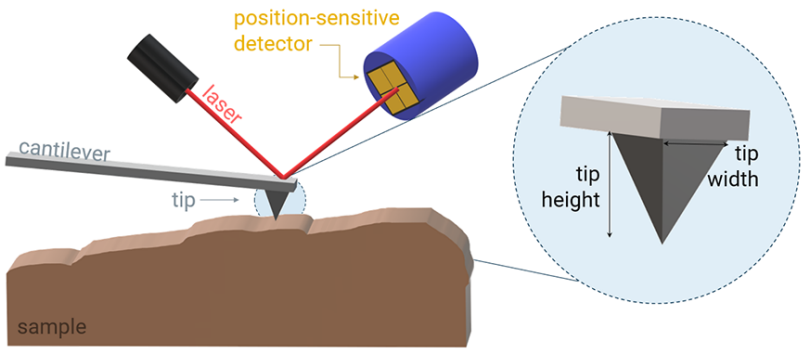

Figure 2.12: Schematic representation of AFM [113]; contact mode.

2.3. State of the Art Graphene-based Neural Interfaces

The properties of graphene mentioned above, as well as its biocompatibility, make it a particularly exotic material for its application in neuroscience. This section presents a review of the state-of-the-art graphene-based components used as neural interfaces. Two main graphene interface configurations are found in the literature: microelectrodes and FETs.

Graphene Electrodes

CVD graphene has been successfully applied in the development of electrode-based devices for neural recording and stimulation. Table 2.1 summarises some of the work in the literature and figures of merit on graphene-based electrodes. To date, most work has used CVD graphene grown on Cu and transferred via PMMA to the substrate of interest [114, 115, 116, 117, 118, 119, 120]. The use of Cu is usually preferred as the creation of graphene can be done in a controllable manner. However, monolayer graphene can limit the application of electrodes to the stimulation mode. Therefore, FLG or MLG is usually preferable for creating electrodes that can be used for recording and stimulation. Consideing Cu as a catalyst, few monolayers of graphene can be transferred, one by one, to the

substrate or, alternatively, Mo can be used as a catalyst, effectively creating good-quality MLG [42]. Considering the materials used to create the devices, Figure 2.13.a shows an schematic representation of a graphene microelectrode array (MEA) material layers. For a flexible, transparent device usually SU-8 or parylene C is used as a substrate for gold tracks and graphene electrodes. SU-8 is the most commonly used encapsulation layer.

In general, graphene electrodes offer good electrical performance allowing for good visibility of the surrounding tissue. All the reported works present area normalized impedance values below 100 kΩ at 1kHz, and optical transmittance values between 80 % and 90 %, allowing devices as the one showed in Figure 2.13.b and 2.13.d to be used in combination with optogenetic techniques. Figure 2.13.c shows a schematic representation of how the microelectrode array could be applied for signal recording after stimulating cells with light. Graphene electrodes also demonstrated effective performance for stimulation, delivering CIC values within safe limits [42, 115, 119]. Overall, although graphene electrodes exhibit higher SNR, and lower CSC and CIC compared to conventional Au and Pt electrodes [11], their performance is commendable for neural recording and stimulation applications. This capability facilitates their effective integration with other techniques, including MRI and other imaging modalities, as well as optogenetics.

Graphene Field Effect Transistors

SLG has been investigated as potential FET channel. The typical graphene transistor configuration is a solution-gated FET (SGFET), where usually a Ag/AgCl electrode modulates the channel current, as can be seen in Figure 2.13.e. In practice, the variations in the potential surrounding of the SGFET is generated by the action potentials of the neurons, which modulates the channel current. The key advantage of a transistor configuration is its ability to achieve a higher SNR compared to an electrode, along with a smaller size that enables higher spatial resolution.

Table 2.2 provides a summary of some of the state-of-the-art GFET and their characteristics. In general, the drain and source are gold electrodes, and the encapsulation is usually made of SU-8 or polyamide, leaving only the graphene channel exposed. Similarly to electrodes, most of the transistors contain transferred CVD Cu-grown graphene [121, 55, 53, 122, 123, 124, 125]. Despite the potential defects introduced as a consequence of the transfer process, which can be more problematic for transistors than for electrodes due to their smaller size, transistors still perform effectively, providing excellent SNR and compact dimensions. Figure 2.13.f shows a microtransistor array (MTA) which proved to be able to accurately record neural signals in vivo [55]. As active components, transistors pose a greater risk for in vivo applications than electrodes due to potential current leakages to the brain. However, this risk can be mitigated by optimizing the device materials and characteristics.

2.4. Relevant Outcomes from the Literature Review

In neural interface design, electrodes serve as passive structures commonly employed for both recording and stimulation, while transistors function as active components primarily used for recording. Transistors typically offer improved SNR and enhanced spatial resolution compared to electrodes. Despite the usefulness of these technologies, spatial resolution remains a significant limitation. To address this challenge, substantial progress has been made in developing transparent neural interfaces. These innovations enable integration with imaging techniques, facilitating multimodal analysis and achieving higher spatial resolution.

Graphene-based technologies have emerged as particularly promising in this area, offering excellent electrochemical performance, flexibility, transparency, and biocompatibility. Although the transfer process introduces defects into the material, it remains the most widely used method for fabricating graphene-based devices. Consequently, a transfer-free approach should be a key strategy for both optimizing the manufacturing process and enhancing device quality. In the pursuit of improving and optimizing graphene-based neural interfaces through transfer-free methods, two main research areas have been identified that remain unexplored.

First, the integration of electrodes and graphene transistors within a single device has not been investigated, not even considering transfer processes. Such a combination could potentially offer both high SNR and improved stimulation performance. However, considering a transfer-free process, this approach would require the simultaneous fabrication of SLG/FLG for transistors and MLG for electrodes, as SLG does not have enough CIC to evoke neuronal response [127]. Understanding how

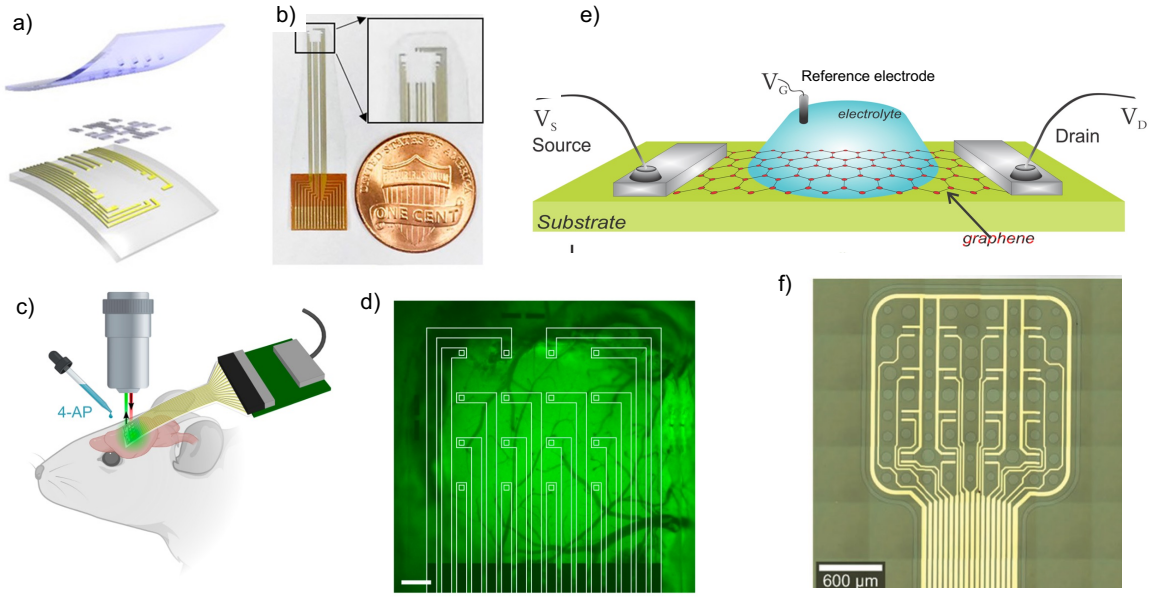

Figure 2.13: State-of-the-art graphene based neural interfaces. a) Schematic representation of the graphene MEA layers. b) Fabricated transparent graphene MEA [116]. c) Graphical illustration of a graphene MEA combined with optogenetic stimulation. d) Fabricated graphene MEA placed over barrel cortex during in vivo testing [120]. e) Schematic representation of a SGFET configuration placed on an electrolyte solution [126]. f) Fabricated transparent graphene MTA [55].

graphene properties are influenced by catalyst (Mo) characteristics variation is therefore essential to determine if SLG/FLG and MLG can be produced on the same substrate.

Second, research has demonstrated that altering the surface topology of graphene and neural electrodes by introducing corrugated surfaces could offer several benefits:

- Enhanced neuron adhesion and/or guidance.
- Increased active surface area, improving the electrochemical properties of the electrode.
- Improved mechanical performance of graphene.

Thus, the creation of graphene electrodes with corrugated surfaces using a transfer-free method becomes an interesting field to explore, as this configuration can provide several improvements. The impact of surface corrugations on graphene growth on molybdenum has not been studied in the literature, leaving this entire area unexplored.

Table 2.1: Summary of graphene-based electrodes for neural interfaces. Z_{norm} refers to the area normalized impedance. CSC refers to the cathodic charge storage capacity.

Graphene type	Catalyst	Transfer	Mode	Size (μm^2)	Z at 1kH (kΩ)	Z_{norm} (kΩ)	OT at 550 nm (%)	Noise	CSC ($\mu C\ cm^{-2}$)	CIC ($\mu C\ cm^{-2}$)	Tests	Encapsulation	Reference
Multilayer	Mo	Transfer-free	Recording & stimulation	68320	27.4	18.7	83	-	2151 ($0.1Vs^{-1}$)	44	Ex vivo	Parylene C	Bakhshaee [40]
Monolayer Doped with HNO3	Cu	PMMA	Recording	10000	963	96.3	80	SNR: 40.8 (neuron signal)		-	In vivo	SU-8	Kuzum [111]
Few layer	Not specified	Polymer	Recording & stimulation	31416	215.7	67.7	90	-	87.8 ($1Vs^{-1}$)	57.13	Ex vivo In vivo	Parylene C	Park [112]
Monolayer	Cu	PMMA	Recording & stimulation	2500	1400	35	80	-		-	Ex vivo	SU-8	Liu [113]
Monolayer	Cu	PMMA	Recording	10000	200	20	80	40 µV under light stimulation		-	Ex vivo	SU-8	Lyu [114]
Monolayer	Cu	PMMA	Recording	707	3000	21.2	85%	20 µV (input 3mV, 0.1 Hz– 3.5 Hz)		-	In vitro	SU-8	Kshirsagar [115]
Few layer	Cu	Chemical transfer	Recording & stimulation	700	2650	18.7	85	SNR: 38.5 (neuron signal)	910 ($1Vs^{-1}$)	150	Ex vivo In vivo	SU-8	Korbitzer [116]
Monolayer Doped with HNO3	Cu	PMMA	Recording	2500	908	22.7	90	SNR: 5 (neuron signal)	15.9 ($0.5Vs^{-1}$)	-	In vivo	Parylene C	Driscoll [117]

Table 2.2: Summary of graphene-based transistors (GFETs) for neural interfaces. The graphene used for all the devices was CVD Cu-grown graphene.

Graphene type	Transfer	W (µm)	L (µm)	$\|g_m\|$	ON/OFF related	Noise	Tests	Encapsulation	Reference
Monolayer	PMMA	60	40	500 µS	-	SNR: 126 V_{DS}: 200mV (1Hz - 10 kHz)	In vitro	Polymide	Cheng [118]
Monolayer	PMMA	60 to 100	40 to 50	1 mS	-	SNR ≅ 30 (neuronal signal)	In vivo	SU-8	Hebert [53]
Monolayer	Chemical transfer	100	80	46 µS	Ratio: 179	-	Ex vivo	NA	Simonescu [51]
Graphene nanowalls	Transfer free	100	80	83 µS	Ratio: 746	-	Ex vivo	NA	Simonescu [51]
Monolayer	PMMA	50	50	400 µS	-	U_{rms} ≅ 40µV	In vivo	SU-8	Schaefer [119]
Monolayer	PMMA	20	10	200 µS	-	SNR: >10 V_{DS}: 100 mV (1Hz - 10 kHz)	In vitro	SU-8	Hess [120]
Monolayer	PMMA	20	10	4 mS	Response time 0.5 ms	10^{-22} A^2/Hz (at V_{LG} = 0 V)	In vitro	SU-8	Veliev [121]
Monolayer	PMMA	30	20	1.3 mS	-	SNR: 38 (neuronal signal)	In vivo	SU-8	Du [122]

3

Materials and Methodology

As discussed in Chapter 1, a key objective of this project is to develop a graphene-based device using a transfer-free process. The feasibility of different processes was explored in order to support the decision of the device design and fabrication. Figure 3.1 represents the sequence of steps involved in the course of this work, along with the corresponding methods applied at each stage. As can be seen, three main manufacturing milestones can be highlighted (in blue; associated with their methodology section), together with the characterization processes (in orange) performed after each fabrication step:

1. Exploration of the technology, the result of which serves to choose the research line.
2. Optimisation of the manufacturing process of the selected device.
3. Manufacturing of the devices with the selected parameters after optimisation.

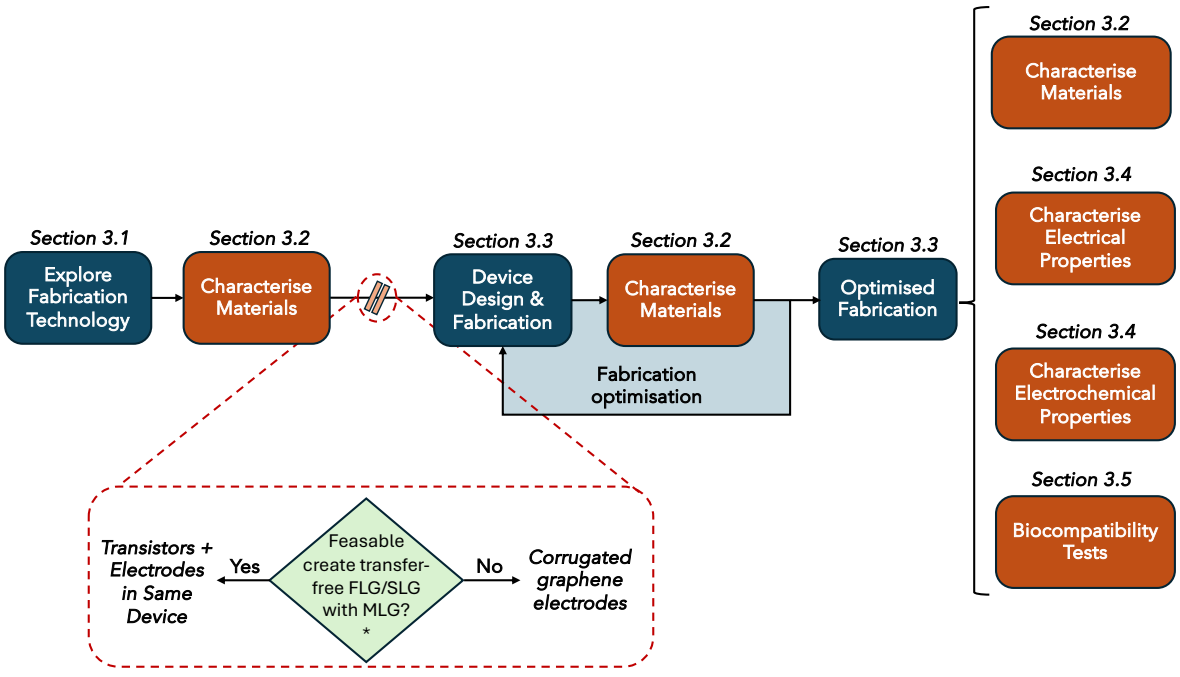

Figure 3.1: Process flow followed in the development of this work, together with the *Materials and Methodology* sections associated to each of the blocks.
*: not feasible in terms of time for an MSc thesis project in the Biomedical Engineering field, but it may be that investing more time will lead to a solution.

As illustrated, the ability to fabricate both FLG/SLG and MLG on the same wafer is the critical factor in determining the device selection. In this section, the materials and methods that have been involved in

each of the steps in the development of this work will be detailed. Note that the term *thin graphene* will be used as a synonymm of SLG/FLG. Previous studies have reported the possible synthesis of FLG using a thick Mo catalyst [128]. For this reason, in this work catalysts of thickness raging 500 nm to 1 µm will be used to study the fabrication of thin graphene. The results of each of the three milestones will be presented separately in Chapters 4, 5 and 6.

3.1. Technology Exploration for Device Selection

This section focuses on the materials and processes used during the first manufacturing stage of the project which, as stated, is an exploratory process. The critical processes to examine are related with CVD graphene growth and posterior substrate etching. For ensuring an adequate and wide study of the technology, three main challenges are proposed. Each challenge is then related with one or more research proposal. Each subsection addresses a specific challenge.

Challenge 1) Fabricate unpatterned thin graphene (subsection 3.1.1).

- **Research Proposal 1:** Grow graphene on non-patterned thick molybdenum (500 nm, 800 nm and 1000 nm). Transfer and analyse its properties.

Challenge 2) Fabricate thin, transfer-free patterned graphene (subsection 3.1.2).

- **Research Proposal 2.1:** Pattern thick molybdenum structures with different 2D dimensions.
- **Research Proposal 2.2:** Pattern graphene after growth on thick molybdenum substrate.

Challenge 3) Determine the effect on graphene when it is grown on a substrate of different heights (subsection 3.1.3).

- **Research Proposal 3:** Create steps in molybdenum bulk substrates and grow graphene.

3.1.1. Fabrication of Unpatterned Thin Graphene

500 µm p-type Si wafers, with a wet oxidation SiO_2 layer of 300 nm underneath, were coated with thick molybdenum layers. In order to understand the properties of thin graphene growth in thick molybdenum substrates, 500 nm, 800 nm and 1000 nm molybdenum thicknesses were deposited by physical vapour deposition using the Trikon Sigma 204 PVD tool at 50ºC. Each wafer corresponds to a unique molybdenum thickness. Considering each wafer, graphene was synthesized using a low-pressure chemical vapor deposition (LPCVD) process on the AIXTRON BlackMagic Pro system, with temperatures set to 935°C at the bottom heating element and 1050°C at the top. The process began with a 20-minute annealing of the molybdenum, followed by the introduction of methane (CH4) as the precursor gas for 20 minutes. A graphene transfer process was conducted following the graphene growth: hydrogen peroxide 30% was used for etching the thick molybdenum layers. Periods between 9 to 10 minutes were sufficient for ensuring graphene delamination, but this depended on the wafer. After that time, the piece of wafer is immersed in DI water, causing the graphene to delaminate and float on the DI water. The transfer process is finished by scooping the graphene with a 90 nm SiO_2 wafer or a glass substrate and drying it with N gas. Graphene properties were then extracted using Raman spectroscopy (for details, see Section 3.2.5), optical transmittance (see Section 3.2.2) and atomic force microscopy (see Section 3.2.6).

3.1.2. Fabrication of Thin, Transfer-free Patterned Graphene

In order to address the fabrication of transfer-free thin graphene, two different research approaches were proposed. The objectives of these set of experiments were to explore the feasibility of a transfer-free process considering a thick Mo substrate, needed to create thin graphene, which required additional understanding on how the graphene growth is affected by the substrate pattern. For both approaches, P-type 500 µm single-side Si wafers with a SiO_2 layer of 600 nm were used for this processes. The oxide layer was created using wet oxidation at 1000 °C. CVD Graphene growth was performed in both processes using the tool and recipe explained in Section 3.1.1. Figure 3.2 shows a schematic representation of both processes considered for thin graphene growth, associated with Research Proposal 2.1 and 2.2.

Considering **Research Proposal 2.1** (**process A** in **Figure 3.2**), the process involved patterning thick molybdenum structures before graphene growth. Wafers with molybdenum layers of 500 and 800 nm were considered. To pattern the thick Mo, a positive photoresist SPR3012 of 1.4 µm was coated, exposed and developed using the ASML PAS 5500/80 Waferstepper tool and a mask from another project contains different structures of different widths and length sizes. The mask consisted of structures with a variety of sizes that was considered convenient for studying how graphene grows on patterned substrates. The patterns were performed before graphene growth using the Trikon Omega 201 ICP-RIE tool, recipe *Mo_Test8*, which uses SF_6 as etching agent and a power of 500 W (etching time depends on Mo thickness). Photoresist removal was performed using NI555 at 40 °C and sonication with 80 kHz and high sonication power. Graphene growth was performed after the molybdenum patterning. After graphene growth, Mo was chemically etched using H_2O_2 30 % and samples were characterised using Scanning Electron Microscopy (SEM, see Section 3.2.3), Energy Dispersice X-ray Spectroscopy (EDX, see Section 3.2.4) and Raman spectroscopy (see Section 3.2.5).

Regarding **Research Proposal 2.2** (**process B** in **Figure 3.2**), the process consisted on growing graphene on a non-patterned thick molybdenum substrate, and create the patterns afterwards. Wafers with molybdenum layers of 50 and 500 nm were prepared. Graphene growth was performed before creating the patterns. After graphene growth, the photoresist was coated, exposed and developed manually, as the wafer was considered as contaminated. As graphene dry etching requires O_2 plasma, the photoresist thickness should be enough to not be completely removed. For this reason, two different photoresist thicknesses were considered in this process: 2.7 µm and 3.1 µm, using AZ ECI 3027 and AZ ECI 3031, respectively. The tool SUSS MicroTec MA/BA8 mask aligner was used for creating the patterns, using the mask *BOTTOM-ELECTRODE*, from the device ROB-MIC-DRUMS, and the soft contact mode. This mask consist on several patterns with different sizes and shapes. The Adixen AMS110 tool was used for creating the patterns on graphene and molybdenum. For graphene etching, an O_2 plasma recipe was used (recipe: EKL GRAPHENE ETCH). Optical microscopy was performed after the procedure to ensure that graphene was etched and to ensure a proper condition of the photoresist. Molybdenum etching was performed on the same tool, using a SF_6 as etching agent. A first test considered 50 nm Mo to test the photoresist tolerance to the recipe. After patterning the molybdenum with graphene, Photoresist removal was performed using NI555 at 60 °C and sonication with 30 kHz and low sonication power to avoid graphene delamination. Considering the 50 nm catalyst, the molybdenum underneath graphene was removed using H_2O_2 30 %. The second test was performed on a 500 nm Mo substrate. A combination of wet (using H_2O_2 %) and dry (using the *EKL MO ETCH MCP* recipe in the same tool, which considered SF_6 at 200 ppm and 500 W) etching processes were used to remove the molybdenum underneath the graphene. The samples were characterised using Scanning Electron Microscopy (SEM, see Section 3.2.3), Energy Dispersice X-ray Spectroscopy (EDX, see Section 3.2.4) and Raman spectroscopy (see Section 3.2.5).

3.1.3. Graphene Growth on Molybdenum Substrate with Variable Step Heights

This section is essential for providing insights into the simultaneous fabrication of thin and thick graphene on the same wafer, as well as for determining if corrugated graphene can be achieved by employing patterns in molybdenum.

In order to study how graphene growth behaves when steps are present in the substrate, two contact aligner masks, *BOTTOM-ELECTRODE* and *GRAPHENE*, from the device ROB-MIC-DRUMS, were used to create molybdenum patterns with different thicknesses in the same wafer. As mentioned, these tests were also considered to initially understand whether graphene retains or replicates the shape of the substrate after wet etching. For this process, p-type 500 µm Si wafers were considered. Wet oxidation was performed to obtain 600 nm SiO_2. Bulk molybdenum layers of 100 nm and 500 nm were sputtered in different wafers. **Figure 3.3** shows the schematic representation of the process. Positive photoresist SPR3012 was coated using the automatic spin coater, achieving a photoresist thickness of 1,4 µm. The mask used for the bulk molybdenum pattern was *GRAPHENE*. The main strucutre was created using the etcher Trikon Omega 201 ICP-RIE tool and the recipe *Mo_Test8*, previously explained. Photoresist removal was performed using NI555 at 40 °C and sonication with 80 kHz and high sonication power. A second lithographic process was performed using the same photoresist characteristics as in the first lithographic step, but using the mask *BOTTOM-ELECTRODE*. This step was used for creating the molybdenum steps inside the patterned molybdenum bulk structure. For substrates of 100 nm, a step of 25 nm was performed. In case of 500 nm, a step of 200 nm was created. In

both of the cases, the recipe used was again *Mo_Test8*, but varying the etching time depending on the desired step height. Photoresist removal was performed as in the first molybdenum pattern step. The structures were characterised using SEM and AFM before graphene growth to understand how the second etch affected the molybdenum surface. Graphene growth was performed using the tool and recipe showed in Section 3.1.1. After graphene growth, wet etch was performed with H_2O_2 30% to remove the molybdenum. The samples were then characterised using SEM, EDX, AFM and Raman spectroscopy.

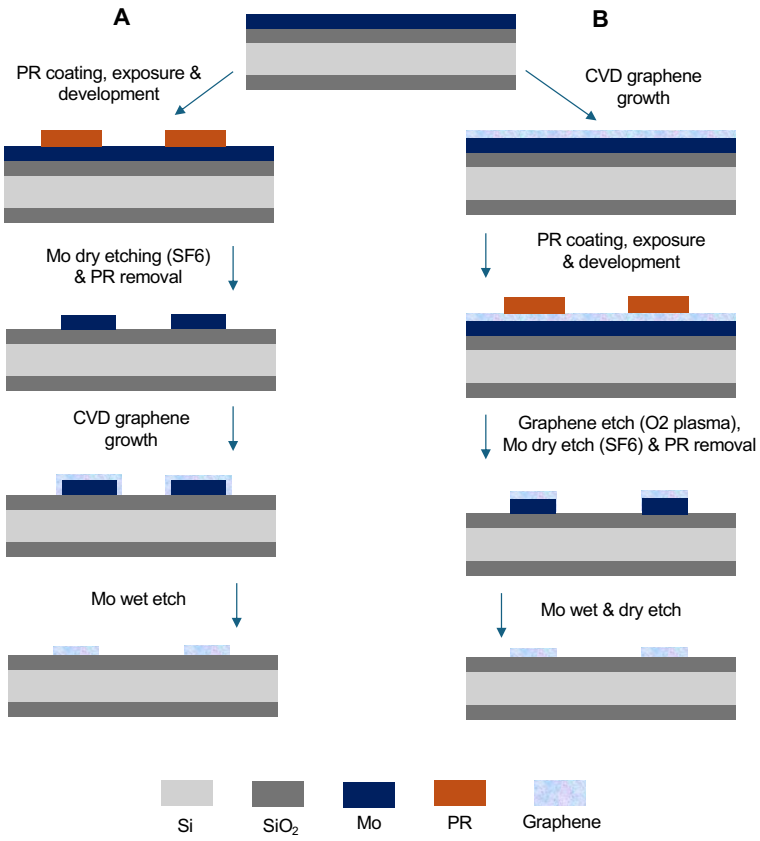

Figure 3.2: Schematic representation of the processes performed for exploring transfer-free, thin graphene growth, considering as common point the whole wafer covered with Mo. Process A considers graphene growth after patterning the substrate; Process B considers graphene growth before creating the patterns.

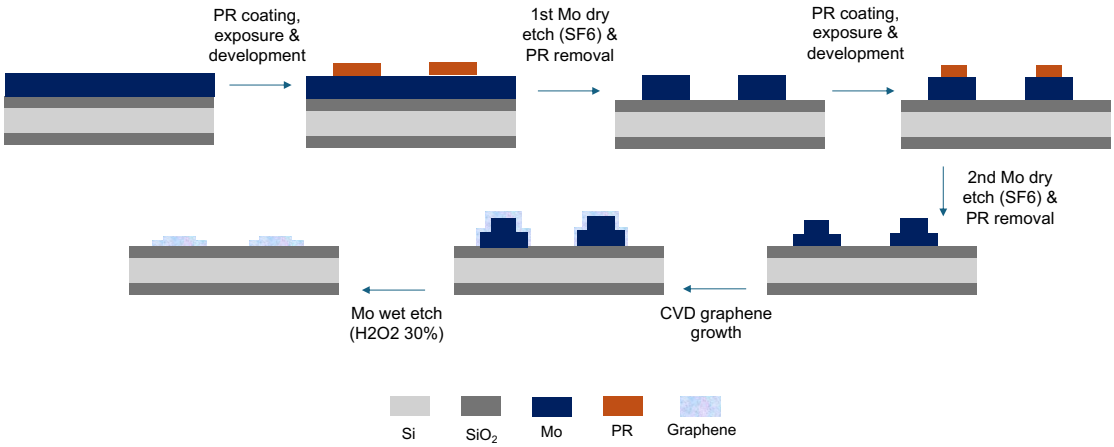

Figure 3.3: Schematic representation of the process performed to study the creation of steps in molybdenum.

3.2. Material Characterization

This section describes the techniques used to characterise the materials obtained during the development of this work. It is important to mention that not all techniques were applied at every manufacturing step; however, all of them were essential at various stages of the work, particularly for characterizing the properties of graphene.

3.2.1. Optical Imaging

All steps involved in the fabrication required inspection using an optical microscope with magnifications from x10 to x100. Moreover, a KEYENCE microscope (VHX-7000 Series) was used to inspect the final devices in detail. This device has two different lenses, covering a magnification range from x20 to x2000. In addition, it offers the possibility of collimating the light beam in various configurations, allowing the desired structures to be highlighted according to the material to be characterised. In addition to being used to confirm the lack of residues in the devices before wire bonding, it was also used to detect possible structural changes in the devices after electrochemical tests.

3.2.2. Optical Transmittance

Optical transmittance (OT) measurements were performed on graphene samples transferred to a glass holder. Measurements were performed in samples grown at both 50 nm Mo and 800 nm Mo. The measurements were conducted using a Perkin Elmer Lambda 1050+ UV/VIS/NIR Spectrometer in the ESP lab over a wavelength range of 300 to 1200 nm, with intervals of 5 nm. During these measurements, the sample was positioned with its front side directed towards the integrating sphere and its backside facing the light source. Measurements were taken for both the glass on its own and the graphene on the glass. The values obtained from the glass alone were subtracted from the graphene-on-glass measurements to isolate the graphene's transmittance values.

3.2.3. Scanning Electron Microscopy

SEM provides high-resolution imaging, with the possibility to observe fine details at the nanoscale. In addition, it has a large depth of field, allowing more parts of the sample to be in focus at the same time, resulting in clear, three-dimensional images. This makes it ideal for studying the topography and morphology of surfaces. Usually, a SEM can provide several image modes, being secondary electrons (SE) mode the main one used in this work. SE images have high spatial resolution and provide good contrast, revealing fine surface structures and textures. The SE signal is more sensitive to topographical changes because secondary electrons are generated close to the surface. High resolution SEM images were obtained using two different tools. SEM Hitachi Regulus 8230 tool, which offers a maximum resolution of 2,000,000X, was used to inspect the materials between fabrication steps inside the cleanroom. The SEM FEI XL30 SFEG was also used to obtain high resolution images of the materials which would have been taken out of the cleanroom.

3.2.4. Energy Dispersive-XRay Spectroscopy

EDX offers the possibility to analyse the elemental composition of a sample. The principle of operation is based on detecting X-rays emitted by the atoms of a sample after an electron beam hits it. These X-rays are element-specific as they depend on the energy released in the transition of electrons between the valence shells of the atoms. EDX measurements require a dedicated detector but are usually performed during SEM procedures. The SEM XL30 SFEG was used to perform EDX measurements, which were mainly used to detect the presence (or absence) of molybdenum after etching processes.

3.2.5. Raman Spectroscopy

As mentioned in Chapter 2.2.2, Raman spectroscopy is one of the most powerful techniques for characterising 2D materials due to its non-destructive nature. It can be used to get an idea of the type of graphene you have (thin or thick), so in this work, Raman spectroscopy is one of the most relevant characterisation techniques has been used to characterise the graphene synthesised after all the manufacturing processes. A Renishaw inVia Raman Microscope was used, employing a 28mW 633 nm laser as monochromatic light source. The laser was ignited 30 minutes before performing the measurements to ensure stable measurements. For all experiments, the range of measurement was from 1100 to 3200 cm^{-1}, with 20 seconds exposure time and a laser power of 50%. Both single point mea-

surements and area mappings were carried out. In both cases the parameters were maintained. The data obtained after the measurements were analyzed in using a modified version of the MATLAB script originally developed by Vollebregt et al. [129].

3.2.6. Atomic Force Microscopy

AFM is a high-resolution imaging technique used to analyse the topography of the sample of interest. AFM is especially useful for characterizing corrugated and rough surfaces, as it can precisely measure variations in height. In this work, AFM was employed to characterise the surface of corrugated samples graphene and determine the thickness of transferred graphene by measuring the step height between the graphene layer and the SiO_2. A Bruker Dimension Icon tool in tapping mode was used to obtain high resoltion images between 5 μm^2 and 50 μm^2 were obtained. AFM images were processed with Gwyddion software.

3.3. Design and Fabrication Process

After having addressed and analysed the technology exploration tests (see Chapter 4), the design of transfer-free, corrugated graphene electrodes was considered as the most feasible alternative for this project. In this section, the design and fabrication process of the devices including the corrugated graphene electrodes will be addressed.

3.3.1. Masks Design

To develop the principle of this work and in order to have a reference work to compare with, electrodes dimensions and device shape were based on Bakhshaee et. al work [42]. Every device is constituted by four electrodes, the tracks, the contact pads and the openings. For all the devices, the electrodes opening dimensions were preserved, being each electrode 250 µm of radius (exposed area after openings: 170 µm radius). Compared to Bakhshaee et al. [42] design, the tracks were shortened for the external electrodes, and the width ot them was increased in a 2.1 factor to reduce the track impedance. As these surface topography is relatively a new field to explore, the final devices substrate was considered to be silicon rather than on a flexible polymer substrate to facilitate the experimental characterisation.

In order to explore the role of the surface topography on graphene properties and in the electrode surface area, 22 different corrugation patterns were created. After exploring the literature, it was found that anisotropic continous geometry of alternating grooves is one of the most used surface patterns. For this reason, this pattern was considered, being referenced as ”lines” throughout the work for practical reasons. On the other hand, in order to consider a broader study, isodimensional structures such as squares were also considered, topography for which literature is also available as discussed in Section 2.2.1. Squares were chosen over circles for practical reasons during the mask design process in the software, as they are equally suitable for the proof-of-concept development in this work.

Table 3.1 shows the different corrugated pattern combinations considered in this work. The pattern variation was achieved by changing the size of the structures, as well as the spacing between them. Within an electrode, only one pattern was considered. At the same time, every pattern was present in at least two different devices. The electrodes of devices D1 to D6 present different corrugation patterns within the same device. The main reason to have different corugation patterns in one device is to eliminate a possible bias during characterization that may be potentially generated by inhomogeneities within a wafer, resulting from the CVD graphene growth process. On the other hand, devices D7 to D28 are composed by electrodes with the same corrugation pattern within the same device. These devices were designed for extracting statistics during the same characterization test. Device D29 consists of four electrodes without any corrugation pattern. Two of the electrodes will have graphene grown on a substrate which thickness is the initial bulk Mo (without etch), and the other two electrodes will have graphene grown on a completely etched area (a thiner substrate without topography). This device was designed to understand the possible differences in graphene growth that might be dependent on the surface roughness and, depending on the etching time, on the thickness of the substrate.

Additionally, for measuring the sheet resistance that might be dependent on the corrugation pattern, transmission line measurement (TLM) structures were created. Each TLM structure contains a defined corrugation pattern and is labelled considering the system on the table. A detailed explanation on how the TLM structures work is provided in Section 3.4.1.

Figure 3.4 shows the detailed layout of the wafer considering the masks designed in this work. As mentioned, a total of 29 devices were designed and distributed through two thirds of the wafer. The remaining third of the wafer was used to fabricate 142 TLM structures. For software optimization reasons while designing the masks, two different TLM sizes were considered. The smaller TLMs (300 µm x 2300 µm) were suitable for smaller size corrugation patterns, while the bigger ones were needed for analysing the sheet resistance of bigger patterns (600 µm x 4600 µm). Each pattern is used at least in four TLM structures and distributed through the wafer to avoid biasing on the results caused by graphene growth inhomogenities. Overlapping of the encapsulation with the Mo layer is necessary in these structures to avoid graphene delamination during the Mo wet etching process. This overlapping is 10 µm per edge for small TLMs and 20 µm per edge for large TLMs, which in this work proved to be sufficient to avoid graphene delamination in large structures.

Table 3.1: Corrugation pattern labelling and device identification

Symbol on Ti/Al layer	Corrugation structure	Dimensions (µm)	Spacing (µm)	Used for device
L0101	Line	1 (width)	1	D1, D7
L0105	Line	1 (width)	5	D1, D8
L0120	Line	1 (width)	20	D3, D9
L0505	Line	5 (width)	5	D2, D10
L0525	Line	5 (width)	25	D2, D11
L0550	Line	5 (width)	50	D3, D12
L2020	Line	20 (width)	20	D4, D13
L2040	Line	21 (width)	40	D4, D14
L2060	Line	20 (width)	60	D6, D15
L5010	Line	50 (width)	10	D5, D16
L5050	Line	50 (width)	50	D5, D17
S0101	Square	1x1	1	D1, D18
S0105	Square	1x1	5	D1, D19
S0120	Square	1x1	20	D3, D20
S0505	Square	5x5	5	D2, D21
S0525	Square	5x5	25	D2, D22
S0550	Square	5x5	50	D3, D23
S2010	Square	20x20	10	D4, D24
S2040	Square	20x20	40	D4, D25
S2060	Square	20x20	60	D6, D26
S10010	Square	100x100	10	D5, D27
S10050	Square	100x100	50	D5, D28
Mo	-	-	-	D29
Mo-x	-	-	-	D29

The fabrication process requires the patterning of different materials. For the lithography of each material a different mask is required. In this case, four different glass masks with a specific chrome pattern were used. The masks used are explained hereunder:

1. MO BULK. Mask used to create the main structure of the molybdenum. This is the electrodes, the tracks and the contact of the metal pads (see Figure 3.5.c).
2. MO CORR. This mask is used to create the corrugation patterns on the electrodes and the TLM structures (see Figure 3.5.f). As will be seen in Section 3.3.2, this mask can be used either to pattern the molybdenum bulk or to pattern the SiO_2.
3. METAL. Mask necessary to create the contact pads for subsequent wire bonding and the pads for performing the TLM measurements (see Figure 3.5.d).
4. OPENINGS. Mask used to create the openings on the photoresist for the final device (see Figure 3.5.e). In this case, photoresist was selected for simplicity reasons, avoiding extra steps to protect graphene.

Additionally, a foil mask containing the same design as mask OPENINGS but in negative was used to pattern SU8. This encapsulation was only used for the biocompatibility tests, as over time SU8 turned out to be partially permeable to H_2O_2, which leads to degradation of the Mo tracks. Foil masks have a lower resolution (10 µm) compared to glass masks (1 µm), but this is not an issue since the

openings are on the scale of hundreds of micrometers.

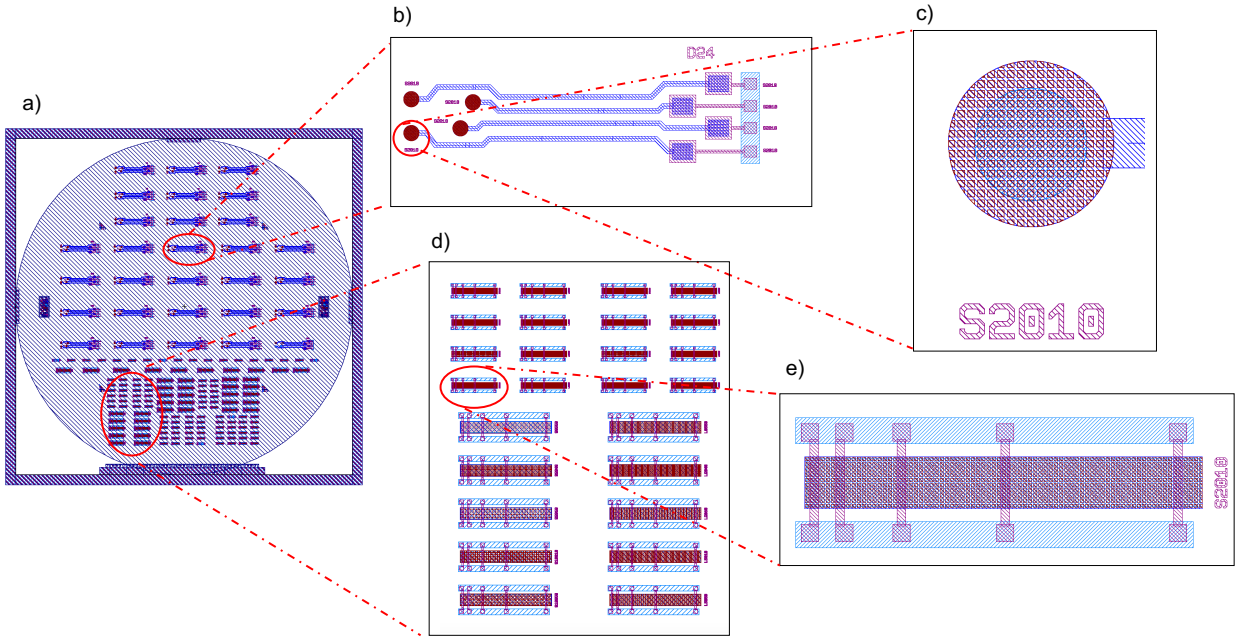

Figure 3.4: Full view of the mask design. **a)** Full wafer layout. **b)** Device view, in this case D24, consisting of four electrodes with the same pattern (squares of dimensions 20x20µm, spaced 10µm between each other). **c)** Detailed view of one of the electrodes from D24. **d)** Zoom to different TL structures. **e)** Detail of a TL structure, with the same pattern as in D24.

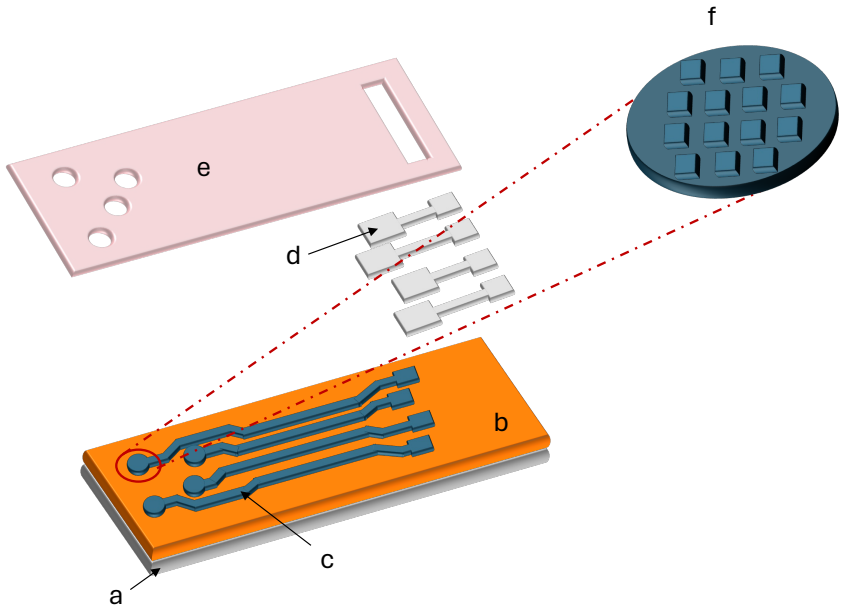

Figure 3.5: Schematic representation of a device, consisting on different materials and patterns. **a)** Silicon layer. **b)** Silicon oxide layer. **c)** Molybdenum layer, conforming the bulk structure of the device. **d)** Metal contact pads. **e)** Photoresist coating (insulation) with openings. **f)** Detailed structure of an electrode with a corrugated pattern.

3.3.2. Optimization of the Fabrication Processes

As discussed in previous chapters, the creation of transfer-free graphene on pre-corrugated surfaces remains a relatively unexplored area. Therefore, the fabrication process in this work requires investigating various parameters to assess the feasibility of producing transfer-free, micrometric corrugated graphene. Characteristics such as sheet continuity and the number of graphene layers are relevant parameters that may change depending on the parameters used.

The aim of this subsection is to insightfully define the steps performed during the optimization of the devices flowchart. Considering the same four glass masks, two different fabrication processes were followed during the optimisation procedure, which differ in the material and step where the corrugation pattern is created. Considering Optimization Process 1, the corrugation pattern is created in the molydenum bulk structure, while in Optimization Process 2 the patterns are created on the SiO_2. Both processes commence creating the alignment marks in a p-type 500 µm silicon wafer. The tool Trikon Omega 201, are used for performing this step. After that, a 600 nm SiO_2 layer is grown using a wet oxidation process. The Tempress Furnace - Tube 4 was used for creating the silicon oxide layer. After this step, two different optimization processes can be considered. Table 3.2 shows the parameters that were varied during the optimisation, associated with each of the processes. Figure 3.7 shows a schematic representation of both optimization processes, considering the transversal section of an electrode. A general explanation of the sequence of steps for each process is provided below to help the reader understand the differences between them.

Table 3.2: Summary of the optimisation parameters varied in each of the processes. OP = Optimization Process. Variables are not correlated between each other. *Bulk Mo thickness* refers to the amount of molybdenum deposit before doing the step (in OP 1) or after doing the step (in OP 2). Contact mode and Exposure time columns are contact aligner parameters varied for the MO CORR mask.

Corrugation substrate (MO CORR)	Bulk Mo thickness (nm)	Contact mode MO CORR	Exposure time MO CORR (s)	Etching method	Step height (nm)	Graphene growth
Corrugation Mo (OP 1)	200	Hard	[4 – 9]	**RIE** (Trikon Omega 201)	100 - 200	After Mo pattern
	300	Soft				
	500					
Corrugation SiO2 (OP 2)	50	Hard	[6 – 7]	**RIE** (Oxford PlasmaLab 100 Polaris)	80 - 400	After Mo pattern
	100			**RIE** (Drytek)		Before Mo pattern
	300	Soft		**DRIE** (Adixen AMS110)		
	500			**Wet** (BHF)		

Regarding **Optimization Process 1**, the process continues with a molybdenum deposition. Tests with molybdenum bulk thicknesses of 200 nm, 300 nm and 500 nm were performed. Thicker layers were not considered to facilitate metallisation of transmission line measurement (TLM) structures. The deposition is performed using the tool Trikon Sigma 204 - Dep C. A litographic process is then followed for creating the device main structure (electrodes shape, tracks and contact pads). A positive photoresist SPR3012 is coated, exposed and developed. The mask **MO BULK** is used in the SUSS MicroTec MA/BA8 mask aligner. Molybdenum is then etched usign the Trikon Omega 201 tool *Mo_Test8*. The photoresist should be then removed using NI555 at 40 °C, and a sonication of 80 kHz and high sonication power. A second litographic process on the molybdenum is then performed to create the corrugation patterns in the molybdenum. The steps are analogous to the previous litographic process, but differing in the mask used, which in this case is **MO CORR**. Molybdenum is etched, considering step sizes varying from 100 nm to 200 nm. This is achieved by changing the etching time parameters on Trikon Omega 201 tool (times varying between 25 s and 30 s). The photoresist is again removed using NI555 and the same conditions explained previously. The following step is performing a CVD of graphene, which was performed using the tool and recipe showed in Section 3.1.1. Once graphene is grown, the contact pads are created for performing electrical tests. One should note that this step is not reflected in Figure 3.7, as no metal layer is deposited on top of the electrodes. The metal optimisation part will be explained after introducing Optimisation Process 2, as it is analogous to both processes and required its own adjustment process.

Considering **Optimization Process 2**, after the oxidation of silicon, a lithography process is followed for creating the corrugated structures on the SiO_2. For this, SPR3012 photoresist is coated, exposed using the mas **MO CORR** and developed using the automatic spin coater. In order to create the patterns on the SiO_2, DRIE and wet etching methods were explored (see Table 3.2). After removing the remaining photoresist using a O_2 plasma or chemical removal, a molybdenum deposition is performed using the Trikon Sigma 201 tool. In order to create the electrodes structure, considering the process of graphene growth after patterning molybdenum, SPR3012 photoresist is coated, exposed using the **MO BULK** mask and developed using the automatic spin coater. After the remaining photoresist is removed, graphene growth is performed in the AXTRON Black Magic, using the same recipe as mentioned above. Considering graphene growth before patterning molybdenum, manual coating and developing are necessaries for creating the litho pattern on both graphene and molybdenum. For this, the AZ ECI 3027 photoresist is manually coated and developed, and both graphene and Mo are dry etched using the Aixden AMS100.

In order to avoid delamination on the pads of the transmission line structures, the metal layer had to be optimised as well. Various metallisation processes with Ti/Al1%Si, Ti/Al and Ti/Au were tested, as can be seen in Table 3.3. The lithographic process involves a manual coating, expose and development, using the AZ3027 photoresist and mask **METAL** (in case of using aluminium), or NLOF-2020 (in case of using gold). After manual development, a wet etching process (for aluminium) or a lift-off process (for gold) should be performed. In case of chemical etching, the photoresist is then removed using IPA. In both cases, for creating the device encapsulation, photoresist AZ3027 is manually coated, exposed and developed. For creating the openings, the mask **OPENINGS** is used.

Table 3.3: Summary of parameters tried for the metallisation layer.

Metallisation material	Tool	Ti thickness (nm)	Thickness (nm)	Pattern method
Al1%Si	Trikon Sigma 204	100	675	Wet etch (0.55% HF)
Al	Trikon Sigma 204	10	300	Wet etch (0.55% HF)
Au	CHA	10	200	Lift-off (NI555)

Considering both flowcharts, the molybdenum layer under the electrode area is removed using a H_2O_2 30% solution. Etching times between 5 and 8 minutes were used. Devices are then submerged in DI water for removing possible H_2O_2 residues and dried using nitrogen gas.

3.3.3. Interface for Electrical Measurements

Considering the final devices (after optimisation), in order to perform stable electrical measurements, a PCB designed to electrically characterise the silicon devices fabricated in [42] was used, as they proved to perform with the expected outcome in terms of electrical stability (see Figure 3.6). After performing the dicing of the devices with the Disco Dicer (DAD3240) , the dies were glued to the PCBs using Superglue. Gold wire bonding was performed to create the interconnection bonding between the device electrodes and the printed circuit board (PCB). The TPT HB05 Au bonder was used for this process, employing gold wire with a ball-wedge wire bonding technique. Ultrasound power settings of 250 mW and 270 mW were applied for the first and second bonds, respectively, both using a force of 20 mN. For the final tests, a total of 29 devices were glued and wire bonded. Polydimethylsiloxane (PDMS) and epoxy resin were used for encapsulation of the pads.

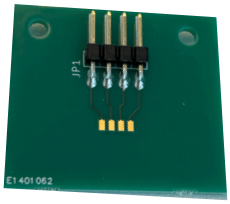

Figure 3.6: PCB used for electrochemical measurements. Designed by S. Rice at [130].

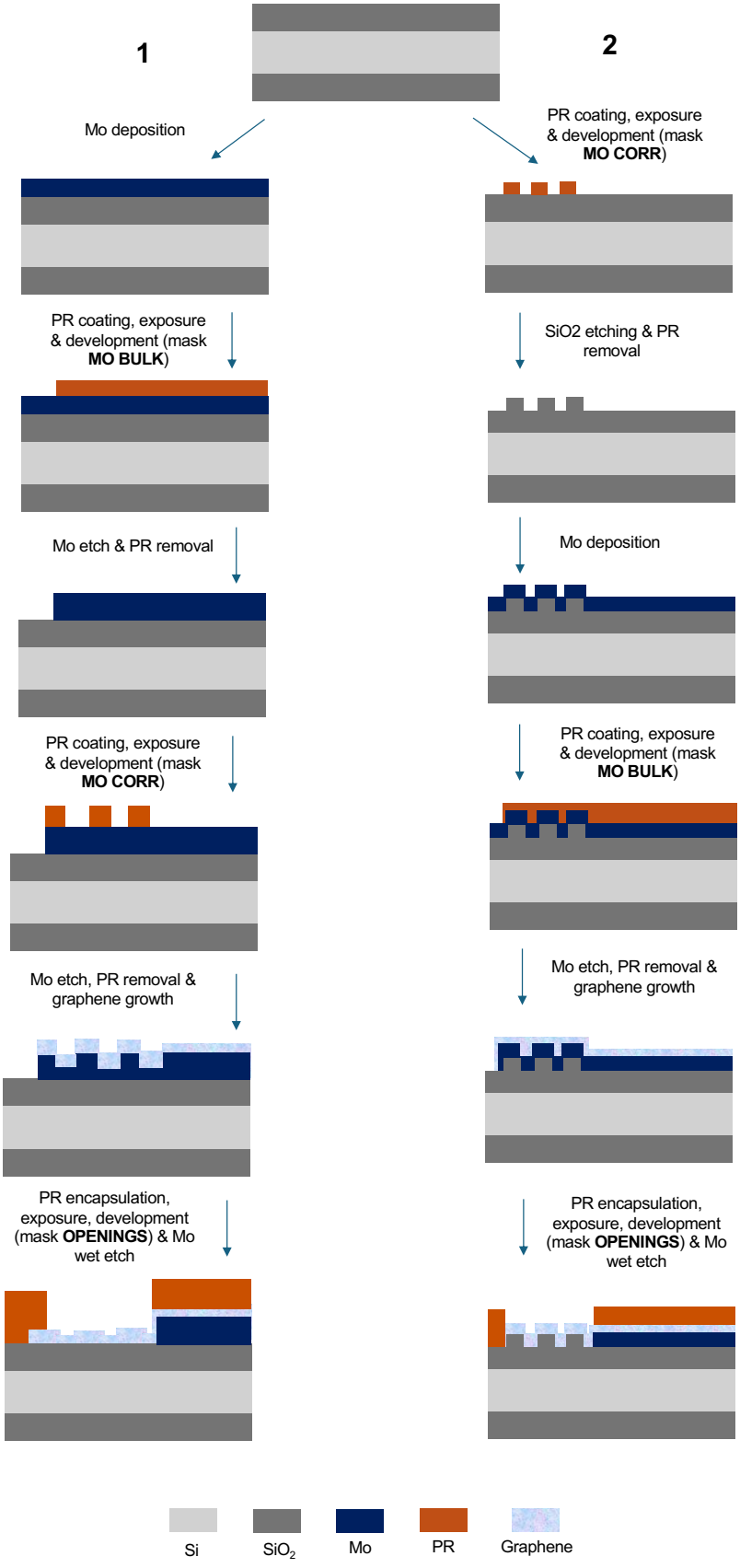

Figure 3.7: Schematic representation of the fabrication processes followed during optimization (cross-sectional view of an electrode with a corrugated pattern). **OP 1:** the corrugation pattern is created on the bulk molybdenum structure. **OP 2:** the corrugation pattern is created at initial steps on the SiO_2. It should be noticed that not all stages of the process are graphically represented, as the aim of this image is to provide the reader with a straightforward understanding of how one process differs from another.

3.4. Electrical and Electrochemical Characterization

Electrical characterisation was performed for some of the wafers created during the optimisation process and final devices wafers, while electrochemical tests were performed only for the final devices.

3.4.1. Transmission Line Measurements

Transmission line structures were designed to measure the sheet resistance of the materials produced, since Van der Pauw structures are not suitable for use with corrugated materials as they assume a flat, uniform sheet. Typically, TLM structures can also be used to measure the contact resistance between pads. The structures of the TLM as well as the procedure for calculating sheet resistance using these structures is outlined below.

Figure 3.8 shows a schematic representation of the TLM structures used in this work, which consist of a rectangular surface, in which the corrugation patterns are embedded. In this surface a series of metallic contacts are placed on the surface of the material at controlled intervals. The configuration usually consists of five or more parallel contacts spaced at different distances along the corrugated surface. The distances, denoted in Figure 3.8 as d_1, d_2, d_3 and d_4, progressively increase, being d_1 the shortest and d_4 the largest. The resistance is then measured between each pair of contacts, measuring the resistance for each distance d_x. In this work, a four-probe point measurement station was employed. Since in this work we were mainly interested in measuring the sheet resistance of the material, the measurements were performed applying a constant voltage across the entire structure during all measurements and measuring the four resistances. This should give small values of contact resistance, since the probes that measure the voltage would not draw any current in an ideal scenario. In practice, this is not exactly the case due to non-uniform current distributions, imperfect contact or variations in probe geometry and pressure, so contact resistance contribution is always present. After measuring the resistances, they are plotted on a 'Resistance vs Contact Spacing' plot. The data are then fitted to a straight line model, as represented in Figure 3.9. As can be seen, plotting all the resistances results in the equation of a straight line of the form:

$$R_T = \frac{R_S L_X}{W} + 2R_c \tag{3.1}$$

where R_T is the resistance measured, R_S is the sheet resistance, L_X is a generic distance, W is the width of the structure and R_c is the contact resistance.

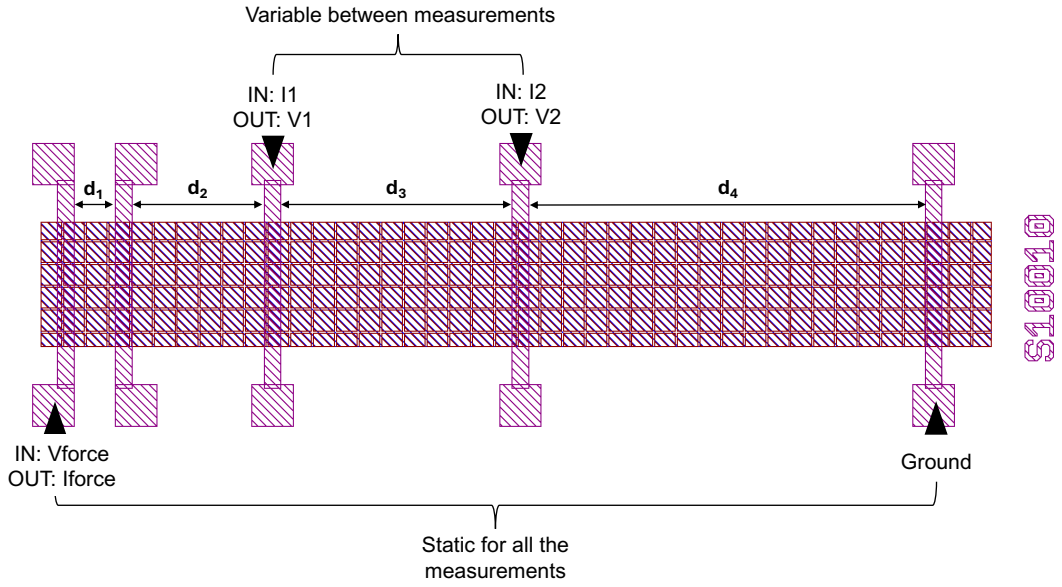

Figure 3.8: Schematic representation of a transmission line structure. With five contact pads separated by distances d_1, d_2, d_3 and d_4. As mentioned above, two sizes of TLMs were created in this work, so these distances depend on the size of the structure.

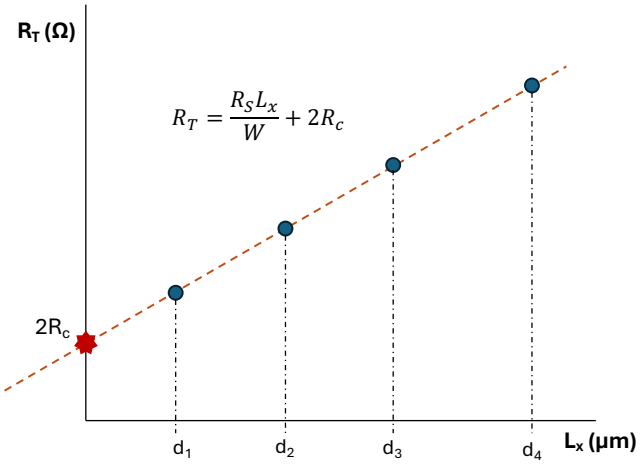

Figure 3.9: Generic example of a 'Resistance vs Contact Spacing' plot. As can be noted, $2R_c$ is the intersection point, while the slope of the curve is R_s/W.

In this work, a Cascade Summit 12000 was used for performing the TLMs, which operates at room temperature. Four needles, each one connected to high resolution channel, were used. A model was used that inputs a variable current (OUT: Iforce) from a variation in voltage (IN: Vforce), see Figure 3.8. Vforce is varied from -200 mV to 200 mV, with 51 points and a step size of 8mV, and a compliance of 100mA. The pad connected to ground also has a compliance of 100 mA. On the measurement pads, IN:I1 and IN:I2 refer to the measurement variable, which in this case is the current flowing through the sample, and OUT:V1 and OUT:V2 are the measured voltages. During the measurements, the needles for force and ground remained positioned on the same pads, while the needles used to measure the voltages between pads were adjusted for each measurement. For each of the distances, a *I vs V* curve was obtained from which the resistance R_T is obtained for that particular measurement.

3.4.2. Electrochemical Impedance Spectroscopy

In order to perform the electrochemical tests, the three electrode setup shown in Figure 3.10 was used, using a Ag/AgCl reference electrode (RE), a platinum counter electrode (CE) and the particular electrode to characterise as working electrode (WE). The devices where carefully placed inside a phosphate-buffered saline (PBS) solution to perform the measurements. A potentiostat Autolab PGSTAT302N and a Faraday cage were used to perform all the electrochemical tests. The software NOVA was used to apply the tests.

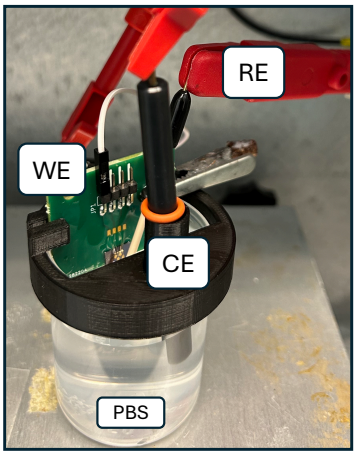

Figure 3.10: Three electrode setup used in this work. The 3D printer holder was fabricated by S. Rice [130].

Considering the EIS measurements, the program *CytO$_2$.0EIS* from the NOVA sofwtare. This model applies a 10 mV RMS sinusoidal signal between the WE and the CE. The current is then measured

between the WE and the RE. Fifty sinusoidal signals with frequencies ranging from 1 Hz to 100 kHz were applied, and the impedance values, along with the phase diagrams, were obtained for each signal. The impedance at 1kHz was used as comparison value.

3.4.3. Cyclic Voltametry

CV measurements were also performed using the three electrode setup mentioned above. The model *Cyclic Voltametry Linear Scan* from the NOVA software was used, and the potential limits used ranged between -0.6 V to 0.8 V, depending on the electrode to be characterised. Three scans per measurements, with a scan rate of 0.1 Vs^{-1} was used in order to compare with [101] and [130]. The cathodic area was used to calculate the CSC.

3.4.4. Voltage Transient

The three electrode setup was also used to perform VT measurements. The program *Chronopotentiometry fast* from the NOVA software was used to inject a biphasic current with 1ms pulse and 100 µs delay. The amplitude of the current was variable and the maximum depended on the electrode used, with the main condition of keeping within the water window (-0.6V a- 0.8V). CIC values were calculated using the largest current pulses.

3.5. Biocompatibility Tests

To assess the cytotoxicity of both the corrugated structure and the material, biocompatibility tests with cells were conducted. The biocompatibility tests were carried out in collaboration with KU Leuven, with the Department of Development and Regeneration and Prometheus research team. Small TLMs were used for performing the biocompatibility tests. To simplify the experimentation, six TLMs were treated as a single sample for cell growth (see Figure 3.11). The samples were distinguished by the shape of the patterns, with different samples featuring either lines or rectangular patterns. The metal part was considered not necessary for this tests. A total of 32 samples with small structures and 2 samples with large structures were prepared. Samples with large strucutres were used for the pilot test.

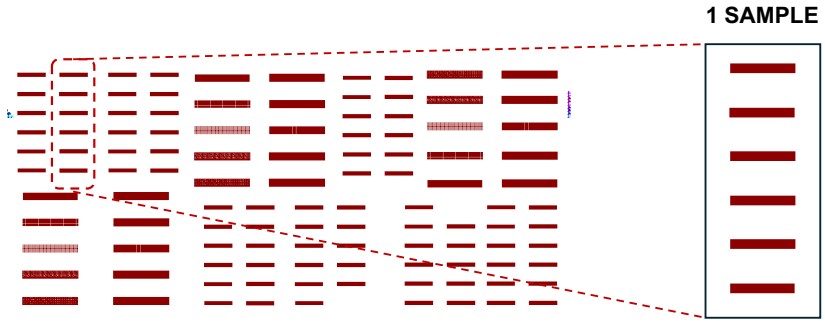

Figure 3.11: Schematic representation of the samples used for biocompatibility tests. 6 structures are considered one unique sample.

3.5.1. Encapsulation and Sterilization

Since the structures are considerably large, encapsulation is necessary to avoid graphene delamination during the molybdenum etching process, as explained in Section 3.3.1. The encapsulation method used for proof-of-concept testing in this work was the positive photoresist AZ 3027, with a thickness of 3.1 µm. However, this material is not biocompatible. For this reason, SU8 was considered as an alternative encapsulation method for the biocompatibility tests, since this polymer is known to be biocompatible [131]. SU8 is a epoxy-based, UV photosensitive negative photoresist, i.e. it changes its mechanical properties when exposed to UV. Since it is a negative polymer, when exposed to UV light the light-exposed part hardens and after development the non-light-exposed parts are diluted. As this is the opposite behaviour to the negative photoresist used in this work to create the encapsulation lithography, it was necessary to order a foil mask that had the negative pattern of the OPENINGS mask, as explained in Section 3.3.1. Several tests were carried out with SU8 - 3005, in order to obtain a 5µm, biocompatible encapsulation. Samples of three different wafers were considered for the final biocompatibility test, as

can be seen in Figure 3.12. Samples were diced with the Disco Dicer (DAD3240) an labelled before being sent. Samples coming from W189 and W188 maintained the SU8 encapsulation, but W229 experienced SU8 delamination during the process. Considering this last wafer, only 4 samples did not experienced graphene delamination after Mo etching and were considered for the biocompatible test.

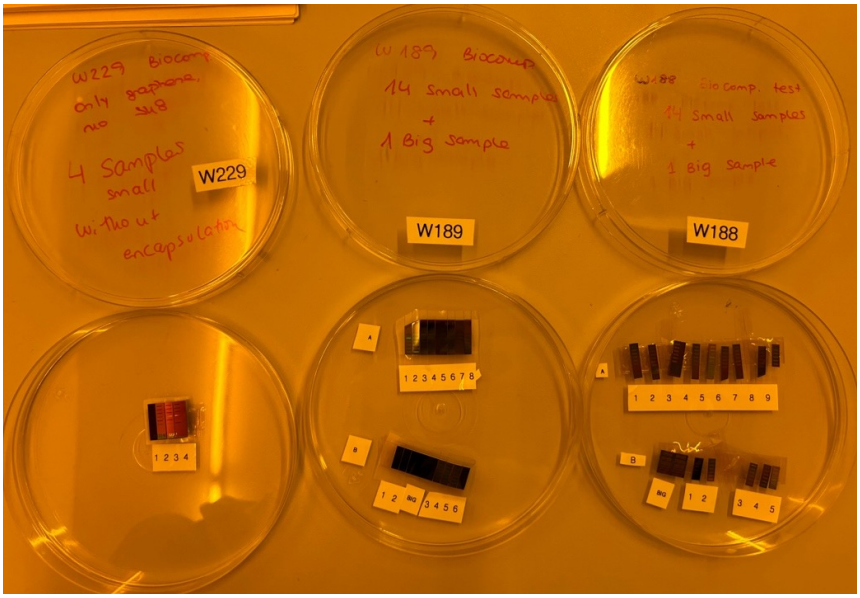

Figure 3.12: Diced and labelled samples used for biocompatibility tests coming from three different wafers.

Considering sterilisation, the typical procedure before a biocompatibility test in KU Leuven involves UV and ethanol sterilisation. Because SU8 is UV sensitive, the UV sterilisation process was discarded. The samples were immersed in 70 % ethanol at 37ºC for 24h to ensure proper sterilisation of the samples, being this a safe sterilisation procedure for materials with SU8 as encapsulation [132].

3.5.2. Cell Expansion and Pilot Test

To address de biocompatibility of the fabricated structures, periosteum cells derived from human donors (hPDCs) were used. Agregated cell samples were obtained from hPDCs cells coming from various donors and cultured until passage 7, where ”passage 7” refers to the amount of time a population was split. In this case, trypsin was used to split the cells 6 times. The cells were cultured at 37ºC considering 95% humidity and 5% CO_2, using the DMEM (Dulbecco's Modified Eagle) medium from Life Technologies. To allow proliferation, the media was supplemented with 10% fetal bovine serum (HyClone FBS, Thermo Scientific) and 1% antibiotic-antimycotic (100 units/mL penicillin, 100 mg/mL streptomycin, and 0.25 mg/mL amphotericin B). The complete medium will be referred as DMEMC.

Cell expansion was performed in different well plates for different cell concentration: 3K, 6K, 10K and 20K. Ideally, the cells should be confluent on the seventh day of proliferation. The pilot test was performed in the big samples in order to gather initial evidence of biocompatibility. For the pilot tests, 10K and 20K concentrations of hPDCs were used to perform the life-dead staining. 4 well plates were used for the tests: 2 well plates with the samples, and 2 well plates as control.

3.5.3. Live/Dead Fluorescence Assay

Death/Life Fluorescence assays were performed to evaluate the cell viability, qualitative distinguishing between the living and the dead cells. Living cells are stained with calcein and generate green fluorescence, indicating the amount of living cells. On the other hand, dead cells are labelled with ethidium homodimer dye, molecule that binds to the DNA, generating a red fluorescence [133]. This test provides a visual and quantitative assessment of cell viability. The LIVE/DEAD Viability/Cytotoxicity Kit (Invitrogen, USA) was used to perform these tests. The protocol starts by rinsing the samples with PBS. After the rinsing, the samples are incubated for 30 minutes in a DMEMC medium with 2µM Calcein AM and 4 µM and 4 µM ethidium homodimer-1 at 37ºC, in a enviromnent with 95% humidity and

5% CO_2. In order to properly visualize the stained cells, after 30 minutes the medium was replaced by PBS. The stained cells were visualized using a fluorescent THUNDER Leica microscope. Live/dead images were obtained for the days 0 and 7.

3.5.4. Presto Blue

PrestoBlue assays are used to address mammalian cell viability or proliferation in a quantitative way, by measuring the fluorescence. This technique offers non-citotoxicity and the possibility to extract information form the same sample through time. The protocol starts by adding 900 µl of the DMEMC medium and 100 µl of the presto blue reagent. The wells containing the samples and the control wells were then incubated for 3h at 37ºC in a enviromnent with 95% humidity and 5% CO_2. 10 wells were used: 5 wells containing a sample per well, and 5 control wells. To perform the measurements, after 3h, 3 times 100 µl are extracted per well and placed in a 96 well plate to perform statistical analysis per sample, per time point (0, 3 and 7 days). The fluorescence was measured using the machine “Infinite 200 Pro”. The measurements for each day were normalized considering the measurements from day 0.

3.5.5. Dapi Phalloidin

Dapi Phalloidin assays were performed to study the structural characteristics of cells. DAPI (4’,6-diamidino-2-phenylindole) is a molecule used to reveal the location of the cell nuclei, while Phalloidin highlights the actin filaments present in the cytoeskeleton. DAPI-stained nuclei usually appear blue, while phalloidin-stained actin filaments can appear in a contrasting color, usually green. In combination, both stains provide insightful information about the cellular structure. The protocol starts by fixating the cells with 4% PFA (paraformaldehyde) for 30 minutes at room temperature. After the fixation, the samples are rinsed with PBS for 3 minutes. The following step is immerse the sample in a 990µl PBS 990ul PBS, 10ul of Triton X -300 solution containing the phaloiding reagent and incubate overnight at 37ºC in a enviromnent with 95% humidity and 5% CO_2. A second PBS rinsing for 3 minutes should follow. Then the sample is exposed to a solution containing 1ml of PBS with 5 µg/mL of DAPI for 15 minutes. The last step of the protocol before visualization with the THUNDER Leica microscope is rinsing again with PBS.

3.5.6. Mitochondrial Activity (MTT)

The MTT assay is a method that measures cellular metabolic activity. It uses a chemical compound, 3-(4,5-di**M**ethyl**T**hiazol-2-yl)-2,5-diphenyl**T**etrazolium bromide, which gets reduced to purple formazan crystals by the mithocondrial dehydrogenases. This provides information on levels of cytotoxicity in cells. A higher level of citotoxicity involves the decrease in the dehydrogenases production, thus indicating cellular damage or death [134]. In this work, 350µl of reagent was used in a 350 µl DMEM medium without BFS or antibiotics to avoid absorbance from this chemical compounds. 15 wells were used during this test: 5 negative control with dead cells, 5 positive control with alive cells in the well and 5 with cells and the samples. For each measurement, 3 replicates of 100 µl was used for esxtracting statistics. Measurements at 12h and 72h were performed.

4

Process Exploration for Device Selection: Results and Discussion

This section presents the results obtained during the technology exploration process. The growth of graphene on thick substrates was explored, as well as the graphene transfer free procedure for graphene created on these thick substrates. The results obtained after patterning on thick molybdenum, graphene growth and posterios Mo etch thereafter are also presented.

4.1. Thin Graphene Grown on Thick Molybdenum

Three different molybdenum thicknesses were used to create thin graphene. While the growth mechanism of thick graphene (MLG) is mediated by thin catalyst (50-70 nm Mo, [42, 100]), it has been demonstrated that thin graphene can be synthesised considering thicknesses larger than the micrometre range [135]. To explore thin graphene formation, in this work CVD graphene growths have been performed considering wafers with 500 nm, 800 nm and 1µm Mo sputtered layers. Greater thicknesses would pose challenges in managing the molybdenum etching process and would complicate the transfer-free graphene transfer process. Additionally, thicker layers could introduce stress within the material due to the interaction between the silicon substrate and the metal layer. In order to compare the graphene growth, the same CVD parameters were used for the three thicknesses.

Figure 4.1 shows the normalized Raman spectra, with respect to the G peak, obtained for graphene grown on a 500 nm Mo substrate on top of a 300 nm SiO_2 layer. As can be seen, the I_{2D}/I_G ratio is ≈ 1.3. Usually, a I_{2D}/I_G > 1 is characteristic of thin graphene, consisting of few layers [106]. A single 2D peak can be depicted from the spectra, with a $FWHM_{2D}$ is 55.1 cm^{-1}. At the same time, its appearance in the spectrum as a single 2D peak and not a combination of these suggests that the graphene obtained is turbostratic [103, 136, 137]. A I_D/I_G of 0.40 indicates the presence of defects on the graphene.

Figure 4.2 shows the normalized Raman spectra obtained after transferring the graphene grown on a 800 nm Mo catalyst. Presenting a I_{2D}/I_G ratio of ≈ 0.95, a $FWHM_{2D}$ of 55.3 cm^{-1} and a I_D/I_G of 0.37, the graphene obtained can be considered similar to that obtained for the 500 nm Mo. It is important to highlight that the scooping process for this wafer was challenging, as the graphene produced tended to break into very small fragments. This suggests that the graphene collected might have originated from regions further away from the center of the wafer, where the catalyst layer could be slightly thinner than anticipated.

Considering CVD graphene grown on 1µm Mo, Figure 4.3.a presents two representative, normalized Raman spectra obtained from graphene on Mo and transferred graphene to a 90 nm SiO_2 wafer. In this case, however, differences could be observed in the spectrum of graphene compared to graphene grown at 500 nm Mo. Not only a higher I_{2D}/I_G ratio is observed, with a value of ≈ 1.8, but also a much narrower $FWHM_{2D}$ of 41.3 cm^{-1}, being these values more close to thinner graphene layers [103, 136]. Additionally, graphene was less defective, preseting a I_D/I_G of 0.25. In this case, the thin graphene layer was also very susceptible to cracking, making the scooping process particularly challenging. Besides the challenges encountered during the scooping process, the creation of very thick layers on silicon wafers posed another limitation. The stresses generated in the material during the Mo sputter-

ing process can lead to delamination of the metal layer itself (see Figure 4.3.b). This phenomenon was encountered by attempting 1 µm Mo deposition on a second Si wafer. These stresses can also affect the growth of graphene. A possible way to decrease the stress generated during the PVD would be to increase the temperature of the physical vapour deposition process, with values even higher than half of the melting point of the material [138]. However, this is not an option for the Trikon Sigma, as it only reaches temperatures of ≈ 400°C, which is far below molybdenum's melting point of 2600°C, making it an unsuitable solution. One should note that, if the stresses generated during the PVD process are too high, the layer can be delaminated even before being able to perform the CVD process.

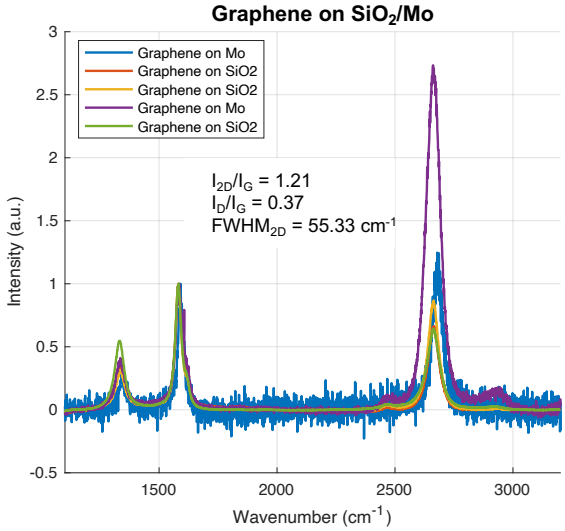

Figure 4.1: Normalized Raman spectra of graphene obtained after a CVD process on a wafer with a 500 nm layer of Mo. Spectra were acquired before (on the Mo) and after transferring the graphene to a wafer with 90 nm of SiO_2 using the scooping method. Spectra are representative. I_{2D}/I_G, I_D/I_G and $FWHM_{2D}$ are average values.

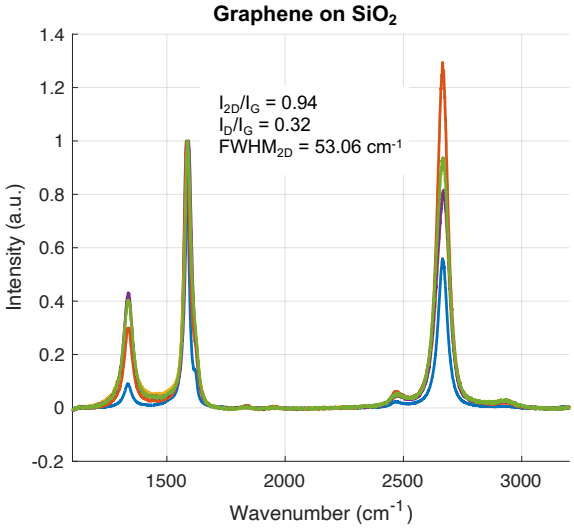

Figure 4.2: Normalized Raman spectra of graphene obtained after a CVD process on a wafer with a 800 nm layer of Mo. Spectra were acquired after transferring the graphene to a wafer with 90 nm of SiO_2 using the scooping method. Spectra are representative. I_{2D}/I_G, I_D/I_G and $FWHM_{2D}$ are average values.

Raman observations are indicative of a thin graphene. However, a more comprehensive study must include AFM and OT measurements to draw conclusions. For this reason, AFM was also to characterise the sample transferred to SiO_2 from the 800 nm catalyst. Figure 4.4.a shows a 5x5 µm^2 AFM image obtained at the edge of the transferred sample after performing a second order polynomial fit and image

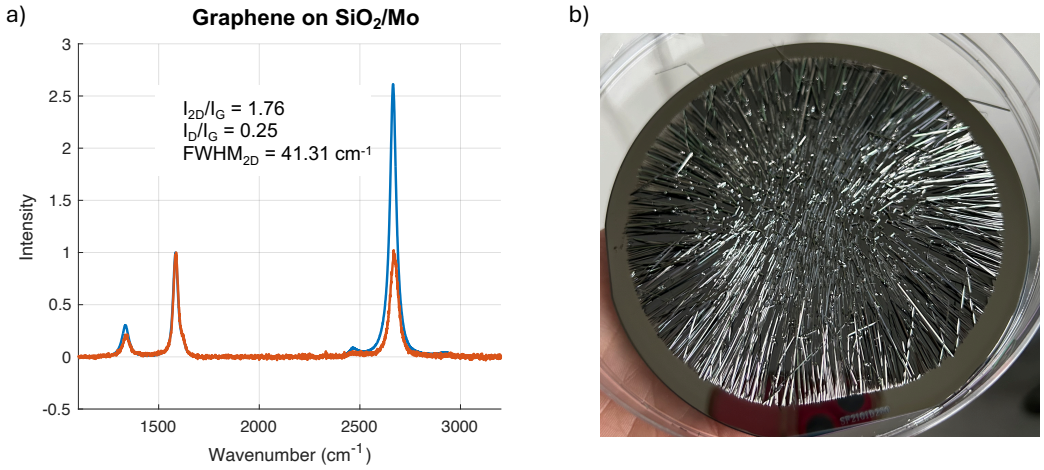

Figure 4.3: a) Normalized Raman spectra of graphene obtained after a CVD process on a wafer with a 1µm layer of Mo. Spectra were acquired before (on the Mo) and after transferring the graphene to a wafer with 90 nm of SiO_2 using the scooping method. Spectra are representative. I_{2D}/I_G, I_D/I_G and $FWHM_{2D}$ are average values. b) 1µm Mo layer sputtered on top of Si. Stresses created during PVD process generated the delamination of the metal layer.

filtering using Gwyddion. Figure 4.4.b illustrates the height topography considering both the vertical and horizontal lines depicted in blue within the AFM image. The thickness of the graphene is derived with reference to the step that creates its edge with SiO_2. From this, it can be deduced that the thickness of the graphene is 3.8 nm. This is thicker than what is usually reported in literature for FLG grown on Cu [139]. However, one should note that AFM measurements can be susceptible to errors due to various factors, including the properties and condition of the AFM tip and the specific measurement environment, among others, which can affect resolution and accuracy [112]. The AFM measurement was conducted several weeks after the transfer process, and the sample had been exposed to the environment multiple times prior to the measurement. This exposure led to the adhesion of some particles on the sample, which were subsequently filtered out using Gwyddion software. As a result of all these conditions, while the AFM data provides an indication of the graphene's thickness, it does not allow for an accurate determination of the exact number of layers.

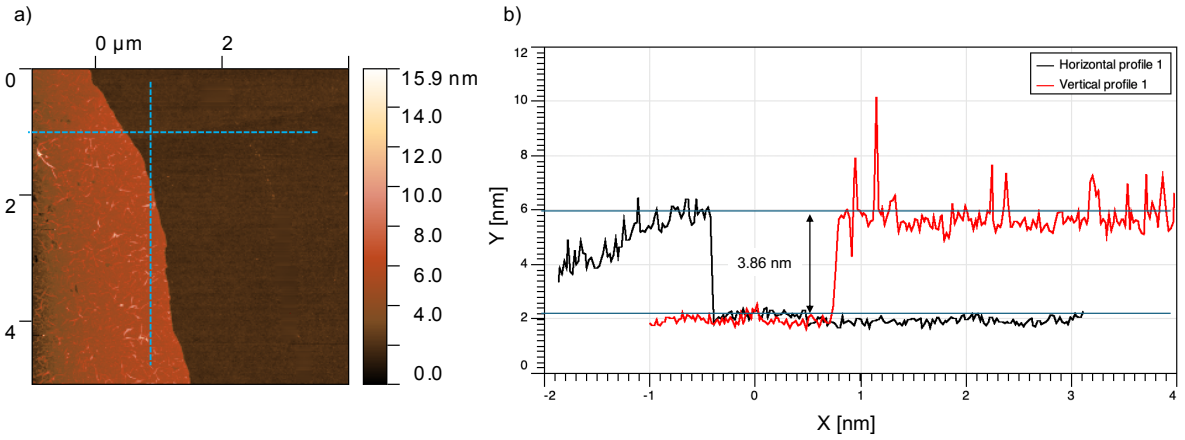

Figure 4.4: AFM profile obtained for a transferred graphene sample grown on a 800 nm Mo substrate. a) 5x5 µm² AFM image. b) Height profile obtained for the blue lines represented in a).

OT measurements were performed to complete the analysis of the graphene obtained at 800 nm Mo. Samples of graphene from the 800 nm Mo wafer were scooped into glass large enough to be able to perform these measurements. A graphene sample coming from the centre of the wafer, where the thickness of the catalyst is expected to be 800 nm Mo, was scooped, as well as graphene from the edges of the wafer, where the amount of catalyst is lower. It is worth mentioning that the graphene in the centre

was evidently thinner (named FLG) and more fragile than the graphene at the edges (named MLG). Figure 4.5 shows the OT measurements obtained for thin and thick graphene on glass. The contribution of the glass was susbtracted from both measurements. OT values for 550 nm were compared. The difference of ≈ 20% makes the difference in material evident. Using the formula provided by Zhu et al. [108], the number of calculated graphene layers for the thin graphene sample is ≈ 5. For MLG the number of layers obtained using the formula is ≈ 16. It is important to note that the formula was originally derived for graphene grown on copper (SLG) and nickel (MLG), and that graphene synthesised by these catalysts has been studied more extensively than in the case of molybdenum.

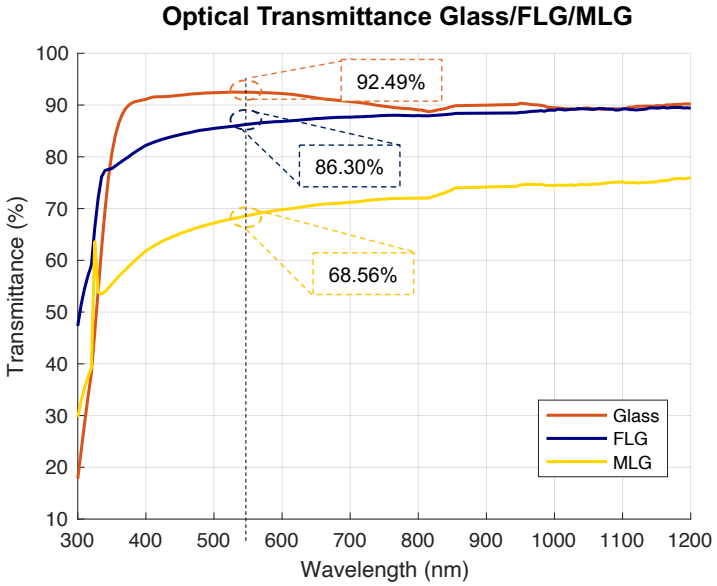

Figure 4.5: OT measurements obtained for a graphene sample created on a 800 nm Mo catalyst transferred to glass.

The growth of graphene on Mo thick substrates is limited by the catalyst thickness, which acts as a bulk reservoir for the carbon atoms. As explained in Section 2.2.2, the carbon atoms must first diffuse into the substrate to form Mo_2C, which is responsible for graphene nucleation. As a thicker catalyst, the C atoms have more material to diffuse before creating Mo_2C, so graphene formation is limited by diffusion [140]. Therefore, during the cooling phase, the Mo_2C layer created between graphene and the bulk Mo limits the carbon atoms precipitation to the surface [141]. As demonstrated also by the experiments discussed in this section, this process results in the formation of thinner graphene layers. Although determining the exact number of graphene layers can be challenging, the combined data from Raman spectroscopy, AFM, and OT measurements indicate that the graphene fabricated on thick substrates are mainly few-layer graphene (FLG). This confirms the possibility of successfully synthesizing this type of graphene in the cleanroom where this project is developed. While the process results in thinner graphene with fewer defects, using 1 µm of Mo as the catalyst presents a significant challenge due to the high internal stresses it generates. Additionally, for transfer-free processes, removing such a thick catalyst layer proved to be a difficult task.

The next key questions to address are: Can this thin graphene be effectively patterned? And, can it be subjected to a transfer-free process?

4.2. Exploration of Transfer-free Processes for Thin Graphene

This section shows the results obtained for each of the approaches followed in order to synthesise patterned FLG by a transfer-free process.

4.2.1. Catalyst Patterned Before Graphene Growth

As mentioned, the creation of good quality multilayer graphene has been successfully done in the cleanroom [101]. The typical procedure involves depositing a thin layer of Mo, typically 50 nm, on a SiO_2 substrate. After deposition, the Mo is patterned, taking into account the desired graphene

structures. After patterning the metal, the CVD graphene creation process is performed. The same procedure was carried out considering a thickness of 500 nm Mo, i.e. x10 times the thickness usually used for fabricating the MLG. A mask with different 2D shapes was used for this purpose. Graphene structures were characterised with Raman, EDX and SEM. Samples were exposed to H_2O_2 for a period of $\approx$ 20 min without suffering delamination.

Figure 4.6 shows SEM images obtained after performing the Mo wet etching step. Brighter areas were observed on the edges of the structures (marked with arrows in the image as examples). Considering these images, the fabricated material seems to be thick. In addition, the presence of apparent small holes indicates the possibility of having a material with high amounts of defects. EDX analysis confirmed the absence of molybdenum at the edges (see Figure 4.7). Accordingly, the phenomenon of the edges was termed *'the carbon fences phenomenon'*, where an accumulation of carbon atoms occurs.

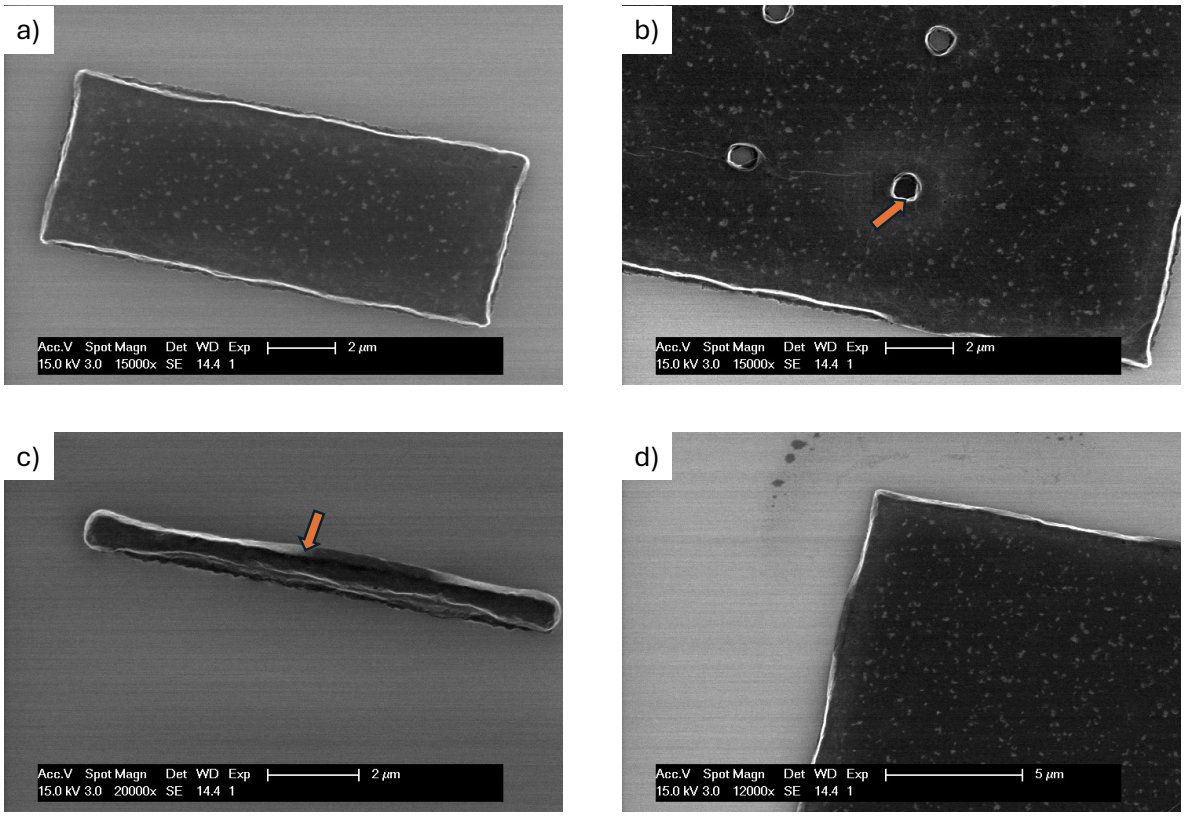

Figure 4.6: SEM images obtained on graphene grown on a pre-patterned 500 nm Mo substrate. Cabron fences are pointed out with orange arrows.

Raman analyses were obtained to provide a more complete analysis of the material obtained. Figure 4.8 shows some of the Raman spectra obtained for several of the graphene structures on SiO_2 obtained during this process. The first major observation is that the I_{2D}/I_G ratio is 0.5, which is significantly lower than that observed in graphene synthesized on a 500 nm Mo substrate without any prior patterning. In addition, a much more pronounced D peak is also observable, resulting in an average I_D/I_G ratio of 0.85, confirming the presence of high amount of defects in the material. A $FWHM_{2D}$ of 64.23 cm^{-1} was obtained, being this value wider than the obtained for the FLG described in the previous section. Given that the 2D peak has a more single peak appearance and is not much wider, it can be depicted that the graphene obtained is turbostratic.

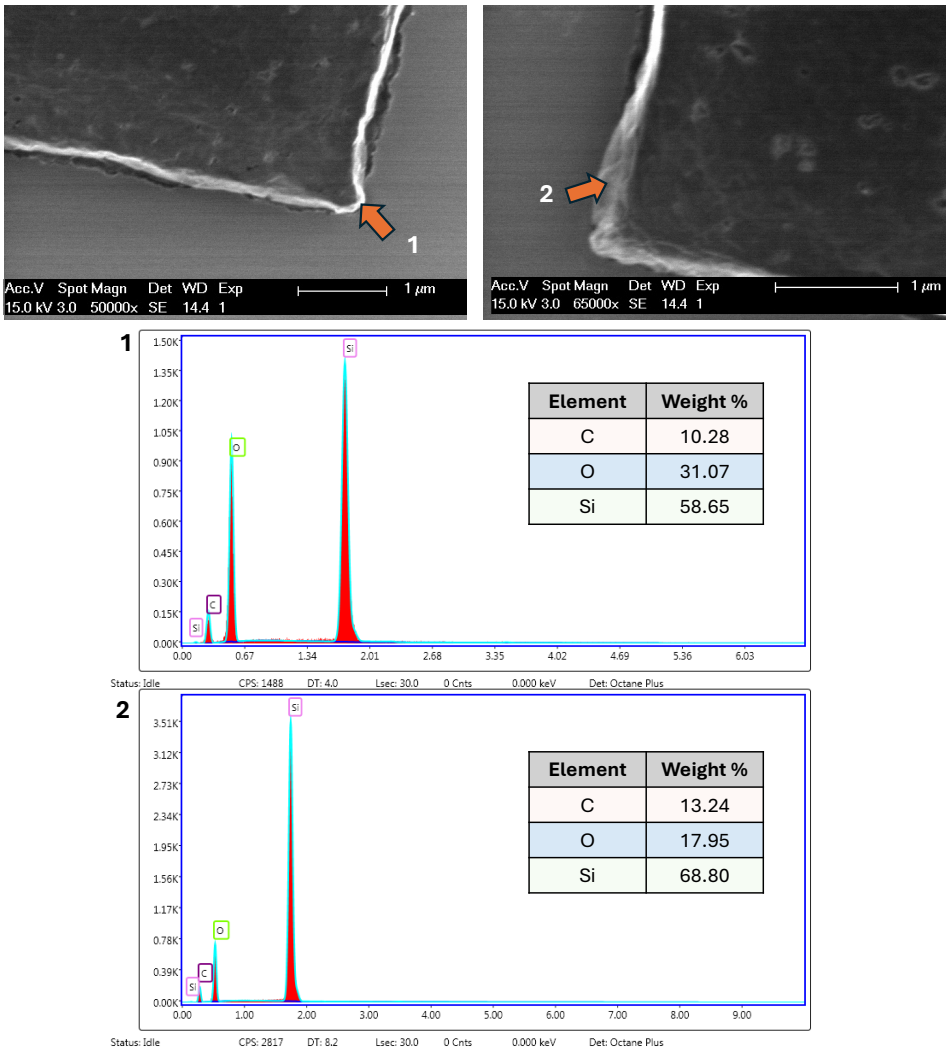

Figure 4.7: EDX analysis extracted on the edges of graphene fabricated on patterned 500 nm Mo strctures, confirming the absence of molybdenum at the edges after performing Mo wet etch.

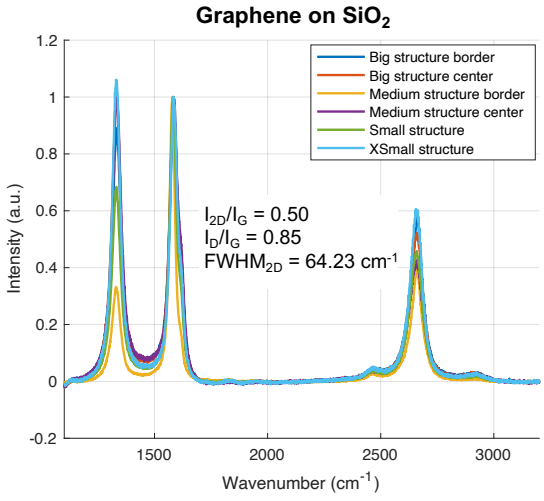

Figure 4.8: Raman spectra obtained for a transfer-free graphene on SiO_2. Graphene was grown after patterning different 500 nm Mo structures. I_{2D}/I_G, I_D/I_G and $FWHM_{2D}$ are obtained for the average of spectra values.

The combination of these characterization results, along with the absence of delamination after extended etching, suggests that the obtained material is multilayer graphene (MLG) with numerous defects. This indicates that the method of patterning thick molybdenum before growing graphene is not suitable for fabricating patterned, transfer-free few-layer graphene (FLG). A possible evidence-based explanation for the results is proposed below.

Cabrero et al. [140] proposed a model for graphene growth on thick transition metals, where graphene growth results from the combination of three main fluxes (see Figure 4.9.a). J_I is the carbon flux due to precursor impingement and dissociation, which occurs on the surface of the catalyst; J_D is the carbon diffusion flux through the catalyst; and J_G is the graphene feeding flux, being the last one defined as $J_G = J_I - J_D$. Graphene growth can occur by isothermal growth (surface process) or by precipitation of the carbon during cooling down. Figure 4.9.a shows a schematic representation of the isothermal growth process, mechanism that seems to be the main responsible of graphene growth in unpatterned, thick Mo substrates. Since the thick Mo acts as a carbon reservoir, J_D keeps high while the CVD process, limiting graphene feeding flux.

Additionally, two possible scenarios can be considered for a thick catalyst. One particular scenario may consider the coexistence of Mo_2C and Mo when the carbon precursor is removed and the cooling starts. In this case, as the substrate is not yet considered saturated and there is still Mo left to form Mo_2C, the C atoms that were diffusing into the Mo would interact with the Mo itself just below the Mo_2C interface. The carbon atoms would therefore contribute to the enlargement of the Mo_2C and not to the precipitation or formation of graphene [141], resulting in a thinner graphene. Provided that the CVD process is short enough so as not to saturate the Mo, on thick substrates graphene growth could be mainly mediated by isothermal growth, resulting in thin graphene (FLG, and potentially SLG). Another scenario considers that all the thick, bulk Mo has been transformed into Mo_2C during the CVD process, but the carbon atoms still diffuse into the material as the large thickness of the carbide is still considered as a bulk reservoir. In this case, the precipitation of carbon atoms during the cooling down can be limited by the slow diffusion due to the thickness of the catalyst, limiting the graphene growth by the precipitation process. In both scenarios, the result is a graphene growth potentially mediated by isothermal growth. It should be noted that the catalyst/substrate interface, in this case Mo_2C/SiO_2, can also play a role on C diffusion and therefore graphene growth.

Figure 4.9.b shows a schematic representation of two processes considering thick molybdenum sputtered on a Si wafer, where the dimensions of the Mo catalyst are d_x, d_y and d_z, d_z being 500 nm Mo. Process 4.9.b1 considers an unpatterned catalyst process, where $d_z <<<< d_x \approx d_y$. In this case, only the top of the structure is considered to be exposed to the carbon based gas, acting this surface as the source of carbon atoms for the bulk material and being J_I and J_D therefore dependent only on the top plane. The phenomenon that occurs in this scenario is the explained before, resulting in a FLG, as was also confirmed by the first set of experiments explained at Section 4.1.

A different scenario seems to occur when thick molybdenum is patterned before the CVD of graphene, where the Mo dimensions are $d_z < d_x \approx d_y$. In this particular scenario, the top plane and four other planes are considered as the source of carbon atoms. Through each plane, carbon atoms can impinge, dissociate and diffuse (similar to what is shown in Figure 4.9.a; now considering five planes instead of a unique one). This generates the saturation of the substrate with carbon atoms, causing $J_D \approx 0$, and $J_G = J_I$. Isothermal growth occurs therefore at all five planes. Additionally, the substrate will saturate with carbon atoms since the carbon atoms have five planes through which to access the bulk material, allowing the precipitation process to also be considered as a graphene generation process. The number of graphene layers generated (and consequent carbon accumulation) is higher on the surface of the planes related to the d_z dimension, phenomenon that is attributed to the smaller size of these planes, which results in a greater/faster degree of carbon saturation on the areas close to the surface compared to the larger d_y x d_x plane (top plane). Overall, this is the mechanism proposed to explain the generation of carbon fences in patterned, thick molybdenum substrates. It should be noted that further analysis and testing by varying CVD recipes should be taken into account to support this theory.

The reader should note that MLG fabricated on patterned thin Mo catalysts (50 nm) can delaminate from the substrate during Mo etching, so the etching is usually limited to about 5 minutes for complete removal of thin Mo. However, with patterned, thicker Mo catalysts (500-800 nm), longer etching times ($\approx$ 20 minutes) are needed for complete removal. In these cases, graphene did not delaminate. This stability was attributed to a large amount of carbon at the edges, which acts as an anchor, helping the MLG adhere to the substrate during the extended etching process.

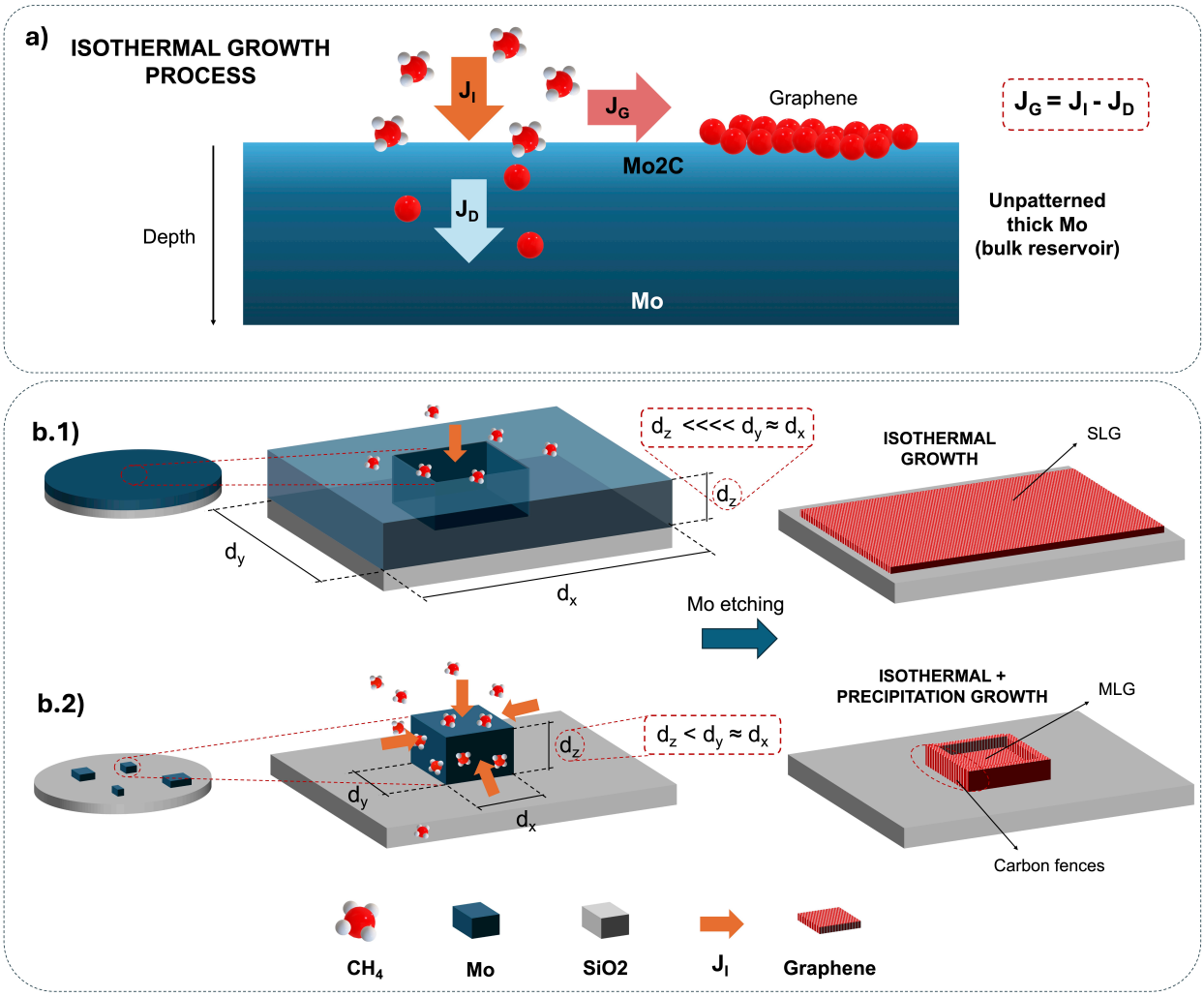

Figure 4.9: Schematic representations of graphene grwoth on a thick molybdenum catalyst. a) Graphene synthesis mediated by isothermal growth on a transition metal catalyst. Adapted from [140]. b.1) Graphene growth on a non-patterned thick Mo substrate, where the thickness d_z is several orders of magnitude smaller than d_x and d_y. b.2) Graphene growth on a patterned thick Mo substrate, where the thickness d_z is only one or two orders of magnitude smaller than d_x and d_y.

4.2.2. Catalyst Patterned After Graphene Growth

As observed, performing the Mo pattern before growing graphene does not result in FLG and leads to the called *carbon fences* phenomenon. In contrast, graphene grown on an unpatterned substrate has shown better quality and characteristics. Therefore, an alternative method to achieve patterned, transfer-free FLG would be to first grow graphene on a flat, unpatterned substrate, performing the patterning of graphene and Mo afterward. This approach may help in obtaining high-quality, few-layer patterned graphene.

A wafer with 300 nm SiO_2 and 500 nm Mo was used. Graphene was grown and the photoresist was manually coated, exposed and developed. Once the photoresist was present, the wafer was exposed to 25 s of etching with O_2 plasma to etch the exposed graphene, followed by a DRIE of the molybdenum in the exposed area. Raman spectra were obtained before and after the etching to ensure that graphene was properly etched (see Appendix A, Figure A.1). After removing the photoresist, wet etching of the thick molybdenum was attempted using H_2O_2. The first samples showed delamination after 10 minutes of etching, so the etching time was reduced to 7 minutes. Figure 4.10.a shows a SEM image of a structure after performing 7 mins of wet etching. Molybdenum is still present under graphene, as confirmed by EDX (see Appendix A, Figure A.2). In particular, only 115 nm of Mo was etched in the 7 minutes (see Appendix A, Figure A.2). Additionally, Raman confirmed that the graphene was still intact on the molybdenum. Figure 4.10.b shows the I_{2D}/I_G ratio obtained for 25x25 µm^2 inside

the structure. Ratio values from 0.9 to 1.6, together with a high delamination rate, confirm that the graphene obtained is thin, having few layer characteristics.

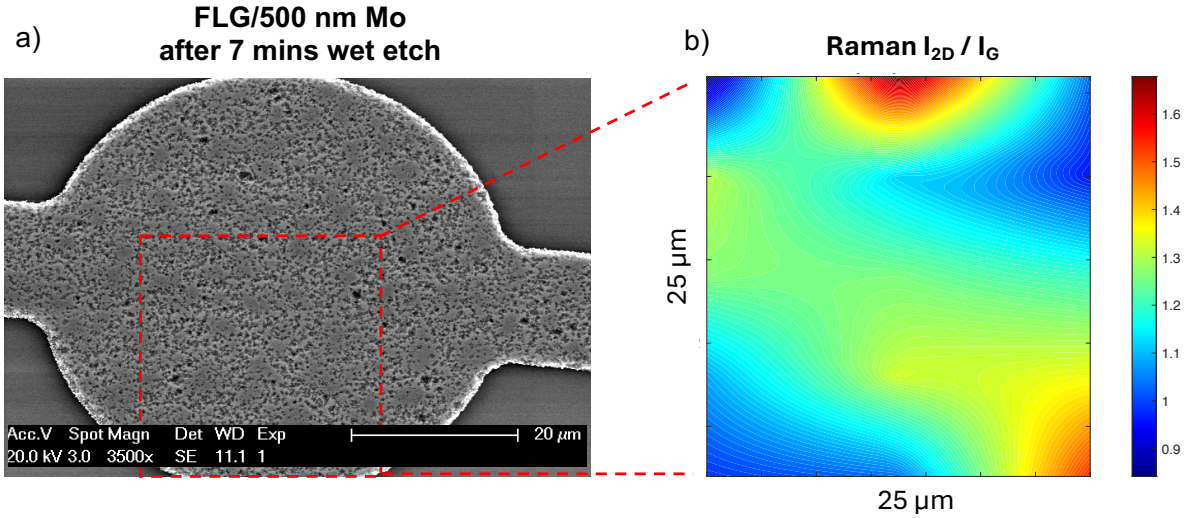

Figure 4.10: a) SEM image of a graphene/Mo structure patterned after graphene growth, after 7 minutes of wet etching to remove the Mo underneath. Molybdenum can still be noticed. b) Raman I_{2D}/I_G ratios of a mapping performed inside the strucutre.

In order to remove the ≈ 400 nm Mo underneath the graphene, an alternative approach was used: a combination of wet and dry etching. Following the 7 minutes of wet etching with H_2O_2, molybdenum and graphene were exposed to a SF_6 RIE process for 25 minutes. Figure 4.11 shows the SEM images of the structures resulting after the dry etching. As can be seen, the carbon fences are not present, as expected. Additionally, according to the Raman spectra, the graphene layer obtained can be considered thinner than the obtained patterning the Mo before the CVD process. However, graphene is damaged, as was later confirmed by Raman, obtaining a very pronounced D peak (see Apendix A, Figure A.3). Additionally, EDX measurements confirmed the absence of Mo (see Apendix A, Figure A.3).

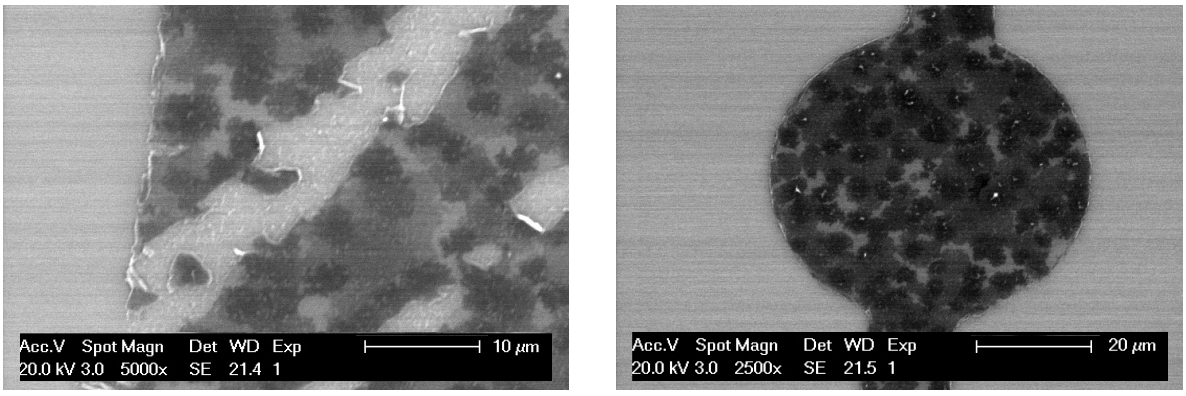

Figure 4.11: FLG after exposure to 25 mins of SF_6 to dry etch the molybdenum underneath.

The dry etching method proved to be highly detrimental to the graphene, leading to significant damage. Additionally, the required etching time for thicker molybdenum layers is excessively long, raising concerns about the integrity of other structures during the process considering the scenario of applying this process to a potential fabrication flowchart. FLG created through this process was also delaminated when it came into contact with DI water, which would have make testing its electrochemical properties in saline media extremely challenging.

The pattern-after-growth method can stil be an option to consider for devices with on flexible polymeric substrates. A flowchart detailing the steps for using this method to create FLG transfer free

flexible transistors is proposed in Chapter 7. However, for this particular MSc thesis work, it was concluded that the short-term feasibility of creating FLG together with MLG would be challenging.

4.3. Graphene Growth on Variable Step Heights Molybdenum

Wafers with 500 nm Mo were patterned, considering a 200 nm step height in the bulk Mo. The SEM image presented in Figure 4.12.a shows a Mo structure after performing both Mo patterns, without graphene. Once the pattern were created, CVD graphene was grown using the same recipe as in the previous processes and the Mo underneath was etched using H_2O_2 during $\approx$ 20 minutes. No extreme delamination was experienced, indicating that the graphene was thick. Figures 4.12.b, 4.12.c and 4.12.d show SEM images of graphene structures after performing the Mo etching. Carbon fences phenomenon at the edges of the structures is observed (see Figure 4.12.d). Initially, it might appear that the graphene maintains the shape of the catalyst. However, a topography analysis using AFM showed how the differences were mostly in material roughness but not in overall thickness (see Figure 4.12.e). AFM also confirmed the presence of carbon fences (see Figure 4.12.f). EDX confirmed the absence of Mo (see Apendix A, Figure A.4). Figure 4.12.g shows the Raman obtained for these type of structures. According to them, graphene shows similar characteristics to the graphene obtained during the "pattern before growth" process, explained in Section 4.2.1, with a I_{2D}/I_G ratio of 0.61, related to more MLG spectrum. Additionally, the amount of defects is considerable, considering the I_D/I_G ratio of 0.48. The $FMHW_{2D}$ is 61.56 cm^{-1}, and the shape of the 2D peak indicate that is turbostratic.

Results show that graphene obtained at different molybdenum heights shows no evident difference in the thickness (hence no difference in the number of layers). However, graphene obtained from the higher Mo areas seems to have different roughness properties compared to the graphene created in the lower Mo areas. This may be due to the way the carbon atoms interact with each of the Mo surfaces. The surface of the lower Mo area (the 300 nm Mo step) has been exposed to the SF_6 gas, which generates a surface with more irregularities than the one initially considered (bulk zone surface of the 500 nm Mo). This can lead to differences in graphene growth, as the way C atoms interact with the surface depends on the Mo surface properties. Further study of molybdenum surface properties after performing SF_6 dry etching, before and after graphene growth, should be performed to confirm this hypothesis. Overall, this procedure cannot be considered as a method for producing graphene with varying numbers of layers. Further investigation is needed, focusing on homogeneous, dense uniform Mo patterns to understand how graphene collapses after the etching of a corrugated Mo surface.

4.4. Summary of Process Exploration for Device Selection

Several conclusions can be drawn from the results shown in the previous sections.

- It is possible to create thin grafene by tuning the catalyst parameters. 500nm, 800 nm and 1µm Mo give thinner graphenes compared to graphene generated with 50 nm Mo. 1 µm Mo seems to give the thinnest graphene, but the thickness of this catalyst would compromise the integrity of the catalyst layer itself and the graphene transfer-free process.
- Performing the pattern of a thick catalyst completely changes the mechanism of graphene growth, resulting in multilayered graphene and the generation of the *carbon fences phenomenon*.
- Patterning the graphene after growth seems to keep the few-layer graphene properties and eliminates the *carbon fences phenomenon*. However, a transfer-free approach considering SiO_2 as final substrate is particullarly challenging for this type of material due to the process of etching the bulk Mo under the graphene.
- Patterning a bulk Mo substrate is possible. However, while the graphene created at different step heights has different properties in terms of roughness, there was no obvious difference in the number of layers (thickness) of the graphene. Therefore, this process cannot be considered for creating graphene with different thicknesses on the same die. Further testing is needed considering corrugated Mo patterns to understand how graphene would collapse in that particular scenario.

Considering all these outcomes, it was determined that working with tranfer-free FLG in SiO_2 was going to be challenging consdiering the duration of a MSc thesis. Therefore, the decision was made to work with thin catalysts (e.g., < 500 nm Mo) and focus on the corrugated electrode design approach.

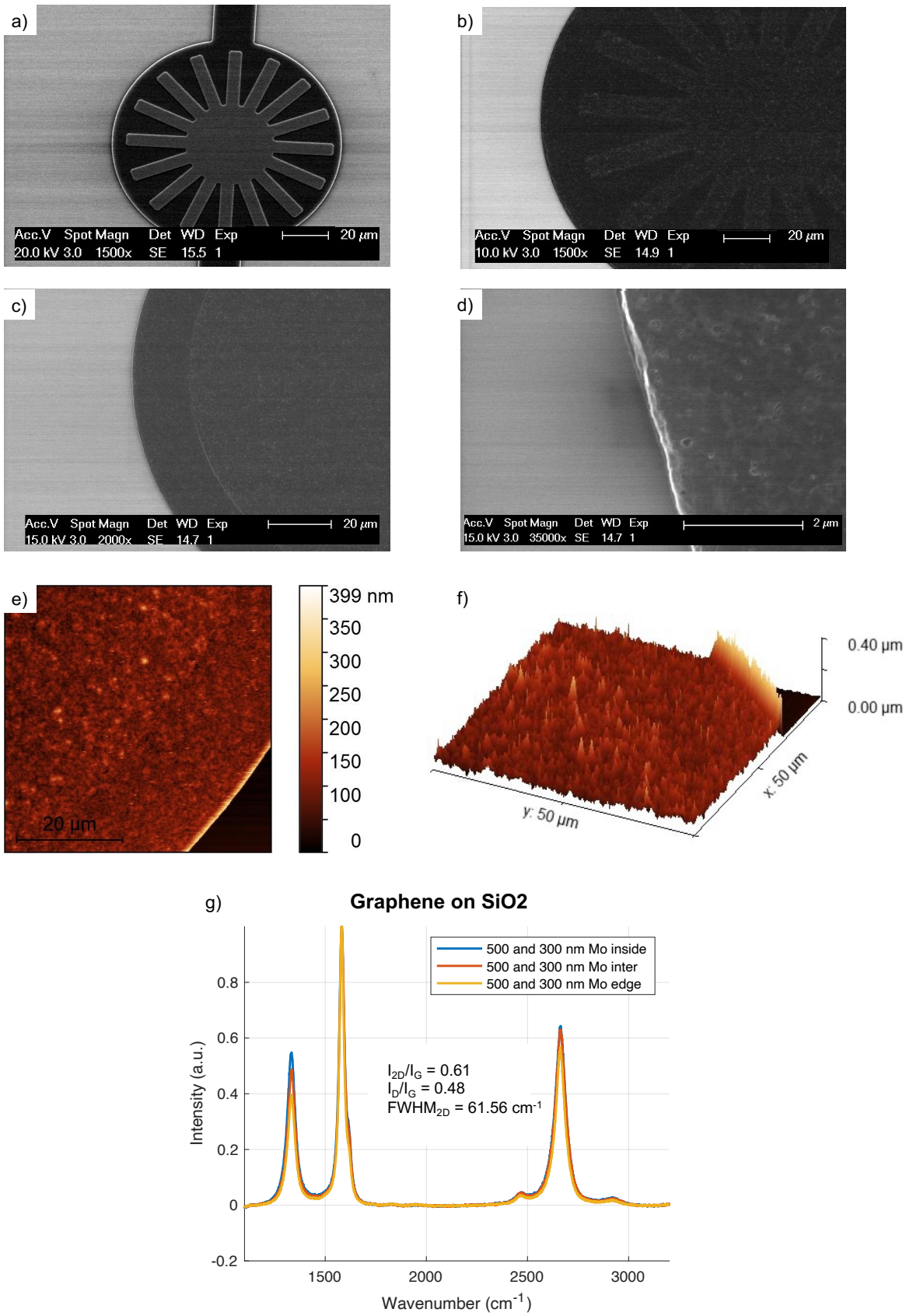

Figure 4.12: a) SEM image of a 500 nm Mo structure patterned. Step height: 200 nm Mo. b), c), d) SEM images of graphene after Mo etching. e) AFM image of the structure shown in c). f) 3D representation of the AFM topography. g) Raman spectra obtained for different points of the graphene structures on SiO_2.

5

Corrugation Process Optimisation: Results and Discussion

Developing a defined flowchart requires an understanding of the phenomena that affect each of its steps. In order to have a complete understanding, it is essential to investigate parameters such as the most suitable substrate for creating corrugation patterns, the properties of the synthesized graphene, and how various factors (such as mask contact mode, UV exposure time, step height, and etching methods) affect the outcome. This chapter shows the results obtained during the manufacturing process optimisation for the fabrication of corrugated graphene structures.

5.1. Corrugation Patterning

As discussed in Section 3.3.2, two different approaches to create the corrugation patterns were considered. Figure 3.7 shows the procedures used to create the two types of corrugation structures (in Mo and in SiO_2). In this section, the results and discussion obtained for each process are presented. Additionally, the corrugation patterning process performed with the contact aligner with the mask MO CORR had to be subjected an optimisation process. Since the resolution limit of the contact aligner is 1µm, it was initially considered to perform the lithography of this step using a hard contact mode to avoid light scattering and to generate the 1µm patterns as accurately as possible. However, whenever hard contact exposure was attempted, the photoresist remained stuck to the glass mask (see Appendix A, Figure A.5.a), making this contact mode not suitable. The extreme adhesion of photoresist to the mask can be attributed to the irregular contact zones generated by the small, dense corrugated patterns, increasing friction and local adhesion, which can make separation after exposure challenging. For this main reason, soft contact mode was selected. The proper exposure time for soft contact mode was determined to be 6.5 s. However, due to the resolution limit, 1µm squares result in circles (see Appendix A, Figure A.5.b). Furthermore, considering the S0101 patterns the light interacts with the structures creating a more abstract shape (see Appendix A, Figures A.5.c and A.5.d). As the structure preserves regularity, it is still considered suitable for this study. All other patterns were adequately resolved and patterned.

5.1.1. Corrugation on Molybdenum

From the experiments conducted and analysed in Section 4.3 one can expect that graphene will not have different thicknesses if it is created in a Mo bulk patterned with steps on the order of nanometers. However, generating homogeneus, repetitive and dense patterns in the molybdenum might provide differences in the way graphene collapses after Mo removal with H_2O_2. Samples containing 500 nm Mo catalyst on top of SiO_2 were patterned, generating corrugated patterns of 200 nm height in the bulk molybdenum. Mo was etched using H_2O_2 after performing the CVD of graphene. Graphene created on the structures containing 1µm lines and 1µm separated collapsed slightly following the lines patterning, as can be seen in Figure 5.1.a which shows an AFM image of the structure together with the graphic representation of the topography. However, the height of the structures was encountered to be 63 nm as maximum, when structures with height on the order of hundreds of nm were desired. Considering

the remaining structures, the result obtained was the same as in Section 4.3, with no obvious change in the way graphene collapses but observing differences in graphene roughness properties (see Figure 5.1.b, and Appendix A, A.5.e and A.5.f).

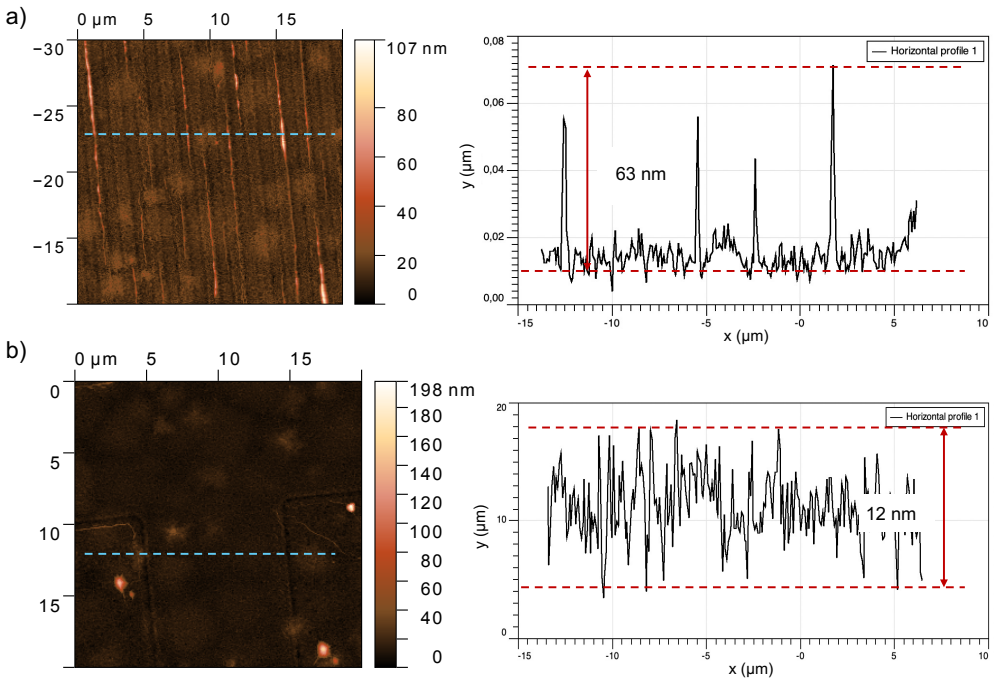

Figure 5.1: AFM images and topography scanning for graphene obtained on corrugated Mo surfaces. 200 nm height structures were patterned on a 500 nm Mo bulk substrate before performing the graphene CVD. a) Graphene obtained after mo etching of 1µm wide lines, separated 1 µm structure. b) Graphene obtained after Mo etching of 20µm x 20 µm squares, separated 10 by µm structure.

Due to the inability to have homogeneous patterns in the order of hundreds of nm in height considering this approach, it was decided to change the scope and create the corrugated patterns in SiO_2. Research efforts were therefore focused mainly on developing the feasibility of this second option.

Nevertheless, in order to have some information about the synthesised graphene on patterned Mo, Raman was performed on some of the structures (see Appendix A, Figure A.6). Both I_{2D}/I_G ratio of 0.53 and the wide $FWHM_{2D}$ of 63 cm^{-1} reflect the multilayer characteristics of the graphene, and the I_D/I_G of 0.61 confirms the presence of defects in the material. The synthesised graphene appears not to be structure-dependent in case of performing the corrugation patterns on the Mo. Additionally, a metallisation tryout was performed for one of the wafers created during this process. Very few TLM structures survived metallisation, as the bulk molybdenum was 500 nm and the adhesion of the metal to this substrate is very poor (Mo etching is done after metallisation to avoid delamination of the graphene).

Sheet resistance values were extracted for some of the structures to determine the order of magnitude and to compare their value with the with the sheet resistance of the wafers in which the corrugation was made in the SiO_2. Rs values were obtained using the TLM procedure explained in Section 3.4.1. Graphic results, used to extract the sheet resistance values of the structures with a width of W = 300 µm, can be seeing in Appendix A, Figure A.7. The sheet resistance is between ≈ 300 Ωsq^{-1} and 800 Ωsq^{-1} (see Table A.1). It is considered relevant to compare the overall Rs range obtained for these structures with the range of sheet resistance values reported for graphene grown on corrugated SiO_2 substrates to understand if the permanent corrugated structures can influence the order of magnitude of the Rs. However, there is insufficient data to correlate the results with the corrugated Mo structures created in this section. The variations in the sheet resistance can be attributed to different factors such as differences in the location of the structures, differences in the roughness of the graphene and bad contact of the metal pads with the molybdenum, among others. This last reason can also be one of the causes of non-linearities and having contact resistances in the order of hundreds of ohms, when they should be close to zero since 4 probe measurements were performed (see Appendix A, Figure A.7).

5.1.2. Corrugation on SiO_2

Since patterning the Mo does not enable the graphene to retain a uniformly corrugated shape, the focus was shifted towards creating the corrugation on the SiO_2 substrate. This approach theoretically allows the graphene to preserve the substrate's shape after Mo etching, resulting in the formation of corrugated graphene structures. Several key aspects should be addressed to investigate the feasibility of creating corrugated graphene structures on SiO_2. Firstly, it was important to determine whether a continuous graphene layer could be successfully created. Another investigated aspect was the relationship between the amount of molybdenum used and the step size in the production process. The question is whether the amount of molybdenum must be precisely matched to the step size dimensions to ensure optimal graphene growth or whether variations in this relationship could still yield proper results. Additionally, the process of SiO_2 etching played a critical role in preparing the substrate for graphene deposition, so both dry and wet etching processes were performed. Finally, a significant part of the investigation focused on understanding whether variations in process parameters would lead to changes in the properties of the graphene.

Four batches were fabricated to explore and extract some statistics of the synthesis of graphene by varying the parameters discussed in Section 3.3.2. Table 5.1 provides an overview of some of the wafers used during the optimization process, along with the corresponding parameters applied. The initial SiO_2 thickness, SiO_2 etching method, structure height and Mo thickness were considered as the main parameters of variation. In addition, some patterns were made after graphene growth (graphene growth B.M.P; Before Molybdenum Pattern), although graphene growth was mainly considered after patterning the molybdenum (graphene growth A.M.P; After Molybdenum Pattern). The characteristics of the graphene synthesised in each wafer were evaluated by OM, SEM and Raman spectroscopy. Additionally, wafer 076 was used to perform TLM measurements in order to confirm the continuity of the graphene layer. The parameters used for the evaluation were the I_{2D}/I_G and I_D/I_G ratios, as well as the $FWHM_{2D}$ values. The outcomes from each batch can be found hereunder.

The majority of the exploratory work was conducted on batches 1 and 2. For each wafer, multiple Raman spectra were extracted considering diverse structures, and differentiating between the top and bottom of the structures. Similar structures were selected for comparison between wafers. Table 5.3 shows the **average** Raman ratios and $FWHM_{2D}$ obtained for each wafer considering specific structures, and differentiating both top and bottom areas of the structures. Additionally, Table 5.2 (and Figure A.8) shows the sheet resistance values obtained for some of the structures of wafer 076, proving graphene layer continuity. These measurements were solely performed to verify the continuity of the graphene layer; the evaluation of these range of Rs values will be conducted in Chapter 6, as the same range of Rs was observed for the wafers used to assemble the final devices. After analysing the results from these two batches, several conclusions were drawn:

- In order to consider correct isolation between graphene and silicon in the etched areas, it is more appropriate to consider an initial SiO_2 thicknesses of around 800 nm.
- In general, the Raman signal of the graphene synthesised on top of the structures shows characteristics of MLG (I_{2D}/I_G < 1), while the graphene synthesised at the bottom shows characteristics of thinner graphene (I_{2D}/I_G > 1). Additionally, I_D/I_G ratios are smaller in the bottom structures for some of the wafers, showing a less defective graphene in comparison to the top. This will be referred as the *top/bottom difference* phenomenon.
- It is not necessary that the step height and the amount of molybdenum are of the same thickness: continuous graphene can be synthesised considering SiO_2 steps of 300 nm and Mo thickness of 50 nm. This facilitates the wet etching process of molybdenum.
- Performing SiO_2 wet etching with BHF is a favourable etching method, providing rounded edges and more isotropic profiles, creating smooth transitions which is favourable for the metal deposition. In addition, using a wet bench eliminates dependencies on dry etching tools.
- When considering wet etch, as it is an isotropic process, in order to preserve the smaller structures (≤ 1 µm), the SiO_2 step size should be limited to about 300-350 nm.
- The test performed by making graphene growth before Mo patterning (wafer 18) showed the lowest values of I_D/I_G ratios and the lowest $FWHM_{2D}$, indicating a better quality graphene.

Batch 3 was fabricated after analysing the data from batches 1 and 2, considering a narrower range of parameters to obtain extract more statistics about the graphene growth and the *top/bottom differences* phenomenon. Two of the wafers from batch 3 were used for the assembly of the final devices, and one was used for biocompatibility tests (wafers 229, 231 and 239, orange in Table 5.1, presented in the same table for convenience. The properties of the graphene of these three wafers will be addressed in Chapter 6). Some of the wafers in this batch exhibited apparent photoresist residues; however, *top/bottom differences* phenomenon remained present in all cases. Compared to batches 1 and 2, the graphene in this batch appears to be thinner and of higher quality, as indicated by the Raman ratios and $FWHM_{2D}$ measurements. The wafers selected for the final devices and biocompatibility tests were residue-free, as will be shown in Chapter 6.

Figure 5.2 shows the box plot representation of the data obtain from the Raman spectra considering batches 1, 2 and 3, excluding the wafers used for final devices and biocompatibility. Figure 5.2.a represents the I_{2D}/I_G and I_D/I_G ratios for both top and bottom structures. Considering the I_{2D}/I_G ratio, there is a clear difference between top and bottom, with most of the ratio values being above 1 for graphene at the bottom. Comparing I_D/I_G, a smaller variation can be seen in the case of the bottom structures, as well as slightly lower values, indicating a graphene with fewer defects at the bottom. Analyzing this data clearly shows that the CVD process of graphene is directly influenced by the surface topography, and that this phenomenon occurs across a wide range of step heights and different combinations of Mo catalyst. This phenomenon might be caused by the combination of several factors, which are schematically illustrated in Figure 5.3.a. Process A shows a possible compression of the molybdenum grains as a result of the physical vapor deposition process in the constrained space of the valleys (or bottom of the structures). This compression might generate differences in the graing geometry and boundaries, limiting the carbon diffusion. Additionally, Process B represents the CVD process of graphene. In the top of the structures, the carbon atoms can diffuse through five different planes as in the case illustrated in Figure 4.9.b, while in the bottom there is a unique carbon source plane as a result of the geometrically confined molybdenum. In addition, if the CH_4 flux is affected by the topography, the bottom areas might be less exposed to the precursor gas. All these phenomena could lead to more controlled growth and less carbon available to form graphene at the bottom. As a result, top parts should have a propensity to generate a thicker and defective graphene, while the bottom parts will be prone to have thinner graphene with higher quality (see Figure 5.3.b). More research is needed to confirm this explanation.

Lastly, batch 4 was fabricated to test both SU8 as encapsulation layer and understand if the step height plays a role on the *top/bottom differences* phenomenon (see Table 5.1 to see the wafers characteristics). This batch initially consisted of 4 wafers, however two broke during testing. The remaining two wafers also exhibited the *top/bottom differences* phenomenon, and as they were free of residues they were used for biocompatibility testing. Their characteristics will be shown in Chapter 6.

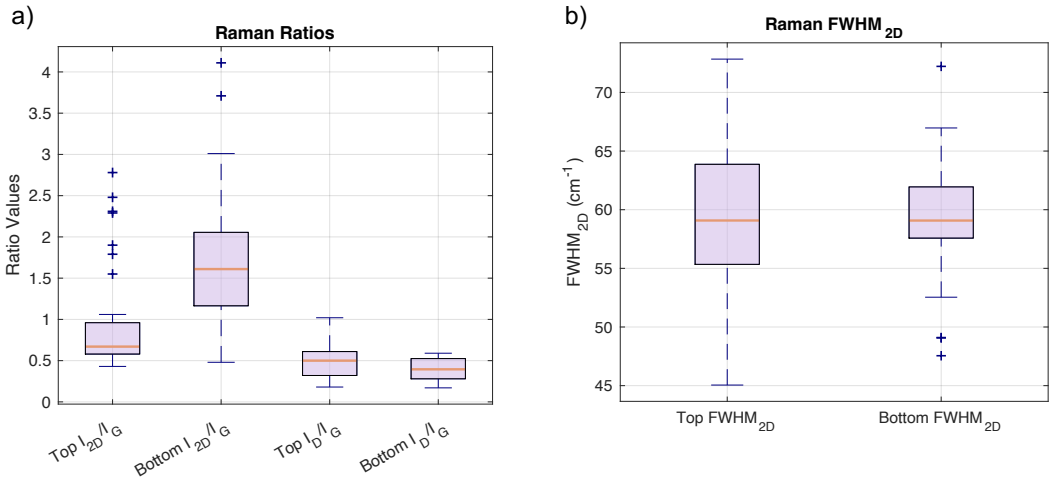

Figure 5.2: Visual representation from Table 5.3 data. For each group, n = 34. a) Box plot representation of I_{2D}/I_G and I_D/I_G ratios for both top and bottom structures. b) Box plot representation of $FWHM_{2D}$ for both top and bottom structures.

Table 5.1: Summary of the wafers and parameters fabricated during the optimization process. Wafers 229, 231, 239, 188 and 189 were considered for Chapter 6. For convenience their characteristics are presented here.

Batch	Wafer	Initial SiO2 thickness (nm)	Etching method	Structures height (nm)	Mo thickness (nm)	Graphene growth	Metallisation	Encapsulation
1	7	500	DRIE (Drytek)	208	200	A.M.P	100 nm Ti + 650 nm Al	PR
	9	500	Wet (BHF)	288	50	A.M.P	NA	PR
	10	500	Wet (BHF)	400	50	A.M.P	10 nm Ti + 200 nm Au	PR
	11	500	Wet (BHF)	288	300	A.M.P	100 nm Ti + 350 nm Al	PR
2	13	860	DRIE (Oxford Polaris)	377	300	A.M.P	100 nm Ti + 350 nm Al	PR
	16	860	DRIE (Oxford Polaris)	108	100	A.M.P	10 nm Ti + 200 nm Au	PR
	18	860	Wet (BHF)	400	500	**B**.M.P	10 nm Ti + 200 nm Au	PR
	076	800	Wet (BHF)	380	100	A.M.P	10 nm Ti + 200 nm Au	PR
	077	800	Wet (BHF)	288	100	A.M.P	NA	PR
	088	800	Wet (BHF)	278	50	A.M.P	10 nm Ti + 200 nm Au	PR
3	101	785	Wet (BHF)	317	50	A.M.P	NA	SU8
	227	785	Wet (BHF)	325	50	**B**.M.P	NA	SU8
	229	785	Wet (BHF)	317	100	A.M.P	NA	SU8
	230	785	Wet (BHF)	325	50	**B**.M.P	NA	PR
	231	785	Wet (BHF)	317	100	A.M.P	10 nm Ti + 200 nm Au	PR
	237	785	Wet (BHF)	325	50	A.M.P	10 nm Ti + 200 nm Au	SU8
	239	785	Wet (BHF)	317	100	**B**.M.P	10 nm Ti + 200 nm Au	PR
4	188	850	Wet (BHF)	430	100	A.M.P	NA	SU8
	189	850	Wet (BHF)	80	100	A.M.P	NA	SU8

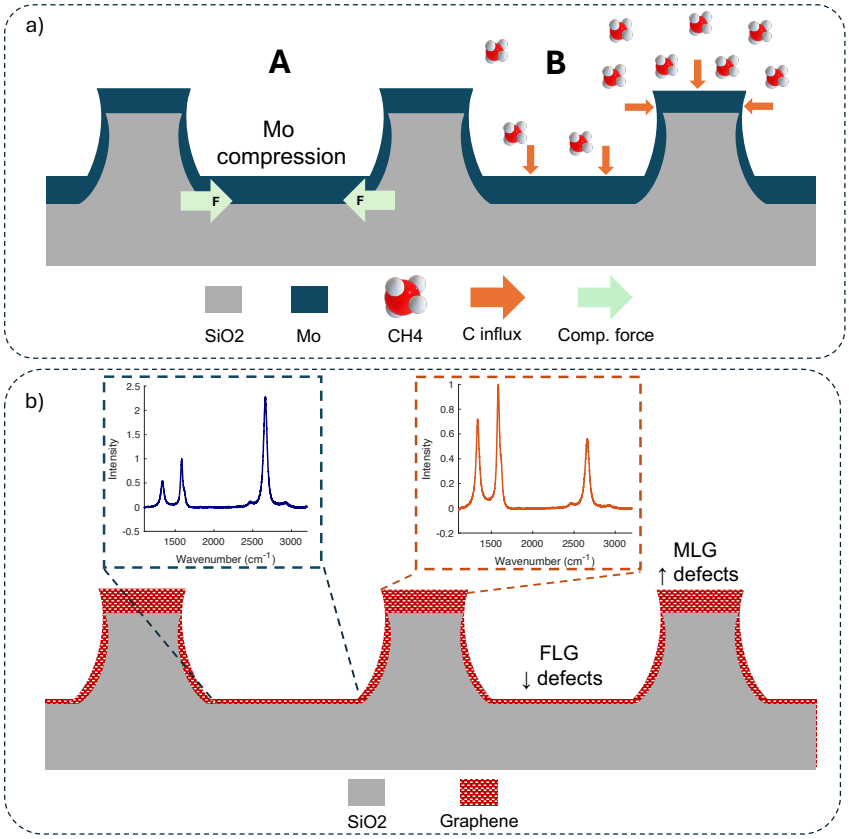

Figure 5.3: a) Schematic representation of the CVD graphene process on corrugated SiO_2 structures, considering a molybdenum catalyst deposited by physical vapour deposition. Process A represents Mo compression generated by the geometry of the valleys, while process B shows the differences in the carbon precursor interaction depending on the structure area. b) Graphene layer on corrugated SiO_2 structures resulting after performing Mo wet etch. Graphene layer is not scaled (Raman from W076).

5.2. Metallisation

As explained in Section 3.3.2, three different metallisation combinations were tested. Figure 5.4.a shows the results obtained for 100 nm Ti as adhesion layer and 650 nm Al1%Si, metallisation used in [42]. The etching process with HF required ≈ 15 minutes to properly resolve the electrode pads. However, due to the smaller width of the metal contacts of the TLMs, the metal on top of these structures suffered overetching. Additionally, the process left a considerable amount of residues. Alternatively, a metallisation using 100 nm Ti as adhesion layer and 350 nm Al was performed. As can be seen in Figure 5.4.b, this combination provided better results, with lower quanity of residues and most of the TLM metallisation properly resolved. However, the metallisation for the TLM structures with smaller and denser patterns suffered overetch, since HF infiltrates more easily between the structures. For this reason, a different metallisaiton approach was performed, using 10 nm Ti and 200 nm Au. This process considers lift-off instead of metal etching, avoiding overetching issues. As can be seen in 5.4.c, all the TLM metal structures got properly patterned. Additionally, the amount of residues considered after the lift-off process was considerably lower than the residues encountered after performing HF etching. Considering all the advantages, gold metallisation was considered for the final flowchart.

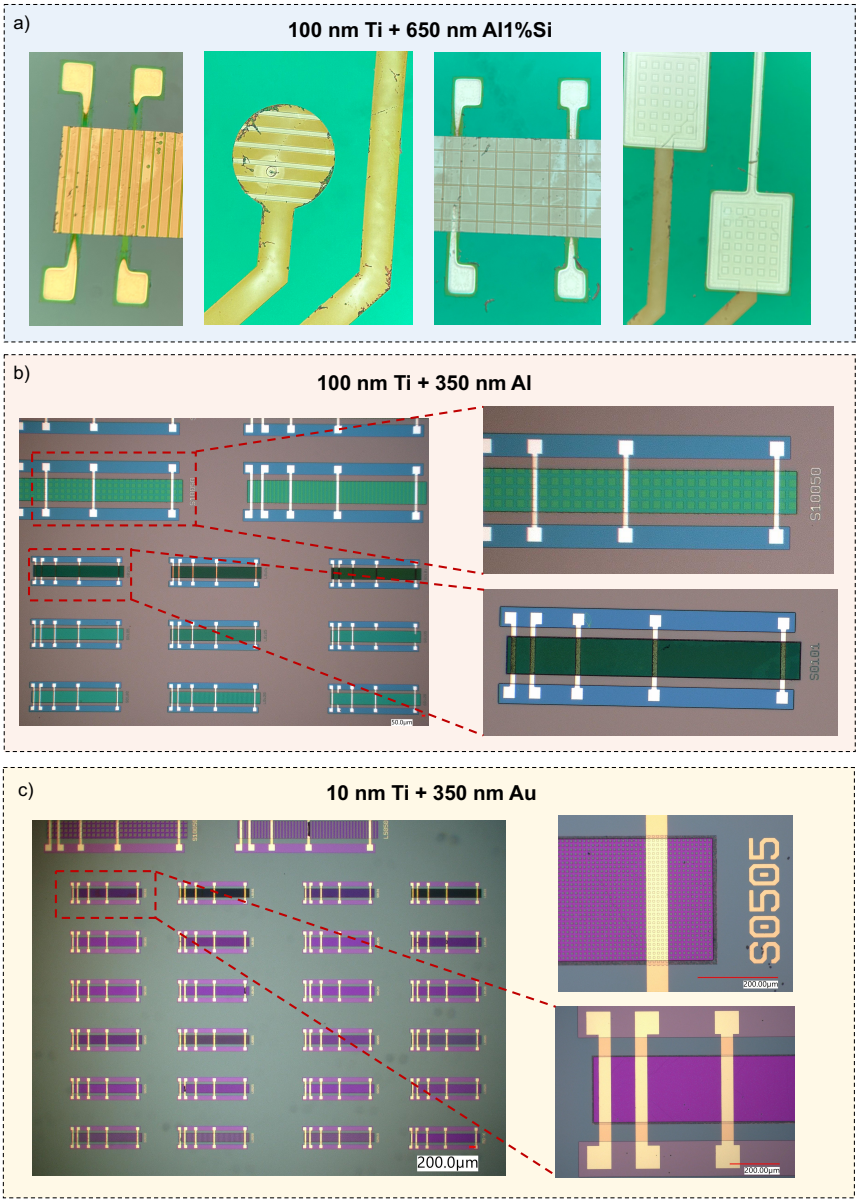

Figure 5.4: Results obtained for each metallisation combination (emphasis on TLM metal structures).

5.3. Device Encapsulation

Initially, the AZ3027 photoresist was considered for encapsulation of the final devices, as it had previously showed to be an effective encapsulation method for the proof of concept [42]. Nervertheless, 5µm of SU8 was used as encapsulation for the biocompatibility tests, as it is known to be a biocompatible polymer. As mentioned in Section 3.5, TLMs were used as samples for these tests. Therefore, in order to take the technology one step further by making it biocompatible, it was considered to use SU8 as the final encapsulation of the devices. Mo etching of the electrodes was performed considering the standard procedure, by placing a drop of H_2O_2 on top of the electrodes after encapsulation. However, this polymer seems to be permeable to H_2O_2, so the molybdenum in the tracks under the SU8 started to dissolve (see Figure 5.5). For this reason, this type of encapsulation could not be taken into account for the final devices, and the encapsulation finally considered was 3.1 µm of AZ3027 photoresist.

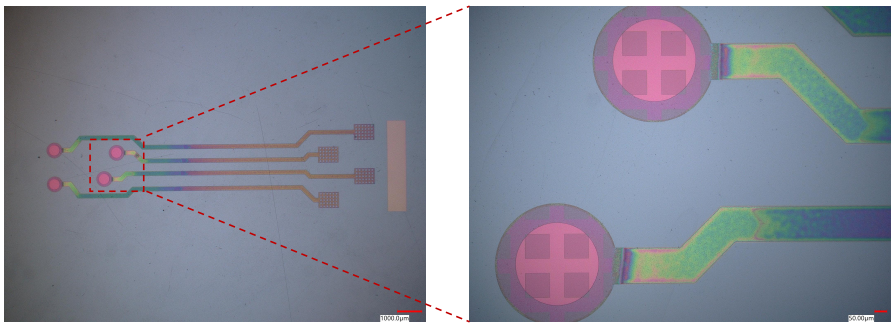

Figure 5.5: SU8 encapsulation after performing Mo etching with H_2O_2 of the graphene electrodes

5.4. Summary of Process Optimisation

While creating the corrugation pattern in Mo does not allow graphene to maintain a structure with recurring forms, **it is possible to create transfer free continuous graphene layers on grooved and ridged SiO_2 structures**, therefore generating corrugated graphene structures. Additionally, **the presence of pre-patterned structures appears to influence the CVD graphene growth process, resulting in what is referred to as the *top/bottom differences* phenomenon.** Overall, the parameters considered for the final devices are limited at:

- Corrugation substrate and initial thickness: $\approx$ 800 nm SiO_2.
- Etching method: wet etching with 0.55% BHF.
- Step height: 300-350 nm.
- Mo thickness: 50-100 nm.

Table 5.2: Summary of resistances and sheet resistance values obtained for different structures from W076. Rs value for structure S0101 was extracted considering only two lengths, since results of the resistance for L1 and L4 showed incongruent values potentially coming from a bad Au-Mo contact. * Values obtained using $R_s = R_x \frac{W}{L_x}$, where R_x is the measured resistance values per length and L_x is the length.

Structure	R_{L1} (Ω)	R_{L2} (Ω)	R_{L3} (Ω)	R_{L4} (Ω)	Rs/W ($\Omega sq^{-1}\mu m^{-1}$)	Sheet resistance (Ωsq^{-1})
L0101	82.47	166.52	233.02	340.78	0.30	90
S0101*	-	157.31*	243.01*	-	-	130
S0105	101.38	157.42	246.08	398.36	0.35	105
S0120	98.97	179.99	269.43	477.67	0.45	135
L0550	133.91	109.42	171.45	398.53	0.16	96
L5010	71.54	93.65	142.80	253.19	0.13	80

Table 5.3: Summary of Raman average parameters obtained for the wafers during the optimization procedure. Based on the I_D/I_G ratio, W7 had the less quality graphene, while W18, W101, W230 and W237 presented the best graphene quality.

Wafer	Structure	Top I_{2D}/I_G	Bottom I_{2D}/I_G	Top I_D/I_G	Bottom I_D/I_G	Top $FWHM_{2D}$ (cm^{-1})	Bottom $FWHM_{2D}$ (cm^{-1})
7	S0101	0.65		0.87		68.94	
	S2040	0.92	0.99	0.79	0.51	72.84	63.48
	S0525	0.63	0.52	0.67	0.59	63.74	62.24
	S10010	0.49	0.48	0.87	0.56	68.12	66.97
9	L0101	1.32		0.50		55.62	
	S0101	1.04		0.40		60.89	
	S2040	1.55	-	0.50	-	58.93	-
	S10010	0.58	1.35	0.58	0.53	68.78	59.23
10	L0101	1.16		0.47		55.39	
	S0101	0.94		0.41		60.37	
	L0505	0.89	1.17	0.51	0.35	61.37	60.74
	S0505	0.80	1.14	0.51	0.39	63.87	60.39
	S0550	0.85	1.22	0.59	0.46	62.74	58.92
	S10010	0.58	1.39	0.61	0.53	62.65	62.51
11	L0101	1.00		0.62		60.34	
	S0101	1.15		0.40		56.15	
	S0550	0.64	1.59	0.39	0.40	54.61	52.54
	S2040	0.67	1.20	0.48	0.34	55.34	57.37
13	L0101	0.67		0.69		66.09	
	S5010	0.48	1.16	1.02	0.37	70.21	72.22
16	S0525	0.76	2.01	0.48	0.45	60.22	62.73
	S10010	0.67	2.03	0.50	0.41	65.46	61.67
18	S0101	2.10		0.29		54.72	
	S0120	1.72		0.24		56.75	
	S2010	0.79	1.63	0.28	0.24	47.54	55.53
	S2040	0.59	2.63	0.18	0.36	48.22	47.55
	S2060	0.43	1.63	0.26	0.26	61.49	57.99
	S5010	0.49	1.18	0.32	0.19	59.20	59.12
	S10010	0.67	1.67	0.33	0.39	55.74	58.41
076	L0101	1.29		0.41		67.06	
	S0101	1.23		0.59		63.49	
	S0550	0.50	2.24	0.69	0.56	67.79	57.79
	S2010	0.58	1.57	0.72	0.49	58.96	62.22
	S5010	0.96	2.14	0.69	0.54	51.49	59.91
	S10010	0.58	1.84	0.70	0.42	64.11	58.80
088	L0101	0.76		0.54		60.18	
	S0101	0.80		0.51		57.19	
	S0120	0.64		0.61		62.44	
	S0525	0.57	0.56	0.52	0.52	56.54	59.03
	S0550	0.73	0.73	0.57	0.58	58.37	58.18
	S10010	0.58	0.58	0.49	0.59	56.19	59.23
101	S2010	1.90	3.71	0.27	0.30	57.57	49.10
	S2040	2.29	3.01	0.41	0.31	54.32	53.57
	S5010	2.31	-	0.51	-	59.27	-
230	S2040	2.48	4.11	0.18	0.18	48.32	49.07
	S0505	1.79	1.84	0.28	0.17	50.48	60.93
	S5010	2.78	2.08	0.19	0.17	45.05	57.81
237	S2040	0.59	1.67	0.33	0.26	56.35	63.47
	S0525	1.06	2.21	0.25	0.22	64.26	53.59

6

Device Characterization: Results and Discussion

This chapter presents the results obtained for the structures and devices fabricated considering the optimized parameters. This includes the material and electrical characterization together with the electrochemical performance and biocompatibility evaluation. For the material and electrical characterization SEM, AFM, Raman spectroscopy and TLM measurements were performed and evaluated. EIS, CV and VT were used to understand the electrochemical performance of the electrodes. Dead/Life, Dapi/Phaloidin, MTT and Presto Blue tests were performed and evaluated to understand the biocompatibility of the fabricated structures.

As mentioned in Chapter 5, the goal of batch 3 was to fabricate a set of wafers to extract statistics about graphene growth and, additionally, use some of the wafers to assemble the final devices and prepare structures for the biocompatibility tests. The batch initially consisted of 12 wafers. Although this did not seem to affect the quality of the graphene, five of the wafers showed what seemed to be photoresist residues. The other six remaining wafers were residue-free and therefore considered as potential for both final device assembling and biocompatibility testing. Finally, three wafers from batch 3 were considered for final device assembly and biocompatibility testing (Wafers 231 and 239 - final device assembling; Wafer 229 - biocompatibility testing). The three remaining wafers were rendered unusable after performing SU8 optimization tests. Two other wafers from batch 4 (188 and 189) were used both to further understand graphene growth in corrugated patterns and for biocompatibility testing.

6.1. Material Characterization

The wafers were observed under optical microscopy and SEM to ensure the absence of residues. Figures 6.1.a-d show SEM images of SiO_2 corrugated patterns with Mo (small grains) and graphene (rosettes). No obvious photoresist residues were observed neither before nor after Mo etching in any of the wafers. In addition to the profilometer measures performed inside the cleanroom during fabrication, the height of the steps was also determined by AFM. Figure 6.1.e shows an AFM image and the respective graphic representation after performing Mo etching. As expected, a step height of around 315 nm on the SiO_2 was measured. Additionally, the wet etching of SiO_2 resulted in sloped sidewalls rather than sharp edges, with a horizontal variation of 450 nm between the top and bottom of the structure, indicating the typical profile of isotropic wet etching. The correctly resolved area of the AFM scanner, as indicated at the corresponding horizontal profile, was taken into account the horizontal variation (or sloped sidewall). The non-symmetry in the horizontal profile is associated with the scan direction; the step-up was properly resolved by the AFM tip, while de descend step was not properly addressed. Morevover, an AFM scan of a delaminated area of graphene (where only SiO_2 was present) was performed, as can be seen in Figure 6.1.f. A nanometrically rough surface is evident resulting from the BHF etching of the SiO_2, which may also influence the properties of the graphene both in its growth and after etching of the molybdenum. An attempt was made to measure the thickness of the graphene, but due to the extreme roughness of SiO_2, it was not feasible to extract the thickness of the graphene itself.

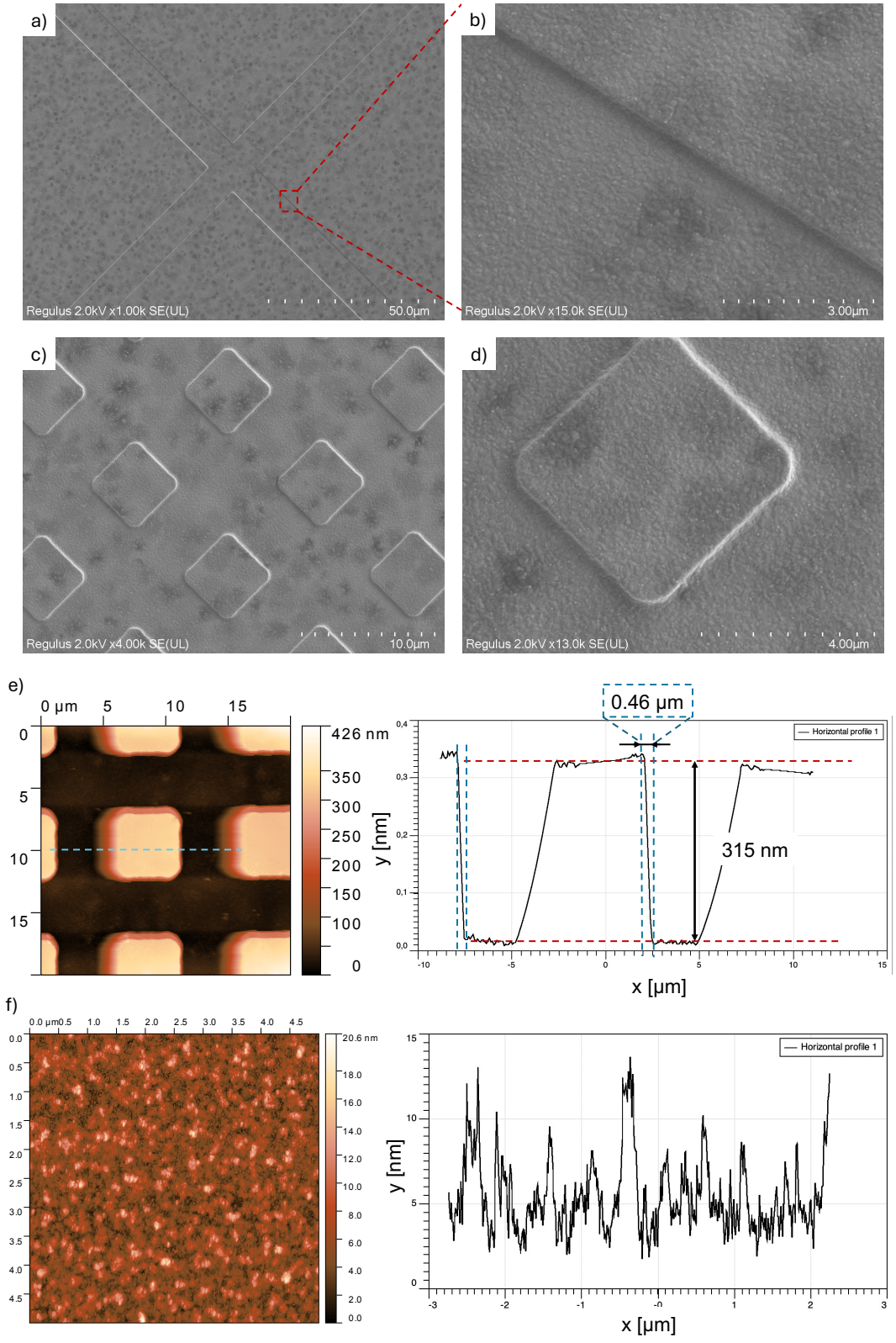

Figure 6.1: a-d: SEM images of corrugated SiO_2 patterns with Mo and graphene. a) S10050 pattern. b) Detail of S10050 pattern. c) S0505 pattern. d) Detail of S0505 pattern. e) AFM image and transversal topography graph of S0505 pattern. The step in scan direction was properly resolved, while the descent of the step was not successfully addressed. f) AFM image and scan horizontal profile of SiO_2 after BHF wet etch.

Raman measurements were performed on different structures for all wafers to obtain additional data on the graphene growth process and to gain insight into the type of graphene present. Table 6.1 presents the average Raman ratios and $FWHM_{2D}$ obtained for the two wafers considered for the final devices and the three wafers used for the biocompatibility tests. As mentioned above, wafers 229, 231, and 239 were fabricated in batch 3. Considering the I_{2D}/I_G ratio of these wafers, thin graphene seems to be present both at the bottom and top of the structures. Moreover, the graphene quality of batch 3 wafers seems to be higher than the graphene quality of wafers coming from batch 4, showing lower general I_D/I_G ratios (and being the graphene from wafer 239 the higher quality one). Graphene thickness and quality differences between batches can be attributed to several reasons, being the SiO_2 surface characteristics one of the most potential influencing factors. Molybdenum deposition, and therefore its grains arrangement and characteristics, can be directly influenced by several SiO_2 factors, including the thickness of the patterns, their shape, and the surface roughness. The amount of Mo deposited may also influence directly its own characteristics, even considering the same SiO_2 configuration.

Lastly, considering wafer 239, molybdenum and graphene structures were patterned after graphene growth, which can be the cause a more homogeneous graphene growth and therefore better quality layers, even considering a thin catalyst (Mo) of 100 nm thickness. This wafer contained the best quality graphene compared to all the wafers considered in this chapter. For this particular wafer, the graphene properties in terms of thickness and quality of the flat (non-corrugated) appears to be similar to the properties of corrugated structures. A fine graphene is apparently obtained even without corrugation thanks to the growth of the graphene on the 100 nm Mo substrate before patterning, which as explained in the previous chapters seems to offer a better structured graphene. Other factors that can affect graphene growth must also be taken into account, such as the influence of carbon flow which can be affected by adjacent corrugated structures, as well as heat transfer which depends on the SiO_2 thickness, among others.

Despite the differences between batches, **the *top/bottom differences* phenomenon remains evident in all cases,** irrespective of the wafer batch. Figures 6.2.a and 6.2.b show box plot representations for the Raman ratios and $FWHM_{2D}$, differentiating the values between the top and bottom of the structures. This representation takes into account all five wafers. In this case, considering the ratios values, a higher mean is observed compared to the wafers obtained during the optimisation process. As in the results shown in Chapter 5, the ratios and $FWHM_{2D}$ values show a higher variance for the top structures compared to the values obtained for the bottom, as can also be seen by analysing the value of the standard deviation in Table 6.1. This demonstrates the presence of a more homogeneous graphene at the bottom than at the top of the structures. Additionally, it is confirmed by the I_{2D}/I_G and I_D/I_G ratios from this set that graphene seems to be thinner and of better quality at the bottom of the structures compared to the top.

Furthermore, to give the reader an appreciation of how the Raman spectra appear when being compared, Figures 6.2.c and 6.2.d representative spectra of the batch 4 wafers have been plotted alongside representative spectra of wafer 239. Considering both top and bottom structures, the 2D peak is the most pronounced for 239. As mentioned, even at the top of the structures 2D peaks were more intense than the G peaks, relating to a thinner graphene on the top for 239 than for 188 and 189. In addition, the D peak is noticeably smaller for this wafer, which relates to better quality graphene.

The devices used to perform the final electrical and electrochemical characterization were extracted from wafer 239 due to several reasons, including the superior quality of the graphene and the cleanliness of the devices after dicing. **After the characterisation of the material, the graphene used in the electrical and electrochemical tests can be considered corrugated (preserving the structure and continuity of the patterns) and thin, classifying it as few-layer graphene (FLG).** The graphene used for the biocompatibility tests (229, 188 and 189) can be regarded as similar, though it may be slightly thicker at the top of the structures when considering the wafers from batch 4. Metallisation of these last three wafers was not necessary.

Table 6.1: Summary of Raman average parameters obtained for some of the patterns of the wafers used for assembling the final devices and to perform the biocompatibility tests. Considering the I_D/I_G ratio, W239 showed the best quality graphene.

Wafer	Structure	Top I_{2D}/I_G	Bottom I_{2D}/I_G	Top I_D/I_G	Bottom I_D/I_G	Top $FWHM_{2D}$ (cm^{-1})	Bottom $FWHM_{2D}$ (cm^{-1})
229	S0101	2.75		0.26		53.19	
	S2010	1.89	2.82	0.29	0.38	67.09	57.09
	S5010	2.21	2.68	0.45	0.42	61.38	59.81
231	S0120	2.62		0.45		55.31	
	S0550	2.30	2.26	0.40	0.38	57.14	55.72
	S10010	4.01	3.08	0.49	0.41	50.26	60.29
239	L0525	1.86	2.62	0.21	0.24	60.49	55.44
	S0525	1.94	2.22	0.22	0.23	62.79	54.21
	S2040	1.55	2.15	0.25	0.26	70.51	60.91
	S5010	2.80	2.24	0.28	0.25	59.59	60.77
	MO	2.32		0.32		60.96	
	MO-x	2.50		0.23		53.15	
189	S0101	2.51		0.52		65.32	
	S2010	0.83	2.51	0.45	0.47	69.98	61.89
	S2040	1.36	2.26	0.77	0.43	58.43	65.65
188	S0101	1.35		0.58		66.43	
	S2010	0.63	1.84	0.66	0.51	66.64	61.16
	S2040	0.89	1.67	0.51	0.51	67.15	61.04
	S5010	1.12	1.69	0.72	0.48	65.31	63.82
MEAN	Total	1.80 ± 0.92	2.31 ± 0.43	0.44 ± 0.19	0.38 ± 0.10	62.83 ± 5.74	59.83 ± 3.35

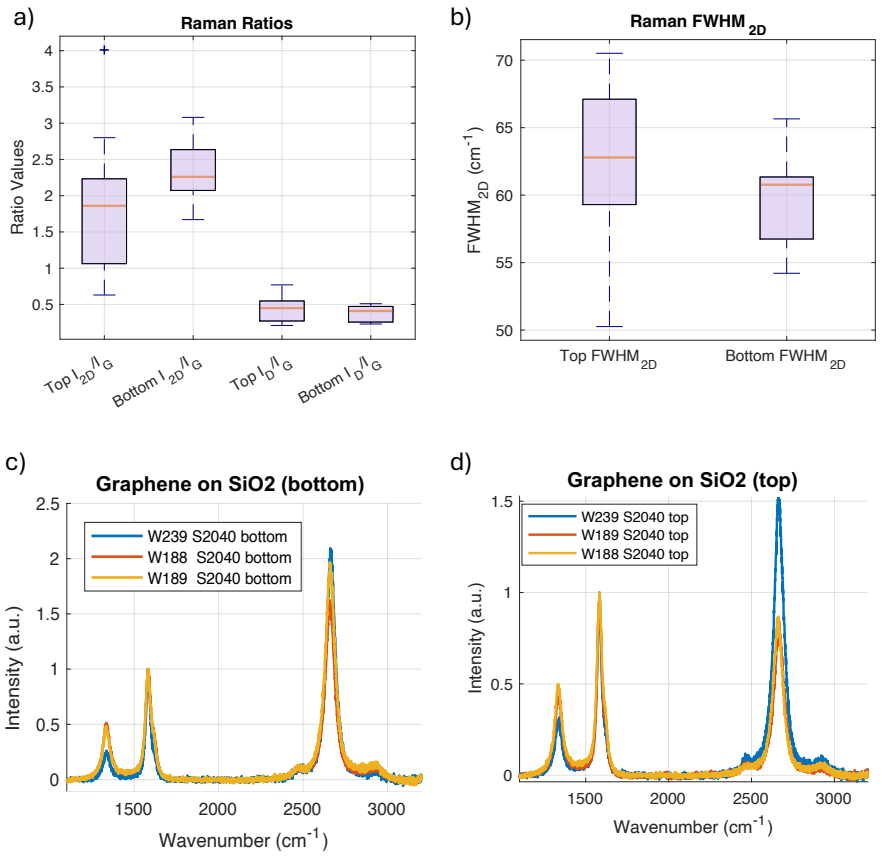

Figure 6.2: a) Box plot representation of I_{2D}/I_G and I_D/I_G ratios, differentiating between top and bottom, considering the structures of the five wafers. a) Box plot representation of $FWHM_{2D}$, differentiating between top and bottom, considering all the structures of the five wafers.

6.2. Electrical and Electrochemical Characterization

TLMs structures were used to perform sheet resistance measurements of the fabricated structures. Additionally, the devices were successfully diced and wire bonded to perform electrochemical measurements. As explained in Chapter 3, PDMS or epoxy were used to mechanically fix the bonds connecting the PCB to the devices. PDMS is highly viscous, which can lead to the wires detaching from the pads during the encapsulation process. For this reason, epoxy was tested as an alternative to encapsulate the bond pads. However, it was observed that epoxy reacts with the PR used as an encapsulation, creating stresses and causing it to delaminate. Therefore, PDMS was used for most of the devices, gently performing the pouring to avoid wire bond detachment.

Figure 6.3 shows a device fully assembled and prepared for characterisation. The assembly process consisted of four steps: 1) dicing, 2) gluing the device to the PCB, 3) wire-bond the PCB-device pads, 4) mechanically fix and encapsulate the device using PDMS or epoxy.

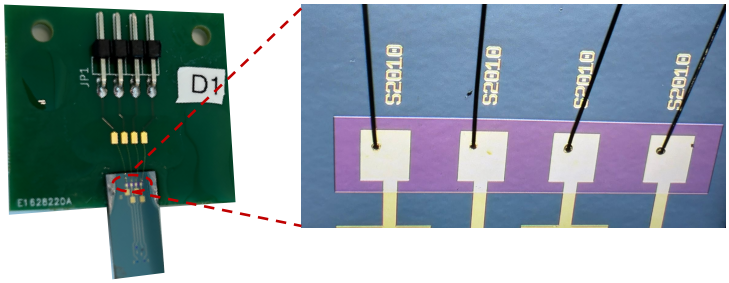

Figure 6.3: D1 device, succesfully assembled, and detail of the contact pads with the wire bond.

For the electrochemical tests, the same area was considered for all electrodes ($\pi 170^2$ µm^2 ≈ 90792 µm^2) to observe how the patterns change the electrochemical properties of the electrodes and to understand if making these vertical patterns actually increases the surface area of the electrode. Denser patterns are expected to have a larger surface area. However, no firm conclusions can be drawn, as graphene growth dynamics can differ depending on the corrugated structure, leading to materials with different electrical properties.

6.2.1. Sheet Resistance of Corrugated Patterns

Sheet resitance measurements were performed using the TLMs structures of wafer 239 using 4-point probe measurements that proved to reduce the effect of the contact resistance [142, 143]. The procedure followed can be found in Section 3.4.1. Table 6.2 summarizes the resistance values obtained for each of the lengths, as well as the final sheet resistance. The curves obtain for each of the resistances calculation can be found in the Appendix A, Figures A.9 and A.10. Additionally, for comparison, Table 6.2 presents the sheet resistance values calculated for some of the structures of wafer 076 (wafer fabricated on batch 2, which corrugation was performed also on SiO_2, presented in section 5.1.2). The same table also provides the sheet resistance values for some structures from a wafer that underwent corrugation on molybdenum.(presented in section 5.1.1). As mentioned on Chapter 5, only a few values of Rs were obtained for W076 as it they were performed to prove graphene layer continuity.

As can be seen, considering both of the wafers in which the corrugation was performed on SiO_2, most of the sheet resistance values are in the 60-180 Ωsq^{-1} range. This range of values can be considered particularly low compared to the graphene obtained performing the corrugation at the catalyst (Mo, right column Table 6.2) and the MLG used as transparent electrodes, grown in a Mo catalyst, whose range was between 400 and 700 Ωsq^{-1} [101]. Graphene properties are directly dependent on the substrate topography and treatment, as well as on the catalyst thickness, among others. Therefore, the properties of graphene can also be expected to be different from the obtained by Bakhshaee et al. [42], in which a flat 50 nm Mo catalyst was used. In the following, information derived from the literature related to FLG sheet resistance values will be provided, as well as several hypotheses that can provide insight into the range of sheet resistance values obtained.

It is well known that sheet resistance is in many cases inversely proportional to the thickness of the material, which has shown to be the case for MLG [101]. However, this is true if the material

maintains its homogeneous characteristics, i.e. increasing the thickness does not affect other aspects such as its homogeneity. MLG roughness can be non-uniform, and the sheet resistance of graphene has proven to be dependent on its surface roughness, which makes the sheet resistance of graphene directly dependent on its quality [144]. Additionally, the transfer process significantly degrades the properties of graphene by introducing contaminants, mechanical stresses, and irregularities into the material, which leads to an increase in the sheet resistance of the graphene [145, 146, 147].

In this work, the Raman spectra indicates that the material obtained is mostly high quality graphene (specially on the bottom of the structures), which also appears to have FLG characteristics. Literature shows how thin CVD graphene (SLG and FLG), even after a transfer process, can provide sheet resistance values in the range of those obtained in this work. Table 6.3 shows some of the lowest sheet resistance values reported on literature for thin graphene. Several studies demonstrate that doping graphene can significantly reduce sheet resistance, achieving values as low as $50\Omega sq^{-1}$, $30\Omega sq^{-1}$ and even $16\Omega sq^{-1}$ [148, 149, 150, 151]. Conversely, many studies consider undoped graphene and different transfer strategies to minimize the adverse underlaying effects of a transfer process. For instance, undoped FLG transferred onto SiO_2 or PMMA substrates has been reported with sheet resistance values ranging from 100 to 350 Ωsq^{-1} [152, 153, 154]. Considering undoped SLG, sheet resistances of approximately $500\Omega sq^{-1}$ have been documented [150]. Other apporaches, such as stacking BLG (bilayer graphene) layers, have shown that FLG can achieve sheet resistances below 300 Ωsq^{-1} with four transferred, stacked BLG [155]. FLG transferred by aqueous media has reported values of around $200\Omega sq^{-1}$ [156]. Furthermore, the roll-to-roll transfer method for SLG has resulted in sheet resistances between 250-$300\Omega sq^{-1}$ [157]. Alternative approaches, including mild oxidation of natural graphite and exfoliation, have produced FLG with sheet resistance values ranging from 100-300 Ωsq^{-1} [158, 159]. Considering transfer-free processes, Chen et al. reported the sheet resistance for a non-transferred polycristaline FLG, ranging values between 200 and 800 Ωsq^{-1} [160], while Bi et al. achieved a significantly lower value of $63\Omega sq^{-1}$ [161]. Considering turbostratic FLG, Richter et al. fabricated graphene disks deposited on SiO_2 which presented sheet resistances between $60\Omega sq^{-1}$ and $180\Omega sq^{-1}$ [162]. Some studies also show how wrinkles can help to have enhanced properties in turbostratic graphene [163].

As can be seen, many of the values reported in the literature closely align with those obtained in this study. The major part of these works consider graphene transfer processes, which reduces its properties. Still, low values of sheet resistance for FLG are reported. In this work a transfer-free graphene is presented, which eliminates the factor of introducing impurities in the transfer process. Comparisons with other graphene growth techniques are challenging, as this study addresses a previously unreported scenario: graphene growth on a 100 nm Mo substrate deposited on a SiO_2 with corrugated patterns generated by wet etching. Furthermore, the graphene on wafer 239 was patterned after its growth on the entire corrugated wafer, representing a novel, exploratory approach that appears to yield high-quality, transfer-free thin graphene, as demonstrated by studying its Raman properties.

Considering both wafers 239 and 076, several factors may therefore account for the ability of the graphene obtained here to exhibit low sheet resistance values. Both wafers were fabricated considering similar fabrication parameters, being the step height 317nm for 239, and 400nm for 076. As can be seen in the tables 6.1 and 5.3, the *top/bottom differences* phenomenon is present in both wafers. The graphene in wafer 239 appears to be of generally better quality than that in 076, which translates into better electron conduction (see Table 6.2; for same structures, wafer 239 provides lower sheet resistance values compared to W076). Considering the metal deposition, wafer 076 was kept in vacuum overnight, which improved the metal adhesion to the smaller, denser structures (L0101; S0101). On wafer 239, measuring the sheet resistance of these structures was more challenging as the adhesion to these small and dense patterns was much less optimal. Additionally, some of the denser structures (L0101 and S0101) of this wafer presented what appeared to be lift-off residues. Nevertheless, sheet resistance values obtained for both wafers are within the same range.

There is an obvious dependence between the shape of the patterns. Figure 6.4 provides a comparative representation of the sheet resistance values for lines, squares and the flat structures. As can be seen, the sheet resistance values for the squares are lower than for the lines. The sheet resistance value obtained for the flat structure is one of the lowest obtained. In the case of wafer 239, this is particularly meaningful, as even the non-corrugated structures (flat structures) exhibited thin, high-quality graphene (low I_D/I_G ratio, see Figure 6.6). In general, the *top/bottom differences* phenomenon was still observed, having therefore more FLG characteristics at the bottom of the structures than at the

top. The explanation behind the higher Rs values for line structures is that electrons encounter more resistance in these patterns due to the larger vertical area they have to traverse, since the current flows perpendicular to the arrangement of the lines, electrons must consistently move through the uppermost sections of the structures. Considering the flat surface, this structure was homogeneously of good quality, allowing the electrons flow not be impeded as in the case of the lines. Overall, lower sheet resistances are obtained for less corrugated structures, which can be attributed to the reduced scattering of electrons, allowing for a more efficient conduction pathway. Considering the lowest resistance value, associated to the S0105 structure, the patterns do not seem to negatively impact the resistance; rather, the opposite appears to be true. In this scenario, the pillars may not be large enough to create significant resistance to electron flow. However, having these structures on the SiO_2 could provide a more compact molybdenum substrate compared to the flat structures, resulting in tbe graphene with the most outstanding properties.

Graphene quality, combined with a few-layer arrangement, seem to be two factors generating low sheet resitance values. This can be also supported by analysing the sheet resistance results for graphene grown on corrugated molybdenum (right column Table 6.2), which show less conductive graphene. This is meaningful considering Raman spectra of these samples (which show graphene, albeit MLG, of considerably lower quality; see Appendix A, Figure A.6). The range of these sheet resistance values are in accordance with those obtained for MLG by Babaroud et al. [42], although the manufacturing process is not comparable. As discussed in Chapter 5, the higher contact resistance values in this case can be attributed to the poor adhesion between the metallisation layer and the molybdenum, which in this case was bulky 500 nm with steps of 300 nm before its etching.

The dependence of sheet resistance on pattern shape suggests that the measurements reflect the properties of the material within the TLM structure. Nevertheless, several validation points were addressed to ensure that these sheet resistance values are not the result of calculation or fabrication-related errors. The calculations and experimental procedures were reviewed several times, and no systematic errors were identified. To ensure that no multiplication factor influenced the extraction of sheet resistance from the interpolation of individual resistance values (measured for each TLM length), an approximate Rs was calculated using each of the Rx resistances along with their respective Lx distances. (see Appendix, Figure A.12). The values were within the Rs range calculated using the TLM method, verifying the absence of error in this regard. Furthermore, the linearity of the calculated values and the order of magnitude of the results show no obvious reason to consider a procedural or post-processing error in the data. Additionally, a 2-point probe measurement was performed placing two needles in different test structures to verify that no molybdenum residues were influencing the sheet resistance measurements (see Figure 6.5). A sweep voltage between -200 mV and 200 mV was applied between structures, and the current obtained was in the order of pA. The same test was performed elevating the needles (no-contact mode), and the current obtained was in the same order of magnitude, relating this values to pure noise in both cases. This way it was verified that the structures were electrically isolated, therefore no molybdenum residues were affecting the measurements. Additionally, the low contact resistance values further confirm the accuracy of the four-point probe measurement, which was employed to minimize contact resistance contribution. In this case, the molybdenum bulk structure was 100 nm, 5 times lower than in the case of the corrugated patterns performed in the bulky Mo, which reasonably provided lower contact resistances. All the factors presented in this section support the feasibility of graphene possessing excellent electrical properties.

Overall, the turbostratic stacking of the thin FLG graphene in this work offer lower sheet resistances, raging from 60 to 180 Ωsq^{-1}, compared to the MLG grown on Mo previously reported in [42]. In comparison to multilayer graphene, FLG can retain good electronic properties without being dominated by the effects of defects that might be more prone to be present in MLG. Still, other possible reasons for these low values may include other reasons, such as unwanted doping with MoO3 residues that might have remained in the material after Mo etching. MoO3 has been shown in the literature to be a dopant of FLG [149], lowering graphene sheet resistance. Further analysis of the structures is needed to provide more understanding to the values obtained.

Table 6.2: Summary sheet resistance calculation for wafer 239. The last column shows the sheet resistances of some of the structures of wafer 076, added to the table for comparison purposes. As mentioned, only a few values of Rs were obtained for W076 as it they were performed to prove graphene layer continuity at Chapter 5. Additional information on Appendix A, Table A.1, and Figures A.7, A.8, A.9 and A.10. L0101 and S0101 values structures in W239 presented what was considered as lift-off residues, which was reflected in their resistance values. It was not possible to perform a proper measurement for the S0120 structure in wafer 239.

Structure	R_{L1} (Ω)	R_{L2} (Ω)	R_{L3} (Ω)	R_{L4} (Ω)	Rs/W ($\Omega sq^{-1}\mu m^{-1}$)	W (μm)	Sheet resistance W239 (Ωsq^{-1})	Sheet resistance W076 (Ωsq^{-1})	Sheet resistance corr on Mo (Ωsq^{-1})
L0101	235.20	640.73	1107.17	1931.53	1.99	300	597	90	
L0105	45.35	128.91	239.52	313.98	0.32	300	96		
L0120	-	116.33	172.22	303.86	0.29	300	87		
L0505	73.47	168.71	265.52	431.62	0.42	300	126		
L0525	81.43	212.48	336.10	-	0.56	300	168		
L0550	29.97	85.20	142.81	230.57	0.12	600	72	96	
L2020	86.92	208.07	341.02	-	0.56	300	168		
L2040	50.93	139.22	202.60	316.08	0.15	600	90		
L5010	27.07	74.43	180.38	199.39	0.11	600	66	78	
L5050	45.38	115.08	180.38	287.91	0.14	600	84		
S0101	214.86	597.07	939.88	1335.23	1.29	300	387	130	
S0105	46.29	77.44	200.85	-	0.18	300	54	105	483
S0505	45.12	112.37	183.23	285.85	0.28	300	84		354
S0120	-	-	-	-	-	-	-	135	687
S0525	60.08	162.65	236.43	354.35	0.34	300	102		783
S0550	24.58	68.55	117.16	189.89	0.10	600	60		
S2010	72.36	228.94	271.76	391.33	0.35	300	105		285
S2040	40.44	106.08	160.31	260.79	0.13	600	78		
S2060	30.80	83.83	132.78	215.49	0.11	600	66		
S10050	39.35	100.68	150.51	227.73	0.11	600	66		
FLAT	35.17	111.39	144.17	229.18	0.22	300	66		

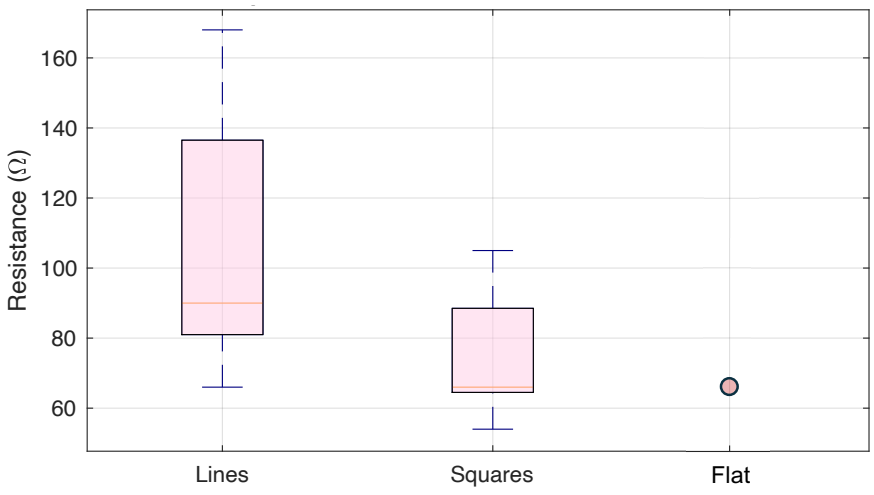

Figure 6.4: Sheet resistance values dependent on each type of structure shape for wafer 239.

Table 6.3: Sheet resistance values reported on literature for SLG and FLG.

Graphene type	R_S (Ωsq^{-1})	Doped	Additional info	Reference
4 Layer by layer stacked FLG	16	Yes	CVD graphene grown in situ on PET, not transferred	Han et al. [148]
FLG	50	Yes	CVD grown on Cu **doped with MoO3**	Meyer et al. [149]
SLG	150	Yes	CVD grown on Cu, roll-to-roll transfer to PET	Kobayashi et al. [150]
Stacked FLG	30-100	Yes	CVD grown on Cu, roll-to-roll transferred to SiO2	Bae et al. [151]
FLG	100	No	CVD grown on Cu, transferred to SiO2	Kim et al. [152]
MLG-FLG	100-350	No	APCVD grown on Cu, transferred with PMMA to SiO2	Pu et al. [153]
FLG	280	No	CVD grown on Ni, transferred to PDMS	Kim et al. [154]
4 Stacked BLG	300		CVD grown on Ni, transferred	Lee et al. [155]
FLG	200	No	CVD on Ni, wet transferred to SiO2	Cai et al. [156]
SLG	300-400	No	CVD grown on Cu, roll-to-roll transfer to PET	Jang et al. [157]
FLG	100-300	No	Mild oxidation of natural graphite	Kim et al. [158]
FLG	100-300	No	Exfoliated graphene	Kottegoda et al. [159]
Polycristalline FLG	210-800	No	CVD grown on SiO2, not transferred	Chen et al. [160]
FLG	63	No	CVD grown on SiO2 through ambient pressure chemical vapor deposition, not transferred	Bi et al. [161]
SLG	500	No	CVD grown on Cu, roll-to-roll transfer to PET	Kobayashi et al. [150]
Turbostratic graphene	60-180	No	Turbostratic graphitic disks created by hydrocarbons pyrolysis, measured on native SiO2	Ritcher et al. [162]
FLG (Raman spectra)	**60-180**	**No**	**CVD grown on Mo, no transfer, measured on SiO2**	**This work**

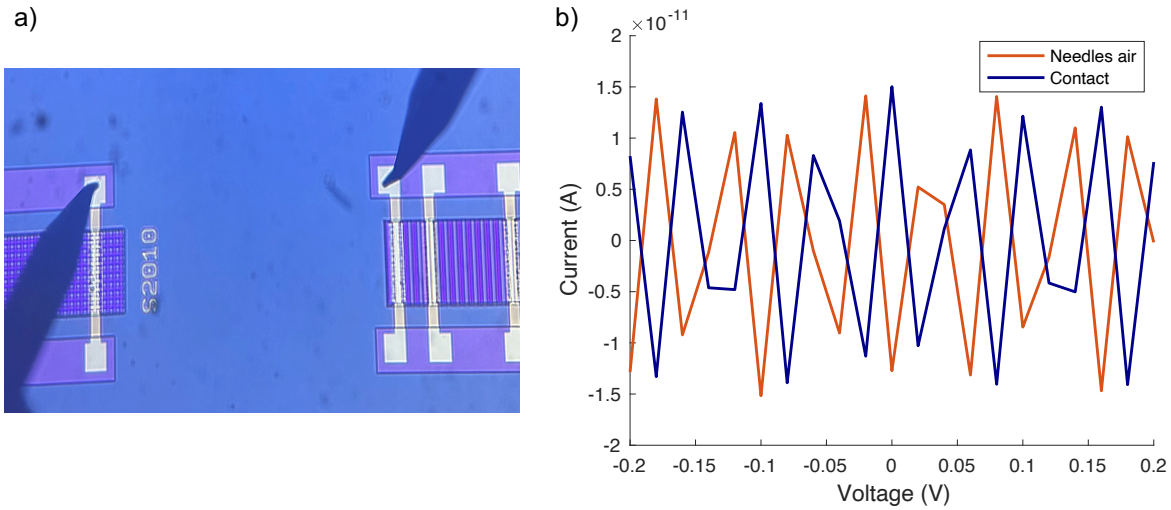

Figure 6.5: Substrate composition verification test performed to confirm the absence of molybdenum underneath the strucutures that could be causing low Rs values. a) 2-point probe setup. b) Current values measured applying a voltage sweep range of -200mV and 200mV between two different test structures.

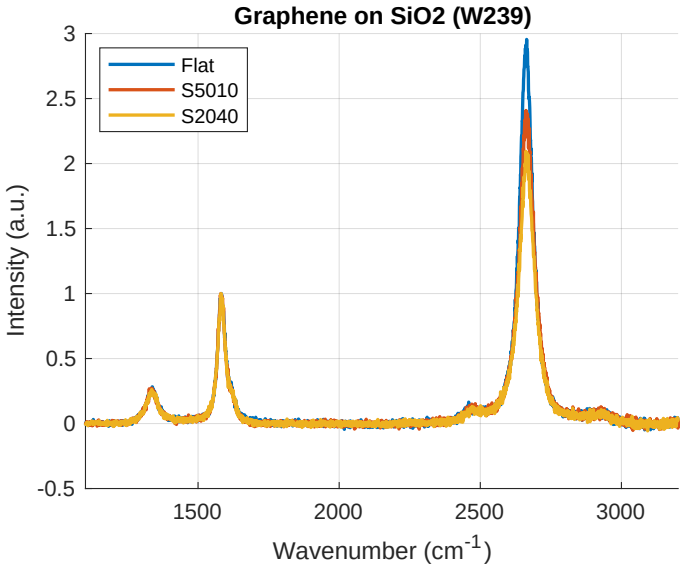

Figure 6.6: Representative Raman spectrum for some of the structures of wafer 239. The low D peak is representative of a low defective graphene.

6.2.2. Electrochemical Impedance Spectroscopy

Electrochemical tests were performed for 29 devices extracted from wafer 239. During initial electrochemical testing, some of the devices suffered severe damage on the Mo tracks, and graphene and photoresist delamination (see Appendix A, Figure A.11). The reason behind this was a broken reference electrode, which caused high current density and excessive current flow, leading to localized heating and eventual damage of both electrodes and molybdenum tracks. As a consequence, D1 to D6 were completely discarded from further electrical testing. After addressing the problem, a functioning reference electrode was obtained, and electrochemical testing could continue with the remaining electrodes. It is noteworthy that some of the electrodes delaminated simply upon being introduced or removed from the testing medium, which was a possible scenario given the thin nature of graphene. Table 6.5 shows the mean values of impedance ($k\Omega$) and area normalized impedance (Ωcm^2) at 1kHz obtained for the devices that survived the electrochemical tests. As explained above, the same area was considered for all the devices, corresponding to 90792 μm^2. Each device was constituted of four electrodes with the same pattern.

A dependence of the impedance on the pattern structure size and shape is evident, as can be seen in figure 6.7, which shows the box plot representation of the impedance results. Each group represents the shape and the size of the shape, representing all densities together for the same shape and shape size (namely, 1µm lines at all densities). Mean and standard deviation values are gathered in Table 6.4. Considering the lines, an increasing trend of impedance is observed with the increase of feature size, which implies that a smaller feature size increases the surface area of the electrode compared to a larger feature size, as expected. The mean of the standards for 5µm and 20µm widths shows that the impedance values obtained are similar to the mean value obtained for the flat electrodes. If the individual impedance results for lines structures are analysed, it can be seen that denser patterns for 5µm and 20 µm widths can give lower impedance values than the flat electrodes (see Table 6.5; D10, D13 and D14). A large pattern, 50 µm widths, seems to worsen the sheet resistance of the electrode. Regarding squares, the same trend in which the impedance increases with the width is observed for squares from sizes 5 µm up to 100 µm. Compared to 1 µm squares, 5 µm and 20 µm square patterns have proven to be more effective at increasing the electrode's effective surface area. In comparison to flat electrodes, 1µm, 5µm and 20µm patterns seem to increase the effective surface area of the electrode, lowering the impedance values. In this case, squares larger than 100µm do not seem to improve the effective electrode area. The results indicate that increasing the amount of material (graphene, in this particular case) generates more sites where electrochemical reactions can occur, which is responsible for reducing impedance. Theoretically, increasing the corrugated patterns

generate more available sites for electrochemical reactions to take place. However, it should not be assumed that the graphene synthesized in different structures has the same properties, as these might differ depending on the corrugation pattern (further investigation is required regarding how the growth of graphene is affected by specific corrugated surfaces). Therefore, the contribution of differences in the characteristics of the graphene itself that might be dependent on the pattern cannot be deemed irrelevant. In any case, although the graphene layer seems to be thin (which has been confirmed also by severe delamination), a trend is observed whereby increasing the amount of material due to the surface corrugations appears to increase the active surface area of the electrode. It should be noted that many of the devices were delaminated during the testing process, so further analysis is needed to gain more knowledge about how the shape and feature density affects the surface area.

Comparing now the area normalised impedance of the flat electrodes with the electrodes fabricated by [130], a considerable increase of up to 12 Ωcm^2 is observed. This also confirms that the graphene in this work is indeed thinner. Although the graphene considered in this work has a lower sheet resistance compared to the thicker MLG synthesised in [130], the interaction of the conductive part of the electrode with an electrochemical medium is significantly influenced by the amount of material that can contribute to charge transfer [164]. The reader should appreciate that the sheet resistance mainly reflects the conductivity of the material in a planar context, while the electrochemical impedance is affected by the complex material/electrolyte interface dynamics [165]. The reduced thickness of FLG might present higher impedance in comparison to MLG due to limited charge storage and ion transfer capabilities [166].

Lastly, relevant information about the behaviour of the electrodes with the environment can also be extracted by analysing the EIS phase diagram. Figure 6.8 shows the average phase diagrams extracted for each type of structure. In general, a combination of resistive and capacitive behaviour is observed. Highlighted in green are the phase diagrams of the structures with the lowest impedance at 1kHz (highlighted in Table 6.5). These structures have a similar phase, with a higher resistive behaviour at lower frequencies compared to the structures that showed higher impedances at 1kHz. Considering 1kHz frequencies, all electrodes show a clear capacitive dominance due to the prominence of the capacitive double layer which as expected seems to dominate the systems in this frequency range.

Overall, the electrodes show impedance values in the range of the $k\Omega$, which is relatively small compared to the maximum impedance recommended for recording applications ($\approx$1 MΩ) [167]. Although further analysis would be required both in vitro and in vivo to determine the real electrode-tissue impedance, **initial results are promising for potential usage of the electrodes in nerual recording applications.**

Table 6.4: Mean impedance at 1kHz for each structure group (shape and size).

Structure group	Area normalised mean impedance at 1 kHz (Ω)
L01	29.33 ± 4.42
L05	36.97 ± 4.54
L20	36.07 ± 4.42
L50	42.76 ± 2.91
S01	32.38 ± 2.64
S05	29.87 ± 2.44
S20	31.24 ± 5.13
S100	40.71 ± 3.66
FLAT	36.42 ± 0.83

Table 6.5: Mean impedance at 1kHz for each type of structure ($3 \leq n \leq 4$). Green values remark the lower impedance values for each feature shape. D29 is the flat electrode. D25 represents the typical impedance values of a delaminated electrode.

Device	Structure	Impedance at 1kHz (kΩ)	Area normalized Impedance (Ωcm²)
D7	L0101	28.81 ± 1.19	26.17 ± 1.08
D9	L0120	29.62 ± 4.47	26.89 ± 4.06
D10	L0505	37.77 ± 1.51	34.30 ± 1.37
D11	L0525	49.56 ± 4.69	45.00 ± 4.26
D12	L0550	45.59 ± 0.45	41.40 ± 0.41
D13	L2020	37.20 ± 1.87	33.78 ± 1.70
D14	L2040	34.09 ± 1.49	30.96 ± 1.36
D15	L2060	45.23 ± 1.04	41.07 ± 0.95
D16	L5010	44.83 ± 2.27	40.70 ± 2.06
D18	S0101	33.35 ± 4.59	30.27 ± 2.16
D19	S0105	36.18 ± 10.71	32.86 ± 9.76
D20	S0120	37.83 ± 3.05	34.35 ± 3.40
D21	S0505	32.86 ± 2.19	29.87 ± 2.44
D24	S2010	32.76 ± 4.62	29.75 ± 4.19
D25	S2040	62.26 ± 1.28	56.53 ± 1.16
D27	S10010	47.68 ± 2.85	43.29 ± 2.59
D29	-	39.06 ± 0.75	35.46 ± 0.68

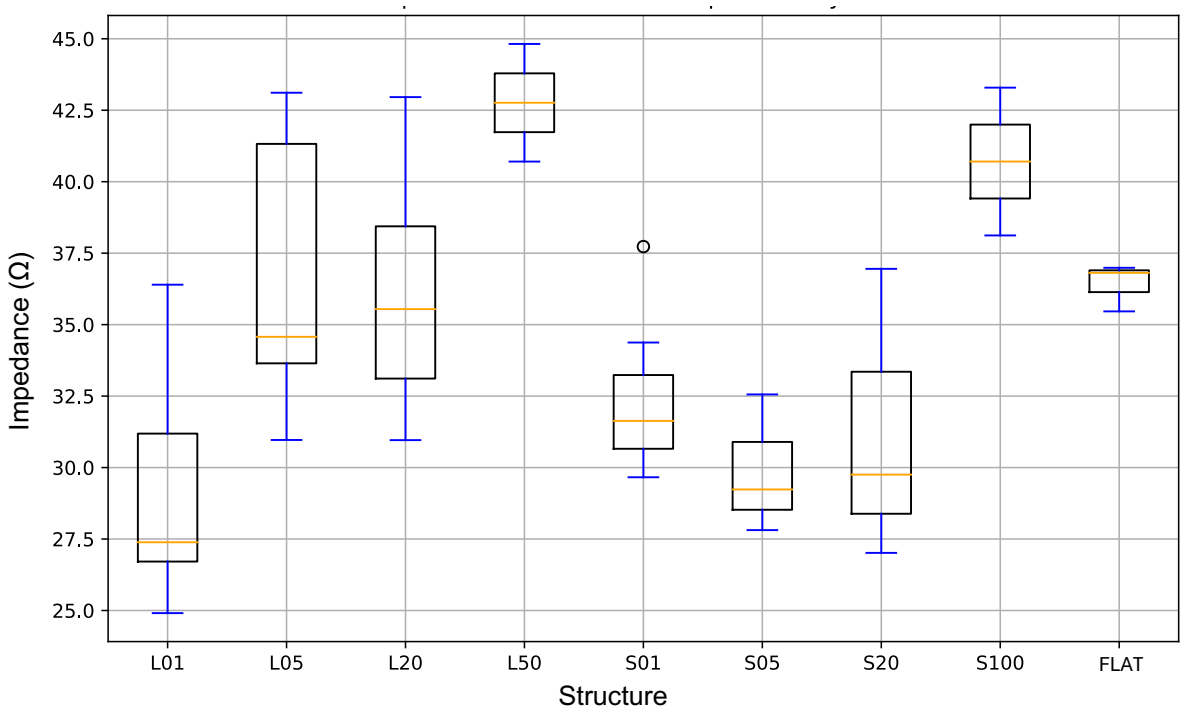

Figure 6.7: Area normalized impedance magnitudes at 1kHz for each structure group (shape and size; $3 \leq n \leq 4$ for each group).

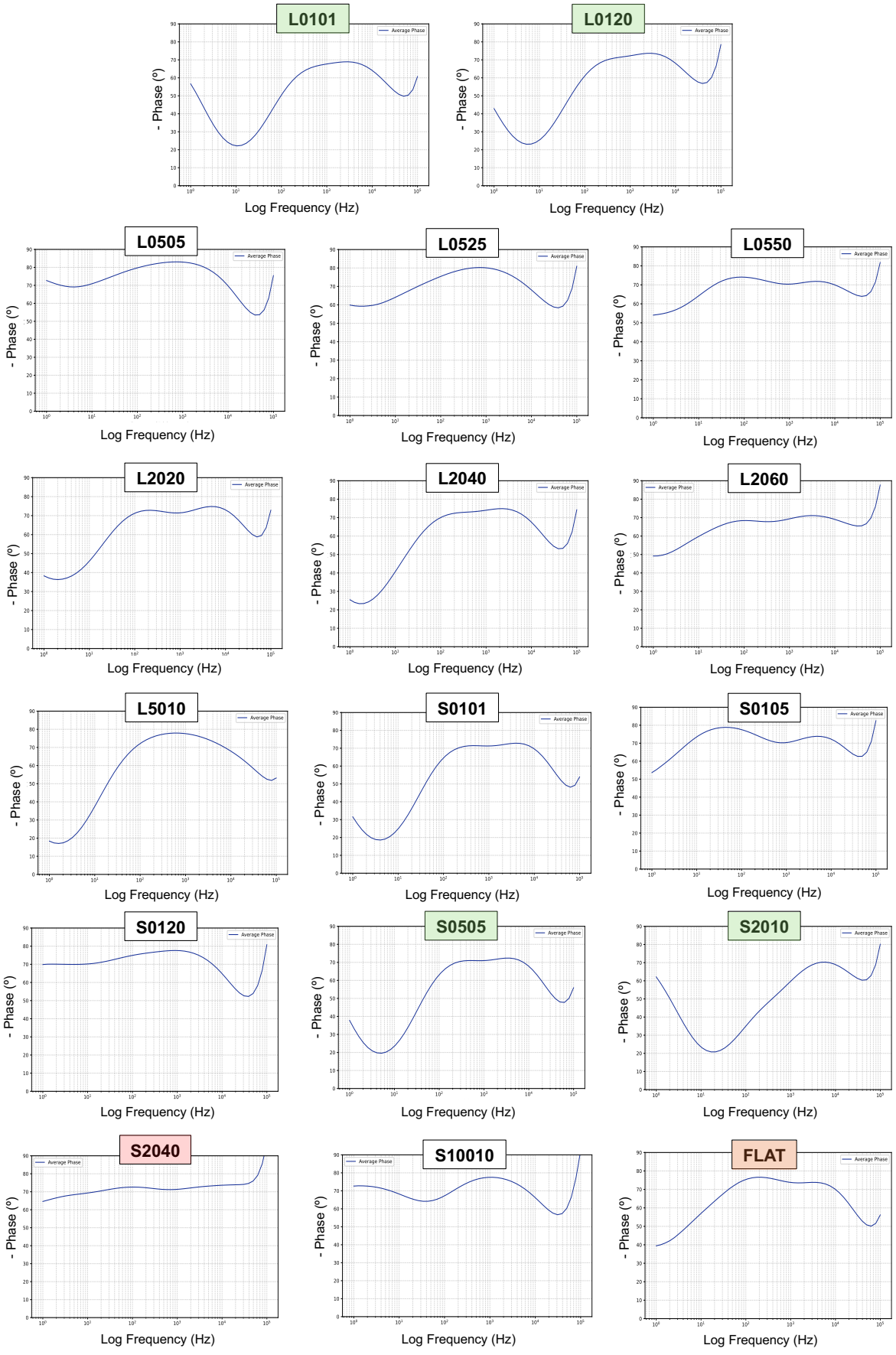

Figure 6.8: Average phase plots for all devices ($3 \leq n \leq 4$). D25 represents the typical phase plot of a delaminated electrode.

6.2.3. Charge Storage Capacity

As has been deduced after the analysis of the previously reported results, the graphene obtained in this work appears to be thin, which would not make it suitable for stimulation applications since the charge storage capacity of electrodes is directly related to the material thickness [168, 169]. Although CV and VT tests are usually performed to characterise neurostimulation electrodes and not to characterise recording electrodes [11], it was considered interesting to perform these tests both to understand the behaviour of the electrodes under charge stimulation and to reaffirm the thing nature of the material.

The CV pilot tests were conducted by varying the voltage from -0.8V to 0.6V, the range previously reported in [101, 130] for conducting CV tests on graphene electrodes. Some of the devices were rendered unusable during the first pilot tests due to severe delamination, stating that the safe range of values for these electrodes was mostly between -0.6V and 0.3V, at $0.1 Vs^{-1}$. This narrower water window might be attributed to changes in the charge carrier concentration due to differences in graphene thickness, which can influence the electrical double layer formed during the electrochemical processes and narrow the water window. Figure 6.9 shows the average cyclic voltammograms of four devices. The difference in hysteresis area highlights the difference in CSC between devices. Table 6.6 shows the average total CSC obtained for the electrodes that survived the test, that was calculated by using the integral of the total hysteresis area, using equation 2.2. Some of the patterns seemed to increase the amount of CSC compared to the flat electrode, these being the patterns that showed the lowest impedance at 1kHz (except device D9). This implies a better interaction of the corrugated patterns with the medium compared to flat electrodes. Device D10 shows a CSC value obtained after delamination of the electrodes. Some of the electrodes of devices D27 and D20 were also damaged, which is reflected in the CSC average.

The maximum value obtained was 80.6 μCcm^{-2}, for device D24, which corrugated structures were dense 20 µm squares. This value is more than one order of magnitude lower than the obtained for MLG electrodes by Babaraud et al. [101] and Rice [130], and three orders of magnitude below typical TiN and Pt electrodes used in neurostimulation [11]. Nevertheless, the highest CSC values presented here appear to be on the same order of magnitude as those obtained by Park. et al. [115], which show 4 stacked monolayer graphene as neurostimulation electrodes that can offer CSC in ranges between 116.07-174.10 μCcm^{-2}.

Overall, **the graphene in the electrodes produced in this work can be considered as relatively thin, resulting in a low charge storage capacity compared to the standard neuroestimulation electrodes. The patterns still seem to influence the performance, showing a possible increase in CSC compared to completely flat electrodes.** Nevertheless, further analysis is needed to extract solid conclusions on whether this type of material can be effective in neurostimulation.

Table 6.6: Average Total CSC obtained for some devices at a scanning rate of 0.1 Vs^{-1} and a water window of -0.6 V to 0.3 V.

Device	Structure	Total CSC (μCcm^{-2})
D7	L0101	69.50
D9	L0120	46.29
D10	L0505	4.13
D11	L0525	24.65
D12	L0550	30.14
D13	L2020	34.85
D14	L2040	60.26
D16	L5010	59.82
D20	S0120	14.31
D21	S0505	76.70
D24	S2010	80.60
D27	S10010	10.08
D29	-	31.56

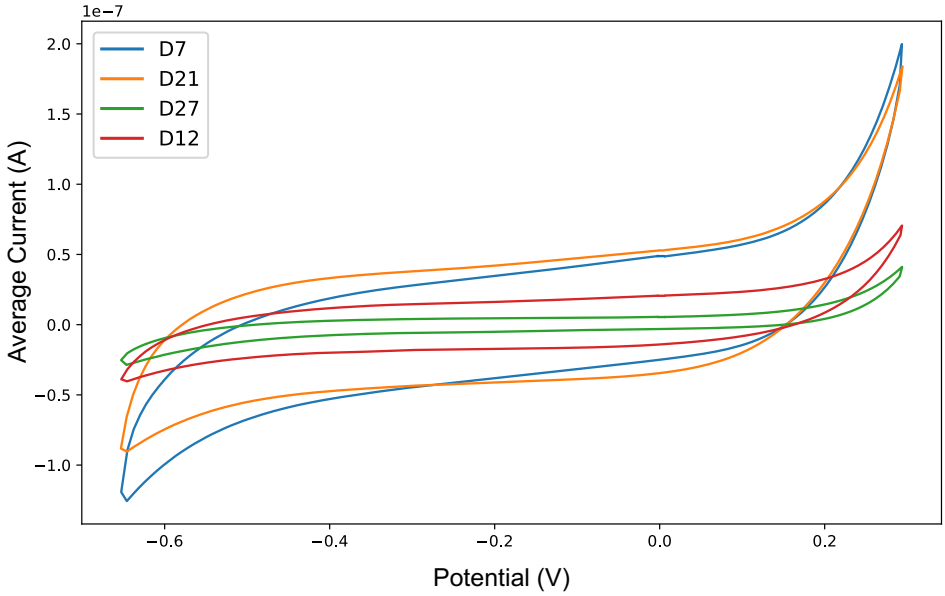

Figure 6.9: Cyclic voltammograms obtained for devices D7, D12, D21 and D27.

6.2.4. Charge Injection Capacity

Voltage transient tests were performed for some of the electrodes to have an estimation about the range of maximum charge injection capacity that these type of electrodes can support. The water window of the electrodes determines the maximum amount of safe current that the electrode can inject. For this particular electrodes, the safe voltage range was estimated to be between -0.6 and 0.3 V, as depicted from the cyclic voltammograms.

VTs were performed for the same devices for which the CSC data was extracted. During these tests, many of the electrodes also suffered damage due to incorrect polarisation with the reference electrode which was caused by a bubble created right on the surface of the reference electrode. Several electrodes from various devices were rendered unusable after this error. Figure 6.10.a represents the biphasic pulses applied to the electrodes, which ranged between 4µA and 7 µA, while Figure 6.10.b shows the average voltage transient for some of the devices. For most of the devices, the maximum current amplitude that can be applied to the electrodes without exceeding the water window does was 7 µA. D14 and D20 curves show the representative curve of most healthy electrodes, whose VT is around -0.6 and 0.3V after applying a biphasic current of 7 µA. On the other hand, D11 and D25 curves show devices whose electrodes had been previously damaged, whose VT exceeds the water window even when applying currents of 4 µA and 5 µA, respectively. The maximum CIC was therefore calculated using equation 6.1, and considering $I_{max} = 7\mu A$.

$$CIC_{max} = \frac{I_{max} t_c}{Area} = \frac{7\mu A \times 10^{-3} s}{90792 \times 10^{-8} cm^2} = 7.71 \frac{\mu C}{cm^2} \tag{6.1}$$

A maximum of 7.71 µC/cm^2 was obtained for the electrodes fabricated in this work. This value is considerably low compared to the pristine multilayer graphene electrodes obtained by Babaroud et al. [42], where the maximum CIC obtained was 44 µC/cm^2, and to the platinum electrodes evaluated in the same work, which could deliver CIC values of 67.33 µC/cm^2. The CIC value of an electrode, as the CSC, is directly dependent on the material thickness [170], making the low CIC values meaningful considering the fine FLG nature of the electrodes manufactured here. More statistical data is needed to understand how the corrugated structure influences the CIC, but as mentioned in the previous section, the electrodes do not seem to meet the values found in the literature for neurostimulation.

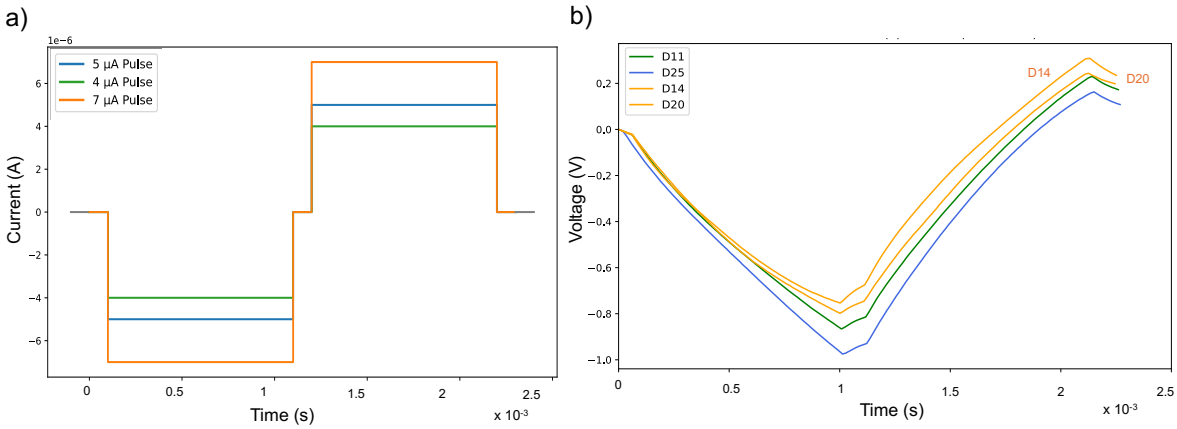

Figure 6.10: a) Biphasic currents. b) Voltage transients.

6.3. Biocompatibility Tests

6.3.1. Cell Expansion and Pilot Test

As explained in Section 3.5, cell expansion was performed for different seeding densities: 3K/cm^2, 6K/cm^2, 10K/cm^2 and 20K/cm^2. Figure A.13 (see Appendix A) shows the results for days 0, 3 and 7 per each of the densities used. As can be seen, for the 3K/cm^2 concentration on day 7 there are still quite a few gaps between cells, determining that the cells were non-confluent. Conversely, for 10K/cm^2 and 20K/cm^2 the cells were confluent even at day 3. At 6K/cm^2 seeding densities the cells can be considered as confluent at the day 7 but not at day 3. This concentration was selected for the final tests to avoid cell overgrowing.

For the pilot life/dead assay test, 10K/cm^2 and 20K/cm^2 concentrations were tested to ensure enough cell-substrate interaction. Figure 6.11 shows the results of the life/dead assays performed using the big test samples and the control wells. As can be seen, proliferation was successful, as more cells can be depicted at day 7 compared to day 0. Moreover, the high abundance of green staining indicates that most of the cells are alive. The reader should note that if the substrate were cytotoxic, one would have expected a large number of dead cells at day 7, and much more red staining. In addition, a cellular response to the substrate seems to be perceived, as it appears that the cells are aligned with the pattern, which in this case was wide lines. Overall, it seems that the cells seed on the samples are more organised than in the control seeding. From this first pilot test it can be deduced that the samples are biocompatible. Further testing was performed on the samples with smaller structures.

6.3.2. MTT and Presto blue assays

For addressing the MTT assays results, the intensity of the formazan purple color, product of viable cells, was measured by absorbance. The number of samples was: n = 5 for negative control (wells without samples, and dead cells), n= 5 for positive control (wells without samples, and living cells), and n = 5 for experiments with samples. Figure 6.12.A shows the normalized absorbance obtained at 12h and 72h for the samples and controls, and their averages. The absorbance obtained for the first 12h reflects the initial metabollic response of the cells to the experimental conditions. The absorbance obtained at 72h is normalized with respect to the absorbance measured at 12h. This point shows an increase in absorbance, both for the control and the sample wells, which suggests that cells proliferated and remained viable. Additionally, no significative differences were observed between the control and the sample wells, indicating that the samples did not interfere on cell viability.

Regarding the Presto blue assays, Figure 6.12.B shows the normalized fluorescence values obtained for days 0, 3 and 7. The number of samples was: n = 5 for control, n = 5 for experiments with samples. An increase in the fluorescence values can be observed, indicating that the cells are viable, proliferating, and metabolically active. Again, the non-significative differences imply that the exposure to the samples has no adverse effect.

Results obtained for MTT and Presto blue assays indicate that the samples are not cytotoxic. Graphene remained successfully attached to SiO_2 throughout the assessment (see Figure A.14.C).

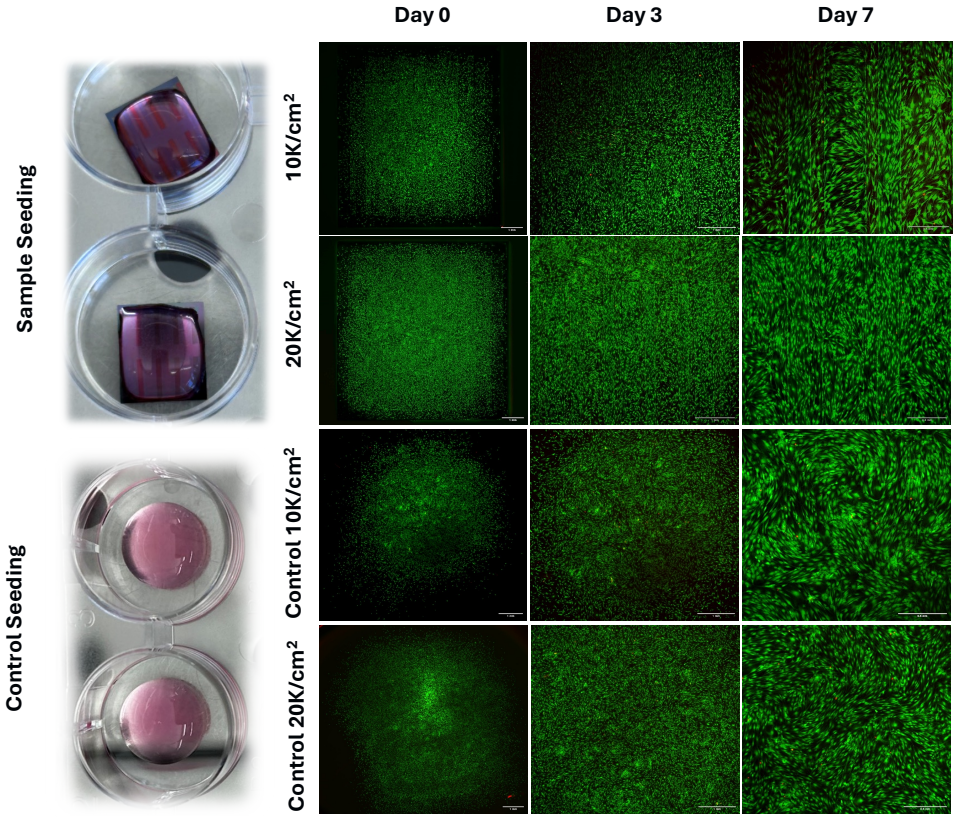

Figure 6.11: Pilot experiment conducted on two big samples encapsulated with SU8, and control. Scale bar days 0 and 3: 1mm. Scale bar day 7: 0.5mm.

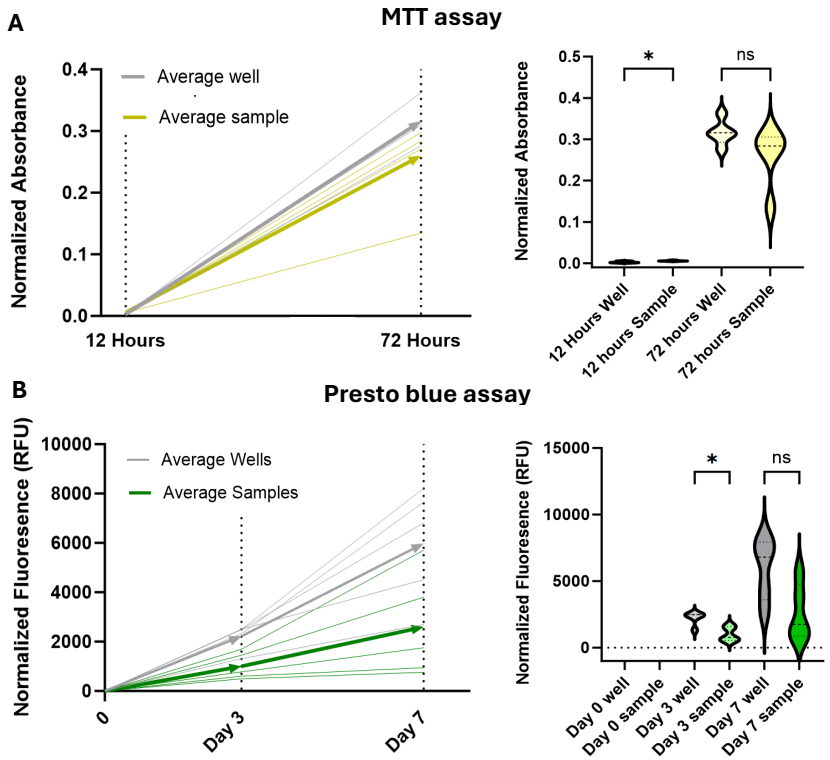

Figure 6.12: A) MTT assay normalized absorbance, measured at 12h and 72h. B) Presto blye normalized fluorescence, measured at days 0, 3 and 7.

6.3.3. Live/Dead assay and Dapi/Phaloidin

In live/dead measurements, green fluorescence stain indicates membrane integrity and metabollic activity, while dead cells are usually stained in red, representing compromised cell membranes. Figure 6.13.A shows the results of the fluorescence measurements obtained for days 0 and 7. An significant increase in the green fluorescence can be observed, while red satined structures are almost neglectible, suggesting that the cells are alive, healthy and proliferating with little to no cytotoxic effect generated by the samples. Figure A.14.A (see Appendix A) shows the live/dead assays performed for the control samples. An alignment of the cells generated by the samples is evident when comparing Figure 6.13.A and Figure A.14.A, suggesting that the cells interact with the sample and patterned areas. Further analysis is needed to understand the orientation effect that the structures might have on cells, and to relate the pattern shape, size and density with celullar responses.

Dapi phaloidin assays results were analysed by extracting flurescence images. Figure 6.13.B shows the images obtained for days 0 and 7, where the nuclei of the cells are stained in blue, while the F-actin in the cytoskeleton is observed in yellow. By observing both components, it can be concluded that the cells are proliferating over time, and that the cell morphology and integrity are preserved. Additionally, comparing the results obtained for the samples with the control results (see Figure A.14.B, Appendix A) again an evident orientation response in the cells generated by its interaction with the sample is evident, generating the sample changes in the cell's cytoskeleton.

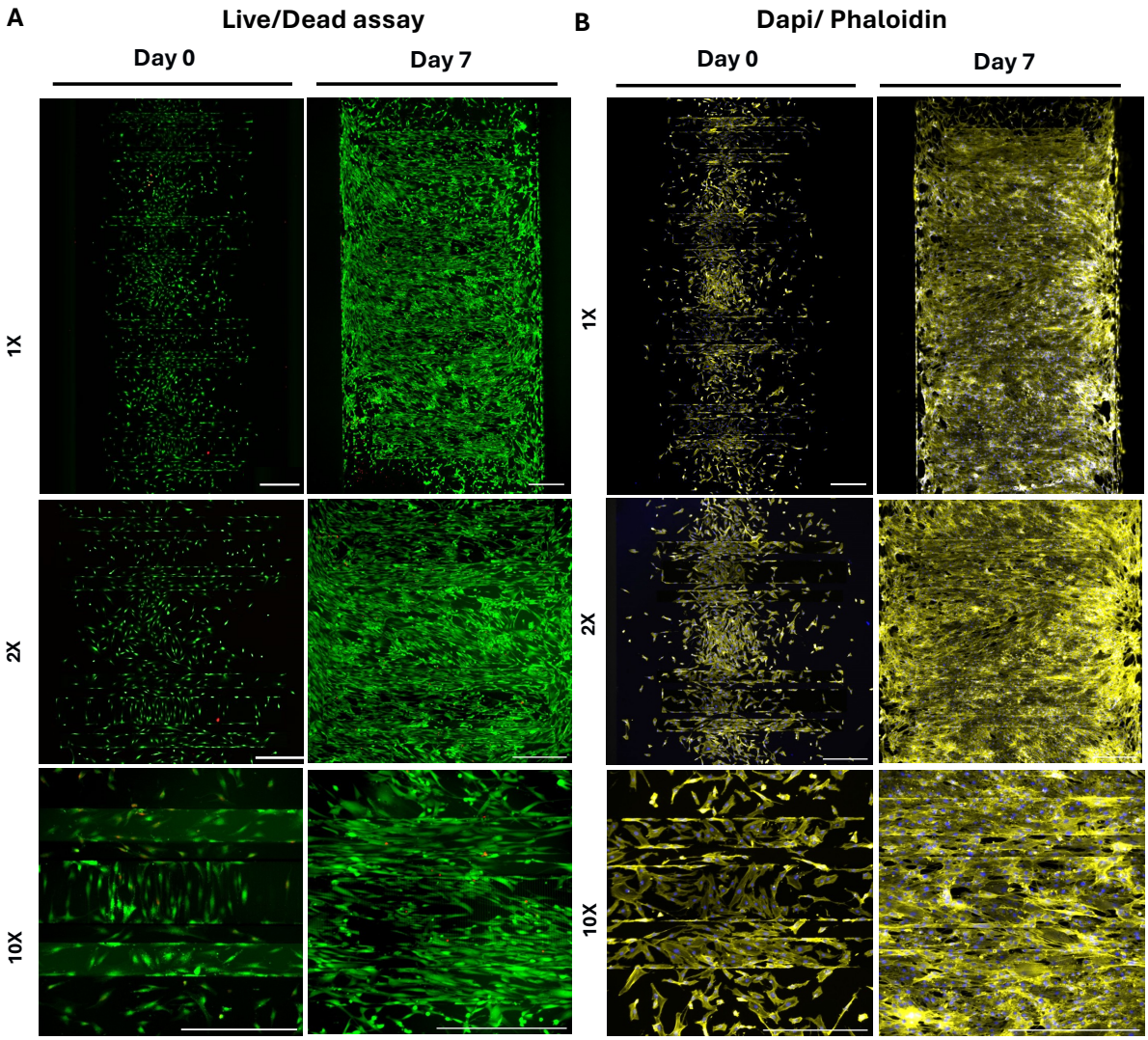

Figure 6.13: A) Live/Dead assay images obtained at different days and magnifications. B) Dapi/Phaloidin assay images obtained at different days and magnifications.

6.4. Summary of Corrugated Structures and Device Characterization

The results of this chapter lead to the following conclusions:

- The properties of graphene synthesised on SiO_2-corrugated wafers 239 and 076 show a low sheet resistance, raging 60 Ωsq^{-1} - 180 Ωsq^{-1}. These low values are attributed to the combination of an FLG graphene with good interlayer electronic coupling, which is possible due to the low number of defects in the material. A transfer-free process for this type of material has enabled its properties to be effectively preserved.
- Sheet resistance values are pattern-dependent: line patterns exhibit higher sheet resistance than square or flat configurations. This increase is due to the greater vertical distance electrons must travel in line patterns, causing more resistance. In other words, less corrugated structures show lower sheet resistance, likely due to reduced electron scattering, which enables a more efficient conduction pathway.
- Electrochemical impedance values are pattern dependendent. All square pattern densities of 1µm, 5µm and 20µm improved the impedance values with respect to the flat electrodes at 1 kHz. In the case of the lines, the 1µm patterns provided lower impedance values than the flat electrodes. Considering the 5µm and 20µm lines, only the denser ones provided lower values compared to the flats.
- In general, impedance values at 1 kHz present values in the order of tens of kΩ, which is way lower that the 1 MΩ that electrodes for neural recording can potentially exhibit. These results are positive for potential application in neural recording modalities.
- Considering the maximum CSC and CIC values, electrodes are not considered particularly suitable for neurostimulation, which is certainly meaningful due to the fine nature of the graphene synthesised in this work. Even if corrugations are present in SiO_2, the primary limitation for stimulation properties of the electrodes is the thickness of the material driving the electrochemical reactions, namely, graphene. Additionally, only a few electrodes survived to extract statistics in that can relate the CSC and CIC values with the pattern variation. More data is therefore needed to generate a proper correlation between patterns.
- Structures generated in this work have proven to be biocompatible and potentially supportive of cell health. Graphene remained successfully attached to the SiO_2 substrate throughout biocompatibility evaluation.
- Stem cells have shown morphological and structural integrity. Additionally, they seem to respond to the patterned substrates, meaning that cells can adapt to the substrate by responding to topography changes, without applying an external stimulation. Nevertheless, more research is needed in this respect.

7

Conclusions and Future Work

7.1. General Conclusions

In the initial phase of this work, efforts were directed towards achieving transfer-free fabrication of thin graphene. Insights gained from these preliminary experiments provide valuable understanding of the mechanisms governing graphene growth on molybdenum. The graphene obtained on patterned thick molybdenum is multilayered, being this characterised by high I_D/I_G ratios, indicating a significant presence of defects. Additionally, the phenomenon termed ”carbon fences” is observed — a feature not previously reported for MLG transfer-free graphene grown on thin substrates, indicating a difference in the growth. This observation implies that graphene growth on thick substrates is influenced by both the primary surface and the four planes perpendicular to it. Conversely, graphene grown on thick but unpatterned substrates shows distinct characteristics, with Raman analysis revealing low I_D/I_G ratios and I_2D/I_G ratios higher than 1, suggesting fewer layers. This suggests that consider non-patterned Mo provides a unique surface source for carbon atoms that can help creating a more homogeneous and less defective graphene in comparison with patterned catalysts. High quality thin graphene can also be patterned after growth, the main limitation being the etching of the molybdenum underneath. In addition, graphene grwoth in the whole wafer generates stresses that may compromise the following steps. In any case, this may be a process to explore for synthesising transfer-free thin graphene with flexible polymers as the graphene can be bonded to them and molybdenum etching can be considered from the back side of the wafer.

The creation of corrugated graphene structures was also explored in this work. Graphene grown on different patterned, corrugated molybdenum structures does not seem to show differences in number of layers or quality when comparing the graphene synthethised on the top and on the bottom of the structures. However, a difference in the roughness is depicted, which can be attributed to the differences in the catalyst thickness and surface roughness. Additionally, graphene coming from the structures patterned with the smaller and denser lines patterns seem to maintain topographical, nanometric changes, as the graphene collapsed following the shape of the pattern. Since it was not considered convenient for this work, this small variations where not further studied, but it is encouraged to study their properties for further understanding of graphene synthesis on molybdenum and the transfer-free process.

In this work, we successfully demonstrated that is possible to create continuous, corrugated graphene structures in a transfer-free way. This was possible considering the corrugation patterns on the SiO_2. From this experiments, several outcomes can be depicted. First, properties of CVD graphene grown on molybdenum are directly dependent on the SiO_2 surface. In comparison to the top of the structures, the SiO_2 ”valleys” or bottom of the structures showed low Raman I_D/I_G ratios, related to higher quality, and high I_2D/I_G ratios, typically encounter on fewer layer graphene. This can be mainly associated to the lower exposure to carbon atoms at the valleys due to the smaller number of planes exposed to the gas (and lower exposure to the precursor) which might generate a more homogeneous growth (therefore low-defective) and thinner graphene. Additionally, there is a possibility that the molybdenum grains also show different characteristics on the valleys. This should be further studied.

The graphene grown on corrugated SiO_2 showed low sheet resistance values, ranging from 60 to 180 Ω/sq, ranking these values among the lowest in comparison to the literature. These low Rs

values were mainly attributed to the low defective graphene together with the combination of an FLG graphene with good interlayer electronic coupling. Sheet resistance values seem to be dependent on the pattern, showing the squares and flat structures lower values than the grooves due to a reduced electron scattering and more efficient conduction pathways.

Corrugated structures were successfully implemented in electrodes designed for neuroelectronic applications. Considering electrochemical testing, all the square 1µm, 5µm and 20µm dense corrugations increase the surface area of the electrode, reducing their impedance (32.9 kΩ - 37.8 kΩ) when comparing it to a flat electrode (≈ 39 kΩ). Additionally, the lowest impedance values were obtained for small, dense lines, the lowest value being 28.8 kΩ. These results are promising, as they reflect an increase in the surface area of the electrode without the need of adding external materials, as nanoparticle coatings, and without increasing the diameter of the electrode. Overall, the results obtained for impedances at 1 kHz are promising for potential application of the electrodes in neural recording. On the other hand, CSC and CIC were low in comparison with the required values for stimulation electrodes, showing values of 80.6 µC/cm² and 7.71 µC/cm², respectively. Even if corrugations are present in SiO_2, the primary limitation for stimulation properties of the electrodes is the thickness of the material driving the electrochemical reactions, namely, graphene. More statistical analysis of how corrugation patterns affect these two values is needed.

Lastly, the samples fabricated in this work have proven to be biocompatible. The results of four types of tests assessing cell activity, proliferation and morphology of human-derived periosteum stemm cells demonstrate that corrugated graphene patterns are not cytotoxic, and that they may have the potential to generate a response in the cytoskeleton of stem cells.

7.2. Future Work

Further study of graphene on corrugated patterns

As the corrugated material fabricated in this work has not been previously reported, it is relevant to further study the properties of the graphene. For this it would be interesting to extract more statistical data obtained from TLM structures and devices fabricated following the flowchart without varying molybdenum thickness. Additionally, comparing further study how graphene properties change depending on the corrugated structures is also of relevance. Furthermore, a complete analysis of the SiO_2 surface, together with the deposited molybdenum on the valleys and the top of the corrugated SiO_2 should be convenient in order to associate or discard graphene properties with molybdenum characteristics variation. In general, further electrochemical testing is also convenient to understand how the patterns can affect the CSC and the CIC. The creation of nanometric size corrugated patterns can further increase the electrode area, as well as generate step heights in the order of micrometres. Both approaches are promising for increasing the amount of material to be synthesised. From the experiments performed in this work, it is known that a continuous graphene layer can be created on corrugated surfaces, so that the corrugation parameters can be played with. In addition, a process of transferring corrugated graphene to glass substrates can be considered to study its response in the visible range, thus allowing further data on the nature of graphene to be extracted.

Developing new approaches for neural interfaces

Given the good electrical properties of the graphene synthesized on corrugated SiO_2, this approach can be applied for the generation of transfer-free graphene based neural interfaces. The low sheet resistance values can enable high-density optically transparent neural interfaces using graphene tracks, allowing to overcome one of the most relevant limitations. Considering step heights in the order of micrometres can be interesting to increase cell interaction, even if the continuous layer of graphene is only that of the valleys and continuity is lost in the walls of the structures. Increasing the contact surface with the neurons already increases the chances of a successful interface. Another application can be considering transistors for neural recording. A flowchart is proposed for the fabrication of transfer-free, graphene-based Solution-Gated Field Effect Transistor (SGFET), interface that can provide high SNR for neural recordings (see Figure 7.1). As can be seen in the flowchart, the corrugations are still maintained in SiO_2. The molybdenum is deposited and the graphene is grown by CVD, analogous to the work done in this project. In addition, the creation of the drain and the source of the transistor is also done by gold lift-off. A first encapsulation is then made with SU8, a photosensitive and biocompatible polymer. Aluminium deposition is necessary to provide the possibility to work from the back-side of the

wafer. Si and SiO2 are then etched, leaving the molybdenum exposed, which is removed by wet etching with H2O2. An encapsulation of the backside with SU8 is considered, followed by UV lithography, which does not affect the graphene. The device is released after removal of the front-side aluminium. Other approaches using other polymers as encapsulation may also be of interest, such as parilyne-C or polyamide.

Cell/substrate interaction considering neuronal tissue

Considering the biocompatibility tests with hDPSC, further analysis of the cells response to the patterns should be convenient to understand which type of pattern can potentially provide better tissue-substrate interaction. It should be also convenient to test devices in brain slices to calculate the SNR that might be dependent on the corrugated pattern of the electrode. Considering testing with neural tissue, further study of the interaction of neurons with the corrugated patterns are strongly recommended in order to understand the cell response for this particular type of cells.

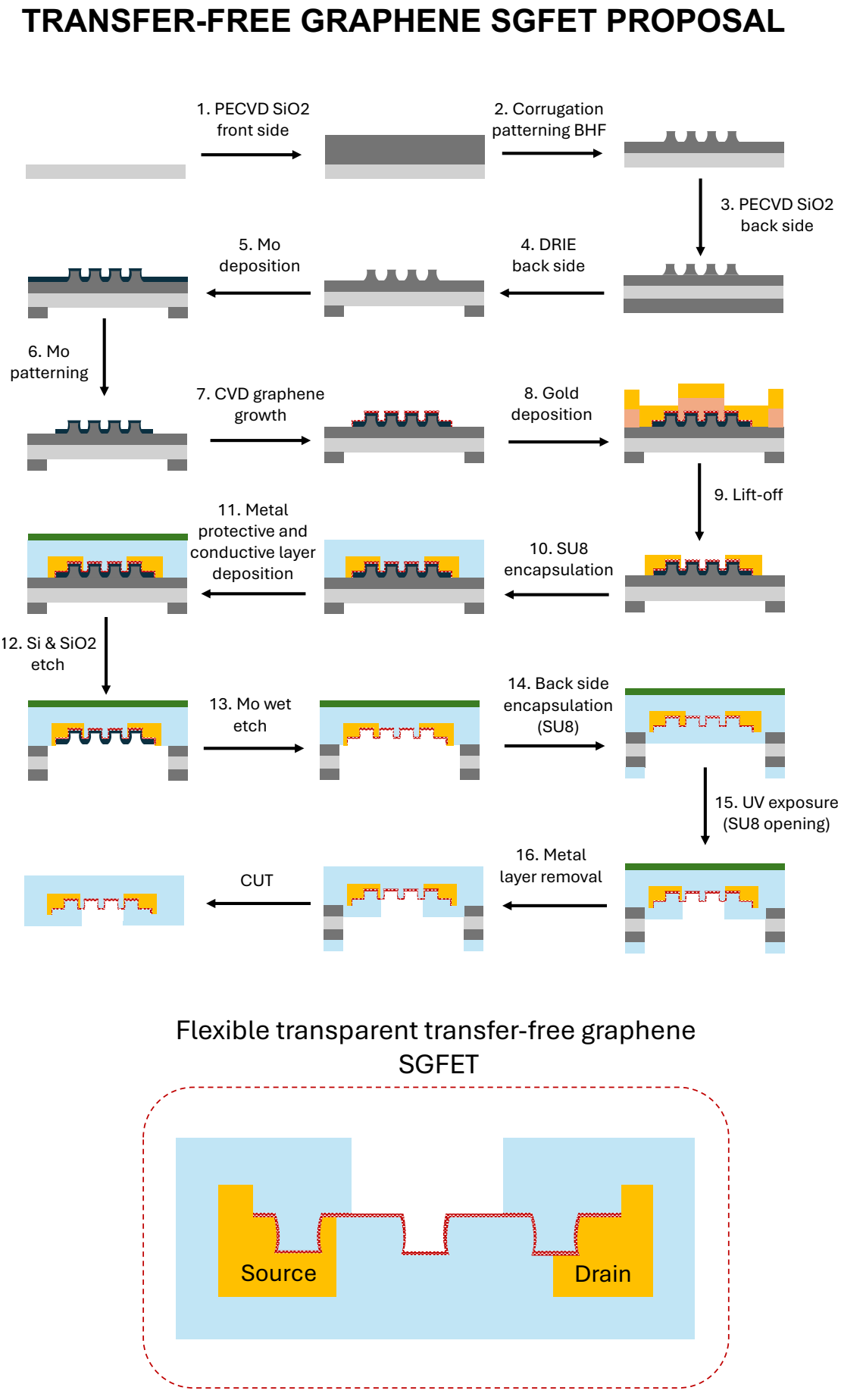

Figure 7.1: SGFET proposal using corrugated graphene structures.

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Appendices

A

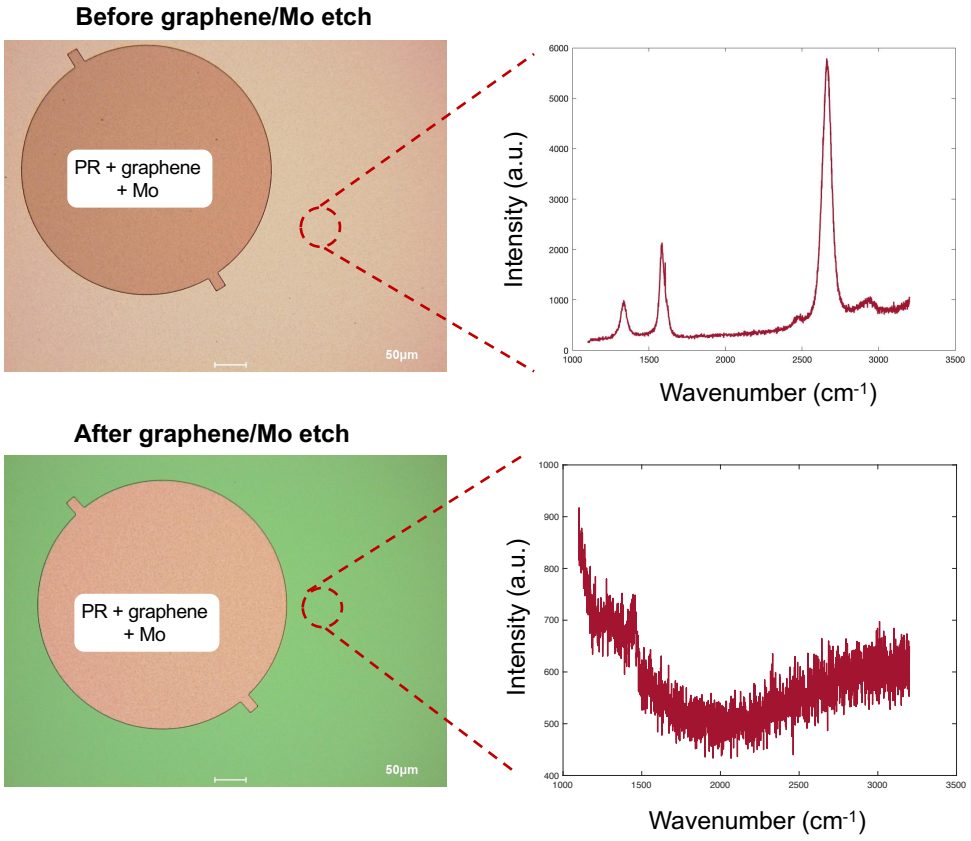
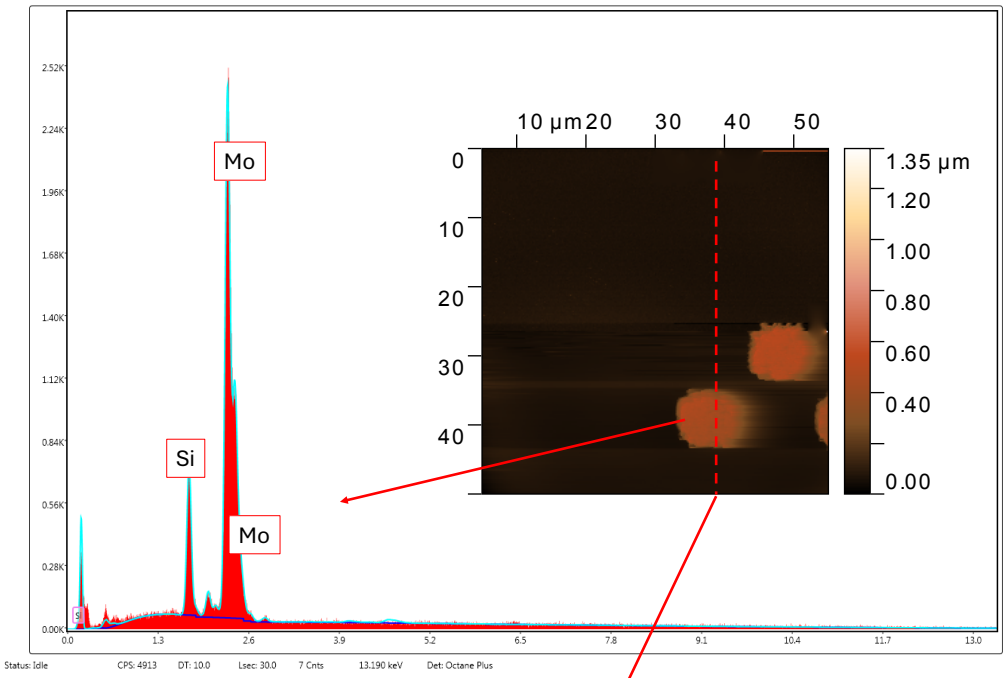


Figure A.1: Wafer with graphene grown on a non-patterned Mo, before and after performing the patterning of both graphene and Mo, and the respective Raman spectrum obtained for the non patterned area before and after etching graphene and molybdenum.

Table A.1: Sheet resistance values obtained for the structures that survived metallisation of wafer with corrugated patterns on Mo.

Structure	R_{L1} (Ω)	R_{L2} (Ω)	R_{L3} (Ω)	R_{L4} (Ω)	Rs/W ($\Omega sq^{-1}\mu m^{-1}$)	Sheet resistance (Ωsq^{-1})
S0105	722.14	800.34	1045.08	2062.97	1.61	483
S0505	429.88	547.14	1050.79	1377.31	1.18	354
S0120	400.28	843.70	1181.47	2376.11	2.29	687
S0525	1538.11	829.40	1474.55	3497.86	2.61	783
S2010	483.84	622.22	829.40	1279.77	0.95	285



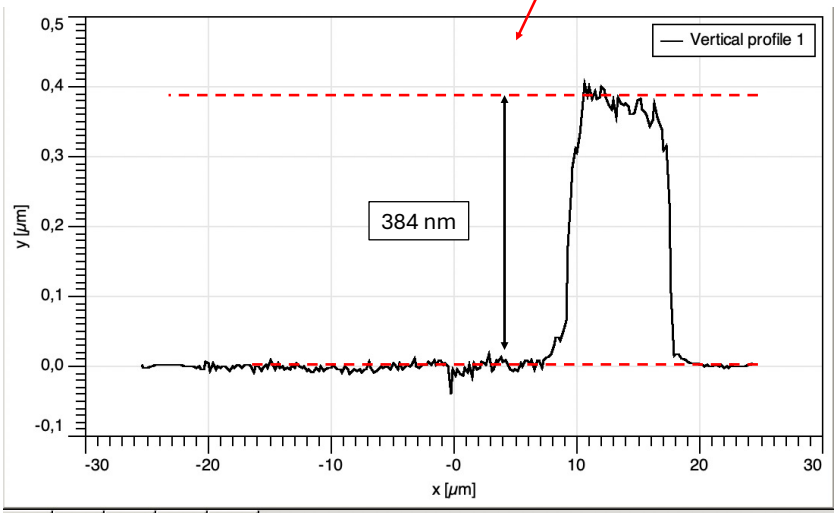


Figure A.2: EDX and AFM measurements performed for the sample patterned after FLG growth, after performing 7 mins of wet etch which remved ≈ 115 nm of Mo.

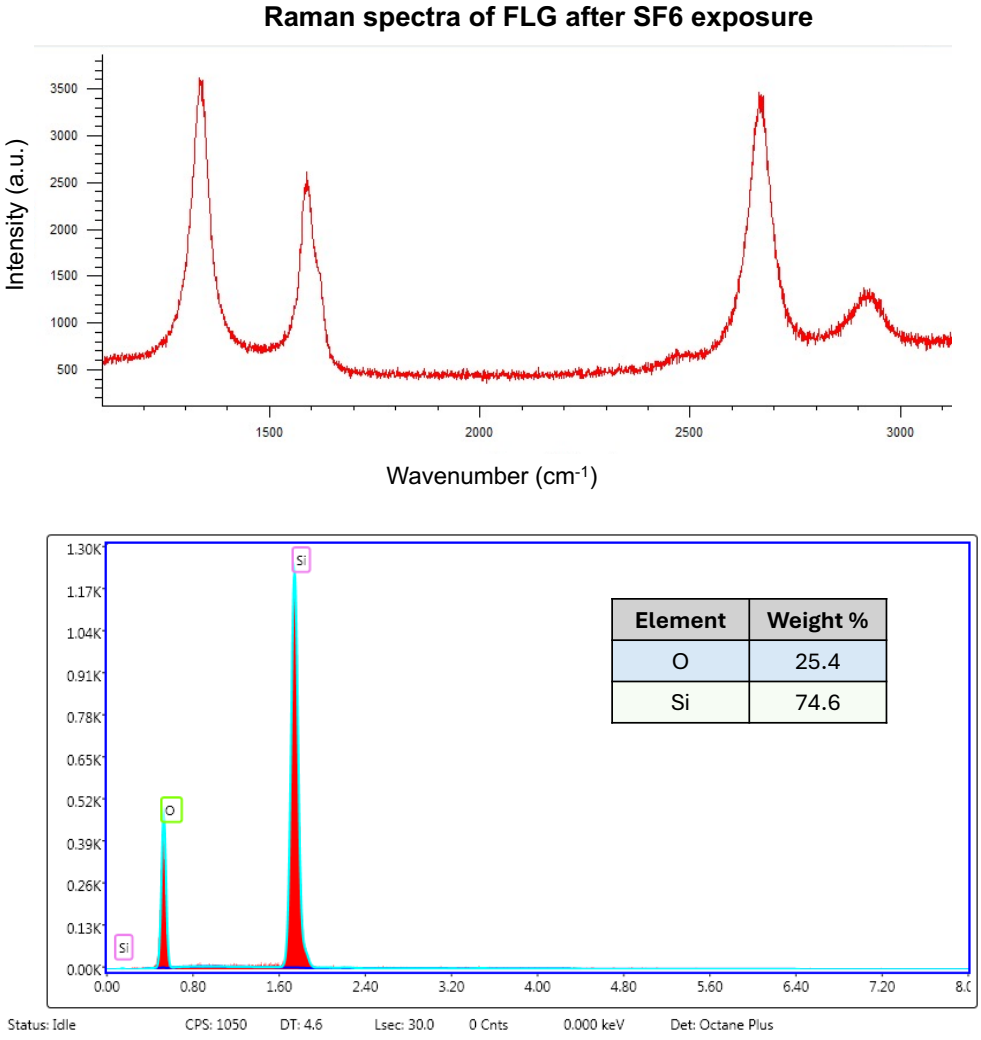


Figure A.3: Raman spectra and EDX obtained for the sample exposed to 7 minutes of wet etching (using H2O2) and 25 minutes of dry etching (using SF6 with a power of 1500 W and 200 sccm).

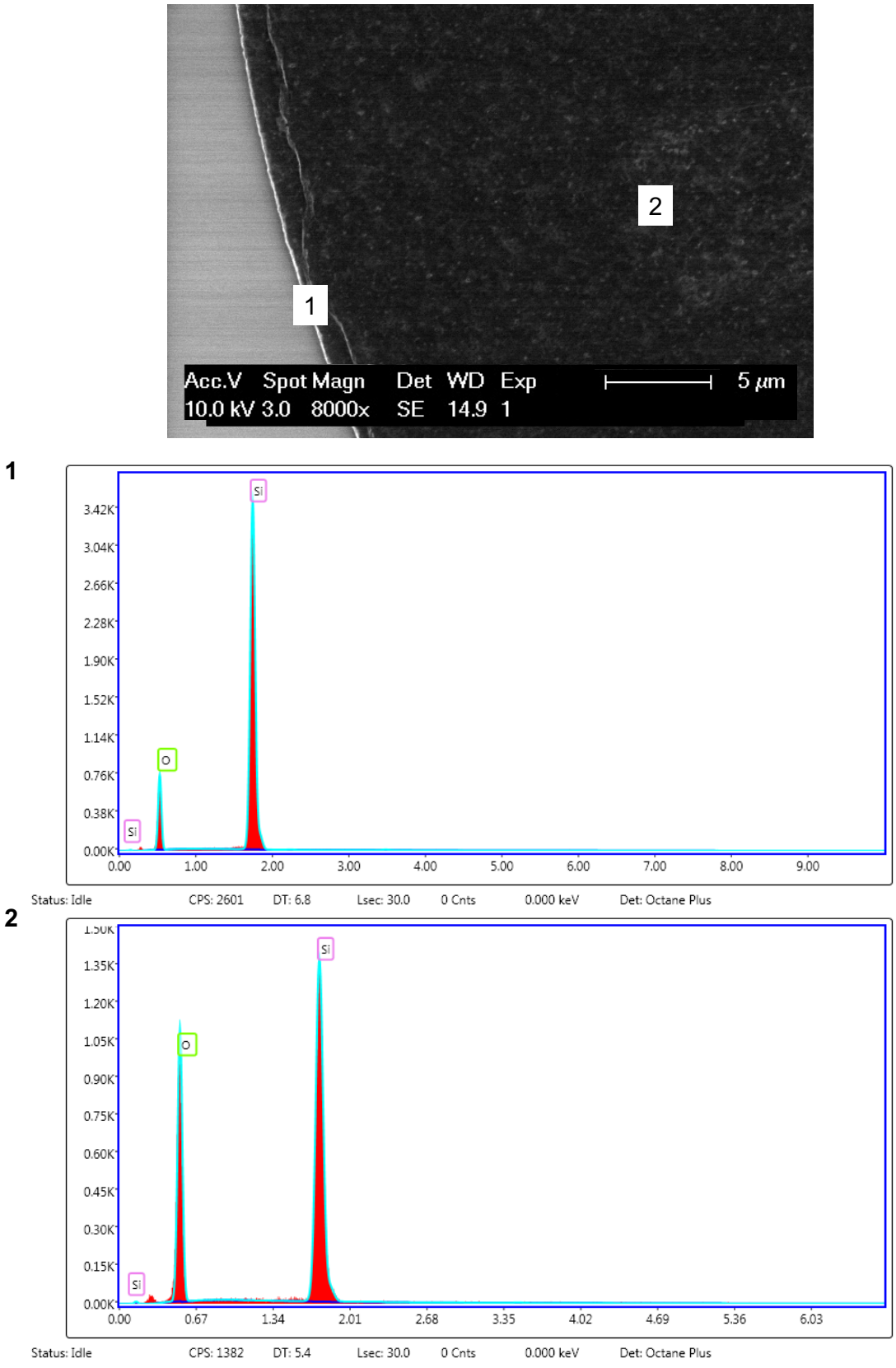


Figure A.4: SEM, EDX and Raman analysis of graphene grown on Mo bulk patterned, after performing Mo wet etch with H2O2.

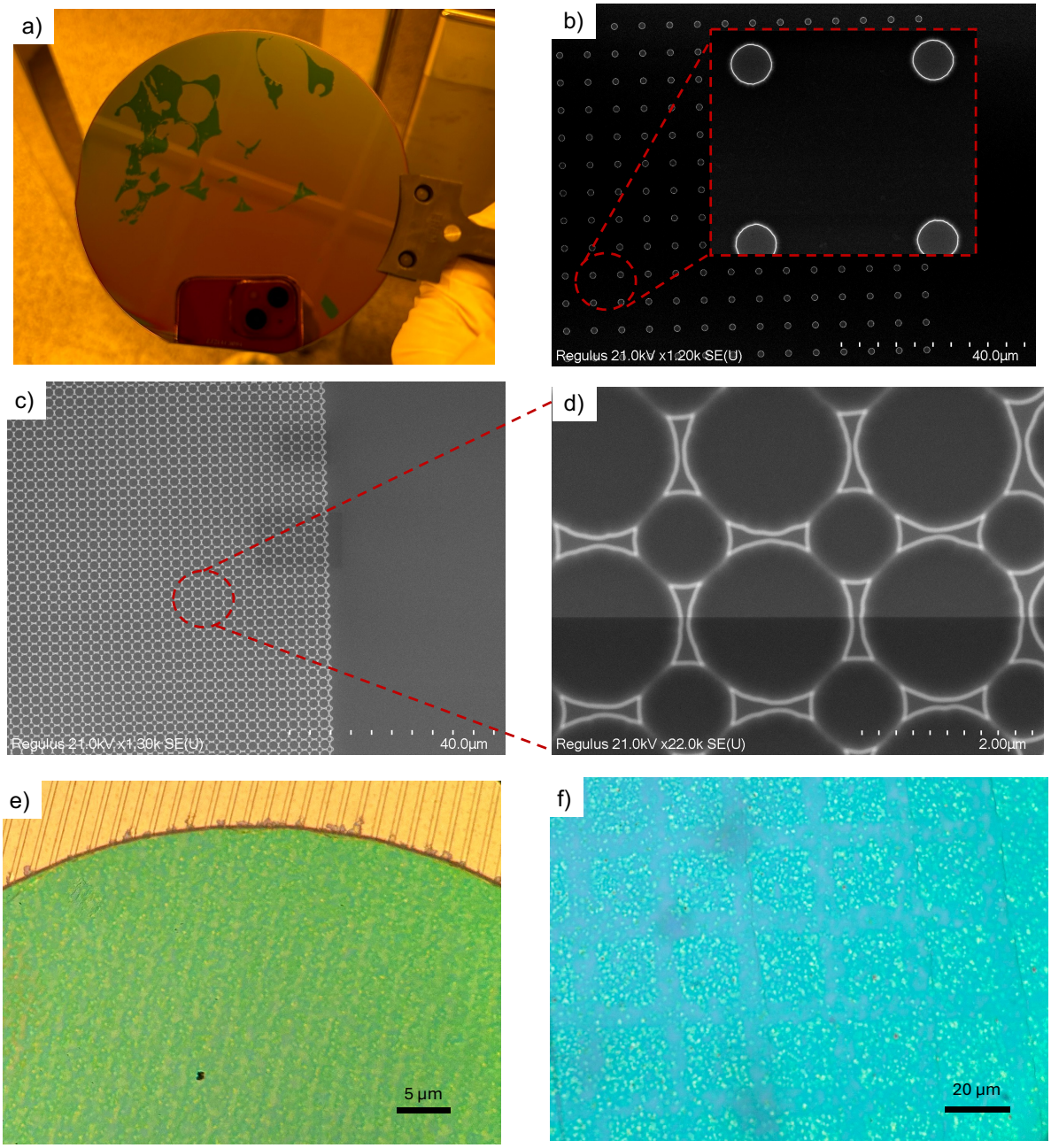


Figure A.5: a) Wafer with photoresist after hard contact exposure. Photoresist sticked to the glass mask during the hard contact exposure procedure. b)

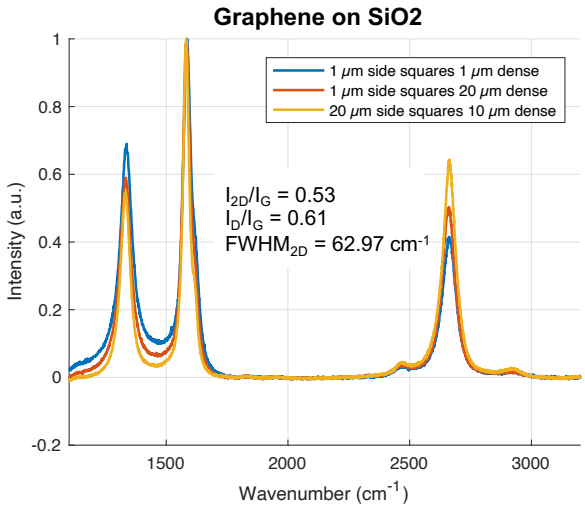


Figure A.6: Raman spectra obtained for some of the graphene on SiO2, synthesised on corrugated Mo substrates after performing Mo wet etch.

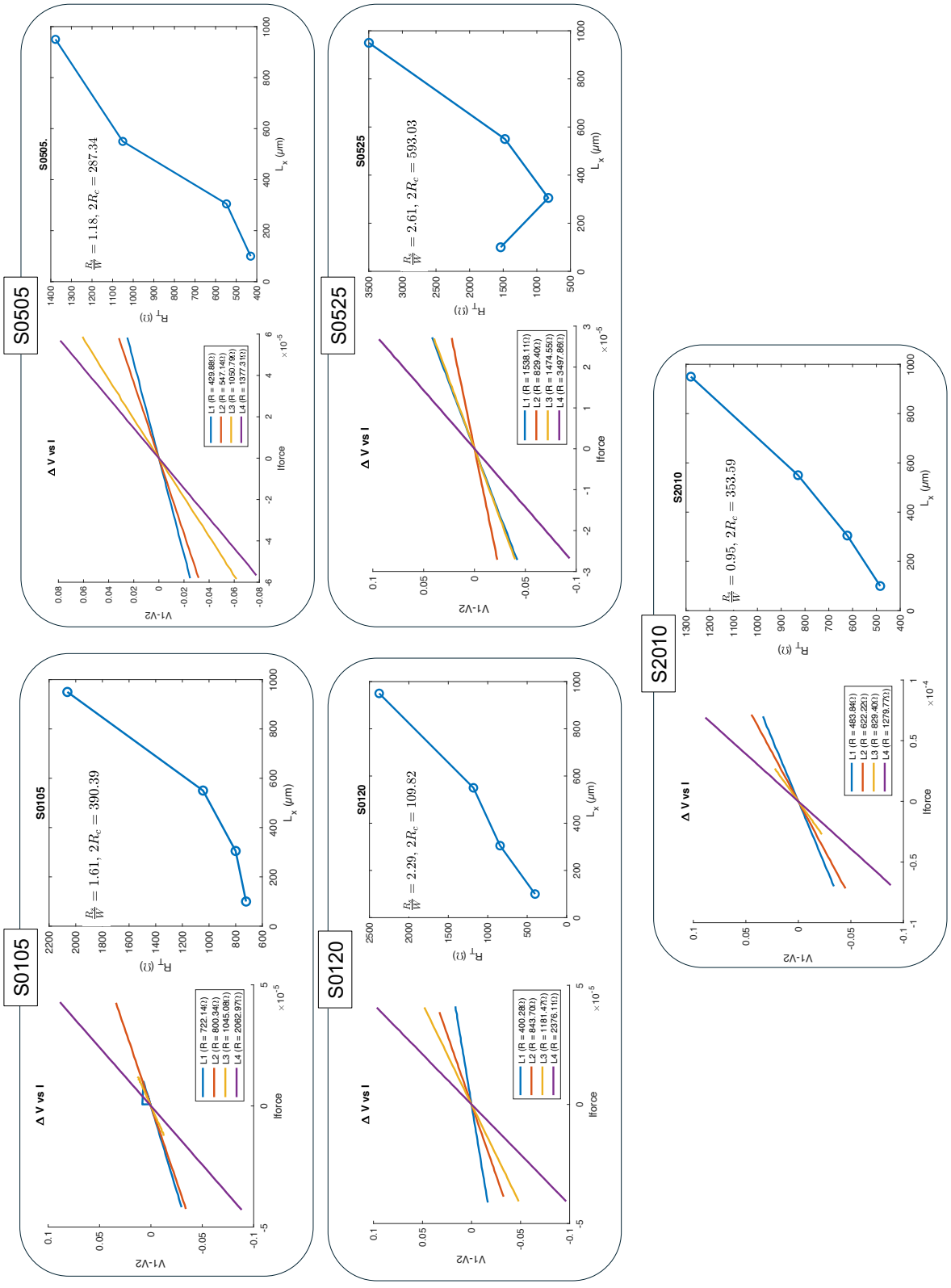


Figure A.7: Graphs obtained from the TLM measurements, used to calculate the sheet resistance values obtained for the structures that survived metallisation of wafer with corrugated patterns on Mo.

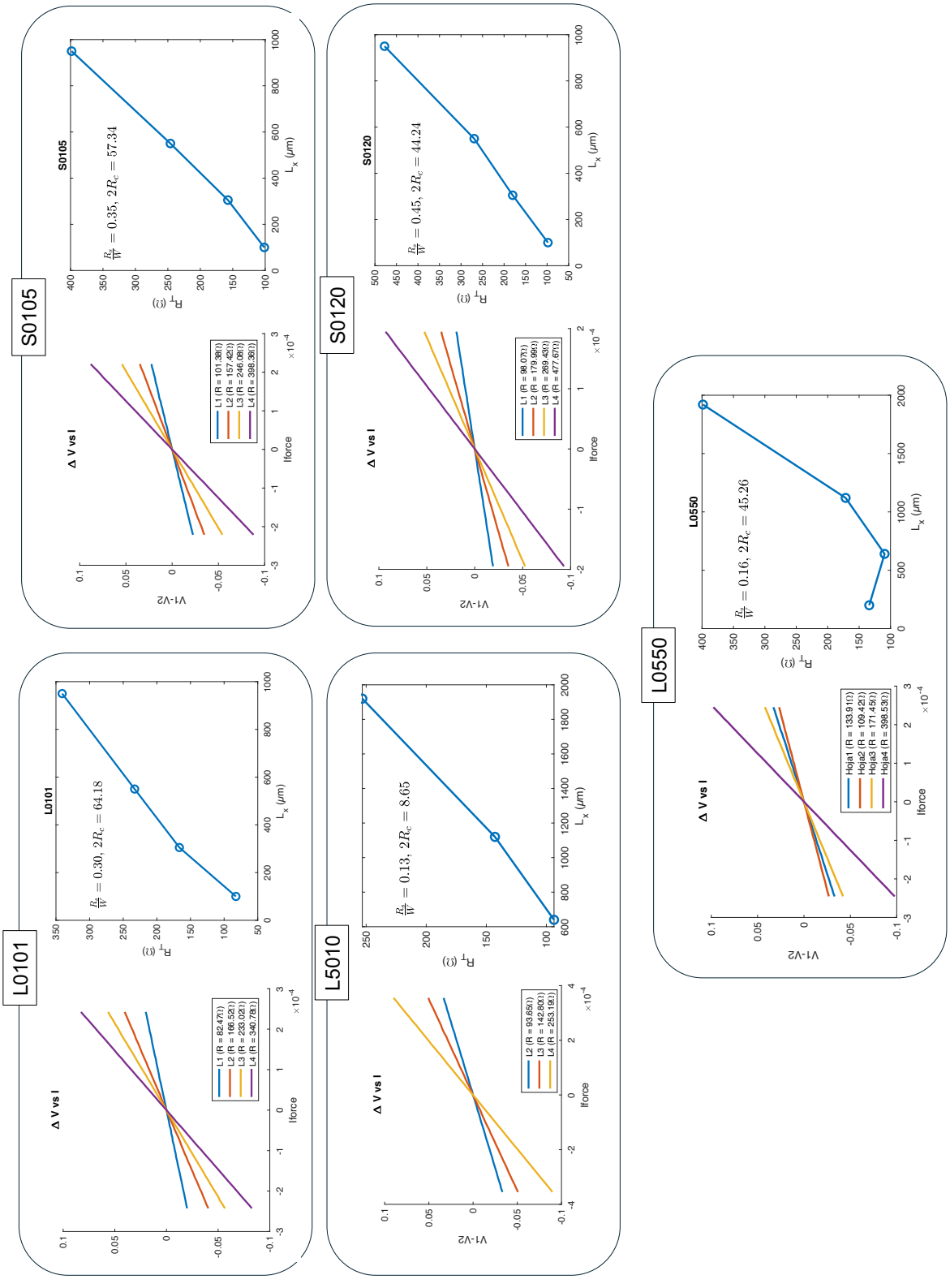


Figure A.8: Graphs obtained from the TLM measurements, used to calculate the sheet resistance values obtained for the structures that survived metallisation of wafer with corrugated patterns on SiO2 (W076).

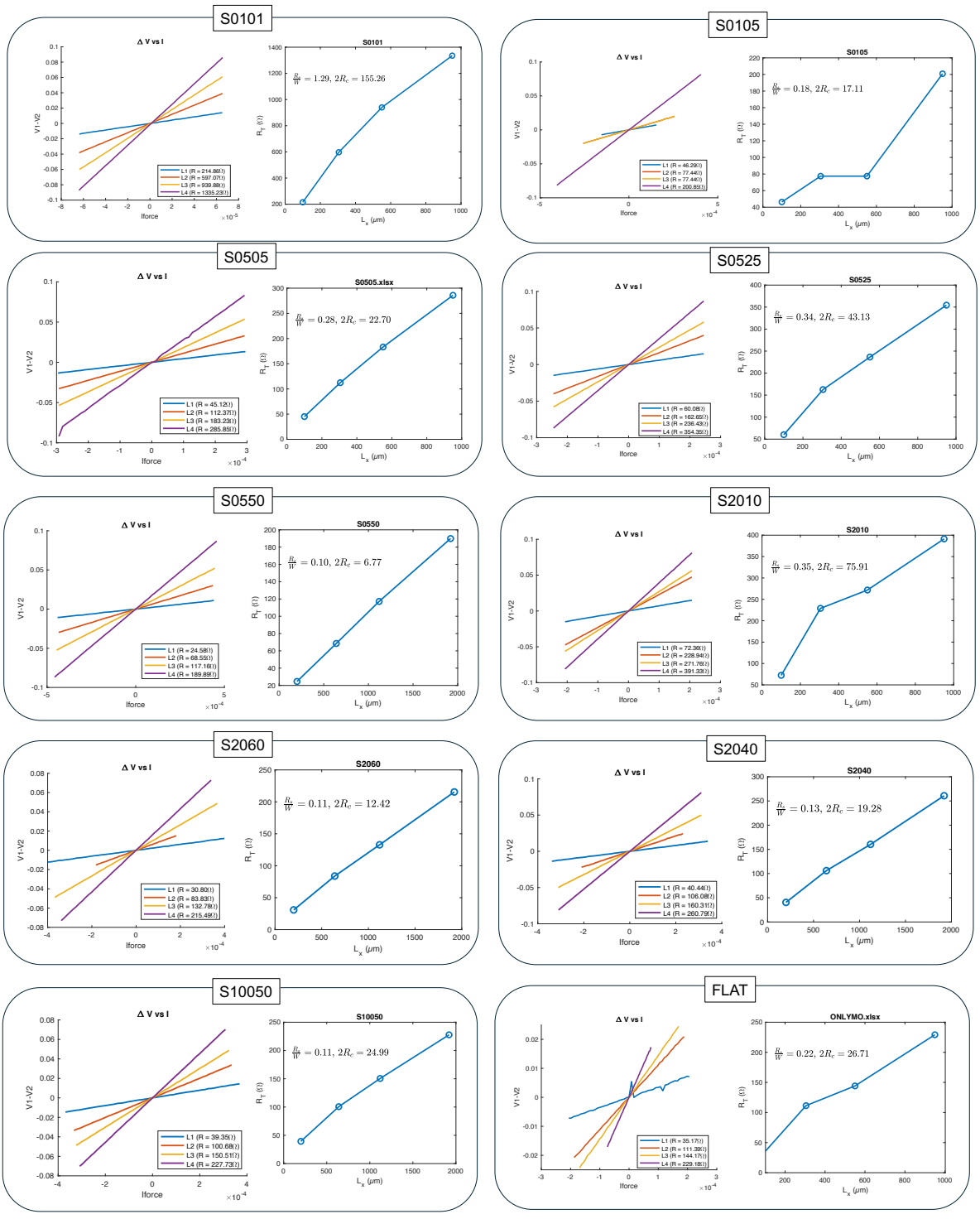

S0101
Δ V vs I
V1-V2
Iforce
L1 (R = 214.86Ω)
L2 (R = 597.07Ω)
L3 (R = 939.88Ω)
L4 (R = 1335.23Ω)
S0101
$\frac{R_c}{W} = 1.29,\ 2R_c = 155.26$
R_T (Ω)
L_x (μm)
S0105
Δ V vs I
L1 (R = 46.29Ω)
L2 (R = 77.44Ω)
L3 (R = 77.44Ω)
L4 (R = 200.85Ω)
S0105
$\frac{R_c}{W} = 0.18,\ 2R_c = 17.11$
S0505
Δ V vs I
L1 (R = 45.12Ω)
L2 (R = 112.37Ω)
L3 (R = 183.23Ω)
L4 (R = 285.85Ω)
S0505.xlsx
$\frac{R_c}{W} = 0.28,\ 2R_c = 22.70$
S0525
Δ V vs I
L1 (R = 60.08Ω)
L2 (R = 162.65Ω)
L3 (R = 236.43Ω)
L4 (R = 354.35Ω)
S0525
$\frac{R_c}{W} = 0.34,\ 2R_c = 43.13$
S0550
Δ V vs I
L1 (R = 24.58Ω)
L2 (R = 68.55Ω)
L3 (R = 117.16Ω)
L4 (R = 189.89Ω)
S0550
$\frac{R_c}{W} = 0.10,\ 2R_c = 6.77$
S2010
Δ V vs I
L1 (R = 72.36Ω)
L2 (R = 228.94Ω)
L3 (R = 271.78Ω)
L4 (R = 391.33Ω)
S2010
$\frac{R_c}{W} = 0.35,\ 2R_c = 75.91$
S2060
Δ V vs I
L1 (R = 30.80Ω)
L2 (R = 83.83Ω)
L3 (R = 132.78Ω)
L4 (R = 215.49Ω)
S2060
$\frac{R_c}{W} = 0.11,\ 2R_c = 12.42$
S2040
Δ V vs I
L1 (R = 40.44Ω)
L2 (R = 106.08Ω)
L3 (R = 160.31Ω)
L4 (R = 260.79Ω)
S2040
$\frac{R_c}{W} = 0.13,\ 2R_c = 19.28$
S10050
Δ V vs I
L1 (R = 39.35Ω)
L2 (R = 100.68Ω)
L3 (R = 150.51Ω)
L4 (R = 227.73Ω)
S10050
$\frac{R_c}{W} = 0.11,\ 2R_c = 24.99$
FLAT
Δ V vs I
L1 (R = 35.17Ω)
L2 (R = 111.39Ω)
L3 (R = 144.17Ω)
L4 (R = 229.18Ω)
ONLYMO.xlsx
$\frac{R_c}{W} = 0.22,\ 2R_c = 26.71$

Figure A.9

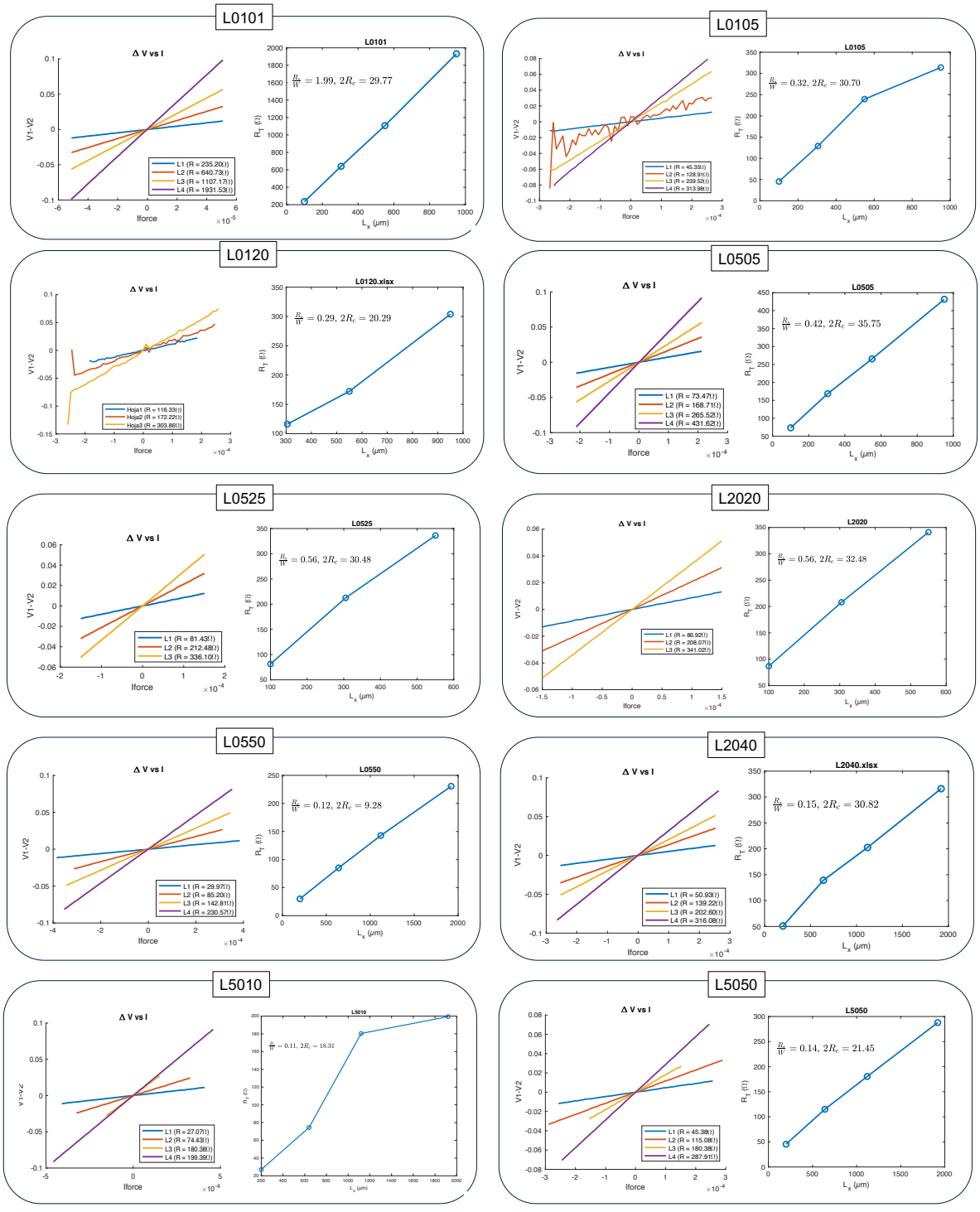

L0101
Δ V vs I
V1-V2
Iforce
L1 (R = 235.20Ω)
L2 (R = 640.73Ω)
L3 (R = 1107.17Ω)
L4 (R = 1931.53Ω)
L0101
$\frac{R_c}{W} = 1.99,\ 2R_c = 29.77$
R_T (Ω)
L_x (μm)
L0105
Δ V vs I
L1 (R = 45.39Ω)
L2 (R = 128.91Ω)
L3 (R = 239.52Ω)
L4 (R = 313.98Ω)
L0105
$\frac{R_c}{W} = 0.32,\ 2R_c = 30.70$
L0120
Δ V vs I
Hoja1 (R = 116.33Ω)
Hoja2 (R = 172.22Ω)
Hoja3 (R = 303.86Ω)
L0120.xlsx
$\frac{R_c}{W} = 0.29,\ 2R_c = 20.29$
L0505
Δ V vs I
L1 (R = 73.47Ω)
L2 (R = 168.71Ω)
L3 (R = 265.52Ω)
L4 (R = 431.62Ω)
L0505
$\frac{R_c}{W} = 0.42,\ 2R_c = 35.75$
L0525
Δ V vs I
L1 (R = 81.43Ω)
L2 (R = 212.48Ω)
L3 (R = 336.10Ω)
L0525
$\frac{R_c}{W} = 0.56,\ 2R_c = 30.48$
L2020
Δ V vs I
L1 (R = 86.92Ω)
L2 (R = 208.07Ω)
L3 (R = 341.02Ω)
L2020
$\frac{R_c}{W} = 0.56,\ 2R_c = 32.48$
L0550
Δ V vs I
L1 (R = 29.97Ω)
L2 (R = 85.20Ω)
L3 (R = 142.81Ω)
L4 (R = 230.57Ω)
L0550
$\frac{R_c}{W} = 0.12,\ 2R_c = 9.28$
L2040
Δ V vs I
L1 (R = 50.93Ω)
L2 (R = 139.22Ω)
L3 (R = 202.60Ω)
L4 (R = 316.08Ω)
L2040.xlsx
$\frac{R_c}{W} = 0.15,\ 2R_c = 30.82$
L5010
Δ V vs I
L1 (R = 27.07Ω)
L2 (R = 74.43Ω)
L3 (R = 180.38Ω)
L4 (R = 199.39Ω)
L5010
$\frac{R_c}{W} = 0.11,\ 2R_c = 18.31$
L5050
Δ V vs I
L1 (R = 45.38Ω)
L2 (R = 115.08Ω)
L3 (R = 180.38Ω)
L4 (R = 287.91Ω)
L5050
$\frac{R_c}{W} = 0.14,\ 2R_c = 21.45$

Figure A.10

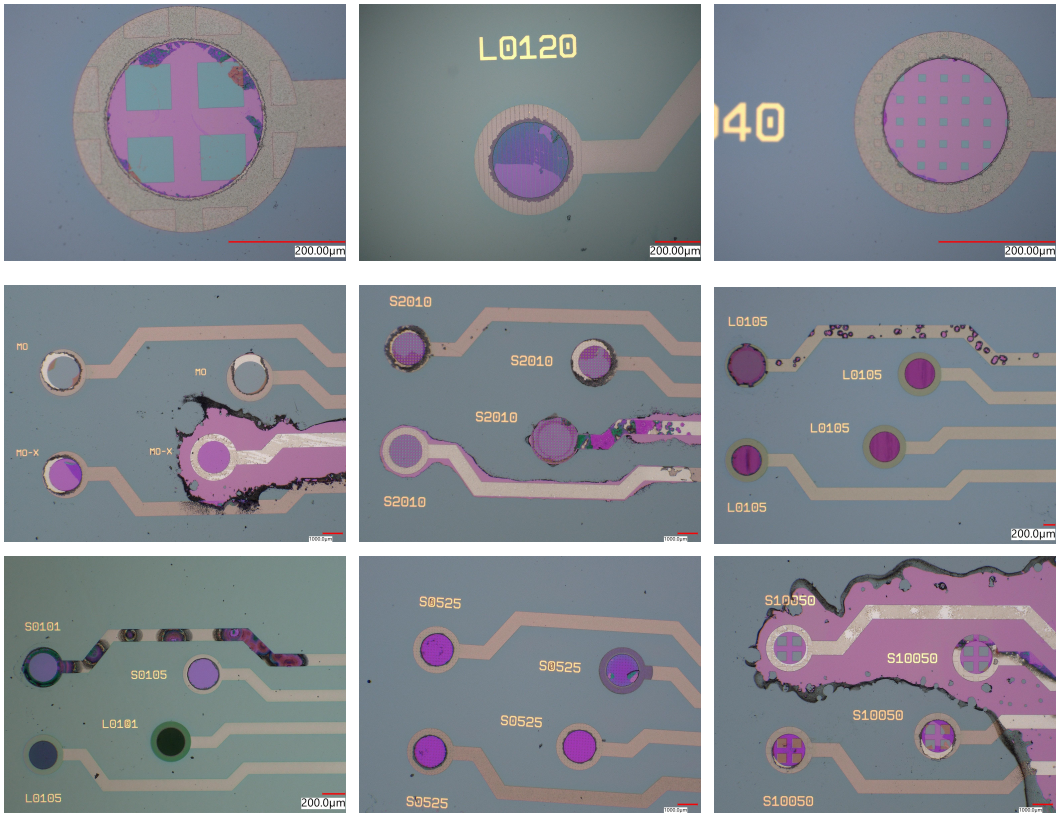


Figure A.11: Delaminated and damaged electrodes after electrochemical testing.

$$R_x = R_S \frac{L_x}{W} \quad \Rightarrow \quad R_S = R_x \frac{W}{L_x}$$

L0505 ≈ 126 Ω

$$R_{S1} = R_1 \frac{W}{L_1} = 73.47 \frac{300}{100} = 220.41$$

$$R_{S2} = R_2 \frac{W}{L_2} = 168.71 \frac{300}{305} = 165.94$$

$$R_{S3} = R_3 \frac{W}{L_3} = 265.52 \frac{300}{550} = 144.82$$

$$R_{S4} = R_4 \frac{W}{L_4} = 432.62 \frac{300}{950} = 136.61$$

L2040 ≈ 90 Ω

$$R_{S1} = R_1 \frac{W}{L_1} = 50.93 \frac{600}{200} = 152.79$$

$$R_{S2} = R_2 \frac{W}{L_2} = 139.22 \frac{600}{640} = 130.52$$

$$R_{S3} = R_3 \frac{W}{L_3} = 202.60 \frac{600}{1120} = 108.53$$

$$R_{S4} = R_4 \frac{W}{L_4} = 316.08 \frac{600}{1920} = 98.78$$

S0505 ≈ 84 Ω

$$R_{S1} = R_1 \frac{W}{L_1} = 45.12 \frac{300}{100} = 135.36$$

$$R_{S2} = R_2 \frac{W}{L_2} = 115.08 \frac{300}{305} = 113.19$$

$$R_{S3} = R_3 \frac{W}{L_3} = 180.38 \frac{300}{550} = 98.38$$

$$R_{S4} = R_4 \frac{W}{L_4} = 287.91 \frac{300}{950} = 90.63$$

S2040 ≈ 78 Ω

$$R_{S1} = R_1 \frac{W}{L_1} = 40.44 \frac{600}{200} = 121.32$$

$$R_{S2} = R_2 \frac{W}{L_2} = 106.08 \frac{600}{640} = 99.45$$

$$R_{S3} = R_3 \frac{W}{L_3} = 160.31 \frac{600}{1120} = 85.88$$

$$R_{S4} = R_4 \frac{W}{L_4} = 260.79 \frac{600}{1920} = 81.50$$

Figure A.12: Rough Rs calculation performed for some of the structures to validate the range of Rs obtained.

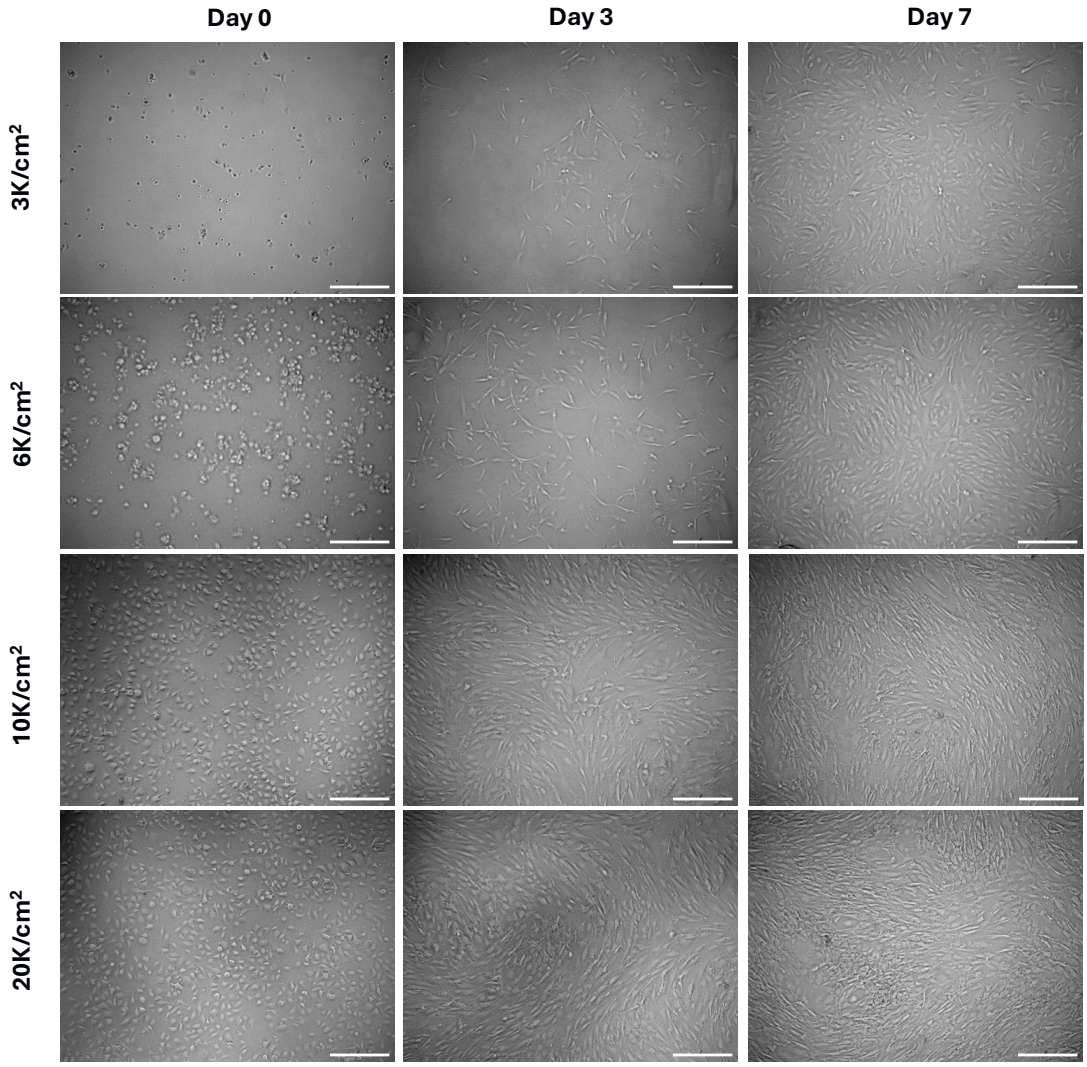


Figure A.13: Pilot experiment conducted on a well without samples for different seeding densities. Scale bar: 100 µm.

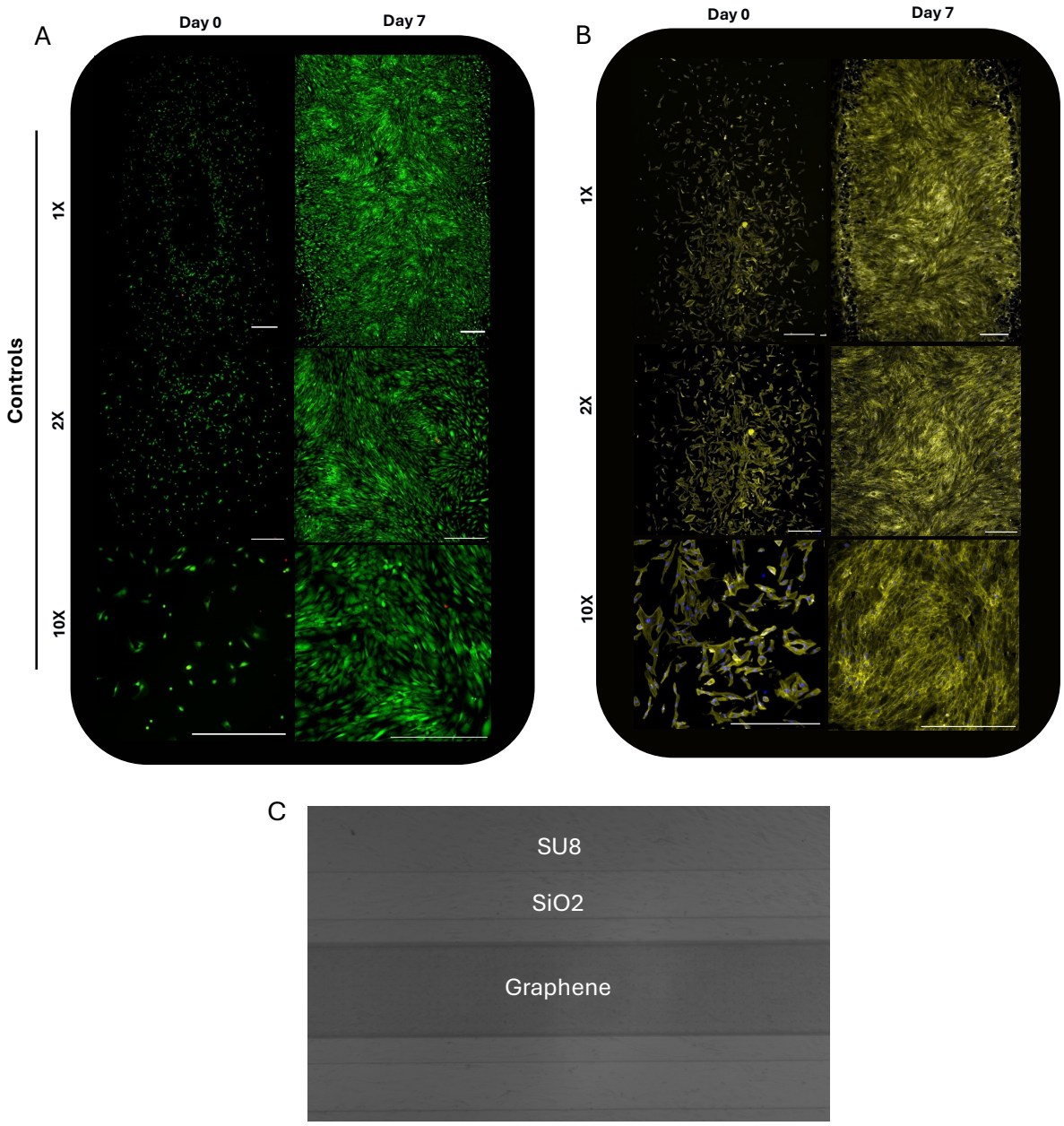


Figure A.14: A) Dapi/phaloidin assays performed for a well without samples. B) Brightfield image of a sample after 7 days of proliferation.

B

Final Flowchart

Corrugated graphene electrodes

FLOWCHART

Valid from x

BATCH INFORMATION			
NAME OF OWNER :	Maria Camarena	MASK SET :	GDS
NAME OF MENTOR :	Sten Vollebregt	MASK BOX :	505
RUN NUMBER :	2024-43	DIE SIZE :	10x10 mm
WAFER AMOUNT :	8	START DATE :	July 2024
SUBJECT TO PCC :	YES	PCC APPROVED :	

Contamination: Yes

Labs: CR100, CR10000

DELFT UNIVERSITY OF TECHNOLOGY
ELSE KOOI LABORATORY

Adress : Feldmannweg 17, 2628 CT Delft, The Netherlands
P.O. Box : 5053, 2600 GB Delft, The Netherlands
Phone : +31 - (0)152783868
Fax : +31 - (0)152622163
Website : www.tudelft.nl/ewi/onderzoek/faciliteiten/else-kooi-lab

Detailed information about possible contamination:

Place/Clean Rooms used in process:

- **Write the sequence of used labs from start to finish.**
- **Which (Non-standard) materials or process steps**
- **What kind of process or machine was used?**
- **The other materials that wafers contain that are also processed on this machine**

Lab/Clean room	**(Non-standard) material/ process steps**	Process/Machine	Other materials used in machine
CR100	Graphene	Sigma	

If other labs are used:
Write the steps number: Possible contamination issues/materials.

Step number	Material	Machine/Tool
22	Graphene	Blackmagic
23	Graphene	Sigma
27	Cr,Au	CHA
28,29	Graphene, Cr/Au	Wetbenches

If there are non-standard processing steps in a standard process: Write down the steps number, the material and machine that is used.
None

GENERAL RULES

CLEANROOM BEHAVIOUR

❶ Always follow the **"Security and Behavior"** rules when working in the EKL laboratories.

❷ Always handle wafers with care during processing. Use cleanroom gloves and work as clean as possible!

❸ Use cleanroom gloves when working with vacuum equipment. Do not touch the inside or carriers with bare hands.

❹ Always check equipment and process conditions before starting a process. Do **NOT** make unauthorized changes!

❺ Directly notify the responsible staff member(s) when there are problems with the equipment (like malfunction or contamination). Flip the status card on the machine over to **DOWN** to warn other users. Also change the status of the system to **DOWN** in the "Phoenix Living Database" system.

❻ **DO NOT TRY TO REPAIR OR CLEAN EQUIPMENT YOURSELF**, and **NEVER** try to refresh a contaminated etch or cleaning bath! Only authorized staff members are allowed to do this.

WORKING WITH NON-STANDARD MATERIALS

❶ All substrates, layers and chemicals which are not CMOS compatible are considered to be "**NON-STANDARD**" materials. These materials may cause contamination of bathes, equipment, wafer boxes, etc..

❷ The use of "non-standard" materials for processing in the class100 and SAL cleanroom must **ALWAYS BE EVALUATED** and **APPROVED** by your mentor and the EKL contamination officer. It is strictly forbidden to use these materials without permission.

❸ Wafers that are contaminated may **NEVER** be processed in any of the bathes or equipment without permission. Special precautions may be required, like the use of a separate container or special substrate holder or carrier.

❹ You must work according to the rules from the **Preventive Cross Contamination** (PCC) document, available on the "EKL Sharepoint webpage", and the **Materials** database from the "Phoenix Living Database" system.

CLASS 100 RULES

CLEANING OF WAFERS

After 4 hours of storage wafers must always be cleaned before performing a **COATING, FURNACE, EPITAXY** or **DEPOSITION** step.

Use the correct cleaning procedure:

- Tepla stripper ⇨ for removal of implanted or plasma etched photoresists.
  - Acetone ⇨ for removal of photoresist that is not implanted or plasma etched.
  - HNO_3 99% (Si) ⇨ for CMOS compatible wafers which do not need a HNO_3 69.5% step.
  - HNO_3 99% (Al) ⇨ for wafers which are or have been in contact with "green" metals (e.g.: Al, Al(1%Si), Ti, Zr, …).
- HNO_3 99% (Si) + HNO3 69.5% (Si) ⇨ for all other CMOS compatible wafers.

Note:
- The above described cleaning procedures are only valid for CMOS compatible wafers with CMOS compatible materials on them. **For all other wafers follow the PCC rules and check the Phoenix Materials database.**
- Wafers do **NOT** have to be cleaned **after** a furnace, epitaxy or deposition step if the next process step will be performed immediately, unless the wafers are covered with particles.

FURNACE RESTRICTIONS

Wafers that are covered with photoresist or a metal layer may **NEVER** be processed in any of the furnaces. This also applies for wafers from which a metal layer has been removed by etching. Only alloying in tube C4 is allowed for wafers with an aluminium layer.

MEASUREMENTS

Always perform all the measurement and inspection steps, and **write down the results in your journal and in the logbooks that can be found at some of the equipment**. The results are used to monitor the processes and/or equipment.

It is possible to measure directly on your (CMOS compatible) process wafers with the following Class 100 equipment:

- The Leitz MPV-SP, the WOOLLAM and the KEYENCE microscope. The first 2 systems are used for thickness measurements of transparent layers, and the third system is used for 3D surface metrology. The measurements are non-destructive and without contact to the wafer surface.
- The Dektak 8 surface profilometer. This system is used for step height measurements. In this case a needle will physically scan over the wafer surface, which can be destructive for structures. It is a contact measurement.
- The XL50 or Hitachi SEM. They can be used for inspection of your wafers and for width, depth or thickness measurements.

Note: ▪ After certain measurements **cleaning of your wafers** may be required for further processing.

▪ An extra wafer must be processed when other measurements are required (like sheet resistance and junction depth measurements). These wafers can not be used for further processing.

STARTING MATERIAL

Use 6 **single side polished process wafers**, with the following specifications:

Type:	P-type
Orientation:	100 deg off orientation
Resistivity:	2-5 Ωcm
Thickness:	525 ± 15 µm
Diameter:	100.0 ± 0.2 mm

Wafers taken out of an already opened box must be cleaned before processing, according to the standard procedure.
Wafers taken out of an unopened wafer box do not have to be cleaned before processing**.**

1. COATING AND BAKING

Use the EVG 120 wafer track to coat the wafers with resist and follow the instructions specified for this equipment.
The process consists of treatment with HMDS (hexa methyl disilazane) vapor with nitrogen as a carrier gas, spin coating with Shipley SPR3012 positive photoresist and a soft bake at 95°C for 90 seconds.
Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

Use coating "**Co – 3012 – 1.4um – no_EBR"** (resist thickness: 1.400 µm).

2. ALIGNMENT AND EXPOSURE

Processing will be performed on the ASM PAS 5500/80 automatic waferstepper.

Follow the operating instructions from the manual when using this machine.

Use **COMURK** mask and the correct litho job:
Job: litho/**ZEFWAM**
Layer ID: 1
Mask ID: COMURK
Exposure energy: **140** mJ/cm^2.

3. DEVELOPMENT

Use the EVG 120 wafer track to develop the wafers and follow the instructions specified for this equipment.

The process consists of a post-exposure bake at 115°C for 90 seconds, followed by a development step using Shipley MF322 developer (single puddle process) and a hard bake at 100°C for 90 seconds.
Always check the temperature of the hotplates first.

Use the development recipe **"Dev – SP".**

4. INSPECTION: LINEWIDTH

Visually inspect the wafers through a microscope, and check the linewidth. No resist residues are allowed.

5. WAFER NUMBERING

Use the glass pen in the lithography room to mark the wafers with the **BATCH** and **WAFER** number.
Write the numbers in the photoresist, just above the wafer flat. Always do this after exposure and development!
NOT allowed to use a metal pen or a scriber (pen with a diamond tip) for this purpose.

6. PLASMA ETCHING OF ALIGNMENT MARKS

Use the Trikon Ωmega 201 plasma etcher.
Follow the operating instructions from the manual when using this machine.
The process conditions of the etch program may not be changed!

Use sequence **URK_NPD** and set the plate temperature to **20 °C** to etch 1200 Å deep ASM URK's into the silicon.

7. CLEANING PROCEDURE: TEPLA + HNO_3 99% and 69.5% (NO METAL ZONE)

Plasma strip Use the Tepla plasma system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use program 1

Cleaning	10 minutes in fuming nitric acid (Merck: HNO_3 99% selectipur) at ambient temperature. Use wet bench "HNO_3 (99%)" and the carrier with the white dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Cleaning	10 minutes in concentrated nitric acid (Merck: HNO_3 69.5% selectipur) at 110 °C. Use wet bench "HNO_3 (69.5%)" and the carrier with the white dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a red dot.

9. OXIDATION

Use the Tempress furnaces. T2 should be used for this process.
Program name: EKL-WET1000 – **800 nm (calculate time and set in recipe).**

10. MEASUREMENT: OXIDE THICKNESS

Use the Woollam Ellipsometer.

Project: DIMES -> all -> general -> **search for the model suitable for the oxide thickness and growth** methodology used (SiO2 on Si 600 nm in this case). Re-analyze the data using different model if necessary.

CREATE CORRUGATION PATTERNS ON SIO2

11. COATING AND BAKING

Use the EVG120 system to coat the wafers with (1.4um) photoresist, and follow the instructions specified for this equipment. The process consists of treating HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with **SPR3012 positive** resist, and a soft bake at 95 °C for 90 seconds. The resist will be dispensed with a pump. Always check the room's relative humidity (48 ± 2 %) before coating.

Use coating "**Co – 3012 – 1.4um – no_EBR"** (resist thickness: 1.400 μm).

12. ALIGNMENT AND EXPOSURE

Processing will be performed on the MA8 contact aligner.
Follow the operating instructions from the manual when using this machine.

Expose mask: **MO CORR, Device G-Corr_MCP2024.**
Recipe: **FSA Soft contact.**
Exposure energy: **140 mJ/cm2**
For the MA8, determine the time of exposure, which is:
Exposure time = Exposure dose (mJ/cm2) / Lamp Power (mW/cm2).

Lamp power is time-dependent. Check it every time MA8 is going to be used.

13. DEVELOPMENT

Location: (Class 100 cleanroom).

Use the EVG120 system to develop the wafers, and follow the instructions specified for this equipment. The process consists of a post-exposure bake at 115 °C for 90 seconds, developing with Shipley MF322 with a single puddle process, and a hard bake at 100 °C for 90 seconds.

Use program " **Dev_SP "** on the developer station**.**

14. SIO2 WET ETCHING

Use the wet bench 2 – etching line.
Perform 30 s of Triton for BHF bath.
Immediately place the wafers in the BHF Si bath. The etching time depends on the step desired.
Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

15. PHOTORESIST REMOVAL WITH ACETONE

Remove the photoresist using Acetone 40ºC.

16. CLEANING PROCEDURE HNO_3 99% and 69.5% (NO METAL ZONE)

Cleaning	10 minutes in fuming nitric acid (Merck: HNO_3 99% selectipur) at ambient temperature. Use wet bench "HNO_3 (99%)" and the carrier with the white dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Cleaning	10 minutes in concentrated nitric acid (Merck: HNO_3 69.5% selectipur) at 110 °C. Use wet bench "HNO_3 (69.5%)" and the carrier with the white dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a red dot.

MO BULK STRUCTURE

17. CATALYST DEPOSITION @ CLASS 100

Catalyst deposition used for creating bulk Mo.

Use the TRIKON SIGMA sputter coater for the deposition of the catalyst metal Mo layer on the process wafers. Follow the operating instructions from the manual when using this machine. Perform a target clean if necessary.

Depending on the desired thickness, use the recipe:
Mo: xx nm, recipe **Mo_xxnm_50C**

Visual inspection: the metal layer must look shiny.

18. COATING AND BAKING

Use the EVG120 system to coat the wafers with (1.4um) photoresist, and follow the instructions specified for this equipment. The process consists of treating HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with **SPR3012 positive** resist, and a soft bake at 95 °C for 90 seconds. The resist will be dispensed with a pump. Always check the room's relative humidity (48 ± 2 %) before coating.

Use coating "**Co – 3012 – 1.4um – no_EBR"** (resist thickness: 1.400 µm).

19. ALIGNMENT AND EXPOSURE

Create the whole Mo bulk structure.
Processing will be performed on the SUSS MicroTec MA/BA8 mask aligner.
Expose mask: **MO BULK, Device G-Corr_MCP2024.**
Recipe: **FSA Soft contact.**
Exposure energy: **140 mJ/cm2**

For the MA8, determine the time of exposure, which is:
Exposure time = Exposure dose (mJ/cm2) / Lamp Power (mW/cm2).

Lamp power is time dependent. Check it every time MA8 is going to be used.

20. DEVELOPMENT

Location: (Class 100 clean room).

Use the EVG120 system to develop the wafers, and follow the instructions specified for this equipment. The process consists of a post-exposure bake at 115 °C for 90 seconds, developing with Shipley MF322 with a single puddle process, and a hard bake at 100 °C for 90 seconds.

Use program " **Dev_SP "** on the developer station**.**

21. PLASMA ETCHING OF MOLYBDENUM

Create whole bulk Mo structure.
Use the Trikon Ωmega 201 plasma etcher.
Follow the operating instructions from the manual when using this machine.
The process conditions of the etch program may not be changed!
MO_test8 (will not remove PR so we can use 1,4µm PR): 40 C, **time depends on Mo thickness.**

*Target time for **50 nm:** ~40 seconds for 50nm, for other thicknesses, this must be determined (do trials with different wafers).*
First, perform a test on one wafer and check for Mo etching residues and SiO_2 over-etch.

22. RESIST WET REMOVAL

Resist removal using NI555 (30 mins, sonicate at 80 kHz and 80 power). Use the wet chemical area at C10K.

23. GRAPHENE GROWTH @ CLASS 10000
Use the AIXTRON BlackMagic Pro to grow CNTs using LPCVD at 1000°C.
Use recipe: **Mo_NEW_935C_20min_20minpreanneal.**

Use graphene reactor interior (Cu contaminated)!

Check if graphene has successfully nucleated by inspecting the wafer in Raman.

USE WHITE BLISTER WITH Cu WRITTEN ON IT

GOLD METALLISATION

24. MANUAL COATING AND BAKING

Always use chuck for contaminated wafers.

1) HDMS treatment: treat for 10 mins in HDMS.
2) Photoresist coating: Use PR **NEGATIVE NLOF-202** (**3,5 µm**). Use coating **'AZ_Nlof-3500nm'**.
3) Soft bake: soft bake on a hot plate for contaminated wafers at **95 C for 3 min**.

25. ALIGNMENT AND EXPOSURE

Follow the operating instructions from the manual when using this machine. Use contaminated chuck in this step.
Expose mask: **METAL, Device G-Corr_MCP2024.**
Recipe: **FSA Soft contact.**
Exposure energy: **calculate it by consulting contact aligner exposure energy data log.**
For the MA8, determine the time of exposure, which is:
Exposure time = Exposure dose (mJ/cm2) / Lamp Power (mW/cm2), 80mJ/cm2.

Lamp power is time-dependent. Check it every time MA8 is going to be used.

26. MANUAL DEVELOPMENT

1) Post-exposure baking: bake at 115 C for 3 min.
2) Photoresist development: use Shipley MF322 developer 1 min. **NO OVERDEVELOP**.
3) Dry: spin dry the wafer, use contaminated chuck.
4) Inspection: use optical microscope to check openings.
5) Hard baking: bake 100 C for 4 min. Use hot plate for contaminated wafers.
6) Inspection: use OM.

27. METAL DEPOSITION

Use the CHA Solution Std. for Ti/Au evaporator to deposit 10 nm of Ti and 200 nm of Au. Make sure the Au dome and shutters have been installed, if not ask a trained senior user to do change them.
Ensure the vacuum is not lost between layer depositions.
Allow the machine to reach vacuum overnight to ensure a better-quality metal layer.

Due to the thickness of the gold layer, in order to avoid overbaking the photoresist, if the temperature gets to 75ºC, stop the recipe, wait 20 mins and resume it.

28. LIFT-OFF WETBENCH

Fill a beaker with NI555.
Use a metallic scriber to scratch the gold on areas where there are no structures. This will increase the surface of the exposed photoresist to the NI555 accelerating the process.
Place the wafers in a holder and submerge it in the beaker with NI555.
Leave the wafers in NI555 overnight. Rinse in DI water and allow to air dry.

ENCAPSULATION

29. MANUAL COATING AND DEVELOPMENT

Always use chuck for contaminated wafers.

1) HDMS treatment: treat for 10 mins in HDMS.
2) Photoresist coating: Use PR **AZ3027 (3,1 µm)**. Use coating **'AZ_AZ3027-3100nm'**.
3) Soft bake: soft bake on a hot plate for contaminated wafers at **95 C for 1 min**.

30. ALIGNMENT AND EXPOSURE

Follow the operating instructions from the manual when using this machine. Use contaminated chuck in this step.

Expose mask: **OPENINGS, Device G-Corr_MCP2024.**
Recipe: **FSA Soft contact.**
Exposure energy: **calculate it by consulting contact aligner exposure energy data log.**

For the MA8, determine the time of exposure, which is:
Exposure time = Exposure dose (mJ/cm2) / Lamp Power (mW/cm2).

31. MANUAL DEVELOPMENT

1) Post Exposure Baking: Bake at **115 deg. For 1 min.**
2) Photoresist Development: Use Shipley **MF322 developer for 1 min**. Make sure not to overdevelop. Rinse gently since graphene can be fragile and then spin dry. Use the contaminated chuck for the spin dryer.
3) Hard baking: bake **100 deg for 1 min.** Use hot plate for contaminated wafers.
4) Inspection: visually inspect the wafers through a microscope and check openings.

DICING

32. WAFER DICING IN BIOSONIC LAB

Wafers should be diced using the **Disco Dicer (DAD3240).**

33. MO ETCHING @ CR10000

Etch the Mo layer away underneath the graphene to form graphene resistors without transfer using H_2O_2 (31%). Etching time depends on Mo thickness used. Inspect visually during the process. Dry using N gas.

PCB MOUNTING

34. DIE ATTACHMENT

Use Superglue to glue the devices to the PCB. Let them dry 24/48h at room temperature (PR encapsulation might be sensitive to temperature changes!!).

35. WIRE BONDING: @EWI building (HB14.320)

Ball wirebond Au wires between the die contact pads and the PCB contact pads using the TPT HB05 Au bonder.

36. PADS AND WIRE BONDING INSULATION

Add a drop of PDMS or epoxy on the bond pad to make it mechanically stable and leave it for several hours to dry.

PDMS recipe:
Use SYLGARD 184 Silicone Elastomer
The base (part A) and curing agent (part B) are mixed in 10:1 mass ratio, respectively.
Use the automatic spinner for mixing. Be sure that the container is securely closed and snug inside the automatic spinner's holder before starting the spin. Clean the work area with acetone afterward. Do not use it immediately on the wire because it is too thin. Wait one hour, so the PDMS is more viscous before applying.

C

Codes

Calculate Sheet Resistance with TLMs (MatLab)

```
% Filename of the Excel file
filename = 'ONLYMO.xlsx'; % Excel file with 4 sheets (one sheet per
length Lx)

% Get the names of the sheets in the Excel file
[~, sheets] = xlsfinfo(filename);

% Check if the file has at least 4 sheets
if length(sheets) < 4
    error('The Excel file must contain at least 4 sheets.');
end

% Distances corresponding to each sheet (in microns)
L = [100, 305, 550, 950];  % L1, L2, L3, L4, this values are for the
small TLM structures. Values for big ones are L1 = 200, L2 = 640, L3 =
1120, L4 = 1920

% Create a figure for the plot of Iforce vs V1-V2
figure;
hold on; % Keep the plot open to add multiple curves

% Colors for each sheet
colors = lines(4);

% Initialize legend text and slopes vector
legendText = {};
slopes = zeros(1, 4);  % Store the slopes for each sheet

% Loop through the first 4 sheets in the Excel file
for i = 1:4
    % Read data from the sheet
    data = readtable(filename, 'Sheet', sheets{i});

    % Check if the columns "Iforce" and "V1_V2" exist
    if    any(strcmp(data.Properties.VariableNames,    'Iforce'))    &&
any(strcmp(data.Properties.VariableNames, 'V1_V2'))
        % Extract the "Iforce" and "V1_V2" columns
        Iforce = data.Iforce;
        V_diff = data.V1_V2;
```

```
        % Plot the data for the current sheet
        plot(Iforce, V_diff, 'DisplayName', sheets{i}, 'LineWidth', 2,
'Color', colors(i, :));

        % Fit a straight line (1st-degree polynomial) to the data
        coeffs = polyfit(Iforce, V_diff, 1); % Linear fit

        % Extract the slope of the line (first coefficient)
        slope = coeffs(1);
        slopes(i) = slope;  % Store the slope. The slope is R = V/I for
each length Lx

        % Display the slope in the console
        disp(['Slope of sheet ' sheets{i} ': ' num2str(slope)]);

        % Add the slope to the legend text for the current sheet
        legendText{i} = [sheets{i}, ' (R = ', num2str(slope, '%.2f'),
'\Omega' ')'];
    else
        disp(['Sheet ' sheets{i} ' does not contain the required columns
(Iforce and V1_V2).']);
    end
end

% Add labels to the axes for Iforce vs V1-V2 plot
xlabel('Iforce');
ylabel('V1-V2');

% Add title and custom legend for the Iforce vs V1-V2 plot
title('\Delta V vs I');
legend(legendText, 'Location', 'best');

% Close the hold for the first plot
hold off;


% --- Plot the resistance values  of each Lx vs the length value (µm) -
-
figure; % Create a new figure for the slopes plot

% Define x-axis values using the actual distances L1, L2, L3, L4
L_values = L;  % Use the defined distances directly

% Plot the slopes as a line
plot(L_values, slopes, '-o', 'LineWidth', 2, 'MarkerSize', 8);

% Add labels to the axes
xlabel('L_x (µm)');  % X-axis label now reflects distance
ylabel('R_T (\Omega)');

% Fit a line to the slopes to calculate the slope of this plot and y-
intercept
coeffs_slopes = polyfit(L_values, slopes, 1);  % Linear fit for slopes
using actual lengths
overall_slope = coeffs_slopes(1);  % This is the slope of the line
y_intercept = coeffs_slopes(2);    % This is the y-intercept

% Create a string for the slope and intercept
legendText = ['$\frac{R_s}{W} = ', num2str(overall_slope, '%.2f'), ...
              '$, $2R_c = ', num2str(y_intercept, '%.2f'), '$'];
```

```
% Create a custom legend with just the text, no graphical elements
lgd = legend('hide');

% Use the annotation instead of the legend to put the custom text
annotation('textbox', [0.15 0.7 0.2 0.1], 'String', legendText, ...
    'Interpreter', 'latex', 'FontSize', 14, 'BackgroundColor', 'white',
...
    'EdgeColor', 'none', 'FitBoxToText', 'on');

% Add title to the plot
title([filename]);

% Hold off after the plot
hold off;
```

Calculate CSC (Python)

```
import pandas as pd
import numpy as np
import matplotlib.pyplot as plt
from scipy.integrate import trapz
from tkinter import filedialog
from tkinter import Tk

# Electrode area in µm²
electrode_area_um2 = 90792  # square micrometers
electrode_area_cm2 = electrode_area_um2 * 1e-8  # Convert to cm² (1 cm² = 1e8
µm²)

# Function to select multiple Excel files
def select_files():
    root = Tk()
    root.withdraw()  # Hide the main Tkinter window
    files = filedialog.askopenfilenames(title="Select Excel files",
filetypes=[("Excel files", "*.xlsx")])
    return list(files)

# Function to calculate CSC and average Scan 3 data
def calculate_csc_and_average(files):
    all_potentials = []
    all_currents = []

    # Iterate over each file
    for file in files:
        # Load the Excel file
        data = pd.read_excel(file)

        # Check column names
        print("Columns in the file:", data.columns)

        # Ensure the columns are correct
        scans = data['Scan']
        potential = data['WE(1).Potential (V)']
        current = data['WE(1).Current (A)']

        # Filter data for Scan 3
        scan_3_data = data[scans == 3]
        potential_3 = scan_3_data['WE(1).Potential (V)']
        current_3 = scan_3_data['WE(1).Current (A)']
```

```
            # Store scan 3 data
            all_potentials.append(potential_3.values)
            all_currents.append(current_3.values)

        # Average Scan 3 data from all files
        avg_potential = np.mean(all_potentials, axis=0)
        avg_current = np.mean(all_currents, axis=0)

        # Numerical integration to calculate CSC using the trapezoidal rule
        csc = trapz(avg_current, avg_potential)  # Total area under the curve

        # Convert CSC to µC/cm²
        csc_per_area = (csc * 1e6) / electrode_area_cm2  # Convert to µC and
divide by the area in cm²
        return avg_potential, avg_current, csc_per_area

# Function to plot the average curve and shade the total area
def plot_average_data(potential, current):
    # Create the current vs. potential plot
    plt.figure(figsize=(8, 6))
    plt.plot(potential, current, label='Average Scan 3', color='b')

    # Labels and title
    plt.xlabel('Potential (V)')
    plt.ylabel('Current (A)')
    plt.grid(True)
    plt.legend()
    plt.show()

# Select multiple files
files = select_files()

# Calculate averaged data and CSC
avg_potential, avg_current, mean_csc = calculate_csc_and_average(files)

# Display the mean CSC value
print(f'The mean CSC value is: {mean_csc:.4f} µC/cm²')

# Plot the averaged current vs. potential curve
plot_average_data(avg_potential, avg_current)
```