**MSc thesis in Electrical Engineering**

# A VCO-based ADC for MEMS microphones

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October 2023

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Submitted to the Office of Graduate Studies of the Delft University of Technology

In partial fulfilment of the requirements for the degree of

MASTER OF SCIENCE

in

Faculty of Electrical Engineering, Mathematics and Computer Science

(Department of Microelectronics)

The work in this thesis was carried out in the:


Electronic Instrumentation

Delft University of Technology


Silicon Integrated B.V.

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# ABSTRACT

MEMS microphones offer a significant scope to improve miniaturization, integration and cost of acoustic systems, poised to be the preferred microphone option for consumer electronics and medical advancements. A MEMS microphone needs a readout interface to convert the microphone's output to a digital code for further processing, while its poor driving ability poses a challenge on the design of readout ADCs.

In this thesis, the theory and implementation of a high input impedance continuous-time sigma-delta modulator (SDM) for a MEMS microphone readout is presented. A pseudo-virtual ground feedforward structure is used to eliminate the internal feedback DAC and contribute to enhanced linearization. To meet the requirement of high input impedance, a Gm-C first integrator is employed, featuring a resistive source degeneration structure and a local Gm-boosting loop to enhance the linearity of the first stage. For the second stage, a VCO-based integrator and quantizer are employed, offering advantages including inherent multilevel quantization and intrinsic clock-level averaging (CLA). The second order SDM consumes an estimated power of 57$\mu$W, achieving an 83dB SNR and a 79dB SNDR in simulation, reflecting its efficiency in audio applications.

# ACKNOWLEDGEMENTS

It is a hard but special journey for me.

I would like to thank Dr. Michiel Pertijs for his help and guidance throughout this thesis project. In moments of difficulty or when I found myself in a bad state, he always understood my situation and provided care and assistance. When I encountered issues in circuit design, he had a remarkable ability to swiftly identify problems and provide insightful suggestions. He also put a lot of effort into my thesis writing and provided almost all the suggestions and guidance on thesis revision.

I would also like to thank Dr. Hui Jiang and Ao Ba for their instructions and discussions with me. I could always ask them questions when I confront problems and they will guide me come up with solutions. When I had almost no knowledge of circuit design, it was their patient guidance that helped me make progress bit by bit.

I would like to express my sincere gratitude to Dr. Dante Muratore for serving on my thesis defence committee.

I would like to thank my fellow students and also my friends in Delft and Eindhoven. Shenyang Li, Ruoyu Huang, Junyu Yang, Zitao Zhu, Jie Dai, Yutong Du and so many so many people. It's you guys who discuss problems with me and bring me joy every day.

I am also very grateful to my girlfriend Song Yuxuan for her care and companionship towards me. I hope we can continue to encourage each other, supervise each other, progress and grow together.

Finally, I would like to express gratitude to my parents. Thank you for your selfless dedication!

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# 1

# INTRODUCTION

This chapter introduces the background information about the micro-electro-mechanical-system (MEMS) microphones and analyzes the requirements of a readout interface. After a brief discussion about the prior work and its limitations, the motivation and targets of our work are given, followed by a section presenting the organization of the thesis.

## 1.1. BACKGROUND

Microphone sensors find application across diverse sectors, spanning from consumer and industrial domains to areas like automotive and military technology. Since their inception in 1876, microphone sensors have evolved through numerous developmental phases, playing a pivotal role in consumer electronics, telecommunications, radio broadcast, medicine, and industry [1].

A microphone is essentially a transducer that converts atmospheric pressure fluctuations into a corresponding electrical signal [2]. Within a microphone, variations in pressure cause a mechanical mass to vibrate, ultimately resulting in the generation of an electrical signal, often in the form of capacitance variations .

### 1.1.1. MEMS MICROPHONE

Notably, the current trajectory highlights the rapid adoption of MEMS capacitive microphones, representing the next wave of acoustic sensor technology and poised to be the preferred microphone option for consumer electronics and medical advancements. By leveraging MEMS technology, MEMS microphone offers a significant scope to improve miniaturization, integration and cost of the acoustic systems [1]. fig. 1.1 simply shows the main structure of a MEMS capacitive microphone. A MEMS microphone consists of two conductive plates at a distance. To convert the capacitance variation associated with sound into an electric signal, the MEMS capacitor is initially charged to a constant voltage. If the capacitor is well-insulated, the stored charge on it remains constant. When the sound comes, the bottom plate is fixed and cannot move, while the top plate is able to vibrate with

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sound pressure, producing a variation of distance proportional to the instantaneous pressure level. With the change of distance, the voltage signal generated by the two plates will also change proportionally to the instantaneous pressure variation.

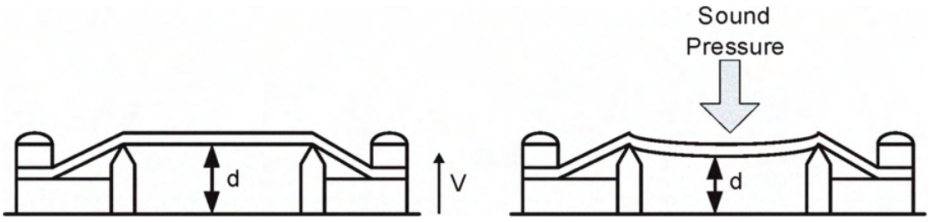


Figure 1.1: MEMS condenser microphone working principle[2]

### 1.1.2. MICROPHONE READOUT INTERFACE

Compared to digital signals, which have high noise margins, analog signals are more sensitive to noise and interference. The weak output analog signal from a MEMS microphone can easily be corrupted by noise and interference in a digital-intensive environment. Therefore, integrating analog-to-digital conversion into the analog microphone to generate a digital signal is beneficial for resisting noise in the environment and maintaining signal purity and robustness.

An analog microphone needs a readout interface to convert the microphone's output to a digital code for further processing. the low bandwidth of the audible sound (20-kHz) promotes the use of oversampled converters, such as sigma-delta modulators (SDM) [3]. There are two common ways to implement such a readout interface, one is using a front-end preamplifier followed by a discrete-time (DT) sigma-delta modulator, the other is using a continuous-time (CT) SDM that directly senses the microphone's output. Compared with the discrete-time SDM, continuous-time SDM is usually more power-efficient and has inherent anti-aliasing filtering, which makes it a more common choice for audio applications [3].

To directly interface with the MEMS microphone and sense its output, the readout circuit must offer a high input impedance. This is essential because the MEMS condenser microphone possesses limited driving capacity. A large resistor is needed to provide the CT SDM with a bias voltage, which can be implemented as a pair of anti-parrallel diode [1].

A condenser microphone can be simply modeled as a voltage source $V_m$ in series with a capacitor $C_m$, typically having a capacitance in the range of several pF [3]. fig. 1.2 shows the condition when the readout SDM is directly connected to the MEMS microphone, from which we can see that the input resistance $R_{in}$ of the readout interface will form a RC high pass filter with the microphone capacitor

$C_m$. To make the high pass filter corner due to $R_{in}$ and $C_m$ low enough to avoid attenuation of in-band audio signals, the value of the input resistance $R_{in}$ needs to be in the order of hundreds of MΩ .

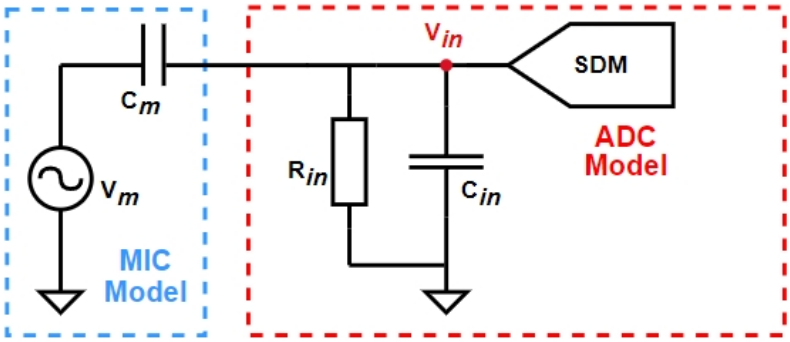


Figure 1.2: Requirement of input impedance

Furthermore, input capacitance Cin of the readout interface should also be small enough in order not to attenuate the signal very much by the capacitive voltage divider, which is also shown in fig. 1.2. In general, the requirement of high input impedance of the readout interface is not only applied to DC but also AC impedance.

## 1.2. MOTIVATION

For the CT SDM used for MEMS microphones, it must present a high input impedance in order to be driven directly by the microphone. While many of today's standard CT SDMs have good performance in linearity and are being used widely in part of the audio applications [4], [5], their low input impedance makes them unsuitable for microphone readout applications.

One viable solution to address this challenge is to use a voltage buffer between the microphone and the CT SDM, which is shown in Fig. 1.4. By this strategy the driving capability of microphone will be enhanced and the linearity of the SDM could be maintained. However, given the oversampled nature of the SDM and the low signal level at the MEMS microphone, this voltage buffer is a critical block requiring a high slew rate and low noise, which results in significant power consumption [6].

Another common solution is to use the Gm-C-based CT SDM and directly connect the MEMS microphone to the gate of the input Gm-cell, which maintains a high input impedance of the CT SDM and is shown in fig. 1.4. However, for this approach, the summing node of the input and feedback DAC are typically implemented at the output of the integrator, which means that the Gm-cell will operate in the open-loop

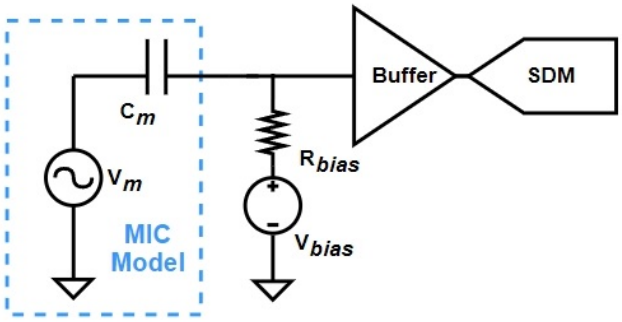


Figure 1.3: SDM with buffer

manner and lead to a degraded linearity performance [7]. Therefore, achieving good linearity while maintaining high input impedance at the same time is a challenge for the microphone readout interface design.

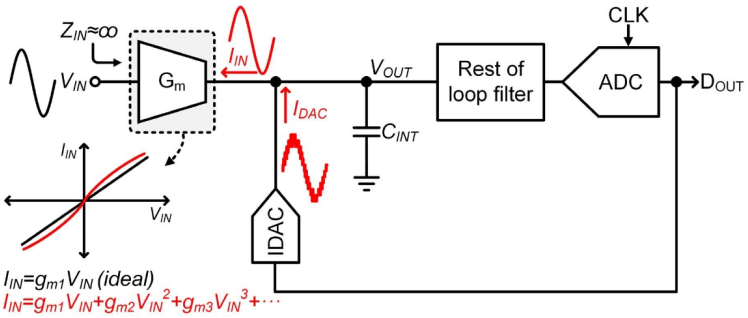


Figure 1.4: Open loop Gm-C-based CT SDM [7]

### 1.2.1. PRIOR WORK

Many attempts have been made to design a suitable readout interface for the MEMs microphone. In [3], A current-sensing boosted (CSB) OTA-C integrator with capacitive feedforward compensation is employed in the CT SDM to achieve high input impedance and high linearity, which is shown in fig. 1.5. The current-to-voltage converter ("$R_A$") minimizes $i_+$ - $i_+$ directly by the negative feedback to achieve high linearity. With a third order topology and a 1-bit quantizer, the CT SDM achieves a peak signal-to-noise-and-distortion (SNDR) ratio of 74.2 dB, with 10-kHz bandwidth and 801-$\mu$W power consumption. [8] presents a highly digital SDM for MEMS microphones. The proposed converter is implemented using only voltage-controlled

oscillators (VCO) and digital circuitry, without operational amplifiers. However, a voltage buffer is needed for this kind of strategy. With a second order topology, it can reach a peak SNDR of 76.6 dB with 20-kHz bandwidth and 560-$\mu$W power consumption.

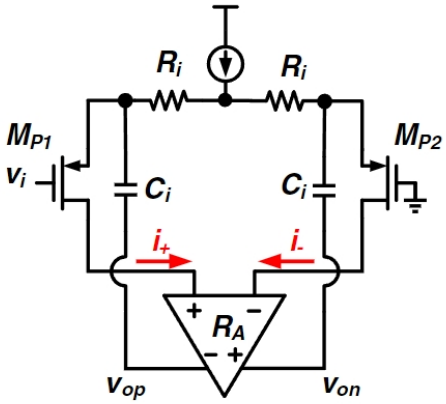


Figure 1.5: The CSB OTA-C integrator [3]

However, for current-sensing boosted OTA-C integrator, the input stage is very power-consuming to meet the requirement of linearity, while for the oscillator-based SDM, the input buffer also results in significant power consumption.

In the latest research progress, excellent readout circuit designs for MEMS microphones have also emerged, like what is shown in [9], a voltage-controlled oscillator based SDM using differential pulse code modulation to mitigate VCO voltage-to-frequency non-linearity is presented, by leveraging a quasideterministic background gain calibration and dynamic element matching (DEM), a peak SNDR of 94.2 dB is achieved in 20-kHz bandwidth with only 142.6-$\mu$W power.

However, the cost of achieving this excellent performance is the complicated digital calibration circuit, which will significantly increase the complexity and cost of large-scale circuit production and makes this approach not widely applicable and not suitable for industrial and commercial applications.

### 1.2.2. PROJECT TARGETS

The main purpose of this project is to design a readout SDM for the MEMs microphone within reasonable power consumption and area, without the need for complicated calibration circuits, in order to be applied in industrial and commercial fields in the future.

Audio applications could allow higher distortion compared to more strict requirement on low noise, normally an over 12-bit linearity is enough, which can be transformed into a peak SNDR of over 74 dB [3]. So in this project, we do not need to consume additional power or increase circuit complexity to achieve a particularly high SNDR performance, which is not necessary for audio application.

Based on these requirements, the targets of this project are listed in table 1.1 along with the comparison with the prior art of the microphone readout SDM. The core part of the project is to meet the SNR and SNDR target with lowest power consumption and reasonable area while no calibration circuit is needed.

Table 1.1: Targets of project and comparison with the prior art

| | This work | [3] | [8] | [9] |
|---|---|---|---|---|
| Architecture | CTSDM | CTSDM | CTSDM | CTSDM |
| Year | 2023 | 2014 | 2018 | 2021 |
| SDM order | 2 | 3 | 2 | 2 |
| Bandwidth (kHz) | 20 | 10 | 20 | 20 |
| Technology (nm) | 180 | 350 | 130 | 65 |
| Supply (V) | 1.5 | 3 | 1.8 | 1 |
| Power ($\mu$W) | 200 | 630 | 560 | 142.6 |
| Area (mm2) | 0.4 | - | 0.04 | 0.11 |
| Peak SNDR (dB) | 74 | 74.2 | 76.6 | 94.2 |
| Peak SNR (dB) | 80 | 75.8 | - | 97.3 |
| Calibration | Not needed | Not needed | Not needed | Needed |

## 1.3. ORGANIZATION OF THE THESIS

The work carried out in this thesis describes the method and implementation of a Gm- C based continuous-time SDM with a VCO-based integrator and quantizer used for MEMS microphone readout applications.

This chapter describes the background information and motivation for the work, then further system level designs are illustrated in Chapter 2. Choices of the modulator topology and circuit architecture are explored and explained. System-level techniques are proposed based on high input impedance and aimed at the required linearity.

Chapter 3 on circuit implementation presents the transistor level implementation of various circuit blocks in the modulator. The design requirements for different blocks are analyzed and simulation results are provided.

Chapter 4 discusses the top-level integration and top-level simulation results in which the functionality of the whole system is shown.

Finally, conclusions are drawn in Chapter 5 and suggestions for future work are given.

# 2

# System-Level Design

This chapter initiates a discussion on the system-level design considerations for the second-order SDM. It begins with a comparative analysis of the system's topology structure, followed by an exploration of the design aspects for each individual building block. Furthermore, it presents the simulation results for the ideal system and validates the impact of some non-ideal characteristics on system performance.

## 2.1. Topology of SDM

A sigma-delta modulator is a type of analog-to-digital converter commonly used for high-resolution and high-precision applications, such as audio and sensor signal processing. The sigma-delta modulator works by oversampling the input signal at a much higher rate than the Nyquist rate. The topology of a sigma-delta modulator is a critical aspect of its design and defines how the modulator operates. In this section, key aspects of the topology of a sigma-delta modulator is described for our design.

### 2.1.1. DT and CT SDM

CT sigma-delta modulators and DT sigma-delta modulators are two different implementations of sigma-delta modulators, each with its own set of advantages and disadvantages.

Where the signal is sampled determines how the discrete-time and continuous-time SDM differ from one another. In a DT SDM, the initial step involves sampling the input signal before it is introduced into the first integrator, as illustrated in fig. 2.1. It is important to note that any errors originating from the sampling process cannot be eliminated through the application of a loop filter. Consequently, the inclusion of a pre-anti-aliasing filter becomes imperative to circumvent aliasing issues.

Conversely, in a CT SDM, the sampling of the signal takes place before the quantization process, as depicted in fig. 2.2. The significance of this arrangement lies in the fact that errors arising from the sampling process will be naturally attenuated

by the modulator itself. Thus, the CT-SDM inherently provides anti-aliasing capabilities, eliminating the need for additional filtering.



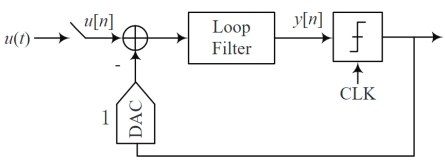


Figure 2.1: Simplified DT SDM [10]

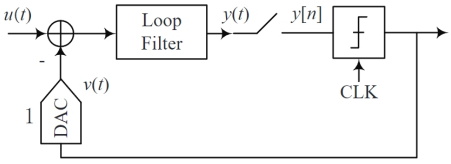


Figure 2.2: Simplified CT SDM [10]

In the context of circuit implementation for these two types of modulators, discrete-time sigma-delta modulators commonly employ switched-capacitor integrators [10]. The coefficients in these modulators are determined by the values of the capacitors, which exhibit robust performance characteristics over time and across varying temperatures. This structural approach is also known for its reduced sensitivity to parasitic capacitance.

However, the switch implementation in DT SDMs can pose challenges, especially in scenarios where the supply voltage drops to the threshold voltage of the transistors [11]. This situation necessitates the inclusion of additional circuitry to ensure the reliable operation of the switches, thereby introducing complexities in the overall circuit design. Furthermore, the settling time of the operational amplifier (opamp) places limitations on the achievable sampling frequency of DT SDMs.

For CT SDMs, circuits can be implemented using either an active-RC or Gm-C technique [10]. However, it's worth noting that the coefficients in CTSDMs, determined by the values of resistors and capacitors, tend to be less stable and reliable compared to DT SDMs. Another challenge associated with CTSDMs is their inherent susceptibility to clock jitter [10]. Nevertheless, certain techniques, such as multi-bit quantization to reduce the step size of the digital-to-analog converter (DAC) feedback waveform, can mitigate the sensitivity to clock jitter.

One notable advantage of CT SDMs is their ease of driveability, as their input impedance is resistive. Additionally, their sampling frequency is primarily limited by the speed of the quantizer and feedback DAC, allowing CT SDMs to achieve higher sampling frequencies with lower power dissipation than DT SDMs.

Taking into account factors such as ease of drive, low power consumption, and the absence of a requirement for anti-aliasing filtering, we have opted for a CT SDM in our design.

### 2.1.2. ORDER OF SDM

According to the project's objectives, we aim to achieve a peak SNDR of 74dB and a peak SNR of 80dB within a 20-kHz bandwidth. To ensure robust performance even in less-than-ideal conditions, we have set a target Signal-to-Quantization Noise Ratio (SQNR) of 95dB in our ideal system-level design. This SQNR target is intentionally set 15dB higher than the target SNR, ensuring that the system is thermal noise limited and allowing for some performance degradation when considering other non-ideal factors.

Theoretical SQNR versus OSR for 1st-oder SDM and 2nd-order SDM with a two-level quantizer is shown in fig. 2.3. Although our design of the second stage integrator and quantizer differs from traditional structures, this figure can still provide us with preliminary theoretical support. It indicates that a 2nd-order SDM with an oversampling ratio (OSR) over $2^7$ could satify our requirement, while for the 1st-order SDM, it is only possible to meet the requirements through extremely high OSR. Higher order SDM can meet the requirements at lower OSR, but this involves more complex system stability considerations, so we ultimately decided to use second-order SDM as the initial design.

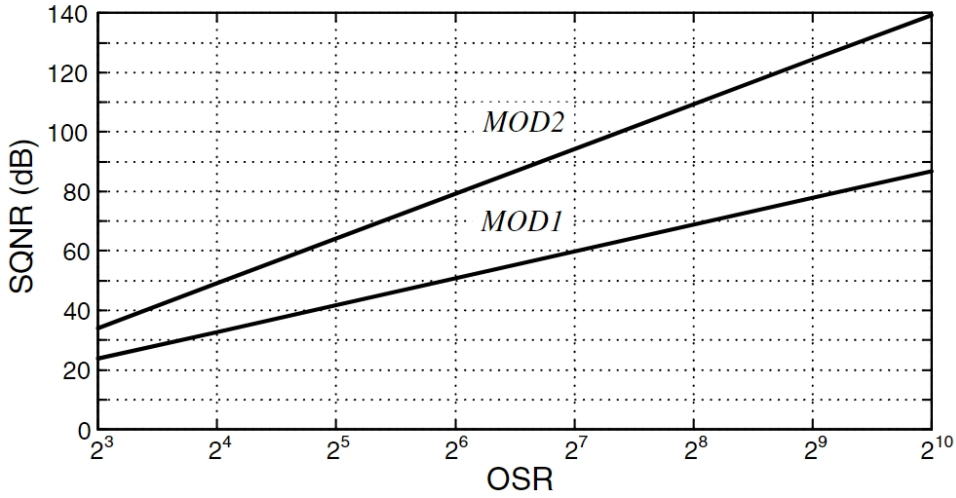


Figure 2.3: Theoretical SQNR versus OSR [10]

### 2.1.3. ARCHITECTURE OF SDM

The well-known cascade of integrators with feedback (CIFB) architecture of second-order SDM is shown in fig. 2.4, where the loop is stabilized through a distributed feedback network. This structure has several advantages like good robustness and high anti-aliasing filtering [10], but it also suffers from a few drawbacks that have lead to the interest to explore alternative architectures.

Because of the loop dynamics, the first integrator's output is compelled to cancel the digital-to-analog converter output. Consequently, the integrator input exhibits strong tonality, and the amplitude of the integrator output varies proportionally with the input amplitude. This constraint imposes limitations on coefficient scaling, resulting in an increase in the area of the ADC and noise impact from subsequent stages, ultimately diminishing overall power efficiency. Additionally, this input-dependent integrator output swing contributes to an elevated degradation in the SQNR for a nonlinear integrator, primarily due to quantization noise folding [12].

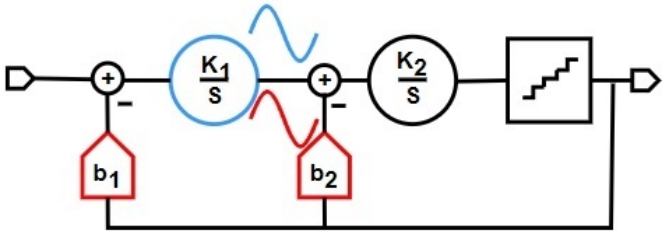


Figure 2.4: CIFB Architecture

Incorporating a feedforward (FF) path, as illustrated in fig. 2.5, addresses several of these challenges. Because the DAC at the integrator's output containing a scaled replica of the input signal, introducing a feedforward path from the ADC input to the integrator's output effectively cancels out the signal component emanating from the DAC. Consequently, the feedforward path mitigates the integrator's output swing, albeit at the cost of certain trade-offs, such as signal transfer function (STF) peaking and a reduction in anti-alias filtering, as the integrator is bypassed in this configuration. The reduced amplitude swing at the integrator's output permits more aggressive coefficient scaling and serves to linearize the integrator as it primarily processes quantization noise.

Nevertheless, it is essential for the feedforward path to maintain linearity as it processes the full swing input signal. Typically, to meet this stringent linearity requirement, the feedforward path is implemented by connecting a resistor from the input to the virtual ground of a closed-loop RC integrator further along the loop [12].

The architecture used in our design is the CIFB structure with pseudo-virtual ground (PVG) feedforward path [12], which is shown in fig. 2.6. It is based on the CIFB architecture with FF path shown in fig. 2.5, from which we can notice that the FF/DAC nodes and the ADC input node perform the same operation, i.e., $V_{in} - V_{DAC}$. Although the path gains exhibit variations, the ratios of these path gains, i.e., $b_2/a_1$ and $b_1$, remain the same, which allows the signal to be fed forward from the output of the first summation node instead of the input with appropriate scaling.

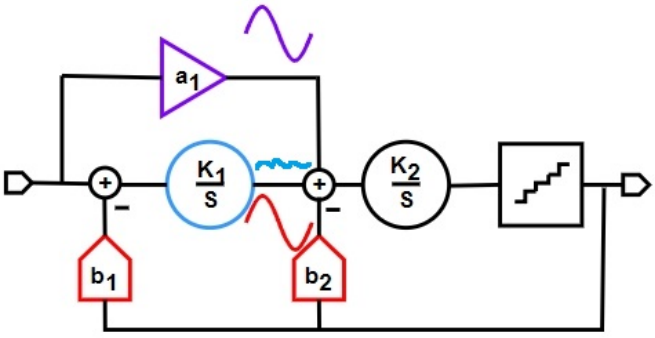


Figure 2.5: CIFB Architecture with FF path

Using this architecture, the loop will exhibit identical dynamics to that of the standard feedforward-based architecture. Furthermore, it offers several advantages, such as the elimination of the internal feedback DAC and the restriction of the feedforward path to processing only minor swings, contributing to enhanced linearization.

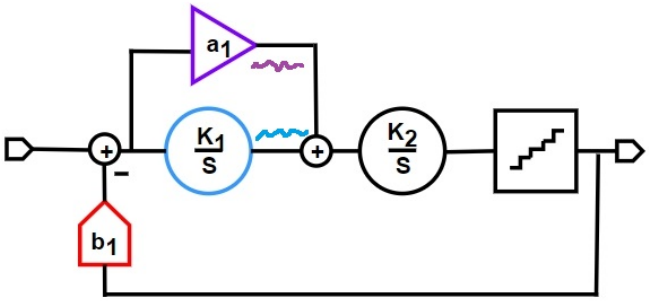


Figure 2.6: CIFB Architecture with PVG FF path

## 2.2. ARCHITECTURE OF DIFFERENT BLOCKS

The main blocks of second order SDM include the first integrator, the second integrator, the quantizer and the feedback DAC. In this section, the architecture choices of all the blocks are discussed.

### 2.2.1. FIRST INTEGRATOR

For CT loop filters, integrators are commonly implemented in active-RC structure, which mainly includes Opamp-RC and operational transconductance amplifier (OTA)-

RC structures. fig. 2.7 and fig. 2.8 shows the structure of the Opamp-RC integrator and the OTA-RC integrator respectively. The active-RC integrator has several attractive features. If the opamp is very ideal, a perfectly linear integrator is possible, because $V_{in}$ will be converted into a current $V_{in}$/R in a very linear fashion with the help of virtual ground. Furthermore, since every filter node is either a virtual ground, or the output of an opamp, opamp-RC filters are largely insensitive to stray capacitance [10].

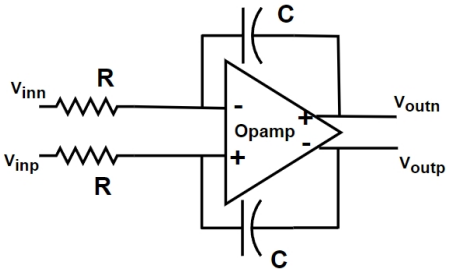


Figure 2.7: Opamp-RC integrator

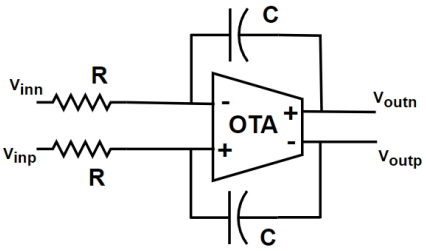


Figure 2.8: OTA-RC integrator

Nevertheless, achieving high performance in these filters necessitates the availability of an opamp with both substantial gain and bandwidth. In the context of low voltage CMOS processes, constructing an opamp with low output impedance capable of accommodating high swing operation proves to be a challenging task. Thus, an active-RC integrator, while having several attractive properties, also has significant disadvantages.

Active-RC integrators have a common problem that the input resistance is determined by resistor R, while the SDM in our design must offer a high input impedance because MEMS microphone possesses limited driving capacity. To prevent significant signal attenuation, a relatively large resistor R is necessary. However, this also results in substantial noise generated by R, which is directly coupled to the input in an active-RC integrator, resulting in an excessively high input-referred noise. Additionally, the elevated resistance value implies that resistor R will consume a considerable amount of area, diminishing the overall area efficiency of the system.

The transconductance-capacitance (Gm-C) integrator could meet the requirement of high input impedance by using an open-loop structure, as shown in fig. 2.9. The input impedance of the integrator is very high as it is the gate impedance of the transistor, and it is also capable of high speed operation due to the open loop nature of the integrator. To achieve a given dynamic range, the power efficiency will be poor due to the superior linearity accompanied by significant excess noise [13]. The presence of parasitic capacitance in parallel with the integrating capacitors makes Gm-C filters vulnerable to stray capacitance. Under these conditions, Gm-C integrators find utility in applications that demand a limited dynamic range, aligning with the intended purpose of this design.

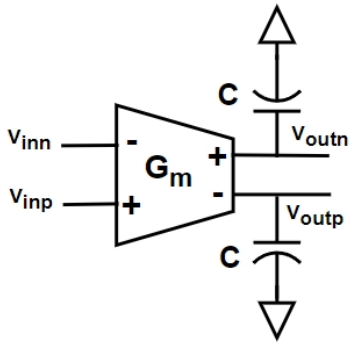


Figure 2.9: Gm-C integrator

There are also examples of using VCO based first stage integrators in related applications [6] [14]. Directly connecting the input signal to VCO can result in poor linearity and introduce a large amount of harmonic distortion, as the tuning curve of VCO is inherently nonlinear, which is shown in fig. 2.10. To mitigate this, a common approach involves running the VCO in a closed-loop configuration, which affects the input impedance and makes it unsuitable for our application. Alternatively, incorporating a highly linearized first stage before the VCO is another strategy. However, this comes at the cost of elevated power consumption, rendering the VCO integrator without clear advantages over the Gm-C integrator and introducing added circuit complexity.

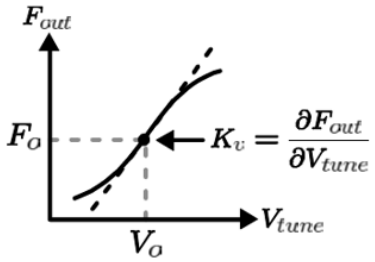


Figure 2.10: Nonlinear tuning curve of VCO [15]

### 2.2.2. SECOND INTEGRATOR

In evaluating options for the second integrator, active-RC, Gm-C, and VCO-based integrators are all under consideration. VCO-based integrators demonstrate advantages when applied as the second stage integrator, as its non-linearity is effectively mitigated by the loop gain. It also offers some advantages compared to conventional

solutions, which will be clarified in the following section.

The architecture of second integrator is shown in fig. 2.11. The VCO incorporates a Gm-cell, which is succeeded by a pair of 15-stage ring current-controlled oscillators (CCOs). The input voltage undergoes conversion into current via $G_{m2}$, and this resulting current governs the behavior of the two 15-stage CCOs. Employing $G_{m2}$, rather than directly controlling the VCO, offers greater flexibility in VCO tuning gain $K_{VCO}$ and results in improved linearity.

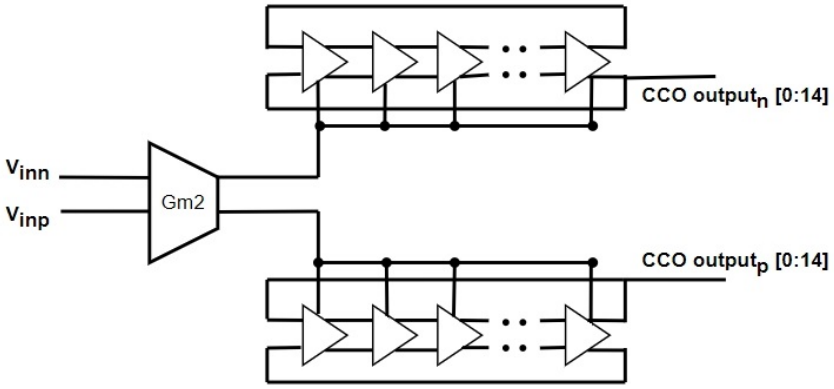


Figure 2.11: VCO-based integrator

### WORKING PRINCIPLE OF VCO-BASED INTEGRATORS

The VCO-based integrator employs multiple inverters. To grasp the functioning of the VCO, a ring oscillator is created using a set of five inverters as depicted in fig. 2.12. The output of each of these five inverters corresponds to $V_{out1}$ through $V_{out5}$, respectively. The gate delay of each ring stage is assumed to be identical and set to $T$ [16]. In the starting state $t$ = 0, $V_{out1-5}$ = [1,0,1,0,1]. At this time, both the input and output of the first inverter are "1". When the time goes to $t$ = $T$, the output of first inverter transitions to "0" and the state of the ring oscillator changes to $V_{out1-5}$ = [0,0,1,0,1]. For the next time $t$ = $2T$, the state of the ring oscillator changes to $V_{out1-5}$ = [0,1,1,0,1]. After repeating these steps ten times, i.e. $t$ = $10T$, the ring oscillator outputs return to its initial state: $V_{out1-5}(10T)$ = $V_{out1-5}(0)$ = [1,0,1,0,1].

Consequently, each output of this inverter chain exhibits a periodic signal with a signal period of $10T$, forming a ring oscillator. The value of $T$ is contingent upon the power supply voltage of the inverters, and this voltage can be considered directly proportional to the output frequency of the ring oscillator [16]. The

voltage-controlled gain, $K_{VCO}$, can be defined as the ratio of the change in VCO frequency ($\Delta f_{VCO}$) to the change in the supply voltage ($\Delta V_{in}$):

$$K_{VCO} = \frac{\Delta f_{VCO}}{\Delta V_{in}}, \tag{2.1}$$

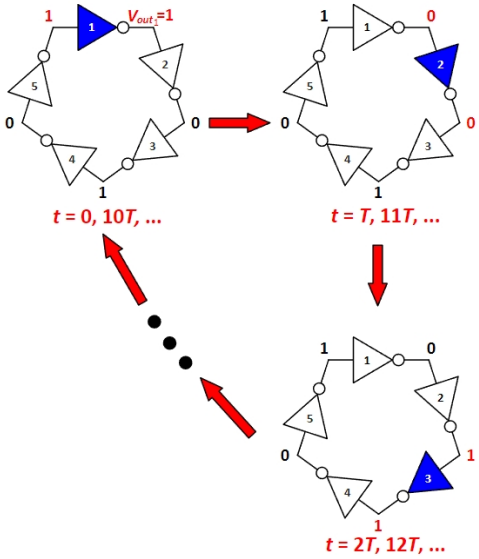


Figure 2.12: VCO operation diagram [16]

When $t = 10T$, the ring oscillator outputs return to its initial state. So the output of the VCO exhibits ten different states that can be uniformly represented across the phase domain, spanning from 0 to $2\pi$. The VCO output phase $\phi_{out}$ can be expressed as follows:

$$\Delta\phi_{\text{out}} = 2\pi \cdot f_{VCO} \cdot t \tag{2.2}$$

Combining Equation (2.1) and (2.2):

$$\frac{\phi_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{2\pi \cdot K_{VCO}}{s}. \tag{2.3}$$

Equation (2.3) demonstrates that the VCO functions as an ideal integrator with infinite DC gain. Consequently, in theory, it can be effectively employed in the design and implementation of the loop filter for a SDM.

### ADVANTAGES OF VCO-BASED INTEGRATORS

Employing VCO-based integrators in the SDM system can offer several advantages, which are outlined below, endorsing their utilization in the design.

**Simple structure**
VCO is mainly composed of inverters, so its structure is very simple, which also leads to its excellent performance in saving area and power consumption.

**Highly digital**
VCO-based integrators are highly digital, while CMOS scaling in both the transistor dimension and supply voltage leads to gate delay reduction in digital circuits, which means VCOs are very scaling friendly.

**Low voltage adaptability**
The simple structure of VCO enables it to work stably even at low voltage supplies, demonstrating great potential in low voltage application scenarios.

**Inherent multilevel quantization**
For the multi-stage inverter chain used in VCO, the output of each stage can be used for quantization operations, and multiple outputs naturally produce multilevel parallel quantization results. The inherent multilevel quantization characteristics of VCO have an active impact on improving quantization accuracy and reducing quantization noise.

**Tunable Integration Time**
The integration time of VCO-based integrators can be adjusted by controlling the VCO's operating frequency, allowing for flexibility in signal processing.

### 2.2.3. QUANTIZER

Multi-bit quantization is used to obtain a higher SQNR. A major advantage of multi-bit quantization is that the quantization has a smaller step size, which leads to less quantization noise. The reduced step size also yields a smaller signal swing in the loop filter and enables the circuit to function at a lower slew rate. Since clock jitter-induced noise is proportionate to voltage levels in the feedback DAC, employing multi-bit quantization with a reduced step size renders the modulator less susceptible to clock jitter.

Nevertheless, the adoption of multi-bit quantization often entails the necessity for additional comparators or one comparator with buffer registers and control logic circuits, consequently elevating circuit complexity and power consumption. Moreover, multi-bit feedback DACs introduce mismatch problems, compromising the overall performance of the modulator.

The second VCO-based integrator makes it easier to realize multi-level quantization as the output of each inverter can be used for quantization operations and naturally produce multilevel parallel quantization results. The outputs of VCO are in the phase domain, so phase quantizer composed of simple logical circuit can be utilized,

without significantly increasing circuit complexity and power consumption.

More importantly, the output pattern of dual-VCO structure has intrinsic Clock Level Averaging (CLA) property [17], the mismatch errors of feedback DACs are up-converted to tones around $2f_c$ and its multiples. With a well chosen $f_c$, the impact of the DAC mismatch will be significantly reduced. In this case, a dynamic element matching circuit is eliminated, which further reduces both power consumption and circuit complexity.



The strucuture of quantizer is shown in fig. 2.13, two CCOs operate differentially, and the output phases of these two CCOs are sampled using D flip-flop (DFFs) and then quantized utilizing an XOR-based phase detector. A differential dual-VCO structure is adopted to relieve the speed constraint of VCOs, as the output phases of the two CCOs are self-referenced, the center frequency $f_c$ of the VCO can be arbitrarily selected, irrespective of the sampling frequency. In the 15-stage ring current-controlled oscillator chain, all 15 outputs can be utilized for quantization, enabling the attainment of a 15-level quantized output and thereby enhancing quantization accuracy.

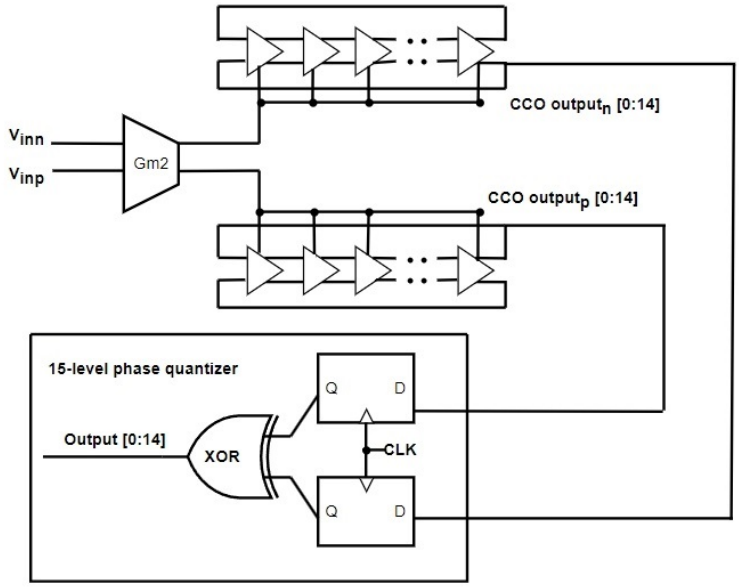


Figure 2.13: Structure of quantizer

### 2.2.4. DAC

In a CT SDM, the feedback DAC is responsible for converting the quantizer's output sequences into a waveform that closely resembles the input signal, with the exception of noise. The process of regulating a DAC to generate a feedback waveform from the digital output code produced by the quantizer can be represented or abstracted as a pulse shape, denoted as $p(t)$. Mathematically, the essence of the DAC can be regarded as the convolution of the digital code and pulse shape. The feedback waveform $v(t)$ injected into the input can be expressed as [18]:

$$v(t) = \sum_n v[n]\, p\,(t - nT_S) \tag{2.4}$$

where $v[n]$ denotes the output sequence of the quantizer, and $Ts$ denotes the sampling period.

A commonly used feedback DAC is the non-return-to-zero (NRZ) DAC, whose pulse shape can be expressed as:

$$p(t) = \begin{cases} 1, & 0 < t < T_S \\ 0, & t > T_S \end{cases} \tag{2.5}$$

A NRZ scheme is chosen to reduce the step size of the feedback DAC. With a 16-level feedback RDAC combined with the NRZ scheme, quantization step size will be reduced, which leads to less quantization noise. The structure of feedback DAC is shwon in fig. 2.14, digital output will go through a buffer and generate the reference voltage, then the reference voltage will control the feedback RDAC and generate the feedback current $I_{DAC}$, which will be subtracted with the input current in the following progress. Fifteen digital outputs correspond to 15 parallel feedback resistor array, which will generate 15 branches of feedback current.

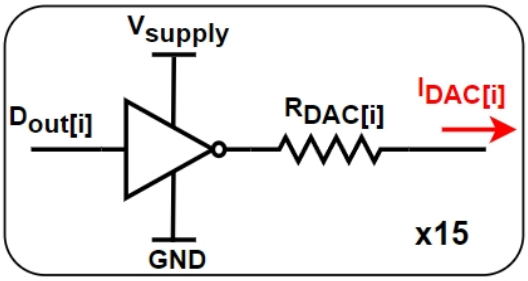


Figure 2.14: Structure of DAC

## 2.3. Total System Architecture

Based on the discussion on the architecture of the different blocks, the total system architecture is obtained by combining all the blocks, which is shown in fig. 2.15.

The second-order SDM comprises several key components: the initial Gm-C-based integrator, a subsequent VCO-based integrator, a 15-level digital phase quantizer, and a resistor feedback array.



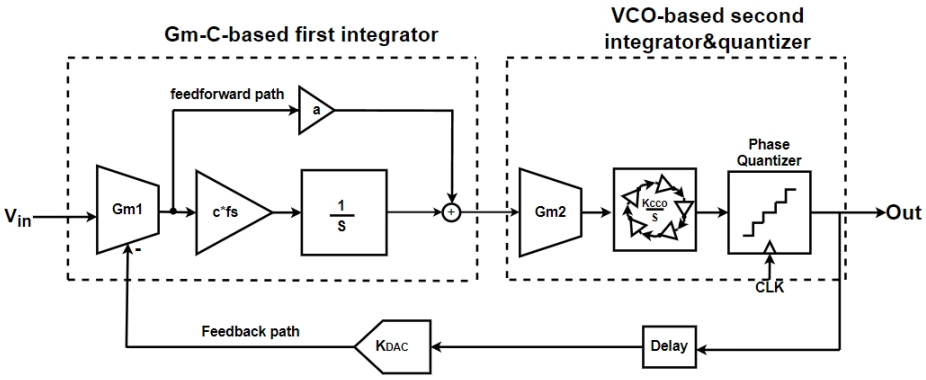


Figure 2.15: System architecture of the proposed second-order SDM

One noteworthy point is that in the first stage of Gm-cell , we used a source degradation structure to enhance linearity and presented it in the system level architecture. The feedback nodes are placed at both ends of the source degradation resistor instead of the input node to achieve a very high input impedance.

A feedforward path is needed to ensure the loop stability. In this work, the VCO serves as the second integrator, with output variables expressed in the phase domain. This choice introduces a challenge in implementing the summation of the feedforward paths before the quantizer. To address this issue, a proportional–integral (PI) transfer function is employed at the first integrator [7].

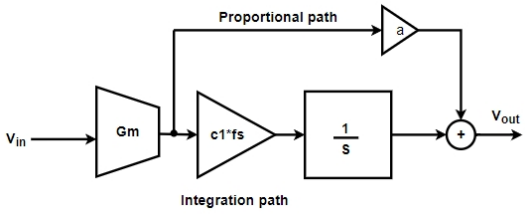


Figure 2.16: Block diagram of a PI

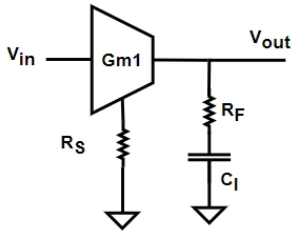


Figure 2.17: PI implemented with Gm-C.

fig. 2.16 shows the block diagram of the PI, which includes two signal paths: an integration path and a proportional path. fig. 2.17 shows the single-ended

implementation of PI with source-degenerated Gm-C integrator. The proportional path $a$ in fig. 2.16 can be easily realized by inserting resistor $R_F$ in series with the integrating capacitor $C_I$. The PI transfer function $H(s)$ can then be expressed as

$$H(s) = \frac{c_1 f_s}{s} + a_1 = \frac{1}{sR_S C_I} + \frac{R_F}{R_S}. \tag{2.6}$$

Since the effective Gm of the Gm-cell can be approximated as $1/R_S$, the proportional forward path $a$ is governed by the resistor ratio $(R_F/R_s)$.

## 2.4. SYSTEM LEVEL SIMULATION WITH IDEAL MODELS

A system-level simulation has been conducted in Cadence to confirm that the entire second-order SDM meets the requirement of achieving a SQNR exceeding 95dB. All components in the circuit are comprised of ideal models.

### 2.4.1. IDEAL MODEL OF VCO

A challenge we encountered was the absence of an accessible ideal VCO model in the simulator capable of producing multi-phase output. As a solution, we employed the Verilog-A programming language to define the VCO's ideal behavior and generate simulation modules.

An ideal VCO output can be expressed as a sinusoidal signal with amplitude and phase as shown below:

$$\mathrm{VCO_{out}}\ (t) = A_{\mathrm{vco}} \sin \phi_{\mathrm{vco}}(t) \tag{2.7}$$

The phase of the VCO is the integral of the VCO frequency which depends on VCO characteristics such as the free running center frequency, $f_c$ , VCO tunign gain, $K_v$ , and input signal to the VCO, i.e., the control voltage $V_{in}(t)$, which can be expressed as:

$$\phi_{\mathrm{vco}}(t) = 2\pi \int_0^{\infty} f_{\mathrm{vco}}(\tau)\mathrm{d}\tau = 2\pi \int_0^{\infty} f_{\mathrm{c}} + K_{\mathrm{v}} V_{in}(\tau)\mathrm{d}\tau \tag{2.8}$$

Based on the mathematical description of the ideal behavior of VCO, fig. 2.18 shows the central code snippet used to describe the ideal operational characteristics of the VCO. The multi-phase outputs of VCO are described as sine-waves with the same amplitude value but different phase delay. Subsequent buffers can pull these sine-wave outputs to either $V_{DD}$ or $V_{SS}$, making the output results closer to the real inverter chain outputs [15].

### 2.4.2. SIMULATION RESULT

In the system-level simulation employing ideal models, we have set the oversampling ratio (OSR) to be 250. The feedforward coefficient determined by the resistor ratio $(R_F/R_s)$ is set to be 2, which is obtained by sweeping the feedforward coefficients

```
analog begin
// Initialized Parameters
@(initial_step) begin
Ac=(vdd-vss)/2.0; // VCO Amplitude
vmid=(vdd+vss)/2.0; // Midrail Voltage
end
// Ideal VCO frequency and phase equations
fvco=Kv*V(in)+fc; // VCO Frequency
phase=2.0*`PI*idtmod(fvco,0,1,-0.5); // VCO Phase
for(i=0;i<N;i=i+1) begin
// Multiphase VCO output N phase taps
vcout[i]=vmid+Ac*sin(phase+i*2.0*`PI/N);
// multiphase VCO outputs go to level shifter
if (vcout[i]>=vmid) vcout[i]=vdd;
if (vcout[i]<vmid) vcout[i]=vss;
end
```

Figure 2.18: Verilog-A code snippet of VCO

from 0.5 to 4 in the simulator. The effective tuning gain of the VCO, denoted as $K_{VCO}$, is configured to be 0.8 MHz/V.

It's important to note that there exists a trade-off when selecting the value of $K_{VCO}$. A higher tuning gain can enhance the loop gain and result in improved Signal-to-Quantization Noise Ratio (SQNR) performance. However, it also means that the VCO will operate at a higher frequency, leading to increased power consumption. Therefore, choosing an appropriate value for $K_{VCO}$ is crucial to strike a balance between meeting the SQNR requirements and minimizing power consumption.

Given a 3.13 kHz sinusoid with an amplitude of 0.3 V, the FFT results of the modulators built using ideal modules is presented in fig. 2.19. Considering the targeted sensing application, bandwidth $f_b$ can be chosen as 20 kHz. The simulated SQNR result is 104.8dB, which is above the target SQNR 95dB and meets the requirement. So we can conclude that the second order SDM with VCO-based quantizer could basically satisfy the requirement of the project.

## 2.5. MODELING AND SIMULATION OF NONIDEALITIES

Incorporating non-ideal factors into the ideal modules used in system is a useful design approach. This allows us to model and assess the impact of these non-idealities on system performance, providing a more realistic representation of the actual circuit implementation. By simulating these non-ideal factors within the ideal system level simulation, we can gain insights into how they may affect the final results, helping us make informed design decisions and optimizations to achieve the desired performance in real-world scenarios.

For the first Gm-C integrator, there has been extensive research and solid theoretical foundation on its non ideal properties, mainly including nonlinearity, noise and bandwidth [7]. Therefore, in this part, we focus more on exploring the non-ideal properties of the second level VCO-based integrator.

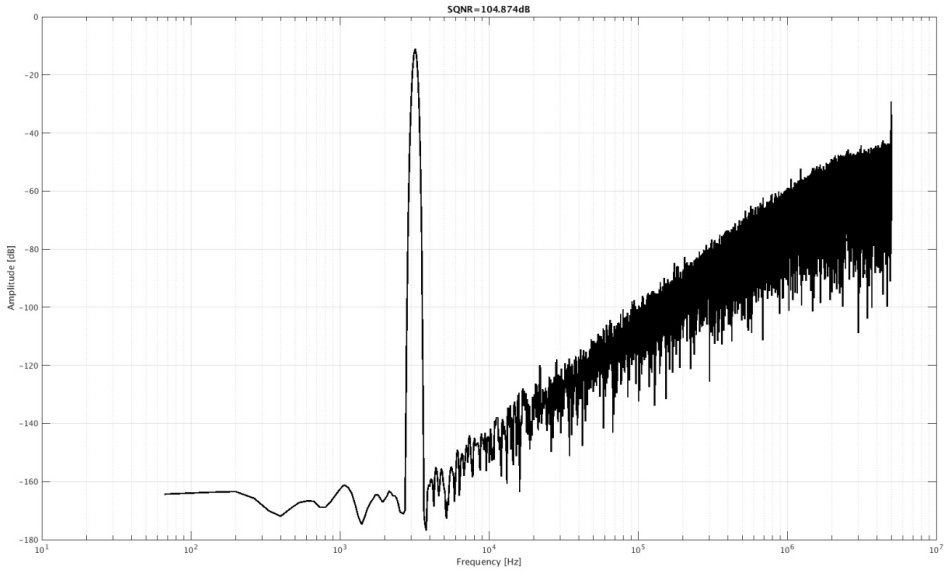


Figure 2.19: FFT results of modulators with ideal models

### 2.5.1. VCO Nonlinearity

The primary limitation in VCO-based quantizers arises from the nonlinearity present in the VCO tuning curve, which shown in fig. 2.10. This nonlinearity in the VCO's tuning characteristic leads to the appearance of harmonic spurs in the output spectrum. These spurs can deteriorate the SNDR, and the extent of this degradation is contingent upon the degree of nonlinearity exhibited in the tuning curve [15].

We characterized the non-ideal attributes of the VCO by incorporating a nonlinear term directly into its gain expression. As the VCO's nonlinearity introduces harmonic distortion into the FFT result, we gauge its impact by comparing the Signal-to-Quantization Noise-and-Distortion Ratio (SQNDR) with the initial SQNR result.

The tuning gain variation of the VCO versus the resulting SQNDR degradation is presented in table 2.1. Based on these results, we can draw the conclusion that the SDM exhibits a substantial tolerance for VCO nonlinearity. Specifically, a 20% tuning gain variation leads to only a 5dB reduction in SQNR. This tolerance ability can be attributed to factors including limited input swing and the suppression of gain in the first stage.

Table 2.1: Tuning gain variation of VCO versus SQNDR degradation

| Tuning gain variation | SQNDR Degradation |
|---|---|
| 0% (Ideally linear) | 0dB |
| 10% | 3.38dB |
| 20% | 5.04dB |
| 30% | 8.43dB |
| 40% | 9.98dB |
| 50% | 16.64dB |

### 2.5.2. VCO PHASE NOISE

Phase noise in the frequency domain can be equivalently represented as jitter in the time domain. Jitter contributes to variations in the VCO period, and these variations ultimately manifest as phase noise in the VCO output signal [15].

To assess the impact of phase noise on the VCO-based quantizers, it's essential to introduce phase noise into the ideal VCO equations. This process involves converting phase noise from the frequency domain into time domain jitter. The resulting time-domain jitter is then added to the instantaneous VCO period, reflecting how phase noise influences the VCO's behavior in a time-dependent manner. fig. 2.20 shows the Verilog-A code of VCO which includes the phase noise. In this model, jitter is considered white, with a normal distribution with standard deviation $\sigma$. This jitter value is then added to the period of the VCO, and inverted to get the instantaneous frequency of the VCO [15].

```
// Begin VerilogA code adjustment: VCO with phase noise
// VCO with phase noise
fvco=Kv*V(in)+fc; // VCO Frequency
fjvco=1/(1/fvco+jitter); // Add jitter
phase=2.0*`PI*idtmod(fjvco,0,1, -0.5); // VCO Phase
vcout=Avco*sin(phase); // VCO output
// Update jitter twice per period
@ (cross(phase + `PI/2, +1, ttol) or cross(phase - `PI/2, +1, ttol)) begin
jitter=sqrt(2)*($rdist_normal(seed,0,sig));
end
```

Figure 2.20: Verilog-A model of VCO phase noise

The outcomes following the inclusion of phase noise are documented in table 2.2, illustrating the correlation between SQNDR degradation and the standard deviation of jitter. These results lead us to the conclusion that the SDM effectively mitigates the influence of VCO phase noise. Specifically, jitter with a standard deviation below 1 ns has a negligible impact on the SQNR, showcasing the robustness of the system to phase noise effects.

Based on the results presented above, it becomes apparent that the non-ideal characteristics introduced by the second-stage VCO are effectively mitigated by the loop gain of the SDM. Consequently, the second stage does not appear to be

Table 2.2: Standard deviation of jitter versus SQNDR degradation

| Standard deviation of jitter | SQNDR degradation |
|---|---|
| 10ps | Almost no degradation |
| 100ps | Almost no degradation |
| 1ns | 3dB |
| 5ns | 8dB |
| 10ns | 12dB |

the primary contributor to the system's performance degradation. In contrast, the performance and non-ideal traits of the first stage integrator exert a more substantial influence on the overall system. Thus, it is advisable to prioritize and focus more on enhancing and addressing the characteristics of the first stage integrator during the circuit design process.

# 3

# CIRCUIT IMPLEMENTATION

As discussed in last chapter, a CT SDM with Gm-C first integrator is the chosen architecture to meet the requirement of high input impedance for the input stage. The considerations about the circuit implementation of the key circuit blocks of the SDM are discussed in this chapter, and simulation results are given.

## 3.1. INPUT INTEGRATOR

For the input stage, a Gm-C based integrator was chosen to meet the requirement of high input impedance. However, in addition to high input impedance, the first stage integrator must also provide good performance in terms of linearity and noise, as the non-ideal characteristics of the first stage are not suppressed by loop gain, thus playing the most critical role in the overall system performance.

Resistive source degeneration stands out as a widely used method for linearization, effectively addressing issues arising from variations in the transconductance of the input transistors at the input level. Using the differential input pair with resistive degeneration in fig. 3.1 as an illustration, the stage's effective transconductance is:

$$G_m = \frac{g_{m1}}{1 + g_{m1} R_s} \tag{3.1}$$

where $g_{m1}$ represents the transconductance of the input transistors $M_1$. When $g_{m1}R_s$ significantly exceeds 1, Equation (3.1) simplifies to $G_m = 1/R_s$, ensuring a relatively constant value. Consequently, the voltage gain of this stage, $A_v = G_m R_{out}$, remains independent of the input level with a stable transconductance.

With the determined current flowing through $M_1$, the source degeneration resistance also extends the input range by a factor of $(1 + g_{m1}R_S)$. The signal current, dictated by the effective transconductance, is $I_{out} = G_m V_{in}$, and it diminishes as $R_s$ increases. $R_s$ is also related to the saturation current flowing through $M_1$, which further affects the power consumption. Simultaneously, $R_s$ acts as a crucial source of input

referred noise. Therefore, the inclusion of resistive degeneration $R_s$ represents a delicate balance, navigating trade-offs among linearity, noise, power dissipation, and gain.



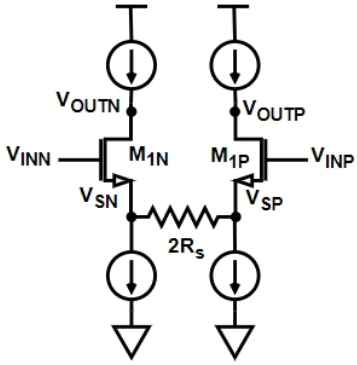


Figure 3.1: Differential input pair with source-degeneration

Increasing $R_s$ enhances linearity but comes at the expense of poorer noise performance and a larger area occupation. To optimize linearity without a significant increase in input-referred noise, Gm-boosting amplifiers are commonly introduced to the input pairs $M_1$ [7], as depicted in fig. 3.2.

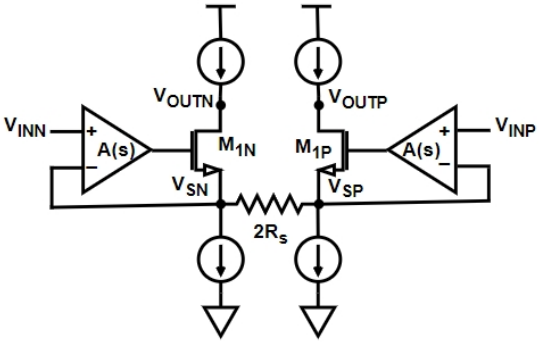


Figure 3.2: Differential input pair with Gm-boosting amplifier

The Gm-boosting cells serve as high-gain amplifiers, possessing a voltage gain denoted by $A(s)$. The differential input is linked to the positive inputs of both Gm-boosting cells, while their negative inputs are tied to the sources of the input pairs $V_{SN}$ and $V_{SP}$, creating negative feedback loops. The output of the Gm-boosting cells is directly connected to the gate of the input pairs.

Assuming a slight change $\Delta V$ in $V_{INN}$, the negative input of the Gm-boosting cell $V_{SN}$ will not change immediately. The input linked to the gate of $M_{1N}$, however, will experience a rise of $A(s)\Delta V$, inducing a corresponding increase in $V_{gs}$ of $M_{1N}$. To maintain the current $I_D$ flowing through $M_{1N}$, $V_{gs}$ will need to remain constant, which means that the source voltage $V_{SN}$ also needs to increase by $A(s)\Delta V$. In essence, the change in source voltages of the input pairs will duplicate the change of differential input. Hence, the Gm-boosting cell and the input transistor function as a transistor with an augmented transconductance, $g_{m1}A(s)$. The overall effective transconductance of the initial integrator can be expressed as:



$$G_{m,eff} = \frac{g_{m1}A(s)}{1 + g_{m1}A(s)R_s} \approx \frac{1}{R_s} \tag{3.2}$$

With a $g_{m1}$ enhanced by $A(s)$, $G_{m,eff}$ can be very close to $1/R_S$ even with a relatively small $R_s$, which achieves high linearity while ensuring low noise introduced by source degeneration resistor.

In this solution, the Gm-boosting cell is typically realized through a folded-cascode amplifier, capable of providing a DC gain $A(s)$ exceeding 80dB [7]. Nonetheless, this heightened gain accompanies a substantial power consumption, making the Gm-boosting amplifier the most power-intensive element of the integrator. As discussed in Chapter 1, audio applications may permit a higher level of distortion compared to stricter demands for low noise. Consequently, the necessity for linearity in the Gm-cell can be eased, allowing for a reduction in power consumption and circuit complexity.

Hence, some adjustments have been implemented to this structure, tailoring it to better align with our specific application requirements. fig. 3.3 shows the schematic of the proposed Gm-C integrator. A local Gm-boosting feedback loop replaces the Gm-boosting amplifier, ensuring an appropriate linearity performance without consuming excessive power consumption. The input stage converts the differential input voltage into a current which is copied to the output stage through the current mirror. Adjusting the proportion of the current mirror allows control over the output current, enhancing the circuit's operational flexibility [19].

The feedback nodes are placed at both ends of the source degradation resistor instead of the input node to achieve a very high input impedance, while the linearity will also be improved. When an input voltage is applied to the input pair, a current proportional to the input flows through the source degeneration resistor $R_S$. If there is no feedback DAC, this current will directly flow into the current mirror and results in an output current that is strongly correlated with the input [7].

While for the proposed structure, the feedback DAC is connected in parallel with the degeneration resistor $R_S$ . The current $I_S$ generated by the $R_S$ and the feedback current $I_{DAC}$ generated by the feedback DAC are subtracted at the source of the

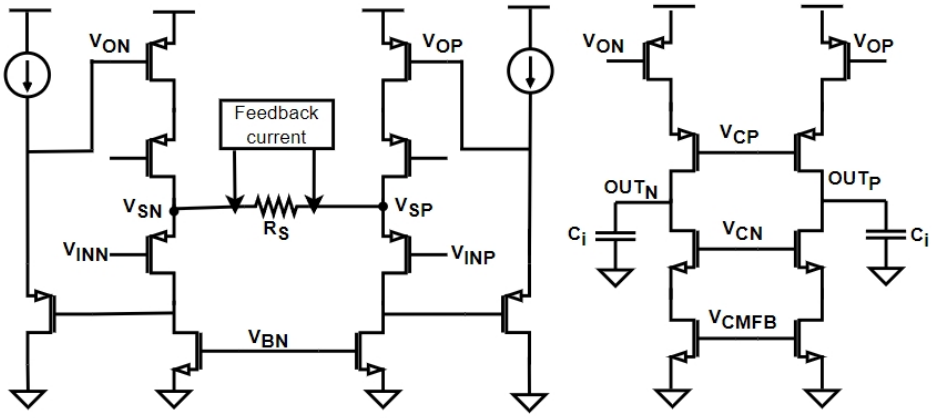


Figure 3.3: Structure of proposed first integrator

input pair. Due to the negative feedback nature of ΣΔ-loop, $I_{DAC}$ follows the $I_S$ very closely. Then, the current flowing into the current mirror will become much smaller and is no longer proportional to the input voltage, which makes a relaxed requirement on the linearity of the Gm-cell.

### 3.1.1. DESIGN OF THE GM-CELL

As for the design of the Gm-cell, several essential metrics need consideration, mainly including linearity, loop stability, transconductance bandwidth and noise performance.

#### LINEARITY AND STABILITY

For the proposed Gm-cell, a local Gm-boosting loop is used to improve the linearity performance of the Gm-cell. The loop is designed to achieve a loop gain over 50dB while ensuring the loop stability at the same time.

The feedback loop is broken by an Iprobe to perform the stability (stb) analysis, and the result is shown in fig. 3.4. With a loop gain larger than 50dB, $1+g_{m1}A(s)R_s$ is guaranteed to be much larger than 1, which helps good linearity to be achieved. The negative feedback loop is also stable with a 64° phase margin. The input PMOS transistors have their bulks directly connected to the sources, effectively mitigating the body effect. This results in a reduction in threshold voltage ($V_{th}$) and an enhancement of the input common-mode range [7].

To assess the efficacy of the Gm-boosting loop in enhancing linearity, an ideal Cadence Fourier component was introduced into the circuit, followed by a transient

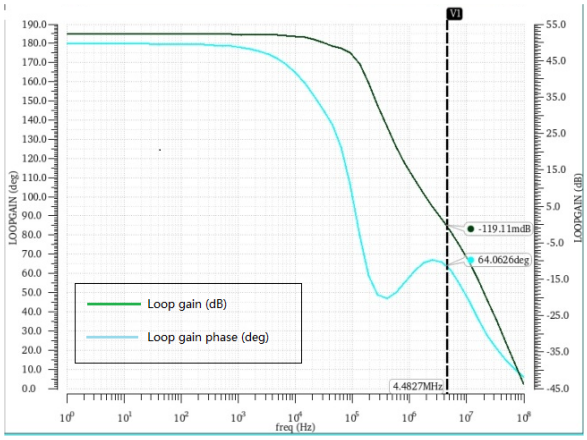


Figure 3.4: Frequency response of the feedback loop

simulation for verification. The simulated block encompasses the first integrator depicted in fig. 3.3, incorporating a common-mode feedback (CMFB) circuit. The details of the CMFB circuit will be elucidated in the subsequent section. The feedback path of the SDM is not included which means the integrator is fully working in open-loop manner. The object of the distortion simualtion is the output voltage of the integrator, which are $OUT_N$ and $OUT_P$ in fig. 3.3.

fig. 3.5 illustrates the distortion introduced in the output current when a sinusoidal voltage is applied at the input of the Gm-cell with a Gm-boosting loop, while fig. 3.6 shows result for a Gm-cell without the Gm-boosting loop. The amplitude of the input signal is 0.3V, corresponding to the full-scale input in our target application. The result shows that total harmonic distortion introduced by the open-loop Gm-cell is around -44.4 dB, while the total harmonic distortion decreases to about -73.3dB after adding the Gm-boosting loop, which indicates that the added loop effectively improves the linearity of the Gm-cell.

### TRANSCONDUCTANCE BANDWIDTH

The transconductance bandwidth of the Gm-cell will affect the performance of noise shaping. A preliminary requirement is that the bandwidth could reach the sampling frequency. To reach the required bandwidth, the biasing current of the main branch of the Gm-cell is set to be 12 $\mu A$. The simulated transconductance bandwidth, as depicted in fig. 3.7, falls slightly short of the 10MHz sampling frequency. However, the simulation results in the next chapter confirm that it sufficiently meets our SNR and SNDR requirements. Therefore, no additional power is allocated to strictly reach the specified frequency requirements.

```
======================
Fourier Analysis 'FOUR0'
======================

Fundamental frequency = 11 kHz.
Fundamental period = 90.9091 us.

Fourier components of V(OUTN,OUTP) for the interval from 409.091 us to 500 us:
DC = 2.08578 mV.

Harm:  Absolute       Absolute       Relative       Relative
       Magnitude      Phase          Magnitude      Phase
   1:  2.176 mV       179.96 Deg     0.000 dB       0 Deg <- normalizer
   2:  2.47327 nV     -89.9768 Deg   -118.888 dB    -269.937 Deg
   3:  467.192 nV     -9.68527 Deg   -73.363 dB     -189.645 Deg
   4:  1.17523 nV     -89.6413 Deg   -125.351 dB    -269.601 Deg
   5:  26.5692 nV     110.613 Deg    -98.266 dB     -69.3467 Deg
   6:  784.854 pV     -89.6258 Deg   -128.857 dB    -269.586 Deg
   7:  7.93116 nV     -96.4148 Deg   -108.766 dB    -276.375 Deg
   8:  588.942 pV     -89.4213 Deg   -131.352 dB    -269.381 Deg
   9:  4.03822 nV     76.6781 Deg    -114.629 dB    -103.282 Deg
Total harmonic distortion = 21.5092 m% (-73.3475 dB).
RMS value of computed spectrum (excluding DC) = 2.176 mV.
RMS value of computed spectrum (including DC) = 3.01421 mV.
Nonperiodicity (first/last point mismatch) = 17.5172 nV (805.017 u%).
```

Figure 3.5: Distortion of Gm-cell with feedback loop

```
======================
Fourier Analysis 'FOUR0'
======================

Fundamental frequency = 11 kHz.
Fundamental period = 90.9091 us.

Fourier components of V(OUTN,OUTP) for the interval from 409.091 us to 500 us:
DC = 418.044 pV.

Harm:  Absolute       Absolute       Relative       Relative
       Magnitude      Phase          Magnitude      Phase
   1:  2.6107 mV      90.3664 Deg    0.000 dB       0 Deg <- normalizer
   2:  39.6922 nV     -91.384 Deg    -96.361 dB     -181.75 Deg
   3:  13.942 uV      178.981 Deg    -45.449 dB     88.6141 Deg
   4:  356.812 pV     174.322 Deg    -137.286 dB    83.9557 Deg
   5:  6.28635 uV     -6.90409 Deg   -52.367 dB     -97.2705 Deg
   6:  756.985 pV     178.412 Deg    -130.753 dB    88.0452 Deg
   7:  3.30708 uV     168.904 Deg    -57.946 dB     78.5373 Deg
   8:  735.762 pV     174.655 Deg    -131.000 dB    84.2885 Deg
   9:  1.76447 uV     -16.2266 Deg   -63.403 dB     -106.593 Deg
Total harmonic distortion = 603.15 m% (-44.3915 dB).
RMS value of computed spectrum (excluding DC) = 2.61074 mV.
RMS value of computed spectrum (including DC) = 2.61074 mV.
Nonperiodicity (first/last point mismatch) = 626.516 nV (23.998 m%).
```

Figure 3.6: Distortion of Gm-cell without feedback loop

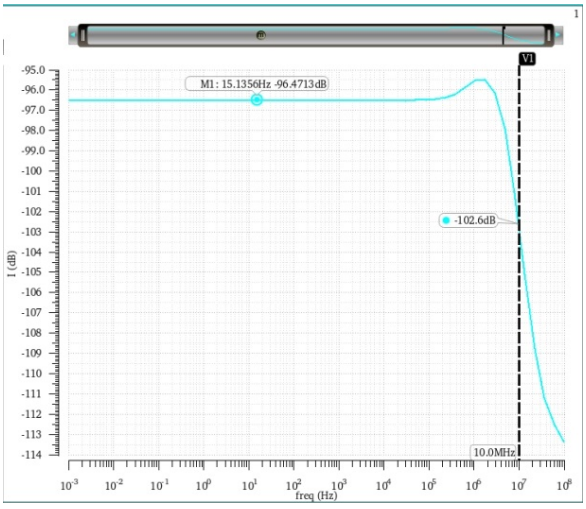


Figure 3.7: Simulated transconductance bandwidth

### NOISE

As the input stage, the first integrator plays a pivotal role in determining the overall noise level of the entire SDM. This section meticulously analyzes each noise source and its respective contribution. fig. 3.8 illustrates an equivalent half circuit of the Gm-C used for noise calculation, where the output stage of the integrator is not included as its noise contribution is negligible.

1) For $M_5$ and $M_6$: The thermal and $1/f$ noise of $M_5$ and $M_6$ will be effectively mitigated by a factor of $A_v^2$ when referred to the input node, with $A_v$ representing the voltage gain from the input to the drain of $M_1$. As a result, the input-referred noise of $M_5$ and $M_6$ is minimal, exerting negligible influence on the overall noise performance.

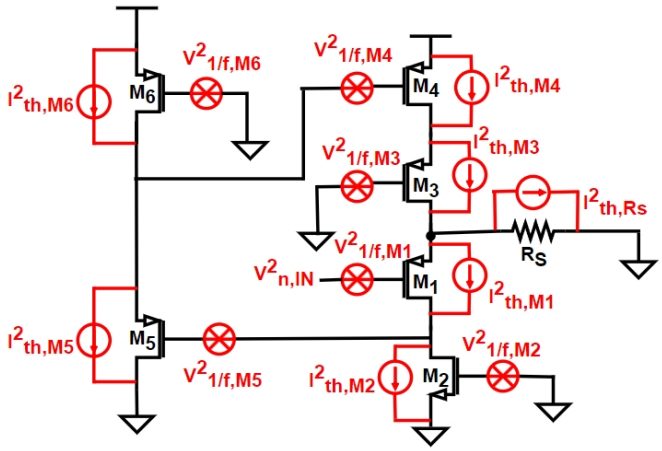


Figure 3.8: Equivalent half circuit of the input stage for noise calculation

2) For $M_3$: $M_3$ is the cascode transistor, which contribute negligible input-referred noise.

3) For $M_2$ and $M_4$: For the noise of the current sources, the input-referred thermal noise of$M_2$ and $M_4$ can be expressed as:

$$v_{n,\ \mathrm{cs.th}}^2 = \frac{4kT\gamma\left(g_{m2}+g_{m4}\right)}{G_{m,\ \mathrm{eff}}^2} = 4kT\gamma R_S \frac{\left(g_{m2}+g_{m4}\right)}{G_{m,\ \mathrm{eff}}} \tag{3.3}$$

where $\gamma$ represents the channel thermal noise factor, while $g_{m2}$ and $g_{m4}$ denote the transconductances of $M_2$ and $M_4$, respectively.

The input-referred $1/f$ noise of $M_2$ and $M_4$ can be expressed as:

$$v_{n,\mathrm{cs.1}/f}^2 = \frac{Kg_{m2}^2}{fC_{\mathrm{ox}}(LW)_2 G_{m,\mathrm{eff}}^2} + \frac{Kg_{m4}^2}{fC_{\mathrm{ox}}(LW)_4 G_{m,\mathrm{eff}}^2} \tag{3.4}$$

To reduce the noise introduced by the current sources, a small ratio of $g_{\mathrm{m2,4}}/G_{m,\mathrm{eff}}$ is used. This ensures a proportional reduction in the input-referred noise. To further reduce the $1/f$ noise, a relatively large size is chosen for the current source.

4) For $R_S$: The noise of degeneration resistor $R_S$ can be expressed as:

$$v_{n,\mathrm{R_S}}^2 = \frac{i_{n,R_S}^2}{G_{m,\mathrm{eff}}^2} = \frac{4kT}{R_S G_{m,\mathrm{eff}}^2} = 4kTR_S \tag{3.5}$$

A resistance of 20kΩ is chosen based on the trade-off of noise, linearity and power consumption.

5) For $M_1$: The input-referred thermal noise of input transistor $M_1$ can be expressed as:

$$v^2_{n,\ M_1.\text{th}} = \frac{4kT\gamma}{g_{m1}} \tag{3.6}$$

The input-referred $1/f$ noise of input transistor $M_1$ can be expressed as:

$$v^2_{n,\ M_1.1/f} = \frac{K}{fC_{\text{ox}}(LW)_1} \tag{3.7}$$

A large pMOS input pair operating in weak inversion is used. With a large width and large transconductance, both thermal noise and $1/f$ noise and be mitigated effectively. The detailed transistor sizes are marked in fig. 3.9, which are designed to meet the requirement of noise performance.

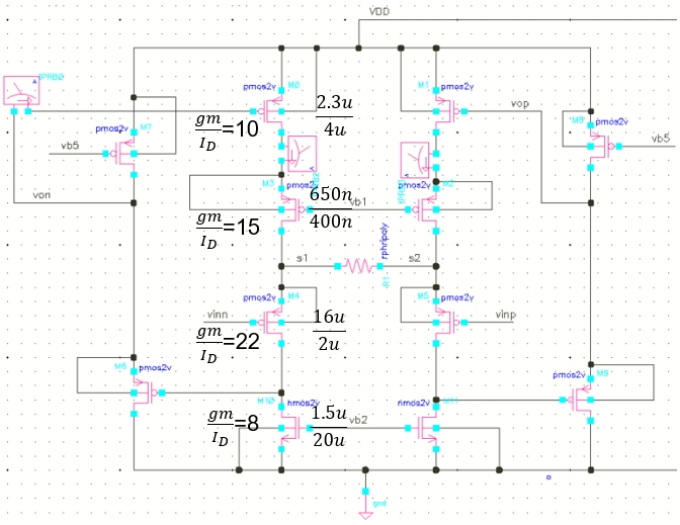


Figure 3.9: detailed transistor size

In our design, the total input-referred noise of the first stage is simulated to be $6.33\mu V_{rms}$ integrated over 20kHz signal bandwidth. The noise contributions of various transistors are illustrated in fig. 3.10. The analysis reveals that the input pair, the source degeneration resistor, and the NMOS current sources predominantly influence the noise, aligning with our design expectations.

| Device | Param | Noise Contribution | % Of Total |
|---|---|---|---|
| /M4 | id | 1.04859e-10 | 17.03 |
| /M5 | id | 1.04859e-10 | 17.03 |
| R1.rpure | thermal_noise | 1.01235e-10 | 16.44 |
| /M10 | id | 8.25719e-11 | 13.41 |
| /M11 | id | 8.25719e-11 | 13.41 |
| /M10 | fn | 4.37164e-11 | 7.10 |
| /M11 | fn | 4.37164e-11 | 7.10 |
| /M1 | id | 1.204e-11 | 1.96 |
| /M0 | id | 1.204e-11 | 1.96 |
| /M4 | fn | 8.33915e-12 | 1.35 |
| /M5 | fn | 8.33915e-12 | 1.35 |
| /M0 | fn | 5.28836e-12 | 0.86 |
| /M1 | fn | 5.28836e-12 | 0.86 |
| R1.rend1 | thermal_noise | 3.02604e-13 | 0.05 |
| R1.rend2 | thermal_noise | 3.02604e-13 | 0.05 |
| /M4 | rs | 4.65449e-14 | 0.01 |
| /M5 | rs | 4.65449e-14 | 0.01 |
| /M10 | rs | 3.90293e-14 | 0.01 |
| /M11 | rs | 3.90293e-14 | 0.01 |
| /M6 | id | 2.24425e-14 | 0.00 |

Integrated Noise Summary (in V^2) Sorted By Noise Contributors
Total Summarized Noise = 6.15744e-10
Total Input Referred Noise = 4.01866e-11
The above noise summary info is for noise data

Figure 3.10: Simulated noise summary

### 3.1.2. COMMON-MODE FEEDBACK CIRCUIT

In fig. 3.3, $OUT_N$ and $OUT_P$ represent the differential output of the Gm-C integrator. A CMFB circuit is employed to sustain a constant output common-mode voltage for the fully differential opamp, ensuring maximal symmetry in the output swing.

Existing types of CMFB circuits are the resistor averaging circuit (R-C), switched-capacitor (S-C) averaging circuit, and differential difference amplifier (DDA) [20]. Due to their susceptibility to clock jitter noise, SC CMFB circuits are deemed unsuitable for integration into oversampling systems. Consequently, initial consideration is given to resistor averaging CMFBs and DDA CMFBs for the output stage because of their uncomplicated circuit design.

Although large resistors contribute to heightened CM detection accuracy, they do come at the cost of occupying excessive area. Hence, for this Gm-cell, the DDA CMFB circuit depicted in fig. 3.11 is selected, which occupies a smaller area. Utilizing differential input pairs to sense and compare the output voltages of the first stage against the reference voltage $V_{CM}$, proportional currents are generated based on the detected voltages. These currents are mirrored to the output stage via $V_{CMFB}$, subsequently influencing the values of $OUT_N$ and $OUT_P$.

The CMFB circuits employ two differential input pairs using special PMOS transistors $pmosmvt2v$ to detect the output and compare it with the reference voltage. These PMOS transistors are medium transistors with a relatively small threshold voltage, ensuring sufficient headroom for the correct operation of other transistors.

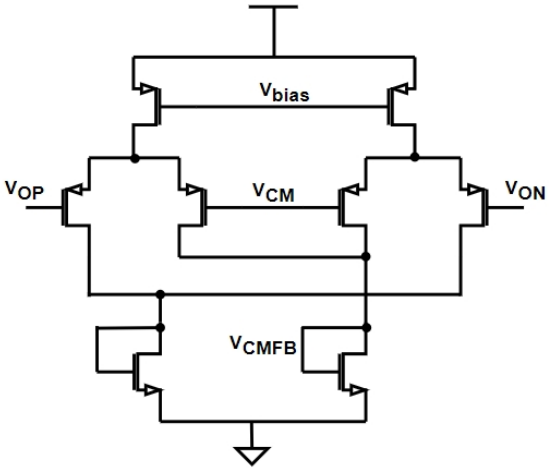


Figure 3.11: Schematic of the DDA CMFB circuit

## 3.2. RDAC

The feedback nodes are placed at both ends of the source degradation resistor, which is $V_{SN}$ and $V_{SP}$ in fig. 3.3. A direct way to realize feedback is to connect a resistor to one end of $R_S$, so that the current generated by $R_S$ and the feedback current generated by RDAC are subtracted at $V_{SN}$ and $V_{SP}$. RDAC is also suitable for VCO-based second integrator, as the thermometer-encoded output from the VCO can directly control the feedback RDAC without the need for additional decoding logic.

For a 15-stage VCO chain, a feedback resistor array composed of 15 resistors in parallel is used, with each resistor driven by thermometer-encoded output of the VCO. As illustrated in fig. 3.12, a NRZ scheme is chosen to reduce the step size of the feedback DAC, by which a voltage buffer implemented as an inverter is needed to generate the reference voltage and control the RDAC according to digital output. The resistance value of each resistor is set to 300kΩ, resulting in a parallel resistance value of 20kΩ for 15 resistors, which is the same as the source degradation resistance value. With a 1.2V $V_{SUPPLY}$, generated feedback current can effectively cancel the signal component in the input current.

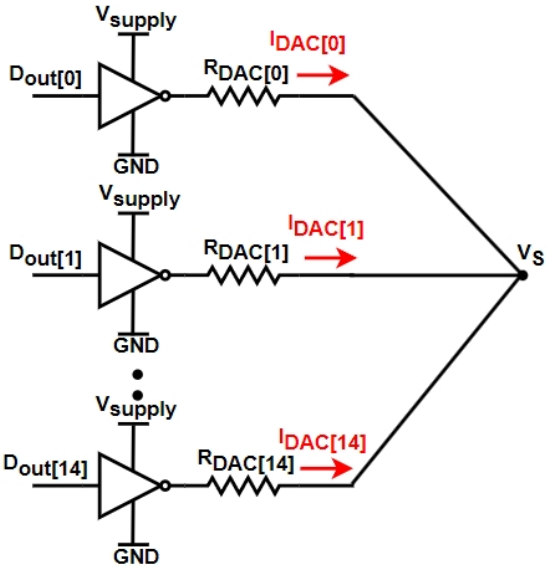


Figure 3.12: Schematic of RDAC

# 4

# SIMULATION RESULTS

This chapter presents and analyzes the simulation results for the entire integrated second-order SDM. The proposed SDM's top-level architecture is depicted in fig. 4.1, featuring the first Gm-C integrator illustrated in fig. 3.3. The second VCO-based integrator and quantizer are represented by an ideal model using Verilog-A to describe their behavior. The feedback DAC consists of a resistor array composed of 15 resistors in parallel with each resistor driven by the thermometer-encoded output of the VCO, as depicted in fig. 3.12.

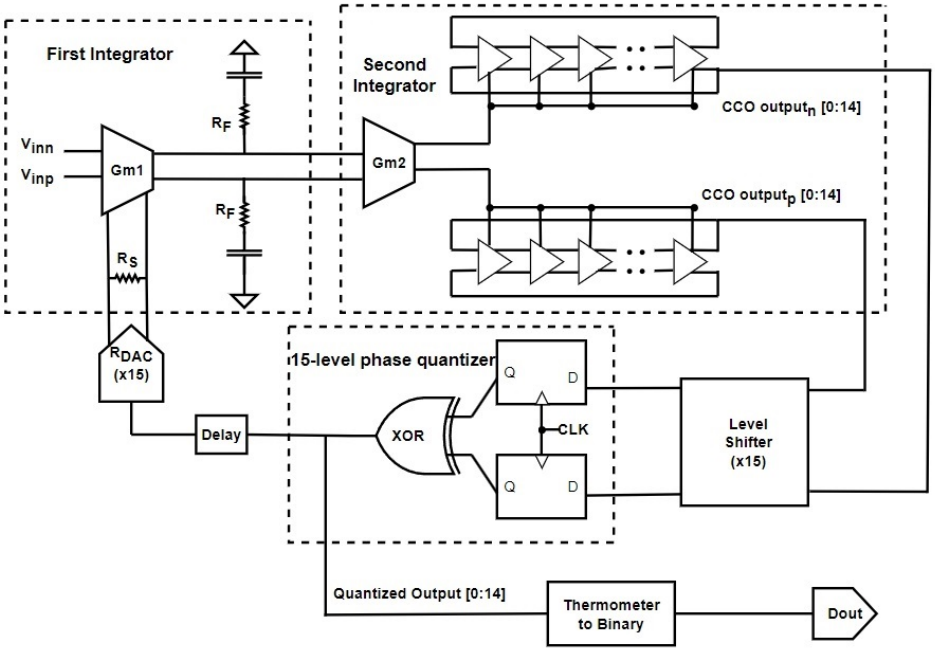


Figure 4.1: Schematic of the proposed SDM

## 4.1. SIMULATION RESULT

The simulation results of the total integrated SDM are presented in this section.

### 4.1.1. SIMULATION RESULT WITHOUT TRANSIENT NOISE

Given a 3.13kHz sinusoidal input with a full-scale amplitude of 0.3V, the frequency spectrum of the modulator output is presented in fig. 3.11. The FFT result shows that the SQNR of the SDM is 95.2dB, and the introduced total harmonic distortion (THD) is -81.7dB. Considering the THD, the obtained SQNDR is 81.5dB. The simulation result basically meets our design requirements.



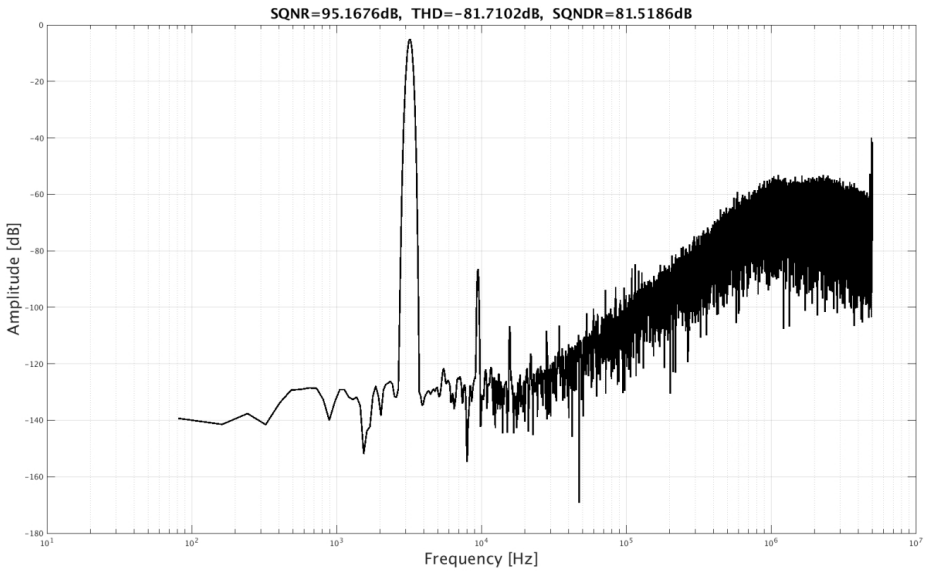


Figure 4.2: FFT result without transient noise

### 4.1.2. SIMULATION RESULT WITH TRANSIENT NOISE

The simulation result after adding the transient noise is shown in fig. 4.3. The red curve is the result without transient noise, while the black curve is result with transient noise. The FFT result shows that the SNR of the SDM is 83dB, which is 3dB higher than the target SNR of 80dB. Considering the THD, the obtained SNDR is 79dB, which is 5dB higher than the target SNDR of 74dB.

### 4.1.3. SIMULATION RESULTS UNDER DIFFERENT PVT CORNERS

Simulation results of SNR and SNDR under different PVT corners are shown in table 4.1. The results show that the SDM could meet the target SNR of 80dB

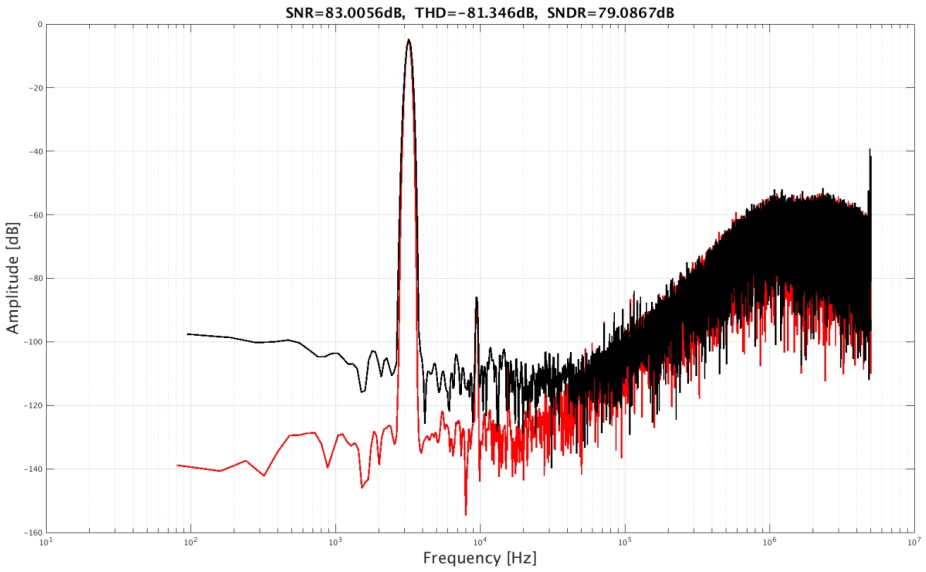


Figure 4.3: FFT result with transient noise

under all the PVT corners. While for the harmonic distortion performance, there is a deterioration where SNDR does not meet the requirement of 74dB under two conditions: at FS corner under -40°C and 27°C. But for audio applications, the impact of distortion is not very serious, and the difference is not much compared to the target of 74dB. Therefore, we can generally conclude that the designed SDM has achieved the set goal and has good stability under changes in PVT conditions.

Table 4.1: SNR and SNDR under different PVT corners

| Corner | TT | | | SS | | | FF | | | FS | | | SF | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| T | -40 | 27 | 125 | -40 | 27 | 125 | -40 | 27 | 125 | -40 | 27 | 125 | -40 | 27 | 125 |
| SNR/dB | 80.1 | 83.5 | 86.7 | 81.4 | 83.3 | 83.4 | 86.1 | 81.1 | 84.2 | 80.3 | 83.4 | 86.2 | 87.9 | 86.2 | 85.1 |
| SNDR/dB | 75.5 | 79 | 84.2 | 75.5 | 78.1 | 80 | 76.1 | 75.2 | 79.1 | 67.3 | 68.2 | 83.1 | 80.2 | 82.3 | 82.9 |

### 4.1.4. POWER CONSUMPTION

The current consumption of various SDM blocks is listed in table 4.2. The table shows that the current consumption of the first integrator is 30.35 $\mu$A, which dominates the power consumption to satisfy the requirement of linearity, noise and bandwidth. The total current consumption amounts to 35.76 $\mu$A, resulting in a power consumption of 54 $\mu$W with a 1.5V supply voltage. The VCO-based second integrator in implemented with ideal model in our system, so its power consumption is unknown. To estimate it, we reference the results in [7], where a similar

VCO-based integrator is used and consumes a current of 1.7 $\mu$A. Given that our ideal VCO operates at a close center frequency to [7], we assume a similar current consumption. Therefore, the estimated power current of the VCO-based blocks is 2 $\mu$A, resulting in a total power consumption for the SDM of approximately 57 $\mu$W.

Table 4.2: Current consumption of various SDM blocks

| | Current consumption ($\mu A$) |
|---|---|
| First integrator | 30.35 |
| Feedback DAC | 3.68 |
| Biasing circuit | 1.73 |



### 4.1.5. COMPARISON BETWEEN TARGETS AND OBTAINED RESULT

The targets and obtained results of the SDM are listed in table 4.3, along with the comparison with the prior art of the microphone readout SDM. The target SNR and SNDR are met with a power consumption of 57 $\mu$W, comfortably below the specified limit of 200 $\mu$W. Compared to prior work [3] and [8] which reach similar SNDR performance, the power consumption of this work has significant advantages. This is mainly attributed to the design of the first level Gm cell. With the help of a simple local Gm-boosting loop, the linearity of the Gm-cell can be effectively improved without significant increase in circuit complexity and power consumption. While for [3] and [8], large amount of power consumption is applied to improve the linearity of the first stage.

Table 4.3: Obtained results and comparison with the prior art

| | Obtained results[a] | Targets | [3] | [8] | [9] |
|---|---|---|---|---|---|
| Architecture | CTSDM | CTSDM | CTSDM | CTSDM | CTSDM |
| Year | 2023 | 2023 | 2014 | 2018 | 2021 |
| SDM order | 2 | 2 | 3 | 2 | 2 |
| Bandwidth (kHz) | 20 | 20 | 10 | 20 | 20 |
| Technology (nm) | 180 | 180 | 350 | 130 | 65 |
| Supply (V) | 1.5 | 1.5 | 3 | 1.8 | 1 |
| Power ($\mu$W) | 57 [b] | 200 | 630 | 560 | 142.6 |
| Area (mm2) | - | 0.4 | - | 0.04 | 0.11 |
| Peak SNDR (dB) | 79 | 74 | 74.2 | 76.6 | 94.2 |
| Peak SNR (dB) | 83.5 | 80 | 75.8 | - | 97.3 |
| Calibration | Not needed | Not needed | Not needed | Not needed | Needed |

[a] The listed results in the table are simulation results.
[b] This is an estimated total power consumption.

As mentioned in introduction, the core part of the project is to meet the SNR and SNDR target with lowest power consumption and reasonable area while no

calibration circuit is needed. According to the obtained result, we have met the requirement of SNR and SNDR with a power consumption that is estimated to be far below the target level. Yet, a precise comparison for the area remains elusive, given that the layout phase has not been finalized.

# 5

# CONCLUSION

## 5.1. SUMMARY

In this thesis, the theory and implementation of a high input impedance CT SDM for a MEMS microphone readout has been presented. A pseudo-virtual ground feedforward structure is used to eliminate the internal feedback DAC and contribute to enhanced linearization. To meet the requirement of high input impedance, a Gm-C first integrator is employed, featuring a resistive source degeneration structure and a local Gm-boosting loop to enhance the linearity of the first stage. For the second stage, VCO-based integrator and quantizer are employed, offering advantages including inherent multilevel quantization and an intrinsic CLA property. The entire system consumes an estimated 57 $\mu$W of power, achieving an 83dB SNR and a 79dB SNDR in simulation, meeting the predefined targets of the project.

There are two main contributions of this work: 1) A system-level ideal model with VCO-based blocks has been built, which helps to explore the characteristics and applications of VCOs on loop filters of SDMs. 2) A Gm-C integrator with local Gm-boosting loop has been designed and implemented to realize a high input impedance and ensure the needed linearity, without heavily increasing the complexity of input stage.

## 5.2. FUTURE WORK

1) In our ideal model, it has been verified that the non-idealities of the second integrator has a limited impact on the performance of the entire system. Therefore, more efforts can be invested in the modeling and simulation of the non-idealities of the first stage, including nonlinearity, finite bandwidth etc. This helps to obtain a complete system level ideal model for subsequent learning and design.

2) The power consumption of first Gm-cell can be further improved. The traditional Gm-boosting amplifier is replaced with a local Gm-boosting loop in this thesis, which simplifies circuit complexity and circuit design. However, compared to solutions

using amplifiers, this solution does not show advantage in power consumption. Although Gm-boosting loop consumes less power than the amplifiers, the main branch of the Gm-cell needs to consume more power to meet the requirement of bandwidth. Therefore, more efficient solutions can be explored from the perspective of further optimizing circuit structure.

3) The circuit implementation part of the VCO-based blocks has not been fully completed. The schematic design of these blocks need to be finished and be integrated in to the whole system.

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