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Cryogenic-Aware Forward Body Biasing in Bulk CMOS

Ramon W. J. Overwater, Masoud Babaie, *Senior Member, IEEE*, and Fabio Sebastiano, *Senior Member, IEEE*

***Abstract*— Cryogenic CMOS (cryo-CMOS) circuits are often hindered by the cryogenic threshold-voltage increase. To mitigate such an increase, a forward body biasing (FBB) technique in bulk CMOS is proposed, which can operate up to the nominal supply without problematic leakage currents, thanks to the larger diode turn-on voltage at cryogenic temperatures. As a result, traditional circuits, such as pass-gates, can operate down to 4.2 K, and their performance is augmented, e.g., digital circuits speeding up by 1.62× or lowering their energy per transition and energy-delay product by 4.24× and 2.33×, respectively. Unlike back biasing in FD-SOI, here all FBB voltages remain within the supplies, hence enabling on-chip and device-specific biasing. The proposed FBB technique thus represents a valuable design tool for bulk cryo-CMOS circuits.**

***Index Terms*— Cryo-CMOS, body biasing, bulk CMOS.**

I. Introduction

FOR several low-temperature applications, such as quantum computing, space exploration, and cryogenic computing, CMOS electronics operating at cryogenic temperatures (cryo-CMOS) have been proposed as an enabling technology [1], [2], [3], [4]. The development of the high-performance, low-power circuits required in these applications favors its unrivaled VLSI capability combined with improved device performance at cryogenic temperatures, e.g., the increased carrier mobility [5], the lower thermal noise [6], the steeper subthreshold slope (SS) [5], the reduced metal resistances and the higher quality factor of passives [7]. Despite these advantages, the significant increase in threshold voltage V_{th} (up to 180 mV at 4.2 K [8]) constitutes a big obstacle for circuit design, for instance, heavily hindering the increase in drive current induced by the enhanced mobility, and limiting the allowed voltage swing in commonly adopted circuits, such as sample-and-hold [9], [10]. Designers can counteract the increased V_{th} using more complex circuits, inevitably costing performance and/or power.

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To alleviate these setbacks, the MOS channel doping could be optimized for cryogenic operation, thus precluding wide-temperature operation and adding fabrication costs. Adopting an FD-SOI technology in combination with back-biasing to tune the V_{th} can drastically improve cryogenic performance [11]. However, in addition to the higher cost of FD-SOI with respect to bulk CMOS, tuning the V_{th} back to its room-temperature value requires biasing the back gate well beyond the process nominal supply due to the low body factor in FD-SOI technologies, e.g., requiring beyond 2 V for the back gate to compensate the V_{th} shift for a body-factor of 0.085 V/V [11], [12], [13]. As a consequence, either high-voltage on-chip generators would be required, increasing power consumption and complexity, or the back-bias voltages need to be delivered from off-chip. As an alternative, we propose using cryogenic-aware forward body biasing (FBB) in bulk CMOS. As the body factor in bulk CMOS is significantly larger, the required body bias voltage is lower [14]. However, a large body-source voltage could turn on the source-bulk diodes, leading to massive unwanted leakage currents. While this is a known hard limit at room temperature, the diode turn-on voltage increases beyond the supply rails at cryogenic temperatures [15], [16], thus potentially preventing the leakage. Recent work [17] has already shown an improvement in reliability down to 80 K and FBB voltages only up to 0.5 V. However, the proposed technique demonstrates, for the first time, the full potential of FBB for cryogenic low-power and high-performance bulk CMOS designs by presenting its experimental characterization and validation for both devices and circuits.

II. Cryogenic-Aware FBB Characterization

A 40-nm LP triple-well CMOS test chip has been fabricated, comprising both standard- and low-V_{th} (SVT/LVT) transistors, and ring oscillators (ROs) to test the performance of digital circuits. All 384 transistors are connected in parallel and share the Kelvin-connected source and drain connections, but their gates are individually switchable to V_g or V_s by a thick-oxide switch. They have been characterized with Keysight 2636B SMUs and their threshold is extracted using the maximum g_m method at $V_{DS} = 50$ mV [18]. Each RO consists of $N = 1025$ inverters and an enabling thick-oxide switch in series. Of the 144 ROs, 116 have varying widths and minimum length (40 nm). The others have minimum width (120 nm) and lengths between 45 nm and 120 nm. The oscillators' output frequency is measured with a Rigol DSA815 spectrum analyzer, while simultaneously measuring their supply and body bias currents using the SMUs. The transition time of

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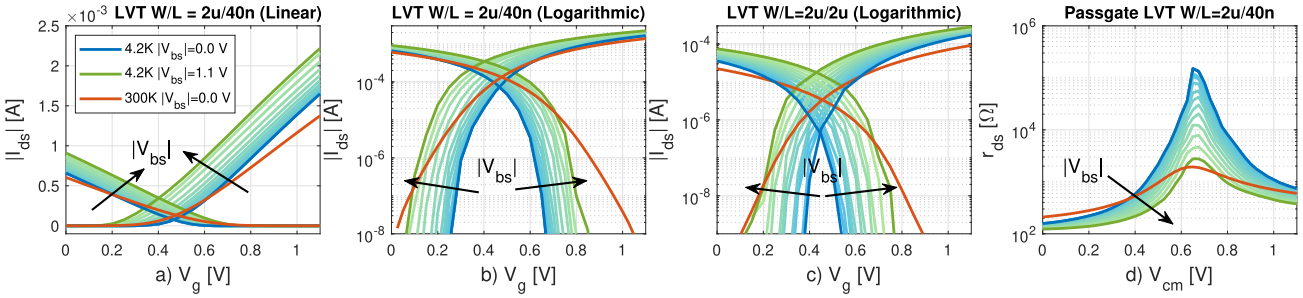

Fig. 1. DC measurements of LVT NMOS/PMOS devices at 300 K (red line) and 4.2 K (green to blue lines). For the 4.2-K results, the body-biasing $|V_{bs}|$ is swept from 0 V to 1.1 V in steps of 0.1 V (shades). To improve readability, the leakage is subtracted. The NMOS source is grounded, and the PMOS source is connected to $V_{dd} = 1.1$ V. (a-b) I_{ds}/V_g at $|V_{ds}| = 1.1$ V for $W/L = 2\mu$m/40nm in linear and semi-logarithmic scale. (c) $W/L = 2\mu$m/2μm in semi-logarithmic scale. (d) Small-signal resistance of the pass gate vs. the voltage applied on the drain/source, obtained by numerically combining in parallel the individually measured NMOS and PMOS resistance of (a-b).

a single stage $t_d = 1/(2Nf)$ is computed from the frequency, and is combined with the total RO power ($P = V_{dd} \cdot I$) to obtain the energy per transition (EPT $= P \cdot t_d$) and energy-delay product (EDP $= P \cdot t_d^2$). The 4.2-K data was obtained by submerging the chip into liquid helium inside a dewar using a dipstick.

A. Transistor Static Characteristics

Figure 1a and b show the I_{ds}/V_g curves of a single minimum-length NMOS and PMOS device. To improve the readability of Fig. 1, the leakage current of all parallel transistors with $V_{gs} = 0$ V is subtracted in the plots. As expected and highlighted in Fig. 2a, the V_{th} increases when cooling down. FBB can reduce the 4.2-K V_{th} even below its room-temperature value, although it is less effective for the PMOS due to its larger V_{th} shift [8]. The body-factor, $\eta = \partial V_{th}/\partial V_{bs}$ in Fig. 2b, only depends on V_{bs} and the doping level, but it is approximately independent of temperature. A similar invariance was found for longer devices ($L = 2\mu$m). This indicates that a relatively high room-temperature body-factor is a good predictor of the suitability of the proposed technique for a given technology. For longer devices, however, the thresholds remain higher (Fig. 1c) due to the reduced DIBL effect and the ratio between the bulk diode leakage and drain current will be larger. The transistor $|I_{ds}|$ leakage at 4.2 K is lower than room temperature (see Fig. 1b and c) due to the steeper SS even for full FBB $|V_{bs}| = V_{dd}$, i.e., the N-well (P-well) to V_{ss} (V_{dd}), while the maximum current at $V_{gs} = V_{dd}$ is always higher at 4.2 K thanks to the higher mobility (see Fig. 1a).

B. Pass Gates

Pass gates, i.e., switches consisting of a PMOS and an NMOS in parallel, are problematic at cryogenic temperatures, as they exhibit high resistance around mid-rail due to the steeper SS and higher V_{th} [10]. Fig. 1d shows that with FBB, the pass-gate resistance is returned to levels similar to 300 K, thus proving its restored functionality. At 4.2 K, the curves are shifted to the right compared to 300 K, confirming that the NMOS threshold is less affected by cooling than the PMOS.

C. Ring Oscillators

In cryogenic digital circuits, FBB brings the opportunity to significantly reduce the dynamic power by simultaneously reducing both the V_{th} and V_{dd}. In addition, the steep SS

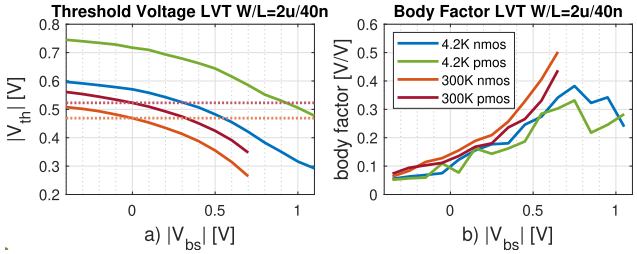

Fig. 2. (a) Threshold voltage at 4.2 K and 300 K of both an NMOS and PMOS LVT $W/L = 2\mu$m/40nm device at $|V_{ds}| = 50$ mV when applying body biasing. The dashed line indicates the 300-K threshold without body biasing. (b) The extracted body factor. At 300 K, $|V_{bs}|$ is limited to 0.7 V due to the bulk diodes turning on.

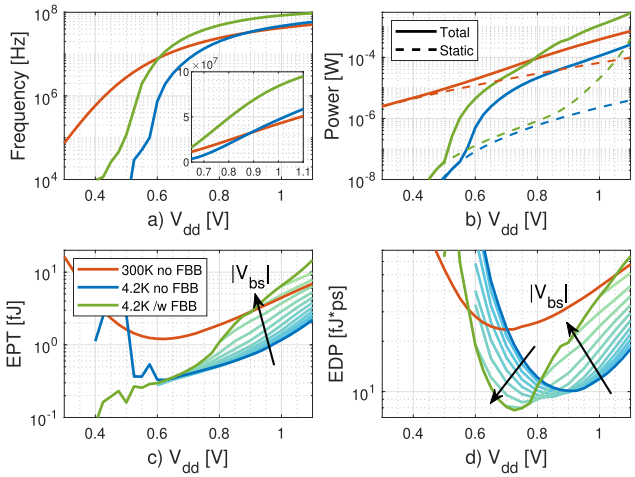

Fig. 3. Measured ring oscillator. (a) Frequency (inset in linear scale), (b) power, (c) energy per transition (EPT), (d) and energy-delay product (EDP). The RO consist of 1025 drive-1 LVT inverters and is measured at 300 K (red lines) and 4.2 K (blue to green lines). For 4.2 K, $|V_{bs}|$ increases from 0 V (blue) to V_{dd} (green) in steps of 0.1 V (shades).

at cryogenic temperature mitigates the leakage induced by this lower V_{th}. A second improvement is the logic speed-up induced by the increased mobility at cryogenic temperature compared to room temperature. While older technologies achieve $> 1.6\times$ speed-up when cooled down, the speed-up for modern technologies is limited by the increased V_{th} constraining the drive current [10]. FBB should alleviate this limitation, thus bringing back the traditional speed-up. The logic performance is assessed by characterizing a ring oscillator with standard drive-1 (D1) LVT inverters (Fig. 3). For these measurements, we focus mostly on full FBB ($|V_{bs}| = V_{dd}$)

TABLE I
A SUMMARY OF THE IMPORTANT QUANTITATIVE METRICS FOR THE RO

T	[K]	300	4.2	4.2	4.2	4.2
V_{dd}	[V]	1.1	1.1	0.9	1.1	0.725
FBB		No	No	No	Full	Full
f	[MHz]	50.8	58.7	34.0	95.0	32.2
P	[μW]	724	265	50.4	2844	34.2
EPT	[fJ]	6.95	2.20	0.723	14.6	0.518
EDP	[fJ · ps]	57.7	18.0	10.1	64.4	7.74

as this is a very practical case not requiring any additional biasing/supply voltage other than V_{dd} and V_{ss}. However, it is important to note that V_{dd} is now being swept. In Fig. 3a, the RO frequency shows a speed-up of 1.16× when cooling down, which increases to 1.87× when applying full FBB, thus aligning with the expectations based on [10]. The plot also clearly shows that FBB lowers the minimum V_{dd} at which the oscillator still works. Figure 3b shows two interesting findings for the power consumed by the ROs. First, a large reduction in static power is induced by the lower leakage at 4.2 K, which significantly increases with FBB. Second, the power consumption with FBB has a step-like increase above $V_{dd} = 0.8$ V. Since this also corresponds to an increase of the EPT and EDP (Fig. 3c,d), the power increases more than the frequency. This is likely due to the lower V_{th} causing an increase in the inverter short-circuit current when both NMOS and PMOS conduct. Next, Fig. 3c shows that the EPT does not benefit from FBB. This is expected as the EPT is limited by CV_{dd}^2 when neglecting the short-circuit current. FBB does however increase the frequency, causing the minimum EDP in Fig. 3d to lower from 10.1 fJ·ps without FBB to 7.7 fJ·ps with FBB. While this is similar to the results for 28-nm FD-SOI [11], the proposed technique avoids the back-bias voltages exceeding 4 V in prior works. An interesting difference appears in Fig. 3d above and below $V_{dd} = 0.9$ V when applying FBB. Above 0.9 V, FBB increases the EDP, while it lowers it below 0.9 V. This is mainly attributed to the optimal V_{dd} point shifting to lower V_{dd} for increasing FBB. A summary of the RO results mentioned above is shown in Table I.

D. Bulk Diode Leakage

Although FBB forces parasitic diodes in forward conduction (Fig. 4a,b), the diode built-in voltage $V_{bi} = E_g - k_B T/q \cdot \ln\left[(N_C N_V)/(N_A^- N_D^+)\right]$ increases well beyond 1.1 V due to the increase in the bandgap E_g and lower $k_B T/q$ at cryogenic temperatures [19]. This, in combination with the steeper Fermi function, which requires the applied voltage to be closer to V_{bi} before conduction starts, makes the leakage via the body terminals negligible at 4.2 K. To verify this, Fig. 4c,d show the combined bulk leakage of the 144 1025-stage on-chip ring oscillators for various FBB voltages at $V_{dd} = 1.1$ V. If the well-to-well leakage were dominant (white diodes in Fig. 4a,b), the N and P bulk currents should be similar. However, since the NMOS and PMOS body current shows a dominant exponential dependence on their respective body voltage, the leakage is mainly attributed to the source/drain-to-well diodes (black diodes in Fig. 4a,b). Interestingly, the leakage changes sign for FBB around mid-supply and shows dependence on the opposite FBB voltage. This may be due to the gate leakage being affected by the FBB-tuned threshold. Normalizing the bulk current at full FBB for

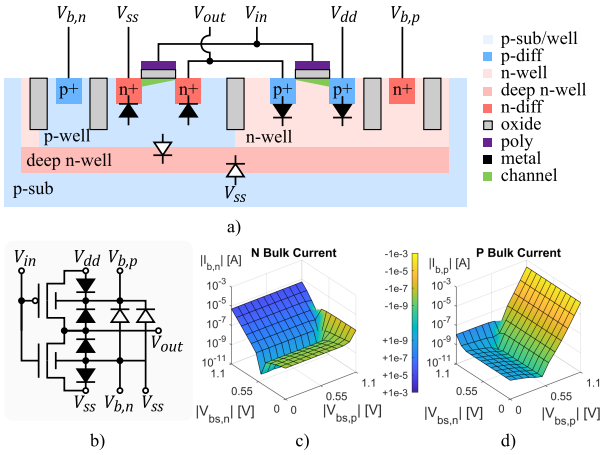

Fig. 4. (a) Simplified cross-section of a body-biased inverter in a triple-well process; the well-to-well diodes and drain/source-to-well diodes are drawn in white and black, respectively. (b) Inverter schematic. (c) NMOS and (d) PMOS body currents for all 144 ROs for $V_{dd} = 1.1$ V at 4.2K.

1.1 V supply to the total combined transistor widths results in 64.1 pA/μm (1.32 nA/μm) for NMOS (PMOS). This difference is ascribed to the difference in doping. Using those factors and the sizing of the D1 LVT RO and $V_{dd} = 1.1$V, results in a bulk leakage power of 632.6 nW at 1.1 V, which is negligible as it is almost 5000 times lower than the total power (2844 μW). Even for much lower dynamic power, e.g. lower activity factor or longer devices, the bulk leakage would be negligible. Still, it might be preferable to switch the body voltage for inactive circuits. Additionally, at a lower supply, leakage will further decrease due to the exponential dependence on the bias voltages.

E. Proposed Cryogenic Design Guidelines

Based on our results, we suggest adopting cryogenic-aware FBB to LVT devices from a bulk CMOS technology with sufficiently high room-temperature body-factor. For pass-gates and high-performance or low-power digital, we suggest applying full FBB. High-performance digital circuits should remain at nominal supply, however, lowering the supply in low-power digital circuits contributes to reducing the EDP. For the LVT D1 RO in our specific technology, this means that for low-power designs the supply should be lowered to 0.725 V with full FBB, yielding an EPT / EDP reduction of 4.24 × / 2.33×, while only reducing speed by 1.82× compared to $V_{dd} = 1.1$ V without FBB at 4.2 K. For high-performance designs, at $V_{dd} = 1.1$ V applying full FBB results in a frequency increase of 1.62× with an EDP comparable to 300 K. Here, the leakage increases mainly due to the short circuit current, the bulk leakage power is only 0.02% of the total power.

III. CONCLUSION

The presented experimental validation shows that FBB can be applied in bulk cryo-CMOS devices and circuits with negligible leakage, even with full FBB, i.e., the N-well (P-well) to V_{ss} (V_{dd}). The proposed cryogenic-aware FBB technique can compensate for the cryogenic V_{th} shift without requiring beyond-supply voltages, thus enabling the operation of circuit topologies otherwise unusable at cryogenic temperatures, such as pass gates. In digital circuits, applying FBB can increase the speed of high-performance circuits by 1.62× or reduce the EPT by 4.24× and the EDP by 2.32× for low-power circuits.

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