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An Element-Matched Band-Pass Delta-Sigma ADC for Ultrasound Imaging

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***Abstract*—This work presents a compact ADC architecture capable of digitizing the signals received by every individual element of a 2D ultrasound transducer array. An element-matched layout of 150 μm $\times$ 150 μm is realized by exploiting each piezo-electric transducer element not only as the signal source, but also as the electro-mechanical loop-filter of a continuous-time band-pass $\Delta\Sigma$ ADC, thus minimizing the required circuit blocks. The transducer's frequency response, which is inherently matched with the signal bandwidth of interest, provides noise shaping to the ADC. A prototype chip has been fabricated in a 0.18 μm CMOS technology, featuring 20 ADCs located directly underneath a 150 μm-pitch piezo-electric transducer array fabricated on top of the chip. Each ADC, clocked at 200 MHz, consumes 800 μW from a 1.8 V supply, and achieves an SNR of 47 dB in a 75% bandwidth around a center frequency of 5 MHz. Acoustic measurements show that the ADC successfully digitizes incoming echo signals.**

Keywords: Band-pass ADC, Electro-mechanical Resonator, Tracking Quantizer, Inverter-based OTA.

I. Introduction

Heart-related diseases are the most common cause of death. Echocardiography, i.e. the use of ultrasound to image the heart, is a safe and affordable imaging technique that is crucial for the effective diagnosis and treatment of heart-related diseases. This work focuses on the realization of miniature ultrasound probes that are capable of making real-time three-dimensional (3D) images of the heart. In particular, we focus on endoscope-based probes for trans-esophageal echocardiography (TEE), which are used to make high-quality cardiac images from the patient's esophagus.

In order to obtain real-time 3D images, a 2D array of transducer elements is needed, leading to a total of 1000+ elements, of which the echo signals have to be processed. In conventional (2D) ultrasound probes, the elements are connected individually to an imaging system. The number of cables that would be needed in a 3D probe, however, exceeds by far what can be accommodated by an endoscope, calling for the use of in-probe integrated circuits. Prior work focuses on analog approaches to reduce the number of cables, such as analog sub-array beamforming [1] [2]. In this work, we report an element-level ADC architecture that enables the digitization of all received signals. Thus, digital beamforming, compression and multiplexing techniques can employed to reduce the number of cables, paving the way towards miniature ultrasound probes with a fully-digital interface.

The proposed design exploits the filtering properties of the ultrasound transducer to reduce the hardware needed for the digitization of the acoustic signal. In particular, the band-pass characteristic of the transducer is used as the noise shaping element of a Continuous-Time Band-Pass $\Delta\Sigma$ Modulator. This paper demonstrates this concept for the first time for ultrasound applications, and shows that it enables the integration of an entire oversampled ADC underneath a 150 μm $\times$ 150 μm transducer element even in a standard 0.18 μm CMOS technology, allowing massively-parallel digitization of all received signals in a 2D transducer array. This size is substantially smaller than a recently-reported element-matched $\Delta\Sigma$ ADC, which employs a conventional electrical loop-filter and was implemented in 28 nm CMOS [3].

II. Transducer Impedance Characteristics

In this work, bulk PZT piezo-electric transducer elements are employed, with a pitch of 150 μm. These transducers are integrated directly on top of the proposed application-specific integrated circuit (ASIC) using the procedure described in [1], in which one electrode of each element connects to a bond-pad of the ASIC, while the other electrode is grounded using a thin conductive layer that covers the whole array.

The electrical impedance of a transducer element, measured with an impedance analyzer, is shown in Fig. 1. The plot shows a largely capacitive behavior, with a resonance around 5 MHz due to the mechanical thickness-mode resonance of the transducer. This behavior can be captured well by an equivalent Butterworth-Van Dyke circuit model, shown in the inset of Fig. 1, in which a motional branch, consisting of R, L and C, accounts for the mechanical resonance, and a parallel capacitor C_S models the capacitance between the transducer's electrodes. The transducer impedance can be expressed as $Z(s) = \frac{LCs^2+RCs+1}{sC_S(LCs^2+RCs+1+\frac{C}{C_S})}$, which shows the capacitive baseline, the resonance in the numerator and the anti-resonance in the denominator. The target of this work is to exploit the resonance in the loop filter of a $\Delta\Sigma$ ADC.

The resistance R directly impacts two extremely important aspects: the intrinsic thermal noise added by the transducer and the quality factor of the resonance. The first yields the required thermal noise performance of the ADC's input stage, and the second, defined as $Q = \frac{\omega_0 L}{R} = \frac{\omega_0}{Bandwidth}$, determines the intrinsic bandwidth of the system.

III. System-Level Design

A. Working Principle

The quantization noise should be suppressed by the modulator around the center frequency. Since the resonance modeled

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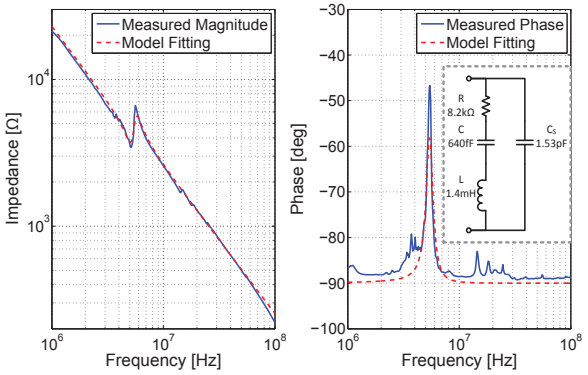

Fig. 1. Impedance of the employed PZT element (magnitude and phase).

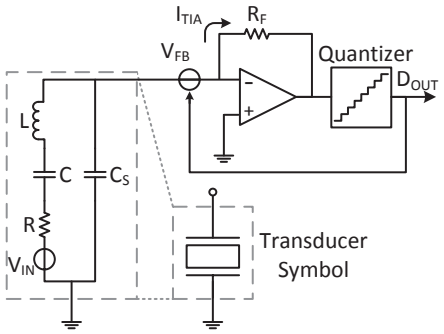

Fig. 2. Explanation of the working principle behind the element-level ΔΣ ADC.

by the RLC branch provides a corresponding band-pass characteristic, this is chosen as the noise-shaping element of the modulator. The signal source within the transducer model is represented by an ideal voltage source V_{IN} in series with R, approximately ranging between 50 μV and 250 mV. Ideally, the summing node of the modulator should be realized at that same location, but that node in the equivalent circuit does not have a physical counterpart. Therefore, voltage feedback (V_{FB}) is applied to the available electrode of the transducer, while the resulting current is read out using a transimpedance amplifier (TIA), as shown in Fig. 2. The TIA's output is then digitized by a quantizer that controls the feedback voltage and thus closes the loop of the modulator. The current sensed by the TIA can be expressed as:

$$I_{TIA} = (V_{IN} - V_{FB})\frac{sC}{LCs^2 + RCs + 1} - V_{FB}sC_S \quad (1)$$

The first part of this equation shows the desired noise shaping behavior, but the second part, due to C_S, adds to the output a differentiated version of V_{FB}, which is undesirable. Moreover, the required floating voltage-feedback DAC is difficult to implement. Fig. 3a shows how these problems can be mitigated. First, the floating DAC is replaced by feedback to the non-inverting input of the TIA, causing the TIA's virtual ground to follow this voltage, thus effectively applying voltage feedback to the transducer. Second, an additional voltage DAC V_{FB2} and a capacitor C_{comp} compensate for the last term in (1), by providing a current $V_{FB2}sC_{comp}$ that cancels out the undesired current $V_{FB}sC_S$ coming from the transducer. A further refinement is shown in Fig. 3b, where the two feedback voltages are merged into one, and the feedback to the non-inverting input is replaced by a capacitive divider, leading to a bridge-type configuration in which the bottom capacitor C_C is made tunable and should be as close to C_S as possible for a perfect compensation.

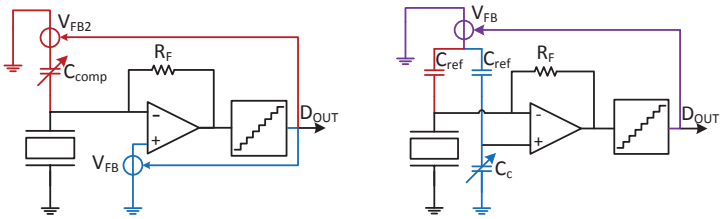

Fig. 3. ADC block diagram with (a) a compensation capacitor and (b) a capacitive bridge configuration to compensate for the effect of C_S

B. Complete Element-Level Architecture

The complete element-level ADC architecture is shown in Fig. 4. Here, V_{FB} is replaced by a bank of inverters, supplied by two reference voltages V_{REF+} and V_{REF-}, each driving a pair of feedback capacitors. A programmable resistor R_C (Full scale = 1.5 kΩ, LSB = 100 Ω) was added in series with C_C (Full scale = 3.2 pF, LSB = 50 fF) in order to compensate for the transducer's high-frequency behavior [4]. C_F, added in parallel with R_F, provides the loop filter with a dominant pole and helps to attenuate the effect of an imperfect compensation of C_S. Finally, a second stage is introduced to amplify the output of the TIA and thus relax the noise requirements of the quantizer.

Due to the propagation attenuation of the acoustic echo signals, the ADC has to be able to handle a relatively large input dynamic range: the nearest tissue produces high-amplitude echoes that reach the transducer elements sooner, while farther tissue generates weak echoes that will take a longer time to be caught by the transducers. To compensate for this, so-called time-gain compensation (TGC) is implemented by varying the reference voltages as a function of time, implemented using off-chip DACs, which could be integrated on-chip in a re-design. This ensures that the feedback voltage is always comparable with the input signal. In addition, the second-stage gain is programmable by two bits (decoded into four states) so as to maintain loop stability and to keep the voltage swing at the input of the quantizer approximately constant. The second stage gains are 9 dB, 16 dB, 24 dB and 33 dB. The second stage also introduces an additional pole, which, together with that of the first stage, helps to attenuate the first-stage noise. Both the g_m stages are implemented using current-reuse differential-to-single-ended operational transconductance amplifiers (OTA) [5], to improve the ADC's current efficiency. An element-level constant-g_m biasing block provides bias currents to the g_m stages.

A 3-bit quantizer is used in order to reach the desired SQNR requirements without having to increase the over-

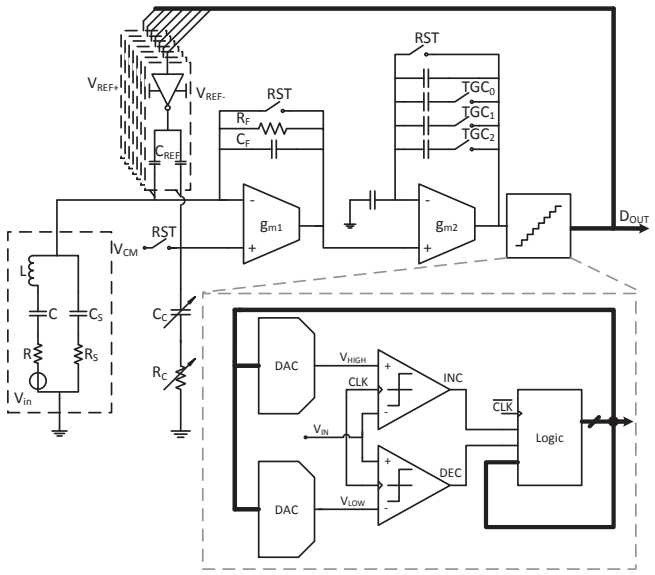

Fig. 4. Implemented ADC architecture.

sampling ratio (OSR) and therefore the sampling frequency excessively. This quantizer, clocked at 200 MHz, employs a tracking architecture [6], depicted in the inset of Fig. 4. Two comparators compare the quantizer's input voltage with reference levels V_{HIGH} and V_{LOW}, generated by two 3-bit capacitive DACs based on the quantizer's previous output. The outputs of these comparators then determine whether the quantizer's output should be incremented, decremented, or kept as-is. While this type of quantizer is unable to track fast changing inputs, system simulations show that this is not an issue in this design, because the signal that reaches the quantizer has already been limited in bandwidth by the poles added by the two stages. This type of quantizer provides a good compromise among speed, power and die area. It also allows the ADC's output to be encoded in a 2-bit format, thus reducing the data rate compared to a full 3-bit output.

IV. Chip-Level Design

A prototype with a transducer array of 5×4 elements has been realized, each of which is interfaced with a copy of the element-matched $\Delta\Sigma$ ADC described above. Every ADC produces two 200 MHz output bitstreams, coming from the tracking quantizer comparators, which are exported to an off-chip FPGA via on-chip LVDS transmitters. To reduce the chip's I/O count to a manageable number, a total of 20 LVDS transmitters and a 2:1 channel multiplexer are implemented, allowing 10 out of the 20 ADCs to be read out simultaneously. For flexibility, software-based decimation filters are employed; in a re-design, these filters could be implemented in each element or in the chip periphery. A micrograph of the chip, fabricated using TSMC 0.18 μm technology, is shown in Fig. 5, together with the layout of the 150 μm $\times$ 150 μm element-matched ADC. The inset in Fig. 5 shows the prototype chip mounted on a PCB substrate with a piezo-electric transducer array built on top using the process described in [1], before applying the top ground layer, so that the individual elements can be seen.

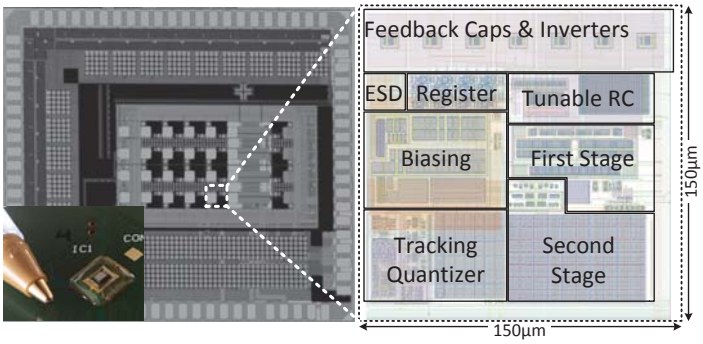

Fig. 5. Chip micrograph, element layout and photo of the prototype array built on top.

V. Measurement Results

Fig. 6 shows the measured ADC output spectrum, with a full-scale acoustic continuous-wave input generated by an unfocused 5 MHz transmitter positioned above the chip (see Fig. 6). The desired noise shaping behavior can be clearly observed: the quantization noise is lowest in the bandwidth of interest, highlighted in green. The measured SNR is 45 dB, 47 dB, 45 dB and 41 dB for the four TGC steps (i.e. gain settings of the second stage). The lower SNR in the last TGC step is likely due to noise coming from the off-chip reference voltages V_{REF+} and V_{REF-}. Digital beamforming (on- or off-chip) could be employed in a re-design to improve the effective SNR of the image.

In order to verify that the ADC output is a good approximation of the actual signal received by the transducer, the response of the ADC to an acoustic pulse has been compared in Fig. 7 to the same element's TIA output, with the ADC feedback disabled. In the latter case, the TIA provides an amplified version of the transducer's output current. The two responses are in good agreement.

Tab. I compares this work with recently published ultrasound ADCs. As this design uses the ultrasound transducer as the loop filter for a $BP\Delta\Sigma$ converter, the area typically reserved for the reactive components in standard loop filters is saved. This allows the designed converter to be very competitive in terms of area. Furthermore, the power consumption is an order of magnitude lower than the state of the art, even if it achieves a worse SNR.

Fig. 8a compares this work with $\Delta\Sigma$ ADCs in general, as reported in [7]. The x-axis represents the area, while on the y-axis, the Walden figure of merit (FOM) is shown, defined as: $FOM_W = \frac{Power}{\frac{f_s}{OSR} 2^{\frac{SNR-1.76}{6.02}}}$ This work achieves by far the smallest area compared to designs using a similar technology. Furthermore, only two of the converters employing a smaller feature size obtain a smaller area. The Walden FOM, while being more than one decade above the state of the art, can still be considered as a competitive result, since the proposed design is not just an ADC, but also includes a TIA and a programmable-gain amplifier (PGA). Finally, Fig. 8b shows a direct comparison between area and power consumption, for ADCs with similar SNR and bandwidth, using any technology node. This work features the smallest area, as well as the lowest power consumption among these designs.

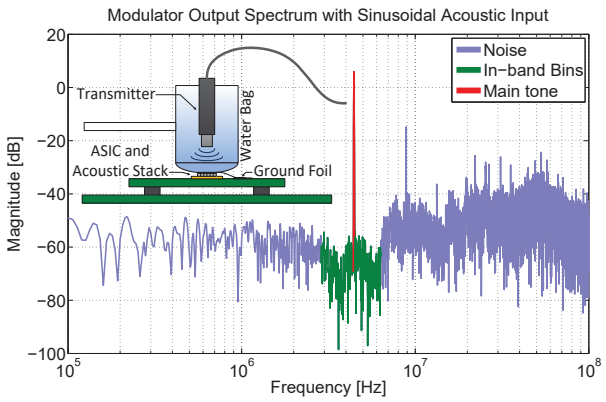

Fig. 6. FFT of the ADC's measured bitstream. The center frequency is slightly shifted because of the uncertainties linked to transducer fabrication

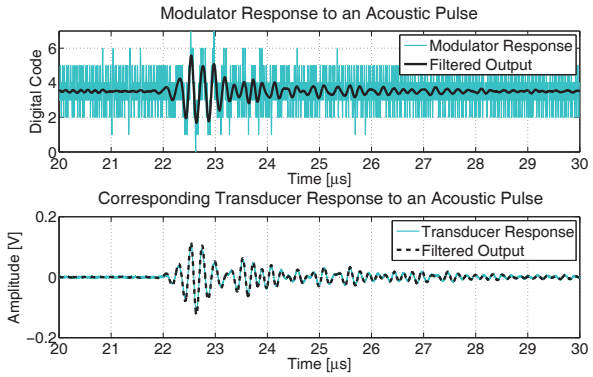

Fig. 7. Time-domain response of the ADC to an acoustic pulse compared with that of the transducer. Measured in water at a distance of 2 cm

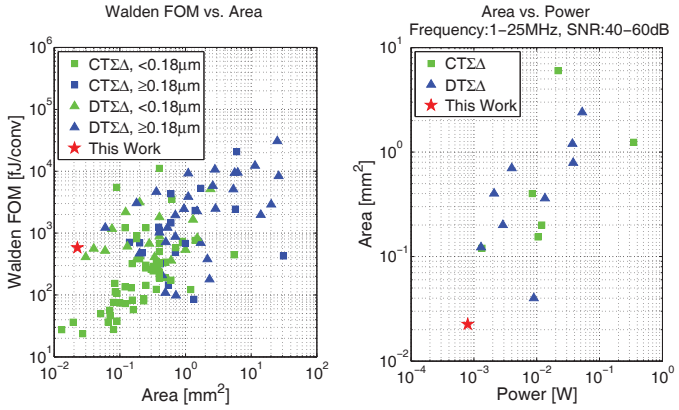

Fig. 8. Comparison of this work's FOM and Power vs. active area with designs published at ISSCC and VLSI [7]

VI. Conclusion

This work demonstrates that a piezo-electric ultrasound transducer can serve as the electro-mechanical loop filter of a $\Delta\Sigma$ ADC, thus inherently reducing complexity, area and power consumption compared to an implementation using a conventional electrical loop filter. We expect that this concept is not limited to the bulk PZT piezo-electric transducers employed in our work, but can be extended to micro-machined transducers, such as capacitive micro-machined ultrasound transducers (CMUTs). An attractive feature of the presented ADC architecture is that it does not introduce much additional circuitry compared to a traditional analog front-end (AFE), which also tends to employ a TIA and a programmable-gain stage. The only extra circuits needed for element-level digitization are the tunable RC branch, the feedback DACs and the tracking quantizer. These circuits occupy only 37% of the area and consume roughly 50% of the power. The acoustic results obtained with our prototype show that the ADC successfully digitizes acoustic echo signals, demonstrating the effectiveness of the presented architecture and making it a promising approach for in-probe digitization in future high-element-count 3D ultrasound probes.

TABLE I. Comparison of this work with similar publications

	This Work	[3]	[8]	[9]	[10]
Transducer Type	PZT	CMUT	N/A	N/A	N/A
Architecture	CTBPDS	DTLPDS	SAR	CTBPDS	CTLPDS
Technology [nm]	180	28	130	65	65
No. of Channels	20	16	64	8	1
Elem. Matched [µm]	Yes (150)	Yes (250)	No	No	No
Center Freq. [MHz]	5	5	5	260	4
Bandwidth [MHz]	3.125-6.875	10	8	20	15
Area/Channel [mm^2]	0.025	0.0625	0.1	0.03	0.4
Power/Channel [mW]	0.8	17.5	6.32	13.1	6.96
SNR/Channel [dB]	47	60	48.5	54	74.6

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