MSc Thesis

Time-to-Digital Converter (TDC) for WiMAX ADPLL in State-of-The-Art 40-nm CMOS

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The undersigned hereby certify that they have read and recommend to the Faculty of Electrical Engineering, Mathematics and Computer Science for acceptance a thesis entitled **"Time-to-Digital Converter (TDC) for WiMAX ADPLL in State-of-The-Art 40-nm CMOS"** by **Popong Effendrik** in partial fulfillment of the requirements for the degree of **Master of Science**.

Dated: *April 18, 2011*

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Abstract

WiMAX (Worldwide Interoperability for Microwave Access) is the emerging wireless technology standard of the near future, which enables high speed packet data access. To anticipate the future demands on WiMAX technology, we proposed an ADPLL (all-digital phase locked loop) solution for the WiMAX system. The developed ADPLL system has targeted frequencies from 2.3 GHz to 2.7 GHz and from 3.3 GHz to 3.8 GHz for low band and high band, respectively. In this approach, an ADPLL replaces the conventional RF synthesizer based on charge-pump architecture. There are three main components of the ADPLL system. One of them is the time-to-digital converter (TDC) system.

A TDC in state-of-the-art 40 nm CMOS technology for WiMAX ADPLL system is chosen and presented in this thesis. The TDC architecture is based on a pseudo-differential structure. This architecture utilizes an inverter as a delay element and a sense amplifier flip-flop as a time comparator. In comparison, the two other TDC architectures evaluated in this thesis (two-dimensional Vernier algorithm TDC and time-windowed TDC) have very complex architectures and complex calibration methods, while the chosen TDC architecture has a simple calibration method. Moreover, this pseudo-differential TDC can meet the time resolution required by the WiMAX ADPLL system.

The TDC system has been tested on a 1.2 V power supply, 33.868 MHz frequency reference clock FREF and with 4.25 GHz frequency of CKV. It is found that the power consumption is about 2.99 mW without a clock gating scheme. Moreover, it is expected that the power consumption can be reduced to 0.78 mW with a clock gating scheme. The INL and DNL of the TDC are lower than 0.4 LSB. The measured TDC resolution is around 10.84 ps - 12.55 ps. In the worst case condition, the TDC resolution of 12.55 ps will give an in-band phase noise better than the limit, which is -95 dBc/Hz as required by the WiMAX ADPLL System. The TDC core layout has an area of only 125×11 μm^2.

Acknowledgement

The final year of my MSc studies has been a special time, mixed with anxiousness, depression and enjoyment. It would have been hard for me to reach this stage without the support of others.

First and foremost I would like to express my sincere thanks and appreciation to my MSc thesis supervisor, Dr. Robert Bogdan Staszewski. It has been an honor to be his first MSc student to work on the ADPLL project. He has taught me from the scratch about ADPLL and TDC design. Once again, thank you for your patience and understanding. I will always remember it.

Special thanks go to Ir. Frank Verwaal and Ir. Marcel van de Gevel for allowing me to explore the experiment and for their daily supervision during my thesis work at Catena Microelectronics B.V, Delft, The Netherlands. I also want to thank Koen van Hartingsveldt, Ivaylo Bakalski, Aylin Donmez, Federico Bruccoleri, Bert Oude Essink, Iqbal Suhaib and Gerard Lassche for their fruitful discussions. I am especially grateful to Krass Maklev, Kave Kianush and Rien Geurtsen of Catena Microelectronics B.V for their generous support and great assistance during my internship.

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Chapter 1

Introduction

1-1 Motivation

1-1-1 Moving From Voltage Domain to Time Domain

The analog signal is the most common signal in the real world, which is a physical signal that human beings can sense. This signal has a continuous-time and continuous-amplitude value. Alternatively, the digital signal has a discrete-time and discrete-amplitude value, which is the value that digital computers can process.

The two main components used for connecting between the analog domain and digital domain are ADC (Analog to Digital Converter) and DAC (Digital to Analog Converter). An ADC will convert an analog signal to digital information while the core of the data processing unit is a DSP (Digital Signal Processing) processor for calculating the digital data to obtain the desired results. The result of a DSP processor will then be converted back to analog domain by DAC.

As shown in Figure 1-1, an ADC is the component that converts the information from an analog value to a digital value. There are two steps should be conducted, usually by an ADC, when performing its task. The first step is a sampling process, which is the discretization in the time domain. This sampling process is realized by a sample and holds circuit and results in a sampled-data signal. The second step is a quantization process, which is the discretization in the amplitude domain. This quantization process is normally done by comparators. Once the quantization process is done, the sampled-data signal is converted to digital domain. However, usually the sampling process and the quantization process will be carried out at the same time.

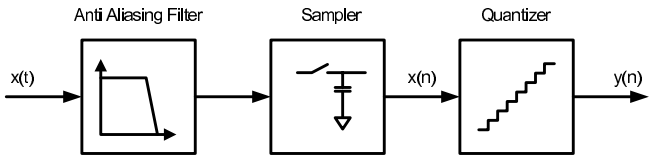

Figure 1-1: ADC block diagram. [39]

The general function of an N-bit analog to digital conversion can be described:

$$V_{in} = \sum_{i=1}^{N} b_i \cdot 2^{-i} \cdot V_{ref} + e_q \tag{1-1}$$

In general, for every ADC they are likely to have a sampler and a quantizer. However, in flash ADC architectures, the sampling and quantization process will be done simultaneously and no dedicated sampling or hold circuit are required. There are three major components of a flash ADC, i.e. voltage reference (string of resistors), comparators and decoder, as shown in Figure 1-2

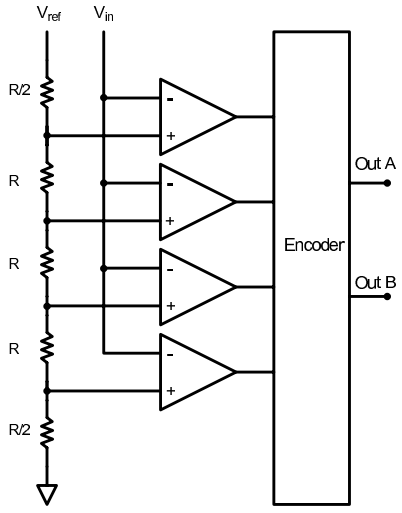

Figure 1-2: A flash ADC.

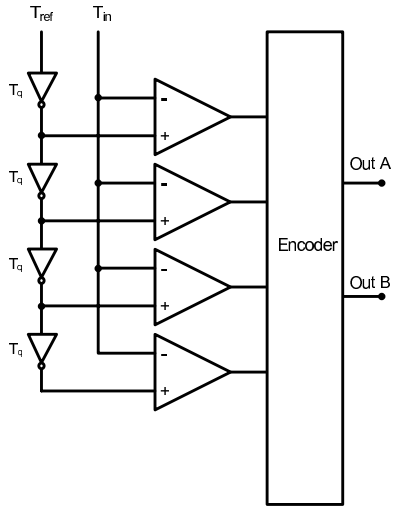

Figure 1-3: A TDC system.

In order to achieve a high signal-to-noise ratio, the old technologies take advantage of a large supply voltage (5 V, 3.3 V and 2.5 V). In a deep-submicron process, which has a low supply voltage (at or below 1.5 V), the available voltage headroom is quite small; therefore a signal representation in the time domain will be more interesting. Regarding this time domain resolution, a new paradigm has been presented below.

> In a deep-submicron CMOS process, the time-domain resolution of a digital signal edge transition is superior to the voltage resolution of an analog signal [Robert Bogdan Staszewski] [1, 2].

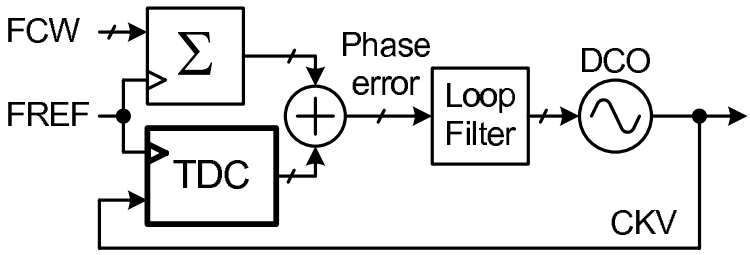

Figure 1-4: All-digital PLL.

1-1-2 All-Digital PLL (ADPLL)

Recently, new techniques have been developed based on that paradigm in transforming the RF and analog part to the digital domain in a wireless RF application as presented in [1]. In these new techniques an ADPLL replaces the conventional RF synthesizer architecture, based on a voltage-controlled oscillator and a phase frequency detector and charge-pump combination, with a digitally controlled oscillator (DCO) and a time-to-digital converter (TDC) [1].

The time information of a signal can be detected by a system, which is called a TDC system. TDC is similar to ADC, but while ADC converts an analog signal in terms of amplitude domain or amplitude information, TDC converts in terms of time domain or time information. Similar to a Flash ADC, a TDC has 3 major components, i.e. delay element, comparator and decoder as illustrated in Figure 1-3.

Figure 1-5 [3] shows the basic operating principles of a TDC (time-to-digital converter). The time interval of the input, $T_{in} = T_{stop} - T_{start}$, will be divided into a number of smaller time intervals or into a time reference T_q plus there is an error of e_q at the beginning and end of the measurement, which is indicated by ΔT_{start} and ΔT_{stop}, respectively. In this design, our TDC has no T_{start} and T_{stop}, however, it has the same operating principles.

$$e_q = \Delta T_{stop} - \Delta T_{start} \tag{1-2}$$

$$T_{in} = \sum_{i=1}^{N} b_i \cdot 2^{-i} \cdot T_q + e_q \tag{1-3}$$

Equations 1-1 and 1-3 are similar, in this thesis the TDC designed will be analyzed with similar methods to those used for examining ADC.

1-1-3 ADPLL Performance

A frequency synthesizer is a circuit that generates one or several frequencies from a reference frequency. Its performance can be measured in terms of frequency purity (phase noise, spurious tone), frequency resolution, frequency tuning range and lock time.

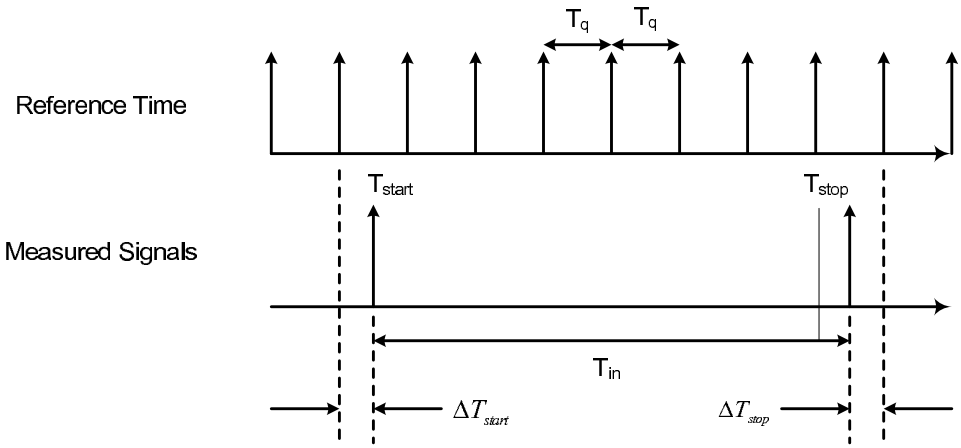

Figure 1-5: Time-to-digital converter operating principle [3].

The TDC performance has an influence on the ADPLL system. The resolution of TDC will contribute to the in-band phase noise of ADPLL. As described in [1], the in-band phase noise of an ADPLL system is:

$$\mathcal{L} = \frac{(2\pi)^2}{12}\left(\frac{\Delta t_{res}}{T_V}\right)^2 \frac{1}{f_R} \tag{1-4}$$

This demonstrates that with lower resolution, the performance of the ADPLL in terms of its in-band phase noise is improved. However, the in-band phase noise requirement of the specified system will determine the resolution of the TDC. The ADPLL for the WIMAX system in this project requires 13 ps of TDC resolution to achieve an in-band phase noise of -95 dBc/Hz.

1-2 Related Works

The first ADPLL system designed took advantage of the capabilities of an inverter as the basic component in its TDC system [4, 5]. TDC architecture of its TDC core is a pseudo-differential architecture that is insensitive to nMOS and pMOS transistor mismatches. This work results in a TDC with a resolution of 20 ps. This resolution is good enough for wireless standards application [6].

To improve TDC performance there are many reports that can be referred to. Tokairin et al. of NEC Semiconductor in [7] designed an ADPLL in 90-nm CMOS technology with time-windowed TDC. This TDC uses a two-step structure with an inverter and a Vernier-delay time to improve the time resolution. The resolution achieved is 5 ps. Moreover, it has a single-shot pulse-based operation that is used for low power consumption and it connects the DCO (digitally control oscillator) clock frequency to the data port of the flip-flop instead of the inverter chain, which will significantly reduce the power .

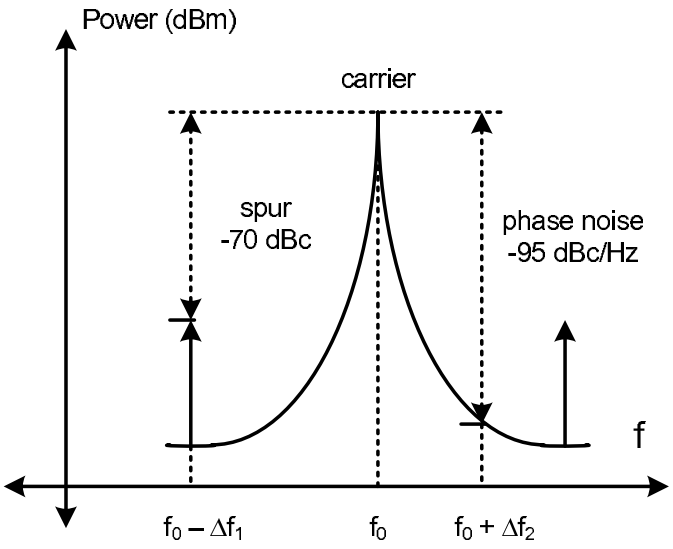

Figure 1-6: Output spectrum of practical oscillators.

Another paper published by Pavia University [8] presents a digital approach in developing PLL with a two-dimensional Vernier algorithm applied to a TDC. It was realized in 65-nm CMOS technology with a time resolution TDC of 4.8 ps. In addition, this architecture needs a calibration process during its operation by using an IIR filter circuit, so a very complex system is presented in that paper.

1-3 Main Contributions of the Thesis

This thesis has the following contributions:

- Characterize the state-of-the-art 40-nm CMOS Technology processes related to TDC design.
- To design a TDC of an ADPLL system for a WIMAX System to achieve the required in-band phase-noise of -95 dBc/Hz with a resolution of 13 ps.
- Build a low cost and a low power TDC system by taking advantage of current digital CMOS performance.
- Detail analysis of TDC as one of the major contributors to ADPLL system performance is presented when building the WiMAX system.
- The speed of the device is adequate for this new technology, while the parasitic capacitances are more dominant, a study of parasitic effects and other physical phenomena

of this new technology, such as WPE (Well Proximity Effects), on the device will be investigated in order to achieve 13 ps resolution.

1-4 Organization of the Thesis

The thesis will be organized as follows.

- Chapter I shows the motivation behind this thesis work, related work, main contributions and organization of the thesis.
- Chapter II evaluates the new technology that is currently being used in this thesis, which is the 40-nm CMOS process.
- Chapter III will introduce the WiMAX ADPLL system and TDC performance that relates to the WiMAX's requirements and it will also evaluate the current state-of-the-art TDC architectures.
- Chapter IV discusses the building blocks of the developed TDC, which includes a time reference and a time comparator, or flip-flop, and its operating principles related to TDC performance.
- Chapter V shows the TDC layout design, simulation, and its performance.
- Chapter VI concludes the thesis and identifies future work.

Chapter 2

The State-of-The-Art 40-nm CMOS New Technology Assessment

2-1 CMOS Technology Scaling

The only constant in the semiconductor industry is constant change. Transistors become smaller and dissipate less power. They have fast switching characteristics and are also cheaper. The Semiconductor Industry Association (SIA) maintains an International Technology Roadmap for Semiconductors (ITRS) predicting future scaling. It identifies that scaling in technology will double the density of digital logic every 2-3 years. Digital circuits have benefits from this scaling process through increased speed and lower power consumption. Moreover, this technology scaling significantly lowers the cost of digital logic systems.

Current research in All-Digital PLL (ADPLL) [1] has shown the advantages of this technology scaling. The TDC system is the main component of ADPLL that really takes advantage of this scaling. The TDC system requires fast delay to achieve a low in-band phase noise. It is expected that with this new technology the device will be faster than before. Technology that is currently being used in this thesis is a 40-nm CMOS process. Cadence Spectre is used for simulation purposes, and the model being used in this simulation tool is BSIM 4.5 [9].

2-2 The 40-nm Technology Overview

In this technology, Shallow Trench Isolation (STI) is used for active isolation to reduce the active pitch. This technology also provides an option for the Deep N-Well (DNW) for isolating the P-Well from the substrate. Furthermore, this PDK provides 3 types of

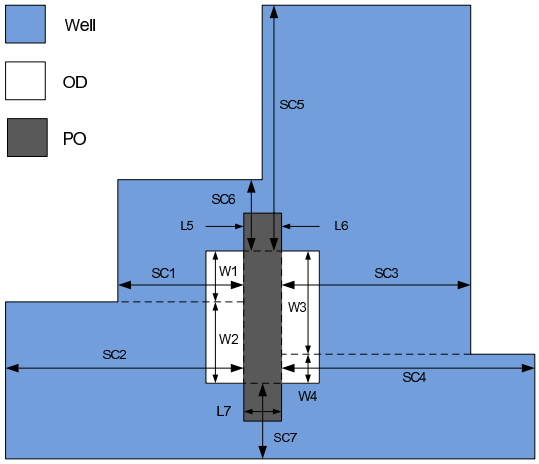

Figure 2-1: Well proximity effects (WPE).

devices with different threshold voltages (V_{TH}). Low V_{TH}, standard V_{TH} and high V_{TH} are provided to the customer for specific applications. In relation to the TDC design, low (V_{TH}) will give a finer resolution of delay, which is better. However, fabrication cost issues should be considered when choosing the type of device.

Regarding the threshold voltage (V_{TH}), WPE (well proximity effects) can alter the threshold voltage of such devices. The WPE model is developed by CMC (Compact Model Council). In [9], it is observed that a threshold voltage can shift up to 100 mV. The BSIM 4.5 model considers not only the influence of WPE on the threshold voltage, but also on mobility and body effects.

Experimental analysis in [9] shows that the well proximity effect is a very strong function of distance of the MOSFET device from the mask edge. SC is the distance between the gate to the well edge as shown in Figure 2-1 and it will affect the threshold voltage (V_{TH}) value. The complete equation solution for WPE related to threshold voltage is complicated enough, and it is not possible to evaluate with hand calculations, therefore experiments must be conducted to ensure optimum value. Subsequently, qualitative results will be available rather than quantitative.

The state-of-the-art 40-nm CMOS process technology is currently used in this design. Basically, the 40-nm CMOS process has 10 metal layers as depicted in Figure 2-2. However, for this PDK, it only has 7 metal layers, which are 4 Mx layers, 1 Mz layer and 1 MURF layer for first inter-layer metal, top-metal, pitch 0.8 μm and top-metal, pitch 1 μm, respectively.

Figure 2-3 shows an interconnect line-to-line, which will result in parasitic capacitances. In this 40 nm PDK, the interconnect line-to-line capacitance is simulated using the TMA Raphael (V2004.06) program on two different structures, as in Figure 2-3. However, the actual interconnect structures on Si are more complicated than this structure. Therefore, once again, qualitative results will be provided instead of quantitative values. This capacitance will significantly affect the performance of the system, which should be taken into account during the design process.

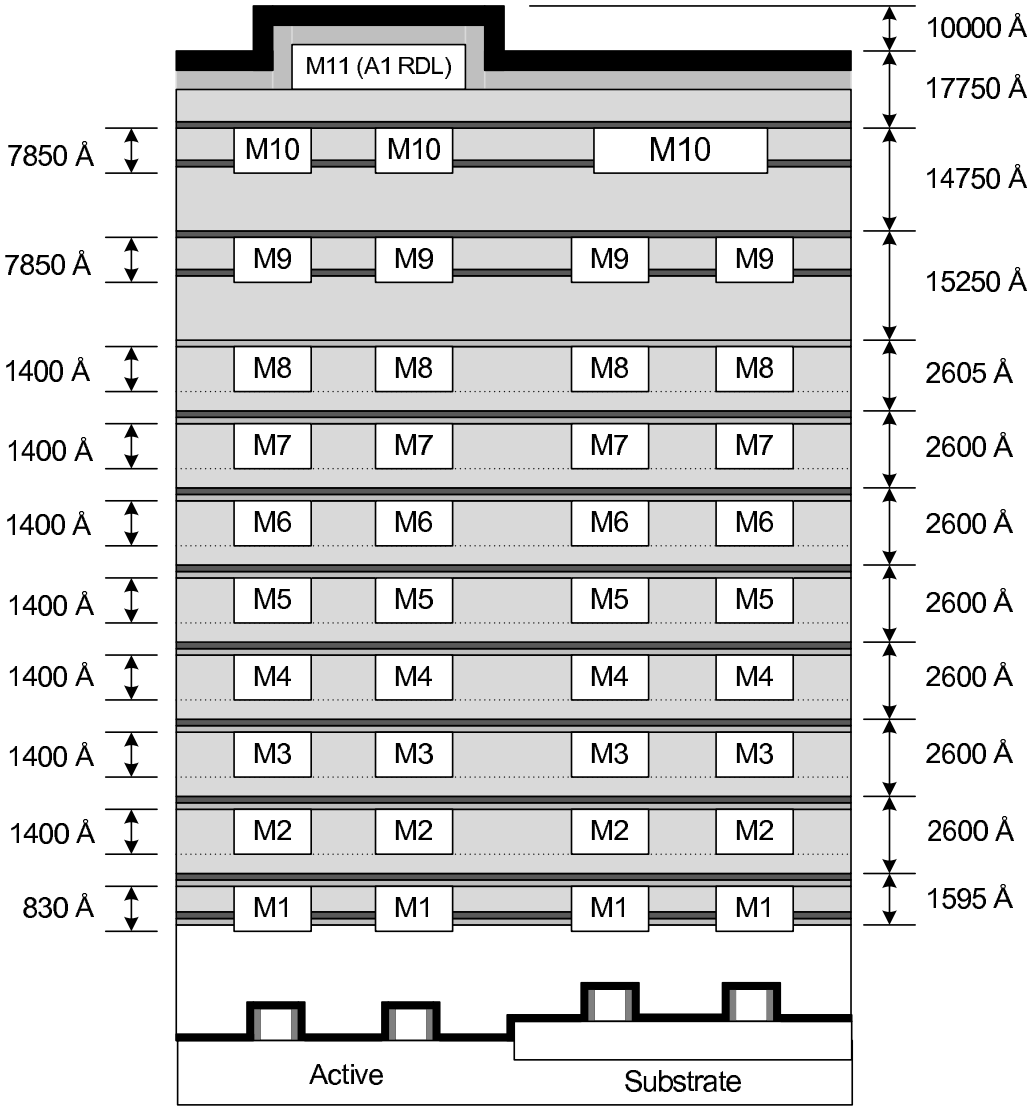

Figure 2-2: Cross section of the metal layers of the 40-nm CMOS process.

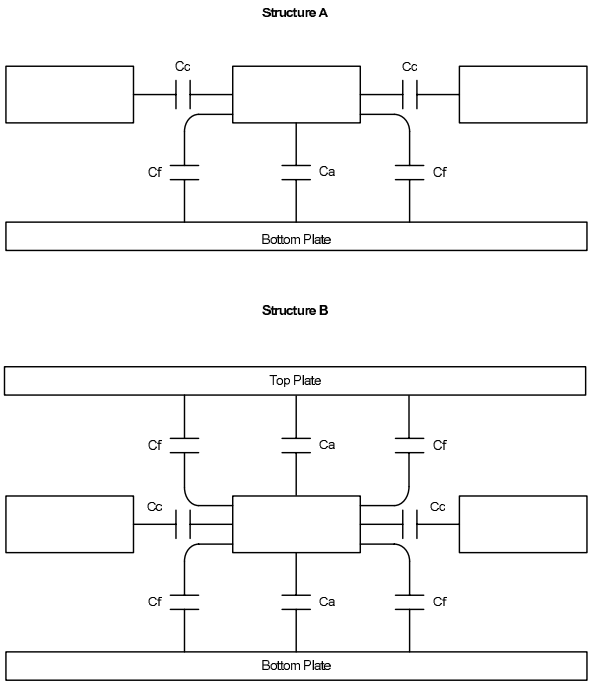

Figure 2-3: Interconnect line-to-line capacitance.

2-3 Inverter Delay

An inverter is the basic component of a digital logic circuit. A CMOS inverter is built using a NMOS and PMOS pair that share a common gate and a common drain at the input and output, respectively. Figure 2-4 shows a basic circuit for an inverter.

An inverter is the fastest logic-level regenerative timing method in CMOS technology. With this characteristic it is used as a delay element or a time reference in the TDC system. The speed of this inverter is measured by its propagation delay time (t_{pd}). The t_{pd} is measured as the average time needed for the output signal to respond to the input signal, as Equation 2-1. t_{PHL} and t_{PLH} are the propagation delays for a high-to-low and a low-to-high transition, respectively, as stated in Equation 2-2 and Equation 2-3 [10].

$$t_{pd} = \frac{(t_{PHL} + t_{PLH})}{2} \tag{2-1}$$

$$t_{PHL} = \frac{C_L \cdot V_{DD}}{K_n \cdot (V_{DD} - V_{TN})^{\alpha}} \tag{2-2}$$

$$t_{PLH} = \frac{C_L \cdot V_{DD}}{K_p \cdot (V_{DD} - V_{TP})^{\alpha}} \tag{2-3}$$

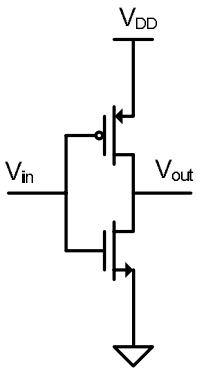

Figure 2-4: CMOS inverter circuit.

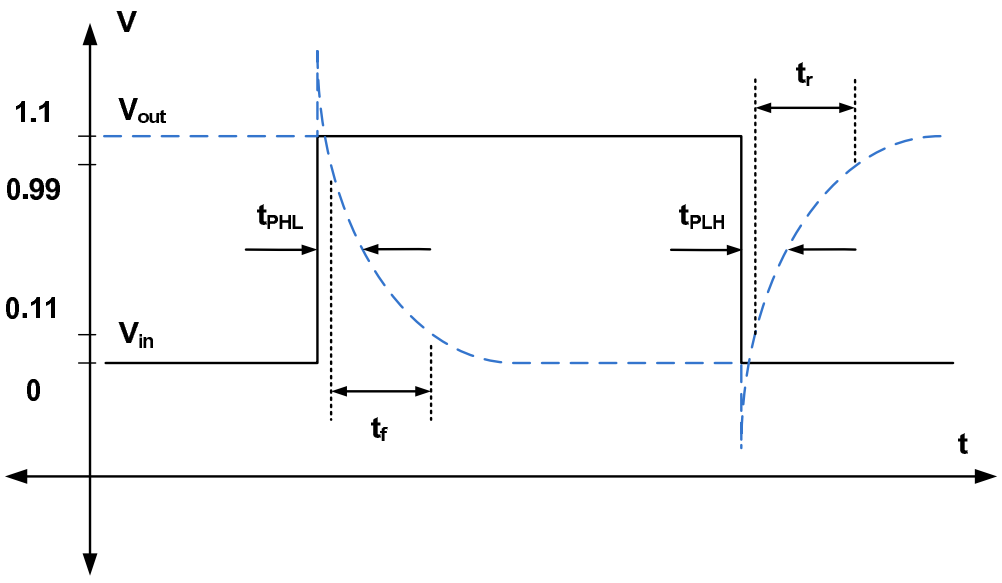

Figure 2-5: Propagation delay.

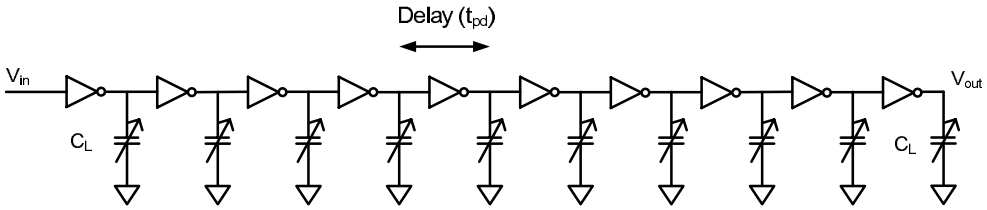

Figure 2-6: Inverter chain with capacitive loads.

$$t_{pd} = \frac{1}{2} \cdot \left(\frac{C_L \cdot V_{DD}}{K_n \cdot (V_{DD} - V_{TN})^{\alpha}} + \frac{C_L \cdot V_{DD}}{K_p \cdot (V_{DD} - V_{TP})^{\alpha}} \right) \tag{2-4}$$

Where C_L is the total load capacitance at the output, V_{DD} is the supply voltage of the inverter, K_n and K_p are the device trans-conductance of NMOS and PMOS, respectively, V_{TN} and V_{TP} are the threshold voltage of NMOS and PMOS, respectively and $\alpha < 2$ is suitable for short channel devices rather than $\alpha = 2$.

2-3-1 Capacitive Load Effect on Inverter Delay

As described by Equation 2-4, the inverter delay is highly dependent on the load capacitance (C_L). This load capacitance is the total amount of inverter intrinsic capacitance at its input and output nodes, and the parasitic capacitances of the interconnects.

As a first attempt, the parasitic capacitances of the interconnects will be modeled by using a lumped component during the simulation and its effects to the inverter delay will be investigated. The experiment set-up has been built as shown in Figure 2-6. With an inverter ratio (Wp/Wn) of 1.32, and the Wn of the inverter is varied from 120 nm to 4800 nm.

The result of this experiment can be seen in Figure 2-7 with a capacitive load value from 100 aF up to 10 fF. It shows that a larger load capacitance will introduce a bigger delay, as is confirmed by Equation 2-4. To have a better view of what is occuring, there are three further figures (2-8, 2-9, 2-10).

2-3-2 Transistor Size Effect on Inverter Delay

As shown in Equation 2-4, the propagation delay of an inverter is inversely proportional to the W/L of a transistor. From the simulation results, Figure 2-7 shows that by increasing the transistor size and by decreasing C_L, the delay will be lower and vice versa. A good agreement has been shown between these simulation results and Equation 2-4.

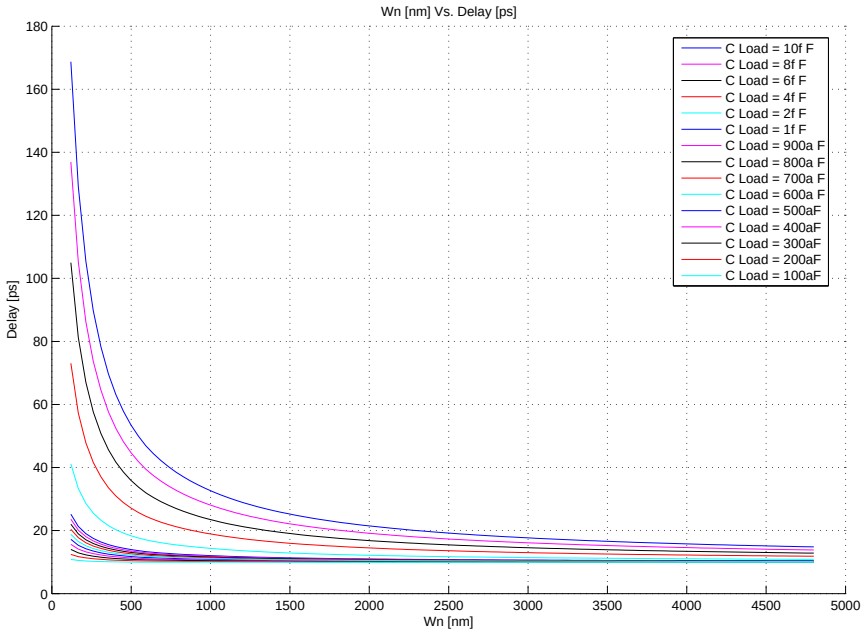

Figure 2-7: Delay with C_{Load} from 100 aF to 10 fF.

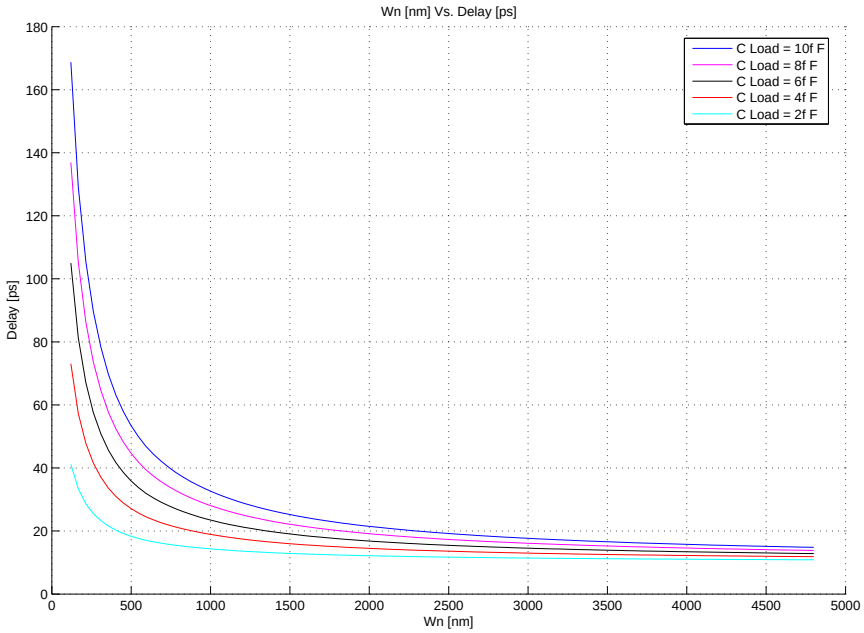

Figure 2-8: Delay with C_{Load} from 2 fF to 10 fF.

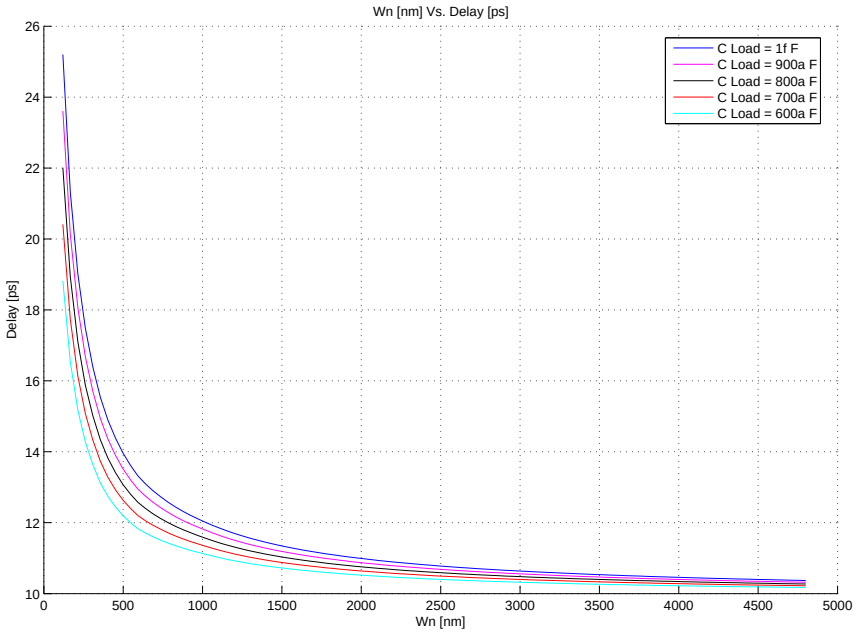

Figure 2-9: Delay with C_{Load} from 600 aF to 1 fF.

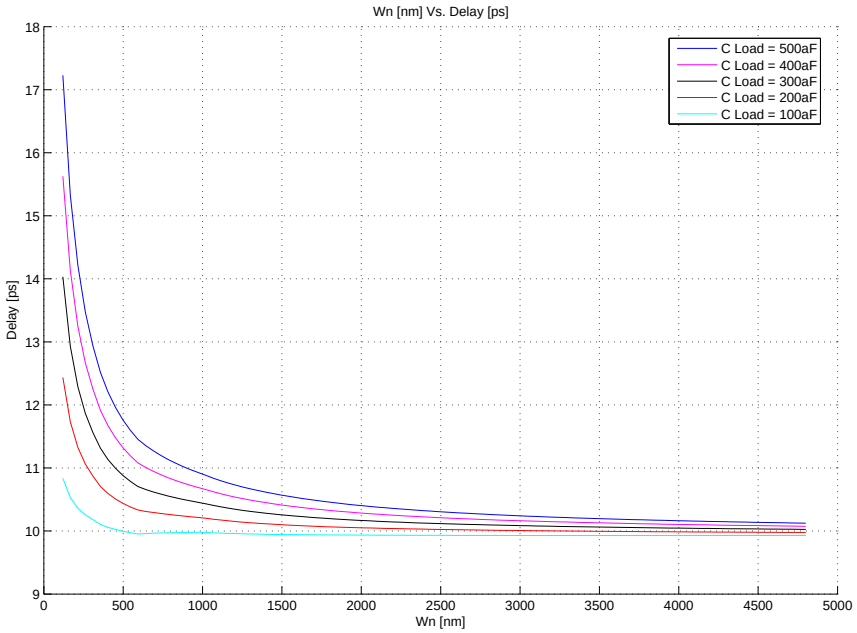

Figure 2-10: Delay with C_{Load} from 100 aF to 500aF.

2-3-3 Threshold Voltage (V_{TH}) Effect on Inverter Delay

The state-of-the-art 40-nm CMOS process provides three types of V_{TH}, they are low V_{TH}, standard V_{TH} and high V_{TH}. Again from Equation 2-4, it can be seen that the lower V_{TH} will reduce the propagation delay. In order to achieve a small propagation delay, which is good for TDC, the low V_{TH} will be considered. However, the low V_{TH} needs an additional mask, which will cost more than a standard V_{TH} in the production process, so low V_{TH} technology is not going to be used in this design. In this design process, the use of an additional mask it is not allowed in order to avoid any additional cost.

2-3-4 Design Corner Effect on Inverter Delay

In CMOS technology, there are two types of device with independent characteristics. These are PMOS and NMOS. Each of these devices has different speeds that should be characterized. In this PDK the corners are denoted with two letters describing the NMOS and PMOS to identify the characterization result. The letters are S, F and T for slow, fast and typical.

From those two devices there will be five combinations that describe the characteristics. The letters are SS, SF, FF, FS and TT for slow-slow, slow-fast, fast-fast, fast-slow and typical-typical, respectively. Three corners will be used to simulate the TDC circuit in this thesis to characterize it in terms of speed. The SS corner will result in the worst case condition of the circuit while the FF corner will result in the best case. The TT corner illustrates the typical operating condition.

To ensure the circuit will operate properly at the worst case condition, the circuit must be simulated under the worst case scenario, which is at the SS corner. During mass production it must result in a high yield.

2-3-5 Supply Voltage Effect on Inverter Delay

It has been shown by Equation 2-2 and 2-3 that for the t_{PHL} and t_{PLH} calculations, the supply voltage (V_{DD}) will greatly affect those parameters. Subsequently, the propagation delay (t_{pd}) as the average result of t_{PHL} and t_{PLH} as written by Equation 2-1 will also be affected.

Higher values of V_{DD} will give more driving strength to the device, therefore a faster delay will be achieved. In this design, the components will be operated at nominal supply of 1.2 volts. However, the power supply may vary due to the tolerances of the voltage regulator and voltage drops along the supply rails. During the design process, this problem should be properly characterized. This problem could usually be solved by designing the appropriate size of power supply path. If the power supply is further increased, the delay will be faster, but at the cost of higher power consumption.

2-4 Power Consumption

The instantaneous power is proportional to the supply current and supply voltage and it is described by Equation 2-5, while the average power is described by Equation 2-6. In terms of frequency, the dynamic power is demonstrated by Equation 2-7.

$$P(t) = i_{DD}(t)V_{DD} \tag{2-5}$$

$$P_{avg} = \frac{E}{T} = \frac{1}{T}\int_0^T i_{DD}(t)V_{DD}\mathrm{d}t \tag{2-6}$$

$$P_{inv} = C_{out}V_{DD}^2 f \tag{2-7}$$

For the power consumption of an inverter, based on Equation 2-7 it is clear that the power dissipation increases with signal frequency.

Chapter 3

The WiMAX ADPLL System and TDC Performance

3-1 WiMAX Technology

WiMAX technology will play a key role in fixed broadband wireless metropolitan area networks in the near future. WiMAX stands for Worldwide Interoperability for Microwave Access. The WiMAX Forum projects an aggressive forecast of users. It is estimated at more than 133 million globally by 2012 [11]. The WiMAX Forum is a non-profit organization, which has more than 540 member companies. Its primary goal is to ensure interoperability among IEEE 802.16 based products through its certification.

The WiMAX Forum identified several applications for 802.16-based systems. These applications can be divided into five major classes. These application classes are Multiplayer Interactive Gaming, VoIP and Video Conference, Streaming Media, Web Browsing and Instant Messaging, and Media Content Downloads.

3-2 Specification of WiMAX ADPLL System

WiMAX technology is based on the IEEE 802.16-2004 air interface standard. Mobile WiMAX profiles developed by the WiMAX Forum will cover 5, 7, 8.75, and 10 MHz channel bandwidths for licensed worldwide spectrum allocations in the 2.3 GHz, 2.5 GHz, 2.7 GHz, 3.3 GHz and 3.5 GHz frequency bands [11].

The 2.3 GHz band is already used in South Korea. The 2.5 to 2.7 GHz band is already allocated in the United States, South America, Europe, and some countries in the Asia-Pacific region for mobile and fixed wireless services. The 3.3 GHz and 3.5 GHz bands are already used for fixed wireless services in many countries worldwide.

Table 3-1: WiMAX system target specification.

Parameter	Target
Frequency Bands	2.3-2.7, 3.3-3.8 GHz
Frequency Step Size	25 Hz
Integrated SSB Noise (1 kHz - 10 MHz)	-39 dBc/Hz
Spot Noise @ 10 kHz	-90 dBc/Hz
Spot Noise @ 100 kHz	-95 dBc/Hz
Far-Out Noise	-150 dBc/Hz

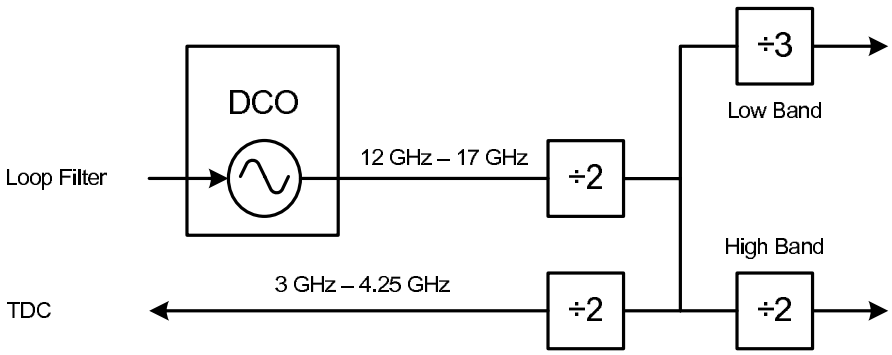

Figure 3-1: All-digital PLL frequency plan.

To cover these WiMAX specification and performance requirements, target specifications have been developed within this project as listed in Table 3-1.

3-3 ADPLL Frequency Planning

In this project, we develop an ADPLL system for a WiMAX application. This project is divided into four sub-projects. Figure 3-1 shows an ADPLL frequency plan. The target frequencies of this ADPLL are from 2.3 GHz to 2.7 GHz for low band and from 3.3 GHz to 3.8 GHz for high band. To meet those ranges and add some margin, the DCO should be designed with output frequencies from 12 GHz to 17 GHz. The output of the DCO will be connected to dividers and will result in the expected frequencies with some margin for the WiMAX ADPLL system as depicted in Figure 3-1. The input frequency for TDC is from 3 GHz to 4.25 GHz.

3-4 TDC Performance for WiMAX ADPLL System

Within the ADPLL system there are two blocks that contribute to the noise, see Figure 3-2 [5]. The first noise source is the block of normalized Digitally Control Oscillator (nDCO),

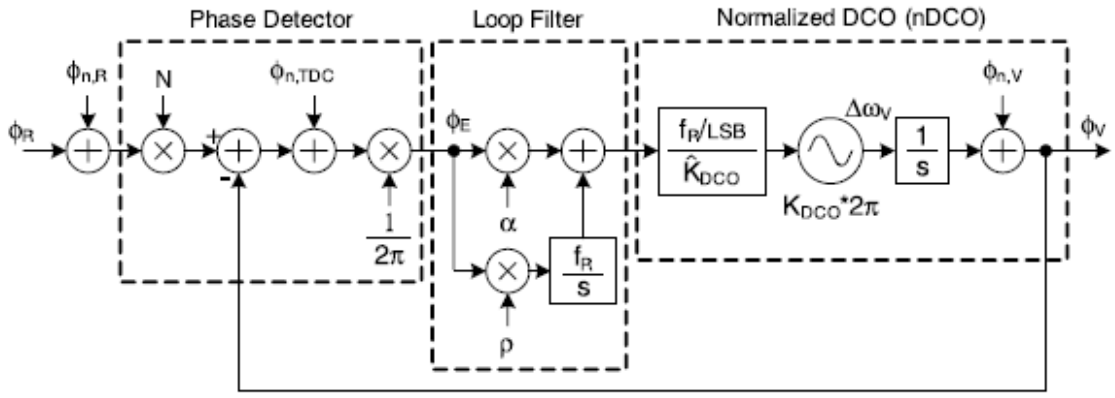

Figure 3-2: S-domain ADPLL noise source.

Table 3-2: Target specification and simulation.

Parameter	Target	Simulated Performance
Spot Noise @ 10 kHz	-90 dBc/Hz	-91.40 dBc/Hz
Spot Noise @ 100 kHz	-95 dBc/Hz	-96.62 dBc/Hz
Integrated SSB Noise (1 kHz - 10 MHz)	-39 dBc/Hz	-41.69 dBc/Hz

which includes the DCO itself and the sigma delta modulator. It has a high-pass noise transfer function characteristic ($\phi_{n,V}$) to the output. The second block is the TDC, which has a low-pass noise transfer function characteristic ($\phi_{n,TDC}$). The rest of the system does not contribute noise due to its digital characteristics. However, the in-band phase noise of an ADPLL is affected by the time resolution of the TDC.

In this project, a TDC is being designed and developed, which has to achieve the target in-band phase noise. It is expected that TDC resolution should be 13 ps, based on the MATLAB simulation results that has been conducted to calculate this requirement.

The MATLAB simulation in Figure 3-3 shows a DCO output frequency of 3.3 GHz and FREF of 33.868 MHz, the phase noise due to the TDC is -97 dBc/Hz at 10 kHz and -100 dBc/Hz at 100 kHz offset. At a DCO output frequency of 4 GHz and FREF of 33.868 MHz, the TDC contribution to the phase noise is -95 dBc/Hz at 10 kHz and -99 dBc/Hz at 100 kHz, as shown in Figure 3-4. The total phase noise due to the DCO and TDC contribution is depicted in Figure 3-5, and is -91.40 dBc/Hz at 10 kHz and -96.62 dBc/Hz at 100 kHz while its integrated phase noise is -41.69 dBc/Hz.

Table 3-2 shows the comparison between the target specification and simulation results. Based on that table, the system has met the specifications and has a 1 dB margin that is acceptable for production.

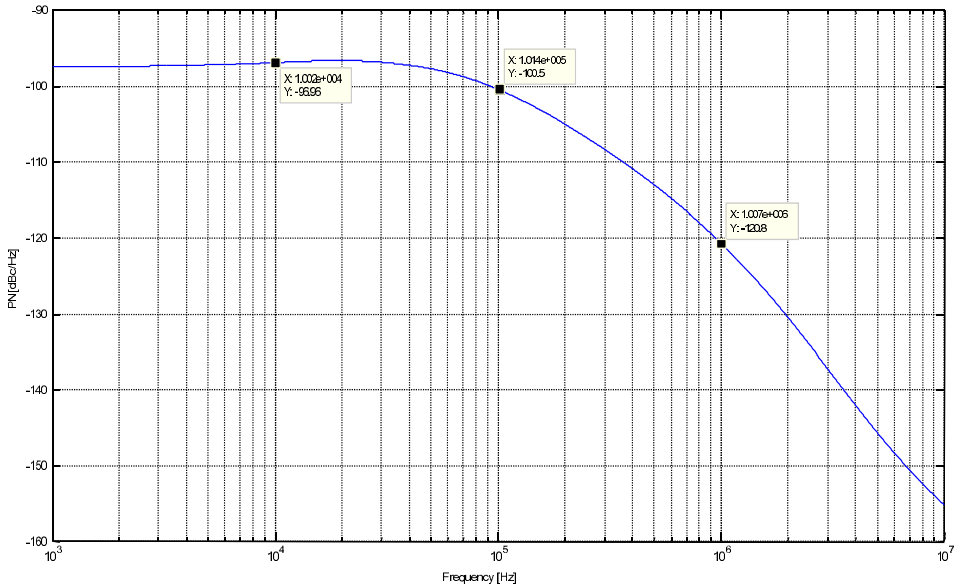

Figure 3-3: TDC noise with DCO frequency of 3.3 GHz and FREF of 33.868 MHz.

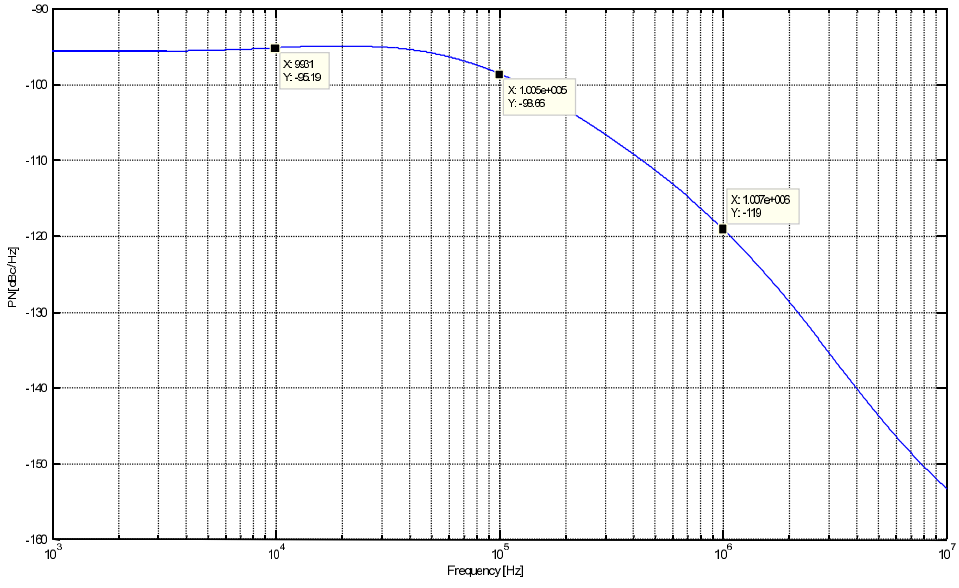

Figure 3-4: TDC noise with DCO frequency of 4.0 GHz and FREF of 33.868 MHz.

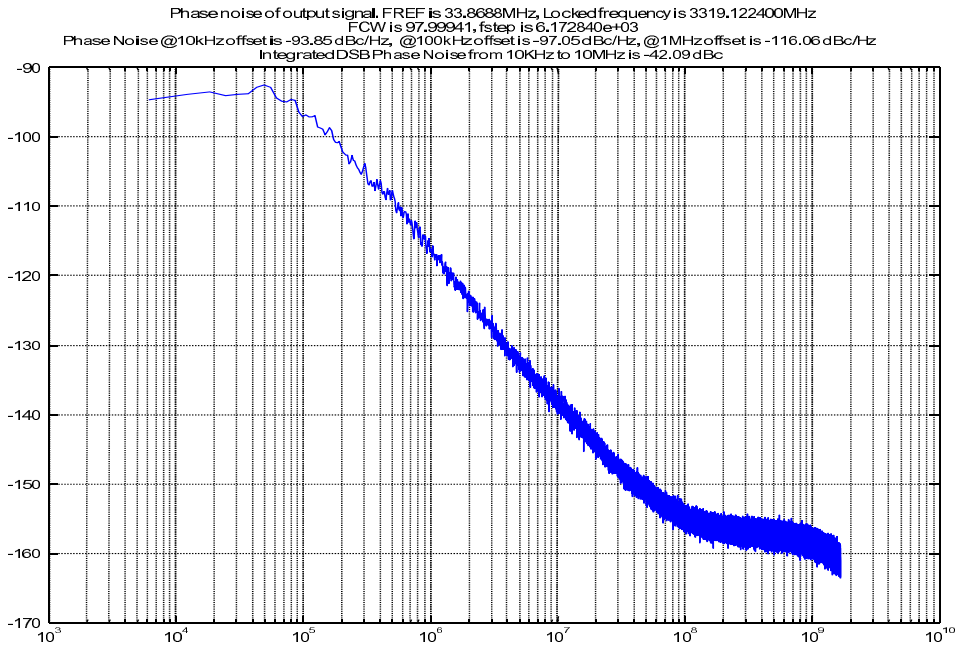

Figure 3-5: Time domain simulation of phase noise on an ADPLL system - FREF of 33.868 MHz.

3-5 Phase Error Detector

Basically, a frequency synthesizer is a circuit that generates one or several frequencies (f_V) from a reference frequency (f_R). To obtain a certain DCO clock of frequency f_V, the FCW (Frequency Command Word) should be first defined and then entered as an input to the ADPLL system by following the equation below.

$$FCW = \frac{f_V}{f_R} \tag{3-1}$$

The FCW value identifies how many high-frequency CKV clocks have to be contained within one FREF clock. Within the ADPLL system, this operation is equivalent to a comparison of the process between the reference phase and variable phase to obtain the phase error. The phase error will be estimated in the hardware by means of the phase detector, and mathematically it is written as in Equation 3-2.

$$\hat{\phi}_E[k] = R_R[k] - R_V[k] + \epsilon[k] \tag{3-2}$$

A block diagram of a phase detector is depicted in Figure 3-6 as presented in [1]. This phase detector has three phase sources: reference phase ($R_R[k]$), variable phase ($R_V[k]$), and fractional error correction ($\epsilon[k]$). The variable phase ($R_V[k]$) runs on the CKV clock

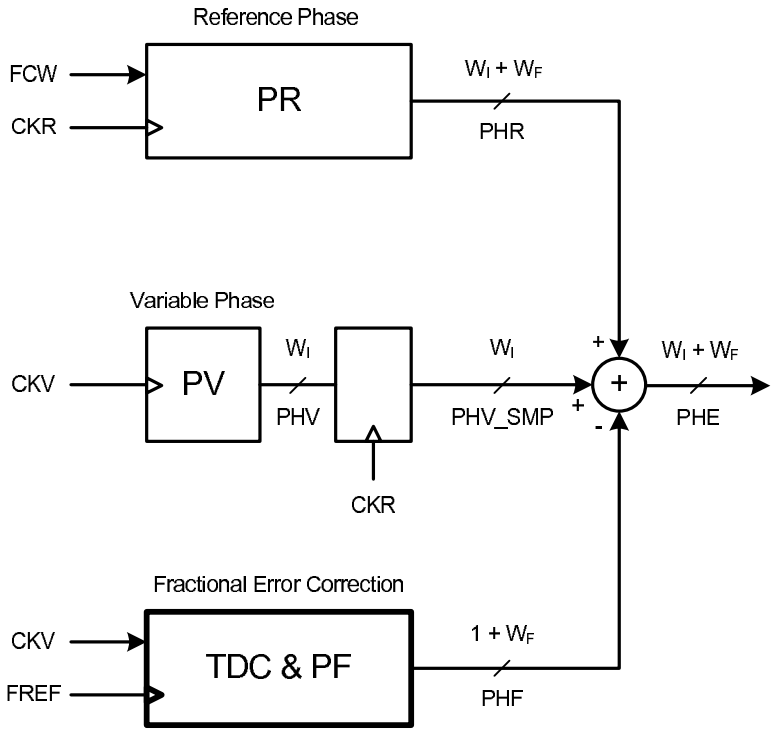

Figure 3-6: A block diagram of a phase detector.

and is reclocked by the CKR clock. Therefore at the end, all three phase sources are synchronous with the CKR clock.

3-5-1 Reference Phase Block

An accumulator is designed for the implementation of $R_R[k]$. It can be obtained by accumulating the Frequency Command Word (FCW), as in Equation 3-3.

$$R_R[k] = \sum_{l=1}^{k} FCW \tag{3-3}$$

3-5-2 Variable Phase Accumulator Block

An accumulator at the first stage and a flip-flop at the second stage are implemented for the block of the variable phase accumulator, $R_V[k]$. The variable phase accumulator counts the increments of the DCO clock as per the following equation.

$$R_V[i] = \sum_{l=1}^{i} 1 \tag{3-4}$$

3-5-3 Fractional Error Correction

Fractional error correction ($\epsilon[k]$) between the reference clock (FREF) and the DCO clock (CKV) is measured by means of *a time-to-digital converter* (TDC). This TDC has a chain of inverters with inverter propagation delay as a time reference. Resolution of one inverter delay (t_{inv}) is the time quantization resolution of the TDC (Δt_{res}). In production and operation, each inverter within the inverter chain will have variance in propagation delay. Therefore, digital representation of the TDC output could not be used directly as a fractional error correction ($\epsilon[k]$). The digital output code of the TDC must be normalized by the oscillator clock period (T_V) before it is used as a fractional error correction ($\epsilon[k]$), as in Equation 3-5.

$$\epsilon[k] = 1 - \Delta t_r / T_V \tag{3-5}$$

As shown in Figure 3-7 and Figure 3-8, Δt_r is a quantized time delay between the rising edge of the DCO clock and the FREF sampling edge, while Δt_f is between the falling edge of the DCO clock and the FREF sampling edge with a resolution of (t_{inv}). In this system, Δt_r and Δt_f will be indicated by the position of the transition from 1 to 0 and the transition detected from 0 to 1, respectively (in Fig.3-7, $\Delta t_r = 10$ and $\Delta t_f = 16$, Fig.3-8, $\Delta t_r = 16$ and $\Delta t_f = 10$).

Information regarding Δt_r and Δt_f from the *time-to-digital converter* (TDC) can be used to calculate the half-period of the DCO clock by using the following calculation.

$$T_V \begin{cases} \Delta t_r - \Delta t_f & \Delta t_r \geq \Delta t_f \\ \Delta t_f - \Delta t_r & otherwise \end{cases} \tag{3-6}$$

Once $R_R[k]$, $R_V[k]$, and $\epsilon[k]$ have been calculated and are available, based on Equation 3-3, Equation 3-4, and Equation 3-5, respectively, then the phase error, $\hat{\phi}_E[k]$, will be calculated by using Equation 3-2.

3-6 The TDC Architecture

In this thesis, three types of current state-of-the-art TDC architectures are carefully studied and analyzed. Considerations in terms of area, cost, power consumption, calibration method, complexity and possibility for future improvement are taken into account in choosing the TDC architecture that is suitable for this WiMAX ADPLL system. It is predicted that the TDC will need a resolution of 13 ps in order to achieve -95 dBc/Hz of in-band phase noise.

The first architecture in Figure 3-12 [4] is a pseudo-differential TDC architecture that is insensitive to nMOS and pMOS transistor mismatches. This TDC has resolution of 20

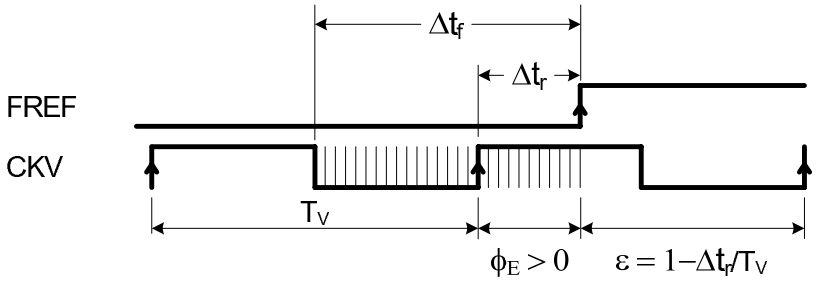

Figure 3-7: Positive phase error (Source:[1]).

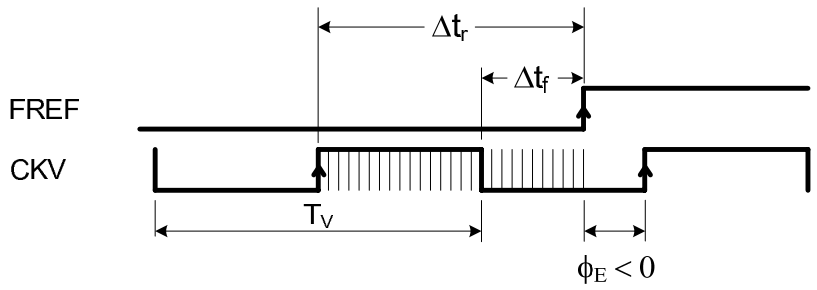

Figure 3-8: Negative phase error (Source:[1]).

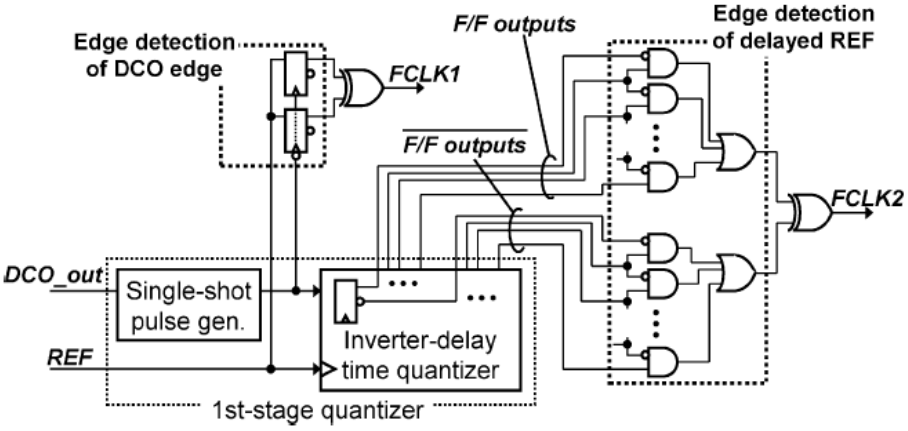

Figure 3-9: First stage of time-windowed TDC architecture.

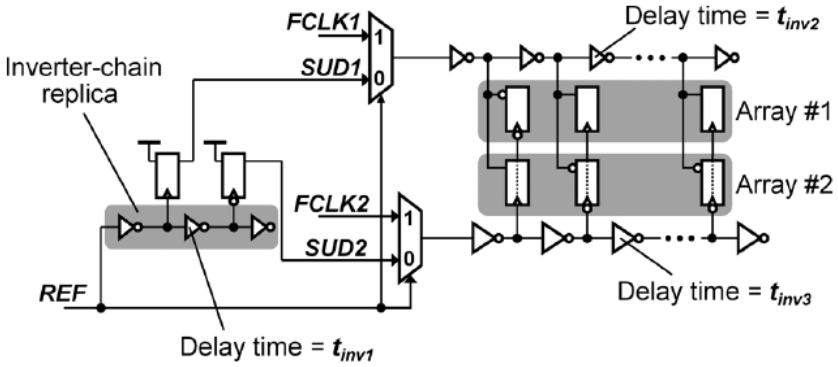

Figure 3-10: Second stage of time-windowed TDC architecture.

ps in 90-nm CMOS technology. It is expected to achieve a better resolution in future technology. However, for wireless application standards, this resolution is sufficient [6]. The drawback of this TDC is the high power consumption required since the DCO clock frequency is applied to the inverter chain.

The second architecture applies the DCO clock frequency to the data port of flip-flop instead of an inverter chain. It was presented in 2010 [7]. The ADPLL was designed in 90-nm CMOS technology with a time-windowed TDC. This TDC has low power consumption since the inverter will operate at a very low frequency. Furthermore, this TDC has a significant improvement in resolution. It uses a two-step structure with an inverter and a vernier-delay time to achieve 5 ps of resolution. However, the flip-flop should be carefully chosen in this design since it has to be matched with the operating principle of the TDC. The drawback of this TDC is that it occupies a large area of silicon and it is more complex since it uses 2-stage architecture, as shown in Figure 3-9 and Figure 3-10.

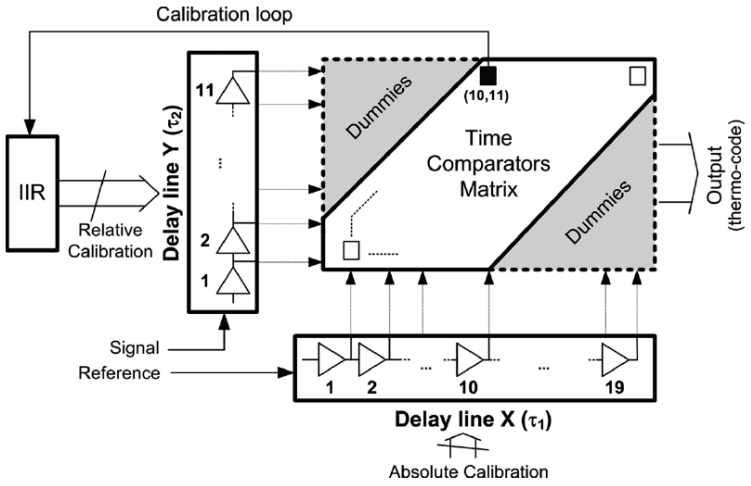

Figure 3-11: Two-dimensional Vernier TDC architecture.

In 2010 [8], a group at the Pavia University used a digital approach to develop a PLL with a two-dimensional vernier algorithm applied to a time to digital converter (TDC). With a time resolution TDC of 4.8 ps, the chip was realized in 65-nm CMOS technology. The drawback of this TDC system is that it has a complex analog calibration and it is analog intensive. This calibration circuit and method for its operation use an IIR filter circuit, as illustrated in Figure 3-11.

Based on the evaluation of the above three architectures, the chosen architecture in this WiMAX ADPLL design will be based on the first architecture [4, 6]. This architecture uses an inverter as a delay element since its propagation delay is the fastest logic-level regenerative timing method in CMOS technology, as in Figure 3-12. Furthermore, it will benefit from the technology scaling process through increased speed and low power consumption. However, parasitic capacitances should be taken into account during the design process. In the next chapter, it will be shown that with this simple architecture the target of a TDC resolution lower than 13 ps can be achieved.

Moreover, this architecture has a very simple calibration method compared to the other two architectures. The calibration process in this all-digital PLL (ADPLL) system works with normalized measurement values. It means that the absolute time interval is not of interest, but rather a fraction of this time interval with respect to another time interval (T_V). Achieving a resolution below T_{inv} is done through averaging.

$$\overline{T}_V = \frac{1}{N_{avg}} \sum_{k=1}^{Navg} T_V[k] \tag{3-7}$$

In the original design [4], the number of inverters within the inverter chain will depend on

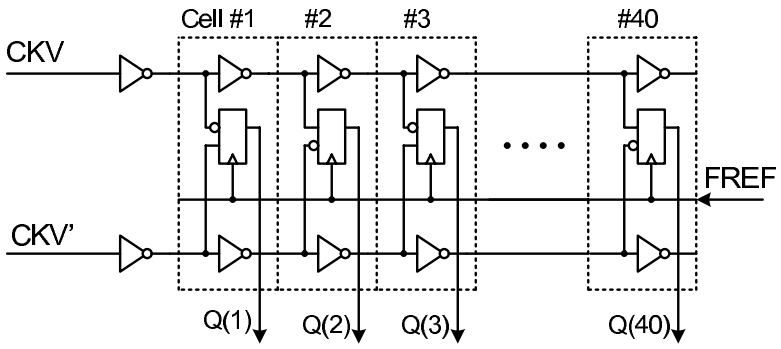

Figure 3-12: Pseudo-differential TDC architecture.

the maximum DCO period of T_V. The number of inverters, L, can be calculated as follows:

$$L \geq \frac{max(T_V)}{min(t_{inv})} \tag{3-8}$$

Some margin on the number of inverter should be provided to guarantee that system will operate properly at the fast process corner and at the lowest DCO frequency (f_V).

Chapter 4

The TDC Building Blocks

4-1 Delay Element

4-1-1 An Inverter as a Delay Element

Within a flash ADC system, resistors act as a voltage reference to carry out the quantization process. Within a TDC system, instead of resistors, inverter delay elements are used. An inverter can be used as a delay element by using its propagation delay (t_{pd}) characteristics. The delay characteristics can be found in Equations [2-1, 2-2, 2-3, and 2-4]. Here, it is re-written as Equation 4-1. Where C_L is the total load capacitance at the output, V_{DD} is the supply voltage of the inverter, and β_n and β_p are the device trans-conductance of NMOS and PMOS, respectively. V_{TN} and V_{TP} are the threshold voltage of NMOS and PMOS, respectively. $\alpha < 2$ is suitable for short channel devices rather than $\alpha = 2$ [12].

$$t_{pd} = \frac{1}{2} \cdot \left(\frac{C_L \cdot V_{DD}}{\beta_n \cdot (V_{DD} - V_{TN})^{\alpha}} + \frac{C_L \cdot V_{DD}}{\beta_p \cdot (V_{DD} - V_{TP})^{\alpha}} \right) \tag{4-1}$$

The propagation delay value (t_{pd}) of an inverter can vary due to PVT variation, mismatch and jitter. These factors have independent and uncorrelated effects on the inverter propagation delay. Each component has a different effect on the TDC performance. The delay variance due to PVT ($\sigma^2_{tpd,PVT}$) will introduce gain error. The TDC linearity performance will be affected by the delay variance due to mismatch ($\sigma^2_{tpd,mismatch}$) and it should be lower than 1 LSB. This TDC linearity will introduce fractional spurs on the ADPLL system. The noise on the system, which cause delay variance ($\sigma^2_{tpd,jitter}$) will introduce phase noise on the TDC system. The following sections of this chapter will cover the details.

4-1-2 Delay Element Mismatch

Mismatch in threshold voltage V_T, device trans-conductance β, and drain current I_d will introduce uncertainties in the propagation delay of a delay element. These uncertainties in propagation delay due to mismatch will only contribute to the output skew between one delay element and another. In a TDC system it will introduce a linearity error.

In [10], the mismatch variance of an inverter can be found from Equation 4-1 via partial derivatives. The result is Equation 4-2 below, where $\sigma^2_{V_{TN}}$, $\sigma^2_{V_{TP}}$, $\sigma^2_{\beta_n}$, $\sigma^2_{\beta_p}$, and $\sigma^2_{C_L}$ are the variances of V_{TN}, V_{TP}, β_n, β_p, and C_L, respectively.

$$\sigma^2_{tpd,mis} = \frac{t^2_{pd}}{4}\left(\frac{2\sigma^2_{C_L}}{C^2_L} + \frac{\sigma^2_{\beta_n}}{\beta^2_n} + \frac{\alpha^2\sigma^2_{V_{TN}}}{(V_{DD}-V_{V_{TN}})^\alpha} + \frac{\sigma^2_{\beta_p}}{\beta^2_p} + \frac{\alpha^2\sigma^2_{V_{TP}}}{(V_{DD}-V_{V_{TP}})^\alpha}\right) \tag{4-2}$$

From Equation 4-2, it is shown that to reduce the delay variance ($\sigma_{tpd,mis}$), that C_L, β and V_{DD} should be increased.

If the delay of each inverter varies independently with a standard deviation of $\sigma_{tpd,mis}$ due to local variations in the chain of inverters, these delay variations will be accumulated through the chain, then after the N-th inverter, as in [13], the signal arrival time will vary, as in Equation 4-3. The maximum mismatch variance will be at the end of the inverter chain.

$$\sigma_{tpd,mismatch} = \sqrt{N} \cdot \sigma_{tpd,mis} \tag{4-3}$$

The total mismatch variance of the TDC is the sum of the inverter chain mismatch variance and comparator mismatch variance, as in Equation 4-4 [14].

$$\sigma^2_{total,mismatch} = \sigma^2_{comp,mismatch} + \sigma^2_{tpd,mismatch} \tag{4-4}$$

The maximum mismatch variance within the TDC ($\sigma_{total,mismatch}$) has to be lower than the TDC resolution in order to produce an integral error with value of less than one LSB [8] [15]. Based on the simulation results and calculations in Chapter 5, this requirement can be met.

4-1-3 Delay Element Jitter

The noise within an inverter will generate timing error with value much lower than the one generated by mismatch since both current and voltage due to noise are much lower than that generated by device mismatch [16, 17]

The compact expression of uncertainty in propagation delay caused by current noise integrating on the capacitor, and an initial noise on the capacitor due to channel resistance prior to the switching event, has been analyzed and described in [18, 19]. With Boltzmann's constant k, temperature T, noise factor γ (typically equal to 2/3), output capacitance C, threshold voltage V_T, and discharge current I, the jitter delay variance is written as presented in Equation 4-5. This jitter will contribute to the in-band phase noise of an ADPLL system.

$$\sigma^2_{tpd,jitter} = \frac{4kT\gamma t_{pd}}{I(V_{DD} - V_T)} + \frac{kTC}{I^2} \tag{4-5}$$

The contribution of jitter to the phase noise should meet the requirement. The phase noise has a limit of -95 dBc/Hz and, based on the simulation results as will be shown in Section 5-3-4, we meet this requirement.

4-1-4 Power Consumption

The power consumption of an inverter has been explained in the Equations [2-5, 2-6, and 2-7]. Here it is re-written, and it is clear that the power dissipation increases with signal frequency.

$$P_{inv} = C_{out}V^2_{DD}f \tag{4-6}$$

Based on the simulation results in Chapter 5, increasing the frequency of the CKV signal, increases the power consumption. Figure 5-17 illustrates the power consumption of the complete TDC core for different frequencies of CKV, not only for the inverter. However, the biggest contributor to this power consumption is the inverter chain since the signal with the highest frequency is in this path.

4-2 Comparators

The conversion accuracy of either flash ADC or TDC depends on the precision of the comparators used. The challenge in designing a comparator are speed, metastability, offset, noise, and power consumption.

The comparator designed in Figure 4-1 is a current-controlled latch sense amplifier based on [20, 21] for low power considerations, which modify the traditional current-mirror sense amplifier. The current flowing through the latch circuits is small. The current flows during

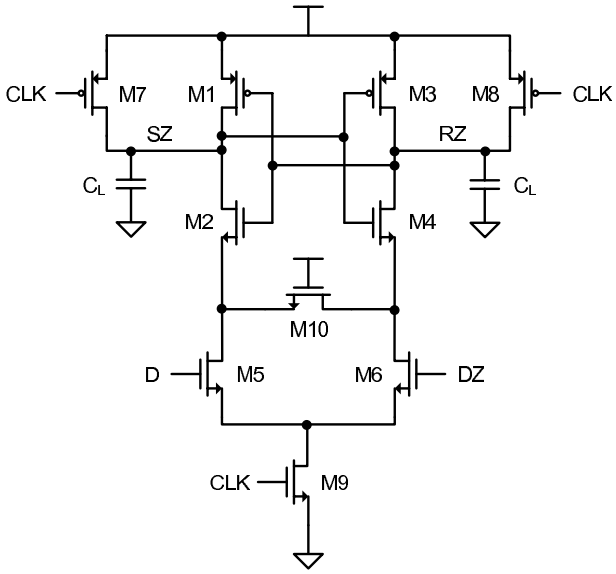

Figure 4-1: Current sense amplifier.

switching process on inverters of the latch sense amplifier only. It does not dissipate any static power during its operation. Therefore, power consumption can be minimized without sacrificing speed.

Moreover, the most important factor, this comparator has a very light input capacitance since it has only one NMOS transistor at the input point. This light load capacitance effect will be used as an advantage by the inverter delay line. The same condition has been applied on paper [4].

4-2-1 Comparator Speed

In [22, 23], a comparator design based on [20] is explored in terms of speed. It has two phases of delay; hence the author in [22, 23] can estimate the speed of a current-controlled latch sense amplifier.

During the first phase, load capacitance discharge delay takes place. In this phase, the load capacitance C_L at node SZ or RZ in Figure 4-1 is discharged and can be expressed as an equation below.

$$t_o = \frac{C_L V_{thp}}{I} \tag{4-7}$$

Subsequently, after the t_o delay is reached, an initial voltage difference will be generated at the output nodes to start the second phase of delay. During the second phase, strong positive feedback occurs and the behavior of the circuit can be analyzed as two cross-coupled inverters as shown in Figure 4-2. For simplicity, the source terminal of M2 and M4 are connected to ground ($VGND$).

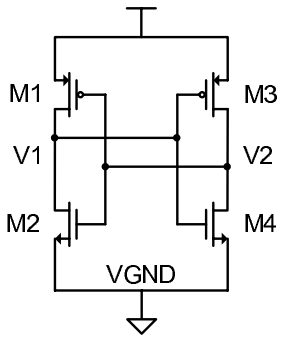

Figure 4-2: Cross-coupled CMOS inverters.

With an initial voltage difference at the output nodes V_1 and V_2 in Figure 4-2 as described by Equation 4-8, the voltage swing ΔV_{out} at the output has to be reached after some time, which is called the latch waiting time or the latch delay time (t_{latch}) and is described mathematically in Equation 4-9 [24].

$$V_0 = V_2\left(t=0\right) - V_1\left(t=0\right) \tag{4-8}$$

$$t_{latch} = \frac{C_L}{g_{m,eff}} \ln\left(\frac{2\Delta V_{out}}{V_o}\right) \tag{4-9}$$

$$\tau_{latch} = \frac{C_L}{g_{m,eff}} \tag{4-10}$$

The effective trans-conductance $g_{m,eff}$ of both inverters is the same if it assumes a matched circuit and it is written as Equation 4-11.

$$g_{m,eff} = g_{m1} + g_{m2} - \frac{1}{r_{DS1} \parallel r_{DS2}} := g_m - \frac{1}{r_{DS}} \tag{4-11}$$

The time constant, as in Equation 4-10, can be re-written as Equation 4-12 below.

$$\tau_{latch} = \frac{C_L}{g_m - \frac{1}{r_{DS}}} \tag{4-12}$$

Recalling the absolute inverter gain as in Equation 4-13, thus Equation 4-12 can be re-written as Equation 4-14 below:

$$A_{inv} = g_m r_{DS} \tag{4-13}$$

$$\tau_{latch} = \frac{r_{DS}C_L}{g_m r_{DS} - 1} \approx \frac{r_{DS}C_L}{A_{inv}} \tag{4-14}$$

From the above equation, it shows that to reach a maximum speed, a large inverter gain and a small load capacitance are required by a latch-type sense amplifier.

In [22, 23], it is shown that the total delay of a latch-type current sense amplifier is given by:

$$t_{sa} = t_o + t_{latch} \tag{4-15}$$

$$t_{sa} = \frac{C_L V_{thp}}{I} + \frac{C_L}{g_{m,eff}} \ln\left(\frac{1}{V_{thp}}\sqrt{\frac{I_o}{2\beta}}\frac{\Delta V_{out}}{\Delta V_{in}}\right) \tag{4-16}$$

Based on the above equation, the total delay is affected by the load capacitance (C_L), inverter gain (g_m), current (I_o) and input voltage (ΔV_{in}).

4-2-2 Metastability

One of the important parameters of a comparator for a flash ADC is metastability. The importance of metastability is also applicable to a TDC. This section will cover the aspects of metastability required for the comparator design.

In a synchronous system, there is a fixed relationship between the data and the clock. However, in an asynchronous system, the relationship between the data and clock is not fixed. When the relationship has met the setup time and hold time requirements during its operation, the output of the device will result in a valid state within its specified propagation delay time. But if the setup and hold times relationship is violated, the output of the device will result in an intermediate level value between its two valid values, and remain at that value for an indefinite amount of time before it is resolved. This event is called metastability, as shown in Figure 4-4. The metastable condition will result in a failure if the output has not been resolved by itself within the specified resolution time when it must be valid for use. A very useful paper regarding metastability testing used in this thesis is written by Gabara [25].

To have a good understanding of the characteristics of metastability and its resolution time, it is helpful to analyze the response of the bistable element made from cross-coupled inverters by using a first order small signal model as shown in Figure 4-3.

Much research has been conducted and many papers have been published regarding metastability. Based on [26, 27, 28], the following equations have been derived, and based

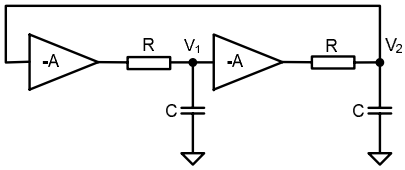

Figure 4-3: First order small signal model of flip-flop.

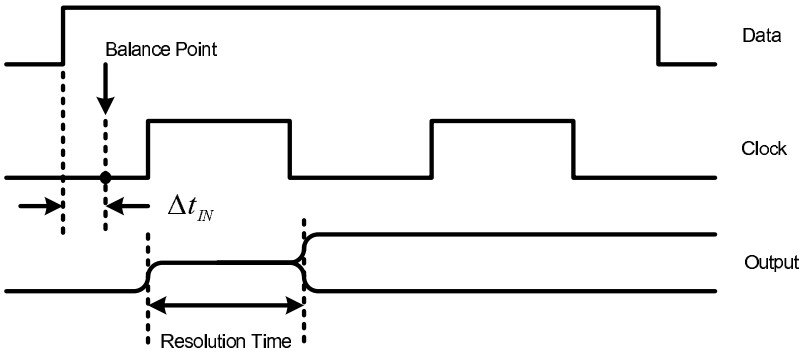

Figure 4-4: Metastable. [28]

on that the analytical work of this thesis is performed. It has been proven that the output voltage of a comparator will grow exponentially as Equation 4-17, therefore the time taken for the metastability condition to be resolved is given by Equation 4-18. Where V_0 is the initial condition as in Equation 4-8, V_{out} is the output voltage, and τ is the time constant of the circuit.

$$V_{out} = V_0 \cdot e^{\frac{t}{\tau}} \tag{4-17}$$

$$t = \tau \ln\left(\frac{V_{out}}{V_0}\right) \tag{4-18}$$

There is no surprise in Equation 4-18. It is similar to the second term of Equation 4-16, which mathematically explains the current sense amplifier response during the second phase of its operation. Both equations are determined from the responses of the bi-stable element made from cross-coupled inverters.

Where V_0 is the initial condition that depends on the overlap time between the clock and data with reference to Figure 4-4 [28]. The value of V_0 itself is given by Equation 4-19, where Δt_{in} is the overlap time between data and clock and a is the rate at which Δt_{in} will be converted into a voltage difference between the two nodes of the cross-coupled inverters. Equation 4-18 and Equation 4-19 will result in Equation 4-20, and thus the metastability window t_w, is given by Equation 4-21 [28].

$$V_0 = a \cdot \Delta t_{in} \tag{4-19}$$

$$t = \tau \ln\left(\frac{V_{out}}{a \cdot \Delta t_{in}}\right) \tag{4-20}$$

$$t_w = \frac{V_{out}}{a} \tag{4-21}$$

When the input time Δt_{in} is smaller, the initial voltage is closer to the metastability point and the resolution time is longer. If the input is exactly at the balance point, $\Delta t_{in} = 0$, then the output will remain at the metastable point and the output resolution time will theoretically be infinite [28]. This amount of resolution time of a device will play a large role in calculating its failure rate.

With a DCO clock period of T_V, the cumulative error probability of input time smaller than t_w is:

$$P_e = \frac{t_w}{T_V} \tag{4-22}$$

If the reference frequency of f_R is given, the error probability of any input time smaller than t_w is:

$$\frac{P_e}{1second} = \frac{t_w}{T_V} \cdot f_R = t_w \cdot f_V \cdot f_R \tag{4-23}$$

The above equation should be multiplied by the number of flip-flops within the TDC to get the total result. Finally, the formula of MTBF (Mean Time Between Failure) can be expressed by Equation 4-24. This mean time between failures (MTBF) is used to represent the error free operation of our comparator in a TDC application.

$$MTBF = \frac{1}{t_w \cdot f_V \cdot f_R} \tag{4-24}$$

If there is a failure, within one FREF cycle, the value of $\epsilon[k]$ will be wrong. Furthermore, the metastability will propagate into the loop filter and the entire system hangs, then it needs to be reset.

Metastability window requirement of the WiMAX ADPLL system

From the WiMAX ADPLL specifications, the maximum DCO frequency output is quite high ($f_V = 4.25GHz$), and the maximum reference frequency is about $33.8688MHz$ ($f_R = 33.8688MHz$).

Supposing that the designed system is intended to have one failure within one year then, based on Equation 4-23 and all available values, the metastability window (t_w) should be

lower than 2.202×10^{-25} seconds within a resolution time of around 29 ns. Section 5-1 will demostrate how to calculate the required number of TDC cells or flip-flop. Based on that calculation, the system needs 40 TDC cells or flip-flop. Since the number of TDC cells or Flip-flop is 40 for our case, then the limit for the metastability window is around 8.81×10^{-24} seconds. The simulation results in Section 5-2-2 shows that we meet this requirement.

4-2-3 Comparator Offset

Comparators in practices have a built-in offset current and offset voltage due to the finite matching of components. Therefore when a zero signal is applied, these offsets will result in a non-zero output voltage or current. Offsets are the largest errors in comparators.

Offsets are classified into systematic offsets and random offsets. Systematic offsets could be reduced by symmetric design and a good layout. Random offsets are the result of random variations during the fabrication process, that cause mismatches in the trans-conductance factor β and the threshold voltage V_T of the transistors. Such mismatches are inversely proportional to the square root of the area of the transistor, as described by the following equations based on [29], where A_{V_T} and A_β are the area proportionality constant for V_T and β, respectively, and S_{V_T} and S_β are the variation of parameter V_T and β with the spacing, respectively, and D is the spacing between the two devices.

$$\sigma^2(V_T) = \frac{A_{V_T}^2}{WL} + S_{V_T}^2 D^2 \tag{4-25}$$

$$\frac{\sigma^2(\beta)}{(\beta)^2} = \frac{A_\beta^2}{WL} + S_\beta^2 D^2 \tag{4-26}$$

Based on the above equations, in order to reduce random offsets, the device designed should be larger or we should increase either W or L.

Static Offset Voltage

In the dynamic comparator, there are two types of mismatch analysis. The first type is due to the static offset voltage on the trans-conductance factor β and the threshold voltage V_T. The second type is a dynamic offset voltage due to the mismatch of parasitic capacitance.

Reference [30] presents a similar analysis on the sources of mismatch in Figure 4-1. These are $M1$ and $M3$ ($\sigma^2_{V_{OS,M1M3}}$), $M2$ and $M4$ ($\sigma^2_{V_{OS,M2M4}}$), and $M5$ and $M6$ ($\sigma^2_{V_{OS,M5M6}}$). This mismatch might be reduced by increasing the size of those transistors.

Dynamic Offset Voltage

For dynamic offset voltages due to the mismatch of parasitic capacitors, the largest contributor is capacitor mismatch at the output nodes [30]. C_1 and C_2 are the parasitic capacitances at the output node SZ and RZ, respectively, as in Figure 4-1. The effects of parasitic capacitance mismatch will only occur during transient. Moreover, it is also shown in [30] that the relative capacitance mismatch ($\Delta C/C_1$) is more important than the absolute capacitance mismatch ($\Delta C = C_1 - C_2$). If the relative capacitance mismatch is increased at the output, then the input referred offset voltage will be increased and vice versa. Therefore to minimize the dynamic offset voltages, one can increase the area of transistors at the output nodes so that the relative mismatch is reduced. However, there will be a trade-off between the dynamic offset voltages ($\sigma^2_{V_{OS,C1C2}}$) and the speed of the comparator.

By considering the static offset voltage and dynamic offset voltage together, the following equation for the overall random offset voltages of the comparator can be obtained [30].

$$\sigma^2_{comp,V_{OS}} = \sigma^2_{V_{OS,M1M3}} + \sigma^2_{V_{OS,M2M4}} + \sigma^2_{V_{OS,M5M6}} + \sigma^2_{V_{OS,C1C2}} \tag{4-27}$$

If the slope is $s = V_{DD}/2t_d$ [31, 14, 32], then:

$$\sigma^2_{comp,mismatch} = \sigma^2_{comp,V_{OS}} \cdot \frac{4t_d^2}{V_{DD}^2} \tag{4-28}$$

This comparator mismatch ($\sigma_{comp,mismatch}$) will contribute to the total mismatch of the TDC, as in Equation 4-4 [14]. The total mismatch within the TDC ($\sigma_{total,mismatch}$) has to be lower than the TDC resolution to be able to produce an integral error with a value of less than one LSB [8] [15]. The simulation results in Chapter 5 show that we meet this requirement.

4-2-4 Comparator Noise Analysis

In [33], the first estimation of the input referred noise of the strobed comparator has been described and validated. Furthermore, in [34] the input referred noise of the current sense amplifier designed is satisfactorily explored and described by the author by dividing it into three operation phases based on an SDE (Stochastical Differential Equation). In a general form, the input-referred noise in the dynamic comparator was described in Equation 4-29, with κ as a constant that depends on the architecture of the comparator, with the Boltzmann's constant k, temperature T, noise factor γ (typically equal to 2/3), output capacitance C_L and $\sigma_{comp,n}$ as the input noise with the unit of Volt as from [33] [34] [35].

$$\sigma^2_{comp,n} = \kappa \frac{kT\gamma}{C_L} \tag{4-29}$$

This expression may limit accuracy; however it will provide a more interpretable expression, where the parameters being considered can be used as references for designing the comparators. It is clear from Equation 4-29, that to reduce noise, the capacitance values need to be larger.

Comparator Jitter Variance

From Equation 4-29, the input-referred noise of the regenerative-latch comparator has been provided. The comparator jitter variance can be approximated by the input-referred noise power ($\sigma^2_{comp,n}$) divided by the square of the inverter slope.

$$\sigma^2_{comp,jitter} = \frac{\sigma^2_{comp,n}}{s^2} \tag{4-30}$$

If the inverter slope is $s = V_{DD}/2t_d$ [31, 14, 32], then comparator jitter variance can be re-written as the following equation.

$$\sigma^2_{comp,jitter} = \kappa \frac{kT\gamma}{C_c} \cdot \frac{4t_d^2}{V_{DD}^2} \tag{4-31}$$

Based on the above equation, the comparator jitter variance $\sigma_{comp,jitter}$ can be reduced by either increasing the output capacitance (C_c) or the power supply.

4-2-5 Power Consumption of Comparator

Power consumption of the designed comparator will be based on Equation 4-16. Here, the equation is re-written by replacing gm and t_{sa} with I/V_{eff} and $1/f_s$, respectively as in [14], one will have the following equation.

$$\frac{1}{f_s} = \frac{C_L V_{thp}}{I} + \frac{C_L V_{eff}}{I} \ln\left(\frac{1}{V_{thp}}\sqrt{\frac{I_o}{2\beta}}\frac{\Delta V_{out}}{\Delta V_{in}}\right) \tag{4-32}$$

$$P_{comp} = \left(C_L V_{thp} + C_L V_{eff} \ln\left(\frac{1}{V_{thp}}\sqrt{\frac{I_o}{2\beta}}\frac{\Delta V_{out}}{\Delta V_{in}}\right)\right) V_{DD} f_s \tag{4-33}$$

In this design, the comparator used is a Sense Amplifier in the first stage and a slave set-reset (SR) latch in the second stage, as shown in Figure 4-5. Therefore, this structure is known as a Sense Amplifier Flip-Flop (SAFF). With this structure, very low power consumption is achieved since it uses the AOI structure, which prevents the crow-bar current (please refer to the left part of Figure 4-5). This flip-flop achieves a small delay

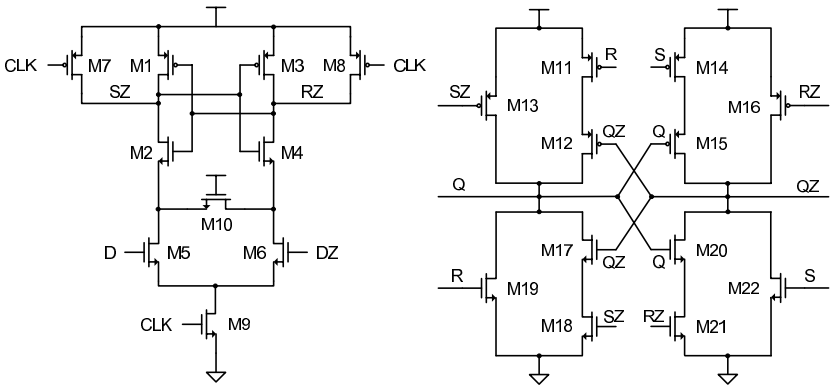

Figure 4-5: Sense amplifier flip-flop (SAFF).

transition between the point of data arrival and the point of output transition, as reported in [21].

Based on Equation 4-33, the power consumption of the comparator (P_{comp}) is linearly proportional to the load capacitance (C_L) and its operating frequency.

4-3 Global Variation

The process, supply voltage and temperature have a global impact on the performance of the TDC. The global variations will affect the offset and gain of the TDC. Theoretically, the TDC has a linear function whose output is proportional to the timing difference between the reference (T_R) and the oscillator clocks (T_V). Due to the process, temperature and supply voltage variations (PVT), drift of the inverter delay cannot be avoided. The TDC gain describes the change of the output word per change of the input time interval. If there is a deviation of the first step position from the ideal value of T_{LSB}, the TDC has an offset error. This offset can cause the value of $\epsilon[k]$ to exceed the range, and the phase error will no longer be valid. To accommodate this condition, the additional 1 bit output (PHF_I (1)) on the Fractional Error Correction Block is required instead of only (PHF_F (W_F)), as depicted in Figure 3-6.

4-4 Local Variation

Mismatch in the threshold voltage V_T, device trans-conductance β, and drain current I_d will introduce local variations. This local variation will affect the TDC system's performance at two points, at the delay elements and at the sampling elements. These will directly affect the TDC linearity characteristics.

A microscopic view of the TDC's non-linearity is differential non-linearity (DNL), which is defined as the deviation of each step from its ideal value (T_{LSB}). Integral Non-Linearity

(INL) is a macroscopic view that describes the deviation of the step position from its ideal value, which is normalized to one T_{LSB}. This TDC non-linearity will introduce fractional spurs on the ADPLL system.

As in Equation 4-2, local variation introduces $\sigma_{tpd,mismatch}$ values to the inverter chain and $\sigma_{comp,mismatch}$ value to the comparator, based on Equation 4-28, these two variance values will produce a total mismatch variance ($\sigma_{total,mismatch}$) within the TDC, as in Equation 4-4. This has to be lower than 13 ps in order to produce an integral error with a value of less than one LSB [8] [15]. Based on the simulation results in Chapter 5 we meet this requirement.

4-5 Noise Effect on TDC Performance

4-5-1 Time Domain Quantization Noise Power

Similar to Analog-to-Digital Converter (ADC), the Time-to-Digital Converter (TDC) has time-domain quantization noise power as in Equation 4-34 [14].

$$\sigma_q^2 = \frac{t_{pd}^2}{12} \tag{4-34}$$

4-5-2 TDC Total Jitter

The TDC total jitter variance is the sum of the jitter variance of the inverter chain and comparator jitter variance. The maximum jitter will be at the end of the inverter chain (total number of inverter, N). By combining Equation 4-5 and 4-31, one has the following equation [14].

$$\sigma_{total,jitter}^2 = \sigma_{comp,jitter}^2 + \sigma_{total,tpd,jitter}^2 \tag{4-35}$$

$$\sigma_{total,jitter}^2 = \kappa \frac{kT\gamma}{C_c} \cdot \frac{4t_{pd}^2}{V_{DD}^2} + \left(\frac{N \cdot 4kT\gamma_N t_{pd}^2}{CV_{DD}(V_{DD} - V_t)} + \frac{N \cdot kTt_{pd}^2}{CV_{DD}^2} \right) \tag{4-36}$$

4-5-3 The Maximum Jitter of TDC

The maximum TDC jitter variance of the TDC system is limited by the required phase noise of the system. The in-band phase noise, as described in Equation 1-4, will be modified

as the equation below by adding TDC total jitter variance [36] where the inverter delay is equal to the TDC resolution ($t_{pd}^2 = \Delta t_{res}^2$).

$$\mathcal{L} = \left(\frac{2\pi}{T_V}\right)^2 \left(\frac{\Delta t_{res}^2}{12} + \sigma_{total,jitter}^2\right) \frac{1}{f_R} \tag{4-37}$$

The contribution of total jitter ($\sigma_{total,jitter}$) together with the TDC resolution on the phase noise should meet the requirements. Phase noise has the limit of -95 dBc/Hz, and based on the simulation results, as will be shown in Section 5-3-4, we meet this requirement.

4-6 TDC Power Consumption

The total power consumption of the TDC is the sum of the power consumption of the inverter chain and comparators. It can be mathematically described as the equations below [14].

$$P_{TDC} = P_{inv} + P_{comp} \tag{4-38}$$

$$P_{TDC} = N \cdot C_{out} V_{DD}^2 f + N \cdot \left(C_L V_{thp} + C_L V_{eff} \ln\left(\frac{1}{V_{thp}} \sqrt{\frac{I_o}{2\beta}} \frac{\Delta V_{out}}{\Delta V_{in}}\right)\right) V_{DD} f_s \tag{4-39}$$

In [14] and [35], it can be assumed that the lowest or the minimum power consumption is achieved when the jitter power is equal to the time-domain quantization noise power, as in Equation 4-34, thus the following relationships hold.

$$\sigma_{total,jitter}^2 = \sigma_q^2 \tag{4-40}$$

$$\left(\kappa \frac{kT\gamma}{C_c} \cdot \frac{4}{V_{DD}^2} + \frac{N \cdot 4kT\gamma_N}{CV_{DD}(V_{DD} - V_t)} + \frac{N \cdot kT}{CV_{DD}^2}\right) t_{pd}^2 = \frac{t_{pd}^2}{12} \tag{4-41}$$

$$\frac{\sigma_{total,jitter}^2}{t_{pd}^2} = \frac{1}{12} \tag{4-42}$$

Chapter 5

TDC Layout Design, Simulation, and Performance

5-1 The TDC Layout Design

The required number of inverter chains or TDC cells can be calculated by using Equation 3-8. With the lowest frequency of 3 GHz, see Figure 3-1 and the lowest inverter delay of 10.50 ps approximately, the number of cells should be 32 and is equal to 2^5. Some margin is provided to guarantee the system will still operate properly under the worst case conditions. Therefore the total number is 40 cells.

Working on this new technology is very interesting as it will introduce more phenomena than the old one. In the modern technology, in terms of speed, while the speed of the transistor is very fast, the parasitic capacitance is a dominant factor. Here, an inexperienced engineer will take a very long time to deal with the layout in order to meet specifications. Moreover, all corners and all operating temperatures are considered in this design, hence the physical factors are important; therefore an iterative layout design must be carried out. Some trade-off should be considered. In this design, 15 versions of layout have so far been designed to achieve the specification.

In this thesis, the design will be based on the basic information found in the PDK manuals. During the layout design, one should consider WPE (Well Proximity Effects) that alter the threshold voltage, metal routing, and contacts that significantly introduce capacitances. As has been previously explained, iterative design processes have been conducted to meet the design specification. Finally, the TDC resolution of 12.55 ps is achieved for the worst case condition. A voltage drop of only 6 mV can be achieved on the power supply path by using a metal width of 3 μm.

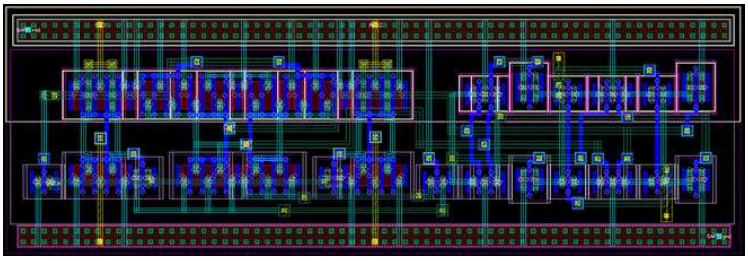

Figure 5-1: Layout of 1 TDC cell.

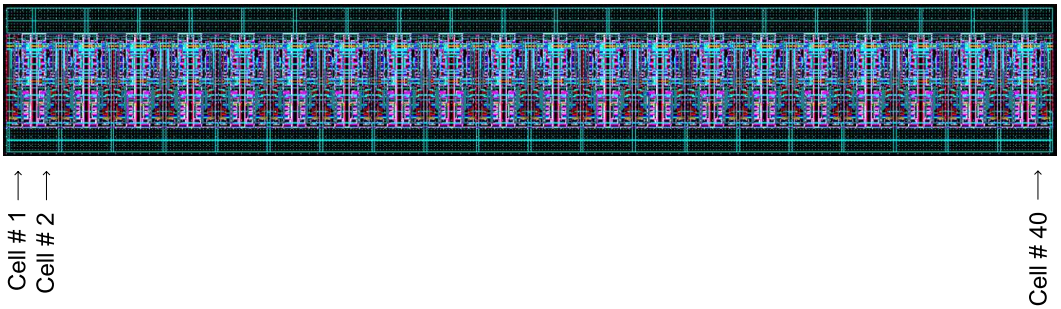

Figure 5-2: TDC core layout.

With regards to the layout design, one cell of the TDC is designed first. It consists of two inputs of inverter delay line and one Sense Amplifier Flip-Flip (SAFF). As shown in Figure 5-1, one cell of the TDC occupies a very small area of only 11 $\times$ 3.7 μm^2. Once one cell is available the TDC core, which contains 40 cells, can be built immediately. Full characterization is conducted on the 40 cells. Figure 5-2 shows the TDC core layout containing 40 cells with total area of only 125 $\times$ 11 μm^2, which is very compact.

5-2 Simulation Results

5-2-1 Inverter Delay Elemet

Delay Element Mismatch

The size of the inverter delay element identifies the driving capability and is also determined by the size of the input capacitance of the comparator to provide a certain propagation delay. The trade-off between propagation delay and power consumption needs to be considered. The chosen size of the inverter delay element produces the average propagation delay (t_{pd}) that varies from 10.84 ps to 12.55 ps over all corners and operating temperatures. The delay element mismatch can be obtained by running a Monte Carlo simulation within the Cadence environment. As depicted in Figure 5-3, it produces a propagation delay of 11.46 ps and around 10 fs of standard deviation. This TDC system has 40 delay elements, which

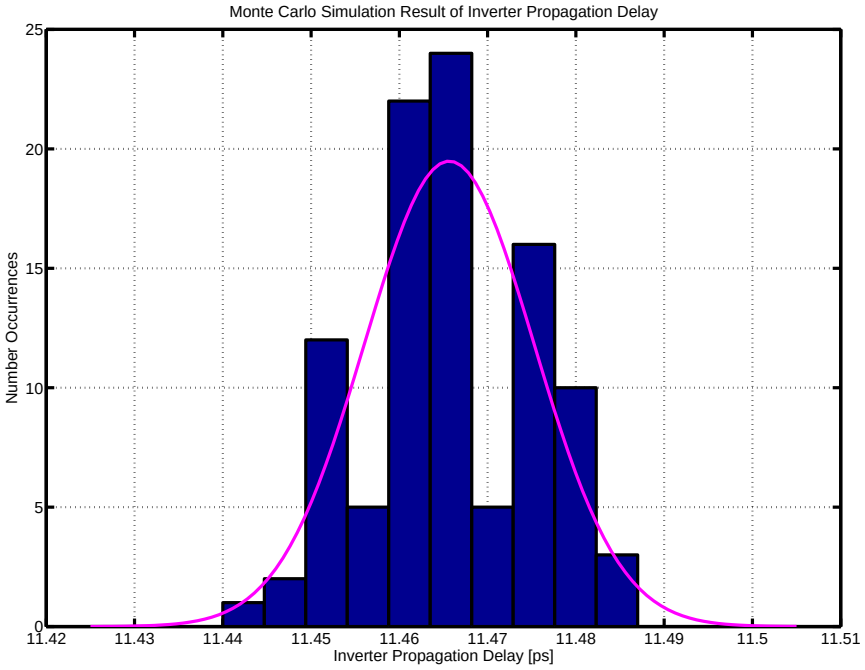

Figure 5-3: Delay element mismatch.

have standard deviation varying from around 9 fs to 12 fs. The delay mismatch can be reduced by increasing the transistor size. However, the power consumption of the inverter is the limitation.

If the standard deviation value of the inverter delay mismatch ($\sigma_{tpd,mis}$) is equal to 12 fs and the standard deviation value of the comparator offset mismatch ($\sigma_{comp,mismatch}$), taken from Section 5-2-2, is 360.05 fs, then by combining those values in Equation 4-4 it is found that the total mismatch variance of the TDC is around 362 fs, which is lower than the limit of 13 ps.

Jitter of an Inverter Delay Element

The presence of voltage noise at the point where the threshold is crossed within an inverter will introduce jitter as described by Equation 4-5. This type of characteristic is measured by the Cadence Tool as the edge-to-edge timing jitter (J_{EE}), or it can also be called the aperture or absolute jitter. Jitter due to the inverter delay element and due to comparator noise will be added together and will contribute to the phase noise based on Equation 4-37.

This jitter can be lowered by increasing the size of the transistor. However, the trade-off between jitter and power consumption is also applied here. In this design, in order to measure the jitter in the Cadence software, one should set-up a PSS and PNoise analysis. The first step is to run a PSS (Periodic Steady State) analysis to determine the periodic

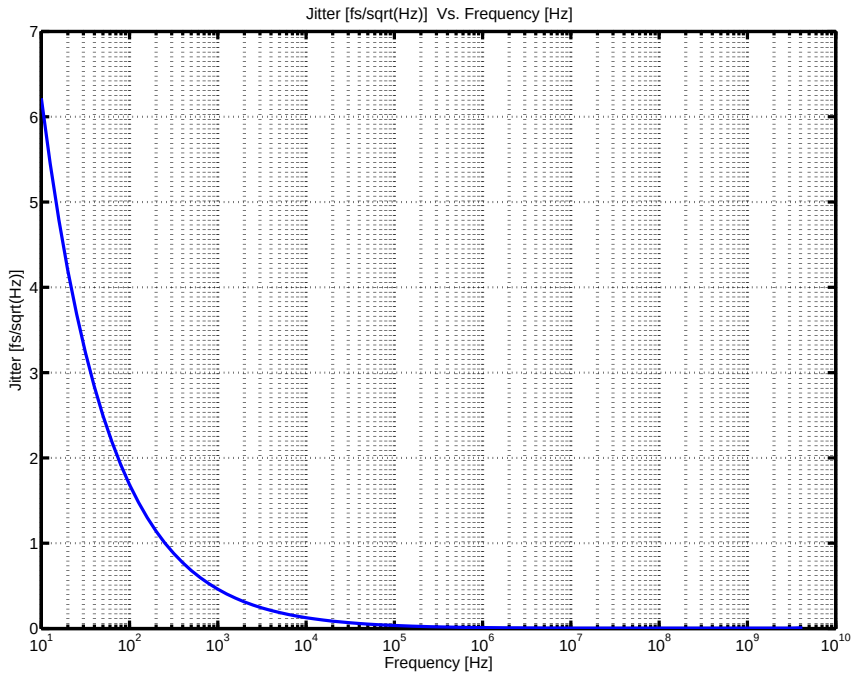

Figure 5-4: Inverter chain jitter.

trajectory or large signal solution. Subsequently, the PNoise (Periodic Noise) analysis is run to calculate the phase noise, and finally to ascertain the jitter [37]. From Figure 5-4, one should integrate the edge-to-edge timing jitter (J_{EE}) within the range of the TDC operating frequencies, and here the maximum frequency of CKV is 4.25 GHz. Based on the simulation from 10 Hz to 4.25 GHz, it was found to be in the range of 320.98 fs up to 340.91 fs for the inverter chain (40 inverters). These values are for the best case and worst case conditions.

The inverter chain jitter and the comparator jitter will produce the total jitter. This total jitter will contribute to the phase noise as in Equation 4-37. In this case, the inverter chain jitter of 340.91 fs and the comparator jitter of 19.52 fs will be added and evaluated in Equation 4-37, and will result in a phase noise better than the limit of -95 dBc/Hz.

5-2-2 Sense Amplifier Flip Flop Performance

The comparator's analog performance in terms of offset, noise, and metastability are independent of the other TDC building blocks. The comparator's design can be used as a starting point when designing a TDC. The input capacitance of the comparator should be minimized since it will be connected to a single stage of the inverter delay element. It will set the required driving capability of the inverter delay element and its power consumption. With the help of a Monte Carlo simulation of the Cadence software, the transistors' sizes

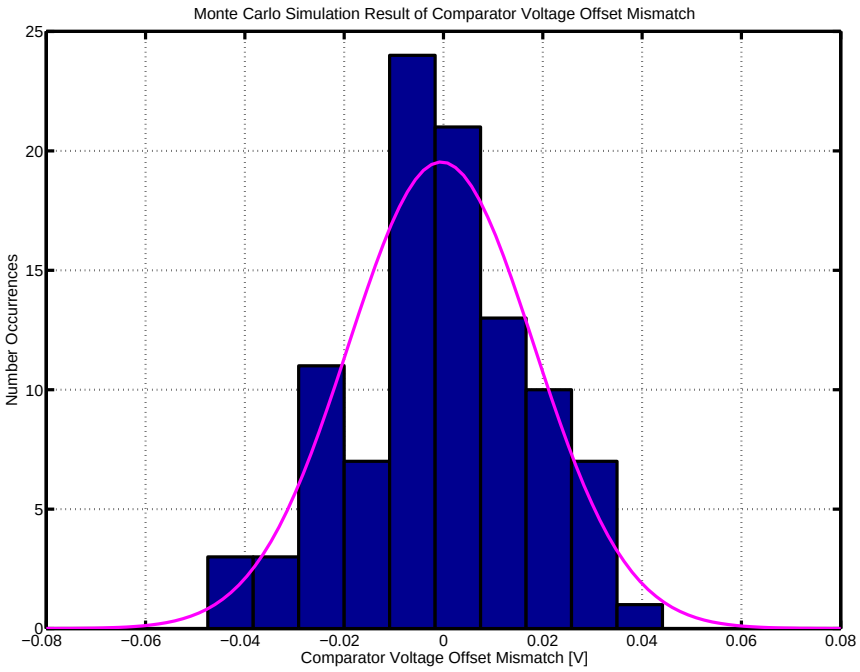

Figure 5-5: Comparator voltage offset mismatch.

for the comparator are designed. This type of simulation is time consuming; therefore the number of reasonable loopings should be considered.

Simulation of Mismatch Voltage Offset

Reference [38] presents the testing method that results in a voltage offset for the high-speed regenerative comparators, where the comparator being tested is configured within a negative feedback loop containing an integrator.

A histogram of the simulated offset is shown in Figure 5-5. It shows the simulation results of the voltage offset mismatch. It has -0.46431 mV and 18.7mV for the mean and standard deviation, respectively. Moreover, in the time domain, based on [31, 14, 32, 15], it has a mean of -8.9380 fs and a standard deviation of 360.05 fs, as depicted in Figure 5-7.

As with the previous calculation result in the previous section, with a standard deviation value of the comparator offset mismatch ($\sigma_{comp,mismatch}$) of 360.05 fs and a standard deviation value of inverter delay mismatch ($\sigma_{tpd,mis}$) of 12 fs then, based on Equation 4-4, the total mismatch variance of the TDC is around 362 fs, which is lower than the limit of 13 ps.

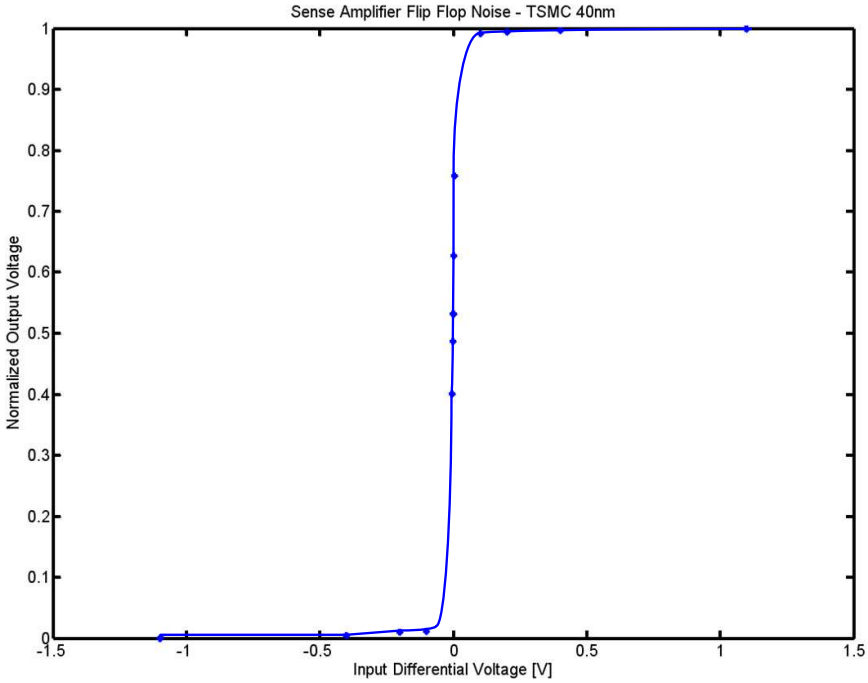

Figure 5-6: Normalized output voltage vs. input differential voltage.

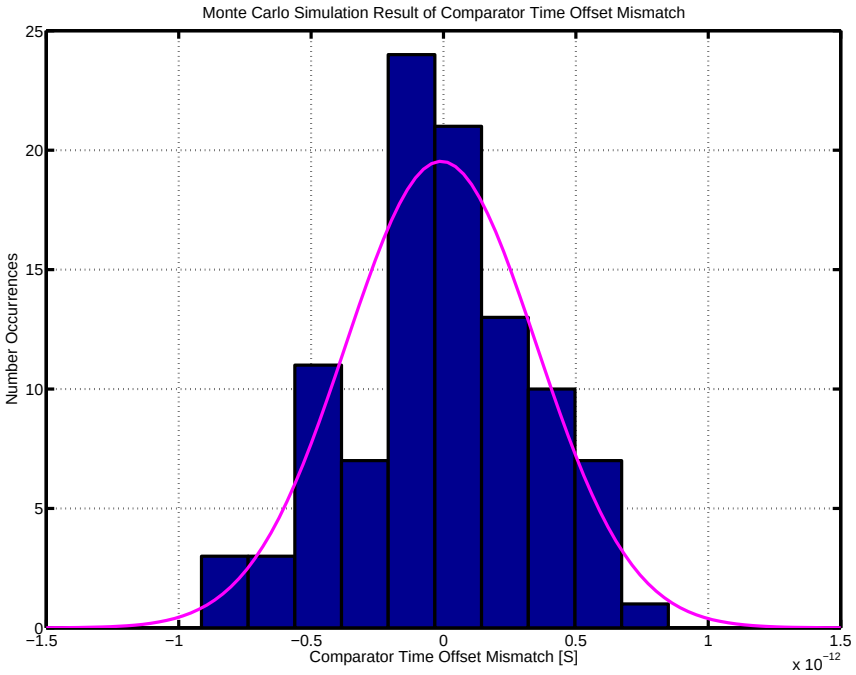

Figure 5-7: Comparator time offset mismatch.

Input-referred Noise

In [33, 34], the input-referred noise measurement method will be based on the variation of the output probability as a function of the input voltage. This means that if the input noise v_n is a white Gaussian process, therefore the probability of getting 1 is as a function of the differential input as depicted in Figure 5-6.

Figure 5-6 shows input differential voltage vs. normalized output voltage. The standard deviation is around 1 mV or approximately 19.52 fs with the slope $s = V_{DD}/2t_d$ [31, 14, 32, 15], which is very small compared to the contribution of the inverter chain.

Metastability of the Sense Amplifier Flip-Flop

Care should be taken in this metastability design, since a typical flip-flop for high-speed digital designs has a metastability characteristic of resolution window more than several inverter delays, which is not allowed in this application.

The method to measure the metastability window is presented in Gabara's paper [25]. Based on this paper, we obtained Figure 5-8 and Figure 5-9 for the metastability window testing results before the layout was determined. For post-layout simulation results, see Figure 5-10 and Figure 5-11. These figures show that the metastability window is very small, with a resolution time of 29 ns, the metastability window is around 2.417×10^{-254} seconds for the worst case scenario of -40°C. This result is much smaller than the limit as explained in section 4-2-2. Hence, there are no bubbles in the TDC code. The limitation on the TDC resolution is now only the inverter delay.

5-3 TDC Performance

5-3-1 TDC Resolution

Figure 5-12 shows the resolution of TDC at 1.2 V of power supply but at different corners and temperatures. The designed TDC is intended to operate between -40°C to +85°C. At a typical corner and at room temperature, the TDC resolution is around 11.66 ps while under the worst case condition it is around 12.55 ps, which is still within the specification limit.

As predicted by Equation 4-1, the TDC delay is reduced by increasing the power supply. The simulation results are shown in Figure 5-13.

5-3-2 Offset Error

The first step of an ideal TDC will occur at the position of T_{INV}. If the first step and the complete TDC step characteristics are shifted along the time axis, this means that an offset

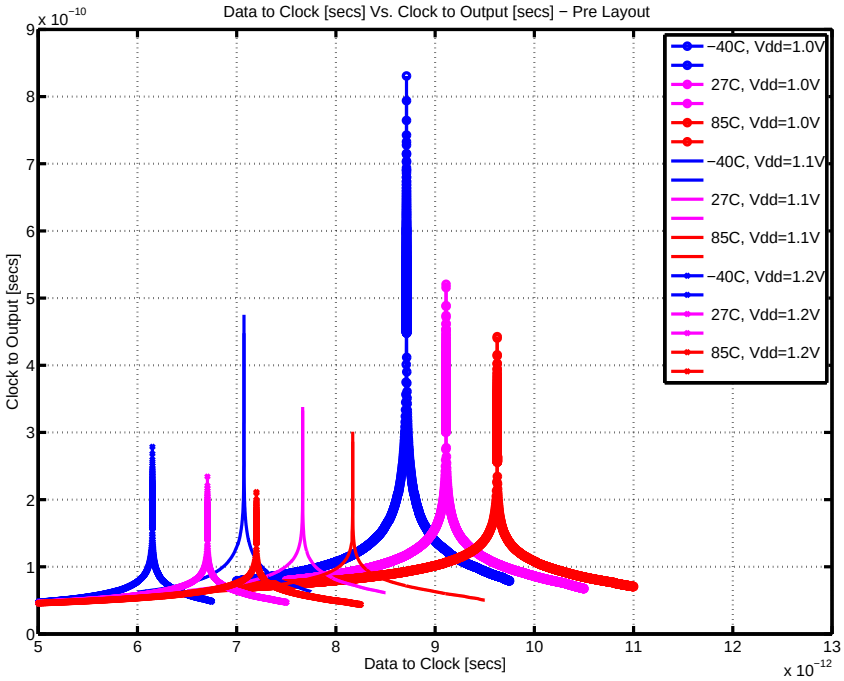

Figure 5-8: Metastability curve of sense amplifier flip-flop - pre layout.

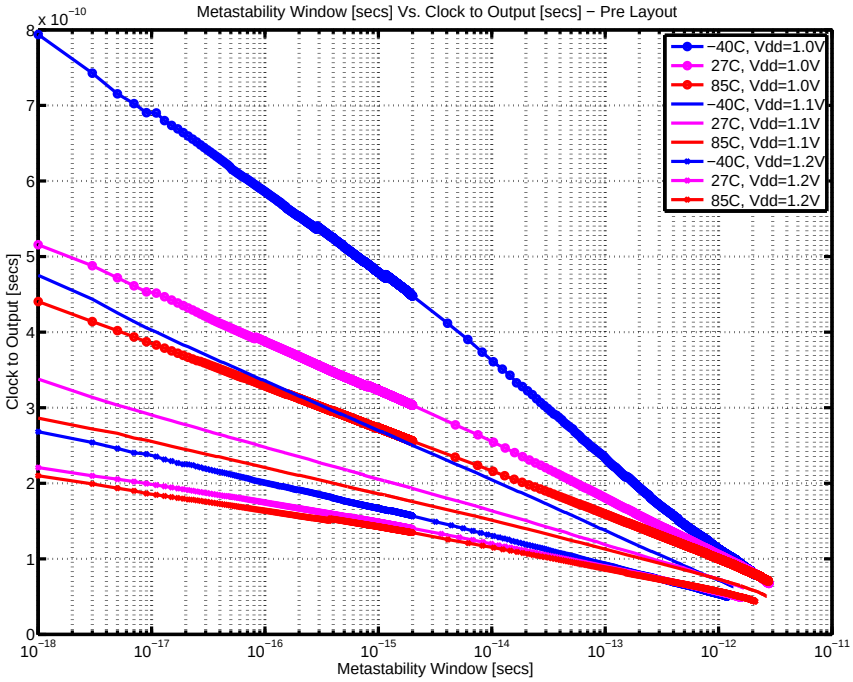

Figure 5-9: Metastability window of sense amplifier flip-flop - pre layout.

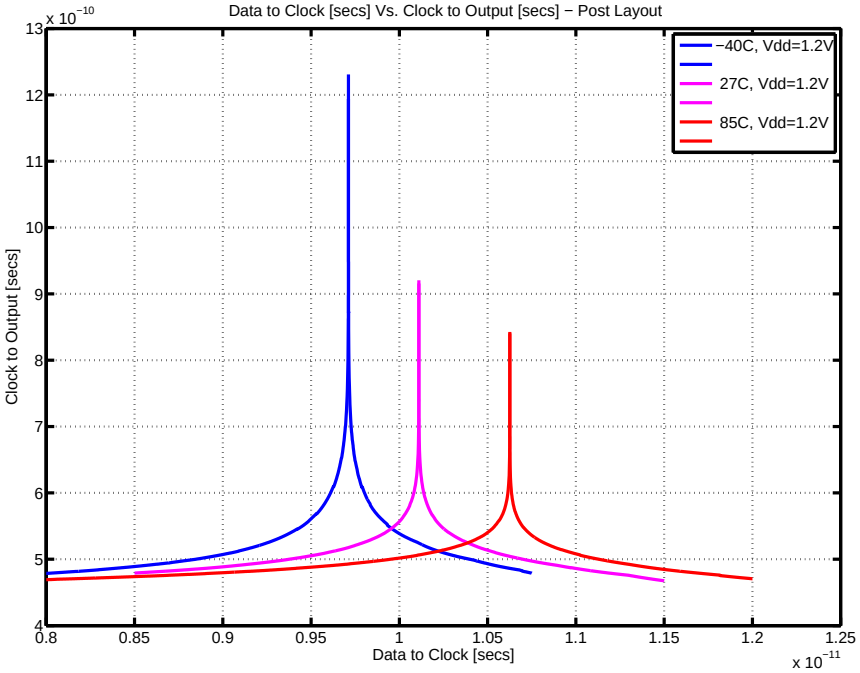

Figure 5-10: Metastability curve of sense amplifier flip-flop - post layout.

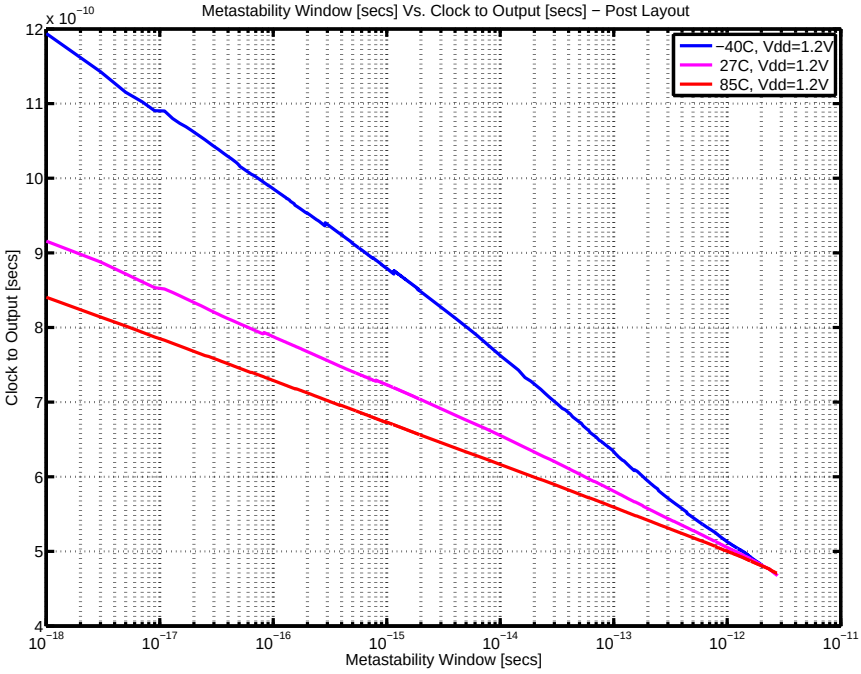

Figure 5-11: Metastability window of sense amplifier flip-flop - post layout.

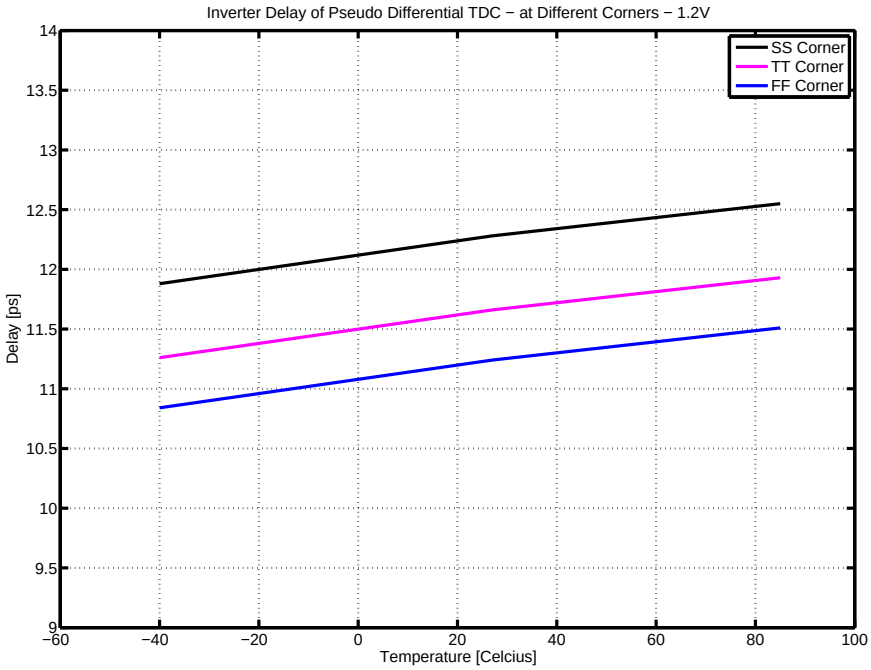

Figure 5-12: Average TDC delay resolution vs. operating temperature.

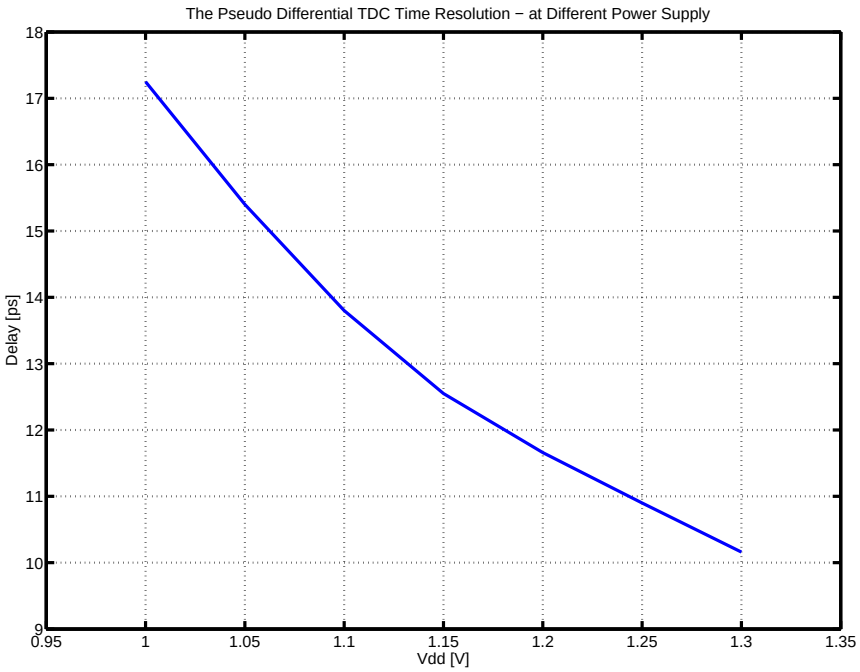

Figure 5-13: The TDC resolution vs. power supply.

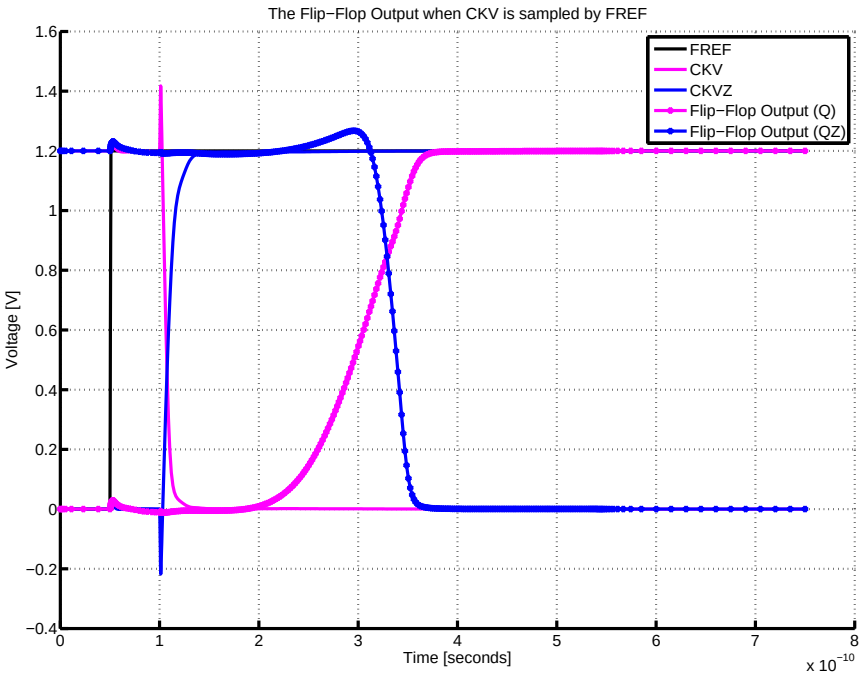

Figure 5-14: Output of flip-flop.

error ($offset$) occurs. The value of $\epsilon[k]$ will exceed the range due to this offset, and finally the phase error will no longer be valid. Therefore, in order to overcome this condition the additional 1 bit output (PHF_I (1)) on the Fractional Error Correction Block is required instead of only (PHF_F (W_F)), as depicted in Figure 3-6.

5-3-3 TDC Linearity

The linearity of the TDC has been measured in terms of differential-non-linearity (DNL) and integral-non-linearity (INL). The measured INL and the DNL were obtained from the circuit simulation of Cadence. This simulation took a long time in transient analysis by sweeping the two input clocks. The TDC transfer function is shown in Figure 5-15, and Figure 5-16 shows the test results of both DNL and INL with values below 0.4 least significant bit (LSB), with mismatch included. The result in Figure 5-15 and Figure 5-16 could not be drawn directly from Cadence, further post-processing with MATLAB is required from the output result of the flip-flop. Figure 5-14 shows how the CKV signal is sampled by an FREF signal and the output of a flip-flop is updated.

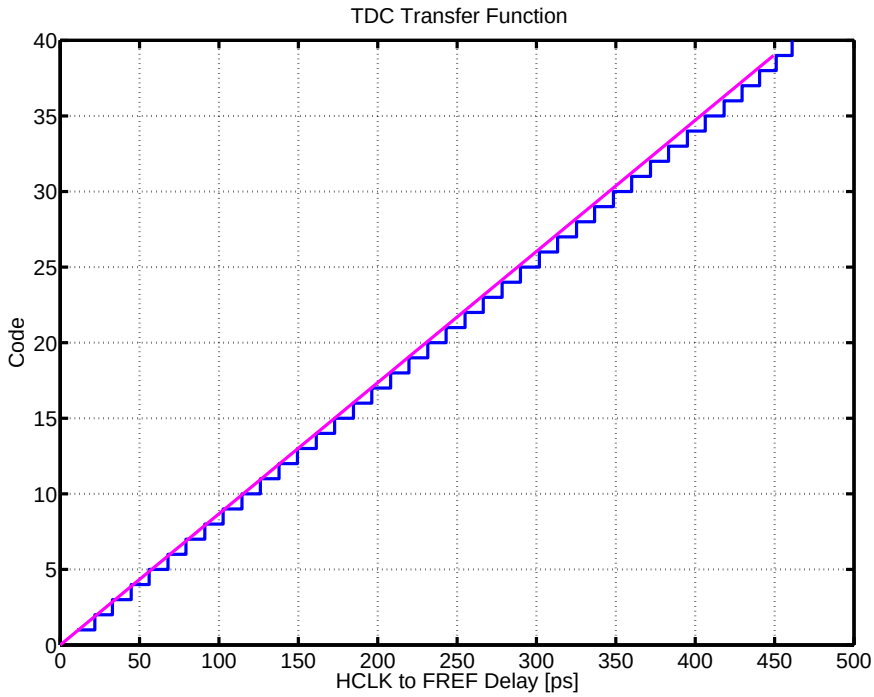

Figure 5-15: TDC transfer function.

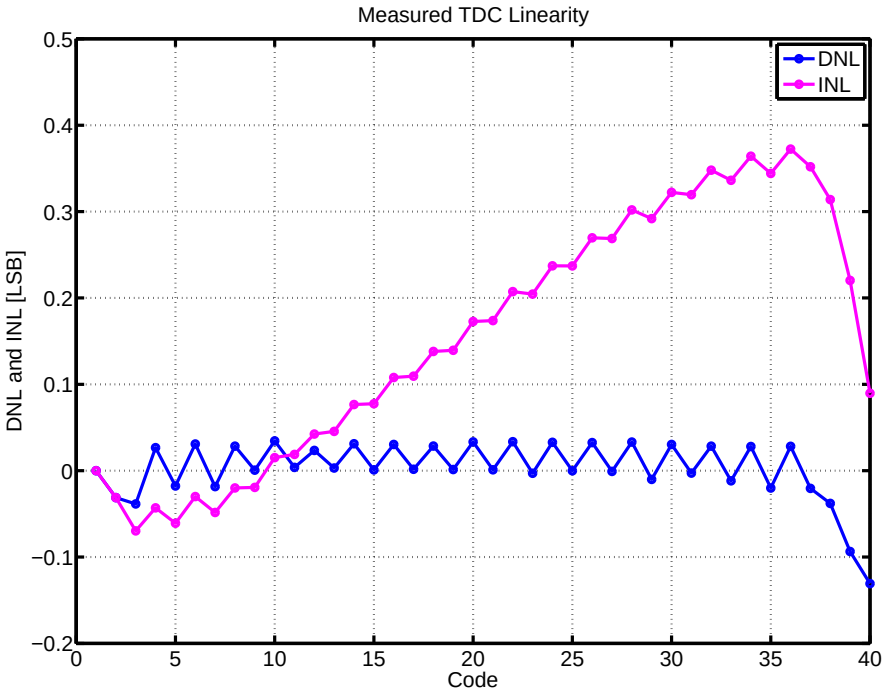

Figure 5-16: TDC linearity.

5-3-4 Phase Noise

The TDC conversion process is conducted in the time domain, therefore the worst case of conversion occurs at a full range input, and the signal must travel through the end of the delay line. Based on Equation 4-37, the in-band phase noise is derived by substituting the propagation delay of the delay element and the total jitter at the final stage and results in the following equation [36, 39]:

$$\mathcal{L} = \left(\frac{2\pi}{T_V}\right)^2 \left(\frac{\Delta t_{res}^2}{12} + \sigma_{total,jitter}^2\right) \frac{1}{f_R} \tag{5-1}$$

By using the above equation, with a TDC resolution of 12.55 ps at the worst case and with total jitter ($\sigma_{total,jitter}$) of 497.675 fs as Equation 4-35, the in-band phase noise is still within the limit of -95 dBc/Hz.

5-3-5 Power Consumption

The whole part of TDC has been simulated to determine power consumption. The power consumption is 2.99 mW, and after dynamic clock gating is applied it will be 0.78 mW. The testing process was carried out for a 1.2 V supply, 33.868 MHz frequency reference clock FREF and 4.25 GHz frequency of CKV. If one compares this with the previous work in [4], this power consumption is lower. Also considering the testing conditions, this TDC is tested at a higher operating frequency compared to [4], therefore this power consumption is much better.

The lower the frequency, the lower the power consumption we can achieve, as expected by Equation 4-39. Figure 5-17 below shows that at the highest frequency of CKV or at 4.25 GHz, the power consumption is around 2.99 mW and the power consumption is around 2.14 mW at 3 GHz of CKV frequency.

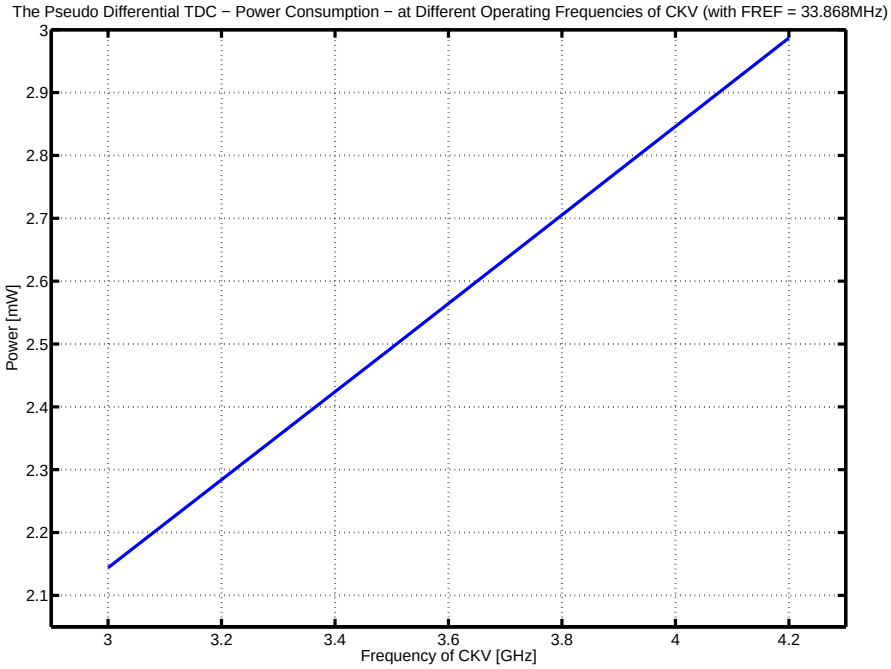

Figure 5-17: The TDC power consumption at different CKV frequencies.

Chapter 6

Conclusion

6-1 Conclusion

This thesis has presented a TDC system design, TDC layout implementation, and TDC system simulation for a WiMAX ADPLL application for state-of-the-art 40-nm CMOS technology. This work is one sub-topic out of four in the WiMAX ADPLL project.

The pseudo-differential TDC architecture is chosen in this design to achieve the WiMAX requirements. The TDC core contains inverters and sense amplifier flip-flops. This architecture has a very simple method in calibration process at the next step.

With a 1.2 V power supply, 33.868 MHz frequency reference clock FREF and 4.25 GHz frequency of CKV, the power consumption is around 2.99 mW. In addition to the low power consumption, the TDC core area in silicon is very small at only 125×11 μm^2. The simulated TDC resolution is around 10.84 ps - 12.55 ps and the linearity is lower than 0.4 LSB. Under worst case conditions, the TDC resolution of 12.55 ps is achieved and it meets the WiMAX ADPLL system requirements, the in-band phase noise of -95 dBc/Hz.

6-2 Future Work

Compared to the previous design in [4], the power consumption of 2.99 mW is lower. The previous work shows a power consumption of 6.9 mW. A power management scheme through dynamic clock gating could be applied to further reduce power consumption as has been done in [4]. This method can reduce consumption by up to 74%. It means that with the current power consumption of 2.99 mW, after the dynamic clock gating applied it could be 0.78 mW. However, this research is very limited by time, but the clock gating circuit could be easily implemented in the future.

With CMOS technology scaling, it is expected that in the future there will be faster transistors. Subsequently, the TDC resolution is improved. However, the parasitic capacitances should be carefully considered. In this research, it is found that the parasitic capacitance is the dominant factor; therefore in future design processes, parasitic capacitances and other physical phenomena such as Well Proximity Effects (WPE), should be thoroughly investigated.

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