DotFETs:
MOSFETs strained by a Single SiGe Dot
in a Low-Temperature ELA Technology

PROEFSCHRIFT

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Dedico este trabalho a minha esposa Andréa e minha filha Stephanie

Contents

Chapter 1

Introduction

The work that is the basis of this thesis was performed in the context of the European Sixth Framework Program FP6 project "Disposable Dot Field Effect Transistor for High Speed Si Integrated Circuits", referred to as the D-DotFET project. This was a very challenging project that started in October 2005 with the goal of realizing strain-enhanced mobility in CMOS (Complementary-Metal-Oxide-Semiconductor) transistors by transferring strain from a self-assembled germanium dot to the channel of a transistor fabricated above the dot. If the strain transfer from the dot to the channel could be fixed by other materials early in the processing, the dot could then be removed at the beginning of the device processing. The idea was thus to dispose of the Ge dot underneath the channel after the gate processing so that the gate-stack could serve to stabilize the channel-bridge and maintain the strain induced in the channel silicon by the Ge dot. A sketch of what the final structure could look like is given in Figure1.1.

To make the D-DotFET concept attractive for CMOS production, research was performed in several areas to assure that the stringent requirements on uniformity, reproducibility and reliability could feasibly be met. Firstly, the skill of growing silicon germanium (SiGe) dots with the necessarily high Ge content, uniformity and reproducibility was brought to a high level of perfection [1-2]. Secondly, the strain of both bare and overgrown dots was extensively analyzed both experimentally and theoretically [3-9]. Thirdly, the strain that could be transferred to the channel of a Metal-Oxide-Semiconductor Field Effect transistor (MOSFET) was evaluated in terms of mobility enhancement via device simulations [10-16], and lastly, the actual integration of dots was demonstrated in a low-complexity n-MOSFET research process that was specially tailored to this application. The latter is the topic of this thesis.

With respect to strain transfer, the advantage of using a SiGe dot was scalability to as low as 10 nm gate dimensions, which is not obvious for currently used methods, some of which are discussed in the following Sections. Moreover, the D-DotFET structure itself offers several advantages for the electrostatic and electrothermal behaviour of MOS devices. For example, Silicon-on-Insulator (SOI) devices with fully-depleted channel are a solution for short-channel effects but the insulating oxide beneath the device introduces a thermal management issue. This problem is solved in Silicon-on-Nothing (SON) devices because the insulating region is then only found under the gate while the source/drain regions are still anchored to the thermally conductive bulk silicon. A schematic cross sections comparing a standard n-MOSFET, a SOI n-MOSFET, and a SON n-MOSFET are shown in Figure 1.2. The D-DotFET resembles the SON transistor but with the added advantage of strain-

enhanced device gain and speed. Thus the D-DotFET combines four aspired features: strain enhanced performance, scalability to future ~ 10 nm generations, suppression of short-channel effects, and good heat dissipation.

The enormous success of present-day strain-enhancement schemes in industry lends itself to the fact that these schemes could be almost directly implemented in running CMOS processes. Hence, in the first year of the D-DotFET project in Delft the work was concentrated on establishing an industry compatible flowchart. This work also received active support from the project partner STMicroelectronics, where the SON process was invented and in development. The resulting process flows, which will be described in Section 1.5.1 of this chapter, are also very closely related to the SON flow. They take advantage from the fact that the SiGe dot is removed early in the process so that the thermal budget of the standard CMOS process can be implemented after dot removal. Then the substrate with the strained channel can be treated almost as a normal substrate and the standard process-steps, including ones at high-temperature, could be transferred directly to the dot situation.

The contributions to the D-DotFET project that are described in this thesis were carried out after the project had already been running for one year. As it happened, in the second year of the project the original D-DotFET team left Dimes (Delft Institute of Microsystems and Nanoelectronics), and the job of realizing a MOS transistor on the SiGe dots was transferred to the Silicon Device Integration group within which this thesis work was performed. After serious evaluation, it became clear that the Dimes cleanrooms were not equipped to set up a state-of-the-art CMOS process. On the other hand, the available expertise and equipment was suitable for running a more advanced process, where excimer laser

annealing could be implemented to replace the standard rapid thermal annealing and a metal gate could replace the standard polysilicon gate. The biggest issue was the patterning of ~ 100 nm gate features, which was not possible with the Dimes waferstepper but instead had to be performed by e-beaming by the project partner Forschungszentrum Jülich (FZ Jülich). This was a both time-and cost-consuming step. Therefore, to avoid as many nanoscale lithography steps as possible, geometry with large source-drain contacting areas was devised so that only one step, the ~ 100 nm gate definition itself, needed to be e-beamed.

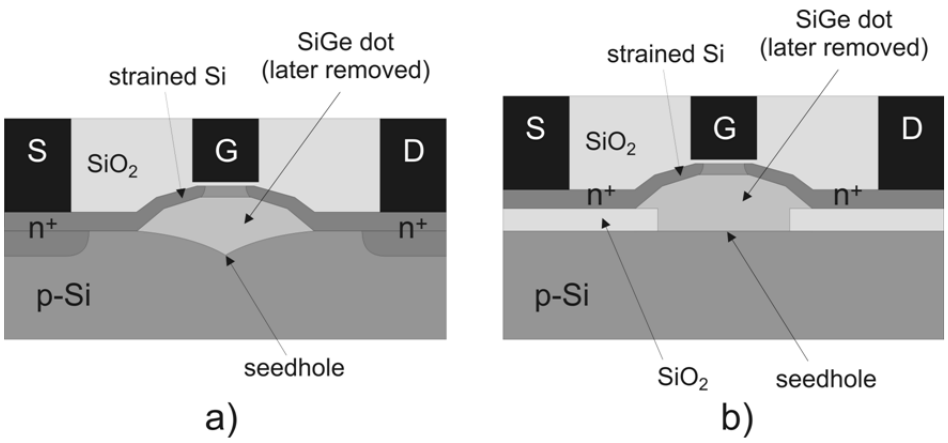


Figure 1.1: Schematic cross sections of possible DotFET structures for a SiGe dot grown (a) by MBE (Molecular Beam Epitaxy) in seedholes etched directly in the Si and (b) by LPCVD (Low Pressure Chemical Vapor Deposition) in seedholes formed by etching windows in oxide. In both cases the gate is placed in the middle of the dot where the strain is high. The dot can be removed at some stage of the processing.

Another very critical step in the D-DotFET processing is the removal of the dot. Since the goal was in first instance to verify the strain-enhanced gain induced by the dot, it was decided to significantly simplify the transistor processing by retaining the dot throughout. Therefore, a "DotFET" rather than a "D-DotFET" was fabricated as shown in Figure 1.3. This meant that after the dot formation only low-temperature processing steps could be implemented in order to avoid intermixing of Si and Ge and consequent strain relaxation. This was realized in a n-MOSFET process where the temperature was kept below 400 °C after epitaxy by using low-temperature gate dielectrics and a metal gate self-aligned to implanted and laser annealed source/drain regions. This processing scheme is in itself an interesting research topic in view of the drive towards future CMOS generations with high-k dielectrics and metal gates that require similar low-temperature processing. Therefore, the two most important results of this thesis are the demonstration of the applicability of (1) SiGe dots as stressor material and (2) full-melt high-power laser annealing as a technique for lowering the source/drain series resistance in a manner self-aligned to the gate.

In the following sections of this introduction the background knowledge for understanding downscaling and strain-enhanced MOS performance along with the use of stressor materials and techniques is given. Moreover, a description is given of the work performed by the other D-DotFET project partners. Globally, the work within the project was divided as follows:

- **Forschungszentrum** (FZ Jülich **-** Germany): epitaxial Si/SiGe and dot growth by MBE and CVD (Chemical Vapor Deposition), e-beaming for transistior processing;
- **Leibniz Institute for Solid State and Materials Research** (IFW Dresden - Germany): template assisted SiGe dot growth;
- **Johannes Kepler University** (Linz - Austria): epitaxial Si/SiGe and dot growth by MBE and SiGe dot material analysis;
- **University of Milano** (Bicocca - Italy): modeling of stress in SiGe dots;
- **Technical University Wien** (Austria): strained device simulations;
- **STMicroelectronics** (Grenoble - France): technology advisor, experts in SON processing;
- **Delft University of Technology** (Dimes, The Netherlands): process flowcharts, mask design, device fabrication and electric characterization.

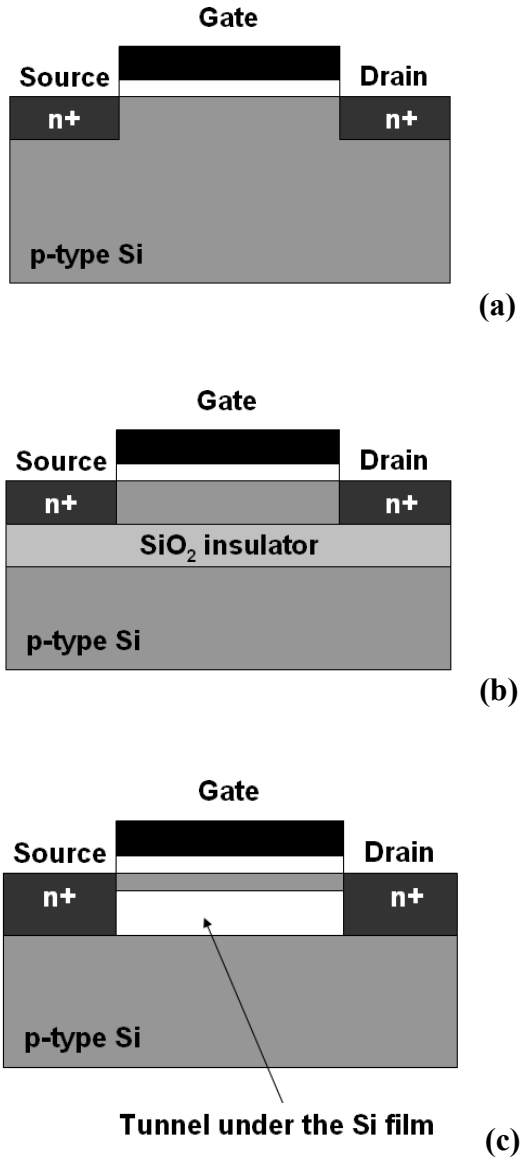
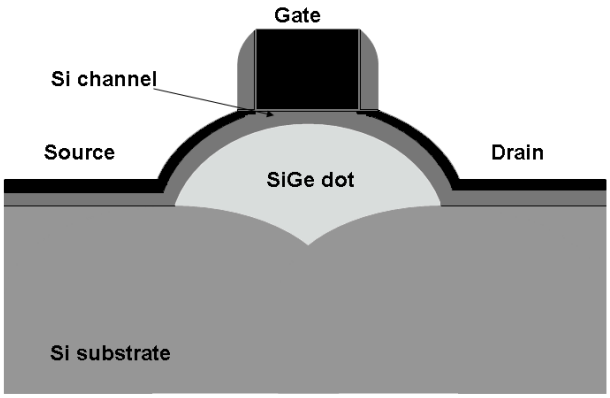
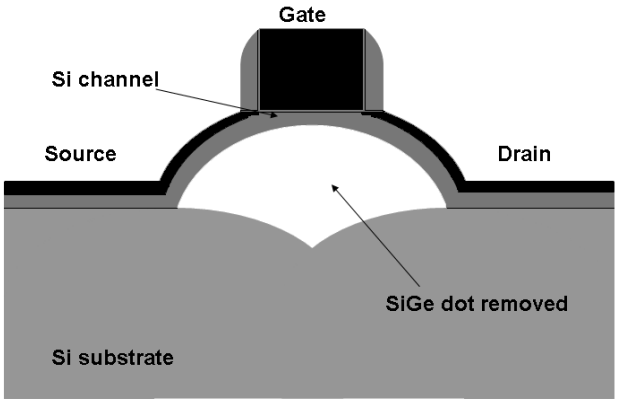


Figure 1.2: Schematic cross sections comparing the final structures of (a) a standard n-MOSFET, (b) a SOI n-MOSFET, and (c) a SON n-MOSFET.



(a)



(b)

Figure 1.3: Schematic cross sections of the (a) DotFET and (b) D-DotFET structures.

1.1 CMOS downscaling and performance enhancement

The basic structure of conventional n-MOSFET and p-MOSFET devices is given in Figure 1.4, and both p-channel and n-channel MOSFETs in a complementary circuit is given in Figure 1.5 [17]. The CMOS is a technology used for a wide variety of analog and digital circuits. Shallow Trench Isolation (STI) is generally used on new CMOS process technology to isolate the devices in substitution of Local Oxidation of Silicon (LOCOS). The Figure 1.5 shows the cross-section of the CMOS technology where the p-channel and n-channel MOS are fabricated on the same substrate.

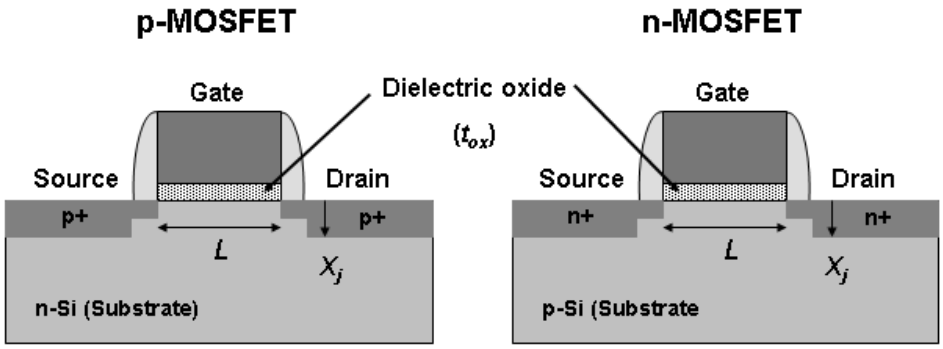


Figure 1.4: Schematic diagram of an n-MOSFET (a) and p-MOSFET (b).

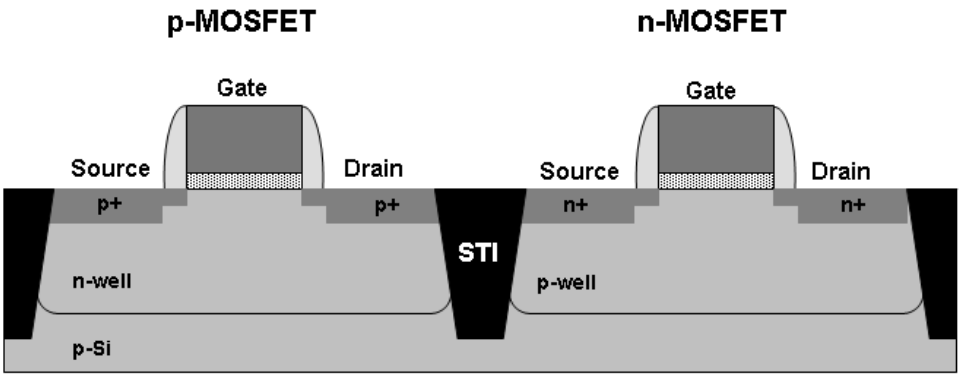


Figure 1.5: Cross-section of the CMOS technology where the p-channel and n-channel MOS are fabricated on the same substrate. Shallow-trench isolation is used on new CMOS process technology to isolate the devices.

The International Technology Roadmap for Semiconductors (ITRS), developed by the semiconductor industry, clearly reflects the strong desire of the industry to continue CMOS scaling in the future, preferably according to Moore`s Law, that in 1965 predicted that the number of transistors on a chip would double about every two years [18]. This trend is for example seen in Figure 1.6 where the evolution is displayed for Intel® processors and the associated technology node.

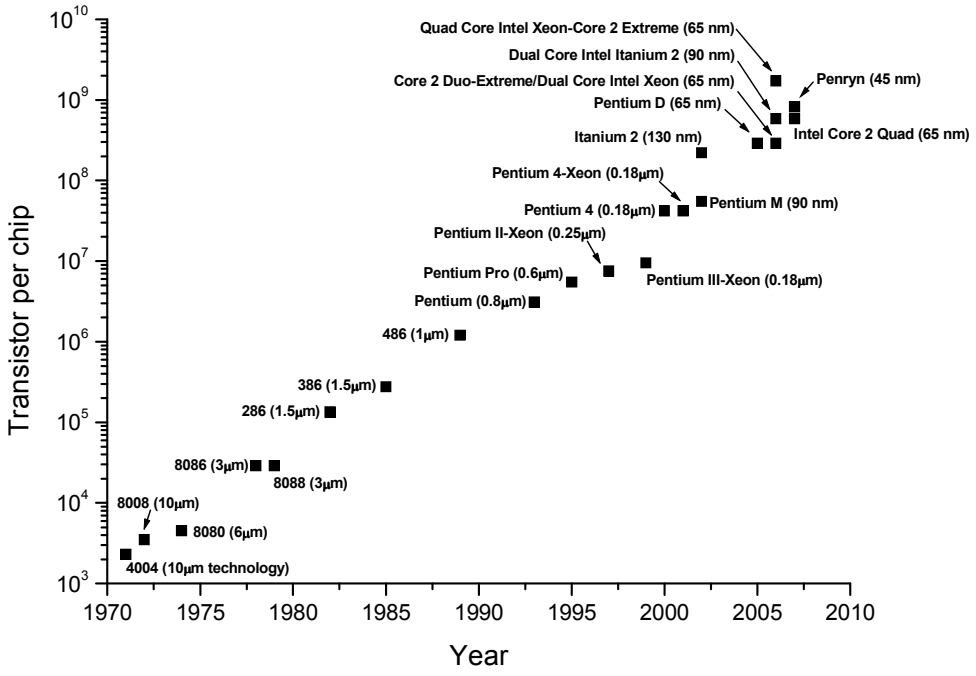


Figure 1.6: The evolution of the Intel® processors and the associated technology node as an example of the trend set by Moore`s Law [19].

Until today, devices scaling is still the most important way to achieve higher performance, although the technological difficulties are becoming extremely challenging. For example, the ITRS 2009 roadmap predicted a physical gate length of 15 nm in 2015 and contact junction depth (*Xj*) of 19.8 nm as shown in Table 1.1.

Table 1.1: CMOS device parameters quoted in the International Technology Roadmap for Semiconductors 2009 [20].

Year of production	**2009**	**2010**	**2011**	**2012**	**2013**	**2014**	**2015**
Physical gate length (nm)	27	24	22	20	18	17	15
Physical EOT (nm)	1	0.95	0.88	0.75	0.65	0.55	0.53
Contact *Xj* (nm)	35.2	32	29	26.7	24.7	22	19.8
Drain extension *Xj* (nm)	13	12	10.5	10	9.5	8.7	8

However, to satisfy the ITRS specifications and continue the CMOS device scaling, it has been obvious that new materials and technologies must be introduced. This is summarized in Figure 1.7, in which the challenges for planar technology are indicated [21]. The following quotes from the ITRS 2009 roadmap also underline this picture with focus on the two main challenges that are treated in this thesis, strain-enhanced performance and ultrashallow S/D fabrication:

"Channel strain engineering to increase mobility was introduced to manufacturing several years ago and is an integral part of MOSFET transistor scaling now and in the future. Continued improvement in strain engineering and application to new device structures is identified as an Front End Processes difficult challenge."

"The introduction of new materials is also expected to impose added challenges to the methods used to dope and activate silicon. Series resistance is critical in the near term and needs to be addressed to achieve the goals through 2015. … In addition to the scaling imposed need for producing very shallow highly activated junctions, the limited thermal stability of most high-κ materials is expected to place new boundaries on thermal budgets associated with dopant activation. In a worst-case scenario, the introduction of these materials could have a significant impact on the overall CMOS process architecture."

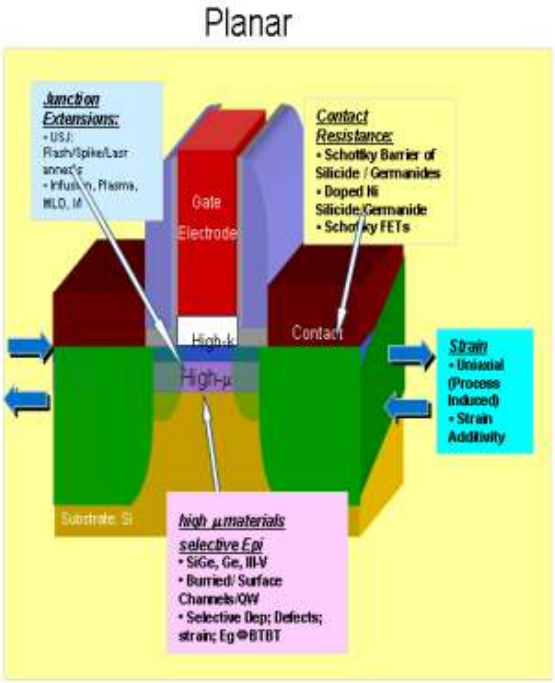


Figure 1.7: Challenges for planar MOSFET technology [21].

1.1.1 Basic theoretical considerations

The basic structure of conventional n-MOSFET and p-MOSFET devices (Figure 1.4), show the gate length (L), the dielectric oxide thickness (t_{ox}) and the contact junction depth (X_j). Under the gate, the silicon substrate is implanted for adjusting threshold voltage (V_{Th}). The gate electrode is made of highly-doped polysilicon, separated from the silicon substrate by a thin layer of Silicon dioxide (SiO_2) formed by thermal oxidation. Sidewall spacers are formed on side walls of the gate structure. The gate oxide, gate electrode and sidewall spacers all together serve as a hard-mask for self-aligned source and drain implantation.

Typical current-voltage (I-V) characteristics of n-MOSFETs are shown in Figures 1.8 and 1.9. The I-V characteristics of p-MOSFETs are a mirror-negative of the I-V n-MOSFET curve. Basically three regions can be identified (Figure 1.8) [22-26]:

- **weak inversion or also called the subthreshold region**: in this region the gate voltage (V_{GS}) is lower than V_{Th}. The V_{Th} is the gate voltage at which the inversion layer is formed. A weak inversion current can be observed for $V_{GS} < V_{Th}$ and $V_{GS}=V_{DS}=0$, where V_{DS} is the drain voltage;

- **linear or triode region**: in this region an inversion channel is formed and a current flows from source to drain.. In this case $V_{GS} > V_{Th}$ and $V_{DS} < V_{GS} - V_{Th}$, and the transistor works as a resistor. The source-drain current can be written as:

$$I_D = \mu C_{ox} \frac{W}{L}\left[\left(V_{GS} - V_{Th}\right) V_{DS} - \frac{1}{2} {V_{DS}}^2 \right], \qquad (1.1)$$

where μ, C_{ox}, W and L are the mobility of the charge carriers (electrons for n-MOSFETs), the gate-oxide capacitance, the channel width and channel length, respectively.
The threshold voltage is defined as:

$$V_{Th} = V_{FB} + 2\psi_F + \frac{\sqrt{4q\varepsilon_{Si}\psi_F N_a}}{C_{ox}}, \qquad (1.2)$$

where V_{FB} is the flat-band voltage, ψ_F the difference between the intrinsic level and Fermi level, ε_{Si} the dielectric constant of silicon, and N_a the dopant density in the channel.

- **saturation region**: the drain current is controlled by the gate voltage almost totally. The transition between the triode and saturation region is determined by the condition $V_{DS} = V_{GS} - V_{Th}$. In this case $V_{GS} > V_{Th}$ and $V_{DS} > V_{GS} - V_{Th}$. The source-drain current can be written as:

$$I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} \left(V_{GS} - V_{Th}\right)^2. \qquad (1.3)$$

When the transistor is working in the weak inversion region is possible calculate the subtreshold swing *S*, which is defined as a voltage required to increase or reduce the drain current by one decade. It can be expressed as:

$$S = \left(\frac{\partial \log(I_{DS})}{\partial V_{GS}} \right)^{-1} = \frac{\partial V_{GS}}{\partial \log(I_{DS})} \tag{1.4}$$

where I_{DS} is the drain current.

The transconductance (g_m) quantifies the drain current variation with a gate-source voltage variation, keeping the drain-source voltage constant and can be written as:

$$gm = \left. \frac{\partial I_{DS}}{\partial V_{GS}} \right|_{V_{DS}} \tag{1.5}$$

With the transcondutance value it is possible calculate the effective mobility:

$$\mu = \frac{LAgm}{WC_{ox}V_{DS}} \tag{1.6}$$

where *A* is the gate area.

The transcondutance and mobility are important electrical parameters in evaluating the performance of MOS transistors.

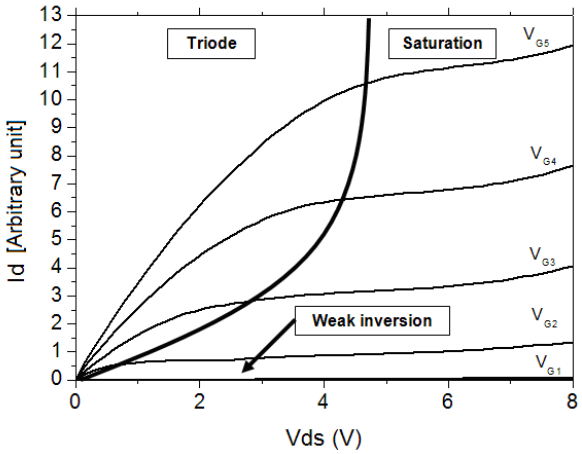


Figure 1.8: Output characteristics, I_{DS} versus V_{DS}, of an n-MOSFET.

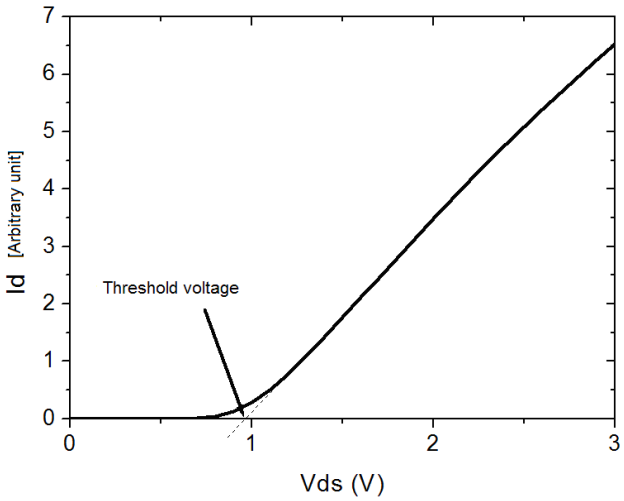


Figure 1.9: Transfer characteristics, I_{DS} versus V_{GS}, versus of a n-MOSFET.

The shrinking of lateral dimensions is invariably followed by vertical downscaling, requiring ever more shallow junctions, a particularly challenging task for source and drain junctions in highly-scaled CMOS. The ITRS roadmap calls for junction depths below 20 nm from 2013 onwards

while, at the same time, the source/drain series resistances must be kept low enough to effectively limit the voltage loss across these regions [20]. To achieve this, the increase in series resistance resulting from reduced junction depth must be counteracted by increasing the doping level in the source and drain regions. Doping technology together with new annealing techniques is necessary to provide solutions for the advanced device technology. Highly activated ultrashallow junctions (USJ), and abrupt dopants profiles are expected in order to minimize the short channel effect (SCE) which can decrease the threshold voltage and mobility of carriers. The SCE can be observed when the channel length of the transistor is of the same order of magnitude as the depletion-layer widths in the channel region. The situation of short channel is characterized when the amount of charges controlled by gate is the same order that the charges on source and drain depletion region. The main SCE are:

- **drain-induced barrier lowering (DIBL) and punch through**: when the drain voltage increases, the electric field of the drain can penetrate to the source area reducing the potential energy barrier of the source-channel junction. The punch through effect is associated to the current flow at the bulk (substrate) region and DIBL attributed to the surface current.

- **hot electrons**: this effect is related to high electric field, mainly in the drain region. This high electric field induces high energy electrons (hot electrons) by impact ionization which can be injected and

trapped in the oxide gate rising the oxide charge and increasing the threshold voltage.

To minimize the SCE, the capacitance C_{ox} should be increased for better gate-control of the channel and the junction depth should be decreased. Other requirements for future technologies also need to be considered such as the parasitic series resistance of the transistor, which must be minimized as shown in Figure 1.10. Basically, the parasitic series resistance consists of the [27,28]:

- R_{co}: contact resistance between the metal contact and implanted source/drain regions;
- R_{sh}: resistance determined by the sheet resistance (Rs) of the source/drain regions. This resistance can be influenced by changing the junction depth and/or concentration of dopants;
- R_{sp}: Spreading resistance, which is strongly dependent on the lateral doping abruptness of the source/drain extension;
- R_{ol}: overlap resistance in the overlap region between the gate and the source/drain;
- R_{ch}: channel resistance between the source and drain of the transistor.

For future CMOS technology nodes the objective is to reduce the contact and overlap resistivity [29].

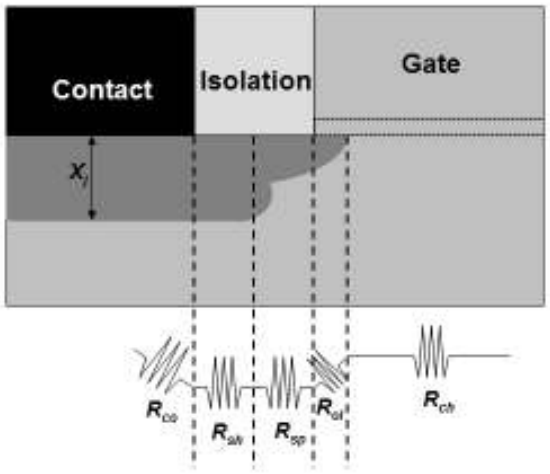


Figure 1.10: Cross-section of the MOS transistor illustrating the parasitic series components.

For the scaling of MOSFET devices down to sub 45 nm dimensions, new materials and device concepts are under consideration:

- silicon dioxide has been used for decades as a gate dielectric, but for thin gate dielectrics (< 1 nm) the tunneling leakage of thermal SiO_2 becomes excessive. New materials are therefore being sought with high dielectric constants (high-k), good quality interfaces with Si, thermal and chemical stability, in order to maintain the downscaling of the capacitance while avoiding the tunneling effect. Silicon oxynitride (SiO_xN_y) films may extend the limit on oxide thickness a little further. It has been shown that SiO_xN_y can be beneficial for reduction of the leakage current, reliability enhancement, and suppression of boron penetration [30-33]. A gate dielectric with higher dielectric constant (higher than SiO_2) can, at the same

thickness, achieve a smaller equivalent oxide thickness (EOT). Table 1.2 gives a list of alternatives gate dielectrics and relevant properties. The capacitance of a metal-insulator-semiconductor (MIS) structure can be written as:

$$C_{ox} = \frac{\varepsilon_o \varepsilon_{ox} A}{t_{ox}} \qquad (1.7)$$

where ε_{ox} the corresponding dielectric constant and ε_o the permittivity of free space (F/cm);

- ultrashallow junctions are required for the source and drain extensions in order to suppress the Short Channel Effects. In this thesis, excimer laser annealing (ELA) of implanted ions is studied for the formation of USJ. This option will discussed in the next section

- reduction of power dissipation;

- improvement of lithography processing;

- etc.

Table 1.2: Properties of high-k dielectric alternatives to SiO_2 [34].

Material	**Dielectric Constant (*k*)**	**Band gap E_G (eV)**	**Conduction band offset (ΔEc) (eV)**
SiO_2	3.9	8.9	3.2
Si_3N_4	7.0	5.1	2
Al_2O_3	9.0	8.7	2.8
HfO_2	25	5.7	1.5
ZrO_2	25	7.8	1.4
La_2O_3	30	4.3	2.3
Ta_2O_5	26	4.5	1-1.5

Next to the high-*k* gate dielectrics, new metal gate electrodes, materials with low-*k* for interconnections [35] and also new substrates have been used in order to improve performance of the circuits. During the past years strained Si Metal-Insulator-Semiconductor Field Effect Transistor (MISFET) devices technology have emerged, and they are also studied on alternative substrates such as Ge and GaAs.

Future downscaling of CMOS technology depends on the ability to suppress SCEs, which is becoming more difficult in standard bulk devices due to the increase of tunneling at the drain junction as the doping concentration in the body is increased. One answer to the challenge of SCEs

is expected to be fully-depleted structures, such as ultra-thin-Body Silicon-on-Insulator (UTB SOI) devices and FinFETs, which inherently have superior electrostatic integrity as compared to bulk devices. A variant of SOI technology is the silicon-on-nothing process in which a layer of SiGe is sandwiched between the Si substrate and the Si channel, and is later removed by selective etching from the region underneath the channel, thereby realizing a local SOI structure. This was illustrated in Figure 1.2.

1.2 Ultrashallow source/drain fabrication

In order to meet the junction depth requirements advanced annealing techniques are being developed. These techniques should be able to create shallow or ultrashallow junction with high activation of dopants, free of defects, minimum diffusion (low thermal budget), lateral doping abruptness and low sheet resistance. The requirements for source and drain extensions are expected to be in the order of 10 nm and sheet resistance expected to increase from 660 Ω/square to 1060 Ω/square from the year 2009 to 2015. The limit for the lateral abruptness of the junction is expected to decrease from 2.8 nm/dec. to 1.5 nm/dec. during the same years. To achieve these requirements, different methods have been used for dopants activation.

The laser annealing technique has been studied at Delft Institute of Microsystems and Nanoelectronics – Delft University of Technology (TUDelft) which proved is a technique very attractive for many applications as:

- ultrashallow junctions and contacts formation. Both p^+n and n^+p near-ideal diodes were fabricated and evaluated in order to apply this technology in bipolar transistor and FET devices [36,37];

- Junction Field Effect Transistors (JFETs) [38];

- Silicon-on-Glass (SOG) bipolar transistors with laser annealed Schottky collector [39-42];

- varactor diodes [37];

- SiGe heterojunction bipolar transistors [43].

1.2.1 Rapid thermal annealing

Rapid Thermal Processing (RTP) is a method which heat the silicon wafer rapidly to an elevated temperature (up to 1000 ^oC) and cooling to perform the activation of dopants in few seconds and with ramp rate typically 20-250 ^oC/sec [44,45]. This process can be also used for oxidation [46], silicide formation [47] and deposition [45]. The RTP equipments often use banks of tungsten-halogen lamps to provide a convenient heating to the silicon wafer and the radiant energy that the Si wafers is receiving from the lamps is controlled by a pyrometer. This system can be used for spike annealing in order to obtain shallow junction, where the temperature of silicon wafer is ramped to high values and after reach the desired temperature level the system is then cooled immediately [45]. In the RTP diffusion effects and

low activation of dopants are present [48]. To avoid these problems new technologies need to be explored and developed.

1.2.2 Laser annealing

As mentioned previously the diffusion effect and low activation of dopants are presents in the RTP system. To improve these effects, a new system with faster ramp rate is necessary. The laser annealing system can offer a faster ramp rate, faster cooling rates and reduce thermal budget. The studies of laser radiation on solids and the effects date back to 1971 [49]. Many different types of laser annealing systems have been used for dopants activation post lower energy implants [50].

During the laser irradiation the solid is bombarded by a beam of photons focused on a sample. These photons will interact with the electrons of the sample transferring energy to the lattice and this energy will heat the sample locally. The wavelength of the light determines how the energy will be absorbed in the solid or in our case in the silicon. ELA has the shortest annealing times and practically eliminates any Transient Enhanced Diffusion (TED) effects of the dopants and also offers benefits such as precise control of the junction depth, good abruptness of dopant profile and high dopant activation [51-56]. The depth of junctions processed by ELA can be precisely controlled by the amorphizing ion implantation since the amorphous silicon has a lower melting temperature than the crystalline one and the energy density of the laser light can be adjusted to only melt the top amorphous region, making the junction depth aligned to the edge of the silicon amorphized by ion implantation. Thus, lowering of the vertical

implantation range can serve as a simple mean for the further reduction of junction depth.

1.2.3 Shallow junction evaluation techniques

Four-point resistance measurements

Four-point probe is simple system which is used to measure the resistivity of a thin film or diffusion layer. By passing a current through the outside probes and measuring the voltage through the inner probes allows measurement of the substrate resistivity [57]. In this thesis it is used to measure the sheet resistance on a semiconductor substrate after low energy implantation and activation of dopants by laser. A CDE Resmap meter was used to measure the sheet resistance of the p-type samples, with starting resistivity of 2-5 Ωcm and implanted at low energies (5 keV). To be able measure ultrashallow junctions a probe with low contact force needs to be use to avoid the penetration of the needles through the formed junction.

Secondary ion mass spectroscopy

Secondary Ion Mass Spectrometry (SIMS) is a technique used to analyze the composition of thin films and solid surfaces. The bombardment of a sample surface with a primary ion beam causes the sputtering of the surface specimen and collecting and analyzing the ejected secondary ions. These secondary ions are analyzed by a mass spectrometer. This technique

provides information about the elemental, isotopic and molecular composition of atomic layers [58].

Transmission electron microscopy

Transmission electron microscopy (TEM) is a technique whereby a beam of electrons is transmitted through the sample, which makes it possible to visualize the cross section of the samples. This technique is capable of imaging at higher resolution (atomic resolution). The samples are specially prepared to thicknesses which allow electrons to transmit through [59]. TEM images were used to evaluate the source and drain junctions in p and n-MOS transistors as well as the gate channel.

1.3 Strained channel engineering

The influence of mechanical strain on carrier transport in silicon has been utilized since the 90 nm node to enhance mobility in CMOS devices [60]. As can be deduced from equations 1.5 and 1.6 this enhanced mobility will increase the current gain and speed of the devices. Experimental results have shown the electron mobility for n-MOSFET devices of approximately 70% high than unstrained Si (Figure 1.11) and the application of this technique, which can create electron mobility benefits from the reduction in longitudinal effective mass, which happens inside the silicon channel once it is subjected to uniaxial and/or biaxial strain. The uniaxially strained channel employed in current CMOS technology requires a certain amount of effective area at the source and drain regions to transfer mechanical force to

the channel, the processing of which will become more and more difficult as the devices are scaled down. The biaxial tensile strain is another technology for enhancing both electron and hole mobility. Usually the biaxial tensile strain can be obtained by epitaxially growing relaxed SiGe layers underneath the channel region. This layer is susceptible to misfit dislocations [61,62] which depend on the Ge content and thickness that can propagate during the processing into the silicon channel and can cause device malfunction.

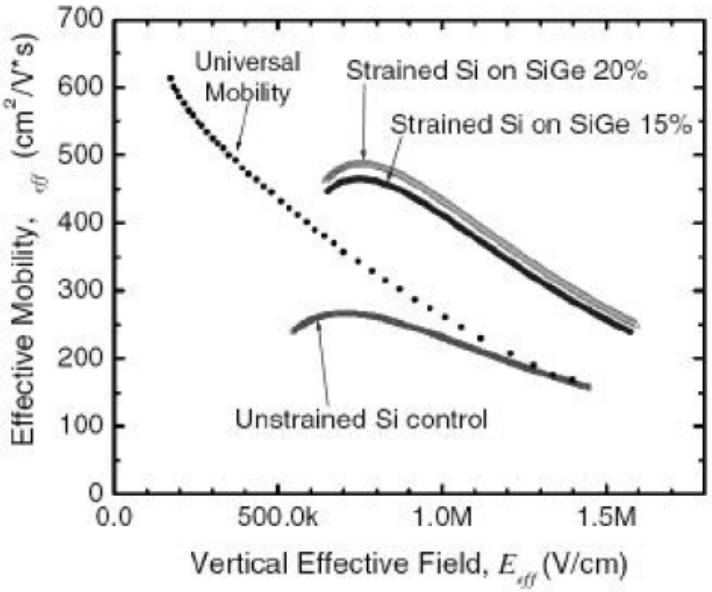


Figure 1.11: Effective Mobility of n-MOSFET devices with strained Si [63].

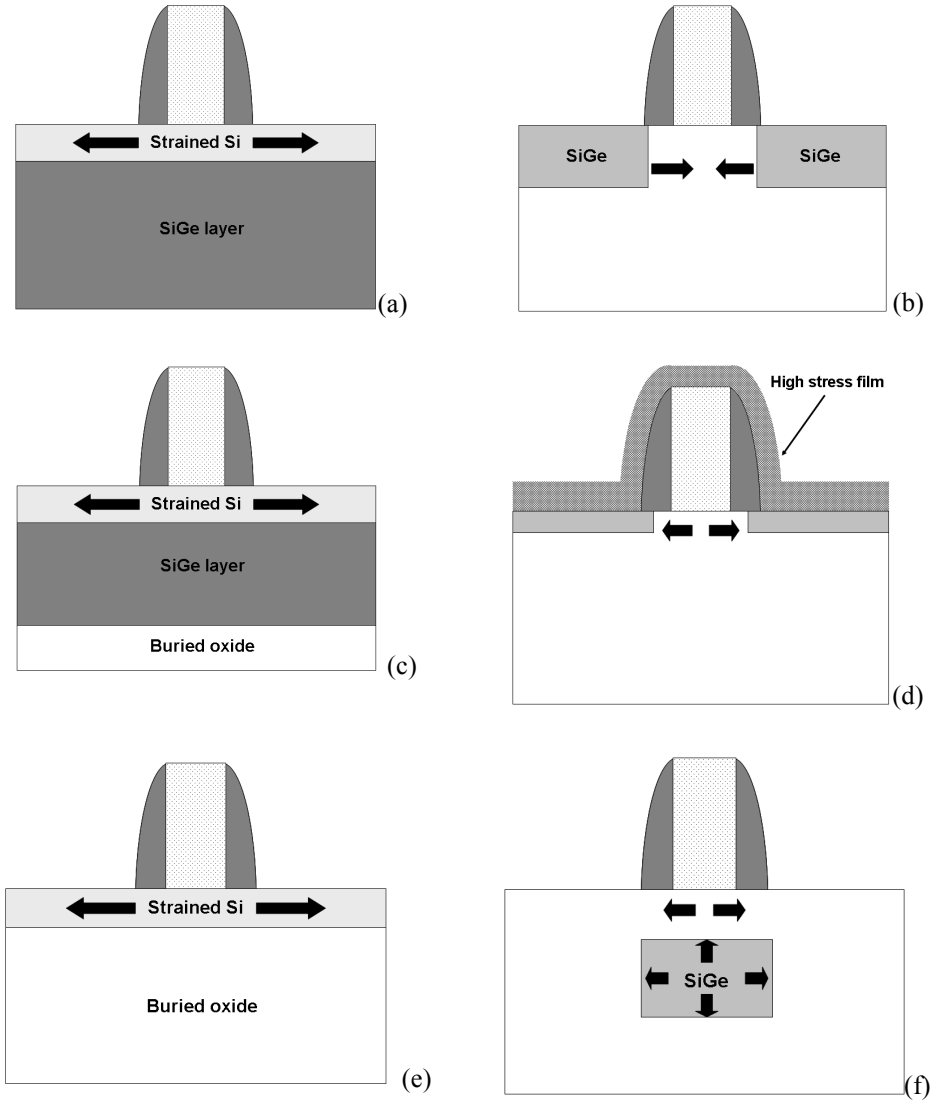


Figure 1.12: Strained Si MOSFET structures. (a) strained Si on SiGe "virtual substrate", (b) strained Si by embedded SiGe, (c) strained Si on SiGe/buried oxide layer, (d) strained Si on buried oxide layer, (e) strained Si by silicon nitride cap layer and (f) strained silicon by reverse embedded SiGe (e-SiGe) structure [64-67].

Strained Si channel improves the carrier mobility of MOSFETs [64] and different structures have been shown during the past years as strained Si on SiGe "virtual substrates" [68,69], strained Si by embedded SiGe, strained Si on SiGe/buried oxide layer, strained Si on buried oxide layer, strained Si by silicon nitride cap layer and strained silicon by reverse embedded SiGe structure (see Figure 1.12) [64-67]. On strained Si/SiGe MOSFET devices, the 4.2% lattice mismatch between Si and Ge induce strain on Si layer (used on the channel) when grown on relaxed SiGe [66]. The SiGe relaxed layer needs to be grown with low defect density to obtain a good strained Si layer and improve mobility.

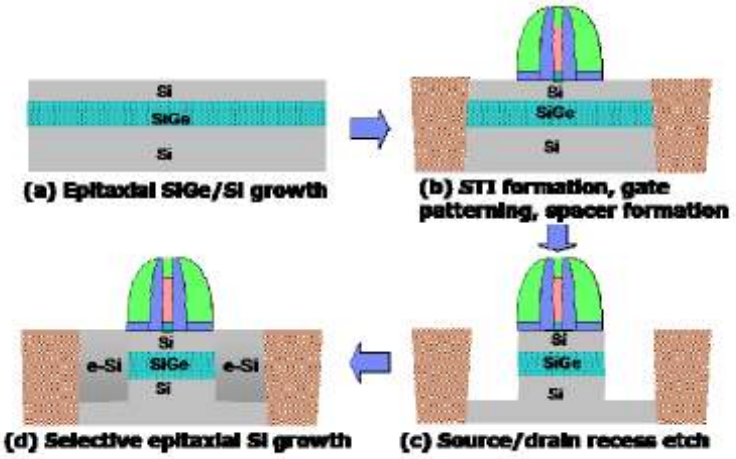


Figure 1.13: Main steps of the IBM reversed e-SiGe device fabrication process [70].

The IBM, in 2006, reported a technology similar to the DotFET that utilizes local SiGe stressor (see Figure 1.12 (f)) [70]. Afterwards, the Section 1.5.2 will show a comparison between both IBM and DotFET technologies. In the IBM process, the source and drain areas are created by

selective epitaxial growth to create a strained Si channel. The IBM processing can be seen in Figure 1.13. The TEM image in Figure 1.14 shows the IBM reverse e-SiGe n-MOSFET.

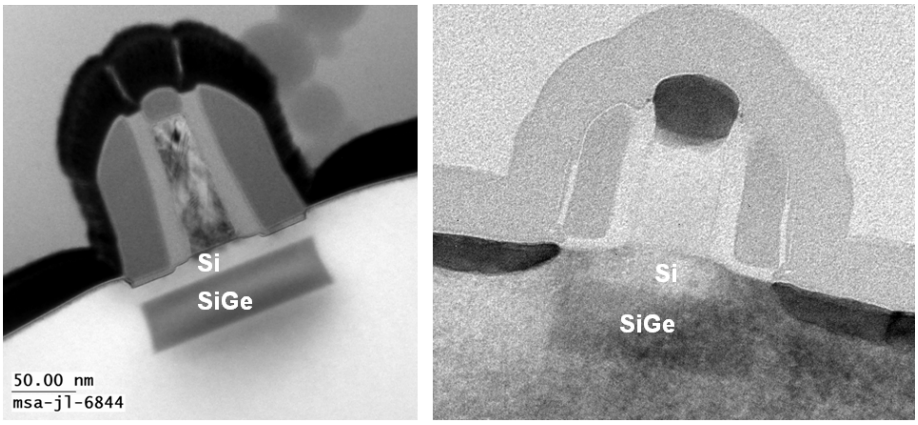


Figure 1.14: Cross section TEM images of the IBM reverse e-SiGe n-MOSFET [70].

1.4 SiGe dot fabrication and properties

The SiGe dots used for the DotFET fabrication were grown in a self-assembling Stranski-Krastanow (S-K) [4] mode that allows single-crystalline dots of SiGe to grow in three-dimensions on predefined seedholes. Under appropriate conditions this growth is defect free and can easily be scaled down. The 3D growth of the SiGe allows a higher Ge content inside the dot before the onset of crystal dislocations as compared to the growth of 2D SiGe layers of similar thickness. The smaller the SiGe dots the higher the Ge content that can be maintained without defect formation and consequently a higher strain can be exerted on any Si layer

grown over the dot. The dots can be grown in a controllable way by either MBE on a silicon substrate with a regular seedhole pattern of submicron periodicity etched into the Si, or by chemical-vapor deposition (CVD) where the dot location is controlled by opening seedholes through an oxide layer to the Si substrate. For the devices described in this thesis, the growth by MBE was investigated in detail in order to determine the optimum growth conditions and seedhole-patterns for achieving a dot-size and strain level suitable for constructing a MOSFET over the center of the dot structure where the biaxial tensile strain could be exploited for channel mobility enhancement. An example of such a structure is shown in Figure 1.1 along with the situation that could be envisioned in the case of a selective CVD process.

1.4.1 SiGe dot growth

For a uniform and reproducible SiGe dot growth, excellent results were achieved by a location-controlled growth method where large, regular arrays of seedholes are patterned on an otherwise flat Si substrate [1,2]. In the case of growth by MBE, suitable seedholes can be fabricated by etching holes directly in the Si. In the present work, both i-line optical lithography and e-beam lithography (EBL) were used to pattern such holes in (100) Si wafers. The results obtained by patterning with optical lithography will be discussed in Chapter 6 along with the double patterning and spacer technology used to obtain the submicron size and pitch needed for successful dot growth. In the case of e-beam lithography a very good control of the seedhole positions

and size is obtained and the resulting dots are extremely regular as seen in Figures 1.15 and 1.16.

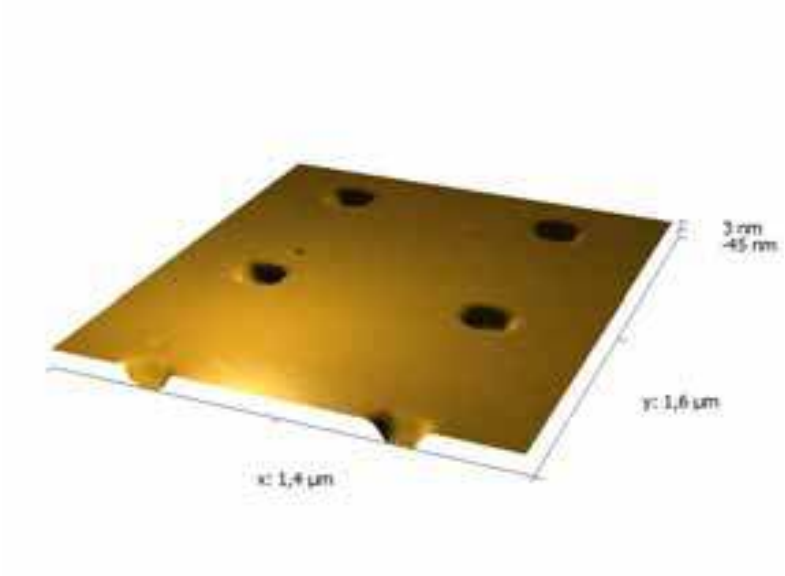


Figure 1.15: Image of typical of e-beam lithography seedholes taken by Atomic Force Microscopy (AFM). The holes are 45nm in depth. Image from Forschungszentrum Jüllich.

The growing of the dots above the seedholes is performed as follows: first a Si buffer layer is deposited which smoothes the surface and transforms the circular pit into one that is square based [61,71]. The dots are then grown at 720 °C from a pure Ge source and they initially take on the form of prepyramids, but with a larger Ge volume they transform into truncated pyramids, then complete pyramids, transition domes and finally domes as shown in Figure 1.17 [71]. With a further supply of Ge, they

evolve into barn and superdome shapes but at this stage dislocations start to appear. The present DotFET fabrication required a dot size that could accommodate a gate of length ~ 100 nm. For this purpose the most suitable seedhole arrays were the ones with a periodicity of 800 nm that rendered a maximum dot diameter in the range of 230 nm. EBL patterning of this configuration was used for the device fabrication, while analysis of the dot properties was also performed on samples processed with optical lithography.

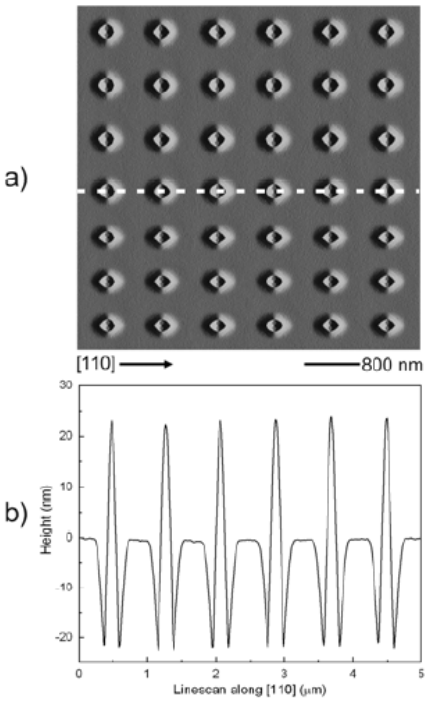


Figure 1.16: An array of SiGe dots imaged by AFM (a) and a linescan along the [110] direction (b). The dots are grown by MBE at 720°C on a Si surface prepatterned with seedholes defined by EBL. Data from Forschungszentrum Jülich and Johannes Kepler University Linz.

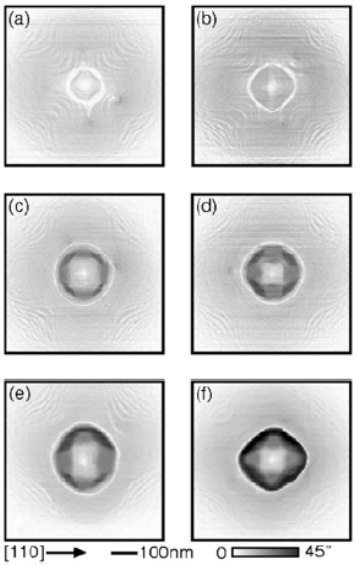
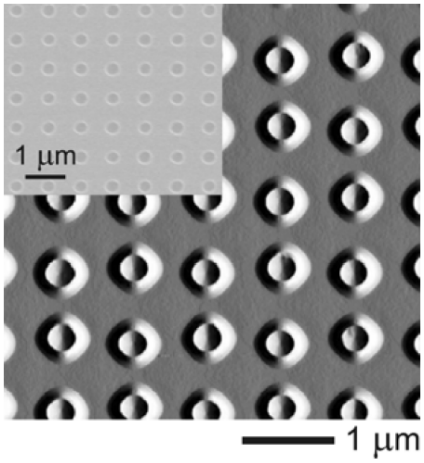
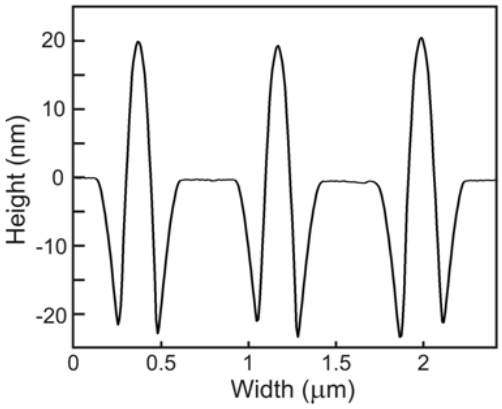


Figure 1.17: SiGe dots grown by MBE at 700°C from a pure Ge source. They initially take on the form of prepyramids (a), but with a larger Ge volume they transform into truncated pyramids, then complete pyramids, transition domes and finally domes (f) [71]. Data from University of Milano Bicocca.

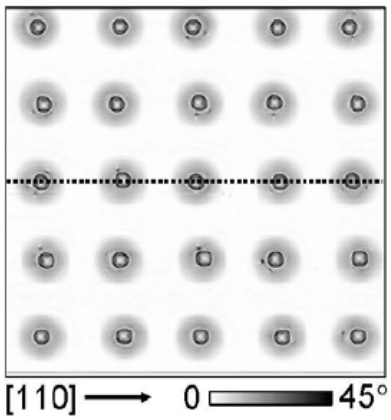
It is moreover possible to grow very small sub-100-nm dots by patterning very dense seedhole arrays, which has been demonstrated in several cases by using either EBL, nano-imprint lithography (NIL) or interference lithography (IL) as shown in Figures 1.18, 1.19 and 1.20, respectively. Here also the very good pattern control of such fine lithography technology translates into very uniform dot arrays.



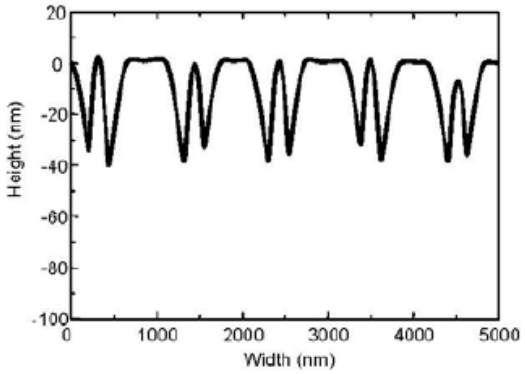
(a)



(b)



(c)



(d)

Figure 1.18: AFM image of an array of SiGe dots grown by MBE on a prepatterned substrate (a) (c) and a height measurement over the sample (b) (d). The inset in top-left corner shows the seed holes before the growth [71, 72]. AFM data from Johannes Kepler University Linz.

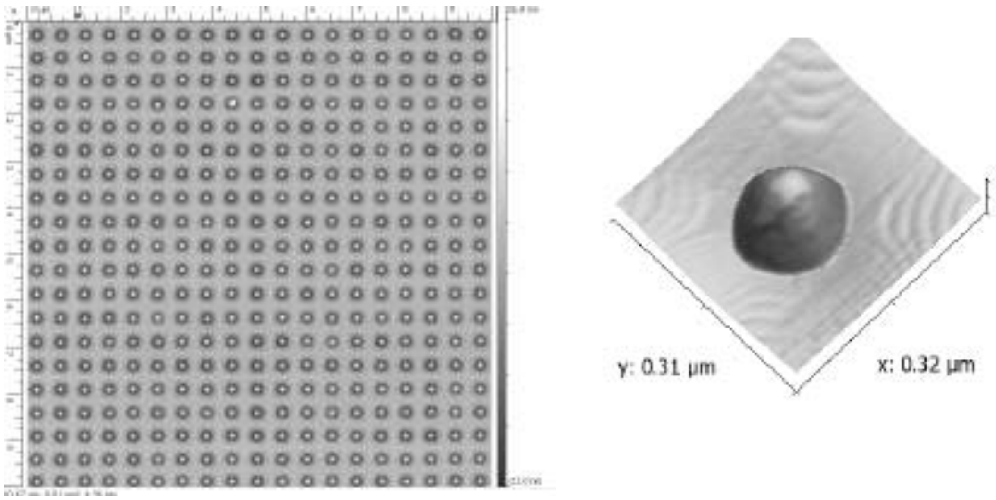


Figure 1.19: AFM image of ordered SiGe island arrays grown on NIL patterned Si substrate. Data from Forschungszentrum.

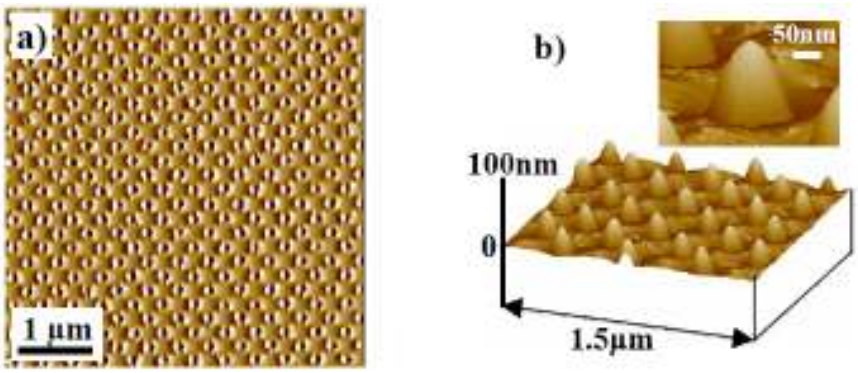


Figure 1.20: Ordered CVD-grown Ge islands on IL patterned Si(100) substrates. Deposition temperature 700°C; Si buffer 11 nm thick; Ge nominal thickness ~1.2 nm. Data from Forschungszentrum Jüllich.

1.4.2 Analysis of strain

The SiGe dots were analyzed with respect to their shape, Ge content and strain. The latter is also examined in layers that were used to cap the dots. In particular, X-ray diffractometry (XRD) was performed on the arrays of SiGe dots grown on substrates patterned by optical lithography and capped with 50-nm-thick silicon layer that was grown *in-situ* after the dot formation. From these measurements the Ge content and the strain in the top silicon layer could be determined. To account for the influence of later process steps related to device fabrication, some samples were additionally capped with a 55-nm-thick layer of silicon nitride deposited by plasma-enhanced (PE) CVD. From the inspection of the measured XRD reciprocal space maps around a (224) Bragg reflection already a rough approximation of the strain and composition can be made. To improve the accuracy, a procedure was developed where the Ge content distributions of the uncapped and capped islands were modeled as an input for finite-element-method (FEM) simulations using the data on the shape of these structures from the AFM measurements. The resulting displacements from the FEM simulations were then used as an input for calculations of the scattered x-ray intensity distribution [9, 73]. This procedure was repeated until a satisfactory agreement between experimental x-ray data and the calculations was achieved. The scattered x-ray intensities for the uncapped samples correspond to a Ge content ranging from 14 % to 47 % for dome-shaped islands and from 36 % to 46 % for barns [9]. The fitting of the simulation data, an example of which is given in Figure 1.21, shows that the center of the silicon capping layer is under a tensile strain of about 0.8 % without and 0.7 % with a 55 nm thick nitride capping layer [9,73].

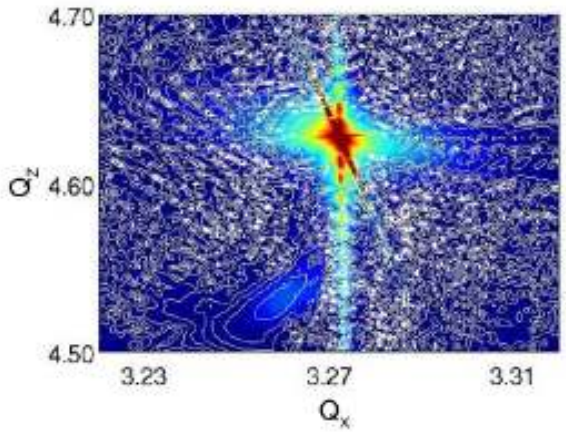


Figure 1.21: XRD measurements fitted to FEM simulations for a SiGe dot capped with 50 nm of Si and 55 nm of SiN_x [9]. Experimental data is the colored plot and simulation white contours. Data from Johannes Kepler University Linz.

Measurements were also performed using Micro-Raman spectroscopy on samples with SiGe dots grown at 620°C and capped with Si layers with a thickness of either 5, 10, 20 or 40 nm [8]. In order to characterize the strain of such an array of nanoscale SiGe dots overgrown with silicon, a resonant Raman system was setup with which the penetration depth of light in nanostructures is significantly reduced, from about 1 μm to sub-10-nm values. Moreover, the efficiency of the system is enhanced up to 100 times with respect to systems using out of resonance excitations, significantly increasing the signal-to-noise ratio and thus enabling the characterization of a small scattering volume in the Si cap layer. After the subtraction of a reference spectrum from the spectrum of the sample under test and assuming the same linear relationship between the frequency shift

and a value of the strain component ε_{xx} as in the case of a flat (001) surface, the averaging over an area of about 1 μm^2 yields detectable strain levels for a Si thickness of up to 20 nm as shown in Figure 1.22 (a). To gain more insight into the properties of a realistically shaped dot structure, the results of the Raman spectra are compared with 3D strain-maps generated by FEM. As seen in Figure 1.22 (b), this analysis confirms that the expected strain level in the centre of the Si capping layer is above 0.5 % for a layer thickness below 40 nm. The good correlation between the strain levels obtained from both the XRD and Raman analysis are an indication of the validity of the analysis methods and corroborate the potential of the 3D SiGe growth as a source of strain for mobility enhancement [8].

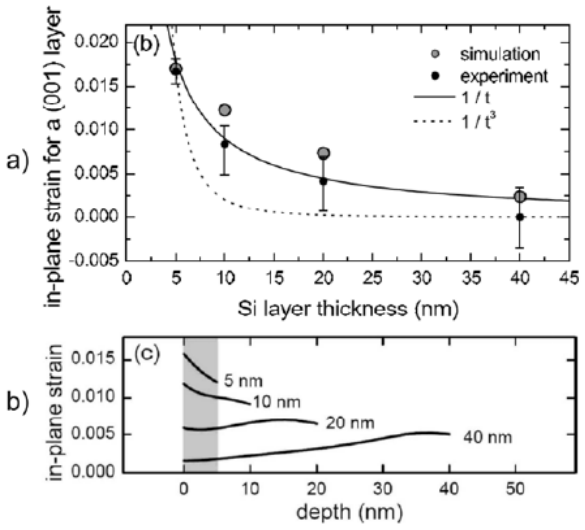


Figure 1.22: In-plane strain obtained by assuming a linear relationship between frequency shift and in-plane strain component (a). In-plane strain as a function of depth for different thicknesses of Si grown over a SiGe dot obtained by fitting the FEM results to the measured Raman spectra (b) [8].

1.5 The Disposable DotFET concept

1.5.1 Industrially compatible D-DotFET process flow

For the fabrication of the Disposable DotFET, where standard CMOS steps, including high temperature steps, are to be maintained during the processing after the SiGe dot growth, the dot needs to be removed early in the process to prevent outdiffusion of Ge from the dot. In this case, before the dot removal, the strain that the dot exerts on the Si channel must be transferred to a layer stack deposited over it, typically a layer of silicon nitride or polysilicon as indicated in Figure 1.23. It can be expected that some of the strain will relax after the dot removal, so some of the mobility enhancement is sacrificed in order to achieve a SON structure [15,16]. The process can be designed in such a way as to either fill the empty area left after the dot removal with a dielectric layer, such as in the standard SON process, or so as to leave the area void, since mechanical support is provided by the connection to the source/drain regions and the gate-stack. In the second approach the channel region is very sensitive to the mechanical force exerted from the gate-stack and contact-etch-stop-layer, which can be attractive for additional strain engineering. In particular, by depositing a tensile contact-etch-stop-layer, the tensile strain in the channel can be increased, or by depositing a compressive contact-etch-stop-layer, it can even be reversed to become compressive as is illustrated by the examples shown in Figure 1.24 [15,16]. With this approach, mobility can be optimized for both n-MOS and p-MOS resulting in a highly efficient CMOS process.

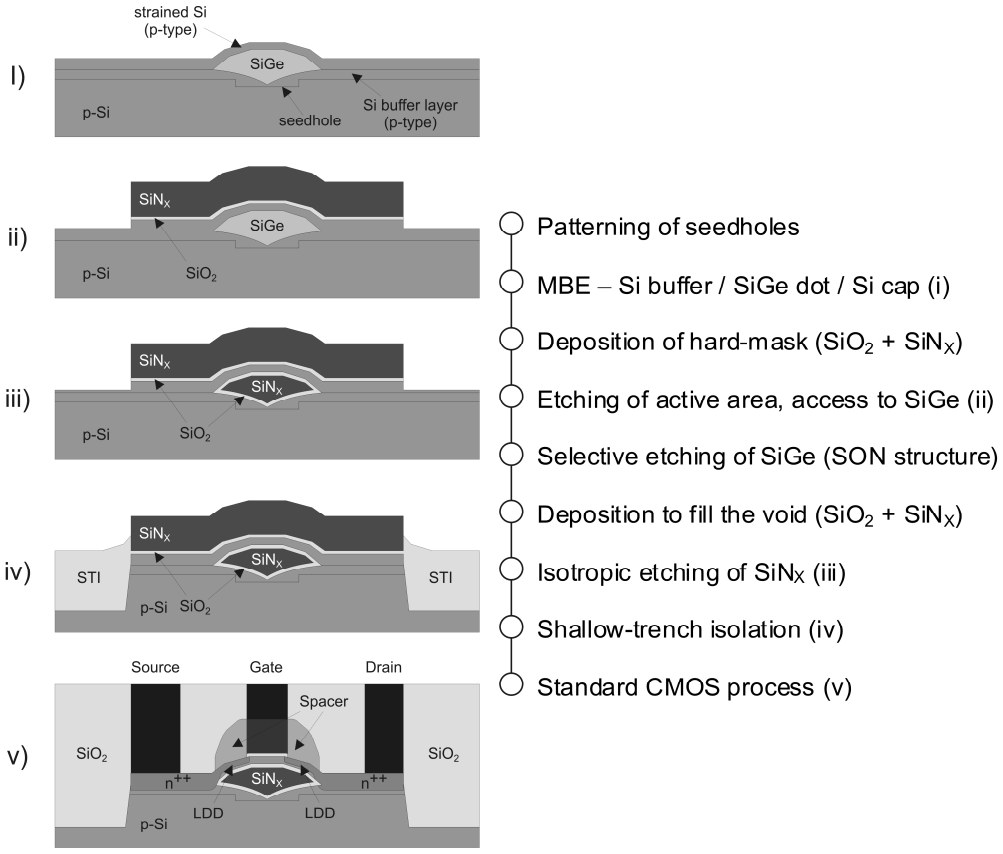


Figure 1.23: Schematic of a process flow suitable for integrating SiGe dots in an advanced SON CMOS process. The strain that the dot exerts on the Si channel is transferred to a layer of Silicon nitride (SiN_x) before the dot is removed, after which the source, drain and gate regions are fabricated.

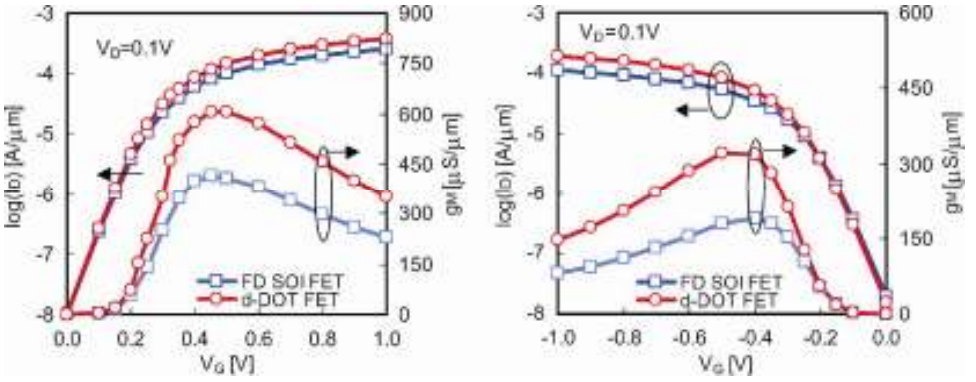


Figure 1.24: Simulated transfer characteristics and transconductance of an n-DotFET (left) and p-DotFET (right) when the dot is removed and a 120 nm SiN_x layer with either 1.2 GPa tensile or 2.5 GPa compressive stress, respectively, is applied to fix the strain transferred by the dot to a Si capping layer [15].

1.5.2 Device simulations

In the first stages of the project device simulation efforts were directed towards evaluating the potential performance benefit in transistor gain and speed when adopting the D-DotFET concept [15,16] and results such as those shown in Figure1.25, Figure 1.26 and Figure 1.27 were based on a very limited knowledge of the strain distribution in the SiGe dots and the layers deposited on them. In the course of the D-DotFET project, however, a very detailed knowledge was gathered on the subject. This formed the basis for extensive D-DotFET device simulations performed by the project team at the Technical University Wien.

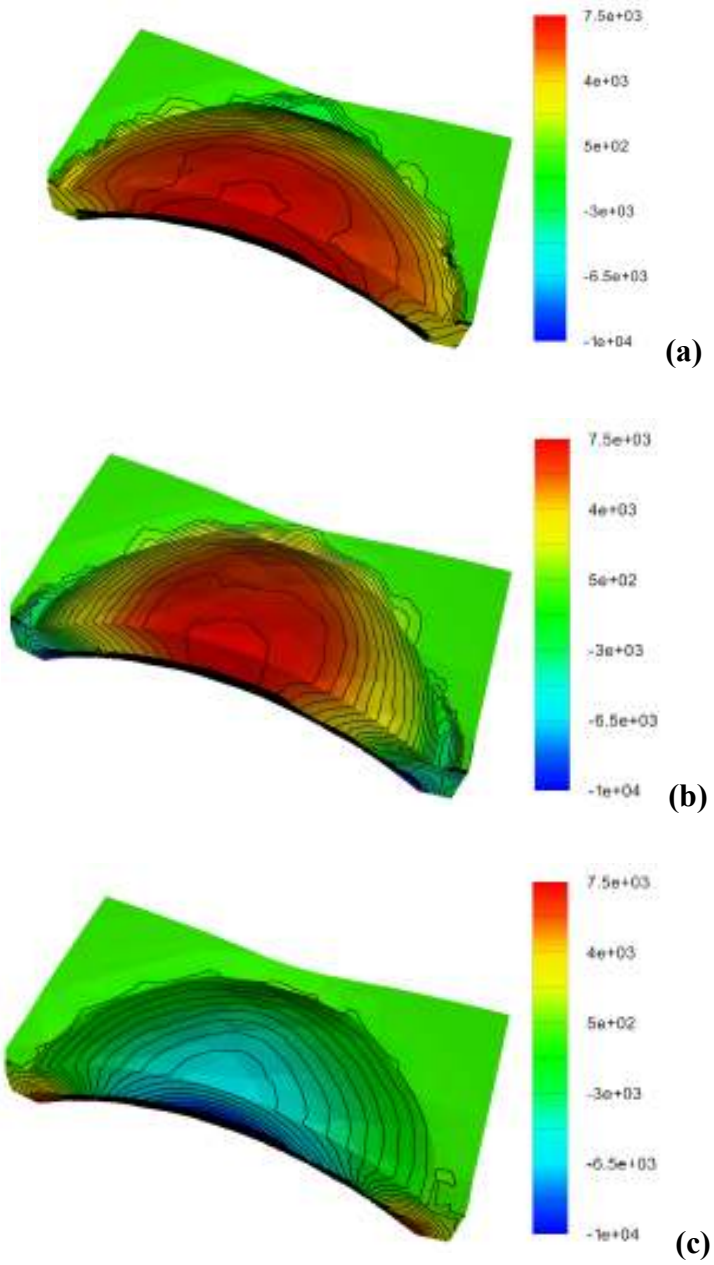


Figure 1.25: Strain components in the Si capping layer (a) e_{xx} (channel length direction) (b) e_{yy} (channel width direction) (c) e_{zz} (vertical direction) [74]. Data from University of Milano Bicocca.

If we compare the IBM technology mentioned in the Section 1.3 with the DotFET, the DotFET process induce more uniform strain up to 0.7% (Figure 1.25 (a), (b), and (c)) in the Si channel in comparison with 0.24% of the IBM device. For the simulations, the Ge content in the SiGe island is 30% on average, 1.5 nm thick oxide, polysilicon gate, boron doping of $4x10^{18}$ cm^{-3} in the Si cap layer, source and drain regions of 60 nm in width and maximum arsenic doping of 10^{21} cm^{-3} (Figure 1.26) were assumed. The final structure with the simulation grid is shown in the Figure 1.27 (only half of the whole device is simulated). The source and drain regions in the DotFET device are fabricated directly on the Si capping layer grown by MBE over the SiGe island by ion implantation and laser annealing, where in the IBM process the source and drain areas are created by selective epitaxial growth to create a strained Si channel. The simulations done by TU Wien predict for the DotFET the same enhancement in the drive current compared to the IBM process (drive current improvement of 15%) [74].

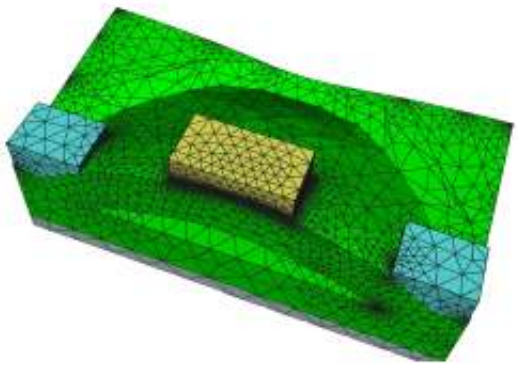


Figure 1.26: Geometry of the generated transistor structure. Only half of the device is simulated [74]. Data from University of Milano Bicocca.

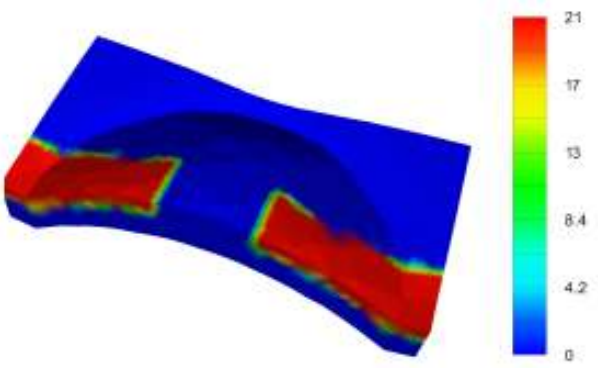
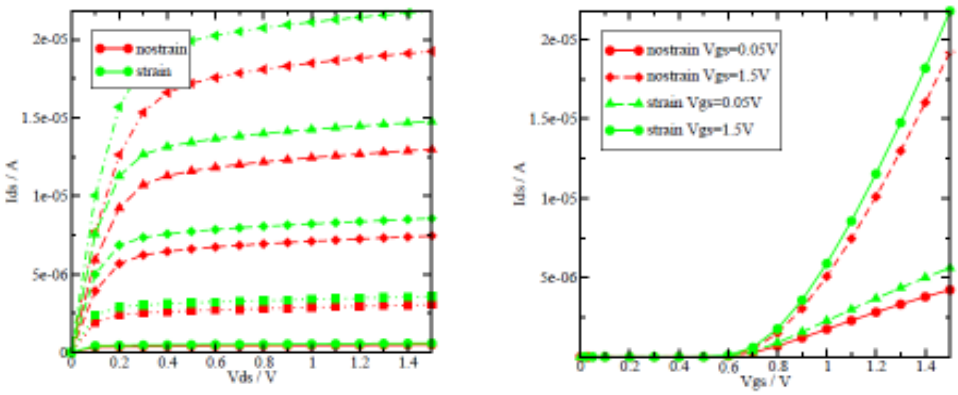


Figure 1.27: Arsenic profile doping implanted (source and drain area) implanted in the Si capping layer [74]. Data from University of Milano Bicocca.



(a) **(b)**

Figure 1.28: (a) Unstrained and strained output characteristics for gate voltages of 0.7V, 0.9V, 1.1V, 1.3V, and 1.5V (b) Unstrained and strained transfer characteristics for drain voltages of 0.05V and 1.5V [74]. Simulations from Technical University Wien.

The strain is three times higher in the DotFET simulations with the same enhancement of drive current can be attributed to different methods of extraction used. In the Figures 1.28 (a) and (b), the output characteristics for unstrained and strained device and the transfer characteristics for drain voltages of 0.05V and 1.5V are plotted, respectively.

1.6 Outline of the thesis

The thesis is organized as follows:

- **Chapter 2, Excimer laser annealing for self-aligned n^+p junctions,** describes the basic laser annealing approach that is used for the fabrication of ultrashallow junctions. This includes the high-power excimer laser system that was used as well as detailed processing considerations and analytical/electrical characterization of the laser annealed layers and junctions. Many aspects must be taken into account in order to achieve near-ideal junctions, such as the silicon surface preparation, the reflective laser masking layer, and the low-energy implantation conditions.

- **Chapter 3, Metal-Insulator-Semiconductor capacitors,** investigates different gate dielectrics deposited and grown at low temperatures. Several MIS capacitors are fabricated and electrically characterized.

- **Chapter 4, MISFET devices** describes the n-MISFET and p-MISFET processing for which the ultrashallow source and drain, metal-gate and contacts are all fabricated at low temperatures. The devices are evaluated by an extensive electrical characterization.

- **Chapter 5, DotFET devices** describes the DotFET process fabrication that makes use of the results of the previous chapters to form ultrashallow source and drain junctions and a metal-gate MOSFET structure on SiGe dots. A detailed electrical characterization is used to evaluate the enhanced gain of these devices. D-DotFET device is also presented.

- **Chapter 6, Conclusions and recommendations** concludes the thesis with a discussion of the presented topics, along with some suggestions for future work.

Chapter 2

Excimer laser annealing for self-aligned n^+p junctions

With the revolutionary progress in semiconductor industries, mainly in micro or nanofabrication techniques, new equipment has been developed in order to reach future technology nodes. Excimer laser annealing systems have received interest for application in microelectronics as an alternative low-temperature processing method for the crystallization of amorphous-Si (*a*-Si) [75]. This includes the laser annealing of implanted regions to form ultrashallow junctions. Many experiments based on doping profiling and sheet resistance measurements have shown that both full-melt and laser thermal processing can result in attractive values for junction depth, abruptness and sheet resistance [76-82]. Recently, much research has been done using excimer laser annealing techniques due to the extremely short annealing times that potentially give an elimination of transient enhanced diffusion effects, high levels of dopant activation and abrupt junctions [83]. Compared to conventional rapid thermal anneal procedures [84] this

technique offers extra advantages, such as good control of the junction depth. With this type of annealing a reduction of the vertical implantation range can serve as a direct means of also decreasing the junction depth. The laser processing research performed at Dimes in the past, rather than being aimed at the fabrication of source and drain regions for CMOS, has been motivated by the need to have access to good quality diodes in integration situations where only very low temperatures are permitted, such as in silicon-on-glass processing [85]. This chapter presents generally applicable guidelines for fabricating good quality n^+p junctions with low-energy As^+ implants and dopant activation by full-melt excimer laser annealing.

2.1 Dimes excimer laser system

The excimer laser system used for the work in this thesis is an Exitech M8000V double laser. The M8000V uses two Lambda Physik LPX 210 xenon chloride (XeCl) excimer laser sources (wavelength of 308 nm) and pulse duration of 25 ns full width at half maximum (FWHM). The energy densities are set through attenuators after which the laser beams are combined by a mirror (M3). A homogenizer is used to produce a flat-top intensity profile over a spot area of 1.75 x 2.5 mm^2. A schematic of the Exitech M8000V laser system is shown in Figure 2.1.

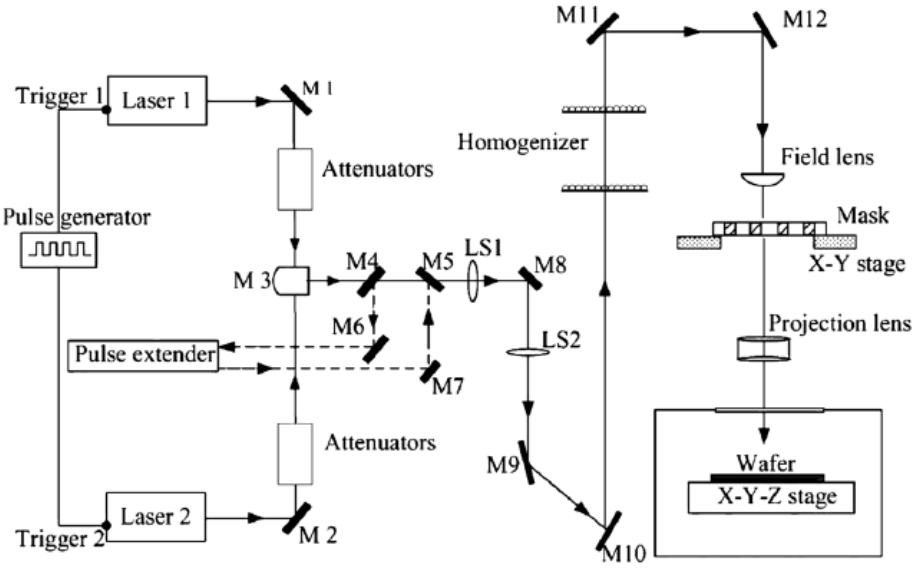


Figure 2.1: Schematic of the Exitech M8000V laser system [86].

2.2 Reflective mask for laser annealing

In order to selectively activate the implanted dopants without damaging surrounding regions of the sample, a reflective masking layer for the laser light can be used to cover these areas. Layers of Al are well suited to this purpose [87]. In this work sputtered Al is applied. In general, Al is often sputtered at 350^{o}C to achieve good step coverage. At the same time larger grains are formed than would be the case at lower temperatures. For example, sputtering the Al reflective mask at 50^{o}C results in much smaller grains [88], which results in a little more reflective surface than obtained for 350^{o}C depositions. Moreover, the grain size also plays an important role during the subsequent plasma etching step. The large Al grains result in

non-uniform plasma etching and Al layers sputtered at 50°C were used because they gave an overall better end result.

2.3 Low energy implantation and laser annealing

The basic process flow for fabricating shallow junctions by ion implantation and laser annealing is shown in Figure 2.2. Silicon dioxide can be grown or deposited on the silicon surface and covered with a reflection layer of Al, followed by the patterning of the stack. The contact window is opened by dry etching with soft landing on the silicon surface. To prepare the silicon surface for low energy implantation, the native oxide from the silicon surface should be removed. Any remaining native oxide will, besides reducing the dose implanted in the silicon, also roughen the surface and hence also the boundary between the amorphous-Si to crystalline-Si (*c*-Si). An important step that should be performed immediately before low energy implantation for high cleanliness of the silicon surface and for the native oxide removal is a 4 minutes dip in low concentration HF or a 15 seconds dip in buffered-HF (BHF) (1:7) solution. The aluminium is etched by HF-solutions, but a dip in BHF (1:7) is the preferred way for the native oxide removal since Al etching saturates after approximately 50 nm leaving a sufficiently thick Al/Si(1%) layer remaining as a reflective mask. The Figure 2.3 shows an example of the Al (1%Si) layer after BHF (1:7) dip-etch 15 seconds prior to implantation. Aluminium is readily etched by HF-solutions, but a dip in BHF (1:7) is preferable here because the Al etching saturates after approximately 50 nm leaving a sufficiently thick Al/Si(1%) layer to function as a reflective mask. However, any etching of the Al/Si(1%) layer creates a rough surface that degrades the reflectivity. Therefore as

much as possible of the Al should be covered by resist during the dip-etch and implantation. The resist used to pattern the windows themselves cannot be used for this purpose because resist at the window perimeter will then be co-implanted in the openings to the silicon and this degrades the ideality of the final laser-annealed junction. Therefore, an additional lithography step where the contact-window mask is oversized by 0.3 – 0.5 μm is applied.

A thin α-Si layer is formed by the low energy implantation and the junction depth can be adjusted by implanting dopants at different angles. After implantation, the photoresist is removed and the samples are cleaned and irradiated by the laser light. During the laser annealing, the chuck was kept at room temperature. The laser annealing of the α-Si layer will result in melting at a temperature about 200-300 ^{o}C lower than that needed to melt *c*-Si [88, 89]. The melting can then be tuned by the laser energy to propagate until it reaches the crystalline interface. The *c*-Si interface serves as seed for recrystallization of α-Si layer by epitaxy. The quality of the annealed layer depends of the laser energy. The melting can propagate through the crystalline region if the melting temperature of *c*-Si is reached. After the complete crystallization of the amorphous region, the dopants implanted become substitutional in the lattice. The sheet resistance of the implanted layers is strongly dependent on the junction depth [88] as shown further in the Section 2.4.

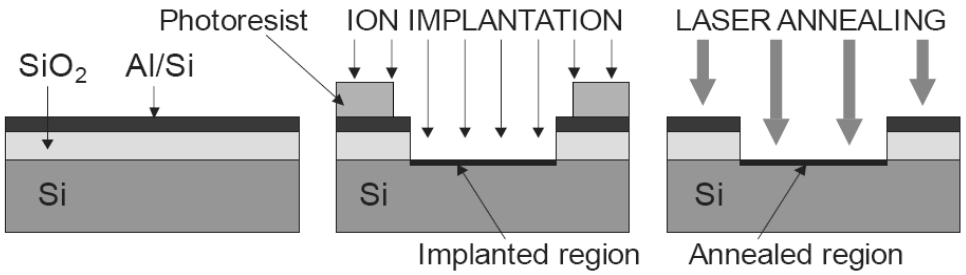


Figure 2.2: Formation of shallow junctions by low energy implantation followed by laser annealing. The Al layer is a reflective mask for laser light.

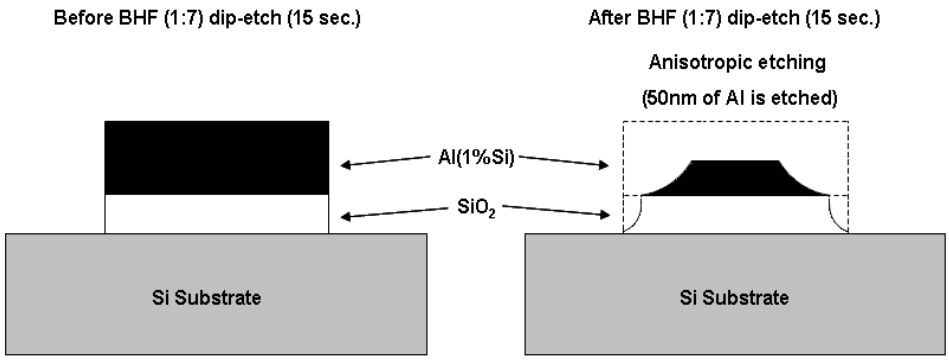


Figure 2.3: Example of Al (1%Si) layer after BHF (1:7) dip-etch 15 seconds prior to implantation. Al-etching saturates after approximately 50 nm leaving a sufficiently thick Al/Si(1%) layer remaining as a reflective mask.

2.4 Junction morphology and doping profile

The implanted and laser annealed layers at different tilt angles and laser energies, were analyzed by measuring the sheet resistance with a four point probe. A CDE Resmap sheet resistance meter was used to measure the sheet resistance. The doping profile, concentration of dopants and the junction depth were analyzed by SIMS.

Si wafers with 100 mm diameter were used during all processing. Wafers of p-type (100) (resistivity 2-5 ohm-cm) were used for As^+ implantation at low energy. Prior to implantation, a 4 minutes dip in low concentration HF (0.55%) is performed to remove native oxide from the Si surface. Then As^+ was implanted with 5 keV to a dose of $1x10^{15}cm^{-2}$ with tilt angles of 7^o, 30^o or 45^o. Over the wafer, 1x1 mm^2 dies were isolated from each other by trench isolation and the sheet resistance was measured for each die by four point probing. The depth of junction process by full-melt ELA can be precisely controlled by applying an amorphizing ion implantation since amorphous silicon has a lower melt temperature than crystalline silicon, and the energy density of the laser light can be adjusted to only melt the top amorphous region, thus aligning the junction depth to the amorphous/crystalline interface region [89, 90]. Therefore, for this type of annealing a reduction of the vertical implantation range can serve as a direct mean of also decreasing the junction depth. After implantation the samples were leaser annealed. The laser annealing parameters can be varied over the wafer. The main parameters are the scanning of the wafer in columns or in rows at different energies, temperature of the chuck, and overlap of the spots. Other parameters as pulse offset can also be changed. In this work the laser annealing was processed in columns, the chuck was kept at room temperature and 1% overlap of the spots (1.75 x $2.5mm^2$) was used. With 1% overlap only a single pulse irradiation of laser is performed at each position. The layout printed on the wafer is composed of 52 dies and 8 columns (from C1 to C8). The Figure 2.4 shows the configuration applied for laser annealing processing (1% overlap).

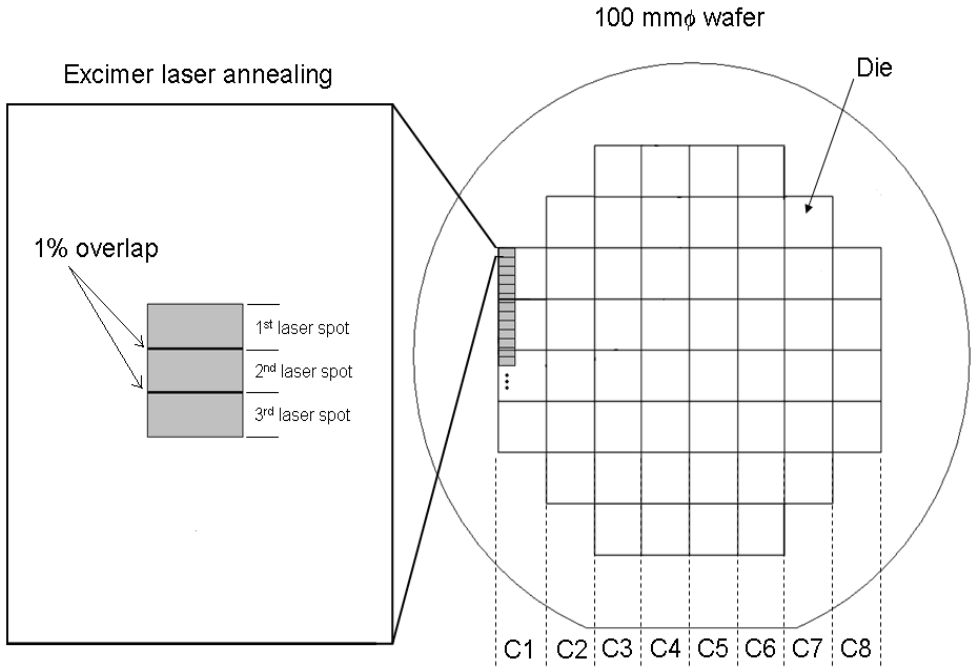


Figure 2.4: Configuration applied for laser annealing processing (1% overlap).

The samples are irradiated by the laser light with energy densities varying from 700 mJ/cm^2 to 1000 mJ/cm^2 (50 mJ/cm^2 step, during which the chuck was kept at room temperature. The Figure 2.5 shows the SIMS profile of the 5 keV As^+ implant with a dose of $1x10^{15}cm^{-2}$ and tilt angles of 7^o, 30^o and 45^o.

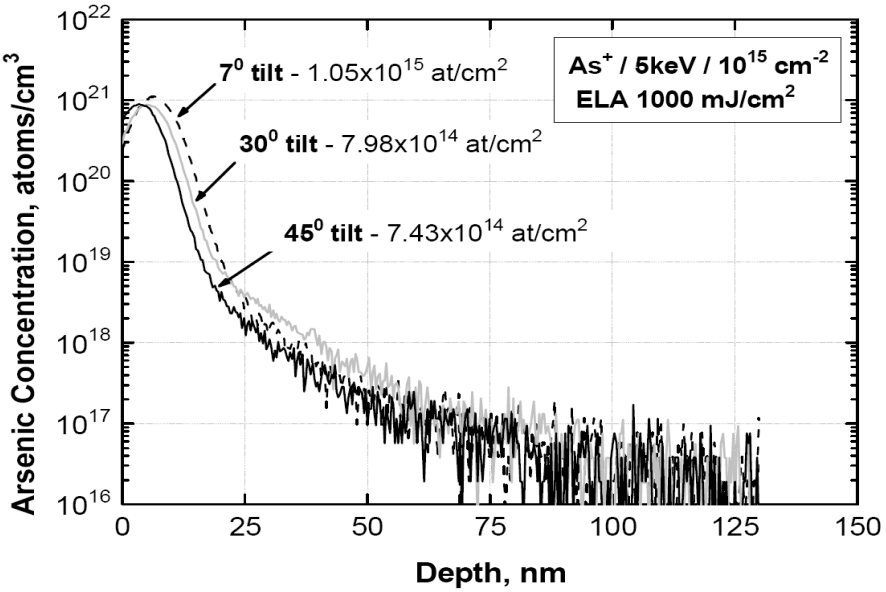


Figure 2.5: SIMS profiles of annealed regions implanted at three different angles. Higher tilt-angles reduce the junction depth at the cost of dose loss.

The results of SIMS analysis (Figure 2.5) of samples implanted at either 7^o, 30^o or 45^o show a reduction of junction depth at higher tilt angles (20, 18, 15 nm, respectively), but also reveal a dose loss due to the fact that more ions are reflected from the surface. As the tilt angle is increased the implanted dose reduces from $1.05x10^{15}$ cm^{-2}, $7.98x10^{14}$ cm^{-2} to $7.43x10^{14}$ cm^{-2}, because more ions are being reflected from the silicon surface, as well as the effective implanted dose being proportional to the cosine of the tilt angle. In the past, low energy BF_2^+ implantations (5 keV) with a 7^o tilt angle, a dose of $1x10^{15}$ cm^{-2} and laser annealing at 600 mJ/cm^2 and 1100 mJ/cm^2 have been shown to have junction depths in the 20 – 30 nm range [91].

The sheet resistance of laser annealed As^+ samples were measured with a four point probe. In Figures 2.6, 2.7 and 2.8 the sheet resistance is shown for the As^+ implanted layer after different laser anneal energy densities (varying from 700 mJ/cm^2 to 1000 mJ/cm^2 in 50 mJ/cm^2 steps) and different implantation tilt angles, 7^o, 30^o and 45^o, respectively. A large spread of the sheet resistance at low laser energy densities can be observed and by increasing the laser energy this spread is reduced. The sheet resistance measurements also show that a higher level of dopant activation is achieved at higher annealing energies. The Figure 2.9 shows the average sheet resistance versus the laser energy density. The TEM analysis (Figure 2.10) shows the As^+ amorphous layer after 5 keV energy implantation at a dose of 1x10^{15} cm^{-2} and a 45^o tilt. An amorphous region of 13 nm in depth is discerned which compares well with the 15 nm depth found after laser annealing in the SIMS profile. A sheet resistance of 220, 275 and 311 Ω/square is achieved at 1000 mJ/cm^2 for implantation tilt angles of 45^o, 30^o and 7^o, respectively. In Table 2.1 a summary is given of the obtained SIMS and sheet resistance values.

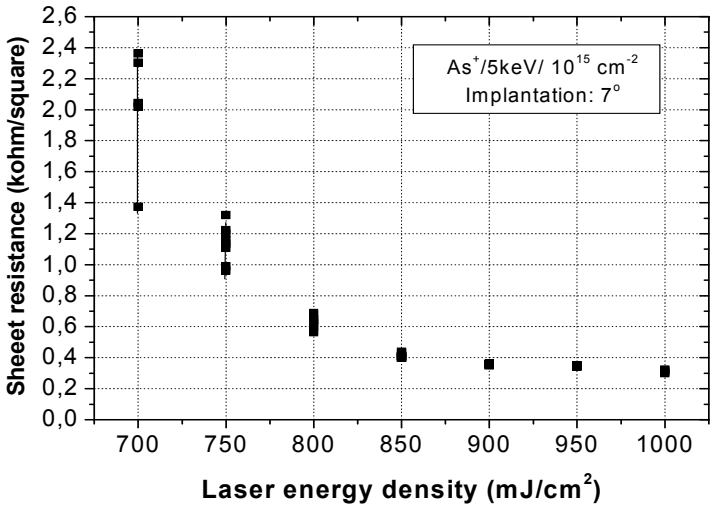


Figure 2.6: Sheet resistance of a laser annealed As^+ 5 keV, 10^{15} cm^{-2}, 7° tilt angle implantation versus the laser energy density.

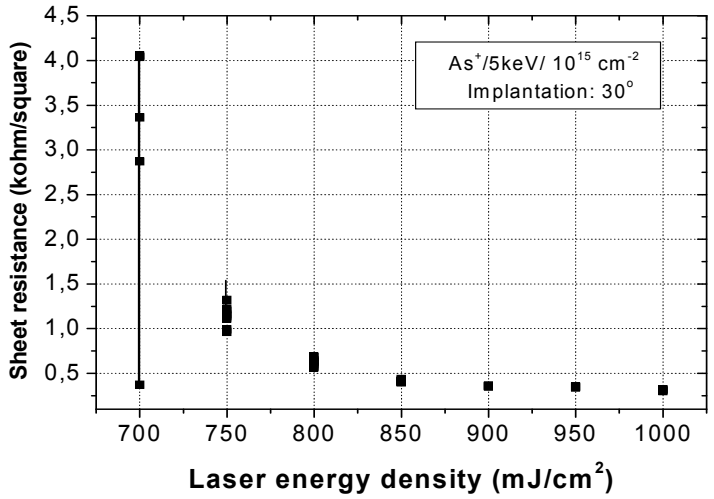


Figure 2.7: Sheet resistance of a laser annealed As^+ 5 keV, 10^{15} cm^{-2}, 30° tilt angle implantation versus the laser energy density.

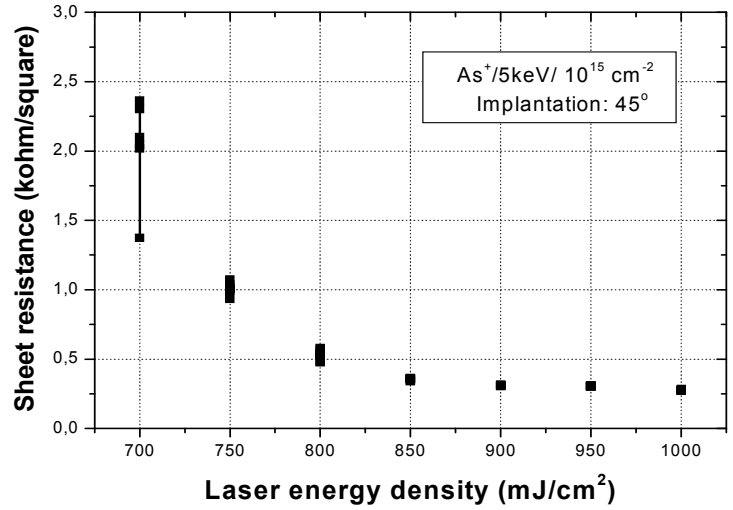


Figure 2.8: Sheet resistance of a laser annealed As^+ 5 keV, 10^{15} cm^{-2}, 45° tilt angle implantation versus the laser energy density.

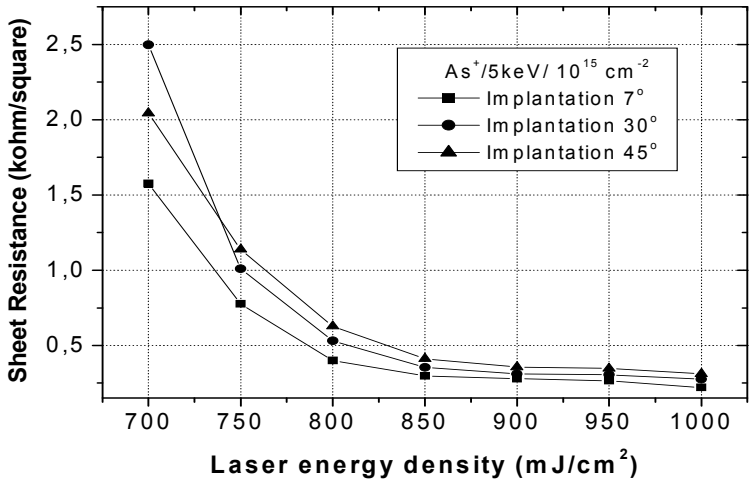


Figure 2.9: Average of the sheet resistance of a laser annealed As^+ 5 keV, 10^{15} cm^{-2}, 7°, 30° and 45° tilt angle implantation versus the laser energy density.

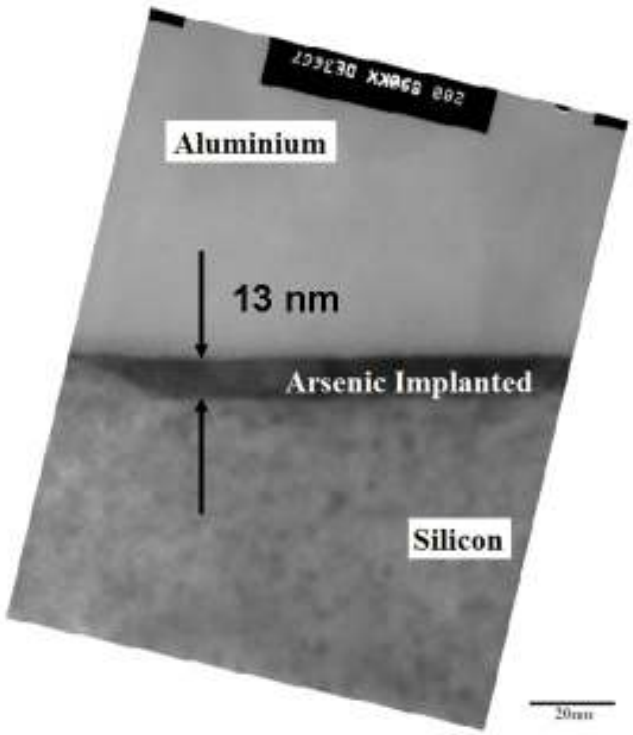


Figure 2.10: Cross-sectional TEM image of the edge of the laser annealed junction, 1000 mJ/cm^2 anneal and a 45^o implantation tilt.

Table 2.1: Summary of parameters extracted for laser annealed low-energy arsenic implants. Average sheet resistance (*Rs*) is shown.

Laser energy density (mJ/cm^2)	Nominal dose (at./cm^2)	SIMS dose (at./cm^2)	Implantation (tilt angle)	Junction depth (nm)	Implantation dose (at./cm^2)	Sheet resistance avg. (Ω/square)
1000	1 E15	1.05 E15	7^o	20	1.05 E15	220
	1 E15	7.98 E15	30^o	18	7.98 E15	275
	1 E15	7.43 E15	45^o	15	7.43 E15	311

2.5 Integrity of Al reflective mask

To investigate the integrity of the Al layer used as a reflective mask during laser annealing two structures were fabricated. The Figures 2.11 (a) and (b) show the structures fabricated.

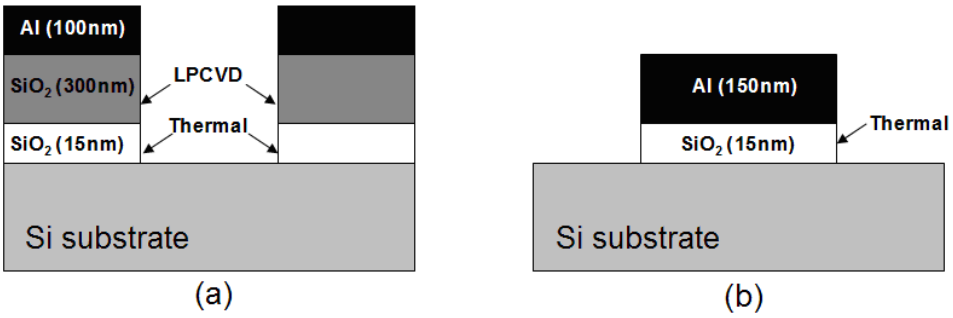


Figure 2.11: Structures fabricated for testing the Al reflective mask. Structure (a) 100 nm thick Al layer etched in lines over 300 nm thick LPCVD oxide and 30 nm thick thermal oxide and structure (b) an 150 nm thick Al layer etched in lines over a 15nm thick thermal oxide.

To fabricate the the first structure (Figure 2.11 (a)), 30 nm thermal SiO_2 is grown at 850°C on the Si substrate, 300nm SiO_2 is deposited by LPCVD at 400°C, and a 100-nm-thick layer of Al(1%Si) is sputtered at 50°C. Windows are patterned by optical lithography. More details about the fabrication of this structure are given in the Section 2.6.1. To create the second structure (Figure 2.11 (b)), 15 nm thermal SiO_2 is grown on the Si substrate and a 150-nm-thick layer of Al(1%Si) is sputtered at 50°C. Lines are patterned by optical lithography. For both structures, the Al layer is sputtered at 50°C to keep the grain size small, which gives a good reflectivity during laser annealing. The samples were irradiated by laser

light with energy densities varying from 700 mJ/cm^2 to 1000 mJ/cm^2, during which the chuck was kept at room temperature. After the laser irradiation, significant heating occurs of the Al layer of the first structure (Figure 2.11 (a)), which causes ablation at the edges of the reflective mask that increases with laser energy density, as seen in Figure 2.12(a). The thick underlying oxide layer used in the first structure has low thermal conductivity and the heat is not easily conducted away to silicon substrate. To be able to integrate self-aligned laser annealed junctions, the ablation at the gate edges must be prevented by reducing the thermal resistance of the dielectric layer. In the case of Metal-Oxide-Semiconductor (MOS) devices, a thin gate dielectric has significantly lower thermal resistance, which makes the integration of laser annealing possible [92]. Experiments conducted with 150 nm thick Al reflective mask over 15 nm thick thermal oxide ((Figure 2.11 (b)) show little variation in width of the narrow Al lines (Figure 2.12(b)) which shows the feasibility of masking a full-melt laser anneal with the reflective layer of the metal-gate in MOSFET devices. During the diode processing, a thin layer of Al is used together with one-shot laser annealing to avoid problems with the post-laser-annealing Al morphology.

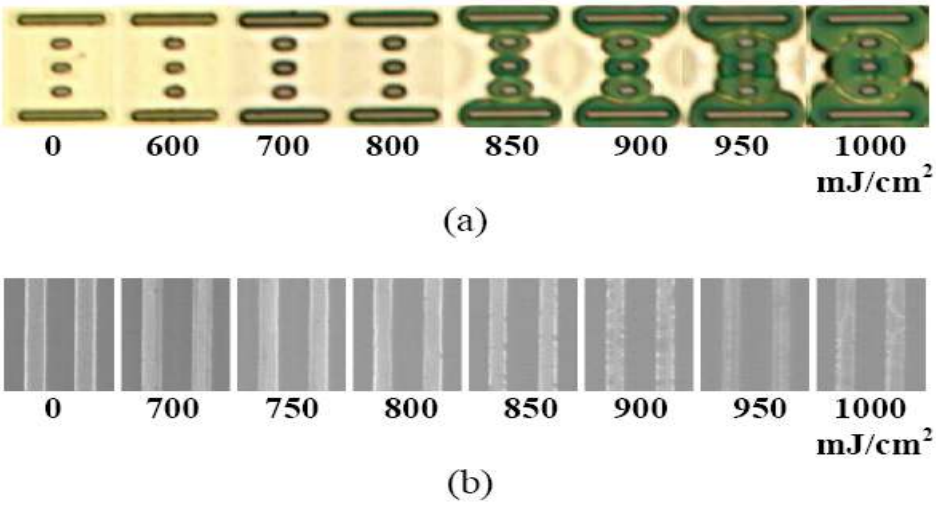


Figure 2.12: (a) Micrograph of reflective Al layers where ablation has occurred at the edges of the annealed region. The size of ablated region increases with laser energy. (b) SEM micrograph of 150 nm thick Al lines over 15 nm thick thermal oxide after annealing. When the underlying oxide is thin, no ablation occurs [92].

2.6 Self-aligned n^+p junction

In line with what has been demonstrated in the past [93-98], low energy implantation of As^+ combined with excimer laser annealing is used here to obtain ultrashallow junctions with higher activation of dopants. In this section a description is given of the process fabrication and the electrical characterization of ultrashallow n^+p diodes which were designed to be implemented in the D-DotFETs.

2.6.1 Self-aligned n^+p junction fabrication

The basic process flow for fabrication of n^+p and p^+n junctions is shown in the Figure 2.13. Silicon dioxide is used as the surface isolation layer. Of the various possible ways to grow or deposit an oxide layer on the silicon surface, thermal oxidation gives the highest quality oxide also with respect to the interface to silicon. In accordance the etch-rate of thermal oxide during a typical dip-etch step to remove native oxide is low. In our case a 4 min dip in a 0.55% hydrofluoric acid (HF) solution is used and only 10 nm is removed in this step, which is attractive for the control of the lateral dimensions. Oxide layers deposited by LPCVD and plasma-enhanced chemical-vapor-deposition (PECVD) have inferior interface properties and etch significantly faster in HF. On the other hand, they can be deposited at much lower temperatures than normally usable for thermal oxidation, The experiments presented here in detail make use of a 330-nm-thick oxide stack consisting of a 30-nm-thick thermal oxide grown at 850 °C, which gives a good interface to the silicon, covered with a 300 nm thick LPCVD oxide deposited at 700 °C from tetraethyl orthosilicate (TEOS) source, which reduces the total thermal budget. A layer of 100 nm thick aluminium with 1% silicon (Al/Si(1%)) is then deposited by physical vapor deposition (PVD) to serve as reflective masking layer for the laser light, as shown in Figure 2.13. Aluminium has been shown to be efficient in protecting regions that should not be modified during laser annealing [80, 82]. The low implantation energy required for fabricating shallow junctions also makes the implantation profile very dependent on the state of the silicon surface prior to ion implantation. It has been demonstrated that a clean and smooth surface is essential for having good electrical characteristics of the

implanted junctions annealed by ELA, which requires soft landing during reactive-ion etching (RIE) steps and native oxide removal before implanting ions [99]. Various HF solutions can be used for the stripping of native oxide, the applicability of which will depend on the degree to which other layers are etched. Openings in the isolating/reflective stack are patterned in resist and etched by first RIE of Al/Si(1%) using hydrogen-bromide and chlorine plasma and oxide RIE using a fluorine-based plasma. To prevent damage to the silicon surface from the RIE process, the removal of the last part of the oxide isolation is done at lower radio frequency (RF) power – 100 W compared to 300 W during bulk oxide etching. As specified in Table 2.2, soft landing on silicon surface results in smaller surface roughness, as good as the one achieved by wet landing using HF-solutions, but with the advantage of not significantly etching in the lateral direction [99, 100]. The native oxide is removed using a BHF diluted with water in a 1:7 ratio during a 15 seconds dip that is performed immediately prior to the implantation of As^+ ions. Aluminium is readily etched by HF-solutions, but a dip in BHF (1:7) is the preferable here because the Al etching saturates after approximately 50 nm leaving a sufficiently thick Al/Si(1%) layer to function as a reflective mask. To prevent the Al/Si(1%) etching an additional lithography step where the contact-window mask is oversized by 0.3 – 0.5 μm is applied as mentioned before. The n^+ region to be laser annealed is formed by a 5 keV, 2-3 x 10^{15} cm^{-2} As^+ implantation with either a 7° or 30° tilt from eight directions. The implanted regions are then annealed by the laser at 1000 mJ/cm^2 energy density for n^+p junctions while the wafer-chuck temperature was kept at room temperature. A 4 min HF (0.55%) dip-etch is performed to remove the native oxide before metallization, which is done by depositing and

patterning 600 nm Al(1%Si). Alloying in forming gas at 400°C is the final process step. The backside of the wafer was also metalized for contact to the p-substrate. To take full advantage of the laser-annealed ultrashallow junctions TED effects [101-103] need to be avoided after dopant activation by the laser and therefore all thermal processing steps above 400°C were avoided after laser annealing.

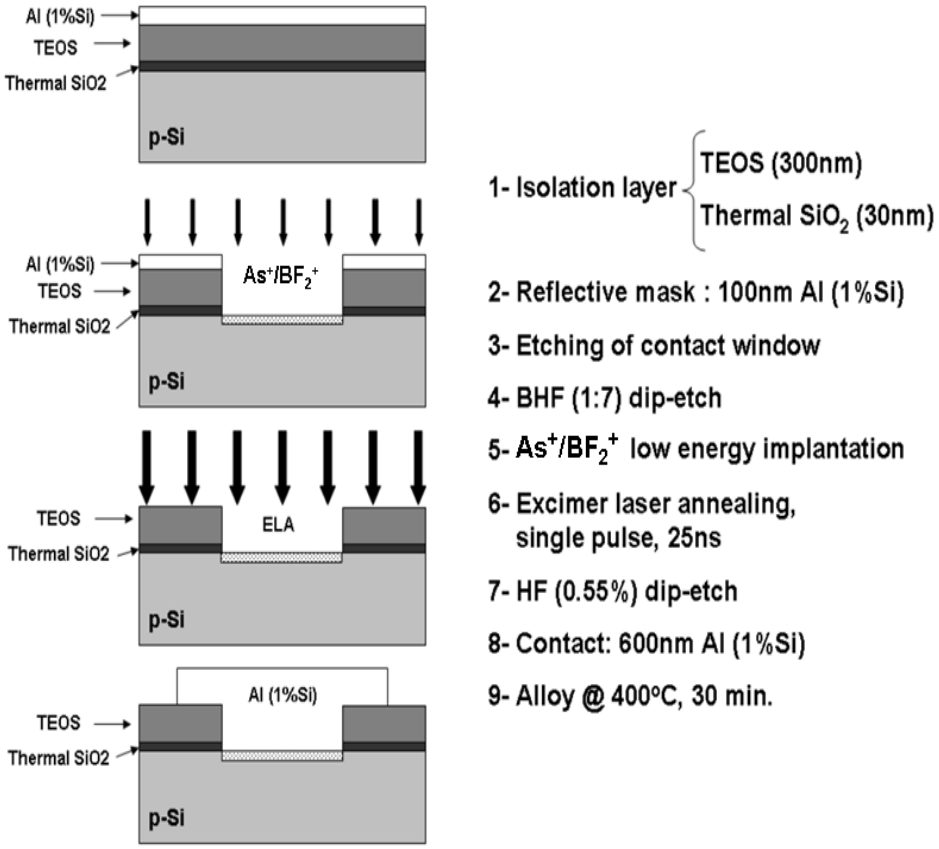


Figure 2.13: Process flow for the fabrication of n^+p and p^+n laser annealed diodes.

Table 2.2: Pre-implantation surface roughness as a function of the type of reflective mask and the etch process used for landing on the silicon [100].

Type of landing	Al	Al/Si(1%)
Hard – 300 W	17 Å	27 Å
Soft – 100 W	12 Å	12 Å
Wet – BHF(1:7)	11 Å	35 Å

An overview of the transformations of the contact perimeter at each of these stages is depicted in Figure 2.14. The selectivity of the oxide RIE in the fluorine-based plasma system to silicon is approximately 10:1, but a certain overetch time is included to remove all oxide inside the opening before junction implantation, albeit at lower RF power. Native oxide removal by surface treatment by BHF(1:7) for 15 seconds immediately prior to the As^+ implantation also etches the isolation oxide in the lateral direction. The LPCVD oxide is removed faster than the thermal oxide, giving a recess of about 60 nm in addition to the 8-9 nm removed near the interface. The slow etch-rate of the thermal oxide is beneficial if maintaining minimum contact window size. This is important since tight control over the junction dimensions is then preserved after this step, but otherwise the type of oxide used at the interface is not critical at this stage of the process. The subsequent high-dose ion implantation amorphizes the surface region of the silicon substrate and also sputters some of the silicon atoms from the surface, an effect that increases with tilt angle: with a tilt angle of either 7°, 30° or 45°, respectively 1, 1.58 or 6 Si atoms are removed per As^+ ion [104]. Illumination by laser light melts the exposed surface layer to a depth that depends on the laser energy, but also on the depth of the region amorphized

by ion implantation because the amorphous silicon has a lower melting temperature than the crystalline silicon [89]. The melt onset begins at 600 mJ/cm^2 and full melt to a depth of 20 nm happens for 1100 mJ/cm^2 [100]. However, for energy densities above 1000 mJ/cm^2 surface degradation patterns can develop that are referred to as laser-induced periodic surface structuring (LIPSS) and the maximum laser energy density was therefore limited to 1000 mJ/cm^2 [105]. The high temperature achieved in the melted region decays toward the bulk of the wafer and in the lateral direction, but it can also exceed ablation limits of the aluminium layer used as the reflective mask, in which case some of the Al/Si(1%) is removed from the edges of the openings while the oxide isolation remains unchanged. This is shown in Figure 2.12(a) for contact windows which were opened through the stack of oxide and reflective Al/Si(1%) layers, implanted and laser annealed. A small part of the laser light is absorbed in the Al/Si(1%) and is not conducted away efficiently due to low thermal conductance of the thick underlying oxide. This causes ablation of Al/Si(1%) at the edges that increases with laser energy density [106]. The pre-metallization HF dip-etch further etches the oxide layers and this step can potentially expose the junction edges as indicated in Figure 2.14 (c). For this reason it becomes attractive to use implantations at higher tilt angles to increase the lateral junction extension under the sides. In Figure 2.15, a TEM image of the final contact opening confirms the shape of the edge of the isolation layer, with only a small lateral removal of the thermal oxide layer as opposed to the LPCVD oxide. A slight loss of the silicon surface in the implanted region can also be observed. This may originate from the overetch during oxide RIE, Si sputtering during implantation and/or native oxide removal.

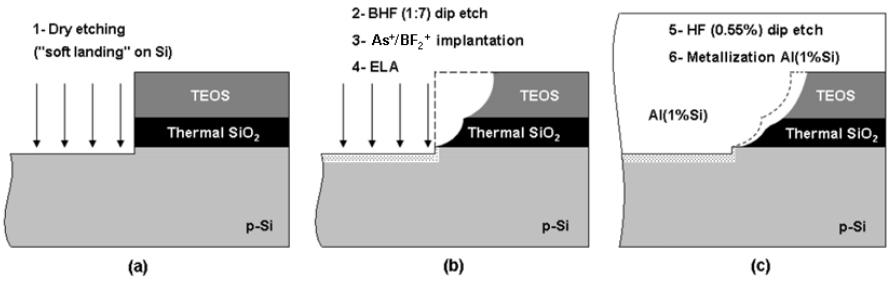


Figure 2.14: Zoom-in of the right corner contact window during the process fabrication. (a) Contact window after dry etching ("soft landing" on Si) (b) BHF (1:7) dip etch, As^+ implantation and excimer laser annealing giving the first enlargement of the contact window in the lateral direction. (c) HF (0.55%) dip etch and metallization giving the second enlargement of the contact window in the lateral direction.

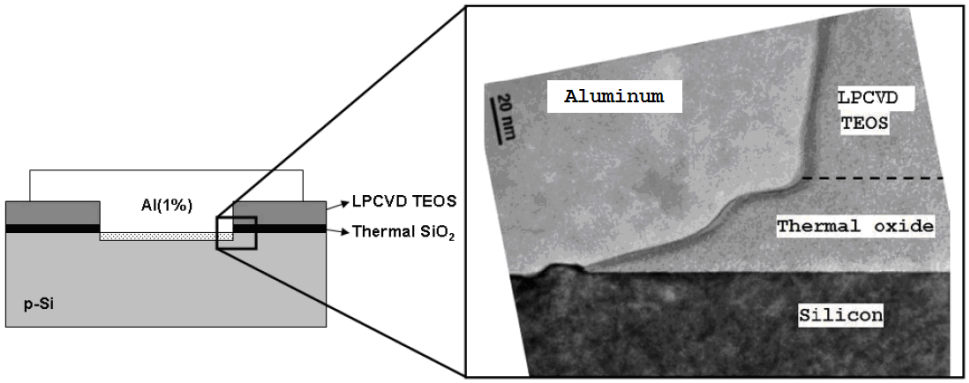


Figure 2.15: TEM image of the right corner contact window [88, 97].

2.6.2 Electrical devices characterization

Previous work has shown good electrical characteristics of laser-annealed junctions [88, 106]. The quality of the ultrashallow n^+p junctions was evaluated here by examining the reverse leakage current and the ideality of the forward current-voltage characteristics using a HP4156B parameter analyzer. The I-V characteristics of the As^+-implanted diodes laser-annealed with an energy density of 1000 mJ/cm^2 are shown in Figure 2.16. The measurements were taken at 100 ºC in order to reduce the relative influence of the leakage current from Shockley-Read-Hall recombination (also called Recombination through defects) on the diode current in the forward region. From the I-V characteristics in the reverse region, the diodes implanted at 7º with a dose of $2x10^{15}$ cm^{-2} suffer from high leakage, which can be attributed to the oxide recess at the edge of the contact hole, as presented in Figures 2.14 and 2.15. A reduction of leakage is achieved by either increasing the implanted dose from $2x10^{15}$ cm^{-2} to $3x10^{15}$ cm^{-2} or by increasing the tilt angle from 7º to 30º. Plausibly the increase to 30° shifts the junction perimeter further underneath the isolation oxide preventing the exposure of the junction edge during the pre-metallization dip in BHF(1:7). For implantation at 7°, increasing the dose can have the same effect and, moreover, the higher dopant concentration can also be more effective in limiting the spread of the depletion into the n-region. The energy transferred to the substrate by laser illumination melts the amorphized region which then recrystallizes where the melt zone has extended to the amorphous-crystalline interface. At the perimeter of the diodes the heat transfer to the substrate may be larger than in the middle because the surrounding silicon mass that can absorb the heat is effectively larger. This would mean a less

effective melting of the edge of the diode. Such an effect is probably the cause of the darker edge region seen in the TEM image of Figure 2.10. These regions suggest that there might be some non-annealed point defects near the junction edges, and it is possible that these defects also contribute to a higher leakage along the diode perimeter [104]. This is substantiated by an area/perimeter analysis of diodes of different sizes. Typical characteristics shown in Figure 2.16 for diodes with sizes 2 x 40 μm^2 and 4 x 20 μm^2, where the comparison shows that the latter diode with the smaller perimeter is less leaky. When the diodes are biased in forward, the influence of the residual defects can be identified as a deviation of the slope of the I-V characteristics from that of an ideal diode with ideality factor n = 1. The extracted values of n, as well as the reverse leakage current at -2 V for the four diodes from Figure 2.16 are summarized in Table 2.3. The larger ideality factors correspond to the diodes with larger leakage in the reverse region and nearly ideal values are obtained for the diodes implanted at 7° to a dose of $3x10^{15}$ cm^{-2} or at 30° and $2x10^{15}$ cm^{-2}. The area component of the current at a forward bias of 0.3 V is extracted from the measurements of diodes with different dimensions and the results are given in Table 2.4. As is evident from the extracted values, the largest area component of the current is achieved for the diode implanted at 30° to a dose of $2x10^{15}$ cm^{-2}, which is the diode with the shallowest junction. With the scaling down of junction depth to the sub-20 nm range the holes injected into the cathode from the p-substrate travel a very short distance before being recombined at the Al/Si(1%)-Si interface, which can result in a hole current that starts to become comparable to the current of electrons injected from the cathode. On the other hand, the electron current has little dependency on the junction

depth since the active doping level inside the n^+ region is close to the maximum that can be achieved and the relative change of the width of the p-side of the junction with the junction depth is insignificant. In accordance, the high area component of the forward current confirms that the 30°, $2x10^{15}$ cm^{-2} junction is very shallow and has a hole current of the same order of magnitude as the electron current. The hole current can therefore not be neglected.

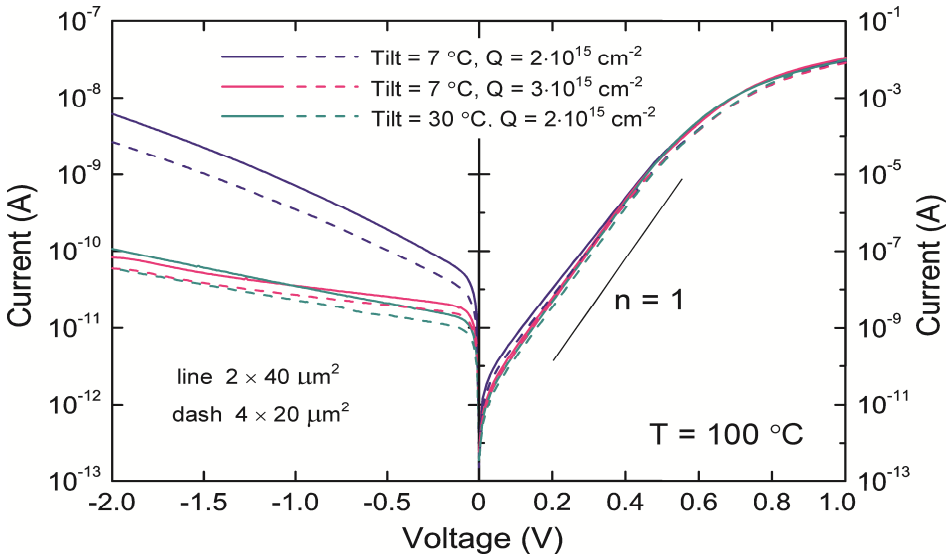


Figure 2.16: Current-voltage characteristics of n^+p diodes laser annealed at 1000 mJ/cm^2, for various implantation doses Q and tilt angles.

Table 2.3: Ideality factors and reverse leakage currents extracted at V = -2 V for the six diode measurements plotted in Figure 2.16. The measurements used for extraction were performed at 100 ºC.

Implantation (tilt angle)	Implantation dose (cm^{-2})	Size (μm^2)	Ideality factor	Reverse current at V = -2 V (A)
7º	$2 \cdot 10^{15}$	2 x 40	1.13	$6.2 \cdot 10^{-9}$
		4 x 20	1.12	$2.7 \cdot 10^{-9}$
7º	$3 \cdot 10^{15}$	2 x 40	1.05	$8.3 \cdot 10^{-11}$
		4 x 20	1.04	$5.9 \cdot 10^{-11}$
30º	$2 \cdot 10^{15}$	2 x 40	1.04	$10.7 \cdot 10^{-11}$
		4 x 20	1.04	$5.9 \cdot 10^{-11}$

Table 2.4: Area component of the current extracted at V = 0.3 V at the temperature of 100 ºC.

Implantation (tilt angle)	Implantation dose (cm^{-2})	Area component at V = 0.3 V ($A/\mu m^2$)
7º	$2 \cdot 10^{15}$	$2.90 \cdot 10^{-10}$
7º	$3 \cdot 10^{15}$	$2.62 \cdot 10^{-10}$
30º	$2 \cdot 10^{15}$	$8.96 \cdot 10^{-10}$

2.7 Conclusions

A simple, low-temperature process flow for achieving good quality ultrashallow n^+p junction diodes has been demonstrated for 5 keV As^+ implants activated by excimer laser annealing. With respect to the bulk laterally-uniform part of the diode away from the perimeter, it is important that the Si-surface to be implanted is smooth and native-oxide free before implantation. The implant should be so shallow that the melt region

encompasses the whole implanted region but deep enough to avoid laser-induced-surface-structuring effects on the Si surface from affecting the perfection of the underlying metallurgic junction region. Tilted implants can reduce the final junction depth of the 5 keV implants to below 20 nm. With respect to the perimeter of the diode, the key to achieving good quality diodes is the ability to terminate the metallurgic junction at an oxide-to-silicon interface that is of good quality. In these experiments this is achieved by using a thin layer of thermal oxide to cover the Si under a thicker low-temperature isolation layer. After the growth of the isolation oxide, all processing steps are performed at temperatures below 400 ºC. Here a 30-nm-thin thermal oxide is applied, which is still sufficiently thick to avoid excessive widening of the contact window during the dip-etch used to remove native oxide before metallization. To localize the laser melting of the silicon to the desired diode region and particularly to protect the perimeter, a reflective mask of Al is applied. A thin layer of Al is used together with one-shot laser annealing to avoid problems with the post-laser-annealing Al morphology. Tilted implants increase the overlap of the oxide isolation with the diode perimeter, thus making the process more robust and reducing perimeter leakage. The completeness of the laser melt at the perimeter will depend on the thermal conductivity of the surroundings. In the present experiments, less melting of the perimeter with respect to the bulk is identified by TEM analysis and this may be a source of extra perimeter leakage that should be taken into account when designing a specific process flow and diode structure. The best results are achieved here with an implant of $2x10^{15}$ cm^{-2} at tilt of 30°. For diodes with an area 80 um^2 this gives an ideality factor of 1.04 and reverse leakage at 2 V in 10^{-5}

A/cm^{-2} range. With these results, diodes with an ultrashallow junction implantation can be fabricated using the laser annealing technique and further results will show the possibility to apply this processing to source and drain junction formation in the D-DotFET device.

Chapter 3

Metal-Insulator-Semiconductor Capacitors

The low-temperature processing needed for the processing of the DotFET transistor puts heavy requirement on the processing temperature of the gate dielectric which conventionally is a high-quality thermal oxide grown at temperatures above 850 °C. In this chapter a study is presented of a number of dielectric layer-stacks deposited or grown at temperatures below 400 °C that could potentially be used as DotFET gate material.

3.1 Extraction of MIS capacitor parameters

Capacitance-Voltage (C-V) measurements are commonly used to evaluate the quality of gate dielectrics. In Figure 3.1 the C-V curve is shown of a p-type MIS capacitor measured at high and low frequencies. For an n-type MIS capacitor the curve is the mirrored version of that of the p-type MIS capacitor.

Basicaly, three modes of operation are observed in a p-type MIS C-V measurement:

- **the accumulation region** is seen where negative voltage is applied between metal and semiconductor and no depletion is formed. Holes will be attracted to and gather at the oxide-semiconductor interface due the negative charge of metal. Since majority carriers accumulate at the interface between the semiconductor and the oxide, the capacitance over the dielectric is measured in the strong accumulation region.

- **the depletion region** occurs when a positive voltage is applied between the metal and semiconductor and majority carriers (holes) are depleted at the oxide-semiconductor surface.

- **the inversion region** is seen when the metal gate voltage has become so positive that minority carries (electrons) are attracted to the oxide semiconductor interface. The minority carriers thus accumulated form the so- called inversion layer.

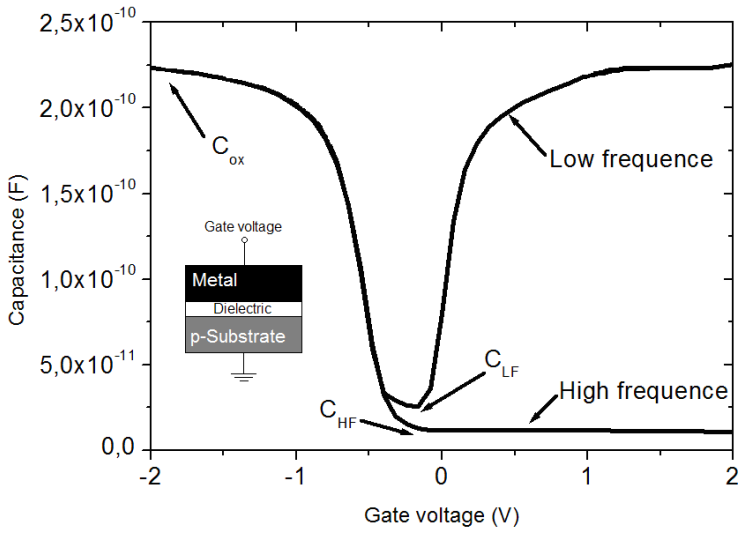


Figure 3.1: C-V curve of a p-type MIS capacitor measured at high and low frequencies.

From the C-V measurements it is possible to calculate parameters such as the gate dielectric thickness (see Chapter 1, equation 1.7), the density of effective charges in the gate dielectric (Q_{ss}/q), and the interface trap level density (D_{it}), which are important parameters for characterizing the SiO_2/Si structure. The following equations are applied [107]:

The Q_{ss}/q can be calculated using the following sequence of three groups of equations:

1- The impurity concentration of the substrate is found by:

$$N_{sub} = \frac{4|\phi f|}{q\varepsilon_0\varepsilon_{Si}}\left(\frac{C_{\min}}{A}\right)^2 \ [1/\mathrm{cm}^3] \qquad (3.1)$$

$$\phi f = \pm \frac{kT}{q} \ln\left(\frac{N_{sub}}{n_i}\right) \text{ [V]} \quad \begin{matrix} + : p-type(NMOS) \\ - : n-type(PMOS) \end{matrix} \tag{3.2}$$

where ϕf is the is the Fermi potential, $C_{min.}$ is the minimum depletion layer capacitance, q is the magnitude of electronic charge, and n_i is the intrinsic carrier concentration. The two equations can be used iteratively using the method of successive approximations.

2- The V_{FB} can be determined graphically by first calculating the flat band capacitance (C_{fb}) and then reading the value of V_{FB} off of the C-V curve:

$$C_{fb} = \frac{C_{ox} C_{sfb}}{C_{ox} + C_{sfb}} \text{ [F]} \tag{3.3}$$

$$C_{sfb} = \frac{\sqrt{2} A \varepsilon_0 \varepsilon_{Si}}{\lambda} \text{ [F]} \tag{3.4}$$

where C_{sfb} is the depletion layer capacitance, and λ is the Debye length;

3- The effective charges in the gate dielectric are then given by:

$$\frac{Q_{ss}}{q} = \frac{C_{ox}}{Aq} \left| \phi_M - V_{FB} \right| \text{ [1/cm}^3\text{]} \tag{3.5}$$

where ϕ_M is the is the difference in the work functions of the semiconductor (Si) and the metal gate;

The D_{it} can be estimated using the high and low frequency at room temperature [107]:

$$D_{it} = \frac{C_{ox}}{Aq}\left(\frac{C_{LF}}{C_{ox}-C_{LF}} - \frac{C_{HF}}{C_{ox}-C_{HF}}\right) \quad [\text{cm}^2\text{-eV}]^{-1} \qquad (3.6)$$

where C_{LF} is the minimum value of the capacitance, and C_{HF} is the high-frequency capacitance at the voltage corresponding to C_{LF} .

3.2 The fabricated high-*k* dielectrics

As discussed in Section 1.1.1, silicon dioxide has been used for decades as a gate dielectric, but with the downsizing of CMOS devices, a thinning of the physical equivalent gate oxide thickness to less than 1nm is necessary and the direct-tunneling leakage current in a pure silicon oxide dielectric layer would increase to excessive levels [108]. To overcome this problem new materials with high-k have been attracting much attention. By replacing the traditional silicon oxide with high-k materials it is possible obtain the same EOT but with a thicker dielectric layer. Currently, several metal-oxide gate dielectrics are promising candidates for high-k isolation and hafnium oxide (HfO_2) is the most popular material used today [109, 110]. In the Dimes facilities three materials are available for use as gate-dielectric: silicon oxide, silicon oxynitride and aluminium oxide

(Alumina- Al_2O_3). For monitoring gain enhancement in DotFETs it is an advantage to have the highest possible coupling between the gate and channel combined with the lowest possible leakage. Therefore, pure silicon oxide as gate material is less interesting and focus was placed on developing other low-temperature dielectrics, in particular, SiO_xN_y grown by inductively coupled plasma (ICP) and Al_2O_3 deposited by atomic-layer deposition (ALD). Both processes could be processed at temperatures below 400^{o}C were studied.

In Figure 3.2 the basic process flow is illustrated for the fabrication of Al/capacitors with the investigated dielectric layer stacks. All results reported in the rest of this Chapter are for capacitors fabricated on (100) 2-5 Ωcm p-type Si wafers. Before deposition of the dielectric layer stack to be studied, the substrates were cleaned by a 4 min HF (0.55%) dip-etch for oxide removal. After the dielectric deposition, a 375 nm thick Al was deposited by sputtering and patterned by conventional optical lithography using i-line combined with RIE to define capacitors of different sizes. On the back of the wafer a 675 nm Al layer was sputtered to form a low-ohmic contact to this terminal. The samples were sintered in a conventional furnace in forming gas at 400 ^{o}C for 20 min.

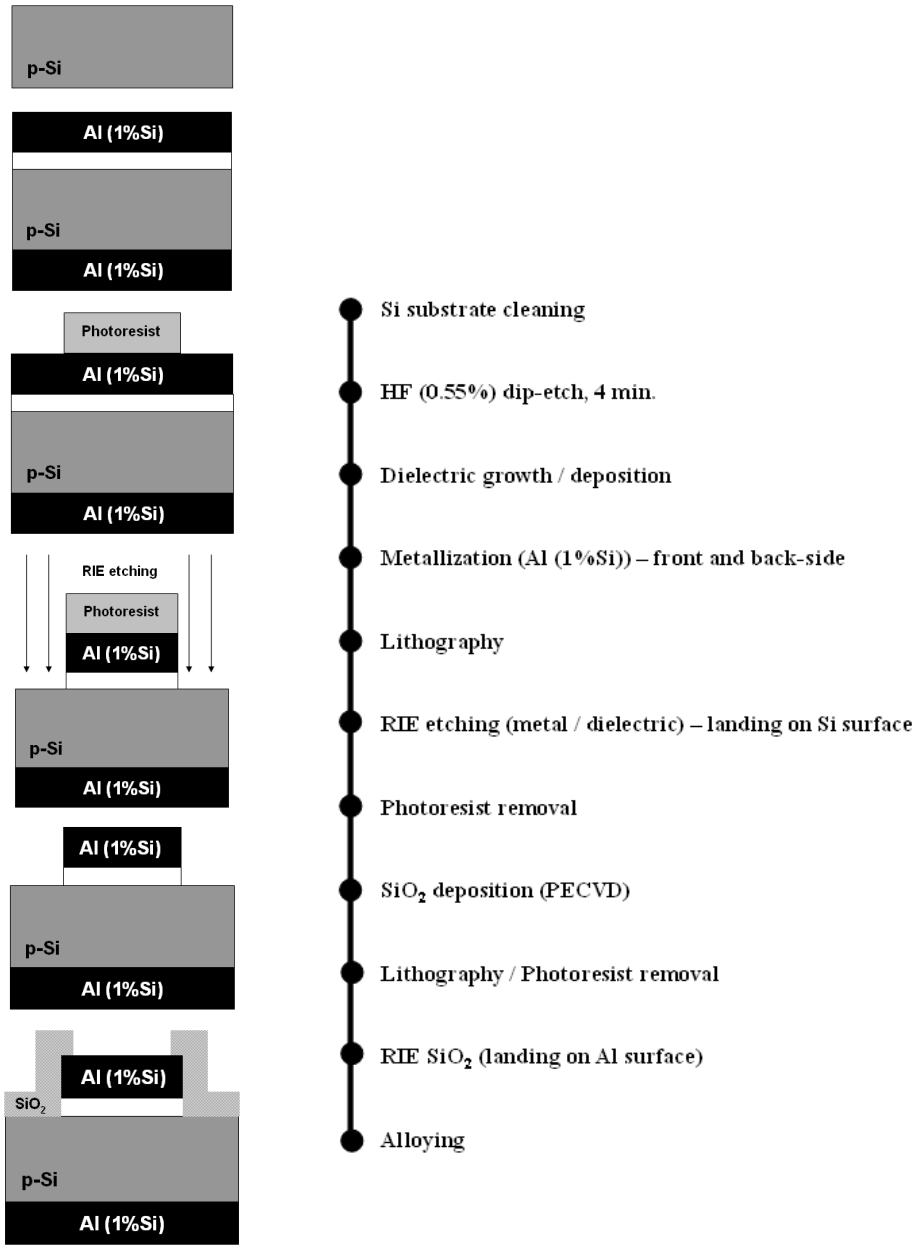


Figure 3.2: Basic process flow for the fabrication of the investigated capacitors.

3.2.1 ICP SiO_xN_y

Many works have explored the use of silicon oxynitride films as antireflective layer [111], membranes for Micro-Electro-Mechanical Systems (MEMS) [112], optical waveguide [113] and gate dielectric applications [114]. For the latter application, it has been proven that SiO_xN_y films may extend the limit of the oxide thickness a little further. In particular, nitridation has been shown to be beneficial for reduction of leakage current, enhancement of reliability, and for suppression of Boron penetration. Usually, the silicon oxynitride films are deposited by low-pressure chemical vapor deposition or PECVD at temperatures higher than either 600°C or 250°C, respectively [115-118]. Depending on the growth parameters, different compositions of silicon oxynitride can be obtained. For example, by reducing nitrogen gas flow in the process chamber, the dielectric constant of the films is also reduced due the low concentration of N [119] and the material can become comparable to thermal oxide with excellent characteristics for gate dielectric applications. However, the high processing temperatures can make these depositions incompatible with other fabrication steps. High-density plasma sources, such as inductively coupled plasma systems, have advantages over conventional low density plasmas for thin film deposition. In the ICP system high-density plasma is available, allowing a high-quality SiO_2 and SiO_xN_y growth and deposition at low temperature. Such ICP systems can operate at low pressures (here, 2.5 Pa). In our reactor, a 13.56 MHz RF power source generates the plasma at high powers (up to 1000 W). For the silicon oxynitride growth (without silane in the gas mixture), and mixture of helium (He), oxygen (O_2) and nitrogen (N_2)

gases is injected in the plasma chamber. Using activated oxygen and nitrogen species which can react with Si surfaces to form SiOxNy at low temperatures (< 500 °C). The Si interfaces were characterized to show the feasibility for the application to MOSFET devices. The growth processes were carried out at a pressure of 2.5 Pa, with both N_2 and O_2 flow rates set at 7.5 standard cubic centimeters per minute or sccm, the He flow rate of 30 sccm and 13.56 RF power of 500 W. The substrate temperature, was fixed at 250 °C. The films that were grown in the ICP system were approximately 18 nm thick, corresponding to a growth rate of 3.6 nm/min, and they were used to fabricate Al/SiO_xN_y/Si capacitors according to the flowchart given in Figure 3.2.

3.2.2 ALD Al_2O_3

Alumina is an attractive material for use as gate dielectric due the high dielectric constant of $k \sim 10$. Aluminium oxide films have been prepared by various techniques such as chemical vapor deposition,metal-organic chemical vapor deposition, thermal evaporation, sputtering, atomic-layer deposition, pulse laser deposition and many others [120-123]. ALD was originally introduced in the early 1970s by Dr. Tuomo Suntola, at the University of Helsinki in Finland [124]. The process can be performed at low temperatures and the resulting films show excellent uniformity, conformality, precise thickness control due to the layer-by-layer deposition and the deposition of high-quality of gate dielectrics is possible [125-127]. The ALD process is based in a sequential deposition of monolayers (adsorption of monolayers on the surface) where two or more precursors are

used. The precursors are introduced into the chamber alternately, controlled by a high actuation speed valve and a vacuum pumping control of the pressure. After each precursor pulse, a rapid purging of the chamber is performed. Here the ASM F120 ALD reactor was used for Al_2O_3 depositions that were carried out at a substrate temperature of 300°C using trimethylaluminium (TMA) and water as precursors. A typical cycle for Al_2O_3 deposition is:

- one pulse of metal precursor;
- purging pulse;
- one pulse of water;
- purging pulse.

The growth processes were carried out at pressures of 133 Pa and the substrate temperature was fixed at 300°C. After 70 cycles the Al_2O_3 thickness was approximately 7-8 nm, with a deposition rate of 1-1.1nm/cycle. The layers were used to fabricate $Al/Al_2O_3/Si$ and Al/Al_2O_3-SiO_xN_y/Si capacitors according to the flowchart given in Figure 3.2.

3.3 Electrical capacitor characterization

3.3.1 Single-gate dielectrics

The fabricated $Al/SiO_xN_y/Si$ and $Al/Al_2O_3/Si$ capacitors were electrically measured by performing C-V sweeps with

a HP4284 LCR meter at both low and high frequencies – 100 Hz and 1 MHz. The equivalent oxide thickness and interface trap level density were extracted from the resulting C-V curves. These are plotted in Figures 3.3 and 3.4 for Al/SiO_xN_y/Si and Al/Al_2O_3/Si capacitors, respectively.

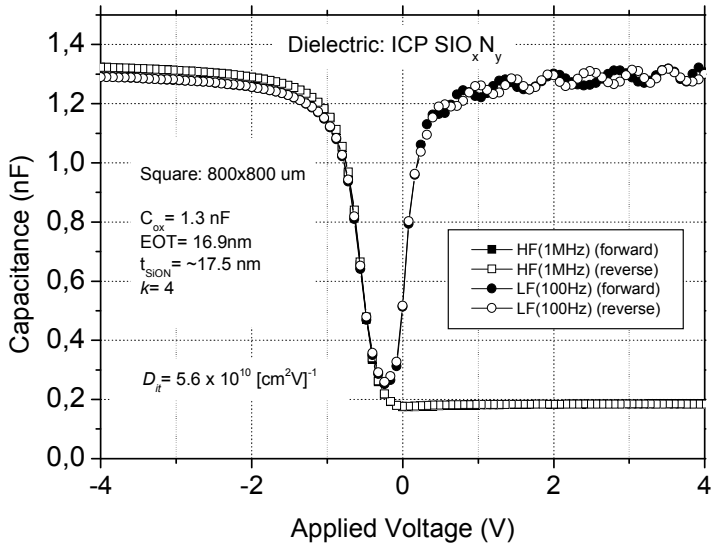


Figure 3.3: C-V characteristics of a capacitor with ICP SiO_xN_y grown at 250°C. The capacitor is square-shaped with a size of 800 μm × 800 μm.

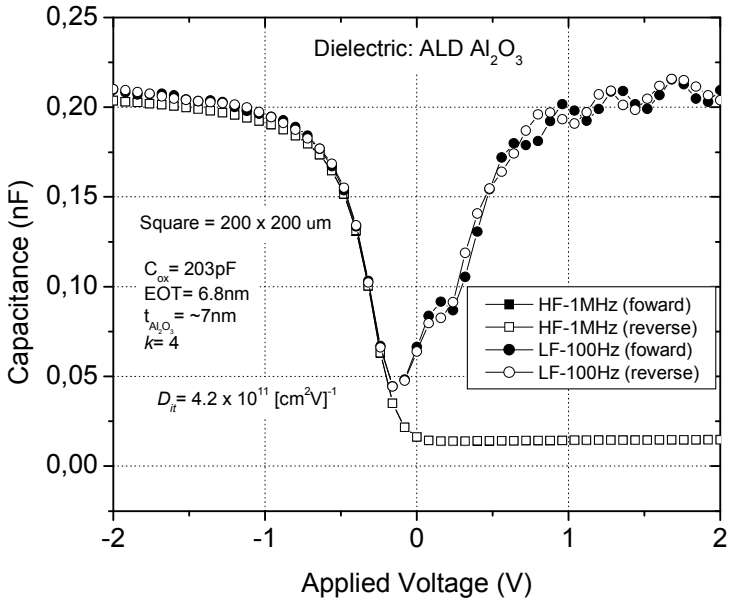


Figure 3.4: C-V characteristics of a capacitor with ALD Al_2O_3 deposited at 300^{o}C. The capacitor is square-shaped with a size of 200 μm × 200 μm.

The C-V characteristics of 800 x 800 μm^2 capacitors with silicon oxynitrides grown by ICP at low temperature (250 ^{o}C) showed no hysteresis and exhibited an EOT of 16.9 nm and a dielectric constant of 4. This value is slightly higher than the silicon oxide dielectric constant of 3.9, indicating oxynitride formation due to a small amount of N in the film [119]. An interface trap level density of 5.6x10^{10} cm^{-2}eV^{-1} and the effective charge density of 7.6x10^{11} cm^{-2}eV^{-1} were calculated.

The C-V characteristics of 200 x 200 μm^2 capacitors made with Al_2O_3 deposited by ALD at 300 ^oC showed no hysteresis, exhibited an EOT of 6.8 nm and a dielectric constant of 4. The dielectric constant of Al_2O_3 is about 10 and the low dielectric constant (~ 4) of the thin Al_2O_3 can be attributed to an interfacial native layer formed prior to the atomic-layer deposition of Al_2O_3 on Si substrate. Such an interfacial layer with very low dielectric constant due to the low density of the film, can be instrumental in creating an overall low dielectric constant of Al_2O_3 thin film. A density interface trap level density of $4.2x10^{11}$ $cm^{-2}eV^{-1}$ was calculated but a high D_{it} is observed for Al_2O_3 capacitors deposited by ALD as compared to SiO_xN_y. This high D_{it} on Al_2O_3 capacitors can be attributed to the low quality of the interfacial native layer grown on Si which degrades the electrical properties [128].

3.3.2 Double-gate dielectrics

Since the SiO_2 and SiO_xN_y layers exhibit electrical dielectric characteristics that are suitable for use as gate dielectrics and are also known to have a good stability on Si for this application, double gate stacks incorporating a first layer of these materials were also fabricated and characterized. Specifically, Al/Al_2O_3-SiO_xN_y/Si and Al/Al_2O_3-SiO_2/Si capacitors were also fabricated and electrically characterized by capacitance-voltage measurements. The SiO_xN_y interface layers were grown using the same parameters as specified in Section 3.1.1. The SiO_2 interface layers were grown in a furnace for 1 hour and 20 minutes at 700ºC to form a very thin thermal oxide layer. The Al_2O_3 film was deposited by ALD, 70

pulses (~ 7 nm), and the SiO_xN_y layer grown by ICP (~ 6 nm), and a thermal SiO_2 layer was grown in a furnace at 700°C (~ 1-1.5 nm). The thickness of the thermal SiO_2 interface layer was calculated by the Massoud model [129, 130], because the Deal-Grove model [131] cannot satisfactorily describe thin-film oxidations. The C-V characteristics of Al/Al_2O_3-SiO_xN_y/Si and Al/Al_2O_3-SiO_2/Si capacitors are shown in Figures 3.5 and 3.6, respectively.

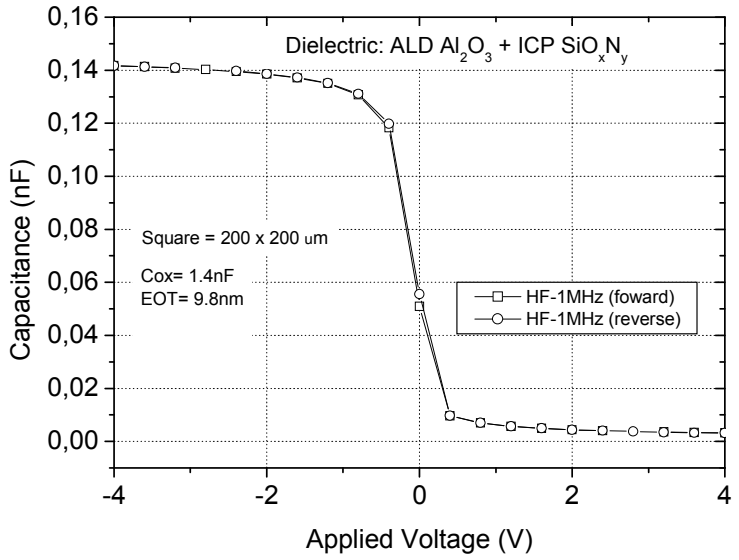


Figure 3.5: C-V characteristics of a capacitor with ICP SiO_xN_y grown at 250°C and ALD Al_2O_3 deposited at 300°C. The capacitor is square-shaped with a size of 200 μm x 200 μm.

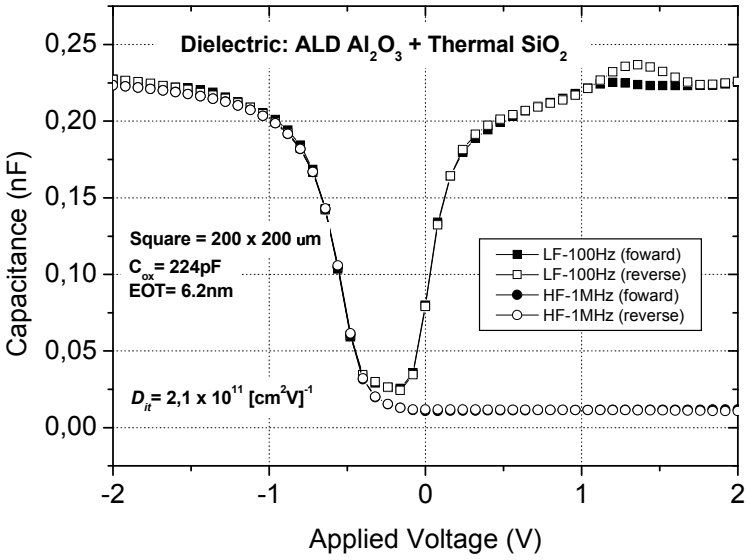


Figure 3.6: C-V characteristics of a capacitor with thermal SiO_2 grown at 700°C and ALD Al_2O_3 deposited at 300°C. The capacitor is square-shaped with a size of 200 μm × 200 μm.

The C-V characteristics of 200 x 200 μm^2 capacitors with an extra interface layer showed no hysteresis. The Al/Al_2O_3-SiO_xN_y/Si capacitors exhibited an EOT of 9.8 nm and the Al/Al_2O_3-SiO_2/Si capacitors exhibited an EOT of 6.2 nm and D_{it} of $2.1x10^{11}$ $cm^{-2}eV^{-1}$. The C-V curves at low frequency could not be measured for Al/Al_2O_3-SiO_xN_y/Si capacitors. The comparison of D_{it} values for capacitors with and without interface dielectric layers shows that the interface layer significantly improves the quality of the capacitors including a reduction of interface trap level density.

In order to calculate the dielectric constant of the high-*k* dielectric layer this formula is applied:

$$EOT = t_{ox} + \left(\frac{k_{ox}}{k_{high-k}} \right) t_{high-k} \tag{3.7}$$

where k_{ox} is the dielectric constant of the interface layer, $k_{high\text{-}k}$ is the dielectric constant of the high-*k* dielectric layer and $t_{high\text{-}k}$ is the thickness of high-*k* dielectric layer.

The Al_2O_3 films deposited on either ICP SiO_xN_y or thermal SiO_2 films exhibited a dielectric constant of approximately 7 and 8, respectively, which is about the double of the silicon oxide dielectric constant of 3.9. Thus, the high-*k* dielectric nature of the film is evident. In Table 3.1 a compilation is given of the parameters extracted from the C-V measurements.

Table 3.1 Gate dielectric parameter extracted from C-V measurements

Gate dielectric	**SiO_xN_y**	**Al_2O_3**	**Al_2O_3 + SiO_xN_y**	**Al_2O_3+Thermal SiO_2**
Area (μm^2)	800 x 800	200 x 200	200 x 200	200 x 200
EOT (nm)	16.9	6.8	9.8	6.2
C_{ac} (pF)	1300	203	140	224
Q_{ss}/q [1/cm^3]	7.6×10^{11}	1.9×10^{12}	1.31×10^{12}	2.09×10^{12}
D_{it} [cm^2-eV]$^{-1}$	5.6×10^{10}	4.2×10^{11}	-	2.1×10^{11}

3.3.3 Current-Voltage characteristics

The above described capacitors were electrically characterized by current-voltage (I-V) measurements using a HP4156B parameter analyzer. with 800 x 800 μm^2 and 200 x 200 μm^2 areas The Table 3.2 shows the current density results of the capacitors. The leakage current was measured at a gate voltage (V_G) of -1 V in accumulation region.

Table 3.2: J-V results of the capacitors fabricated.

Gate dielectric	**SiO_xN_y**	**Al_2O_3**	**Al_2O_3 + SiO_xN_y**	**Al_2O_3 + Thermal SiO_2**
Area (μm^2)	800 x 800	200 x 200	200 x 200	200 x 200
EOT (nm)	16.9	6.8	9.8	6.2
Density leakage current (A/cm^2) at V_G= -1V (avg.)	$25.7x10^{-8}$	$25.5x10^{-8}$	$40.2x10^{-8}$	$19.6x10^{-8}$

The leakage current density of the sample with thermal SiO_2 interface layer is a bit lower than the others, which substantiates the known good quality of thermal SiO_2/Si interfaces. However, for all capacitors fabricated a low density leakage current in order of 10^{-7} A/cm^2 was measured.

3.3.4 Summary of MIS capacitor properties

To summarize the results of the electrical measurements for MIS capacitors fabricated with single and double gate dielectric, Table 3.3 lists

all the parameters extracted from the electrical results obtained from the C-V and I-V measurements.

Table 3.3: Summary of the electrical parameters for MIS capacitors.

Gate dielectric	**SiO_xN_y**	**Al_2O_3**	**Al_2O_3 + SiO_xN_y**	**Al_2O_3 + Thermal SiO_2**
Area (μm^2)	800 x 800	200 x 200	200 x 200	200 x 200
EOT (nm)	16.9	6.8	9.8	6.2
C_{ac} (pF)	1300	203	140	224
D_{it} (cm^2-eV)$^{-1}$	$5.6x10^{10}$	$4.2x10^{11}$	-	$2.1x10^{11}$
Q_{ss}/q [1/cm^3]	$7.6x10^{11}$	$1.9\ x10^{12}$	$1.31\ x10^{12}$	$2.09\ x10^{12}$
Density leakage current (A/cm^2) at V_G= -1V (avg.)	$25.7x10^{-8}$	$25.5x10^{-8}$	$40.2x10^{-8}$	$19.6x10^{-8}$

3.4 Conclusions

In this Chapter, MIS capacitors were fabricated at low temperature ($\leq 400^oC$) with different gate-dielectric layer stacks and electrically characterized. A comparison was also made to capacitors with an SiO_2 interface layer thermally-grown at $\leq 700^oC$. It was chosen to investigate atomic-layer deposited Al_2O_3 layers because this technique gives an excellent uniformity, conformality, precise control of the thickness of the films, and it is possible to deposit high quality layers at low temperature. Cycles of TMA and water were applied in order to deposit the Al_2O_3 layers at a temperature of 300 ^oC. The SiO_xN_y films with a low concentration of N were grown by inductively coupled plasma at a temperature of 250 ^oC.

The capacitance-voltage and current-voltage characteristics were measured for different gate stacks. The results demonstrated that ALD Al_2O_3 and ICP SiO_xN_y exhibited a dielectric constant of 4 and 8, respectively. With ICP SiO_xN_y, capacitors were fabricated with low interface trap level density and low effective charge density, $< 10^{11}$ $cm^{-2}eV^{-1}$ and $<10^{11}$ $cm^{-3}eV^{-1}$, respectively, as well as low leakage current density ($< 10^{-7}$ A/cm^2).

For Al_2O_3 layers the interface quality to Si was poor. In order to improve this situation, a high-quality interface layer was either grown or deposited between the alumina and Si substrate. The quality of the interface layer is beneficial for the physical interface properties and consequently improves the electrical characteristics. Due to the simple, fast processing and good quality of the ICP SiO_xN_y dielectric at low temperature, the SiO_xN_y was chosen for for the fabrication of the MOSFETs and DotFETs that are described in the following chapters.

Chapter 4

MISFET devices

This chapter combines the processing techniques described in Chapter 2 (the successful fabrication of n^+p diodes with ultrashallow junction annealed by excimer laser technique) and Chapter 3 (capacitors using Al_2O_3 and SiO_xN_y gate dielectrics deposited by atomic layer deposition and inductive coupled plasma, respectively, both processed at low temperatures $\leq 400^oC$) to create a simple MISFET device [132]. Moreover, a brief overview is given of the methods used to extract the electrical parameters of the MOSFETs. Two different types of MISFET structures are fabricated using the ultrashallow junctions to form the source/drain regions and the low temperature dielectrics in the gate-stack. The first type of MISFET has a ring-shaped gate and an existing mask-set of standard test structures is used for an initial testing of all the processing steps. The second type of MISFET is fabricated with a specially designed mask-set that was made in preparation of the technology transfer to the D-DotFET device structure.

4.1- Extraction of MOSFET parameters

A comparison of the fabricated p- and n-MISFET devices is made on the basis of the methods described in this section to extract the fundamental electrical parameters [133], which have already been summarized in Chapter 1.

a) Extraction of the I_{on} to I_{off} ratio

The on current, I_{on}, and off current, I_{off}, values are extracted from the V_{GS} versus log I_{DS} curve. The I_{on} is extracted for $V_{GS} = V_{DS} = V_{DD}$, where V_{DD} is the power supply voltage, and the I_{off} is extracted for $V_{GS} = 0$ and $V_{DS} = V_{DD}$. The Figure 4.1 shows an example of an V_{GS} versus log I_{DS} curve as used for the I_{on} and I_{off} extraction.

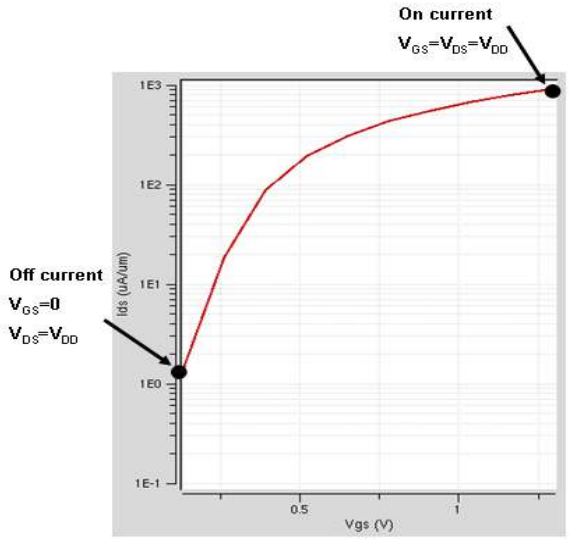


Figure 4.1: Example of V_{GS} versus log I_{DS} curve as used for I_{on} and I_{off} extraction.

b) Subthreshold Swing (*SS*) extraction

The subthreshold swing, *SS*, gives a measure for the dependence of the drain current I_{DS} on gate bias voltage V_{GS}. Typically, this parameter is extracted at high drain bias. In an ideal case, when the gate is biased below subthreshold conduction, the drain current decreases to zero. In reality, there is a drain current below the threshold voltage and this is know as the subthreshold current. The Figure 4.2 presents an example of an V_{GS} versus log I_{DS} curve where the extracted subthreshold swing is indicated.

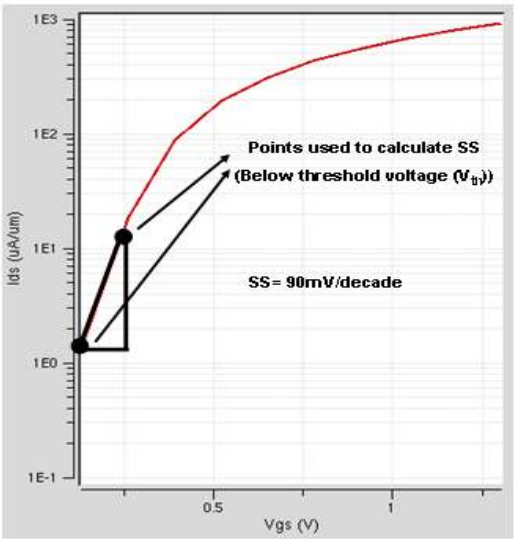


Figure 4.2: An example of an V_{GS} versus log I_{DS} curve and the extracted subthreshold swing (SS).

c) Extraction of the Drain Induced Barrier Lowering (DIBL)

The drain potential over the channel region can have a significant impact on the performance of the MOSFET devices in saturation. If a high drain voltage is applied, the drain channel depletion width can expand to the extend that it can cause a leakage current between source and drain. In this case the drain current is not controlled only by the gate voltage, but also by the drain voltage. This effect called DIBL can reduce the threshold voltage in a manner that is dependent on the drain voltage. DIBL can be calculated by extracting the horizontal shift in the subthreshold region divided by change in the drain voltage on the log I_{DS} versus V_{GS} plot. The Figure 4.3 shows an example of V_{GS} versus log I_{DS} curves where the extracted DIBL value is indicated.

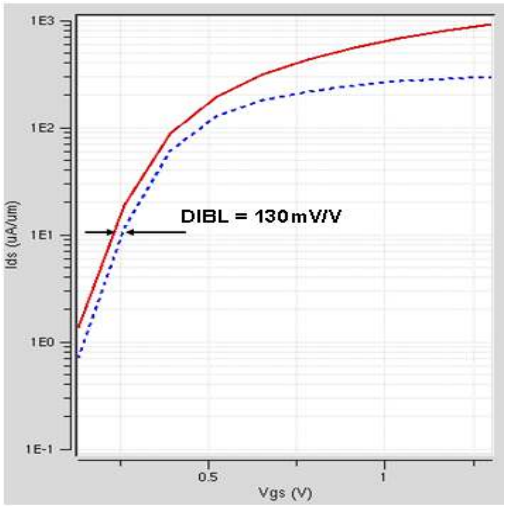


Figure 4.3: Example of V_{GS} versus log I_{DS} curves and the extracted DIBL value.

d) Threshold Voltage (V_{Th}) extraction

The threshold voltage is defined as the gate voltage at which an inversion layer is formed in the channel of the transistor at the interface between the gate dielectric and the silicon bulk. Basically, V_{Th} is the minimum voltage that is required to turn on the transistor MOS. The V_{Th} is obtained by extrapolating the I_{DS} versus V_{GS} curve, and the intersection point of the extrapolation to the V_G-axis is the V_{Th} (for $V_D << V_G$) (see Figure 4.4).

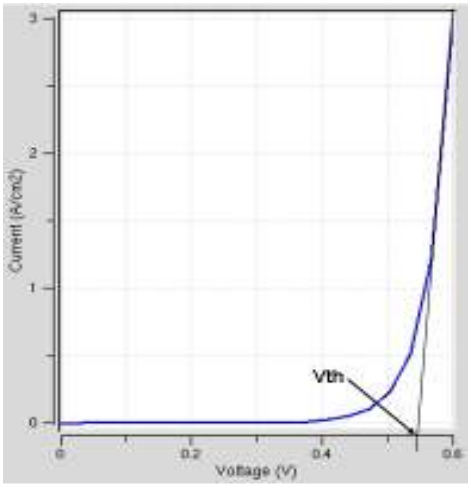


Figure 4.4: Example of I_{DS} versus V_{GS} curve for the V_{Th} extraction.

e) Extraction of the Total Resistance R_T

The total resistance can be described as the sum of channel resistance, R_{ch}, and source/drain resistance, $R_{S/D}$, by using the formula $R_T = R_{ch} + R_{S/D}$. The total resistance is calculated by taking the V_{DS} versus I_{DS} curve in the linear region. The $\Delta V_{DS} / \Delta I_{DS}$ value is the total resistance (see Figure 4.5).

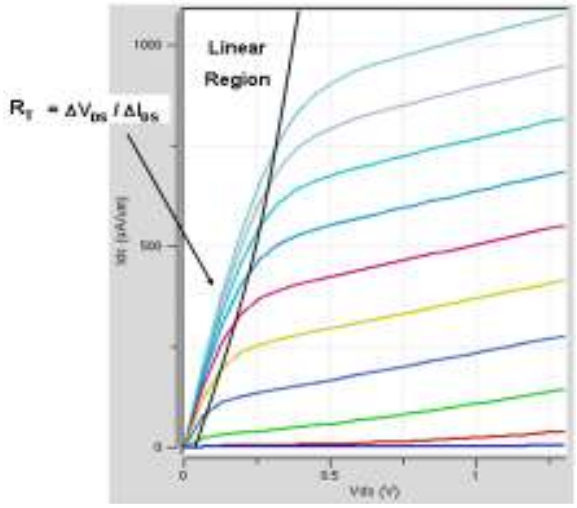


Figure 4.5: Example of a V_{DS} versus I_{DS} curve for the R_T extraction.

4.2 n-MISFET ring-gate test structures

The n-MISFET ring-gate structures were fabricated on silicon (100) p-type wafers with a resistivity of 2-5 Ωcm. The process flow for fabricating these structures is given in the following sub-sections.

a) Gate-stack formation

In Figure 4.6 the processing steps used to form a high-*k* gate stack are depicted. A silicon dioxide layer of 20 nm is grown by thermal oxidation of the silicon surface. Prior to the thermal oxidation, a HF (0.55%) dip-etch (4 minutes) is performed immediately before oxidation in order to remove the native oxide over the silicon surface. After oxidation a B^+ implantation to dope the bulk silicon is performed through the SiO_2 layer, by using a 40keV implant to a dose of $1x10^{11}$ cm^{-2}. The thermal SiO_2 is removed using

buffered-HF (1:7) until the front-side of the Si wafer is hydrophobic and the implanted layer is annealed in a furnace at 1000^{o}C for 30 minutes in an N_2 gas flow. Immediately before the gate-stack growth/deposition the Si wafer is cleaned and a 4 minutes HF (0.55%) dip-etch is performed. The wafers are transferred to the ICP chamber for oxynitride interface growth. The *high-k* gate dielectric is comprised of first a thin silicon oxynitride layer deposited by ICP at 250°C to achieve a high quality oxide interface to the silicon. Then an aluminium oxide layer was deposited by atomic layer deposition in 70 pulses with TMA and water as precursors at 300°C. A 13-15 nm oxynitride layer was grown on the Si surface followed by 7-8 nm of Al_2O_3. An Al(1%Si) metal-gate of a thickness of 375 nm was then sputtered at 50^{o}C because this gives a small Al-grain size which is necessary for achieving optimal reflectivity to laser light. As will be detailed in the following section, the Al-gate layer forms the reflective mask for the laser anneal processing in the manner described in Chapter 3.

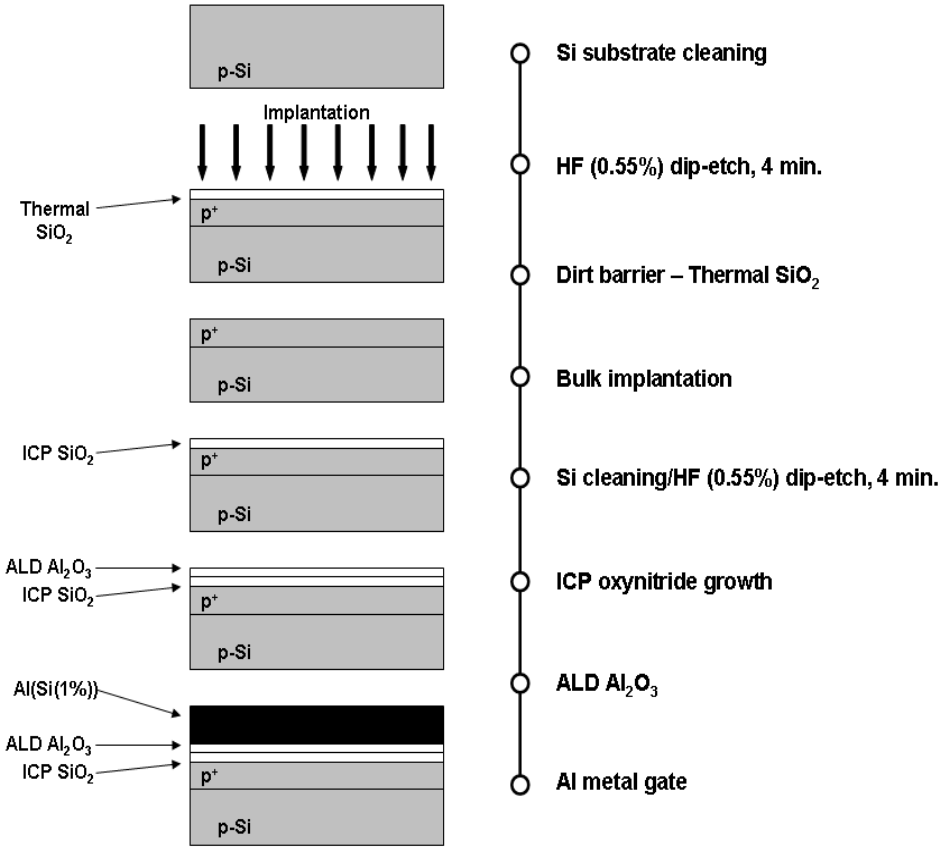


Figure 4.6: Process flow for the high-*k* gate stack formation.

b) Patterning of the gate and source/drain regions

When the dielectric gate and Al reflective mask have been deposited over the Si wafer, the gate and source/drain regions can be defined. Photoresist is deposited on the aluminium layer and the gate region is defined by illumination in the i-line waferstepper ASML PAS5500/80 which can define dimensions down to 500 nm and has an alignment accuracy of ≤ 70nm. Photoresist layers with a thickness of 1.4 μm were used for the pattern transfer. The correct exposure energy and focus are adjusted

for a good pattern transfer. Openings to the isolating/reflective stack are developed and followed by RIE of Al/Si(1%) and Al_2O_3 using hydrogen-bromide and chlorine plasmas and RIE of oxynitride using a fluorine-based plasma. As mentioned before, for ultrashallow junctions a possible etching of the substrate can alter junction characteristics. Therefore, to prevent damage to the silicon surface from the RIE process, the removal of the oxynitride isolation close to the Si surface is performed at lower RF power – 100 W. A 300 W RF power is used for a few seconds just to ignite the plasma. Then, the photoresist is removed in an oxygen plasma and a cleaning cycle is performed. The Figure 4.7 shows the process flow for the gate-stack patterning.

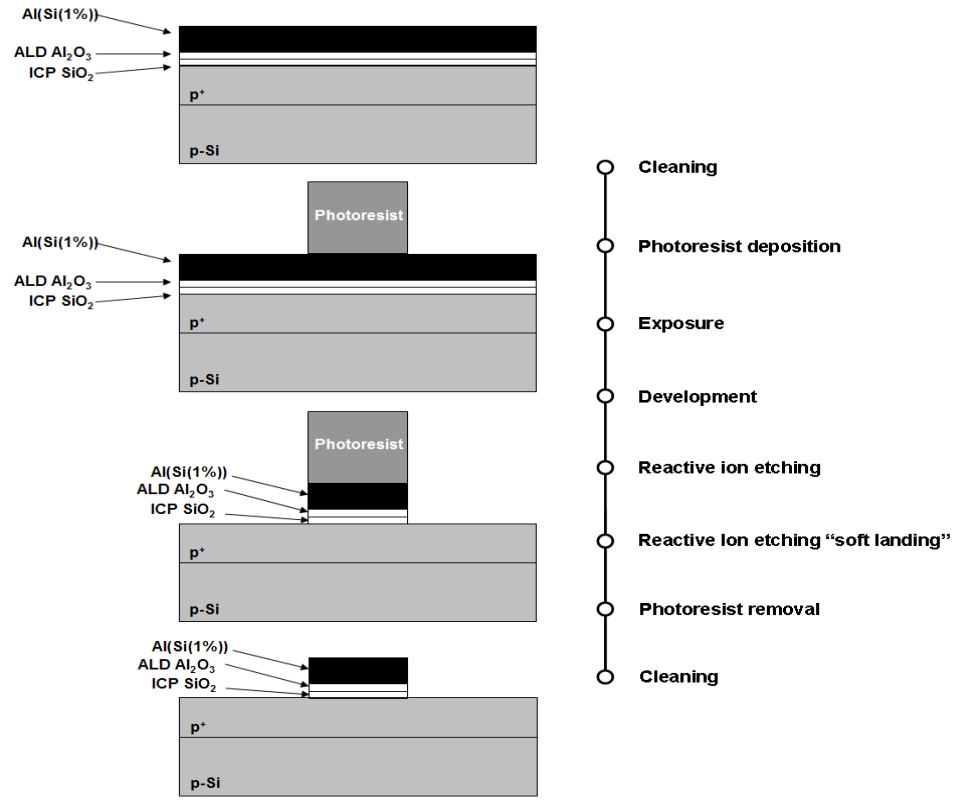


Figure 4.7: Process flow for the gate-stack patterning.

c) Low-energy implantation and laser annealing for ultrashallow source/drain formation

The next step after the gate and source/drain definition is the preparation of the source and drain region for low-energy implantation and laser annealing. As mentioned in Chapter 2, the native oxide on the silicon surface should be removed. Therefore, a 15 second dip in buffered-HF (1:7) solution is performed immediately before the low-energy implantation. During this step the aluminium gate is etched by the BHF solution, which is a self-stopping process that removes approximately 50 nm Al, leaving a sufficiently thick Al/Si(1%) layer to serve as reflective mask over the gate dielectric region. When decreasing the gate length to submicron dimensions the Al-gate can be etched completely during this pre-implant dip-etch step. In that case, the use of other metal-gate materials must be considered. An omission of the HF treatment before the source/drain implantation could also be considered but this would degrade the quality of the source/drain junction as already discussed in Chapter 2. Tests were nevertheless performed in this direction but, as expected, the resulting diodes were excessively leaky.

Implantation of arsenic ions at 5 keV to a dose of 10^{15} ions/cm^2 at 30^o tilt angle was performed immediately after dipping the wafers in a BHF(1:7) solution for 15 seconds. The implanted regions were then laser-annealed with the remaining Al gate layer serving as the reflective mask. The laser energy density was varied from 700 mJ/cm^2 to 1000 mJ/cm^2 in columns and in 50 mJ/cm^2 steps with 1% overlap. A homogenizer is used to produce a flat-top intensity profile over the 1.75 x 2.5 mm^2 spot. The Figure

4.8 shows the configuration applied for source/drain laser annealing on MISFET ring-gate structures.

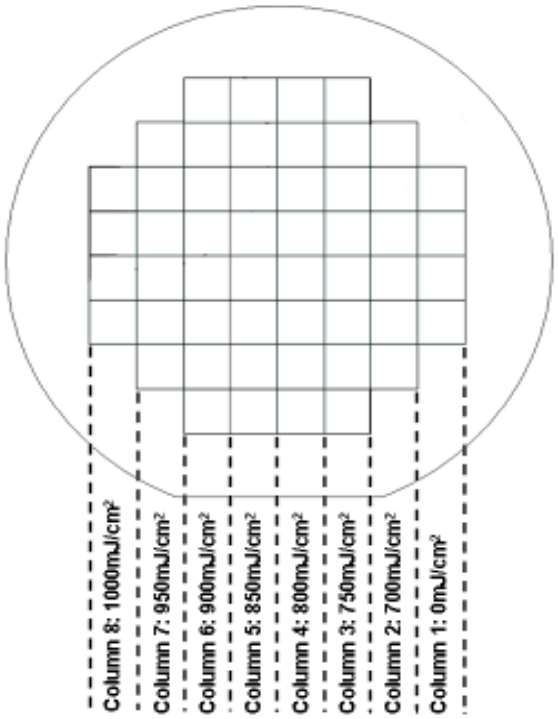


Figure 4.8: Configuration applied for source/drain laser annealing on MISFET ring-gate structures.

d) Contacts and metallization

After laser annealing, the wafers were cleaned and a 800-nm-thick isolation layer of PECVD SiO_2 was deposited at 400 ^{o}C. A photoresist layer of 1.4 µm is deposited and the source/drain contacts are defined by i-line waferstepper lithography. The SiO_2 layer is RIE etched down to the Si. To prevent damage to the silicon surface from the RIE process, the etching of the oxide isolation layer close to the Si surface is done at lower RF power.

A RF power of 300 W is used for the bulk SiO_2 etching and reduced to 100 W close to the Si implanted surface. The photoresist is then removed using O_2 plasma, a cleaning step is performed, and a 4 minutes HF (0.55%) dip-etch is done to remove the native oxide before metallization. A 905-nm-thick Al(1%Si) is then sputtered at 350 ^oC to contact the source/drain regions. The HF dip-etch must be performed immediately before the metallization to ensure reliable contacting.

After the source/drain metallization, the lithography of the gate contact window is performed. The aluminium and SiO_2 isolation layer are etched by RIE until reaching the Al metal gate, and after that a second Al(1%Si) metal layer of 1.4 μm is sputtered at 350 ^oC for gate contact. Finally, an additional lithography is used for interconnections and source, drain and gate contact and an alloying in forming gas at 400 °C for 20 min are done. The Figure 4.9 shows the steps for doping, laser annealing of the source/drain and the device fabricated and Table 4.1 presents a detailed process flow for n-MISFET ring structure fabricated. The Figure 4.10 shows the n-MISFET ring structure fabricated.

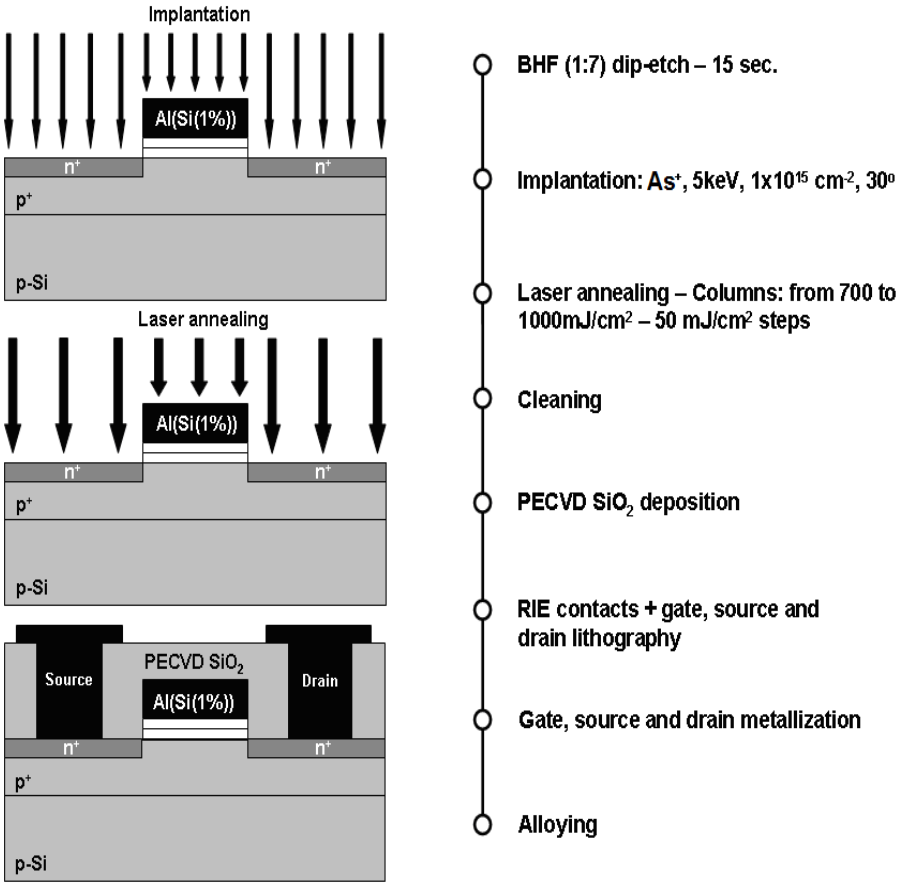


Figure 4.9: Process flowchart for doping and laser annealing of the source/drain regions followed by device contacting.

Table 4.1: Detailed process flow for the fabricated n-MISFET ring-gate structure.

p-type Si wafer (100)
Si cleaning
HF (0.55%) dip-etch, 4 min
20 nm thermal SiO_2
Bulk Si implantation – 40 keV, $1x10^{11}$ cm^{-2}, Boron
Removal of thermal SiO_2 – BHF (1:7)
Cleaning
Furnace annealing at 1000°C, 30 minutes in N_2 gas flow
Cleaning
HF (0.55%) dip-etch, 4 min
ICP oxynitride growth, 12-15 nm
ALD Al_2O_3, 7-8 nm
375 nm Al sputtered at 50°C Al(1%Si) – reflective mask for laser annealing
Gate-stack lithography – source/drain openings
RIE - Al(1%Si) and Al_2O_3 etching
RIE "soft landing" – oxynitride etching
Photoresist removal – O_2 plasma
Cleaning
BHF (1:7) dip-etch: 15 s
S/D implantation: As+, 5 keV, 1015 ions/cm^2, 30° tilt angle
Cleaning
S/D excimer laser annealing (in columns) 0-700-750-800-850-900-950-1000mJ/cm2 (1% overlap)
Cleaning
PECVD SiO_2 deposition – 800 nm at 400°C
Source/drain contact-region lithography
PECVD SiO_2 etching – RIE with "soft landing"
Cleaning
4 minutes HF (0.55%) dip-etch
905 nm Al(1%Si) sputtered at 350°C
Gate contact-region lithography
RIE- Al(1%Si) and PECVD SiO_2 etching, landing on Al metal-gate
Photoresist removal – O_2 plasma
Cleaning
Gate contact metallization - Al(1%Si) 1.4 µm
Lithography of interconnections for source/drain and gate
RIE - interconnections metal
Photoresist removal – O_2 plasma
Cleaning
Alloying in forming gas at 400°C – 20 min

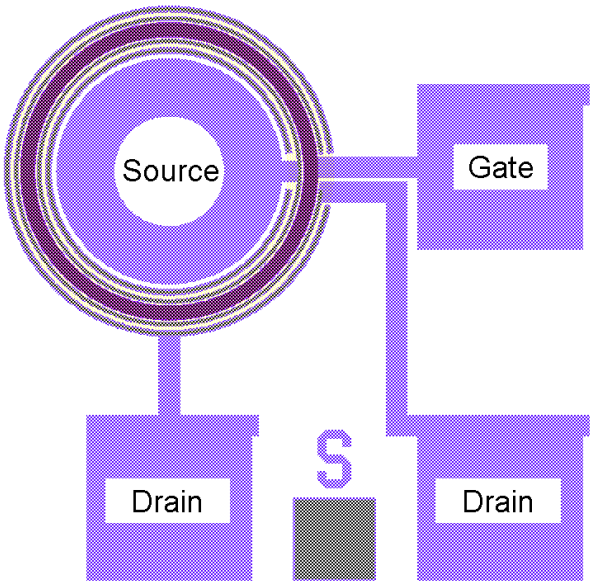


Figure 4.10: Layout of the fabricated n-MISFET ring-gate structure.

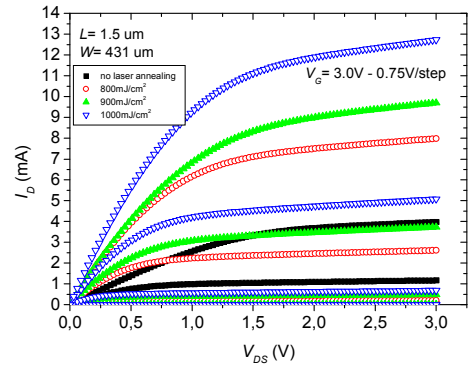
4.3 Electrical test device characterization

In this section the electrical characteristics of the processed MISFETs are presented. The devices were fabricated with an existing mask-set, which could be done only by accepting a very large drain area that is common to all transistors. Due to this large area, the drain junction diodes current is high in all cases. The output characteristics as drain current versus drain voltage (I_D versus V_{DS}) and drain current versus gate voltage (I_D versus V_{GS}) were measured and characteristics such as the threshold voltage and transcondutance were extracted.

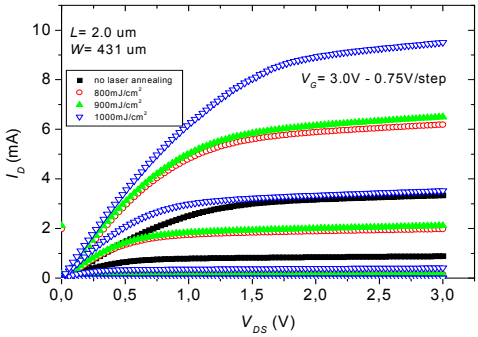
Current-voltage characteristics were extracted for three different types of n-MISFETs and the source/drain laser-anneal was performed at different energies. Several n-MISFET ring-gate structures were measured with gate lengths, L, of 1.5 µm, 2.0 µm and 3 µm and a gate width, W, that

was 431μm in all cases. The laser annealing energy was varied from 700 mJ/cm^2 to 1000 mJ/cm^2, in 50 mJ/cm^2 steps with 1% overlap. Devices were also fabricated without laser annealing. The I_D x V_{DS} transfer characteristics and the I_D versus V_{GS} curves, with different gate lengths, are plotted in Figure 4.11 and Figure 4.12, respectively.

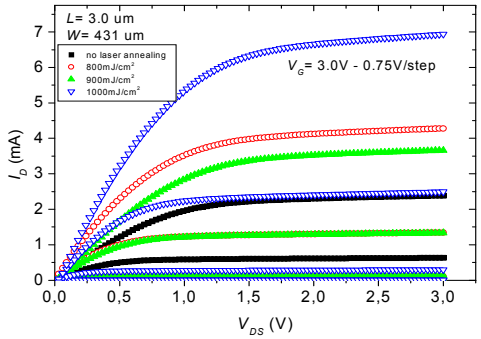
Comparing I_D versus V_{DS} transfer characteristics (Figure 4.11 (a), (b), (c)) for all devices, the drain current increases by 190% to 220% when going from devices with no laser-anneal to devices annealed at 1000 mJ/cm^2 Therefore, the dopant activation by excimer laser annealing is high and the MISFETs devices show an increase in current drivability with increasing laser energy. The increase in the on-current can be traced back to the lower sheet and contact resistance of implanted regions annealed at higher laser energies as shown in the Chapter 2. The I_D versus V_{GS} transfer characteristics with different gate lengths, are plotted in Figure 4.13 and the Figure 4.14 (a), (b), (c) show the I_D versus V_{GS} curves of devices with a gate length of 1.5 μm, 2.0 μm and 3.0 μm, respectively, and source/drain laser-annealing at energies of 800, 900, 1000 mJ/cm^2 as well as no laser annealing. The V_{Th} is determined by measuring the drain current I_D for various values of gate voltage V_{GS}. For all devices presented on this thesis, the threshold voltage was extracted by the linear extrapolation, which is the most common method of determining V_{Th}.



(a)



(b)



(c)

Figure 4.11: I_D versus V_{DS} transfer characteristics for n-MISFETs with different gate lengths. (a) 1.5 µm, (b) 2.0 µm and (c) 3 µm. The gate width was in 431µm in all cases.

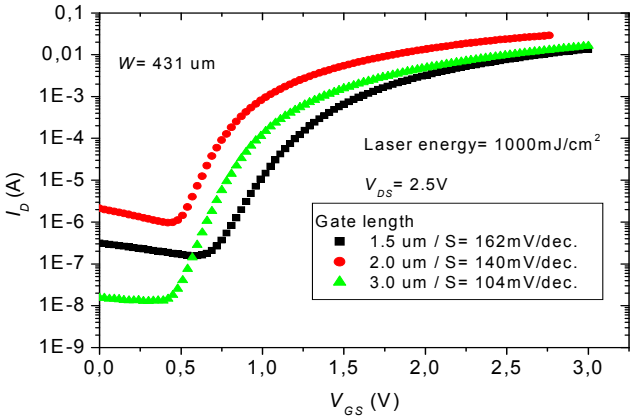


Figure 4.12: I_D versus V_{GS} transfer characteristics for n-MISFETs with different gate lengths and a source/drain laser-anneal at 1000 mJ/cm^2. The gate width was 431µm in all cases.

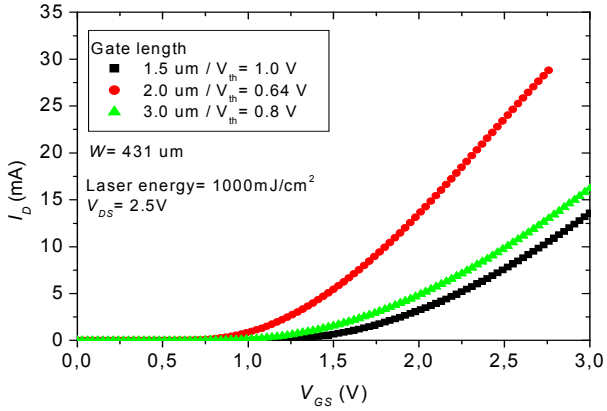
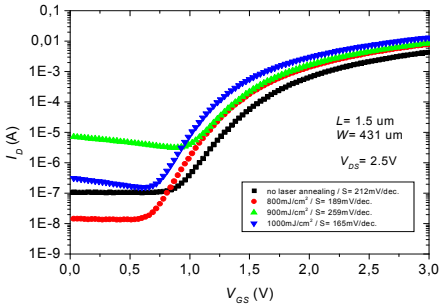
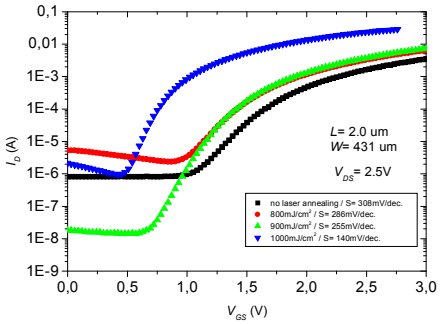


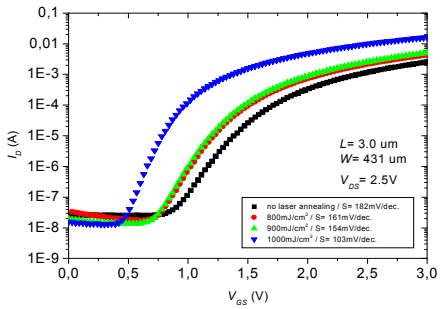
Figure 4.13: The I_D versus V_{GS} transfer characteristics with different gate lengths. The gate width was 431 µm in all cases.



(a)



(b)



(c)

Figure 4.14: I_D versus V_{GS} transfer characteristics curves of n-MISFET devices with different gate lengths: (a) 1.5 µm (b) 2.0 µm (c) 3.0 µm. The source/drain regions were laser annealed at energies of 800, 900, 1000 mJ/cm^2 and not laser annealed at all. The gate width was 431 µm in all cases.

In the I_D versus V_{GS} curves for 1.5 μm and 2.0 μm gate length (Figure 4.14 (a) and (b)), a spread in the leakage current can be observed for different laser energies and this spread becomes smaller for devices with the 3.0 μm gate length (see Figure 4.14 (c)). For all devices the leakage current that can be identified in the subthreshold region, is relatively high for different gate lengths because the ring layout is used in a manner that makes the source and drain areas are much larger than the gate area. A leakage current in the range of 1.5×10^{-8} to 5.2×10^{-6} was measured and the subthreshold slopes, S, are smaller for devices with source and drain laser annealed at high energies. The curve of gate capacitance versus gate area has also been plotted and the results are shown in the Figure 4.15. From this a equivalent gate oxide thickness of 6.1 nm was calculated. For all devices an I_{on}/I_{off} of approximately 10^6 can be observed.

The TEM analysis of one of the device cross-sections shows no loss of the Al gate as a result of the annealing and no damage to the gate dielectric, but the image also reveal that the epitaxial regrowth of the implanted region is not complete close to the edge of the source and drain junctions (Figure 4.16). These edge effects close to the gate area can be attributed to fact that the gate stack absorbs heat during the laser annealing step. Therefore the temperature at the edges can be lower than that necessary for melting and consequently no recrystallization occurs. This can potentially cause an increase in junction leakage if these regions are within the source/drain depletion regions and higher laser energy is possibly needed to completely recrystallize this region.

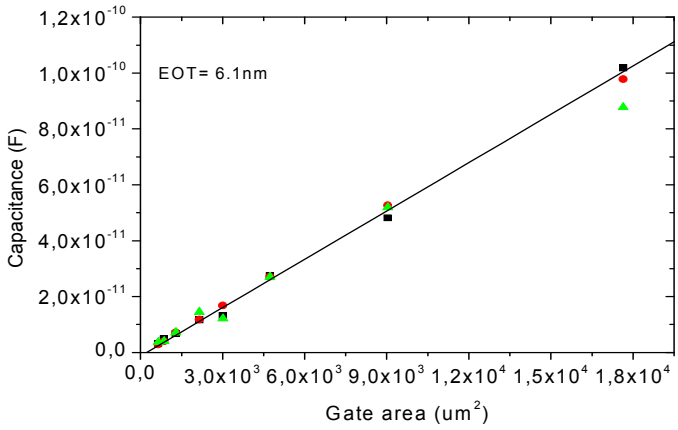


Figure 4.15: Curve of gate capacitance versus gate area of a series of n-MISFET devices. An EOT of 6.1 nm was calculated on this basis.

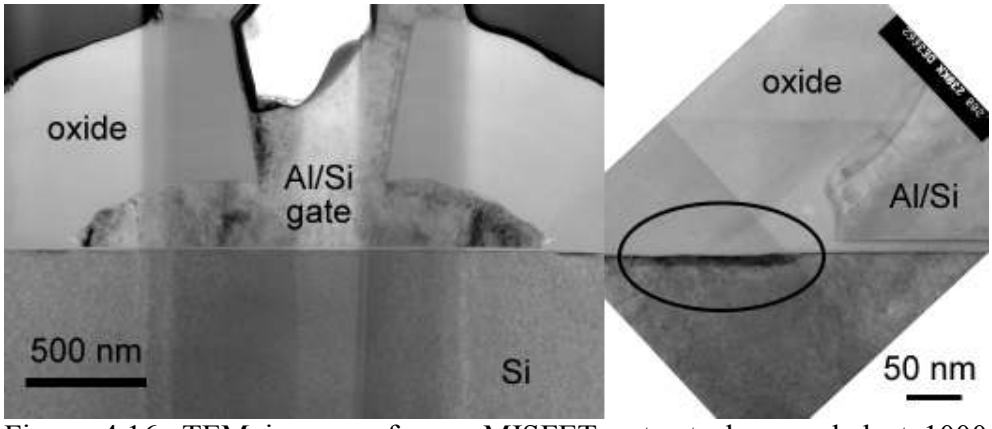


Figure 4.16: TEM images of an n-MISFET gate-stack annealed at 1000 mJ/cm^2. The Al-gate length of 1.5 µm remains after laser processing and there is no damage to gate dielectric (left). Incomplete epitaxial regrowth after annealing close to gate edge – dark region marked on higher resolution image (right).

The results of the n-MISFET ring-gate structures presented in this Section have demonstrated that laser annealing of implanted dopants can be successfully integrated in a high-*k* metal gate n-MISFET. After substrate doping, no processing steps are done at temperatures above 400°C making this process extremely attractive for applications where the thermal budget is of critical concern. Laser processing requires careful optimization, particularly in view of the heat conduction through the gate-stack used as reflective mask, which can prevent a complete epitaxial regrowth after annealing close to gate edge. High dopant activation in source/drain regions can give a high current drivability of n-MISFETs. The performance of the devices can be improved by the following points:

- a dedicated mask-set in order to reduce the drain area and consequently reduce the leakage current;
- an increase of the laser energy during the source/drain dopant activation could additionally reduce the sheet resistance and consequently increase the drive current;
- an increase of the number of devices would give better statistics to improve comparisons between different devices.

4.4 Fabrication of n- and p-MISFETs

In this Section MISFET devices are described which were fabricated using a new mask set designed to reduce the leakage current inherent to the n-MISFETs test devices discussed in the previous sections. Moreover, the

gate/source/drain structure is designed to improve the dopants activation on source and drain close to gate edge. The layout is as conventional finger-structured transistors with different gate lengths of 3.0, 4.0, 6.0 and 10.0µm and gate width fixed at 20µm were designed. In Figure 4.17 the new transistor layout is shown for n-/p-MISFET fabrication. The process flow for new MISFET fabrication is the same that used for the test n-MISFET devices with a few minor modifications.

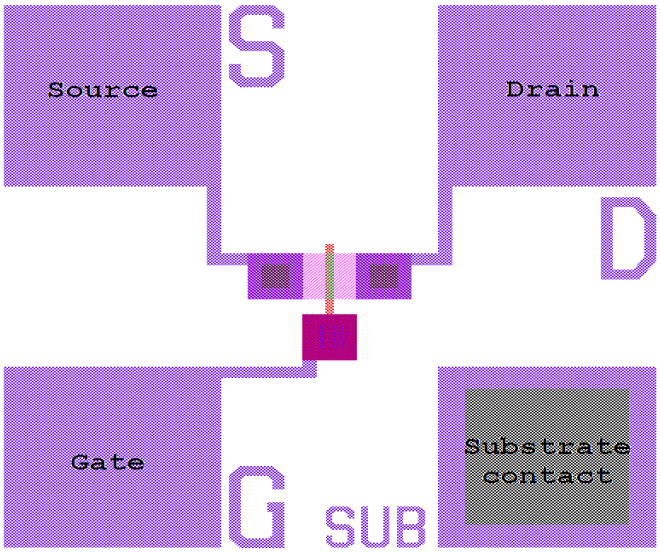


Figure 4.17: Transistor layout for n-/p-MISFET fabrication.

The process steps for the n-/p-MISFET fabrication are given in Table 4.2. Initially a silicon dioxide layer of approximately 20 nm is grown by thermal oxidation on the silicon surface. First, a HF dip-etch is performed immediately before oxidation in order to remove the native oxide on the silicon surface. After oxidation the implantation to dope the bulk silicon is performed thought the SiO_2 layer by implanting 50keV, $1x10^{12}$

cm^{-2} B^+ and 100keV, $1x10^{12}$ cm^{-2} P^+ in respectively the p-type wafers and n-type wafers. Then the thermal SiO_2 is removed using buffered-HF (1:7) and the annealing of this implanted layer is performed in a furnace at 1000°C for 30 minutes in a N_2 gas flow. A 400-nm-thick PECVD SiO_2 is deposited at 400°C and the first lithography step to define the active region in performed. The photoresist is deposited over the SiO_2 layer and the active region is defined with the i-line waferstepper ASML PAS5500/80. The opening of active area is performed in two steps. In the first step the SiO_2 is etched by RIE followed by wet etching (second step). A thickness of 20 nm should be remaining after RIE for subsequent landing on the Si surface with wet etching. The photoresist is removed by O_2 plasma stripping. Immediately before the gate dielectric growth the Si wafer is cleaned and a 4 min HF (0.55%) dip-etch is performed. A silicon-oxynitride layer of 12 nm is grown by ICP-PECVD at 250°C to achieve a high quality oxide interface to the silicon. A 375-nm-thick Al/1%Si layer is sputtered at room temperature to keep the grain size small and thereby making it suitable as gate-metal also serving as reflective masking layer for the subsequent laser annealing. The gate-stack is then patterned and the source and drain regions are defined. A "soft-landing" is applied to prevent damage to the silicon surface during from the RIE process. To dope the source/drain regions, As^+ ions at 5 keV to a dose of 10^{15} ions/cm^2 and BF_2^+ ions at 5 keV to a dose of 10^{15} ions/cm^2 at 7°, 30°, 45° tilt angles were implanted on p-type and n-type wafers, respectively. A 15 s dip in BHF (1:7) solution is performed immediately before these low energy implantations. They are activated by laser annealing with energy densities was varying from 750 mJ/cm^2 to 1050 mJ/cm^2 in columns and in 50 mJ/cm^2 steps with 66% overlap. The maximum laser energy was increased by 50 mJ/cm^2 as compared to the n-MISFET test

devices to try to compensate for the heat conduction through the gate-stack which can cause an incomplete epitaxial regrowth close to gate edge as described in Section 4.3. The wafers were cleaned and a PECVD SiO_2 layer of 800 nm was deposited. A PECVD SiO_2 layer was deposited at 400^oC. Lithography was performed for source/drain contact definition and RIE was used to etch the SiO_2 layer until reaching the Si substrate. To prevent damage to the silicon surface, the etching was also performed in two steps. A 905-nm-thick Al(1%Si) was sputtered at 350^oC for source/drain contacting. Before the aluminium sputtering a 4 min HF (0.55%) dip-etch was done to remove the native oxide. Lithography and etching of the gate contact window was performed and a 1.4-µm-thick Al(1%Si) metal layer was sputtered at 350^oC for gate contacting. Finally, the interconnections to the source, drain and gate contacts are patterned and an alloying in forming gas at 400°C for 20 minutes completes the processing. During the lithography steps the correct exposure energy and focus are adjusted for good pattern transfer. In Table 4.2 a detailed process flow is given for the n-/p-MISFET fabrication.

Table 4.2: Detailed process flow for n and p-MISFET fabrication.

n-MISFET	**p-MISFET**
p-type Si wafer (100)	**n-type Si wafer (100)**
Si cleaning	
HF (0.55%) dip-etch, 4min	
20 nm Thermal SiO_2	
Bulk implantation 50 keV, 1x10^{12} cm^{-2}, Boron	**Bulk implantation 100 keV, 1x10^{12} cm^{-2}, Phosphorus**
Thermal SiO_2 removal – BHF (1:7)	
Cleaning	
Furnace annealing - at 1000^oC, 30 min in N_2 gas flow	
Cleaning	
PECVD SiO_2 deposition – 400 nm at 400^oC	
Active area lithography	

PECVD SiO_2 etching – RIE + wet etching (BHF (1:7))	
Photoresist removal – O_2 plasma	
Cleaning	
HF (0.55%) dip-etch, 4 min	
ICP oxynitride growth – 12 nm	
375 nm Al sputtered at 50°C Al(1%Si) – reflective mask for laser annealing	
Gate-stack lithography – source/drain openings	
RIE – 375 nm Al(1%Si) sputtered at 50°C	
SiO_xN_y (gate dielectric) etching – wet etching (BHF (1:7))	
Photoresist removal – O_2 plasma	
Cleaning	
BHF (1:7) dip-etch: 15 seconds	
S/D implantation As^+, 5 keV, 10^{15} ions/cm^2 7°, 30°, 45° tilt angles	**S/D implantation BF_2^+, 5 keV, 10^{15} ions/cm^2 7°, 30°, 45° tilt angles**
Cleaning	
S/D excimer laser annealing (in columns) 0-750-800-850-900-950-1000-1050mJ/cm^2 (66% overlap)	
Cleaning	
PECVD SiO_2 deposition – 800 nm at 400°C	
Source/drain contacting lithography	
PECVD SiO_2 etching – RIE + wet etching (BHF (1:7))	
Cleaning	
4 min HF (0.55%) dip-etch	
905 nm Al(1%Si) sputtered at 350°C	
Gate contacting lithography	
RIE- Al(1%Si) and PECVD SiO_2 etching, landing on Al metal gate	
Photoresist removal – O_2 plasma	
Cleaning	
Gate contact metallization - Al(1%Si) 1.4 µm	
Lithography of interconnect for source/drain and gate	
RIE - interconnect metal	
Photoresist removal – O_2 plasma	
Cleaning	
Alloying in forming gas at 400°C – 20 minutes	

4.5 Electrical device characterization

In this Section a description is given of the electrical measurements of the n and p-MISFET devices along with an analysis of the results. The

measurements were performed on an HP-4156C semiconductor parameter analyzer and an HP-4284A precision LCR meter for the *C-V* measurements.

The I_D versus V_{GS} transfer characteristics were determined for transistors with source/drain implants at 7^o, 30^o and 45^o tilt angles and laser-annealing at 1050 mJ/cm^2. The I_D versus V_{GS} and I_D versus V_{GS} curves of transistors with gate lengths of 3.0 and 10 µm are plotted in Figure 4.18 and 4.19, respectively. The V_{th} is determined by measuring the drain current I_D for various values of gate voltage V_{GS}, at low V_{DS} (0.1V). The threshold voltage was extracted by the linear extrapolation.

The Figures 4.20 and 4.21 show the I_D versus V_{DS} output characteristics curves of n-/p-MISFETs with source/drain implants at 7^o, 30^o and 45^o tilt angles, laser annealing at 1050 mJ/cm^2 and different gate lengths of 3.0 and 10 µm, respectively. The gate width was fixed to be 20 µm.
The I_D versus laser energy curves of the n-/p-MISFET devices show an increase in current drivability with increasing laser energy which correlates well with the expected low sheet resistances of the source/drain implanted regions annealed at high energies. A reduction of the on-current is also evident for increasing gate length in accordance with the increase of the series resistance between source/drain. The Figures 4.22 and 4.23 show the statistical analysis of the drain current for both n- and p-MISFET devices with fixed $|V_G| = 5$V and $|V_{DS}| = 8$V implanted at 7°, 30° and 45° tilt angles and laser annealed from 750 mJ/cm^2 to 1050 mJ/cm^2 (50 mJ/cm^2 steps), respectively. The drain current of the transistors annealed at 1050 mJ/cm^2 is compared to that of transistors without annealing, and a significant increase of the drain current can be observed.

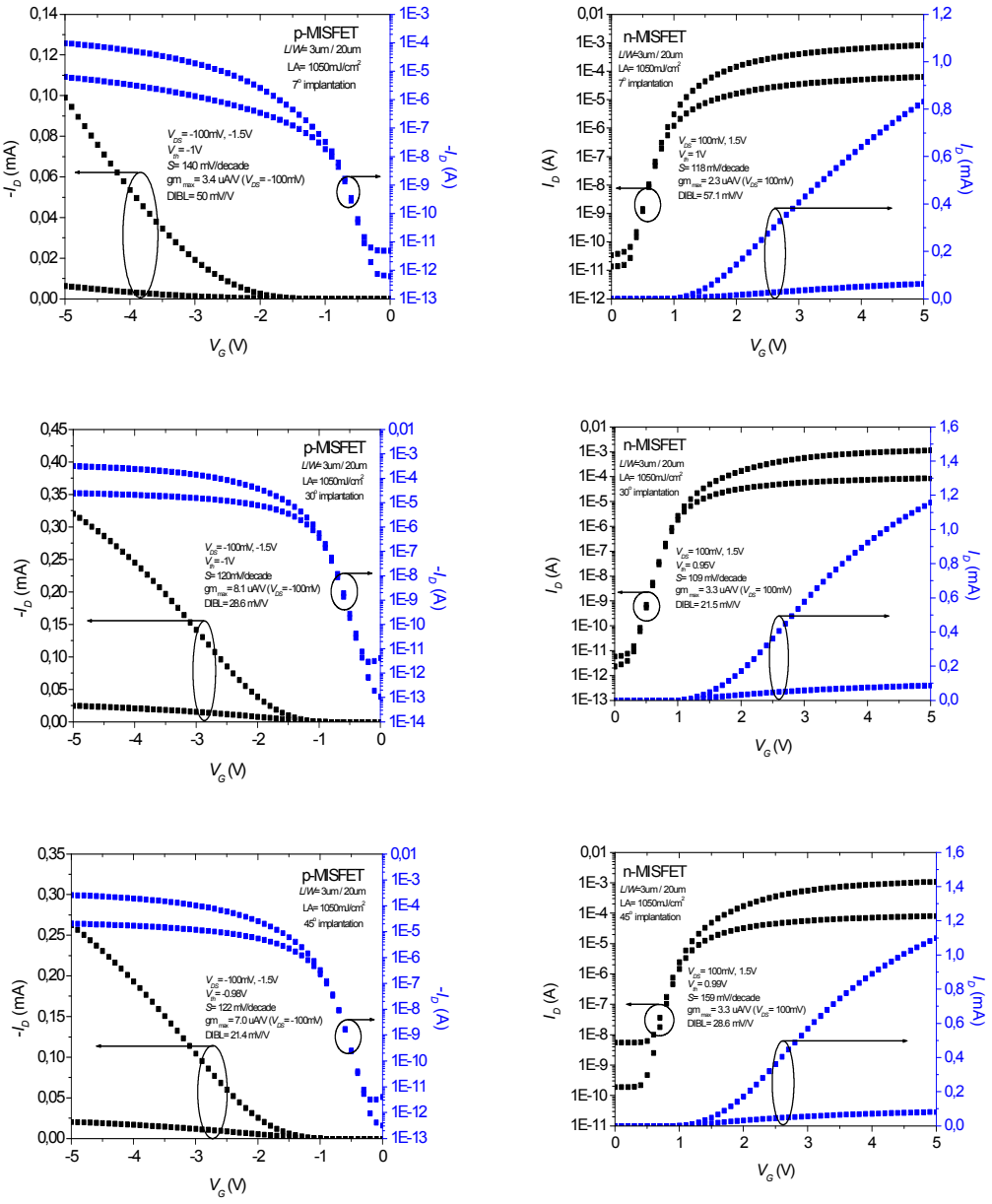


Figure 4.18: I_D versus V_{GS} curves on linear/scales for n-/p-MISFETs with a gate length of 3 µm with source/drain laser annealing at 1050 mJ/cm^2 and implanted at 7°, 30° and 45°. The gate width was fixed to be 20 µm.

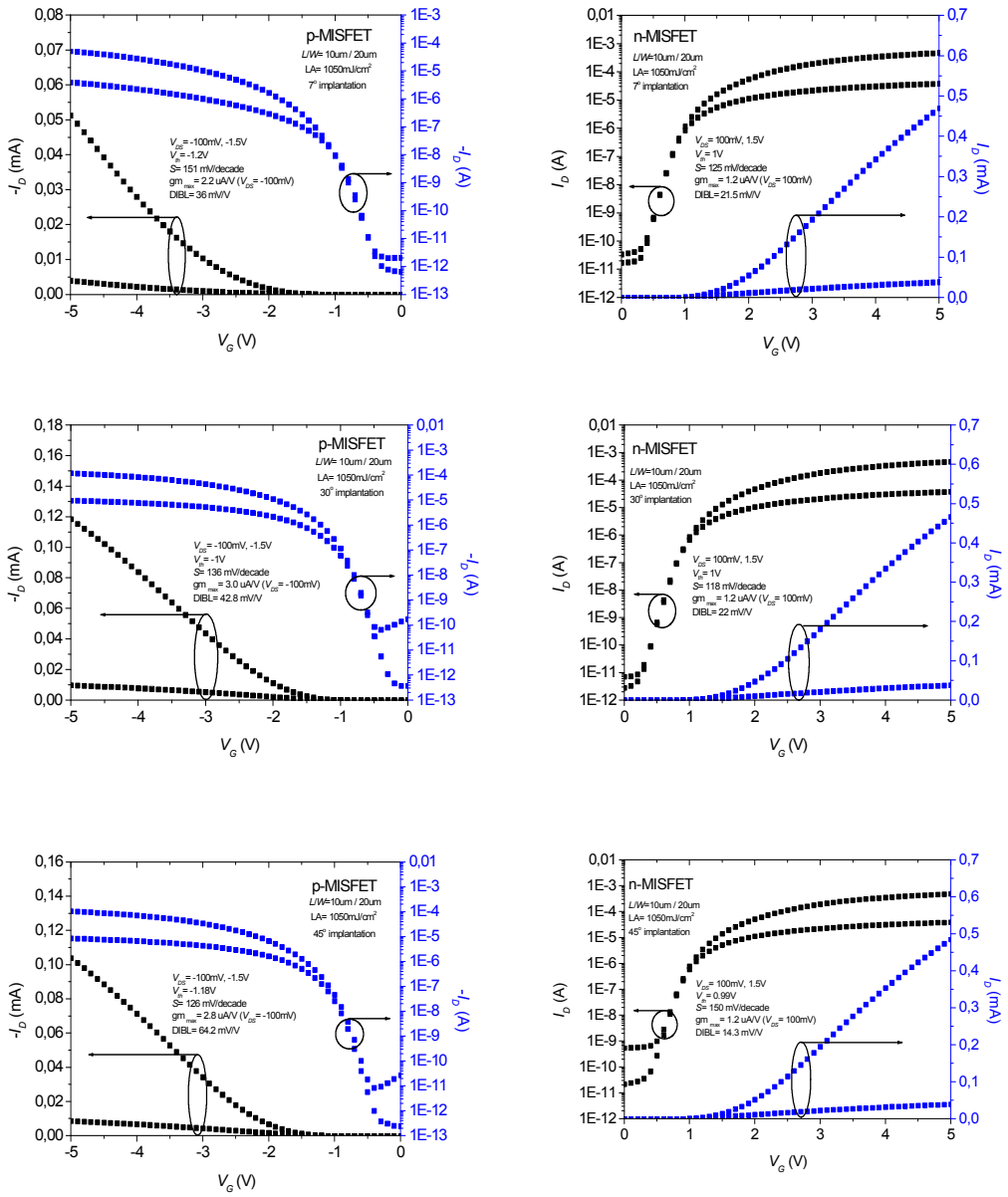
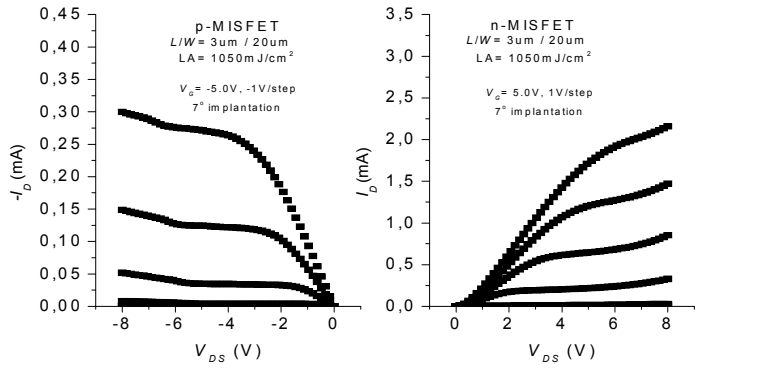
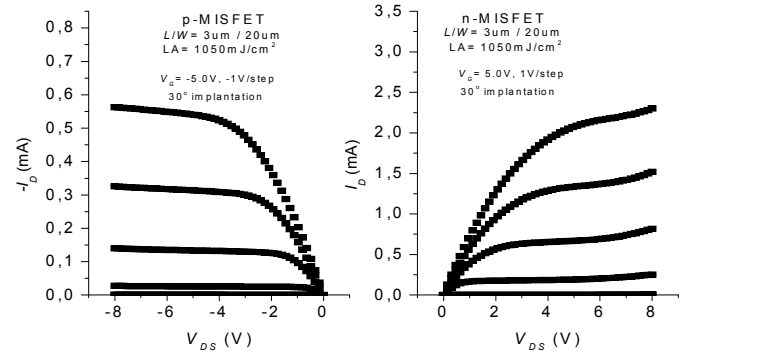


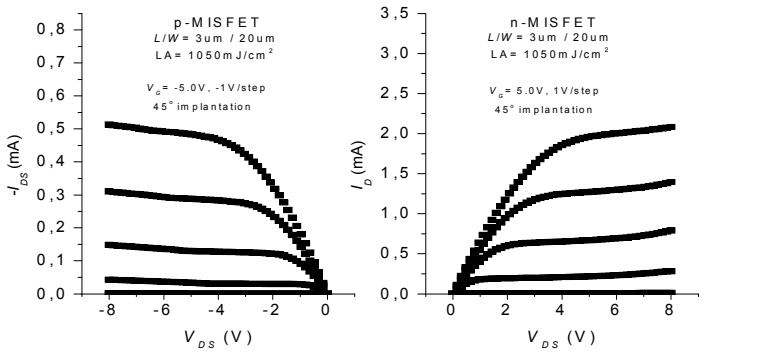
Figure 4.19: I_D versus V_{GS} curves on linear/log scales for n-/p-MISFETs with a gate length of 10 µm with source/drain laser annealing at 1050 mJ/cm^2 and implanted at 7°, 30° and 45°. The gate width was fixed to be 20 µm.



(a)

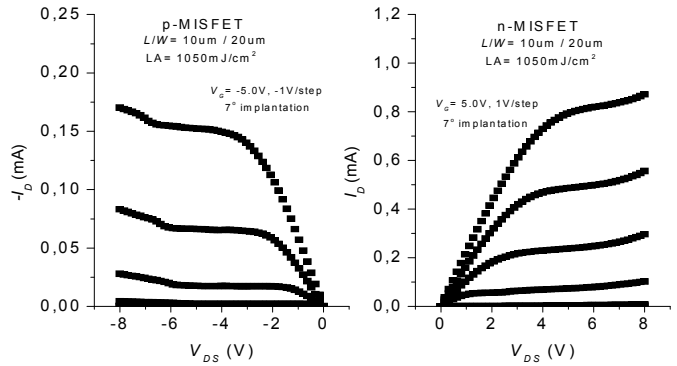


(b)

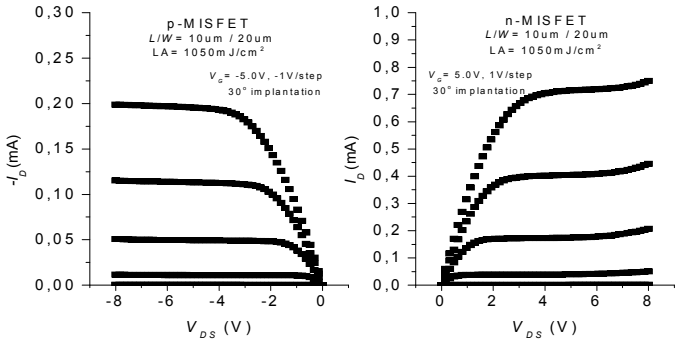


(c)

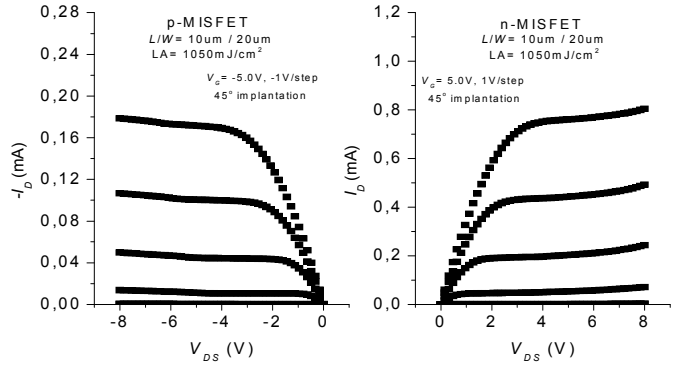
Figure 4.20: I_D versus V_{DS} output characteristics of n-/p-MISFETs with a gate lengths of 3 μm with source/drain laser annealing at 1050 mJ/cm^2 and implanted at (a) 7°, (b) 30° and (c) 45°, respectively. The gate width was fixed to be 20 μm.



(a)

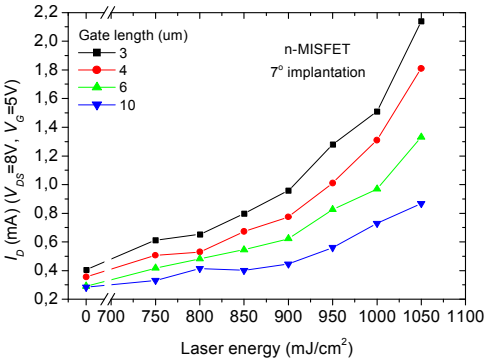


(b)

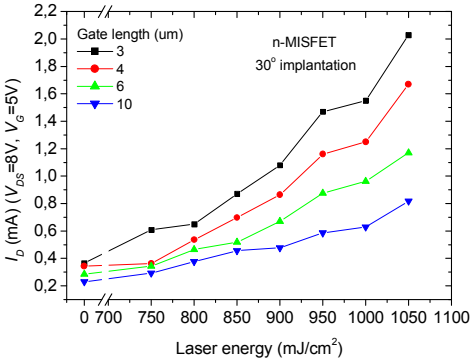


(c)

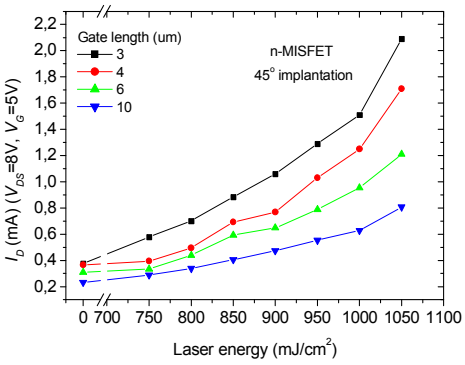
Figure 4.21: I_D versus V_{DS} output characteristics of n-/p-MISFETs with a gate length of 10 µm with source/drain laser annealing at 1050 mJ/cm^2 and implanted at (a) 7°, (b) 30° and (c) 45°, respectively. The gate width was fixed to be 20µm.



(a)

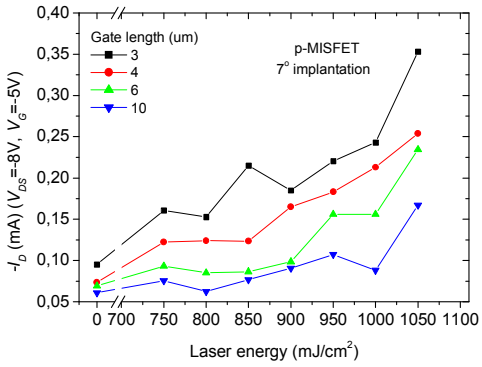


(b)

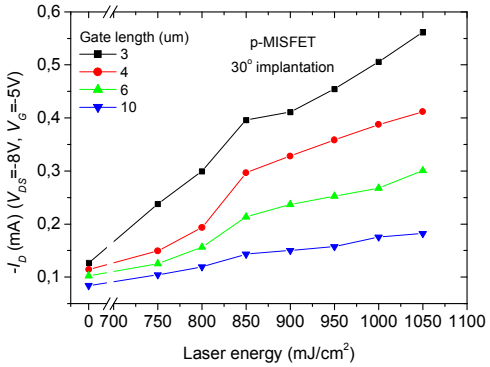


(c)

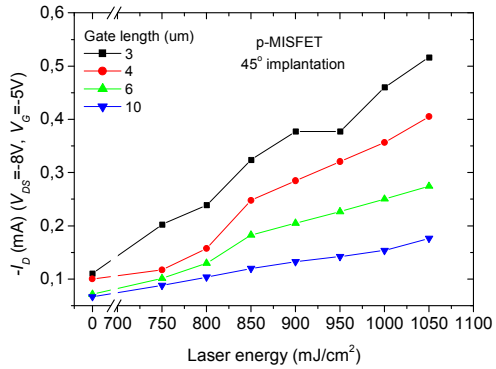
Figure 4.22: I_D versus laser energy for n-MISFET devices with a fixed V_G = 5 V and V_{DS} = 8 V implanted at (a)7°, (b)30° and (c)45° tilt angles.



(a)



(b)



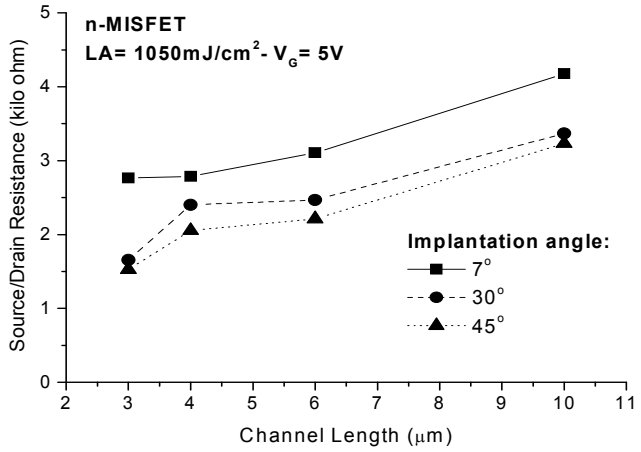
(c)

Figure 4.23: I_D versus laser energy for p-MISFET devices with fixed V_G = -5 V and V_{DS} = -8 V implanted at (a) 7°, (b) 30° and (c) 45° tilt angles.

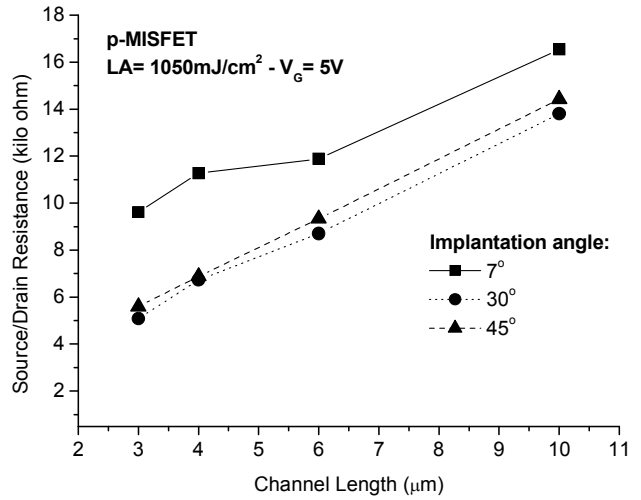
Comparing the n-MISFETs results, the drain current for different angles of implantation increases as the angle is increased. In contrast, the p-MISFETs implanted at have a lower drain current than that found for 30° and 45° implants. This could indicate that source/drain implants at 7° do not connect as well to the channel region as the tilted implants. This would also correlate well with the larger spread in drain current values seen in Figure 4.23a as a function of laser energy.

In Figure 4.24 the source–to-drain resistance is plotted as a function of channel length as extracted from the I_{DS} versus V_{GS} curve in the linear region with V_G = 5 V. As expected, it is possible to see that the total resistance increases linearly with the channel length, and also the influence on the resistance from the different implantation angles becomes more clear. The channel resistance per unit gate-length, given by the slope of the curves, is approximately the same for all tilt angles as it should be. Two effects that determine the contribution to the total resistance from the source/drain regions play a role: the sheet resistance of the source/drain regions and resistance of the connection on the channel region. The former will increase with tilt angle while the latter will decrease due to a better overlap of the two regions. There will also be a small reduction in the distance between source and drain. From the curves in Figure 24 it appears that the variation in overlap between the source/drain and channel region is dominating the total resistance. At 7° the total resistance is significantly higher than for the other tilt angles. A small difference can be seen between the implantation angles of 30° and 45°. The Figure 4.25 shows the I_D versus gate length for different laser annealing energies and a 30° implantation, for both n-

MISFET and p-MISFET devices. Here the effect of reducing the S/D sheet resistance can be seen as a significant increase of the drain current.

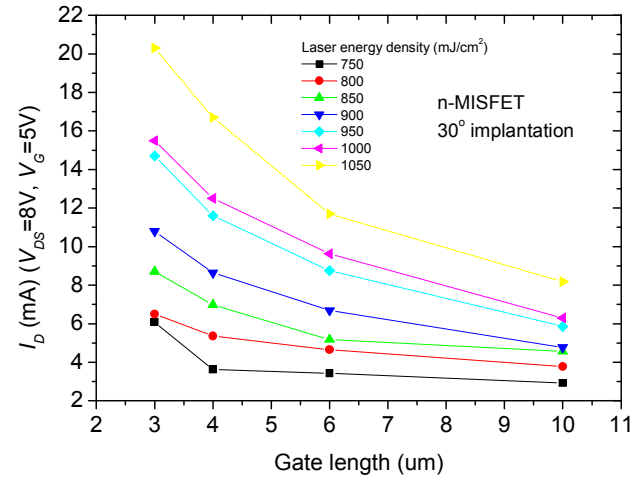


(a)

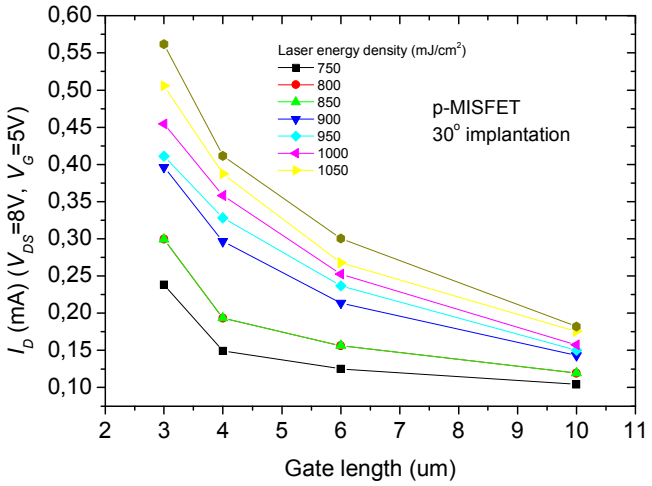


(b)

Figure 4.24: Total resistance between source and drain for a) n-MISFET and b) p-MISFET devices.



(a)



(b)

Figure 4.25: I_D versus gate length for different laser anneal energies going from 750 mJ/cm^2 to 1050 mJ/cm^2 (for 50 mJ/cm^2 steps) and 30^o implantation angle for (a) n-MISFET and (b) p-MISFET devices.

From the I_D versus V_{GS} curves subthreshold slopes (S) can be extracted as 113-191 mV/decade for n-MISFETs and 117-162 mV/decade for p-MISFETs, and I_{on}/I_{off} ratios between $7.5x10^4$ and $1.2x10^8$ were reached. The transconductances varied from 12 μS to 26 μS for n-MOSFETs, and 2.2 μS to 8.1 μS for p-MOSFETs. The DIBL was also extracted although this would be a much more important effect in short channel MOSFET devices. The DIBL effect can be observed by a shift of the threshold voltage as a function of drain voltage. With the reduction of the channel length the DIBL effect can increase because for higher drain bias, the electric field can penetrate to the source region. When the electric field over the drain penetrates to the source region, the potential barrier at source is reduced and the drain current can increase due to higher injection of carriers from the source. In addition, the threshold voltage is reduced. A DIBL of 35 mV/V and 64.2 mV/V was measured for n- and p-MISFETs, respectively. The Table 4.3 summarizes the measured MISFET parameters. Current-Voltage measurements on MIS capacitors with an area of 80x80 μm^2 were also performed in order to extract the equivalent oxide thickness of the MISFETs. The EOT is extracted from capacitance values at high frequency (1 MHz) and in accumulation. A capacitance of 17.8 pF was measured and an EOT of 12.3 nm was calculated. In the Figures 4.26 and 4.27 a TEM image is shown of the gate-stack and the junction depth of n and p-MISFET, respectively. The 12 nm thick ICP-SiO_xN_y gate-dielectric and a junction depth of 10-12 nm can be discerned. A statistic analyze of the I_D versus V_{GS} results would be required if the behavior of DIBL, S and I_{on}/I_{off} for different devices was to be extracted.

Table 4.3: Summary of the measured MISFET parameters (average).

n-MISFET						
Gate length (µm)	**Implantation tilt angle**	**V_{th} (V)**	**I_{on}/I_{off}**	**gm $_{max.}$ (µS), V_D= 100mV**	**S (mV/dec.)**	**DIBL (mV/V)**
3	7°	1.1	9.0E6	23	121	71.4
	30°	1.1	1.2E8	33	113	35.7
	45°	1.1	1.0E5	33	170	42.8
4	7°	1.1	1.3E7	24	120	50.0
	30°	1.1	7.5E7	26	119	36.0
	45°	1.1	9.3E4	26	183	64.2
6	7°	1.1	7.7E6	18	124	42.8
	30°	1.2	3.9E6	18	128	36.2
	45°	1.1	7.5E4	17	188	71.4
10	7°	1.1	2.8E6	12	130	35.7
	30°	1.2	2.2E7	12	132	35.0
	45°	1.2	9.3E4	12	191	85.7
p-MISFET						
Gate length (µm)	**Implantation tilt angle**	**V_{th} (V)**	**I_{on}/I_{off} (A)**	**gm $_{max.}$ (µS), $\lvert V_D \rvert$ = 100mV**	**S (mV/dec.)**	**DIBL (mV/V)**
3	7°	-1.3	2.5E7	3.4	131	136.0
	30°	-1.2	1.5E7	8.1	127	64.2
	45°	-1.2	3.6E7	7.0	117	64.3
4	7°	-1.3	1.2E7	3.7	142	150.0
	30°	-1.2	5.9E6	5.9	147	71.4
	45°	-1.2	5.4E6	5.7	146	78.5
6	7°	-1.3	1.1E7	3.1	148	178.0
	30°	-1.2	8.1E5	4.6	136	64.3
	45°	-1.3	1.6E6	4.4	162	92.8
10	7°	-1.3	9.8E6	2.2	161	107.0
	30°	-1.2	4.4E5	3.0	149	65.0
	45°	-1.3	1.0E6	2.8	154	106

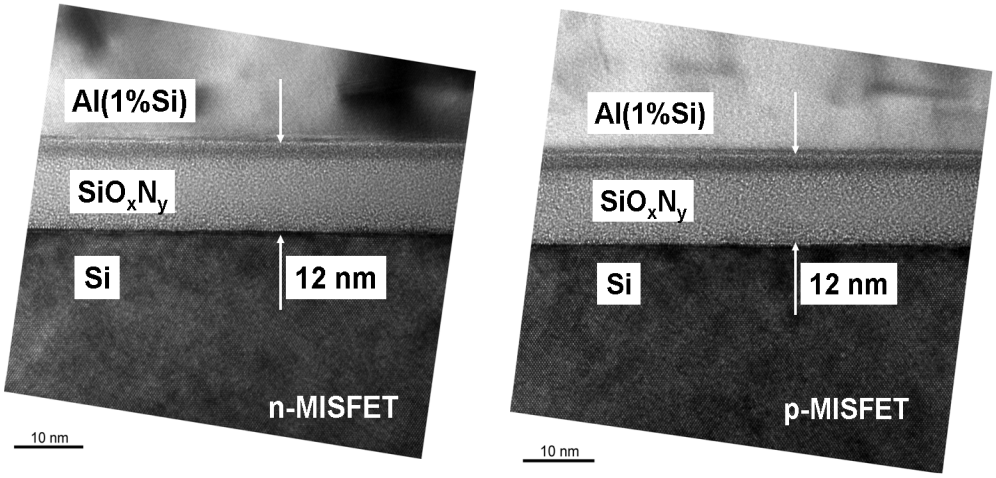


Figure 4.26: TEM micrograph of a gate-stack with 12 nm ICP-SiO_xN_y gate dielectric.

The TEM images in Figure 4.28 show a cross section of an n-MISFET (a) and p-MISFET (b) with a 3 µm gate length and 20 µm gate width, with a source and drain laser annealing of 1000 mJ/cm^2. An incomplete epitaxial regrowth after annealing close to gate stack area can be again observed for both n and p-MISFET devices (Figure 4.29).

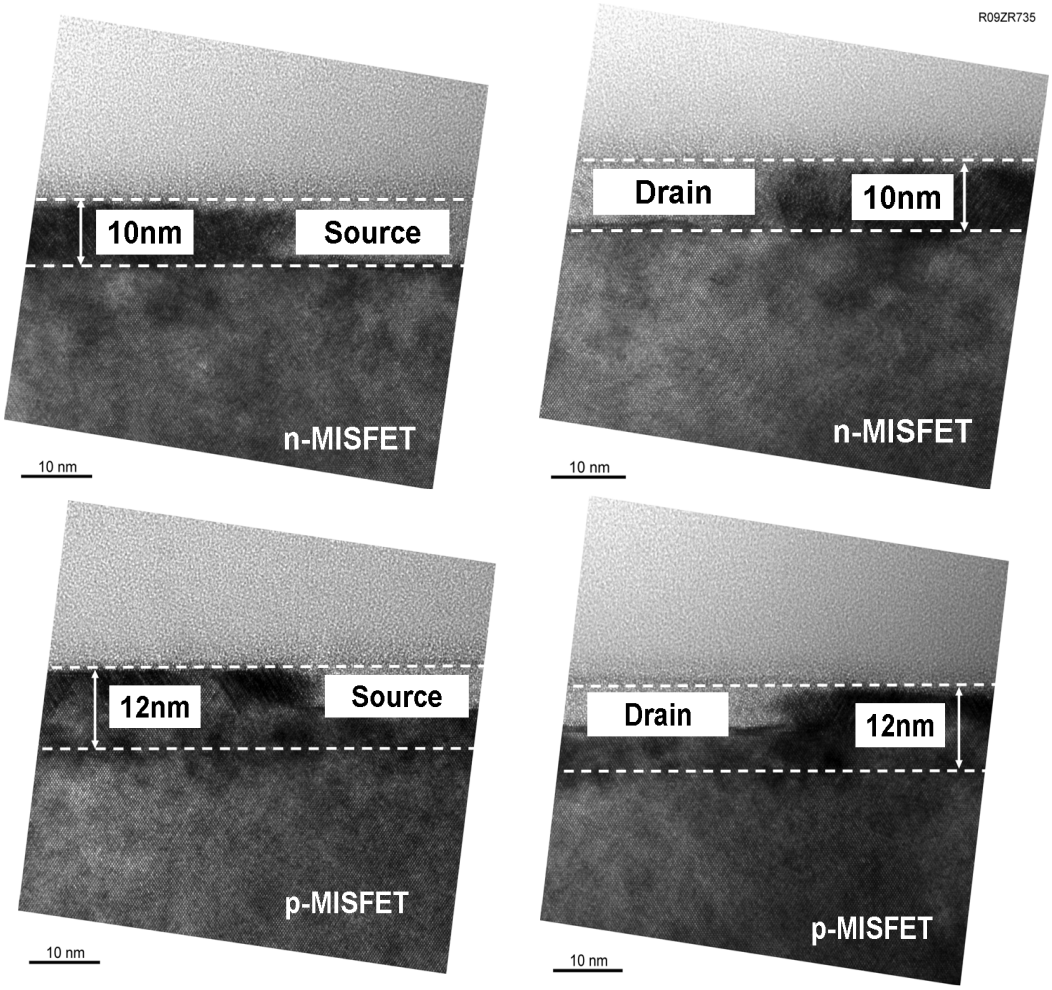
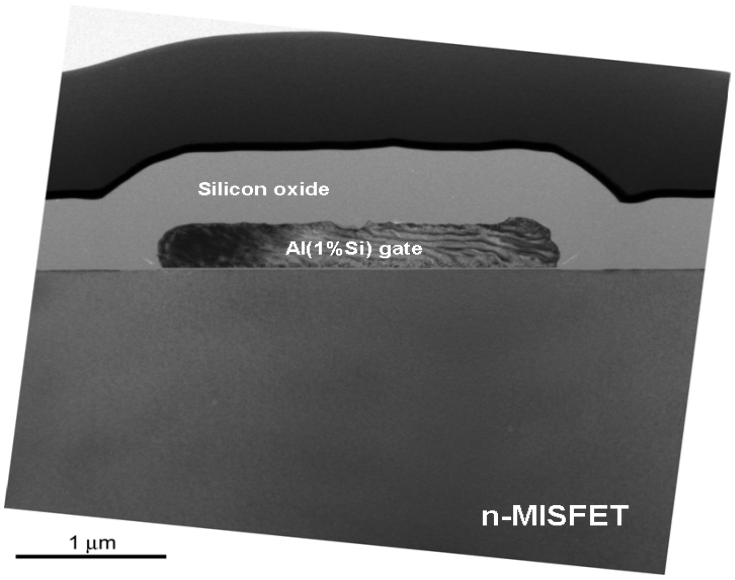
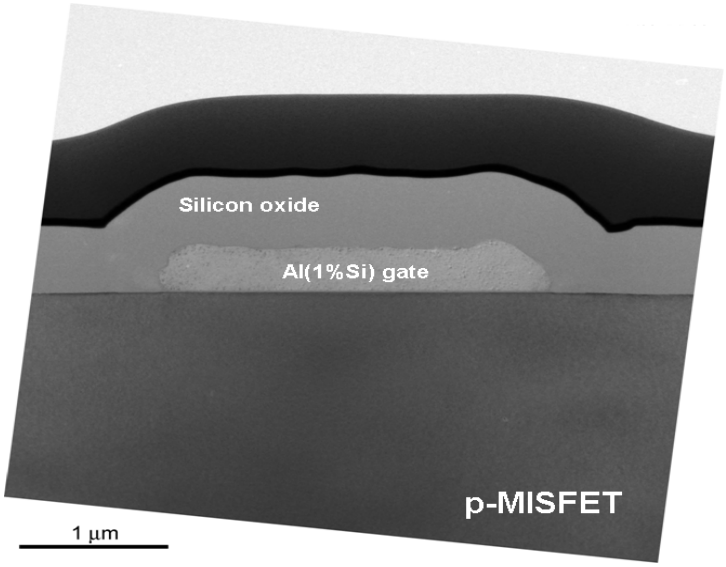


Figure 4.27: A TEM micrograph of the source and drain regions with the junction depth indicated.



(a)



(b)

Figure 4.28: Cross section of an n-MISFET (a) and p-MISFET (b), with L = 3 µm and W = 20 µm. Source and drain regions were laser annealed at 1000mJ/cm^2.

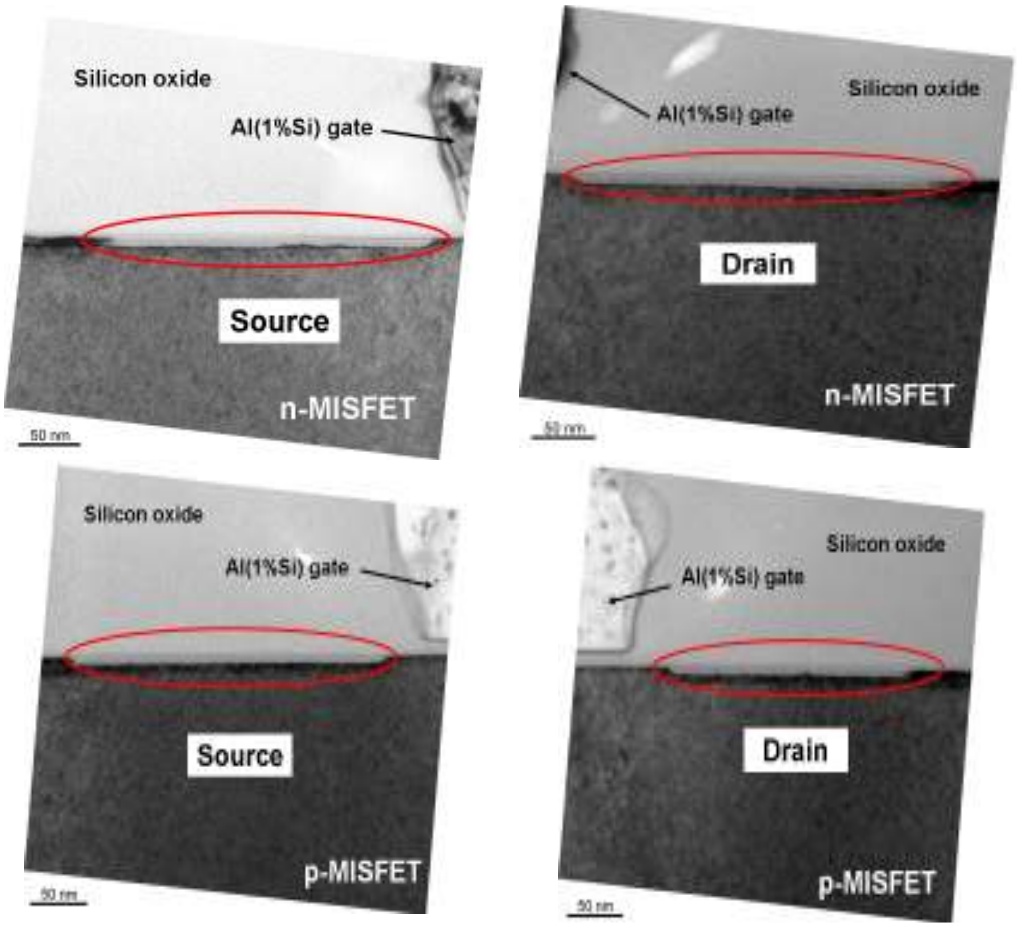


Figure 4.29: TEM images of n- and p-MISFET devices laser annealed at 1000 mJ/cm^2. An Al-gate with L = 3 μm remains after laser action and there is no damage to the gate dielectric. There is incomplete epitaxial regrowth after annealing close to gate edge (region marked).

4.6- Laser irradiation overlap

A set of n-MISFET devices were fabricated using the same processing presented in Section 4.4 but with a few modifications:

- the bulk implantation was changed to B^+ with energies of 20keV, 50 keV or 100 keV, to a dose of $1x10^{12}$, $1.1x10^{12}$or $1.3x10^{12}$ cm^{-2},
- the source/drain implantation for all devices was As^+ at an energy of 5 keV, dose $1x10^{15}$ ions/cm^2, and 7^o tilt angle,
- the source and drain areas were irradiated with a single pulse laser at energies from 800 mJ/cm^2 to 1000 mJ/cm^2 (in 100 mJ/cm^2 steps) at overlaps of 1% or 66%.

Transistors with 3.5, 4.5, 6.5 and 10.5 μm gate length were measured (gate width was fixed to be 20 μm), and good output characteristics were observed for both 1% and 66% laser overlaps.

In Figure 4.30 a statistical analysis is given of the drain current for n-MISFETs irradiated with either 1% or 66% overlap with fixed V_G = 5 V and V_{DS} = 8 V, implanted at a 7° tilt angle and laser annealed from 800 mJ/cm^2 to 1000 mJ/cm^2 (100 mJ/cm^2 steps). The transistors laser annealed with 1% overlap displayed a lower drain current lower than those annealed with 66% overlap. The drive current for 1% overlap saturates for laser energies from 800 mJ/cm^2 as seen in Figure 4.30. For triple shot laser annealing (66% overlap) the drain current is higher and continues to increase with increasing energy (Figure 4.30). The 66% overlap laser annealing allows more activation of dopants due to the triple exposure which also results in better uniformity over the wafer. However, more heating can also be expected and for submicron devices, over-heating needs

to be taken into consideration, since a melting of the metal-gate of the transistors may occur especially for high energies.

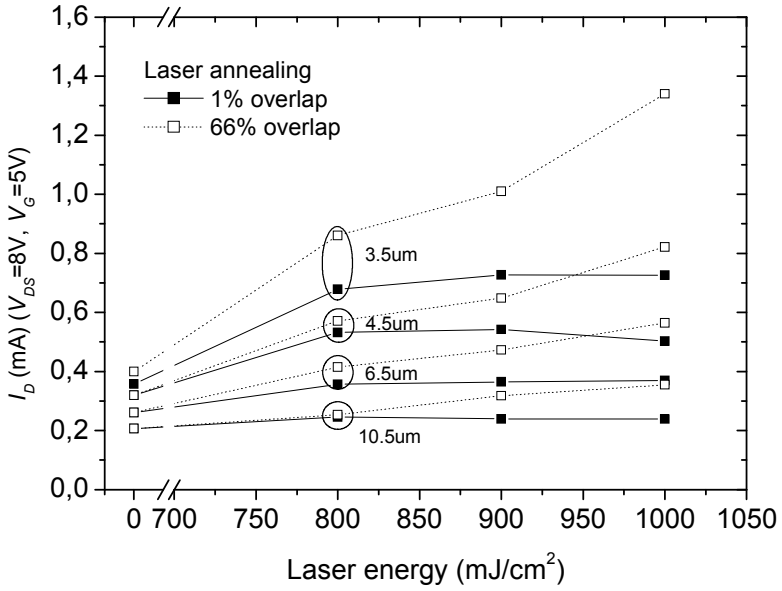


Figure 4.30: Comparison of the drain current for n-MISFET devices laser annealed with either a 1% or 66% overlap, with V_G = 5 V and V_{DS} = 8 V.

4.7- Conclusions

In this Chapter the fabrication of n- and p-MISFET devices was demonstrated for processing temperatures below 400^{o}C. Four important processing steps must be performed in order to have good electrical device performance:

- to obtain a good quality growth of ICP-SiO_xN_y used as gate-dielectric, the Si surface must be cleaned immediately before the growth. To achieve this a 4 min HF (0.55%) dip-etch is performed.

- a 15 seconds dip in BHF (1:7) solution is performed immediately before source/drain implantation. A BHF dip-etch is used to remove the native oxide on the Si surface so that a uniform implantation of the low-energy ions can be achieved.

- during the oxide etching to open the source/drain contact windows, damage to the implanted silicon surface must be prevented. This is achieved by using a RIE process with low RF power (100W).

- a 4 min HF (0.55%) dip-etch is necessary to remove native oxide before source/drain metallization in order to ensure a low-ohmic contacting.

For both n- and p-MISFET devices, with laser annealed implanted source/drain regions, have good performance, in particular with respect to drain current driving capability. With increasing the laser energy, the sheet resistance of source/drain regions is reduced due to a high dopant activation. An incomplete epitaxial regrowth of the implanted regions during the laser processing close to the gate edge has been observed. This indicates that the metal-gate is providing cooling of the perimeter regions. Therefore, in each specific structure the laser annealing must be adjusted to the thermal conductivity of the surroundings. The source to drain resistance was also extracted from the measurements and an increase was observed when the channel length increases. Ultrashallow source/drain junctions were activated

and the TEM images shown junctions of 10-12 nm deep for 1000 mJ/cm^2 laser energy. The influence of the overlapping of the laser spot was studied for 66% and 1% overlap. The drain current is higher for 66% overlap due to a higher activation of dopants but an extra heating can be expected. The overall good results achieved for the MISFET devices with laser-annealed source/drain, shows great potential for application in next generation of CMOS devices, including D-DotFETs, and this processing scheme will be used in the fabrication of the DotFET as described in the next section.

Chapter 5

DotFET devices

The low temperature processing of source/drain and gate regions that was developed in the previous chapters is now applied in the fabrication of DotFETs. The implantation at low energies in source/drain region and subsequent laser annealing was successfully applied for n^+p diodes, p^+n diodes, n-MISFET and p-MISFET devices. The previous results showed that by using laser annealing technology it is possible to obtain a high activation of dopants in the source/drain region, low sheet resistance, ultrashallow junction formation and low temperature processing, all properties that are very important for the DotFET and D-DotFET devices. In this Chapter a DotFET prototype device is fabricated and also an option for further processing for creating a D-DotFET is discussed.

5.1 The DotFET fabrication process

In this Section first an overview is given of the complete DotFET fabrication process, a schematic representation of which is in Figure 5.1. Furthermore, in the following sub-sections, each process step will be discussed in more detail.

The fabrication starts with an array of holes patterned on the Si surface by optical lithography. These holes are used for a localized growth of SiGe dots by molecular beam epitaxy and in the same system the dots are covered with a strained 30-nm-thick Si layer. An isolation oxide is then deposited by plasma-enhanced chemical-vapor-deposition and the active areas of the device are then patterned by etching back of this oxide. The gate-stack consists of an oxynitride layer grown in an inductively-coupled-plasma PECVD system and an aluminium layer with a 1% Si content PVD. The oxynitride layer ensures a high-quality interface to silicon. The Al (1%Si) layer also serves as a reflective mask for the laser light. Electron-beam lithography is used to define the actual gate region: on the source/drain regions the gate-stack is removed by reactive-ion etching to the silicon. A high dose of arsenic ions is implanted into the source/drain to amorphize the surface layer, which is then melted and recrystallized using the energy of a single pulse of 308 nm wavelength light from a XeCl excimer laser. The pulse duration is 25 ns at full width at half maximum. The source/drain areas are annealed during this step, whereas the rest of the structure is protected from the influence of laser energy by the reflective Al(1%Si) layer. This is followed by deposition of the isolation oxide, contact opening, and deposition and patterning of additional metal layers.

The final step is the alloying in forming gas at 400°C. After the preparation of SiGe dots, all processing is performed at low temperatures.

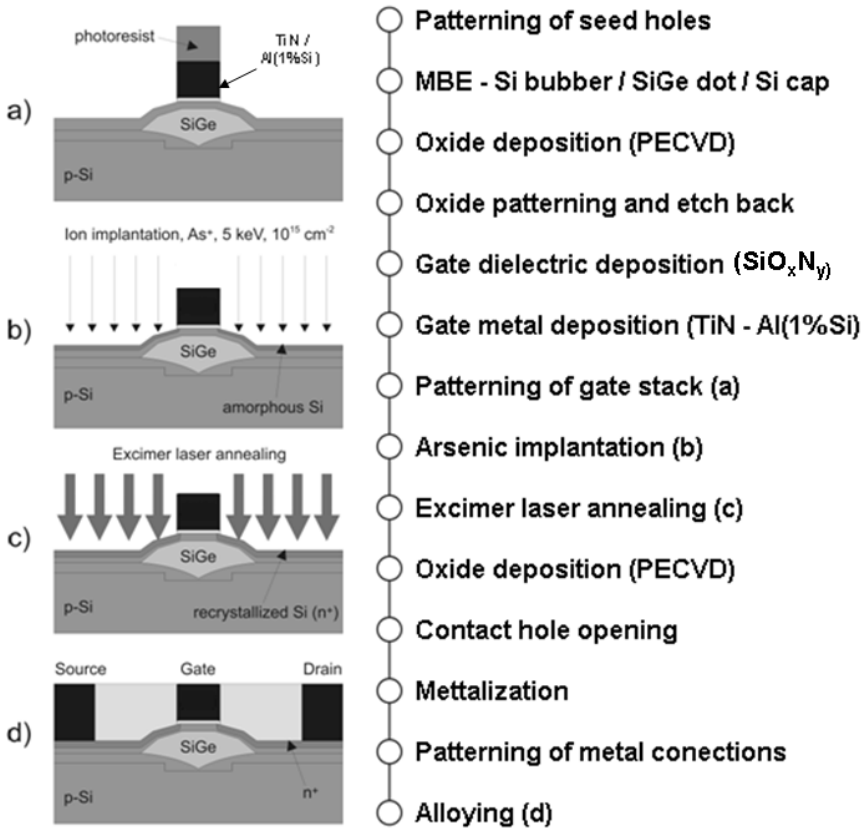


Figure 5.1: Overview of the DotFET process flow.

5.1.1 Seed hole patterning

The process for the fabrication of the DotFETs starts with the patterning of standard 100 mm silicon (100) 2-5 Ωcm p-type wafers with a regular array of holes with submicron periodicity. This is done by first growing a 20-nm-thick oxide layer thermal oxidation on the silicon surface. Immediately before oxidation, a 4 min HF (0.55%) dip-etch is performed in order to remove the native oxide from the silicon surface. After oxidation an implantation is performed with boron ions at different energies (20 keV, 50 keV, or 100 keV) and doses ($1x10^{12}$, $1.1x10^{12}$, or $1.3x10^{12}$ cm^{-2}). After implantation the thermal oxide layer is removed using BHF(1:7) until the front-side of the Si wafer is hydrophobic and the annealing of this implanted layer is performed in a furnace at 1000^{o}C, 30 min in an N_2 gas flow. The wafers are transferred to the furnace again and a layer stack of 400-nm-thick thermal oxide and 40-nm-thick polysilicon is deposited (Figure 5.2a) and the first hole pattern is etched in the polysilicon by RIE with soft landing on the oxide (Figure 5.2b). The lithography process is then repeated with the second mask where the hole pattern is shifted relative to the first mask and holes are again etched in the polysilicon (Figure 5.2c). It is important to transfer the pattern to the thin polysilicon layer to reduce the photoresist thickness variation that arises in the second litho step from any non-planar surface topography. The diameters of the first and second set of holes patterned on polysilicon layer are 600 nm in diameter and the pitch between holes is 1400 nm (see Figure 5.3). However, the next step is reactive-ion etching of oxide, where polysilicon serves as the hard-mask and needs to be thick enough for this task (Figure 5.2d). Since the selectivity of the oxide

etching process to polysilicon is approximately 10:1, the polysilicon layer is consumed during this step.

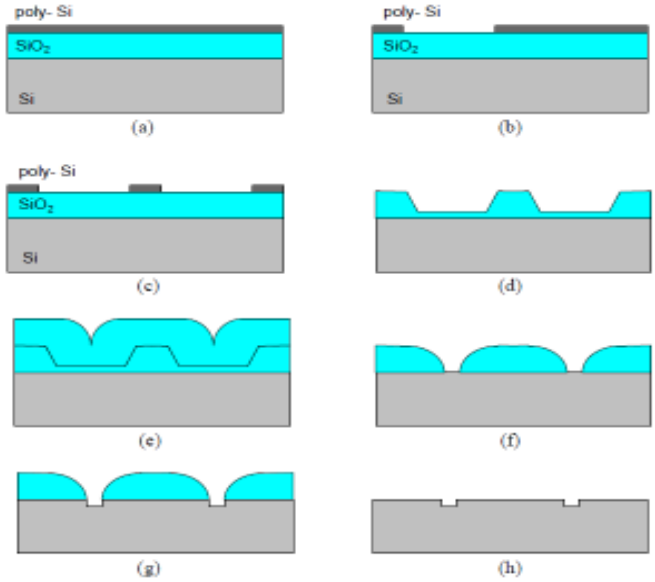


Figure 5.2: Process flow for the double pattern transfer technique used for seed holes formation. (a) The hard-mask stack is formed by 400 nm of oxide and 40 nm of polysilicon. (b) Polysilicon RIE using the first mask with a hole pattern. (c) Polysilicon RIE using the second mask with a shifted hole pattern. (d) Oxide RIE using polysilicon as hard-mask. (e) Oxide deposition by LPCVD. (f) Oxide RIE to form inside spacers for reduction of the holesize. (g) Silicon RIE to etch the hole pattern in the Si. (h) Hard-mask removal.

The oxide etching is carefully timed to stop before reaching the silicon surface. A 20-nm-thick oxide layer should remain during this step. The hole size is then reduced by depositing an LPCVD oxide layer (Figure 5.2e), which is etched until reaching the silicon surface to form inside spacers (Figure 5.2f). In order to prevent any etching of silicon in this step, the RF

of the RIE is then reduced from 300 W to 100 W close to the Si surface. The pattern is finally transferred to silicon by RIE of silicon (Figure 5.2g). The remains of the hard mask are removed by wet, chemical etching with high selectivity to silicon to render a patterned bare silicon surface (Figure 5.2h). For a good control of the SiGe dot growth, holes approximately 300 nm in diameter and 100-nm deep are fabricated. The Figures 5.4 and 5.5 show a SEM and an atomic force microscopy image of seed holes patterned by this double pattern transfer technique.

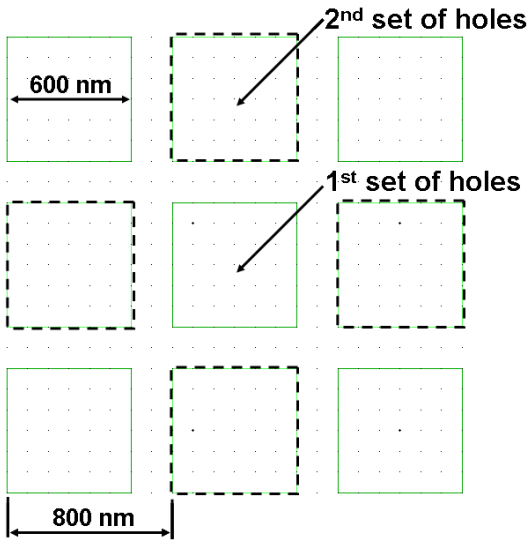


Figure 5.3: Mask design of seed holes fabrication. (600nm diameter and distance between holes of 800nm).

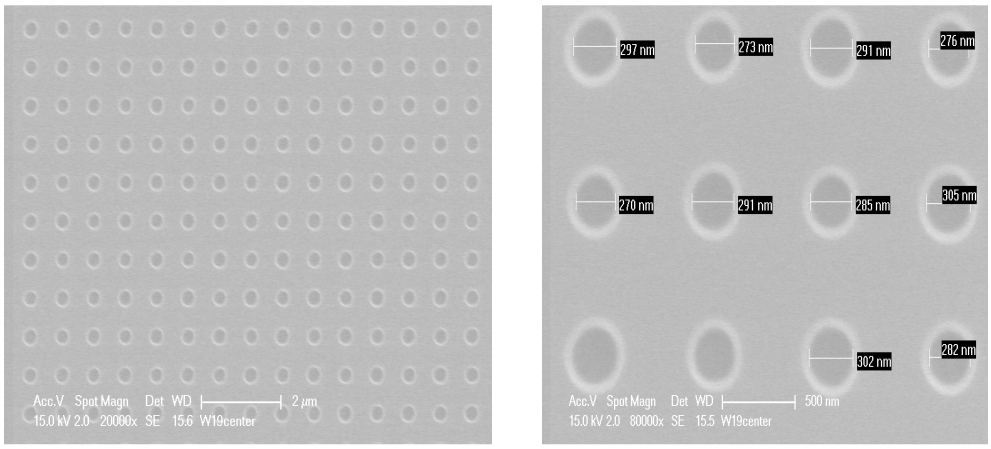
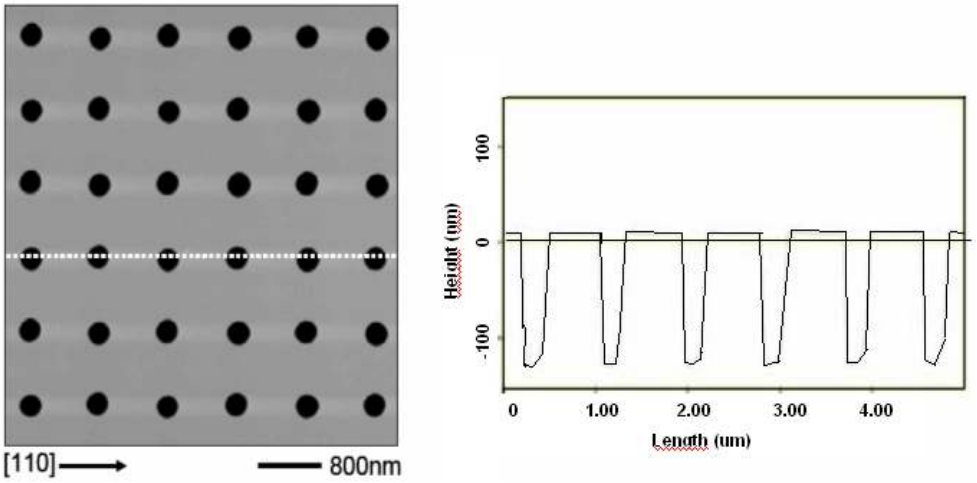


Figure 5.4: SEM images of seed holes patterned by the double pattern transfer technique.



(a) (b)

Figure 5.5: (a) A cross-sectional linescan taken along the dotted line (b) AFM scan of the patterned Si substrate. Data from Johannes Kepler University Linz.

5.1.2 SiGe dots and strained silicon

Ordered SiGe-island arrays were grown by MBE [71] on prepatterned substates with a dot pitch of 800 nm. The SiGe islands were grown and studied by Forschungszentrum Jülich and Johannes Kepler University. Before growth of the SiGe islands an 18-nm-thick silicon buffer layer with a boron doping level of about 10^{17} cm^{-3} was grown by MBE at 700 ^{o}C in order to concentrate any defects at the interface between Si buffer layer and Si substrate. After growth of the silicon buffer layer, SiGe islands and a silicon capping layer were also grown by MBE at 700 ^{o}C and 500 ^{o}C, respectively. The 30-nm-thick Si capping layer, boron doped to about 10^{18} cm^{-3}, was grown at low growth temperature to minimize the intermixing of the SiGe islands with the surrounding Si. In Figure 5.6 atomic force microscope images of the SiGe dots with the 30-nm Si capping-layer are seen to have a perfect lateral ordering and shape. Before growth, the wafers were cleaned by a standard RCA cleaning process and dipped in a HF solution before loading the wafers into a load lock. An in-situ outgassing at 700 °C for 30 minutes was also performed. The AFM images show a well-controlled positioning of SiGe dots on a Si substrate as a result of the pre-patterning. The exact positioning and ordering of the dots is crucial for the further processing of DotFETs on the SiGe islands.

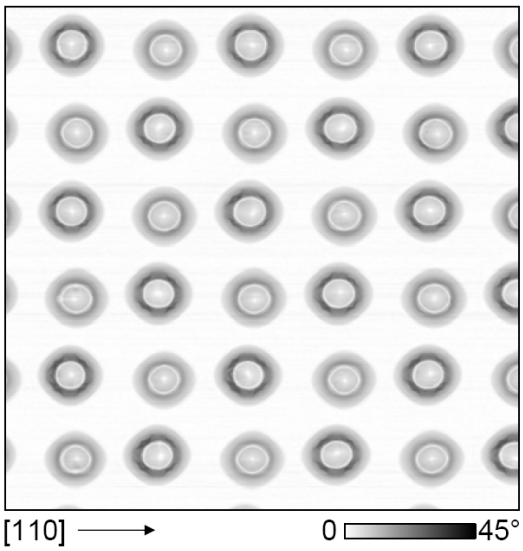


Figure 5.6: AFM scan (5 μm x 5 μm) of the SiGe dots and the 30-nm Si capping-layer showing perfect lateral ordering and preservation of the dot shape. Data from Johannes Kepler University Linz.

The SiGe dot samples were analyzed in detail at the Johannes Kepler University in Linz. The μ-Raman and X-ray spectroscopy techniques were used to measure the strain and the Ge-content in the islands as well as the strain in the silicon capping layer [8, 9, 73]. An average of Ge content of about 40% and a biaxial strain of ~1.5% was found for devices with SiGe islands. The Ge content on the base of SiGe island is approximately 20% and it increase to 65% at the top. These results were confirmed by simulations using a finite element simulation method [5] by the theoretical group of University of Milano-Bicocca. With the available measurement results, the dot geometry was reconstructed in the FEM code. The Figure 5.7 shows the strain of the Si capping-layer in the x direction (ε_{xx}) and a central section of the island along the dashed red lines were simulated by

University of Milano-Bicocca for both DotFET and D-DotFET devices. The ε_{xx} is more uniform over the Si capping-layer after the dot removal but a small relaxation can be observed which slightly decreases the strain.

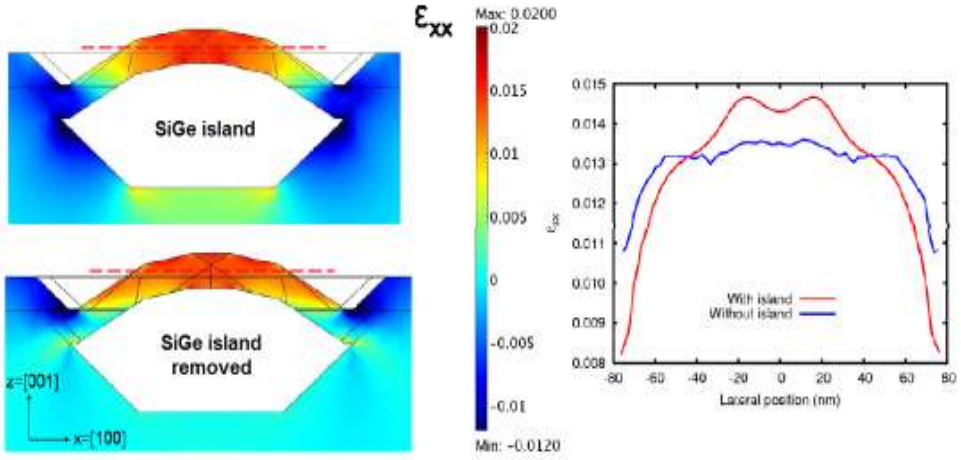


Figure 5.7: Map of ε_{xx} in the DotFET device (top left) and D-DotFET (botton left). The calculated ε_{xx} along the dashed red line is presented on the righ side. Data from University of Milano-Bicocca.

The electrical characteristics of DotFET devices were simulated by the Technical University Wien. The channel length of the simulated DotFET is 100 nm and the oxide thickness of 1.5 nm. The substrate is p-doped to 10^{17} cm^{-3} and the strained Si capping-layer is 30-nm-thick with a p-doping of 10^{18} cm^{-3}. The electrical simulations show that the samples patterned by Johannes Kepler University Linz and Forschungszentrum Jülich, which have a slightly different geometry of the SiGe islands, will only have a negligible effect on the transfer characteristics (Figure 5.8). At $V_{GS} = V_{DS} =$ 1.5 V, the enhancements due to the strained Si layer are 20% and 22% for the SiGe islands grown in either Linz or Jülich, respectively (Figure 5.9).

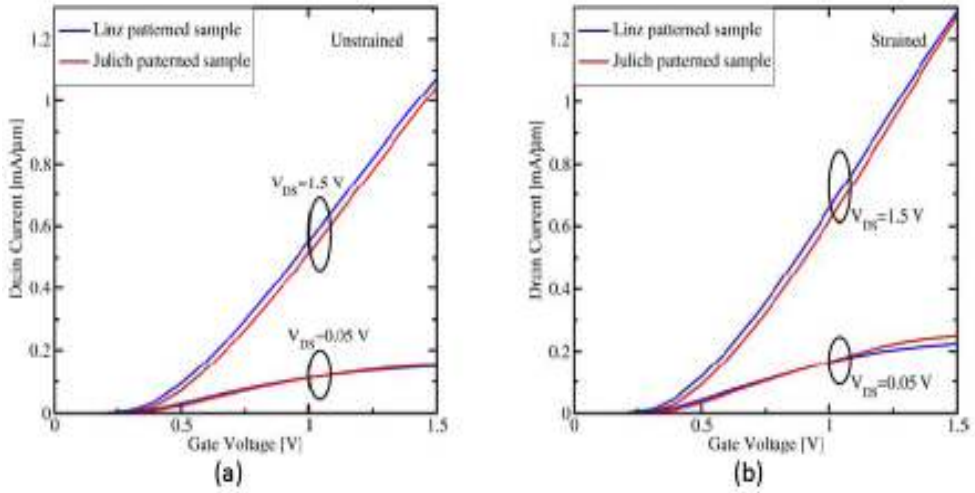


Figure 5.8: Transfer characteristics of samples with SiGe islands patterned by Johannes Kepler University Linz (blue line) and Forschungszentrum Jülich (red line) with and without a strained Si-layer. Data from Technical University Wien.

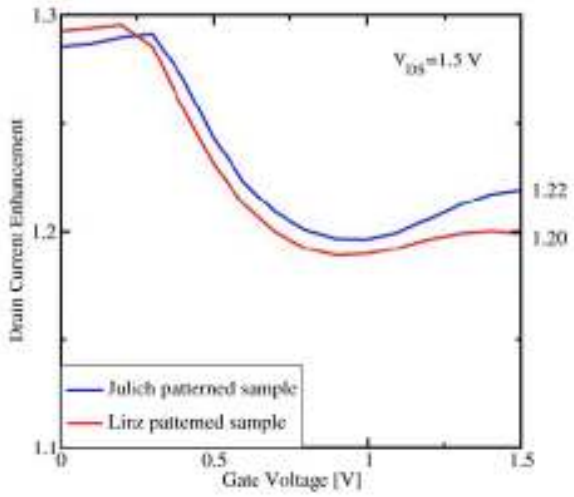


Figure 5.9: Enhancement of the drain current for samples with SiGe islands patterned by Johannes Kepler University Linz (red line) and Forschungszentrum Jülich (blue line). Data from Technical University Wien.

5.1.3 Gate stack, source and drain surface preparation

The DotFET fabrication after creating the SiGe islands (dots) requires low temperature processing to prevent intermixing of the Ge dots with Si that would change the desired strain properties. In all the following processing the temperatures are kept below 400 ^{o}C. After the SiGe-island formation, the same process as used for creating the S/D/gate regions in the n- and p-MISFETs discussed in the previous chapter was implemented. A 400-nm-thick PECVD SiO_2 was deposited at 400 ^{o}C and the active area is defined by lithography. The opening of active area was done in two steps by RIE followed by wet landing on Si surface. The photoresist was then

removed by O_2 plasma. A 13-nm-thick silicon-oxynitride gate dielectric layer was grown by ICP-PECVD at 250°C, immediately before which the Si wafer was cleaned and a 4 minutes HF (0.55%) dip-etch was performed to achieve a high-quality oxide interface to the silicon. An 150-nm-thick Al(1%Si) reflective gate-metal layer was sputtered at 50°C to keep the grain size small.

The next step is the source/drain area definition exactly over the SiGe dot and good alignment accuracy is a crucial requirement for the positioning of the DotFET device. Moreover, it was necessary to introduce e-beam lithography to be able to define a narrow gate length of about 100 nm. A very good alignment accuracy is also possible with e-beam lithography [2, 134]. Therefore, e-beam alignment marks were created for the whole wafer alignment and for each DotFET device as show in Figure 5.10. The markers for e-beam lithography and seed holes patterning were written by optical lithography, while the gate and the source/drain extensions were written by e-beam lithography at Forschungszentrum Jülich. The Jülich group performed some tests to prove the feasibility of the e-beam lithography technology on SiGe dot alignment. Ordered SiGe dots of ~ 300 nm in diameter were grown with MBE on prepatterned substates with a dot spacing of 800 nm and with e-beam lithography lines were defined with a width of 50 nm aligned to the dots. In Figure 5.11 the e-beam lithography test is shown. The gate finger (from left to right) crosses the source/drain extensions right on the top of the dot where three overlays are applied. The overlay accuracy of e-beam defined structures on structures defined with optical lithography was measured to better than ±10 nm [134].

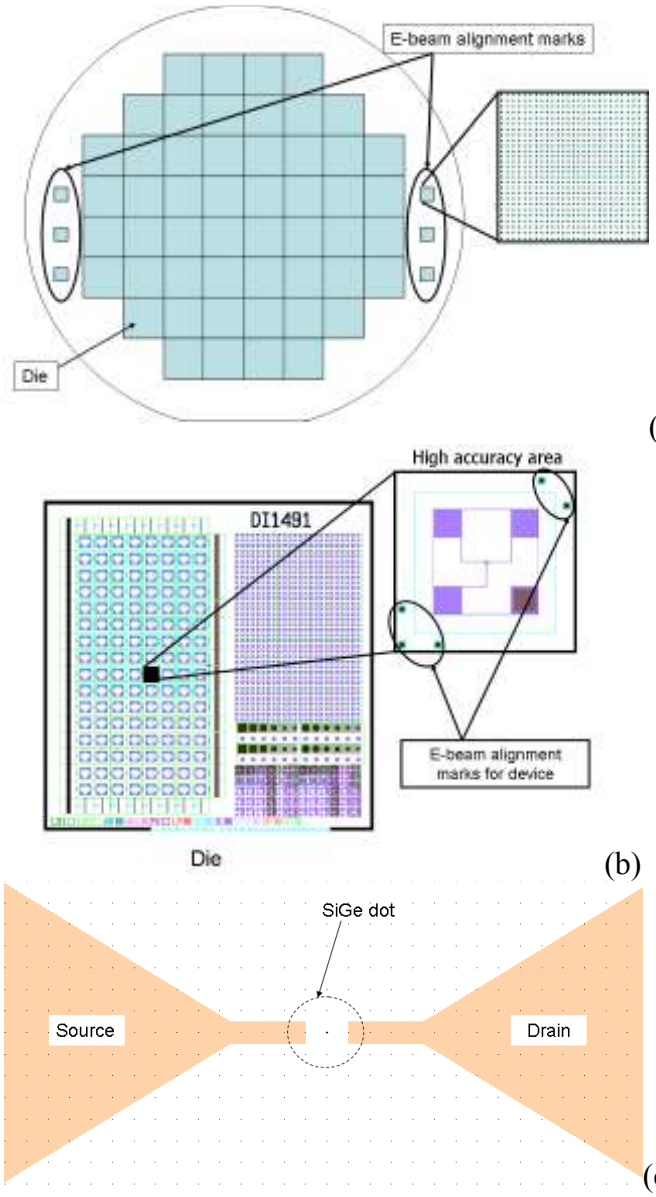


Figure 5.10: E-beam alignment marks created by optical lithography. (a) e-beam alignment marks for the whole wafer, (b) e-beam alignment marks for high accuracy alignment, and (c) the source/drain areas aligned to the SiGe dot.

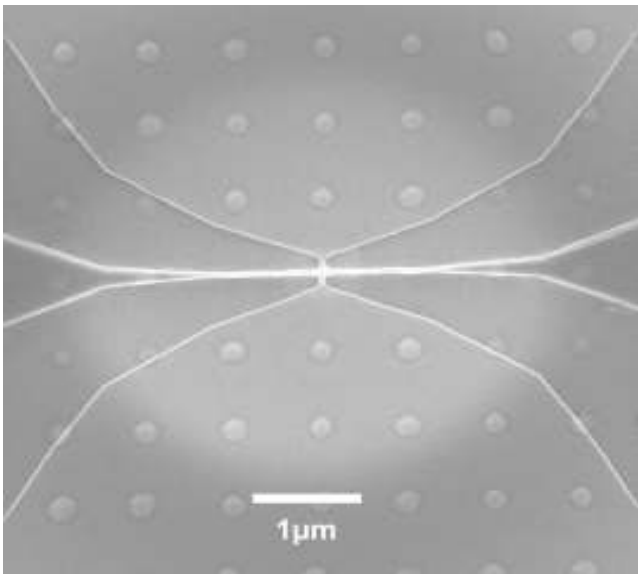


Figure 5.11: E-beam overlay test structure and prepatterning of the SiGe dots. The source/drain extensions and the gate finger were produced with e-beam lithography with an accuracy of ±10 nm [134].

After the e-beam lithography, the gate-stack is then patterned and the source/drain regions were defined by RIE (HBr/Cl_2 plasma) with soft-landing on the Si surface. A two-segment gate structure is chosen to reduce process complexity since it makes it possible to pattern the channel region with only one e-beam lithography step. Before the source/drain implantations a 15 seconds dip in BHF (1:7) solution needs to be performed to remove the native oxide and allow a uniform low energy implantation in the Si. Since the DotFET devices are submicron devices with a minimum gate length of about 50 nm, during the BHF dip-etch the Al functioning as metal-gate and reflective mask, was almost completely etched during this step (as mentioned in Chapter 3). In Figure 5.12 a SEM image is shown of such an Al gate region after the preimplant dip-etch. It is clear that a new

material with high resistance to BHF needs to be considered. Therefore, the integration a TiN layer is introduced in the next sub-section.

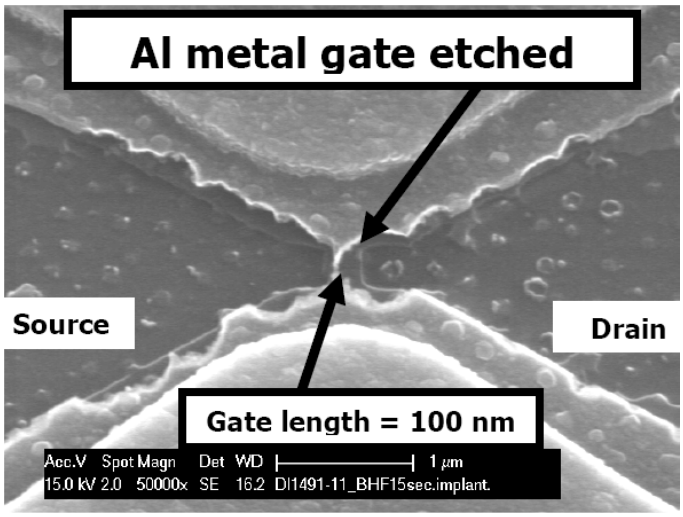


Figure 5.12: SEM image of an Al metal-gate region etched away by the preimplant dip-etch.

5.1.4 Titanium nitride/aluminium metal-gate

In order to prevent the etching away of the Al gate-metal during the preimplant BHF dip-etch, titanium nitride (TiN) was studied as a possible alternative. Titanium nitride was considered to be a potential candidate due to its high thermally stability and compatibility with conventional CMOS processing [135-138]. This material also possess the necessarily high resistance to HF solutions [139].

In view of these properties, the TiN was used as gate metal in order to protect the gate region during the preimplant dip-etch. Structures in a layer stack of SiO_xN_y(13 nm)/TiN(50 nm) were patterned on Si wafer and submitted to a 15 s BHF(1:7) dip-etch. SEM images were taken before and

after the dip-etch as shown in Figure 5.13. No etching of the SiO_xN_y and TiN layers are observed, indicating that they are highly resistant to BHF etch solutions.

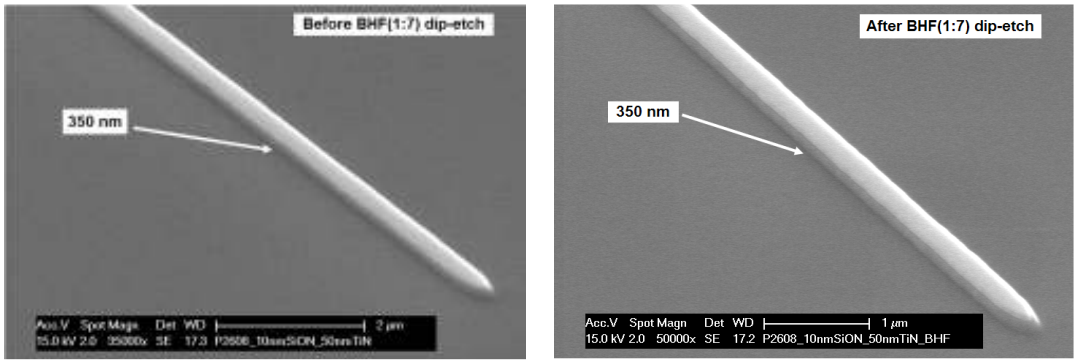


Figure 5.13: SEM images of a 350 nm wide strip of TiN on SiO_xN_y before (left) and after (right) a BHF(1:7) dip-etch for 15 s. The TiN is and the SiO_xN_y 13 nm thick.

In addition, Al-TiN/SiO_xN_y/Si capacitors were also fabricated and electrically characterized by capacitance-voltage measurements using a HP4284 LCR meter. The silicon oxynitride layers were grown on p-type single crystal Si (100) wafers using the parameters presented in Chapter 3. Before deposition, the substrates were cleaned by using a 4 min HF (0.55%) dip-etch for oxide removal. The substrate temperature was fixed at 250°C. The films grown in the ICP system were approximately 13 nm thick. A 50 nm TiN and 150 nm thick Al gate electrode were sputtered at 350^{o}C and 50^{o}C, respectively. On the wafer backside 675 nm Al(1% Si) was sputtered to form an ohmic contact. After that, the samples were sintered in a conventional furnace in forming gas at 400^{o}C for 20 min. The equivalent oxide thickness and interface trap level density were extracted from

capacitance values. Measurements were performed at low and high frequencies – 100 Hz and 1 MHz. Good C-V characteristics were measured and a low interface trap level density of the capacitors was extracted as shown in Figure 5.14.

These good results indicate that a TiN metal layer in combination with an Al(1%Si) reflective mask will be suitable for nanoscale metal-gate electrode processing. Therefore, for the DotFET devices the gate stack was chosen to be comprised of a 13-nm-thick ICP SiO_xN_y layer grown at 250°C, a 50-nm-thick TiN layer and a 150-nm-thick Al(1%Si) layer both deposited by sputtering at 350°C and 50°C, respectively.

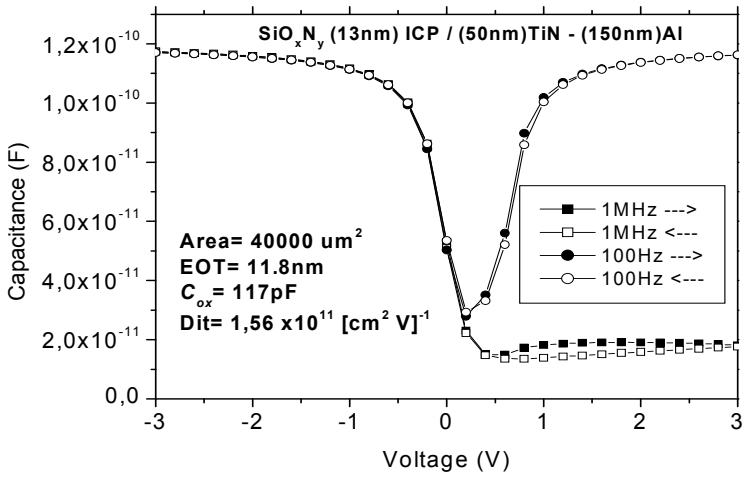


Figure 5.14: C-V characteristics of a gate stack comprised of an ICP SiO_xN_y dielectric grown at 250°C and a TiN-Al(1%Si) metal-gate.

5.1.5 Low energy implantation and laser annealing for ultrashallow source/drain doping

When the source/drain areas have been patterned by e-beam lithography, the etching away of the gate stack in these areas is carefully adjusted to remove all gate material from the small openings and to land on the Si surface. The surface is then prepared for the low energy implantation by a 15 s dip-etch in a buffered-HF (1:7) solution. A SEM image of the etched source and drain is shown in Figure 5.15 and 5.16. The major part of the source-drain current flows under the short gate section through the strained Si capping-layer, which is the main area of concern for enabling an evaluation of the influence of SiGe dots on the channel strain. The analysis by TEM shown in Figures 5.17a and 5.17b confirms that the SiGe dot and the top silicon layer have perfect crystallinity. The implantation of arsenic ions at 5 keV to a dose of 10^{15} ions/cm^2 at 30^o tilt angle in 8 directions was done immediately after dipping the wafers in a BHF(1:7) solution. The implanted regions were then laser-annealed with the Al-gate layer serving as the reflective mask. The laser energy density was varied from 850 mJ/cm^2 to 1000 mJ/cm^2 (50 mJ/cm^2 steps) with 1% overlap and a 1.75 x 2.5 mm^2 spot size. After the recrystallization of source/drain implanted regions the gate-metal track is patterned by optical lithography and etching of TiN/Al(1%Si) metal stack is performed by RIE. The accurate alignment of the structures patterned by e-beam to the dot structure is also confirmed by the SEM analysis shown in Figure 5.16. This SEM image is taken of a test structure with the Al(1%Si) gate patterned over the dot structure after the laser annealing.

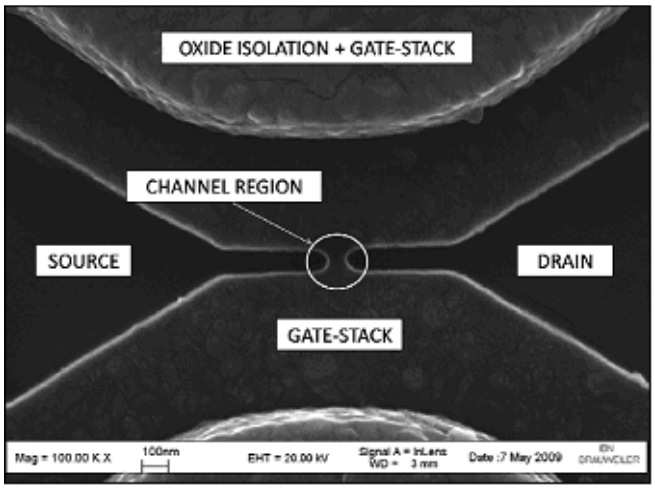


Figure 5.15: SEM micrograph after the etching of the gate stack patterned by e-beam lithography to define the source/drain/channel regions. Image from Forschungszentrum Jülich.

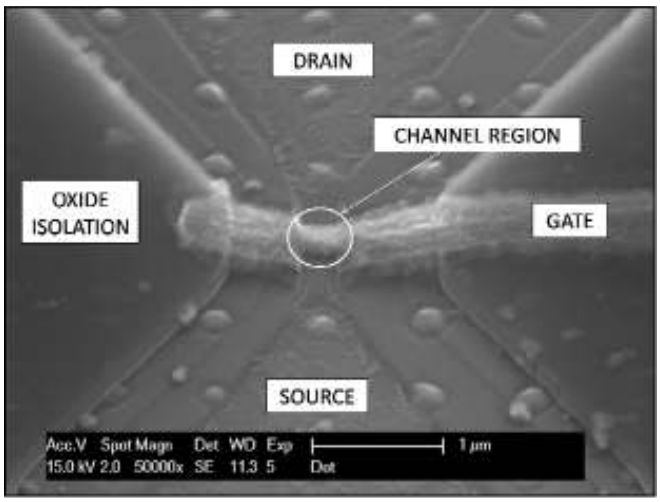
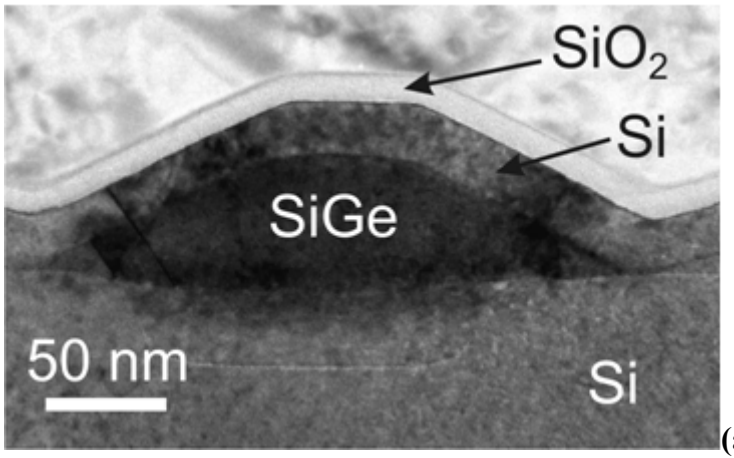
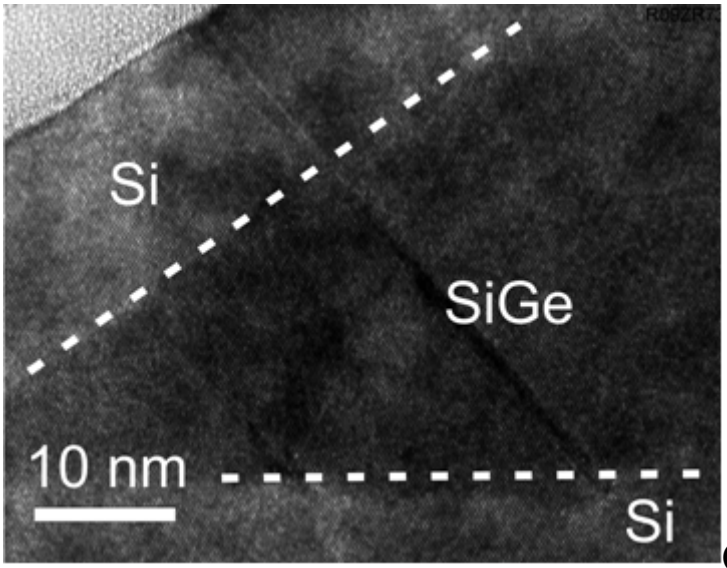


Figure 5.16: SEM micrograph of the DotFET device with gate-metal track patterned by optical lithography. The channel region is accurately aligned to a single SiGe dot.



(a)



(b)

Figure 5.17**:** TEM image of a DotFET cross-section (a). Close-up of the Si/SiGe/Si stack (b).

5.1.6 Contacts and metallization

After the gate patterning the photoresist is removed, the wafers are cleaned and an 800-nm-thick PECVD SiO_2 was deposited at 400 ^{o}C and contacts are opened to the source and drain with soft-landing on Si surface. This is

followed by the PVD of a 905-nm-thick Al(1%Si) layer at 350°C. The metal is then removed where not needed on the surface and contact windows are opened to the gate metal. A second layer of Al(1%Si) with a thickness of 1475 nm is then deposited and patterned to create the metal tracks connecting the active device areas to the metal pads. The final process step is alloying in a forming gas mixture for 20 min at 400°C. In Table 5.1 an overview is given of the process flow for the DotFET device fabrication.

Table 5.1: Process flow for the DotFET fabrication.

DotFET
p-type Si wafer (100)
Si cleaning
HF (0.55%) dip-etch, 4 min
Dirt barrier – 20 nm thermal SiO_2
Bulk implantation **20 $1x10^{12}$ / 50 keV, $1.1x10^{12}$ / 100keV, $1.3x10^{12}$ cm^{-2}, Boron**
Thermal SiO_2 removal (dirt barrier) – BHF (1:7)
Cleaning
Annealing- Furnace at 1000°C, 30 min in N_2 gas flow
Seed holes patterning (see Figure 6.4)
SiGe dot growth and Si capping layer (30 nm)
PECVD SiO_2 deposition – 400 nm at 400°C
Active area lithography
PECVD SiO_2 etching – RIE + wet etching (BHF (1:7))
Photoresist removal – O_2 plasma
Cleaning
HF (0.55%) dip-etch, 4 min
ICP oxynitride growth – 13 nm
50 nm TiN sputtered at 350°C
150 nm Al sputtered at 50°C **Al(1%Si) – reflective mask for laser annealing**
Source/drain e-beam lithography
Gate-stack etching (RIE) – source/drain openings
E-beam photoresist removal – O_2 plasma
Cleaning
BHF (1:7) dip-etch: 15 s
S/D implantation

As^+, 5 keV, 10^{15} ions/cm^2, 30^o tilt angle
S/D excimer laser annealing **0-850-900-950-1000 mJ/cm^2 (1% overlap)**
Cleaning
Gate lithography
RIE – Al(1%Si) of 150 nm and TiN of 50 nm
Photoresist removal – O_2 plasma
Cleaning
PECVD SiO_2 deposition – 800 nm at 400°C
Source/drain contact lithography
PECVD SiO_2 etching – RIE – soft-landing on Si surface
4 min HF (0.55%) dip-etch
905 nm Al(1%Si) sputtered at 350°C
Gate contact lithography
RIE- Al(1%Si) and PECVD SiO_2 etching, landing on Al metal-gate
Photoresist removal – O_2 plasma
Cleaning
Gate contact metallization - Al(1%Si) 1.4 µm
Lithography of metal interconnections to source, drain and gate
RIE – metal interconnection patterning
Photoresist removal – O_2 plasma
Cleaning
Alloying in forming gas at 400°C – 20 min

5.2 Electrical device characterization

The DotFET devices fabricated as described in the previous Section were measured on an Agilent 4156C parameter analyzer and the output characteristics are analyzed. Transistors were fabricated with a gate length varying between 50 nm and 200 nm and a gate width between 100 nm and 300 nm. The source/drain regions of the transistors were exposured to laser energy densities between 850 mJ/cm^2 and 1000 mJ/cm^2 and some devices were not annealed at all. The laser irradiation was done by a single shot of light from the XeCl excimer laser (wavelength 308 nm) with a pulse

duration of 25 ns at full-width half-maximum and a laser spot size of 1.75 x 2.5 mm^2. A set of reference devices were fabricated on the same wafer as the DotFETs using an identical layout, but without the underlying SiGe dot. By processing these devices on the same die as the DotFETs, the influence of wafer-to-wafer and over the wafer variations is minimized.

The V_{DS} versus I_D and the output characteristics of DotFETs were measured and the drain current points were extracted for the bias condition of V_G = 4 V and V_{DS} = 3 V. The summary of the drain currents extracted for devices with different dimensions is given in Figure 5.18 which shows an increase of the drain current for the laser annealed devices as compared to those that were not laser annealed. A maximum in drain current can be observed at 850-900 mJ/cm^2 but there is a significant spread in values above these energies. This spread, also towards lower drain current values, be attributed to degradation of the device performance sue to damage at the high laser energy levels in combination with the nanoscale dimensions of the device. From the results is possible see that the optimum energy density of the laser light seems to be in the range of 850-900 mJ/cm^2.

The size of the SiGe dot is in the range of 250-300 nm which means that transistors with gate width of 300 nm are very close to or larger than the dot diameter. In this case, a large portion of current between the source and drain may flow around the dot structure rather than through the silicon channel over the SiGe dot. Therefore, for the following analysis devices were chosen with gate dimensions that guarantee that the source and drain current flows through the channel region over the SiGe dot. A threshold voltage, subthreshold swing, DIBL and transcondutance varying between 1.57 V and 1.69 V, 270 V/dec. and 410 V/dec, 8 mV/V and 83mV/V, 1.5

μA/V and 2.47 μA/V were calculated, respectively. A high subthreshold swing can be observed for all DotFET devices and consequently the ratio between on and off currents is not optimal. The possible cause is related to the processing, since the bulk region under the channel is highly doped and this can increase the subthreshold swing. Reduction of the bulk implantation under the channel region and simulations needs to be considered for an optimum doping level to reduce the subthreshold swing close to 60 mV/V and adjust the threshold voltage. The Figures 5.19, 5.20, 5.21 and 5.22 show the output characteristics of DotFET devices with different dimensions and good characteristics of DotFET devices can be observed.

The most important results obtained from the electrical characterization of the processed devices are related to the comparison of DotFETs with the reference devices processed outside of the regular arrays of SiGe dots. Reference devices with different gate lengths and a gate width of 100 nm and 150 nm were fabricated and laser annealed at 900 mJ/cm^2. The variability plays a significant role in the measured devices due to their small dimensions resulting in a large spread of measured characteristics. However, the analysis of the measured data reveals that the DotFETs have higher current drivability under the same bias conditions as the reference devices. The improvement in the drain current is in the range between 2% and 35% for devices annealed at 850mJ/cm^2 and between 2% and 21% for devices annealed at 900mJ/cm^2, as shown in Figure 5.23.

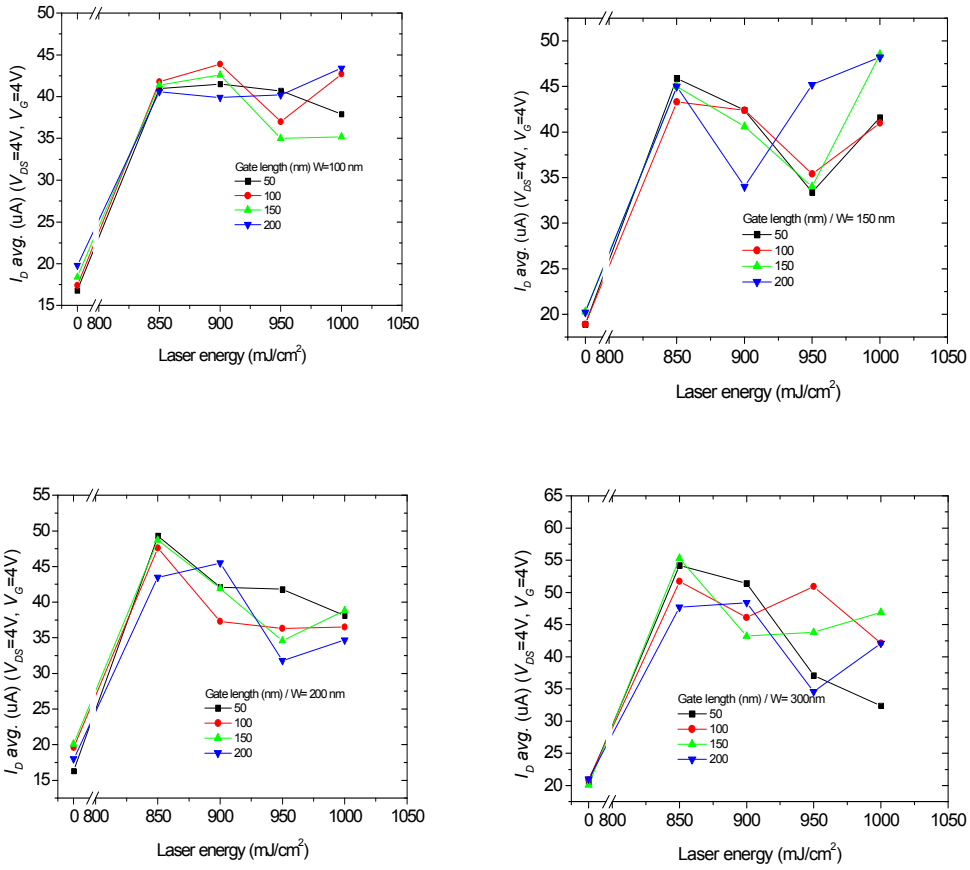
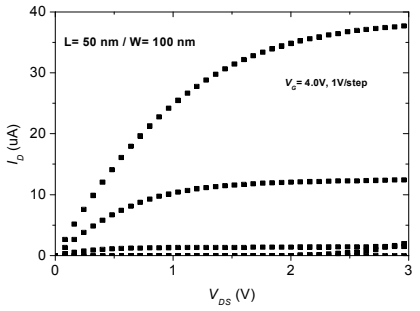
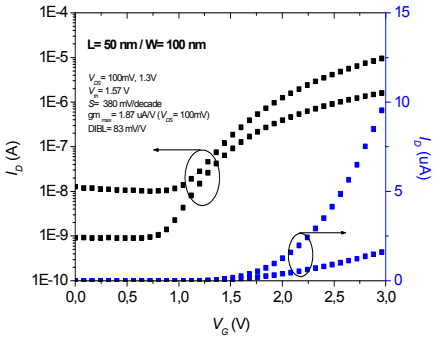
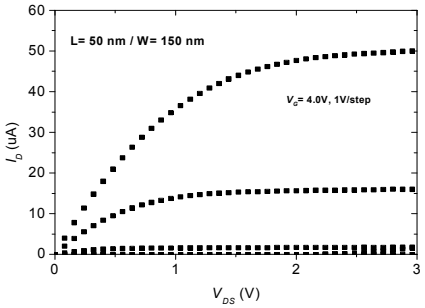
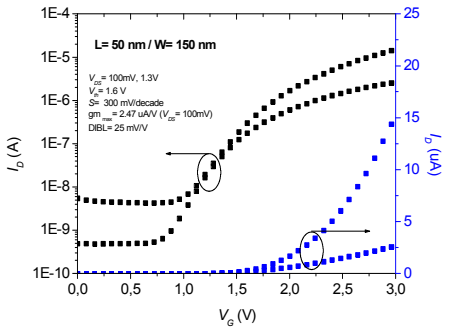


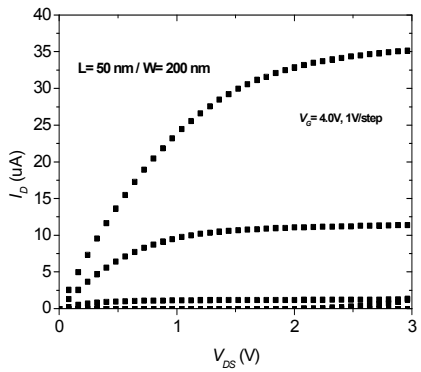
Figure 5.18: I_D versus laser-anneal energy for DotFETs with different gate lengths and a fixed V_{DS} = 3 V and V_G = 4 V.


L= 50 nm / W= 100 nm
V_G= 4.0V, 1V/step
I_D (uA)
V_{DS} (V)


L= 50 nm / W= 100 nm
V_{DS}= 100mV, 1.3V
V_G= 1.57 V
S= 380 mV/decade
gm$_{max}$= 1.87 uA/V (V_{DS}= 100mV)
DIBL= 83 mV/V
I_D (A)
I_D (uA)
V_G (V)


L= 50 nm / W= 150 nm
V_G= 4.0V, 1V/step
I_D (uA)
V_{DS} (V)


L= 50 nm / W= 150 nm
V_{DS}= 100mV, 1.3V
V_G= 1.6 V
S= 300 mV/decade
gm$_{max}$= 2.47 uA/V (V_{DS}= 100mV)
DIBL= 25 mV/V
I_D (A)
I_D (uA)
V_G (V)


L= 50 nm / W= 200 nm
V_G= 4.0V, 1V/step
I_D (uA)
V_{DS} (V)

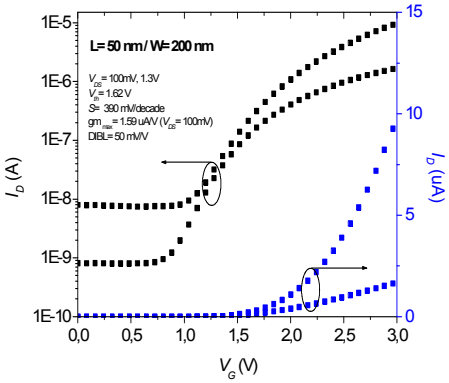
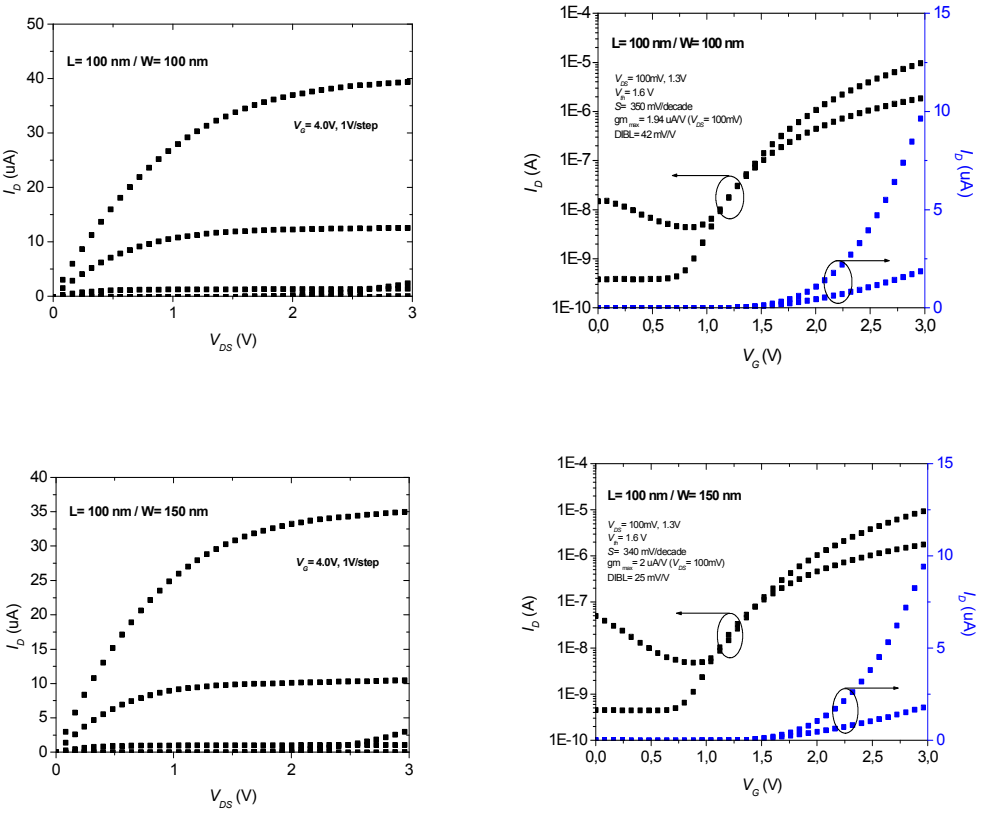

L= 50 nm / W= 200 nm
V_{DS}= 100mV, 1.3V
V_G= 1.62 V
S= 390 mV/decade
gm$_{max}$= 1.59 uA/V (V_{DS}= 100mV)
DIBL= 50 mV/V
I_D (A)
I_D (uA)
V_G (V)

Figure 5.19: I_D versus V_{DS} (left-side) and I_D x V_G (right-side) transfer characteristics curves of DotFET devices with different gate width and with source and drain laser annealed at energy of 900 mJ/cm^2. The gate length was fixed in 50nm.



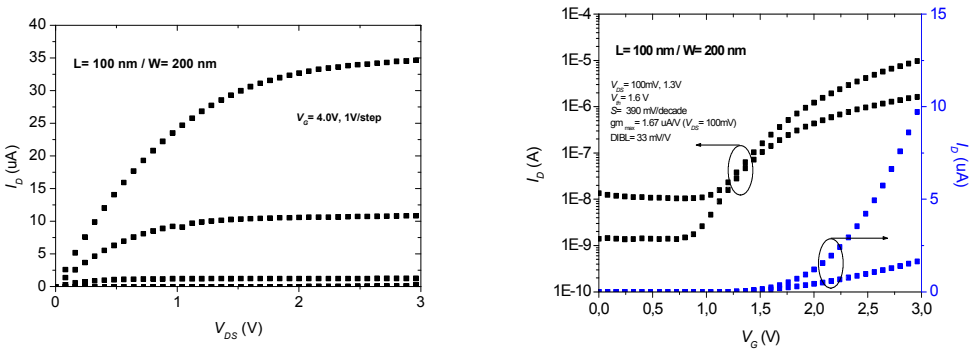


Figure 5.20: I_D versus V_{DS} (left) and I_D versus V_G (right) transfer characteristics of DotFET devices with different gate width and with source/drain laser annealed at an energy of 900 mJ/cm^2. The gate length has a fixed value of 100 nm.

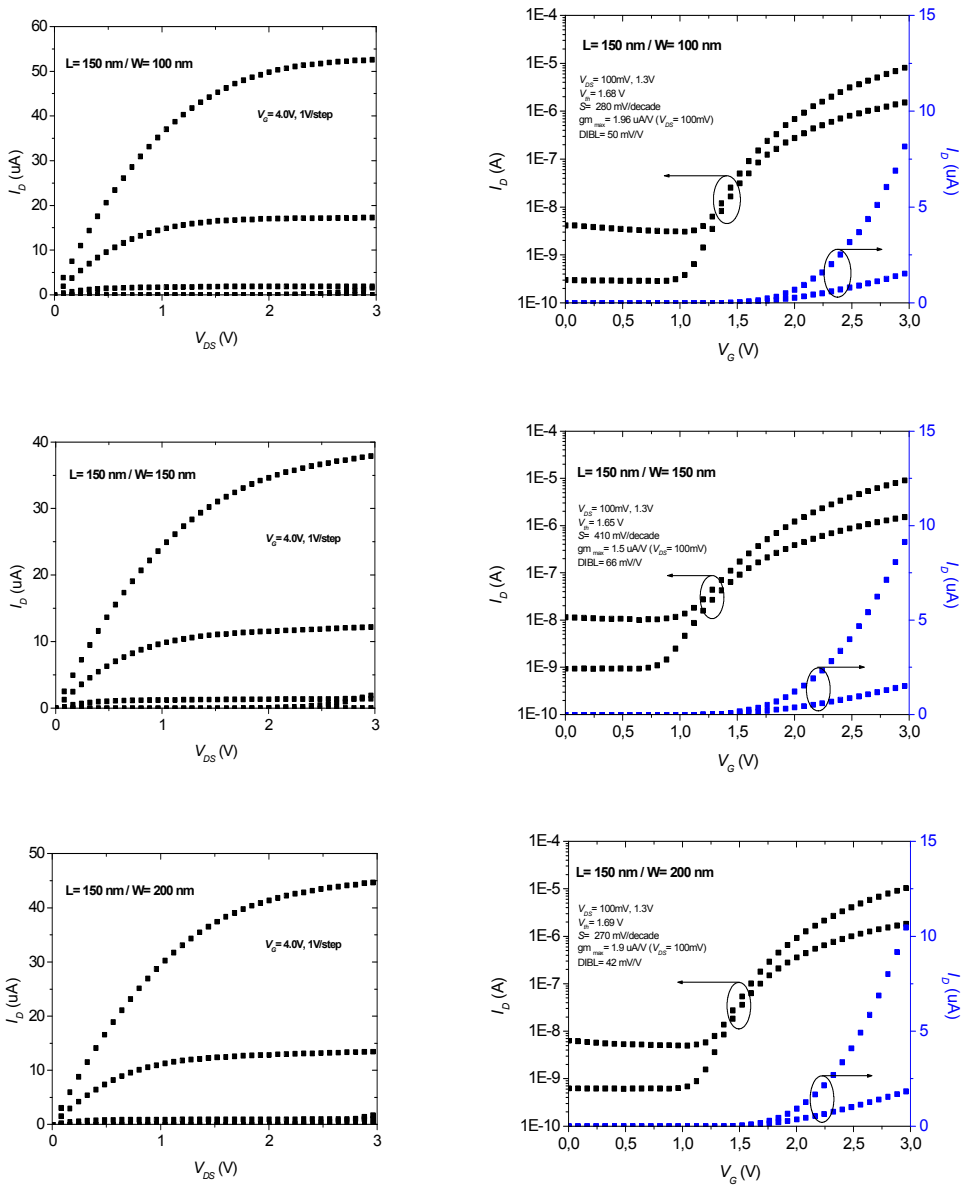


Figure 5.21: I_D versus V_{DS} (left) and I_D versus V_G (right) transfer characteristics of DotFET devices with different gate width and with source/drain laser annealed at an energy of 900 mJ/cm^2. The gate length has a fixed value of 150 nm.

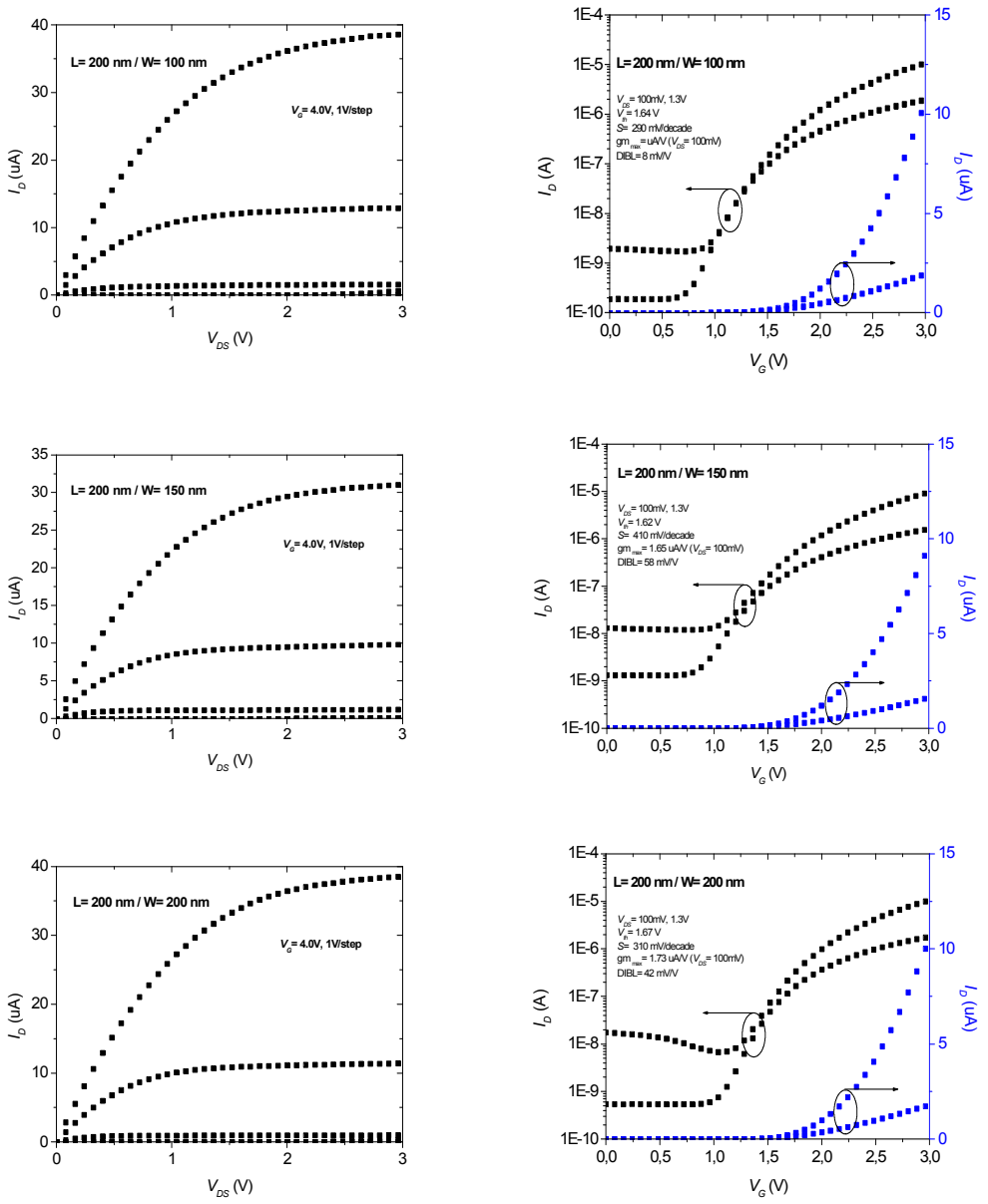


Figure 5.22: I_D versus V_{DS} (left) and I_D versus V_G (right) transfer characteristics of DotFET devices with different gate width and with source/drain laser annealed at an energy of 900 mJ/cm^2. The gate length has a fixed value of 200 nm.

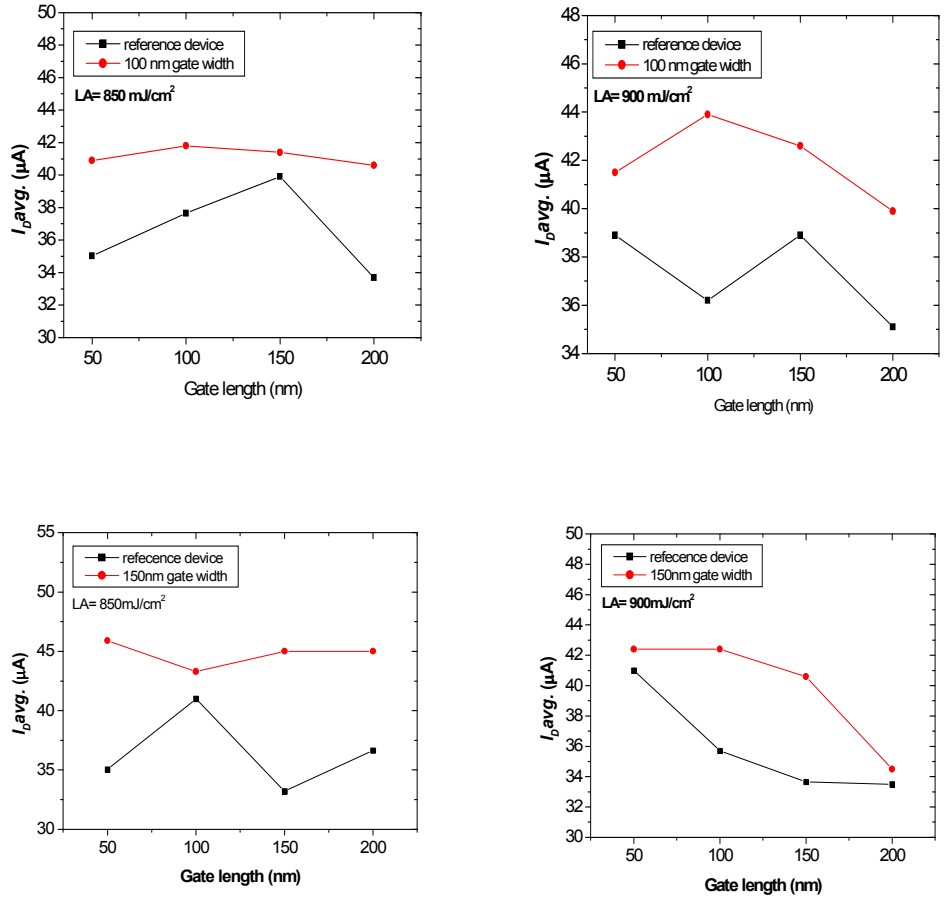


Figure 5.23: Comparison of the extracted drain current versus gate length for DotFETs and reference devices annealed at 850 mJ/cm^2 and 900 mJ/cm^2. The devices have a gate width of 100 nm and 150 nm. The drain current is extracted for $V_G = 4$ V, $V_{DS} = 3$ V.

5.3 D-DotFET devices

After the development of the technology already discussed in this chapter for the fabrication of the DotFET devices, the possibilities of adding steps to make a disposable DotFET were studied in order to create the aspired Silicon-on-Nothing type structure. The approach that seemed most accessible was to define holes close to the channel area and use a dry etch step to go through the top oxide down to the SiGe dot. Then a selective wet or dry chemical etch could be used to remove the germanium as indicated in Figure 5.24. The high Ge content inside the dot and the high selectivity of the etchant should then guarantee the removal of the dot without significant etching of the silicon or oxide. To access the Ge dot without damage to the active device part, high accuracy and small dimensions are required for the etching of the access holes. For this reason, it would be necessary to planarized the surface by, for example, depositing PECVD oxide over the structures and applying chemical mechanical polishing (CMP). Then the lithography could be performed by e-beam and the etching should be performed by highly anisotropic RIE.

The following etchants are found in the literature for efficiently etching selectively to the SiGe dot:

- Thermal approach: chemical vapour etching using a HCl/H_2 gas mixture at temperatures from 500^oC-750^oC. The etch-rate increases when the Ge content increases (anisotropic etching) [140];

- Plasma dry: plasma of pure CF_4 at low temperatures (isotropic etching) [14];

- Wet chemistry:

- selective wet etching based on oxidant and etching reagents. A mixture composed of hydrofluoric acid (HF), nitric acid (HNO3), acetic acid (CH3COOH) and water can be used (HNA solution). The etching rate depends of the Ge concentration (isotropic etching) [146];

- selective etching using a mixture consisting of ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2) and deionized water [147, 148].

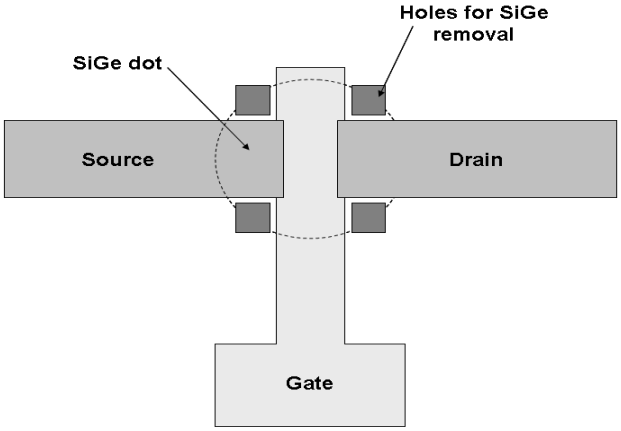


Figure 5.24: Proposed scheme for the removal of the SiGe dot in a DotFET in order to realize a D-DotFET: (a) oxide deposition by PECVD and planarization by CMP for lithography accuracy improvement, (b) positions of four access holes defined by e-beam.

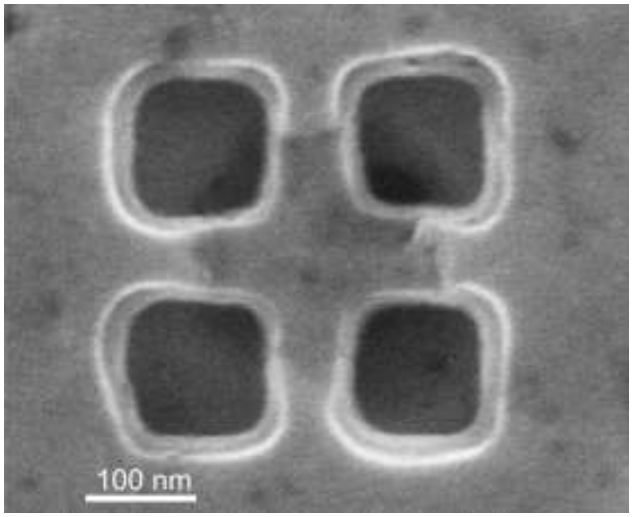


Figure 5.25: Four access holes defined by e-beam lithography and etched by RIE for SiGe dot removal. The SiGe dot is the dark circular area in the middle of the four holes. Data from IFW Dresden.

At the IFW Dresden it was investigated whether the SiGe dot could be selectively etched away by using a mixture of 28% NH_4OH, 31% H_2O_2 and deionized water. In order to reach the edges of the SiGe island, an additional e-beam step had to be introduced in the process flow of the DotFET structures to define the holes through which the SiGe dot could be removed. After definition of the access holes, an anisotropic etching of the gate-stack and Si capping-layer could be performed to reach the SiGe dot and it is in principle possible to remove the dot by wet etching with high selectivity to silicon and the gate materials. The strain in the silicon bridge should then be preserved by the gate-stack. Since the wet etching solution is not selective to Al, it would be necessary to replace the Al/TiN gate with a purely TiN gate metal. An example of a sample where the SiGe dot was is

shown in Figure 5.25. This sample was made for testing purposes only and was not submitted to full DotFET processing.

5.4 Self heating simulations: D-DotFET versus SOI-FET

For the D-DotFET devices an improvement is expected in the electrostatic properties that is comparable to an SOI-FET but without the thermal drawback of the poor heat conduction associated with an SOI substrate. The Technical University Wien simulated the D-DotFET electrthermally and made the comparison to DotFET devices on SOI substrates. For this simulation at $V_G = V_{DS} = 1.5$ V was assumed. The profiles of the temperature distribution are shown in Figure 5.26. In the D-DotFET a reduction of self-heating is observed as compared to the SOI-DotFET. A peak in the temperature can be observed in the pinch-off area of the channel.

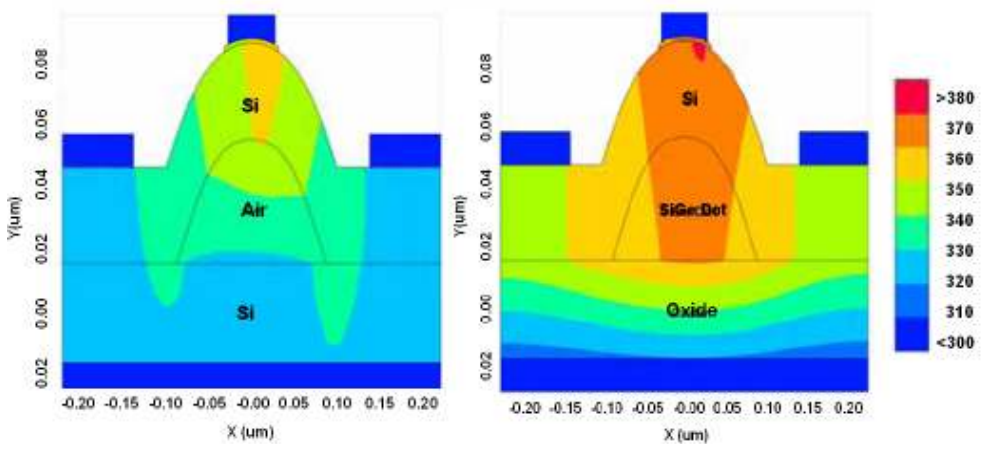


Figure 5.26: Comparison of the temperature distribution in a D-DotFET and a DotFET on SOI. Data from Technical University Wien.

5.5 Conclusions

High performance n-DotFET devices have been successfully fabricated at low temperature, thus avoiding excessive Ge diffusion. Transistors with a minimum gate length dimension of 50 nm using TiN/Al(1%Si) metal-gates were processed. A SiGe dot grown by MBE was used as stressor material to obtain locally in the gate area a strained Si channel. Before the SiGe dot growth, an array of holes patterned by optical lithography using a double pattern transfer technique was developed. The SiGe/strain-Si layers were studied and simulated and a good improvement of drain current drivability was observed. To obtain ultrashallow junctions and high activation of source/drain dopants, excimer laser annealing was used and the best energies for annealing these structures were found to be between 850 mJ/cm^2 and 900 mJ/cm^2. High laser energies can degrade the performance of the submicron devices. E-beam lithography was used to define nanoscale gate dimensions in the central region of the dot and a 1-µm-wide gate finger is defined to contact this narrow gate. Thus a part of the current between the source and drain flows around the dot structure rather than through the silicon channel over the SiGe dot. Despite this effect, it is still possible to determine the influence of the strain on the drain current.

The electrical characteristics show a drain current enhancement between 2% and 35%. The simulations show enhancements due to the strained Si layer of 20% - 22%. The small dimensions result in a large spread of measured characteristics. Nevertheless, the impact of the strain Si layer can be indentified.

The SiGe dot was removed on a test sample using ammonium hydroxide, hydrogen peroxide and deionized water which shows the possibility of fabricating a D-DotFET device. Simulations of D-DotFETs and DotFETs fabricated on SOI substrates were done and the results show a reduction of self-heating for D-DotFET devices.

Chapter 6

Conclusions and recommendations

In this thesis several new processing techniques were combined to fabricate DotFETs with which the transfer of strain from a buried SiGe dot to a silicon channel above the dot could be evaluated. Central in the fabrication flow is the use of excimer laser annealing to replace high temperature thermal steps that would cause the Ge to diffuse out of the dot into the surrounding Si. Excimer laser annealing was successfully applied to the fabrication of diodes and MISFETs with good electrical characteristics. To keep the processing temperature low after dot formation, a low-temperature gate dielectric and metal stack was also developed so that the whole source/drain and gate regions of the transistor could be fabricated below 400°C. This low-temperature process flow that was developed for fabrication of DotFETs with the dot preserved during the whole processing, demonstrates the robustness of the dots and the desired strain enhanced mobility. The overall results presented in this thesis together with the theoretical work performed by Vienna/Milano and the strain analysis

performed by Linz, give strong evidence that SiGe dots can be a viable way of transferring strain to the Si channel of MOSFETs for the purpose of enhancing the mobility. Important factors are the demonstrated precision with which the position, size and shape of the dots can be fabricated. The potential early removal of the dot, that would make the fabrication of a D-DotFET possible, would also make the integration in existing advanced CMOS processes a small evolution rather than revolutionary and therefore this could be an attractive option for CMOS downscaling to the 10 nm node.

The main conclusions from this work are:

- Excimer laser annealing of implanted dopants is a very promising technique for ultrashallow junction formation. The junction depth can be precisely controlled by low energy implantation of the dopants. After implantation an amorphous Si layer above the *c*-Si is formed and during the laser annealing this layer will melt at a lower temperature than in *c*-Si which serves as seed for recrystallization. The sheet resistance of the laser annealed layer depends strongly of the laser energy and implantation parameters. Junctions that are 13 nm deep, as verified by SIMS and TEM imaging, have been demonstrated with 5 keV As^+ implants at a 45° tilt and annealed with a 1000 mJ/cm^2 laser irradiation.

- Laser processing requires careful optimization, in particular to avoid the build-up of hot-spots that can lead to ablation of the Al reflective mask. This problem can be minimized by reducing the thermal

resistance of the dielectric layer under the Al reflective masking layer. In this respect the DotFET structure is attractive because the gate dielectric is only a few nm thick and it was possible to find a configuration where the source/drain regions could be annealed without damaging the gate dielectric-metal stack. This is a point that should be studied in more detail in relationship to the specific structure to be annealed.

- With the presented process flow for fabricating laser-annealed diodes self-aligned to the contact window it is possible to create good quality ultrashallow junctions. When pure oxide windows are employed, the necessary wet dip-etching in HF requires that the etch rate of the oxide is low enough to prevent exposure of the laser annealed junction at the window perimeter. A high implantation tilt angle can also be used with advantage to increase the overlap of the implant with the window perimeter and achieve much better diode characteristics. Diodes with an ideality factor of 1.05 have been fabricated using a thermal grown oxide as an isolation layer.

- Both before low energy implantation and contact metallization, a 4 minutes dip in low concentration HF or a 15 seconds dip in buffered-HF (1:7) solution is strictly recommended for surface passivation and native oxide removal. Without these steps, good electrical performance of the devices is not guaranteed.

- MIS capacitors were fabricated at low temperature using stacks of Al(1%Si) and TiN as metal gates. Silicon oxynitride and aluminium

oxide layers were studied as gate dielectrics and good electrical characteristics were obtained. The measurements show that there is a low interface trap density and low leakage current densities. In future, a more thorough investigation of the dielectric layer could be done by using Fourier transform infrared spectroscopy (FTIR) or Rutherford backscattering spectrometry (RBS) to identify compounds and investigate sample composition.

- A low temperature ($\leq$ 400 ^{o}C) process for n and p-MISFET fabrication was developed where the excimer laser-annealing technique was used to activate the implanted dopants in the source/drain region. The electrical performance of the devices was good with respect to the drain current driving capability. The drain current drive is dependent on the laser energy density and consequently on the source/drain sheet resistance and gate length. An incomplete epitaxial regrowth of the implanted regions during the laser processing close to the gate edge was observed indicating that the gate stack is providing cooling of the perimeter regions. Since the next generation metal oxide semiconductor field-effect transistors require very thin equivalent oxide thickness, the heat conduction will be improved and this edge epitaxial effect reduced. Ultrashallow source/drain junctions were activated and TEM imaging revealed that the junctions were 10-12 nm deep for a 1000 mJ/cm^2 laser energy.

- A 66% and 1% laser-spot overlap was studied and for 66% overlap a higher dopant activation was achieved and consequently more

current was driven through the channel. In fact, by increasing the overlap an extra heating can be expected.

- The DotFETs and D-DotFETs represent novel concepts for the fabrication of strained Si MOSFETs that have significant advantages as compared to SOI technology: there is an improvement in the electrostatic properties and a reduction of the self-heating and it is a low cost technology that does not require the use of expensive SOI substrates. In the D-DotFET approach, the channel is fabricated in a freestanding Si bridge stabilized by the gate stack and the SiGe dots are used to transfer the strain to the channel. Several parts of the device fabrication and simulations were performed in cooperation with other universities. A process using a double pattern transfer technique was used for seed-hole formation, the SiGe dot and strained Si capping layer were grown by MBE and the actual device was built on these layers. The DotFET devices have been successfully fabricated at low temperature and transistors with gate length of 200 nm down to 50 nm using a TiN/Al(1%Si) metal-gate were processed. Low temperature processing ($\leq 400^{o}$C) after SiGe dot growth is very important to avoid any Ge diffusion during the processing which can change the characteristics of the SiGe-dot and strain transfer to the Si stack. The electrical characterization revealed that good functional devices were produced with source/drain laser annealed at 850-900 mJ/cm^2 and an enhancement of the drain current between 2% and 35% was measured. Due to the small dimensions of our devices, a large spread of measured characteristics was observed.

- For the fabricated devices, a source and drain current flowing around the dot structure can be expected due to large gate finger patterned by optical lithography (1 μm). In future, the portion of current that flows outside the dot region could be reduced by a second e-beam lithography to define a perfect gate finger over the dot.

- Silicon oxynitride used as a gate dielectric can be substituted by other materials with a high dielectric constant as, for example, Al_2O_3 or HFO_2, to reduce the equivalent thickness, thus improving the device performance by increasing the drive current and reducing leakage currents through the gate.

- The activation of dopants in the source/drain regions needs to be analyzed more carefully to be sure that the thermal effects close to the gate stack are not predominent enough to be destructive for submicrom devices.

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List of symbols and abbreviations

List of symbols

ε_o - permittivity of free space

ε_{ox} - oxide dielectric constant

ε_{Si} - dielectric constant of silicon

n_i - intrinsic carrier concentration

λ - Debye length

μ - mobility of the charge carriers

ϕ_M - difference in the work functions

ϕf - Fermi potential

ψ_F - difference between the intrinsic level and Fermi level

A - gate area

C_{fb} - flat band capacitance

$C_{min.}$ - minimum depletion layer capacitance

C_{HF} - high-frequency capacitance

C_{LF} - minimum value of the capacitance

C_{ox} - gate-oxide capacitance

c-Si - crystalline-Si

C_{sfb} - depletion layer capacitance

D_{it} - interface trap level density

e_{xx} - channel length direction

e_{yy} - channel width direction

e_{zz} - vertical direction

g_m – transconductance

I_{DS} - drain current

I_{off} - off current

I_{on} - on current

L - gate length

N_a - dopant density in the channel

N_2 - nitrogen

O_2 - oxygen

q - magnitude of electronic charge

Q_{ss}/q - of effective charges in the gate dielectric

R_{ch}: channel resistance between the source and drain of the transistor

R_{co}: contact resistance between the metal contact and implanted source/drain regions

R_{ol}: overlap resistance in the overlap region between the gate and the source/drain

Rs - sheet resistance

R_{sh}: resistance determined by the sheet resistance of the source/drain regions.

R_{sp}: Spreading resistance

$R_{S/D}$ - source/drain resistance

SiO_2 - Silicon dioxide

SiO_xN_y - Silicon oxynitride

SiN_x - Silicon nitride

t_{ox} - dielectric oxide thickness

Xj - junction depth

V_{DD} - power supply voltage

V_{DS} - drain voltage

V_{FB} - flat-band voltage

V_{GS} - gate voltage

V_{Th} - threshold voltage

W - channel width

XeCl - xenon chloride

List of abbreviation

AFM - Atomic Force Microscopy

ALD - atomic-layer deposition

Al_2O_3 - aluminium oxide

a-Si - amorphous-Si

BHF - buffered-HF

CMOS - Complementary-Metal-Oxide-Semiconductor

CMP - chemical mechanical polishing

C-V - capacitance-voltage

CVD - chemical-vapor deposition

DIBL - drain-induced barrier lowering

Dimes - Delft Institute of Microsystems and Nanoelectronics

D-DotFET - Disposable Dot Field Effect Transistor

EBL - e-beam lithography

EOT - equivalent oxide thickness

ELA - Excimer Laser Annealing

FEM - finite-element-method

FP6 - Sixth Framework Program

FTIR - Fourier transform infrared spectroscopy

FWHM - full width at half maximum

FZ Jülich - Forschungszentrum Jülich

He - helium

HF - hydrofluoric acid

HfO_2 - hafnium oxide

ICP - inductively coupled plasma

IL - interference lithography

I-V - current-voltage

ITRS - International Technology Roadmap for Semiconductors

JFETs - Junction Field Effect Transistors

LOCOS - Local Oxidation of Silicon

LPCVD - Low Pressure Chemical Vapor Deposition

MBE - Molecular Beam Epitaxy

MEMS - Micro-Electro-Mechanical Systems

MIS - metal-insulator-semiconductor

MISFET - Metal-Insulator-Semiconductor Field Effect Transistor

MOS - Metal-Oxide-Semiconductor

MOSFET - Metal-Oxide-Semiconductor Field Effect transistor

NIL - nano-imprint lithography

PE - plasma-enhanced

PECVD - plasma-enhanced chemical-vapor-deposition

PVD - physical vapor deposition

RBS - Rutherford backscattering spectrometry

RIE - reactive-ion etching

RF - radio frequency

RTP - Rapid Thermal Processing

SCE - Short Channel Effect

SiGe - Silicon Germanium

SIMS - Secondary Ion Mass Spectrometry

SOG - Silicon-on-Glass

SOI - Silicon-on-Insulator

SON - Silicon-on-Nothing

S-K - Stranski-Krastanow

SS - subthreshold swing

STI - Shallow Trench Isolation

TED - Transient Enhanced Diffusion

TEM - Transmission Electron Microscopy

TEOS - tetraethyl orthosilicate

TMA - trimethylaluminium

TiN - titanium nitride

TUDelft - Delft University of Technology

USJ - ultrashallow junctions

UTB SOI - Ultra-Thin-Body Silicon-on-Insulator

XRD - X-ray diffractometry

Summary

by Cleber Biasotto

The work presented in this thesis was performed in the context of the European Sixth Framework Program FP6 project "Disposable Dot Field Effect Transistor for High Speed Si Integrated Circuits", referred to as the D-DotFET project. The project had the goal of realizing strain-enhanced mobility in CMOS transistors by transferring strain from a self-assembled germanium dot to the channel of a transistor fabricated above the dot. The initial idea was to dispose of the Ge dot underneath the channel after the gate processing so that the gate-stack would also serve to stabilize the channel-bridge and maintain the strain induced in the channel silicon by the Ge dot. The advantage of using a SiGe dot as a strain source is its scalability to as low as 10 nm gate dimensions, which is not obvious for currently used methods for imparting strain on the Si channel. Furthermore, the D-DotFET structure offers advantages for the electrostatic and electrothermal behavior of MOS devices. For example, SOI devices with fully-depleted channel are a solution for short-channel effects but the insulating oxide beneath the device introduces a thermal management issue. This problem is solved in Silicon-on-Nothing (SON) devices because the insulating region is then only found under the gate with the source and drain regions still being anchored to the thermally conductive bulk silicon. The D-DotFET resembles the SON transistor but with the added advantage of strain-enhanced device gain and speed. In that way the D-DotFET combines four potential improvements: strain enhanced performance, scalability to future ~ 10 nm generations, suppression of short-channel effects, and good heat dissipation.

Research was done in several areas to assure that the stringent requirements on uniformity, reproducibility and reliability could potentially be met to

transfer the D-DotFET concept to advanced CMOS. The growing of silicon germanium (SiGe) dots with the necessarily high Ge content was first developed, and uniformity and reproducibility were brought to a high level of perfection. The strain of both bare and overgrown dots was extensively analyzed both experimentally and theoretically. Then, the strain that could be transferred to the channel of a MOSFET was evaluated in terms of mobility enhancement via device simulations, and lastly, the actual integration of dots was demonstrated in a low-complexity n-MOSFET research process that was specially tailored to this application, which is the topic of this thesis.

The Dimes cleanrooms were not equipped to set up a state-of-the-art CMOS process to investigate the D-DotFET concept. However, the available expertise and equipment was suitable for running a more advanced process, where excimer laser annealing could be implemented to replace the standard rapid thermal annealing and a metal gate could replace the standard polysilicon gate. Furthermore, the patterning of ~ 100 nm gate features was performed by e-beam lithography by the project partner Forschungszentrum Jülich. To avoid as many nanoscale lithography steps as possible, geometry with large source-drain contacting areas was devised so that only one step, the ~ 100 nm gate definition itself, needed to be patterned by e-beam.

Additionally, since the goal was in first instance to verify the strain-enhanced gain induced by the dot, it was decided to significantly simplify the transistor processing by retaining the dot throughout. A “DotFET” rather than a “D-DotFET” was therefore fabricated. This meant that only low-temperature processing steps could be performed after the dot formation, in order to avoid intermixing of Si and Ge and consequent strain relaxation. This was realized in a dedicated n-MOSFET process where the temperature was kept below 400°C after epitaxy by using low-temperature gate dielectrics and a metal gate self-aligned to implanted and laser annealed source/drain regions.

The SiGe dots used for the DotFET fabrication were grown in a self-assembling Stranski-Krastanow mode that allows single-crystalline dots of SiGe to grow in three-dimensions on predefined seedholes. Under appropriate conditions this growth is defect free and can easily be scaled down. The 3D growth of the SiGe allows a higher Ge content inside the dot before the onset of crystal dislocations as compared to the growth of 2D

SiGe layers of similar thickness. The smaller the SiGe dots the higher the Ge content that can be maintained without defect formation and consequently a higher strain can be exerted on any Si layer grown over the dot. For the devices described in this thesis, the dots were grown by MBE on a regular seedhole pattern of submicron periodicity etched into the Si. The growth was investigated in detail to determine the optimum growth conditions and seedhole-patterns for achieving a dot-size and strain level suitable for constructing a MOSFET over the center of the dot structure where the biaxial tensile strain could be exploited for channel mobility enhancement.

For a uniform and reproducible SiGe dot growth, excellent results were achieved by a location-controlled growth method where large, regular arrays of seedholes are patterned on an otherwise flat Si substrate. In the present work, both i-line optical lithography and e-beam lithography (EBL) were used to pattern such holes in (100) Si wafers. In the case of e-beam lithography a very good control of the seedhole positions and size is obtained and the resulting dots are extremely regular. The present DotFET fabrication required a dot size that could accommodate a gate of length ~ 100 nm. For this purpose the most suitable seedhole arrays were the ones with a periodicity of 800 nm that rendered a maximum dot diameter in the range of 230 nm. EBL patterning of this configuration was used for the device fabrication, while analysis of the dot properties was also performed on samples processed with optical lithography. The growing of the dots on the seedhole pattern starts with the deposition of a Si buffer layer which smoothes the surface. The dots are then grown at 720°C from a pure Ge source

In **Chapter 2**, a simple, low-temperature process flow for achieving good quality ultrashallow n^+p junction diodes has been demonstrated for 5 keV As^+ implants activated by excimer laser annealing. Much research has recently been done using ELA techniques due to the extremely short annealing times that potentially eliminate transient enhanced diffusion effects, reach high levels of dopant activation and give abrupt junctions. Compared to conventional rapid thermal anneal procedures ELA offers the advantage of a good control of the junction depth, where a reduction of the vertical implantation range can serve as a direct means of also decreasing the junction depth. The laser processing research performed at Dimes in the past, rather than being aimed at the fabrication of source and drain regions

for CMOS, has been motivated by the need to have access to good quality diodes in integration situations where only very low temperatures are permitted, such as in silicon-on-glass processing.

With respect to the bulk laterally-uniform part of the diode away from the perimeter, it is important that the Si-surface to be implanted is smooth and native-oxide free before implantation. The implant needs to be so shallow that the melt region encompasses the whole implanted region but deep enough to avoid laser-induced-surface-structuring effects on the Si surface from affecting the underlying metallurgic junction region. Tilted implants can reduce the final junction depth of the 5 keV implants to below 20 nm. With respect to the perimeter of the diode, the key to achieving diodes of good quality is the termination of the metallurgic junction at an oxide-to-silicon interface that is of good quality. In the presented experiments this is achieved by using a thin layer of thermal oxide to cover the Si under a thicker low-temperature isolation layer. The oxide at the interface is a 30-nm-thin layer of thermal oxide, which is still sufficiently thick to avoid excessive widening of the contact window during the dip-etch used to remove native oxide before metallization. After the growth of the isolation oxide, all processing steps are performed at temperatures below 400ºC. A reflective mask of Al is applied to localize the laser melting of the silicon to the desired diode region and to protect the perimeter. The tilted implants also increase the overlap of the oxide isolation with the diode perimeter, making the process more robust which in turn reduces perimeter leakage. The completeness of the laser melt at the perimeter depends on the thermal conductivity of the surroundings. Less melting of the perimeter with respect to the bulk is identified by TEM analysis in diodes processed in Dimes and this may be a source of extra perimeter leakage that needs to be taken into account when designing a specific process flow and diode structure. The best results are achieved here with an implant of $2x10^{15}$ cm^{-2} at tilt of 30°. For diodes with an area of 80 μm^2 this gives an ideality factor of 1.04 and reverse leakage at 2 V in 10^{-5} A/cm^2 range.

The low-temperature processing needed for the DotFET transistor puts heavy demands on the processing temperature of the gate dielectric which conventionally is a high-quality thermal oxide grown at temperatures above 850°C. In **Chapter 3** a study is presented of a number of dielectric layer-stacks formed at temperatures below 400°C that could potentially be used as DotFET gate material. MIS capacitors were fabricated with different gate-

dielectric layer stacks and electrically characterized, and a comparison was made to capacitors with a SiO_2 interface layer thermally-grown at ≤ 700°C. It was chosen to investigate atomic-layer deposited Al_2O_3 layers because this technique gives an excellent uniformity, conformality, precise control of the thickness of the films, and it is possible to deposit high-quality layers at low temperature. Cycles of TMA and water were applied in order to deposit the Al_2O_3 layers at a temperature of 300°C. The SiO_xN_y films with a low concentration of N were grown by inductively coupled plasma at a temperature of 250°C.

The results of capacitance-voltage and current-voltage measurements demonstrated that ALD Al_2O_3 and ICP SiO_xN_y exhibited a dielectric constant of 4 and 8, respectively. With ICP SiO_xN_y, capacitors were fabricated with low interface trap level density and low effective charge density, $< 10^{11}$ $cm^{-2}eV^{-1}$ and $<10^{11}$ $cm^{-3}eV^{-1}$, respectively, as well as low leakage current density ($< 10^{-7}$ A/cm^2). For pure Al_2O_3 layers the interface quality to Si was poor and in order to improve this situation, a high-quality interface layer was either grown or deposited between the alumina and Si substrate. Due to the simple, fast processing and good quality of the ICP SiO_xN_y dielectric at low temperature, the SiO_xN_y was finally chosen for the fabrication of the MOSFETs and DotFETs.

The processing techniques for the fabrication of n^+p diodes with ultrashallow junction annealed by excimer laser technique and capacitors using Al_2O_3 and SiO_xN_y gate dielectrics were combined to create a simple MISFET device presented in **Chapter 4**. The fabrication of n- and p-MISFET devices was demonstrated for processing temperatures below 400°C. Four important processing steps need to be performed in order to have good electrical device performance: (*i*) for a good quality growth of ICP-SiO_xN_y, the Si surface must be cleaned immediately before the growth, achieved with a HF dip-etch; (*ii*) a dip in BHF is performed immediately before source/drain implantation to remove the native oxide on the Si surface and achieve a uniform implantation of the low-energy ions; (*iii*) a RIE process with low RF power is used for oxide etching to open the source/drain contact windows in order to reduce damage to the implanted silicon surface; (*iv*) a HF dip-etch is used to remove native oxide before source/drain metallization and ensure a low-ohmic contacting.

Both n- and p-MISFET devices show good performance, especially with respect to drain current driving capability. By increasing the laser energy, the sheet resistance of source/drain regions is reduced due to higher dopant activation. The source to drain resistance was also extracted from the measurements and an increase was observed when the channel length increases. Ultrashallow source/drain junctions were activated and the TEM images show junctions of 10-12 nm deep for 1000 mJ/cm^2 laser energy. The overlapping of the laser spot was studied for 66% and 1% overlap. The drain current is higher for 66% overlap, again due to higher dopant activation but at a cost of some extra heating.

In **Chapter 5**, the demonstration of high performance n-DotFET devices, successfully fabricated by adapting the n-MISFET process to the dot structure, is presented. Transistors with a minimum gate-length dimension of 50 nm using TiN/Al(1%Si) metal-gates were processed. A SiGe dot grown by MBE was used as stressor material. The best energies for excimer laser annealing of these structures were found to be between 850 mJ/cm^2 and 900 mJ/cm^2. E-beam lithography was used to define nanoscale gate dimensions in the central region of the dot and a 1-µm-wide gate finger is defined to contact this narrow gate. Thus a part of the current between the source and drain flows around the dot structure rather than through the silicon channel over the SiGe dot. Despite this effect, it is still possible to determine the influence of the strain on the drain current. The electrical characteristics show a drain current enhancement between 2% and 35%. The simulations show enhancements due to the strained Si layer of 20% - 22%. The small dimensions of the channel result in a large spread of measured characteristics, but nevertheless, the impact of the strain Si layer can be indentified. On a test sample the SiGe dot was removed using ammonium hydroxide, hydrogen peroxide and deionized water, which shows the possibility of fabricating a D-DotFET device in the future. Simulations of D-DotFETs and DotFETs fabricated on SOI substrates were done and the results show a reduction of self-heating for D-DotFET devices.

Conclusions to the thesis are given in **Chapter 6**. The two most important results of this thesis are the demonstration of the applicability of (1) SiGe dots as stressor material and (2) full-melt high-power laser annealing as a technique for lowering the source/drain series resistance in a manner self-aligned to the gate.

Samenvatting

door Cleber Biasotto

Het in dit proefschrift gepresenteerde werk is uitgevoerd in het kader van het Europese Sith Framework Program (FP6) project “Verwijderbare-dot veld-effect transistoren voor hoge snelheid in Si geïntegreerde schakelingen”, aangeduid als het D-DotFET project. Het project had als doel het realiseren van strain-versterkte mobiliteit in CMOS transistors door de overdracht van strain van een zelf-geassembleerde germanium dot naar het kanaal van een transistor boven de dot. Het oorspronkelijke idee was om de Ge dot te verwijderen onder het kanaal na het aanbrengen van de gate, zodat de gate-stack dan ook dient om de kanaalbrug te stabiliseren en voor het behoud van de strain geïntroduceerd in het kanaal door de Ge dot. Het voordeel van het gebruik van een SiGe dot als bron voor strain is de schaalbaarheid naar gate-dimensies tot wel afmetingen zo klein als 10 nm, wat niet voor de hand ligt bij momenteel gebruikte methoden. Bovendien biedt de D-DotFET structuur voordelen voor het elektrostatische en elektrothermische gedrag van MOS transistoren. Bijvoorbeeld, SOI devices met volledig uitgeput kanaal zijn een oplossing voor korte kanaaleffecten, maar het isolerende oxide onder het device introduceert een thermisch beheersingsprobleem. Dit probleem is opgelost in Silicium-op-Niets (SON) devices omdat het isolerende gebied alleen onder de gate te vinden is, met de source en drain gebieden nog steeds verbonden met het thermisch geleidende bulk silicium. De D-DotFET lijkt op de SON transistor, maar met het voordeel van strain-verbeterde transistor versterking en snelheid. Op deze manier combineert de D-DotFET vier potentiele verbeteringen: verbeterde prestaties door strain schaalbaarheid naar toekomstige ~10 nm CMOS generaties, onderdrukking van korte kanaal effecten en goede warmte geleiding.

Binnen het DotFET project, is onderzoek gedaan in verschillende gebieden om te verzekeren dat strikte eisen aan uniformiteit, reproduceerbaarheid en betrouwbaarheid zouden aan voldaan kunnen worden als het D-DotFET concept overgebracht zou worden naar geavanceerd CMOS. Het groeien van silicium germanium (SiGe) dots met de noodzakelijk hoge Ge inhoud is het eerst ontwikkeld, en uniformiteit en reproduceerbaarheid werden naar een hoog niveau van perfectie gebracht. De strain van zowel kale als overgroeide dots is zeer uitgebreid experimenteel en theoretisch geanalyseerd. Vervolgens werd de strain die overgebracht kon worden naar het kanaal van een MOSFET geëvalueerd in termen van mobiliteitsverbetering middels device simulaties. Tenslotte werd de daadwerkelijke integratie van dots gedemonstreerd in een n-MOSFET onderzoeksproces van lage complexiteit, welk speciaal is aangepast voor deze toepassing, wat het onderwerp is van dit proefschrift.

De Dimes cleanrooms zijn niet toegerust om een state-of-the-art CMOS proces op te zetten om het D-DotFET concept te onderzoeken. Echter, de beschikbare expertise en apparatuur waren geschikt voor het realiseren van meer geavanceerd processtappen, zodat excimer laser gloeien kon worden geïmplementeerd om het conventioneel rapid thermal anneal te vervangen en de metalen gate een vervanging kon zijn voor de standaard polysilicium gate. Bovendien werd het schrijven van de ~100 nm gate patronen uitgevoerd met e-beam lithografie door de projectpartner Forschungszentrum Jülich. Om zoveel mogelijke nanoschaal lithografie stappen te voorkomen werd een geometrie met grote source-drain contactgebieden ontworpen, zodat slechts één processtap, namelijk de ~100 nm gate, uitgevoerd hoefde te worden met e-beam.

Omdat het doel in eerste instantie het verifiëren van de strain-verbeterde versterking geïnduceerd door de dot was, werd bovendien besloten om de transistor fabricage significant te versimpelen door de dot te behouden tijdens de gehele process. Een “DotFET” in plaats van een “D-DotFET” werd daarom gefabriceerd. Dit betekent dat alleen lage temperatuur fabricage stappen uitgevoerd konden worden na de fabricage van de dot, om het mixen van Si en Ge en de bijbehoorend minderen van de strain te voorkomen. Dit werd gerealiseerd in een speciale n-MOSFET proces waarin de temperatuur onder de 400 °C werd gehouden na epitaxie door gebruik van lage temperatuur gate diëlektrica en een metalen gate self-aligned op de gedoteerde en laser gegloeide source/drain regio’s.

De gebruikte SiGe dots voor de DotFET fabricage werden gegroeid in een zelf assemblerende Stranski-Krastanow modus die het mogelijk maakt enkel-kristallijne dots van SiGe te groeien in drie dimensies op vooraf gedefinieerde seedholes. Onder passende condities is deze groei defectvrij en kan eenvoudig worden geschaald naar kleinere dimensies. De 3D groei van de SiGe staat een hogere concentratie van Ge toe in de dot voordat kristal dislocaties vormen dan de groei van 2D SiGe lagen met eenzelfde dikte. Des te kleiner de SiGe dot is, des te hoger is het Ge gehalte dat kan worden behouden zonder defect formatie, zodoende kan een grotere strain worden uitgeoefend op elke Si laag gegroeid over de dot. Voor de transistoren beschreven in dit proefschrift werden de dots gegroeid met MBE op een regelmatig seedhole patroon van submicron periodiciteit geëtst in het Si. De groei is in detail onderzocht om de optimale groei condities en seedhole patronen te bepalen om een dot-grootte en strain niveau geschikt zouden zijn voor het construeren van een MOSFET over het centrum van de dot, zodat de biaxiale strain gebruikt kon worden voor kanaal mobiliteitsverbetering.

Voor een uniforme en reproduceerbare SiGe dot groei werden uitstekende resultaten behaald met een locatie-gecontroleerde groei methode waarbij grote, regelmatige, reeksen van seedholes zijn aangebracht op een anders vlak Si-substraat. In dit werk werden zowel i-line als e-beam lithografie gebruikt om zulke gaten aan te brengen in (100) Si plakken. In het geval van e-beam lithografie is een erg goede controle over de seedhole posities en afmetingen behaald en de resulterende dots zijn extreem regelmatig. De huidige DotFET fabricage vereist een dot afmeting welk een gate met een lengte van ~100 nm kan accommoderen. Voor dit doel waren de meest geschikte seedhole reeksen degene met een periodiciteit van 800 nm die een maximale dot diameter van 230 nm leverde. EBL werd gebruikt voor deze configuratie in het device fabricage, terwijl analyse van de dot eigenschappen ook is uitgevoerd op monsters bewerkt met optische lithografie. Het groeien van de dots op het seedhole patroon begint met de depositie van een Si buffer laag welk het oppervlak gladder maakt. De dots werden dan gegroeid op 720 °C uit een puur Ge-bron.

In hoofdstuk 2 wordt een simpel, lage temperatuur fabricage methode voor het behalen van hoogwaardige zeer ondiepe n+p junctiediodes gedemonstreerd. Een 5 keV As+ implantatie is geaktiveren door middel van excimer laser annealen (ELA). Recent is veel onderzoek gedaan met ELA technieken omdat de extreem korte anneal tijden de potentieel transient

enhanced diffusie effecten elimineren, hoge niveaus van dotering activatie behalen en abrupte juncties geven. Vergeleken met conventioneel snel thermisch anneal procedures biedt ELA het voordeel van een goede controle over junctie diepte. Een reductie van de verticale implantatie omvang kan dienen als een directe methode om ook de junctie diepte te verminderen. Het laser verwerkingsonderzoek in het verleden uitgevoerd bij Dimes is gedaan uit noodzaak voor het verkrijgen van goede kwaliteit diodes in integratie situaties waarbij alleen een lage temperatuur is toegestaan zoals het silicium-op-glas proces, in plaats van gefocust op de fabricage van source en drain gebieden voor CMOS.

Met respect tot het bulk lateraal-uniforme deel van de diode weg van de rand is het belangrijk dat het Si oppervlak dat gedoteerd moet worden glad is en vrij van natuurlijk oxide voor de implantatie. De dotering moet zo ondiep zijn dat het smelt gebied het gehele gedoteerde gebied omvat, maar diep genoeg om te voorkomen dat laser geïnduceerde Si-oppervlakte effecten het onderliggende metallische junctie gebied beïnvloeden. Gekantelde 5 keV implantaties kan de uiteindelijke junctiediepte reduceren tot minder dan 20 nm. Met respect tot de rand van de diode is de sleutel tot het behalen van diodes van goede kwaliteit de beëindiging van de metallurgische junctie op een oxide interface van goede kwaliteit. In de gepresenteerde experimenten wordt dit behaald door het gebruik van een dunne laag thermisch oxide om het Si te bedekken onder een dikkere lage temperatuur isolatielaag. Het oxide op de grens is een 30 nm dunne laag thermisch oxide, welk nog steeds dik genoeg is om excessieve verbreding van het contact gat te voorkomen gedurende de dip-etch die wordt gebruikt om het natuurlijk oxide te verwijderen voor metallisatie. Na het groeien van de isolatie oxide worden alle proces stappen uitgevoerd op temperaturen onder de 400 °C. Een reflecterend masker van Al wordt toegepast om het laser smelten van het silicium te lokaliseren tot het gewenste diode gebied en om de rand te beschermen. De gekantelde implantatie vergroot ook de overlap van de oxide isolatie met de diode rand wat het proces meer robuust maakt en rand lekkage vermindert. De volledigheid van de laser smelt aan de rand hang af van de thermische conductiviteit van de omgeving. Minder smelten aan de rand ten opzichte van de bulk is geïdentificeerd door middel van TEM analyse van de diodes. Dit kan een bron zijn van extra rand lekkage waarmee rekening moet worden gehouden. De beste resultaten zijn hier behaald met een implantatie van 2x1015 cm-2 bij een helling van 30°. Voor diodes met een oppervlak van 80 μm2 geeft dit een idealiteitsfactor van 1.04 en een speerstromslekkage bij 2 V van ~ 10-5 A/cm2.

De lage temperatuur fabricage benodigd voor de DotFET transistors stelt hoge eisen aan de fabricage temperatuur van het gate diëlektricum welk normaal een hoge kwaliteit thermisch oxide is, gegroeid bij temperaturen boven de 850 °C. In hoofdstuk 3 wordt een onderzoek gepresenteerd naar een aantal diëlektrische lagen gemaakt bij temperaturen lager dan 400 °C die potentieel gebruikt kunnen worden als DotFET gate materiaal. MIS capaciteiten werden gefabriceerd met verschillende gate-diëlektricum lagen en elektrisch gekarakteriseerd. Een vergelijking is gemaakt met capaciteiten met een SiO2 grenslaag thermisch gegroeid op $\leqslant$ 700 ° C. Er werd gekozen om atomic-layer-deposited (ALD) Al2O3 te onderzoeken omdat deze techniek een uitstekende uniformiteit, conformiteit, accurate controle over de dikte van de film levert, en het mogelijk is om hoge kwaliteit lagen op lage temperatuur te deponeren. Cycli van TMA en water werden gebruikt om Al2O3 lagen te deponeren bij een temperatuur van 300 °C. Ook SiOxNy lagen met een lage N-concentratie zijn gegroeid met een inductief gekoppeld plasma bij een temperatuur van 250 °C.

De resultaten van capaciteit-spanning en stroom-spanning metingen demonstreren dat ALD Al2O3 en ICP SiOxNy een diëlektrische constante van respectievelijk 8 en 4 vertonen. Met ICP SiOxNy werden capaciteiten gefabriceerd met een laag interface state dichtheid en een lage effectieve ladingsdichtheid, respectievelijk <1011 cm-2eV-1 en < 1011 cm-3eV-1, als ook een lage lekstroomdichtheid (< 10-7 A/cm2). Voor pure Al2O3 lagen was de interface kwaliteit naar Si slecht en om dit te verbeteren werd een hoge-kwaliteit grenslaag gegroeid of gedeponeerd tussen het aluminiumoxide en Si substraat. Dankzij de eenvoudige en snelle fabricage en goede kwaliteit van het ICP SiOxNy diëlektricum bij lage temperatuur werd deze uiteindelijk gekozen voor de fabricage van de MOSFETs en DotFETs.
De verwerkingstechnieken voor de fabricage van n+p diodes met zeer ondiepe juncties annealed met de excimer laser techniek en capaciteiten gebruik makend van Al2O3 en SiOxNy gate diëlektricums werden gecombineerd om een simpel MISFET device zoals gepresenteerd in Hoofdstuk 4 te creëren. De fabricage van n- en p-MISFET devices is gedemonstreerd voor verwerkingstemperaturen onder de 400 °C. Vier belangrijke processtappen moeten worden uitgevoerd om goede elektrische device prestaties te verkrijgen: (i) voor een goede groei kwaliteit van ICP SiOxNy moet het Si oppervlak direct voor de groei worden schoongemaakt, dit is behaald met een HF dip-ets; (ii) een onderdompeling in BHF wordt

uitgevoerd direct voor de source/drain dotering om het natuurlijk oxide op het Si oppervlak te verwijderen en een uniforme dotering van de lage energie ionen te behalen; (iii) een RIE proces met laag RF vermogen wordt gebruikt voor het etsen van het oxide voor de source/drain contact openingen, om de schade aan het gedoteerde silicium oppervlak te verminderen; (iv) een HF dip-ets wordt gebruikt om het natuurlijk oxide te verwijderen voor de source/drain metallisatie om een laag ohms contact te verzekeren.

Zowel n- en p-MISFET devices vertonen goede karakteristikken, in het bijzonder met betrekking tot de drain stroom driving capabiliteit. Door middel van het verhogen van de laser energie wordt de sheet weerstand van de source/drain gebieden gereduceerd door de hogere doteringsactivatie. De source naar drain weerstand was ook geëxtraheerd uit de metingen en een toename was geobserveerd wanneer de kanaallengte toenam. Zeer ondiepe source/drain juncties zijn geactiveerd en de TEM beelden toonden juncties van 10-12 nm diep voor een laser energie van 1000 mJ/cm2. Het overlappen van de laser spot is bestudeerd voor 66% en 1% overlap. De drain stroom is hoger voor 66% overlap, opnieuw door de hogere doteringsactivatie, maar ten koste van wat extra verhitting.

In hoofdstuk 5 worden n-DotFET devices met goede prestaties, succesvol gefabriceerd door het aanpassen van het n-MISFET proces aan de dot structuur, gepresenteerd. Transistoren met een minimale gate-lengte van 50 nm gebruik makend van TiN/Al(1%Si) gates zijn gemaakt. Een SiGe dot gegroeid door middel van MBE is gebruikt als stress inducerend materiaal. De beste energie voor excimer laser annealen van deze structuren bleek tussen 850 mJ/cm2 en 900 mJ/cm2 te zijn. E-beam lithografie was gebruikt om de nanoschaal gate dimensies te definiëren in het centrale gebied van de dot, en een 1 μm brede gate vinger werd gedefinieerd om deze nauwe gate te contacteren. Op deze manier vloeit een deel van de stroom tussen source en drain om de dot structuur hen in plaats van door het silicium kanaal over de SiGe dot. Ondanks dit effect is het nog steeds mogelijk om de invloed van de strain op de drain stroom te bepalen. De elektrisch karakterisatie toont een drain stroom verbetering tussen de 2% en 35%. De simulaties tonen een verbetering door de strained Si laag van 20-22%. De kleine dimensies van het kanaal resulteren in een grote spreiding van de gemeten karakteristieken, maar toch kan de invloed van de strained Si worden geïdentificeerd. Bij een testmonster was de SiGe dot verwijderd door middel van ammoniumhydroxide, waterstofperoxide en gedeïoniseerd water,

waaruit blijkt dat het mogelijk is om een D-DotFET device in de toekomst te fabriceren. Simulaties van D-DotFETs en DotFETs gefabriceerd op SOI substraten zijn uitgevoerd en de resultaten tonen een reductie van de zelf-verhitting voor D-DotFET devices.

De conclusies van dit proefschrift worden gegeven in hoofdstuk 6. De twee belangrijkste resultaten van dit proefschrift zijn de demonstratie van de toepasbaarheid van (1) SiGe dots als stress inducerend materiaal en (2) volledige-smelt hoog-vermogen laser-annealing is een techniek om de source/drain serie weerstand te verlagen bij een self-aligned gate.

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