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A -87.2 dB THD+N 89.1 dB DR Fully-Integrated Shunt-Resistor-Based In-Line Current Sensor with up to 2 MHz 14.4 V PWM Rejection

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Abstract

This paper presents a cost-effective, fully-integrated shunt-resistor-based in-line current sensor offering high linearity and effective PWM rejection for audio applications. To mitigate the on-chip shunt resistor self-heating, which could severely compromise the linearity of the current sensor, a thermal compensation method is proposed and improves the THD+N by up to 23.6 dB. A floating G_m stage is proposed to reject high-frequency high-voltage (HV) PWM signals at the audio amplifier switching node. Implemented in a 180 nm BCD process, the prototype achieves a peak THD+N of -87.2 dB and a DR of 89.1 dB with up to 2 MHz, 14.4 V PWM rejection, while supporting a ± 6 A current range.

Introduction

High-linearity shunt-resistor-based current sensing is often employed in audio systems to compensate for the non-ideality of the loudspeaker [1-3]. In this application, high-linearity current sensing (THD+N < -68 dB) is desired [3]. However, due to the self-heating of the shunt resistor, an $HD3 = 20\lg(TCR \cdot T_{AC})$ is generated [4], where TCR is the shunt resistor's temperature coefficient and T_{AC} is the shunt resistor's temperature varying with the AC audio signals. To mitigate this, off-chip resistors [5] or resistors [6] fabricated in special processes with low TCR can be employed, but this increases the system cost and bulk. Active thermal compensation [1, 5, 7-8] can be employed, but they either only target DC current or exhibit poor linearity for AC current (THD+N > -58 dB). Besides the resistor self-heating, PWM rejection is crucial for in-line current sensors. This is because Class-D amplifiers (CDA) with PWM modulation are widely employed in audio applications due to their high efficiency, and since the in-line current sensor is placed directly at the amplifier output in series with the load, it is in full exposure to the high dv/dt PWM common-mode (CM) signal (Fig. 1). The PWM switching can easily result in glitches during transition, and thus introduce distortion. Despite this challenge, in-line current sensing is preferred since it avoids distortion during signal reconstruction, which is inevitable for ground/supply current sensing [9]. To mitigate the PWM-induced glitches, a hold phase is introduced in [10] during switching, but this phase degrades linearity and further limits the PWM frequency to only 125 kHz. In this work, a thermal compensation scheme is proposed to mitigate shunt resistor self-heating, while a floating G_m (FG_m) stage is proposed to provide effective HV PWM rejection up to 2 MHz.

Proposed Fully-Integrated In-line Current Sensor

The sensor block diagram is shown in Fig. 1. The shunt resistor R_S converts the load current into a voltage, which is then converted into a current by FG_m. A current buffer directs the output current of FG_m from the floating voltage domain to a 5 V transimpedance amplifier (TIA) to produce V_{OUT} . The transimpedance of the current sensor is thus $R_S \cdot FG_m \cdot R_{FB}$ in the audio band. FG_m (Fig. 2) consists of a resistor-degenerated common-gate stage ($R_{I1,2}$; $M_{I,2}$) [11] and is powered by a bootstrap voltage V_{BST} , which is readily available in most high-power CDAs [2, 8, 12]. A floating regulator keeps the voltage stress of FG_m stage within 5 V. $M_{D1,2}$ function as a current buffer and isolate FG_m from the TIA. The parasitic capacitance between R_S/FG_m and the substrate is further isolated by a Deep-Nwell (DNW) connected to V_{BST} . Despite these isolations, parasitic capacitors $C_{PARA1,2}$ can still produce significant glitches during switching and introduce distortion. To mitigate these, a 2nd-order low pass filter is employed in the biasing circuit, and the size of $M_{D1,2}$ is minimized to reduce C_{PARA2} .

The R_S is implemented by a 27 m Ω diffusion resistor, consisting of 7680 $\times$ parallel-connected unit resistors with an L/W of 5 μ m/2 μ m. Compared to the metal resistor, it has a 3 $\times$ lower TC. Although p-type poly resistors can achieve low TC, this only holds with a long length in this process, which leads

to a large chip area. With the same chip area, p-poly resistors exhibit a similar TC but suffer from 3 $\times$ worse saturation effect [13], increasing distortion. Diffusion resistor, however, suffers from depletion effect. To mitigate this, R_S is split and connected with complementary body connections [14] (Fig. 2).

High-Linearity Thermal Compensation

First, to compensate for the TC of R_S (TC_{RS}), $R_{I1,2}$ (5 k Ω) in Fig. 2 are implemented using the same unit resistors as R_S , but connected in series with similar body connections. Since $M_{I,2}$ are biased in weak inversion, the TC of FG_m is largely determined by that of $R_{I1,2}$. By matching the temperatures of R_S (T_{RS}) and that of $R_{I1,2}$ (T_{RI}), the temperature sensitivity of $R_S \cdot FG_m$ can be minimized. However, self-heating of R_S introduces a temperature gradient across itself (Fig. 3 top) with e.g. a 4 A/1 kHz input current (iin). Considering the huge dimension difference (43 $\times$) between R_S and $R_{I1,2}$, the location of $R_{I1,2}$ is crucial [5]. At 50 locations inside R_S , the temperature errors (absolute values) in amplitude and phase relative to the averaged T_{RS} are shown. At a single location, e.g. location 3, where relatively small errors are achieved for a 1 kHz signal, the errors shift as signal frequency varies due to the thermal filtering effect [15] (Fig. 3 bottom right). Thus, placing $R_{I1,2}$ at a single location would never yield good thermal compensation. Trimming cannot help either since it is often done in particular conditions. To address this, $R_{I1,2}$ is split into multiple sub-units and inserted into R_S with a distance L between the adjacent sub-unit (Fig. 4 left). Fig. 4 top right shows the relationship between L and averaged temperature errors between R_S and $R_{I1,2}$ with a 4 A/1 kHz current. Finally, L is set to 60 μ m as a trade-off between layout complexity and temperature errors (<5% in amplitude; <2 $^\circ$ in phase), and yields a simulated 26 dB HD3 improvement over frequencies (Fig. 4 bottom right).

Apart from the thermal matching of R_S and $R_{I1,2}$, $M_{I,2}$ still has a residual effect. Since the TC of $M_{I,2}$ is higher than that of R_S , for their thermal matching, $M_{I,2}$ are strategically placed ~ 325 μ m away from R_S to experience a smaller R_S temperature fluctuation (Fig. 5). Doing so can keep the HD3 degradation within 1.9 dB due to this effect over PVT and frequency with a 4 A current. Lastly, $R_{FB1,2}$ are placed far away from R_S to minimize its exposure to R_S temperature fluctuation. A serially connected CTAT p-type poly resistor and PTAT diffusion resistor further reduce the overall TC_{RFB} to <60 ppm/ $^\circ$ C over PVT, resulting in a negligible effect on the overall HD3.

Measurement

The proposed current sensor is implemented in a 180 nm BCD process and occupies 2 mm² (Fig. 5). Fig. 6 top shows the measured HD3 is reduced by 20 dB with the proposed method at 2 A/1 kHz input current. The spectrum of V_{OUT} with a -60 dBFS input current is shown in Fig. 6 bottom, demonstrating a DR of 89.1 dB (A-weighted). Fig. 7 presents the measured THD+N with various current frequencies versus amplitude. The proposed method improves THD+N by up to 23.6 dB. At higher frequencies, THD+N decreases due to the thermal filtering effect [15], which essentially reduces the temperature fluctuations across R_S . Fig. 8 shows the measured THD+N of 4 samples versus input current amplitude at 1 kHz and versus frequency over the entire audio band (20 Hz-20 kHz) at 4 A amplitude. The THD+N varies by less than ± 2 dB. Fig. 9 shows the transient response of the current sensor with a 2 MHz 14.4 V PWM signal at V_{OUT} . Fig. 10 shows the measured THD+N varies less than 2 dB with/without PWM voltage when the current sensor is driven by a Class-D/Class-AB amplifier respectively, demonstrating strong PWM rejection.

As Table I shows, this work achieves 17.1 dB/28.2 dB better peak THD+N (-87.2 dB) at 1 / 6 kHz compared to other works either using on-chip or low-TC off-chip resistor [1-2, 6, 8, 16]. It also demonstrates PWM rejection capability up to 2 MHz (16 $\times$ higher than [10]) and achieves at least 9.1 dB higher DR.

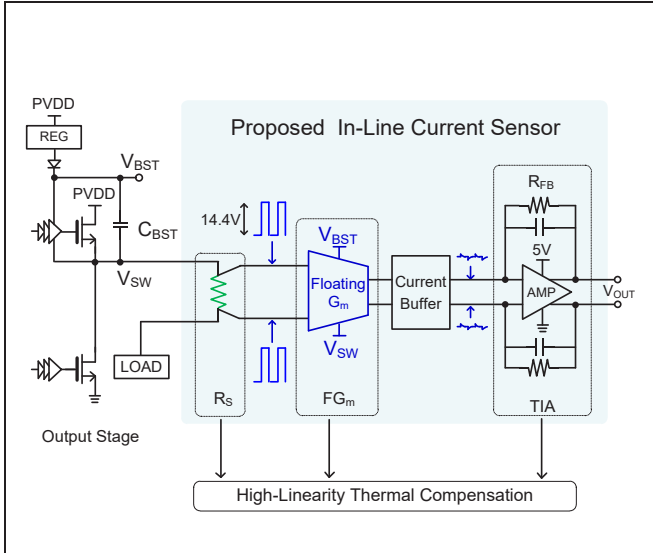


Fig. 1. The simplified block diagram of the proposed current sensor

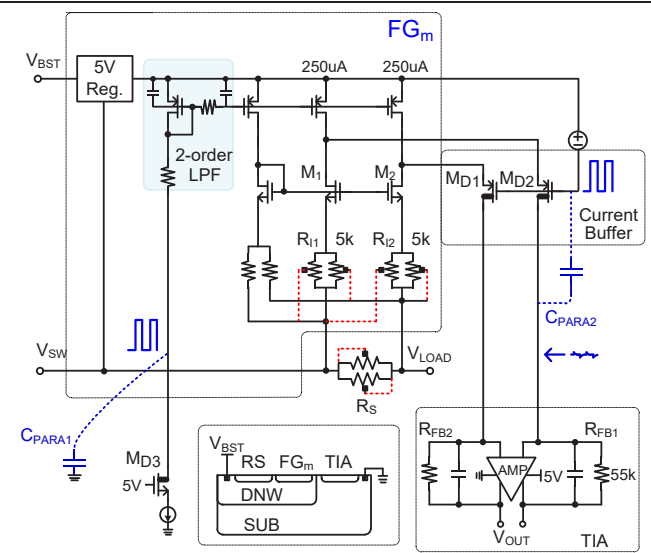


Fig. 2. Schematic of the proposed FG_m-based current sensor and the cross-section of the substrate

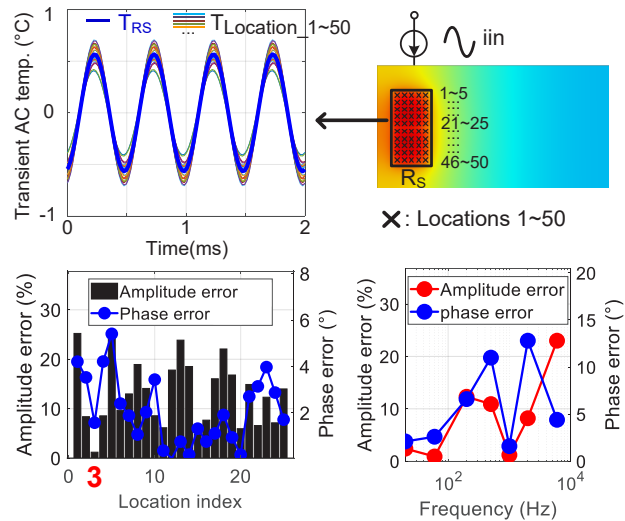


Fig. 3. Temperature distribution across R_s with a current of 4A, 1kHz (top), and the absolute value of temperature errors relative to the averaged T_{RS} at different locations (bottom left), and the frequency dependency of the errors at location 3 (bottom right)

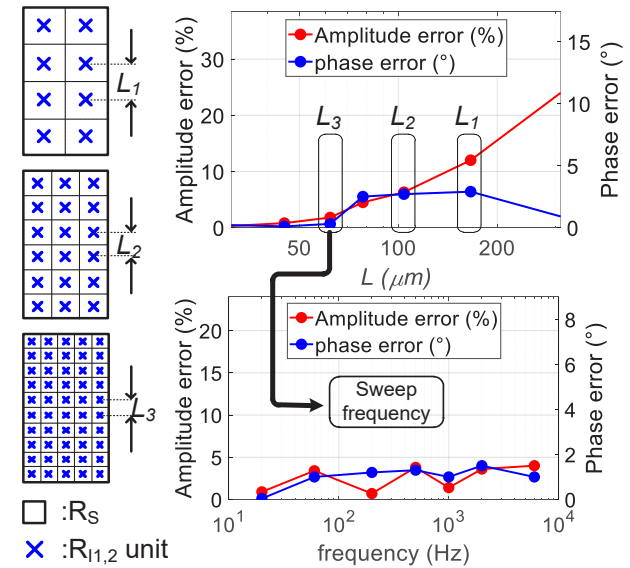


Fig. 4. Thermal compensation between R_s and $R_{11,2}$ with different patterns (left) and error analysis (right)

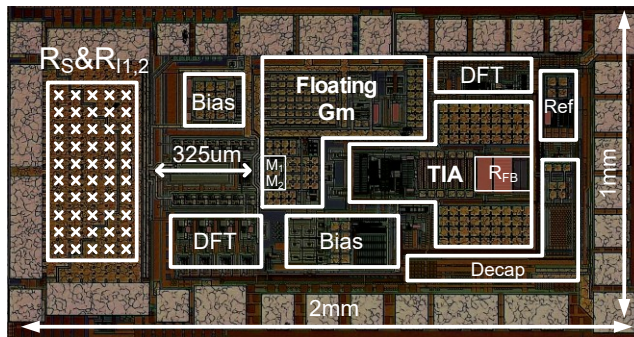


Fig. 5. Die photo

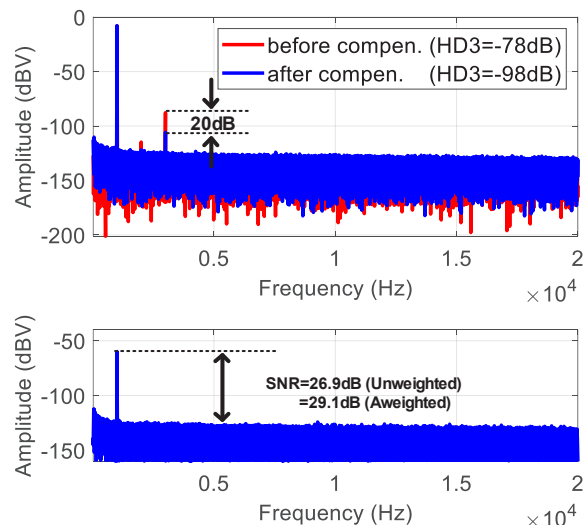


Fig. 6. Measured spectrum of V_{OUT} before and after the proposed thermal compensation with 2 A, 1 kHz input current (top) and spectrum of V_{OUT} with -60 dBFS, 1 kHz input current (bottom)

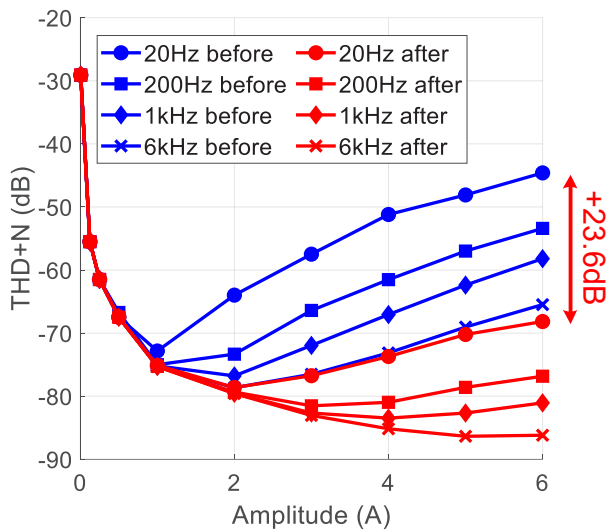


Fig. 7. Measured THD+N versus current amplitudes before and after the proposed thermal compensation at different current frequencies.

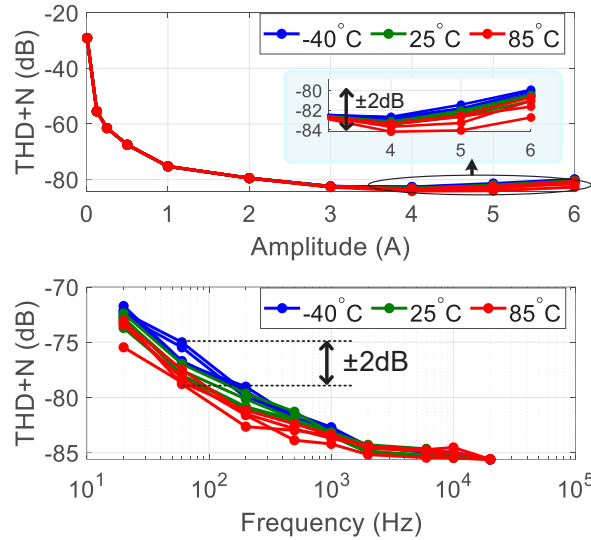


Fig. 8. Measured THD+N versus current amplitudes (top, frequency fixed at 1 kHz) and frequencies (bottom, current amplitude fixed at 4 A) at 3 ambient temperatures with 4 samples.

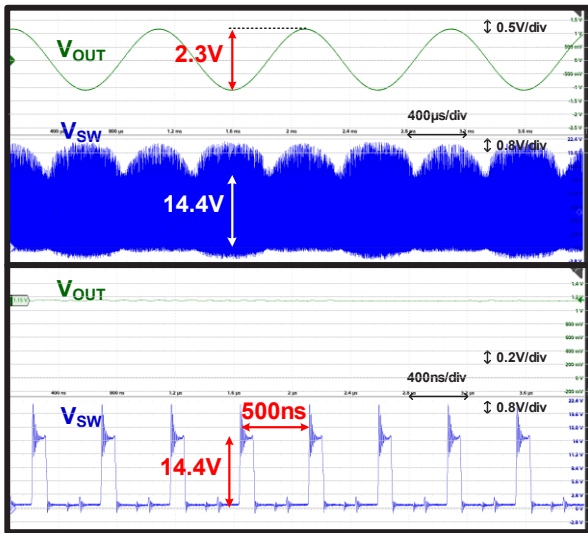


Fig. 9. Measured transient wave of V_{OUT} and V_{SW} (top) and zoomed-in wave (bottom) with an input current of 4 A, 1 kHz, and a PWM frequency of 2 MHz

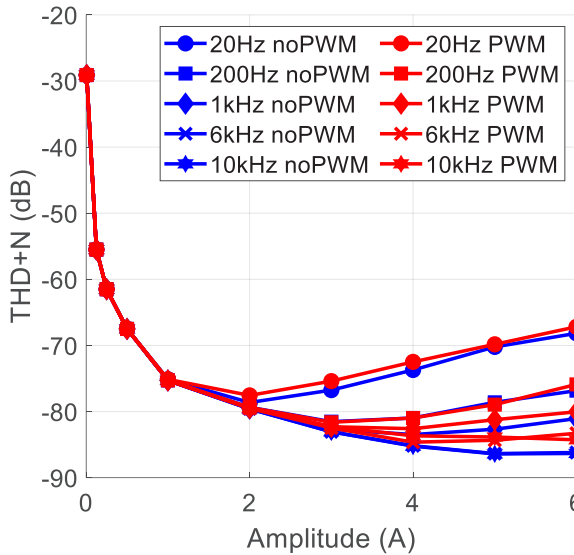


Fig. 10. Measured THD+N versus current amplitude with/without PWM CM voltage at different current frequencies.

Table. I. Performance summary and comparison.

	[1]	[2]	[6]	[8]	[10]	[16]	This work
R_s	4× 30mΩ	/	2mΩ	2× 80mΩ	/	/	27mΩ
Fully Integrated?	Yes	Yes	/	Yes	No	Yes	Yes
TC of R_s (ppm/°C)	3900 ¹	/	15	3900 ¹	/	/	1250
In-line Sensing?	No	/	Yes	No	Yes	/	Yes
Peak THD+N @1kHz	-58dB ²	-60dB ²	-66.4dB ^{2,3}	-45dB ^{2,4}	/	-63dB ²	-83.5dB (wo PWM) -83.1dB (wi PWM)
Peak THD+N @6kHz	/	/	-55.4dB ^{2,3}	/	/	-59dB ²	-87.2dB (wo PWM) -85.2dB (wi PWM)
DR ⁵	77.5dB (I)	66dB (un)	74.5dB ² (un)	80dB (A)	/	73dB (un)	89.1dB(A) 86.9dB(un)
Supply Current	0.8mA ²	/	1.8mA	2mA	2.5mA	/	1.2mA
PWM Rejection	/	/	/	/	125kHz	/	2MHz
Current Range	±0.5A ²	±3.8A	±15A ⁶	±0.8A ²	/	±3A	±6A

¹Noted metal resistor ²Estimated from data/graph ³Measured at 90% full scale ⁴Simulated at full scale ⁵Aweighted (A) or unweighted (un) ⁶DC current

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