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DOI
10.1109/NSSMIC.2017.8533036

Publication date
2018

Document Version
Final published version

Published in
2017 IEEE Nuclear Science Symposium and Medical Imaging Conference, (NSS/MIC)

Towards a fully digital state-of-the-art analog SiPM

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***Abstract* – We present a design that implements digitization of an analog SiPM's fast output on chip to pave the way to higher granularity in the digital conversion of photon detection. The design comprises a comparator bank, time-to-digital converters (TDCs), and electronics for interfacing with the external world. The TDC is a multipath, gated ring oscillator with a counter and phase detector, implemented in 0.35µm CMOS technology. Simulation results indicate a DNL of ±0.55LSB and an INL of ±1LSB, a large, adjustable range, and a typical resolution of 65ps (LSB).**

***Index Terms* - Silicon photomultiplier, time-to-digital converter, TDC, DNL, INL.**

I. General Concept

THE output of an analog SiPM is generally coupled either with a current amplifier or a passive load and a voltage amplifier through a PAD and PCB interconnect. The output path has generally a large capacitance that impacts the timing performance of the SiPM. To counter these effects, several front-end circuits have been proposed based on a number of techniques described in [1]. We recently proposed an approach, based on the use of digital SiPMs that are partitioned in segments (ideally a single SPAD microcell) each with a time-to-digital converter (TDC), denominated multi-channel digital SiPM (MD-SiPM) [2]. The approach enables the use of multiple timestamps to reconstruct a timemark for the gamma event that is robust and always guaranteed to reach the Fishburn-Seifert lowerbound [3],[4].

In this paper, we propose to use an analog SiPM [5], possibly partitioned in mini-SiPMs of hundreds of SPAD microcells, and to perform a capacitive decoupling, comparison, and conversion on chip (Fig. 1). One or more timestamps are generated and transmitted off-chip sequentially. The original analog 'fast output' is preserved for backward compatibility, while the gamma-photon timemark can be extracted from the timestamps, externally [6]. Furthermore, one TDC will be internally connected to this analog output to allow time-over-threshold measurements to be done. This will result in a fully integrated system capable of energy and time estimation. One or more reference voltages are provided externally or generated by on-chip D/A converters with voltages as low as 10mV. In addition to simplicity, the obvious benefit of this concept is the reduction of the capacitive load on the fast output, thus improving the overall timing performance.

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II. TDC Architecture

Keeping the architecture as simple and robust as possible was one of the primary objectives when designing the TDC. The architecture consists of a ring oscillator, a counter, and a phase detector (Fig. 2). The phase detector can discriminate as little as 65ps (LSB), while the overall range of the TDC is 65ns, for a total resolution of 10 bits.

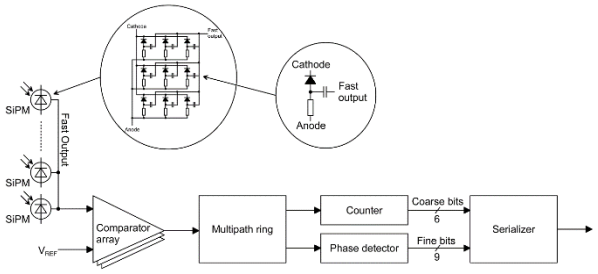

Fig. 1. Concept of one or more analog mini-SiPMs coupled with TDCs via comparators through the fast output, so as to extract timestamps that are combined, off-chip, onto a single timemark for a gamma event time-of-arrival estimation.

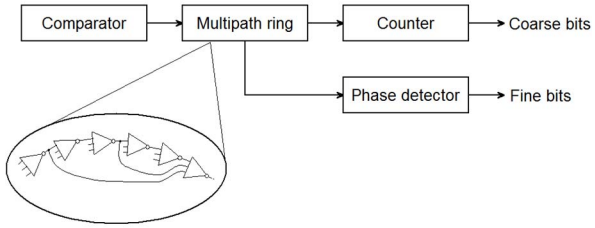

Fig. 2. TDC architecture; the digital output is stored in a memory that is then read out sequentially.

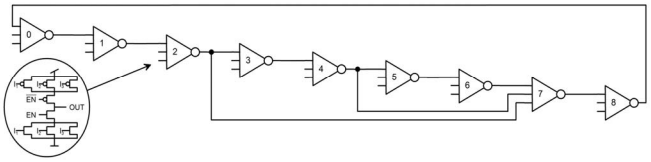

Fig. 3. Gated multipath ring oscillator structure for the TDC. In the inset the tri-state delay element is shown.

A gated multipath ring oscillator was chosen (Fig. 3), whereas each stage is composed of three parallel inverters of different sizes connected through a pair of transistors that allow tri-state operation. The multipath structure allows the ring to have a higher oscillation frequency, hence a better LSB. The three separate inputs are connected to different points along the ring. This type of connection means that the

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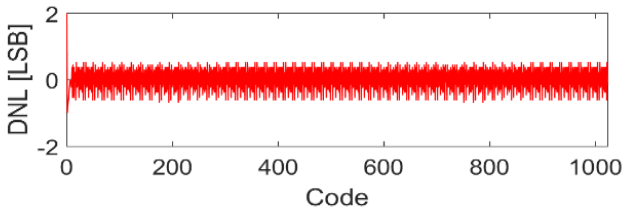
output of a stage will start transitioning ahead of time and therefore, the total delay will be reduced. The use of three input connections for each tri-state inverter limits the minimum number of stages in the ring to nine, which in turn translates into 18 phase states being used for the fine bits. The 15 bits are transferred through a serializer that operates at 40MHz. A redundancy therefore appears when computing the result with (1).

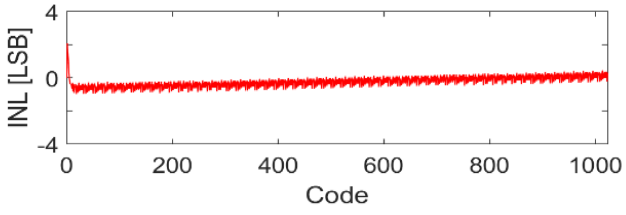
$$N_{result} = 18N_{coarse} + N_{fine}. \quad (1)$$

III. TDC POST-LAYOUT RESULTS

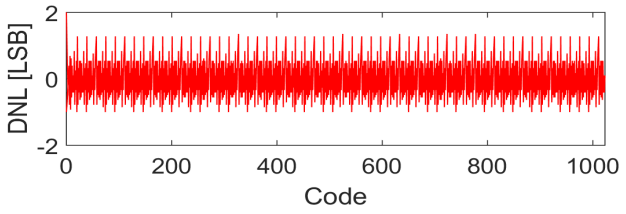
Through careful sizing of the transistors in the stage as well as adjusting separately the power supply of the ring oscillator, the transfer characteristics can be adjusted. Fig. 4 shows the DNL (differential non-linearity) and INL (integral non-linearity) simulation results with nominal power supply voltage, in other words, no compensation.

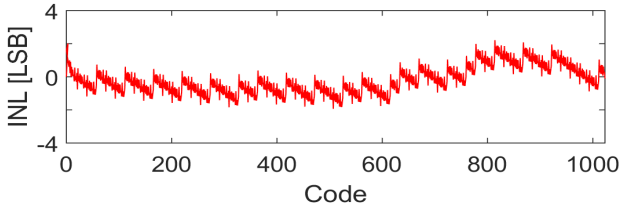
In the worst case scenario, the DNL is +1.28/-1LSB while the INL is +2.12/-1.66LSB.



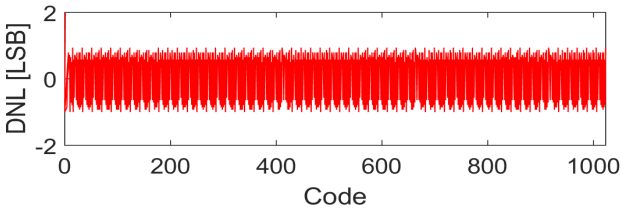


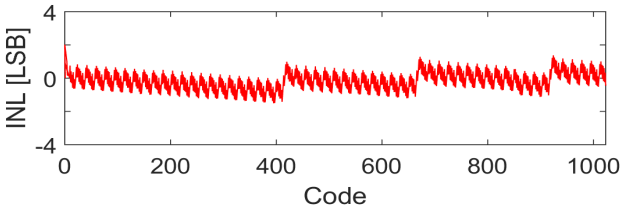
a) typical-typical (TT).



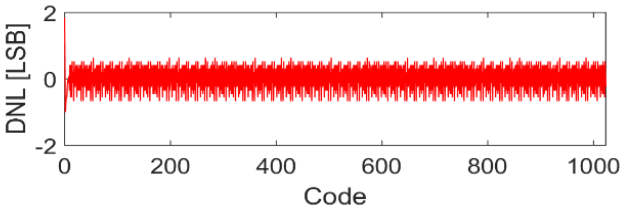


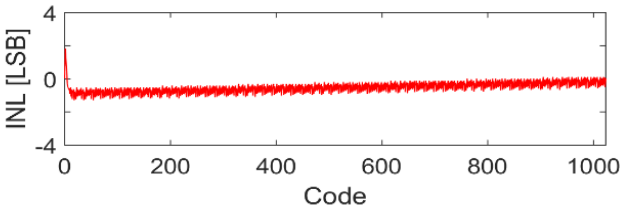
b) fast-slow (FS).



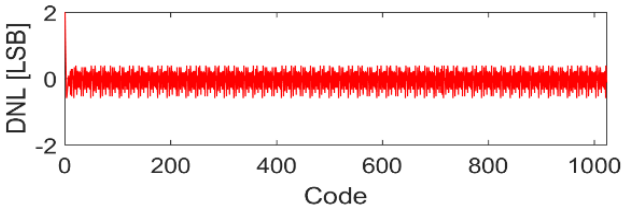


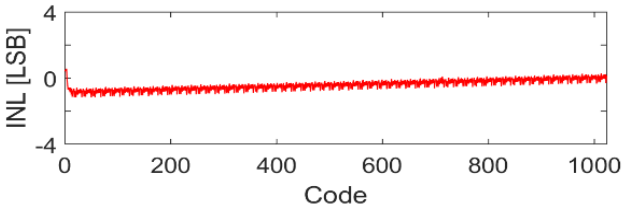
c) slow-fast (SF).





d) fast-fast (FF).





e) slow-slow (SS).

Fig. 4. Simulation of the differential non-linearity and integral non-linearity in all design corners.

Table I summarizes the LSB results in all five corners, which have been obtained after post-layout simulations. As expected, the worst case corresponds to the SS corner. However, in TT the LSB is smaller than 70ps.

TABLE I. LSB IN ALL FIVE CORNERS

Corner	LSB [ps]
TT	65
FS	67.95
SF	69.39
FF	45.71
SS	91.79

Further simulations have been performed in order to determine the LSB shift with temperature and power supply. The results are presented in Fig. 5 and Fig. 6. The LSB is estimated by sweeping the input pulse width with a 5ps step. For this reason, a fitting curve is plotted as well in order to emphasize the trend of the results. The results indicate an increase of the LSB with temperature, the reason being that the effect of parasitic components becomes dominant and decrease the oscillation frequency of the ring at high temperatures. An increase of the power supply of the ring determines a decrease of the LSB until one point, when the LSB becomes constant. By comparing the two figures (Fig. 5 and Fig. 6), it can be concluded that a compensation for the LSB in a military range of temperatures is not only possible but advisable.

IV. DECOUPLING AND POWER SUPPLY NOISE SUPPRESSION

The design of the power distribution network is a critical step and requires careful modeling in order to ensure good functionality of the entire system. Changes in the power supply can highly degrade the circuit operation, thus the power distribution network was modeled and PMOS decoupling capacitors were placed on chip so that the power supply and ground noise can be minimized. 3000 decoupling capacitors were placed between each power supply of the circuit and ground (see Fig. 7).

Preliminary simulation results indicate a decrease of around 20dB at 800MHz (close to the oscillation frequency) in PSD (power spectral density) at room temperature (see Fig. 8 and Fig. 9).

Based on the aforementioned results, the noise voltage RMS values as well as the average power consumption of the TDC are presented in Table II.

TABLE II. TDC POWER SUPPLY NOISE

	Vdd		Vdd RING	
	P_n	V_n (rms)	P_n	V_n (rms)
No decap	8.5µW	104.6mV	4.7µW	107.2mV
With decap	5.6 µW	62.3mV	1.75µW	52mV

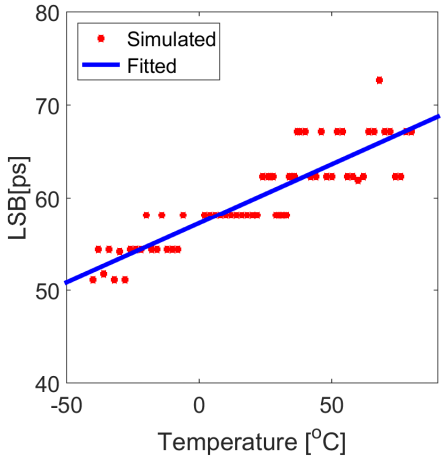


Fig. 5. LSB vs. temperature.

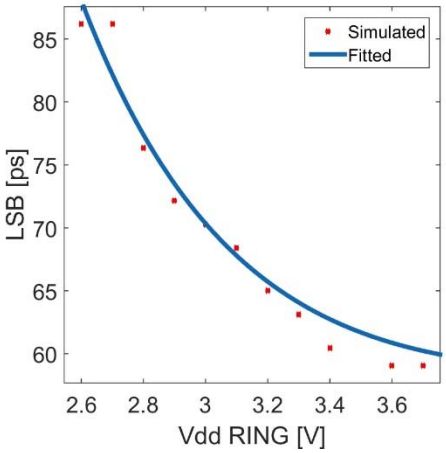


Fig. 6. LSB vs. ring power supply.

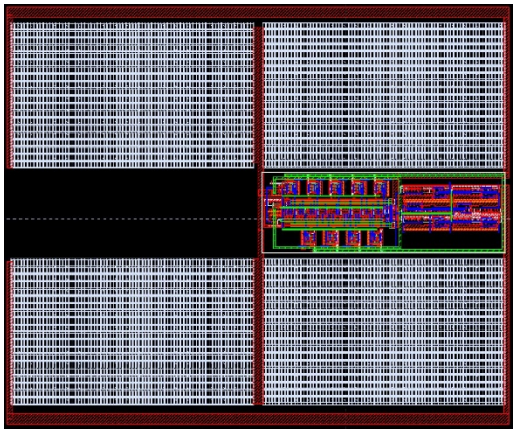


Fig. 7. TDC with decoupling capacitors.

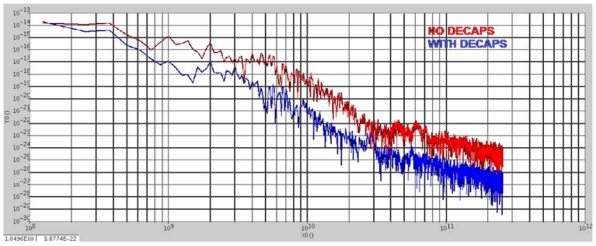


Fig. 8. PSD of the power supply network in the whole system.

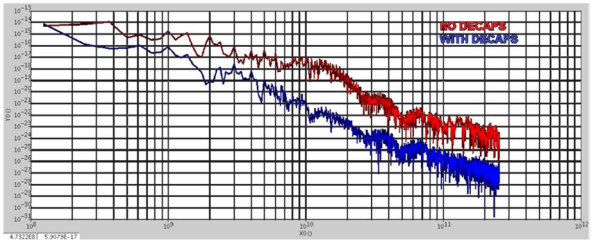


Fig. 9. PSD of the power supply network in the ring oscillator.

V. Preliminary Results

The proposed digital analog SiPM was implemented in a 0.35µm CMOS technology, called *Osprey,* where the DCR is better than 50kcps/mm^2. The PDE at 420nm is 51% for an excess bias voltage of 6V with an overall fill factor of 75% and an area of 3x3mm^2, while the pitch of the SPAD microcells is 35µm [5]. The comparator/TDC bank occupies a small area in the chip, representing a negligible loss of fill factor. The entire system performance is summarized in Table III.

Fig. 10 shows measurements of the CRT achieved in [7] by using fast vs. standard outputs and multiple timestamps. In our design, we expect a further improvement with respect to these measurements, thanks to a drastic reduction of capacitive load from 1000pF (standard output) to 50pF (fast output), down to 1pF (estimated internal parasitics). Note that the current improvement of pulse width is 53x with a 20x reduction of capacitive load.

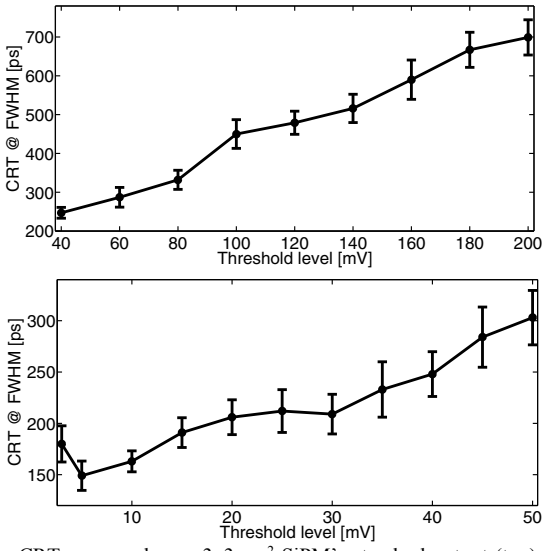


Fig. 10. CRT measured on a 3x3mm^2 SiPM's standard output (top) and the fast output (bottom) to a TDC [6].

VI. Conclusions

This study aimed at drastically improving timing performance in analog SiPMs by reducing the capacitive load through segmentation and integrating mechanisms for multiple timestamp measurement. An added benefit of integration is simplicity, compactness, and, potentially, power consumption, thus paving the way to scalable, networked SiPMs and multi-channel digital SiPMs. This design represents the first step towards low cost, high performance digital SiPMs.

TABLE III. System Performance Summary

	Performance	**Value**
SiPM	PDE @420nm	51 %
	FF	75 %
	DCR	50 kcps/mm^2
TDC	LSB	65ps
	Jitter	< 18 ps (1σ est.)
	DNL/INL (TT)	±0.55 / ±1 LSB
	Resolution	10 bits
	Supply	3.3 V
	Input	Single-ended
	Output	125 Mbps
	Clock	40 MHz
	Power (peak / standby)	<9 mW/<1 mW
System	Area	3x3.3mm^2
	Backward-compatible	Yes

VII. Future Investigations

Future research will focus on increasing time stamping granularity by creating more/faster TDCs which will be integrated on-chip. 3D ICs will enable the combination of SiPM optimized technologies with advanced CMOS low-power processes.

Acknowledgments

The research has been supported, in part, by the Swiss National Science Foundation. SensL, which co-funded this research, also provided technology support.

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