Electronically Controlled Etch-Mask for Silicon Bulk Micromachining

T. A. Kwa and R. F. Wolffenbuttel

Abstract— **Wafers that are to be submitted to anisotropic etching in aqueous KOH are conventionally passivated with a silicon dioxide or nitride layer in which backside windows are etched to define the microstructures. A different method to mask the backside of a silicon wafer for this purpose is presented. The method makes use of the phenomenon that silicon is not etched in KOH when biased above the passivation potential. The mask is defined by applying a set of bias voltages to the front of the wafer instead of patterning a deposited passivation layer at the backside, for which an accurate double-sided alignment is required. The feasibility of the method was demonstrated with the fabrication of membranes and suspended masses of various sizes. [95]**

I. Introduction

WHEN bulk micromachining silicon, the backside of the wafer is conventionally protected against the etchant with an oxide or nitride layer in which windows are opened where the micromechanical structures are to emerge. An accurate alignment of the etch windows is essential to obtain the structures at the proper position with respect to the photolithographic patterns at the front. Several techniques have been developed to align the backside etch-mask with the structures at the front, including commercially available double-sided mask aligners based on an infrared or double microscope, the use of special jigs and alignment masks [1], and the use of pre-etched alignment marks [2].

In this paper, a masking method is investigated that eliminates the need for a backside etch-mask while maintaining compatibility with bipolar IC processing. Consequently, a backside alignment procedure and the extra processing steps required to realize the mask are superfluous. Some insight into the etching behavior was acquired by simulation and some experiments were performed to verify the feasibility of the method.

II. Principle

The principle of the electronically controlled etch-mask is based on the bias-dependent etch-rate of silicon in aqueous KOH [3]. Both p- and n-type silicon are etched in KOH, but the etch-rate decreases when the silicon is biased above a certain voltage with respect to a counter electrode in the solution.

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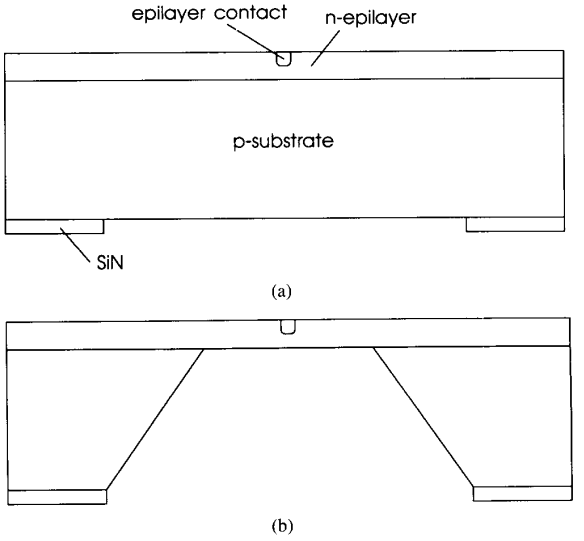


Fig. 1. Electrochemically controlled fabrication of a membrane, using a conventional, deposited nitride etch-mask (a) before etching and (b) after etching has stopped on the epilayer.

For even higher voltages, the silicon becomes passivated and eventually the etching stops. The passivation effect has been accounted for as the result of an anodic oxide growth [3]. For p-type silicon, the potential against a saturated calomel electrode (SCE) at which the etch-rate suddenly drops is called the passivation potential (PP) and is equal to -1.04 V in a KOH solution at 60°C [4]. However, when using the simple two-electrode configuration, a voltage of at least 0.5 V ($=V_{\text{pass}}$) has to be applied to stop the etching [5].

The passivation mechanism has already been used for the Electrochemically Controlled Etch-Stop (ECES)-based fabrication of membranes [5]. The n-type epilayer on top of a p-type wafer shown in Fig. 1(a) is kept at a voltage higher than V_{pass}. The backside of the wafer is passivated with a conventional etch-mask, using, e.g., silicon nitride as the masking material. As the p- and n-type silicon are more or less isolated, the substrate can stay at or close to the open-circuit potential (OCP), and the p-type substrate in the exposed window is etched. Etching takes place along the slowly etching $\{111\}$ crystal planes, if the mask is aligned properly along the (110) plane. As the etchant approaches the epilayer-substrate junction, the floating potential of the silicon being etched drifts

towards the passivation value [6]. Etching terminates when this value is reached, and a wafer-thick deep cavity surrounded by $\{111\}$ planes remains, as shown in Fig. 1(b).

Applying a voltage difference between two line-shaped contacts at the front of a silicon wafer, as shown in Fig. 2(a), results in an electric potential distribution in the wafer (Fig. 2(b)), and a potential gradient as shown in Fig. 2(c) is obtained at the backside. In the area where the potential is anodic of V_{pass}, the silicon is passivated, while in the area cathodic of V_{pass}, the silicon is etched. In this way, it is possible to selectively etch and passivate areas at the backside that are defined from the front [7].

This is the principle on which the Electronically Controlled Etch-Mask (ECEM) is based. Fig. 3(a) shows a (100) p-type wafer with an n-type epitaxial layer. Several deep p-type (DP) diffused contacts enable the substrate to be biased locally at the desired voltage. Shallow n-type contacts are made in the epilayer to enable an etch-stop on the epilayer. During the etching, the substrate is biased with a set of voltages via the DP contacts, defining the backside etch-mask. The outer DP contacts (passivating contacts) are biased with a voltage above V_{pass} and the center DP contact (etching contact) with a voltage below V_{pass}. This should have the effect that only the central surface area is etched, while the outer parts of the silicon substrate are passivated. The sheet resistance in the center part increases as a layer of silicon is etched away and results in a larger potential drop around the center. Therefore, the positions at which the potential is equal to V_{pass} shift towards the etching contact, and an ever smaller etching area remains. The etching stops electrochemically on the epilayer. The resulting etch-profile that can be expected is shown in Fig. 3(b) and is dependent on the distance between the contacts and the potentials applied. The angle between the bevels and the wafer surface, however, never exceeds 54.7°, as this is determined by the intersection of the (100) and the $\{111\}$ plane.

It is important that the dopant (i.e., boron) concentration of the etching contact is high enough to induce an etch-stop. This prevents the KOH from etching through the epilayer when the center contact is reached. Furthermore, the sheet resistance of the deep p-type diffusions must be sufficiently low to obtain a uniform potential distribution at the contacts.

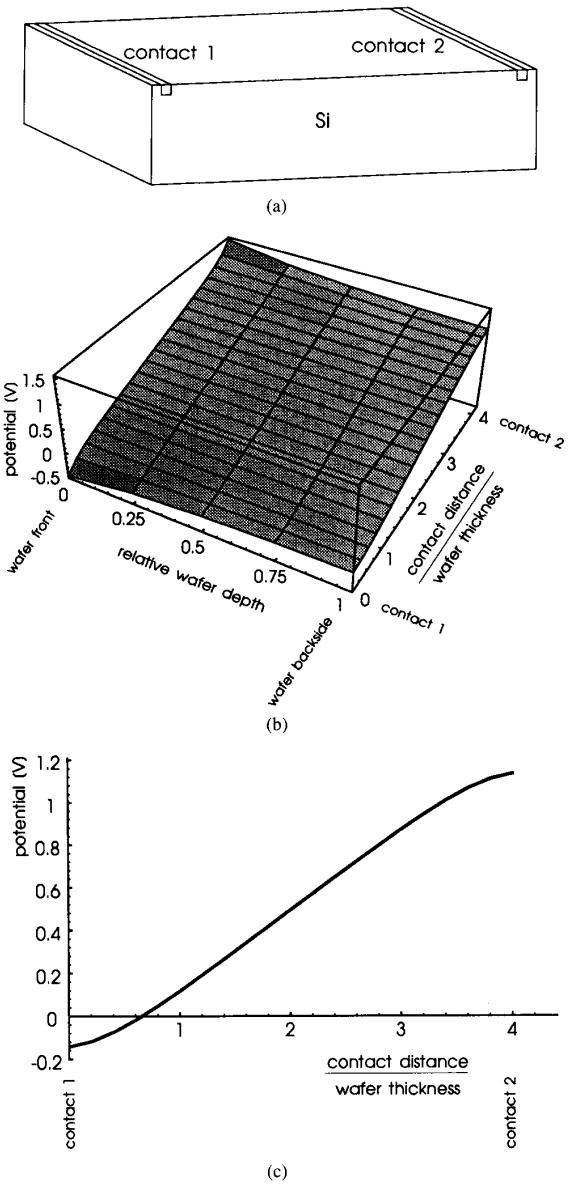


Fig. 2. Part of a silicon wafer with two line-shaped contacts at the front of a silicon wafer, between which a potential difference is applied. (a) Cross-sectional view. (b) Electric potential distribution in the wafer. (c) Potential distribution at the backside of the wafer.

III. Simulations

Biasing the passivating contacts with equal voltages obviously results in a symmetric etch-profile. The etch-profile can be relatively easily determined when setting the bias voltages symmetrically with respect to V_{pass}, i.e., for the passivating contacts $V = V_{\text{pass}} + dV$ and for the etching contact $V = V_{\text{pass}} - dV$, where the voltage difference dV is a positive value.

Three assumptions are made in the simulations of the etch-profile: 1) the resistivity is uniform throughout the wafer, 2) there is an infinitely sharp transition in the etch-rate at V_{pass}, the maximum etch-rate occurring below V_{pass} and dropping to zero above this value, and 3) the location at which the potential is equal to V_{pass} is, from the front to the backside, at the same lateral position. By calculation of the potential distribution, the last assumption was found to be true, in approximation, when the passivating and etching contacts are biased symmetrically with respect to V_{pass} and the distance between the contacts, D, is large compared to the wafer thickness, t. The actual etch-rate around V_{pass} decreases from the maximum etch-rate, determined by the solution temperature and the KOH concentration, to 1/100 of this rate within 50 mV above V_{pass} [8]. Consequently, the exact position of the onset of the bevel and its slope depend in reality on the potential gradient

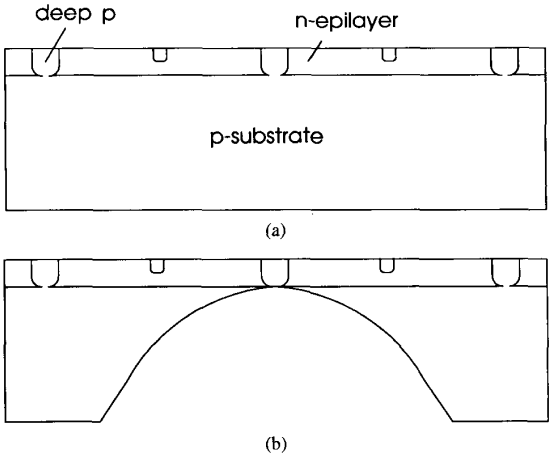


Fig. 3. Configuration of contacts in a silicon wafer showing the principle of the electronically controlled etch-mask. (a) Wafer before etching. (b) Resulting profile after etching.

at the backside. Furthermore, V_{pass} is strongly temperature dependent. For the simulations, a value of 0.5 V is chosen for V_{pass}, as the two-electrode configuration is used. Fig. 2(b) and 2(c) already showed the potential distribution and gradient for $V_{\text{pass}} = 0.5$ V, $dV = 1$ V, and $D/t = 4$. A larger potential gradient at the backside, and thus a steeper bevel slope, can be obtained with a larger voltage difference, a decreased spacing between the contacts or a decreased wafer thickness.

The passivating contacts are chosen located and biased symmetrically around the etching contact, as described above. It suffices, therefore, to simulate the etching for half a wafer cross-section only. Fig. 4 shows the simulated etch-profiles (only the right half) for various distances between the contacts, with $V_{\text{pass}} = 0.5$ V and an arbitrarily chosen value of 1 V for dV. The etch depth and position of the moving boundary between the silicon being etched and the silicon being passivated are given as a percentage of the wafer thickness. It can be seen that the slope of the bevels is steeper when the distance between the passivating and etching contacts is decreased, resulting in a smaller cavity. When D/t is set smaller than $2\sqrt{2}$, the slope angle does not increase any further, as it is limited by the $\{111\}$ planes to 54.7° (Fig. 4(c)). While the area being etched decreases as the etch is deeper, the slope of the interface between the area where etching continues and the sidewall is reduced. Consequently, a large flat membrane surface cannot be obtained with this contact configuration. An alternative contact configuration is, therefore, one where the area to be etched is enclosed by etching contacts. This results in the configuration shown in Fig. 5(a), with the expected etch-profile shown in Fig. 5(b).

IV. Experimental Results

A. Experimental Setup

For a first investigation into the feasibility of the method, the electronic masking experiments described in this paper were

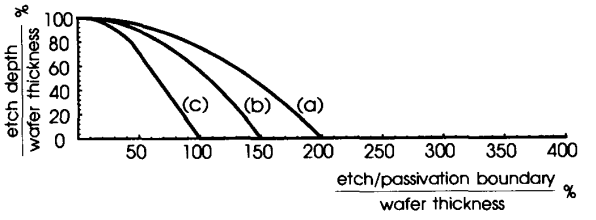


Fig. 4. Simulated etch-profiles (only the right half) for various distances between the etching and passivating contacts ($V_{\text{pass}} = 0.5$ V, $dV = 1$ V): (a) $D/t = 4$, (b) $D/t = 3$, (c) $D/t = 2$.

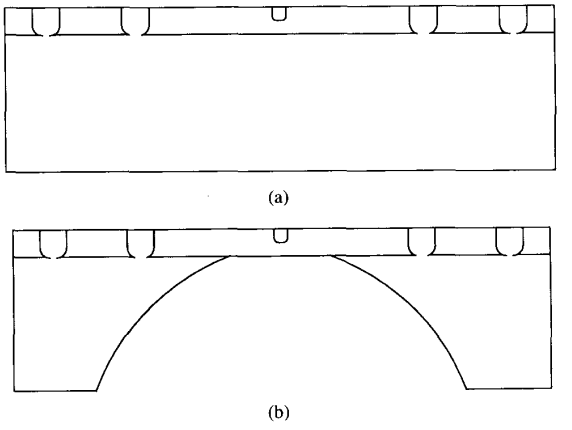


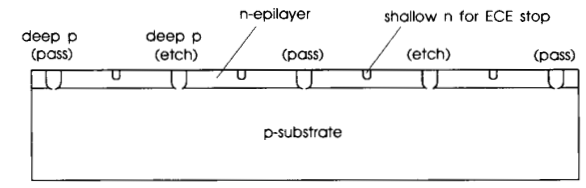
Fig. 5. Double-pair contact configuration. (a) Wafer before etching and (b) resulting profile after etching.

performed in a setup with a platinum counter electrode only. When successful, this technique could be developed further, expanding the setup with a reference electrode. A stainless steel/plexiglass wafer holder was designed to apply the various potentials to the front, leaving only the backside accessible to the etchant. Etching took place in a 33 wt.% KOH solution at 85°C in a double-walled glass vessel.

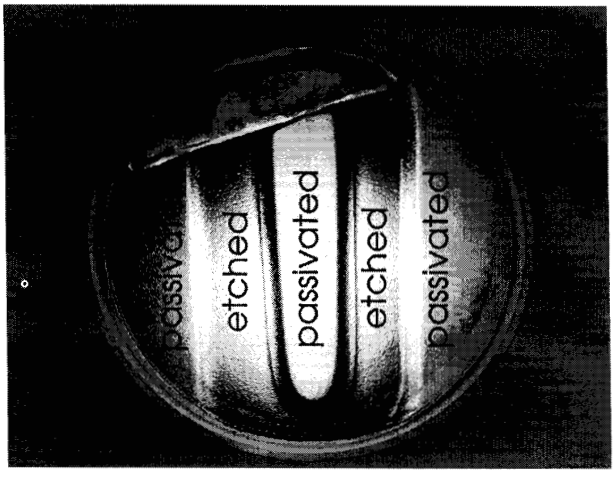
B. Initial Experiments

The etch-stopping voltage V_{pass} was verified first. A 4″, 525-μm-thick, 3.5-Ωcm, (100) single-sided polished p-type wafer, with a boron implantation and metallization to create a low-ohmic contact, was etched using the two-electrode configuration. The etch-rate decreased when a positive voltage was applied and the etching current increased with increasing voltage. However, when the voltage exceeded about 0.5 V, the current dropped suddenly and the etching stopped.

In the subsequent experiments a 4-μm-thick n-type epilayer was grown on the p-type wafers. A pattern of deep p-type diffusions form the passivating and etching contact lanes (Fig. 6(a)). Each lane is 64 mm long and the distance between a passivating and an etching lane is 7 mm, thus, $D \gg t$. Hence, we expect to obtain an etch-profile similar to the profiles shown in Fig. 4. The wafers were immersed in the solution and when biasing the passivating lanes well above and the etching lanes well below V_{pass} (1.9 V and -0.3 V, respectively, and



(a)



(b)

Fig. 6. Wafer with a pattern of deep p-type diffusions for the passivating and etching contacts. (a) Definition of the electronic etch-mask. (b) Photograph after etching. The upper part of the wafer was held above the solution and thus was not etched.

1.2 V for the epilayer), areas of etched and passivated silicon could be distinguished. (Initially, the passivating and etching contacts were set to $V_{\text{pass}} + dV$ and $V_{\text{pass}} - dV$, respectively, with $dV = 1$ V, but due to a large potential drop along the passivating contact lanes, these voltages had to be adjusted.) The area being etched diminished during the etching, which is in accordance with the simulations.

Two parallel moats should have resulted after the etching. However, the potential distribution was non-uniform along the biasing lanes, due to their relatively high resistance (8 $\Omega/\square$). The potential dropped below V_{pass} at a distance from the contact holes, and the silicon was etched. The etch-rate of the areas biased at a voltage far below V_{pass} was about 1.4 μm/min, which is in accordance with literature for the solution concentration and temperature used [9]. Hence, we can conclude that, at the etching contacts, the silicon is etched at the maximum rate. This experiment confirms the feasibility of a backside etch-mask, which is electronically controlled from the front. When the resistance of the biasing lanes was reduced (50 m$\Omega/\square$) to obtain a more uniform potential distribution, indeed parallel moats were obtained, as is shown in Fig. 6(b). Etching stopped on the epilayer-substrate junction, indicated by the etch-stop current peak.

C. Fabrication of Membranes and Suspended Masses

Membranes and suspended masses of various sizes were designed to investigate whether these could be fabricated using the electronic masking method. Two types of contact configurations were used in order to obtain membranes, one of which consists of one small contact in the center of the membrane to which a voltage cathodic of V_{pass} is applied and surrounded by a DP contact moat to which a voltage anodic of V_{pass} is applied, as shown in Fig. 7(a) (single-moat contact configuration of Fig. 3). The second configuration consists of two moats within each other, as shown in Fig. 7(b) (double-moat contact configuration of Fig. 5). Suspended masses were defined by four moats, as shown in Fig. 7(c).

When the wafer was immersed and biased with the appropriate voltages, structures appeared at the positions defined. Steeper slopes were obtained with an increased potential gradient by increasing the voltage difference. As the wafer became thinner, the structures could be seen more clearly. Alternatively, the potential gradient was increased by thinning the wafer first to about half the initial wafer thickness, thus enlarging the ratio of contact distance to wafer thickness. A peak in the epilayer current occurred when the epilayer was reached.

It was found that membranes are much better defined with the double-moat than with the single-moat contact configuration, as was expected. Therefore, only the results obtained with the double-moat version are given below. A membrane of this type is shown in Fig. 8(a). The photograph was taken from the etched side while illuminated from the front. The aluminium patterning at the front can be seen through the membrane. The design dimensions (Fig. 7(b)) are $m_1 = m_2 = 100\mu$m, $D = 1000$ μm, and $M = 4000$ μm, with an expected membrane size of $M + 2 \cdot m_2 = 4200$ μm. A surface profile plot of the membrane was made with a profilometer (Tencor Instruments Alpha-step 200), showing a membrane size of about 4000 $\times$ 4000 μm^2 (Fig. 8(b)). In accordance with the simulated etch-profiles, the slope angle decreases towards the membrane. An unequal steepness of the slopes was obtained due to a difference in potential drop at the passivating contacts. The maximum angle of the right-hand slope is 23°, whereas of the left-hand slope it is only 13°.

Smaller membranes were also fabricated in the same wafer. A membrane with design dimensions $m_1 = m_2 = 100$ μm, $D = 250$ μm, and $M = 500$ μm is shown in Fig. 9(a), where smooth, rounded corners can be seen. The surface profile plot in Fig. 9(b) shows that the membrane dimensions are about 700 $\times$ 700 μm^2. The slopes are, as expected from the simulations, steeper due to a decreased distance between the passivating and etching contacts and have a maximum angle of about 30°. The center part of the membrane is about 4 μm thick, which is the thickness of the epilayer. The dips at the sides of the membrane are the DP contact moats (100 μm wide) that were etched until stopped by the high boron concentration.

Fabrication of suspended masses proved to be feasible as well with this method. A photograph of a suspended mass with design dimensions $m_1 = m_2 = m_3 = m_4 = 50$ μm, $D_1 = D_3 = 350$ μm, $D_2 = 500$ μm, and $M = 1050$ μm (Fig. 7(c), expected mass size is $M+2\cdot D_3+2\cdot m_4 = 1850\mu$m), is shown in Fig. 10(a), and its surface profile plot is given in Fig. 10(b). The size of the mass is about 2000 $\times$ 2000 μm^2.

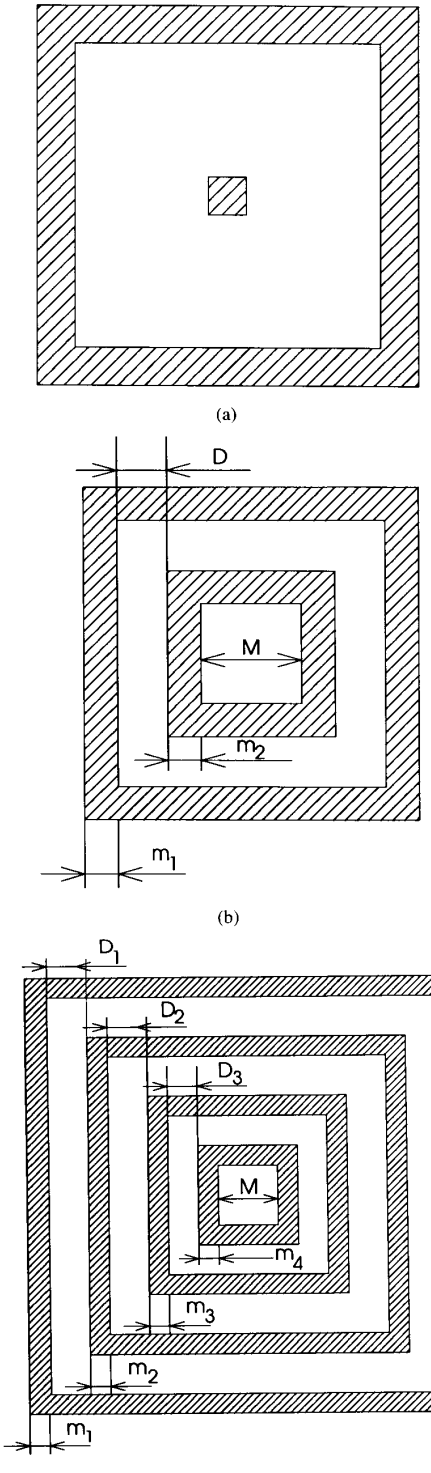


Fig. 7. Contact configurations: (a) single moat for a membrane, (b) double moat for a membrane, and (c) four moats for a mass.

Furthermore, it is only 90 μm high, due to a potential drop at the passivating contact. When suspended masses are fabricated

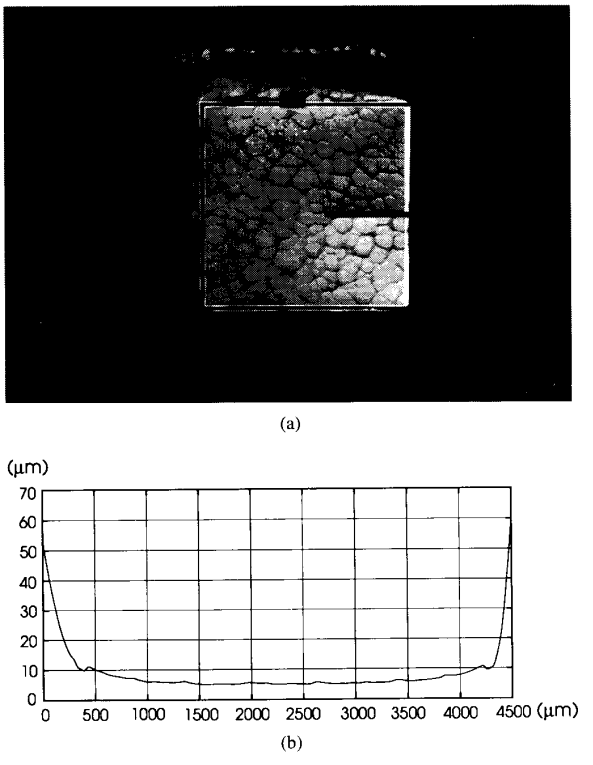


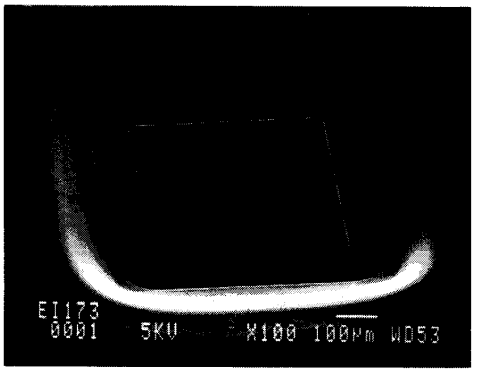
Fig. 8. Membrane fabricated using the electronic masking method, defined with the double-moat contact configuration. (a) Photograph with illumination from the back. (b) Surface profile plot.

using a conventional passivation mask, corner compensating structures are required to prevent premature etching of the corners, resulting in sharply edged, faceted corners [10]. The corners of the suspended mass fabricated with the electronic mask, however, are smooth and convex. This indicates that the local potential is etch-rate determining over the crystal planes.

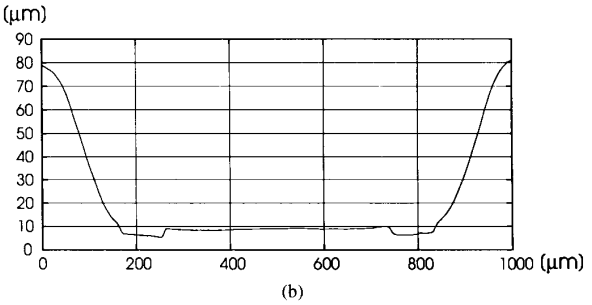
V. Conclusion

In this paper, it has been demonstrated that it is possible to define the position and shape of bulk-micromachined structures by setting the appropriate contact positions and potentials at the wafer front. The electronically controlled etch-mask makes a backside etch-mask and the related process steps unnecessary, thus eliminating the need for a front-to-backside alignment. The process steps required for the definition of the electronic etch-mask can be combined with those needed for the electronic circuitry to be integrated in the same device.

The electronic etch-mask gives the possibility to control, with the location of the contacts and the potentials applied, the size of the membranes and the steepness of the sidewalls. Hence, the angle is no longer defined by the intersection of the (100) and the {111} plane at 54.7°. However, the conventional selectivity along the {111} planes, the electrochemical etch-stop, and the high boron concentration etch-stop still apply.



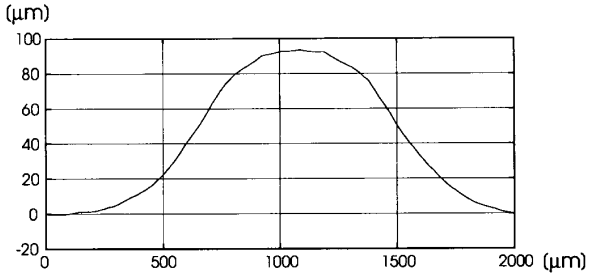
(a)



(b)

Fig. 9. Double-moat contact defined membrane with decreased distance between the passivating and etching contacts. (a) SEM photograph. (b) Surface profile plot.

(a)



(b)

Fig. 10. Suspended mass fabricated using the electronic masking method. (a) Photograph. (b) Surface profile plot.

The method is compatible with bipolar processes for the fabrication of electronic circuits, which is a necessity in the fabrication of smart sensors. In addition, the electronically controlled etch-mask can be used in conjunction with all conventional bulk micromachining techniques to benefit from all the possibilities.

ECE-stopped epilayer membranes of various sizes have been designed and fabricated. A deviation of less than 5% between the expected and actual membrane size was accomplished. The experimental results are in agreement with the expectations from the simulations. The slope angle decreases towards the membrane, and a steeper slope is obtained when the potential gradient is increased by a larger voltage difference, a smaller contact distance, or a decreased wafer thickness. A slope limited by the {111} planes has not been realized yet, but in further work this should be achieved by lowering the resistance of the biasing contacts to obtain a uniform potential distribution and using a reference electrode for a better control of the potentials.

Although good quality membranes and suspended masses have not been obtained so far, the principle of locally controlled passivation and etching has some possibilities for bulk micromachining combined with a conventional backside etch-mask. For example, the etching substrate can be passivated *in-situ* to create membranes or suspended masses with different thicknesses in one wafer. Furthermore, local passivation seems to give the possibility to create well-defined suspended masses without the use of corner compensating structures.

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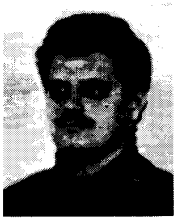

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