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Analytic Design of an EV Charger Controller for Weak Grid Connection

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***Abstract*—This article proposes an analytic approach to design the typical power factor correction (PFC) control of an electric vehicle (EV) charger to ensure small signal stability in weak grid conditions. Compared to the previous works, the proposed method considers the dynamics of all the control loops, i.e., phase-locked loop (PLL), voltage loop (VL), and current loop (CL). The impacts of key influential parameters on stability are analyzed. Furthermore, the upper limits of the PLL and VL bandwidth to ensure small signal stability are derived. Accordingly, the influences of the CL bandwidth, short circuit ratio (SCR), and the filter inductance on the upper limit of the PLL bandwidth and the VL bandwidth are quantified. Consequently, a design procedure that eliminates the need to model the input impedance for tuning the controller to prevent small signal instability is proposed. Simulations and experiments validate the analysis.**

***Index Terms*—Control design, EV charging, impedance-based method, stability analysis, weak grid.**

I. Introduction

AMID the rollout of electric vehicles (EVs), more EV chargers will be connected to the power grid. However, connecting an EV charger to a grid may result in small signal instability [1], [2]. The situation could become worse if the grid strength becomes lower.

The problem is mainly caused by the ac/dc converter of the EV charger [3]. Typically, this ac/dc converter has the power factor correction (PFC) ability that attempts to control the power factor (PF) as one. So, the ac/dc converter is called PFC for simplicity. A widely adopted PFC control for EV chargers is using a phase-locked loop (PLL) for grid synchronization. A voltage loop (VL) is implemented to stabilize the dc-link voltage. Inside the VL, a current loop (CL) is implemented to provide a fast current response. Such a PFC control can lead to small signal instability, especially with a weak grid connection.

The root cause of the small signal instability by adopting such control is well studied via the impedance-based approach [4], [5], [6], [7], [8], [9]. In brief, due to the PFC control, the real part of the charger's input impedance becomes negative at low frequencies, which is thereby called a nonpassive region (NPR). Small signal instability appears if the resonance between the grid impedance and the charger's input impedance has a resonant frequency located inside the NPR [10], [11]. Otherwise, small signal instability happens because the negative resistance will energize the resonance between the grid and the charger leading to unbounded responses.

To address the issue, many studies have been carried out to analyze the influence of controller parameters on the input impedance to give design recommendations. An early work [12] revealed that the bandwidth of the PLL and VL should be kept low to narrow the NPR of the input impedance. It was further recommended to limit the bandwidth of the PLL and VL to one-tenth of the CL bandwidth. However, the recommendation is given regardless of the difference in short circuit ratio (SCR), which can be too conservative or too aggressive since the SCR influences the system stability [13]. The influence of the SCR on stability was considered in [14], and the suggestion on the selection of the PLL bandwidth was given. However, a design procedure to prevent the small signal instability was not given. A more recent work regarding the selection of PLL gain to prevent instability was presented in [15]. Nonetheless, to follow the approach and design the converter control is not intuitive, as the converter impedance needs to be first modeled. Besides, the dynamic of the VL is not relevant in inverter control and thus is not considered, which is not the case for EV chargers. The VL dynamics were considered in [16] and the influence of the VL gain on stability was discussed. However, no design recommendations are given. A more recent work [17] proposed an analytic approach to design the VL bandwidth. However, the relation between the VL bandwidth and the CL bandwidth was overlooked, which easily leads to a either conservative or aggressive design. An analytic approach for the controller gain selection considering the influence of the SCR and all PLL, VL, and CL dynamics can hardly be found in the literature. Without such an analytic design, the controller gains have to be selected by trial and error, which hardly gives an accurate design.

The main contribution of the article is the proposed analytic gain selection method aiming to optimize the PLL bandwidth

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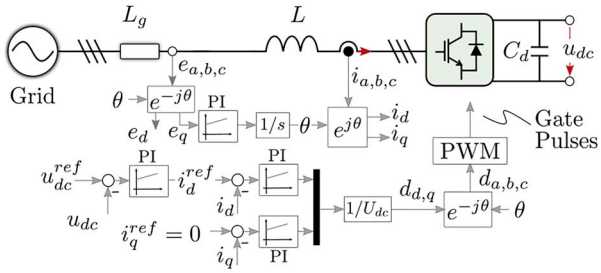

Fig. 1. Typical design of an EV charger's PFC.

and the VL bandwidth while keeping the stability of an EV charger, or a PFC more broadly, with a weak grid connection. To that end, after clarifying the background in Section II, in Section III, the NPR maximum frequencies and the resonant frequencies expressed as the loop bandwidth are derived, which reveals the influences of the grid impedance, the filter inductance, and the bandwidth of the PLL, CL, and VL on stability. Further, the upper limits of the PLL and the VL bandwidths are derived analytically, which is presented in Section IV. Intriguingly, the analytically derived upper limits reveal that, with the same SCR, the bandwidth of the PLL and VL can be higher by increasing the CL bandwidth and the filter inductance. Simulations and experiments for validations are presented in Section V.

II. Fundamentals

A. System Description

Fig. 1 depicts a prevalent design of an EV charger's PFC [18], [19] that dominates the ac stability. An L-filter is assumed for the analysis. However, the proposed approach can be extended to a design with the LC filter. Since the LC-resonant frequency is far above the NPR caused by the control, when the L-filter has the same inductance as the LC filter, the difference between the input impedance of the PFC with the L-filter and the input impedance of the PFC with the LC filter is negligible, which makes the obtained conclusion suitable for both. The grid impedance is assumed purely inductive because it is the worst case for the small signal stability [20].

B. Small Signal Stability Criterion for a Charging System

The small signal stability of a charging system can be evaluated with the impedance-based analysis [1], [2]. For a system with a high PF, e.g., a charger's PFC, the coupling impedance is low and the stability is dominated by the diagonal impedance. Consequently, the stability of the system can be analyzed with the two single-input single-output (SISO) systems on the d-axis and the q-axis [21]. Briefly, for both the d-axis and q-axis systems, the resonant frequency, where the magnitude of the grid impedance equals the converter's input impedance, should be located outside the NPR [12].

Such a stability criterion should be satisfied during the whole charging course despite the change in the charging power. Since the charger's input impedance changes at different charging powers, the worst-case scenario should be analyzed to ensure stability during the entire charging process.

Fig. 2 illustrates the influence of the charging power on the stability margin. As seen, it shows the input impedance of a charger's PFC whose specifications are given as Design 1 in Table II. The charger's d-axis and q-axis input impedance are denoted as $Z_{dd}(s)$ and $Z_{qq}(s)$, respectively. The d-axis and q-axis grid impedance are denoted as $Z_{g,dd}(s)$ and $Z_{g,qq}(s)$, respectively. The acronym $f_{nx,y}$, where x is d or q and y is 0 or 15 or 30, denotes the maximum x-axis NPR frequency, where the real part of the x-axis impedance changes from negative to zero and the phase of the x-axis impedance crosses $-90°$ when the charging power is y in kilowatt. For example, $f_{nd,15}$ denotes the maximum d-axis NPR frequency when the charging power is 15 kW. The acronym $f_{rx,y}$, where x is d or q and y is 0 or 15 or 30, denotes the x-axis resonant frequency, where the magnitude of the x-axis input impedance equals the magnitude of the x-axis grid impedance when the charging power is y in kilowatt. For example, $f_{rd,15}$ denotes the maximum d-axis NPR frequency when the charging power is 15 kW.

Clearly, with a higher charging power, the NPR of the $Z_{dd}(s)$ expands, and the magnitude $|Z_{dd}(s)|$ decreases. Consequently, the resonant frequency f_{rd} decreases from $f_{rd,0}$ to $f_{rd,30}$ whereas the maximum d-axis NPR frequency f_{nd} increases from $f_{nd,0}$ to $f_{nd,30}$. However, with increasing power, the resonant frequency f_{rq} increases from $f_{rq,0}$ to $f_{rq,30}$ whereas the maximum q-axis NPR frequency f_{nq} decreases from $f_{nd,0}$ to $f_{nd,15}$ and completely vanishes when the charging power is 30 kW.

As a result, for the d-axis system, the margin between the f_{rd} and the f_{nd}, which is referred to as the stability margin, is the smallest when the charging power reaches the maximum. On the contrary, the stability margin of the q-axis system is the lowest when the charging power is zero. Therefore, the criterion for ensuring small signal stability during the entire charging process is

$$f_{nd,P_{\max}} < f_{rd,P_{\max}} \quad \text{and} \quad f_{nq,P_0} < f_{rq,P_0} \tag{1}$$

where the subscript P_0 denotes zero charging power and $P_{\max}$ denotes the maximum charging power. The frequencies denoted with f in (1) can be changed to the angular frequencies denoted with ω. For convenience, both of the two kinds of expressions will be used. With an analytical expression of (1), the control parameters can be designed analytically instead of by trial and error, which is the main focus of the article.

III. Stability Criterion Breakdown

A. Full-Order Model

The full-order impedance model of a PFC has already been derived in [9], [13]. Accordingly, the expression of $Z_{dd}(s)$ and $Z_{qq}(s)$ when the PF is unity can be obtained as

$$Z_{dd}(s) = (Ls + R + \frac{3E_g^2}{2C_d U_{dc}^2 s})(1 + G_{oi,dd}(s)) \cdot (1 + G_{ov}(s))\frac{1}{1 - T(s)} \tag{2}$$

$$Z_{qq}(s) = \frac{(Ls + R)(1 + G_{oi,qq}(s))}{1 - G_{cpll}(s)\left(1 - (k_{pi} + \frac{k_{ii}}{s})\frac{I_d}{E_g}\right)} \tag{3}$$

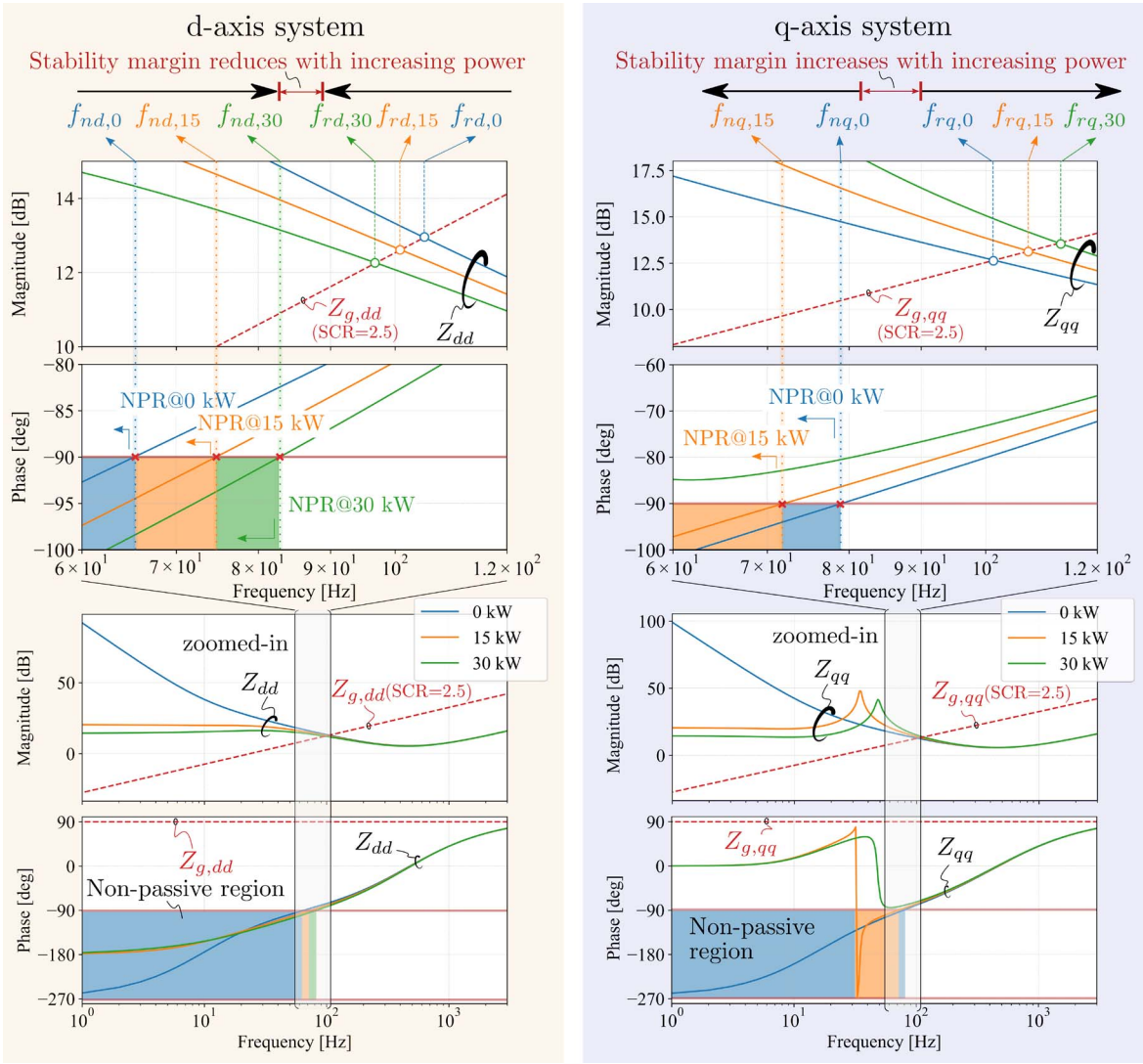

Fig. 2. Change of the maximum NPR frequency, the resonant frequency, and the small signal stability margin of the d-axis system and the q-axis system of a charger's PFC with different charging power levels.

where E_g and U_{dc} denote the grid voltage amplitude and the dc-link voltage, respectively. I_d denotes the d-axis current at a steady state. L and R denote the inductance and the resistance of the power filter, respectively. C_d denotes the output capacitance of the PFC. $G_{oi,dd}(s)$, $G_{oi,qq}(s)$, $G_{ov}(s)$, $T(s)$, and $G_{cpll}(s)$ are functions of s, whose expressions are given by

$$G_{oi,qq}(s) = \frac{k_{pi} + k_{ii}/s}{Ls + R} e^{-sT_{\text{del}}} \tag{4}$$

$$G_{cpll}(s) = \frac{E_g(k_{ppll}s + k_{ipll})}{s^2 + E_g(k_{ppll}s + k_{ipll})} \tag{5}$$

$$G_{oi,dd}(s) = \frac{\left(1 + \frac{3E_g I_d}{2C_d U_{dc}^2 s}\right)(k_{pi} + \frac{k_{ii}}{s})}{Ls + R + \frac{3E_g^2}{2C_d U_{dc}^2 s}} e^{-sT_{\text{del}}} \tag{6}$$

$$T(s) = \frac{3E_g}{2C_d U_{dc} s}\left(k_{pv} + \frac{k_{iv}}{s}\right)\left(k_{pi} + \frac{k_{ii}}{s}\right)\frac{I_d}{E_g} \tag{7}$$

$$G_{ov}(s) = \frac{3E_g}{2C_d U_{dc} s}\left(k_{pv} + \frac{k_{iv}}{s}\right)\frac{G_{oi,dd}(s)}{1 + G_{oi,dd}(s)} \tag{8}$$

where T_{del} is the delay caused by pulse wave modulation and control. k_{pi}, k_{pv}, and k_{ppll} are the proportional gain of the current controller, the voltage controller, and the PLL controller, respectively. k_{ii}, k_{iv}, and k_{ipll} denote the integral gain of the current controller, the voltage controller, and the PLL controller, respectively.

B. Reduced-Order Model

To obtain concise expressions of the $f_{nd,P_{\max}}$, $f_{rd,P_{\max}}$, f_{nq,P_0}, and f_{rq,P_0} in (1), replacing the controller parameters in (2) and (3) with the cut-off frequencies and damping ratios of the control loops is beneficial.

Considering the CL bandwidth is much smaller than the switching frequency, the CL can be simplified as the model shown in Fig. 3.

Accordingly, the CL cut-off frequency ω_{ci} can be approximated by neglecting the low-order term of s in the open-loop

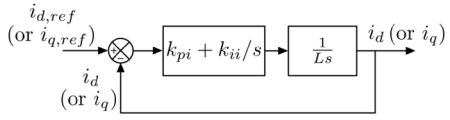

Fig. 3. Block diagram of the simplified CL.

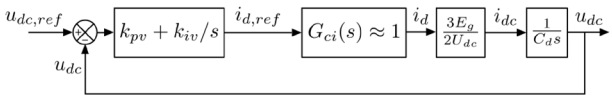

Fig. 4. Block diagram of the simplified VL.

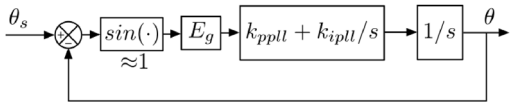

Fig. 5. Block diagram of the PLL.

TF because of their small value about ω_{ci}. Then, ω_{ci} can be obtained as

$$\omega_{ci}=\frac{k_{pi}}{L}. \tag{9}$$

The closed loop of the CL is a second-order system whose damping ratio δ_i can be derived as

$$\delta_i=\sqrt{\frac{k_{pi}^2}{4{\cdot}L{\cdot}k_{ii}}}. \tag{10}$$

The block diagram of the VL is depicted in Fig. 4. The TF of the inner CL is denoted as $G_{ci}(s)$, which can be approximated as a gain of one because the CL bandwidth is much higher than the VL bandwidth.

Similarly, the VL cut-off frequency ω_{cv} can be approximated by neglecting the low-order term of s in the open-loop TF, which is obtained as

$$\omega_{cv}=\frac{3{\cdot}E_g{\cdot}k_{pv}}{2{\cdot}U_{dc}{\cdot}C_d}. \tag{11}$$

Clearly, the closed loop of the VL is also a second-order system whose damping ratio δ_v can be obtained as

$$\delta_v=\sqrt{\frac{3{\cdot}E_g{\cdot}k_{pv}^2}{8{\cdot}U_{dc}{\cdot}C_d{\cdot}k_{iv}}}. \tag{12}$$

As for the PLL, its block diagram is illustrated in Fig. 5, where θ_s is the grid voltage angle. Since the difference between the PLL output angle θ and θ_s is small, $\sin(\theta_s-\theta)$ can be approximated as $\theta_s-\theta$.

The cut-off frequency ω_{cpll} of the PLL can be obtained as

$$\omega_{cpll}=k_{ppll}{\cdot}E_g. \tag{13}$$

The closed loop of the PLL is, again, a second-order system whose damping ratio is derived as

$$\delta_{pll}=\sqrt{\frac{E_g{\cdot}k_{ppll}^2}{4{\cdot}k_{ipll}}}. \tag{14}$$

According to (9)–(14), the controller parameters, e.g., k_{pi} and k_{ii}, can be expressed with the cut-off frequencies and damping ratios of the corresponding control loops, e.g., ω_{ci} and δ_i. Substituting these expressions of the controller parameters into (2) and (3), the full-order impedance model is then expressed with the cut-off frequencies and damping ratios of the CL, VL, and PLL. Then, based on the full-order impedance model and the practical conditions, several assumptions are made to obtain a reduced-order model.

Assumption 1: the delay T_{del}, which equals $1.5/f_{sw}$, where f_{sw} is the switching frequency, can be neglected. This is reasonable because the NPR of the input impedance is at low frequencies. The effect of the control delay inside the NPR is negligible since f_{sw} is far beyond the NPR.

Assumption 2: the resistance of the power filter is negligible. This is reasonable because the influence of the resistance on the input impedance is small [12].

Assumption 3: the cut-off frequency ω_{cv} of the VL, and the cut-off frequency ω_{cpll} of the PLL, are much lower than the cut-off frequency ω_{ci} of the CL. Thus, $\omega_{cv}+\omega_{ci}\approx\omega_{ci}$ and $\omega_{cpll}+\omega_{ci}\approx\omega_{ci}$.

After simplifying the expressions in MAPLE, the reduced-order model of $Z_{dd}(s)$ when the PF is unity is obtained as

$$Z_{dd}(s)=L{\cdot}\frac{s^4+\omega_{ci}{\cdot}s^3+a_2{\cdot}\omega_{ci}{\cdot}s^2+a_1{\cdot}\omega_{ci}{\cdot}s+a_0}{s^3-I_d{\cdot}b_2{\cdot}[\omega_{ci}{\cdot}s^2+b_1{\cdot}\omega_{ci}{\cdot}s+a_0/\omega_{cv}]} \tag{15}$$

where the a_2, a_1, a_0, b_2, and b_1 are given by

$$\begin{aligned}
b_2&=\frac{L{\cdot}\omega_{cv}}{E_g},\quad a_0=\frac{\omega_{ci}^2}{4{\cdot}\delta_i^2}{\cdot}\frac{\omega_{cv}^2}{4{\cdot}\delta_v^2}\\
b_1&=\frac{\omega_{ci}}{4{\cdot}\delta_i^2}+\frac{\omega_{cv}}{4{\cdot}\delta_v^2},\quad a_1=b_1{\cdot}\omega_{cv}+\frac{\omega_{ci}}{4{\cdot}\delta_i^2}{\cdot}\frac{3{\cdot}E_g{\cdot}I_d}{2{\cdot}C_d{\cdot}U_{dc}^2}\\
a_2&=\omega_{cv}+\frac{3{\cdot}E_g{\cdot}I_d}{2{\cdot}C_d{\cdot}U_{dc}^2}+\frac{3{\cdot}E_g^2}{2{\cdot}C_d{\cdot}L{\cdot}\omega_{ci}{\cdot}U_{dc}^4}+\frac{\omega_{ci}}{4{\cdot}\delta_i^2}.
\end{aligned} \tag{16}$$

Similarly, the reduced-order model of Z_{qq} when the PF is unity is obtained as

$$Z_{qq}(s)=L{\cdot}\frac{s^4+\omega_{ci}{\cdot}s^3+c_2{\cdot}\omega_{ci}{\cdot}s^2+c_1{\cdot}\omega_{ci}{\cdot}s+c_0}{s^3+I_d{\cdot}d_2{\cdot}[\omega_{ci}{\cdot}s^2+d_1{\cdot}\omega_{ci}s+c_0/\omega_{cpll}]} \tag{17}$$

where the c_2, c_1, c_0, d_2, and d_1 are given by

$$\begin{aligned}
d_2&=\frac{L{\cdot}\omega_{cpll}}{E_g},\quad d_1=\frac{\omega_{ci}}{4{\cdot}\delta_i^2}\\
c_2&=\omega_{cpll}+\frac{\omega_{ci}}{4{\cdot}\delta_i^2},\quad c_1=d_1{\cdot}\omega_{cpll},\quad c_0=\frac{\omega_{ci}^2}{4{\cdot}\delta_i^2}{\cdot}\frac{\omega_{cpll}^2}{4{\cdot}\delta_{pll}^2}.
\end{aligned} \tag{18}$$

Practically speaking, the optimum damping ratio is 0.707 [22]. Thus, the damping ratio is fixed at 0.707 for the CL, the PLL, and the VL in the following discussion. In this case, the bandwidth is about the cut-off frequency. Thus, the cut-off frequencies are referred to as the bandwidth, which are to be designed to ensure stability.

C. Expressions of the Maximum NPR Frequencies

At the maximum NPR frequency $\omega_{nd,P_{\max}}$, the real part of $Z_{dd}(j\omega)$ equals zero. Therefore, the analytical expression of $\omega_{nd,P_{\max}}$ can be obtained by solving

$$Re(Z_{dd}(j\omega)) = \omega_{ci}\cdot\frac{4\cdot\omega^4 - 2\cdot\omega_{ci}\cdot k_1\cdot\omega^2 - k_1\cdot k_2\cdot\omega_{ci}^3}{(2\cdot\omega^2+\omega_{ci}\cdot k_2)^2+4\cdot k_2^2\cdot\omega^2} = 0 \tag{19}$$

where

$$k_1 = \omega_{cv} + \underbrace{\frac{3\cdot E_g}{2\cdot C_d\cdot U_{dc}^2}\cdot I_m}_{\omega_r},\quad k_2 = \underbrace{\frac{L}{E_g}\cdot I_m}_{h}\cdot\omega_{cv}. \tag{20}$$

I_m denotes the steady-state current I_d at the maximum charging power. The term ω_r can be regarded as a frequency whose value is much smaller than ω_{ci}. Since $\omega_{nd,P_{\max}}$ is positive, (19) has only one reasonable solution obtained as

$$\omega_{nd,P_{\max}} = \sqrt{\frac{\omega_{ci}}{2}\cdot\frac{k_1+\sqrt{k_1\cdot(k_1+4\cdot k_2\cdot\omega_{ci})}}{2}}. \tag{21}$$

Similarly, the maximum NPR frequency ω_{nq,P_0} can be obtained by solving

$$Re(Z_{qq}(j\omega)) = L\cdot\omega_{ci} - L\cdot\frac{\omega_{ci}^2\cdot\omega_{cpll}}{2\cdot\omega^2} = 0. \tag{22}$$

Since (22) has only one reasonable solution, the ω_{nq,P_0} is obtained as

$$\omega_{nq,P_0} = \sqrt{\frac{\omega_{cpll}\cdot\omega_{ci}}{2}}. \tag{23}$$

D. Expressions of the Resonant Frequencies

Given that $k_1 < \omega_{ci}/2$ and k_2 is always positive, the expression of the $\omega_{nd,P_{\max}}$, namely (21), indicates a lower boundary of k_1 and a upper boundary of $\omega_{ci}/2$ of the $\omega_{nd,P_{\max}}$. Therefore, if the $\omega_{rd,P_{\max}}$ is smaller k_1, the system is unstable because the $\omega_{rd,P_{\max}}$ is smaller than the $\omega_{nd,P_{\max}}$ in this case. On the contrary, when the $\omega_{rd,P_{\max}}$ is located in the frequency range beyond $\omega_{ci}/2$, the system is stable because the $\omega_{rd,P_{\max}}$ is larger than the $\omega_{nd,P_{\max}}$ in this case.

To simplify the expression of $\omega_{rd,P_{\max}}$, three frequency ranges, namely low frequency range, medium frequency range, and high frequency range, are defined according to the lower and upper boundary of the $\omega_{nd,P_{\max}}$. The magnitude $|Z_{dd}(j\omega)|$ is approximated by ignoring the small items in the different frequency ranges, which is obtained as

$$|Z_{dd}(j\omega)| \approx \begin{cases} \left|\frac{L}{k_2}\cdot\frac{2\cdot k_1\cdot j\omega+\omega_{cv}^2}{2\cdot j\omega+\omega_{cv}}\right| & (\omega\le k_1) \\ \left|\frac{L\cdot\omega_{ci}^2\cdot j\omega}{-2\cdot\omega^2-2\cdot k_2\cdot\omega_{ci}\cdot j\omega-k_2\cdot\omega_{ci}^2}\right| & \left(k_1<\omega\le\frac{\omega_{ci}}{2}\right) \\ \left|\frac{-L\cdot\omega^2+\omega_{ci}\cdot j\omega}{j\omega-k_2\cdot\omega_{ci}}\right| & \left(\omega>\frac{\omega_{ci}}{2}\right). \end{cases} \tag{24}$$

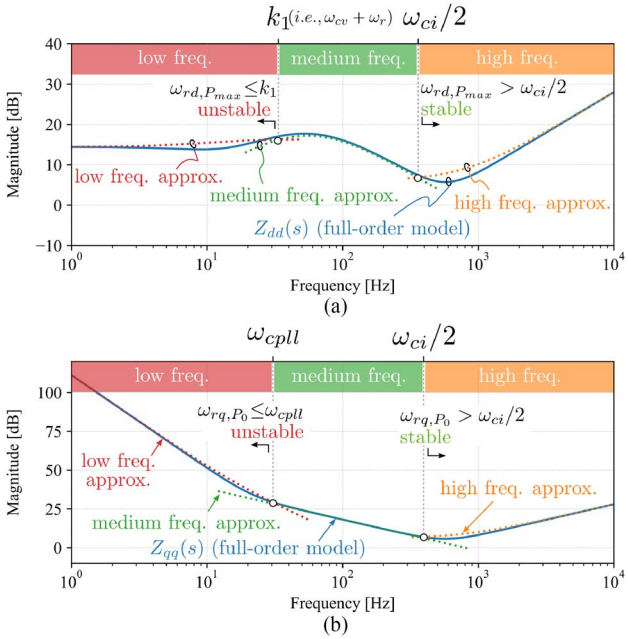

Fig. 6. (a) Comparison of the approximation of $|Z_{dd}(j\omega)|$ using (24) to the full-order model in the different frequency ranges evincing the approximation is accurate. (b) Comparison of the approximation of $|Z_{qq}(s)|$ using (26) with the full-order model in the different frequency ranges evincing the approximation is accurate.

Fig. 6(a) illustrates the accuracy of the magnitude approximation given by (24) using Design 1 specifications in Table II. As aforementioned, only the math expression of the $\omega_{rd,P_{\max}}$ in the medium frequency range is of interest. Substituting the expression of $|Z_{dd}(j\omega)|$ in the medium frequency range into $|Z_{dd}(j\omega_{rd,P_{\max}})| = |L_g\cdot\omega_{rd,P_{\max}}|$, the expression of $\omega_{rd,P_{\max}}$ is obtained as

$$\omega_{rd,P_{\max}} = \frac{\omega_{ci}}{\sqrt{2}}\cdot\sqrt{\frac{L}{L_g}-\frac{L}{E_g}\cdot I_m\cdot\omega_{cv}}. \tag{25}$$

Similarly, given that $\omega_{cpll} < \omega_{ci}/2$, (26) indicates that the lower boundary and the high boundary of the ω_{nq,P_0} are ω_{cpll} and $\omega_{ci}/2$, respectively. Accordingly, the low-, medium-, and high-frequency ranges are defined to simplify the expression of $|Z_{qq}(j\omega)|$ in the different frequency ranges, which is beneficial for obtaining a concise expression of the ω_{rq,P_0}. As a result, the magnitude $|Z_{qq}(j\omega)|$ at zero charging power is approximated by ignoring the small items in the different frequency ranges, which results in

$$|Z_{qq}(j\omega)| \approx \begin{cases} \left|\frac{L\cdot c_1\cdot\omega_{ci}\cdot j\omega+L\cdot c_0}{\omega^3}\right| & (\omega\le\omega_{cpll}) \\ \left|\frac{L\cdot\omega_{ci}^2}{2\cdot\omega}\right| & \left(\omega_{cpll}<\omega\le\frac{\omega_{ci}}{2}\right) \\ |L\cdot(\omega+\omega_{ci})| & \left(\omega>\frac{\omega_{ci}}{2}\right). \end{cases} \tag{26}$$

The approximation results are illustrated in Fig. 6(b) evincing the error caused by the approximation is low. Similarly, only the

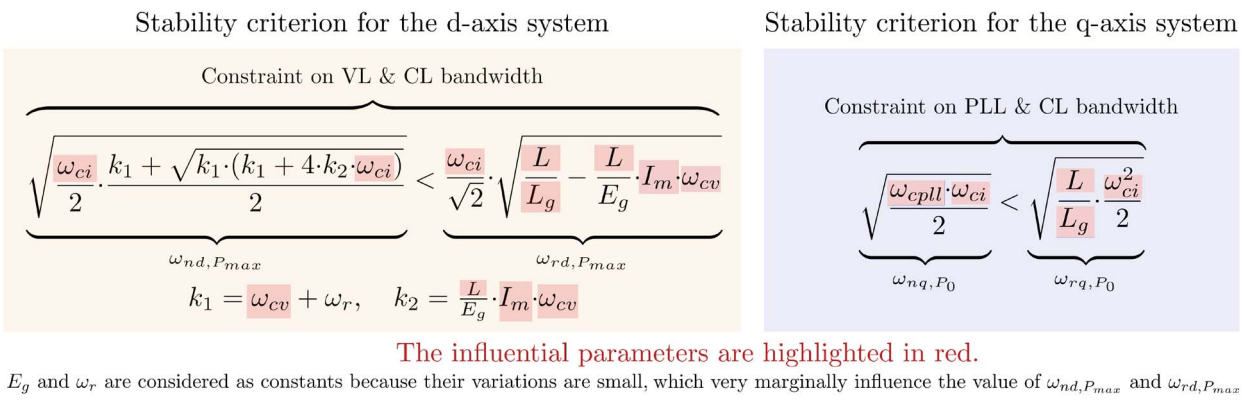

Fig. 7. Sufficient and necessary conditions for stability expressed with the design parameters obtained by substituting (21), (25), (23), and (27) into (1).

TABLE I
IMPACT OF THE INFLUENTIAL PARAMETERS ON THE CRITICAL FREQUENCIES AND STABILITY AS INDICATED BY (21), (25), (23), AND (27)

Action	Consequences				Stability Impact
	$\omega_{nd,P_{max}}$	$\omega_{rd,P_{max}}$	ω_{nq,P_0}	ω_{rq,P_0}	
$\omega_{ci}\uparrow$	$\uparrow$	$\uparrow$	$\uparrow$	$\uparrow$	–
$\omega_{cv}\uparrow$	$\uparrow$	$\downarrow$	N.A.	N.A.	Negative
$\omega_{cpll}\uparrow$	N.A.	N.A.	$\uparrow$	N.A.	Negative
$L\uparrow$	$\uparrow$	$\uparrow$	N.A.	$\uparrow$	–
$L_g\uparrow$	N.A.	$\downarrow$	N.A.	$\downarrow$	Negative

Denotation meaning	
$\uparrow$	Increase. E.g., increasing ω_{ci} leads to the increase of $\omega_{nd,P_{max}}$.
$\downarrow$	Decrease. E.g., increasing ω_{cv} leads to the decrease of $\omega_{rd,P_{max}}$.
N.A.	Not related.
–	Unclear. Further analysis will be given in Section IV.

expression of the ω_{rq,P_0} in the medium frequency range is of interest. Substituting (26) in the medium frequency range into $|Z_{qq}(j\omega_{rq,P_0})|=|L_g\cdot\omega_{rq,P_0}|$ gives

$$\omega_{rq,P_0}=\sqrt{\frac{L}{L_g}\cdot\frac{\omega_{ci}^2}{2}}. \tag{27}$$

E. Impact of Influential Parameters on Stability

The sufficient and necessary conditions to maintain small signal stability can be obtained by substituting (21), (25), (23), and (27) into (1), which are illustrated in Fig. 7. It is revealed that the stability criterion for the d-axis system actually poses a constraint on the selection of the VL and CL bandwidth whereas the stability criterion for the q-axis system poses a constraint on the selection of the PLL and CL bandwidth. For maintaining stability, reducing the maximum NPR frequency and increasing the resonant frequency are preferred, since it enlarges the stability margin. Based on (21), (25), (23), and (27), the impact of the influential parameters on stability are summarized in Table I.

IV. ANALYTIC DESIGN OF THE CONTROLLER

A. Upper limit of the PLL and VL bandwidth

Based on Fig. 7, the boundary constraining the selection of the PLL bandwidth is obtained as

$$\omega_{cpll}<\frac{L}{L_g}\cdot\omega_{ci}. \tag{28}$$

Given the definition of the SCR [10], (28) can be rewritten as

$$\omega_{cpll}<\underbrace{\frac{2\cdot P_{\max}\cdot\omega_1}{3\cdot E_g^2}\cdot\mathrm{SCR}\cdot L}_{g}\cdot\omega_{ci} \tag{29}$$

where ω_1 is the grid angular frequency, and $P_{\max}$ is the maximum charging power. Note that satisfying (29) is a sufficient condition for the existence of the solution of (27).

Further, based on Fig. 7, the boundary constraining the selection of the VL bandwidth is obtained as

$$\omega_{cv}<\frac{g}{h}-\frac{\sqrt{g^2+4\cdot g\cdot h\cdot\omega_{ci}\cdot(g+h\cdot\omega_r)}-g}{2\cdot h^2\cdot\omega_{ci}}$$
$$\Longrightarrow \omega_{cv}<\omega_1\cdot\mathrm{SCR}\cdot\left(1-\frac{\sqrt{1+4\cdot h\cdot\omega_{ci}\cdot(1+\frac{\omega_r}{\omega_1\cdot\mathrm{SCR}})}-1}{2\cdot h\cdot\omega_{ci}}\right). \tag{30}$$

It is worth mentioning that satisfying (30) is a sufficient condition for the existence of the solution of (25).

B. Discussion

Based on (29) and (30), the following can be observed.

1) (29) indicates that the maximum allowed PLL bandwidth ω_{cpll} decreases with the reduction of the SCR. However, it can be increased by increasing the CL bandwidth ω_{ci} and the filter inductance.
2) (30) indicates that the maximum allowed VL bandwidth ω_{cpll} decreases with the reduction of the SCR. However, it can be increased by increasing the CL bandwidth ω_{ci} and the filter inductance.
3) Increasing the filter inductance increases the maximum allowed PLL and VL bandwidth. Inversely, keeping the

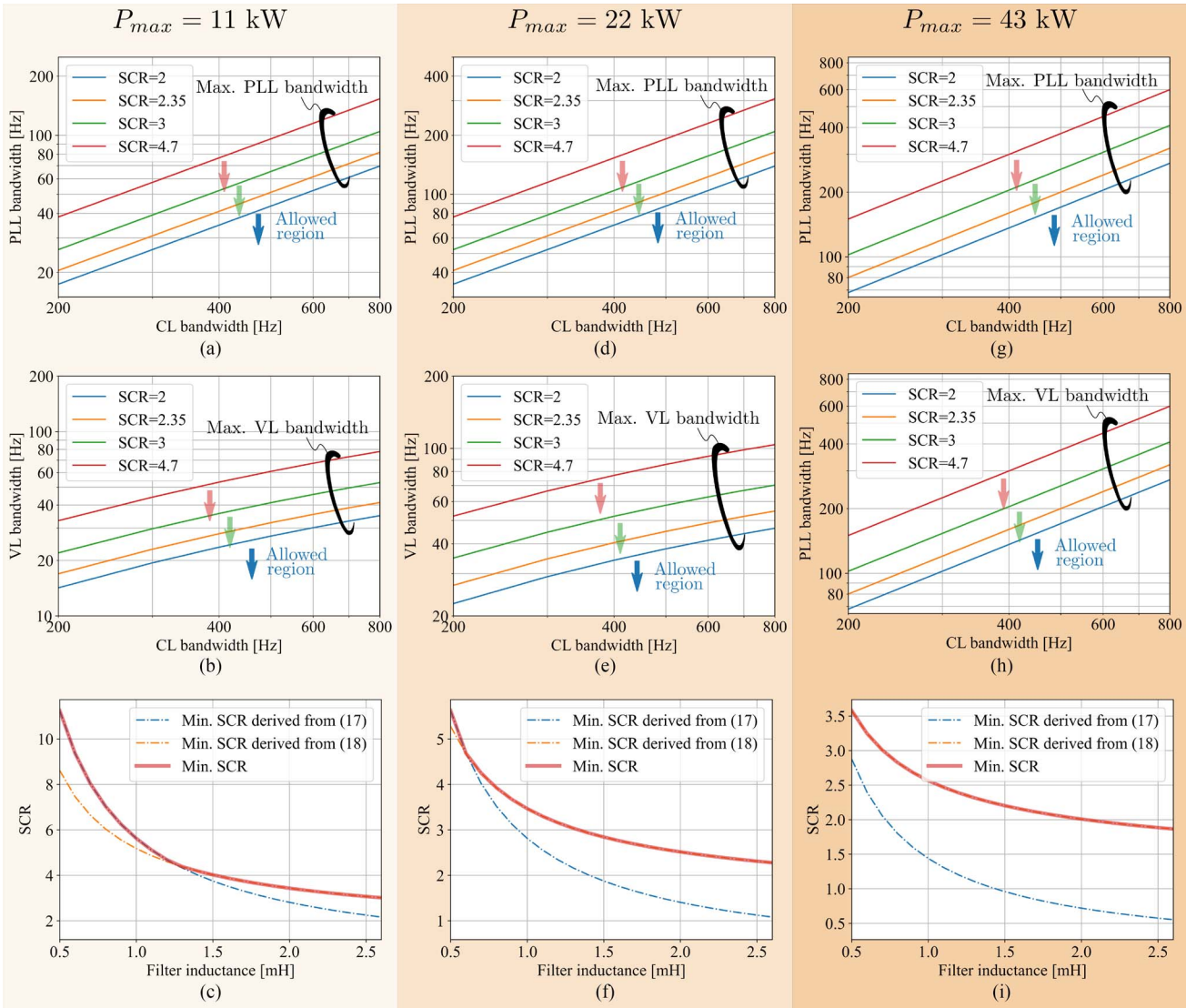

Fig. 8. Visualization of the observations from (29) and (30) with an example PFC whose specifications are given by Design 2 in Table II with three different typical power rating levels of EV chargers. (a), (b), (d), (e), (g), and (h) show the upper limits of the PLL and VL bandwidth increase with a higher CL bandwidth. (c), (f), and (i) show the minimum allowed SCR can be reduced by increasing the filter inductance. Comparing (a), (b), and (c) to (d), (e), and (f) or (g), (h), and (i) indicates that without changing the control and filter design, a PFC with a higher power rating can stably operate in a lower SCR case.

PLL, VL, and CL bandwidth unchanged, using a higher filter inductance allows the PFC of a charger stably operate with a lower SCR.

4) Without changing the control and filter design, the charger PFC with a higher charging power can stably operate in a lower SCR case. The reason is that a higher charging power leads to a smaller grid impedance L_g if the SCR is unchanged. Such increases the resonant frequency and the stability margin since the charger input impedance does not significantly change with different charging power. Thus, a lower SCR is allowed.

To showcase the observations above, an example PFC with the specifications shown in Design 2 in Table II is given. The calculated f_{cpll} and f_{cv} upper limit when selecting different f_{ci} and the minimum SCR for the stable operation when choosing different filter inductance are illustrated in Fig. 8 for three standard power rating levels of EV chargers.

The calculations shown in Fig. 8 are verified with simulations. Specifically, assuming the SCR is 2.35 and the P_{max} is 11 kW, when f_{ci} is 800 Hz, the calculated upper limit of the f_{cv} and f_{cpll}, as seen in Fig. 8(a) and 8(b), is about 41 Hz and 77 Hz, respectively. In the simulation shown in Fig. 9(a), the PFC is operating at the maximum power and it has the same design as Design 2 but with a f_{cpll} reduced to 10 Hz to be far below its upper limit. As seen, once reducing the f_{ci} at t_0, the system becomes unstable. It happens because the upper limit of the f_{cv} reduces after decreasing the f_{ci}, and the 41-Hz f_{cv} exceeds the reduced upper limit of the f_{cv}.

With the same PFC and SCR, another simulation shown in Fig. 9(b) is carried out in no load condition since it is the worst

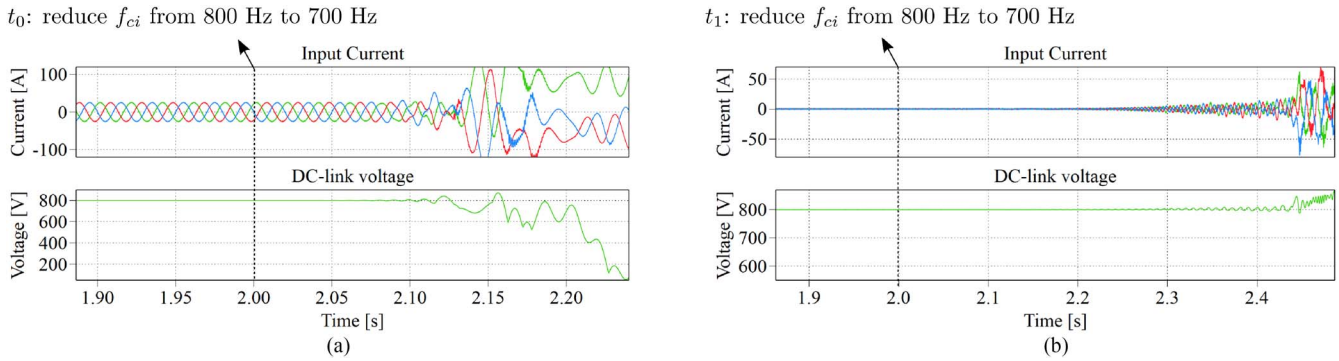

Fig. 9. Influence of the CL bandwidth on (a) the upper limit of the VL bandwidth and (b) the upper limit of the PLL bandwidth.

case for the PLL-related stability. This time, the f_{cpll} is changed to its upper limit of 77 Hz while the f_{cv} is reduced to 10 Hz to be much smaller than its upper limit. As seen, instability appears once reducing the f_{ci}, which happens because the f_{cpll} exceeds the reduced upper limit after decreasing the f_{ci}.

C. Design Steps

Based on the analysis and obtained upper limits for the PLL bandwidth and the VL bandwidth, a design method illustrated in Fig. 10 is concluded to prevent the small signal instability caused by improper controller gain selections.

As seen, the CL bandwidth can be selected first, which is typically below one-twentieth of the switching frequency to sufficiently attenuate the switching noises [23]. Then, after knowing the hardware specifications and the lowest possible SCR, the upper limits of the PLL and VL bandwidth can be calculated. Accordingly, after leaving a proper gain margin (GM) of 3-6 dB [15], [17], as shown in Fig. 11, all controller gains can be selected directly without trials and errors. However, without the proposed approach, one needs to establish the input impedance model of the EV charger. Then, the controller gains are obtained through trials and errors by plotting the characteristic loci of the return ratio matrix [13] and check if any characteristic loci encircle the point of -1+j0. Such a process might take many rounds of iterations to find proper controller gains, which is prevented by applying the proposed approach. Hence, the proposed approach reduces the effort and time of properly tuning the controller in practice.

D. Influences of Neglecting the Coupling Effects

It is worth mentioning that the influences of the coupling effects on stability are neglected when applying (1) as the stability criteria for simplicity. Such a simplification can influence the accuracy of the upper limits of the PLL bandwidth and the VL bandwidth obtained from (29) and (30). However, since a charger's PFC has a unity PF, the coupling impedance is small, which leads to practically trivial influences of neglecting the coupling effects on stability analysis. Hence, the errors of the obtained bandwidth upper limits are small. With leaving a GM of 3-6 dB, the errors caused by neglecting the coupling effects are unproblematic for stability.

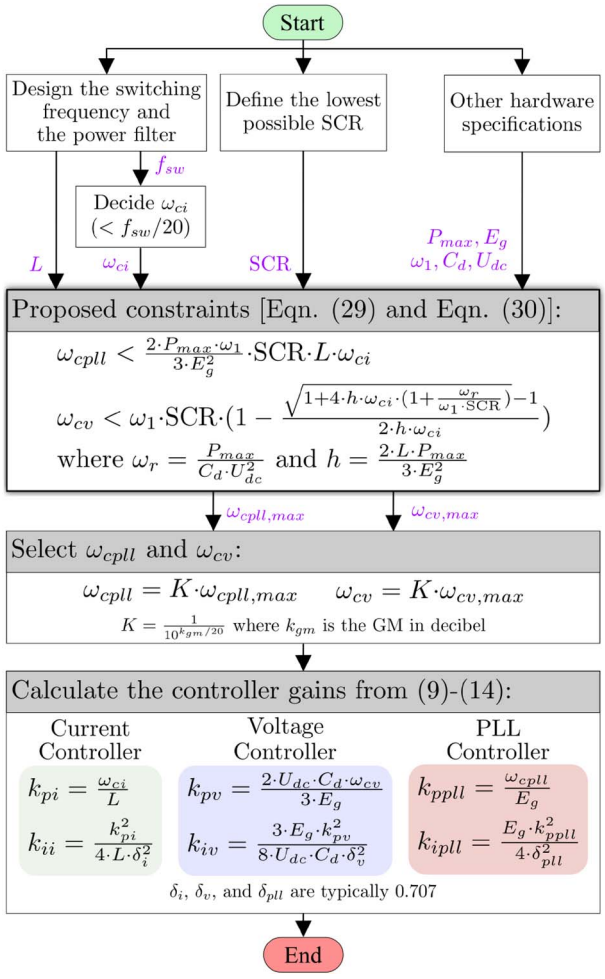

Fig. 10. Flowchart of the proposed approach to tuning the controllers.

Specifically, for the PFC in Fig. 8, the influences of neglecting the coupling effects on the characteristic loci of the return ratio matrix [6] when the SCR is 4.5 are depicted in Figs. 12 and 13. According to the general Nyquist stability criterion (GNC), none of the characteristic loci should encircle the point of -1+j0 for the sake of stability [6]. In the two characteristic loci of the return ratio matrix, namely $\lambda_1(s)$ and $\lambda_2(s)$, only $\lambda_2(s)$ presents the risk of encircling the point of -1+j0 in the

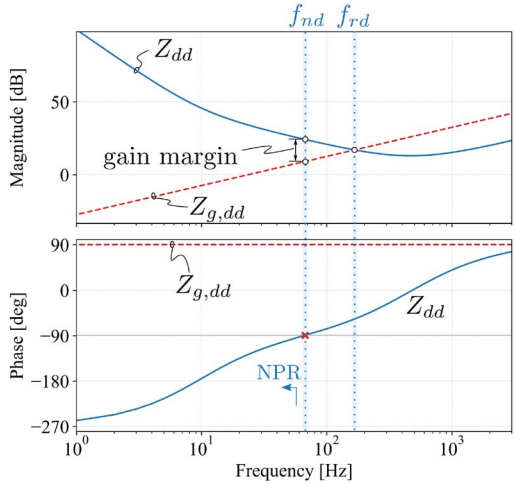

Fig. 11. Gain margin of the d-axis system of a grid-charger system.

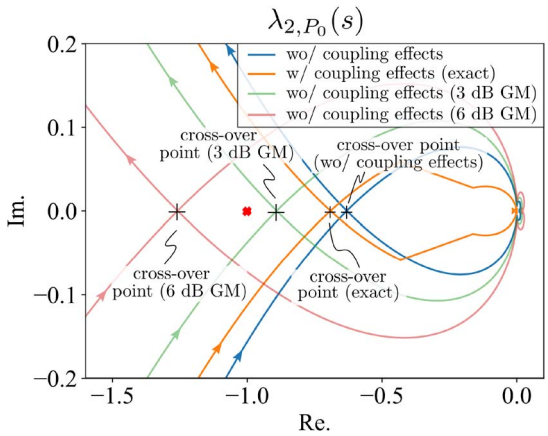

Fig. 12. Influences of neglecting the coupling effects on the characteristic loci of the return ratio matrix when the charging power is zero.

worst case for the q-axis system stability, i.e., when the charging power is zero. Therefore, Fig. 12 compares the locus of the $\lambda_{2,P_0}(s)$, i.e., $\lambda_2(s)$ when the charging power is zero, in the cases with and without considering the coupling effects. It can be seen that the differences between the two are minor. When leaving a GM of 3-6 dB, the point of $-1+$j0 is located between the cross-over point of the locus with a 3-dB GM and the cross-over point of the one with a 6-dB GM. In this case, there is no risk of encircling the point of $-1+$j0 for the loci both with and without the coupling effects.

When the charging power is maximum, which is the worst case for the d-axis system stability, only the $\lambda_1(s)$ presents the risk of encircling the point of $-1+$j0. Hence, Fig. 13 depicts the locus of the $\lambda_{1,P_{\max}}(s)$, which represents the $\lambda_1(s)$ when the charging power is the maximum, in the cases with and without considering the coupling effects. Similarly, after leaving a GM of 3-6 dB, the point of $-1+$j0 is located between the cross-over point of the locus with a 3-dB GM and the cross-over point of

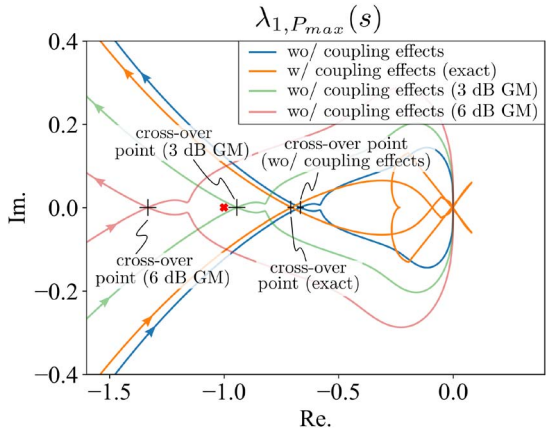

Fig. 13. Influences of neglecting the coupling effects on the characteristic loci of the return ratio matrix when the charging power is maximum.

the one with a 6-dB GM. Consequently, the errors caused by ignoring the coupling effects are unproblematic for stability.

E. Comparison With the Existing Methods

In [12], design recommendations for the control of voltage source converters (VSCs), which include PFC, are given to shape their input impedance to prevent small signal instability. It concluded that the maximum allowed VL bandwidth and the PLL bandwidth are one-tenth of the CL bandwidth. However, following the recommendation may lead to instability in an extremely weak grid condition.

As an example, two simulations are carried out. The PFC in the simulation has the parameters of Design 2 in Table II and the maximum power of 11 kW. In the first simulation, the VL bandwidth is increased from 41 to 80 Hz, i.e., one-tenth of the CL bandwidth. And, the charger is operating at the maximum power. As seen in Fig. 14(a), at $t_1 = 6$ s, the SCR starts decreasing from 10. When the SCR is decreased to 4.7, the PFC loses stability. The simulation result complies with the analytical result shown in Fig. 8(b) since when SCR is 4.7, a VL bandwidth of 80 Hz is just outside the allowed region.

In the second simulation, the PLL bandwidth is increased to 80 Hz, while the VL bandwidth is reduced to the original 41 Hz. The charger is operating at no-load condition since, for a PFC, it is the worst case for the PLL-related instability. Similarly, at $t_1 = 6$ s, the SCR starts decreasing from 10. When SCR is decreased to 2, the PLL bandwidth of 80 Hz is just over the upper limit, as shown in Fig. 8(a). Thus, the PFC becomes unstable.

The influence of the SCR on small signal stability is considered in two more recent works [15], [17]. However, the influence of the CL bandwidth on the upper limit of the PLL bandwidth or the VL bandwidth was not revealed. Specifically, [15] proposed a method to derive the maximum allowed PLL bandwidth for grid-tied inverters. The proposed method is also valid for the case when the PF is not unity. However, the method still requires modeling the input impedance, and the influence

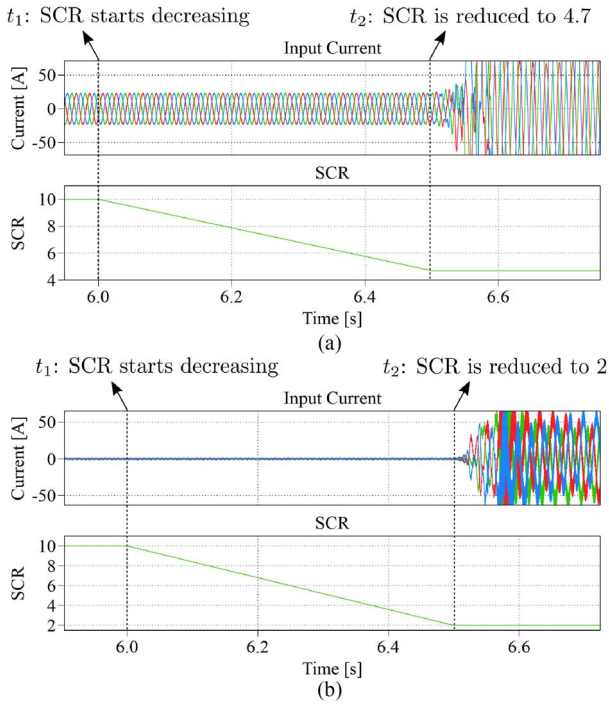

Fig. 14. Influence of SCR on the upper limit of (a) the VL bandwidth and (b) the PLL bandwidth.

of the CL bandwidth on the upper limit of the PLL bandwidth was not revealed and quantified. Wang et al. [17] proposed an approach to select the maximum allowed VL bandwidth for PFCs. It was noticed that with a smaller SCR, the maximum allowed VL bandwidth is decreased, which is also revealed by (30). However, the influence of the CL bandwidth on the maximum allowed VL bandwidth was overlooked. Such an influence of the CL bandwidth on the upper limit of the PLL bandwidth and the VL bandwidth can be seen in the simulation shown in Fig. 9 since the PFC loses stability once the CL bandwidth is reduced.

V. Validations

The analytically derived upper limits of the PLL bandwidth and VL bandwidth are validated by experiments using the setup shown in Fig. 15. The Cinergia grid emulator is used to generate the three-phase grid voltage. The Imperix power test bench mimics a 10-kW EV charger PFC whose power filter is an LC filter. After the PFC, a dc load is connected to emulate the load. The specifications of the PFC in the experiment are given in Table II as Design 3. Three 14.4-mH inductors are used to emulate a 3.5 SCR.

During the experiment, the CL bandwidth is fixed at a certain frequency. Then, the PLL bandwidth and the VL bandwidth are increased by 5 Hz each time until instability happens to verify the calculated upper limit. To demonstrate how instability happens once the bandwidth reaches its upper limit, the transient of increasing the PLL bandwidth to its upper limit is shown in Fig. 16. As seen, before t_0, the CL, PLL, and VL bandwidth are 500 Hz, 50 Hz, and 20 Hz, respectively. At t_0,

Fig. 15. Setup for the experimental verification.

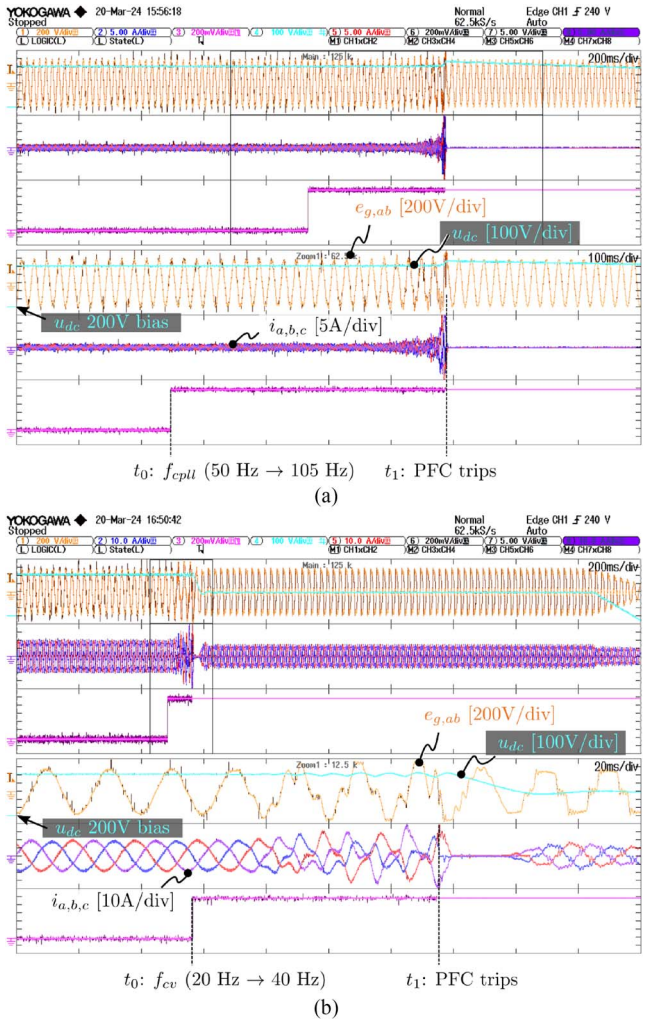

Fig. 16. Experimental validation of (a) the upper limit of the PLL bandwidth calculated with (29) and (b) the upper limit of the VL bandwidth calculated with (30).

only the PLL bandwidth f_{cpll} is increased from 50 to 105 Hz. Then, the PFC loses stability and eventually trips at t_1, which can be seen from the unregulated u_{dc} and ripple-free current

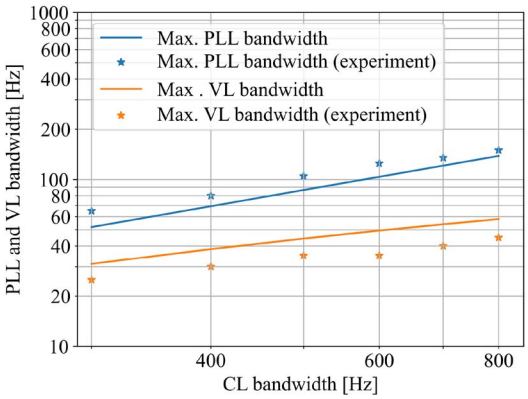

Fig. 17. Validation of the upper limit of the PLL and VL bandwidth.

waveform. Again, note the experiment is conducted at zero operating power because it is the worst case for the PLL-related stability.

In the experiment shown in Fig. 16(b), the bandwidth of the control loops is kept the same as those in the first example. However, this time, the operating power is at the maximum, namely 10 kW, which is the worst case for the VL-related stability. Similarly, at t_0, only the VL bandwidth f_{cv} is increased from 20 to 40 Hz. Then, the PFC loses stability and eventually trips at t_1, which can be seen from the unregulated u_{dc}.

The upper limits of the PLL and VL bandwidth in cases of different CL bandwidths are summarized in Fig. 17. The measured results show a good match with the calculations. The errors of the analytical calculations are not problematic for stability after leaving a 3-6 dB GM as explained in Section IV-C. However, if the control of the EV charger is not the mainstream cascade control method shown in Fig. 1 so that the impedance model of the PFC is different, the obtained upper limits might be invalid. In this case, one should establish the impedance model and apply GNC to analyze if the controllers are properly tuned.

VI. Conclusion

An analytic design approach for the typical PFC control of an EV charger with a weak grid connection was presented. Based on the simplified impedance model, the upper limits of the PLL bandwidth and VL bandwidth, which ensure small signal stability in the whole charging session, were derived analytically and validated with the simulations and experiments. Accordingly, the influences of the CL bandwidth, the filter inductance, and the SCR, on the maximum allowed PLL bandwidth and VL bandwidth, are quantified. Based on the obtained upper limits, a design procedure is proposed, which ensures small signal stability without excessively compromising the PLL bandwidth and the VL bandwidth. The proposed design procedure prevents tuning by trails and errors and does not require establishing the impedance model, which makes the controller tuning much easier.

Appendix

The specifications of the example PFCs are given below.

TABLE II
SPECIFICATIONS OF THE PFC

Param.	Description	Value		
		Design 1	Design 2	Design 3
E_g	Grid RMS voltage	230 V	230 V	230 V
U_{dc}	Dc-link voltage	800 V	800 V	700 V
f_1	Grid frequency	50 Hz	50 Hz	50 Hz
f_{sw}	Switching frequency	20 kHz	20 kHz	20 kHz
L	Power filter inductance	0.4 mH	2.5 mH	2.5 mH
C_f	Power filter capacitance (if applicable)	-	10 μF	5 μF
C_d	PFC output capacitance	1.5 mF	1.5 mF	0.83 mF
f_{cpll}	PLL bandwidth	30 Hz	77 Hz	50 Hz
δ_{pll}	PLL damping ratio	0.707	0.707	0.707
f_{ci}	CL bandwidth	800 Hz	800 Hz	500 Hz
δ_i	CL damping ratio	0.707	0.707	0.707
f_{cv}	VL bandwidth	20 Hz	41 Hz	20 Hz
δ_v	VL damping ratio	0.707	0.707	0.707
$P_{\max}$	Nominal power	30 kW	-	10 kW

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