Integrated Design of a Scalable SPAD-array for On-Chip Magnetometers

Analyzing and designing an on-chip SPAD-array for bio-sensing applications fabricated with 40-nm CMOS technology

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ANALYZING AND DESIGNING AN ON-CHIP SPAD-ARRAY FOR BIO-SENSING APPLICATIONS FABRICATED WITH 40-NM CMOS TECHNOLOGY

Thesis

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Felix BARZILAIJ
Zhi JIN

Students:	Felix Barzilaij	5728673
	Zhi Jin	5796083
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Thesis committee:	Dr. S. Nur,	TU Delft, supervisor
	Dr. ir. M. A. P. Pertijs,	TU Delft, jury chair
	Dr. ir. S. Izadkhast,	TU Delft, jury member

ABSTRACT

The biomedical world is seeking imaging devices that are compact, operative at room-temperature and of high spatial resolution to enhance the localization and detection of living cells. This includes applications such as the detection of cancer cells among healthy tissue. To this end, CMOS chips containing arrays of single-photon avalanche diodes (SPADs) are a promising subject with excellent potential to drive advancements in the field of bio-sensing. In this work, we present a 1.32 x 1.32 mm imaging chip consisting of a 16 x 16 SPAD-pixel array and a 32 pin I/O ring. The SPAD-pixels are organized into rows, with each SPAD-row connected to a single I/O pin. To output all the data from each SPAD-pixel in a row serially, a parallel in, serial out (PISO) shift register is integrated into the SPAD-row. Each SPAD-pixel consists of a photon-detecting SPAD-cell, a voltage controlled resistor (VCR) and its complementary circuit. This circuitry includes an active quenching and recharge circuit, a counter-based externally configurable hold-off mechanism and a count register with a Schmitt-trigger capable of counting up to $1.0 \cdot 10^6$ detected photons over an 1-s integration time. In addition, the SPAD-array architecture is scalable, requiring minimal adjustments to expand to a larger format. The chip is developed for applications in quantum diamond sensing, a promising method for high-resolution magnetic field imaging. This work was conducted in the context of the Bachelor Graduation Project at the TU Delft Faculty of Electrical Engineering, Mathematics and Computer Science, in collaboration with the Quantum Integration Technology (QIT) group.

PREFACE

The work presented in this thesis titled *Integrated Design of a Scalable SPAD-array for On-Chip Magnetometers* is a testament to years of dedication, devotion and determination throughout our journey of the Bachelor Electrical Engineering. Over the course of the project, we refined our existing academic skills and developed new ones. We acquired a deeper understanding of the importance of thorough literature study, familiarized ourselves with the environments of Cadence and Comsol and achieved a high level of proficiency in writing HDL code. Even though the going got tough due to our initial inexperience in chip design, we persevered and managed to successfully complete the project, learning a great amount in the process. It goes without saying that the accomplishments of this project were by virtue of excellent all-round teamwork, which extends beyond merely the authors of this thesis.

We would like to express our deepest gratitude to our main supervisor Dr. Salahuddin Nur for supervising us over the course of the Bachelor Graduation Project. Embarking on this endeavor has been an enormous honor and privilege, and we are truly thankful for the amazing opportunity you have given us. In addition, we would like to thank our daily supervisor Diederik Dekkers, for his magnificent feedback and close monitoring of our progress, for which we are immensely grateful. We would also like to acknowledge Asmae El Arrassi for providing us with helpful command scripts and short-term guidance on IC design software, which significantly aided our progress. Furthermore, we are greatly thankful to Dr. Ryoichi Ishihara, Nikolaj Nietzsche and Dylan Aliberti for attending our weekly meetings and offering invaluable input on the trajectory of our project. We would also like to express our sincerest appreciation to Dr. Ir. Michiel Pertijs and Dr. Ir. Seyedmahdi Izadkhast for serving as members of the jury during our final defense. Lastly, we wish to thank our extraordinary teammates Jurre Botman, Seppe Dijkstra, Isa Spoler and Kevin Vermaat for their key contributions to the project and the occasional laughs and giggles they provided.

Felix Barzilaij
Zhi Jin
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CONTENTS

1

INTRODUCTION

Single-photon avalanche diode (SPAD)-based imaging is a well-established technology with applications in fluorescence lifetime imaging microscopy (FLIM) [1], 3D optical imaging [2] and quantum key distribution [3]. An emerging area of interest for fluorescence imaging is its application in cancer diagnosis. According to a study conducted by the World Health Organization, among the most common causes of cancer death in 2020 were lung cancer and liver cancer [4]. These two cancer types also fall into the category of most difficult diagnosable cancers with the likes of pancreatic cancer and kidney cancer [5] [6]. Frequent and effective screening is essential to increase the probability of detecting a tumor before they progress to the third stage. However, current technologies are poorly suited for large-scale screening operations. Physical examinations are ineffective for detecting tumors located deep within organs, regular X-ray CT scans can exceed permissible radiation exposure limits resulting in increased risk exacerbation to tumor formation, and MRI scans, while non-invasive, suffer from low spatial resolution in addition to its lengthy and expensive procedure [7] [8]. There is, therefore, a high demand for imaging methods that are effective, efficient, and capable of achieving high spatial resolution.

Fluorescence imaging using on-chip SPAD-arrays as cameras have proven to be a compact, reliable and highly effective imaging method in applications where low-intensity light must be detected [9]. This approach has already shown notable progress in the field of bio-sensing, where detection of lower light intensities are common practice [8] [10]. Building upon this foundation we strive in this project to make significant strides towards the development of a handheld room-temperature quantum-based magnetometer for early-stage cancer cell detection. The magnetometer detects magnetic fields induced by certain cells in the bio-sample and is subdivided into three main components: the laser excitation module, the nitrogen-vacancy (NV) center layer on top of which the bio-sample is situated, and the on-chip SPAD sensor. A general overview of the magneto-sensing setup is illustrated in Figure 1.1. This thesis will primarily focus on the SPAD sensor, specifically the design and implementation of the SPAD sensor on-chip. We shall be discussing an improved SPAD-array architecture compared to the one presented by the previous BAP group [11]. Modifications have been made at all three hierarchal levels of the chip, mainly the SPAD-pixel, the SPAD-row and the complete SPAD-array.

The outline of this thesis is presented as follows. Firstly the necessary background theory on the working principles of photon-emitting NV centers and SPAD-pixels is discussed in chapter 2. In chapter 3 the Programme of Requirements for the design is pre-

sented, followed by an overview of the complete design given in chapter 4. Moving on to chapter 5, the components of the SPAD-pixel, which are the SPAD-cell, SPAD-circuit and the counter & multiplexer complex, are discussed in-depth, after which the SPAD-array and its components are presented in chapter 6. The tape-out for the proposed design will be covered in chapter 7, followed by the discussion on the project as a whole in chapter 8. Finally, this thesis will conclude with the main drawn conclusion and recommendations on this project in chapter 9 and a list of proposed future work in chapter 10.

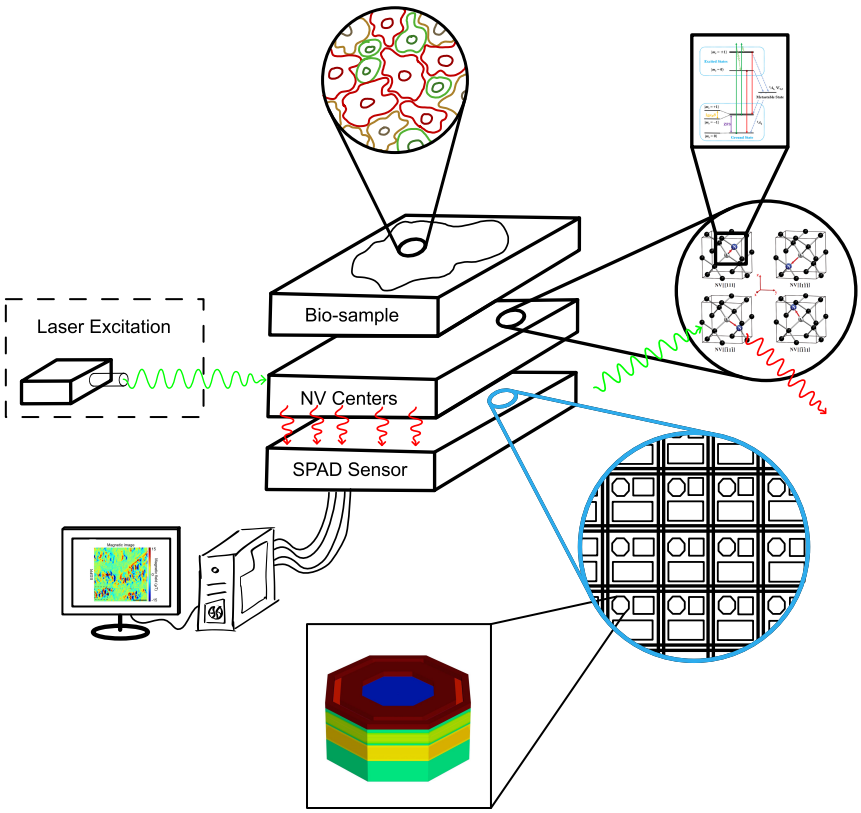

Figure 1.1: **General overview of the magneto-sensing setup.** NV centers are excited by a green photoluminescence through the laser excitation module. Through this excitation red photons are emitted by the NV centers under the influence of the magnetic field in the bio-sample, which are captured and detected by the SPAD sensor. Data from the SPAD sensor is then interpreted and processed by the computer to produce a magnetic field image of the bio-sample. Highlighted in blue is the main focus of this thesis: the design of the SPAD sensor on-chip. Adapted from [12].

2

BACKGROUND THEORY

Summary - *Nitrogen-vacancy (NV) centers are point defects consisting of a nitrogen atom and a vacancy forming a quantum system. The energy-level diagram of a NV center consists of a ground state $|g\rangle$, excited state $|e\rangle$ and metastable shelving state $|s\rangle$. The degeneracy of each of these states is lifted by spin-spin interaction into a zero-spin state $|m_s = 0\rangle$ and a unity-spin state $|m_s = \pm 1\rangle$, together forming a triplet state. Optical excitation by green light transfers systems from $|g\rangle$ to $|e\rangle$. While NV defects in the $|m_s = 0\rangle$ spin state relax back to the ground state by radiating red light, those in the $|m_s = \pm 1\rangle$ spin state may enter a secondary non-radiative decay path via the shelving state $|s\rangle$ and return to the $|0,g\rangle$ state. A dip in the red photoluminescence can therefore be related to the presence of systems in the $|m_s = \pm 1\rangle$ spin state. The $|0,g\rangle$ state may be transferred to the $|\pm 1,g\rangle$ state by applying microwaves at the resonance frequency on the NV centers. In the absence of external DC magnetic fields this value is equal to the zero-field splitting ZFS $D_G = 2.87$ GHz. By applying static magnetic fields the resonance frequencies are split due to the Zeeman effect. The resonance frequency splitting (or: linewidth) $\Delta\nu$ between the resonance frequencies is directly related to the magnitude of the magnetic field and therefore by sweeping microwaves in the region of ~ 2.87 GHz an optically detected magnetic resonance (ODMR) spectrum can be plotted from which $\Delta\nu$ can be derived. To achieve a magnetometer with a high sensitivity, the alignment of microwaves with the quantization axes of the NV centers needs to be optimized and the effect of off-axis static magnetic fields minimized. The detection of red luminescence is done by single-photon avalanche diodes (SPADs), which are essentially pn-junctions reversely biased above the breakdown voltage such that a single photon triggers a self-sustaining avalanche. After photon detection a SPAD is quenched to below the breakdown voltage to suppress the avalanche, where after a set hold-off time the SPAD is recharged to the desired reverse bias. Photon count accuracy is constrained by internal noise such as dark counts, after-pulsing and crosstalk. SPADs arranged in an array structure form a photon detector. In the present day, microwave-launching structures exist which ensure high uniformity across a large area as well as high power-delivery efficiency.*

2.1. INTRODUCTION

A quantum-based magnetometer relies on the detection of magnetic field mainly on decreases in photoluminescence in the visible spectrum from point defects in the diamond lattice upon exposure to microwaves at frequencies ~2.87 GHz. To achieve representative measurements of the local magnetic field it is of great importance that the microwave frequencies at which photoluminescence is at a minimum can be determined accurately and precisely thus increasing the sensitivity of the magnetometer. Several factors influence the magnetic sensitivity including the relative distribution of point defect orientations, internal detector noise and uniformity of microwave fields. In this chapter, the three most significant aspects of an intricate quantum-based magnetometer will be discussed. Firstly, the photodynamics of nitrogen-vacancy centers, which are the source of the previously mentioned photoluminescence, will be treated. Next, the working principles of single-photon avalanche diodes, which will function as the detector of incoming photons from the diamond lattice, are covered. Finally, this chapter concludes with a brief discussion on different concepts of microwave-launching structures for the generation of microwaves.

2.2. PHOTODYNAMICS OF NV CENTERS

A nitrogen-vacancy (NV) center is a point defect in a face-centered cubic diamond lattice, where one of the carbon atoms is replaced by a nitrogen atom with one of its adjacent carbon atoms also being displaced forming a vacancy as a result as shown in Figure 2.1a. By capturing an additional free-floating electron from the conduction band, the hybridization of two unpaired electrons leads to a two-level quantum system with a spin magnetic triplet in its ground state [13]. This ground state consists in the absence of an external magnetic field of a zero-spin state at the lowest energy level denoted by $|m_s = 0\rangle$, and a state with unity spin $|m_s = \pm 1\rangle$ separated by a zero-field splitting (ZFS) of $D_G = 2.87$ GHz, together forming the triplet state [14]. Similarly in the excited state the two spin states are separated by a smaller ZFS parameter of $D_E = 1.42$ GHz [15]. Negatively charged NV centers will from now on be referred to as simply 'NV centers'.

Illumination with green light on a NV center results in the excitation of electrons from the ground state $|g\rangle$ to the excited state $|e\rangle$, which occurs in a spin-conserving manner. Therefore, upon excitation quantum systems in the $|0,g\rangle$ and $|\pm 1,g\rangle$ states are transferred to the $|0,e\rangle$ and $|\pm 1,e\rangle$ states respectively. The zero-spin state relaxes back to the ground state $|0,g\rangle$ accompanied by the emission of a red photon. On the other hand, electrons in the $|\pm 1,e\rangle$ state may enter a secondary decay path: a non-radiative intersystem crossing through the metastable shelving state $|s\rangle$ coupled with IR emission [18]. The complete energy-level diagram of a diamond NV center including the states with its respective spin projections is shown in Figure 2.1b.

Most notably, electrons that enter the non-radiative decay path return to the $|0,g\rangle$ ground state. Therefore through optical pumping for a sufficient period of time, the spin population in the ground state is progressively transferred into the $|0,g\rangle$ state, thereby allowing for efficient spin-polarization in the NV centers to the zero-spin state. This initialization step is required to be able to detect the presence of electrons in the $|m_s = \pm 1\rangle$ spin states, since a reduction in red light fluorescence can be associated to the

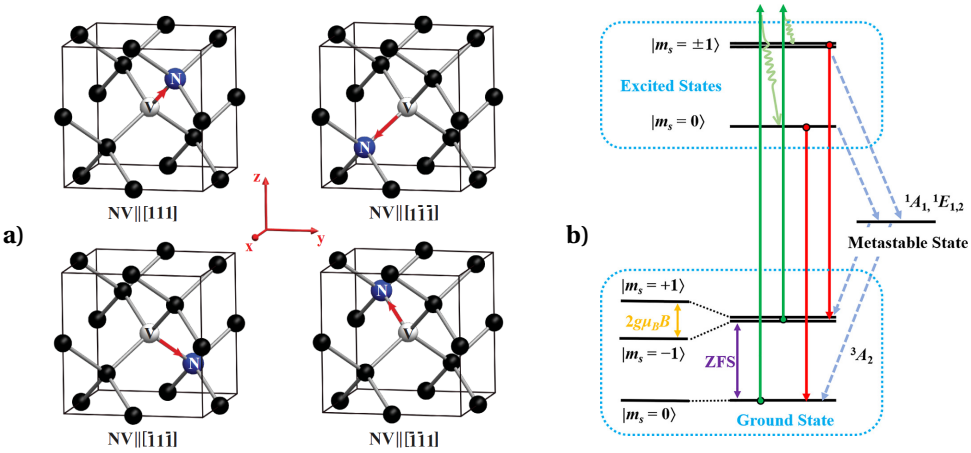

Figure 2.1: **Orientations and energy-level diagram of NV color centers in diamond. (a)** The symmetry axis of NV centers may have four possible orientations along one of the crystallographic axes in the diamond crystal structure. The NV axis, defined as the z-axis in the local reference frame of the NV center, are indicated with red arrows. Carbon atoms, nitrogen atoms and vacancies are depicted here in black, blue and white respectively. **(b)** The spin magnetic triplet in the ground state consists of the $|m_s = 0\rangle$ and $|m_s = \pm 1\rangle$ spin states separated by a zero-field splitting (ZFS) $D_G = 2.87$ GHz. The latter states are further split under influence of the external magnetic field component aligned with the quantization axis of the point defect. Optical excitation to the excited states occurs under illumination of green light. Electrons returning to the ground state are accompanied by broadband red photoluminescence, unless they enter a secondary decay path through the metastable shelving state. Adapted from [16] [17].

aforementioned secondary decay path of the non-zero spin states.

Microwave signals resonant to the $|0\rangle \leftrightarrow |\pm 1\rangle$ transition allow electrons in the $|0,g\rangle$ state to jump to the $|\pm 1,g\rangle$ state. In the absence of external magnetic fields, the spin transition frequencies $\nu_\pm$ correspond to the ZFS $D_G = 2.87$ GHz. However, by applying a finite static (DC) magnetic field $\mathbf{B}_{ext}$ with a component $\mathbf{B}_z$ along the quantization axis of the NV center, a lifting of the degeneracy of the $|m_s = +1\rangle$ and $|m_s = -1\rangle$ can be observed . By recording the fluorescence of NV centers as a function of applied microwave frequency, a technique called optically detected magnetic resonance (ODMR), the spin transition frequencies ν_+ and ν_- in the ODMR spectrum are also split symmetrically from the ZFS as illustrated in Figure 2.2. This phenomenon is called the Zeeman effect and provides the fundamental foundation for nanoscale magneto-sensing. This is due to fact that the splitting between the resonance frequencies is directly related to the magnitude of the component of the magnetic field parallel to the NV quantization axis, as given in Equation 2.1:

$$\Delta\nu = \frac{2g_e\mu_B}{h}|\mathbf{B}_z| = 2\overline{\gamma}_e|\mathbf{B}_z|, \tag{2.1}$$

with $g_e = 2.003$ the NV electronic Landé factor, $\mu_B \approx 9.274 \cdot 10^{-24}$ J T^{-1} the Bohr magneton, $h \approx 6.626 \cdot 10^{-34}$ m^2 kg s^{-1} the Planck constant and $\overline{\gamma}_e$ the reduced NV gyromagnetic ratio ≈ 28 GHz T^{-1} [19].

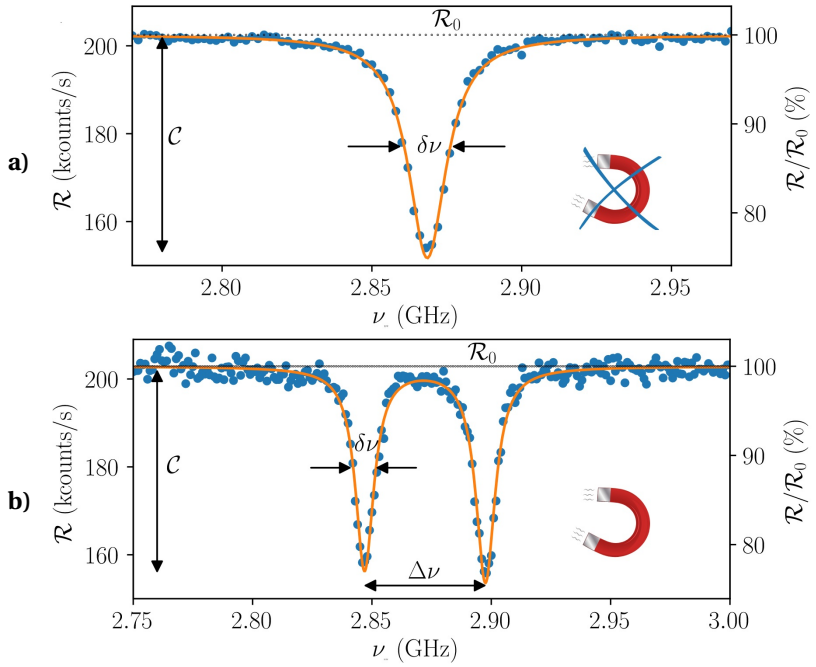

Figure 2.2: **ODMR spectra of NV centers. a)** The magnetic induction is given in units of gauss. $\mathscr{C}$ is the contrast indicating the ODMR resonance amplitude, $\delta\nu$ the resonance linewidth, $\mathscr{R}_0$ the photon count rate at zero resonance and $\Delta\nu$ the splitting between the resonance frequencies $\nu_\pm$. A dip in the normalized fluorescence intensity can be observed at ~ 2.87 GHz in the absence of external DC magnetic fields. **b)** By applying external magnetic fields the dips, and therefore the resonance frequencies $\nu_\pm$ are split further apart from the ZFS. Adapted from [14].

There are two common methods to measure the ODMR spectrum of the NV magnetometer: pulsed excitation and continuous wave (CW) excitation [20]. The performance of the magnetometer under CW excitation can be measured from the magnetic sensitivity, which is defined as the minimum detectable magnetic field with an integration time of 1 s [13]. For magnetometers limited by shot noise, the magnetic sensitivity is defined as shown in Equation 2.2:

$$\eta_{NV}(\mathscr{R}_0, \delta\nu, \mathscr{C}) = B_{min}(t)\sqrt{t} = \frac{\mathscr{P}_f}{\overline{\gamma}_{NV}} \frac{\delta\nu}{\mathscr{C}\sqrt{\mathscr{R}_0}}, \tag{2.2}$$

with $\mathscr{R}_0 = \frac{N_{ph}}{t}$ the photon count rate, $\mathscr{C}$ the contrast, $\delta\nu$ the resonance linewidth and $\mathscr{P}_f$ the profile factor, which is related to the shape of the resonance peak [14]. In this thesis, peaks of the Lorentzian type are primarily covered, for which $\mathscr{P}_f \approx 0.77$. As mentioned before, the sensitivity is assumed to be limited most significantly by shot noise. This limitation is caused by statistical variation in arriving photon distribution. Similar to the large fluctuations in the number of counted heads and tails for a handful of throws each iteration, the relative fluctuations of low photon count-rates may vary significantly such

that it has a detrimental effect on the SNR of the system [21]. A low magnetic sensitivity is desired since it allows for detection of magnetic fields of lower orders of magnitude in the same time period for a less sensitive magnetometer (with a larger η_{NV}) to detect magnetic fields in higher orders of magnitude. Therefore by lowering $\delta\nu$, and increasing $\mathscr{C}$ and $\mathscr{R}_f$ optimization of the magnetic sensitivity can be achieved.

These parameters are influenced by many factors, two of which are the microwave field strength parallel and the external static magnetic fields perpendicular with respect to the quantization axis of the NV centers. The interaction between NV centers and microwaves allows for a transfer of population from the $|0,g\rangle$ to the $|\pm 1,g\rangle$ states, thereby reducing the observed photoluminescence in the optically-detected ESR spectra at the resonance frequency ν. Therefore by aligning the microwave field in such a way that it corresponds with the orientation of the NV centers of interest, the population of NV centers in the $|\pm 1,g\rangle$ state increase, which in turn manifests itself in a larger contrast $\mathscr{C}$ and a smaller resonance linewidth $\delta\nu$ [13].

Application of a DC magnetic field on the diamond lattice serves two main purposes. Firstly, it lifts the degeneracy of the four different NV axis directions of the NV centers differently resulting in eight different resonance peaks in the ODMR spectrum. Secondly, magnetic fields with a negative z-component can be measured relatively straightforward. This is due to the fact that a linewidth $\Delta\nu$ lower than that for zero local magnetic fields is an indication of magnetic fields with a locally negative magnitude. However, off-axis static fields with respect to the orientation of NV axes are regarded as undesirable, since the components perpendicular to the quantization axis induce mixing of electron spin states both in the ground as well as in the excited levels, which results in an overall decrease in photoluminescence intensity and therefore a reduction in ODMR contrast [15]. Off-axis magnetic fields therefore have a detrimental effect on the magnetic sensitivity of the system and should therefore be kept at a minimum for optimization of the system's performance.

2.3. SPAD

Red photon counting is at the core of magnetic field sensing using NV centers. It is therefore of utmost importance to achieve image sensors of high resolution and localization capabilities, such that the detection of single photons and the location of its source can be attained. Single-photon avalanche diodes, or SPADs for short, are ideal for photon correlations detection due to their ability to sense single photons in low intensity illumination as well as their capability to be integrated into high frame-rate arrays. Moreover, their compactness, reliability and room-temperature compatibility make SPADs ideal candidates for NV center-based magnetic field sensing. [9]

SPADs are embedded into digital pixels which include quenching circuits, hold-off with recharge circuits and counter-based timing logic. These supporting circuits are required for proper suppression of avalanches after photon detection and restoration of the detector to the sensing state. Ideally these circuits occupy minimal pixel area such that the fill-factor, defined as the active area over the pixel area, of the SPAD-pixel is maximum hereby enhancing photon collection and sensitivity [22].

Multiple SPAD-pixels can be arranged in an array structure to form a SPAD-array, the photon count data of which allows for the creation of a magnetic field image. Due

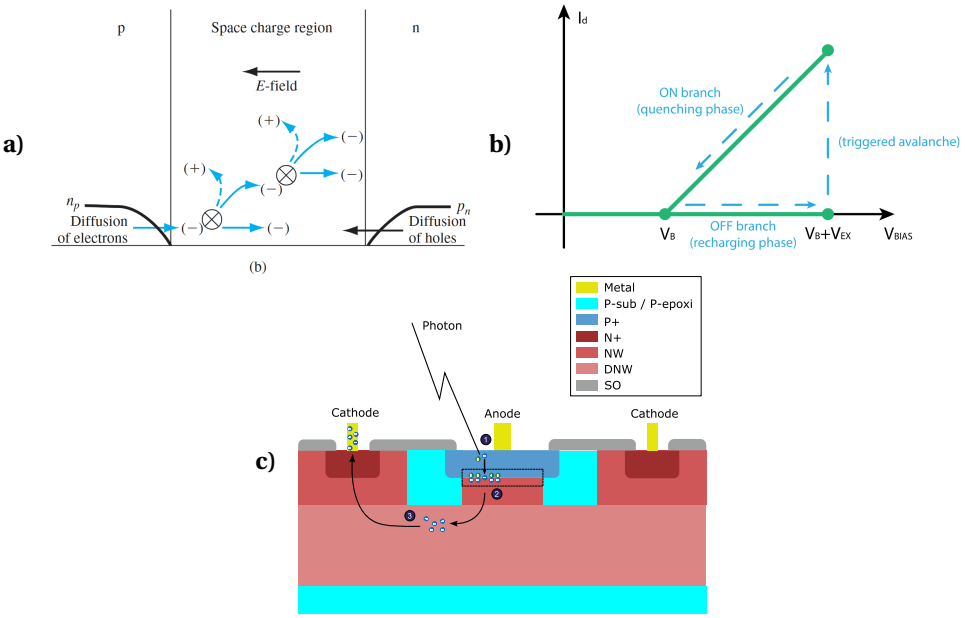

Figure 2.3: **Working principle of single-photon avalanche diodes (SPADs) (a)** Avalanche breakdown process in a SPAD. A single electron acquires sufficient energy to ionize atoms and generate electron-hole pairs, which in turn can also ionize other atoms. The generation of charge carriers that can generate more charge carriers in the depletion region by themselves is the driving force behind the avalanche breakdown process. **(b)** IV characteristics of a SPAD. The pn-junctions is reverse biased to a voltage V_A, which is above the breakdown voltage V_B by an amount equivalent to the excess voltage V_{EX}. Upon excitation by a photon, an avalanche is triggered inside the depletion region and a macroscopic detectable current flows through the SPAD. Through quenching, the reverse bias is lowered to V_B or below, which consequently suppresses the avalanche. The SPAD can be brought back to the sensing state by recharging the SPAD to the desired sensing reverse bias of V_A. **(c)** Cross-sectional view of avalanche breakdown caused by photon excitation in realistic SPAD. In the first step a photon excites a single charge carrier such that it acquires sufficient energy to move through the depletion region. In the second step the excited charge carrier ionizes atoms and generates electron-hole pairs that themselves can also ionize atoms. Finally, the self-sustained avalanche produces a macroscopic detectable output current. Adapted from [23] [24].

to limitations in the number of I/O pins different methods exist for readout of photon counts of each SPAD. These methods range from utilization of multiplexers [1] to PIPO-based readout logic [9].

In the following subsections the working principles of the SPAD-array will be discussed, starting from the lowest hierarchical level, the SPAD-cell, gradually advancing to the highest level, which is the on-chip SPAD-array itself.

2.3.1. SPAD-CELL

SPADs are essentially pn-junctions reversely biased with a voltage V_A above the breakdown voltage V_B. The electric field in the depletion region becomes sufficiently large such that a single charge carrier upon acquiring sufficient energy can create electron-hole pairs by colliding with atomic electrons. The newly generated charge carriers in

turn may also collide and ionize other atoms resulting in a chain reaction of electron-hole pair generation. This phenomenon is known as an avalanche breakdown process and it is self-sustaining as long as the electric field, and therefore the reverse bias remains sufficiently large [25] [23].

Since the SPAD does not turn itself off after photon detection, the avalanche process needs to be quenched. Different methods for quenching exist, the two predominantly utilized will be discussed in the next section. After quenching a restoration of the reverse bias is necessitated. This is traditionally done by connecting the anode of the SPAD to ground for a certain period of time, hereby restoring the necessary over-voltage such that the SPAD is sensitive to photon excitation again [26] [27]. The working principle of SPADs is illustrated in Figure 2.3.

Ideally all photons that reach a SPAD should be detected and consequently result in tangible output pulses. However, in reality the photon-detection efficiency is limited due to non-ideal absorption probability and imperfect triggering of avalanches: not all photons are properly absorbed nor do they always trigger an avalanche. The photon-detection efficiency is defined by the product of the avalanche triggering probability $P_b(\lambda)$ and quantum efficiency $QE(\lambda)$, as shown in Equation 2.3.

$$PDP(\lambda) = P_b(\lambda) \cdot QE(\lambda) \tag{2.3}$$

The avalanche triggering probability is dependent on excess voltage and device structure, while the quantum efficiency is dependent on the silicon absorption coefficient, space-charge region thickness and junction depth.

Photon excitation is not the only source for avalanche breakdown to occur: internal noise of the detector may also contribute to (unwanted) avalanche to be triggered inside the SPAD. For instance, thermally generated carriers may also spuriously trigger avalanches and produce tangible output pulses. The output pulse rate related to these type of generated carriers is called the dark count rate (DCR). The DCR increases with temperature, excess voltage and space-charge region size, which is illustrated in Figure 2.4a and Figure 2.4b.

Another contribution to the internal noise is an phenomenon called after-pulsing. Due to local defects in the depletion region, according to the Shockley-Read-Hall theory an allowed energy state within the forbidden bandgap between the valence band and conduction band exists [23] [25]. This energy state is called a trap. During the avalanche process electrons are captured in these traps, which are then gradually released over time. If this release occurs during the recharge or photon-sensitive states of the SPAD, in other words when the voltage over the SPAD exceeds the breakdown voltage, an unwanted avalanche is triggered, as shown in Figure 2.4c.

The effects of after-pulsing can be limited by introducing a hold-off time, in which the SPAD-voltage is below the breakdown voltage and releases of trapped electrons do not result in initiation of avalanches. The longer the hold-off time, the lower the probability of after-pulsing effects to occur during the light-sensitive state of the SPAD, as illustrated in Figure 2.4d. However, consequently the maximum photon count is reduced significantly. After-pulsing can be additionally reduced by increasing the operating temperature of the SPAD, but as shown in Figure 2.4b, the DCR then increases with increasing temperature. Optimization of all the different parameters to limit the effects

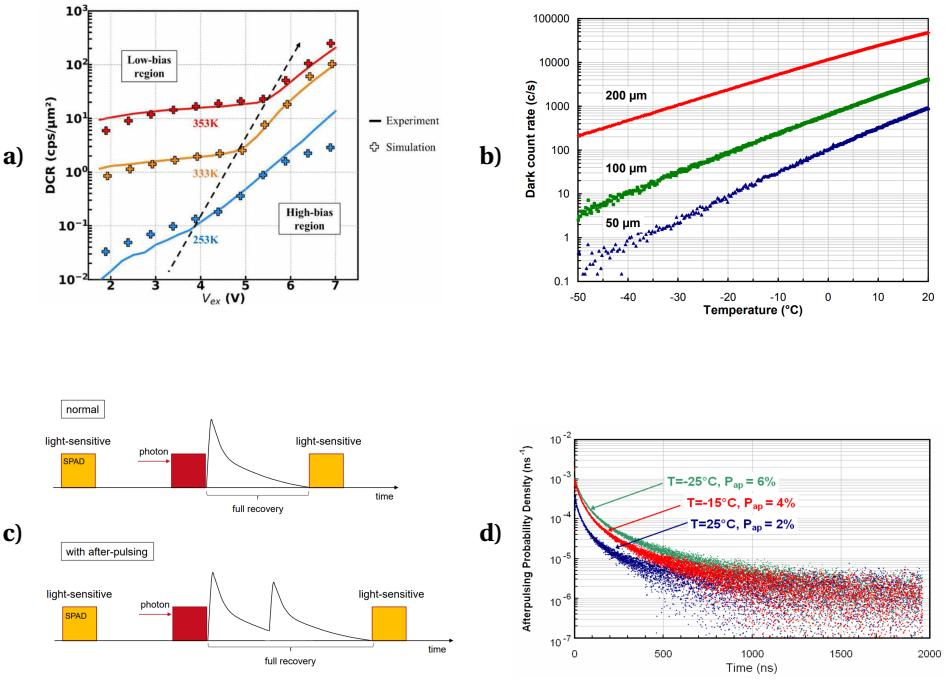

Figure 2.4: **Key characteristics of a SPAD (a)** DCR as a function of excess voltage V_{EX}. The solid curves represent best-fitted experimental measurement curves and the dashed curve simulated measurements. As the excess voltage increases so does the DCR. Moreover, an increase in the operating temperature also gives rise to a surge in DCR. **(b)** DCR as a function of temperature. The scatter plot shows an logarithmic relation between temperature and DCR as temperature increases. Additionally a larger active region also increases the frequency at which dark counts occur. **(c)** Normal SPAD operation compared to after-pulsing occurrence. On the timeline yellow blocks represent the moment SPADs become sensitive to the photoluminescence, red blocks the moment a photon is absorbed by the SPAD, and the curves the avalanche current. The top timeline shows the SPAD making a full recovery in minimum time after a photon is absorbed. The bottom timeline shows the penalty in recovery time due to spurious triggering of an avalanche caused by after-pulsing. **(d)** The after-pulsing probability density as a function of hold-off time. It becomes clear that a longer hold-off is beneficial for minimizing the effects of after-pulsing. However, this comes at the cost of maximum count rate, since the SPAD is insensitive to photons for a longer period of time. The scatter plot also illustrates the effect of decreasing temperature on the probability of after-pulsing occurring. Adapted from [28] [29] [30].

of internal noise is therefore a delicate balancing act.

2.3.2. SPAD COMPLEMENTARY CIRCUIT

Quenching of avalanches, holding-off the SPAD and recharging the SPAD-voltage are done through the supporting circuits of the SPAD. The area that these circuits occupy should be kept at an minimum to maximize the fill factor of the SPAD-cells themselves.

Quenching can be done either passively or actively. Passive quenching is done by connecting a large ballast resistor to the anode of the SPAD. Upon initiation of an avalanche,

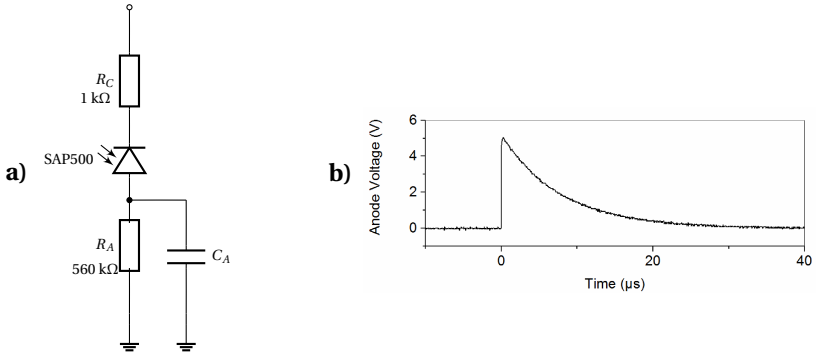

Figure 2.5: **Passive quenching circuit simulation. a)** Example of a passive quenching circuit. The ballast resistor R_A is set at $560k\Omega$ with a parasitic capacitance C_A connected in parallel to it. **b)** Simulation of the passive quenching circuit. At $t = 0$ μs an avalanche is initiated. Gradually over time the anode voltage V_A decreases until it reaches 0 V. Adapted from [31].

a current surge will flow through the resistor, which causes the anode voltage to increase resulting in the SPAD-voltage to drop below the breakdown voltage [31]. As a result, the avalanche is suppressed and the current, and therefore anode voltage gradually decrease. An example of a passive quenching circuit is illustrated in Figure 2.5a and the corresponding response of the anode voltage over time is plotted in Figure 2.5b. Active quenching utilizes a pull-up mechanism using transistors which can detect the rising edge of avalanches. This quenching method is usually combined with active hold-off and recharge. The anode side of the SPAD is connected either to V_{DD} to drop the SPAD-voltage below the breakdown voltage, or to V_{SS} to reinstate the over-voltage across the SPAD.

Due to after-pulsing effects it is necessary to hold the SPAD off for a period of time, such that sufficient time passes for trapped electrons to be released without causing an avalanche to occur. Moreover, it is of great importance that the hold-off time is tunable, due to variability in operating conditions e.g. varying temperature. Different methods exist for tuning the hold-off time. Examples include counter mechanisms [26], resistance tuning [31] and capacitance tuning [27].

Recharging the SPAD to its desired sensing voltage is closely related to the quenching circuit. In passive quenching the decrease in current through the SPAD and consequently ballast resistor allow for the anode voltage to gradually drop to the desired ground level. On the other hand, active quenching relies on transistors to provide a path from the anode side to a ground node for a period of time. Usually the recharge circuit in active quenching is integrated together with the quenching and hold-off components and is therefore not a standalone part of the supporting circuit.

2.3.3. SPAD-ARRAY

A SPAD-cell together with its complementary circuit and counting logic, which keeps track of photon detections, forms a SPAD-pixel. However, a single SPAD-pixel is not

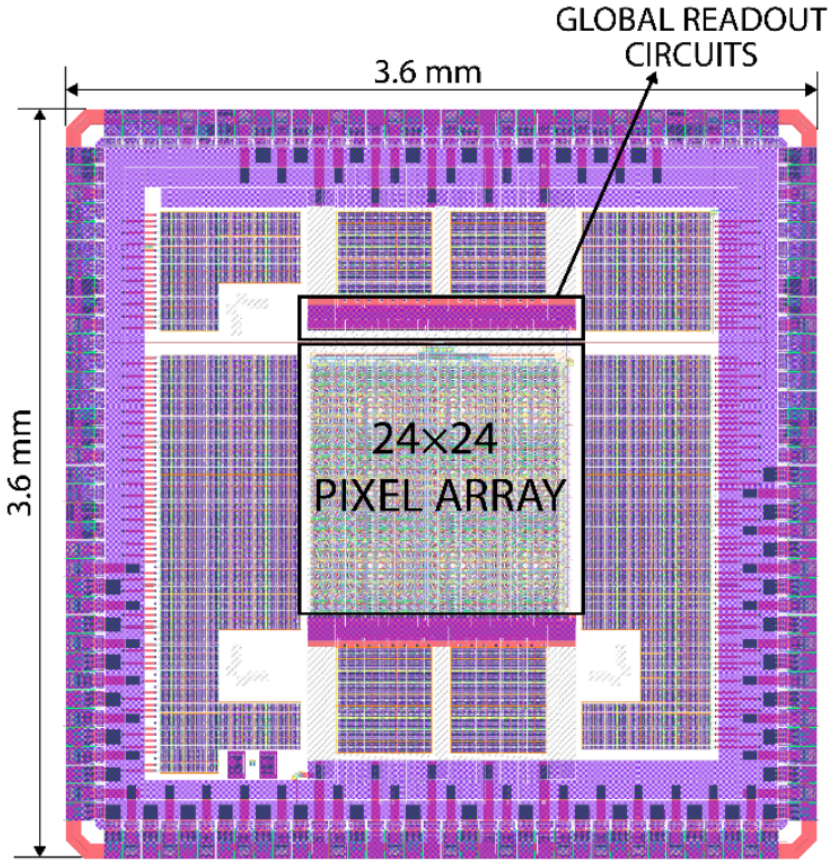

Figure 2.6: **Layout of a 24x24 SPAD imager**. The center contains the 24x24 SPAD-pixel array. Additionally, global readout circuits are integrated on the die and connected to the SPAD-array. Adapted from [9].

greatly useful, and therefore for real-world applications these pixels are arranged together to form a SPAD-array. Sizes range from 24x24 [9] to 512x512 [1], the layout of the former of which is illustrated in Figure 2.6. The two major aspects of SPAD-arrays are data reading and crosstalk.

Rapid and precise data reading are paramount for creating high-contrast ODMR spectra and therefore accurate magnetic field images. With increasing array size, however, direct data reading, so SPAD-pixel directly connected to output pin, gets increasingly constrained. This is due to the fact that the area of a square array growths quadratically with increasing side-length and as a result, relatively less in- or output pads are able to be placed on the sides of the array compared to the amount of SPAD-pixels that can fill the array.

It is therefore necessary to devise smart design choices when it comes to readout architecture. A solution to the previously mentioned problem would be to employ mul-

tiplexers, for example 4:1 multiplexers, for every output pin [1]. This allows for four columns of a single SPAD-pixel row to be connected to the same output pin and for the data of every column to be read sequentially. Another solution, specifically for SPAD-pixels that each output more than one bit, would be to store the data in a parallel input, parallel output (PIPO) register and sequentially read the data of a single SPAD-pixel at the time [30]. Moreover, by using a global readout logic that keeps track if at least one pixel has detected a photon, rows can be skipped that have not registered any photon detections speeding up readout time.

Smart readout architectures are merely beneficial provided that the data is representative. Internal detector noise may cause avalanches to be spuriously triggered without the involvement of photon absorption. On the hierarchical level of the SPAD-pixel we have already discussed two contributions: thermally generated charge carriers and afterpulsing. However, on the level of the SPAD-array an additional factor causes unwanted triggering of avalanches, namely crosstalk. When an avalanche breakdown process occurs charge carriers are accelerated through the depletion region by the present electric field. These charge carriers can lose energy through the emission of photons, a phenomenon called electroluminescence. These charge carrier emitted photons may also be absorbed by adjacent SPAD-pixels resulting in initiation of avalanches. Crosstalk mitigation varies from increasing the distance between devices, etching trenches between adjacent SPADs with opaque material and increasing trench depth [32] [33].

2.4. MICROWAVE GENERATION

As mentioned in Section 2.2, application of a microwave field on NV centers in a diamond lattice allow for the possibility of spin state transitions to occur from the zero spin state $|0,g\rangle$ to the $|\pm1,g\rangle$ state. NV centers in the $|\pm1,e\rangle$ state decay back to the ground state non-radiatively, which can be detected through dips in photon count in the ODMR spectrum. High uniformity of the microwave fields are desired such that the effects of broadening of the ODMR spectrum is kept at a minimum, which is more easily achieved by integrating the microwave-launching structure on-chip [15].

Microwave (MW) signals are generated by a microwave generator (MWG), whose architecture vary from fractional-N synthesizers [34] to multiphase local oscillators [35]. The induction currents generated by the MWG are then led into an microwave-launching structure such that microwave fields are induced. The shapes of traditional microwave-launching structures vary widely from straight wires [8] [36], metal loops [37] and multi-loop coils [19]. However, the former two implementations may suffer from low homogeneity area coverage and poor power-delivery efficiency, which result in low ODMR contrast and excessive heat dissipation respectively [13].

The latter solves these performance constraints by integrating the multi-loop coils onto the chip. Because of this a high magnitude of the microwave field onto the NV centers can be realized without the need of driving larger AC currents through the structure which as a result increases power-delivery efficiency. Moreover the integration of the microwave-launching structure on-chip allows for improved compatibility of the design with respect to the NV centers, an example of which is the possibility of the multi-loop coil to enclose the entire diamond region of interest, consequently increasing microwave field uniformity.

3

Programme of Requirements

The fabricated chip will need to effectively detect the incoming photons from the NV-centers and send information to an external device which can then store the amount of photons detected at each frequency for each SPAD. The chip has several requirements it should adhere to. Firstly, the requirements for the complete chip are listed as follows:

- **Fabrication Technology** – The chip shall be fabricated using TSMC 40-nm technology with a total of seven metal layers used for routing at different heights;
- **Area** – The chip area should be 1.085mm x 1.085mm based on the chip of the previous BAP group with a tolerance of ± 0.25mm [11];
- **I/O pins** – No more than 32 input/output pins shall be used;
- **Sealing** – No sealing should be applied on-top of the chip.

For the SPAD-array and its SPAD-circuits the following requirements are listed:

- **SPAD size** – The width of the SPAD-cell should be between 24 and 32 μm;
- **Hold-off circuit** – The hold-off circuit connected to a SPAD-cell must be configurable off-chip;
- **Quenching** – The quenching process should be performed actively;
- **Counter** – The counter must be able to count to 1 million detected photons and should be able to detect overflow;
- **SPAD-row** – Each SPAD-row must contain 16 SPAD-pixels and a single PISO shift register;
- **SPAD-array** – The complete SPAD-array must contain 16 SPAD-rows;
- **Scalability** – The SPAD-array architecture must be designed in a way so more SPAD-pixels can be added to the design without the need of redrawing all parts.

4

Design Overview

4.1. Introduction

The design of the integrated circuit can be structured as a semi-scalable design. The scalable part of the design is the SPAD-array, which serves as the main measurement device for sensing red photoluminescence. The array comprises non-scalable SPAD pixels, each consisting of a SPAD-cell and its complementary circuit. Only part of the complementary circuit is unique inside a SPAD-row, making this the only non-scalable part of the design. In this chapter, an overview of the semi-scalable design, will be discussed in detail, focusing on the connections of the signal paths and the internal communication within the design. The discussion begins with the lowest hierarchical component in the design, which is the SPAD-pixel, followed up by the SPAD-row and concludes with the total view of the complete SPAD-array. A more in-depth discussion is covered in chapter 5 and chapter 6.

4.2. Scalable design

One of the requirements mentioned in chapter 3 is the scalability of the proposed photon-detecting SPAD-array design. The importance of this requirement lies in the fact that, for testing purposes, the tape-out will include a limited number of SPADs, whereas the final product will feature a significantly larger number of SPADs on-chip for larger producible images. The authors will discuss this scalable design in a bottom-up hierarchical fashion.

The lowest hierarchical level in the design is the SPAD-pixel, shown in Figure 4.1. The SPAD-pixel contains the SPAD-cell itself, the supporting SPAD-circuit, and the counter. The SPAD-cell reacts to photons by generating a macroscopic, sensible current, which is output to the SPAD-circuit. The SPAD-circuit then stabilizes this incoming signal from the SPAD-cell into a logical '1' or '0'. Additionally, the SPAD-circuit controls the SPAD-cell by resetting or holding the SPAD-cell of for a period off time (as explained in subsection 2.3.1). The digitalized signal is connected to the counter, which counts until the 21st bit. The counter only counts when the enable signal is high and the reset signal is low. The SPAD-circuit is controlled by the $setting$ bit stream to determine its hold-off time (also explained in subsection 2.3.1). Furthermore, the SPAD-cell is connected to a V_{bias} source, which is used to set the SPAD-voltage to near the breakdown point. The photon-sensing ability of the SPAD-pixel is therefore key to optimizing imaging resolution.

The next level in the hierarchy is the SPAD-row illustrated in Figure 4.2. The SPAD-row consists of 16 SPAD-pixels arranged in a row, along with a PISO unit. The function of the PISO is to connect the photon count data from all SPADs in the row to a single I/O pin of the chip. The PISO sends information from the counters of each SPAD-pixel using a bit-shifting method to an external device e.g. a FPGA or micro-controller. Upon completion of the data transfer from one SPAD, the PISO selects a new SPAD-pixel using the $SubSelect$ signal, and the cycle repeats until data from all SPADs have been processed. The reading sequence is initiated off-chip with the $read$ signal, and the PISO will send a $Valid$ bit to the off-chip readout components, indicating that all information from a complete array read cycle has been sent.

The next level in the hierarchy is the SPAD-array, which is situated at the apex of the design hierarchy. An overview of the design is shown in Figure 4.3. The SPAD-array contains 16 SPAD-rows and logical AND gates for the valid bits. The SPAD-array provides insight into how much area the proposed design will occupy for a 16 x 16 SPAD array, as well as the number of I/O pins required. The required amount of I/O pins for a SPAD-array independent of the amount of SPAD rows is 13. The *hold-off* takes 4 I/O pins and the tuning voltage takes a single I/O pin, resulting in 5 out of 13 I/O pins used for tuning.

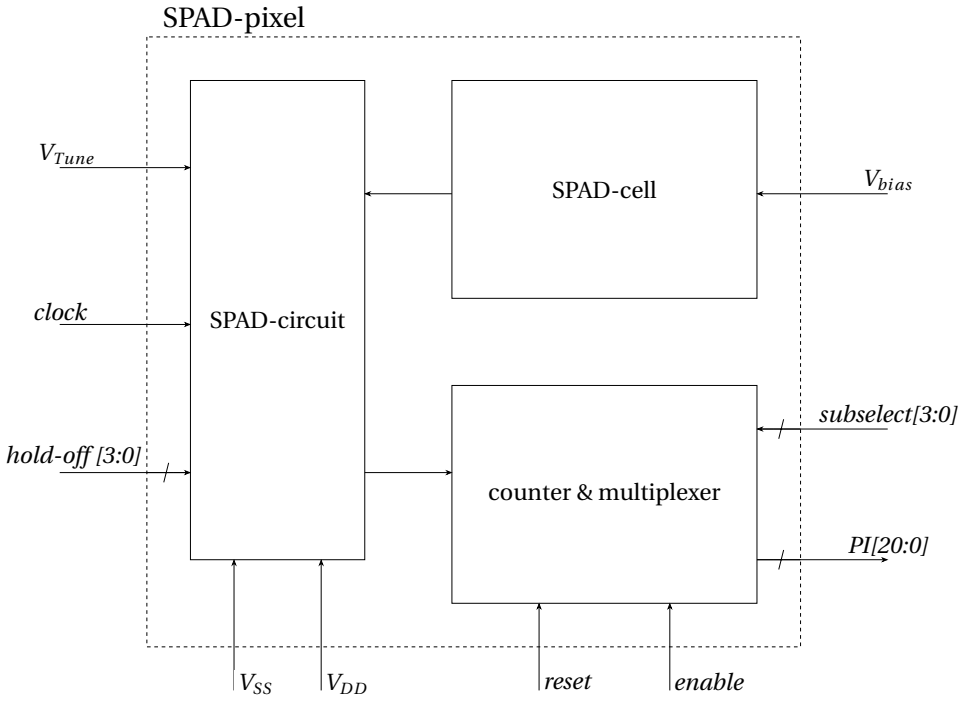

Figure 4.1: **Layout of SPAD-pixel.** The SPAD-pixel consists of the SPAD-cell, the SPAD-circuit and the counter & multiplexer complex. Additionally, the signals to and out of the SPAD-pixel are also illustrated.

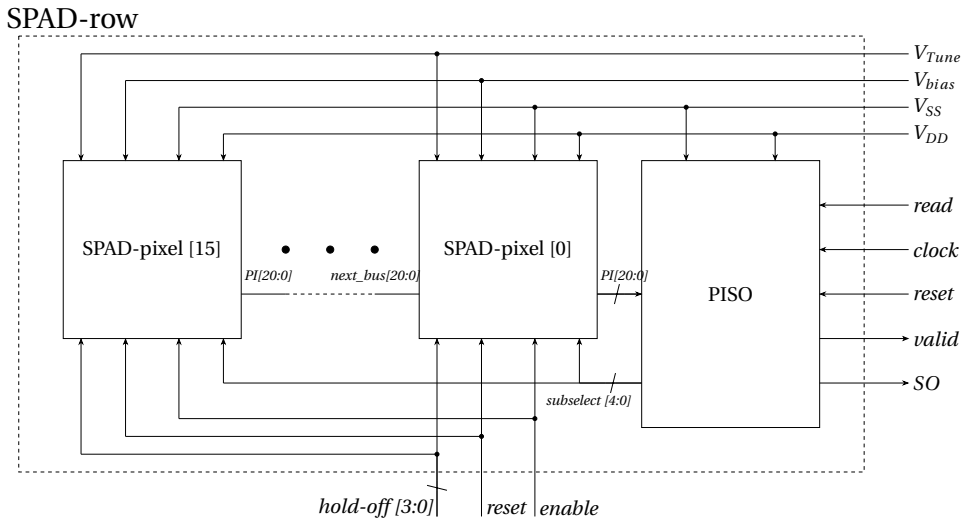

Figure 4.2: **Layout of SPAD-row.** The SPAD-row consists of the 16 SPAD-pixels and PISO. Additionally, the signals to and out of the SPAD-row are also illustrated.

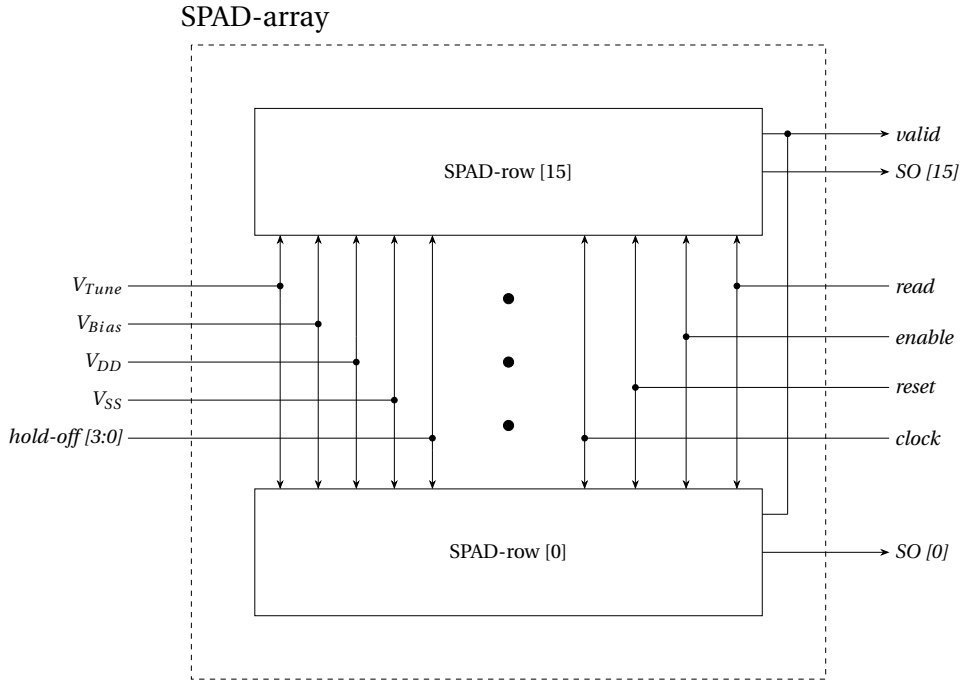

Figure 4.3: **Layout of SPAD-array.** The SPAD-array consists of the 16 SPAD-rows. Additionally, the signals to and out of the SPAD-array are also illustrated.

5

SPAD-PIXEL

5.1. INTRODUCTION

The sensing and evaluation of the number of detected photons is performed by the SPAD-pixel. A SPAD-pixel consists first of a SPAD-cell, which comprises only the doping regions and metal pins. It also contains a complementary SPAD-circuit, which is responsible for ensuring proper sensing operation through the quenching and recharging of the SPAD. The final components of the SPAD-pixel are the counter and multiplexer. The counter registers the number of avalanche peaks, which represent photon events detected by the SPAD circuit, while the multiplexer is used for further control and for sending the information via the PISO, which is part of the SPAD-row as further explained in chapter 6. A block diagram of the SPAD-pixel is illustrated in Figure 5.1.

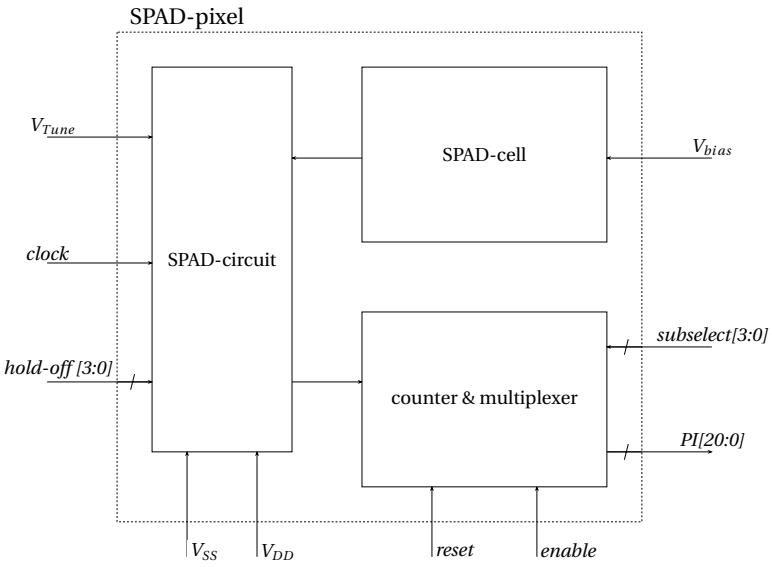

Figure 5.1: **Block diagram of the SPAD-pixel**. The SPAD pixel contains three modules and 10 signal pins of which three are bit-vectors. The SPAD-cell sends analog signals to the SPAD-circuit where they are converted to digital signals and sent to the counter & multiplexer. The counter & multiplexer send the total count to the PISO depending on the value of $subselect$.

5.2. SPAD-CELL

The SPAD-cell is the component responsible for absorbing photons and producing tangible indications of the detection of said photons, which for SPADs are rising edges of avalanches. The SPAD-cell contains the doping region structure and metal wires connecting the SPADs anode and cathode to other components. It is important that the Anode region is in direct contact with air, and that no oxide is placed on top or metal wires are placed above the SPAD with a width larger than 400 nm. Otherwise, a smaller fraction of photons will land on the P+ region and therefore trigger an avalanche [13]. The layout of our design is based on the architectures presented by Perenzoni [38] and is also discussed in the master's thesis of Aliberti [39]. A new SPAD-cell was designed as the design of the previous BAP group deviated from that of an actual SPAD-cell layout, as it was missing any type of well below the Anode region [11]. The newly developed design additionally uses an octagonal structure to meet the constraints of the standard fabrication technology used and to provide a better distributed current flow than that of a square SPAD [40]. The new SPAD layout can be seen in Figure 5.2, where the left image presents a top-down view and the right image shows a cross-sectional view of the same SPAD. The dimensions of the SPAD are based on the designs from the previous BAP group [11]. The active sensing area is 12 µm, the total width is 24 µm and the shortest distance between Cathode and Anode regions is 3.6 µm. The total area occupied by the SPAD cell is approximately 12.96 µm^2.

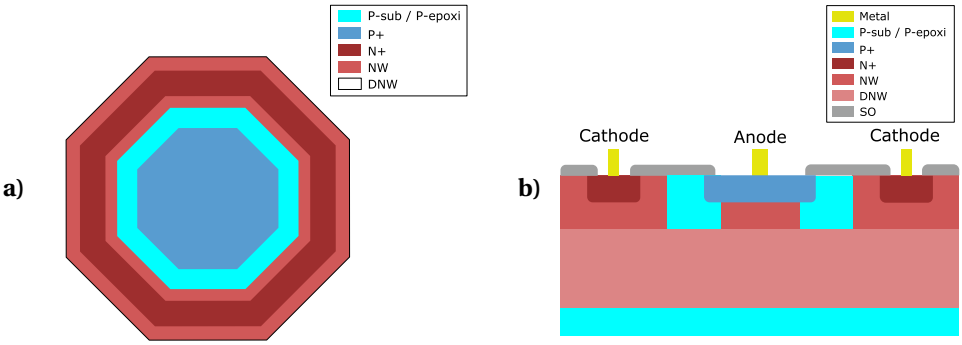

Figure 5.2: **Layout of the SPADs doping regions (a)** Top-view of the SPAD. The SPAD shown is an octagonal SPAD, where the OD region indicates where oxide is diffused, and P+ and N+ can be placed along with metal contacts, if used. In this figure, it can be seen that the inner area contains the P+ region, which is the active region of the SPAD and therefore functions as the anode. **(b)** Cross-section of the SPAD. The SPAD contains seven distinct regions. This layout creates a depletion region between the P+ and the connecting NW region. If a photon landed on the P+ region, it allows an electron flow to take place through the N-type region to the cathode, and a hole flow in the other direction.

5.3. SPAD-CIRCUIT

The SPAD-circuit consists of three separately designed components: the sensing entity, the quenching & recharge circuit, and finally the control circuit. All these components are required to have a clearly defined '1' or '0' as output to indicate whether or not a photon has been detected. The circuit should also stabilize and recharge the SPAD-cell, as explained in section 2.3. In the proposed design the area, that the SPAD-circuit covers is roughly 50x25 μm^2.

5.3.1. SENSING

The sensing entity consists of a Voltage Controlled Resistor (VCR) and a Schmitt-trigger. The VCR is used to transform the avalanche current into a voltage that is readable by the Schmitt-trigger. A VCR is chosen instead of a regular resistor since the exact optimal resistive value could not be determined, which justifies the choice of a tunable resistance. The ability to tune the resistance of the VCR, however, comes at the cost of an I/O pin. The VCR is a simple NMOS transistor connected to ground, as illustrated in Figure 5.3a.

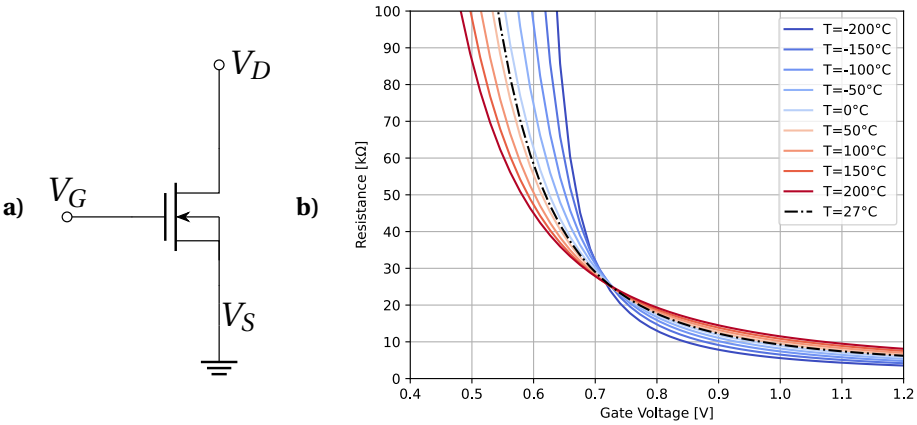

Figure 5.3: **Voltage Controlled Resistor (VCR) design and simulations. (a)** Schematic of a VCR. The VCR is an NMOS transistor where the gate voltage is tuned to specify the resistance. The bulk is connected to the source voltage, while the drain is connected to the sensing node, which in this application is the SPAD anode. **(b)** Simulations of a VCR with the resistance plotted against the gate voltage. The VCR is simulated with Spectre from temperatures -200 to 200 °C in steps of 50. The width and length of the transistor are 600 nm and 240 nm, respectively. The gate voltage is swept from 0.4 to 1.2 V, and the resistance is shown on the y-axis in kΩ. Additionally, the R-V curve at room temperature is plotted with a dashed black line.

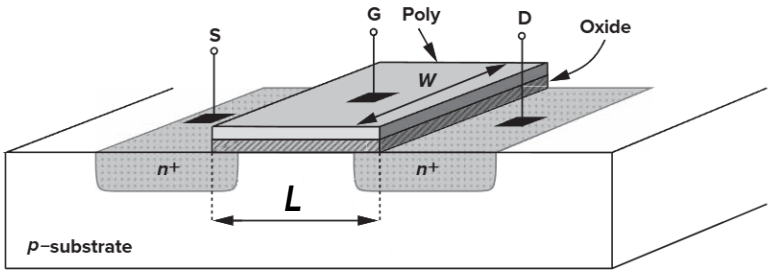

Figure 5.4: **Dimensions of an NMOS transistor**. W and L are defined as the width and length of the poly-gate of the NMOS transistor respectively. Adapted from [41].

The gate is connected to an I/O pin called V_{Tune} in the schematic. The resistive value of the NMOS transistor depends on its length, width, gate voltage, and temperature [41]. The equation for the resistance is shown in Equation 5.1.

$$R = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)} \tag{5.1}$$

where μ_n is the mobility of electrons in cm^2/V-s, C_{ox} the oxide capacitance in F/cm^2, W and L the width and length of the poly-gate of the NMOS in cm respectively, as illustrated in Figure 5.4, V_{GS} the gate-to-source voltage in V and finally V_T the threshold voltage in V.

From literature, it was found that most SPADs in this configuration have a resistor with values ranging from 10 kΩ to 100 kΩ [42]. In order for the VCR to cover these ranges of resistance values, the length was set to the maximum possible value and the width to the minimum possible value determined by the fabrication technology. A simulation of the resistive values at different temperatures and gate voltages is shown in Figure 5.3b. The tested model has a width of 0.6 µm and a length of 0.24 µm. These values are the maximum and minimum values allowed by the fabrication technology and are plotted with a constant drain-to-source voltage of 1.2 V and a gate voltage swept from 0.4 to 1.2 V. The simulation is tested with different temperatures since the threshold voltage depends on the operating temperature [41]. From the plot, it can be observed that the lower resistive values of 10 kΩ to 50 kΩ are easily tunable, whereas the 60 kΩ and 100 kΩ values are more dependent on changes in temperature than changes in the gate voltage. This means that the resistive values become unreliable based on the gate voltage at higher resistances. Therefore, it is taken into account that measurements of the resistance of an NMOS during operation should be made possible.

The Schmitt-trigger is chosen for sensing the anode voltage that arises due to the voltage drop across the VCR, owing to its reliable output values and quick response time [43], and by the recommendation of the previous BAP group [11]. A conventional Schmitt-trigger was selected due to the short duration of this project and premature familiarity with chip design and its associated software. The conventional schematic of the Schmitt-trigger made from CMOS transistors is shown in Figure 5.5.

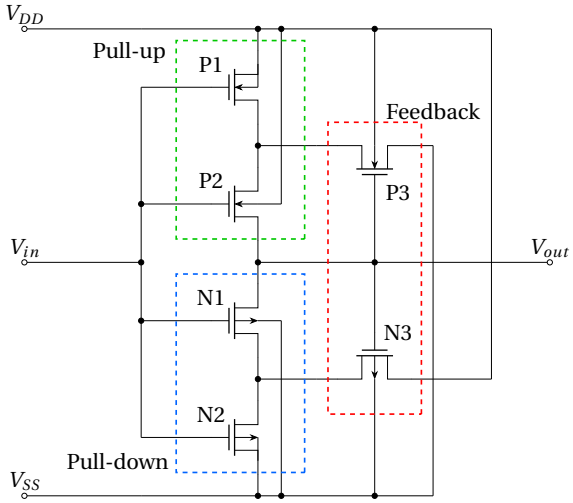

Figure 5.5: **Schematic of the conventional Schmitt-trigger**. The Schmitt-trigger schematic is based on the design by Baltes et al. [43]. The transistors labeled N are NMOS transistors, and those labeled P are PMOS transistors. The Schmitt-trigger has three distinct regions. The pull-up network, indicated by the green box, is responsible for pulling the output voltage to V_{DD}; the pull-down network, indicated by the blue box, pulls the output voltage to V_{SS}; and the feedback network, indicated by the red box, determines the transitions based on the output and input voltages. The output of the Schmitt-trigger is an inverted version of the input voltage.

The Schmitt-trigger is simulated in two different aspects: one where the delay is simulated, and the other where the hysteresis is simulated. Both simulations are shown in Figure 5.6 where the delay is shown in Figure 5.6a and the hysteresis is shown in Figure 5.6b. Both simulations are tested with different design considerations: one where the design uses the default width and length parameters of the transistors from the fabrication technology, and another where the PMOS transistors are of sizes $W = 3 \cdot W_{def}$ and $n = 2 \cdot n_{def}$. Increasing the PMOS sizes creates a stronger pull-up strength, which is then roughly the same as the pull-down strength. An increase in pull strength will decrease the delay of Schmitt-trigger. These time delays of rise (t_r) and fall (t_f) can be seen in Figure 5.6a. The delay of the optimized version is roughly 500 ps for both t_r and t_f, while the non-optimized version has a t_r of nearly 2 ns, which is a large delay in the context of sensing photon detections with SPADs. In addition to the delay times, the hysteresis is also simulated to determine the threshold voltages at which the Schmitt-trigger switches from high to low and vice versa. These points are called the Low-to-High voltage (V_{LH}) and the High-to-Low Voltage (V_{HL}). From simulation the following values are obtained: $V_{HL} = 0.76$ V and $V_{LH} = 0.44$ V for the larger PMOS design. This High-to-Low voltage can be lowered by changing the design to a voltage tunable Schmitt-trigger [44]. This design includes an NMOS transistor connected to a voltage source, which can change the threshold voltages to a certain degree. However, the design would require an additional I/O pin and was therefore not chosen for this project, as the VCR should already be able to tune the excess voltage to be above the V_{HL} value. Adding the sensing circuit to the SPAD results in the schematic shown in Figure 5.7.

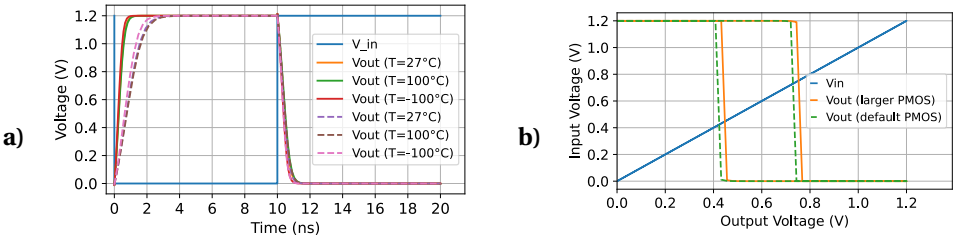

Figure 5.6: **Simulations of the conventional Schmitt-trigger.** **(a)** Timing delay simulation. The two designs are simulated with a transient simulation from 0 to 20 ns. The design with default PMOS transistors is plotted with dashed lines. **(b)** Hysteresis simulation. The two designs are simulated with a DC hysteresis sweep. The default-sized design is plotted with a dashed line. The hysteresis sweep also includes the input voltage to show the transition voltages.

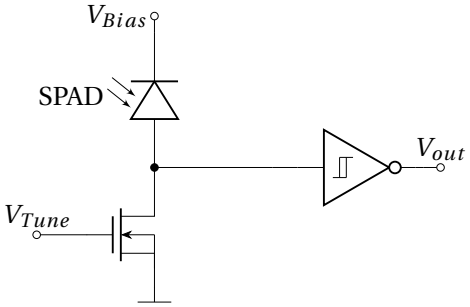

Figure 5.7: **Schematic of the SPAD together with the sensing entity.** The schematic contains the SPAD connected to V_{bias} at the cathode and the sensing circuit at its anode. The input of the sensing circuit is the Tuning voltage (V_{Tune}) with the output being the output voltage of the sensing entity (V_{out}).

5.3.2. QUENCHING AND RECHARGE

The quenching and recharging of the SPAD are needed to reset the SPAD back to a photon-sensing state, as explained in subsection 2.3.2. Introducing a hold-off time before the recharging phase allows minimization of after-pulsing effects as well as increased reliability. Quenching connects the metal wires attached to the Schmitt-trigger and anode side of the SPAD to V_{DD}, effectively keeping a high input signal for the Schmitt-trigger and lowering the voltage drop across the SPAD below the breakdown voltage, as shown in Figure 2.3. During recharging, both the Schmitt-trigger input and, in turn, the anode side of the SPAD are connected to V_{SS}. This resets the Schmitt-trigger to indicate that a new sensing cycle has been initiated and the SPAD-voltage has been set to above the breakdown voltage to V_{Bias}. After recharging, the V_{SS} connection to the anode of the SPAD is closed and the circuit is ready for a new photon detection. The quenching and recharge connections are implemented by a PMOS and NMOS transistor, respectively, and are controlled by the control circuit discussed in the next subsection. The NMOS and PMOS transistors with their control signals are added to the schematic illustrated in Figure 5.8.

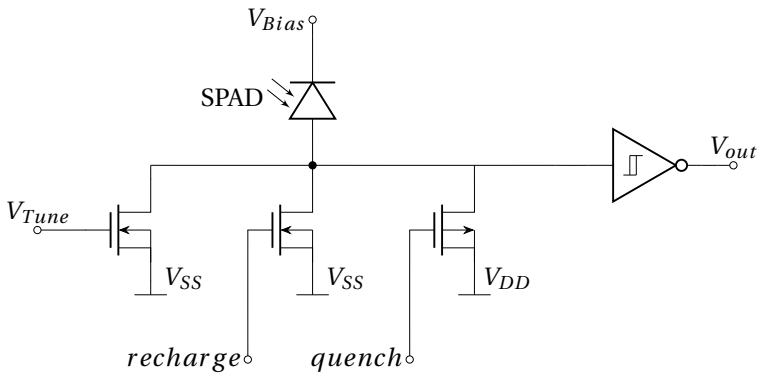

Figure 5.8: **Schematic of the SPAD with sensing entity and quenching and recharge transistors**. The SPAD is connected to V_{Bias} at the cathode. The anode is connected to the sensing entity and the quenching and recharge transistors. The quenching transistor is a PMOS used to pull the voltage at the anode up to V_{DD}, and the recharge transistor is an NMOS used to pull the voltage down to V_{SS} for recharging. The inputs are now the bias voltage (V_{Bias}), the tuning voltage (V_{Tune}), and the signals $recharge$ and $quench$. The output is still the output of the Schmitt-trigger (V_{out}).

5.3.3. CONTROL CIRCUIT

The control circuit is used to control the *recharge* and *quenching* signals based on the output value of the Schmitt-trigger. A low output at the Schmitt-trigger means that a photon has been absorbed by the SPAD and triggered an avalanche. The moment the Schmitt-trigger changes to this low value, the control circuit will immediately indicate that the circuit should quench the SPAD. This is done by changing the *quench* signal from high to low, as quenching is turned off for high signals because a PMOS transistor is used. A low value will turn on the PMOS transistor and connect the SPAD's anode to V_{DD}. Afterwards, the control circuit initiates the hold-off mechanism discussed in subsection 2.3.2. This hold-off scheme is based upon that of Deng et al. and Xu et al. [45][32]. The control circuit receives a clock signal and a hold-off setting bit-vector of 4 bits. Depending on the clock frequency, the hold-off time can be tuned from 0 to 15 times the clock period. After the hold-off time has expired, the *quench* signal and the *recharge* signal are set to a logical high. This will turn off the connection to V_{DD} and turn on the connection to V_{SS}. By turning on this connection, the SPAD-voltage above the breakdown voltage is restored, and the Schmitt-trigger output value returns to high. A high output of the Schmitt-trigger will reset the control circuit, effectively setting the value of *recharge* low, disconnecting the anode from V_{SS}, and preparing the SPAD circuit for a new photon detection. The schematic is shown in Figure 5.9 where the complete SPAD-circuit is now presented. In Figure 5.10, a simulation is shown of the signal inputs and outputs of the circuit with two different hold-off settings and an estimation of when the Schmitt-trigger output changes to high after the recharge has initiated.

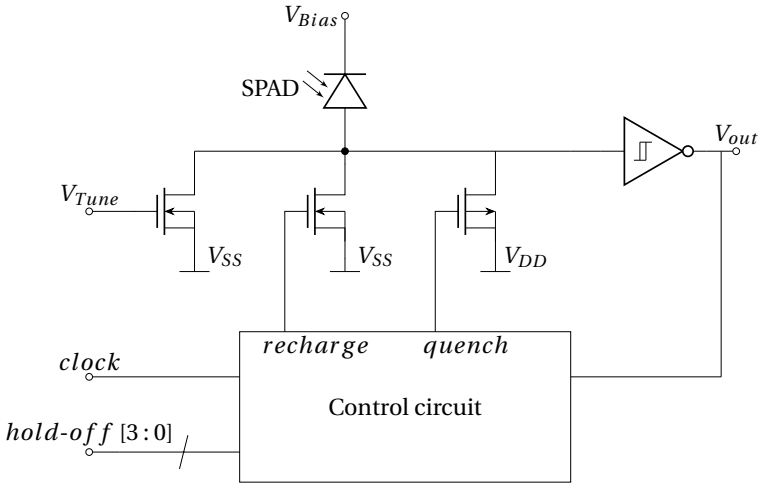

Figure 5.9: **Schematic of SPAD circuit.** The added control circuit regulates at which moments and how long the anode voltage of the SPAD should be connected to V_{DD} and V_{SS}.

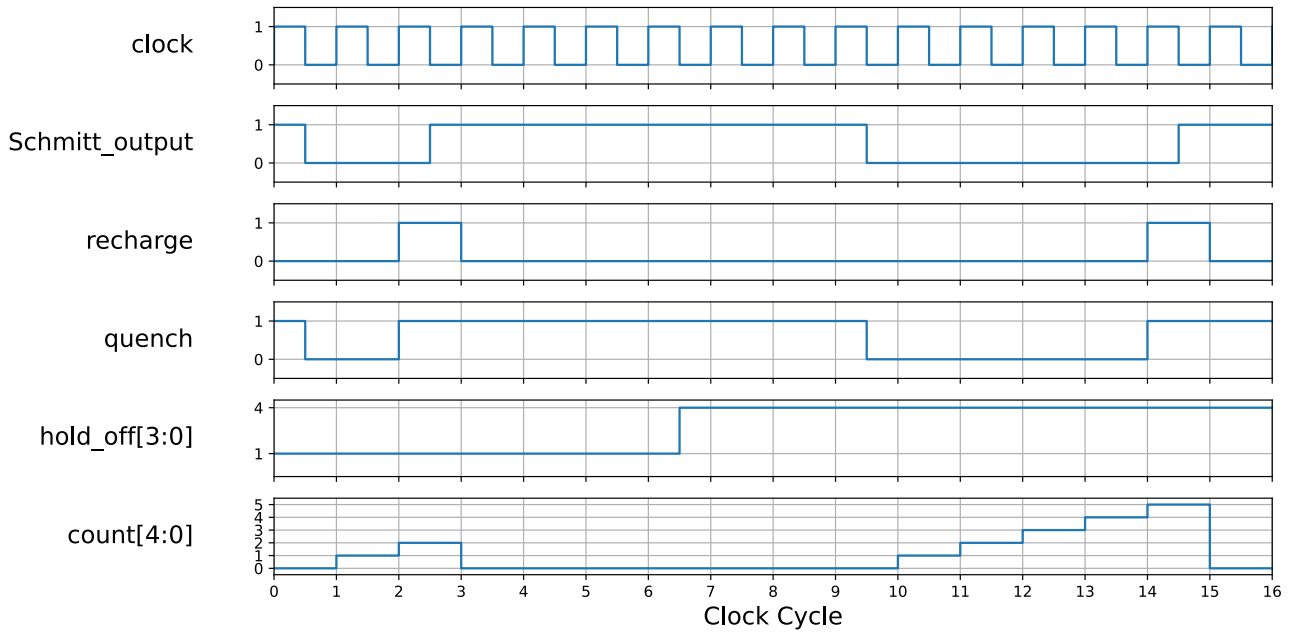

Figure 5.10: **Simulation of the SPAD-circuit**. The SPAD-circuit has been simulated with ModelSim with two different hold-off settings. The first setting is of value 1 and runs from cycle 0 to 6.5. The second setting is of value 4 and runs from cycle 6.5 to 16. From these two settings the difference in hold-off time can be observed and the behavior of quenching and recharge signals can be validated.

5.4. COUNTER & MULTIPLEXER

The last module needed for the SPAD-pixel is the counter and the multiplexer. The counter is used to count the amount of photons detected, which are the digitalized versions of the analog signals from the SPAD-cell. The counter does not use any clocks and works with the output from the Schmitt-trigger and counts every change from low to high. The counter is sized to 21 bits to count at least 1 million photons in a second conforming to the requirements set in chapter 3. The 21st bit is added as a safety feature to indicate when the counter has overflowed and an error has occurred. Other signals to the counter are the *enable* and *reset* signals. These signals are responsible for enabling and resetting the counter. The *enable* signal will be pulled low when the counter should stop counting but keep its value. The reset signal is pulled high when the counter is disabled and the value should be set to 0.

The multiplexer is used to communicate with the PISO. The multiplexer has connections to the PISO, to the next SPAD-pixel, and the *subselect* bit-vector. The multiplexer will either connect the wires from the counter of the next SPAD, further called *next_bus*, to *PI*, or the count bus to *PI*. This is done at every SPAD-pixel and each has their own *subselect* value for which the multiplexer connects the count bus to *PI*. The only SPAD-pixel where no multiplexer is used is the SPAD at the furthest end from the PISO module. A schematic of how the structure connects is shown in Figure 5.11. This design is chosen to decrease the amount of wires flown throughout the chip, as will be discussed in chapter 6.

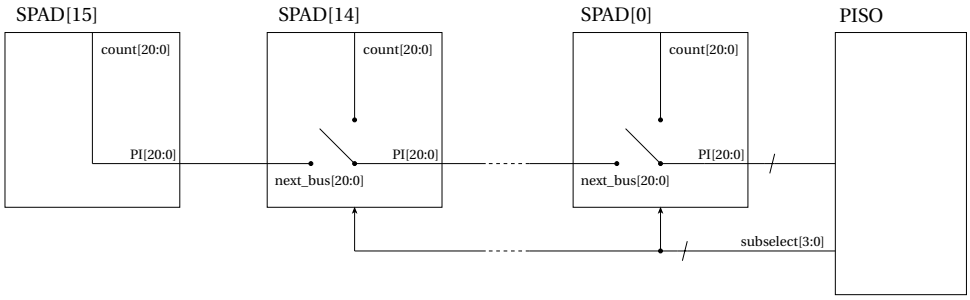

Figure 5.11: **Block scheme of the multiplexer structure**. The SPADs are connected via the multiplexer to each other via the lines between *PI* and *next_bus* and to the PISO. Depending on the value of *subselect*, the multiplexer will either connect the *PI* of the SPAD-pixel to *count* or *next_bus*.

6

SPAD-ARRAY

The SPAD-array consists of 16 SPAD-rows, where each SPAD-row consists of 16 SPAD-pixels. There are two different configurations of the SPAD-row: the left-sided and the right-sided version. The left-sided version has the PISO module at the leftmost side, and the right-sided version at the rightmost side. Each SPAD-row outputs the photon count data of all 16 SPAD-pixels, which is handled by the PISO, through a single output bit stream. The total area size taken up by all necessary components totals approximately 1050 by 1050 µm without the I/O ring. The distance between the centers of two SPAD-pixels is 55 µm, therefore the area of a single SPAD-pixel is by definition 55 by 55 µm. The SPAD-array layout is shown in Figure 6.1. This layout contains 256 SPAD-pixels and 16 SPAD-rows, where each SPAD-pixel in a row is connected as explained in section 5.4.

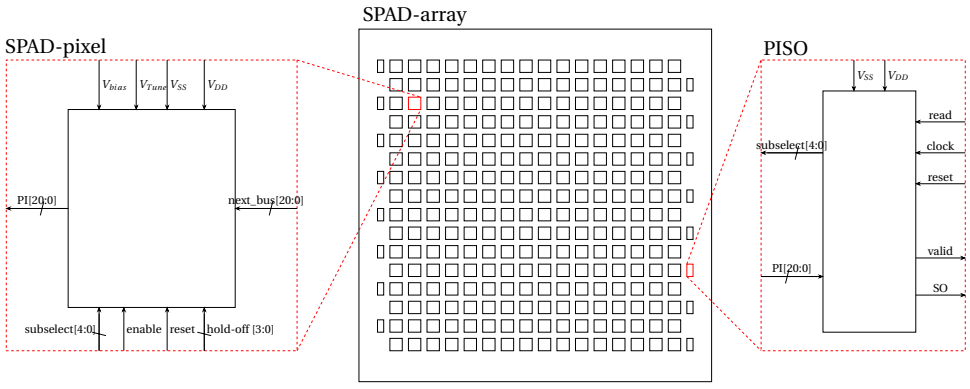

Figure 6.1: **Overview of the SPAD-array**. The SPAD-array consists of 16x16 SPAD-pixels where each row is connected to a PISO. The two components visible are the SPAD-pixel, highlighted on the left, and the PISO, highlighted on the right. Both components show the connections needed with the corresponding on-chip direction.

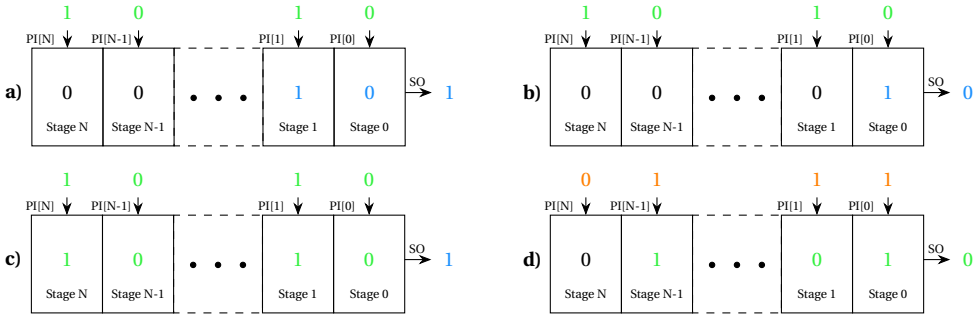

Figure 6.2: **Working principle of the PISO during the reading state.** The stages are labeled according to the positional value of the bit that is stored inside each stage, with the leftmost stage labeled N and the rightmost stage 0. Each stage represents a memory module which stores either a bit directly loaded from the *PI* input or one shifted from a previous stage, and shifts its stored value forward to the next stage at the positive edge of the following clock cycle. The shifting process occurs from left to right, meaning that upon starting the reading process, the least-significant bit of the *PI* gets output to *SO* first, since it is stored immediately in Stage 0, and zeros are shifted in from the left. **a)** The final two stages, Stages 1 and 0, contain bits, depicted in blue, that were loaded inside the PISO previously. Count data from another SPAD, the bits of which are depicted in green, make up the *PI* input. The shift register is in the midst of processing the blue bits and therefore does not load in the new data yet. **b)** Only Stage 0 contains a relevant bit from the blue data. The PISO prepares to immediately load the new (green) data during the next clock cycle. **c)** The final bit from the blue data is output. During this process, the new data is loaded into the shift register. **d)** The PISO processes the green bits, while data from another SPAD, whose bits are depicted here in orange, are at the input *PI*. Only when all green bits are shifted to the output *SO* are the orange bits loaded inside the shift register.

6.1. PISO

As mentioned in Chapter 3, the PISO will perform parallel-to-serial data conversion of the 16 SPAD-pixels interlinked in each SPAD row. Each SPAD-pixel outputs a 21-bit vector as shown in Figure 4.2, meaning a total of $16 \cdot 21 = 336$ bits in each row requires processing during each read cycle. The PISO processes these 336 bits in an alternating fashion, where one SPAD-pixel at a time outputs its contents to the input of the PISO through a bus. This data bitstream can be controlled through the $subselect$ signal, which puts a logical high on the desired SPAD-pixel and a logical low on all other pixels.

Outputting data serially from a parallel input in this PISO is based largely on a bit-shifting procedure. During the inactive phase of the PISO when the *Read* signal becomes high, a read cycle is initiated throughout which the PISO is irresponsive to any other *Read* signals. The photon count of a SPAD is inputted into the PISO in the form of a N-bit vector, where each bit is stored in their respective stages according to their positional value as illustrated in Figure 6.2. On the rising edge of the clock a logical shift right operation is performed to the stored bits, in which the least-significant bit (LSB) stored in Stage 0 is outputted and a zero is shifted into stage N. After N clock cycles the photon count from another SPAD is loaded into the PISO and the shifting process repeats again until data from all SPADs have been processed.

Upon completion of the parallel-to-serial conversion the PISO returns to an inactive state where a high $Valid$ signal is outputted to indicate the successful completion and readiness for another read cycle. The PISO design has been validated using a Model-

Sim simulation, which is illustrated in Figure A.1 in Appendix A. Alternatively, a 336-bit PISO shift register may also be proposed. However, despite its simplicity the penalty of increased chip area coverage goes against the principle of efficient area usage and therefore this idea has been disregarded and further explained in the next section.

6.2. SPAD-ROW

As discussed at the beginning of this chapter, the SPAD-rows within the SPAD-array must meet the requirement of scalability. There are two types of SPAD-rows, both of which contain the same components. The only difference lies in the location of the PISO module and, consequently, the orientation of the internal wire paths that connect the SPAD-pixels. Due to I/O pin constraints it is necessary to support both left- and right-oriented I/O pins for reading the counter values. The connections between the SPADs and the PISO are illustrated in Figure 6.3. The two SPAD-row configurations are also shown: the right-sided version in Figure 6.3a and the left-sided version in Figure 6.3b. The use of SPAD-rows facilitates a modular and easily expandable design. This approach allows for the integration of more SPAD-pixels without requiring a redesign of each individual cell. Only the $subselect$ bus width and the number of multiplexer units per SPAD-pixel need to be adjusted.

The PISO is connected to the SPADs through a bus called PI[20:0], which directly interfaces with the multiplexer of the nearest SPAD. Depending on the value of $subselect$ the multiplexer either connects the output of the SPAD's own counter or that of the next SPAD in the row. This is determined by comparing the $subselect$ value with the SPAD's index number. This configuration is preferred over connecting all SPADs directly to the PISO, which would require a number of wires proportional to the number of SPADs, which is not at all scalable and consumes excessive chip area. Such a method is not viable for large-scale designs. The internal and external signals of the SPAD-row are summarized in Table 6.1.

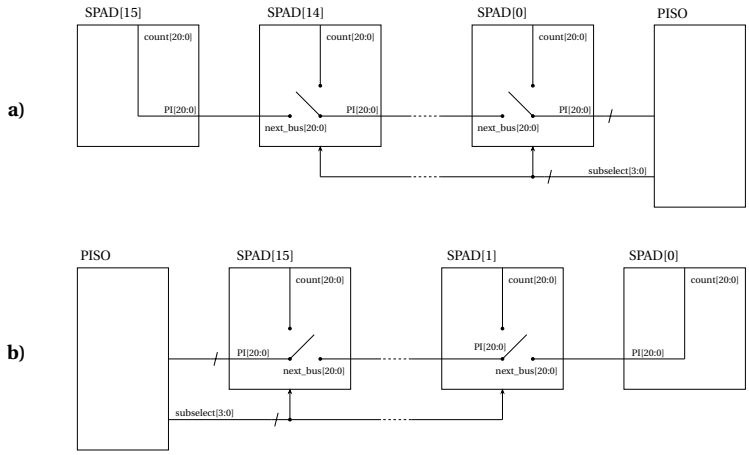

Figure 6.3: **Overview of the two SPAD-row orientations. a)** Right-oriented SPAD-row. The PISO is located on the right side, and the left-most SPAD-pixel does not include a multiplexer. **b)** Left-oriented SPAD-row. The PISO module is located on the left side, and the right-most SPAD-pixel does not include a multiplexer. In both configurations, the SPAD-pixels are numbered from 15 on the left to 0 on the right, maintaining consistent indexing regardless of orientation.

Table 6.1: **Internal and external signals of the SPAD-row**.

Signals	**Internal/ external**	**Size**	**Description**
V_{DD}	external	1	The power supply
V_{SS}	external	1	The ground source
V_{Bias}	external	1	The voltage supply used to bias the SPAD-cells
V_{Tune}	external	1	The voltage supply used to set the VCR of the SPAD-pixel
clock	external	1	The clock signal provided externally
SO	external	1	The output signal from the PISO module
enable	external	1	The signal used to enable the counters of the SPAD-pixels
reset	external	1	The reset signal used by the counters and the PISO module
read	external	1	The signal to start the reading sequence
valid	external	1	The signal to indicate a complete readout
hold-off	external	4	The bus signal used to determine the length of thehold-off time for the SPAD-pixels
PI	internal	21	The bus wires used to connect the PISO to the nearest SPAD-pixels
next_bus	internal	21	The bus wires placed between SPAD-pixels to connect them into a single row
subselect	internal	4	The bus signal used to determine which SPAD-pixel outputs its data to the PISO

7

PROPOSED TAPE-OUT

The proposed design for fabrication utilizes 32 I/O pins to support both the SPAD-array and the testing of the SPAD-cell and SPAD-circuit. The I/O ring for the chip is designed with the same components as those employed in the previous tape-out, which was part of an earlier iteration of the previous BAP project [11]. The current design integrates both the SPAD-array and a dedicated SPAD-testing module, the latter of which will be discussed later in this chapter. A pin-out diagram of the proposed tape-out is shown in Figure 7.1. The total chip-area measures 1.32mm by 1.32mm. The full layout of the chip, including the 16×16 SPAD array, the testing circuit, and all necessary interconnections, both internal and to the I/O ring, is shown in Figure 7.2.

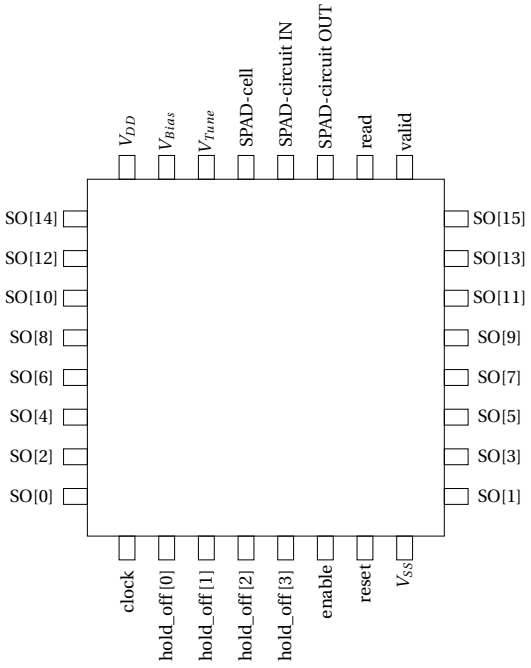

Figure 7.1: **Pin-out diagram of the proposed design.** The chip contains a total of 32 I/O pins, 3 of which are for testing purposes and 2 are ground and power pins. 27 are used by the SPAD-array of which 16 are SO pins.

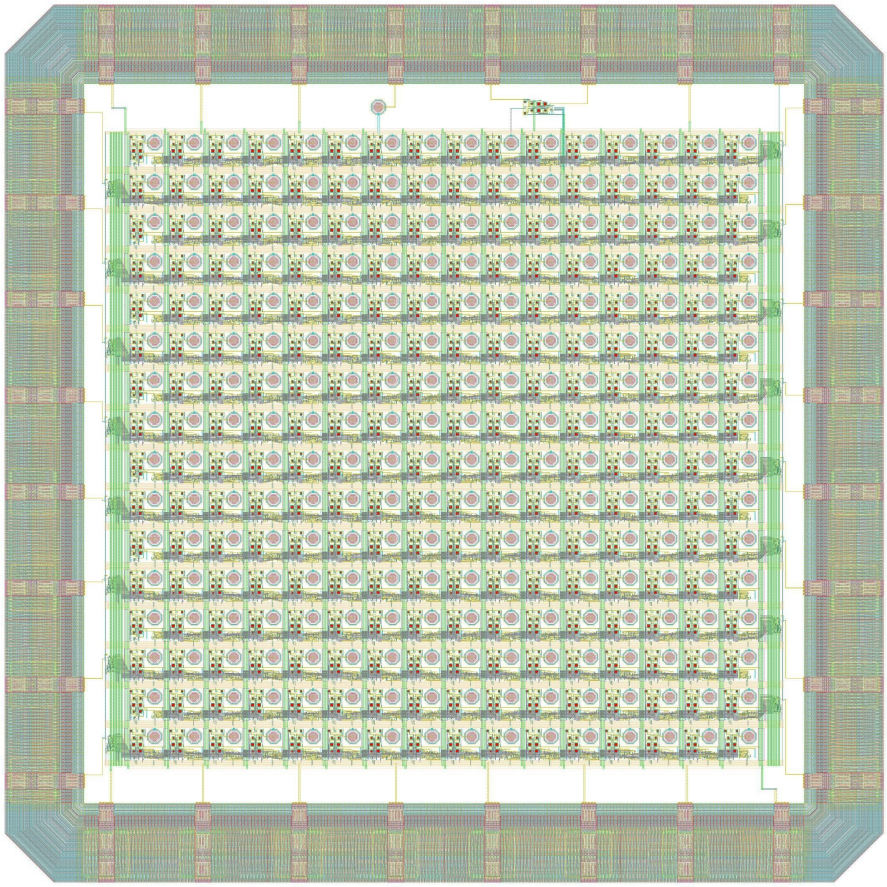

Figure 7.2: **Proposed Chip tape-out.** The layout consists of the SPAD-array, SPAD-testing circuits and the I/O ring with all metal wire paths.

7.1. SPAD-TESTING MODULE

A single SPAD-cell and accompanying SPAD-circuit have been integrated into the chip utilizing available space at the top of the layout. This space became available due to the lateral area occupied by the PISO modules on both the right and left sides. The inclusion of these two components enables their independent validation. Figure 7.3 illustrates the connection of the SPAD-cell and SPAD-circuit to the I/O pins and other required signal and power lines.

The SPAD-cell can be tested using procedures outlined in the characterization report on the previous SPAD-chip [12]. These tests allow determination of key parameters such as the breakdown voltage, the required bias voltage, and the appropriate VCR setting to achieve the desired anode voltage during avalanches. Regardless of the operational status of the SPAD-cell, the SPAD-circuit itself can be tested independently. In the case of a non-functional SPAD-cell, an equivalent circuit can be constructed to emulate the behavior of the SPAD-cell, allowing validation of the SPAD-circuit by observing its output at *SPAD-circuit OUT*. If both modules are confirmed to function correctly, they can be interconnected via the *SPAD-cell* and *SPAD-circuit IN*. This enables combined testing of the integrated functionality. Measurements at the *SPAD-circuit IN* pin can be used to determine the SPAD-cell's excess voltage and current response during photon incidence. Additionally, propagation delays can be assessed by probing the voltages at *SPAD-circuit IN* and *SPAD-circuit OUT*. Finally, the characteristics of the VCR can be evaluated across different temperatures and tuning voltages V_{Tune} with a multimeter or LCR meter.

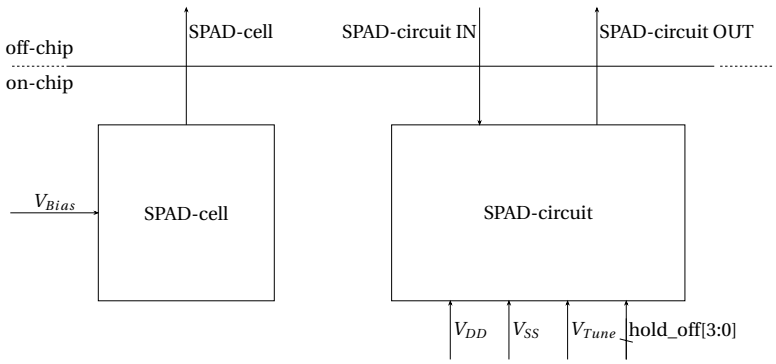

Figure 7.3: **Overview of the testing circuit.** Two dedicated modules are included for the purpose of validating individual components of the design: the SPAD-cell and the SPAD-circuit. The SPAD-cell is connected to a dedicated I/O pin labeled *SPAD-cell* and to V_{Bias}. The SPAD-circuit is interfaced through two distinct I/O pins: *SPAD-circuit IN* and *SPAD-circuit OUT*.

8

DISCUSSION

At the beginning of the project, a set of design requirements was defined, as outlined in chapter 3. These requirements guided the design process and were successfully satisfied. All modules were designed for compatibility with the TSMC 40-nm CMOS process, utilizing no more than seven metal layers. The total chip area, including the I/O ring, is 1.32 x 1.32 mm, which is within the defined bounds. Exactly 32 I/O pins were utilized, and no sealing was necessary during the I/O ring integration. Regarding SPAD-specific design criteria, the pixel size is 24 µm. The hold-off circuit supports configuration via four I/O pins, enabling 15 distinct settings. The SPAD circuit implements active quenching and recharge, fulfilling the requirement for an active quenching mechanism. Additionally, the overall design emphasizes scalability: SPAD-rows and arrays were implemented in groups of 16, matching the configuration of a previous chip, simplifying design reuse and comparative analysis.

Validation at the lowest hierarchy level was successful, confirming the functional correctness of individual components. However, validation of the complete SPAD cell, pixel, and array could not be performed, as a simulation was not possible and a full tape-out is beyond the scope of this project due to the time limitation. One significant challenge encountered early in the project was the steep learning curve associated with unfamiliar design tools and defining the design context. Technical difficulties also emerged during the design flow, specifically with transferring synthesized netlists from Innovus to Virtuoso. This limitation prevented validation of those modules within Virtuoso. Nevertheless, the hardware descriptions were functionally verified, and Innovus successfully executed internal layout-versus-schematic (LVS) checks. An additional constraint was Virtuoso's inability to simulate the SPAD-cell: simulating this would require a photonic testing integration in Virtuoso and schematic-less simulation, which were not feasible within the scope of this project. To address this, a standalone SPAD-cell was added to the design for post-fabrication testing and characterization.

Despite these challenges, the project provided valuable insights into advanced chip design workflows and highlighted areas for future improvement in tool integration and validation strategies.

9

Conclusion and Recommendations

The SPAD-array architecture proposed in this thesis represents a significant advancement over the design developed by the previous BAP group. The redesigned SPAD-cell introduces an enhanced doping region layout combined with an octagonal geometry, which allows for a better distributed current flow. A VCR has been integrated into the design to allow tunable control of the SPAD anode voltage. Moreover, a Schmitt-trigger was selected in place of a conventional comparator due to its reliable output values and faster response time, as demonstrated through simulation. The quenching and recharging are done actively through a pull-down mechanism, which can be controlled through the externally configurable control circuit allowing for a tunable hold-off time. For digital readout, each SPAD-pixel includes a 21-bit asynchronous counter capable of detecting overflows. A multiplexer facilitates data selection, and a PISO module enables serialized data transmission from each SPAD-row via a single output pin. The architecture supports a 16×16 SPAD-pixel array within a compact 1.32 × 1.32 mm chip area using 32 I/O pins. Finally, due to the layout of SPAD-pixels, The SPAD-array architecture is indeed scalable allowing for larger formats of the design to be created without large modifications. In conclusion, our designed SPAD-array architecture fulfills all requirements outlined in chapter 3 resulting in a successful completion of the project.

Several opportunities for optimization and further validation have been identified. These are recommended for future iterations of the design:

- **Dynamic Configuration** – The SPAD circuit can be improved by incorporating on-chip, per-pixel configurability of the hold-off time and VCR.
- **On-Chip MW Antenna Integration** – Future versions could benefit from integrating a microwave antenna directly on-chip, with adaptive field orientation to align with the NV-axis.
- **3D Integration for Area Optimization** – Employing 3D integration techniques (e.g. through 3D printing or stacking) could offload SPAD-cells onto a separate layer, improving area efficiency and scalability.

In addition to design optimizations, further validation is strongly advised. Full characterization of the SPAD cell, the SPAD circuit, and the complete SPAD array should be performed once the chip is fabricated. These validations will provide critical performance metrics and guide subsequent design refinements.

10

FUTURE WORK

Building on the recommendations of the previous chapter, four key directions are proposed for the future development. These directions aim to enhance the design in terms of area, scalability, performance, and system integration. The proposed areas of improvement are as follows:

- **Dynamic Configuration of the Hold-Off Time** – In the current design the hold-off time needs to be configured manually off-chip. This manual adjustment carries the risk of suboptimal hold-off times, which can be either too small resulting in excessive after-pulsing and degraded photon detection accuracy, or too large reducing the achievable maximum photon count rate. To address this limitation, a promising future enhancement is the integration of an intelligent hold-off autotuning module. The hold-off time can be self-tuned eliminating the need for external configuration and ensure reliable, high-performance operation [46].
- **Dynamic Configuration of the VCR** – The Voltage Controlled Resistor (VCR) is currently tuned off-chip via a power-supply. Future work could involve designing a control circuit that dynamically adjusts the VCR based on measured excess voltage at each pixel. This would eliminate the need for additional I/O pins and allows for more precise tuning, as optimal resistance may vary between SPAD pixels.
- **On-Chip MW Antenna and Frequency Modulator Integration** – Incorporating a Microwave (MW) antenna and Frequency Modulator (FM) module directly on-chip would enable fine-tuned control of the magnetic field for optimal NV-axis alignment. This could greatly improve the accuracy and resolution of Optically Detected Magnetic Resonance (ODMR) measurements. Due to potential interference from distributing MW signals across the chip via wires, local modulation is necessary. Additionally, each pixel would require a calibration routine to correctly orient the local magnetic field. This approach is inspired by designs proposed by Ibrahim et al. and Edakkadan et al. [19], [34].
- **3D Integration for Area Optimization** – As SPAD-array resolutions increase, spatial efficiency becomes critical. A promising strategy for improving spatial efficiency and scalability is the adoption of 3D integration techniques. By stacking the SPAD-detection layer separately from the control logic and data processing layers, the overall chip footprint can be reduced, while also improving power distribution and simplifying routing.

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LIST OF ABBREVIATIONS

AC - Alternating Current
BAP - Bachelor Afstudeer Project (translation: Bachelor Graduation Project)
CMOS - Complementary Metal Oxide Semiconductor
CW - Continuous Wave
DC - Direct Current
DCR - Dark Count Rate
ESR - Electron Spin Resonance
FLIM - Fluorescence Lifetime Imaging Microscopy
FM - Frequency Modulator
I/O - Input / Output
IR - Infrared
LSB - Least-Significant Bit
LVS - Layout-Versus-Schematic
MSB - Most-Significant Bit
MW - MicroWave
NMOS - N-type Metal-Oxide-Semiconductor
NV - Nitrogen-Vacancy
OD - Oxide Diffusion
ODMR - Optically Detected Magnetic Resonance
PDE - Photon Detection Efficiency
PIPO - Parallel Input, Parallel Output
PISO - Parallel Input, Serial Output
PMOS - P-type Metal-Oxide-Semiconductor
QE - Quantum Efficiency
QIT - Quantum Integration Technology
SNR - Signal-to-Noise Ratio
SPAD - Single-Photon Avalanche Diode
TSMC - Taiwan Semiconductor Manufacturing Company
VCR - Voltage Controlled Resistor
ZFS - Zero-Field Splitting

A

APPENDIX A: FIGURES

Figure A.1: **Validation of the PISO in a ModelSim simulation**. The PISO used in this simulation handles 4-bit data from 3 SPADs, instead of the 21-bit data from 16 SPADs used in the actual design. During the first read cycle, the numbers 0xE = '1110', 0x1 = '0001' and 0xA = '1010' are read consecutively. The PISO should read every number starting from the LSB towards the MSB. The output of the first read cycle should therefore be: '0111 1000 0101'. During the second read cycle, the numbers 0xF = '1111', 0x3 = '0011' and 0xB = '1011' are read consecutively. The output of the second read cycle should therefore be: '1111 1100 1101'. The ModelSim simulation illustrates that the PISO correctly outputs the given numbers of each read cycle and is capable to reset itself after the first read cycle and process another cycle.