# Strategies for the implementation of ion implantation doping technique in c-Si wafer-based solar cells

Limodio, Gianluca

**DOI**
10.4233/uuid:7faee5f5-21ed-4dba-b539-9427907fd55b

**Publication date**
2019

**Document Version**
Final published version

**Citation (APA)**
Limodio, G. (2019). *Strategies for the implementation of ion implantation doping technique in c-Si wafer-based solar cells*. [Dissertation (TU Delft), Delft University of Technology].
https://doi.org/10.4233/uuid:7faee5f5-21ed-4dba-b539-9427907fd55b

**Important note**
To cite this publication, please use the final published version (if applicable).
Please check the document version above.

# STRATEGIES FOR THE IMPLEMENTATION OF ION IMPLANTATION DOPING TECHNIQUE IN C-SI WAFER-BASED SOLAR CELLS

Gianluca LIMODIO

# STRATEGIES FOR THE IMPLEMENTATION OF ION IMPLANTATION DOPING TECHNIQUE IN C-SI WAFER-BASED SOLAR CELLS

## Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof. dr. ir. T.H.J.J. van der Hagen,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op woensdag 9 oktober 2019 om 10:00 uur

door

**Gianluca LIMODIO**

Master of Science in Electronics Engineering, University of Napoli Federico II, Italy
geboren te Scafati, Italy.

Dit proefschrift is goedgekeurd door de

promotor: prof. dr. M. Zeman
copromotor: dr. O. Isabella

Samenstelling promotiecommissie:

| | |
|---|---|
| Rector magnificus, | voorzitter |
| Prof. dr. M. Zeman, | Technische Universiteit Delft |
| Dr. O. Isabella, | Technische Universiteit Delft |
| | |
| *Onafhankelijke leden:* | |
| Prof. dr. A.W. Weeber, | Technische Universiteit Delft |
| Prof. dr. J. Werner, | Universität Stuttgart |
| Dr. I. Gordon, | IMEC |
| Prof. dr. J. Schmitz, | University of Twente |
| Dr. R.C.G. Naber, | Tempress Systems BV |

*Keywords:* c-Si wafer-based solar cells, ion implantation, carrier-selective passivating contacts, passivation,

*Printed by:* IPSKAMP Printing

*Front & Back:* *Cleanroom in a shell*, designed by Vincenzo Venoki Tortora, inspired by a chat of the author with the artist. Follow @vinzjackell on Facebook and @Venoki on Instagram.



An electronic version of this dissertation is available at
`http://repository.tudelft.nl/`.

# CONTENTS

# 1

# INTRODUCTION

## 1.1. PHOTOVOLTAIC MARKET

THE photovoltaic market share among renewable energy sources has increased exponentially in the last two decades [1]. The electricity generation capacity from PV source in the European Union is increased up to 102 GW in 2016 exceeding the target of 83 GW fixed by the National Renewable Energy Action Plan (NREAP) in 2005 [2]. The expansion of the European market is limited when compared to the important developments in China, Japan and USA. Figure 1.1 shows the annual installed capacity in the

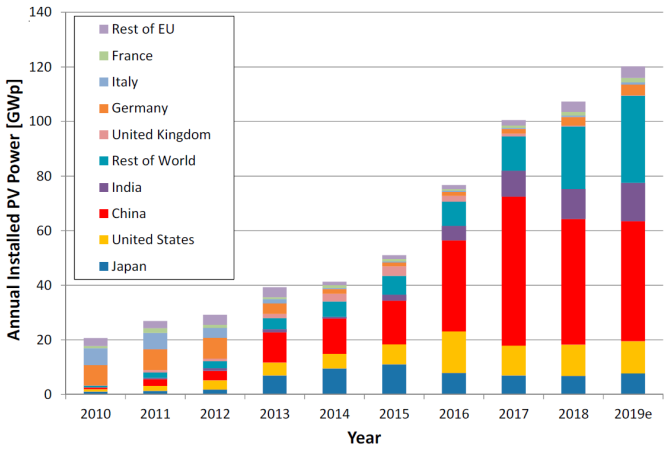


Figure 1.1: Annual installed PV capacity in GWp, taken from [2].

last ten years. In 2008 and 2009, more than 50 % of market share was detainated by European Union. From 2010 to 2016, China, Japan and USA took over much of the installed capacity. This is due to various energy policies at government level. In the European

market, discount conditions change from country to country. Indeed, most of the supporting schemes of the Member States of European Union have not been designed to match the exponentially growing market, leaving high uncertainity for investors [3].

For this reason, according to International Energy Agency medium-term report, EU installed capacity share is expected to drop below 30 % by 2020 when compared to worldwide installation capacity, impacting signficantly jobs in PV sector [4][5]. Price of a PV module substantially decreased below 1 US$/$W_p$ because of the supporting schemes given by governments [6]. Therefore, the consequence is a lower levelized cost of electricity (LCOE), that is the ratio between lifetime costs and energy production [7]. Currently, LCOE for photovoltaic energy is around 0.07 $/kWh, averaged on worldwide, and it is expected to decrease down to 0.02 $/kWh in 2027 [8].

Another key parameter to assess the suitability of an energy source is the so-called energy pay-back time (EBPT), that corresponds to the time the energy system has to operate to recover both the energy and the associated generation of pollutants to fabricate the system [9]. In the case of PV energy source, EPBT depends on the location of the system. Indeed, in Northern Europe, a PV system is estimated to operate ~2.5 years before recovering the invested energy, while in Southern Europe EPBT goes down to ~1 year for commercial c-Si PV modules [10]. Both EPBT and LCOE depend on technology used in solar cells.

Indeed, different absorber layers are available in the current state of the art, from mono to multi-crystalline silicon wafer technology (between 100 and 200 $\mu$m-thick material) or so-called thin-film technology, consisting in a very thin absorber layer (1 – 2 $\mu$m-thick) of a-Si, CIGS or CdTe. Wafer-based Si technologies have the advantage of high efficiency (current world record efficiency for mono-crystalline, single junction, silicon solar cell at lab-scale is 26.7% [11], while for multi crystalline silicon solar cell is 22.3% [12]), so the energy production is much higher than thin film solar cells. On the other hand, thin-film solar cells consume less raw material in the fabrication process. Currently,~95% of the PV market share is held by Si wafer technology [13]. Around 60% of the module production is based on multi-crystalline Si, with 30% left to mono-crystalline silicon technology and the rest is occupied by thin-film technology.

According to the international roadmap for photovoltaics (ITRPV), by the next ten years, the market will see an exponential increase of module production based on mono-crystalline silicon solar cells because of mass-production implementation of passivated emitter and rear (PERC) solar cells [14]. The reason for this is the improved efficiency of mono-crystalline silicon solar cells (due to diamond wiring sewing process that reduces kerf losses) and the continuos reduction of c-Si wafers' price due to mass production. This will give a better EPBT and LCOE than multi c-Si wafers. In the next paragraphs, operation of a wafer-based c-Si solar cell, the main existing technologies, the state-of-the-art efficiencies and all the main aspects of this promising technology will be reviewed.

## 1.2. C-SI SOLAR CELL OPERATION AND TECHNOLOGY

The ideal working principle of a solar cell is that photons in the absorber layer generate electron-hole pairs that can diffuse/drift without any losses and are collected at appropriate contacts. Then, electron hole pairs are extracted without any recombination neither in the bulk or at the surfaces [15]. The hole or electron contacts, also referred to

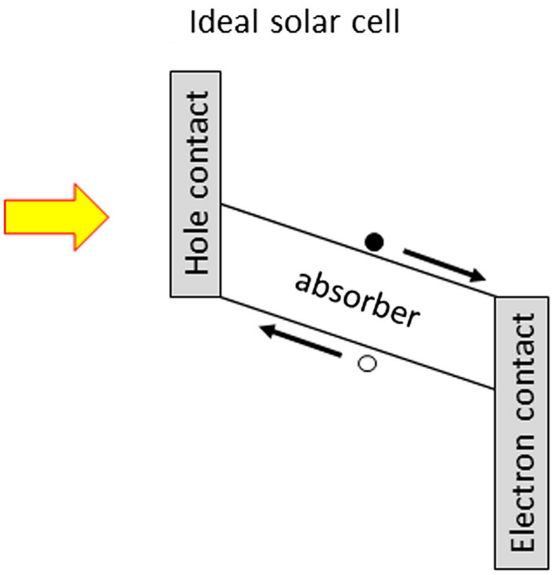


Figure 1.2: Working principle of ideal solar cell, taken from [16].

as carrier-selective contacts, have ideally an asymmetric barrier that accepts only majority carriers and fully repel minority carriers, as shown in Figure 1.2. A solar cell is a p-n junction that works in illuminated condition, therefore always in forward bias. The relationship between current and voltage is determined by the sum of the photo-generated, thermal generated currents and the recombination current [17].

$$J(V) = J_{rec}(V) - J_{gen}(V) - J_{ph} = J_0(exp(\frac{V}{V_t}) - 1) - J_{ph} \tag{1.1}$$

Typical current (power) – voltage characteristics are shown in figure 1.3. It is possible to define key parameters to assess quality of a solar cell; open-circuit voltage ($V_{OC}$), short circuit current density ($J_{SC}$), and Fill-Factor (FF). $V_{OC}$ consists in the voltage obtained when no current is flowing in the external circuit. It follows the equation 1.2;

$$V_{OC} = V_t log(\frac{J_{ph}}{J_0} + 1) \tag{1.2}$$

Where $V_t$ is thermal voltage equal to kT/q (k is the Boltzmann constant, T is temperature and q is the elementary charge) and $J_0$ is defined as saturation current density. Short-circuit current density is the current flowing when short-circuit is a load of a solar cell and it is typically equal to photo-generated current. FF defines the extraction efficiency of carriers and it is calculated as below;

$$FF = \frac{J_{MPP}V_{MPP}}{J_{SC}V_{OC}} \tag{1.3}$$

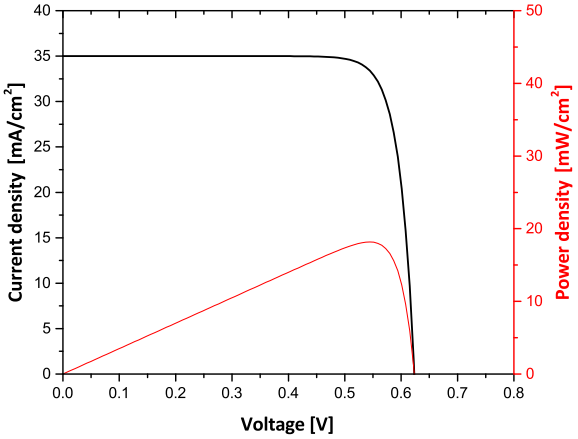


Figure 1.3: Typical J-V (Black line) and P-V (red line) characteristics of a solar cell.

Where $J_{MPP}$ and $V_{MPP}$ are current and voltage measured at maximum power point. Efficiency then will be the product of $V_{OC}$, $J_{SC}$ and FF measured under standard test conditions (STC, 25 °C, Air Mass 1.5 global spectrum and 1000 W/m$^2$ as input irradiance), divided by input power;

$$\eta = \frac{J_{SC} V_{OC} FF}{P_{IN}} \tag{1.4}$$

In typical wafer-based c-Si solar cells absorber layer is usually 100-200 $\mu$m-thick. Therefore, the photo-generated carriers are collected into their respective contacts through the mechanism of diffusion. So, long diffusion lengths and high crystalline quality of c-Si bulk are required to complete this process efficiently. Therefore, recombination at silicon surface must be quenched. This feature is called passivation. There are two different types of passivation, i) chemical and ii) field-effect.

Chemical passivation aims to saturate dangling bonds at Si surface [18]. This is often obtained by thin-film (between 5 and 30 nm-thick) of dielectric materials as $SiO_2$ [19], $Al_2O_3$ [20] or hydrogenated PECVD/sputtered materials as $SiN_x$ [21] [22], $SiC_y$ [23] or a-Si:H [24].

Field-effect passivation consists instead of depositing a layer that is capable to shield one type of carriers to allow only the other polarity to be collected at the contact [25]. This shading is created via an inversion layer that generates a space charge region. Across this space charge region a built-in electrical field will direct the flow of carriers, collecting electrons (holes) and rejecting holes (electrons) [26]. This built-in electrical field can be induced by either a dielectric layer with high density of positive/negative fixed charges [27] or a highly-doped wide band-gap material, therefore un-balancing Fermi levels inducing a strong band-bending [28].

A noteworthy layer that induces field-effect passivation of p-type c-Si surface is aluminum oxide ($Al_2O_3$) [29], which, deposited by atomic layer deposition (ALD) technique, is capable to reach very low surface recombination velocity [30]. This is due to fact that $Al_2O_3$ layer has high density of negative fixed charges [31], therefore inducing a depletion

region at the interface with p-type c-Si. In the next subparagraphs, the most important c-Si solar cells architectures, their advantages and their limits will be reviewed.

### 1.2.1. AL-DOPED BACK SURFACE FIELD SOLAR CELLS

Al-BSF solar cell architecture is the simplest wafer-based c-Si solar cell. It has been developed in late 1970s [32]. It typically consists in a Czochralski or mc-Si p-type wafer textured at the front. Then, as the conceptual scheme in figure 1.4 shows, phosphorous emitter is diffused at the front side while at rear-side silicon is alloyed with Al at temperatures between 700 and 900°C to form back surface field (BSF) passivation layer and rear ohmic contact. Contact formation consists in four main steps; i) printing of Al, ii)

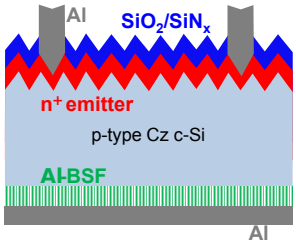


Figure 1.4: Conceptual scheme of Al-BSF solar cell.

alloy in a belt furnace above the eutectic temperature (by eutectic it is meant the lowest possible melting temperature of possible combination of the compounds), iii) cool down and epitaxial regrowth of the $p^+$ BSF and iv) final solidification [33]. It is possible to control junction depth, uniformity and thickness of this contact by optimizing temperature peak firing and temperature profile of cool down [34]. The critical feature of

Table 1.1: External parameters of the highest efficiencies Al-BSF solar cells, based on [39] and [40].

| Area [$cm^2$] | $V_{OC}$ [mV] | $J_{SC}$ [$mA/cm^2$] | FF [%] | $\eta$ [%] |
|---|---|---|---|---|
| 4[39] | 648 | 38.6 | 80.6 | 20.1 |
| 239[40] | 645 | 38.9 | 80.7 | 20.3 |

this technology is the trade-off between the uniformity of Al-BSF layer and its thickness [35]. Nonetheless, typical surface recombination velocities (SRV) are between 200 and 600 cm/s [36][37], although interesting results have been presented with SRV below 200 cm/s [38]. One of the highest efficiencies is 20.1% reached by Fellmeth et. al. on 4 $cm^2$-large device with external parameters as highlighted in table 1.1. Open-circuit voltage ($V_{OC}$) is less than 650 mV. By scaling up to large-area devices (239 $cm^2$), presented in [40], $V_{OC}$ decreases down to 645 mV. Moreover, short-circuit current density ($J_{SC}$) does not overcome 39 $mA/cm^2$ due to not optimized back reflector [41]. FF is high in both cases (> 80%) because a good ohmic contact is ensured at the rear-side and a low sheet

resistance ($R_{SH}$) emitter is diffused at the front, in an eventual selective configuration [42]. The reason for a limited $V_{OC}$ lies in the fully-metallized rear-contact that induces very high contact recombination evaluated to be 900 fA/cm$^2$ [43]. A recombination analysis at maximum power point (MPP) of this solar cell architecture, made by Battaglia et. al. [44], shows that 49% of the total recombination is ascribed to the rear contact. Figure 1.5 summarizes these results. Al-BSF solar cell is the main device fabricated since

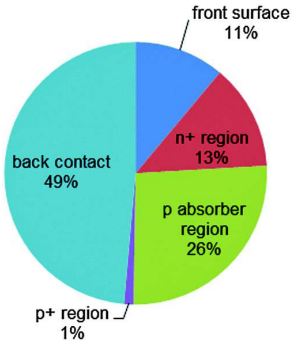


Figure 1.5: Analysis of recombination losses at maximum power point (MPP) of a typical homojunction Al-BSF solar cell, taken from [44].

the birth of PV industry, with a 60% of the production of the c-Si market share in 2017 [8]. Nonetheless, it has limitation in performances due to very high contact recombination and poor internal reflectance. Despite the attempts of optimizing efficiencies with Boron BSF or wafer thickness reduction to 100 $\mu$m [45], the efficiency will always be limited because of $V_{OC}$ losses. To quench contact recombination, it is possible to restrict contact area at the rear side, introducing the so-called Passivated Emitter and Rear Cell (PERC), a concept that will be discussed in the next sub-paragraph.

### 1.2.2. PASSIVATED EMITTER AND REAR CELLS (PERC)

In view of Al-BSF solar cells limits, rear side contact area restriction, introducing a rear passivation layer, represents a further step towards high efficiency devices. The first Passivated Emitter and Rear Cell (PERC) has been presented in 1989 with an efficiency of 22.8% [46].

As figure 1.6 shows, PERC solar cell is a concept that can be divided in four categories; i) PERD (figure 1.6 (a)), in which p-type silicon is directly locally contacted without any BSF doping, ii) PERL (figure 1.6 (b)), with a local highly doped BSF contacted by metal, iii) PERT (figure 1.6 (c)), in which the BSF is fully-diffused at rear, then local contacts are made, then iv) PERF (figure 1.6 (d)), that employs floating emitter deposited also at rear-side to enhance lateral transport [47]. A passivation layer is needed in any case at rear side for p-type Si, therefore either $SiO_2/SiN_x$ or $Al_2O_3/SiN_x$ stacks are typically employed [48][30], enhancing also the internal reflectance of the cell. This gives the advantage of having greater $V_{OC}$ than full-area Al-BSF because of less contact recombination occurring [49]. The world-record efficiency for this family of devices is 25% obtained by Zhao et. al. [50] on a PERL device. The industry is slowly shifting from Al-BSF solar cells

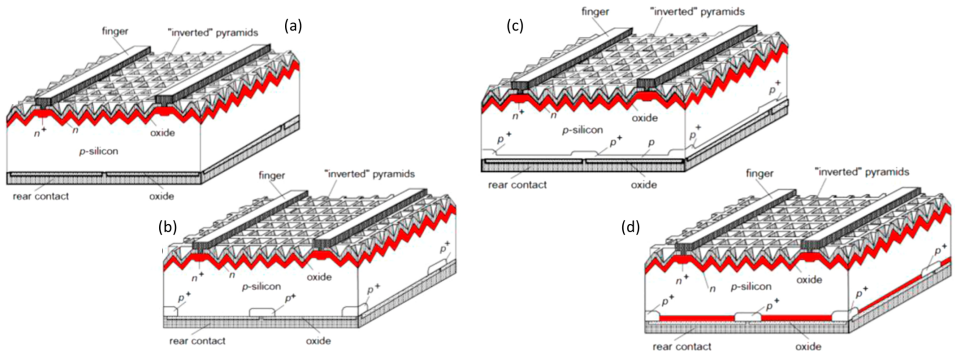


Figure 1.6: PERC Solar cell family; (a) PERD (Passivated Emitter Rear Directly Contacted); (b) PERL (Passivated Emitter Rear Locally-doped; (c) PERT (Passivated Emitter Rear Totally-diffused); (d) PERF (Passivated Emitter Rear Floating Junction), taken from [47].

to PERC solar cells in the last ten years, employing mostly PERT and PERL. Chinese researchers are particularly active in this area, with impressive 22.2% efficient PERT solar cell [51], attempting also to optimize processing of emitter and back surface field via co-diffusion [52]. Efficiencies > 21% are also achieved by Benick et. al for both PERL and PERT [53]. These devices have a lot of room for improvement, nonetheless the problem of contact recombination between Si and metal is only masked by contact area restriction at the rear side. Moreover, there is a two-dimensional flow of carriers also at rear side that gives a trade-off between $V_{OC}$ and series resistance, i.e., FF [54], so careful metallization design and scheme at rear side needs to be applied [55]. The industrialization of this device is critical because extra steps have to be performed to passivate the rear side. This collides with mass production and simplicity of the process. For these reasons, it would be preferable to eliminate completely contact recombination, switching to the so-called carrier-selective passivating contacts.

### 1.2.3. PASSIVATING CONTACTS TECHNOLOGY

Several solutions have been proposed to quench contact recombination that limits its efficiency in commercial solar cells. All the schemes that aim to quench contact recombination are called carrier-selective passivating contacts (CSPC). The scientific idea behind this concept scheme is to separate Si absorber layer and metal by depositing a layer capable to perform a chemical passivation (i.e., saturating dangling bonds at c-Si surface) and concurrently select only one type of carriers that is extracted at the metal contact [56][57]. Indeed, the issue with homojunction contact scheme is that, since metal has a very high surface recombination velocity (SRV), the recombination rate at the metal contact is also very high [58]. Figure 1.7 shows the main passivating contacts known applied in a front/rear contacted solar cell scheme. It is possible to sort out this technology based on the thermal budget needed for deposition/activation of the contact. It is important to highlight that current standard metallization, screen printing/firethrough in c-Si solar cells industry is set to high temperature (> 700 °C).

The most known and studied passivating contact technology is hydrogenated amor-

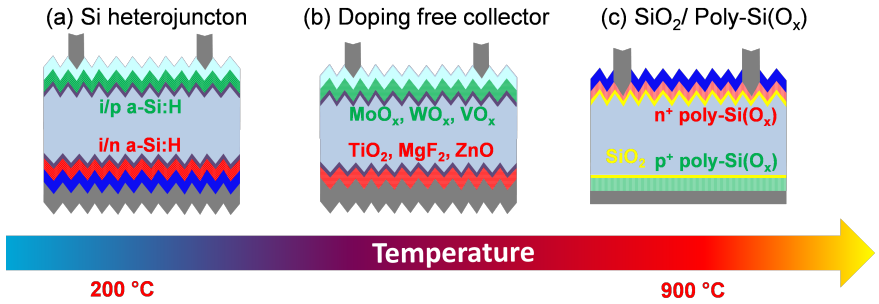


Figure 1.7: Three main passivating contacts are depicted; (a) Silicon Heterojunction (SHJ), (b) Doping-free collector, (c) $SiO_2$ / doped poly-Si.

phous silicon (a-Si:H). Typically, a stack composed by intrinsic and doped a-Si:H is deposited in order to obtain excellent chemical passivation, on one hand, and a field-effect passivation thanks to doped a-Si:H and wider band gap than c-Si [59]. By applying this passivation scheme on both sides of a front/rear contacted solar cell, $V_{OC}$ of 750 mV has been achieved [60], an efficiency of 25.1% in front/rear contacted solar cell [61] and the current world-record (efficiency greater than 26%) has been obtained by Kaneka in an interdigitated back contacted device [62]. The reason for high efficiency lies into passivation mechanism that is highlighted in figure 1.8. Indeed, by depositing a thin film of intrinsic a-Si:H, chemical passivation is performed and all interface defects density ($D_{it}$) are saturated by hydrogen. Since this material has a wide band-gap of 1.7 eV, by depositing a doped a-Si:H thin layer, an asymmetric band-bending is induced due to un-balanced Fermi levels between a-Si:H and c-Si [63]. This band-bending generates an electrical field across the junction that makes majority carriers (in case of figure 1.8 electrons) capable of tunnelling across a-Si:H, while minority carriers are pushed back to c-Si bulk.

A wafer preparation is needed before a-Si:H deposition to remove any contaminant on Si textured surface [64][65][66]. Post-deposition annealing at temperatures between 150 and 190 °C improves passivation quality because $H^+$ ions diffuse at c-Si/a-Si interface, enhancing thus chemical passivation [67][68]. If placed at the front side of a front/rear contacted solar cell, parasitic absorption occurs in a-Si:H, therefore degrading short-circuit current [69]. The main drawback of this passivation scheme is its temperature limitation that is not compatible with standard solar cell manufacturing. In fact, T > 250 °C dramatically degrades passivation quality [70]. Therefore, a dedicated low-temperature back-end processing (TCO and metallization depositions) is compulsory for this technology.

To solve front transparency issue of SHJ solar cells, a different technology of carrier-selective contacts is used. It is the so-called dopant-free collector materials. It is basically a metal-insulator-semiconductor (MIS) induced junction. Typically, c-Si wafer is chemically passivated by a stack of an intermediate layer as a-Si:H or other ultra-thin dielectrics and a relatively thin layer (around 20 nm) of a material with high (low) work function, typically through sputtering or physical vapour deposition, for selectivity pur-

pose [71][72]. The explanation for the selectivity lies in band-diagram shown in figure 1.9. In fact, given the high (low) work function of these materials, they induce a strong band-bending across the junction.

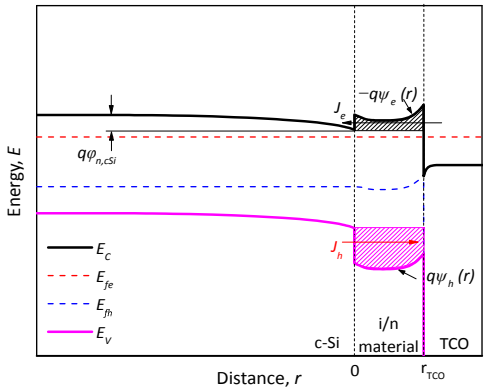


Figure 1.8: Band diagram of SHJ passivated contacts in illuminated and short circuit current condition.

Therefore, an electrical field is induced and selectivity is achieved through a band-to-band tunnelling mechanism. If this material has a lower work function than the one of the absorber layer, it is intrinsically electron-selective, otherwise it is hole-selective contact [73]. They are called dopant-free collectors because there is no need to introduce any dopant species into these materials, but just work function offset gives selectivity of the contact. Since no doping is introduced into these materials, they are more transparent than doped a-Si:H [74]. Typical materials for electron-selective contacts are $TiO_2$, $MgF_2$, ZnO [75], while the most used hole-selective contacts are $MoO_x$, $WO_x$, $VO_x$ [76].

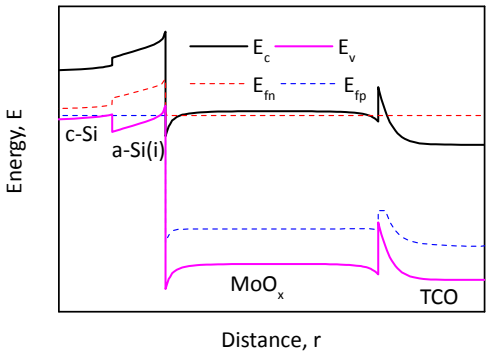


Figure 1.9: Transition Metal Oxide (TMO) passivating contact band-diagram at V = 0V with $MoO_x$ as hole-collector.

Efficiencies beyond 22% have been demonstrated in front/rear contacted devices in combination with HTJ technology [77]. Typically, thermal budget of these contacts is around 400 °C, therefore higher than a-Si:H. This type of solar cells is compatible with tandem configuration in combination with thin-film solar cells. Due to its higher thermal budget, it is possible to integrate emerging technologies as perovskite or $NiO_2$ in a monolithic tandem solar cells [78]. As of now, the exact features of these layers depend on the deposition method.

All of these passivating contact technologies are not compatible with standard solar cells manufacturing because of their restricted thermal budget. $SiO_x$/doped poly-Si stack passivating contact can instead withstand high temperature as 700 °C, therefore it matches industry requirements for high thermal budget. The carrier selectivity, explained in the band-diagram of figure 1.10, is achieved by (i) slightly different band-gap between poly-Si and c-Si, (ii) large difference between the quasi Fermi levels of the doped poly-Si and the c-Si, (iii) band offset asymmetry of the $SiO_x$ compared to Si and (iv) high tunnelling probability [79]. The transport principle at this junction is still under debate and it might occur either via tunneling [80][81] and/or via pin-holes present at c-Si/$SiO_x$ interface [82]. Typically, $SiO_x$ is deposited via thin, wet oxidation in nitric acid ($HNO_3$) [83], ozone-based solution [84] or dry thermal process [85]. Instead poly-Si is deposited first in form of amorphous silicon via plasma enhanced chemical vapour deposition (PECVD) or low pressure chemical vapour deposition (LPCVD) [86], then annealed at high temperature for crystallization. Doping process occurs either via in-situ [87] or ex-situ doping, as ion-implantation [88].

By applying $SiO_x$/P-doped poly-Si full-area at rear side in combination with homojunction contact at the front, 25.8% efficiency has been achieved [89]. This layer has been applied also in bifacial solar cells with 21.0% efficiency [90]. By placing poly-Si layer at the front side, parasitic absorption occurs into this layer especially in the short-wavelength range [91]. For this reason, solar cells with poly-Si at the front side might be used in tandem application with thin-film solar cells [92]. In order to gain in transparency, poly-Si can be alloyed in $O_2$ or $CH_4$ to form poly-$SiO_x$ or poly-$SiC_y$, respectively. Some demonstrators of efficiencies beyond 21% are obtained with poly-$SiO_x$ deployed on both sides [93] and beyond 22% with poly-$SiC_y$ in combination with a-Si:H contact [94]. I

### 1.2.4. INTERDIGITATED BACK CONTACTED (IBC) SOLAR CELLS

In order to solve the issue of front metal reflection losses, both contacts are placed at the rear side in the so-called interdigitated back contacts (IBC) solar cell. This concept was born in late 1970s applied mainly in concentrated sunlight [95]. The contacts are placed at rear side, alternating p- and n-type collectors in an interdigitated scheme. This architecture allows to boost in principle short-circuit current density. Moreover, there is no requirement of metal contacts width, such that high FF can be ensured. Nonetheless, the pitch, intended as the distance covered by n-type contact and p-type contact, influences transport and electrical shading [96]. In order to partially solve this issue and to avoid any short circuit between p- and n-type fingers, different architectures have been implemented; i) trench isolation [97], ii) gap-less IBC [98] and iii) self-aligned IBC [99].

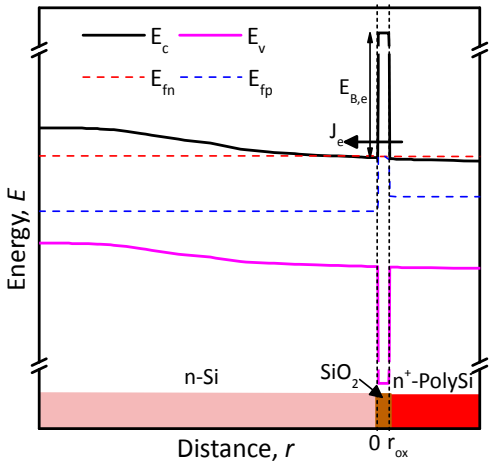


Figure 1.10: Band-diagram, at short circuit current condition, of $SiO_x$/ n-type poly-Si passivating contact.

Figure 1.11 shows IBC technology combined with different contact schemes depending on thermal budget. As for front/rear contacted solar cells, silicon heterojunction technology has the lowest thermal budget. So, back-end processing is temperature limited. While for doping-free collector they can withstand higher temperature (T = 350 °C) than a-Si, while homojunction or $SiO_x$/doped poly-Si contact scheme thermal budget is 900 °C. Table 1.2 below highlights the highest efficiencies known in literature. All the technologies (except dopant-free collector), overcome 25% efficiency. n the case of homojunction IBC solar cells, a point-contact approach can also improve passivation properties of doped layers. Using this feature, 24.4% has been achieved by Franklin et. al [100]. A combination of this solar cell architecture with high-efficiency concepts as carrier-selective passivating contacts exposed in the previous paragraph leads to very high efficiency.

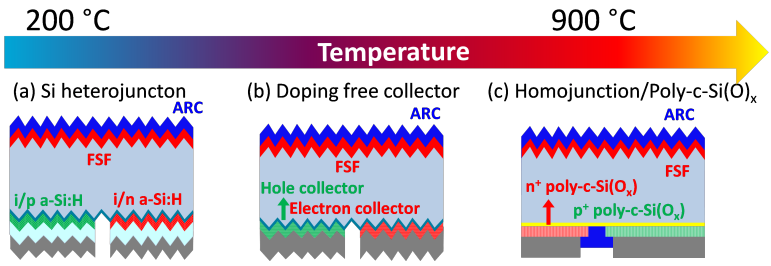


Figure 1.11: (a) IBC silicon heterojunction, low thermal budget, (b) IBC with doping free contacts, medium thermal budget (c) IBC homojunction or TOPCON/POLO, high thermal budget.

An interesting concept embedded in IBC solar cell is the so-called tunnelling IBC that is a

stack of n-doped and p-doped a-Si:H such that a tunnel junction is induced. This contact has high selectivity due to high tunnel efficiency in this tunnel recombination junction. By employing this concept, 24.1% efficiency has been achieved by Tomasi et. al. [105]. Nonetheless, all the patterning processes of rear side are very complicated. Therefore, IBC solar cell manufacturing is more expensive than front/rear contacted solar cells. It is anyway forecasted that the production of IBC solar cells will be raising in 2027 up to 30% of the total share.

Table 1.2: The world-record efficiencies for IBC solar cells, divided into different passivation technologies.

| Institute | Passivation technology | Area [$cm^2$] | $V_{OC}$ [mV] | $J_{SC}$ [$mA/cm^2$] | FF [%] | $\eta$ [%] |
|---|---|---|---|---|---|---|
| Kaneka [101] | Silicon Heterojunction | 79.0 | 738 | 42.6 | 84.9 | 26.7 |
| SYSU - CSEM [102] | Doping – free collector | 9.0 | 633 | 40.0 | 75.4 | 19.1 |
| Trina Solar [103] | Homojunction/Poly-Si | 243.1 | 715 | 42.3 | 82.8 | 25.0 |
| ISFH [104] | Polysilicon on Oxide | 4.0 | 726 | 42.6 | 84.2 | 26.1 |

## 1.3. AIM AND OUTLINE OF THIS THESIS

This thesis provides strategies to employ ion implantation as doping technique in c-Si wafer-based solar cells. As reported in International Technology Roadmap for Photovoltaic (ITRPV), Al-BSF will be almost completely replaced, in 2027, by PERC and back contacted solar cells [14]. For this reason, local doping is needed. Therefore, ion implantation matches perfectly with this feature. Indeed, with ion implantation it is possible to pattern independently different areas of a wafer by using dielectric masks as $SiN_x$ or $SiO_x$. Since it is a one-sided doping technique, it is not needed to further strip any silicate glass as in the case of tube furnace diffusion. By matching this doping technique with high thermal budget carrier-selective passivating contacts, it is possible to potentially achieve high efficiency and low production cost. This low production cost is given by high-throughput (> 1000 wafers/hours) given by typical ion implantation equipments [106]. This doping technique also reduces the total number of processing steps, therefore simplyifing a mass-production design [107]. These advantages come at a cost of an important initial economic investment (several M$) [108].

This thesis provides scientific insight on the development of ion-implanted carrier-selective passivating contacts. So, the author highlights what are the conditions in which $SiO_x$/implanted poly-Si stack shows enhanced passivation quality. These layers are then embedded in a front/rear contacted solar cell that shows this contact scheme on both sides. High passivation quality ($V_{OC}$ ~700 mV) is demonstrated. Nonetheless, high parasitic absorption hinders current collection in the short-wavelength region. This brings to two eventual paths that can be followed; i) use this type of solar cells as bottom cell in tandem application, ii) employ different structures at the front side to improve current collection.

This thesis focuses on the second option. In fact, by employing a selective structure at front, with a lightly doped homojunction front surface field for optical transparency

and poly-Si underneath the metal contact for contact passivation, current collection is improved in the short-wavelength region. The downside is that this structure is more complex because it requires at least one additional patterning step and consequent etching to form selective structure. As a tool-box to reduce losses in poly-poly solar cells, front side is replaced by full-area a-Si:H contact. In this way, an overview of all the possible devices is shown. Regardless solar cell architecture, electro-plating metallization on novel metal seed layers is developed. Indeed, according to ITRPV, this will be one of the metallization schemes that will replace screen-printing in mass production in the next ten years. This thesis shows the development and embodiment into solar cells of Cu plated front contacts. Since it is a metallization scheme, the development is made for all the solar cells technologies shown in this work. Moreover, it is shown a pre-treatment method for a-Si:H deposition that consists in a single step high temperature oxidation that does not involve any hazardous wet chemistry and it is less time-consuming than the standard state-of-the-art thin, wet oxidation-etching cycles. Aside of the introduction chapter shown here, this thesis contains eight more chapters. The outline of thesis is as follow:

In chapter 2 an insight on ion implantation technique is given. It is explained why this doping technique is becoming widely used both in homojunction and high thermal budget passivated contacts solar cells. Moreover, a brief overview of solar cell fabrication and characterization is highlighted with particular attention to doping techniques and metallization.

In chapter 3 an application of fully-implanted P-doped BSF front/rear contacted solar cell is shown. This solar cell is a front junction device with boron and phosphorous implanted surfaces at the front and rear, respectively. Front side is passivated by $Al_2O_3/SiN_x$ stack that acts also as anti-reflection coating. An investigation of passivation quality of B-implanted surfaces is also presented.

In chapter 4 the development of ion-implanted poly-Si carrier-selective passivating contacts is shown. In particular, poly-Si electron selective contact on textured Si and poly-Si hole selective contact on flat Si are highlighted at different poly-Si thicknesses. Aside of showing how to form the contact and its characterization, it is shown how doping conditions (implantation dose, energy, annealing temperature and time) can influence passivation properties. Moreover, hydrogenation through forming gas annealing can significantly enhance passivation properties. These layers are then embodied in poly-poly solar cells in a lean, straightforward process. High open-circuit voltages and reasonable transport (FF) are shown. The pitfall of this solar cell is the low short-circuit current, due to front poly-Si parasitic absorption. Indeed, photons (mostly in high-energy range) are absorbed by front poly-Si layer, but the generated electron-hole pair is not collected because of asymmetric barrier of $SiO_x$ at interface with c-Si bulk that does not allow holes collection. The highest efficiency is 19.6%, employing different poly-Si thicknesses at front and rear side, respectively.

Chapter 5 shows a possible architecture to overcome the limits of poly-poly solar cells. Indeed, a selective front surface field that can concurrently passivate the contact and be optically transparent can solve the problem of current collection. Therefore, a lightly doped homojunction front surface field is employed in combination with poly-Si passivating contact underneath the metal contacts while the rear-side is coated on the

full-area by p-type poly-Si contact. Despite lower open-circuit voltage due to back-end processing, higher short-circuit current density is measured with an improved collection in short-wavelength range due to optically transparent front surface field. The highest efficiency achieved is 20.0%.

In chapter 6 the front side of the poly-poly solar cell is further modified replacing front poly-Si with low thermal budget, full-area a-Si:H contact in combination with a TCO, employing the so-called hybrid solar cell. The highest achieved efficiency is 21.0%. The development of the electron-selective a-Si:H contact is presented and the conditions in which this contact shows its best properties are highlighted. Also, Indium Tin Oxide (ITO) and Hydrogenated Indium Oxide (IO:H) are characterized and implemented into hybrid solar cell.

Chapter 7 shows a development of Cu-plating technique for metallization step. This technique is developed both on dielectric anti-reflection coating as $SiN_x/SiO_2$ and TCO material. The development is based mainly on evaporated Ti/Ag seed layer that acts as a conductive material to plate in the most efficient way. The plating characteristics and characterization of the contact are highlighted together with a special focus on adhesion of Cu to Si wafer and aspect ratio of the metal contact. It is shown also as an application into poly-poly and hybrid solar cells.

In chapter 8 a novel pre-treatment method for a-Si electron selective contact deposition on textured wafer is presented. This pre-treatment method is based on high temperature oxidation process that encapsulates all the surface contaminants. Therefore, a slow etching of this thermal $SiO_2$ will result in a smoothened, defects-free textured surface. This pre-treatment shows enhanced passivation compared to standard thin, wet oxidation cycle of silicon (NAOC).

Chapter 9 reports the conclusions of this work. Moreover, an outlook of this work is given in order to possibly implement these scientific developments at industrial level.

## 1.4. MAIN CONTRIBUTIONS TO THE FIELD

This section reports the main contribution to scientific community of PV field reported in this thesis.

- Application of ion implantation doping technique in a P-doped back surface field front/rear contacted solar cell
- Application of ion implantation as ex-situ doping technique to form selective contact in $SiO_x$/doped poly-Si passivation scheme.
- Textured front/flat rear contacted solar cells employing $SiO_x$/poly-Si contact on both sides have been designed and fabricated.
- Solar cells with full-area rear poly-Si passivating contact and a selective structure at the front employing lightly doped homojunction front surface field and poly-Si carrier-selective contact underneath metal has been designed and fabricated to increase current collection if compared to poly-poly solar cells.
- Hybrid solar cell, employing a-Si:H contact and a TCO, keeping full-area rear poly-Si passivating contact, has been proposed, designed and fabricated to verify the impact of rear poly-Si layer.
- Development of Cu plated front contacts and its application into poly-poly and

hybrid solar cells.

- Novel pre-treatment method for a-Si:H deposition on textured Si wafer, based on high temperature oxidation process, has been developed and tested.

## 1.5. REFERENCES

[1] https://www.iea.org/newsroom/news/2016/july/renewable-energy-continuing-to-increase-market-share.html.

[2] Arnulf Jäger-Waldau, Snapshot of Photovoltaics—February 2019, Energies 2019, 12, 769; doi:10.3390/en12050769

[3] Arnulf Jäger-Waldau, PV status report 2016, Publications Office of the European Union; 2016. ISBN 978-92-79-63055-2 (pdf).

[4] International Energy Agency, Medium-Term Renewable Energy Market Report. - Market trends and projections to 2021, 278 pages; 2016. ISBN 978-92-64-26497-7.

[5] IRENA, Renewable energy and jobs. Annual Review; 2016.

[6] http://www.renewableenergyworld.com/articles/2017/04/photovoltaic-cost-and-price-relationship.html

[7] http://energyeducation.ca-encyclopedia-Levelized-cost-of-energy

[8] International Technology Roadmap for Photovoltaic (ITRPV), 2016 results including maturity report.

[9] https://www.nrel.gov//docs//fy04osti/35489.pdf

[10] M.J. de Wild-Scholten, V. Cassagne, T. Huld (2014) Solar resources and carbon footprint of photovoltaic power in different regions in Europe, 29th European Photovoltaic Solar Energy Conference, Amsterdam, the Netherlands, 22-26 September 2014.

[11] K.Yamamoto, Asian Photovoltaic Energy Conference, Otsu, Japan, 2016.

[12] https://www.ise.fraunhofer.de/en/press-media/press-releases/2017/fraunhofer-ise-pushes-world-record-for-multicrystalline-silicon-solar-cells-to-22-point-3-percent.html

[13] Photovoltaics report, Fraunhofer Institute for Solar Energy Systems, ISE with support of PSE Conferences and Consulting GmbH Freiburg, 26 February 2018.

[14] International Technology Roadmap for Photovoltaic (ITRPV), 2017 results, updated to March 2018.

[15] E. Yablonovitch and T. Gmitter, R. M. Swanson and Y. H. Kwark, A 720 mV open circuit voltage SiOx:c/Si:SiOx double heterostructure solar cell, Applied Physics Letters 1985 47:11, 1211-1213, https://doi.org/10.1063/1.96331.

[16] Chavali, Raghu V. K., De Wolf, Stefaan, Alam, Muhammad A., PIP-17-151.R1, Device physics underlying silicon heterojunction and passivating-contact solar cells: A topical review, http://dx.doi.org/10.1002/pip.2959.

[17] Klaus Jäger, Olindo Isabella, Arno H.M. Smets, René A.C.M.M. van Swaaij, Miro Zeman, Solar Energy Fundamentals, Technology, and Systems, Uit Cambridge Ltd, 2016.

[18] Aberle, A. G. (2000), Surface passivation of crystalline silicon solar cells: a review. Prog. Photovolt: Res. Appl., 8: 473-487. doi:10.1002/1099-159X(200009/10)8:5<473::AID-PIP337>3.0.CO;2-D.

[19] Jan Schmidt, Mark Kerr and Andrés Cuevas, Surface passivation of silicon solar cells using plasma-enhanced chemical-vapour-deposited SiN films and thin thermal

SiO2/plasma SiN stacks, Semiconductor Science and Technology, Volume 16, Number 3, 2001.

[20] Schmidt, J. , Merkle, A. , Brendel, R. , Hoex, B. , de Sanden, M. C. and Kessels, W. M. (2008), Surface passivation of high-efficiency silicon solar cells by atomic-layer-deposited Al2O3. Prog. Photovolt: Res. Appl., 16: 461-466. doi:10.1002/pip.823.

[21] Armin G Aberle, Overview on SiN surface passivation of crystalline silicon solar cells, Solar Energy Materials and Solar Cells, Volume 65, Issues 1–4, 2001, Pages 239-248, ISSN 0927-0248, https://doi.org/10.1016/S0927-0248(00)00099-4.

[22] Wim Soppe , Henk Rieffe and Arthur Weeber, Bulk and Surface Passivation of Silicon Solar Cells Accomplished by Silicon Nitride Deposited on Industrial Scale by Microwave PECVD, Prog. Photovolt: Res. Appl. 2005; 13:551–569, DOI: 10.1002/pip.611.

[23] P.M. Kaminski, A. Abbas, K. Bass, G. Claudio, Passivation of silicon wafers by Silicon Carbide (SiCx) thin film grown by sputtering, Energy Procedia, Volume 10, 2011, Pages 71-75, ISSN 1876-6102, https://doi.org/10.1016/j.egypro.2011.10.155.

[24] M. Schmidt, L. Korte, A. Laades, R. Stangl, Ch. Schubert, H. Angermann, E. Conrad, K.v. Maydell, Physical aspects of a-Si:H/c-Si hetero-junction solar cells, Thin Solid Films, Volume 515, Issue 19, 2007, Pages 7475-7480, ISSN 0040-6090, https://doi.org/10.1016/j.tsf.2006.11.087.

[25] Mohammad Ziaur Rahman, Shahidul Islam Khan, Advances in surface passivation of c-Si solar cells, Mater Renew Sustain Energy (2012) 1:1, DOI: 10.1007/s40243-012-0001-y.

[26] J. Schmidt, F. Werner, B. Veith, D. Zielke, S. Steingrube, P.P. Altermatt, S. Gatz, T. Dullweber, R. Brendel, Advances in the Surface Passivation of Silicon Solar Cells, Energy Procedia, Volume 15, 2012, Pages 30-39, ISSN 1876-6102, https://doi.org/10.1016/j.egypro.2012.02.004.

[27] Terlinden, N.M., et al.: Role of field-effect on c-Si surface passivation by ultrathin (2–20 nm) atomic layer deposited Al2O3. Appl. Phys. Lett. 96, 112101 (2010).

[28] Corsin Battaglia, Silvia Martín de Nicolás, Stefaan De Wolf, Xingtian Yin, Maxwell Zheng, Christophe Ballif, and Ali Javey, Silicon heterojunction solar cell with passivated hole selective MoOx contact, Applied Physics Letters 2014 104:11.

[29] G. Dingemans and W. M. M. Kessels, Status and prospects of Al2O3-based surface passivation schemes for silicon solar cells, Journal of Vacuum Science and Technology A: Vacuum, Surfaces, and Films 2012 30:4.

[30] Pierre Saint-Cast, Jan Benick, Daniel Kania, Lucas Weiss, Marc Hofmann, Jochen Rentsch, Ralf Preu, Stefan W. Glunz, High-Efficiency c-Si Solar Cells Passivated With ALD and PECVD Aluminum Oxide, IEEE Electron Device Letters, ( Volume: 31, Issue: 7, July 2010 ), DOI: 10.1109/LED.2010.2049190.

[31] G. Dingemans, N. M. Terlinden, M. A. Verheijen, M. C. M. van de Sanden, and W. M. M. Kessels, Controlling the fixed charge and passivation properties of Si(100)/Al2O3 interfaces using ultrathin SiO2 interlayers synthesized by atomic layer deposition, Journal of Applied Physics 2011 110:9, https://doi.org/10.1063/1.3658246.

[32] J. del Alamo, J. Eguren, A. Luque, Operating limits of Al-alloyed high-low junctions for BSF solar cells, Solid-State Electronics, Volume 24, Issue 5, 1981, Pages 415-420.

[33] S. Narasinha ; A. Rohatgi, Optimized aluminum back surface field techniques for silicon solar cells, Photovoltaic Specialists Conference, 1997., Conference Record of the

Twenty-Sixth IEEE, DOI: 10.1109/PVSC.1997.653925.

[34] Elias Urrejola, Kristian Peter, Heiko Plagwitz and Gunnar Schubert, Silicon diffusion in aluminum for rear passivated solar cells, Appl. Phys. Lett. 98, 153508 (2011); https://doi.org/10.1063/1.3579541.

[35] Vichai Meemongkolkiat,Kenta Nakayashiki, Dong Seop Kim, Radovan Kopecek and Ajeet Rohatgi, Factors Limiting the Formation of Uniform and Thick Aluminum–Back-Surface Field and Its Potential, J. Electrochem. Soc. 2006 volume 153, issue 1, G53-G58, doi: 10.1149/1.2129106.

[36] S. Narasimha ; A. Rohatgi ; A.W. Weeber, An optimized rapid aluminum back surface field technique for silicon solar cells, IEEE Transactions on Electron Devices ( Volume: 46, Issue: 7, Jul 1999 ), DOI: 10.1109/16.772477.

[37] S. Peters, “Rapid Thermal Processing of Crystalline Silicon Materials and Solar Cells”, Ph.D. thesis, University Konstanz, 2004, p. 62.

[38] P. Lolgen ; C. Leguijt ; J.A. Eikelboom ; R.A. Steeman ; W.C. Sinke ; L.A. Verhoef ; P.F.A. Alkemade ; E. Algra, Aluminium back-surface field doping profiles with surface recombination velocities below 200 cm/s, Photovoltaic Specialists Conference, 1993., Conference Record of the Twenty Third IEEE, DOI: 10.1109/PVSC.1993.347046.

[39] Tobias Fellmeth, S. Mack, J. Bartsch, D. Erath, U. Jäger, R. Preu, F. Clement, and D. Bi, 20.1% Efficient Silicon Solar Cell With Aluminum Back Surface Field, IEEE ELECTRON DEVICE LETTERS, VOL. 32, NO. 8, AUGUST 2011, DOI: 10.1109/LED.2011.2157656.

[40] Ki Hyung Kim et al 2017 Jpn. J. Appl. Phys. 56 08MB25.

[41] Andrea Ingenito, Juan Camilo Ortiz Lizcano, Stefan L. Luxembourg, Rudi Santbergen, Arthur Weeber, Olindo Isabella, Miro Zeman, Optimized back Reflectors for Rear Diffused c-Si Solar Cells, Energy Procedia, Volume 55, 2014, Pages 94-100,https://doi.org/10.1016/j.egypro.2014.08.085.

[42] G. Hahn, Status of selective emitter technology, 25th European Photovoltaic Solar Energy Conference and Exhibition / 5th World Conference on Photovoltaic Energy Conversion, 6-10 September 2010, Valencia, Spain, DOI: 10.4229/25thEUPVSEC2010-2DP.2.2.

[43] Jens Muller, Karsten Bothe, Sebastian Gatz, Heiko Plagwitz, Gunnar Schubert and Rolf Brendel, Contact Formation and Recombination at Screen-Printed Local Aluminum-Alloyed Silicon Solar Cell Base Contacts, IEEE Transactions on Electron Devices ( Volume: 58, Issue: 10, Oct. 2011 ), DOI: 10.1109/TED.2011.2161089.

[44] C. Battaglia, A. Cuevas and S. D. Wolf, "High-efficiency crystalline silicon solar cells: status and perspectives," Energy Environ. Sci., vol. 9, pp. 1552-1576, 2016, DOI:10.1039/C5EE03380B.

[45] K.A. Munzer, K.T. Holdermann, R.E. Schlosser, S. Sterk, IEEE Trans. Electron Devices 46 (1999) 2055.

[46] Andrew W. Blakers, Aihua Wang, Adele M. Milne, Jianhua Zhao, and Martin A. Green, 22.8% efficient silicon solar cell, Appl. Phys. Lett. 55, 1363 (1989); https://doi.org/10.1063/1.101596.

[47] Martin A. Green, The Passivated Emitter and Rear Cell (PERC): From conception to mass production,Solar Energy Materials and Solar Cells, Volume 143, 2015, Pages 190-197, ISSN 0927-0248, https://doi.org/10.1016/j.solmat.2015.06.055.

[48] W. Blakers and M. A. Green, Oxidation condition dependence of surface pas-

sivation in high efficiency silicon solar cells, Appl. Phys. Lett. 47, 818 (1985); https://doi.org/10.1063/1.95994.

[49] S. Gatz, J. Müller , T. Dullweber, and R. Brendel, Analysis and optimization of the bulk and rear recombination of screen-printed PERC solar cells, SiliconPV: April 03-05, 2012, Leuven, Belgium, doi: 10.1016/j.egypro.2012.07.035.

[50] Zhao, J. , Wang, A. and Green, M. A. (1999), 24·5% Efficiency silicon PERT cells on MCZ substrates and 24·7% efficiency PERL cells on FZ substrates. Prog. Photovolt: Res. Appl., 7: 471-474. doi:10.1002/(SICI)1099-159X(199911/12)7:6<471::AID-PIP298>3.0.CO;2-7.

[51] Wenhao Cai, Shengzhao Yuan,Yun Sheng,Weiyuan Dua,Zigang Wang, Yifeng Chen, Yang Yang, Pietro. P. Altermatt, Pierre J. Verlinden and Zhiqiang Feng, 22.2% efficiency n-type PERT solar cell, 6th International Conference on Silicon Photovoltaics, SiliconPV 2016, doi: 10.1016/j.egypro.2016.07.119.

[52] Qingzhu Weia, Shude Zhang, Shuanglong Yu, Junyu Lu, Weifei Lian, Zhichun Ni, High efficiency n-PERT solar cells by B/P co-diffusion method, 7th International Conference on Silicon Photovoltaics, SiliconPV 2017, doi: 10.1016/j.egypro.2017.09.345.

[53] Jan Benick, Bernd Steinhauser, Ralph Müller, Jonas Bartsch, Mathias Kamp, Andrew Mondon, Armin Richter, Martin Hermle, Stefan Glunz, High efficiency n-type PERT and PERL solar cells, Photovoltaic Specialist Conference (PVSC), 2014 IEEE 40th, DOI: 10.1109/PVSC.2014.6924895.

[54] A. Cuevas, Physical Model of Back Line-Contact Front-Junction Solar Cells. J. Appl. Phys. 2013, 113 (16), 164502.

[55] Armin Richter , Jan Benick, André Kalio, Johannes Seiffe, Matthias Hörteis, Martin Hermle, Stefan W. Glunz, Towards industrial n-type PERT silicon solar cells: rear passivation and metallization scheme, SiliconPV: 17-20 April, Freiburg, Germany, 2011, doi:10.1016/j.egypro.2011.06.169.

[56] J. Melskens, B. van de Loo, B. Macco, M. Vos, J. Palmans, S. Smit and W. Kessels, “Concepts and prospects of passivating contacts for crystalline silicon solar cells,” in IEEE 42nd Photovoltaic Specialist Conference, New Orleans, 2015.

[57] E. Yablonovitch, T. Gmitter, R. M. Swanson, and Y. H. Kwark,. Appl. Phys. Lett. 47, 1211 (1986).

[58] T. Fellmeth, A. Born, A. Kimmerle, F. Clement, D. Biro, R. Preu, Recombination at Metal-Emitter Interfaces of Front Contact Technologies for Highly Efficient Silicon Solar Cells, Energy Procedia, Volume 8, 2011, Pages 115-121, ISSN 1876-6102, https://doi.org/10.1016/j.egypro.2011.06.111.

[59] S. D. Wolf, A. Descoeudres, Z. C. Holman and C. Ballif, “High-efficiency Silicon Heterojunction Solar Cells: A Review,” Green, vol. 2, no. 1, pp. 7-24, 2012.

[60] M. Taguchi, A. Yano, S. Tohoda, K. Matsuyama, Y. Nakamura, T. Nishiwaki, K. Fujita, and E. Maruyama, “24.7% Record Efficiency HIT Solar Cell on Thin Silicon Wafer”, IEEE JPV, 4, 1 (2014).

[61] Daisuke Adachi, José Luis Hernández, and Kenji Yamamoto, Impact of carrier recombination on fill factor for large area heterojunction crystalline silicon solar cell with 25.1% efficiency, Applied Physics Letters 2015 107:23, https://doi.org/10.1063/1.4937224.

[62] Kunta Yoshikawa et. al., SiliconPV (2017), Freiburg.

[63] S. D. Wolf, A. Descoeudres, Z. C. Holman and C. Ballif, "High-efficiency Silicon Heterojunction Solar Cells: A Review," Green, vol. 2, no. 1, pp. 7-24, 2012.

[64] D. Deligiannis, S. Alivizatos, A. Ingenito. D. Zhang, M. van Sebille, R.A. C. M. M. van Swaaij, M. Zeman, "Wet-chemical Treatment for Improved Surface Passivation of Textured Silicon Heterojunction Solar Cells", Energy Procedia, 55, 197-202 (2014).

[65] H. Angermann, Passivation of structured p-type silicon interfaces: Effect of surface morphology and wet-chemical pre-treatment, Applied Surface Science, Volume 254, Issue 24, 2008, Pages 8067-8074,

[66] L. Zhang et al., "Effective interface pretreatment for amorphous-crystalline silicon heterojunction solar cells," 2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC), Portland, OR, 2016, pp. 0743-0746. doi: 10.1109/PVSC.2016.7749701

[67] J.W.A. Schüttauf, et al., Journal of non-crystalline solids, 358.17: 2245-2248. 2012

[68] S. De Wolf and M. Kondo, Appl. Phys. Lett. 90, 042111 (2007).

[69] Z. C. Holman et al., "Current Losses at the Front of Silicon Heterojunction Solar Cells," in IEEE Journal of Photovoltaics, vol. 2, no. 1, pp. 7-15, Jan. 2012. doi: 10.1109/JPHOTOV.2011.2174967.

[70] Stefaan De Wolf and Michio Kondo, Nature of doped a-Si:H/c-Sia-Si:H/c-Si interface recombination, Journal of Applied Physics 105, 103707 (2009); https://doi.org/10.1063/1.3129578

[71] J. Bullock et al., "Survey of dopant-free carrier-selective contacts for silicon solar cells," in Proc. 2016 IEEE 43rd Photovolt. Spec. Conf., 2016, pp. 210–214.

[72] Frank Feldmann, Kurt-Ulrich Ritzau, Martin Bivour, Anamaria Moldovan, Siddharth Modi, Jan Temmler, Martin Hermle, Stefan W. Glunz, High and Low Work Function Materials for Passivated Contacts, Energy Procedia, Volume 77, 2015, Pages 263-270, https://doi.org/10.1016/j.egypro.2015.07.037.

[73] Melskens, J., van de Loo, B. W. H., Macco, B., Black, L. E., Smit, S., and Kessels, W. M. M. (2018). Passivating contacts for crystalline silicon solar cells: from concepts and materials to prospects. IEEE Journal of Photovoltaics, 8(2), 373-388. DOI: 10.1109/JPHOTOV.2018.2797106

[74] C. Battaglia, S.M. de Nicolás, S. De Wolf, X. Yin, M. Zheng, C. Ballif, A. Javey, Silicon heterojunction solar cell with passivated hole selective MoOx contact, Appl. Phys. Lett. 104 (2014) 113902.

[75] S. Avasthi et al., "Hole-blocking titanium-oxide/silicon heterojunction and its application to photovolt.," Appl. Phys. Lett., vol. 102, 2013, Art. no. 203901.

[76] J. Meyer et al., "Transition metal oxides for organic electronics: Energetics, device physics and applications," Adv. Mater., vol. 24, pp. 5408–5427, 2012.

[77] Jonas Geissbühler, Jérémie Werner, Silvia Martin de Nicolas, Loris Barraud, Aïcha Hessler-Wyser, Matthieu Despeisse, Sylvain Nicolay, Andrea Tomasi, Bjoern Niesen,Stefaan De Wolf, and Christophe Ballif, 22.5% efficient silicon heterojunction solar cell with molybdenum oxide hole collector , Appl. Phys. Lett. 107, 081601 (2015); https://doi.org/10.1063/1.4928747.

[78] Ibraheem Almansouri, Anita Ho-Baillie, Stephen P. Bremner, and Martin A. Green, Supercharging Silicon Solar Cell Performance by Means of Multijunction Concept, IEEE JOURNAL OF PHOTOVOLTAICS, VOL. 5, NO. 3, MAY 2015, 10.1109/JPHOTOV.2015.2395140

[79] J. Melskens, B. van de Loo, B. Macco, M. Vos, J. Palmans, S. Smit and W. Kessels, “Concepts and prospects of passivating contacts for crystalline silicon solar cells,” in IEEE 42nd Photovoltaic Specialist Conference,, New Orleans, 2015.

[80] F. Feldmann, M. Simon, M. Bivour, C. Reichel, M. Hermle, and S. W. Glunz, Carrier-selective contacts for Si solar cells, Appl. Phys. Lett. 104, 181105 (2014); https://doi.org/ 10.1063/1.4875904

[81] C. Reichel, F. Feldmann, R. Müller, R. C. Reedy, B. G. Lee, D. L. Young, P. Stradins, M. Hermle and S. W. Glunz, "Tunnel oxide passivated contacts formed by ion implantation for applications in silicon solar cells," Journal of Applied Physics, p. 118, 2015.

[82] R. Peibst, U. Römer, Y. Larionova, M. Rienäcker, A. Merkle, N. Folchert, S. Reiter, M. Turcu, B. Min, J. Krügener, D. Tetzlaff, E. Bugiel, T. Wietler, R. Brendel, Working principle of carrier selective poly-Si/c-Si junctions: Is tunnelling the whole story?, Solar Energy Materials and Solar Cells, Volume 158, Part 1,2016,Pages 60-67,

[83] G. Yang, A. Ingenito, N. v. Hameren, O. Isabella and M. Zeman, "Design and application of ion-implanted polySi passivating contacts for interdigitated back contact c-Si solar cells," Applied Physics Letters, p. 108, 2016.

[84] Anamaria Moldovan, Frank Feldmann, Martin Zimmer, Jochen Rentsch, Jan Benick, Martin Hermle, “Tunnel oxide passivated carrier-selective contacts based on ultra-thin SiO2 layers” Solar Energy Materials and Solar Cells,Volume 142, November 2015, Pages 123-127.

[85] T.F.Wietler, D. Tetzlaff, J. Krügener, M. Rienäcker, F. Haase, Y. Larionova, R. Brendel, and R. Peibst, Pinhole density and contact resistivity of carrier selective junctions with polycrystalline silicon on oxide, Applied Physics Letters 2017 110:25, https://doi.org/10.1063/1.4986924

[86] LPCVD polysilicon passivating contacts Bart (L.J.) Geerligs, Maciej Stodolny, Yu Wu, Astrid Gutjahr, Gaby Janssen, Ingrid Romijn, John Anker, Evert Bende, Hande Ciftpinar, Martijn Lenes and Jan-Marc Luchies, Workshop on Crystalline Silicon Solar Cells and Modules: Materials and Processes, Vail, Co., USA, 28 - 31 August 2016.

[87] Yu Wu, Maciej K. Stodolny, , L. J. Geerligs, Martijn Lenes, Jan-Marc Luchies, In-situ doping and local overcompensation of high performance LPCVD polysilicon passivated contacts as approach to industrial IBC cells, 6th International Conference on Silicon Photovoltaics, SiliconPV 2016, doi: 10.1016/j.egypro.2016.07.123

[88] Frank Feldmann, Ralph Müller, Christian Reichel, and Martin Hermle, Ion implantation into amorphous Si layers to form carrier-selective contacts for Si solar cells, Phys. Status Solidi RRL 8, No. 9, 767–770 (2014) / DOI 10.1002/pssr.201409312

[89] A.Richter, J.Benick, R. Müller, F.Feldmann, C. Reichel, and M. Hermle, Tunnel oxide passivating electron contacts as full-area rear emitter of high-efficiency p-type silicon solar cells. Prog. Photovolt. Res Appl. 2017, https://doi.org/10.1002/pip.2960

[90] M. Stodolny, M. Lenes, Y.Wu, G. Janssen, I. Romijn, J. Luchies and L. Geerligs, "n-Type polysilicon passivating contact for industrial bifacial n-type solar cells," in 6th International Conference on Silicon Photovoltaics, Chambery, 2016.

[91] F. Feldmann, M. Simon, M. Bivour, C. Reichel, M. Hermle and S. W. Glunz., "Efficient carrier selective p- and n- contacts for Si solar cells," Solar Energy Materials and Solar Cells, vol. 131, pp. 100-104, 2014.

[92] Stefan L. Luxembourg, Dong Zhang, Yu Wu, Mehrdad Najafi, Valerio

Zardetto, Wiljan Verhees, Antonius R. Burgers, Sjoerd Veenstra, L.J. Geerligs, Crystalline silicon solar cell with front and rear polysilicon passivated contacts as bottom cell for hybrid tandems, Energy Procedia, Volume 124, 2017, Pages 621-627, https://doi.org/10.1016/j.egypro.2017.09.091

[93] G. Yang, P. Guo, P. Procel, G. Limodio, A. Weeber, O. Isabella and M. Zeman, High-efficiency black IBC c-Si solar cells with poly-Si as carrier-selective passivating contacts, Solar Energy Materials and Solar Cells, under review (2018).

[94] G. Nogay, J. Stuckelberger, P. Wyss, E. Rucavado, C. Allebe, T. Koida, M. Morales-Masis, M. Despeisse, F.-J. Haug, P. Löper, C. Ballif, Interplay of annealing temperature and doping in hole selective rear contacts based on silicon-rich silicon-carbide thin films, Solar Energy Materials and Solar Cells 173, 18-24 (2017).

[95] M. D. Lammert and R. J. Schwartz, "The interdigitated back contact solar cell: A silicon solar cell for use in concentrated sunlight," in IEEE Transactions on Electron Devices, vol. 24, no. 4, pp. 337-342, Apr 1977, doi: 10.1109-T-ED.1977.18738.

[96] P. Procel, A. Ingenito. R. De Rose, S. Pierro, F. Crupi, M. Lanuzza, G. Cocorullo, O. Isabella and M. Zeman (2017) Opto-electrical modelling and optimization study of a novel IBC c-Si solar cell. Prog. Photovolt. Res. Appl., 25: 452-469, doi: 10.1002/pip.2871

[97] Kim, Soo Min and Chun, Seungju and Kang, Min Gu and Song, Hee-Eun and Lee, Jong-Han and Boo, Hyunpil and Bae, Soohyun and Kang, Yoonmook and Lee, Hae-Seok and Kim, Donghwan. (2015). Simulation of interdigitated back contact solar cell with trench structure. Journal of Applied Physics. 117. 074503. 10.1063/1.4913254.

[98] Kim Y-S, Mo C, Lee DY, et. al. Gapless point back surface field for the counter doping of large-area interdigitated back contact solar cells using a blanket shadow mask implantation process. Prog Photovolt Res Appl. 2017,25:989-995 https://doi.org/10.1002/pip.2910

[99] Ingenito, A, Isabella, O and Zeman, M 2016, 'Simplified process for high efficiency, self-aligned IBC c-Si solar cells combining ion implantation and epitaxial growth: Design and fabrication' Solar Energy Materials and Solar Cells, vol 157, pp. 354-365. DOI: 10.1016/j.solmat.2016.05.021.

[100] E. Franklin et. al., (2016) Design, fabrication and characterization of a 24.4% efficient interdigitated back contact solar cell. Prog. Photovolt: Res. Appl. 24: 411-427, doi: 10.1002/pip.2556

[101] K. Yoshikawa, H. Kawasaki, W. Yoshida, T. Irie, K. Konishi, K. Nakano, T. Uto, D. Adachi, M. Kanematsu, U. H. and K. Yamamoto, "Silicon heterojunction solar cell with interdigitated back contacts for a photoconversion efficiency over 26%," Nature Energy, vol. 2, 2017.

[102] Weiliang Wu, Wenjie Lin, Sihua Zhong, Bertrand Paviet-Salomon, Matthieu Despeisse, Zongcun Liang, Mathieu Boccard, Hui Shen, and Christophe Ballif, 22% efficient dopant-free interdigitated back contact silicon solar cells, AIP Conference Proceedings 1999, 040025 (2018); https://doi.org/10.1063/1.5049288

[103] https://solarbuildermag.com/news/trina-solar-hits-25-04-percent-efficiency-for-large-area-ibc-mono-crystalline-silicon-solar-cell/

[104] https://isfh.de/en/26-1-record-efficiency-for-p-type-crystalline-si-solar-cells

[105] Andrea Tomasi, Bertrand Paviet-Salomon, Quentin Jeangros, Jan Haschke, Gabriel Christmann, Loris Barraud, Antoine Descoeudres, Johannes Peter Seif, Syl-

vain Nicolay, Matthieu Despeisse, Stefaan De Wolf and Christophe Ballif, Simple processing of back-contacted silicon heterojunction solar cells using selective-area crystalline growth, Nature Energy volume 2, Article number: 17062 (2017), doi:10.1038/nenergy.2017.62.

[106] Ajeet Rohatgi, Daniel L. Meier, Bruce McPherson, Young-Woo Ok, Ajay D. Upadhyaya, Jiun-Hong Lai, Francesco Zimbardi, High-Throughput Ion-Implantation for Low-Cost High-Efficiency Silicon Solar Cells, Energy Procedia, Volume 15, 2012, Pages 10-19, https://doi.org/10.1016/j.egypro.2012.02.002.

[107] H. Hieslmair, L. Mandrell, I. Latchford, M. Chun, J. Sullivan, B. Adibi, High Throughput Ion-Implantation for Silicon Solar Cells, Energy Procedia, Volume 27, 2012, Pages 122-128, https://doi.org/10.1016/j.egypro.2012.07.039.

[108] https://www.alibaba.com/showroom/ion-implanter.html

# 2

# EXPERIMENTAL DETAILS

*ABSTRACT - This chapter shows insight on ion implantation doping technique applied in c-Si solar cells processing. First, the main synopsis of this doping technique is presented. Then, advantages of embedding it in c-Si solar cells are listed. Furthermore, all the experimental details of the solar cells presented in the next chapters are presented. Moreover, an overview of the characterization techniques is made regardless of the solar cell architecture.*

## 2.1. ION IMPLANTATION DOPING TECHNIQUE IN C-SI SOLAR CELLS



ION implantation is a doping technique widely used in integrated circuit processing. It consists in two main steps, i) introducing dopant species into the substrate accelerated by an electrical field and ii) thermal annealing to recover from implantation damage and to activate the dopants [1], as figures 2.1 sketch. The impining energy of the

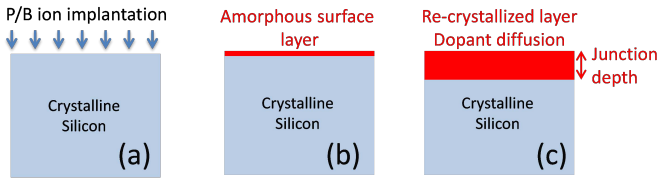


Figure 2.1: Synopsys of ion implantation doping process; (a) acceleration of dopants ions into silicon substrate, (b) consquent amorphization of c-Si surface and (c) re-crystallization of the surface, dopant activation and diffusion.

dopant ions into the substrate is usually called implantation energy and it is measured in keV. It is related to electrical field intensity needed to generate the beam containing ion dopants. The amount of dopant species reaching the target surface is named as implantation dose and it is measured in ions/cm$^2$. Other two important parameters are annealing temperature and time. Typically, temperatures between 750 and 1150 °C are employed with different temperature slopes for a variable time. When an impinging ion impacts Si substrate, its energy is transferred to silicon and a displacement into lattice is generated, therefore vacancy and interstitial defects are created, so-called Frenkel pair [2]. The energy transfer mechanism can be divided in two categories; i) nuclear stopping and ii) electronic stopping. The first one typically occurs when implanted ion's atom mass unit is rather heavy (for instance phosphorus), and it is due to collisions between impinging ion and Si atoms. The electronic stopping mechanism instead is related to the collisions between impinging ions and free carriers that determine energy transfer [3]. This type of stopping mechanism is more frequent for light atoms as Boron (B atomic mass unit is 11, while for phosphorus it is 31).

When ions imping the substrate, an amorphized layer is created by the displaced atoms randomly distributed if the dose is sufficiently high. The interface a-Si/c-Si interface should be as sharp as possible such that after annealing, all the defects will be recovered. During high temperature annealing, re-crystallization of a-Si, through a mechanism called solid-phase epitaxial regrowth, occurs. Indeed, amorphous silicon will recrystallize in ordered manner (epitaxial) and the interface a-Si/c-Si will be reduced at speed of few hundred nm/s, depending on annealing temperature [4]. In this phase, dopants also diffuse from the surface inside the c-Si bulk. From doping profile point of view, implantation energy and dose give the depth of the dopants into Si and the doping level, respectively. Annealing temperature and time define instead the junction depth, defined as the thickness for which the doping level is at least two orders of magnitude

higher than bulk's one. This doping technique matches well with c-Si solar cells processing. Indeed, ion implantation is a room-temperature technique in the first phase of the process. Therefore, it is possible to optimize independently one side of the wafer and different areas on the same side. This feature is particularly handy when a selective front surface field architecture is employed, a PERC or an IBC solar cell is processed. In particular conditions, both hole and electron contacts (Emitter / front (back) surface field) can be co-annealed in only one high-temperature annealing step [5]. It has been shown how ion implantation in an interdigitated back contacted solar cell can half the number of process steps compared to tube furnace diffusion [6], also because after ion implantation, a further step of BSG/PSG (Boron/Phophosilicate glass) removal is not needed. It has also been demonstrated how, by implanting right dose of a combination of As and $H^+$ ions, it is possible to induce a textured-like surface such that reflectance is 3% at a wavelength of 600 nm [7]. In the next paragraph, the author shows how to embed this doping technique into c-Si wafer-based solar cells in different architectures.



## 2.2. PROCESSING FRONT/REAR CONTACTED SOLAR CELLS

Unless differently specified, the starting material deployed for all solar cells shown in this thesis is as follows: 4 inches, n-type, 280-$\mu$m thick, float zone <100> with a resistivity of 2.5 Ωcm. Before any processing, standard cleaning is performed. It consists in dipping the wafer in $HNO_3$ 99% at room temperature and $HNO_3$ 69.5% at 110 °C to remove any organic or metallic contaminants. Wafer texturing is made by dipping the substrate in a solution of $H_20$, TMAH and AlkaTex at 80 °C. In all the cases, ion implantation is performed by means of a VarianEHP 500. After wafer texturing or ion implantation, the wafers are always cleaned according the aforementioned procedure. $SiN_x$ is deposited by Novellus Concept 1 at 400 °C. The metallization process, unless differently specified, is made by photolithography (10 µm-thick AZ9260 photoresist, 60 seconds of UV exposure and development in AZ400K:$H_20$ = 1:2 for 90 seconds), etching of $SiN_x$ ARC, metal evaporation and lift-off in acetone. All solar cells fabricated on 4 inches wafers are either 7.84-cm$^2$ or 9-cm$^2$ large. For the case of 7.84-cm$^2$ large solar cells, an H-grid design is employed with 5% shading. This grid contains 15 fingers that are 70-$\mu$m wide and a 640-$\mu$m wide single busbar. For the case of 9-cm$^2$ solar cells, a busbarless design is employed with 40-$\mu$m wide fingers such that 2.64% metal coverage is achieved.

### 2.2.1. HOMOJUNCTION FULLY-IMPLANTED P-DOPED BSF

Processing of P-doped BSF solar cell is straightforward. Starting from a silicon wafer (figure 2.2 (a)), after a standard cleaning, texturing is performed (step (b) in figure 2.2). Afterwards, a full-area lightly doped boron implantation is performed at front side as lateral hole transport layer. The implantation energy is 5 keV and the dose is $9{\cdot}10^{14}$ ions/cm$^2$. Then, through a photoresist mask, highly doped boron implantation ($2{\cdot}10^{15}$ ions/cm$^2$) is performed in the metal contact openings such that ohmic contact will be obtained (step (c) in figure 2.2). Since B dopant species have higher annealing temperature than phosphorous [8], a 1050 °C annealing for 60 minutes in $N_2$ environment is performed in a Tempress furnace. Then, phosporous implantation is performed (D = $2{\cdot}10^{15}$ ions/cm$^2$) at the rear side and its annealing at 850 °C for 90 minutes is done to

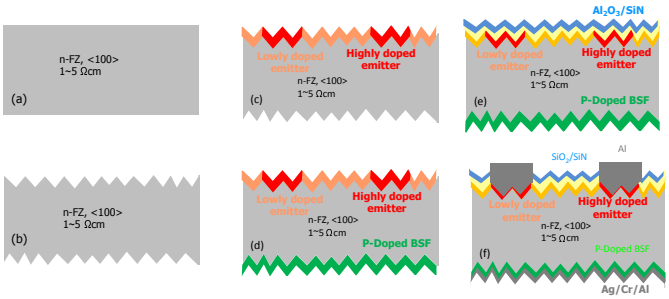


Figure 2.2: Flowchart of fully implanted front rear contacted P-doped BSF solar cell; (a) HF dip and cleaning, (b) double side wafer texturing, (c) selective B-ion implantation at the front, (d) P-ion implantation at the rear, (e) $Al_2O_3/SiN_x$ front passivation layer, (f) front/rear metallization process.

activate P dopants (figure 2.2 (d)). After stripping native/thermal $SiO_2$, wafers are placed into plasma enhanced atomic layer deposition (PE-ALD) reactor by Oxford instruments for 30 nm-thick $Al_2O_3$ deposition at the front side for passivation purpose. Then, as further passivation layer and anti-reflection coating, 60 nm-thick $SiN_x$ is deposited by plasma enhance chemical vapour deposition (PECVD) (Step (e) in figure 2.2). Finally, as sketched in figure 2.2 (f), front metallization is performed via photolithography etching of $Al_2O_3/SiN_x$ stack, evaporation of 2 $\mu$m-thick e-beam Al and then lift-off. At rear side, a stack of (200 nm) Ag / (30 nm) Cr / (2000 nm) Al is evaporated to increase internal reflectance. Cr is placed as interlayer to avoid any Al spike into Ag.

### 2.2.2. POLY-POLY SOLAR CELL

Poly-poly solar cells are fabricated by texturing only the front side of the c-Si wafer. This is achieved by covering one side with 100 nm-thick $SiN_x$ protective layer. After $SiN_x$ removal, cleaning and HF dipping, thin $SiO_x$ (approx. 1.5 nm-thick) is grown via nitric acid oxidation of silicon (NAOS), as described in [9]. The samples are then coated with

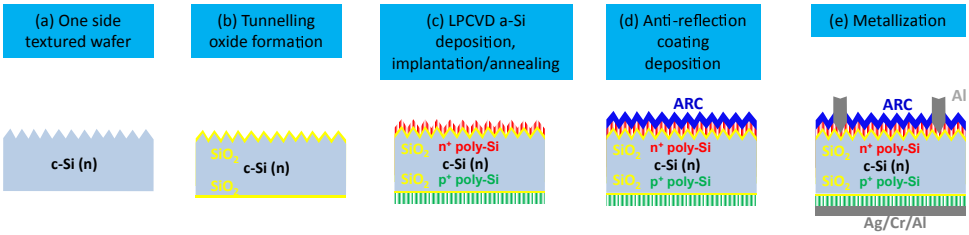


Figure 2.3: Macro-steps for fabrication of poly-poly solar cell; (a) starting material one sided textured wafer, (b) Tunneling oxide formation; (c) LPCVD a-Si deposition, implantation and annealing, (d) Anti-reflection coating deposition, (e) Front/rear metallization.

intrinsic amorphous silicon layer deposited by low-pressure chemical vapour deposition (LPCVD) by Tempress furnace at a temperature of 580°C, pressure of 150 mTorr and $SiH_4$ flow of 45 sccm. The deposition time is adapted to obtain layers with 250, 75, 35 and 20 nm (113, 40, 20 and 8 minutes, respectively). The deposited LPCVD intrinsic amorphous

silicon layers are implanted with P or B (with a dose variable between $5{\cdot}10^{15}$ and $1.2{\cdot}10^{16}$ ions/cm$^2$) and co-annealed at the optimal temperature according to the crystallization and dopants diffusion. To have excellent passivation, a-Si must crystallize and most of the active dopants should be confined into poly-Si layer, leaving only a small doping tail in c-Si bulk. In the case of 250 nm-thick poly-Si, the annealing is performed at 950 °C for 5 minutes, when poly-Si is thinned to 75 nm, 850 °C for 90 minutes is employed. In the last two cases (35 nm and 20 nm-thick poly-Si layers), the annealing is performed at 850 °C for 45 minutes. In every case, annealing is made in $N_2$ environment.

Eventually, forming gas annealing (FGA) at 400 °C for 2 hours is performed to enhance passivation quality. Afterwards, 75 nm-thick $SiN_x$ is deposited by PECVD at the front side as ARC. Then, the solar cell is metallized with lithography, etching of ARC, Al evaporation and lift-off. At rear side, Ag/Cr/Al (200 nm / 30 nm / 2 $\mu$m) stack is evaporated.

It is important to remark that in this case, doses are much higher than the homojunction case. This is due to the fact that the ion implantation is performed into an amorphous silicon layer, while in the case of homojunction solar cells, it is employed into a crystalline silicon layer. The necessity of having an important doping difference between poly-Si layer and c-Si bulk ($10^{20}$ and $10^{16}$ cm$^{-3}$, respectively) and the higher amount of defects into a-Si respect to c-Si are the reasons for higher implantation dose in poly-poly solar cells than homojunction ones.

In the case of poly-poly solar cells with decoupled front/rear poly-Si thicknesses, the fabrication process consists in repeating twice the $SiO_x$ /poly-Si deposition using a $SiN_x$ layer to protect one of the wafers surface and a poly-Si etching in between, as figures 2.4 sketch. The rear side thickness is kept at 250 nm while the front layer is varied from 250

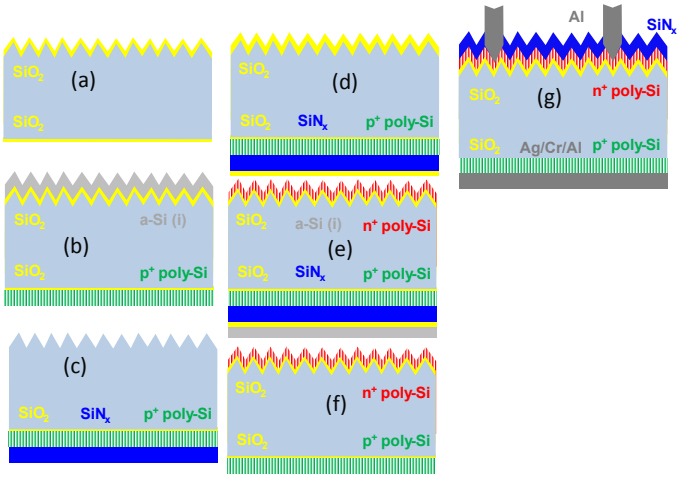


Figure 2.4: Flowchart of fully implanted poly-poly solar cell with different poly-Si thicknesses at front/rear: (a) One side texturing, cleaning, HF dip and tunnel $SiO_2$ growth, (b) double side LPCVD intrinsic amorphous silicon deposition, rear B-ion implantation and annealing (c) etching of front poly-Si, (d) $SiN_x$ rear deposition, (e), $SiO_2$/poly-Si deposition, P-ion implantation at the front side and annealing, (f) Stripping a-Si (i) and SiN on both sides, (g) anti-reflection coating and front/rear metallization.

nm down to 20 nm. The cell precursors are then processed as described above for implantation and annealing performed at optimized temperature depending on the poly-Si thickness. Forming gas annealing is eventually deployed to increase chemical passivation. To minimize reflection losses, in both cases a 75 nm-thick $SiN_x$ layer is deposited by PECVD on the textured front side and finally the cells are completed with metal contacts. At rear side a stack of Ag / Cr / Al (200 nm / 30 nm / 2 $\mu$m) is evaporated through a hard mask to define the cell area of 7.84 $cm^2$, while at the front a 2 $\mu$m-thick Al metal grid (5% metal coverage) is structured via photolithography, etching of $SiN_x$ ARC, evaporation and lift-off as well as described above. Additionally, the front grid of some solar cells is metallized with Cu plating process using evaporated titanium as seed layer.

### 2.2.3. PERFECT SOLAR CELL

In order to mitigate the possible parasitic absorption losses due to front poly-Si, another cell, named PERFeCT (Passivated Emitter Rear and Front ConTacts) is developed. The flow-chart for fabricating a rear junction PeRFeCT solar cell is reported in Figure 2.5. Macro step 1: Starting from typical silicon substrate described above, a very thin $SiO_2$ (approx. 1.5 nm) is chemically grown by means of nitric acid oxidation of silicon (NAOS) approach on the surface of both sides. Then, the wafers are loaded in a LPCVD furnace to grow, also on both sides, 250-nm thick amorphous silicon (a-Si). The wafers are sub-

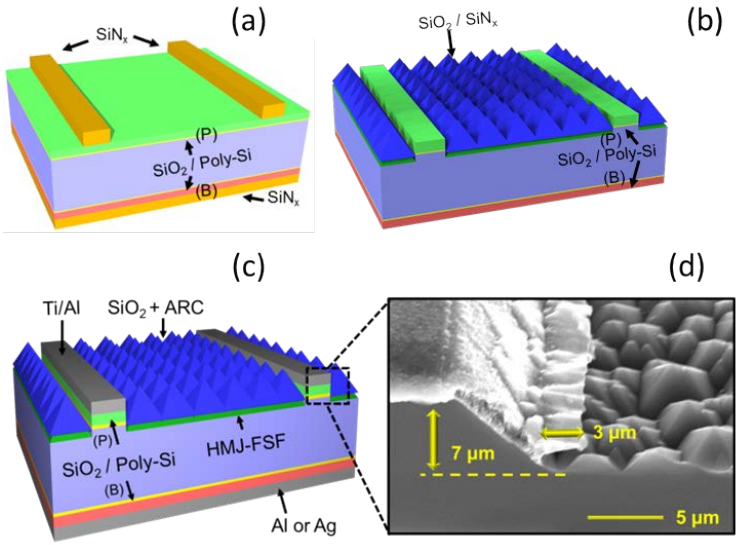


Figure 2.5: Flowchart of PeRFeCT solar cell: (a) Macro step 1: NAOS $SiO_2$, a-Si deposition, implantation, annealing (poly-Si formation) and protection with $SiN_X$ of both front pattern and rear area; (b) Macro step 2: Texturing, FSF implantation, removal of patterned $SiN_x$ (front side) and full-area $SiN_x$ (rear side), thermal $SiO_2$ formation and $SiN_x$ deposition at front side (ARC = $SiO_2$ + $SiN_x$); (c) Macro step 3: Lithography and lift-off for front metallization, rear side full-area evaporation. (d) Cross-sectional SEM micrograph depicting the black-dashed detail on the completed device.

sequently implanted with B at the back side (D = $5{\cdot}10^{15}$ ions/cm$^2$) and P at the front side (D = $6{\cdot}10^{15}$ ions/cm$^2$) and co-annealed at 950 °C for 5 minutes to activate and diffuse the dopants and concurrently crystallize the a-Si. PECVD silicon-nitride ($SiN_x$, 150 nm) is used at the front side of the sample to create the front grid pattern via photolithography and subsequent HF etching. Another protective $SiN_x$ layer is then deposited at the back side. Macro step 2: Alkaline texturing is employed to first etch the poly-Si at the front side between the front grid pattern and then to form micro-pyramids. Such texturing etches back roughly 7 µm of bulk material. The lightly-doped homojunction FSF is either ion-implanted or $POCl_3$-diffused and then annealed at 850 °C for 90 minutes in $O_2/N_2$ atmosphere to grow a 10-nm thick passivating $SiO_2$. Subsequently, the rear $SiN_x$ is removed, while a 60-nm thick $SiN_x$ is deposited at the front side for anti-reflection. Thus, our anti-reflective coating (ARC) is a dual dielectric stack formed by thermal $SiO_2$ plus $SiN_x$. Macro step 3: the front metallization (5% area coverage) is carried out via lithography and lift-off process of e-beam evaporated Al, while the rear metallization is a full-area sputtered Al or thermally-evaporated Ag. Note that described macro steps could be easily specialized to realize a front junction PeRFeCT cell by inverting the side of ion-implantation and deploying, in case of diffused front junction, $BBr_3$ or $B_2H_6$-based diffusion.

### 2.2.4. HYBRID SOLAR CELL

Hybrid solar cells are fabricated following the steps described in figure 2.6. This fabrication process is very straightforward and involves first the high thermal budget poly-Si carrier-selective passivating contacts at the rear side, then the low thermal budget silicon heterojunction passivating contacts at the front. Firstly, the $SiO_2$/ (250 nm-thick) p-type poly-Si stack is deposited on the both sides of the c-Si wafer (Figure 2.6 (a)), following the same procedure as for poly-poly solar cells. Then, the backside of the wafer is covered with $SiN_x$ to perform front-side random texturing. The front side is processed by depositing the i/n- a-Si:H stack on the textured c-Si surface (Figure 2.6 (b)) after an oxidation-etching cycle called NAOC (Nitric acid oxidation cycle), consisting in a chemical oxidation by nitric acid ($HNO_3$) and a subsequent etching in hydrofluoric acid (HF). A post-deposition annealing at 180 °C is carried out to further improve passivation qual-

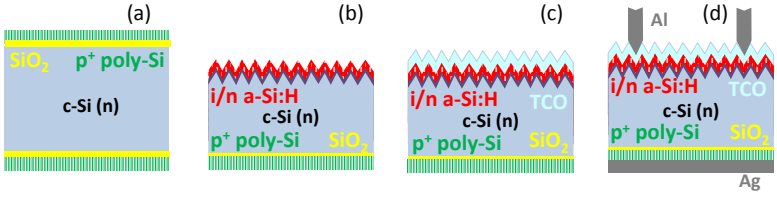


Figure 2.6: Highlights of hybrid solar cell fabrication macro-steps; (a) Double side polished wafer coated by $SiO_2$ / p-type poly-Si; (b) Front texturing and i/n a-Si:H deposition; (c) Front-TCO deposition;(d) Finished cell with front/rear metallization

ity [10] and the TCO layer is sputtered with a thickness of 75 nm to minimize reflection losses (Figure 2.6 (c)) and solve lateral conductivity issues. The last step is the metallization (Figure 2.6 (d)) with a rear metal contact consisting in stack of Ag/Cr/Al (200 / 30 /

2000 nm) thermally evaporated though a metal mask to define the cell area. The front side contact of some devices is completed with a 2 $\mu$m-thick e-beam evaporated Al layer and, afterwards, the grid is defined by photolithography and lift-off process. For some other cells the front grid is deposited via Ti-Cu plated contacts. The process consists of several steps. A Ti layer is deposited on the full area and structured by photolithography to obtain a grid pattern that acts as seed-layer for the Cu electro-plating. This method is similar to the one applied for bifacial heterojunction solar cells in Ref. [11].

## 2.3. CHARACTERIZATION TECHNIQUES

### 2.3.1. FILM CHARACTERIZATION

In order to understand the limits in performance of solar cells, it is important to analyse every single layer that compounds a device. In the case of homojunction solar cells, it is crucial to analyse passivation quality of the layers that will be used as emitter in P-doped BSF solar cell. As seen in figure 2.2 (a), B-doped textured silicon is passivated by $Al_2O_3/SiN_x$. To investigate the contribution of this single layer, we fabricate symmetric samples, also referred to as lifetime samples, as shown in figures 2.7. In this phase, it is important to understand how implantation dose, energy, annealing recipe and thickness of dielectric layers can influence passivation quality. The same applies for carrier-selective passivating contacts as $SiO_2$/doped poly-Si stack or silicon heterojunction passivation, shown in figures 2.7 (b) and (c).

All these layers are characterized by lifetime measurement tester, Sinton WCT – 120 carrier lifetime measurement setup with a method called quasi-steady state photoconductance (QSSPC) [12]. The principle of this measurement is highlighted in figure 2.8. Test sample is placed under a lamp that is flashed with a certain pulse. At this point, generation of electron-hole pairs occur in the device under test (DUT). In the case of this thesis, lifetime measurement is averaged on 20 measurements on different points of a wafer. When the generated electron hole pairs recombine, the recombination cur-

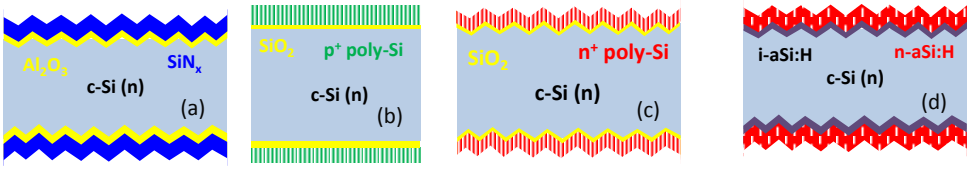


Figure 2.7: (a) Lifetime sample of B-doped silicon on textured wafer passivated by $Al_2O_3/SiN_x$, (b) Double side polished wafer passivated by $SiO_2$/doped poly-Si, (c) double side textured wafer passivated by $SiO_2$/doped poly-Si, (d) double side textured wafer passivated by i/n a-Si:H.

rent will be sensed by a coil placed underneath the DUT. At this point, it will be possible to measure effective lifetime varying injection level. The outputs of this measurement are effective lifetime ($\tau_{eff}$), recombination current density ($J_0$) and implied open-circuit voltage ($iV_{OC}$). They provide significant parameters to understand how chemical and field-effect passivation work. Typically, lifetime at low injection level ($\Delta n < 10^{15}$ cm$^{-3}$) provides indication on field effect passivation as Auger recombination is not significant.

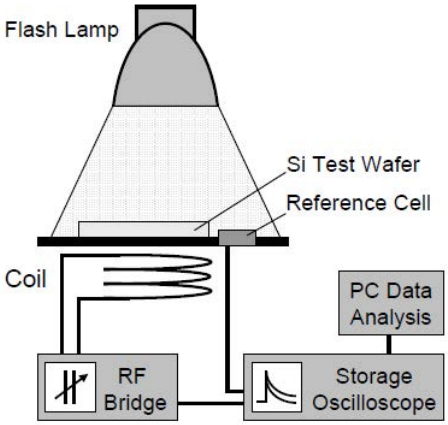


Figure 2.8: Schematic of Photoconductance decay for lifetime measurement, taken from [13]

At high injection level instead, ($\Delta n > 5{\cdot}10^{15}$ cm$^{-3}$), lifetime is limited by Auger recombination, therefore chemical passivation of the surface is the main limiting factor for recombination.

The layers used as emitter or front/back surface field are also characterized from other different perspectives. For instance, sheet resistance is measured through a 4 point probe measurement setup. By means of transfer method length (TLM) structures, contact resistance between metal (typically Al or Ag) and doped layer is evaluated. This is related to doping level of the emitter or front/back surface field. In order to understand the active doping concentration into junctions, electro capacitance voltage (ECV) measurements are performed. Especially into c-Si/$SiO_2$/doped poly-Si junction, this measurement is very important to investigate how doping distribution across the junction can influence passivation quality. When sheet resistance of the doped layer is very high (in the range of 1 k$\Omega/sq$), a transparent conductive oxide (TCO) is needed to solve any issues with lateral transport at the front, as in the case of hybrid solar cell. For this reason, also TCO should be individually characterized. A typical way of characterizing TCOs is to deposit this layer on polished glass and measure mobility, free carrier concentration and consequently conductivity through Hall measurement setup [14]. Using a spectrophotometer, it is possible to measure parasitic absorption into this layer by measuring reflection and transmission.

### 2.3.2. SOLAR CELL CHARACTERIZATION

To assess solar cells performance, the device is placed under a solar simulator and all the load conditions are applied during illumination. In the case of this thesis, class AAA Wacom WXS-156S is used to simulate AM1.5G spectrum. The solar cell is placed on a golden chuck acting as rear contact and the front side metal is contacted by a Ag probe to extract carriers. The extracted parameters are open-circuit voltage ($V_{OC}$), short-circuit current ($I_{SC}$), fill factor (FF) and efficiency ($\eta$). It is also useful to characterize solar cell

without the effect of series resistance to understand the quality of the processed junction. This diagnostic instrument is usually referred as Sinton Suns$V_{OC}$ setup and it is capable, through a flash light and means of Ag probe, to sweep along the J-V characteristic of the solar cell avoiding the effect of series resistance, calculating the so-called pseudo J-V curve and pseudo parameters as suns$V_{oc}$, pseudo-FF (pFF) and pseudo-efficiency (p$\eta$).

In order to understand the spectral response of a solar cell, external quantum efficiency is also measured through a means of light generator in combination with monochromator setup. The solar cell will be then illuminated by a monochromatic light with the same photon flux density as AM1.5G spectrum. The EQE then will be the percentage of successfully collected carriers generated by incident photons. To evaluate the photogenerated current ($J_{PH}$) from EQE it is possible to employ the following formula;

$$J_{PH} = \int_{300nm}^{1200nm} EQE\phi(\lambda)d\lambda \tag{2.1}$$

Where $\phi(\lambda)$ is the spectral photon flux density of AM 1.5G spectrum. Reflectance and transmittance are measured by a Lambda Parker spectrophotometer. It is possible to calculate then the absorption, following the formula below;

$$A(\lambda) = 1 - R(\lambda) - T(\lambda) \tag{2.2}$$

Where A,R and T are the absorption, the reflectance and the transmittance, respectively. In this way, internal quantum efficiency (IQE) is possible to be evaluated as follow:

$$IQE(\lambda) = \frac{EQE(\lambda)}{A(\lambda)} \tag{2.3}$$

IQE represents the collection efficiency of a solar cell excluding its optical losses as reflectance or transmittance [15].

## 2.4. REFERENCES

[1] L. N. Large, Ion implantation: A new method of doping semiconductors, Contemporary Physics, Volume 10, 1969 - Issue 5, Pages 505-531 | Published online: 20 Aug 2006, https://doi.org/10.1080/00107516908204407.

[2] L. Kittiratanawasin, Roger Smith, B.P. Uberuaga, Kurt Sickafus, Displacement threshold and Frenkel pair formation energy in ionic systems, Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms, Volume 268, Issue 19, 2010, Pages 2901-2906, https://doi.org/10.1016/j.nimb.2010.04.024.

[3] N. Cheung, Berkeley, http://www-inst.eecs.berkeley.edu/ee143/fa10/lectures/Lec-08.pdf

[4] H. Hieslmair, L. Mandrell, I. Latchford, M. Chun, J. Sullivan, B. Adibi, High Throughput Ion-Implantation for Silicon Solar Cells, Energy Procedia, Volume 27, 2012, Pages 122-128, https://doi.org/10.1016/j.egypro.2012.07.039.

[5] Adeline Lanterne, Samuel Gall, Yannick Veschetti, Raphaël Cabal, Marianne Coig, Frédéric Milési, Aurélie Tauzin, High Efficiency Fully Implanted and Co-annealed Bifacial N-type Solar Cells, Energy Procedia, Volume 38, 2013, Pages 283-288, https://doi.org/10.1016/j.egypro.2013.07.279.

[6] Nicholas Bateman, Paul Sullivan, Christian Reichel, Jan Benick, Martin Hermle, High quality ion implanted boron emitters in an interdigitated back contact solar cell with 20% efficiency, Energy Procedia, Volume 8, 2011, Pages 509-514, https://doi.org/10.1016/j.egypro.2011.06.174.

[7] Nirag Kadakia, Sebastian Naczas, Hassaram Bakhru, and Mengbing Huang, Fabrication of surface textures by ion implantation for antireflection of silicon crystals, Applied Physics Letters 97, 191912 (2010); doi: 10.1063/1.3515842, https://doi.org/10.1063/1.3515842.

[8] Henry Hieslmair, Ian Latchford, Lisa Mandrell, Moon Chun and Babak Adibi, Ion implantation for silicon solar cells, Intevac, Santa Clara, California, USA, https://pdfs.semanticscholar.org/03fe/0ad4f3b0efbe05813783455a7e3dbcb2396a.pdf

[9] G. Yang, A. Ingenito, N. v. Hameren, O. Isabella and M. Zeman, "Design and application of ion-implanted polySi passivating contacts for interdigitated back contact c-Si solar cells," Applied Physics Letters, p. 108, 2016.

[10] S. D. Wolf, A. Descoeudres, Z. C. Holman and C. Ballif, “High-efficiency Silicon Heterojunction Solar Cells: A Review,” Green, vol. 2, no. 1, pp. 7-24, 2012.

[11] Agata Lachowicz et. al., Reliable copper plating process for bifacial heterojunction cells, 7th Workshop on Metallization and Interconnection for Crystalline Silicon Solar Cells, 23. October 2017, Konstanz.

[12] R. Sinton, A. Cuevas and M. Stuckings, "Quasi-steady-state photoconductance, a new method for solar cell material and device characterization," in Conference Record of the IEEE Photovoltaic Specialists Conference ,1996.

[13]Stefan Rein, Lifetime Spectroscopy, A Method of Defect Characterization in Silicon for Photovoltaic Applications, edited by R. Hull, J. Parisi, R.M. Osgood and H. Warlimont, 2006.

[14]https://www.lakeshore.com/Documents/Hall-mobility-measurement-of-solar-cell-material-MagneticsTechIntl.pdf

[15]https://www.pveducation.org/pvcdrom/solar-cell-operation/quantum-efficiency

# 3

# FULLY-IMPLANTED HOMOJUNCTION FRONT/REAR CONTACTED SOLAR CELL PASSIVATED BY $AL_20_3$ AT THE FRONT AND P-DOPED BSF

*ABSTRACT - This chapter presents a fully-implanted solar cell that employs a double sided textured wafer. The front B-implanted selective emitter is passivated by $Al_2O_3$ and $SiN_x$ and a rear P-implanted layer acts as back surface field. Then, a front Al grid is structured at the front, while a Ag/Cr/Al stack is evaporated on the full-area as rear contact and back reflector. First, an investigation of $Al_2O_3$ passivation quality of $p^{++}$ surfaces is performed, then this layer is embodied in the BSF solar cell described above.*

## 3.1. INTRODUCTION

BACK surface field (BSF) solar cell holds the largest share of the c-Si solar cells market [1]. It consists typically in a p-type textured wafer front / rear contacted solar cell with the $n^+$ emitter, usually diffused, located at the front side coated by passivation layers as $SiO_2$ and $SiN_x$. The back surface field is formed by alloying silicon with aluminium at temperatures between 700 and 900 °C [2]. In this case, BSF also acts an ohmic contact to extract holes.



Typical surface recombination velocity (SRV) obtained for this contact is between 200 and 600 cm/s [3][4]. This type of solar cell, also referred as Al-BSF solar cell, is the most adopted within solar cell market due to its processing simplicity and relatively high efficiency. The world-record efficiency for this device is 20.1% on 4-$cm^2$ large solar cell [5]. As drawback, the internal reflectance given by Al is not optimal, therefore collection efficiency in the near infrared region is poor [6]. Boron doped BSF has been developed to avoid these issues [7]. This highly doped layer is usually diffused by $B_2H_6$ or $BBr_3$ precursors [8] or implanted by $BF_2$ or $BF_3$ source [9]. Then, back metal contact is evaporated or sputtered to ensure an ohmic contact and an optimal rear reflector.

In this chapter, an application of phosphorous doped back surface field solar cell is presented. Indeed, starting from n-type float zone wafer, a double side textured, fully-implanted, front junction solar cell with front B-doped front emitter and P-doped back surface field is fabricated. Front emitter is passivated by a stack of aluminium oxide ($Al_2O_3$) and silicon nitride ($SiN_x$) while rear side is metallized by a full-area silver (Ag) blanket. This chapter shows first a study of $Al_2O_3/SiN_x$ stack passivation quality of B-doped textured Si in function of the implantation dose. Then, these layers are embodied in a front/rear contacted solar cell with a full-area rear metal blanket.

## 3.2. EXPERIMENTAL DETAILS

In order to study passivation properties, symmetric samples are fabricated. These wafers are implanted by Boron ions on both sides (figure 3.1). Implantation energy is fixed at 5 keV, dose is variable between $9{\cdot}10^{14}$ and $2{\cdot}10^{15}$ ions/$cm^2$. Annealing temperature and time are fixed to 1050 °C for 60 minutes. Then, after an HF dip, $Al_2O_3$ is deposited through plasma-enhanced atomic layer deposition (PE-ALD). Afterwards, a forming gas annealing is performed at 450 °C for 20 minutes. 60 nm-thick $SiN_x$ layer

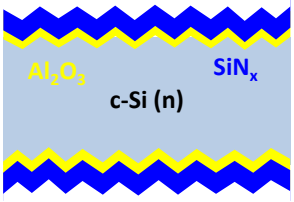


Figure 3.1: Double side textured wafer implanted by Boron and passivated by $Al_2O_3/SiN_x$ stack.

is deposited via plasma enhanced chemical vapour deposition (PECVD) for passivation

purposes. Quasi-steady-state photoconductance lifetime measurements [10] (QSSPC, using a Sinton Instruments WCT-120) are performed on the symmetric test samples. Effective lifetime ($\tau_{eff}$), implied open-circuit voltage ($iV_{OC}$) and recombination current density ($J_0$) are extracted from the measured curves. Sheet resistance is measured with a four-point probe.

For solar cells preparation, the flowchart follows the procedure already presented in paragraph 2.2.1. There is then a selective emitter at the front (Contact openings are implanted with a dose of $2{\cdot}10^{15}$ ions/cm$^2$ while non-contacted regions are implanted by $9{\cdot}10^{14}$ ions/cm$^2$). The rear side of the wafer is implanted by $2{\cdot}10^{15}$ P ions/cm$^2$. Front side passivation is performed by $Al_2O_3/SiN_x$ stack. Front Al is evaporated through a photoresist mask and full-metal blanket of Ag/Cr/Al stack is evaporated at the rear. The solar cells are characterized using a class AAA Wacom WXS-156S solar simulator to extract the following cell parameters: open-circuit voltage ($V_{OC}$), fill-factor (FF), short-circuit current density ($J_{SC}$) and efficiency ($\eta$). Sinton Suns$V_{OC}$ setup allows to measure pseudo parameters, such as pseudo-FF (p-FF) excluding the series resistance contribution. An in-house built EQE setup allows spectral response measurement.



## 3.3. RESULTS AND DISCUSSION

### 3.3.1. B-DOPED TEXTURED SI PASSIVATION QUALITY TESTS

Emitter of our P-doped BSF solar cell has been characterized from different perspectives. Figure 3.2 summarizes lifetime versus minority carrier density for double side textured, B-implanted wafer passivated by $Al_2O_3/SiN_x$ stack with three different implantation doses. By applying the lowest implantation dose ($9{\cdot}10^{14}$ ions/cm$^2$), lifetime is 1.2 ms at $10^{15}$ cm$^{-3}$ injection level. When dose is increased up to $10^{15}$ cm$^{-2}$, lifetime is similar to the previous case. By implanting double amount of B atoms ($2{\cdot}10^{15}$ ions/cm$^2$), lifetime severely degrades down to ~0.1 ms at $10^{15}$ cm$^{-3}$ injection level and it lies in that range in the whole injection level span. Table 3.1 summarizes implied $V_{OC}$, $J_0$ and sheet

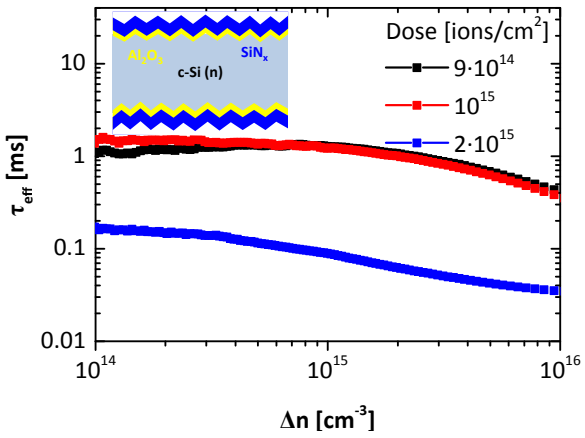


Figure 3.2: Lifetime versus injection level for textured, B-implanted, wafers passivated by $Al_2O_3/SiN_x$ stack with different implantation doses.

resistance of these layers. $iV_{OC}$ tends to decrease with increasing implantation dose. $J_0$ is instead higher with higher doses. $Al_2O_3$ is a well-known passivating material for p-type surface [11]. This is due to the high density ($10^{13}$ C/cm$^2$) of negative fixed charges that induce a depletion region with $p^+$ silicon [12]. This accumulation region induces a built-in electrical field that results in high field-effect passivation [13].

Table 3.1: implied $V_{OC}$, $J_0$ and sheet resistance of double side textured, B-doped, silicon wafers passivated by $Al_2O_3$ and $SiN_x$. These values are the average of 20 measurements on different points of the Si wafer.



| Sample | Dose [ions/cm$^2$] | $iV_{OC}$ [mV] | $J_0$ [fA/cm$^2$] | $R_{sh}$ [Ω/sq] |
|---|---|---|---|---|
| p1 | $9{\cdot}10^{14}$ | 688 | 28 | 100 |
| p2 | $10^{15}$ | 684 | 30 | 95 |
| p3 | $2{\cdot}10^{15}$ | 623 | 460 | 30 |

Moreover, $Al_2O_3$ is capable to saturate dangling bonds at Si surface since it is highly diluted in $H_2$. Indeed, typical precursors of $Al_2O_3$ in ALD reactor are trimethylaluminum (TMA) and water ($H_20$) [14]. Therefore, the whole layer ensures also high quality chemical passivation quality. This explains our results when samples p1 and p2 are deployed. Achieved lifetime is in line with the results obtained in literature with similar sheet resistance values [15][16]. When implantation dose is doubled to $2{\cdot}10^{15}$ ions/cm$^2$ instead (case of p3 in table 3.1), Auger recombination plays a main role in recombination, therefore lifetime is very low along the whole injection level span. The fact that $J_0$ of samples p1 and p2 stays in the range of 30 fA/cm$^2$ indicates that chemical passivation is excellent in both cases. Since sheet resistance values are similar, we can understand that doping level does not change too much from p1 to p2. When it comes to sample p3, $J_0$ increases to 450 fA/cm$^2$ because it is Auger-limited. This is well in accordance with literature values [17] [18] [19] showing an increasing $J_0$ with decreasing sheet resistance. Also inactive B dopants might contribute to the rise of $J_0$, but no evidence of this behaviour is shown. Sheet resistance for sample p3 is much lower because of higher doping level. Since contact resistance of sample p3 with aluminium is found to be 0.1 mΩ/cm$^2$, it is used as highly doped emitter of the final solar cell. In a selective emitter configuration, sample p1 will be used a lightly doped emitter region, while sample p3 will be used as highly doped region underneath the contacts. In this phase, P-doped BSF passivation quality is not tested because it will be directly in contact with metal, so its $J_0$ can be directly estimated without any passivation tests in 900 fA/cm$^2$.

### 3.3.2. SOLAR CELL DEMONSTRATORS

Two solar cells are fabricated via the process according to experimental details section. Selective emitter configuration is employed at the front side. Lowly doped emitter side is formed by the same features as sample p1 in table 3.1 while highly doped emitter region is formed by sample p3 in table 3.1. Two different devices are processed with different front geometry grid. Both of the devices have an H-grid shape as front contacts with different metal coverage. Indeed, SC1 has a metal coverage of 5% while for

SC2 metal coverage is 12.5%. SC2 has a larger busbar (200 $\mu$m-wide) and 140 $\mu$m-wide fingers. The solar cell area for both is 7.84 $cm^2$. In this phase, SC1 is fabricated to understand whether there are any FF losses related to relatively low metal coverage. SC2 is instead fabricated to understand how much is the short-circuit current density losses due to optical shading and also to understand any $V_{OC}$ losses related to a wider emitter region and higher recombination rate at Si-metal interface.

Table 3.2: External parameters of two different P-doped BSF solar cells with different front geometry.



| Sample | Area [$cm^2$] | Metal coverage [%] | $V_{OC}$ [mV] | $J_{SC}$ [$mA/cm^2$] | FF [%] | $\eta$ [%] | $\eta_{aperture}$ [%] | pFF [%] |
|---|---|---|---|---|---|---|---|---|
| SC1 | 7.84 | 5.00 | 622 | 39.9 | 73.0 | 18.1 | 18.6 | 83.0 |
| SC2 | 7.84 | 12.5 | 616 | 37.5 | 76.7 | 17.8 | 18.0 | 82.5 |

Solar cells results are highlighted in table 3.2. SC1 has a $V_{OC}$ of 622 mV, a $J_{SC}$ of 39.9 $mA/cm^2$ and a FF of 73%. SC2 instead has a $V_{OC}$ of 616 mV, a $J_{SC}$ of 37.5 $mA/cm^2$ and a FF of 76.7 %. FF > 70% is ensured thanks to ohmic contact formed both at rear and front contact. Since lowly doped emitter region has a sheet resistance of 100 $\Omega$/sq, lateral conductivity also contributes to the series resistance evaluated in 1.7 $m\Omega/cm^2$ for SC1 and 1.1 $m\Omega/cm^2$ for SC2. The limitation in FF comes from back-end processing. Indeed, in our wafer-based solar cells, SC1 and SC2 are processed on the same wafer. There is no emitter isolation nor any metal isolation, therefore there is cross-talking between solar cells that affects severely FF. $V_{OC}$ is lower than 630 mV because of high contact recombination given by Si/metal interface [20]. Indeed, the full-area rear metal contact induces more than 50% of the total recombination at maximum power point [21]. In SC2, $V_{OC}$ is 6 mV lower than SC1 because of added contact recombination due to higher metal coverage. Since there is a higher metal fraction, also a larger highly doped emitter is employed. This also contributes to higher recombination rate. By adding up all the $J_0$s obtained as follows:

$$J_{0tot} = J_{0bulk} + fJ_{0frontcontact} + (1-f)J_{0FSF} + J_{0rearcontact}$$

where $J_{0bulk}$ is 10 $fA/cm^2$, f is 5% or 12.5% and it is the metal coverage area fraction and the other $J_0$ given by the FSF is 30 $fA/cm^2$ and $J_0$s of the contacts are estimated to be 900 $fA/cm^2$. For the measured $J_{SC} = 39.9 mA/cm^2$, a $V_{OC}$ of 629 mV is expected and it is line with what is obtained by SC1. In the case of SC2, the ideal $V_{OC}$ is 626 mV. This $V_{OC}$ loss with the respect to the calculation is also ascribed to the fact that no spatial separation is left between highly doped emitter region opening and metal contact opening. Therefore, metal contacts and selective emitter are misaligned, introducing an additional recombination.

The difference in current instead is given by front metal optical shading. A local EQE measurement, shown in figure 3.3, characterizes the spectral response of this solar cell architecture. It is important to remark that, since this is a local EQE measurement, it is the same for both SC1 and SC2. Collection in the short wavelength is affected by parasitic absorption into $SiN_x$ and a not perfect anti-reflection coating (it is optimized for $R$ =

$0@\lambda = 600nm$). In the visible part of the spectrum, collection is almost ideal, so very little recombination occurs in the bulk or at the surface. Then, at long wavelength, free carrier absorption into rear Ag metal affects carrier collection. Figure 3.3 shows also reflectance and internal quantum efficiency. Reflectance is very low in the visible range, therefore absorption is very high in that range. Transmittance is not plotted since is zero in whole wavelength span because rear side is fully metallized. In our solar cells,



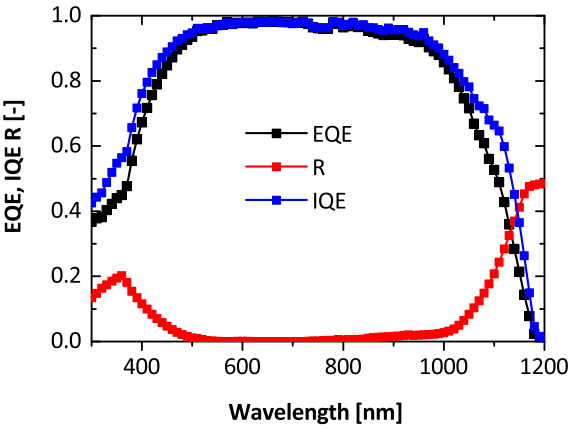


Figure 3.3: External/Internal quantum efficiency (EQE/IQE) local measurement and reflectance of P-doped BSF solar cell

$V_{OC}$ is comparable to the ones found in literature [22]. This means that the total surface recombination velocity is very similar to the state-of-the-art values. Fill factor lacks a couple of points behind due to not optimized processing of the wafer-based solar cells. Short circuit current density is more than 1 mA/cm$^2$ above literature values because Ag back metal gives much higher internal reflectance than Al [23].

## 3.4. CONCLUSION

This chapter has shown an investigation of ALD $Al_2O_3$ passivation of B-implanted textured Si surface against implantation dose. This boron-doped layer is then embedded in a fully-implanted solar cell with selective emitter at front side and P-doped back surface field. Passivation properties of $Al_2O_3$ with different implantation doses have been investigated. Lifetime of ~1 ms and $J_0$ of ~30 fA/cm$^2$ if implantation dose is kept at $10^{15}$ ions/cm$^2$ are measured. If this value is doubled, Auger recombination will be mainly responsible for poor passivation properties, with lifetime of 0.1 ms and a $J_0$ of ~400 fA/cm$^2$. Sheet resistance is decreasing from 100 to 30 Ω/sq from the lowest to the highest dose. In solar cells, a lowly doped B-implanted layer has been used as transport layer while highly doped boron has been implanted in the contact openings. On the rear side, highly doped phosphorous has been implanted to form back surface field to form an ohmic contact with rear metal. Annealing temperatures are for Boron and Phosphorous are 1050 °C and 850 °C, respectively. $Al_2O_3/SiN_x$ stack is used for passivation/anti-reflection coating. Al front grid is formed through photolithography and Ag as rear contact.

Two solar cells demonstrators have been fabricated with two different front metal coverage, 5% and 12.5%, respectively. A trade-off between short-circuit current density and FF between the two solar cells has been identified. Indeed, SC1 shows a higher $J_{SC}$ but lower FF than SC2. Moreover, also $V_{OC}$ is affected by front metal coverage. In fact, it is 6 mV higher in SC1 than SC2. FF of 73% and ~77% for SC1 and SC2, respectively, are demonstrated. The highest efficiency is 18.1% in the case of SC1. Therefore, to enhance light absorption, it is important to keep a relatively low metal coverage. This also favours less recombination losses and therefore a slightly higher $V_{OC}$. The drawback is to have transport losses due to less lateral conductivity. Furthermore, local EQE and reflectance have been measured, evaluating therefore IQE. While in short-wavelength range we have losses due to non-absorption and electrical recombination, in the visible part a minimum amount of recombination occurs. In the long wavelength range instead, current collection is poorer than in visible spectrum because free carrier absorption into rear metal occurs. Therefore, since low $V_{OC}$ is achieved, it is suggested to switch to passivating contact technology.



## 3.5. REFERENCES

[1] International Technology Roadmap for Photovoltaic (ITRPV), 2016 results including maturity report.

[2] J. del Alamo, J. Eguren, A. Luque, Operating limits of Al-alloyed high-low junctions for BSF solar cells, Solid-State Electronics, Volume 24, Issue 5, 1981, Pages 415-420.

[3] S. Narasimha, A. Rohatgi, A.W. Weeber, An optimized rapid aluminum back surface field technique for silicon solar cells, IEEE Transactions on Electron Devices ( Volume: 46, Issue: 7, Jul 1999 ), DOI: 10.1109/16.772477.

[4] P. Lolgen, C. Leguijt, J.A. Eikelboom, R.A. Steeman, W.C. Sinke, L.A. Verhoef, P.F.A. Alkemade, E. Algra, Aluminium back-surface field doping profiles with surface recombination velocities below 200 cm/s, Photovoltaic Specialists Conference, 1993., Conference Record of the Twenty Third IEEE, DOI: 10.1109/PVSC.1993.347046.

[5] Tobias Fellmeth, S. Mack, J. Bartsch, D. Erath, U. Jäger, R. Preu, F. Clement, and D. Bi, 20.1% Efficient Silicon Solar Cell With Aluminum Back Surface Field, IEEE electron device letters, vol. 32, no. 8, august 2011, DOI: 10.1109/LED.2011.2157656.

[6] Andrea Ingenito, Juan Camilo Ortiz Lizcano, Stefan L. Luxembourg, Rudi Santbergen, Arthur Weeber, Olindo Isabella, Miro Zeman, Optimized back Reflectors for Rear Diffused c-Si Solar Cells, Energy Procedia, Volume 55, 2014, Pages 94-100,https://doi.org/10.1016/j.egypro.2014.08.085.

[7] K.A. Munzer, K.T. Holdermann, R.E. Schlosser, S. Sterk, IEEE Trans. Electron Devices 46 (1999) 2055.

[8] A. F. W. Willoughby, A. G. R. Evans, P. Champ, K. J. Yallup, D. J. Godfrey, and M. G. Dowsett, Diffusion of boron in heavily doped n- and p-type silicon, Journal of Applied Physics 59, 2392 (1986); doi: 10.1063/1.336340.

[9] Mark B. Spitzer, Stanley J. Solomon, and Peter R. Younger, An effect of back-surface boron implantation on silicon solar cells, Journal of Applied Physics 53, 3926 (1982); doi: 10.1063/1.331103.

[10] R. Sinton, A. Cuevas and M. Stuckings, "Quasi-steady-state photoconductance, a new method for solar cell material and device characterization," in Conference Record

of the IEEE Photovoltaic Specialists Conference ,1996.

[11] G. Dingemans and W. M. M. Kessels, Status and prospects of Al2O3-based surface passivation schemes for silicon solar cells, Journal of Vacuum Science and Technology A 30, 040802 (2012);

[12] Schmidt, J.; Merkle, A.; Bock, R.; Altermatt, P.P.; Cuevas, A.; den Harder, N.P. (Nicolaas); Hoex, B.; van de Sanden, M.C.M.; Kessels, W.M.M.; Brendel, R. Progress in the surface passivation of silicon solar cells, Proceedings 23rd European Photovoltaic Solar Energy Conference, Valencia, Spain, 2008.

[13] Paul M. Jordan, Daniel K. Simon, Franz P.G. Fengler, Thomas Mikolajick, Ingo Dirnstorfer, 2D Mapping of Chemical and Field Effect Passivation of Al2O3 on Silicon Substrates,Energy Procedia, Volume 77, 2015, Pages 91-98,https://doi.org/10.1016/j.egypro.2015.07.014.

[14] M. D. Groner, F. H. Fabreguette, J. W. Elam, and S. M. George, Low-Temperature Al2O3 Atomic Layer Deposition, Chem. Mater. 2004, 16, 639-645 639.

[15] Haibing Huang, Jun Lv, Yameng Bao, Rongwei Xuan, Shenghua Sun, Sami Sneck, Shuo Li, Chiara Modanese, Hele Savin, Aihua Wang, Jianhua Zhao, 20.8% industrial PERC solar cell: ALD Al2O3 rear surface passivation, efficiency loss mechanisms analysis and roadmap to 24%, Solar Energy Materials and Solar Cells, Volume 161, 2017, Pages 14-30, https://doi.org/10.1016/j.solmat.2016.11.018.

[16] Pierre Saint-Cast, Jan Benick, Daniel Kania, Lucas Weiss, Marc Hofmann, Jochen Rentsch, Ralf Preu, and Stefan W. Glunz, High-Efficiency c-Si Solar Cells Passivated With ALD and PECVD Aluminum Oxide, IEEE ELECTRON DEVICE LETTERS, VOL. 31, NO. 7, JULY 2010

[17] Lachlan E. Black, Thomas Allen, Keith R. McIntosh, and Andres Cuevas, Effect of boron concentration on recombination at the p-Si–Al2O3 interface, Journal of Applied Physics 115, 093707 (2014); doi: 10.1063/1.4867643.

[18] K. R. C. (Caroline) Mok, Bas W. H. van de Loo, Ard H. G. Vlooswijk, W. M. M. (Erwin) Kessels and Lis K. Nanver, Boron-Doped Silicon Surfaces From B2H6 Passivated by ALD Al2O3 for Solar Cells, IEEE JOURNAL OF PHOTOVOLTAICS, VOL. 5, NO. 5, SEPTEMBER 2015, DOI: 10.1109/JPHOTOV.2015.2438640.

[19] A. J. Wolf, S. M. Mack, R. C. G. Naber, A. H. G. Vlooswijk, U. Belledin, E. Lohmüller, S. Lohmüller, Optimization of BBr3 Diffusion Processes for n-Type Silicon Solar Cells, 31st European Photovoltaic Solar Energy Conference and Exhibition, EU PVSEC 2015 : 14 to 18 September 2015, Hamburg, Germany, pp.637-641, DOI: 10.4229/EUPVSEC20152015-2AV.2.5

[20] A Kaminski, B Vandelle, A Fave, J.P Boyeaux, Le Quan Nam, R Monna, D Sarti, A Laugier, Aluminium BSF in silicon solar cells, Solar Energy Materials and Solar Cells, Volume 72, Issues 1–4, 2002, Pages 373-379, https://doi.org/10.1016/S0927-0248(01)00185-4.

[21] C. Battaglia, A. Cuevas and S. D. Wolf, "High-efficiency crystalline silicon solar cells: status and perspectives," Energy Environ. Sci., vol. 9, pp. 1552-1576, 2016.

[22] S. Gatz, K. Bothe, J. Müller, T. Dullweber, R. Brendel, Analysis of local Al-doped back surface fields for high efficiency screen-printed solar cells, Energy Procedia, Volume 8, 2011, Pages 318-323, https://doi.org/10.1016/j.egypro.2011.06.143.

[23] A. Ristow, M. Hilali, A. Ebong and A. Rohatgi, Screen-printed back surface re-

flector for light trapping in crystalline silicon solar cells, 17th European Photovoltaic Solar Energy Conference and Exhibition; Munich, Germany; October 22-26, 2001, http://hdl.handle.net/1853/26164.

# 4

# IMPLANTATION-BASED PASSIVATING CONTACTS FOR CRYSTALLINE SILICON FRONT/REAR CONTACTED SOLAR CELLS

*ABSTRACT - In this work we develop $SiO_x$/poly-Si carrier-selective contacts grown by low pressure chemical vapor deposition and boron- or phosphorus-doped by ion implantation. We investigate their passivation properties on symmetric structures while varying the thickness of poly-Si in a wide range (20 - 250 nm). Dose and energy of implantation as well as temperature and time of annealing were optimized, achieving implied open-circuit voltage well above 700 mV for electron-selective contacts regardless of the poly-Si layer thickness. In case of hole-selective contacts, the passivation quality decreases by thinning the poly-Si layer. For both poly-Si doping types, forming gas annealing helps to augment the passivation quality. The optimized doped poly-Si layers are then implemented in c-Si solar cells featuring $SiO_2$ / poly-Si contacts with different polarities on both front and rear sides in a lean manufacturing process free from transparent conductive oxide (TCO). At cell level, open-circuit voltage degrades when thinner p-type poly-Si layer is employed, while a consistent gain in short circuit current is measured when front poly-Si thickness is thinned down from 250 to 35 nm (up to +4 mA/cm$^2$). We circumvent this limitation by decoupling front and rear layer thickness obtaining, on one hand, reasonably high current ($J_{SC\text{-}EQE}$ = 38.2 mA/cm$^2$) and, on the other hand, relatively high $V_{OC}$ of 690 mV. The best TCO-free device using Ti-seeded Cu-plated front contact exhibits a fill factor of 75.2% and conversion efficiency of 19.6%.*

Parts of this chapter have been submitted to Progress in Photovoltaics, G. Limodio et. al., PiP, 2019, Under Review

## 4.1. INTRODUCTION

VERY low surface recombination velocity at the c-Si/metal interface is required to enhance the conversion efficiency of a c-Si solar cell [1]. This task is successfully achieved by inserting a layer separating the c-Si absorber from the metal contact, that properly passivates the c-Si surface and, at the same time, selectively collects one type of carriers [2]. A first type of such carrier-selective passivating contact (CSPC) employs a stack of intrinsic and doped hydrogenated amorphous silicon (a-Si:H) grown on both sides of c-Si wafer, enabling open-circuit voltages ($V_{OC}$s) up to 750 mV [3]. Kaneka has recently reported a conversion efficiency ($\eta$) above 25% for a front/back-contacted (FBC) c-Si solar cell [4] and a world record efficiency of 26.7% for an interdigitated back-contacted (IBC) architecture [5]. However, due to electrical degradation of a-Si:H layers for temperature above 250 ºC [6], such device concept has limited compatibility with standard solar cell manufacturing processes. An alternative type of CSPC featuring higher thermal budget was proposed by Yablonovich et al. [7] and is the so-called semi-insulating polycrystalline silicon (SIPOS) hetero-structure as a mixture of micro-crystalline silicon and silicon oxide. Several research groups [8][9] have recently further developed such device scheme consisting of an ultra-thin silicon oxide ($SiO_2$) (< 2 nm) layer grown on the c-Si surfaces [10] coated by in- or ex-situ doped polycrystalline silicon (poly-Si) layer deposited via low pressure/plasma-enhanced chemical vapor deposition (LP/PECVD) techniques [11].

The thin $SiO_2$ provides excellent chemical passivation of c-Si interface defects and also acts as a barrier that allows the collection of only majority carriers at poly-Si contact [12]. The transport principle at this junction may occur via tunneling [13][14] and/or via pin-holes present at c-Si/$SiO_2$ interface [15]. This passivation scheme has proved to give excellent passivation properties [16], with implied open-circuit voltage ($iV_{OC}$) obtained up to 730 mV and saturation current density ($J_0$) well below 10 fA/cm$^2$. Moreover, as typical process temperatures are above 900 °C, such devices exhibit high thermal stability and are, in principle, compatible with conventional metallization techniques based on screen-printing. Poly-silicon based CSPCs are successfully applied at cell level using different device architectures, such as IBC solar cells [17][18] with a remarkable efficiency over 26% [19], or bifacial [20] and FBC solar cells [21][22]. Similarly, promising hybrid concepts combining homo-junction with poly-Si CSPC are under research as front homo-junction and CSPC at the back side [23] with experimental $\eta$ very close to 26% and selective front surface field (FSF) architecture and rear poly-Si CSPC [24] with modelled $\eta$ also in the range of 26%. Poly-Si has been applied at the front side of FBC solar cells with transparent conductive oxide (TCO) [25] or with $SiN_x$ as anti-reflection coating [26] for tandem device applications or at the rear side of industrial n-type wafer-based FBC cells [27] [28].

However, placing thick poly-Si layers at the front side of a solar cell induces consistent parasitic absorption [29] estimated in the range of 1.5 mA/cm$^2$ each 30 nm of poly-Si [30]. Furthermore, poly-Si accounts for free carrier absorption (FCA) in the near infrared (NIR) wavelength range [31]. Therefore, into an attempt to obtain more transparent high-thermal budget CSPCs, poly-Si layer has been alloyed with oxygen [32][33] or carbon [34] and applied in FBC devices in combination with a-Si:H-based CSPC at the textured front side [35][36]. Notwithstanding the promising results at both passivation

level and cell level, these alloys are still not optically optimal [32] [37], presenting higher absorption coefficient than c-Si in the visible range and FCA in the NIR range, just like poly-Si [38]. Thus, to minimize these optical losses due to poly-Si layers while keeping high their passivation quality, a careful surface engineering has to be performed. In this chapter, we present the optimization of n- and p-type implanted poly-Si contacts deposited by LPCVD on top of ultra-thin chemical $SiO_2$.

We optimized both implantation dose/energy and annealing time/temperature while thinning the poly-Si layer thickness from 250 nm to 20 nm. The effect of the layer thickness on the passivation quality is investigated monitoring effective carriers' lifetime ($\tau_{eff}$), implied open-circuit voltage ($iV_{OC}$) and saturation current density ($J_0$). Supported by TCAD simulations, we also evaluate the effects of doping profile in poly-Si / $SiO_2$ / c-Si stack on passivation quality and band alignment for carrier collection. The investigated layers are tested on completed devices in a rear emitter configuration with a textured-front and a flat-rear side in a lean and TCO-free manufacturing process. We discuss the relation among short-circuit current density ($J_{SC}$), open-circuit voltage ($V_{OC}$) and fill factor (FF) for different poly-Si thicknesses.



## 4.2. EXPERIMENTAL DETAILS

As well as in chapter 3, the passivation study is carried out by fabricating symmetric samples, as figure 4.1 (a) and (b) sketch. Therefore, double side polished wafers passivated by thin $SiO_2$/ B-doped poly-Si and double side textured wafers passivated by thin $SiO_2$/ P-doped poly-Si are fabricated as described in chapter 2. Phosphorous (P) and boron (B) are implanted, selecting an energy of 10 keV and 5 keV, respectively, with variable dose from $5{\cdot}10^{15}$ to $1.2{\cdot}10^{16}$ ions/cm$^2$. Respect to chapter 3, a higher implantation dose is employed to obtain higher doping level into poly-Si. Afterwards, the samples are annealed in a tube furnace to activate and diffuse the implanted dopants within the a-Si lattice and, concurrently, to obtain poly-Si layer. Annealing temperature for samples in Figure 4.1 (a) and (b) is either 950 °C or 850 °C and annealing time is variable between 5 and 90 minutes, depending on the thickness of the poly-Si layer. Temperature is lower than 1050 °C. It is lower than in Chapter 3 to obtain shallower junction depths and also to avoid ruptures into thin $SiO_2$. Eventually, a forming gas annealing (FGA) at 400 °C for 2 hours (10% $H_2$ in $N_2$) is performed to enhance chemical passivation at c-Si/$SiO^2$ interface [39]. Quasi-steady-state photoconductance lifetime measurements (QSSPC) [40] are performed using a Sinton Instruments WCT-120 on the symmetric samples in Figure 4.1 (a) and (b) to assess the surface passivation quality of the fabricated structures. Effective carriers' lifetime ($\tau_{eff}$) is evaluated at low injection level ($\Delta n = 10^{15}$ cm$^{-3}$), implied open-circuit voltage ($iV_{OC}$) and recombination current density ($J_0$) are extracted from the measured curves at high injection level ($\Delta n = 10^{16}$ cm$^{-3}$). Furthermore, electrocapacitance voltage (ECV) technique is employed on the same samples to investigate the active doping concentration profile from the doped layers into the c-Si substrate.

Solar cells are fabricated by combining the layer stacks optimized in a poly-poly configuration (see Figure 4.1 (c)). The process follows the flowchart already explained in paragraph 2.2.2. Front, textured side is passivated by thin $SiO_x$/n-type poly-Si while polished rear side is passivated by thin $SiO_x$/p-type poly-Si. $SiN_x$ as anti-reflection coating, front Al contacts and rear Ag/Cr/Al stack complete the solar cell. The reason to locate

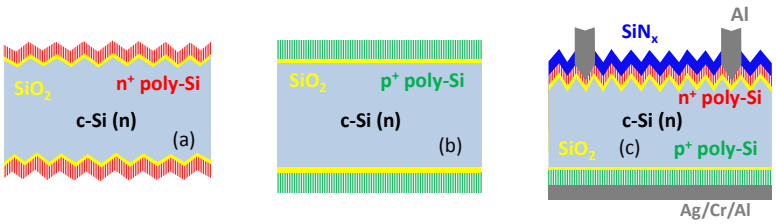


Figure 4.1: Symmetric samples with a) $SiO_x$/n-type poly-Si on textured c-Si wafer, b) $SiO_x$/p-type poly-Si on flat c-Si wafer and (c) poly-poly solar cell sketch with variable front/rear poly-Si thicknesses between 250 nm and 20 nm.



the hole contact at rear side is to avoid holes-based current crowding at the front that hinders fill factor [24], as also demonstrated in [41] for the case of silicon heterojunction solar cells. Additionally, the front grid of some solar cells is Cu-plated by means of a mask-less process (plating current density of 576 mA/cm$^2$ for 1500 seconds) using evaporated titanium as seed layer [42]. The development of this technique will be shown in Chapter 7. For solar cells with decoupled front/rear poly-Si thicknesses, the fabrication process consists in repeating twice the $SiO_2$/poly-Si deposition using a $SiN_x$ layer to protect one of the wafer's surface and a poly-Si etching in between. We keep the rear side thickness at 250 nm while the front layer is varied from 250 nm down to 20 nm.

The solar cells are characterized using a calibrated, class AAA, Wacom WXS-156S solar simulator to extract the following cell parameters: $V_{OC}$, FF, $J_{sc}$ and $\eta$. External quantum efficiency (EQE) is measured by an in-house built setup and a calibrated mono-silicon diode with known spectral response was used as a reference. Sinton Suns$V_{OC}$ setup allows to measure pseudo parameters, such as pseudo-FF (pFF), which excludes the series resistance contribution. Accurate opto-electrical simulations of poly-poly solar cells are performed using a modelling framework based on TCAD Sentaurus [43][44][45][46][47], combining thin film optics and opto-electrical properties, such as free carrier absorption. The simulated structure is reported in Figure 4.1(c) using experimentally-extracted wavelength-dependent refractive index of poly-Si [48]. From each simulated absorption profile, equivalent photocurrent densities are calculated. We assume here that all the light absorbed in the front or rear layers (except the c-Si absorber) is parasitically absorbed and contributes therefore to current losses.

## 4.3. RESULTS AND DISCUSSION

### 4.3.1. C-SI SURFACE PASSIVATION BY POLY-SI SELECTIVE CONTACTS

Table 4.1 summarizes the implantation parameters tested for the $SiO_2$ / n-type poly-Si stack on textured substrates with the symmetric structure reported in figure 4.1 (a). The poly-Si layer thickness is kept constant at 250 nm for the three samples fabricated while the P implantation is performed at an energy of 10 keV. Sample n1 receives a dose of $7.5 \cdot 10^{15}$ ions/cm$^2$, while for samples n2 and n3 implantation dose is $10^{16}$ ions/cm$^2$. All the samples undergo the same annealing process for 5 minutes at temperature of 950 °C and the FGA is tested only for sample n3. In this phase, employing an annealing temperature of 850 °C is not taken into consideration because it does not induce

enough dopant diffusion. Surface passivation quality of the fabricated samples is reported in the same Table 4.1. Sample n1, implanted at lower dose, exhibits relatively low performance with $\tau_{eff}$ of 0.8 ms, $J_0$ = 72 fA/cm$^2$ and $iV_{OC}$ = 664 mV. When implantation dose is increased up to $10^{16}$ ions/cm$^2$ (sample n2), lifetime increases up to 1.8 ms and $J_0$ decreases to 39 fA/cm$^2$ with improved $iV_{OC}$ up to 688 mV. The better passivation properties observed for increased implantation dose can be explained by the higher doping concentration into poly-Si layer that enhances carrier selectivity inducing a stronger electrical field across the junction [49]. Finally, we test the effect of FGA on the investigated stack (sample n3), measuring a significant improvement in the passivation properties. In particular, we measured $\tau_{eff}$ of 4.6 ms, $J_0$ = 14.5 fA/cm$^2$ and $iV_{OC} > 700$ mV. Sample n3 benefits from the FGA treatment owing to the diffusion of $H^+$ atoms into the stack, enhancing chemical passivation at the c-Si / $SiO_2$ interface [50][39]. Similar results about FGA have been reported in [51], although in our case the implantation dose is higher than typical literature values [52][53] with similar annealing conditions. Next,



Table 4.1: Lifetime measurements of symmetric textured wafers passivated by $SiO_x$/250 nm-thick n-type poly-Si shown in 4.1 (a)

| Sample | Energy [keV] | Dose [ions/cm$^2$] | Annealing T/t [°C/min] | FGA | $\tau_{eff}$ @ $10^{15}$ cm$^{-3}$ [ms] | $J_0$ [fA/cm$^2$] | $iV_{OC}$ [mV] |
|---|---|---|---|---|---|---|---|
| n1 | 10 | $7.5\cdot 10^{15}$ | 950/5 | No | 0.8 | 72.0 | 664 |
| n2 | 10 | $10^{16}$ | 950/5 | No | 1.8 | 39.0 | 688 |
| n3 | 10 | $10^{16}$ | 950/5 | Yes | 4.6 | 14.5 | 709 |

we investigate the effect of poly-Si layer thickness on passivation. Figure 4.2 depicts the phosphorous concentration profile across the $SiO_2$ / poly-Si structure for the case of 75-nm thick poly-Si implanted with fixed dose of $10^{16}$ ions/cm$^2$ and annealed at 950 °C for 5 minutes and 850 °C for 90 minutes, respectively. The sample annealed at 950 °C (green curve in Figure 4.2), confines $10^{20}$ P atoms/cm$^3$ into poly-Si layer and a similar amount is diffused into c-Si bulk. For the case of 850 °C (red curve in Figure 4.2), the junction depth is shallower with $10^{20}$ P atoms/cm$^3$ confined into the poly-Si layer. The doping profile decreases with a sharp tail into the c-Si with $10^{18}$ atoms/cm$^3$ near the c-Si / $SiO_2$ interface. This doping diffusion into c-Si bulk facilitates carrier transport across the junction [54]. Consequently, the differences observed in the doping profiles are reflected in passivation quality. We measure $\tau_{eff}$ of 0.8 ms and $\tau_{eff}$ of 2.2 ms for the sample annealed at 950 °C and 850 °C, respectively. This difference in passivation performance suggests that a weak field-effect passivation occurs in case doping is constant across the junction. After the optimal temperature is found, we optimize the doping level for the 75-nm thick n-type poly-Si by sweeping implantation dose in the range from $0.5\cdot 10^{16}$ ions/cm$^2$ to $1.2\cdot 10^{16}$ ions/cm$^2$. Annealing temperature is kept at 850 °C for 90 minutes. The corresponding carrier lifetime curves versus minority carrier density are reported in Figure 4.3. The layer implanted with a dose of $5\cdot 10^{15}$ ions/cm$^2$ exhibited the lowest $\tau_{eff}$ (0.5 ms), with a poor behaviour at low injection level. By increasing the dose up to $7.5\cdot 10^{15}$ and $10^{16}$ ions/cm$^2$, the lifetime curves shift up in the entire injection level with a $\tau_{eff}$ = 2 ms. Further increasing the dose up to $1.2\cdot 10^{16}$ ions/cm$^2$, $\tau_{eff}$ degrades

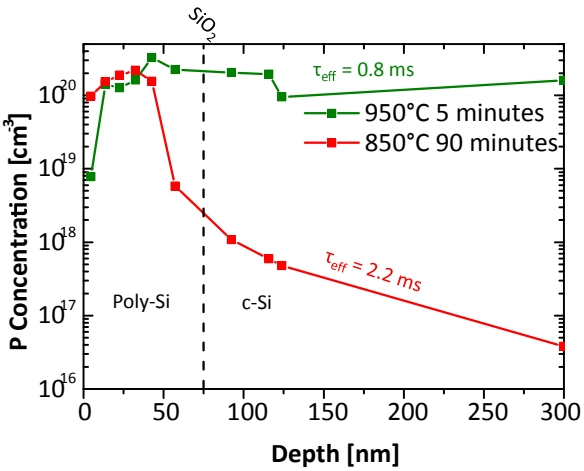


Figure 4.2: ECV measurement of phosphorous doping concentration profile as function of the depth in 75-nm thick n-type poly-Si contact implanted with a dose of $10^{16}$ ions/cm$^2$ and energy of 10 keV and annealed at different temperatures and times. Reported $\tau_{eff}$ indicated for each sample is probed at $\Delta n = 10^{15}$ cm$^{-3}$. It is important to note that oxide scale might be slightly off in the ECV measurement.

down to 0.5 ms with a severe effect on the surface passivation ($iV_{oc}$ = 663 mV). As for the case of 250-nm thick poly-Si, implantation dose lower than $10^{16}$ ions/cm$^2$, does not induce such strong electric field across the junction to increase carrier-selectivity. On the other hand, a dose higher than $10^{16}$ ions/cm$^2$ induces lower lifetime. This is because the resulting junction is Auger-limited with a $J_0 = 95 fA/cm^2$, according to a qualitative simulation run by EDNA 2 [55]. The optimum for 75-nm thick poly-Si layer is found indeed for a dose of $10^{16}$ ions/cm$^2$. In this case, $J_0 = 14 fA/cm^2$ and $iV_{OC} = 703 mV$ indicate a trade-off between optimal surface vs Auger recombination mechanisms. Figure 4.4 (a) shows optimal doping profile for 250-nm, 75-nm and 35-nm thick poly-Si layers and their corresponding $\tau_{eff}$ and $J_0$. For the 35-nm thick poly-Si layer, we obtain a sharp doping profile for an annealing performed at 850 °C for 45 minutes. We obtain a not fully-optimized 75-nm thick layer because its doping profile (shown in Figure 4.4(a)), albeit decaying as steeply as the other two cases into c-Si bulk, does not mantain a strong doping un-balance at poly-Si/$SiO_2$/c-Si interface as close as possible to the poly-Si / $SiO_2$ interface. Therefore, a less effective field-effect passivation is in place for this sample. Consequently, both 250-nm and 35-nm thick poly-Si layers exhibit $\tau_{eff}$ above 4.5 ms, while the 75-nm thick one is limited at 2.3 ms. The three samples depicted in figure 4.4(a) have $10^{20}$ atoms/cm$^3$ into the poly-Si layer, while the doping tail in the c-Si bulk becomes not significant after about 100 nm. Figure 4.4 (b) summarizes these $\tau_{eff}$ results while measuring a fairly constant $J_0 = 14.5 fA/cm^2$, independently from the poly-Si thickness. This means that the chemical passivation is excellent in all the three samples.

A similar study is performed on B-implanted poly-Si CSPC on flat substrate. Table 4.2 shows $\tau_{eff}$, $J_0$ and $iV_{OC}$ in as-annealed condition and after FGA treatment for the case of 250-nm thick poly-Si layer. The samples are implanted with 5 keV as ion en-

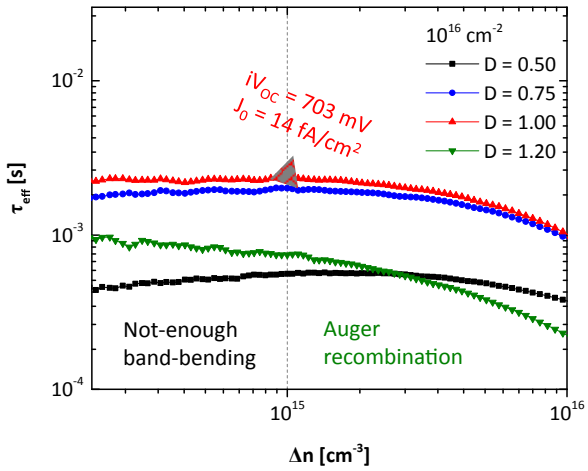


Figure 4.3: QSSPC lifetime measurements of 75-nm thick n-type poly-Si symmetric samples on textured wafer sweeping implantation dose (D) from $0.5 \cdot 10^{16}$ ions/cm$^2$ to $1.2 \cdot 10^{16}$ ions/cm$^2$.

ergy and a dose of $5 \cdot 10^{15}$ ions/cm$^2$. Annealing is at temperature of 950 °C and time is 5 minutes. For sample p1, after annealing for dopants activation and crystallization,

Table 4.2: Implantation and annealing parameters for symmetric samples on polished wafers with 250 nm-thick B-doped poly-Si. Measured passivation quality parameters: effective lifetime $\tau_{eff}$, $J_0$ and $iV_{OC}$.

| Sample | Energy [keV] | Dose [ions/cm$^2$] | Annealing T/t [°C/min] | FGA | $\tau_{eff}$ @ $10^{15}$ cm$^{-3}$ [ms] | $J_0$ [fA/cm$^2$] | $iV_{OC}$ [mV] |
|---|---|---|---|---|---|---|---|
| p1 | 5 | $5 \cdot 10^{15}$ | 950/5 | No | 3.8 | 19.0 | 704 |
| p2 | 5 | $5 \cdot 10^{15}$ | 950/5 | Yes | 5.2 | 12.5 | 716 |

we measure $\tau_{eff}$ of 3.8 ms, $J_0 = 19 fA/cm^2$ and $iV_{OC} = 704 mV$. For sample p2, which subsequently received also FGA, it is evident that hydrogenation treatment via FGA is capable of increasing lifetime by 25% relative with respect to p1 with $\tau_{eff}$ of 5.2 ms and $J_0 = 12.5 fA/cm^2$. Furthermore, $iV_{OC}$ increases by more than 10 mV, up to 716 mV. As in case of the electron-selective contact, we investigate the effect of thinning the p-type poly-Si layer on passivation properties. When the p-type poly-Si layer is 75-nm thick, an annealing at 950 °C is not suitable to perfectly confine the boron doping into poly-Si layer. For this reason, annealing temperature is scaled down to 850 °C and time is increased to 90 minutes. As for n-type poly-Si layers, a series of different implantation doses from $5 \cdot 10^{15}$ to $10^{16}$ ions/cm$^2$ is performed. Figures 4.5 show QSSPC lifetime curves of symmetric samples passivated by $SiO_2$ / p-type poly-Si stack with different implantation doses and ion energy of 5 keV.

By increasing implantation dose, the curves shift towards higher carrier lifetimes. The highest passivation quality is measured for $10^{16}$ ions/cm$^2$ with $\tau_{eff}$ of 2.3 ms, $J_0 = 23 fA/cm^2$ and $iV_{OC} = 691 mV$. For lower doses, as the doping level into poly-Si is not

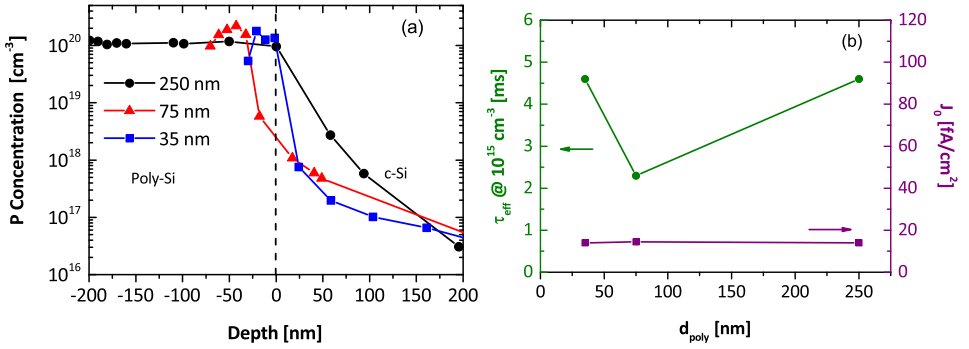


Figure 4.4: (a) ECV measurement of phosphorous doping concentration profile as function of the depth in 250-nm, 75-nm and 35-nm thick n-type poly-Si; (b) $\tau_{eff}$ and $J_0$ versus poly-Si thickness.

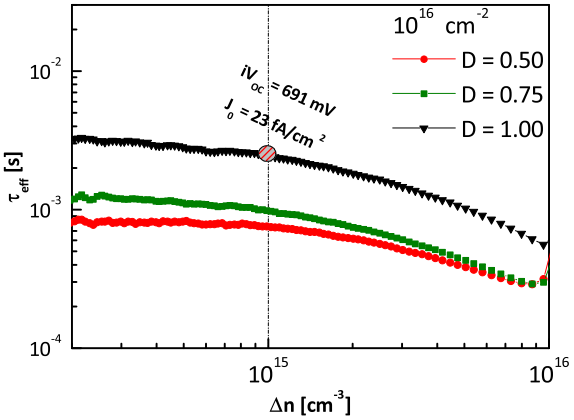


Figure 4.5: QSSPC lifetime curves of 75-nm thick p-type poly-Si on flat wafer sweeping implantation dose (D) for a fixed ion energy at 5 keV. The samples are annealed at 850 °C for 90 minutes.

optimal, lifetime is limited at ~1 ms. Figure 4.6 (a) shows doping profiles of 250-nm, 75-nm and 35-nm thick p-type poly-Si samples. In the case of 250-nm thick layer, $10^{20}$ B atoms/cm$^3$ are confined well into the poly-Si layer and its doping tail in c-Si bulk, ensuring $\tau_{eff} > 5$ ms.

For the 75-nm thick sample (see figure 4.6 (a), red line), the doping level into poly-Si is around $3 \cdot 10^{20}$ B atoms/cm$^3$ and it decreases in c-Si bulk such that after 100 nm in c-Si bulk there are $10^{18}$ B atoms/cm$^3$, giving a weaker field-effect passivation ($\tau_{eff}$ of 2.3 ms) than the case of 250-nm thick poly-Si.

When 35-nm thick poly-Si is deposited, the B-doping concentration at c-Si/$SiO_2$/poly-Si junction is on the order of $10^{20}$ cm$^{-3}$ on both sides of the $SiO_2$ tunnelling layer, causing almost no field-effect passivation and therefore lifetime is 0.5 ms. In this case, also Auger recombination plays a role in the recombination processes. Since boron

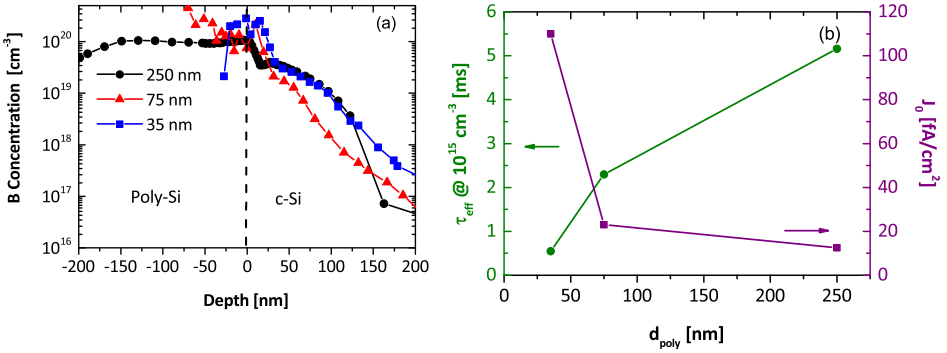


Figure 4.6: (a) ECV measurement of boron doping concentration in 250-nm, 75-nm and 35-nm thick B-doped poly-Si and (b) corresponding $\tau_{eff}$ and $J_0$ measured on symmetric samples on double side polished wafer as function of poly-Si thickness.



is a light atom (atomic mass unit of 11), its implantation depth into silicon is greater than that of phosphorous [56] in specific conditions; therefore, having already limited the annealing temperature to 850 °C to prevent unwanted diffusion of boron into the c-Si bulk, the annealing time could be reduced further. In this case, also solid solubility is playing a role for dopant diffusion. Segregation coefficient between Si and $SiO_2$ might be negligible because the annealing is always performed in $N_2$ environment. On the other hand, boron typically needs higher activation temperatures than phosphorous [56], thus narrowing the optimization window of B-implanted poly-Si. In the two thicker layers, junction depths are optimized such that doping unbalance at the junction is high enough to induce strong electrical field, while in the 35-nm thick case diffusion of dopants is rather high causing weak electrical field at the junction and also high Auger recombination.

Furthermore, we observe that the optimized implantation dose for thinner poly-Si layer is higher than the one used for 250-nm thick layer. This might be caused by a more complicated incorporation of B dopants into thinner poly-Si layers. A possible way to minimize junction depth is to use lower implantation energy [57], which is unfortunately not possible in our setup. Figure 4.6 (b) summarizes all the results obtained so far about p-type poly-Si passivating contact for different thicknesses. It shows that $\tau_{eff}$ increases when poly-Si thickness increases with an opposite trend for $J_0$. For the 35-nm thick B-doped poly-Si layer, low lifetime of 0.5 ms, $iV_{OC}$ of 655 mV and $J_0 = 100 fA/cm^2$ are obtained, indicating overall that also chemical passivation is affected, most likely by inactive clusters of B atoms acting as recombination centers. For both hole-selective and electron-selective contacts, annealing temperature is higher when the poly-Si thickness is in the range of 250 nm. This is also partially confirmed in [58], where a $BBr_3$ diffusion instead of ion implantation is used as ex-situ doping technique. Finally, also for our hole-selective poly-Si contacts, implantation doses are much higher than the state of the art [59]. We believe that this might be due to different density of the poly-Si layers. For a deeper understanding of our results, we simulated, by means of our TCAD Sentaurus modelling platform [47], the energy band diagrams of both n-type and p-type poly-Si CSPCs based on the measured doping concentration profiles shown in 4.4 (a) and figure

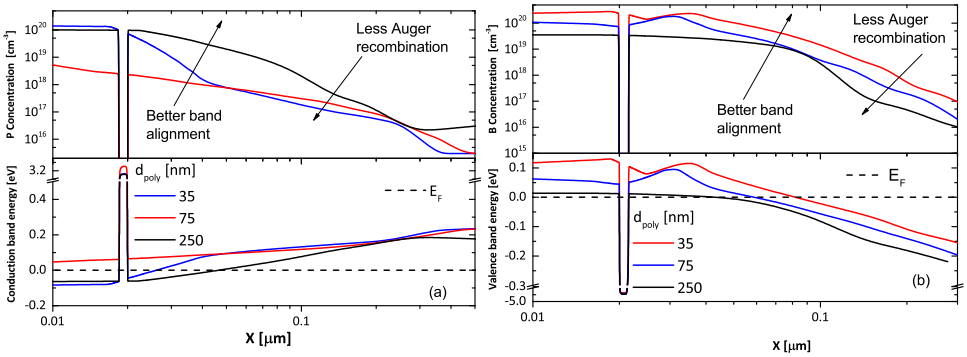


Figure 4.7: (a) Top panel: measured doping profile (in log-log scale) in the stack n-type poly-Si / $SiO_2$ / c-Si;bottom panel: corresponding band diagram for different poly-Si thicknesses; (b) top panel: measured doping profile (in log-log scale) in the stack p-type poly-Si / $SiO_2$ / c-Si; bottom panel: corresponding band diagram for different poly-Si thicknesses.

4.6 (a) of n-type and p-type poly-Si contacts, respectively.

Figure 4.7 (a) reports in the top panel the measured phosphorous doping concentration profiles and in the bottom panel the corresponding conduction energy level together with the Fermi energy level in equilibrium of n-type poly-Si / $SiO_2$ / c-Si junction simulated for different poly-Si thicknesses. For n-type contact, a strong band bending is observed for the 250-nm and 35-nm thick samples, revealing a stronger field-effect passivation than that related to the 75-nm thick sample. This is compatible with the measured lifetime achieved by n-type poly-Si (see Figure 4.4 (b)). In particular, strong electrical field across the junction is induced by high electron density at the interface. This has the effect to place the conduction band energy level below the Fermi level in c-Si. This mechanism is the effect of the optimized doping profile across the junction. This effect, together with high doping level at poly-Si side, leads to a band alignment which is crucial for transport through tunneling oxide [47]. In the case of 75 nm (red curves in figures 4.6 (a)), the conduction band is above the fermi level. This leads a relatively weak electrical field across the junction and less efficient tunneling. It is important to highlight that, in c-Si bulk, high doping profile potentially boosts transport through tunneling oxide, but also increases Auger recombination. Therefore, the doping tail in c-Si bulk should be kept such sharp to obtain the effect of higher electron accumulation only at c-Si/$SiO_2$ interface. A similar analysis has been carried out regarding the p-type poly-Si contact. Figure 4.7 (b) shows in the top panel the measured doping profile and in the bottom panel the corresponding valence energy level together with the Fermi energy level in equilibrium of p-type poly-Si / $SiO_2$ / c-Si junction simulated for different poly-Si thicknesses. In this case, the doping profiles of 250 nm and 75 nm-thick cases induce a strong valence band bending and, therefore, a strong electrical field. Similarly, the valence bands of poly-Si and c-Si exhibit an alignment above the Fermi energy level, for which tunneling is expected to be efficient for all the samples. However, the depth of the doping profile tail inside c-Si limits the passivation as Auger recombination is higher for deeper doping profiles. Accordingly, 250-nm, 75-nm and 35-nm thick poly-Si sam-

ples exhibit doping profiles as deep as 100 nm, 250 nm and 300 nm inside c-Si, respectively. The passivation quality observed in Figure 4.6 (b) highlights the effect of Auger recombination on the passivation in terms of $\tau_{eff}$ and $J_0$ = 23 fA/cm$^2$. Therefore, in our experimental framework, the 250-nm thick poly-Si sample exhibits the best potential for p-type poly-Si contact in solar cells. We can conclude that an ideal doping profile should have high doping concentration at c-Si/$SiO_2$ interface to enhance collection of carriers, but, at the same time, it should have a relatively shallow doping tail such that Auger recombination is minimized. Accordingly, reduced layer thickness in both electron and hole-selective contact requires a careful tuning of implantation dose, annealing temperature and time to confine the dopants atoms into poly-Si layer, leaving a sufficiently high doping tail that results in better passivation quality.

### 4.3.2. SOLAR CELLS



The optimized carrier-selective contacts discussed in section 4.1 are integrated into front textured poly-poly solar cells. We combine the n-type and p-type poly-Si layers with different thicknesses at the front and rear side of the device, respectively. Table

Table 4.3: Poly-poly solar cells results with different combination of front/rear poly-Si thickness and eventual FGA. Reported external parameters are for Al-based front contacted solar cells; * indicates Ti-seeded Cu-plated front contacts. The cell sketch is reported in Figure 4.1 (c)

| Solar cell | FGA | $d_{front/rear}$ [nm] | $V_{OC}$ [mV] | $J_{SC}$ [mA/cm$^2$] | FF [%] | $\eta$ [%] | $\eta_{aperture}$ [%] | pFF [%] |
|---|---|---|---|---|---|---|---|---|
| SC1 | No | 250 / 250 | 684 | 32.0 | 68.7 | 15.0 | 15.8 | 82.9 |
| SC2 | No | 75 / 75 | 663 | 36.0 | 72.8 | 17.3 | 18.2 | 82.0 |
| SC3 | Yes | 35 / 35 | 675 | 36.5 | 71.0 | 17.5 | 18.4 | 82.5 |
| SC4 | Yes | 35 / 250 | 701 | 35.1 | 72.8 | 17.9 | 18.8 | 82.3 |
| SC5 | Yes | 20 / 250 | 689 | 36.5 | 73.0 | 18.4 | 19.3 | 82.1 |
| SC6* | Yes | 20 / 250 | 682 | 36.3 | 75.2 | 18.7 | 19.6 | 84.0 |

4.3 summarizes the different poly-poly solar cells fabricated and the external parameters of the devices. SC1 with 250-nm thick poly-Si on both front and rear side exhibits $V_{OC} = 684mV$, $J_{SC} = 32mA/cm^2$ and $FF = 68.7\%$. As this cell has not received the FGA treatment, it appears to be limited by the n-type poly-Si. In fact, its $V_{OC}$ is in line with the $iV_{OC}$s values shown in Table 4.1 for sample n2 ($iV_{OCn,poly,250nm} = 688mV$ before FGA), which was used for this device. FF lies below 70%, most likely because lateral transport is mostly supported by the large doping tail in c-Si at the front electron contact. Also the lack of a TCO as transport layer plays an important role in FF values. In a similar solar cell architecture [26] with a 200-nm thick poly-Si, $V_{OC}$ was found 10 mV lower than ours and FF 4% absolute higher than ours. Those parameters were obtained by screen-printed front contacts that introduce higher recombination but also ensure lower contact resistivity than our PVD-evaporated contacts. By decreasing front and rear poly-Si thicknesses to 75 nm (SC2 in table 4.2), $V_{OC}$ decreases to 663 mV, but FF goes up to 72.8%. Since the front poly-Si thickness is reduced with respect to SC1, part of the

front lateral conduction is now supported in the poly-Si layer that has high doping and also high mobility [60]. This result is also obtained without FGA treatment. When 35-nm thick poly-Si is employed (SC3 in Table 4.3), we measure an improved $V_{OC}$ up to 675 mV with a gain of 12 mV as compared to SC2. This improvement in $V_{OC}$ is due to the FGA treatment. In this case, FF is reduced to 71%. We speculate that this FF reduction is due to a different lateral transport through the front contact owing to different doping profile in poly-Si layers. Short circuit current density is very poor for SC1 (32 mA/cm$^2$). We measure an improvement of 4 mA/cm$^2$ when 75-nm thick poly-Si layers are employed. Further improvement up to 36.5 mA/cm$^2$ is observed in case of SC3. When front and rear thicknesses are decoupled to 35 nm at the front and 250 nm at the back (SC4), $V_{OC}$ is 701 mV (the gain is 17 mV compared to SC1), short current density is 35.1 mA/cm$^2$ and FF is again at 72.8 %, as in SC2. The lower current might be due to not optimized texturing and anti-reflection coating thickness. By further thinning the front poly-Si to 20 nm and keeping the rear side poly-Si thickness to 250 nm (SC5), $V_{OC}$ slightly decreases to 689 mV with respect to SC4, but an increase in $J_{SC}$ is noted up to 36.5 mA/cm2 and FF is equal to 73% ( $\eta_{active}$ of 19.3%). Finally, the same solar cell as SC5 has been fabricated with Ti-seeded Cu-plated front contacts (SC6), resulting in $FF = 75.2\%$ ( 2% absolute higher than SC5) and $V_{OC} = 682mV$ (7 mV lower compared to SC5). $J_{SC}$ is 36.3 mA/cm$^2$, which is slightly lower than SC5. The overall $\eta_{active}$ is 19.6%. The gain in FF is due to more conductive Ti/Cu stack respect to the previously used 2-µm thick e-beam evaporated Al [61]. The reduction in $V_{OC}$ of 7 mV might be explained by the so-called "background-plating" [62] that consists in Cu growing outside the designed fingers areas and acting as deep impurity in Si [63]. Figure 4.8 reports the EQE spectra of SC1, SC2 and SC3, clearly show-

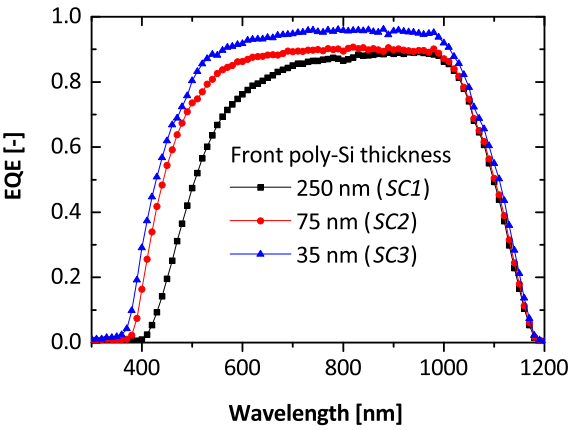


Figure 4.8: External quantum efficiency for SC1, SC2 and SC3 (see Table 4.1).

ing the losses in the short-wavelength part of the spectrum due to parasitic absorption in the front poly-Si layer. SC2 and SC3 devices show higher current collection than SC1, because of the reduced parasitic absorption in the front poly-Si layer. In this respect, there is a substantial improvement in collection from 380 nm to 800 nm. Furthermore, maximum EQE reached is 90% in both SC1 and SC2. This can be explained by electri-

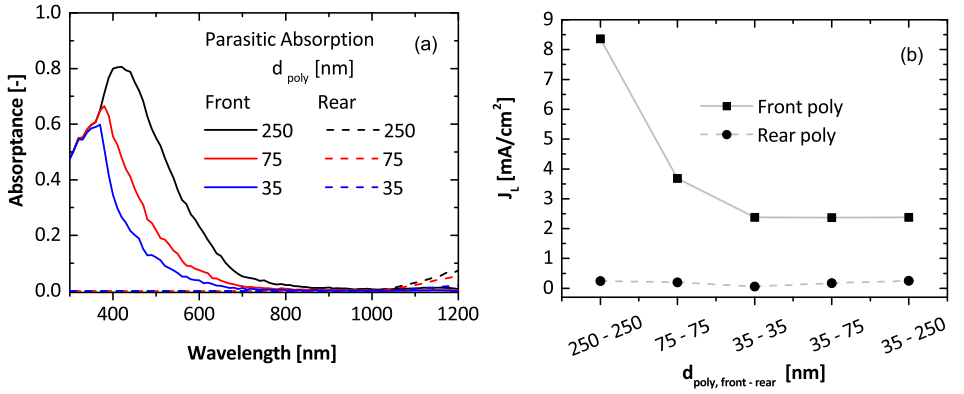


Figure 4.9: (a) Simulated absorptance in front poly-Si (continuous line) and rear poly-Si (dashed line) layers for different thicknesses as used in SC1, SC2 and SC3; (b) Simulated equivalent photocurrent density losses ($J_L$) related to different front and rear poly-Si layer thicknesses.

4

cal recombination occurring at the front and rear Si surfaces since no FGA treatment is performed. In case of SC3, instead, we observe an improved carrier collection across the whole spectral range up to 97%. This is not only due to thinner poly-Si layers but also owing to the FGA treatment. Regardless the poly-Si layers thickness, these layers suffer from parasitic absorption in the long wavelength range between 1000 nm and 1200 nm [30][31], which, together with the additional parasitic absorption due to the rear metal contact, contributes to current losses. From these experiments, we can demonstrate that the front poly-Si layer should primarily be kept as thin as possible in order to limit parasitic absorption.

We performed opto-electrical simulations of the abovementioned SC1, SC2 and SC3 devices with TCAD Sentaurus [43][47] using experimentally-extracted optical properties of poly-Si layers [48]. Figure 4.9 (a) shows the simulated absorptance in front and rear poly-Si layers. The device with 250-nm thick poly-Si layers shows a consistent absorption of the incoming light which peaks up to 0.8 in the short-wavelength range and decays to a negligible value at around 800 nm. When the thickness of poly-Si layers is reduced to 75 nm and 35 nm, the absorption strongly decreases in the ultra-violet and visible parts of the spectrum but still peaks to values close to 0.6. For the rear poly-Si layer, we observe a weak dependence of absorption against poly-Si thickness. It is noteworthy to mention that our simulations take into consideration both front texturing [44] and free carrier absorption into poly-Si given by high doping. By integrating these absorption profiles with the AM1.5 photon flux [64], we obtain the equivalent photocurrent density losses ($J_L$) for different poly-poly solar cell configurations. The values are shown in Figure 4.9 (b), where we observe a strong dependence of front poly-Si thickness on photocurrent density losses ($J_L$ of 8.5 mA/cm$^2$ for SC1 configuration). If the front poly-Si layer is kept at 35 nm, $J_L$ decreases to 2.5 mA/cm$^2$. Regarding absorption in the rear poly-Si, we obtain $J_L < 1 mA/cm^2$ with a weak dependency on the backside layer thickness. Therefore, in order to reach on one hand relatively high short circuit current density and, on the other hand, high $V_{OC}$ (see Figure 4.6), it is necessary to decouple the front thickness from the

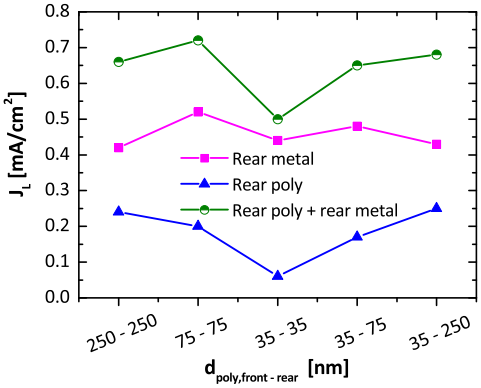


Figure 4.10: Simulated short-circuit current losses in backside poly-Si and back Ag contact depending on poly-poly solar cell configuration

rear one. Focusing on the rear side only, Figure 4.10 describes the $J_L$ of rear poly-Si and rear metal in the abovementioned cell configurations. Losses due to metal absorption are limited between 0.4 and 0.5 mA/cm$^2$, while the losses into rear poly-Si account for less than 0.25 mA/cm$^2$. By adding those two losses, the total rear losses differ by only about 0.15 mA/cm$^2$ between the configurations 35 nm / 35 nm and 35 nm / 250 nm. Therefore, we justify the decoupling of front/rear poly-Si thicknesses.

## 4.4. CONCLUSION

In this chapter we optimize poly-Si layers as carrier-selective passivating contacts prepared by LPCVD and boron- or phosphorous-doped via ion implantation. With the aim to reduce parasitic absorption in the poly-Si layers, their thickness is drastically reduced from 250 nm to 35 nm and both passivation quality and junction profile are investigated on symmetric samples by varying ion dose and annealing treatment (i.e. temperature/time). For $SiO_2$ / n-type poly-Si fabricated on textured c-Si wafers, we obtain $J_0 < 15$ fA/cm$^2$ regardless of the deposited poly-Si thickness. For these samples, carrier lifetimes above 4 ms are measured for both the thickest and thinnest investigated poly-Si layers. On the contrary, 75-nm thick layer exhibits $\tau_{eff}$ ~2 ms, due to not-optimized doping profile that leads to a degraded field-effect passivation. ECV measurements confirm this hypothesis indicating that, for an acceptable passivation quality, a shallow junction depth into c-Si bulk and $10^{20}$ P atoms/cm$^3$ confined into the poly-Si layer for the 250-nm and 35-nm thick samples is needed.

With regards to the $SiO_2$ / p-type poly-Si, it was found that passivation quality increases with poly-Si thickness. This result is the consequence of an easier doping confinement in 250-nm thick poly-Si. Although we changed implantation dose and annealing temperature/time, doping profile has a wide junction depth when thinner poly-Si is employed, leading to weaker field-effect passivation. We evaluated the effect of doping profile on field-effect passivation and band alignment on the basis of TCAD simulations. Accordingly, the experimentally optimized doping profile maximizes the trade-off be-

tween electrical field and Auger recombination by means of high doping concentration at c-Si surface and thinner buried doping profile inside c-Si, concurrently. The optimized p- and n-type $SiO_2$ / poly-Si contacts are tested in completed TCO-free FBC poly-poly solar cells with $SiN_x$ as anti-reflection coating. It is important to remark that the fabrication process is lean, such that it has only four steps. By decreasing front/rear poly-Si thicknesses, as expected, more incoming light can reach the c-Si without being parasitically absorbed in the front stack. We measure a gain in $J_{SC}$ up to 4 mA/cm$^2$ when switching from 250-nm to 35-nm thick front poly-Si. Moreover, we have shown that most of the optical losses are in the short-wavelength range. In fact, according to TCAD simulations, equivalent photo current density losses are highly dependent on front poly-Si thickness, while the equivalent photocurrent density lost at the rear side in the long-wavelength range is only 0.15 mA/cm$^2$ when switching the rear side poly-Si thickness from 250 nm to 35 nm. Therefore, we decouple the front/rear poly-Si thicknesses, keeping the p-type on the rear side at 250 nm and thinning the film on the front down to 35 nm to concurrently optimize transparency of the front film and p-type passivation at rear. This cell (SC4) exhibits a $V_{OC}$ of 701 mV with a gain of 17 mV as compared to the device with thicker p-type poly-Si (SC1). Further decrease in the front n-poly-Si layer down to 20 nm leads to a trade-off between $V_{OC}$ (decreased to 689 mV) and $J_{SC}$ (increased to 36 mA/cm$^2$). Finally, using Ti-Cu plated front contacts, FF increases up to 75.2% while $V_{OC}$ decreases to 682 mV, ascribed to background plating outside the designated grid area. A TCAD simulation of our poly-poly solar cells shows that the efficiency of our solar cells is mainly limited by FF losses coming from various sources: (i) not-optimized front metal grid, (ii) series resistance given by poor lateral transport due the small in-diffusion in c-Si bulk, (iii) thin metallization scheme, (iv) no rear edge-isolation of poly-Si structure. With all these adjustments, we forecast efficiencies greater than 21% in single junction configuration. It is remarkable that processing of this solar cell consists in only four steps and therefore it is suitable for industrial up taking with further engineering. This solar cell architecture can be a good candidate for a bottom cell in tandem configuration with emerging technologies such as perovskite. Indeed, given its high thermal budget and the poor responsivity in the blue part of the spectrum, it matches all the requirements for a fabrication of both two and four terminal tandem devices since it is possible to deposit high quality TCO layers without compromising the solar cell performances.



## 4.5. REFERENCES

[1] C. Battaglia, A. Cuevas and S. D. Wolf, "High-efficiency crystalline silicon solar cells: status and perspectives" Energy Environ. Sci., vol. 9, pp. 1552-1576, 2016, DOI: 10.1039/C5EE03380B.

[2] M. Hermle, Passivated Contacts, John Wiley and Sons, Ltd, http://dx.doi.org/10.1002/9781118927496.ch13, 10.1002/9781118927496.ch13, 125, 135, From Fundamentals to Applications, 2016

[3] M. Taguchi, A. Yano, S. Tohoda, K. Matsuyama, Y. Nakamura, T. Nishiwaki, K. Fujita, and E. Maruyama, “24.7% Record Efficiency HIT Solar Cell on Thin Silicon Wafer”, IEEE JPV, 4, 1 (2014), DOI: 10.1109/JPHOTOV.2013.2282737

[4] D. Adachi, J.L Hernández, and K. Yamamoto, Impact of carrier recombination on fill factor for large area heterojunction crystalline silicon solar cell with 25.1% efficiency,

Applied Physics Letters 2015 107:23, https://doi.org/10.1063/1.4937224.

[5] K. Yoshikawa, H. Kawasaki, W. Yoshida, T. Irie, K. Konishi, K. Nakano, T. Uto, D. Adachi, M. Kanematsu, U. H. and K. Yamamoto, “Silicon heterojunction solar cell with interdigitated back contacts for a photoconversion efficiency over 26%” Nature Energy, vol. 2, 2017, https://doi.org/10.1038/nenergy.2017.32

[6] S. D. Wolf, A. Descoeudres, Z. C. Holman and C. Ballif, "High-efficiency Silicon Heterojunction Solar Cells: A Review," Green, vol. 2, no. 1, pp. 7-24, 2012. https://doi.org/10.1515/green-2011-0018

[7] E. Yablonovitch et. al., A 720 mV open circuit voltage SiOx:c-Si:SiOx double heterostructure solar cell, applied physics letters, vol. 47, p 1211, 1985, https://doi.org/10.1063/1.96331

[8] S. Glunz, F. Feldmann, A. Richter, M. Bivour, C. Reichel, H. Steinkemper, J. Benick and M. Hermle (2015). The irresistible charm of a simple current flow pattern – 25% with a solar cell featuring a full-area back contact. 10.4229/EUPVSEC20152015-2BP.1.1.

[9] J. Stuckelberger, G. Nogay, P. Wyss, M. Lehmann, C. Allebé, F. Debrot, M. Ledinsky, A. Fejfar, M. Despeisse, F.-J. Haug, P. Löper and Christophe Ballif, Passivating Contacts for Silicon Solar Cells with 800 °C Stability Based on Tunnel-Oxide and Highly Crystalline Thin Silicon Layer, Photovoltaic Specialists Conference (PVSC), 2016 IEEE 43rd, DOI: 10.1109/PVSC.2016.7750100

[10] A. Moldovan, F. Feldmann, M. Zimmer, J. Rentsch, Jan Benick, Martin Hermle, “Tunnel oxide passivated carrier-selective contacts based on ultra-thin SiO2 layers” Solar Energy Materials and Solar Cells,Volume 142, November 2015, Pages 123-127, https://doi.org/10.1016/j.solmat.2015.06.048

[11] LPCVD polysilicon passivating contacts B. (L.J.) Geerligs, M. Stodolny, Y. Wu, A. Gutjahr, G. Janssen, I. Romijn, J. Anker, E. Bende, H. Ciftpinar, M. Lenes and J.M. Luchies, Workshop on Crystalline Silicon Solar Cells and Modules: Materials and Processes, Vail, Co., USA, 28 - 31 August 2016.

[12] J. Melskens, B. van de Loo, B. Macco, M. Vos, J. Palmans, S. Smit and W. Kessels, “Concepts and prospects of passivating contacts for crystalline silicon solar cells,” in IEEE 42nd Photovoltaic Specialist Conference, New Orleans, 2015, DOI: 10.1109/PVSC.2015.7355646.

[13] F. Feldmann, M. Simon, M. Bivour, C. Reichel, M. Hermle, and S. W. Glunz, Carrier-selective contacts for Si solar cells, Appl. Phys. Lett. 104, 181105 (2014); https://doi.org/10.1063/1.4875904

[14] C. Reichel, F. Feldmann, R. Müller, R. C. Reedy, B. G. Lee, D. L. Young, P. Stradins, M. Hermle and S. W. Glunz, "Tunnel oxide passivated contacts formed by ion implantation for applications in silicon solar cells" Journal of Applied Physics, p. 118, 2015, https://doi.org/10.1063/1.4936223

[15] R. Peibst, U. Römer, Y. Larionova, M. Rienäcker, A. Merkle, N. Folchert, S. Reiter, M. Turcu, B. Min, J. Krügener, D. Tetzlaff, E. Bugiel, T. Wietler, R. Brendel, Working principle of carrier selective poly-Si/c-Si junctions: Is tunnelling the whole story?, Solar Energy Materials and Solar Cells, Volume 158, Part 1,2016,Pages 60-67, https://doi.org/10.1016/j.solmat.2016.05.045

[16] Y. Tao et al., "730 mV implied Voc enabled by tunnel oxide passivated contact with PECVD grown and crystallized n+ polycrystalline Si," 2015 IEEE 42nd

Photovoltaic Specialist Conference (PVSC), New Orleans, LA, 2015, pp. 1-5. doi: 10.1109/PVSC.2015.7356218.

[17] G. Yang, A. Ingenito, N. v. Hameren, O. Isabella and M. Zeman, "Design and application of ion-implanted polySi passivating contacts for interdigitated back contact c-Si solar cells" Applied Physics Letters, p. 108, 2016, https://doi.org/10.1063/1.4940364

[18] U. Römer, A. Merkle, R. Peibst, T. Ohrdes, B. Lim, J. Krügener and R. Brendel, "Ion-implanted poly-Si / c-Si junctions as a back-surface field in back-junction back-contacted solar cells" in 29th European Photovoltaic Solar Energy Conference, Amsterdam, The Netherlands, 2014.

[19] F. Haase, C. Hollemann, S. Schäfer, A. Merkle, M.H. Rienäcker, J. Krügener, R. Brendel, R. Peibst, (2018). Laser contact openings for local poly-Si-metal contacts enabling 26.1 %-efficient POLO-IBC solar cells. Solar Energy Materials and Solar Cells. 186. 10.1016/j.solmat.2018.06.020.

[20] M. Stodolny, M. Lenes, Y.Wu, G. Janssen, I. Romijn, J. Luchies and L. Geerligs, "n-Type polysilicon passivating contact for industrial bifacial n-type solar cells" in 6th International Conference on Silicon Photovoltaics, Chambery, 2016.

[21] Y. Tao et. al., (2016), Large area tunnel oxide passivated rear contact n-type Si solar cells with 21.2% efficiency. Prog. Photovolt: Res. Appl., 24: 830-835. doi: 10.1002/pip.2739

[22] R.C.G. Naber, M. Lenes, A.H.G. Vlooswijk, J.R.M. Luchies, J. Wang, F. Zheng, J. Lin, Z. Zhang, N-PERT solar cells with passivated contact technology based on LPCVD polysilicon and fire-through contact metallization, Proc. 32nd EU-PVSEC, Munich, Germany, Pages 430-433, https://doi.org/10.4229/EUPVSEC20162016-2CO.3.2

[23] A. Richter et. al., Tunnel oxide passivating electron contacts as full-area rear emitter of high-efficiency p-type silicon solar cell. Prog Photovolt Res Appl. 2017; 1-8. https: // doi.org/10.1002/pip.2960

[24] A. Ingenito, G. Limodio, P. Procel, G. Yang, H. Dijkslag, O, Isabella, and M, Zeman, (2017), Silicon Solar Cell Architecture with Front Selective and Rear Full Area Ion-Implanted Passivating Contacts. Sol. RRL, 1: n/a, 1700040. doi:10.1002/solr.201700040.

[25] F. Feldmann, M. Simon, M. Bivour, C. Reichel, M. Hermle and S. W. Glunz., "Efficient carrier selective p- and n- contacts for Si solar cells" Solar Energy Materials and Solar Cells, vol. 131, pp. 100-104, 2014, https://doi.org/10.1016/j.solmat.2014.05.039

[26] S. L. Luxembourg, D. Zhang, Y. Wu, M. Najafi, V. Zardetto, W. Verhees, A. R. Burgers, S. Veenstra, L.J. Geerligs, Crystalline silicon solar cell with front and rear polysilicon passivated contacts as bottom cell for hybrid tandems, Energy Procedia, Volume 124, 2017, Pages 621-627, https://doi.org/10.1016/j.egypro.2017.09.091.

[27] M. K. Stodolny, J. Anker, B. L.J. Geerligs, G. J.M. Janssen, B. W.H. van de Loo, J. Melskens, R. Santbergen, O. Isabella, J. Schmitz, M. Lenes, J.M. Luchies, W.M.M. Kessels, I. Romijn, Material properties of LPCVD processed n-type polysilicon passivating contacts and its application in PERPoly industrial bifacial solar cells, Energy Procedia,Volume 124, 2017, Pages 635-642, https://doi.org/10.1016/j.egypro.2017.09.250

[28] S. Duttagupta, N. Nandakumar, P. Padhamnath, J. Kitz Buatis, R. Stangl, A. G. Aberle, monoPoly™ cells: Large-area crystalline silicon solar cells with fire-through screen printed contact to doped polysilicon surfaces, Solar Energy Materials and Solar Cells, Volume 187, 2018, Pages 76-81, https://doi.org/10.1016/j.solmat.2018.05.059.

[29] F. Feldmann, M. Nicolai, R. Müller, C. Reichel, M. Hermle, Optical and electrical characterization of poly-Si/SiOx contacts and their implications on solar cell design, Energy Procedia, Volume 124, 2017, Pages 31-37, ISSN 1876-6102, https://doi.org/10.1016/j.egypro.2017.09.336.

[30] F. Feldmann, C. Reichel, R. Müller, M. Hermle, The application of poly-Si/SiOx contacts as passivated top/rear contacts in Si solar cells, Solar Energy Materials and Solar Cells, Volume 159, 2017, Pages 265-271, ISSN 0927-0248, https://doi.org/10.1016/j.solmat.2016.09.015.

[31] S. C. Baker-Finch, K. R. McIntosh, D. Yan, K. Chern Fong, and T. C. Kho, Journal of Applied Physics 116, 063106 (2014); doi: 10.1063/1.4893176.

[32] G. Yang, P. Guo, P. Procel, A. Weeber, O. Isabella, M. Zeman, (2018). Polycrystalline silicon-oxide films as carrier-selective passivating contacts for c-Si solar cells. Applied Physics Letters. 112. 193904. 10.1063/1.5027547.

[33] I. Mack, J. Stuckelberger, P. Wyss, G. Nogay, Q. Jeangros, J. Horzel, C. Allebé, M. Despeisse, F.-J. Haug, A. Ingenito, P. Löper, C. Ballif, Properties of mixed phase silicon-oxide-based passivating contacts for silicon solar cells, Solar Energy Materials and Solar Cells, Volume 181, 2018, Pages 9-14, https://doi.org/10.1016/j.solmat.2017.12.030.

[34] G. Nogay, J. Stuckelberger, P. Wyss, Q. Jeangros, C. Allebé, X. Niquille, F. Debrot, M. Despeisse, F.-J. Haug, P. Löper, and C. Ballif, Silicon-Rich Silicon Carbide Hole-Selective Rear Contacts for Crystalline-Silicon-Based Solar Cells, ACS Appl. Mater. Interfaces, 2016, 8 (51), pp 35660–35667, DOI: 10.1021/acsami.6b12714.

[35] F. Feldmann, G. Nogay, J.-I. Polzin, B. Steinhauser, A. Richter, A. Fell, C. Schmiga, M. Hermle, and S. W. Glunz, A Study on the Charge Carrier Transport of Passivating Contacts, IEEE JOURNAL OF PHOTOVOLTAICS, VOL. 8, NO. 6, NOVEMBER 2018, DOI: 10.1109/JPHOTOV.2018.2870735.

[36] G. Limodio, G. Yang, H. Ge, P. Procel, Y. De Groot, L. Mazzarella, O. Isabella, M. Zeman, Front and rear contact Si solar cells combining high and low thermal budget Si passivating contacts, Solar Energy Materials and Solar Cells, Volume 194, 2019, Pages 28-35, https://doi.org/10.1016/j.solmat.2019.01.039

[37] A. Ingenito et al., "Phosphorous-Doped Silicon Carbide as Front-Side Full-Area Passivating Contact for Double-Side Contacted c-Si Solar Cells," in IEEE Journal of Photovoltaics, vol. 9, no. 2, pp. 346-354, March 2019. doi: 10.1109/JPHOTOV.2018.2886234.

[38] R. Santbergen, G. Yang, P. Procel, G. Limodio, A. Weeber, O. Isabella, and M. Zeman, "Optical Analysis of Poly-Si and Poly-SiOx Carrier-Selective Passivating Contacts for c-Si Solar Cells," in Light, Energy and the Environment, OSA Technical Digest (online) (Optical Society of America, 2017), paper PW3A.5.

[39] M. Schnabel, B. W. H. van de Loo, W. Nemeth, B. Macco, P. Stradins, W. M. M. Kessels, and D. L. Young, Hydrogen passivation of poly-Si/SiOx contacts for Si solar cells using Al2O3 studied with deuterium, Applied Physics Letters 2018 112:20, 203901 (2018); https://doi.org/10.1063/1.5031118

[40] R. Sinton, A. Cuevas and M. Stuckings, "Quasi-steady-state photoconductance, a new method for solar cell material and device characterization" in Conference Record of the IEEE Photovoltaic Specialists Conference ,1996, DOI: 10.1109/PVSC.1996.564042

[41] M. Bivour, S. Schröer, M. Hermle and S. W. Glunz, “Silicon heterojunction rear emitter solar cells: Less restrictions on the optoelectrical properties of front

side TCOs" Solar Energy Materials and Solar Cells, vol. 122, pp. 120-129, 2014, https://doi.org/10.1016/j.solmat.2013.11.029

[42] G. Limodio et. al., Copper plating metallization with alternative seed layers for c-Si solar cells embedding carrier-selective passivating contacts, submitted to IEEE JPV (2019).

[43] https://www.synopsys.com/silicon/tcad.html (Accessed 12th September 2018)

[44] P. Procel et. al., Opto-electrical modelling and optimization study of a novel IBC c-Si solar cell, Prog. in Photovoltaics: Research and application, Volume 25, Issue 6, 2017, https://doi.org/10.1002/pip.2874

[45] P. Procel, G. Yang, O. Isabella, M. Zeman, Theoretical evaluation of contact stack for high efficiency IBC-SHJ solar cells, Solar Energy Materials and Solar Cells, Volume 186, 2018, Pages 66-77, https://doi.org/10.1016/j.solmat.2018.06.021.

[46] Paul Procel, Philipp Löper, Felice Crupi, Christophe Ballif, Andrea Ingenito, Numerical simulations of hole carrier selective contacts in p-type c-Si solar cells, Solar Energy Materials and Solar Cells, Volume 200, 2019, 109937, https://doi.org/10.1016/j.solmat.2019.109937.

[47] P. Procel, G. Yang, O. Isabella and M. Zeman, "Numerical Simulations of IBC Solar Cells Based on Poly-Si Carrier-Selective Passivating Contacts," in IEEE Journal of Photovoltaics, vol. 9, no. 2, pp. 374-384, March 2019. doi: 10.1109/JPHOTOV.2019.2892527.

[48] R. Santbergen, G. Yang, P. Procel, G. Limodio, A. Weeber, O. Isabella, and M. Zeman, "Optical Analysis of Poly-Si and Poly-SiOx Carrier-Selective Passivating Contacts for c-Si Solar Cells," in Light, Energy and the Environment, OSA Technical Digest (online) (Optical Society of America, 2017), paper PW3A.5.

[49] J. Melskens, B. W. H. van de Loo, B. Macco, L. E. Black, S. Smit and W. M. M. Kessels, "Passivating Contacts for Crystalline Silicon Solar Cells: From Concepts and Materials to Prospects," in IEEE Journal of Photovoltaics, vol. 8, no. 2, pp. 373-388, March 2018. doi: 10.1109/JPHOTOV.2018.2797106

[50] B. A. Khan and R. Pandya, "Activation Energy of Source-Drain Current in Hydrogenated and Unhydrogenated Polysilicon Thin-Film Transistors," IEEE TRANSACTIONS ON ELECTRON DEVICES, vol. 37, no. 7, p. 1727, 1990.

[51] R. Peibst, Y. Larionova, S. Reiter, M. Turcu, R. Brendel, D. Tetzlaff, J. Krügener, T. Wietler, U. Höhne, J.-D. Kähler, H. Mehlich, S. Frigge, Implementation of n+ and p+ Poly Junctions on Front and Rear Side of Double-Side Contacted Industrial Silicon Solar Cells, EUPVSEC, 2016, Munich, Germany

[52] D. L. Young, W. Nemeth, V. LaSalvia, R. Reedy, N. Bateman and P. Stradins, "Ion implanted passivated contacts for interdigitated back contacted solar cells," 2015 IEEE 42nd Photovoltaic Specialist Conference (PVSC), New Orleans, LA, 2015, pp. 1-5. doi: 10.1109/PVSC.2015.7356141

[53] F. Feldmann, R. Müller, C. Reichel, and M. Hermle, (2014), Ion implantation into amorphous Si layers to form carrier-selective contacts for Si solar cells. Phys. Status Solidi RRL, 08: 767–770. doi:10.1002/pssr.201409312

[54] H. Steinkemper, F. Feldmann, M. Bivour and M. Hermle, "Numerical Simulation of Carrier-Selective Electron Contacts Featuring Tunnel Oxides," in IEEE Journal of Photovoltaics, vol. 5, no. 5, pp. 1348-1356, Sept. 2015. doi: 10.1109/JPHOTOV.2015.2455346

[55] https://www2.pvlighthouse.com.au/calculators/EDNA%202/EDNA%%202.aspx

(Accessed 12th September 2018).

[56] H. Hieslmair, I. Latchford, L. Mandrell, M. Chun and B. Adibi, Ion implantation for silicon solar cells, Photovoltaics International Volume 18, 2012

[57] F. Feldmann, C. Reichel, R. Müller and M. Hermle, "Si solar cells with top/rear poly-Si contacts," 2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC), Portland, OR, 2016, pp. 2421-2424. doi: 10.1109/PVSC.2016.7750076

[58] D. Yan, A. Cuevas, Y. Wan, J. Bullock, Passivating contacts for silicon solar cells based on boron-diffused recrystallized amorphous silicon and thin dielectric interlayers, Solar Energy Materials and Solar Cells, Volume 152, 2016, Pages 73-79, ISSN 0927-0248, https://doi.org/10.1016/j.solmat.2016.03.033.

[59] U. Römer et al., "Ion Implantation for Poly-Si Passivated Back-Junction Back-Contacted Solar Cells," in IEEE Journal of Photovoltaics, vol. 5, no. 2, pp. 507-514, March 2015. doi: 10.1109/JPHOTOV.2014.2382975

[60] L. Juan, L. Chong, M. Zhi-Guo, X. Shao-Zhen and H. S. Kwok, “The mechanism of hydrogen plasma passivation for poly-crystalline silicon thin film,” Chinese Phys. B, vol. 22, no. 10, p. 105101, 2013.

[61] http://www.tibtech.com/conductivity.php, Properties table of Stainless steel, Metals and other Conductive materials

[62] S. Braun, A. Zuschlag, B. Raabe, G. Hahn, The Origin of Background Plating, Energy Procedia, Volume 8, 2011, Pages 565-570, ISSN 1876-6102, https://doi.org/10.1016/j.egypro.2011.06.183.

[63] A. ur Rehman and S. Hong Lee, Review of the Potential of the Ni/Cu Plating Technique for Crystalline Silicon Solar Cell, Materials 2014, 7, 1318-1341; doi:10.3390/ma7021318.

[64] https://www.nrel.gov/grid/solar-resource/spectra.html

# 5

# SILICON SOLAR CELL ARCHITECTURE WITH FRONT SELECTIVE AND REAR FULL AREA ION-IMPLANTED PASSIVATING CONTACTS

*ABSTRACT - In this chapter the application of carrier-selective passivating contacts based on tunnelling silicon-dioxide and ion-implanted poly-Si in front and rear contacted Si solar cells is presented. This paper addresses the need to minimize the contact recombination while still keeping high short circuit current. We aim to solve such trade-off with a novel solar cell architecture called Passivated Rear and Front ConTacts (PERFeCT). Such design employs a selective passivating contact combined with standard homo-junction on the front side in order to minimize contact recombination while achieving high optical transparency and a full area passivating contact on the rear side. The opto-electrical modelling of this front/rear contacted architecture indicates a potential efficiency above 26%. As technology demonstration, we also report on the optimization of front surface field and processing of 9-cm$^2$ wide solar cells leading to 20.1% conversion efficiency.*

Parts of this chapter have been published to Solar Rapid Letters, A. Ingenito, G.Limodio P. Procel, G. Yang, H. Dijkslag, O, Isabella, and M, Zeman, (2017), Silicon Solar Cell Architecture with Front Selective and Rear Full Area Ion-Implanted Passivating Contacts. Sol. RRL, 1: n/a, 1700040. doi:10.1002/solr.201700040.

## 5.1. INTRODUCTION

CONTACT recombination is the main limiting factor for high-efficiency homojunction c-Si solar cells [1]. This can be easily tackled using carrier-selective passivating contacts, as shown in Chapter 4. An attractive strategy to reduce contact recombination consists indeed in replacing conventional metal/Si contacts with carrier selective contacts. The key element of this contact technology consists of the insertion of an additional buffer layer which physically displaces the metal from the Si interface, minimizes interface defects without impeding charge carrier transport. Prime examples are silicon heterojunction (SHJ) [2] and tunnelling oxide passivating contacts [3]. SHJ technology enables open-circuit voltage ($V_{OC}$) up to 750 mV [4] and world record efficiency (26.7%) [5]. Hydrogenated amorphous silicon-based passivation does not withstand high temperature [6]. Therefore, a dedicated back-end processing has to be employed, featuring temperatures below 250 °C for both transparent conductive oxide deposition and metallization steps. The need for a carrier-selective contact layer compatible with high thermal budget processes [7] brought researchers to investigate the passivating properties of doped polysilicon (poly-Si) by in-situ [8] [9][10] or ex-situ [11][12][13]on thin $SiO_x$ (< 2 nm) a technique inherited from integrated circuit industry [14]. Carrier selectivity of poly-Si contact is achieved by (i) slightly wider band-gap of the poly-Si compared to c-Si (ii) large difference between the quasi Fermi levels of the doped poly-Si and the c-Si, (iii) band offset asymmetry of the $SiO_2$ compared to Si and (iv) high tunnelling probability trough the $SiO_x$ [15]. A recent debate in the photovoltaic community deals with identifying the transport mechanisms through the thin $SiO_x$. Some studies have indicated that pinholes intentionally formed by annealing at T > 1000 °C in thermally grown $SiO_2$ layers with a thickness higher than 2 nm can provide the main charge carrier [16].

In view of the complexity of the characterization of pinhole density of our contact and its implementation in the device modelling we have employed a tunnelling model developed for electronic devices [17]. Poly-Si technology has been successfully employed for fabricating high efficiency interdigitated back contacted [18][19] as well as fully rear metallized c-Si solar cells [20]. In the latter case, for which $V_{OC} = 718mV$ and a 1-sun efficiency of 25.8% have been demonstrated, the TOPCon constitutes the rear selective contact, while on the front side an homojunction B-doped selective emitter is employed. Such high efficiency was obtained with a front-side metal coverage of ~2% allowing to minimize front contact recombination rate and optical shading losses. In fact, conversion efficiency of solar cells employing a well passivated rear contact, becomes limited by front side contact recombination. Metallization coverage < 2% are usually realized by using expensive photolithographic steps and might introduce high series resistance losses in large area devices. To minimize front contact recombination TOPCon technology has been also employed on the front side [21]. High $V_{OC}$ have been demonstrated at large metallic coverage (10%), however, front side parasitic absorption severely degraded the short-circuit current density ($J_{SC}$) [21].

In this chapter, a novel solar cell architecture, the so-called PERFeCT (Passivated Rear and Front ConTacts) solar cell is presented with the aim of combining high transparency and low recombination rate of the front contact. The objective of this chapter is to mitigate the effect of front-side parasitic absorption in poly-poly solar cells shown in Chapter 4, while employing carrier-selective passivating contacts for high $V_{OC}$ purpose. To do

this, for n-type c-Si bulk, we developed a selective front contact combining (i) a highly transparent lightly P-doped homojunction as front surface field (FSF), (ii) a P-doped TOPCon layer formed only underneath the front metal grid. This structure, compared to the one with full-area front poly-Si passivating contact, is advantageous because of the optically transparent FSF, thus not losing in short-circuit current density ($J_{SC}$), while solar cells with full-area front side poly-Si suffer from high parasitic absorption [21]. As rear emitter, we used a B-doped poly-Si layer deposited on thin $SiO_x$. We first justify our rear-junction configuration by means of an advanced opto-electrical model and then we report on the first technology demonstration of a PERFeCT solar cells.

## 5.2. EXPERIMENTAL DETAILS

The flow-chart for fabricating the rear junction PERFeCT solar cell follows the procedure reported in paragraph 2.2.3. So, the front side employs poly-Si passivating contacts only underneath metal contacts, while a lightly doped homojunction front surface field is implanted/diffused to ensure optical transparency and good lateral transport. The rear side is instead fully passivated by thin $SiO_x$/p-type poly-Si. The same B-doped poly-Si features of chapter 4 have been used also for this chapter. A stack composed of $SiO_x$ and $SiN_x$ at the front is used as a passivation layer and anti-reflection coating. Tyipical front Al contacts (5% metal coverage) and Ag/Cr/Al stack at the rear complete the solar cell. The solar cells shown here are fabricated all together until different processes are performed. For instance, some of the solar cells have an implanted FSF while some others have a diffused FSF. Some solar cells are evaporated with Al back contact while some other Ag back contact evaporation is performed.



Table 5.1: Most relevant physical models and parameters used in the electrical model

| Model parameter | Values |
|---|---|
| Free carrier statistics | Fermi-Dirac [24] |
| Bandgap Narrowing | Schenk [25] |
| Mobility | Klaassen [28] |
| Intrinsic Recombination | Richter [29] |
| Intrinsic carrier density | Altermatt [26] |
| Metal/Si SRV | $10^7$ cm/s |
| SRH lifetime | $\tau_{bulk}$ = 2 ms |
| Finger and bus bar resistance | Distributed model: 2.8 μΩcm for Al metal resistance |

Estimating the highest potential efficiency of a PERFeCT cell means evaluating whether the emitter should be located at the front or at the rear side of the device. As this choice has impact on the carrier transport at the front contact, we deployed an advanced opto-electrical modelling based TCAD Sentaurus tool [22] to study the performance limit. In our modelling approach, we simulated the three-dimensional absorption profile of a front textured PERFeCT device via the TCAD built-in ray tracer while concurrently solving the drift-diffusion model. Details of this modelling approach can be found Ref. [23]. State-of-the-art parameters were used to properly calibrate the used

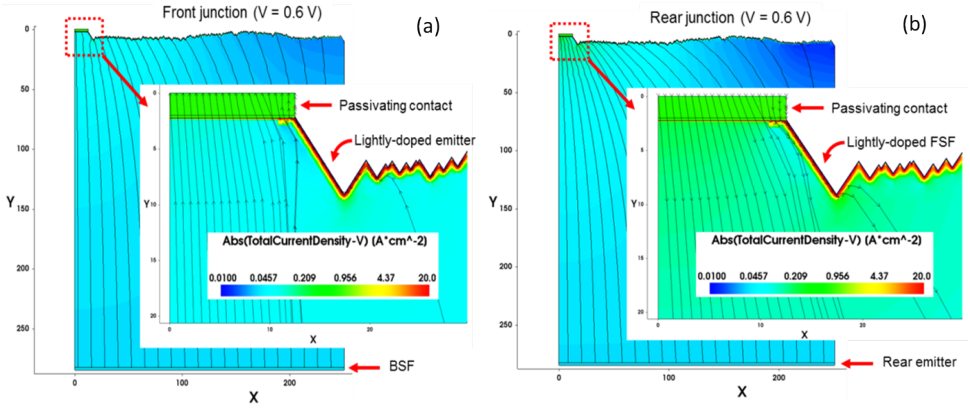


Figure 5.1: Simulated current density map at $V = 0.6V$ and related streamlines for a symmetric modelled element of (a) front junction and (b) rear junction PERFeCT cells. The maps highlight current crowding close to the front contact and front the homojunction.

5

physical models [24][25][26][27][28][29] as the table below shows. Simulated devices feature 100-$\mu$m thick wafer with 2.5 Ωcm resistivity and 1% of front contact shading.

## 5.3. RESULTS AND DISCUSSION

The limits of the carrier transport on the front contact in both front and rear junction PERFeCT cells were evaluated at 0.6 V, a voltage level close to the voltage at the maximum power point. As shown in Figure 5.1, in both rear and front emitter configurations, a current crowding can be observed at the edge between the homojunction region and the carrier-selective contact. Therefore the choice between front junction and rear junction comes down to allow at the front contact, where current crowding occurs, the transport of those charge carriers with the highest tunnelling probability through the thin $SiO_2$. To solve this dilemma and to evaluate its consequences on device performance, we report in Figure 5.2 the conversion efficiency of rear junction and front junction PERFeCT cells as function of the effective tunnelling masses for electrons ($m_{t,e}$) and holes ($m_{t,h}$). Considering reported values $m_{t,h} = 0.32 < m_{t,e} = 0.4$ for $SiO_2$ [17], a rear junction PERFeCT cell possesses higher potential efficiency (>26%) than a front junction one (24%). This is because a more favourable transport of holes, characterized by lower tunnelling mass, occurs in conditions of no current crowding, i.e. through the rear full-area passivating contact. It is noteworthy that similar result (A rear junction is more suitable than a front junction solar cell) for silicon heterojunction solar cell (SHJ) was demonstrated in [30], as the result of a trade-off between lateral conductivity, parasitic absorption in the TCO and the Schottky-barrier at the p-contact / TCO.

Having justified the rear junction architecture of our PERFeCT solar cell, we continue with its experimental demonstration. Since the homojunction FSF can easily become a bottleneck for the device $V_{OC}$, it has to be optimized. To this end, double-sided textured symmetric samples were prepared for lifetime testing. For ion-implanted FSF, we kept

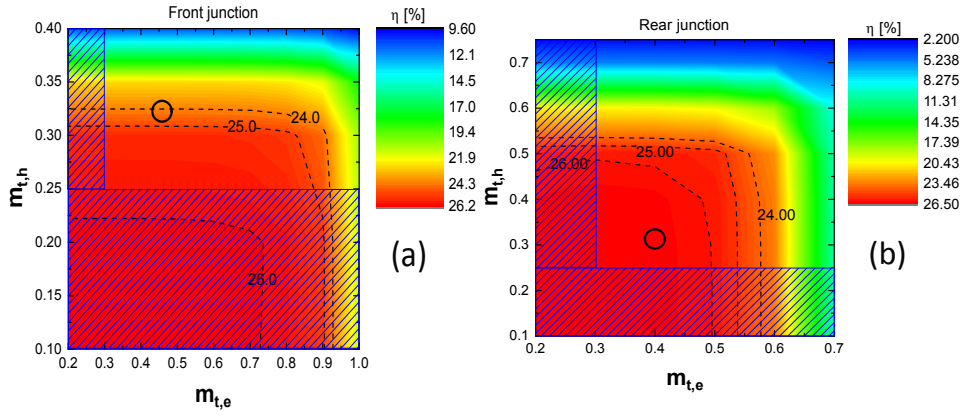


Figure 5.2: Calculated conversion efficiency for (a) front junction and (b) rear junction PERFeCT cells as function of $m_{t,e}$ and $m_{t,h}$. Efficiency values under blue pattern correspond to not reported $m_{t,e}$ and $m_{t,h}$ values. Efficiency values for $m_{t,e}$ of 0.4 and $m_{t,h}$ of 0.32 for less than 3.6-nm thick $SiO_2$ [17] are marked with black circles.

5

the dose constant to $5 \cdot 10^{14}$ ions/cm$^2$, while changing the implantation energy from 20 keV to 10 keV. For $POCl_3$-diffused FSF, the pre-deposition was optimized to 10 minutes. The resulting phosphosilicate glass was etched in HF before the drive-in. In both types of FSFs, the annealing/drive-in was executed at 850 °C for 90 minutes in $O_2$ atmosphere. Surface passivation was finalized with PECVD $SiN_x$.

The effective minority carrier lifetime $\tau_{eff}$ and saturation current density $J_0$ were measured by means of a Sinton WCT-120 lifetime tester. In Figure 5.3, $\tau_{eff}$ versus minority carrier density is reported. For ion-implanted lightly-doped FSF, implantation energy plays an important role in terms of recombination. Indeed, because a lower implantation energy induces less damage on the lattice, higher lifetime could be obtained. As reported in Table 5.2, the lowest measured $J_0$ is in the order of 30 fA/cm$^2$ or both optimized ion-implanted and $POCl_3$-diffused FSFs. To complete the necessary building blocks for our rear junction PERFeCT solar cell, the ion-implanted poly-Si-based passivating rear emitter and front contact exhibited, respectively, $J_{0emitter}$ of 31 fA/cm$^2$ and $J_{0frontcontact}$ of 8 fA/cm$^2$ before metallization. These values are already measured by G.Yang and published in [11].

Four 7.84-cm$^2$ wide PERFeCT solar cells with different FSF and back reflectors were processed. Two of these solar cells (SC1 and SC2) were endowed with ion-implanted FSF (type n1 as in Table 5.2) and, respectively, with 2-µm thick Al or Ag-based back reflector (100 nm Ag / 30 nm Cr / 2 µm Al). These cells were meant to analyse the impact of the Ag back reflector respect to Al. The other two solar cells (SC3 and SC4) were both endowed with $POCl_3$-diffused FSF (type n4 as in Table 5.2) and an Ag-based back reflector (like SC2). The difference between them is that SC4 was processed with a layer of $SiN_x$ on the rear side during the $POCL_3$ diffusion. This layer has the benefits (i) to avoid counter P-doping of the rear B-doped poly-Si and (ii) to increase the mobility of the poly-Si by

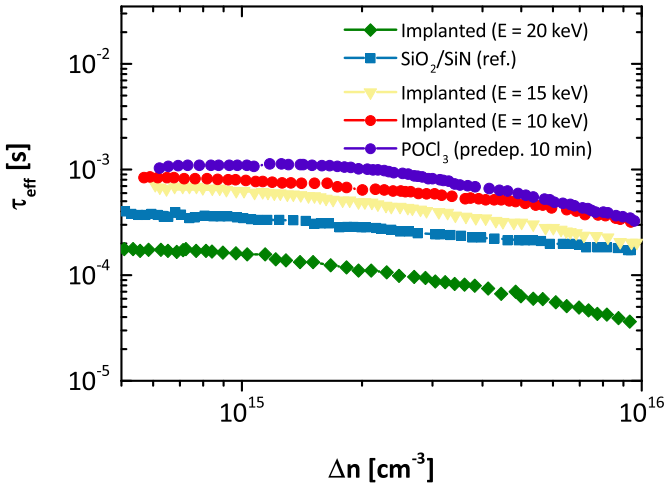


Figure 5.3: Effective minority carrier lifetime versus minority carrier density of symmetrical $SiO_2/SiN_x$-passivated lightly-doped ion-implanted or $POCl_3$-diffused FSF on double-sided textured wafers. The reference sample is a front and rear $SiO_2/SiN_x$-passivated double-sided textured wafer (no FSF).



hydrogen diffusion at elevated temperature [31].

Table 5.2: Energy and dose of ion-implanted FSFs and predeposition time of $POCl_3$ diffused FSF with related sheet resistance ($R_{SH}$) and dark saturation current density $J_0$.

| Sample name | Energy [keV] | Dose [ions/cm$^2$] | $POCL_3$ Time [min] | $R_{shFSF}$ [Ω/sq ] | $J_{0FSF}$ [fA/cm$^2$] |
|---|---|---|---|---|---|
| n1 | 10 | $5 \cdot 10^{14}$ | - | 263 | 28 |
| n2 | 15 | $5 \cdot 10^{14}$ | - | 258 | 50 |
| n3 | 20 | $5 \cdot 10^{14}$ | - | 250 | 120 |
| n4 | - | - | 10 | 187 | 30 |

SC3 and SC4 were used to evaluate the impact on the fill factor (FF) owing to different FSF fabrication methods. An Ag-based back reflector ensures the highest internal rear reflectance, resulting in an increased external quantum efficiency (EQE) in near-infrared region [32]. As shown in Figure 5.4(a), we confirm it by comparing the EQE of SC1 and SC2. Indeed, the collection of photo-generated charges is higher in the near-infrared part of the spectrum when Ag back reflector is applied at the rear side of SC2. This highlights the optical potential of our PERFeCT architecture when an excellent rear reflector is employed. In Figure 5.4(b), instead, the EQE spectra of SC3 and SC4 are reported. The spectra are nearly the same in the near-infrared region, owing to having the same Ag-based back reflector, but the one of SC4 exhibits a slight increase in the short wavelength range. This is possibly due to a slight variation in the ARC thickness, as witnessed by the reflectance spectra in the same figure. Looking at the external parameters reported in Ta-

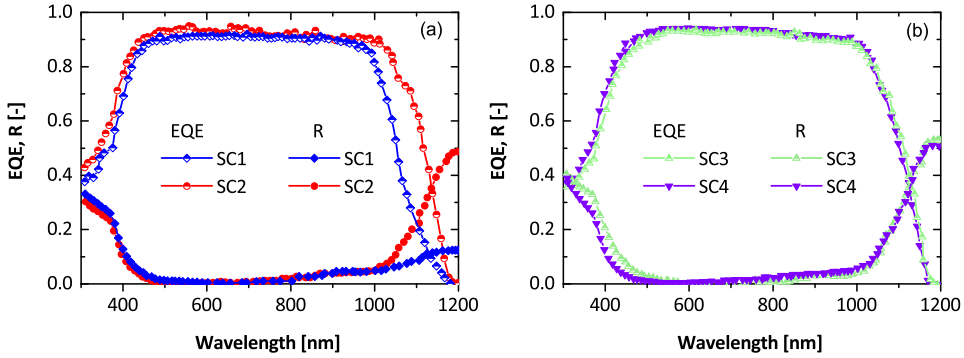


Figure 5.4: External Quantum Efficiency of (a) PERFeCT SC1 and SC2 and (b) PERFeCT SC3 and SC4.



ble 5.3, the $V_{OC}$ stays mostly constant at around 654 mV, while FF increases from 72.8% of SC1 to 75.2% of SC4, leading to a 20.1% conversion efficiency (aperture area). Considering that all devices show very comparable p-FF (measured with Suns $V_{OC}$), eventual FF differences are most likely to be related to series resistance. We speculate that the higher FF for SC4 compared to SC1 is possibly due to two different reasons: (i) the $POCl_3$-diffused FSF is more conductive than the ion-implanted FSF (see Table 5.2); (ii) capping the emitter with $SiN_x$ before $POCl_3$ diffusion avoids counter doping of the emitter and enables hydrogen diffusion [33]. Nevertheless, since $POCl_3$-diffused FSF has a relatively high $R_{SH}$ (187 Ω/sq), FF is still limited by lateral conductivity of FSF. Eventually, hydrogen diffusion slightly ameliorated also the surface passivation of SC4, bringing the $V_{OC}$ to 658 mV. Looking into the potential of this solar cell architecture, the saturation current density analysis gives a total $J_0$ ($J_{0,tot}$) for SC4 equal to 70 fA/cm$^2$, according to the following breakdown equation:

$$J_{0\text{tot}} = J_{0\text{bulk}} + f J_{0\text{frontcontact}} + (1-f) J_{0\text{FSF}} + J_{0\text{rearcontact}}$$

where $J_{0bulk}$ is 10 fA/cm$^2$, f is 5% and it is the metal coverage area fraction and the other $J_0$s are from the aforementioned symmetric samples. For the measured $J_{SC} = 40.7 mA/cm^2$, a $V_{OC}$ of 700 mV would be expected but in practice we experienced a loss in $V_{OC}$ of 40 mV. The first 20 mV were likely lost due to cleanliness issues and/or imperfections in processing, since a lifetime measurement made on SC1 before front and rear metallization, resulted in an implied $V_{OC}$ of 681 mV and pseudo-FF of 82%. A very similar value is expected for all the other solar cells since $J_0$ contribution is very similar. Therefore, a possible reason to explain a lower $V_{OC}$ than expected is that there is no spatial separation between poly-Si opening and metal contact opening.

Aside the reason given above, we ascribe the remaining losses of other 20 mV to the e-beam evaporated metallic front contact and/or deposited rear metallic blanket. This latter $V_{OC}$ loss has already been observed in literature [34][35] and it deals with the surface recombination velocity at metal/semiconductor interface. Notwithstanding these issues, we estimate that a conversion efficiency beyond 23% is at hand for

Table 5.3: External parameters of four rear junction PERFeCT cells. SC4 is as SC3 but with a $SiN_x$ layer deployed during $POCl_3$ diffusion of the FSF to protect the emitter from counter-doping and enable hydrogenation. $J_{SC}$ is computed from convoluting AM1.5 [27] with EQE spectra between 300 and 1200 nm.

| Solar cell | Back Reflector | FSF | $V_{OC}$ [mV] | $J_{SC\text{-}EQE}$ [mA/cm$^2$] | FF [%] | pFF [%] | $\eta$ [%] | $\eta_{aperture}$ [%] |
|---|---|---|---|---|---|---|---|---|
| SC1 | Al | n1 | 654 | 37.8 | 72.8 | 82.4 | 17.1 | 18.0 |
| SC2 | Ag | n1 | 653 | 40.0 | 72.7 | 82.4 | 18.2 | 19.1 |
| SC3 | Ag | n4 | 654 | 40.3 | 73.5 | 82.5 | 18.5 | 19.4 |
| SC4 | Ag | n4 | 656 | 40.7 | 75.2 | 82.7 | 19.1 | 20.0 |

our rear junction PERFeCT architecture, because (i) the optical transparency of the FSF gives a good blue response of the solar cells ($J_{SC} > 41 cm^2$); (ii) the carrier-selective passivating contacts ensure low contact recombination recombination ($V_{OC} > 700 mV$); (iii) industrially-relevant metallization techniques such as Cu-plating (front side) and screen printing (rear side) can greatly reduce series resistance ($FF > 80\%$).

Compared to poly-poly solar cells shown in chapter 4, the short-circuit current density is increased by 2 mA/cm$^2$, while the highest $V_{OC}$ measured here is much lower than the $V_{OC}$ of a poly-poly solar cell. Although there is no evidence for that in this thesis, this drop in $V_{OC}$ for PERFeCT solar cell might be due to the fact that the selective structure is built without considering an eventual metal overlapping the contact. This metal in contact with HMJ FSF might be the cause of higher recombination losses. Therefore, a recommendation for future expansion of this work is to develop a design of a metal mask such that the metal does not touch the front surface field. Fill-factor in both solar cells is rather similar. This means that the carrier transport is deployed in a similar manner.

## 5.4. CONCLUSION

In this chapter we introduced a new solar cell architecture, the so-called PERFeCT (Passivated Rear and Front ConTacts) cell. It minimizes the contact recombination owing to the carrier-selective passivating layers (full-area at the back and only underneath the metallic grid at the front). At the same time, it is capable to ensure high current density due to the optical transparency of a lightly-doped front side. Advanced opto-electrical modelling shows that a rear junction PERFeCT device (i) can achieve conversion efficiencies beyond 26% and (ii) outperforms the front junction configuration, since holes transport in fully metallized rear poly-Si-based emitter avoids current crowding through tunnelling $SiO_2$. Realizing a rear junction PERFeCT device, possible bottlenecks are the passivation quality of the FSF and the metallization quality. We fabricated different solar cells with different back reflectors and different FSF fabrication methods. We showed that cells endowed with Ag back reflector realize high current collection in the infra-red part of the spectrum ($J_{SC}$ > 40 mA/cm$^2$). Also, a combination of $POCL_3$-diffused FSF with hydrogenating capping $SiN_x$ at the backside increased the FF up to 75.2%, leading to an aperture efficiency of 20.1% in a 7.84-cm$^2$ wide PERFeCT device. The $V_{OC}$ loss before and after metallization step is under investigation and it is ascribed

to the deployed e-beam evaporation at the front side. State-of-the-art front side passivation and a more delicate metallization (thermal evaporation/plating/printing) may enable an industrially-compatible 23% PERFeCT device. A step towards industrial compatibility may come from patterning front poly-Si with inkjet printing and fire-through screen printing technique to suppress all the metallization steps currently performed. The investigation of contact resistance between poly-Si and printed Ag as well as of additional recombination losses [36] will be the key point to achieve > 23% efficiency PERFeCT solar cell.

## 5.5. REFERENCES

[1] C. Battaglia, A. Cuevas and S. D. Wolf, "High-efficiency crystalline silicon solar cells: status and perspectives," Energy and Environmental Science, pp. 1552-1576, 2016.

[2] M. Taguchi, H. Sakata, Y. Yoshimine, E. Maruyama, A. Terakawa and M. Tanak, "An approach for the higher efficiency in the HIT cells," in 31st IEEE Photovoltaic Specialists Conference, 2005.

[3]E. Yablonovitch et. al., A 720 mV open circuit voltage SiOx:c-Si:SiOx double heterostructure solar cell, applied physics letters, vol. 47, p 1211, 1985, https://doi.org/10.1063/1.96331

[4] K. Masuko, M. Shigematsu, T. Hashiguchi, D. Fujishima, M. Kai, N. Yoshimura, T. Yamaguchi, Y. Ichihashi, T. Mishima, N. Matsubara, T. Yamanishi, T. Takahama, M. Taguchi and E. Maruyama, "Achievement of More Than 25% Conversion Efficiency With Crystalline Silicon Heterojunction Solar Cell," IEEE Journal of Photovoltaics, vol. 4, no. 6, pp. 1433-1435, 2014.

[5] K. Yoshikawa, H. Kawasaki, W. Yoshida, T. Irie, K. Konishi, K. Nakano, T. Uto, D. Adachi, M. Kanematsu, U. H. and K. Yamamoto, "Silicon heterojunction solar cell with interdigitated back contacts for a photoconversion efficiency over 26%," Nature Energy, vol. 2, 2017.

[6] S. D. Wolf, A. Descoeudres, Z. C. Holman and C. Ballif, "High-efficiency Silicon Heterojunction Solar Cells: A Review," Green, vol. 2, no. 1, pp. 7-24, 2012.

[7] U. Wurfel, A. Cuevas and P. Wurfel, "Charge Carrier Separation in Solar Cells," IEEE JOURNAL OF PHOTOVOLTAICS, vol. 5, no. 1, pp. 461-467, 2015.

[8] F. Feldmann, BivourM., C. Reichel, H. Steinkemper, M. Hermle and S. W. Glunz, "Tunnel oxide passivated contacts as an alternative to partial rear contacts," Solar Energy Materials and Solar Cells, vol. 131, pp. 46-50, 2014.

[9] J. Stuckelberger, G. Nogay, P. Wyss, Q. Jeangros, C. Allebé, F. Debrot, X. Niquille, M. Ledinksy, A. Fejfar, M. Despeisse, F.-J. Haug, P. Löper and C. Ballif, "Passivating electron contact based on highly crystalline nanostructured silicon oxide layers for silicon solar cells," Solar Energy Materials and Solar Cells, vol. 158, pp. 2-10, 2016.

[10] G. Nogay, J. Stuckelberger, P. Wyss, Q. Jeangros, C. Allebé, X. Niquille, F. Debrot, M. Despeisse, F.-J. Haug, P. Löper and C. Ballif, "Silicon-Rich Silicon Carbide Hole-Selective Rear Contacts for crystalline-silicon-based solar cells," ACS Applied Materials and Interfaces, vol. 8, pp. 35660-35667, 2017.

[11] G. Yang, A. Ingenito, N. v. Hameren, O. Isabella and M. Zeman, "Design and application of ion-implanted polySi passivating contacts for interdigitated back contact c-Si solar cells," Applied Physics Letters, p. 108, 2016.

[12] D. Yan, A. Cuevas, Y. Wan and J. Bullock, “Passivating contacts for silicon solar cells based on boron-diffused recrystallized amorphous silicon and thin dielectric interlayers,” Solar Energy Materials and Solar Cells, vol. 152, pp. 73-79, 2016.

[13] C. Reichel, F. Feldmann, R. Müller, R. C. Reedy, B. G. Lee, D. L. Young, P. Stradins, M. Hermle and S. W. Glunz, “Tunnel oxide passivated contacts formed by ion implantation for applications in silicon solar cells,” Journal of Applied Physics, vol. 118, p. 205701, 2015.

[14] R. Bashir, S. Venkatesan and G. W. Neudeck, “A Polysilicon Contacted Subcollector BJT for a Three-Dimensional BiCMOS Process,” IEEE ELECTRON DEVICE LE’ITERS, vol. 13, no. 8, pp. 392-395, 1992.

[15] J. Melskens, B. van de Loo, B. Macco, M. Vos, J. Palmans, S. Smit and W. Kessels, “Concepts and prospects of passivating contacts for crystalline silicon solar cells,” in IEEE 42nd Photovoltaic Specialist Conference„ New Orleans, 2015.

[16] R. Peibst, U. Römer, Y. Larionova, M. R. (. Häberle), A. Merkle, N. Folchert, S. Reiter, M. Turcu, B. Min, J. Krügener, D. Tetzlaff, E. Bugiel, T. Wietler and R. Brendel, “Working principle of carrier selective poly-Si/c-Si junctions: Is tunnelling the whole story?,” Solar Energy Materials and Solar Cells, vol. 158, no. 1, pp. 60-67, 2016.

[17] Gehring and S. Selberherr, “Modeling of tunneling current and gate dielectric reliability for non volatile memory devices,” Device Mater. Reliab. IEEE Trans., vol. 4, no. 3, p. 306–319, 2004.

[18] G. Yang, A. Ingenito, O. Isabella and M. Zeman, “IBC c-Si solar cells based on ion-implanted poly-silicon passivating contacts,” Solar Energy Materials and Solar Cells, vol. 158, p. 84, 2016.

[19] M. Rienächer, M. Bossmeyer, A. Merkle, U. Römer, F. Haase, J. Krügener, R. Brendel and R. Peibst, “Junction Resistivity of Carrier-Selective Polysilicon on Oxide Junctions and Its Impact on Solar Cell Performance,” IEEE Journal of Photovoltaics, vol. 7, no. 1, p. 11, 2017.

[20] S. Glunz, F. Feldmann, A. Richter, M. Bivour, C. Reichel, H. Steinkemper and M. H. J. Benick, “The Irresistible Charm of a Simple Current Flow Pattern – 25% with a Solar Cell Featuring a Full-Area Back Contact,” in 31st European Photovoltaic Solar Energy Conference and Exhibition, Hamburg, 2015.

[21] F. Feldmann, C. Reichel, R. Müller and M. Hermle, “The application of poly-Si/SiOx contacts as passivated top/rear contacts in Si solar cells,” Solar Energy Materials and Solar Cells, pp. 265-271, 2016.

[22] Synopsis, “Sentaurus Device User,” 2013.

[23] P. Procel, A. Ingenito. R. De Rose, S. Pierro, F. Crupi, M. Lanuzza, G. Cocorullo, O. Isabella and M. Zeman (2017) Opto-electrical modelling and optimization study of a novel IBC c-Si solar cell. Prog. Photovolt. Res. Appl., 25: 452-469, doi: 10.1002/pip.2871

[24] Fell, K. R. McIntosh, P. P. Altermatt, J. M. Janssen, R. Stangl, A. Ho-Baillie, H. Steinkemper, J. Greulich, M. Muller, B. Min, K. C. Fong, M. Hermle, I. G. Romijn and M. D. Abbott, “Input parameters for the simulation of silicon solar cells in 2014„” IEEE J. Photovoltaics, vol. 5, no. 4, p. 1250–1263, 2015.

[25] Schenk, "Finite-temperature full random-phase approximation model of band gap narrowing for silicon device simulation," Journal of Applied Physics, vol. 84, no. 7, pp. 3684-3695, 1998.

[26] P. P. Altermatt, A. Schenk, F. Geelhaar and G. Heiser, “Reassessment of the intrinsic carrier density in crystalline silicon in view of band-gap narrowing,” J. Appl. Phys, vol. 93, no. 3, p. 1598, 2003.

[27] ASTM G173 - 03, “Standard Tables for Reference Solar Spectral Irradiances: Direct Normal and Hemispherical on 37° Tilted Surface,” 2012.

[28] D. Klaassen, "A unified mobility model for device simulation: II. temperature dependence of carrier mobility and lifetime," Solid-State Electronics, vol. 35, no. 7, pp. 961-967, 1992.

[29] Richter, S. Glunz, F. Werner, J. Schmidt and A. Cuevas, “Improved quantitative description of Auger recombination in crystalline silicon,” PHYSICAL REVIEW B, vol. 86, no. 165202, 2012.

[30] M. Bivour, S. Schröer, M. Hermle and S. W. Glunz, “Silicon heterojunction rear emitter solar cells: Less restrictions on the optoelectrical properties of front side TCOs,” Solar Energy Materials and Solar Cells, vol. 122, pp. 120-129, 2014.

[31] L. Juan, L. Chong, M. Zhi-Guo, X. Shao-Zhen and H. S. Kwok, “The mechanism of hydrogen plasma passivation for poly-crystalline silicon thin film,” Chinese Phys. B, vol. 22, no. 10, p. 105101, 2013.

[32] A. Ingenito, J. C. O. Lizcano, S. L. Luxembourg, R. Santbergen, A. Weeber, O. Isabella and M. Zeman, “Optimized back Reflectors for Rear Diffused c-Si Solar Cells,” in Journal of Photovoltaics, 2015.

[33] M. Sheoran, D. S. Kim and A. Rohatgi, “Hydrogen diffusion in silicon from PECVD silicon nitride,” in 33rd IEEE Photovoltaic Specialists Conference, San Diego, CA, USA, 2008.

[34] Edler, V. Mihailetchi, C. Comparotto, L. Koduvelikulathu, R. Kopecek, R. Harney, T. Böscke and J. Lossen, “On the metallization losses of bifacial n-type silicon solar cells,” in 27th EUPVSEC, Frankfurt, 2012.

[35] L. Wang, J. Han, A. Lochtefeld, A. Gerger and A. Barnett, “Analysis of Losses in Open Circuit Voltage for an 18-µm Silicon Solar Cell,” applied sciences, vol. 5, pp. 682-694, 2015.

[36] L. Geerligs, M. Stodolny, Y. Wu, A. Gutjahr, G. Janssen, I. Romijn, J. Anker, E. Bende, H. Ciftpinar, M. Lenes and J.-M. Luchies, “LPCVD polysilicon passivating contacts,” in Workshop on Crystalline Silicon Solar Cells and Modules: Materials and Processes, Vail, Co., USA, 2016.

# 6

# FRONT AND REAR CONTACT SI SOLAR CELLS COMBINING HIGH AND LOW THERMAL BUDGET SI PASSIVATING CONTACTS

*ABSTRACT - In this chapter we develop a rear emitter silicon solar cell that integrates carrier-selective passivating contacts (CSPCs) with different thermal budget in the same device. The solar cell consists of a B-doped poly-Si/$SiO_x$ hole collector and an i/n hydrogenated amorphous silicon (a-Si:H) stack acting as electron collector placed on the planar rear and textured front side, respectively. We investigate the passivation properties of both CSPCs on symmetric structures by optimizing the interdependency among annealing temperature, time and environment. The optimized B-doped poly-Si/$SiO_x$ reaches a saturation current density of 10 fA/cm$^2$ on n-type wafers and an implied open circuit voltage ($iV_{OC}$) of 716 mV. Furthermore, the i/n a-Si:H stack shows an effective carrier lifetime above 4 ms and $iV_{OC}$ of 705 mV for cell-relevant layers thickness. After a post-deposition anneal in $H_2$, lifetime is above 10 ms and $iV_{OC} = 708 mV$. Finally, we optimize the optoelectronic properties of indium-based transparent conductive oxide (Indium Tin Oxide ITO and hydrogenated indium oxide IO:H) to reduce parasitic absorption with a gain in short circuit current density of 0.23 mA/cm$^2$. In conclusion, the optimized layer stacks are implemented at device level obtaining a device with $V_{OC} = 704 mV$, fill factor of 73.8%, a short circuit current of 39.7 mA/cm$^2$ and 21.0% aperture-area conversion efficiency.*

Parts of this chapter have been published in Solar Energy Materials and Solar Cells, G. Limodio et. al., Solar Energy Materials and Solar Cells, Volume 194, 2019, Pages 28-35, https://doi.org/10.1016/j.solmat.2019.01.039.

## 6.1. INTRODUCTION

In homojunction crystalline silicon (c-Si) solar cells, the high surface recombination velocity at the Si/metal interface prevents devices from achieving high conversion efficiencies ($\eta$) owing to consistent open-circuit voltage ($V_{OC}$) losses [1]. A possible solution to reduce contact recombination is to restrict metal contact area at the rear side, employing the so-called passivated emitter rear contact (PERC) approach [2]. Since metal contact fraction is strongly limited, this leads to higher series resistance. The optimization requires a trade-off between recombination losses (detectable in $V_{OC}$) and fill factor (FF) [3][4]. Moreover, the fabrication process requires an additional patterning step that increases the manufacturing costs. The use of carrier-selective passivating contacts (CSPCs) has been proposed to cope with the $V_{OC}$ limitation [5]. It consists of inserting a material that can concurrently act as passivation and contact layer to separate the metal contact from c-Si absorber and to overcome the $V_{OC}$ losses. In silicon heterojunction (SHJ) solar cells [6], the growth of intrinsic and doped hydrogenated amorphous silicon (a-Si:H) stacks on both c-Si wafer surfaces enables extremely high $V_{OC}$s of up to 750 mV [7]. With this device concept, Kaneka has reported conversion efficiency ($\eta$) above 25% for a front and back-contacted (FBC) scheme [8] and recently $\eta$ = 26.7% in interdigitated back-contacted (IBC) devices [9]. Besides the advantages of using a-Si:H passivation contacts [10][11][12] and their limited thickness, intrinsic and doped a-Si:H layers placed on the front side of a SHJ cell suffer from high parasitic absorption losses due to high defect density within the material and high absorption coefficient owing to the quasi-direct bandgap of a-Si:H [13]. Therefore, part of the photo generated carriers is parasitically absorbed without contributing to the carrier collection [14]. Additional source of current loss comes from the use of transparent conductive oxide (TCO) layer, such as indium tin oxide ($In_2O_3$:Sn, $I_{TO}$), to solve lateral conductivity issues of a-Si:H. To improve the near-infrared transparency, hydrogenated indium oxide (IO:H) has been developed with much reduced optical parasitic losses [15]. The higher contact resistance at the IO:H/metal interface is mitigated by inserting a thin ITO buffer layer as suggested by Barraud et al. [16]. In total, more than 2 mA/cm$^2$ in photocurrent density is estimated to be lost in the front layer stack of a typical SHJ solar cell. Furthermore, SHJ fabrication process is temperature-limited. In fact, passivation properties of a-Si:H layers strongly degrade for T > 250 °C [13], therefore dedicated back-end processes, such as TCO depositions and metallization need to be carefully developed. A very promising contact scheme, originally proposed by Yablonovitch et al. [17], consists of an ultra-thin silicon oxide layer ($SiO_2 < 2nm$) [18] coated with doped poly-Si layer grown by either low pressure- or plasma-enhanced chemical vapour deposition (LP/PE-CVD) methods [19][20]. This passivation scheme involves fabrication processes in the range of 900 °C; therefore, it is compatible with standard solar cell manufacturing. The presence of an ultra-thin $SiO_2$ layer reduces the defect density at c-Si surface providing simultaneously surface passivation, and a tunnel barrier that allows only majority carriers to be collected at poly-Si contact [21][22]. Possible mechanisms of transport from crystalline silicon into poly-Si across $SiO_2$ are based on tunnelling [23][24], mediated by pin-holes [25] or both. After annealing and hydrogenation steps, recombination current densities ($J_0$) below 1 fA/cm$^2$ and 10 fA/cm$^2$ for n-type and p-type poly-Si/$SiO_2$ junctions, respectively [26]. A conversion efficiency of 25.8% has been recently achieved applying this selective

layer at the backside of the solar cell, while keeping a classic homojunction contact at the front side [27]. A wide range of device architectures has been exploited, such as IBC [28][29][30], semi-industrial bi-facial Passivated Emitter Rear Polysilicon (PERPoly) [31] and FBC solar cells. Furthermore, poly-Si can be alloyed with oxygen or carbon during the deposition process to enhance material stability and render these contacting materials more transparent owing to a larger band gap. They have been applied in FBC devices either in a selective front surface field (FSF) [32] or at the planar back side of FBC devices in combination with a-Si:H-based CSPCs coating the textured front side [33], a so-called hybrid device. The simplest architecture combines $SiO_2$/poly-Si on both sides of the wafer in a front/rear contacted solar cell as shown in Chapter 4. In literature, this has been accomplished by Feldmann et. al. [34] and Luxembourg et. al. [35]. Nonetheless, high absorption coefficient of the relatively thick (> 20 nm) front poly-Si limits short-circuit current density ($J_{SC}$) of the solar cells. Therefore, it is necessary to mitigate these parasitic absorption losses while still employing excellent passivation quality and keeping the manufacturing process as simple as possible.

In this chapter, we present an optimization study of CSPCs with different thermal budgets for c-Si solar cells. This architecture embodies a rear emitter configuration consisting of poly-Si/$SiO_2$ hole-selective contact and an i/n a-Si:H stack acting as electron-selective contact at the front side. This solar cell architecture represents another alternative front-surface field to be employed to mitigate front parasitic absorption losses from poly-poly solar cells in Chapter 4 and avoid complicated structure as PERFeCT solar cell in Chapter 5. The hole collector has been located at the rear side to maximize collection of holes (as shown in chapter 5) and to compare rear junction solar cells fabricated here to the solar cells of Chapters 4 and 5. This architecture ensures more flexibility with the front structure because of its degree of freedom at the front side [32][36]. We investigate the passivation properties of both CSPCs on symmetric structures by optimizing the interdependency among annealing temperature, time and environment. Post-deposition annealing and layers stability are investigated to further improve the passivation quality at the c-Si/a-Si interface. Furthermore, we present a comparison between ITO and IO:H/ITO bilayer to improve the opto-electrical performance on the illuminated side of the device. Finally, the optimized layers are combined and embedded in silicon solar cells with aperture-area efficiency of up to 21%.



## 6.2. EXPERIMENTAL DETAILS

For preparing symmetric samples, we follow the same procedure highlighted in paragraph 2.2.4. Three types of dedicated symmetric samples for carrier lifetime investigation were fabricated as depicted in Figure 6.1. Samples (a) consisted of an i/n a-Si:H stack deposited on both sides by plasma enhanced chemical vapour deposition (PECVD). A gas mixture of hydrogen-diluted $SiH_4$ and $PH_3$ gas was used to obtain n-doped films. Some of these test samples were completed with 75-nm thick TCO layers on both sides (ITO or IO:H/ITO) deposited by RF sputtering with Ar as carrier gas during deposition (sample (b) in Figure 6.1). The ITO was sputtered at 110 °C and it consisted of a thin buffer layer deposited at low power (20 W) and of a bulk layer deposited at high power (200 W). The aim of this approach is to protect the a-Si:H layer stack by potential sputter damage [37]. The IO:H film was instead deposited at room temperature into amorphous

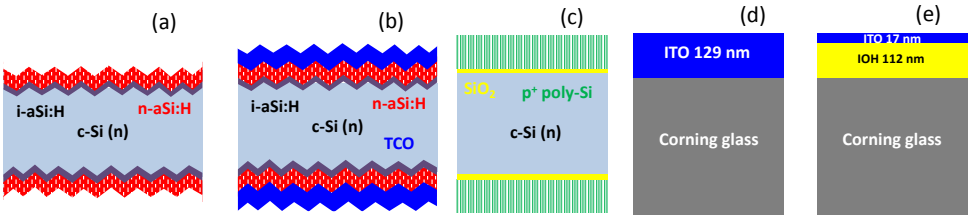


Figure 6.1: Cross-sectional sketch of symmetric lifetime samples: i/n a-Si:H (3.5 or 4.5/6 nm) stack without (a) and with (b) with 75-nm thick ITO; (c) $p^+$poly-Si/$SiO_2$ (250 nm / 1.5 nm); (d) 129-nm thick single layer ITO on corning glass; (e) IO:H/ITO (112 nm / 17 nm) stack on corning glass.

phase. A thin buffer layer is deposited also at low power (20 W) to minimize sputtering damage. Afterwards, samples (a) and (b) were annealed to further improve passivation [38] and to recover from sputtering-induced damage in air atmosphere or in 200 sccm $H_2$ flow at 180 °C for 30 minutes. In the case of IO:H sample, the annealing was performed also to crystallize the layer [15]. Ten samples of this type of samples have been prepared for characterization.

To fabricate samples (c), a wet-chemical $SiO_2$ layer is grown on the c-Si surface according to the NAOS procedure described in [39] with a nominal thickness of 1.5 nm. Subsequently, a 250-nm thick a-Si layer is deposited via LPCVD at 580 °C with $SiH_4$ flow of 45 sccm and pressure of 150 mTorr. The samples (c) were then $p^+$-doped via ex-situ B-implantation by a Varian EHP500 implanter ($BF_3$ source, dose of $5 \cdot 10^{15}$ ions/cm$^2$ and energy of 5 keV). Afterwards, these samples were annealed at 950 °C for 5 minutes to crystallize the a-Si film and simultaneously activate and diffuse the dopants atoms within the poly-Si layer. The layer used here is the same as Chapter 4.

Finally, annealing in forming gas (FG, 10% $H_2$ in $N_2$) at 400 °C for 2 hours was performed. Quasi-steady-state photoconductance (QSSPC) lifetime measurements [40] were performed using a Sinton Instruments WCT-120 on the symmetric test samples after each fabrication macro-steps. Effective lifetime ($\tau_{eff}$), implied open-circuit voltage ($iV_{OC}$) and $J_0$ were extracted from the measured curves. Furthermore, B-implanted samples (In figure 6.1 (c)) were characterized via electro-capacitance voltage (ECV) to measure active doping concentration profile in the structure. ITO and IO:H/ITO stack were deposited on glass substrates with a nominal thickness of 75 nm and 65 nm / 10 nm, respectively (Figure 6.1 (d) and (e)) to reproduce the typical, single-layer anti-reflection coating, 75-nm thick layer on textured Si, considering area factor [41]. The optical characterization was carried out using a Lambda Parker spectrophotometer and measuring reflectance (R) and transmittance (T). Sheet resistance was measured with a four-point probe, while carrier concentration and electron mobility were measured by an Ecopia 5500 Hall setup.

Solar cells were fabricated combining the layer stacks described above in the proposed hybrid configuration. The flowchart follows the steps highlighted in 2.2.4. It is important to remark that this process is particularly lean and only four main steps are employed. Compared to the standard Al front-contacted solar cells, some other cells employed Cu-plated front grid on novel Ti seed layer. The process consists of several

steps, similar to the method reported in [42]. A 300 nm-thick Ti layer was e-beam evaporated on the full area and structured by photolithography to obtain a grid pattern and act as seed-layer for the Cu electro-plating. After copper electro-plating (1.4 A direct current for 1500 seconds), we performed photoresist removal and Ti seed layer etching in $H_2O/NH_4O_4$. These steps will be highlighted in Chapter 7.

To assess the quality of the fabrication process, lifetime measurements were carried out after each fabrication macro-step. The solar cells were characterized using a class AAA Wacom WXS-156S solar simulator to extract cells' external parameters: $V_{OC}$, fill-factor (FF), short-circuit current density ($J_{SC}$) and efficiency ($\eta$). Precisely-cut metallic masks were used to properly illuminate the device. Sinton Suns$V_{OC}$ setup allowed to measure pseudo parameters, such as pseudo-FF (p-FF), which excludes the series resistance contribution.

## 6.3. RESULTS AND DISCUSSION

### 6.3.1. CARRIER-SELECTIVE CONTACTS PASSIVATION QUALITY TESTS

Low-thermal budget electron selective contacts based on a-Si:H CSPC have been characterized from different perspectives. Figure 6.2 (a-d) summarize the passivation properties of the i/n a-Si:H stack on symmetric structures fabricated on double sided textured wafers. Figure 6.2 (a) shows the effect of the i-layer thickness on the effective lifetime and implied open circuit voltage. In the as-deposited condition, the two FSF stacks exhibited a $\tau_{eff}$ of 2 ms and 4 ms for the 3.5 nm and 4.5 nm-thick layers, respectively. There is a clear i-layer thickness dependence on the passivation quality that is enhanced by a post-deposition annealing in $H_2$ environment at 190 °C for 30 minutes. Lifetime increases from 2 ms to 5 ms in the case of 3.5 nm / 6-nm i/n a-Si:H and from 4 ms to 12 ms in case of 4.5 nm / 6 nm i/n a-Si:H stack. Looking at the i$V_{OC}$ in the same Figure 6.2 (a), we measure an increase from 695 mV to 705 mV and from 704 mV to 708 mV for 3.5 nm and 4.5 nm i-layer, respectively. Post-deposition annealing further improves chemical passivation of c-Si/a-Si interface [37][43]. For the sample with 3.5 / 6-nm thick i/n a-Si:H we further investigated the dependence on post-deposition anneal time and temperatures (150 °C, 190 °C and 230 °C). The outcomes are reported in Figure 6.2 (b). The lowest temperature of 150 °C has only a limited effect on passivation reaching a saturation at 3.5 ms after 20 minutes treatment. Low annealing temperature (T = 150 °C) has a weak effect on passivation because it does not change defect density at the interface [44]. Increasing the annealing temperature, the passivation quality improves with the highest $\tau_{eff}$ of 6 ms obtained at T of 230 °C for 10 minutes. Similar results have been achieved in [45], for even higher annealing temperature. Since low temperature annealing is performed, we expect that this improvement is ascribed to i/n a-Si passivation quality improvement rather than bulk lifetime improvement.

For longer treatment time the passivation performances progressively degraded to 4 ms after 50 minutes. For the intermediate temperature of 190 °C, $\tau_{eff}$ increases with the treatment time in the first 30 minutes; above this threshold the measured lifetime stays constant at 5.5 ms. Furthermore, we investigated the stability of the annealed samples at 190 °C for 30 minutes and 230 °C for 20 minutes after exposing them to air for 48 hours as depicted in Figure 6.2 (c). This analysis is made to understand what are the

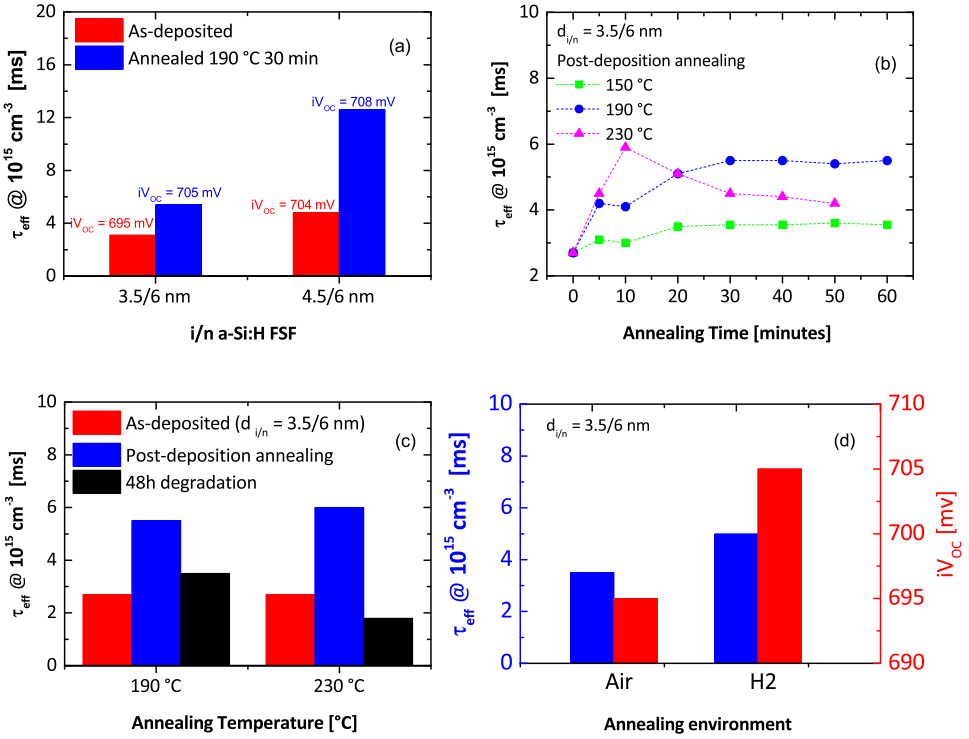


Figure 6.2: (a) Passivation quality of double sided textured wafer passivated with 3.5 nm / 6 nm or 4.5 nm / 6 nm i/n a-Si:H stack. (b) Effective lifetime at minority carrier density of $10^{15}$ $cm^{-3}$ versus post-deposition annealing time in air at different temperatures for a double sided textured wafer passivated by 3.5 nm / 6 nm i/n a-Si:H. (c) Degradation of lifetime against two different post-deposition annealing temperatures for a double sided textured wafer passivated by 3.5 nm/6 nm i/n a-Si:H. (d) Lifetime and $iV_{OC}$ versus two different annealing environments for a double sided textured wafer passivated by 3.5 nm /6 nm i/n a-Si:H.

processing conditions to be implemented during solar cells fabrication. Both samples have a comparable initial and post-deposition annealing lifetime, but the degradation effect is different. The sample treated at lower temperature 190 °C has a lifetime twice that of the one annealed at 230 °C with corresponding loss in $\tau_{eff}$ by 60% after 48 hours. In [46] and [47], slower degradation is observed. The mechanism for this phenomenon is not entirely understood. A possible explanation could be a different re-arrangement of hydrogen atoms into the a-Si structure with respect to the annealing temperature [48]. Finally, we investigated the effect of the annealing environment on passivation quality. The annealing in air is compared to the $H_2$ atmosphere in Figure 6.2 (d). As found in [49], we expect that the $H_2$ gas improves the surface passivation quality by providing additional $H^+$ atoms that can diffuse from the ambient to the i-layer and saturate dangling bonds at the (i) a-Si / c-Si interface [50]. The annealing in air instead restructures Si-H bonds rupture at interface a-Si/c-Si [38]. The results confirm the expectations with an increase in lifetime from 3.5 ms up to 5.5 ms and $iV_{OC}$ improvement from 695 mV to 705

mV. Since the TCO layer is implemented only on the front side of the investigated device (see cell sketch in 2.2.4), we monitor the effective carrier lifetime of textured wafer passivated by 4.5-nm /6-nm thick i/n a-Si:H stack covered on both sides with IO:H/ITO bilayer after the sputtering deposition. This is done to identify possible sputtering damage. As table 6.1 reports, when TCO is deposited on a-Si:H, the effective lifetime decreases from 4.1 ms in the case of a-Si:H passivation to 3.8 ms. After annealing at 180 °C for 30 minutes, lifetime increases up to 4.8 ms. This confirms that sputtering damage has been removed. This result confirms that 180 °C for 30 minutes is the optimal annealing

Table 6.1: Passivation quality of double sided textured wafer passivated by 4.5 nm /6 nm i/n a-Si:H stack and covered by sputtered 65 nm / 10 nm IO:H/ITO

| | $\tau_{eff}$ @ $10^{15}$ $cm^{-3}$ [ms] | $J_0$ [$fA/cm^2$] |
|---|---|---|
| i/n a-Si:H passivation | 4.1 | 12 |
| IOH/ITO sputtering | 3.8 | 15 |
| IOH/ITO annealed | 4.8 | 8 |

recipe to recover from induced damage due to ion bombardment during sputtering process [51]. Nonetheless, during the low-thermal budget fabrication of the this solar cell, annealing at 190 °C for 30 minutes is performed straight after a-Si:H deposition. Then, a second annealing to recover from TCO damage at 180 °C for 30 minutes is performed. This action does not affect passivation properties since a prolonged annealing at similar temperature as 190 °C leads to a saturation of carrier lifetime as shown in Figure 6.2 (b). Another reason for which lifetime is weakly affected by IO:H / ITO sputtering is that, as mentioned in the experimental details section, deposition power is very low (20 W) for the first few nanometres of deposition.



High thermal budget CSPC $SiO_2$ / p-type poly-Si has been also characterized in a symmetric test sample as shown in Figure 6.1 (c). The same features of B-doped poly-Si of Chapter 4 and 5 have been employed also here. For completeness, lifetime and ECV measurements are reported again. Figure 6.3 (a) describes effective lifetime and $J_0$ after dopant activation and after hydrogenation step. After annealing, for dopant diffusion and activation, $\tau_{eff}$ is 4 ms and $J_0$ is around 20 $fA/cm^2$. In this case, $iV_{OC}$ is 704mV. By applying FG annealing at 400 °C for 2 hours the $J_0$ decreased to 10 $fA/cm^2$, indicating that the hydrogenation improves the chemical passivation by driving $H^+$ ions to the $SiO_2$/c-Si interface [52]. In this respect, effective lifetime increased to 5 ms and $iV_{OC}$ reached 716 mV. Active doping distribution in the structure was measured before FG annealing, as reported in Figure 6.3 (b). It is worth noting that a boron doping concentration of $10^{20}$ $atoms/cm^3$ is confined inside the poly-Si layer surface progressively decreasing tail into c-Si bulk down to $10^{16}$ $atoms/cm^3$ at a depth of 300 nm. This doping difference between poly-Si and c-Si is responsible for field-effect passivation because it induces a strong electrical field across the junction that attracts only holes in this case while repelling electrons. Since the hydrogenation treatment is performed at low temperature (400 °C), the doping distribution is given by the annealing step at 950°C and it is not expected to

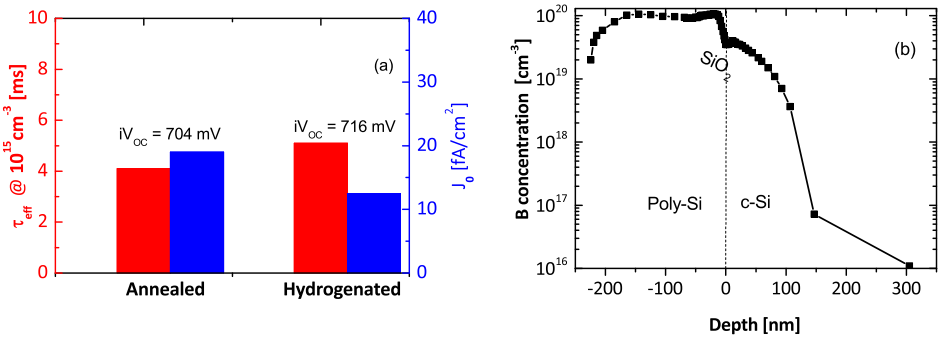


Figure 6.3: Effective lifetime (at injection level of $10^{15}$ cm$^{-3}$) and extracted $J_0$ measured on B-doped poly-Si symmetric sample in different conditions as specified. The annealing is performed at 950 °C for 5 min and hydrogenation is performed in FG at 400 °C for 2 hours, (b) ECV doping profile measured on the same B-doped poly-Si symmetric sample as shown in the inset in (a) before the annealing in FG.

change.

### 6.3.2. TRANSPARENT CONDUCTIVE OXIDE MATERIAL OPTIMIZATION

In this section, we report on optical and electrical quality of 129-nm thick sputtered ITO and IO:H/ITO deposited on glass substrates. It is important to note that 129-nm thick TCO layer is obtained on flat glass using the same recipe to achieve 75 nm-thick on textured silicon. Figure 6.4 shows the difference in absorptance between two TCOs developed in this work. The IO:H film absorbs less in ultra-violet range than ITO as already reported in literature [15]. The difference in transparency, at short wavelength, is ascribed to different bandgap of these two materials [53][54][55]. In the long wavelength range, we observe a comparable behaviour in terms of absorption between ITO and IO:H/ITO stack. If measured absorption is integrated with AM1.5 global spectrum [56], it can be translated directly into a gain in photo-generated current of 0.23 mA/cm$^2$ when IO:H/ITO stack is employed. By employing 75 nm-thick TCO on textured Si, absolute absorption will be lower but the relative difference would be similar. Figure 6.5 reports carrier density and mobility of ITO and IO:H/ITO stack in as-deposited condition and after annealing at 180 °C for 30 minutes. For the case of ITO, carrier density in as-deposited condition is $1.2 \cdot 10^{20}$ cm$^{-3}$. After annealing, it increases to $2 \cdot 10^{20}$ cm$^{-3}$. Instead mobility shows the opposite trend, it decreases from 30 to 20 cm$^2$/Vs after post-sputtering annealing. Bilayer IO:H/ITO stack has instead a carrier density in as-deposited condition of $2.4 \cdot 10^{20}$ cm$^{-3}$ and it halves when annealing is performed. Mobility shows again the opposite trend, increasing from 60 cm$^2$/Vs in as-deposited state to up to 120 cm$^2$/Vs after the post-sputtering annealing. As expected, when carrier concentration is increasing, mobility is decreasing and vice versa [57]. Post-sputtering annealing is performed in both cases to know how the TCO will behave while simulating the recover from sputter-induced damage [51]. In case of IO:H/ITO bilayer, the post-sputtering annealing plays also the crucial role of transforming the IO:H film from its amorphous phase to poly-crystalline [15]. Measured values are well in accordance to state-of-the-art results [58][59], also with respect to resistivity ($\rho_{ITO}$ = $1.5 \cdot 10^{-3}$ Ωcm,

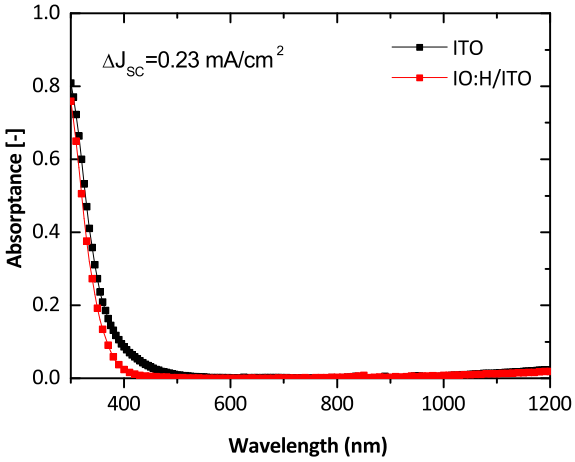


Figure 6.4: Absorptance (1-R-T) curves of 129 nm-thick ITO and 117 nm / 12 nm-thick IO:H/ITO layer stack deposited on glass substrates (sketch in Figure 6.1 (d) and (e)).

$\rho_{IO:H/ITO}$ = 5.4 · $10^{-4}$ Ωcm after annealing). This analysis shows a representative range of values for 75-nm thick TCO on textured Si since its thickness dependence is weak in the range 70 – 140 nm [60] [61].



### 6.3.3. SOLAR CELL DEMONSTRATORS

The optimized layer stacks discussed so far were combined in solar cells following the fabrication process described in 2.2.4. Figure 6.6 reports effective lifetime and $iV_{OC}$ after each fabrication macro-step. As reported in Figure 6.6, our process does not harm the passivation quality. Following all the steps described in 2.2.4, the effective lifetime lies above 4 ms and the $iV_{OC}$ above 705 mV. This means that no additional contamination is introduced during our process and eventual damage due to sputtering has been recovered. For the particular solar cell shown in Figure 6.6, we employed annealing at 190 °C for 30 minutes after a-Si:H deposition and we deposited IO:H / ITO stack (solar cell SC2 in table 6.2). The lifetime measurement shown in Figure 6.6 is performed after post-TCO sputtering annealing at 180° for 30 minutes. Table 6.2 reports solar cells external parameters for different devices with variable intrinsic a-Si:H thickness. For SC1, which did not undergo any post-deposition annealing, the $V_{OC}$ lies below 700 mV, while $J_{SC}$ is 36.5 mA/cm$^2$ and FF is 71.6%. The $J_{SC}$ is affected by parasitic absorption into i-layer. For this reason, we fabricated SC2 with a 3.5-nm thick i-layer. By employing IO:H/ITO stack, $J_{SC}$ is established to 37 mA/cm$^2$. $J_{SC}$ is 0.5 mA/cm$^2$ higher because of two factors: (i) 1 nm thinner intrinsic a-Si:H and (ii) improved TCO transparency due to IO:H. In SC2, $V_{OC}$ is 703 mV due to post-a-Si:H deposition annealing and FF is limited 71%. This limitation comes from the front grid design. In fact, by passing to a larger area and a different front design (9-cm$^2$ wide square shaped with bus bars outside the active area and 2.64% metal shading), SC3 exhibits a higher $J_{SC}$ up to 39.7 mA/cm$^2$ and $FF$ = 72%. With such front contact design and device area, if only ITO is employed as in SC4, FF increases up to

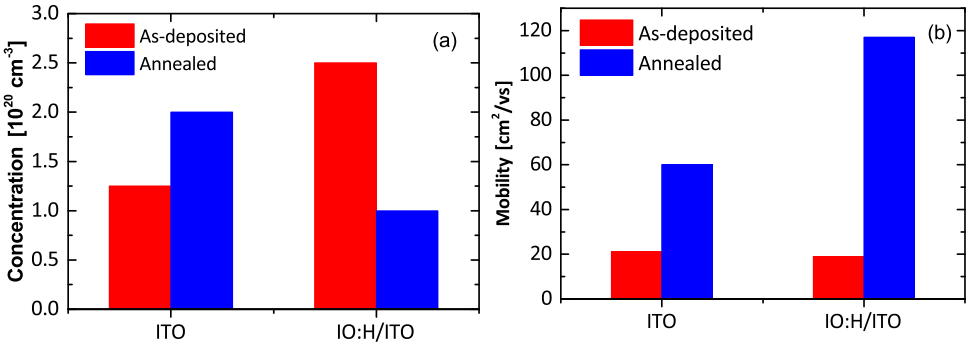


Figure 6.5: (a) Carrier concentration and (b) mobility of samples in Figure 6.1 (d) and (e) with ITO or IO:H/ITO stacks before and after annealing at 180 °C for 30 minutes.

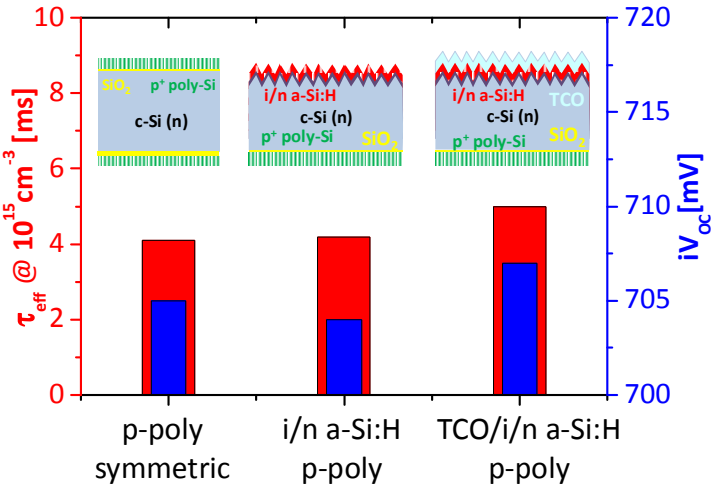


Figure 6.6: Effective lifetime and $iV_{OC}$ measurement after each macro-step of solar cell fabrication. In the inset, each fabrication macro-step prior metallization is depicted.

73.8% because of a better band alignment at a-Si/ITO interface compared to IO:H/ITO stack [62]. This is due to higher carrier concentration in ITO that results in lower work-function than IO:H/ITO [63], therefore a more favourable condition for n-type contact. Nonetheless, $J_{SC}$ decreases of 0.2 mA/cm$^2$ compared to SC3 because of higher parasitic absorption in the ITO TCO while $V_{OC}$ is kept at 704 mV. Finally, the overall aperture-area efficiency of SC3 is 20.7% and, for SC4, it is 21.0%. The main difference between SC2 and SC3 is the front grid design. Indeed, SC2 employs an H-grid design with one busbar and 15 fingers with a 5% metal coverage. SC3 instead has a busbar-less design with 10 fingers to achieve 2.64% metal coverage. Ti-seeded Cu-plated contacts have been employed at

the front side of SC5. This contact formation technology enables a 0.3% absolute higher FF compared to SC4. However, as the process is not fully optimized yet, Cu is grown outside the designated area, costing a loss of 10 mV in $V_{OC}$ and affecting also the $J_{SC}$. This effect is known as background plating [64] and solar cells performance might have been hindered due to Cu contamination [65]. Looking at the pFF column in 6.2, all our devices exhibit values > 81% and up to 83%. This implies that our process is not fundamentally flawed but rather limited by (i) the rear metallization, (ii) the possible dis-uniformity of the tunnelling oxide at the rear side and (iii) the conductivity of the front TCO. It is important to remark that the solar cells are made together with quality control of each layer at every macro-step (Lifetime measurement, thickness measurement ecc), until the point the solar cells are differentiated in the specific process (Different TCO, different metallization).

Table 6.2: External parameters of solar cells, (*) indicates that no annealing has been performed after a-Si:H deposition, (**) indicates that SC5 is the same as SC4 but with Ti-Cu plated front contacts.

| Solar cell | Area [$cm^2$] | $d_{i/n}$ [nm] | $d_{IOH/ITO}$ [nm] | $V_{OC}$ [mV] | $J_{SC}$ [$mA/cm^2$] | FF [%] | Metal Fraction [%] | $\eta$ [%] | $\eta_{aperture}$ [%] | pFF [%] |
|---|---|---|---|---|---|---|---|---|---|---|
| SC1* | 7.84 | 4.5/6 | 0/75 | 695 | 36.5 | 71.0 | 5.0 | 18.1 | 19.0 | 81.0 |
| SC2 | 7.84 | 3.5/6 | 65/10 | 703 | 37 | 71.2 | 5.0 | 18.5 | 19.4 | 81.0 |
| SC3 | 9.00 | 4.5/6 | 65/10 | 707 | 39.7 | 72.0 | 2.64 | 20.1 | 20.7 | 82.1 |
| SC4 | 9.00 | 4.5/6 | 0/75 | 704 | 39.5 | 73.8 | 2.64 | 20.4 | 21.0 | 81.6 |
| SC5** | 9.00 | 4.5/6 | 0/75 | 694 | 36.2 | 74.1 | 2.64 | 18.6 | 19.1 | 83.0 |



Once more, by employing a SHJ full-area FSF, it is possible to mitigate the front-parasitic absorption losses into poly-poly solar cells shown in Chapter 4. The processing of this solar cell architecture is also much simpler than PERFeCT shown in Chapter 5. To obtain 40 $mA/cm^2$, a dedicated design of the solar cell front grid was made to keep low optical shading losses while still mantaining a good transport of electrons at the front side. Since we are employing 10 nm-thick a-Si:H FSF, front parasitic absorption is reduced compared to a 20 nm-thick front poly-Si FSF. By employing 10 nm-thick poly-Si FSF, the parasitic absorption would be similar but, at the state of our technology, the passivation would be much poorer.

## 6.4. CONCLUSION

In this work we applied carrier-selective passivating contacts with different thermal budgets to obtain a low thermal budget device. It consists in a rear p-type poly-Si/$SiO_2$ emitter annealed at temperatures up to 950 °C, followed by a low thermal budget deposition ( 200 °C) of an intrinsic/n-type doped a-Si:H stack / TCO on the illuminated front side. We firstly investigated passivation properties of these CSPCs in dedicated symmetric samples. The poly-Si/$SiO_2$ passivation contact benefits from hydrogenation process with $J_0$ of around 10 $fA/cm^2$ owing to improved chemical passivation at $SiO_2$/c-Si interface. Concerning the i/n a-Si:H stack, we observed that post-deposition annealing improves passivation quality with an optimum annealing temperature of 190 °C. This effect is most likely due to a redistribution of hydrogen atoms into the film and at the

c-Si/a-Si:H interface. Furthermore, we showed that annealing in $H_2$ leads to improved chemical passivation of the same surface. A series of annealing temperatures was made and 190 °C was found to be the most performing if 48 hours degradation is considered. Moreover, also annealing environment is important. Indeed, annealing in $H_2$ has a better performance than conventional nitrogen environment. Moreover, we show the use two different TCO layer stacks consisting of either a single layer of ITO or a bi-layer of IO:H/ITO. Optical absorption measurement showed that the use of IO:H improves the transparency in the short-wavelength range with respect the ITO. Measured mobility is much higher for the IO:H/ITO stack (120 $cm^2$/Vs) than ITO (20 $cm^2$/Vs) and resistivity is lower in case of IO:H/ITO ($\rho_{ITO} = 1.5 \cdot 10^{-3}$ Ωcm, $\rho_{IO:H/ITO} = 5.4 \cdot 10^{-4}$ Ωcm after annealing). Post-sputtering annealing not only recovers from sputtering-induced damage, but also increases the mobility of our bi-layer TCO. In this chapter we have demonstrated that at cell level, we keep high $V_{OC} > 700$ mV if annealing after a-Si:H deposition is performed. Then, changing front metal design with relatively low metal coverage (2.6%), $J_{SC}$ increases up to 40 mA/$cm^2$ and FF is 72% for the case of IO:H/ITO stack and 73.8% in the case of ITO only (up to 74.1% with Cu-plated front contact). Such FF value, together with a $V_{OC} = 704mV$ and a $J_{SC} = 39.5mA/cm^2$ gives an aperture area efficiency of 21.0%. Some processing issues (Cu-plating, backside edge isolation (pattering of the conductive layers at wafer level to avoid cross-talking between adjacent cells and consequent cut), rear metallization, front TCO, etc.) still hold better performance, which targets an efficiency well beyond 22.5% in short term ($V_{OC} > 705mV, J_{SC} > 40.5mA/cm^2, FF > 79\%$).



## 6.5. REFERENCES

[1] C. Battaglia, A. Cuevas and S. D. Wolf, High-efficiency crystalline silicon solar cells: status and perspectives, Energy and Environmental Science, pp. 1552-1576, 2016, DOI:10.1039/C5EE03380B.

[2] M. Green, (2015), The Passivated Emitter and Rear Cell (PERC): From conception to mass production. Progress in Photovoltaics Research and Applications, https://doi.org/10.1016/j.solmat.2015.06.055.

[3] A Wolf,. D. Biro, J. Nekarda, S. Stumpp, A. Kimmerle, S. Mack, R. Preu, Comprehensive Analytical Model for Locally Contacted Rear Surface Passivated Solar Cells. J. Appl. Phys. 2010, 108 (12), 124510. https://doi.org/10.1063/1.3506706.

[4] A. Cuevas, Physical Model of Back Line-Contact Front-Junction Solar Cells. J. Appl. Phys. 2013, 113 (16), 164502. https://doi.org/10.1063/1.4800840.

[5] P. Wurfel, Physics of Solar Cells: From Principles to New Concepts, WILEY - VCH Verlag GmbH - Co. KGaA, 2008.

[6] S. D. Wolf, A. Descoeudres, Z. C. Holman and C. Ballif, High-efficiency Silicon Heterojunction Solar Cells: A Review, Green, vol. 2, no. 1, pp. 7-24, 2012. https://doi.org/10.1515/green-2011-0018.

[7] M. Taguchi, A. Yano, S. Tohoda, K. Matsuyama, Y. Nakamura, T. Nishiwaki, K. Fujita, and E. Maruyama, 24.7% Record Efficiency HIT Solar Cell on Thin Silicon Wafer, IEEE JPV, 4, 1 (2014). doi: 10.1109/JPHOTOV.2013.2282737.

[8] D. Adachi, J. L. Hernández, and K. Yamamoto, Impact of carrier recombination on fill factor for large area heterojunction crystalline silicon solar cell with 25.1% efficiency, Applied Physics Letters 2015 107:23. https://doi.org/10.1063/1.4937224.

[9] Kenji Yamamoto, Kunta Yoshikawa, Hisashi Uzu and Daisuke Adachi, High-efficiency heterojunction crystalline Si solar cells, 10.7567/JJAP.57.08RB20, 2018

[10] D. Deligiannis, S. Alivizatos, A. Ingenito. D. Zhang, M. van Sebille, R.A. C. M. M. van Swaaij, M. Zeman, Wet-chemical Treatment for Improved Surface Passivation of Textured Silicon Heterojunction Solar Cells, Energy Procedia, 55, 197-202 (2014). https://doi.org/10.1016/j.egypro.2014.08.117.

[11] S. Bowden, U. Das, S. Herasimenka, R. Birkmire, Stability of amorphous/crystalline silicon heterojunctions, 2008 33rd IEEE Photovoltaic Specialists Conference, San Diego, CA, USA, 2008, pp. 1-4. doi: 10.1109/PVSC.2008.4922850.

[12] D. Zhang, R.A. C. M. M. van Swaaij, M. Zeman, Influence of Intrinsic Layer Thickness in the Emitter and BSF of HIT Solar Cells, 27th European Photovoltaic Solar Energy Conference and Exhibition (2012). Doi: 10.4229/27thEUPVSEC2012-2BV.6.3

[13] S. D. Wolf and M. Kondo, Nature of doped a-Si:H/c-Sia-Si:H/c-Si interface recombination, Journal of Applied Physics 105, 103707 (2009); https://doi.org/10.1063/1.3129578

[14] Z. C. Holman, A. Descoeudres, L. Barraud , F.Z. Fernandez, J.P. Seif, S.D. Wolf, C. Ballif, Current Losses at the Front of Silicon Heterojunction Solar Cells, in IEEE Journal of Photovoltaics, vol. 2, no. 1, pp. 7-15, Jan. 2012. doi: 10.1109/JPHOTOV.2011.2174967

[15] T Koida, H Fujiwara, M Kondo, Reduction of Optical Loss in Hydrogenated Amorphous Silicon/Crystalline Silicon Heterojunction Solar Cells by High-Mobility Hydrogen-Doped In2O3 Transparent Conductive Oxide, 2008 Appl. Phys. Express 1 041501, https://doi.org/10.1143/APEX.1.041501 .

[16] L. Barraud, Z.C. Holman, N. Badel, P. Reiss, A. Descoeudres, C. Battaglia, S. De Wolf, C. Ballif, Hydrogen-doped indium oxide/indium tin oxide bilayers for high-efficiency silicon heterojunction solar cells, Solar Energy Materials and Solar Cells, Volume 115, 2013, Pages 151-156 ,ISSN 0927-0248, https://doi.org/10.1016/j.solmat.2013.03.024.

[17] E. Yablonovitch et. al., A 720 mV open circuit voltage SiOx:c-Si:SiOx double heterostructure solar cell, applied physics letters, vol. 47, p 1211, 1985, https://doi.org/10.1063/1.96331

[18] A. Moldovan, F. Feldmann, M. Zimmer, J. Rentsch, J. Benick, M. Hermle, Tunnel oxide passivated carrier-selective contacts based on ultra-thin SiO2 layers, Solar Energy Materials and Solar Cells,Volume 142, November 2015, Pages 123-127. https://doi.org/10.1016/j.solmat.2015.06.048.

[19] M. Stodolny et al., 'Material properties of LPCVD processed n-type polysilicon passivating contacts and its application in PERPoly industrial bifacial solar cells', Energy Procedia 124, 2017, pp. 635-642.

[20] F. Feldmann, R. Müller, C. Reichel, M. Hermle , Ion implantation into amorphous Si layers to form carrier-selective contacts for Si solar cells, physica status solidi (RRL) – Rapid Research Letters, vol.08, pp. 767-770, 2014. https://doi.org/10.1002/pssr.201409312.

[21] J. Melskens, B. van de Loo, B. Macco, M. Vos, J. Palmans, S. Smit and W. Kessels, Concepts and prospects of passivating contacts for crystalline silicon solar cells, in IEEE 42nd Photovoltaic Specialist Conference, New Orleans, 2015.

[22] J. Melskens et al, 'Passivating Contacts for Crystalline Silicon Solar Cells: From

Concepts and Materials to Prospects', IEEE Journal of Photovoltaics 8 (2), March 2018.

[23] F. Feldmann et al., 'A Study on the Charge Carrier Transport of Passivating Contacts', IEEE Journal of Photovoltaics 2018, pp. 1-7

[24] Zhang et al., 'Carrier transport through the ultrathin silicon-oxide layer in tunnel oxide passivated contact (TOPCon) c-Si solar cells', Solar Energy Materials and Solar Cells Volume 187, 2018, pp. 113-122.

[25] R. Peibst, U. Römer, Y. Larionova, M. Rienäcker, A. Merkle, N. Folchert, S. Reiter, M. Turcu, B. Min, J. Krügener, D. Tetzlaff, E. Bugiel, T. Wietler, R. Brendel, Working principle of carrier selective poly-Si/c-Si junctions: Is tunnelling the whole story?, Solar Energy Materials and Solar Cells, Volume 158, Part 1,2016,Pages 60-67, https://doi.org/10.1016/j.solmat.2016.05.045.

[26] R. Peibst, Y. Larionova, S. Reiter, M. Turcu, R. Brendel, D. Tetzlaff, J. Krügener, T. Wietler, U. Höhne, J.-D. Kähler, H. Mehlich, S. Frigge, Implementation of n+ and p+ Poly Junctions on Front and Rear Side of Double-Side Contacted Industrial Silicon Solar Cells, EUPVSEC, 2016, Munich, Germany

[27] A. Richter et. al., n-Type Si solar cells with passivating electron contact: identifying sources for efficiency limitations by wafer thickness and resistivity variation. Sol Energy Mater Sol Cell. 2017;173:96 - 105. https://doi.org/10.1016/j.solmat.2017.05.042.

[28] G. Yang., A. Ingenito, O. Isabella, M. Zeman, IBC c-Si solar cells based on ion-implanted poly-silicon passivating contacts, Solar Energy Materials and Solar Cells, 158, 84-90 (2016), https://doi.org/10.1016/j.solmat.2016.05.041.

[29] U. Römer, R. Peibst, T. Ohrdes, B. Lim, J. Krügener, T. Wietler, R. Brendel, Ion Implantation for Poly-Si Passivated Back-Junction Back-Contacted Solar Cells, IEEE Journal of Photovoltaics, 5, 507-514 (2015). doi: 10.1109/JPHOTOV.2014.2382975.

[30] https://isfh.de/en/26-1-record-efficiency-for-p-type-crystalline-si-solar-cells/ (accessed 21st of August 2018).

[31] M. Stodolny, M. Lenes, Y.Wu, G. Janssen, I. Romijn, J. Luchies and L. Geerligs, n-Type polysilicon passivating contact for industrial bifacial n-type solar cells, Solar Energy Materials and Solar Cells, Volume 158, Part 1, 2016, Pages 24-28, https://doi.org/10.1016/j.solmat.2016.06.034.

[32] A. Ingenito, G. Limodio, P. Procel, G. Yang, H. Dijkslag, O. Isabella and M. Zeman, (2017), Silicon Solar Cell Architecture with Front Selective and Rear Full Area Ion-Implanted Passivating Contacts. Sol. RRL, 1: n/a, 1700040. doi:10.1002/solr.201700040.

[33] G. Nogay, J. Stuckelberger, P. Wyss, E. Rucavado, C. Allebé, T. Koida, M. Morales-Masis, M. Despeisse, F.J Haug, P. Löper, C. Ballif, Interplay of annealing temperature and doping in hole selective rear contacts based on silicon-rich silicon-carbide thin films, Solar Energy Materials and Solar Cells, Volume 173,2017, Pages 18-24, https://doi.org/10.1016/j.solmat.2017.06.039.

[34] F. Feldmann, M. Simon, M. Bivour, C. Reichel, M. Hermle and S. W. Glunz., "Efficient carrier selective p- and n- contacts for Si solar cells," Solar Energy Materials and Solar Cells, vol. 131, pp. 100-104, 2014. https://doi.org/10.1016/j.solmat.2014.05.039S.

[35] S. L. Luxembourg, D. Zhang, Y. Wu, M. Najafi, V. Zardetto, W. Verhees, A. R. Burgers, S. Veenstra, L.J. Geerligs, Crystalline silicon solar cell with front and rear polysilicon passivated contacts as bottom cell for hybrid tandems, Energy Procedia, Volume 124, 2017, Pages 621-627, https://doi.org/10.1016/j.egypro.2017.09.091.

[36] Bivour, M., Schröer, S., Hermle, M., Glunz, S. W., Sol. Energ. Mater. 15, Sol. Cell. 2014, 122, 120.

[37] L. Tutsch, M. Bivour, W. Wolke, M. Hermle, J. Rentsch, Influence of the transparent electrode sputtering process on the interface passivation quality of silicon heterojunction solar cells, 33rd European PV Solar Energy Conference and Exhibition, 24-29 September 2017, Amsterdam, The Netherlands

[38] J.W.A.Schüttauf, C.H.M.van der Werf,.M.Kielen, W.G.J.H.M.van Sark, J.K.Rath, R.E.I.Schropp, Improving the performance of amorphous and crystalline silicon heterojunction solar cells by monitoring surface passivation, Journal of Non-Crystalline Solids, Volume 358, Issue 17, 1 September 2012, Pages 2245-2248, https://doi.org/10.1016/j.jnoncrysol.2011.12.063.

[39] G. Yang, A. Ingenito, N. v. Hameren, O. Isabella and M. Zeman, Design and application of ion-implanted polySi passivating contacts for interdigitated back contact c-Si solar cells, Applied Physics Letters, p. 108, 2016. https://doi.org/10.1063/1.4940364 .

[40] R. Sinton, A. Cuevas and M. Stuckings, "Quasi-steady-state photoconductance, a new method for solar cell material and device characterization," in Conference Record of the IEEE Photovoltaic Specialists Conference, 1996.

[41] S. Olibet, C. Monachon, A. Hessler-Wyser, E. Vallat-Sauvain, S. De Wolf, L. Fesquet, J. Damon-Lacoste, C. Ballif, Textured silicon heterojunction solar cells with over 700 mv open-circuit voltage studied by transmission electron microscopy, 23rd European Photovoltaic Solar Energy Conference, 1-5 September 2008, Valencia, Spain.

[42] A. Lachowicz, J. Geissbühler, A. Faes, J. Champliaud, J. Hermans, J.F Lerat, P.J Ribeyron, C. Roux, G. Wahli, P. Papet, B. Strahm, J. Horzel, C. Ballif and M. Despeisse, Reliable copper plating process for bifacial heterojunction cells, 7th Workshop on Metallization - Interconnection for Crystalline Silicon Solar Cells, 23. October 2017, Konstanz

[43] A. Illiberi, K.Sharma, M. Creatore and M.C.M van de Sanden, (2010), Role of a-Si:H bulk in surface passivation of c-Si wafers. phys. stat. sol. (RRL), 4: 172–174. doi:10.1002/pssr.201004139

[44] M. Mews, T. F. Schulze, N. Mingirulli and L. Korte, Hydrogen plasma treatments for passivation of amorphous-crystalline silicon-heterojunctions on surfaces promoting epitaxy, Applied Physics Letters 2013,102:12, https://doi.org/10.1063/1.4798292.

[45] M. Edwards, S. Bowden, U. Das, M. Burrows, Effect of texturing and surface preparation on lifetime and cell performance in heterojunction silicon solar cells, Solar Energy Materials and Solar Cells, Volume 92, Issue 11, 2008, Pages 1373-1377, https://doi.org/10.1016/j.solmat.2008.05.011

[46] S. Bowden, U. Das, S. Herasimenka and R. Birkmire, Stability of amorphous/crystalline silicon heterojunctions, 2008 33rd IEEE Photovoltaic Specialists Conference, San Diego, CA, USA, 2008, pp. 1-4.doi: 10.1109/PVSC.2008.4922850

[47] X. Cheng, E. Stensrud Marstein, C.C. You, H. Haug, M. Di Sabatino, Temporal stability of a-Si:H and a-SiNx:H on crystalline silicon wafers, Energy Procedia, Volume 124, 2017, Pages 275-281, ISSN 1876-6102, https://doi.org/10.1016/j.egypro.2017.09.299.

[48] H. Plagwitza, B. Terheiden and R. Brendel, Staebler–Wronski-like formation of defects at the amorphous-silicon–crystalline silicon interface during illumination, Journal of Applied Physics 2008 103:9, https://doi.org/10.1063/1.2913320

[49] F. Wang, X. Zhang, L. Wang, Y. Jiang, C. Wei, S. Xua and Y. Zhao, Improved

amorphous/crystalline silicon interface passivation for heterojunction solar cells by low-temperature chemical vapor deposition and post-annealing treatment, Phys. Chem. Chem. Phys., 2014, 16, 20202, DOI: 10.1039/c4cp02212b.

[50] S. Olibet, E. Vallat-Sauvain, L. Fesquet, C. Monachon, A. Hessler-Wyser, J. Damon-Lacoste, S. De Wolf. and C. Ballif (2010), Properties of interfaces in amorphous/crystalline silicon heterojunctions. phys. stat. sol. (a), 207: 651–656. doi:10.1002/pssa.200982845.

[51] B. Demaurex, S. De Wolf, A. Descoeudres, Z. C. Holman, and C. Ballif, Damage at hydrogenated amorphous/crystalline silicon interfaces by indium in oxide overlayer sputtering, Appl. Phys. Lett. 101, 171604 (2012), https://doi.org/10.1063/1.4764529.

[52] Schnabel et al. 'Hydrogen passivation of poly-Si/SiOx contacts for Si solar cells using Al2O3 studied with deuterium', Appl. Phys. Lett. 112, 203901 (2018). [53] T. Koida, H. Fujiwara and M. Kondo, Hydrogen-Doped In2O3 as High-Mobility Transparent Conductive Oxide, Japanese Journal of Applied Physics, 46, L685 (2007).

[54] O. Bierwagen, 2015 Semicond. Sci. Technol. 30 024001, https://doi.org/10.1088/0268-1242/30/2/024001

[55] L. Gupta, A. Mansingh, P.K. Srivastava, Band gap narrowing and the band structure of tin-doped indium oxide films, Thin Solid Films, Volume 176, Issue 1, 1989, Pages 33-44, https://doi.org/10.1016/0040-6090(89)90361-1.

[56] https://www.pveducation.org/pvcdrom/appendices/standard-solar-spectra (Accessed 21st September 2018)

[57] K. Ellmer and R. Mientus, Carrier transport in polycrystalline transparent conductive oxides: A comparative study of zinc oxide and indium oxide, Thin Solid Films 516, 4620(2008), https://doi.org/10.1016/j.tsf.2007.05.084.

[58] Y. Kuang, B. Macco, B. Karasulu, C. K. Ande, P. C.P. Bronsveld, M. A. Verheijen, Y. Wu, W.M.M. Kessels, Ruud E.I. Schropp, Towards the implementation of atomic layer deposited In2O3:H in silicon heterojunction solar cells, Solar Energy Materials and Solar Cells, Volume 163, 2017, Pages 43-50, https://doi.org/10.1016/j.solmat.2017.01.011.

[59] R. B. H. Tahar, T. Ban, Y. Ohya, and Y. Takahashi, Tin doped indium oxide thin films: Electrical properties, Journal of Applied Physics 83, 2631 (1998). https://doi.org/10.1063/1.367025.

[60] C. Nunes de Carvalho, A. Luis, G. Lavareda, E. Fortunato, A. Amaral, Surface and Coatings Technology 151 – 152 (2002) 252–256, DOI: 10.1016/S0257-8972(01)01641-3

[61] Ir. Ariyanto Wibowo Setia Budhi, Hydrogenated Indium Oxide (IO:H) for Thin Film Solar Cell, https://repository.tudelft.nl/islandora/object/uuid:78eed80f-2d9e-4c9a-b806-40b8adb9ccda/datastream/OBJ/download

[62] Paul Procel, Guangtao Yang, Olindo Isabella, Miro Zeman, Theoretical evaluation of contact stack for high efficiency IBC-SHJ solar cells, Solar Energy Materials and Solar Cells, Volume 186, 2018, Pages 66-77, https://doi.org/10.1016/j.solmat.2018.06.021.

[63] Andreas Klein, Christoph Korber,Andre Wachau, Frank Sauberlich, Yvonne Gassenbauer, Steven P. Harvey, Diana E. Proffitt and Thomas O. Mason, Transparent Conducting Oxides for Photovoltaics: Manipulation of Fermi Level, Work Function and Energy Band Alignment, Materials 2010, 3, 4892-4914; doi:10.3390/ma3114892

[64] Stefan Braun, Annika Zuschlag, Bernd Raabe, Giso Hahn, The Origin of Back-

ground Plating, Energy Procedia, Volume 8, 2011, Pages 565-570, ISSN 1876-6102, https://doi.org/10.1016/j.egypro.2011.06.183.

[65] Andreas Büchler, Sven Kluska, Jonas Bartsch, Gisela Cimiotti, Andreas A. Brand, Martin C. Schubert, Markus Glatthaar, Optimizing adhesion of laser structured plated Ni-Cu contacts with insights from micro characterization, Energy Procedia 92 ( 2016 ) 913 – 918, doi: 10.1016/j.egypro.2016.07.101.

# 7

# COPPER PLATING METALLIZATION FOR C-SI SOLAR CELLS EMBEDDING CARRIER-SELECTIVE PASSIVATING CONTACTS

*ABSTRACT - In this chapter we develop in parallel two fabrication methods for copper electro-plated contacts suitable for either silicon nitride or transparent conductive oxide anti-reflective coatings. We employ alternative seed layers, such as evaporated Ag or Ti, and optimize the Ti- or Ag-Cu contacts with the respect to uniformity of plating and aspect ratio of the final plated grid. Moreover, we test plating/de-plating sequence instead of a direct current plating and placing an additional $SiO_2$ layer to solve undesired plating outside the designed contact openings. The main objective of this chapter is to explore the physical limit of this contact formation technology whilst keeping the process compatible with industrial adoption. In addition, we employ the optimized Cu-plating contacts in three different front/back-contacted c-Si solar cells architectures: (i) silicon heterojunction solar cell with hydrogenated nano-crystalline silicon oxide as doped layers, (ii) thin $SiO_2$ / doped poly-Si-poly-Si solar cell, and (iii) hybrid solar cell endowed with rear thin $SiO_2$ / poly-Si contact and front heterojunction contact. To investigate the metallization quality, we compare fabricated devices to reference ones obtained with standard front metallization (Ag screen printing and Al evaporation). We observe a relatively small drop in $V_{OC}$ by 5 to 10 mV by using Cu-plating front grid, while FF was improved for solar cells with Cu-plated front contact if compared to evaporated Al.*

Parts of this chapter have been submitted to IEEE Journal of Photovoltaics G. Limodio et. al., IEEE JPV, Under Review

## 7.1. INTRODUCTION

THE final step in solar cells fabrication consists in metallization, that allows the extraction of collected electron/hole pair generated in the absorber layer and transported across contact stacks. This step is critical, since it greatly affects solar cell performance [1]. For c-Si solar cells, the state-of-the-art of metallization technology is screen printing of Al or Ag paste followed by curing at high temperature to actually form the contact [2]. By using such technique, commonly measured value of contact and line resistivity are in the range of 0.22 - 1.45 m$\Omega$/cm$^2$ and 2 $\mu\Omega$/cm, respectively [3]. Standard solar cells such as homojunction [4], Al-BSF or PERC [5] solar cells can survive to such high temperature treatment and take advantage of the high contact quality. The high thermal budget gives different benefits; (i) low resistance of the metal fingers, (ii) low contact resistivity between metal and doped Si and (iii) high industrial throughput. Among solar cells architectures, carrier-selective passivating contacts (CSPCs) have the advantage of much lower surface recombination velocity at Si/metal interface by adding layers capable to perform chemical passivation and collect the photogenerated carriers selectively [6]. A very well-known example of CSPC is represented by silicon heterojunction (SHJ) solar cells performing open circuit voltages ($V_{OC}$s) of 750 mV [7], conversion efficiencies beyond 25% in front/back-contacted (FBC) [8] and 26.7% in interdigitated back-contacted (IBC) configuration [9]. The use of the intrinsic hydrogenated amorphous silicon (a-Si:H) provides chemical passivation, while doped a-Si:H induces a field-effect passivation that makes this contact selective. SHJ solar cells are very sensitive to temperature above 250 °C with strong degradation effect on $V_{OC}$ [10]. The metallization step becomes thus very critical for device performances.



Therefore, low-temperature Ag paste has been developed for screen printing of such sensitive devices. Curing temperature in the range 150-230 °C are sufficient to dry the paste and form a working contact between Ag and transparent conductive oxide (TCO) avoiding degradation of the a-Si:H passivation quality [11]. Moreover, also thermal evaporation is a low-temperature solution for a good contact formation in SHJ solar cells [12]. Another example of CSPC is a stack composed of ultra-thin $SiO_2$, typically grown via chemical, thermal or ozone oxidation [13][14] coated by an in- or ex-situ doped poly-Si layer, typically deposited by plasma-enhanced / low pressure chemical vapour deposition (PE/LPCVD) [15][16][17]. The carrier selectivity is achieved by (i) slightly different band-gap between poly-Si and c-Si, (ii) large difference between the quasi Fermi levels of the doped poly-Si and the c-Si and (iii) high tunnelling probability across the ultra-thin $SiO_2$ [18]. The transport mechanism across $SiO_2$ is mediated either by tunnelling [19][20] or pinholes [21]. By combining this layer (in the role of back surface field) with homojunction front emitter in FBC solar cell, efficiency of 25.8% has been achieved [22], while in IBC architecture an efficiency of 26.1% has been measured [23]. In some cases, poly-Si is covered by a stack of aluminium-doped zinc-oxide / indium tin oxide (ITO) stack [24] as transparent conductive oxide (TCO) layer and anti-reflection coating (ARC). In some other cases, silicon nitride ($SiN_x$) is used as ARC since poly-Si is conductive enough [25]. Therefore, screen-printing fire-through metallization is employed as very simple solution. Nonetheless, this approach affects severely the performance of poly-Si, especially when it is very thin. Indeed, the penetration of Ag paste into poly-Si etches part of the poly-Si layer, therefore lowering field-effect passivation. If poly-Si layer is very thin, Ag

paste might completely etch it, therefore introducing high contact recombination, estimated between 200 and 300 fA/cm$^2$ [26].

To improve efficiency and reduce costs, reduction of Ag consumption is sought after c-Si solar cells by finding effective low-temperature and alternative methods to Ag screen printing. According to the International Technology Roadmap for Photovoltaic (ITRPV), c-Si solar cells with copper (Cu) plated contacts will have around 30% of the market share within 2027 [27]. This increase is due to potential higher aspect ratio than Ag screen printed contacts, therefore resulting in higher short-circuit density due to less optical shading [28]. Moreover, also contact and line resistivity can be comparable to screen-printed Ag [29]. Working principle of Cu plating technique requires the use of a conductive seed layer patterned with the designed grid contacts. On top of it, a thick Cu layer can grow to obtain lower series resistance. The drawback of this metallization technology is the poor adhesion of Cu grown onto the seed layer [30][31] and a deep diffusion of Cu into Si, which affects device performances [32][33]. An optimized cleaning procedure and a careful handling process can help to ameliorate the adhesion issue of Cu on the seed layer [31].

Typically, the most used seed layer is Nickel (Ni), deposited by physical vapour deposition (PVD). The copper layer is actually deposited by placing a wafer into a Cu-rich solution (such as $CuSO_4$ $[H_2O]_5$ [34]) and applying a potential between a Cu anode and a cathode. The grid is used as cathode while current flows through an external anode. The resulting current will make Cu aquo-complexes dissociate and therefore Cu ions migrate towards the silicon wafer. Electrical current can be induced by exploiting the photovoltaic effect of a Si wafer by the so-called light induced plating [35]. Likewise, electrical current can be induced either by a chemical solution of reducing agents [36], so-called electro-less plating, or by a wired electrical connection, in that case the technique is called electro-plating. The latter gives a fast and reliable process for Cu-plating contacts [37]. By employing electroplating technique, 21.4% efficiency has been achieved on PERL solar cell with remarkable FF of 81.95% [28] and efficiency > 21% has been shown in SHJ solar cells [38][39]. Despite technology improvements [40][41], Ni-Cu plated contacts suffer from issues as adhesion to silicon wafer [42] or formation of interfacial oxides [43] that might hinder applicability in real solar cells. In this chapter, we present the development of Cu electro-plated contacts with Ag or Ti seed layers. The choice of using Ti seed layer has several advantages; i) Ti can be used in combination with both n- and p-type semiconductors because of lower contact resistance and good work-function matching with both polarities [44], ii) it has excellent adhesion to Si [45] and iii) it can be deposited with several technologies, such as sputtering or evaporation on Si and it is possible to execute plating onto it [46].

In this chapter, we aim to explore the physical limit of this contact formation technology keeping the process as simple as possible. We investigate the plating conditions, current and time to obtain uniform and well-defined contacts. Moreover, we study how passivation quality of the doped layers is influenced by Cu electro-plating process. Finally, we apply this metallization technology in solar cells embedding carrier-selective passivating contacts to identify pros and cons compared to standard printing or evaporation technique.

## 7.2. EXPERIMENTAL DETAILS

For preparing test samples and solar cells, we used 4 inches n-type float zone (FZ) silicon wafers (c-Si) with polished <100> oriented surfaces, a resistivity of 2.5 Ωcm and initial thickness of 280 $\mu$m. C-Si substrates were cleaned in a nitric acid (99% $HNO_3$) bath for 10 min at 20 °C, followed by a dip in 69.5% $HNO_3$ at 110 °C to remove organic residuals and metallic contaminations, respectively. Test samples were chemically textured in a solution containing TMAH, Alkatext surfactant and $H_2O$ to obtain random pyramids on both sides of the wafer and <111> oriented facets. Test samples were differently fabricated depending on anti-reflection coating used as drawn in Figure 7.1 and 7.2. In both approaches, we used 300-nm thick seed layer, either e-beam evaporated Ti or thermally evaporated Ag. The plating deposition was carried out using a Meco Cu-plater consisting of an electro-plating solution made of Cu-rich mixture with a pH of 3 and Autolab 10 A current booster generator. Electroplating is performed after seed layer deposition without any further processing and surface treatments in between. The reason for developing two different fabrication processes is to protect the TCO layer stack from the solution of Cu electro-plating that etches the layer away.

### 7.2.1. DEVELOPMENT OF CU-PLATED CONTACTS ON CONDUCTIVE ANTI-REFLECTION COATING

Attempting to grow Cu on an un-protected TCO is not possible, as TCO would be etched away. Therefore, we devised a flow chart for Cu-plating on TCO, which is full-area protected by the seed layer (see Figure 7.1). As figure 7.1 shows, a TCO layer is sputtered (Figure 7.1 (a)), followed by full-area deposition of the seed layer (Figure 7.1 (b)). In our case, we deposit 75 nm-thick ITO layer via physical vapour deposition sputtering. Then, the contacts are opened by photolithography with the designed grid pattern (Figure 7.1 (c)) by using a 10-µm thick AZ9260 photoresist layer that acts also as mask during the electro-plating process (Figure 7.1 (d)). After electro-plating process, the photoresist is removed by dipping the wafer in acetone and the Ti seed layer (outside the grid pattern) is etched via chemical solution mixed of $H_2O$, $H_2O_2$ and diluted $NH_3$ (Figure 7.1 (e)). The method used here, albeit based on a different seed, is already employed in [47]. Figure 7.1 (f) shows a cross-section SEM of the Cu-plated contacts.

### 7.2.2. DEVELOPMENT OF CU-PLATED CONTACTS ON DIELECTRIC ANTI-REFLECTION COATING

When the anti-reflection coating (ARC) is non-conductive as in case of $SiN_x$, an alternative fabrication process is followed as sketched in Figure 7.2. After 75 nm-thick $SiN_x$ deposition (Figure 7.2 (a)), photolithography is performed to open the front grid pattern in the $SiN_x$ layer (Figure 7.2 (b)). Then, the seed layer is full-area evaporated, filling the openings created (Figure 7.2 (c)) and followed by lift-off in an ultra-sonic bath to remove both metal and photoresist outside the contact region (Figure 7.2 (d)). At this point, the wafer is transferred for Cu electro-plating process. For both approaches, we varied the plating current density ($J_{PL}$) between 144 mA/cm$^2$ and 576 mA/cm$^2$ (total current from 350 mA to 1400 mA) and plating time ranges from 500 to 2000 seconds in order to investigate the adhesion of Cu, its thickness and the uniformity of Cu growth. Both methods

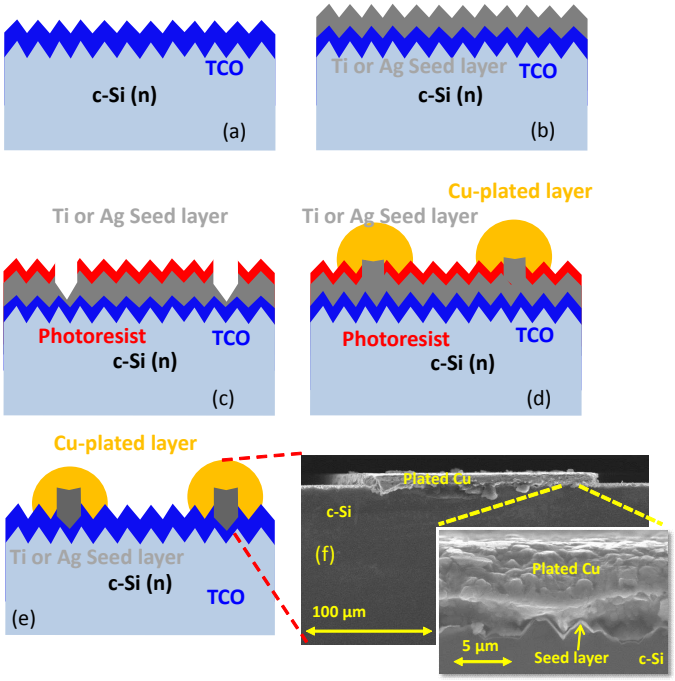


Figure 7.1: Flowchart for Cu-plating test sample with TCO ARC. (a) TCO deposition as ARC; (b) Ti or Ag (Ti-Ag) seed layer deposition on full-area; (c) Photolithography to define contact openings; (d) Cu electro-plating; (e) Photoresist removal and seed layer etching; (f) cross-section of a Cu-plated contact with a detailed inset.



developed in this work are rather versatile and can be employed also in different process conditions such as different TCO (IO:H, IWO) or other dielectric layers as anti-reflection coating ($MgF_2$, $SiO_2$ or $Al_2O_3$). On the other hand, we also note that our case is relative to indium tin oxide. We remark that the TCO need to be stable in the etching mixture ($H_2O/H_2O_2/NH_3$) used otherwise this step has to be likely re-optimized to find the right solutions that is able to etch the seed layer without affecting the layers underneath.

### 7.2.3. SOLAR CELL DEMONSTRATORS EMBEDDING CU-PLATED CONTACTS

To investigate the impact of Cu-plating at device level, we choose three different solar cells architectures schematically shown in Figure 7.3. Out of every solar cell architecture, there will be two different front metallization scheme; the references use Al contacts after lithography, e-beam evaporation and lift-off or screen printing on ITO; the other employs Ti-Cu plated contacts with the method explained in Figures 7.1 and 7.2. The first one is silicon heterojunction (SHJ) solar cells sketched in Figure 7.3 (a). The double-side textured wafer is coated on both sides by 10-nm thick intrinsic a-Si:H and then 20-nm thick n- and p-type nanocrystalline silicon oxide (nc-$SiO_x$) at the front and rear, respectively, similarly to [48]. Then, ITO is deposited on both sides of the wafer. Finally, Ag / Cu stack is grown at the front side following the procedure reported in Figure 7.1. We compare this method to a classical, state-of-the-art screen-printing metallization using

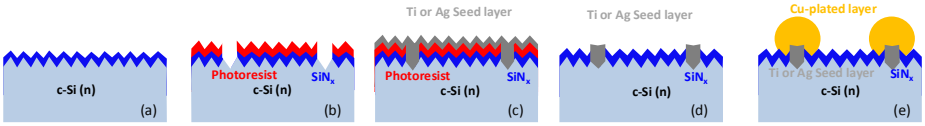


Figure 7.2: Flowchart for Cu-plating test sample with $SiN_X$ ARC (a) $SiN_X$ ARC deposition, (b) Photolithography and etching of $SiN_X$, (c) Ti or Ag seed layer evaporation, (d) lift-off, (e) Cu-plating.

low temperature Ag paste. In both cases, the front grid design is the same. To check if Cu-plating technique and processing introduce any possible damage, we measure carrier lifetime using Sinton WCT-120 tool [49] after PECVD + ITO depositions and finally after Cu-plating. The measurement is performed after Cu-etching from the surface. The second solar cell architecture is the so-called poly-poly solar cell shown in Figure 7.3 (b) [50]. It consists of a front textured wafer passivated by a thin tunnelling $SiO_2$ and 20-nm thick n-type and 250-nm thick p-type doped poly-Si at the front and rear, respectively. Then, $SiN_X$ is used as ARC at the front side and metallization is finished through lithography, $SiN_X$ etching, full-area evaporation of Al and lift-off (reference process). Alternatively, after $SiN_X$ deposition, we employ Ti/Cu-plated contacts at the front with the method explained in Figure 7.2. A third solar cell architecture, shown in Figure 7.3 (c), is a so-called hybrid solar cell that combines front textured silicon passivated by a stack of 4.5 / 6 nm-thick of (i) / (n) type a-Si:H and flat rear passivated by 1.5 nm-thick $SiO_2$ / 250 nm-thick (p) type poly-Si [51]. At the front side, the wafer is coated by ITO. In all the three



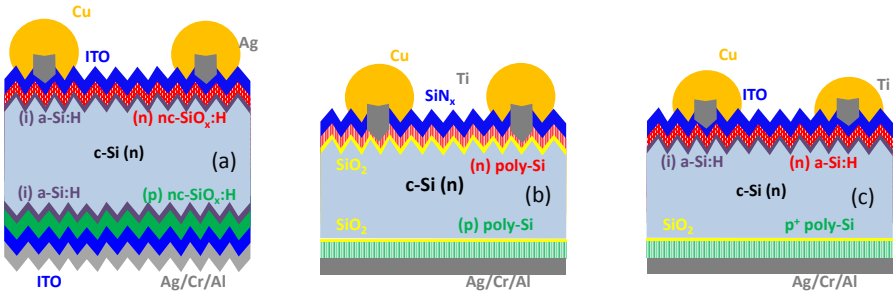


Figure 7.3: (a) Sketch of SHJ solar cell with nc-$SiO_X$:H; (b) poly-poly solar cell; (c) hybrid solar cell. Layers thickness and front contact inter-distance are not in scale.

architectures, a stack of Ag/Cr/Al is evaporated as back contact and to enhance internal reflectance. In the SHJ solar cell, also ITO is full-area deposited to further boost the internal reflectance [52]. Metal grid morphology was characterized by Keyence Confocal microscope, scanning electron microscopy (SEM) and 1D Dektak profile meter. Confocal microscope employs laser and optical light in a spot of 1.5 $mm^2$ and it is able to reconstruct the surface topology with a resolution in the order of 1 $\mu$m. By using 3D confocal microscopy, metal height and aspect ratio (defined as the ratio between the height and width of a metal finger) are evaluated. 1D Dektak profile meter uses a mechanical tip to

investigate the step height difference between two different areas of a wafer. SEM XL50 Philips is used to investigate the presence of metal spots outside the designated area. Solar cells external parameters, such as open circuit voltage ($V_{OC}$), fill-factor (FF), short-circuit current density ($J_{SC}$) and efficiency ($\eta$) were measured with a Wacom WXS-156S solar simulator. Finally, we used also a Sinton Suns$V_{OC}$ setup to measure the pseudo-FF (pFF), which neglects the contribution of the series resistance.

## 7.3. RESULTS AND DISCUSSION

### 7.3.1. DEVELOPMENT OF AG – CU PLATED CONTACTS

Although Ag-seeded Cu-plated contacts were developed for both flow charts reported in Figures 7.1 and 7.2, results reported in this section mainly attain to the flow chart based on ITO ARC. Figures 7.4 (a) show a picture of Cu-plated contacts on Ag seed layer and ITO anti-reflection coating on a full wafer that has 4 cells with different grid designs. Step height of the busbar and fingers were taken by profile measurement on the spot indicated by the red square for different plating current densities ($J_{PL} = 144, 288 or 576 mA/cm^2$) and fixed time of 1500 s (see Figures 7.4 (b) and (c)). For the lowest $J_{PL}$, the average height of the contact was around 20 $\mu$m with a quite uniform distribution over the entire wafer. The peak-to-peak noise of 2 µm overlapping onto the signal is due to texturing pyramids' size of the Si substrate. By increasing $J_{PL}$ to 288 mA/cm$^2$, the contact became thicker at the edge of the busbar and thinner inside it. Same trend of lateral growth was observed for $J_{PL} = 576 mA/cm^2$. The difference between the edge and the centre of the busbar was as high as 20 $\mu$m (max 70 $\mu$m, min 50 $\mu$m) with a significant increase of roughness. We ascribe this behaviour to the high current that is not uniformly distributed in all plated parts because of higher current drop due to resistive effect of the seed layer in the thin busbar and fingers. On the contrary, using the lowest current value resulted in a uniform current distribution across the plated area.



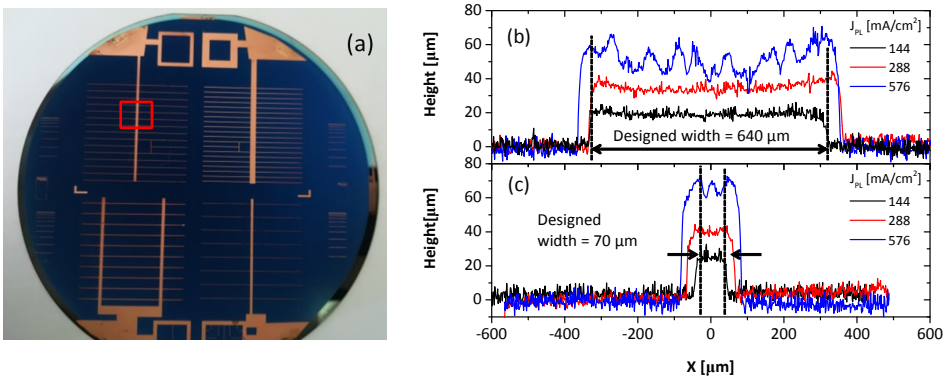


Figure 7.4: (a) ITO-covered wafer with Ag-seeded Cu-plated front contacts. The red square indicates the area where profile measurements have been taken. Step height profiling of busbar and one of the fingers for a variable $J_{PL}$ are reported in (b) and (c), respectively. Plating time was fixed at 1500 s. Vertical dashed lines in (b) and (c) indicate designed width as set in the photolithographic step.

Overgrowth of copper starts to appear only when higher current densities are employed. Figure 7.5 shows the aspect ratio of grown fingers against plating current. An increase from 0.2 to 0.35 was noted with a similar variance. The higher aspect ratio of the fingers with respect to that of the busbars is due to narrower finger design. It is important to note that the photoresist layer is much thinner than plated layers. Figures 7.6

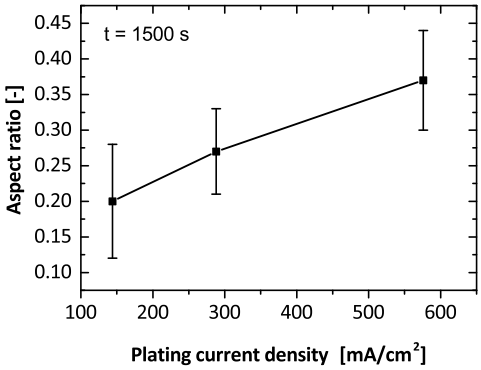


Figure 7.5: Aspect ratio of one the fingers as function of plating current density. Plating time is fixed at 1500s.

show 3D confocal microscope images taken on the same spot indicated in Figure 7.4 (a) by the red square. We clearly note that low plating current ($J_{PL} = 144 mA/cm J_P{}^2$) gave a well-defined, uniform and 20-µm thick contact. By increasing $J_{PL}$ to 288 mA/cm$^2$ (see Figure 7.6 (b)), as previously mentioned, we note an increase in height as well as in width in both busbar and finger. As the plating current was not uniformly distributed for $J_{PL} = 576 mA/cm^2$ (see Figure 7.6 (c)), the width of the plated contact is at least 20 µm greater than the previous two cases. A very similar trend is noted on one of the fingers shown in Figure 7.4 (c). For application in a complete solar cell, we chose $J_{PL} = 144 mA/cm^2$, since it realized the designed width avoiding additional shading losses. Once plating current

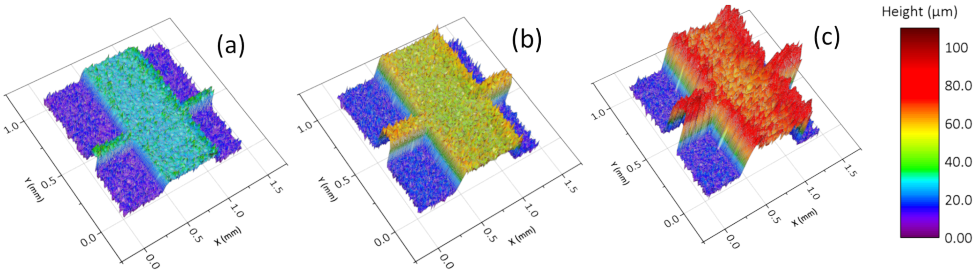


Figure 7.6: 3D confocal microscopy images taken for samples in Figure 4 and Figure 5, processed at fixed plating time (1500 seconds) and variable $J_{PL}$: (a) 144 mA/cm$^2$, (b) 288 mA/cm$^2$ and (c) 576 mA/cm$^2$.

was analyzed, we varied the plating time from 500 to 2000 seconds, keeping current fixed at the optimum value previously found, $J_{PL} = 144 mA/cm^2$ ,(see Figures 7.7). Perform-

ing plating for 500 seconds (see Figure 7.7 (a)), the resulting Cu layer was very thin (5-µm thick in average). For longer plating times, 1000 and 1500 seconds (see Figures 7.7 (b) and Figure 7.6 (a)), Cu layer was significantly thicker than the pyramids' size with an average value of 30 and 40 $\mu$m, respectively. Finally, for 2000 seconds (see Figure 7.7 (c)), Cu contact is thicker (60 µm). For the last sample, we detected poor adhesion of the Cu layer onto the substrate that might be caused by mechanical stress induced into the growing layer. As in the analysis for plating current, also in this case we evaluated aspect ratio of

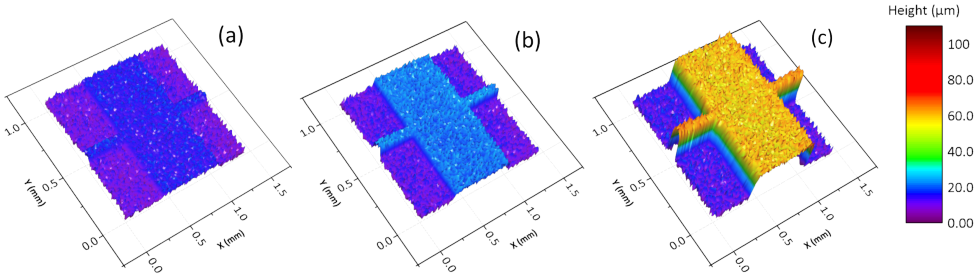


Figure 7.7: 3D confocal microscopy images of Ag-seeded Cu-plated front contacts on ITO with fixed plating current density ($J_{\mathrm{PL}} = 144 mA/cm^2$) and variable plating time: (a) $t = 500s$; (b) $t = 1000s$; (c) $t = 2000s$. The case of $t = 1500$ s is reported in Figure 7.6 (a).

fingers. In Figure 7.8 we note how aspect ratio increased for increasing plating time from 0.1 to 0.5 for a finger. Therefore, we choose the best plating recipe with a current density of 144 mA/cm$^2$ and time of 1500 seconds for further tests at device level. To investigate adhesion, we performed the tape test ASTM D4541 [53] that consists in placing a tape on the wafer and then pulling it. If metal is attached to the tape, the test is considered failed and the adhesion is very poor; on the other hand, if the test is passed, the adhesion is considered good. When employing a plating current density of 144 mA/cm$^2$ for 2000

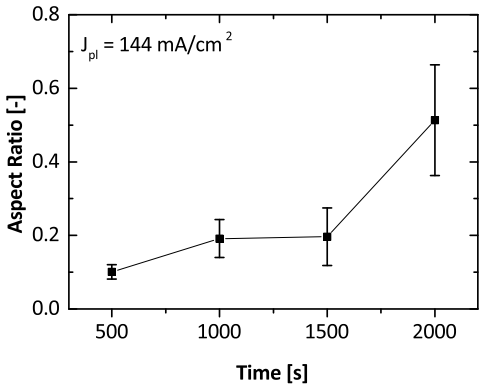


Figure 7.8: Aspect ratio of one of the fingers against plating time for a fixed plating current density ($J_{\mathrm{PL}} = 144 mA/cm^2$).

seconds, the fingers tended to detach off the substrate as soon as the wafer drying was performed (see left-hand side of Figure 7.9 (a)). Similar behavior was observed for the case of plating current density of 576 mA/cm$^2$ for 1500 seconds, as picture in Figure 7.9 (b) demonstrates. The detachment is due to an important mechanical stress induced in the copper layer due to the thick copper deposited. In all the other cases (lower current density or shorter time), the tape test was passed.

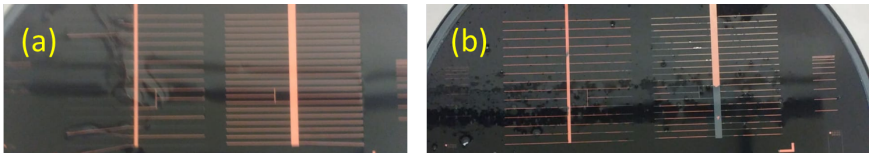


Figure 7.9: Pictures of Cu-plated wafers with very poor adhesion (a) $J_{PL} = 144 mA/cm^2$ t = 2000 s; (b) $J_{PL} = 576 mA/cm^2$, t=1500 s

We repeated a similar optimization process following the steps highlighted in Figure 7.2 for samples with $SiN_x$ as ARC instead of ITO layer and using Ag as seed layer. The results were similar as found for samples with ITO. Therefore,i aseed layer, with our contact openings, corresponds to a plating current density of 144 mA/cm$^2$ and a plating time of 1500 seconds. These plating conditions give the best aspect ratio together with optimal adhesion for both flow-charts in Figure 7.1 and Figure 7.2.

### 7.3.2. DEVELOPMENT OF TI-SEEDED CU-PLATED CONTACTS

In order to completely avoid Ag usage at the front side, we replaced Ag with a Ti seed. Similarly to the previous section, although Ti-seeded Cu-plated contacts were developed for both flow charts reported in Figure 7.1 and Figure 7.2, results reported in this section mainly attain to the flow chart based on $SiN_x$ ARC. Using Ti seed layer, we needed to re-optimize the recipe, in particular to find a new optimum plating current density and time, taking into consideration that titanium is less conductive than Ag and this difference will lead to a lower current distribution. We first performed two different tests with $J_{PL}$ of 576 and 1152 mA/cm$^2$ to identify the range in which the Cu migration from the electrolyte to the Si wafer is sufficient to induce deposition. The experiments were both performed with a fixed plating time of 1500 seconds. Figures 7.10 show optical microscopy images of Ti-seeded Cu-plated contacts with the abovementioned currents. For $J_{PL} = 576 mA/cm^2$, the finger was well defined but some Cu growth was observed outside the seed pattern (see Figure 7.10 (a) and Figure 7.11(a)). For $J_{PL} = 1152 mA/cm^2$ (corresponding to a total current of 2800 mA), Cu appeared bulky and grew outside the designed region on the ARC (see Figure 7.10 (b)). This phenomenon is known as background plating [54]. In view of these experiments, we decided to keep the current density at 576 mA/cm$^2$ to obtain a relatively thick layer only in the contact region and limited overgrowth and/or background plating. The choice of plating current density of 576 mA/cm$^2$ is a result from a series of tested current densities that give a uniform and well-defined Cu-plated layer. Figure 7.11 (a) shows overgrowth observed indeed also for $J_{PL} = 576 mA/cm^2$ on the entire wafer surface. Closer images taken via SEM in Figure 7.11 (b) and (c) illustrate that, at device level, the short-circuit current might be clearly

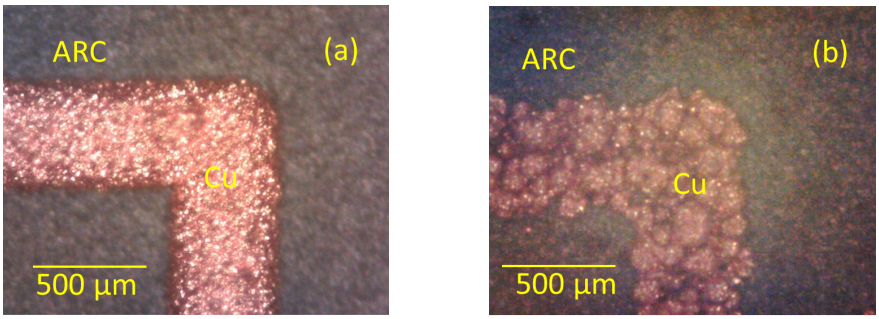


Figure 7.10: Optical microscopy images of Ti-seeded Cu-plated with plating current density of (a) 576 mA/cm$^2$ and (b) 1152 mA mA/cm$^2$ for a fixed plating time of 1500 seconds.

lowered due to optical shading and, in some cases, it might also lead to open-circuit voltage drop caused by penetration of Cu atoms into silicon, constituting active recombination centers [32]. Similar results have been found also in Ref. [54], in which seed layer consisted of Ni– a very typical seed layer used in literature [55] – is employed. It is suggested how a full-wafer cleaning and low-induced mechanical stress by wafer handling can decrease the background plating. In our case, even though wafer cleaning was performed with $HNO_3$ and the wafers were carefully handled manually with the aid of vacuum tweezers, we observed this phenomenon simply when too high $J_{PL}$ was employed. In our case $SiN_x$ is deposited by PECVD, therefore it is quite porous and it might contribute to the formation of background plating [56].



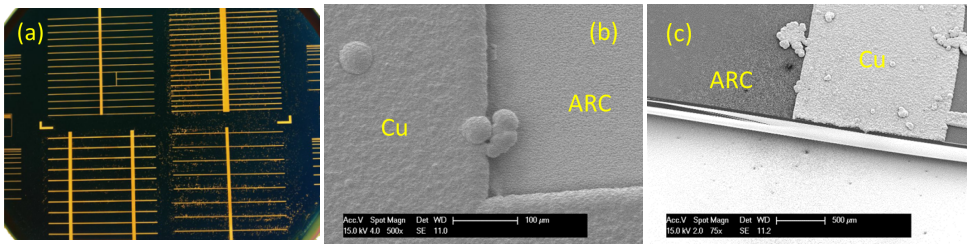


Figure 7.11: (a) Picture of Ti-seeded Cu-plated wafer with $SiN_x$ ARC; (b) and (c) scanning electron microscopy of the wafer to highlight background plating outside the designed region

### 7.3.3. OVERCOMING BACKGROUND PLATING

It should be noted that background plating was observed in both Ag-seeded and Ti-seeded Cu-plated contacts on $SiN_x$ for high $J_{PL}$ values. This issue evidently affected mostly the route with Ti seeding, since in case of Ag seeding lower $J_{PL}$ values allowed to obtain reasonably thick and mechanically stable Cu-plated contacts. For completeness, background plating was not observed at all when plating on ITO, since the ITO itself was full-area protected by either Ag or Ti/photoresist stack against etching of the Cu-rich so-

lution (see Figure 7.1 (d)). To overcome the problem of background plating, we tested two different solutions. The first one was to use a different current distribution. Instead of a direct current (DC) induction, we used an alternate current (AC), also known as pulse plating current. This solution has already demonstrated to be capable of reducing the overgrowth of plating outside the contact region on Ni seed layer [41][57][58]. The physical process behind is that, during the positive current, Cu ions migrate from the electrolyte to Si wafer while, during the negative cycle, the opposite migration occurs. As positive plating current density is much higher than negative current density, the small spots accumulated during the positive current cycle are removed while the whole stack does not detach. Aside positive and negative current densities, also the duty cycle is important. It is defined as the time of positive current over the total period of a cycle. In our case, we used a duty cycle of 83% with forward current density of 246 mA/cm$^2$ (corresponding to a total current of 600 mA) for 300 seconds and a reverse current density of 41 mA/cm$^2$ (corresponding to a total current of 100 mA) for 40 seconds. During the switch, there was a waiting time of 10 seconds to stabilize the system. 18 cycles were repeated for a total of 84 minutes. It is noteworthy to say that typical pulse-plating technique has a range in the order of milliseconds [41], while our plating / de-plating sequence lasts minutes. A lower positive current than standard DC is used to prevent excessive inductive effect during the transient in the switching time, adding therefore an additional component of background plating. Figures 7.12 shows SEM images of the contact obtained with pulsed current. The wafer surface looked cleaner than in case of Figure 7.11 with very rare spots outside the contact region. Moreover, we investigated the effect of pulse



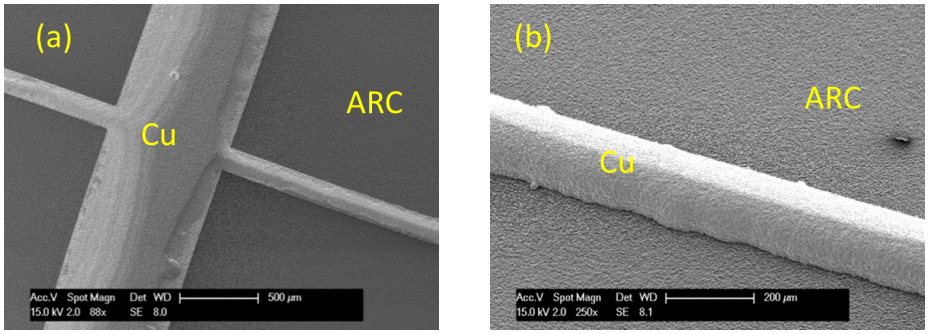


Figure 7.12: Scanning Electron Microscopy images of Ti-seeded Cu-pulse-plated contact: (a) busbar and fingers, (b) zoom-in on finger.

plating on the shape of the contacts. Figure 7.13 shows the height of a finger respect to the distance obtained with DC and pulsed plating method. Since we employed lower forward current density, the total thickness of the finger was much smaller than the DC case, but we noted also a slight difference in shape that might be ascribed to the lower total charge accumulated on the surface of the wafer. In the DC case, the height was 32.5 µm, while in the pulsed case the average height reduced to 20 µm. In this case, the aspect ratio for DC case was 0.21, while for the pulsed case was 0.13, since the width of the finger was 150 µm. With a further engineering of the pulse-plating process, we can obtain a higher aspect ratio than DC plating case with no overgrowth. Another possible solution

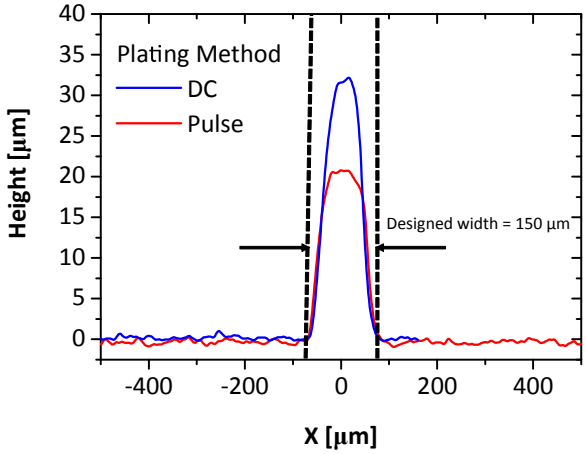


Figure 7.13: 1D profile measurements of a finger of a pulsed Ti-seeded Cu-plated wafer with $SiN_x$ ARC.

to cope with background plating is to use a thicker dielectric layer to offer a more resistive path to the plating current, therefore the overgrowth and background plating can be minimized. To do so, we need to carefully choose the materials composing the stack and their thickness in order to avoid reflection losses. We designed a double ARC stack composed of 75-nm thick $SiN_x$ followed by 110-nm thick $SiO_2$ that offers a lower reflectivity over the spectrum as shown in Ref. [59]. The results are reported in Figure 7.14 (a) that shows the picture of a wafer, with a relatively clean Cu-plated contacts, while in (b) a SEM picture is shown. When the double anti-reflection coating layer is employed, the overgrowth is much lower than the DC case. Similar results have been obtained when Ni seed layer is employed, with even improved long term stability of the contact [60]. It is important to remark that $SiN_x$ and $SiO_2$ are both deposited by PECVD which can result in porous layers. To avoid background plating formation we plan to use, in the eventual expansion of this work, other deposition technologies, such as low pressure chemical vapour deposition (LPCVD), ensuring denser dielectric layers. This would be reflected in a process flow change since LPCVD materials are extremely resilient against wet etching.

### 7.3.4. SOLAR CELL DEMONSTRATORS

To investigate the effect of Cu-plating process on passivation quality, we fabricated a silicon heterojunction (SHJ) solar cell as described in the experimental methods section. Before metal deposition, lifetime measurement was taken on the so-called solar cell precursor. Figure 7.15 shows effective lifetime measurement against injection level taken on solar cell precursor before metallization and after Cu-plating processing as explained in Figure 7.1. The measurement after Cu-plating process, red dots in Figure 7.15, is taken after stripping away both Cu and Ti seeding layers. Effective lifetime at $\Delta n = 10^{15}$ $cm^{-3}$ was around 2 ms in both cases. It differs only of 100 µs after Cu-plating processing. This difference might be ascribed to the etching process and to the fact that the wafer has most likely a slightly higher number of surface contaminant rather than be-

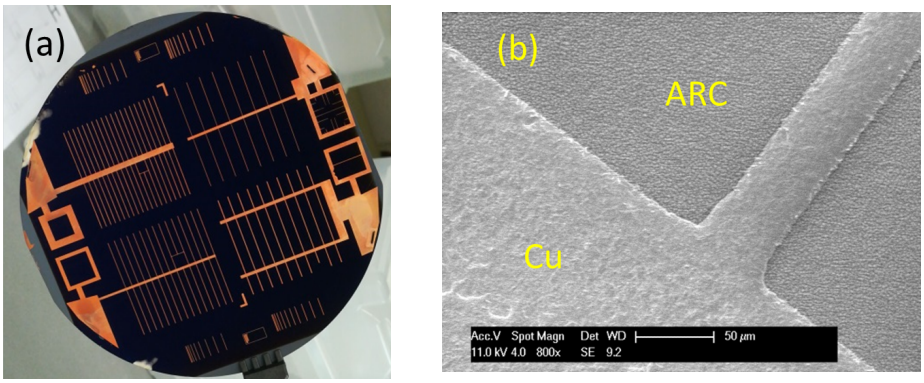


Figure 7.14: a) Picture of a Ti-seeded Cu-plated wafer with double anti-reflection coating; (b) scanning electron microscopy image of an intersection between the busbar and a finger.

fore the Cu-plating process. Therefore, we can conclude that DC Cu-plating processing

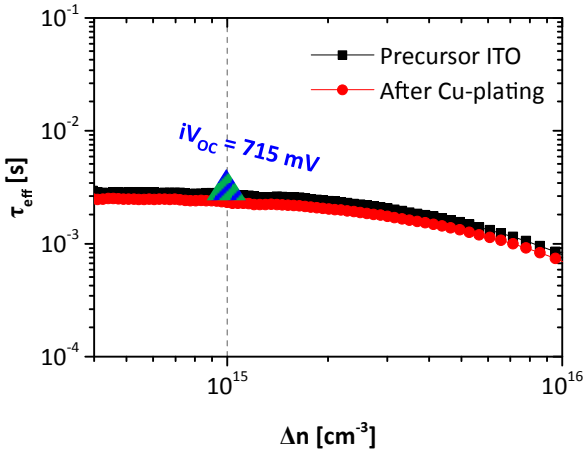


Figure 7.15: Effective lifetime against injection level in the case of ITO precursor in SHJ solar cell (Black line) and after Cu-plating (red line). The measurement is taken after etching copper and silver seed layer.

does not affect significantly passivation quality of SHJ cells, with stable implied open circuit voltage ($iV_{OC}$) of 715 mV. Table 7.1 shows the external parameters of solar cells highlighted in Figure 7.3. In the case of SHJ solar cell, the reference device with screen printed front contact realized a $V_{OC}$ of 710 mV, a current of 37.5 mA/cm$^2$ and a FF of 73%. When Ag / DC Cu-plated contacts were employed, we obtained 5 mV lower $V_{OC}$ than in screen-printed case, a current of 37.1 mA/cm$^2$, 0.4 mA/cm$^2$ lower than screen-printed case and a FF of 71%, 2% absolute lower than the reference cell. The aperture-area efficiencies are 20.4% and 19.4% for the reference and Cu-plated cells, respectively. In the case of poly-poly solar cell, sketched in Figure 7.3 (b), we used as a reference Al evaporated front contacts. For the reference cell, we obtained a $V_{OC}$ of 689 mV, a $J_{SC}$ of 36.5

mA/cm$^2$ and a FF of 73%. When switching to Ti-seeded DC Cu-plated front contacts, $V_{OC}$ slightly degraded to 682 mV, 7 mV lower than the reference. $J_{SC}$ was 36.3 mA/cm$^2$, 0.2 mA/cm$^2$ smaller than reference case while FF was 75.2%, 2.2% absolute greater than the evaporated case. Aperture-area efficiencies are 19.3% and 19.6% for reference and plated case, respectively. Regarding the last case considered, a hybrid solar cell as Figure 7.3 (c) sketches, a slightly larger front design was used (9 cm$^2$) with respect the previous solar cells. In the reference case endowed with Al evaporated front contacts, $V_{OC}$ is 704 mV, current is 39.9 mA/cm$^2$ and FF is 73.8%. In the case of Ti-seeded DC Cu plating, $V_{OC}$ drops to 694 mV, 10 mV lower than the reference case, $J_{SC}$ is 37.1 mA/cm$^2$, 2.8 mA/cm$^2$ lower than evaporation case, but the FF improves to 74.1%, 0.3% absolute higher than the reference. All these solar cells demonstrate that $V_{OC}$ lowers in plated cases with respect to the reference cells. This is ascribed to residual background plating occurring in Ti-seeded or Ag-seeded Cu-plating for SHJ solar cell (-5 mV), poly-poly cell (-7 mV) and hybrid cell (-10 mV). Regarding $J_{SC}$, the plated solar cells exhibited slightly lower current than standard, only in the case of hybrid solar cell had 2.8 mA/cm$^2$ lower current. We speculate that this was due to lower quality texturing and anti-reflection coating thickness variation. Regarding FF, we do not observe any impact of contact resistivity on series resistance since it is 0.1 $\Omega$/cm$_2$ in both cases. The observed higher FF with for Cu-plated cells (poly-poly and hybrid devices) might be ascribed to the higher aspect ratio of the contact compared to evaporated aluminium. Moreover, work function of Ti has a lower mismatch with n-type poly-Si rather than Al [62]. In comparison with the screen printed SHJ solar cell, the plated cell counterpart still exhibited a 2% absolute lower FF. This was due to lower line conductivity of plated Cu than screen printed Ag [63]. Finally, we observed higher pFF for the Cu-plated solar cells which indicates that series resistance is a limit for FF of our devices.

Table 7.1: External parameters of solar cells reported in Figure 7.3

| Solar cell | Area [cm$^2$] | Nominal Metal Fraction [%] | Front metallization | $V_{OC}$ [mV] | $J_{SC}$ [mA/cm$^2$] | FF [%] | $\eta$ [%] | $\eta_{aperture}$ [%] | pFF [%] |
|---|---|---|---|---|---|---|---|---|---|
| SHJ[51] | 7.84 | 5.0 | Screen printing | 710 | 37.5 | 73.0 | 19.4 | 20.4 | 82.5 |
| SHJ | 7.84 | 5.0 | Ag – DC Cu plating | 705 | 37.1 | 71.0 | 18.5 | 19.4 | 83.0 |
| Poly-poly[43] | 7.84 | 5.0 | Al evaporation | 689 | 36.5 | 73.0 | 18.3 | 19.3 | 82.3 |
| Poly-poly | 7.84 | 5.0 | Ti- DC Cu plating | 682 | 36.3 | 75.2 | 18.7 | 19.6 | 84.1 |
| Hybrid[52] | 9.00 | 2.64 | Al evaporation | 704 | 39.9 | 73.8 | 20.4 | 21.0 | 81.6 |
| Hybrid | 9.00 | 2.64 | Ti- DC Cu plating | 694 | 37.1 | 74.1 | 18.6 | 19.1 | 83.0 |

An important challenge of this technology is the long-term reliability. Since solar modules are expected to work for 25 years, they have to comply with IEC 61215 [64]. This provides a 1000 h damp heat exposure at 85 °C with 85% humidity. Two main issues are related to long-term reliability of Cu-plated contacts; i) contact adhesion and ii) metal interdiffusion in case of metal stacks as Ni-Cu or Ti-Cu as this chapter shows [65]. Some studies have been shown tests on long-term reliability in Ni-Cu plated contacts [66]. In our case, since we have Ti seed layer, long-term reliability is one of the main studies that must be carried out for an upscaling of this technology. Although no evidence is brought in this chapter, the author believes that Ti seed layer might be considered an important alternative to Ni since it has good resistance against Cu diffusion.

## 7.4. CONCLUSION

In this work, we have shown the optimization of Cu-plated front contacts with Ti or Ag seed layer applied in solar cells endowed with carrier-selective passivating contacts. The advantages of using Ti are multiple: i) good contact properties to both n- and p-type (poly)silicon, ii) excellent adhesion to Si and iii) different deposition technologies available. We have developed two different fabrication methods depending on the conductivity of the anti-reflection coating. These two methods are equivalent and fully compatible with c-Si solar cell fabrication. First, we have developed Ag-seeded Cu-plated contact. We optimized the plating parameters (i.e. plating current density and time) to obtain a reasonably thick Cu layer with high uniformity and adhesion at the same time. We found that, for our mask design, the optimal combination of plating current density and time was 144 mA/cm$^2$ and 1500 seconds. For this metal stack, the aspect ratio appeared to be 0.2 for a 70-µm wide finger. Similarly, we demonstrated Cu-plating with a Ti seed layer, therefore avoiding any Ag consumption at the front of our solar cells. In this case, since conductivity of Ti is lower than Ag, we used higher current density (576 mA/cm$^2$) than in Ag case to make the plating process effective. Nonetheless, this very high current density level induced background plating outside the designed region. We then implemented two different solutions to eventually overcome this issue; i) plating/de-plating sequence instead of direct current plating and ii) double dielectric anti-reflection coating. The first solution used relatively high direct current density (246 mA/cm$^2$) for to 300 seconds and low (- 41 mA/cm$^2$) reverse current density to grow Cu layer above the seed layer and remove any Cu spots on the ARC. We found through SEM that wafers treated with pulsed plating were much cleaner compared to the DC case. The aspect ratios for DC and pulsed cases were evaluated in 0.21 and 0.13, respectively for a 150 µm-wide finger. The other method to avoid background plating was to use a double dielectric anti-reflection coating made by $SiN_x$ and $SiO_2$. By employing this method, we observed improved wafer cleanliness and less background plating. At device level, we have seen how Cu-plating process does not affect significantly passivation quality in solar cell precursors. Finally, we fabricated different instances of solar cells with Cu-plated front contacts: SHJ solar cell with nc-$SiO_x$:H as doped layers, poly-poly solar cell and hybrid solar cell. It turns out that $V_{OC}$ is, in all three cases, at least 5 mV lower when Cu-plating is employed instead of evaporated Al or screen-printed Ag. Short-circuit current is similar except the case of hybrid solar cell. Cu-plated solar cells improve FF if compared to evaporated Al. With respect to screen printed Ag, FF is still lower. This is due to difference in conductivity of the metals. In conclusion, we investigated the physical limit of copper plating on both Ti and Ag seed layers while keeping the process as simple as possible and applied this metallization technology to three different c-Si solar cell FBC architectures.



## 7.5. REFERENCES

[1] C. Battaglia, A. Cuevas and S. D. Wolf, "High-efficiency crystalline silicon solar cells: status and perspectives," Energy Environ. Sci., vol. 9, pp. 1552-1576, 2016.

[2] Rene Hoeniga, Michael Duerrschnabel, Willem van Mierlo, Zainul Aabdin, Joerg Bernhard, Johannes Biskupek, Oliver Eibl, Ute Kaiser, Juergen Wilde, Florian Clement, Daniel Biro, The Nature of Screen Printed Front Side Silver Contacts - Results of the

project MikroSol, Energy Procedia 43 ( 2013 ) 27 – 36, doi: 10.1016/j.egypro.2013.11.085.

[3] Hannebauer, H and Falcon, T and Hesse, Rene and Dullweber, T and Brendel, R. (2011). 18.9%-efficient screen-printed solar cells applying a print-on-print process. Proceedings of the 26th European Photovoltaic Solar Energy Conference. 1607-1610.

[4] S. Riegel, F. Mutter, T. Lauermann, B. Terheiden, G. Hahn, Review on screen printed metallization on p-type silicon, Energy Procedia 21 (2012) 14 – 23, doi: 10.1016/j.egypro.2012.05.003.

[5] Martin A. Green, The Passivated Emitter and Rear Cell (PERC): From conception to mass production,Solar Energy Materials and Solar Cells, Volume 143, 2015, Pages 190-197, ISSN 0927-0248, https://doi.org/10.1016/j.solmat.2015.06.055.

[6] Peter Wurfel, Physics of Solar Cells: From Principles to New Concepts.

[7] M. Taguchi, A. Yano, S. Tohoda, K. Matsuyama, Y. Nakamura, T. Nishiwaki, K. Fujita, and E. Maruyama, “24.7% Record Efficiency HIT Solar Cell on Thin Silicon Wafer”, IEEE JPV, 4, 1 (2014)

[8] Daisuke Adachi, José Luis Hernández, and Kenji Yamamoto, Impact of carrier recombination on fill factor for large area heterojunction crystalline silicon solar cell with 25.1% efficiency, Applied Physics Letters 2015 107:23, https://doi.org/10.1063/1.4937224.

[9] K. Yoshikawa, H. Kawasaki, W. Yoshida, T. Irie, K. Konishi, K. Nakano, T. Uto, D. Adachi, M. Kanematsu, H. Uzu and K. Yamamoto, “Silicon heterojunction solar cell with interdigitated back contacts for a photoconversion efficiency over 26%,” Nature Energy, vol. 2, 2017.

[10] Stefaan De Wolf and Michio Kondo, Nature of doped a-Si:H/c-Sia-Si:H/c-Si interface recombination, Journal of Applied Physics 105, 103707 (2009); https://doi.org/10.1063/1.3129578

[11] S. D. Wolf, A. Descoeudres, Z. C. Holman and C. Ballif, “High-efficiency Silicon Heterojunction Solar Cells: A Review,” Green, vol. 2, no. 1, pp. 7-24, 2012.

[12] Faes, Antonin and Despeisse, Matthieu and Ballif, Christophe and Li, Heng-Yu and Geissbühler, Jonas and Ballif, Christophe and Lachowicz, Agata and Bettinelli, Armand and Ribeyron, Pierre-Jean and Munoz, Delfina and Lerat, Jean-François. (2018). Metallization and interconnection for high-efficiency bifacial silicon heterojunction solar cells and modules. Photovoltaics Bulletin. 41.

[13] Anamaria Moldovan, Frank Feldmann, Martin Zimmer, Jochen Rentsch, Jan Benick, Martin Hermle, “Tunnel oxide passivated carrier-selective contacts based on ultra-thin SiO2 layers” Solar Energy Materials and Solar Cells, Volume 142, November 2015, Pages 123-127.

[14] G. Yang, A. Ingenito, N. v. Hameren, O. Isabella and M. Zeman, "Design and application of ion-implanted polySi passivating contacts for interdigitated back contact c-Si solar cells," Applied Physics Letters, p. 108, 2016.

[15] Feldmann, F., Müller, R., Reichel, C. and Hermle, M. (2014), Ion implantation into amorphous Si layers to form carrier-selective contacts for Si solar cells. Phys. Status Solidi RRL, 08: 767–770. doi:10.1002/pssr.201409312

[16] F. Feldmann, M. Simon, M. Bivour, C. Reichel, M. Hermle and S.W. Glunz, Carrier-selective contacts for Si solar cells, Apply. Phys. Lett. 104, 181105 (2014); https://doi.org/10.1063/1.4875904.

[17] Bill Nemeth, Steven P. Harvey, Jian V. Li, David L. Young, Ajay Upadhyaya, Vincenzo LaSalvia, Benjamin G. Lee, Matthew R. Page, Paul Stradins, Effect of the SiO2 interlayer properties with solid-source hydrogenation on passivated contact performance and surface passivation, Energy Procedia, Volume 124, 2017, Pages 295-301, https://doi.org/10.1016/j.egypro.2017.09.302.

[18] J. Melskens, B. van de Loo, B. Macco, M. Vos, J. Palmans, S. Smit and W. Kessels, “Concepts and prospects of passivating contacts for crystalline silicon solar cells,” in IEEE 42nd Photovoltaic Specialist Conference„ New Orleans, 2015.

[19] C. Reichel, F. Feldmann, R. Müller, R. C. Reedy, B. G. Lee, D. L. Young, P. Stradins, M. Hermle and S. W. Glunz, "Tunnel oxide passivated contacts formed by ion implantation for applications in silicon solar cells," Journal of Applied Physics, p. 118, 2015.

[20] Frank Feldmann, Gizem Nogay, Philipp Löper, David L. Young, Benjamin G. Lee, Paul Stradins, Martin Hermle, Stefan W. Glunz, Charge carrier transport mechanisms of passivating contacts studied by temperature-dependent J-V measurements, Solar Energy Materials and Solar Cells, Volume 178, 2018, Pages 15-19, https://doi.org/10.1016/j.solmat.2018.01.008.

[21] R. Peibst, U. Römer, Y. Larionova, M. Rienäcker, A. Merkle, N. Folchert, S. Reiter, M. Turcu, B. Min, J. Krügener, D. Tetzlaff, E. Bugiel, T. Wietler, R. Brendel, Working principle of carrier selective poly-Si/c-Si junctions: Is tunnelling the whole story?, Solar Energy Materials and Solar Cells, Volume 158, Part 1,2016,Pages 60-67,

[22] Richter A, Benick J, Müller R, et al. Tunnel oxide passivating electron contacts as full-area rear emitter of high-efficiency p-type silicon solar cells. Prog Photovolt Res Appl. 2017;1–8. https://doi.org/10.1002/pip.2960

[23] Haase, Felix and Hollemann, Christina and Schäfer, Sören and Merkle, Agnes and Rienäcker (geb. Häberle, Michael and Krügener, Jan and Brendel, Rolf and Peibst, Robby. (2018). Laser contact openings for local poly-Si-metal contacts enabling 26.1%-efficient POLO-IBC solar cells. Solar Energy Materials and Solar Cells. 186. 10.1016/j.solmat.2018.06.020.

[24] F. Feldmann, M. Simon, M. Bivour, C. Reichel, M. Hermle and S. W. Glunz., "Efficient carrier selective p- and n- contacts for Si solar cells," Solar Energy Materials and Solar Cells, vol. 131, pp. 100-104, 2014.

[25] Stefan L. Luxembourg, Dong Zhang, Yu Wu, Mehrdad Najafi, Valerio Zardetto, Wiljan Verhees, Antonius R. Burgers, Sjoerd Veenstra, L.J. Geerligs, Crystalline silicon solar cell with front and rear polysilicon passivated contacts as bottom cell for hybrid tandems, Energy Procedia, Volume 124, 2017, Pages 621-627, https://doi.org/10.1016/j.egypro.2017.09.091.

[26] B. L. Geerligs, M. Stodolny, Y. Wu, A. Gutjahr, G. Janssen, I. Romijn, J. Anker, E. Bende, H. Ciftpinar, M. Lenes and J.-M. Luchies, “LPCVD polysilicon passivating contacts,” in Workshop on Crystalline Silicon Solar Cells and Modules: Materials and Processes, Vail, Co., USA, 2016.

[27] International Technology Roadmap for Photovoltaic (ITRPV), 2017 results, updated to March 2018.

[28] Kim D. S.; Lee E. J.; Kim J.; Lee S. H., Low-cost Contact formation of High-Efficiency Crystalline Silicon Solar Cells by Plating, Journal of the Korean society for New and Renewable Energy, Volume 1, Issue 1, 2005, pp.37-43.

[29] S.P. Murarka, S.W. Hymes, Copper metallization for ULSI and beyond, Crit. Rev. Solid State Mater. Sci. 20 (2) (1995) 87–124.

[30] Jinmo Kang, JaeSung You, ChoonSik Kang, James Jungho Pak, Donghwan Kim, Investigation of Cu metallization for Si solar cells, Solar Energy Materials and Solar Cells, Volume 74, Issues 1–4, 2002, Pages 91-96, https://doi.org/10.1016/S0927-0248(02)00052-1.

[31] Chao-Chi jain, Shiuan-Shen Wang, Tung-Han Chuang and Sang-Ray Yang (2009), Low temperature direct electroless nickel plating on silicon wafer, Journal of the Chinese Institute of Engineers, 32:1, 137-140, DOI: 10.1080/02533839.2009.9671490.

[32] Guy Beaucarne, Gunnar Schubert, Jaap Hoornstra, Jšrg Horzel, Stefan W. Glunz, Summary of the Third Workshop on Metallization for Crystalline Silicon Solar Cells, Energy Procedia, Volume 21, 2012, Pages 2-13, https://doi.org/10.1016/j.egypro.2012.05.002.

[33] Achim Kraft, Christian Wolf, Jonas Bartsch, Markus Glatthaar, Characterization of Copper Diffusion in Silicon Solar Cells, 5th Workshop on Metallization for Crystalline Silicon Solar Cells, Energy Procedia 67 ( 2015 ) 93 – 100, doi: 10.1016/j.egypro.2015.03.292.

[34] Raval, Mehul and Solanki, C. (2013). Review of Ni-Cu Based Front Side Metallization for c-Si Solar Cells. Journal of Solar Energy. 2013. 10.1155/2013/183812.

[35] L.F. Durkee, Method of plating by means of light, US Patent No. 4,144,139, Solarex Corporation, Rockville, Md, USA, 1979.

[36] Miles V. Sullivan and John H. Eigler, Electroless Nickel Plating for Making Ohmic Contacts to Silicon, J. Electrochem. Soc. 1957 volume 104, issue 4, 226-230, doi: 10.1149/1.2428541

[37] H. H. Kuehnlein, N. Koesterke, G. Cimiotti et al., “>0.4% absolute efficiency gain by fast Ni-Cu-Sn electroplating of solar cells with fine line printed contacts by a single side wet treatment technology,” in Proceedings of the 24th European Photovoltaic Solar Energy Conference and Exhibition (EU PVSEC ’09), pp. 282–284, Hamburg, Germany, September 2009.

[38] A. Aguilar Antony Aguilar, Stanislau Y Herasimenka, Joseph Karas, Harsh Jain, Jongwon Lee, Krystal Munoz, Lynne Michaelson, Tom Tyson, William J Dauksher, Stuart Bowden, "Development of Cu plating for silicon heterojunction solar cells," 2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC), Portland, OR, 2016, pp. 1972-1975. doi: 10.1109/PVSC.2016.7749972

[39] Markus Glatthaar , Rukmangada Rohit, Andreas Rodofili, Yitzhak J. Snow, Jan Nekarda, and Jonas Bartsch, Novel Plating Processes for Silicon Heterojunction Solar Cell Metallization Using a Structured Seed Layer, IEEE JOURNAL OF PHOTOVOLTAICS, VOL. 7, NO. 6, NOVEMBER 2017, DOI: 10.1109/JPHOTOV.2017.2748999

[40] Thibaud Hatt, Vivek P. Mehta, Jonas Bartsch, Sven Kluska, Mike Jahn, Dietmar Borchert, and Markus Glatthaar, Novel mask-less plating metallization route for bifacial silicon heterojunction solar cells, AIP Conference Proceedings 1999, 040009 (2018); doi: 10.1063/1.5049272.

[41] Sven Kluska, Andreas Buchler, Jonas Bartsch, Benjamin Gr¨ubel, Andreas A. Brand, Simon Gutscher, Gisela Cimiotti, Jan Nekarda, and Markus Glatthaar, Easy Plating—A Simple Approach to Suppress Parasitically Metallized Areas in Front Side Ni/Cu

Plated Crystalline Si Solar Cells, IEEE JOURNAL OF PHOTOVOLTAICS, VOL. 7, NO. 5, SEPTEMBER 2017, DOI: 10.1109/JPHOTOV.2017.2720461.

[42] Andreas Büchler, Sven Kluska, Jonas Bartsch, Gisela Cimiotti, Andreas A. Brand, Martin C. Schubert, Markus Glatthaar, Optimizing adhesion of laser structured plated Ni-Cu contacts with insights from micro characterization, Energy Procedia 92 ( 2016 ) 913 – 918, doi: 10.1016/j.egypro.2016.07.101.

[43] Andreas Büchler, Sven Kluska, Fabian Meyer, Andreas A. Brand, Gisela Cimiotti, Jonas Bartsch, Markus Glatthaar, Interface oxides in femtosecond laser structured plated Ni-Cu-Ag contacts for silicon solar cells, Solar Energy Materials and Solar Cells 166 (2017) 197–203, http://dx.doi.org/10.1016/j.solmat.2017.03.016.

[44] A. M. Cowley, Titanium-Silicon schottky barrier diodes, Solid-State Electronics Pergamon Press 1970. Vol. 12, pp. 403-414.

[45] LaFontaine, W., Yost, B., and Li, C. (1990). Effect of residual stress and adhesion on the hardness of copper films deposited on silicon. Journal of Materials Research,(4), 776-783. doi:10.1557/JMR.1990.0776.

[46] R. Jaeger, Introduction to Microelectronic Fabrication: Volume 5 of Modular Series on Solid State Devices (2nd Edition), 1988, Addison-Wesley Longman Publishing Co., Inc. Boston, MA, USA ©1987, ISBN:0-201-14695-9

[47] A. Lachowicz, J. Geissbühler, A. Faes, J. Champliaud, J. Hermans, J.F Lerat, P.J Ribeyron, C. Roux, G. Wahli, P. Papet, B. Strahm, J. Horzel, C. Ballif and M. Despeisse, Reliable copper plating process for bifacial heterojunction cells, 7th Workshop on Metallization and Interconnection for Crystalline Silicon Solar Cells, 23. October 2017, Konstanz

[48] Luana Mazzarella , Ana Belen Morales-Vilches , Max Hendrichs, Simon Kirner, Lars Korte , Rutger Schlatmann , and Bernd Stannowski, "Nanocrystalline n-Type Silicon Oxide Front Contacts for Silicon Heterojunction Solar Cells: Photocurrent Enhancement on Planar and Textured Substrates," in IEEE Journal of Photovoltaics, vol. 8, no. 1, pp. 70-78, Jan. 2018. doi: 10.1109/JPHOTOV.2017.2770164

[49] R. Sinton, A. Cuevas and M. Stuckings, "Quasi-steady-state photoconductance, a new method for solar cell material and device characterization," in Conference Record of the IEEE Photovoltaic Specialists Conference ,1996.

[50] G. Limodio, G. Yang, P. Procel, O. Isabella, M. Zeman, “Carrier-Selective contacts with different thermal budget for front / back contacted (fbc) solar cells”, SiliconPV, Lausanne, (2018).

[51] G. Limodio, G. Yang, H. Ge, P. Procel, Y. De Groot, L. Mazzarella, O. Isabella, M. Zeman, Front and rear contact Si solar cells combining high and low thermal budget Si passivating contacts, Solar Energy Materials and Solar Cells, Volume 194, 2019, Pages 28-35, https://doi.org/10.1016/j.solmat.2019.01.039

[52] Z. C. Holman, A. Descoeudres, S. De Wolf and C. Ballif, "Record Infrared Internal Quantum Efficiency in Silicon Heterojunction Solar Cells With Dielectric/Metal Rear Reflectors," in IEEE Journal of Photovoltaics, vol. 3, no. 4, pp. 1243-1249, Oct. 2013. doi: 10.1109/JPHOTOV.2013.2276484

[53] https://ktauniversity.com/coating-adhesion-testing-knife-tape/ (Accessed 19th September 2018)

[54] Stefan Braun, Annika Zuschlag, Bernd Raabe, Giso Hahn, The Origin of Back-

ground Plating, Energy Procedia, Volume 8, 2011, Pages 565-570, ISSN 1876-6102, https://doi.org/10.1016/j.egypro.2011.06.183.

[55] Atteq ur Rehman and Soo Hong Lee, Review of the Potential of the Ni/Cu Plating Technique for Crystalline Silicon Solar Cells, Materials 2014, 7, 1318-1341; doi:10.3390/ma7021318.

[56] Q. Xu, Y. Ra, M. Bachman, and G. P. Li, Characterization of low-temperature silicon nitride films produced by inductively coupled plasma chemical vapor deposition, Journal of Vacuum Science and Technology A 27, 145 (2009); doi: 10.1116/1.3054133.

[57] M.S. Chandrasekar, Malathy Pushpavanam, Pulse and pulse reverse plating—Conceptual, advantages and applications, Electrochimica Acta, Volume 53, Issue 8, 2008, Pages 3313-3322, https://doi.org/10.1016/j.electacta.2007.11.054.

[58] Rukmangada Rohit, Andreas Rodofili, Gisela Cimiotti, Jonas Bartsch, Markus Glatthaar, Selective plating concept for silicon heterojunction solar cell metallization, Energy Procedia, Volume 124, September 2017, Pages 901-906 , https://doi.org/10.1016/j.egypro.2017.09.289.

[59] D. Zhang, I.A. Digdaya, R. Santbergen, R.A.C.M.M. van Swaaij, P. Bronsveld, M. Zeman, J.A.M. van Roosmalen, A.W. Weeber, Design and fabrication of a SiOx/ITO double-layer anti-reflective coating for heterojunction silicon solar cells, Solar Energy Materials and Solar Cells, Volume 117, 2013, Pages 132-138, https://doi.org/10.1016/j.solmat.2013.05.044.

[60] Daisuke Adachi, Toru Terashita, Toshihiko Uto, José Luis Hernández, Kenji Yamamoto, Effects of SiOx barrier layer prepared by plasma-enhanced chemical vapor deposition on improvement of long-term reliability and production cost for Cu-plated amorphous Si/crystalline Si heterojunction solar cells, Solar Energy Materials and Solar Cells, Volume 163, 2017, Pages 204-209, https://doi.org/10.1016/j.solmat.2016.12.029.

[61] Y. Zhao, "Contact stack evaluation for SHJ solar cells and process development for IBC-SHJ solar cells", 2018, https://repository.tudelft.nl/islandora/object/uuid%3A77f483ae-f1da-42c1-8c5a-ae601b140d90

[62] https://public.wsu.edu/ pchemlab/documents/Work-functionvalues.pdf (accessed 12th March 2019)

[63] https://www.tibtech.com/conductivite.php?lang=en-US (Accessed 1st October 2018).

[64] International Electrotechnical Commission, Crystalline silicon terrestrial photovoltaic (PV) modules – Design qualification and type approval, IEC 61215:2005(E)

[65] Alison Lennon, Jack Colwell, Kenneth P. Rodbell, Challenges facing copper-plated metallisation for silicon photovoltaics: Insights from integrated circuit technology development, Progress in Photovoltaics: Research and Applications, https://doi.org/10.1002/pip.3062.

[66] Russell, R.; Tous, L.; Labie, R.; Aleman, M.; Duerinckx, F.; Bertens, J.; Horiuchi,T.; Szlufcik, J. Cost-effective and reliable Ni/Cu plating for p- and n-type PERx silicon solar cells yielding efficiencies above 20.5%. Photovolt. Int. 2013, 2013, 62–69.

# 8

# HIGH TEMPERATURE OXIDATION PRE-TREATMENT OF TEXTURED C-SI WAFERS PASSIVATED BY A-SI:H

*ABSTRACT - This chapter shows an alternative surface cleaning method for c-Si wafers to replace the standard chemical procedures as RCA or $HNO_3$ which involve hazardous chemicals or unstable processes. The method consists in a high-temperature oxidation treatment (HTO) performed in a classical tube furnace that incorporates organic and metal particles present on the c-Si surfaces in the growing $SiO_2$ layer. The result is as a reliable pre-treatment method for obtaining less defective c-Si surfaces ready for solar cell fabrication after $SiO_2$ removal. To test the surface passivation quality obtained with our alternative cleaning method, we grow amorphous silicon (a-Si:H) layers by plasma enhanced chemical vapor deposition on both sides of the c-Si wafer and systematically compare the effective carrier lifetime $\tau_{eff}$ and implied open-circuit voltage ($iV_{OC}$) to the wafer treated with the standard cleaning in our laboratory. We optimize HTO treatment time reaching $\tau_{eff}$ of 6 ms and $iV_{OC}$ of 721 mV for the best sample. We ascribe the improved passivation quality using HTO to two concurrent factors. Firstly, the encapsulation of defects into $SiO_2$ layer that is then etched prior a-Si:H deposition and secondly, to modification of the pyramids' morphology that facilitates the surface passivation. SEM pictures and reflection measurements support the latter hypothesis.*

Parts of this chapter have been published to Material Science in Semiconductor Processing G. Limodio et. al., MSSP, Volume 97, 2019, Pages 67-70, https://doi.org/10.1016/j.mssp.2019.03.008.

## 8.1. INTRODUCTION

In both semiconductor and photovoltaic industries, the cleaning of the crystalline silicon (c-Si) wafers to remove residues prior device fabrication is a crucial step. Therefore, wafers are dipped in chemical baths to remove organic and metallic impurities from the Si surfaces. The most commonly used procedure consists in a cycle of oxidation-etching steps in order to encapsulate all the surface contaminants into thin $SiO_2$ grown on the c-Si surface and etch them away using highly diluted hydrofluoric acid (HF) [1][2][3][4]. This method is fundamental to achieve high performance devices. Indeed, a contamination-free Si surface will reduce defect density at interface, giving higher passivation quality than a not-treated surface [5][6]. This thin oxidation is often done via RCA cleaning [7] or ozone-based treatment [8]. Alternatively, the use of so-called nitric acid oxidation cycle (NAOC) results in comparable lower surface recombination velocity [9]. NAOC procedure consists of dipping the wafers three times in nitric acid to form a thin $SiO_x$ layer and HF etching in between. Both mentioned cleaning methods involve hazardous chemical substances that make the treatment costly owing to the disposal of the chemical waste, safety and environmental risks. Therefore, alternative cleaning methods might be attractive to reduce costs and simplify the fabrication of devices, such as c-Si solar cells. Attempts to reduce number of steps in the cleaning procedure were made by Lu et. al. [10] with promising values of saturation current density ($J_0$) below 10 fA/cm$^2$. Hydrogen plasma pre-treatment is eventually used to hydrogenate c-Si bulk [11]. Also, replacing the final HF etching step with hydrogen plasma etching was suggested by Mueller et. al. [12]. In this chapter, we propose a novel wafer cleaning method that consists in a single-step high temperature oxidation (HTO) followed by $SiO_2$ etching in diluted HF solution. This method can be evidently deployed also in batch mode. As a result of volume expansion process, the HTO process consumes c-Si surface such that organic/metallic contaminants are encapsulated into $SiO_2$ layer. Typically, 50% of the total $SiO_2$ thickness is expanded into Si during thermal oxidation process [13]. Moreover, also impurity gettering is performed during this process. A similar approach has been developed in [14], with gettering and hydrogenation of the wafer through $SiN_x$ layer and rapid thermal firing. We investigate the passivation quality of double-side textured wafers treated with HTO for variable treatment time by passivating the c-Si surfaces with a-Si:H layers growth via plasma enhanced chemical vapor deposition (PECVD). These a-Si:H layers provide both chemical and field-effect passivation. We compare the HTO-treated samples to a wafer treated with the standard wet-chemical oxidation NAOC method. The better passivation quality obtained with the optimized HTO treatment time is related also to morphology modifications of the random pyramids that additionally facilitate the growth of high quality a-Si:H layer.



## 8.2. EXPERIMENTAL DETAILS

For symmetric samples fabrication, we use 4 inches n-type float zone (FZ) silicon wafers (c-Si) with polished <100> oriented surfaces, a resistivity of 2.5 Ωcm and initial thickness of 280 $\mu$m. The c-Si substrates are cleaned in a nitric acid (99% $HNO_3$) bath for 10 min at 20 °C, followed by a dip in 69.5% $HNO_3$ at 110 °C to remove organic residuals and metallic contaminations, respectively. Samples are then chemically textured in

a solution containing TMAH, AlkaText and $H_2O$ to obtain random pyramids with <111> oriented facets on both sides of the wafer (Figure 8.1(a)). Then, the wafers are subjected to HTO process in a tube furnace (Tempress Systems) at a temperature of 1050 °C in $O_2$ atmosphere. The treatment time is varied between 20 and 230 minutes that corresponds to a resulting $SiO_2$ film of from 40 to 200 nm-thick (Figure 8.1 (b)). The temperature

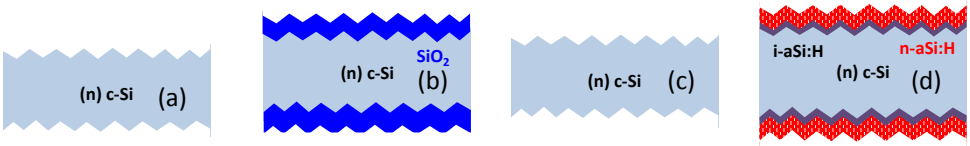


Figure 8.1: Sample fabrication steps: (a) Chemical texturing of the wafer; (b) Thermal oxidation of double sided textured wafer; (c) Etching of $SiO_2$ in HF; (d) i/n a-Si:H stack PECVD deposition as a passivation layer.

is reached with a ramp of 10 °C/min and the $O_2$ flow is set at 3 slm in a dry environment. After oxidation, we remove the $SiO_2$ layer by dipping the sample in 0.55% HF (step (c) in Figure 8.1) with an etching rate of 1 nm/m for the necessary time to make the silicon wafer surface hydrophobic. Instead, the reference wafer is treated with the so-called nitric acid oxidation cycle (NAOC) method, consisting in $HNO_3$ 99%, subsequent $HNO_3$ 69.5% and HF step, as described in [15], that we repeat three times [9]. Finally, the samples are loaded into the PECVD reactor where both sides of the c-Si substrate are covered by a stack of intrinsic and phosphorous doped a-Si:H layers with a thickness of 4.5 and 6 nm, respectively (step (d) in Figure 8.1). Afterwards, the samples are annealed at 190 °C for 30 minutes to enhance passivation quality [16]. Quasi-steady-state photoconductance (QSSPC) lifetime measurements [17] are performed on the fabricated samples using a Sinton Instruments WCT-120 carrier lifetime setup. Effective lifetime ($\tau_{eff}$), implied open-circuit voltage ($iV_{OC}$) and recombination current density ($J_0$) are extracted from the measured curves. Furthermore, the as-textured and the optimized HTO treated samples are further characterized by cross-sectional scanning electron microscopy (SEM XL50 Philips with acceleration voltage of 5 kV) and optical reflectance is carried out using a Pelkin Elmer Lambda UV-VIS near-infrared spectrophotometer.



## 8.3. RESULTS AND DISCUSSION

Figure 8.2 shows the minority carrier lifetime against injection level for double-sided textured wafers passivated by i/n a-Si:H stack pre-treated with variable HTO time and compared to the reference pre-treated with NAOC. All the results shown here are after annealing at 190 °C for 30 minutes to improve chemical passivation [18]. The reference sample (black curve in Figure 8.2) shows $\tau_{eff}$ of 2 ms extracted at $10^{15}$ $cm^{-3}$ injection level. By increasing the HTO time, the measured lifetime progressively increases as compared to the value of the reference. For the shorter HTO times tested (from 22 to 56 minutes), the passivation quality improvement is limited only to the low injection level. We observe a slight decrease in lifetime of around 200 µs at low injection level when 37 and 56 minutes HTO treatment are applied. This is most likely due to different pre-conditioning of the PECVD chamber since the samples have been processed in different time slots. It is remarkable how similar values of lifetime at high injection level are

achieved in the NAOC and 37 and 56 minutes HTO cases. When a sample is oxidized for 77 minutes, corresponding to 100 nm-thick $SiO_2$, lifetime improves significantly both in high and low injection level with $\tau_{eff}$ of around 4 ms which doubles the value measured for NAOC reference. By increasing the HTO time to 230 minutes (200 nm-thick

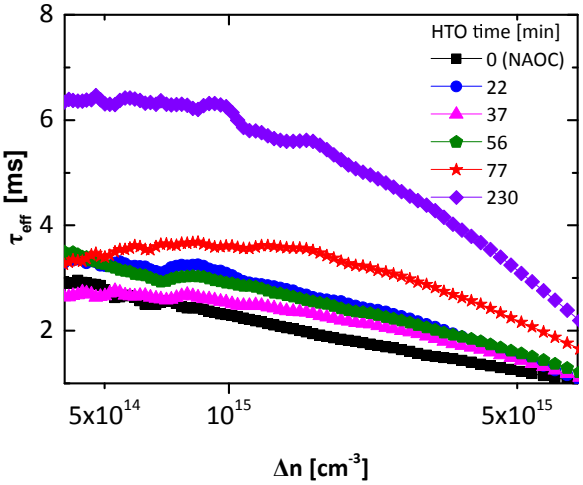


Figure 8.2: Minority carrier lifetime versus carrier density of double sided textured wafers passivated by 4.5/6 nm-thick a-Si:H for a variable HTO treatment time. The curves are measured after a post-deposition annealing at 190 °C for 30 minutes. Reference samples cleaned with NAOC is also added for comparison

$SiO_2$ layer) the entire curve shifts up with $\tau_{eff}$ of around 6 ms at $10^{15}$ $cm^{-3}$ injection level. Figure 8.3 displays the implied $V_{OC}$ and $J_0$ extracted from the curves in Figure 8.2 as function of the HTO treatment time. We clearly note the effect described above with a progressive increase in $iV_{OC}$ (i.e. surface chemical passivation) with increasing thickness of the $SiO_2$ layer. For the NAOC reference sample, $iV_{OC}$ is 705 mV, while the highest $iV_{OC}$ of 721 mV is measured for the sample treated with 230 minutes of HTO. The opposite trend is noted for $J_0$. For the NAOC reference, $J_0$ is 12 $fA/cm^2$, while for the sample pre-treated with 230 minutes of oxidation, $J_0$ decreases to 7 $fA/cm^2$. We can conclude that the passivation quality of i/n a-Si:H stack is then affected by HTO treatment time and therefore by the grown $SiO_2$ thickness. We tentatively explain the improved surface passivation obtained with HTO by the encapsulation of surface contaminants present on the Si surface within thermal $SiO_2$, which partially expands into the Si bulk. All these surface contaminants are then etched away by removing the $SiO_2$ in HF solution. This results in a clean c-Si surface ready for passivation by a-Si:H stack. Increasing the HTO time, $SiO_2$ goes deeper into the Si bulk and more impurities are removed from Si surface [19]. An enriched chemical passivation is achieved by $J_0 < 10$ $fA/cm^2$. This indicates that more surface contaminants have been removed from the surface than in the NAOC case. It is noteworthy to remark how the proposed HTO process is capable of improving performances in FZ wafers. By transferring this method to industrially-relevant Czochralski wafers (CZ), the encapsulation of surface impurities into $SiO_2$ and stabilization of bulk lifetime by the so-called tabula rasa treatment [20] can be achieved at the same time.

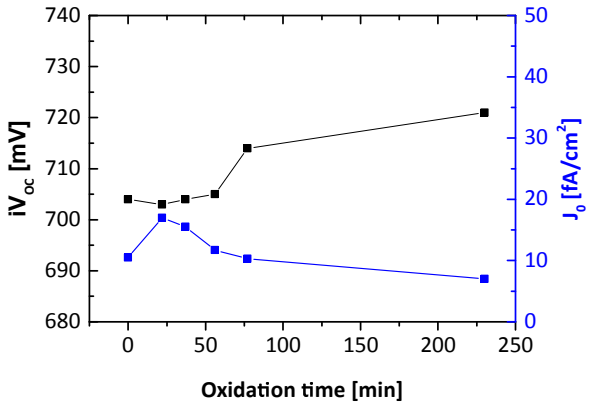


Figure 8.3: Implied $V_{OC}$ and saturation current density ($J_0$) of double-sided textured wafers passivated by 4.5/6-nm thick i/n a-Si:H with NAOC or thermal $SiO_2$ pre-treatment as function of the oxidation time.

To further analyze the effect of HTO on the c-Si wafer surface, we rely on cross-sectional scanning electron microscopy (SEM). Figure 8.4 (a) shows a SEM image of an as-textured wafer, while Figure 8.4 (b) is the image taken after HTO treatment (230 minutes) and subsequent etching of $SiO_2$. The scale is slightly different due to different focus obtained to have optimal images. The reference textured wafer in Figure 8.4 (a) has steep valleys of the pyramids. On the other hand, the HTO-treated wafer has rounded valleys; there-

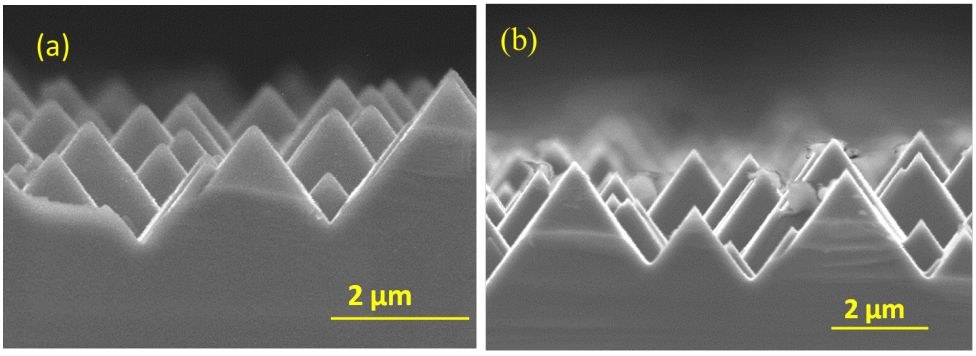


Figure 8.4: Cross-sectional Scanning Electron Microscopy (SEM) of textured wafers (a) after texturing and (b) 230 minutes of HTO treatment. Both images are taken after etching the $SiO_2$ layer.

fore, the amount of defects is decreased. In general, the more the tip or the valley of a textured wafer is rounded, the less is the structural defect density associated to it [21]. Therefore, it is easier to obtain enriched chemical passivation. In particular, the more the valley is rounded, the more it is unlikely to have epitaxial growth of a-Si [22]. This concurs to the improved passivation properties. The images reveal residuals that are the results of a cut in 6-cm wide slab to fit the cross-sectional stage of SEM. The drawback of this procedure stays in the slightly reduced reflectivity due to not perfect light scattering

and reduced optical path length in the c-Si wafer [23]. Figure 8.5 shows the reflectance exhibited by the same wafers shown in Figure 8.4. In the whole wavelength range, the reflectance is lower for the HTO-treated wafer. Therefore, light scattering is more efficient in the reference sample than the HTO-treated one. We can conclude that, although the

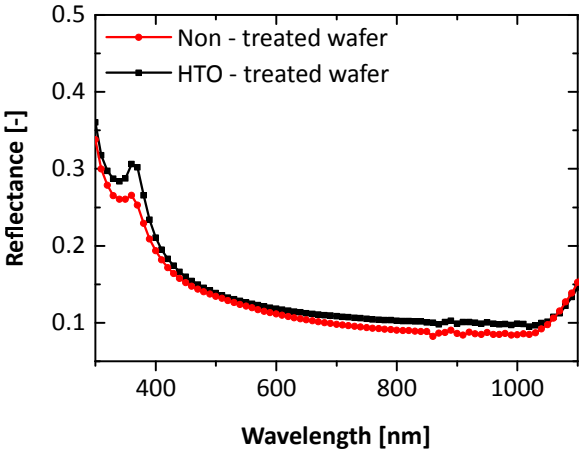


Figure 8.5: Measured reflectance of reference (red line) and HTO-treated (black line) wafers.

pyramids' size is the same in both textured and HTO-treated cases, the pyramids' valleys are slightly more rounded in the HTO-treated case compared to as-textured wafer. This issue can be nevertheless overcome by using transparent conducting oxide layer or anti-reflective dielectrics, such as $MgF_2$ or $SiO_x$ [24].

## 8.4. CONCLUSION

In conclusion, we investigate an alternative cleaning method suitable for textured c-Si wafers that does not involve the use of hazardous chemicals. This method consists in a high-temperature oxidation (HTO) treatment in a conventional furnace followed by an etching step HF solution prior further processing the substrate for device fabrication. To measure the passivation quality, the textured c-Si surfaces are covered with a-Si:H layers deposited by PECVD. Since the HTO encapsulates Si surface impurities, we perform a series of HTO treatment time to investigate the impact on chemical passivation. After HF etching, the wafers are immediately transferred to PECVD chamber to deposit 4.5/6 nm-thick i/n a-Si:H layer. These samples have been characterized using QSSPC method and compared to a sample equally passivated but pre-treated with 3 cycles of thin wet-oxidation and HF etching (NAOC). This analysis is carried out by passivating the textured wafer by 4.5/6 nm-thick i/n a-Si:H, but the conclusions drawn are the same for other a-Si:H layer thicknesses. We find out that increasing oxidation time, i.e. thermal $SiO_2$ thickness, both carrier lifetime and implied $V_{OC}$ progressively improved and exceeded the values measured on the reference sample treated with NAOC. The best HTO treatment time is found at 230 minutes with $\tau_{eff}$ and $iV_{OC}$ of 6 ms and 721 mV, respectively. Since the passivation layers stack is kept constant for all the samples fabricated, we can

conclude that the improvement in chemical passivation are to be ascribed to the removal of impurities from the c-Si surface and to the formation of rounded valleys after etching the thermally-grown $SiO_2$, as shown by cross-sectional SEM images. It is to remark that HTO process can be applicable also to planar wafers. The drawn conclusions are the same except for less defect density of the polished c-Si interface compared to textured one. This method could be further engineered and optimized for batch process compatible with mass production. Moreover, this method is also beneficial for industrial CZ wafers, since a tabula rasa could be performed at the same time with encapsulation of surface contaminants.

## 8.5. REFERENCES

[1] W. Kern and D. A. Puotinen, RCA Rev. 31, 187 (1970).

[2] Werner Kern, J. Electrochem. Soc., Vol. 137, No. 6, June 1990.

[3] K. Sakamoto, K. Nishi, F. Ichikawa, and S. Ushio, Journal of Applied Physics 1987 61:4, 1553-1555

[4] J. Haschke et. al., AIP Conference Proceedings 1999, 030001 (2018); doi: 10.1063/1.5049262

[5] A. Froitzheim, K. Brendel, L. Elstner, W. Fuhs, K. Kliefoth, M. Schmidt, Journal of Non-Crystalline Solids 299–302, (2002), 663–667.

[6] H. Angermann, Applied Surface Science, Volume 254, Issue 24, 2008, pp. 8067-8074,

[7] L. Zhang, W. Liu, R. Chen, L. Jinning, F. Meng, Z. Liu, K. Toshima, A. Ota, T. Yoshihara, 2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC), Portland, OR, 2016, pp. 0743-0746. doi: 10.1109/PVSC.2016.7749701

[8] A. Danel, F. Jay, S. Harrison, C. Arnal, G. D'Alonzo, N. Nguyen, A. S. Ozanne, P. E. Hickel, D. Muñoz and P. J. Ribeyron, Proc. 26th European Photovoltaic Solar Energy Conference and Exhibition, Hamburg, Germany, 2011.

[9] D. Deligiannis, S. Alivizatos, A. Ingenito. D. Zhang, M. van Sebille, R.A. C. M. M. van Swaaij, M. Zeman, Energy Procedia, 55, 197-202 (2014).

[10] X. Lu, M. Koppes, P.C.P Bronsveld, AIP Conference Proceedings 1999, 050005 (2018); https://doi.org/10.1063/1.5049295.

[11] Fengyou Wang, Xiaodan Zhang, Liguo Wang, Yanjian Jiang, Changchun Wei, Jian Sun, and Ying Zhao, ACS Appl. Mater. Interfaces, 2014, 6 (17), pp 15098–15104, DOI: 10.1021/am5031837.

[12] T. Mueller, M. Tang, J. Ge and J. Wong, 2015 IEEE 42nd Photovoltaic Specialist Conference (PVSC), New Orleans, LA, 2015, pp. 1-4. doi: 10.1109/PVSC.2015.7356324

[13] B. E. Deal and A. S. Grove, Journal of Applied Physics 1965 36:12, 3770-3778, https://doi.org/10.1063/1.1713945

[14] Brett Hallam, Daniel Chen, Jianwei Shi, Roland Einhaus, Zachary C. Holman, Stuart Wenham, Solar RRL, 2018, Volume 2, Issue 2, https://doi.org/10.1002/solr.201700221.

[15] G. Yang, A. Ingenito, N. v. Hameren, O. Isabella and M. Zeman, Applied Physics Letters, p. 108, 2016.

[16] J.W.A. Schüttauf, C.H.M. van der Werf, M. Kielen, W.G.J.H.M.van Sark, J.K. Rath, R.E.I. Schropp, Journal of Non-Crystalline Solids, Volume 358, Issue 17, 1 September

2012, Pages 2245-2248, https://doi.org/10.1016/j.jnoncrysol.2011.12.063.

[17] R. Sinton, A. Cuevas and M. Stuckings, in Conference Record of the IEEE Photovoltaic Specialists Conference ,1996.

[18] Illiberi, A., Sharma, K., Creatore, M. and van de Sanden, M. C. M. (2010), phys. stat. sol. (RRL), 4: 172–174. doi:10.1002/pssr.201004139

[19] J. Dabrowski, H.-J. Mussig, V. Zavodinsky, R. Baierle and M. J. Caldas, PHYSICAL REVIEW B, VOLUME 65, 245305, 2002, DOI: 10.1103/PhysRevB.65.245305

[20] V. LaSalvia, M.A. Jensen, A. Youssef, W. Nemeth, M. Page, T. Buonassisi, P. Stradins, 2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC), Portland, OR, 2016, pp. 1047-1050. doi: 10.1109/PVSC.2016.7749771

[21] A. Moldovan, T. Dannenberg, J. Temmler, L. Kroely, M. Zimmer, J. Rentscha, Energy Procedia 92,(2016),374–380,doi: 10.1016/j.egypro.2016.07.115.

[22] S. Olibet, C. Monachon, A. Hessler-Wyser, E. Vallat-Sauvain, S. De Wolf, L. Fesquet, J. Damon-Lacoste, C. Ballif, 23rd European Photovoltaic Solar Energy Conference, 1-5 September 2008, Valencia, Spain

[23] Gong, H.-Y, Huang, Haibin, Zhou, Lang. (2015). Rengong Jingti Xuebao/Journal of Synthetic Crystals. 44. 913-917.

[24] D. Zhang, I.A. Digdaya, R. Santbergen, R.A.C.M.M. van Swaaij, P. Bronsveld, M. Zeman, J.A.M. van Roosmalen, A.W. Weeber, Solar Energy Materials and Solar Cells, Volume 117, 2013, Pages 132-138, https://doi.org/10.1016/j.solmat.2013.05.044.

# 9

# CONCLUSION AND OUTLOOK

## 9.1. CONCLUSION

THIS thesis provides strategies for the implementation of ion implantation doping technique in c-Si wafer-based solar cells. Since crystalline silicon solar cells dominate the market, it is crucial to research possible ways to further minimize production costs. For this reason, ion implantation can play a very important role in this field. Reasons for this are various; i) ion implantation is already successfully deployed in microelectronic integrated circuit industry, ii) it is a local doping technique, so it can be used in PERC solar cells which represent the standard architecture in the PV market and iii) the combination of this doping technique with carrier-selective passivating contacts can give very high efficiency. The author believes that, after PERC, the evolution of c-Si solar cells will be to employ high-thermal budget passivating contacts. Therefore, ion implantation can play a crucial role in this evolution. The main conclusions drawn from this thesis are listed in this chapter: Chapter 1 shows the conditions of PV market, the theoretical working principle of a c-Si wafer-based solar cell and a literature review, highlighting advantages and drawbacks, of the state-of-the-art technology employed in c-Si wafer-based solar cells field.

In chapter 2 an insight on ion implantation with focus on its applicability to c-Si solar cells has been shown. Moreover, experimental details have been deeply explained for all the solar cells architecture deployed along this thesis.

Chapter 3 shows a first application of ion implantation in c-Si solar cells. Indeed, a homojunction solar cell with P-implanted BSF and B-implanted front emitter has been fabricated. The cell is finished by $Al_2O_3$ front passivation layer, $SiN_x$ as anti-reflection coating and front Al grid and rear full-area Ag/Cr/Al blanket. First a study of $Al_2O_3$ passivation of B-implanted textured silicon has been carried out. It turns out that passivation quality is in contrast with sheet resistance of B-doped layer. Indeed, the lower the sheet resistance is, the poorer the passivation quality is. Regarding devices, it is possible to note that although Al-BSF is replaced by a P-doped layer as back contact, very low open circuit voltage ($V_{OC}$) is achieved. This is due to high recombination rate occurring at c-

Si/metal interface. A full-area rear metal coverage introduces such high recombination that limits $V_{OC}$ to 620 mV and efficiency to 18.6% in our case.

Chapter 4 shows the application of ion implantation doping technique in combination with tunnelling $SiO_2$ / doped poly-Si stack. First, passivation properties depending on ion implantation parameters (energy and dose) and annealing time and temperature are highlighted for both p- and n-type poly-Si. Then, this analysis is done at different poly-Si thicknesses. It turns out that, to have excellent field-effect passivation, high doping concentration should be confined into poly-Si layer with a relatively sharp tail into c-Si. Excellent passivation properties are found independently of poly-Si thickness in the case of electron selective contact ($J_0$ < 15 fA/cm$^2$). In the case of poly-Si hole-selective contact instead, passivation properties worsen with decreasing poly-Si thickness because of deeper penetration of boron dopants into c-Si bulk, generating inactive clusters of dopants and weaker electrical field across the junction. By employing TCAD Sentaurus modelling software, it is possible to understand that doping in-diffusion into c-Si bulk is very handy for selectivity purpose because band-bending will influence majority carriers' accumulation at c-Si/$SiO_2$ interface. Then, the optimized layers are employed into a poly-poly solar cell. This consists in a rear junction device with $SiO_2$/doped poly-Si stack on both sides. At the textured front the electron-selective layer, consisting in $SiO_2$ / P-doped poly-Si, is deposited, while the flat rear side is coated by $SiO_2$ / B-doped poly-Si stack. Dielectric anti-reflection coating as $SiN_x$ is employed and then H-grid shaped and full-area metallization are deployed at the front and rear side, respectively. It is demonstrated that it is possible to achieve reasonably high fill-factor (FF > 70%) without any transparent conductive oxide (TCO). At device level, short-circuit current density ($J_{SC}$) increases of 4 mA/cm$^2$ when front side poly-Si thickness is reduced from 250 nm to 35 nm because of improved current collection at the short-wavelength and in the visible part of the spectrum. $V^{OC}$ worsens when front and rear poly-Si thicknesses are thinned because of the hole-selective contact poor passivation quality. Therefore, to achieve relatively high $J_{SC}$) and improve $V_{OC}$, front and rear poly-Si thicknesses were decoupled. Supported by TCAD Sentaurus modelling software, it turns out that this choice does not affect significantly current collection. Therefore, we achieve an aperture-area efficiency of 19.6% thanks also to improved FF due to advanced Ti/Cu-plated metallization. The efficiency limit of this solar cells lies in low short-circuit current density due to parasitic absorption of front poly-Si.



In chapter 5 one of the possible strategies to overcome current collection limit of poly-poly solar cell is presented. Indeed, fabrication of PeRFeCT (Passivated Emitter and Rear ConTacts) solar cell is shown. It consists in a front-selective front surface field structure with tunnelling $SiO_2$/doped poly-Si only underneath the contacts. Elsewhere, a lightly doped homojunction (HMJ) front-surface field is employed. Once again anti-reflection coating is made by $SiN_x$, Al is structured at the front and Ag is evaporated on the full-area at rear. This architecture, more complex than poly-poly from fabrication point of view, can achieve short-circuit current density greater than 40 mA/cm$^2$. This is due to very good collection at short-wavelength due to optical transparency of the front surface field. In this case, conversion efficiency is 20.0% but the $V_{OC}$ is limited to 660 mV by back-end processing due to no spacing between poly-Si fingers and metal openings.

Chapter 6 provides another strategy to avoid current collection limit in poly-poly so-

lar cell with a hybrid approach. It consists in a rear junction with the front side passivated by i/n hydrogenated amorphous silicon (a-Si:H) stack and rear side by $SiO_2$ / B-doped poly-Si. Then, indium tin oxide (ITO) is used as transport layer and anti-reflection coating. Al or Ti/Cu grid is deposited at the front and full-area Ag/Cr/Al stack is deposited at rear. Also in this case, with a careful engineering of the front grid design, it is possible to achieve a current in the range of 40 $mA/cm^2$. First, the i/n a-Si:H passivation properties are deeply investigated regarding aspects as post-deposition annealing temperature, time, environment and degradation in time. Then, a lean manufacturing process consisting in only 4 steps is presented. Best conversion efficiency achieved in this case is 21.0%.

Chapter 7 presents Cu-plating as alternative metallization technique respect to standard Al/Ag e-beam/thermal evaporation. In fact, it is shown how this technique is implemented on c-Si wafer-based solar cell embedding carrier-selective passivating contacts with high and low thermal budget. First, two dedicated processing methods are developed for dielectric and conductive anti-reflection coating, respectively. Then, the development and the optimization of Cu-plated contacts with Ti or Ag seed layer is presented taking into account contact uniformity, thickness and aspect ratio. Then, two different solutions to overcome the issue of background plating are proposed; i) pulse-plating instead of direct current plating and ii) dielectric layer barrier as $SiO_x$. Finally, this technique is employed into solar cells embedding carrier selective passivating contacts. Compared to evaporated Al, Cu-plating can achieve high FF. It still has poorer performances than screen printed Ag. In all the tested cases, $V_{OC}$ drops of at least 5 mV is observed when Cu-plating is observed.

Finally, in chapter 8 a novel pre-treatment method before i/n a-Si:H stack deposition is presented. It consists in a single step high-temperature oxidation (HTO). This thermal $SiO_2$ is then stripped straight before the a-Si:H deposition. This pre-treatment has beneficial effects since no hazardous chemicals are involved compared to standard thin oxidation-etching process (Nitric Acid Oxidation of Silicon). Moreover, other advantages of this technique are that i) impurity gettering at wafer level is performed, leaving a 'contaminants-free' surface ready for passivation and ii) in the case of textured substrates, pyramids are rounded especially in the valleys, therefore epitaxial growth of a-Si:H is less likely. Therefore, by employing this method, we achieve effective lifetime of 6 ms for double sided textured wafers passivated by 4.5/6 nm-thick i/n a-Si:H stack when 200 nm-thick $SiO_2$ is grown at the pre-treatment stage.



## 9.2. OUTLOOK

Along this PhD research, many ideas have been conceived and developed. However, some of these ideas are still to be developed in further research due to time constraints. Basically, fully-implanted standard homojunction solar cells (Chapter 3) are the starting point of this research. Then, a switch towards poly-Si carrier-selective passivating contacts with a poly-poly device (Chapter 4) was made. From there, to avoid limitations of the front parasitic absorption, the structure at the front side has been changed, with a selective front-surface field employing homojunction outside the contact region and poly-Si passivating contacts only underneath the contact openings (PeRFeCT solar cell, chapter 5) or a hybrid concept employing a-Si:H front passivation (Hybrid solar cell, chapter

6). Starting from poly-poly solar cell, this can be still used as single junction device with further developments or in a tandem configuration in combination with thin-film technology, such as perovskite. The outlook of this research line is shown in figure 9.1. To

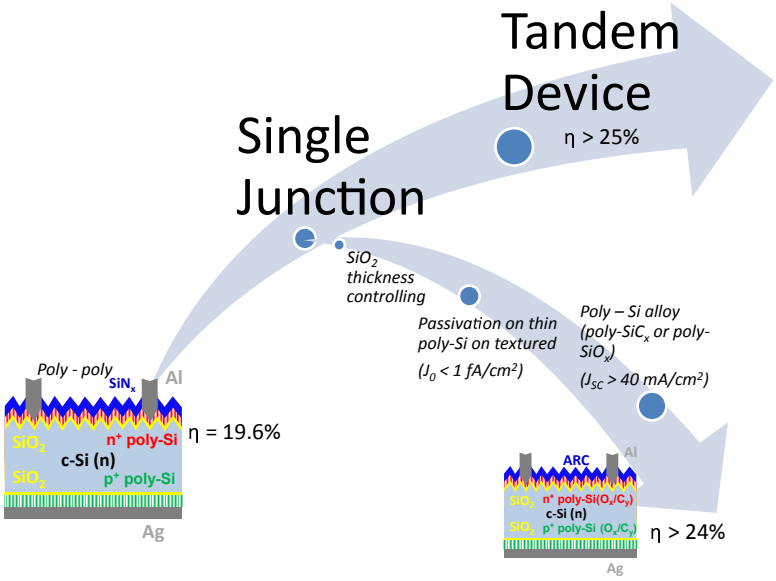


Figure 9.1: Roadmap for high-efficiency c-Si front/back contacted solar cells embedding carrier-selective passivating contacts.

reduce thermalisation losses, there is a possibility of having two different tandem configurations as i) monolithic integration and ii) four-terminal device. There are already instances of such configurations with excellent results as Sahli et. al, Luxembourg et. al. or Loper et. al. for monolithic integration and four terminal, respectively [1][2][3] with perovskite and SHJ solar cells. So, in the author's vision, poly-poly solar cell can be used in tandem device as bottom cell with also front-flat such that a better front transport and an easier processing of top-cell can be done in monolithic integration case. Of course, current matching analysis such that it results in a current higher than 20 mA/cm$^2$ is crucial for this case. In the case of four terminal device, although this configuration enables greater flexibility than the monolithic integration, the challenge will be to develop transparent contact at the rear side of the top cell. It is remarkable how the proposed bottom cell has a high thermal budget; therefore the fabrication of top-cell does not have special requirements in terms of temperature. Regarding the single junction solar cell structure itself, it is crucial to look at three aspects; i) $SiO_2$ as chemical passivation layer, ii) doping distribution across poly-Si/$SiO_2$/c-Si junction and iii) eventual poly-Si alloy to increase band-gap for improved optical transparency. The first aspect is mostly related to the transport across the junction. Indeed, as already discovered in [4], a good tunnelling layer is a necessary condition to achieve FF > 80%. If we assume that tunnelling is the dominant transport mechanism rather than pinhole mediated one, then $SiO_2$ layer must not be thicker than 1.5 nm. Therefore, the thickness of this tunnelling should be

controllable and tuneable to achieve optimum transport layer. So, atomic layer deposition (ALD) or forms of wet chemistry as nitric acid vapour can accomplish this task [5]. ALD-deposited tunnelling $SiO_2$ might represent a significant future research topic. As an eventual expansion, also ALD-deposited tunnelling $Al_2O_3$ can be an alternative if p-type base is used. The reason for using a p-type wafer is that, with $Al_2O_3$, enhanced field-effect passivation can be achieved on p-type surfaces due to high negative fixed charges density [6] together with excellent chemical passivation. Moreover, it is also crucial to explore wet chemistry to obtain tunnelling layers thinner than 1.5 nm as Piranha or HCl cleaning [7]. The challenge will be to monitor how these tunnelling layers will behave when high temperature annealing is performed and how $J_0$ and contact resistivity are influenced by varying tunnelling layer thickness. A parallel development that is a subject for future research is the improvement in passivation properties on very thin poly-Si layer ($d_{poly} < 10$ nm) on textured Si. This is very useful as front electron-selective contact in poly-poly device. Chapter 4 has already shown how n-type poly-Si has a $J_0 < 15$ fA/cm$^2$ independently of its thickness. Doping distribution across the junction has been measured and related to the passivation properties. The author believes that in the future, a tunnelling passivation layer has to be developed, as already stated before, such that $J_0 <$ 1 fA/cm$^2$ and $\tau_{eff} > 10$ ms in the textured case. This means that the tunnelling layer is very effective and, at the same time, its chemical passivation is excellent. To accomplish this task, two main things can be explored, i) using different poly-Si deposition method and/or doping technique, ii) using high-resistivity wafers. For the first point, an in-situ doping, in combination with PECVD poly-Si deposition, or tube furnace diffusion (with still LPCVD poly-Si deposition) could represent a solution to have a doping distribution close to the ideal. The high resistivity wafers are instead needed to induce a stronger electrical field at the poly-Si / $SiO_2$ / c-Si junction. Furthermore, a possible solution to simplify this process is to deposit a silicon-based, crystallized and doped layer after tunnel $SiO_2$ formation. For instance, this can be accomplished by vapour-phase epitaxial growth deposition. The challenge in this case is to avoid that the $SiO_2$ tunnelling layer is etched away by epitaxial deposition. At device level, such thin layer of poly-Si has a very high sheet resistance (> 1000 Ω/sq), therefore a transparent conductive oxide layer is needed. In chapter 6, opto-electronic properties of ITO have been analysed with respect to low-temperature deposition for SHJ processing. Moreover, the influence on passivation properties has been investigated in a double side textured wafer passivated by a-Si:H. This is a starting point to investigate properties of high-temperature deposited ITO for poly-poly solar cells. The author believes that ITO can be employed also in poly-poly devices in combination with PECVD deposited and in-situ doped poly-Si, as partially already demonstrated in literature [8]. Moreover, since there are no special requirements from temperature point of view, ITO or other TCOs can be deposited at higher temperature and therefore its conductivity increases. In order to understand the ultimate efficiency of the poly-poly solar cells fabricated in chapter 4, TCAD Sentaurus simulations of the fabricated solar cells are performed. Since it is a qualitative simulation, it is important to note that these simulations are not optimally calibrated, since they represent a qualitative indication of the routes to pursue to achieve higher efficiencies with these devices. Figures 9.2 shows the simulated and the measured external parameters of the first four solar cells indicated in Table 4.3 in Chapter 4. The simulation replicates the

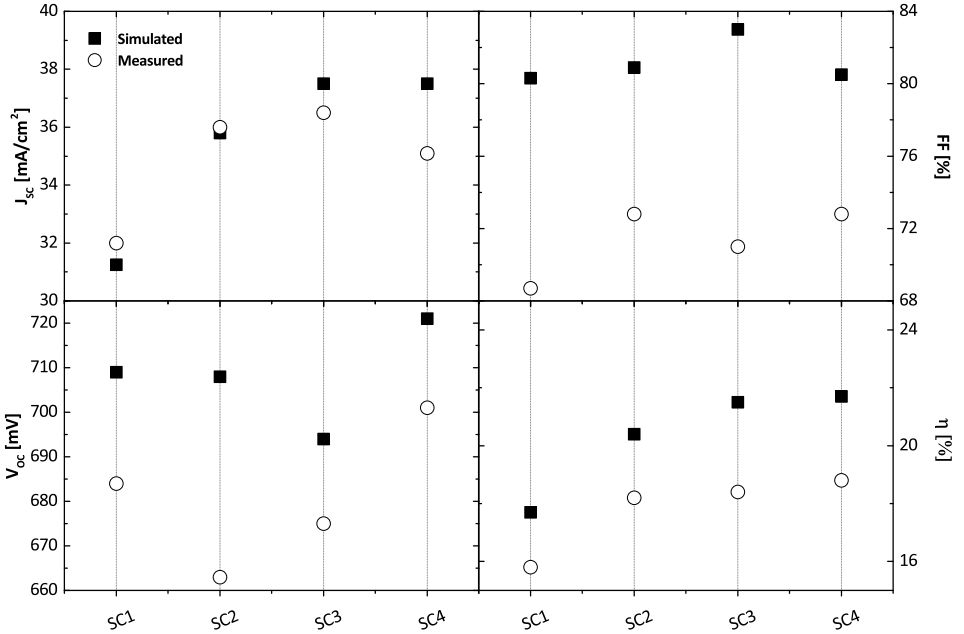


Figure 9.2: Simulated and measured external parameters of SC1, SC2, SC3 and SC4 (see Chapter 4). Note that the purpose of these simulations is to have a qualitative idea of the pitfalls of our fabricated solar cells.

same conditions as the fabricated solar cells ($SiN_x$ anti-reflection coating, 5% coverage metal grid at the front side, Ag/Cr/Al stack at the rear side). In some cases, measured $J_{SC}$ overcomes simulated one (see Figure 9.2 top-left panel), as a not-optimal calibration of the model might underestimate the $J_{SC}$. Regarding $V_{OC}$ (bottom left graph in Figure 9.2), measured values are significantly lower than the simulated ones. In the case of SC1 and SC2, ideal $V_{OC}$ is around 710 mV, for SC3 $V_{OC}$ 695 mV while for SC4 $V_{OC}$ is 720 mV. This confirms our claim of a weak passivation of the 35-nm thick p-type poly-Si layer due to its not optimal doping distribution. Indeed, when we switch from SC3 to SC4, simulated $V_{OC}$ increases of 30 mV. Regarding FF (top-right panel in Figure 9.2), values of our fabricated solar cells are behind the ideal values. All the simulated values are above 80%, while measured ones are between 68 and 73%. We ascribe this major difference to the use of (e-beam) evaporation for realizing the metallization and the not optimal thickness of deposited metals. At the end, the ultimate efficiencies (Figure 9.2 bottom-right panel) are estimated to increase from 17.7% (SC1) to 21.7% (SC4). Also SC5 (the solar cell employing 20/250 nm-thick front/rear poly-Si) has been simulated to recognize its ultimate efficiency. This simulation is performed in two cases; (i) front electron selective contact with an ideal doping profile taken from [4] and rear hole-selective contact with the measured doping profile (see figure 4.7 in Chapter 4) and (ii) both front and rear poly-Si contacts with ideal doping profiles shown in [4].

Table 9.1 highlights the external parameters of such simulated solar cells. In the case of front-ideal and rear-measured doping distributions (SC5-1), $V_{OC}$ is expected to be

Table 9.1: External parameters of simulated solar cell SC5 with ideal/measured doping profiles

| Solar cell | Front poly-Si doping profile | Rear poly-Si doping profile | $V_{OC}$ [mV] | $J_{SC}$ [mA/cm$^2$] | FF [%] | $\eta$ [%] |
|---|---|---|---|---|---|---|
| SC5-1 | Ideal | Measured | 723 | 38.3 | 80.3 | 22.3 |
| SC5-2 | Ideal | Ideal | 725 | 38.3 | 81.8 | 22.7 |

equal to 723 mV, $J_{SC}$ to 38.3 mA/cm2 and FF to 80.3%. The simulated efficiency is thus 22.3%. By employing an ideal doping profile also at rear (SC5-2), the $J_{SC}$ stays at the same level as for SC5-1, $V_{OC}$ improves by 2 mV, but most importantly FF increases by 1.5% absolute. This is because of a better transport of holes at rear side. The ideal efficiency is therefore 22.7%. In perspective, these results are important to understand what to improve in our fabricated solar cells. Indeed, FF losses are the main limiting factor of efficiency of our TCO-free poly-poly solar cells. To tackle these losses, the outlook is to (i) optimize front metal grid, (ii) lower series resistance by enhancing lateral transport with in-diffusion in c-Si bulk [9] (iii) realize an efficient metallization scheme (this has already, partially, been demonstrated by Cu-plating developed in Chapter 7) and (iv) develop rear edge-isolation of poly-Si layer. Moreover, also $V_{OC}$ of our solar cells is affected by non-ideal doping profile. In [4], it is shown how a semi-squared doping profile across c-Si/$SiO_2$/poly-Si junction leads to optimal selectivity. In an expansion of this work, this ideal doping profile (used for simulations shown in Table 4.4) can be achieved by in-situ doped epitaxially-grown layers, LPCVD or PE-CVD techniques. It is noteworthy to mention that recently reported poly-poly cells based on the PECVD route show $V_{OC}$ beyond 720 mV and FF very close to 80% [10]. However, from such experimental results as well as our simulations, it is possible to recognize that the limit of these solar cells is the $J_{SC}$ that, even for front poly-Si thickness of 20 nm, does not overcome 38 mA/cm$^2$. This is due to strong parasitic absorption at the front poly-Si layer. To avoid these losses, there are several different solutions. The first one is to reduce front poly-Si thickness to $d_{poly} < 10$ nm. At that point, a TCO transport layer will be necessary to ensure good fill-factor [11]. Another possible solution is to change the front side structure with either amorphous silicon or a lightly doped homojunction front surface field with poly-Si passivating contacts only underneath the contacts. Figure 9.3 shows the EQE of poly-poly SC3, PeRFeCT solar cell from Chapter 5 and a hybrid solar cell from Chapter 6. With both the hybrid and the PeRFeCT architectures losses in the blue part of the spectrum can be mitigated. The poor responsivity at the short-wavelength of our poly-poly cell is much less problematic if such architecture is deployed in a tandem configuration together with a thin-film top cell such as perovskite. Figure 9.3 shows the necessity of alloying poly-Si material in oxygen or carbon environment such that its bandgap is higher and therefore it is more transparent. There are already instances of this methodology at Delft University of Technology for poly-$SiO_x$ [12] or at EPFL for poly-$SiC_y$ [13][14][15]. The challenge here is to engage active doping by means of ion implantation or in-situ techniques. However, this modification will lead to short-circuit current density higher than 40 mA/cm$^2$ in the poly-poly solar cell. Together with all the tasks set above, a $V_{OC}$

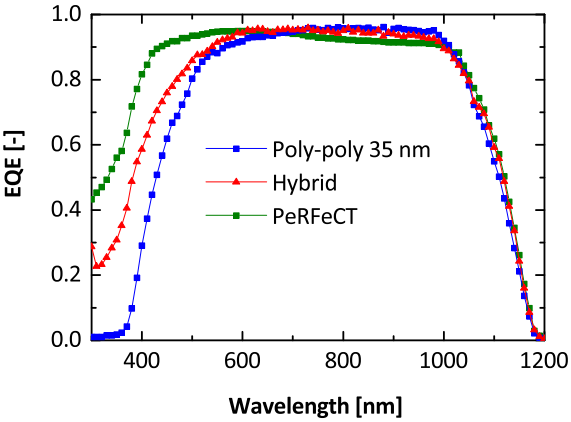


Figure 9.3: External quantum efficiency of poly-poly SC3, a hybrid solar cell with front side based on PERFeCT solar cell (Chapter 5) and on intrinsic amorphous silicon passivation and rear p-type poly-Si (Chapter 6).

> 710 mV and FF > 80%, efficiency greater than 22% can be easily achieved keeping the process flow extremely simple as it is now. Aside these improvements, in the author's vision also structural changes in processing should be implemented to achieve efficiencies higher than 22%. Indeed, until now the poly-poly process was kept as simple as possible to achieve a scientific proof-of-concept. Therefore, the process of different solar cells on one wafer was done full-area on the front and rear side. When the solar cells are ready for measurements, they suffer of low shunt resistance because of the highly conductive path between front and rear contacts. Therefore, the solar cells were cut by a diamond pen to increase significantly the shunt resistance. This cut introduces undesired edge recombination and increases series resistance. Therefore, author's vision is that an optimal patterning/isolation of emitter and front surface field such that the shunting is avoided should be done. Moreover, also anti-reflection coating ($SiN_x$/TCO) has to be patterned at the front side. In this way, it will be possible to avoid any cross-talking between adjacent cells. Moreover, as demonstrated in Chapter 7, Cu-plating should be adopted as reference metallization as it can give low metal resistance. By employing these processing adjustments, in combination with the points previously mentioned, it will be possible to overcome 22% efficiency in a single-junction solar cell.



## 9.3. REFERENCES

[1] Florent Sahli, Jérémie Werner, Brett A. Kamino, Matthias Bräuninger, Raphaël Monnard, Bertrand Paviet-Salomon, Loris Barraud, Laura Ding, Juan J. Diaz Leon, Davide Sacchetto, Gianluca Cattaneo, Matthieu Despeisse, Mathieu Boccard, Sylvain Nicolay, Quentin Jeangros, Bjoern Niesen and Christophe Ballif, Fully textured monolithic perovskite/silicon tandem solar cells with 25.2% power conversion efficiency, Nature Materials volume 17, pages 820–826 (2018), https://doi.org/10.1038/s41563-018-0115-4.

[2] Stefan L. Luxembourg, Dong Zhang, Yu Wu, Mehrdad Najafi, Valerio Zardetto, Wiljan Verhees, Antonius R. Burgers, Sjoerd Veenstra, L.J. Geerligs, Crys-

talline silicon solar cell with front and rear polysilicon passivated contacts as bottom cell for hybrid tandems, Energy Procedia, Volume 124, 2017, Pages 621-627, https://doi.org/10.1016/j.egypro.2017.09.091.

[3] Philipp Löper, Soo-Jin Moon, Sílvia Martín de Nicolas, Bjoern Niesen, Martin Ledinsky, Sylvain Nicolay, Julien Bailat, Jun-Ho Yum, Stefaan De Wolf and Christophe Ballif, Organic–inorganic halide perovskite/crystalline silicon four-terminal tandem solar cells, Phys. Chem. Chem. Phys., 2015,17, 1619-1629, 10.1039/C4CP03788J.

[4] P. Procel, G. Yang, O. Isabella and M. Zeman, "Numerical Simulations of IBC Solar Cells Based on Poly-Si Carrier-Selective Passivating Contacts," in IEEE Journal of Photovoltaics, vol. 9, no. 2, pp. 374-384, March 2019. doi: 10.1109/JPHOTOV.2019.2892527.

[5] Woo-Byoung Kim, Taketoshi Matsumoto and Hikaru Kobayashi, “Ultrathin SiO2 layer with a low leakage current density formed with 100% nitric acid vapor”, 2010 Nanotechnology 21 115202, https://doi.org/10.1088/0957-4484/21/11/115202.

[6] Schmidt, J. , Merkle, A. , Brendel, R. , Hoex, B. , de Sanden, M. C. and Kessels, W. M. (2008), Surface passivation of high-efficiency silicon solar cells by atomic-layer-deposited Al2O3. Prog. Photovolt: Res. Appl., 16: 461-466. doi:10.1002/pip.823.

[7] Malte Köhler, Manuel Pomaska, Florian Lentz, Friedhelm Finger, Uwe Rau, and Kaining Ding, Wet-Chemical Preparation of Silicon Tunnel Oxides for Transparent Passivated Contacts in Crystalline Silicon Solar Cells, ACS Applied Materials and Interfaces 2018 10 (17), 14259-14263, DOI: 10.1021/acsami.8b02002

[8] F. Feldmann, M. Simon, M. Bivour, C. Reichel, M. Hermle and S. W. Glunz., "Efficient carrier selective p- and n- contacts for Si solar cells," Solar Energy Materials and Solar Cells, vol. 131, pp. 100-104, 2014.

[9] Olindo Isabella, Paul Alejandro Procel Moya, Miroslav Zeman, solar cells with transparent contacts based on poly-silicon-oxide, patent nr. WO2019066648A1.

[10] D.L. Young, V. LaSalvia, B. Nemeth, S. Theingi, A. Kale, D. Findley, J. Atkins, M. Page, P. Stradins. Front/Back Poly-Si/SiO2 Passivated Contact Device with Voc > 720 mV. 35th European Photovoltaic Solar Energy Conference and Exhibition, 10.4229/35thEUPVSEC20182018-2AV.3.32.

[11] L. Tutsch, F. Feldmann, J. Polzin, C. Luderer, M. Bivour, A. Moldovan, J. Rentsch, M. Hermle, Implementing transparent conducting oxides by DC sputtering on ultrathin SiOx / poly-Si passivating contacts, Solar Energy Materials and Solar Cells, Volume 200, 2019, 109960, https://doi.org/10.1016/j.solmat.2019.109960.

[12] G. Yang, P. Guo, P. Procel, A. Weeber, O. Isabella, M. Zeman, (2018). Polycrystalline silicon-oxide films as carrier-selective passivating contacts for c-Si solar cells. Applied Physics Letters. 112. 193904. 10.1063/1.5027547.

[13] Gizem Nogay, Josua Stuckelberger, Philippe Wyss, Quentin Jeangros, Christophe Allebé, Xavier Niquille, Fabien Debrot, Matthieu Despeisse, Franz-Josef Haug, Philipp Löper, and Christophe Ballif, Silicon-Rich Silicon Carbide Hole-Selective Rear Contacts for Crystalline-Silicon-Based Solar Cells, ACS Appl. Mater. Interfaces, 2016, 8 (51), pp 35660–35667, DOI: 10.1021/acsami.6b12714.

[14] A. Ingenito et al., "Phosphorous-Doped Silicon Carbide as Front-Side Full-Area Passivating Contact for Double-Side Contacted c-Si Solar Cells," in IEEE Journal of Photovoltaics, vol. 9, no. 2, pp. 346-354, March 2019. doi: 10.1109/JPHOTOV.2018.2886234

[15] G. Nogay et al., "Crystalline Silicon Solar Cells With Coannealed Electron- and

Hole-Selective SiCxPassivating Contacts," in IEEE Journal of Photovoltaics, vol. 8, no. 6, pp. 1478-1485, Nov. 2018. doi: 10.1109/JPHOTOV.2018.2866189

# SUMMARY

Electricity consumption is increased in last twenty years. It is crucial therefore to find alternative, renewable and sustainable sources to mantain this development. Solar energy has proved to be a valid alternative to produce clean energy. The gigantic development of solar energy technology in the last twenty years has lead to a scenario in which solar energy is no more a dream or an experimental demonstration of scientific principles, but it is fully integrated in energy production. To make it comparable with other sources, prices are lowered employing mass-production and more simple technologies. One of the possible technologies available is to use crystalline silicon wafers as absorber layer in combination with ion implantation doping technique. This doping technology is inherited by integrated circuit industry.

Therefore, the context of this thesis is to explore ion implantation to simplify processing of c-Si solar cells. Indeed, the feature of this doping technique allows to speed up processing of current industrial standard named passivated emitter rear contact (PERC). Moreover, the integration of so-called carrier-selective passivating contacts with ion implantation is of great interest for future evolution of c-Si solar cell industry.

After a careful review of the state-of-the-art technology and a synopsys of ion implantation physics (Chapter 1 and 2), the research is firstly focused on homojunction, fully-implanted solar cells with P-doped BSF (Chapter 3). Given the intrinsic limit in open circuit voltage due to full-area metal contacts, ion-implanted poly-Si in combination tunnelling oxide is explored in a so-called poly-poly solar cells (Chapter 4). A deep passivation study is carried-out considering poly-Si thickness, doping level and annealing conditions. TCAD simulations were employed to understand whether it is possible to improve device performance and what are the intrinsic limits. Due to high absorption of poly-Si, poly-poly solar cells are limited in short-circuit current density and therefore an alternative front structure, keeping high open-circuit voltage, needs to be explored. Therefore, either selective front surface field with poly-Si under the contacts and lightly homojunction (Chapter 5) or silicon heterojunction front surface field (Chapter 6) are employed. These structures represent a toolbox to verify the impact of rear poly-Si layer and also to overcome short-circuit current density limit, keeping $J_{SC}$ at around 40 $mA/cm^2$.

Then, in order to employ high quality metal contacts regardless the solar cell architecture, a novel metallization method based on Ti-seeded Cu-plating is developed (Chapter 7). Aside this development, this metallization technology is tested in complete device embedding passivating contacts to prove that it is reliable and non-destructive. Finally, a novel method, based on high temperature oxidation, is developed to clean silicon wafers from surface contaminants and to allow higher open-circuit voltage due to encapsulation of contaminants in an oxide sacrificial layer (Chapter 8).

# ACKNOWLEDGEMENTS

I will never forget the trip of the last four years. I will never forget when I was working in Rome and Dr. Olindo Isabella called me discussing the possibility of pursuing a PhD. It was 17th November 2014 when I came for an interview to TUDelft in PVMD group. The first person I spoke to, aside Dr. Olindo Isabella, was prof. dr. Miro Zeman that asked me, among other things, a question I will never forget :«*If you are asked by your team to shoot four penalties, how many do you score?*». I was a bit astonished by such question and I tried, very shy, to reply :«*I will score three penalties, I won't score them all*». Then, the discussion verted on promises and expectations of one of the best PV group in the world.

That said, dear prof. dr. Miro Zeman, I did not clearly understand your winning mentality from the very beginning, but the high level of trust in PVMD group was immediately clear. Indeed, after not even one week I started my PhD, you asked me to check exams of PVBasics course. This gives an idea of how high is the trust you have in your students. You are a true leader with an important carisma that nobody can replicate. I really wish to give you my thanks for giving me this opportunity in developing myself in such great research group. During these years, I learnt not only how to fabricate solar cells, but also how to deal with new, different cultures and situations.

The trip would have been pretty short without the constant presence of Dr. Olindo Isabella. Olindo, I remember when you decided to select me for the PhD you said these words :«***I would like to run a bet with myself and with you, and I wanna win this bet!***». After four years, I think we won this bet with the fate. We grew professionally together, in 2015 you were an assistant professor and now you are the head of PVMD group. About me, I was not even capable of writing something in a decent English, now it is a little bit better. I acquired some technical, analytical and soft skills that, without you, it would have never come out of my head.

Special thanks go to the committee members that reviewed my PhD thesis and partecipated in the defense ceremony; Prof. Dr. Arthur Weeber, Prof. Dr. Jurgen Werner, Dr. Ivan Gordon, Prof. Dr. Juriaan Schmitz, Dr. Ronald Naber. It was a honour to receive feedback from such international experts like you.

Along this (not always) fantastic trip, some people are particularly important. One of them is Dr. Andrea Ingenito (O' Zi), that I should personally first thank to tell me about the PhD position that was available and then to teach all the very basic things in the laboratory. Your teaching looked like when a kid learns to go on the bike for the first times. I made a lot of mistakes whatsoever but at the end I learnt. Good luck with your career in Switzerland.

It is really important to go on a trip with the right people, otherwise you don't enjoy and you don't have fun. Dr. Guangtao Yang, you are a very important scientist, without you probably this thesis would never have been written. In 2016, c-Si team was constituted just by me and you, therefore you were guiding me to go on my bike faster than

just staying in equilibrium. During all the discussion we have, all the technical issues that happened, you were always unexpectedly calm, relaxed although your brain was working at 300 km/h. For all the help, the scientific discussion and all the saturdays and sundays we shared in the cleanroom, I thank you very much for what you did for me without expecting nothing in return. Good luck with c-Si team that now is much bigger than 2016.

I must be thankful to all the people (of the present and of the past) of PVMD group. We are a great family! Prof. Dr. Arno Smets, there is a big difference between people that are one step ahead of the others and people like you that are *three* steps ahead. Thank you for letting me stay in PVMD group within the fantastic FLAMINGOPV project in collaboration with HyEt Solar. I hope to score many goals there! Prof. Dr. Arthur Weeber, Dr. Rene van Swaaij, thank you for all the discussion, I learnt a lot from you about c-Si solar cell physics. All the members of the group should be acknowledged; Dr. Dimitris Deligiannis ("The magician"), Dr. Paula Perez Rodriguez, Dr. Rudi Santbergen, Dr. Paul Procel (Grande Capo), Dr. Hesan Ziar, Dr. Fai Tong Si, Dr. Ravi Vasudevan, Dr. Dong Zhang, Dr. Yuan Gao (one of the funniest person I have ever met), Johan Blanker, Juan Camilo Ortiz Lizcano (great officemates). Special thanks to Dr. Luana Mazzarella, thank you very much for reviewing all the articles you see in this thesis without expecting nothing in return. I should thank all the PhD students who shared the trip with me; Yifeng Zhao (the biggest boss), Manvika Singh, Can Han, Daniele Scire, Andres Calcabrini, Klaas Bakker, Nasim Rezaei, Robin Vismara (Thank you for your friendship, you are a great guy), Thierry de Vrijer, Yilei Tian, Ana Rita Bento Montes, Carlos Tibon, Yudai Yamashita, Sun Xun, dr. Silvio Pierro and Vincenzo Maccaronio. You all added that tiny little bit to make days less bitter sometimes. A super-special thanks go to Martijn Tijssen and Stefaan Heirman, without you our group is lost! The same applies for Sharmila Rattansingh (Thank you for helping me to settle here in Delft!), Ilona van der Wenden, Ellen Schwencke-Karlas and Mark Vielvoije, without your support, we can't do nothing so easily! Dr. Gregory Pandraud should be acknowledged since he taught me a lot of things, you are a freaky boss! Go St. Etienne!

Without the following people, this thesis would never exist; Yvar De Groot, Hao Ge, Gerwin Van Kuler and Guillame Le Boucher-D'Herouville, I supervised you in the technical field, but you helped me a lot with the research shown here, you are the bosses! Good luck with your future career!

Many people from else Kooi Laboratory should be acknowledged; Tom Scholtes, thank you for teaching me ion implanter secrets! I really appreciated your continuos help as well as the help from Mario Laros, Koos Van Hartingsveldt, Silvana Milosavljevic, Dr. Paolo Sberna, Dr. Aleksandar Jovic, Hitham Amin, Robert Verhoven, Johannes van Wingerden, Wim Wien and all the technicians from EKL.

This trip brought along a couple of good people I found on my way, for instance Dr. Nikolas Gaio (I tried to welcome you once in a football match, you always refused, I admire your steadiness), Dr. Cinzia Silvestri, Dr-to-be Violeta Prodanovic, Dr. Bruno Morana, Dr. Filiberto Ricciardella, Prof. Sarro, Dr. William Quiros Solano, Dr-to-be Juan Alfaro Barrantes, Boyao Zhang, Dr. Massimo Mastrangeli, Dr. Sten Vollebregt, Dr. Amir Sammak.

During this trip, other people shared with me some things and helped to make it

(more or less) joyful. Dr. Fabrizio Silvestri, you are a spin doctor! I can talk about all the possible aspects of optics, you are top-class scientist! We share a lot of memories in the last four years (I have never got so much rain here in the Netherlands like that time in Utrecht!). Dr-to-be Satoshi Malatoux, you are at the same time the most un-organized but also the most-efficient person on the Earth. Please keep this unique quality for the future! Also with you I shared a lot of things (Remember (Maybe not) the New-Years-Eve party in San Marzano?). Dr-to-be (very soon) Luca Galatro, you are one of the people I can always count on. You supervised me during my MSc thesis project and also showed me how improvised humour can cheer up a bad day. Thank you for making me discover *Il Faraone Janfranco Marziano*! You have assured a career as stand-up comedian. You are a random generator of gags.

Many other people are good friends and should be acknowledged as such. Raffaele Romano, Carmine De Martino, Annarita Petrosino, Kleoniki Rerra (and greetings to Bernard!), Nikoletta Kaberi, Margherita Vaselli, Lisan Janssen (I dont remember all the other surnames!), Riccardo Donantonio and Antonio Farace (Presidenti), Roberto "Roccia" Napoli, Uto Toshihiko, Dr. Marco Spirito (You are super-funny, full-of-energy kitesurfer!), Michele Squillante, Ghazaleh Nazarian, Valeria Napoli, Alferio La Pastina (O' Zi bell!), Emmanouela Korkakaki, Chiara Salvoni, Carminiello La Gorga, Roberta della Peruta, Ciruzzo, Franco, Vicienzo Mascolo, Ilaria Matacena, StudEnzo, Antonio Fertuso, Michele Del Mastro, Stefano Di Martino, Salvatore Forte, (Zio) Federico Marciano (Presidente).

I was lucky to have amazing flatmates as Stefano Galbano (Presidente), Davide Pollini, Vladimir Novakovic, Oskar Wallin, Gaetano Parisi, Vincenzo Mascolo, Nicolo' Ancona, Phil Chazee and Davide Moretti.

My historic friends are part of my daily life, Domenico D'antuono (Si o' pegg), Cosimo Scutiero, Teresa Longobardi, Maria Tramontano, Emilio Cesarano, Alessia Accardo, Emanuele Panella, Marika Sabini, Angelo Chierchia (Ottonero), Giuseppe Fontanella, Gaetano Winchester Esposito (great Winchester-Venoki method!), Vincenzo Venoki Tortora (Thank you so much for designing the cover!), Andrea Mauramati (Andrea Hip Hop) Alessandro Naccarato, when I come back to Angri, it is like nothing changed and we are the kids of the good times!

My brother Nicola should be always thanked, you stand by me everytime, no matter what was going on. Remember, because this is the only time I will write this, you are always right.

I shared this trip with a very special person in my life, Anna. We started the trip nearly together and all the precious memories are when we were together (Angri, Casalvelino, Aberdeen, Edinburgh, Delft, London, Leuven, Loch Lomond, Crete, Menorca, Sicily, Silvi Marina). We supported each other and only like that we kept up with rhytme of two gigantic PhD projects. You don't find a girl like you not even after 1 billion of kilometers! You are the love of my life.

Alla fine, in questa tesi voglio ringraziare mia mamma Carmela e mio padre Vincenzo che hanno messo tutto il loro amore per me e mio fratello. Questo libricino che ho pubblicato e' per voi che mi avete sopportato tutti i giorni anche quando le cose non andavano al meglio.

# LIST OF PUBLICATIONS

## JOURNAL PUBLICATIONS

1. **G. Limodio**, G. Yang, H. Ge, P. Procel, Y. De Groot, L. Mazzarella, O. Isabella, M. Zeman, Front and rear contact Si solar cells combining high and low thermal budget Si passivating contacts, Solar Energy Materials and Solar Cells, Volume 194, 2019, Pages 28-35, https://doi.org/10.1016/j.solmat.2019.01.039

2. **G. Limodio**, Y. De Groot, G. Van Kuler, L. Mazzarella, Y. Zhao, P. Procel, G. Yang, O. Isabella and M. Zeman, Copper plating metallization with alternative seed layers for c-Si solar cells embedding carrier-selective passivating contacts, IEEE Journal of Photovoltaics, 2019, Under Review.

3. **G. Limodio**, G. Yang, Y. De Groot, P. Procel, L. Mazzarella, A. W. Weeber, O. Isabella, M. Zeman, Implantation-based passivating contacts for crystalline silicon front/rear contacted solar cells, Progress in Photovoltaics, 2019, Under Review.

4. **G. Limodio**, G. D'Herouville, L. Mazzarella, Y. Zhang, G. Yang, O. Isabella, M. Zeman, High temperature oxidation pre-treatment of textured c-Si wafers passivated by a-Si:H, Material science semiconductor processing, Volume 97, 2019, Pages 67-70, https://doi.org/10.1016/j.mssp.2019.03.008.

5. A. Ingenito, **G. Limodio**, P. Procel, G. Yang, H. Dijkslag, O, Isabella, and M, Zeman, (2017), Silicon Solar Cell Architecture with Front Selective and Rear Full Area Ion-Implanted Passivating Contacts. Sol. RRL, 1: n/a, 1700040. doi:10.1002/solr.201700040.

## CONFERENCE CONTRIBUTIONS

1. **G. Limodio**, G. Yang, P. Procel, A. Weeber, O. Isabella, M. Zeman, "Application of carrier-selective contacts in c-Si front/back contacted (FBC) and IBC solar cells with different thermal budget", 2018 IEEE 7th World Conference on Photovoltaic Energy Conversion (WCPEC) (A Joint Conference of 45th IEEE PVSC, 28th PVSEC and 34th EU PVSEC), Waikoloa Village, HI, 2018, pp. 3908-3913. doi: 10.1109/PVSC.2018.8548142

2. Poster presentation @ SiliconPV 2018 **G.Limodio**, G. Yang, P. Procel, O. Isabella, M. Zeman, Carrier-Selective Contacts With Different Thermal Budget For Front / Back Contacted (FBC) Solar Cells, Lausanne Switzerland.

3. Poster presentation @ SiliconPV; **G.Limodio**, G. Yang, P. Procel, Y. De Groot, A.W. Weeber, O. Isabella, M. Zeman 'Implantation-based carrier-selective contacts in c-Si solar cells', Freiburg, Germany, 2017

4. Poster presentation @ EUPVSEC; **G.Limodio**, G. Yang, P. Procel, H. Ge, Y. De Groot, A.W. Weeber, O. Isabella, M. Zeman 'Passivated rear and front contacts (PeRFeCT) solar cells: the poly-poly and the hybrid approaches', Amsterdam, The Netherlands, 2017.

5. Oral presentation @ Material Research Society Fall Meeting; **G.Limodio**, G. Yang, P. Procel, H. Ge, Y. De Groot, A. W. Weeber, O. Isabella, M. Zeman 'Ion-implanted carrier-selective passivating contacts for high-efficiency c-Si solar cells' Fall Meeting, Boston, USA, 2017, **Awarded with the best student paper award**.

# CURRICULUM VITÆ

Gianluca Limodio was born in Scafati (Salerno), Italy on 09-02-1990. In 2011, he received the bachelor degree cum laude from University of Napoli Federico II in Electronic Engineering with a thesis on bias-stress of organic field-effect transistors under the supervision of Prof. Ruggero Vaglio. In 2013, he moved to Delft University of Technology to develop his master thesis on load-pull microwave measurement setup characterization and optimization under the supervision of Dr. Marco Spirito and Dr. Luca Galatro. In July 2014, he received cum laude the master degree in Electronic engineering from University of Napoli Federico II. After a brief experience in a consulting company as test engineer, he moved to Delft to purse a PhD degree in Solar Energy within the Advanced Dutch Energy Material (ADEM) project. His work has been awarded with "Best student award" at Material Research Society Conference 2017 in Boston, USA. His interests cover a broad range of topics as football (Both playing and watching), music, history, cooking and singing (Just for fun, not professionally nor semi-professionally).