Flex Power Grid Lab

Modeling & Validation

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Supervisor:
Dr. dipl.-ing. Marjan Popov
Associate Professor

M.Sc. Thesis in Sustainable Energy Technology

Faculty of Applied Sciences
Specialization in Electrical Power Engineering

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Challenge the future

……
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This project has been carried out at Delft University of Technology and DNV KEMA.

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Peter Vaessen	Dr. Erik de Jong
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Abstract

The increasing penetration of dispersed generation changes the way in which distribution grids are comprised. The impact of the introduction of grid-connected distributed energy resources is expected to receive growing attention in the near future. Power electronic equipment is now indispensable part of the electricity generation and distribution; however apart from its benefits, it may affect the grid adversely as well. Power quality and reliability are the challenges that grid operators face, because of fluctuating loads and penetration of decentralized electricity generation. The use of power electronics has the potential to enhance the energy management and enables grid operators to make smarter use of their grid.

The Flex Power Grid Lab (FPGL) in Arnhem provides an ideal testing and research environment for advanced power electronics. Businesses and universities can make use of this excellent facility to study how locally generated energy, such as wind turbines, solar cells, CHP plants, can be safely integrated into the grid. The lab facility is capable of generating both static and dynamic voltage phenomena and creating test conditions, such as harmonic distortion, voltage dips, frequency and voltage fluctuations. As a result, equipment involved in decentralized power generation can be tested under “bad grid” conditions, prior to its actual connection to it.

The intent of this Master Thesis is to model the FPGL using certain software in order to ultimately be able to predict the performance of the lab. MATLAB/Simulink environment is used for the purposes of the project. The modeling starts from the 50kV substation in Kattenberg. A transformer steps down the voltage to 10.5kV. FPGL along with other labs of DNV KEMA is connected to the 10.5kV bus-bar, which is located in the Business Park, Arnhem. Two three-phase and three single-phase temperature dependent transformer models have been developed. Special attention is paid to the modeling of the grid-connected 4Q, 1MVA, AC/DC – DC/AC converter, which consists of two three-level neutral-point clamped PWM converters. Different control scheme is applied to each of these converters. The grid-side converter is controlled in the rotational reference frame, using proportional-integral (PI) controllers with ultimate goal to keep the DC-link voltage stable. Park transformation (dq0) is necessary to transfer the system to the rotational frame. In contrast, the load-side converter is controlled in the stationary reference frame using proportional-resonant controllers (PR). This innovative control strategy stabilizes the plant by state-feedback, while ten available resonant controllers ensure zero steady-state error for up to nine harmonics. Both control schemes are developed in the z-domain to take into account the effect of the Digital Signal Processor. Ultimately, the model is validated through several lab tests.

Key words: power quality, three-level converter, resonant controller, vector control, dq transformation, Park, Simulink, validation

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Abbreviations

FPGL	Flex Power Grid Laboratory
4Q	Four-Quadrant
MV	Medium Voltage
DC (dc)	Direct Current
AC (ac)	Alternating Current
FACTS	Flexible AC Transmission System
VSC	Voltage-Sourced Converter
IGBT	Insulated-Gate Bipolar Transistor
PWM	Pulse Width Modulation
PLL	Phase Locked Loop
EMC	Electro-Magnetic Compatibility
EMF	Electromotive Force
NPC	Neutral Point Clamped
DSP	Digital Signal Processor
PI	Proportional-Integral
PR	Proportional-Resonant
Dq0	Direct-quadrature zero
ZOH	Zero Order Hold
FF	Feed Forward
CFF	Command Feed Forward
DFF	Disturbance Feed Forward
ADC	Analog-to-Digital Converter
AFE	Active Front End
PCC	Point of Common Coupling
LTI	Linear Time Invariant System
THD	Total Harmonic Distortion
HIL	Hardware in the Loop

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Chapter 1 : Introduction

1.1 Background

In the 20th century the energy demand increased drastically. Due to convenience and low prices, fossil fuels became the main source of energy. Nevertheless, over the years the price of oil and the environment pollution have been increased considerably. These facts as well as the increased concern about the high-rate of fossil fuel diminishing that puts the energy security in jeopardy, led to putting pressure on the society to come up with sustainable solutions. The last decade, the contribution of renewable energy sources and distributed energy resources into the electrical generation energy mix is increasing rapidly. Tomorrow's distribution networks should be able to support power flow, not only from a centralized generation unit through the transmission grid towards consumers, but generation and energy storage devices connected all along the network as well. As a result, a more complex network is arising, where voltage control and satisfying power quality become at least challenging. On the one hand, network operators must ensure that power quality is maintained or even improved when smart grid components are connected. On the other hand, manufacturers must be able to demonstrate that their products comply with the requirements that the operators set, or that their product is able to withstand potential severe disturbances.

To fill this gap between the manufacturers and the grid operators along with research purposes, in 2005 a foundation – known as the EMVT (ElektroMagnetische VermogensTechniek) Laboratory Foundation – was established. The foundation is the result of a public-private partnership between DNV KEMA, the Energy Research Centre of the Netherlands (ECN) and the Dutch Technical Universities of Eindhoven and Delft [1], [2]. The FPGL is the outcome of this foundation and it is dedicated to testing smart grid components at real distribution voltages and power levels. It comprises a realistic and flexible environment, where "bad grid" conditions can be emulated. More specifically, unbalances, phase jumps, harmonic distortion and other transients can be emulated in this lab. Within this environment, components based on advanced and sophisticated technologies can be de-risked before they are connected to the grid. A sustainable grid in the foreseeable future will need to be clean, energy efficient and secure. The FPGL contributes to the development of such a grid through research, innovation and testing.

1.2 Problem definition & objectives of the study

The FPGL is equipped with a 4-quadrant, 1MVA power converter, which has direct connection to the public grid. The power converter consists of a three-level IGBT Active Front End (AFE) as well as the load-side three-level IGBT converter with an adjustable output voltage up to 3.3kV. The specifications of the lab confirm the huge range of applications and tests that may be carried out as well as the wide range of R&D projects that may be hosted in this facility. However, the first step of a test

procedure is to decide whether the lab is indeed suitable to perform a particular test. Of course there are limitations because of the physical properties of the lab and its protection system. Hence, in order to avoid time-consuming analytical methods and calculations to evaluate the feasibility of the customers' requests, it is preferable to develop an equivalent model of the lab using certain software. Apart from convenience, an equivalent simulation tool will provide a better overview of the entire system before the actual test run. As a result, possible failures, trips or other unexpected events can easily be predicted and avoided.

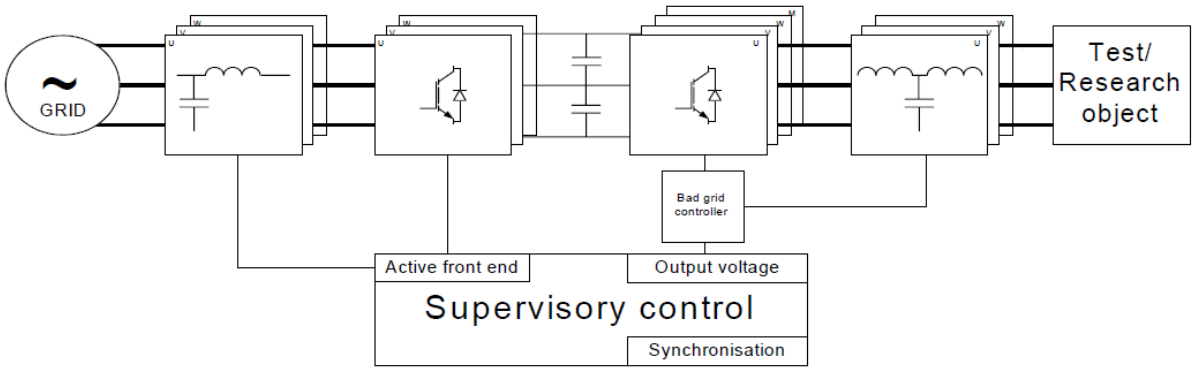


Figure 1-1 Equivalent circuit of the 4Q, DC-75Hz, 3.3kV, 1MVA power converter [1]

Figure 1-1 presents an overview of the lab equipment that is intended to be modeled and in addition to these components, two three-phase and three single-phase transformers will be included in the model as part of the equipment. The complete single-line diagram of the lab is attached in APPENDIX A.

Within this thesis the FPGL will be modeled using MATLAB/Simulink software. Special focus will be given on the modeling and control of the power converters, which are the heart of the lab and the ones that make it unique. The AFE model has to be controlled in order to keep the DC-link voltage at the required level. The model of the output converter has to be able first and foremost to perform basic system stability studies. This can be achieved by plotting the zeros and the poles of the system's transfer function and its step response. Moreover, it has to produce the required grid conditions that the user asks for. In particular, the integrated scheme must be able to actively control and superimpose higher harmonic frequencies onto the output voltage, if the test requires this. Additionally, voltage unbalances, as well as dynamic voltage phenomena such as dynamic system voltage variations, rapid voltage variations, balanced or unbalanced voltage dips and short interruptions or an arbitrary combination thereof, are considered within the objectives of the control strategy to be implemented and explained in the present thesis work. Moreover, the experimental validation of the proposed model is one of the major issues to be achieved through this Master Project.

1.3 Contribution of the Thesis work

The contribution of this research work reported in the present thesis can be seen from two different perspectives. From the model development and power electronics point of view, two different converter control strategies are presented in detail. The load-side converter is controlled in the

stationary reference frame with PR controllers, whereas the grid-side converter is controlled using a PI controller in the rotating reference frame. The two control schemes are compared to each other, their advantages and drawbacks are presented as well, and mainly their detailed development in a graphical interface (MATLAB/Simulink) is shown. Moreover, it is worth noting that the model development in both cases has been done in discrete time domain in order to compile and run it on a Digital Signal Processor (DSP) platform. From the power system point of view, a useful tool has been built, which promotes the development of decentralized power generation and generally the research around the field of intelligent electricity networks. In particular, power quality issues are considered as one of the main obstacles that hold up the integration of distributed energy resources in the grid. Utility grid connected equipment and especially power electronic components are sensitive to various abnormalities in the electric supply [3]. This model along with the FPGL itself provides a great facility to elaborate on such issues and through simulation and emulation of other power electronic based devices ensures acceptable disturbances from the grid to the object-under-test and vice versa.

Moreover, the equivalent model of the FPGL comprises a great starting point for further study in this field. This model can be the basis of new R&D projects related to system stability, power quality, static and dynamic phenomena of the grid. In other words, its contribution in the academic and business world is the presentation of a specific tool, which will facilitate studies related to grid-connected components and their interaction with the grid.

Last but not least, the scientific approach of the thesis becomes complete through the inclusion of the validation of the model. The final part of the thesis is the verification of the results of the Simulink-based lab with actual measurements from the FPGL.

1.4 Outline of the Thesis

The thesis starts with a brief presentation and comparison among the possible computer programs that could potentially be used for the purposes of the FPGL equivalent representation. After deliberating on this subject, which is certainly very crucial for a successful outcome, and selecting the most suitable software, the transformers are modeled in Chapter 3. Chapter 4 includes the rest components of the lab, which need to be taken into account in the modeling procedure and the following chapter is focused on the back-to-back converter. It includes all the necessary background regarding the working principles of three-level IGBT converters, as well as investigates the different control schemes that can be used. The converter modeling is followed by Chapter 6, where the model is verified through several simulations and scenarios. Chapter 7 is the last part of this report and includes conclusions and recommendations for future work.

Chapter 2 : Software selection

2.1 Criteria & possible options

The first task of this project is the optimal software selection. This task should not be underestimated; on the contrary, it comprises a strong basis for a successful outcome. The software should meet the following criteria in order to achieve satisfactory results:

- Integrated approach:
  All the components and systems have to be modeled using one single program. The software to be selected should present sufficient libraries for power electronic components, transformers, cables and anything else included in the lab. It should also cover both three- and single- phase systems, or even provide the designer with the possibility to cause changes to each phase separately in a three-phase system, considering that unbalances are also in the operating scope of the lab. In a nutshell, the modeling of the lab has to be done without building any interfaces consisting of two or more programs.

- Time scale:
  Suitable accuracy at the right time scale is considered also one of the main features of the model. Both transient and steady-state analyses are considered significant for the use of the model. Ultimately, it is desired to be able to perform real time simulations. Hence, minimum time steps and processing times are factors to be considered.

- User friendliness:
  The ease of use for both the development and the use of the model once it has been developed is also a desired feature. However its priority is set lower compared to the other criteria.

The following table presents all the objective requirements that the model should fulfill with respect to each component of the lab:

Converter
- Ratings (V/I/f/P)
- Harmonic generation and analysis (FFT)
- Time scale: low enough to simulate the power system dynamics (<1ms)
Transformers
- Tap positions
- Ratings
- Possible influence on harmonics
- Saturation
- Temperature effect (optionally)
Loads, cables and grid line
- Reconfigurable loads
- Cable impedances
- Limits (voltage and current)
- Temperature effect (optionally)

Table 2-1 Objective requirements per component of the lab that should be modeled

The next table includes the list of the programs that had been considered as possible options.

Software options
RSCAD
PowerFactory
PSS/E
PSCAD/EMTDC
ATP/EMTP
MATLAB/Simulink

Table 2-2 Possible software options

Each of them has several advantages and drawbacks as well as covers different modeling aspects. These facts have to be taken into consideration before the final selection.

2.2 Comparison of the different options

RSCAD is a user friendly platform and includes several modules in its library, so that real-time simulations can be created, executed, controlled and analyzed without the use of third party products [4]. It is a power system simulator that solves electromagnetic transient simulations in real-time with the assistance of the RTDS (Real-Time Digital Simulator) hardware. The system is used for high speed simulations, closed-loop testing of protection and control equipment and hardware in the loop applications. However, RSCAD does not support offline simulation, as long as it is dedicated to real time simulations. RSCAD – RTDS is designed specifically to simulate electrical power systems and to test physical equipment, such as control and protection devices in real-time [5].

PowerFactory and PSS/E are two similar programs. They include many important features that the FPGL modeling requires, but they are developed, dedicated and commercially available mainly for

different purposes. Analysis and optimization of transmission and distribution complex networks and traditional power flow analysis are their main operations. Specifically, PSS/E is mainly focused in transmission networks and even the analysis of a distribution network would be a challenge. The flexibility of both is limited when the user needs to include some single phase components in a three-phase power system. This is a huge disadvantage for the FPGL modeling, providing that three similar single-phase transformers for three-phase applications are among the equipment of the lab. Moreover, PowerFactory library does have some simple power electronic devices (diodes/thyristors), compared to PSS/E that does not. In PowerFactory additional functions required, which are not included in the built-in model- and macros-library, can be created using the DSL language. It allows flexible definition of macros, functions and models. However, this flexible definition may limit the flexibility of the entire model [5], [6].

PSCAD is a time domain simulation program for multi-phase power systems and control networks. It is mainly focused on transient studies of the power systems and it is a very convenient tool as it has a rich library with precise models, letting the user develop models graphically and in a very user friendly environment. The library of models supports most AC and DC of power plant components and controls, in such way that FACTS, custom power and HVDC systems can be modeled with speed and precision [7]. The library includes frequency dependent transmission lines and cables, transformers (classical model with saturation), various machines (synchronous, asynchronous, DC), various turbines (hydro, steam, wind), converters & FACTS, drive & control blocks, relays [8]. Both ready models in the library and user defined models are available [9]. EMTDC serves as the electromagnetic transients' solution engine for PSCAD. EMTDC (which stands for Electromagnetic Transients including DC) represents and solves differential equations (for both electromagnetic and electromechanical systems) in the time domain [10]. ATP is another similar EMTP-type program for transient analysis. It could also be considered as possible option for this project's purposes, because it covers most of the requirements.

MATLAB/Simulink accompanied with the SimPowerSystem Toolbox is certainly another promising solution. It is a great tool for every engineer, and meets the criteria, that have been set up, in a high level. More specifically, using Simulink it is possible to develop both single and three-phase systems, using the rich library of electrical components in a user-friendly graphical environment. Both steady-state and transient simulations are supported. Simulink is considered as one of the most powerful programs for dynamics analysis. Algebraic loops and large number of warnings and errors are sometimes unfriendly to the user and difficult for them to identify and solve. Certainly this is not a problem of Simulink exclusively. This may be considered as a disadvantage, but not a setback to choose Simulink. Great advantage of Simulink is its integration with xPC Target toolbox [11] and PLECS blockset [12] that offer the possibility for further real-time and thermal simulations respectively.

To sum up, considering all the information stated above, PSCAD, ATP/EMTP and MATLAB/Simulink are the most suitable solutions. However, Simulink offers more possibilities for further work, such as real time and thermal simulations. The FPGL model will therefore be developed in Simulink environment.

Chapter 3 : Transformers

3.1 Introduction

The FPGL has three transformer sets. The first - referred to as TR3/T3 - is used exclusively for the grid line connection to the lab's equipment. The second - referred to as TR2/T2 - is a set of three single phase 600kVA transformers that allow the available 10kV, 50Hz voltage to be transformed from 400V up to 4kV or alternatively these transformers can be used as output transformer for the converter, extending the converter's full-power range from 400V to 12.5kV. The last one - referred to as TR3/T4 - is a three-phase 1.25 MVA transformer. This can be used as output transformer for the converter, extending the converter's full-power range from 400V to 24kV. Because of the broad voltage range that the transformers provide, they are indispensable part of the lab, as they extend the range of the applications and the tests that can be carried out.

3.2 Theoretical background

Some theoretical information, prior to the modeling of the transformers, would be useful as it will make the calculations and assumptions have been made in this part clearer.

The transformers have durable construction, high efficiency and no moving parts. They consist of two or more windings and a common ferromagnetic core. The windings normally are not electrically connected to each other, but the only connection they develop is caused because of the magnetic field inside the core. The core is characterized by its cross-section S, its total length l_μ and the magnetic permeability μ. The permeability behavior of the core material is non-linear and determines the relation between flux density B and the field strength H; $B = f(H)$.

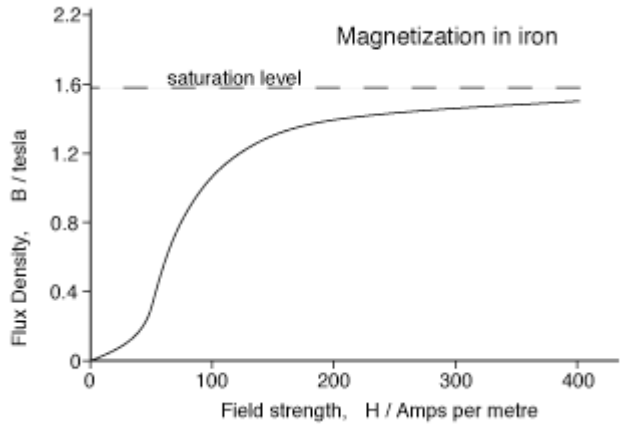


Figure 3-1 Iron magnetizing curve

As the curve shows, in the beginning a slight increase of the field strength H causes a large increase of the flux density. This is the unsaturated region. From a certain point and on, further increase of H causes relatively smaller increase in B. Here is the saturation knee. The saturated region is the region where the curve tends to become horizontal. The ferromagnetic materials offer the advantage that for a certain value of H, it is produced multiple magnetic flux inside them, compared to that flux which would be produced in the air.

**Assumption:* the saturation of the transformers will not be integrated in the model. Lack of information such as the hysteresis curve does not allow taking saturation into account. In reality, the transformers of the lab operate in the linear region and hence accuracy will not be significantly affected by neglecting saturation.

The transformers' operation is based on the Ampere's Law according to which an alternating current produces magnetic field and on the Faraday's Law, according to which a magnetic field interacts with an electric circuit to produce electromotive force (EMF). In other words, an induced EMF is created by a changing magnetic flux: $= -N\frac{d\varphi}{dt}$.

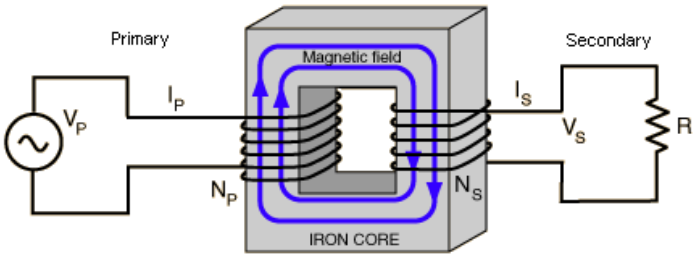


Figure 3-2 Transformer with a common iron core

When an alternating voltage is applied to the primary coil, the back EMF generated by the primary is given by:

$$E_1 = -N_1\frac{d\varphi}{dt} \qquad 3\text{-}1$$

Although there is a slight loss to fringe fields, the magnetic field is almost totally contained in the ferromagnetic core. The induced voltage in the secondary coil is also given by the Faraday's Law:

$$E_2 = -N_2\frac{d\varphi}{dt} \qquad 3\text{-}2$$

The rate of change of flux is the same in both coils, so the number of turns determines the secondary voltage. The sinusoidal flux ϕ produced by the primary can be represented as:

$$\varphi = \varphi_m \sin(\omega t) \qquad 3\text{-}3$$

The instantaneous EMF E_1 induced in the primary is:

$$E_1 = -N_1\frac{d\varphi}{dt} = -N_1\frac{d}{dt}(\varphi_m \sin(\omega t)) = -\omega N_1 \varphi_m \cos(\omega t) \\ = 2\pi f N_1 \varphi_m \sin(\omega t - 90) \qquad 3\text{-}4$$

Thus the maximum value of the primary EMF is given by:

$$E_{m1} = 2\pi f N_1 \varphi_m \quad 3\text{-}5$$

Dividing by $\sqrt{2}$, the rms value is given by:

$$E_1 = 4.44 f N_1 \varphi_m \quad 3\text{-}6$$

Similarly for the secondary:

$$E_2 = 4.44 f N_2 \varphi_m \quad 3\text{-}7$$

For further theoretical information you can refer to [13] and [14].

3.3 Losses

In contrast to an ideal transformer, the output power of which is equal to the input power, a practical transformer has losses, which can be classified in the following categories:

- Iron losses:
  Since the iron core is subjected to alternating flux, there occurs eddy current and hysteresis loss in it. These two losses together are known as iron losses or core losses. The iron losses depend upon the supply frequency, maximum flux density in the core, volume of the core etc. It may be noted that magnitude of iron losses is quite small in a practical transformer [13].
- Winding resistance:
  Since the windings consist of copper conductors, it immediately follows that both primary and secondary will have winding resistance. The primary resistance R1 and secondary resistance R2 act in series with the respective windings, as shown in the figure below. When current flows through the windings, there will be power loss as well as voltage drop [13].

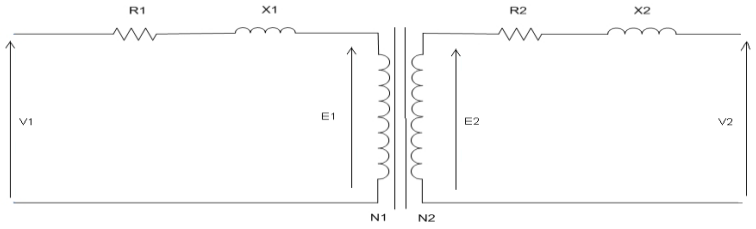


Figure 3-3 Winding resistance and reactance in a practical transformer

- Leakage reactance:
  Both primary and secondary currents produce flux. The flux ϕ which links both the windings is the useful flux and is called mutual flux. However, primary current would produce some flux $\phi_{\sigma 1}$, which would not link the secondary winding. Similarly, secondary current would produce some flux $\phi_{\sigma 2}$ that would not link the primary winding. The flux such as $\phi_{\sigma 1}$ or $\phi_{\sigma 2}$, which links only one winding, is called leakage flux. The effect of primary leakage flux $\phi_{\sigma 1}$ is to introduce an inductive reactance X1 in series with the primary winding. Similarly, the secondary leakage flux $\phi_{\sigma 2}$ introduces an inductive reactance X2 in series with the secondary winding. There will be no

power loss due to leakage reactance. However, the presence of leakage reactance in the windings changes the power factor as well as there is voltage loss due to I·X drop [13].

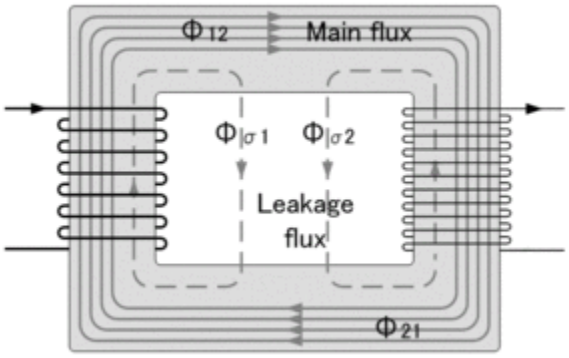


Figure 3-4 Leakage reactances

Figure 3-5 depicts the transformer's equivalent circuit.

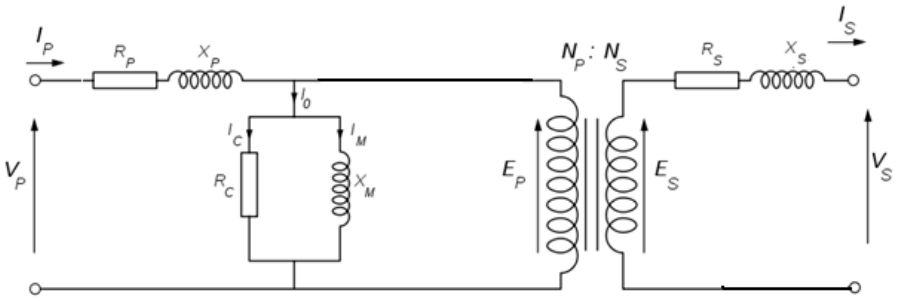


Figure 3-5 Practical transformer equivalent circuit

3.4 Skin effect

Considering the use of the FPGL, it is worth mentioning some information regarding the skin effect in the copper windings. According to the skin effect, the R and L of the copper windings are frequency dependent. The FPGL is capable of producing harmonics up to 2.4 kHz. Thus, it is required to examine whether the skin effect should be taken into account or not.

Let us consider the single copper conductor shown in Figure 3-6 (a), which is carrying a time-varying current i(t). This current generates the magnetic fields shown in the same figure, and they in turn generate the eddy currents illustrated in (b). These eddy currents flow in the opposite direction to the applied current i(t) in the interior of the wire and thus tend to shield the interior of the conductor from the applied current and resulting magnetic field. As a result, the total current density is largest at the surface of the conductor, and it decays exponentially with distance into the interior of the conductor as shown in (c) [15].

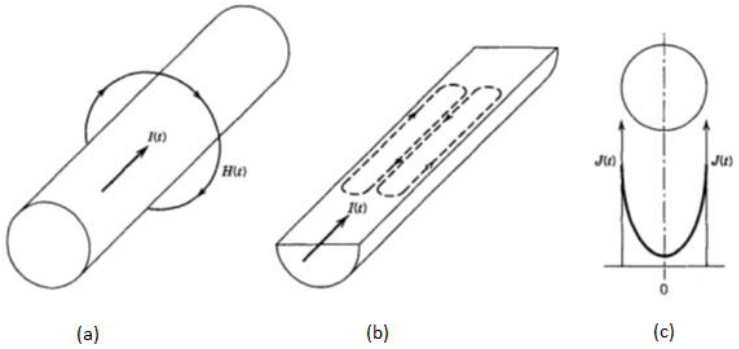


Figure 3-6 Isolated copper conductor carrying (a) a current i(t), (b) eddy currents generated by the resulting magnetic field and (c) the consequences of the skin effect on the current distribution [12]

The characteristic decay length is the skin depth given by:

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} \qquad 3\text{-}8$$

Where:
μ: magnetic permeability
σ: electrical conductivity
Table 3-1 shows the skin depth in copper at several different frequencies at a temperature of 100°C.

Frequency	50 Hz	5 kHz	20 kHz	500 kHz
δ	10.6 mm	1.06 mm	0.53 mm	0.106 mm

Table 3-1 Skin depth of copper at 100°C at several frequencies [15]

Considering the fact that the lab is a testing center and the transformers are never used in continuous operation, it is unlikely to reach 100°C. From several tests up to now, it can be assumed that the temperature is almost never higher than 50°C. Moreover the bandwidth of the converter is 0-2400Hz. It easily deduced that the skin depth will never become lower than 1.53mm, which corresponds to 2400 Hz and 100°C (for lower temperatures will be even higher). The thickest conductor of the lab has cross section 185mm^2, hence 15mm diameter, which is of the same order of magnitude of the estimated skin depth. As a result, the skin depth is high enough and hence it is considered negligible.

There have been developed several methods by the manufacturers to overcome the skin effect. The solution to this problem is to use conductors with cross-sectional dimensions on the order of the skin depth in size. If d is the diameter of a round conductor or the thickness of a rectangular conductor, calculations have shown that ideally when d≤ 2δ, the consequences of the skin effect can be neglected. Such considerations have led to the development of special conductor arrangements for high-frequency applications. These conductor arrangements include Litz wire, and the use of thin foil windings [15]. The conductor may be composed of a single round wire or it may be a special multi-stranded conductor. This is the so called Litz wire in which each strand has a diameter of the order of a few hundred microns or less [15]. The second solution is the thin foil windings. Figure 3-7 illustrates the Siemens Geafol transformer, which is a dry type transformer with aluminum windings. This particular transformer, although it is not the one of the FPGL, it is used as an example in this report. The transformers of the FPGL are custom-made transformers and due to fact that they are used for

high-frequency applications, they are constructed in the same way (with only difference that the windings are made by copper). The thin foil windings, likewise the steel lamination of the core limit the eddy currents and consequently the skin effect. Hence, this is an additional reason which strengthens the assumption of ignoring the skin effect, as the skin depth will be large enough, even at 2400Hz.

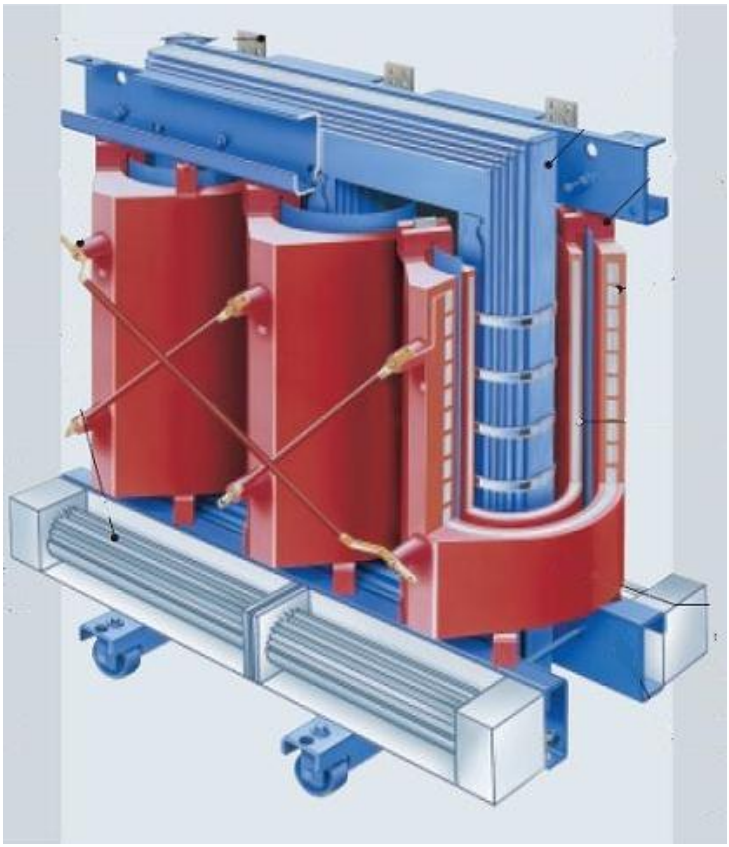


Figure 3-7 Siemens GEAFOL transformer. The thin foils at the HV and LV windings are shown (similar to FPGL transformers)

3.5 Calculations

In order to determine the required transformers' specifications, all the calculations are mainly based on the witness tests that have been carried out right after their construction by the manufacturer. IEC 60076 [16] is the relevant international standard for the power transformers, according to which the witness reports were published. Hence, this will be the guide for the calculations. The per-unit system will make the calculations easier for the reader to understand and the model more generic. Simulink supports per unit inputs.

- DC Resistance Measurement

Measurements of dc resistance (R) are of fundamental importance because they are used in the calculation of the winding conductor losses I^2R. The measurements are taken at known temperatures and a temperature correction procedure shall be followed, so that the conductor losses are realistic. The measurement of power transformer winding resistance is normally done using the voltmeter-ammeter method or using a ratio metric method to display the voltage-current ratio directly. A

circuit for the measurement of winding resistance is shown in Figure 3-8. A dc source is used to establish the flow of steady direct current in the transformer winding to be measured.

$$R_{meas} = R_{wind} + \frac{L_{wind}}{I}\frac{dI}{dt} \quad 3\text{-}9$$

After the R-L transient has subsided, simultaneous readings are taken of the voltage across the winding and the current through the winding. The resistance of the winding is determined from these readings based on Ohm's law.

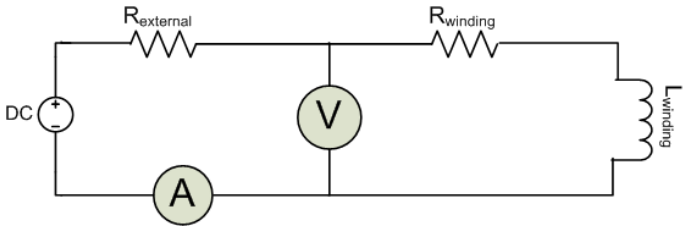


Figure 3-8 Setup of the circuit for measuring winding dc resistance

- Load Loss Test

With the load loss or short circuit test, the calculation of the windings' impedances is done. Load losses are normally measured by connecting one winding, usually the low-voltage winding, to a short circuit and connecting the other winding, usually the high-voltage winding, to an AC source. The measurements shall be carried out at rated frequency and other possible windings (in the case of 3 or more winding transformer) shall be left open-circuited. The figure below illustrates the test setup.

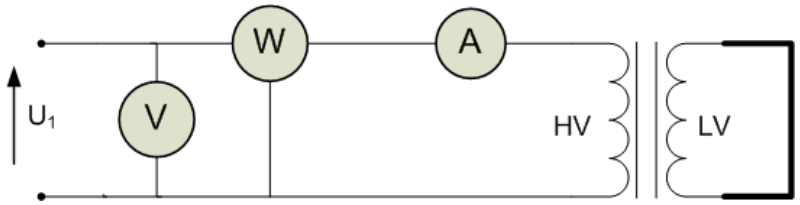


Figure 3-9 Test setup for load loss measurement [17]

According to IEC 60076-1, the supplied current should be equal to the relevant rated current (tapping current), but shall not be less than 50% thereof. Variable low voltage is applied to the primary side, which is gradually raised till the current becomes the rated (or lower, but no lower than 50% or the rated). In the case of the FPGL transformers all the tests have been carried out at 50% of the rated current. However, the provided values of load loss have already been multiplied with the square of the ratio of the rated current to test current (for 50% the multiplication factor is 4). The measurements shall be performed quickly so that temperature rises do not cause significant errors. Having obtained the load loss values at ambient temperature, the following temperature correction procedure shall be followed, as described in the standards [16]:

$$R_2 = R_1 \frac{235 + \theta_2}{235 + \theta_1} \quad 3\text{-}10$$

$$P_{a2} = P_2 - \sum I^2 R_2 \quad 3\text{-}11$$

Where:

$\sum I^2 R_2$ is the sum of the dc resistive losses in all windings at rated current.

Index 1 refers to measurement of the ''cold winding resistance''.

Index 2 indicated conditions during measurement of load loss.
I is the rated tapping current.
P_a refers to additional loss.
θ winding temperature in ^oC

Next the winding resistance, the additional loss and the whole load loss are calculated at reference temperature θ_r.

$$R_r = R_1 \frac{235 + \theta_r}{235 + \theta_1} \quad 3\text{-}12$$

$$P_{ar} = P_{a2} \frac{235 + \theta_2}{235 + \theta_r} \quad 3\text{-}13$$

$$P_r = \sum I^2 R_r + P_{ar} \quad 3\text{-}14$$

The witness test reports include temperature correction to 75^{o}C. However, this is a common temperature that the windings of a power transformer can reach under continuous operation, i.e. in a substation. The transformers of the FPGL are parts of testing facility and hence it is assumed that this temperature is never reached, as they are not used continuously. For the final model a temperature correction to 35-50^{o}C will be used. The temperature can be roughly predicted per study case; the model gives the chance to the user to modify the temperature according to the needs of every test.

Under short-circuit conditions input power is almost entirely loss on the copper windings. This is because iron loss in the core is negligibly small since the V_{SC} is very small. Thus, the equivalent setup of the load loss test becomes as follows:

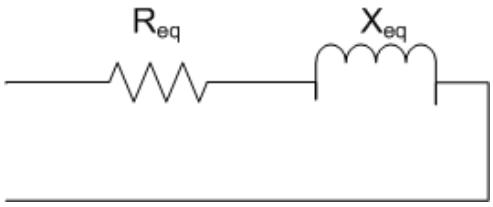


Figure 3-10 Equivalent circuit for short-circuit test

The following equations (3-15, 3-16, 3-17) are easily deduced from the equivalent circuit, and the lumped resistance and reactance can be calculated.

**Assumption:* in the Simulink model the impedances are considered to be equally distributed in the two windings through which the power is transferred. On a three-winding transformer, such as the TR3/T4, the measurements are performed on the three different two-winding combinations. The results are re-calculated, allocating impedances and losses to individual windings, in the same manner as it is done in the two-winding transformers.

$$Z_{eq} = \frac{U_m}{I_m} \quad 3\text{-}15$$

$$R_{eq} = \frac{P_r}{I_{1N}^2} \quad 3\text{-}16$$

$$X_{eq} = \sqrt{Z_{eq}^2 - R_{eq}^2} \quad 3\text{-}17$$

Additionally, it is important to point that due to the fact that the FPGL is capable of generating harmonics of higher order, it is needed to include the frequency dependency of the inductance. Thus, the inductance - and not the reactance - is given as input in the model.

- No-load Loss Test

This test is conducted to determine the iron losses (or core losses) and parameters Rc and Xm of the transformer model. In this test, the rated voltage is applied to the primary (usually low-voltage winding), while the secondary is left open-circuited. The applied primary voltage U_N is measured by the voltmeter, the no-load current I_o by ammeter and no-load input power P_o by wattmeter. As the normal rated voltage is applied to the primary, therefore, normal iron losses will occur in the transformer core. Hence wattmeter will record the iron losses and small copper loss in the primary. Since no-load current is very small (usually 2-10 % of rated current), Cu losses in the primary under no-load condition are negligible as compared with iron losses. Hence, the wattmeter reading practically gives the iron losses in the transformer [13].

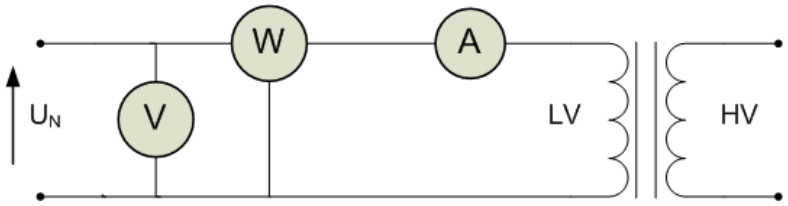


Figure 3-11 Test setup for no-load loss measurement [17]

The no-load losses shall not be corrected for any effect of temperature [16].

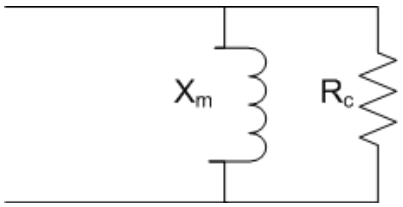


Figure 3-12 Equivalent circuit for open-circuit test

Using the following formulas, which result from the equivalent circuit, it is possible to calculate the magnetizing branch of the transformer.

$$R_c = \frac{U_N^2}{P_o} \quad 3\text{-}18$$

$$Z_h = \frac{U_N}{I_o} \quad 3\text{-}19$$

$$X_m = \frac{R_c Z_h}{\sqrt{R_c^2 - Z_h^2}} \qquad 3\text{-}20$$

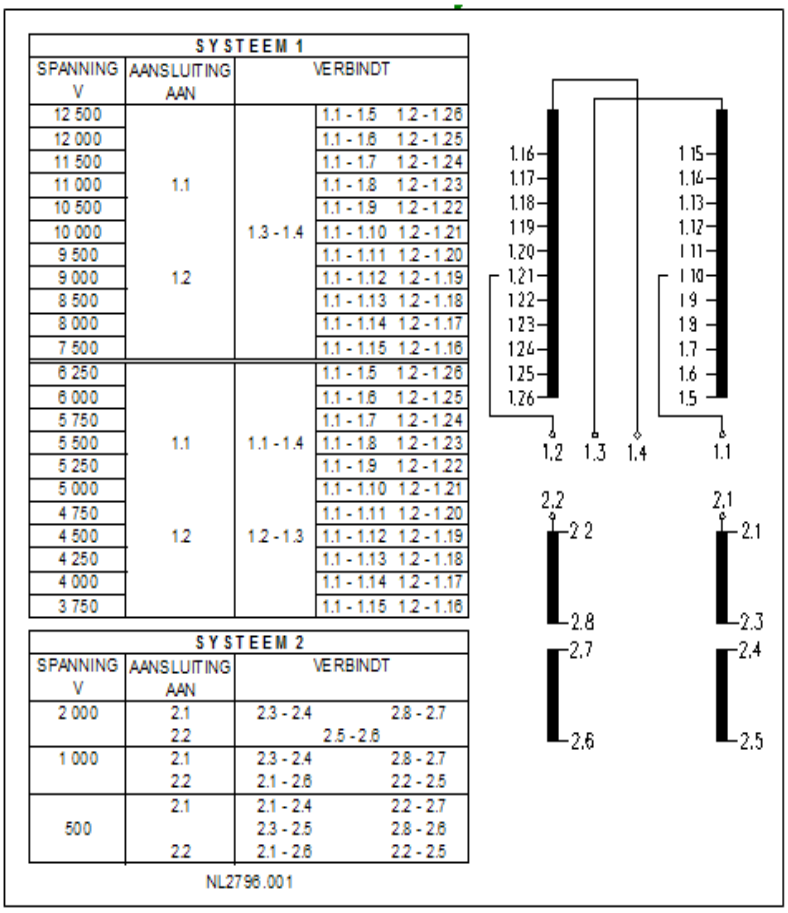
3.5.1Transformers TR2/T2

TR2/T2 is a set of three single-phase air-cooled transformers, 600kVA each, nominal frequency 50Hz and copper windings.

	1 - Fasen Transformator								
	Type	GEGN 750 / 12 - 2		Nr.	*	IEC 60726			
	Beschermings	IP 00		Schakeling	I i0	Bouwjaar	2007		
Systeem		1		2		Frequentie	50	Hz	
Nom.Vermogen		600	kVA	600	kVA	kVA	Kortsluitstroom		kA
Span.			V		V	V	Kortsluitstr. duur max.	2,0	s
		10000	V	2000	V	V	Wikkelingsmateriaal HS / LS		Cu / Cu
			V	1000	V	V	Isolatieklasse		F / F
		5000	V	500	V	V	Omgevingsklasse		E2
			V		V	V	Brandklasse		F1
			V		V	V	Klimaatklasse		C2
Stroom		60 120	A	0,3 0,6 1,2	kA	A	Totaalgewicht	1970	kg
Korstsluitspan.			%		%	%	Oliegewicht		kg
	Um	12	kV	3,6	kV	kV	Koelingmedium		
	LI / AC	75 / 28	kV	40 / 10	kV	kV	Koeling	AN	
	Hierzo schakelbeeld 2796.001								NL 10 /0

Figure 3-13 TR2/T2 transformer plate

The secondary (low-voltage) side consists of 4 separate windings (500V, 300A) and depending on their connection the user is able to get three different tap positions: 2000V, 1000V and 500V. It is worth noting that there is also the possibility to leave one or more windings entirely disconnected, only if the power is also adjusted (150kVA per winding). However, the witness tests have been carried out for normal operation conditions (all windings involved), and this information is used for the modeling. The per-unit representation though lets the user to adapt the nominal power and simulate the transformer all cases. The primary (high-voltage) side consists of two windings and depending on their configuration can give tap positions within a range from 3750 to 12500V in steps of 2%. This can be used in both single- and three-phase applications and because of the numerous tap positions it becomes one of the most useful tools of the FPGL.



SYSTEEM 1

SPANNING V	AANSLUITING AAN	VERBINDT	
12 500	1.1	1.3 - 1.4	1.1 - 1.5 1.2 - 1.26
12 000			1.1 - 1.6 1.2 - 1.25
11 500			1.1 - 1.7 1.2 - 1.24
11 000			1.1 - 1.8 1.2 - 1.23
10 500			1.1 - 1.9 1.2 - 1.22
10 000			1.1 - 1.10 1.2 - 1.21
9 500			1.1 - 1.11 1.2 - 1.20
9 000	1.2		1.1 - 1.12 1.2 - 1.19
8 500			1.1 - 1.13 1.2 - 1.18
8 000			1.1 - 1.14 1.2 - 1.17
7 500			1.1 - 1.15 1.2 - 1.16
6 250	1.1	1.1 - 1.4	1.1 - 1.5 1.2 - 1.26
6 000			1.1 - 1.6 1.2 - 1.25
5 750			1.1 - 1.7 1.2 - 1.24
5 500			1.1 - 1.8 1.2 - 1.23
5 250			1.1 - 1.9 1.2 - 1.22
5 000			1.1 - 1.10 1.2 - 1.21
4 750			1.1 - 1.11 1.2 - 1.20
4 500	1.2	1.2 - 1.3	1.1 - 1.12 1.2 - 1.19
4 250			1.1 - 1.13 1.2 - 1.18
4 000			1.1 - 1.14 1.2 - 1.17
3 750			1.1 - 1.15 1.2 - 1.16

SYSTEEM 2

SPANNING V	AANSLUITING AAN	VERBINDT	
2 000	2.1	2.3 - 2.4	2.8 - 2.7
	2.2	2.5 - 2.6	
1 000	2.1	2.3 - 2.4	2.8 - 2.7
	2.2	2.1 - 2.6	2.2 - 2.5
500	2.1	2.1 - 2.4	2.2 - 2.7
		2.3 - 2.5	2.8 - 2.6
	2.2	2.1 - 2.6	2.2 - 2.5

Figure 3-14 Tap positions of the TR2/T2 transformers

You can refer to APPENDIX B for the base values used for the per-unit conversion as well as for the provided information from the witness tests.

- No-load loss test

The high-voltage side is left open-circuited and the low-voltage side is supplied with 1000Vrms. Using the corresponding tables from APPENDIX B and the calculation as already described, it is possible to determine the core resistance and magnetizing inductance in per-unit:

	TR2/T2.1 - 0734062	TR2/T2.2 - 0734061	TR2/T2.3 - 0734060
R_c [pu]	605.45	608.52	617.92
L_m [pu]	634.28	564.36	564.24

Table 3-2 Magnetizing branch of the TR2/T2 transformers

- DC resistance measurement

During this test not all the tap positions are measured (see Table B-3, Table B-6 and Table B-9). However the resistances from three tap positions from each configuration of System 1 (series windings 7500-12500V and parallel windings 3750-6250V) are available. Based on Figure 3-14 and on the measurements that the witness test reports include, it can be assumed that for each configuration the resistance is increasing linearly with the voltage. Hence the full table of dc resistance of the high-voltage side is given in Table 3-3.

Position	TR2/T2.1 R_dc [mΩ] at 18.8 °C	TR2/T2.2 R_dc [mΩ] at 18.6 °C	TR2/T2.3 R_dc [mΩ] at 19 °C
12500	1037.5	1040	1043.5
12000	992.52	994.86	998.3
11500	947.54	949.72	953.1
11000	902.56	904.58	907.9
10500	857.58	859.44	862.7
10000	812.6	814.3	817.5
9500	768.8	770.42	773.54
9000	725	726.54	729.58
8500	681.2	682.66	685.62
8000	637.4	638.78	641.66
7500	593.6	594.9	597.7
6250	259.6	260.3	261.3
6000	248.34	248.98	249.98
5750	237.08	237.66	238.66
5500	225.82	226.34	227.34
5250	214.56	215.02	216.02
5000	203.3	203.7	204.7
4750	192.34	192.76	193.7
4500	181.38	181.82	182.7
4250	170.42	170.88	171.7
4000	159.46	159.94	160.7
3750	148.5	149	149.7

Table 3-3 DC resistances of the high voltage side of the three TR2.T2 transformers

For the secondary side the dc resistance of each winding separately is provided (Table B-3). Thus, the resistance for each tap position is calculated based on the Figure 3-14, which indicates how the four windings are connected to each other in every tapping.

Position	TR2/T2.1 R_dc [mΩ] at 18.8 °C	TR2/T2.2 R_dc [mΩ] at 18.6 °C	TR2/T2.3 R_dc [mΩ] at 19 °C
2000	20.721	20.682	20.706
1000	5.18	5.17	5.17
500	1.295	1.293	1.294

Table 3-4 DC resistances of the low voltage side of the three TR2/T2 transformers

- Load loss test

As already mentioned the short circuit tests have been performed increasing gradually the voltage until the ammeter shows the 50% of the rated current of the tapping. However, the values for the measured power have already been multiplied by 4, so that they refer to the rated condition. Looking into these values (APPENDIX B), one can notice that when changing the low-voltage tap position and keeping the primary constant, the variation on the short circuit voltage is almost zero. In contrast, varying the primary tap position the values of the u_z show significant differences. Hence, this is an

assumption that has been made during the calculation procedure and finally the impedance per primary tap position has been calculated.

Following the procedure as described above, it is possible to calculate the lumped resistance and reactance for the given measurements. However, some smart assumptions are needed to specify these data for the tap positions in between the given ones. Let us consider the primary tappings from 7500 to 12500V. This is the configuration that the two primary windings are connected in series. Three measurements are provided by the manufacturer. The resistance for the other tap positions can be determined by simple linear interpolation. However, as for the reactance, according to the Faraday's Law the induced voltage is given by:

$$E_{ind} = N\frac{d\bar{\varphi}}{dt} \qquad 3\text{-}21$$

Where $\bar{\varphi}$ is the average magnetic flux per turn and equals to the sum of the mutual flux and the leakage flux. Hence:

$$E_{ind} = N\frac{d\overline{\varphi_M}}{dt} + N\frac{d\overline{\varphi_L}}{dt} \qquad 3\text{-}22$$

The second term represents the leakage flux and considering that it is constant (on average) per turn, it is deduced that the winding reactance (electrical representation of the leakage flux) depends mainly on the number of turns. So, the linear interpolation for the reactance is a reliable assumption.

For the parallel configuration only the tap position of 5000V is provided with actual measurement in the test report. Thus the interpolation seems not possible. However, for two resistors R, the resistance in series connection would be 2R, whereas the resistance in parallel would be R/2. Based on this and on the fact that for each tap connection the resistance -in series configuration- is known, dividing the series values by 4, it becomes possible to calculate the corresponding tap connections in parallel configuration.

The following table gives an overview of the lumped winding impedances in pu. They are corrected for 75^{o}C. The model is accompanied by an excel file where all the calculations have been carried out and the temperature modification is possible.

	TR2/T2.1		TR2/T2.2		TR2/T2.3	
	R [pu]	L [pu]	R [pu]	L [pu]	R [pu]	L [pu]
12500	0.009149331	0.086702593	0.009140934	0.087186124	0.009009211	0.087312429
12000	0.009383271	0.086688809	0.009378741	0.087200583	0.009263671	0.087287917
11500	0.00962419	0.086344778	0.009624246	0.086887984	0.009529286	0.086928946
11000	0.009871133	0.085578556	0.009876646	0.086156925	0.009806012	0.086142531
10500	0.010122587	0.084271326	0.010134621	0.084889252	0.010093485	0.084808519
10000	0.010376233	0.082268221	0.010396097	0.08293092	0.010390861	0.082770323
9500	0.01068541	0.082156335	0.010682762	0.08280086	0.010703785	0.082667879
9000	0.011001151	0.081511067	0.010970725	0.082129176	0.011024038	0.082031109
8500	0.011319421	0.080140949	0.011254509	0.080721783	0.011347786	0.080668008
8000	0.011633799	0.077780793	0.011525746	0.078309913	0.011668875	0.078312614
7500	0.011934189	0.074057919	0.011771684	0.074515911	0.011977573	0.074591129
6250	0.009149331	0.086702593	0.009140934	0.087186124	0.009009211	0.087312429
6000	0.009383271	0.086688809	0.009378741	0.087200583	0.009263671	0.087287917
5750	0.00962419	0.086344778	0.009624246	0.086887984	0.009529286	0.086928946
5500	0.009871133	0.085578556	0.009876646	0.086156925	0.009806012	0.086142531
5250	0.010122587	0.084271326	0.010134621	0.084889252	0.010093485	0.084808519
5000	0.01038314	0.082227032	0.010408218	0.082949557	0.01041584	0.082867971
4750	0.01068541	0.082156335	0.010682762	0.08280086	0.010703785	0.082667879
4500	0.011001151	0.081511067	0.010970725	0.082129176	0.011024038	0.082031109
4250	0.011319421	0.080140949	0.011254509	0.080721783	0.011347786	0.080668008
4000	0.011633799	0.077780793	0.011525746	0.078309913	0.011668875	0.078312614
3750	0.011934189	0.074057919	0.011771684	0.074515911	0.011977573	0.074591129

Table 3-5 Short circuit impedances of TR2/T2 transformers at 75°C

3.5.2 Transformer TR3/T4

This is a 1.25MVA three-phase, three-winding transformer. It can be used as output transformer for the converter, extending its full power range from 400 to 24kV. The System 1 has delta connection, while the Systems 2 and 3 have star connection with accessible neutral point and a phase shift 150 degrees from the System 1.

	3 - Fasen Transformator									
	Type	GDGN 1875 / 24 - 1			Nr.	09 35621		IEC 60076		
	Beschermings	IP 00		Schakeling		D yn5 yn5		Bouwjaar	2009	
Systeem		1		2		3		Frequentie	50	Hz
Nom.Vermogen		1250	kVA	1250	kVA	1250	kVA	Kortsluitstroom		kA
Span.			V		V		V	Kortsluitstr. duur max.	2,0	s
			V		V		V	Wikkelingsmateriaal HS / LS		Cu / Cu
		24000	V	3300	V	400	V	Isolatieklasse		F / F
			V		V		V	Omgevingsklasse		E2
			V		V		V	Brandklasse		F1
			V		V		V	Klimaatklasse		C2
Stroom		30,1	A	219	A	1804	A	Totaalgewicht	4800	kg
Korstsluitspan.			%		%		%	Oliegewicht		kg
	Um	24	kV	3,6	kV	1,1	kV	Koelingmedium		
	LI / AC	95 / 50	kV	40 / 10	kV	- / 3	kV	Koeling	AN	
										NL 10 /0

Figure 3-15 TR3/T4 transformer plate

- No-load loss test

The core resistance and magnetizing inductance is calculated in the same way as TR2/T2. You can refer to APPENDIX B for the measurements that the witness test reports include. In this case of three-winding transformer, the System 1 and 2 are left open-circuited and the System 3 is supplied with the nominal 400Vrms.

R_c [pu]	396.32
L_m [pu]	226.95

Table 3-6 Magnetizing branch of the TR3/T4 transformer

- DC resistance measurement

The dc resistance is needed to ultimately determine the short-circuit impedance of the transformer. The dc resistance has been measured three times per winding (U-V, V-W and W-U). The average per phase resistance calculation is needed for the further steps.

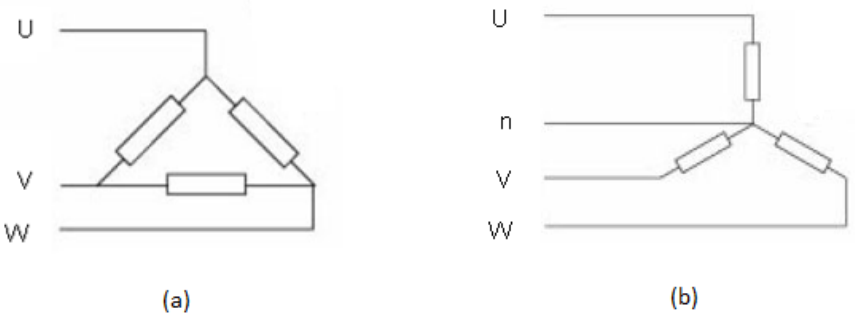


Figure 3-16 (a) delta winding (b) star winding

In the case of delta connection $R = 1.5R_{eq}$ and in the case of star connection$R = \frac{R_{eq}}{2}$.

System	R_dc [mΩ] at 23.5 °C
1 (delta)	9096.5
2 (star)	35.5
3 (star)	0.274

Table 3-7 DC resistances of the TR3/T4 transformer

- Load loss test

As the relevant IEC indicates, in a three-winding transformer, measurements are performed on the three different two-winding combinations. Working in pu system, it is possible to use the same equations like those used for the single phase transformer. The excel file accompanied with the Simulink model, which includes all the calculations in detail gives the chance to the user to select the temperature. The following table refers to 75°C.

System 1	System 2	System 3	R [pu]	L [pu]
24000	3300 (sc)	Open-circuited	0.0112384	0.067935031
24000	Open-circuited	400 (sc)	0.0105088	0.138936471
Open-circuited	3300	400 (sc)	0.0070624	0.067997862

Table 3-8 Short circuit impedances of TR3/T4 transformer at 75°C

3.5.3 Transformer TR3/T3

The FPGL has a direct 10.5kV, 50Hz grid connection. A special three-phase, two-winding transformer is used to step-down the voltage to 3800, 1900 or 950V.

Systeem	1					2					
Vermogen (kVA)	1700					1700	850	425			
Spanning (V)	11000	10750	10500	10250	10000	3800	1900	950			
Stroom (A)	93,5					258	258	258			
Um (kV)	12					7,2					
LI / AC (kV)	75 / 28					60 / 20					
Aansluiting / Positie	volgens schakelbeeld NL2589.002										
Frequentie (Hz)	50		Schakeling		Dyn 5			Koeling		AN	
Totaalgewicht (kg)	4650		Beschermingsgraad		IP 00			Bouwjaar		2007	
Isolatie Klasse HS / LS	F / F		Type		GDGN 1700/12-2			IEC / VDE		60726 / 0532	
Waardes bij 75°C	Po (W) = 2700		+ 15 %		Pk (W) = 14200		+ 15 %	Uz (%) =		> 6	
Opmerking											

Figure 3-17 TR3/T3 transformer plate

The System 1 is delta connected and the System 2 star connected, with accessible neutral and 150 degrees phase shift (Dyn5). The winding and the core impedances are calculated in a similar way, using the base values and the measurements as presented in APPENDIX B.

- No-load loss test

The winding of System 1 is open-circuited and the System 2 is supplied with 3800Vrms.

R_c [pu]	717.905
L_m [pu]	898.53

Table 3-9 Magnetizing branch of the TR3/T3 transformer

- DC resistance measurement

In the same way as in the TR3-T4, the per-winding resistance value is calculated.

System	Voltage [V]	R_dc [mΩ] at 19.1 °C
1 (delta)	10500	883.5
2 (star)	3800	18.646
	1900	8.56
	950	4.36

Table 3-10 DC resistances of the TR3/T3 transformer

- Load loss test

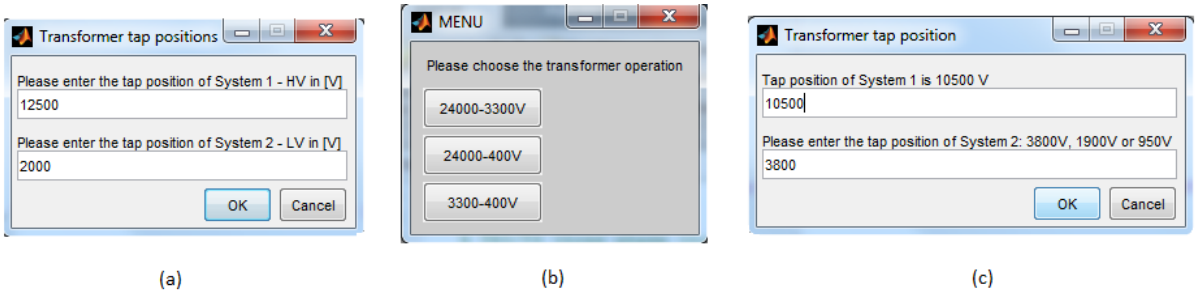
Similarly to TR3/4 transformer the short circuit impedance of this transformer is calculated. The excel file accompanied with the Simulink model, which includes all the calculations in detail gives the chance to the user to select the temperature. The following table includes the pu values for 75 °C.

System 1	System 2	R [pu]	L [pu]
10500	3800	0.00862721	0.063795286
10500	1900	0.005509394	0.042175619
10500	950	0.004059523	0.022153574

Table 3-11 Short circuit impedances of TR3/T3 transformer at 75°C

3.6 Models

Once all the necessary information is available, it becomes possible to input them in the Simulink models. Due to the fact that the transformers are never used in the non-linear region (they are always in the unsaturated region), the hysteresis curve is not integrated in the models. The Simulink models are accompanied by a MATLAB m-file, which is a script consisting of a set of commands that initialize the transformers (import the model's properties). The initialization through such a script makes the model faster, as it does not need to make any calculations in the Simulink model itself. The m-files allow the user to select the suitable tap position for their application through an input dialog box, and hence the corresponding winding impedance is imported in the model.



(a) (b) (c)

Figure 3-18 Input dialog boxes for the (a) TR2/T2, (b) TR3/T4 and (c) TR3/T3 transformers

The impedance of the winding is dependent on the tap position. The full data base of the transformers' data are included in three excel files (.xlsx), which are loaded on MATLAB Workspace through the corresponding m-files. Additionally, it is noteworthy that because from the short circuit

test, it is possible to calculate the lumped resistance and inductance of the windings, following the bibliography [14], to make a more reliable representation of the transformer, the lumped values are equally distributed in the two windings. In the case of the three-winding transformer the values are equally distributed in the two windings used in every single application. The third winding which is not used gets zero impedance. In APPENDIX C, the Simulink realization of the models is presented.

Next, the tables verify the effectiveness of the proposed simulation models at their nominal frequency. This is done through the comparison of the results that the model returns with the data obtained from the hardware experiments (witness tests). The validation of the models at higher frequencies follows in Chapter 6.

Tapping	U [Vrms]	Im (witness test) [Arms]	Im (simulation) [Arms]
10000 : 2000	414.6	30	30
12500 : 2000	544.9	24	24
7500 : 2000	281.3	40	40
5000 : 2000	207.2	60	60
10000 : 1000	414.1	30	29.96
5000 : 1000	207.2	60	60
10000: 500	411.5	30	29.78
5000 : 500	206.1	60	59.68

Table 3-12 TR2/T2.1 short circuit comparison table

Secondary Voltage [Vrms]	Io [Arms] (witness test)	Io [Arms] (simulation)
1000	1.37	1.37

Table 3-13 TR2/T2.1 open circuit comparison table

Secondary Voltage [Vrms line-to-ground]	Io [Arms] witness test T2.1	Io [Arms] simulation T2.1	Io [Arms] witness test T2.2	Io [Arms] simulation T2.2	Io [Arms] witness test T2.3	Io [Arms] simulation T2.3
1000	1.37	1.37	1.45	1.45	1.44	1.44

Table 3-14 Three-phase TR2/T2 open circuit comparison table

Table 3-14 shows the differences on the magnetizing current in a three-phase open-circuit implementation of the TR2/T2. The model indeed recognizes the differences per phase.

Tapping	U [Vrms]	Im (witness test) [Arms]	Im (simulation) [Arms]
24000 : 3300	826.3	15.05	15.04
24000 : 400	1672	15.05	15.04
3300 : 400	112.8	109.5	109.36

Table 3-15 TR3/T4 short circuit comparison table

Tertiary Voltage [Vrms]	Io [Arms] (witness test)	Io [Arms] (simulation)
400	9.16	9.16

Table 3-16 TR3/T4 open circuit comparison table

Tapping	U [Vrms]	Im (witness test) [Arms]	Im (simulation) [Arms]
10500 : 3800	337.7	46.7	46.7
10500 : 1900	223.6	23.4	23.4
10500 : 950	118.4	11.7	11.7

Table 3-17 TR3/T3 short circuit comparison table

Secondary Voltage [Vrms]	Io [Arms] (witness test)	Io [Arms] (simulation)
3800	0.46	0.46

Table 3-18 TR3/T3 open circuit comparison table

The tables prove that the transformer models return values with no difference in most cases with the actual measurements of the witness test reports. This comparison between the witness test measurements and the simulation results confirm the validity of the model at the transformers' nominal frequency. As aforementioned, the evaluation of the models' response at frequencies other than the nominal will be completely shown at the model validation chapter.

Chapter 4 : Other components

4.1 Grid line

Once the transformers of the FPGL have been modeled, the next step is to model the power converter. However, the power converter is connected through the TR3/T3 transformer directly to the public grid. For better evaluation of the converter model, it is preferable to model first the grid line. Figure 4-1 depicts the single-line diagram of the grid, which is directed from Kattenberg substation to DNV KEMA 10.5kV distribution system. A separate 50kV grid line is dedicated exclusively to DNV KEMA laboratories in the Business Park, Arnhem. Through a 50kV/10.5kV, Yy0 transformer the line reaches the 10.5kV distribution center. As the single-line diagram shows the Capitole bus-bar feeds several labs and facilities of DNV KEMA including the FPGL.

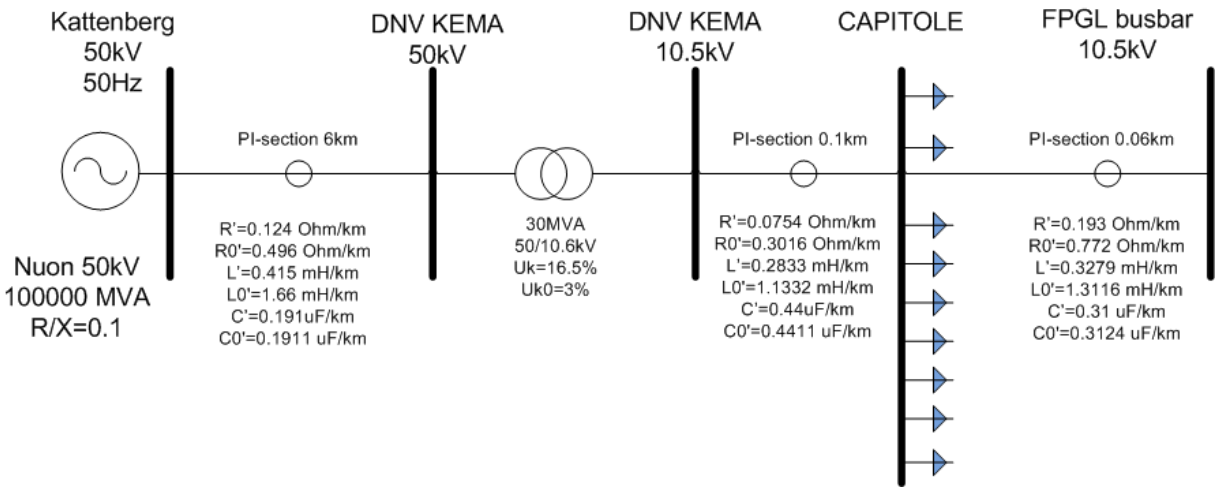


Figure 4-1 Single-line diagram of the grid line

The Active Front End, which is connected to the FPGL bus-bar through the TR3/T3 transformer can inject high frequency current content back to the grid because of the switching frequency of the PWM generator (~1800Hz). The capacitor that is part of the grid-side converter input filter provides a low impedance path for high frequency PWM ripple and thus attenuates the content of current ripple in utility current. However, in high power applications and high frequencies this content may not be negligible and thus it is of high importance to have a first view of the injected current harmonics to the grid using the model. This will prevent disturbances and low power quality for the other labs that are connected to the same bus-bar. The Simulink realization of the grid line is presented in APPENDIX D.

4.2 Load components

Adjustable passive loads are also part of the FPGL equipment. Three different load banks with voltage range up to 4kV can be used in multiple possible combinations (delta or star connected). The resistive load bank is available at a total power capacity of 500kW. Additionally, the inductive and the capacitive load banks have a total power capacity of 1MVAr each. The following figures illustrate the multiple possible configurations of the banks.

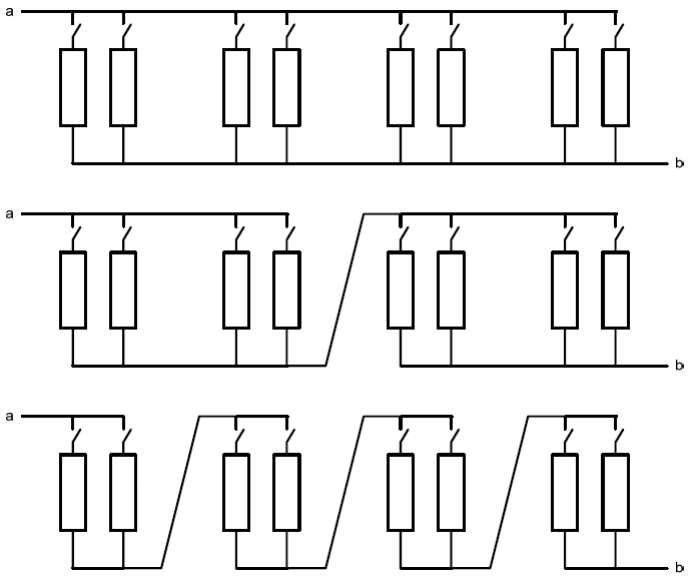


Figure 4-2 Possible configuration of load banks

In the case of the resistive load bank pairs of 12 and 24Ω are available, whereas the inductive and capacitive banks consist of pairs of 38.2 and 19.1 mH and 500 and 250 uF respectively. In Simulink they can be modeled easily as RLC loads from the library of the software.

Chapter 5 : Converter

5.1 Introduction

The heart of the FPGL comprises a four-quadrant (4Q), medium-voltage (MV) power electronic converter. This converter has a power level of 1 MVA, and is freely programmable using its so-called GridSim control interface, which has been specially designed for the FPGL. The converter can generate freely programmable static and dynamic grid phenomena [2]:

Static phenomena

- Harmonic voltage distortion up to 2400 Hz (closed loop control up to 15th harmonic)

Dynamic phenomena

- Voltage fluctuations
- Power frequency variations (between DC and 75 Hz)
- Voltage dips and interruptions
- Zero and negative sequence variations
- Voltage unbalance
- Fault ride through conditions

Figure 5-1 Flex Power Grid Lab: The converter

The nominal power from 400V to 24kV, 50Hz is 1MVA. 4Q operation of the test generator is mandatory, since the load may consume active and reactive power from the converter's load side or deliver active and reactive power to it. The controller was developed and implemented by AixControl GmbH.

5.2 Multilevel Converter

Multilevel voltage source converters (VSC) are emerging as a new breed of power converter options for high power applications. The multilevel VSC typically synthesize the staircase voltage wave from

several levels of dc capacitor voltages. Such kind of topologies are selected in many high voltage and high power applications, due to advantages of high quality waveforms, low switching losses, high voltage capability and low electromagnetic compatibility (EMC) concerns [18], [19], [20].

The general idea of multilevel converters is to synthesize a sinusoidal voltage from several voltage levels, typically obtained from capacitor voltage sources. As the number of levels increases, the synthesized output waveform adds more steps, producing a staircase wave, which approaches the sinusoidal wave with minimum harmonic distortion. Additionally, the voltage stress across the devices is lower, and smaller passive components are required. However, increasing the number of the levels, the complexity of the control strategy increases as well, and limitations such as the voltage unbalance between the different levels may appear [18]. Figure 5-2 shows the fact that in a multilevel topology, the output is achieved by dividing the dc-link potential into multiple sections, so that each phase leg can switch between multiple voltage levels.

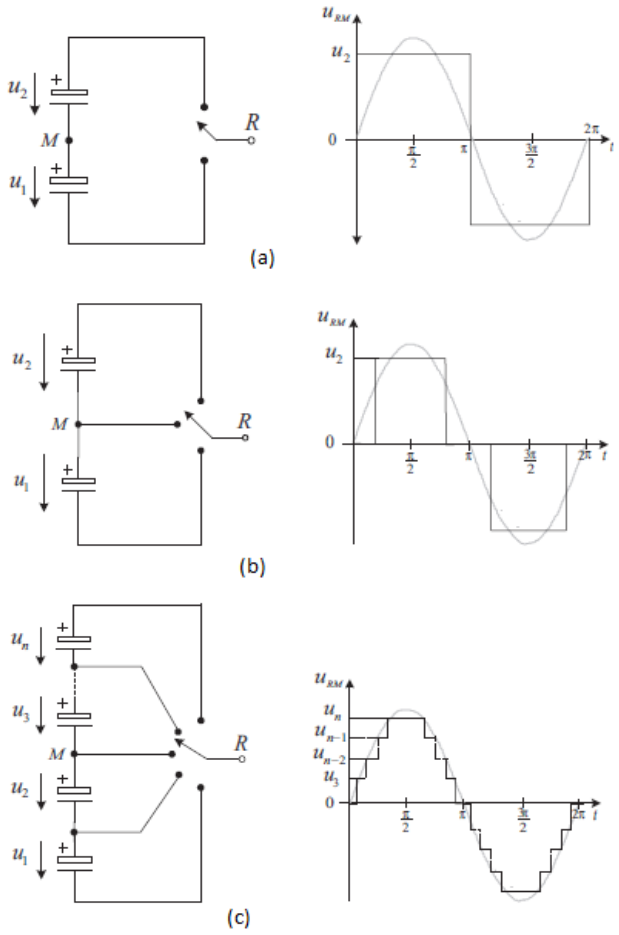


Figure 5-2 Simplified circuit and generated output voltage of (a) 2-level, (b) 3-level and (c) 5-level converter [19]

A. Yazdani and R. Iravani present in [21] the three mostly used topologies; the neutral-point clamped (NPC), the flying capacitors and the cascaded H-bridge. In this thesis, the working principle of the NPC, three-level VSC is briefly presented, as this is the type of the converter that is used in both the load and grid side converter of the FPGL.

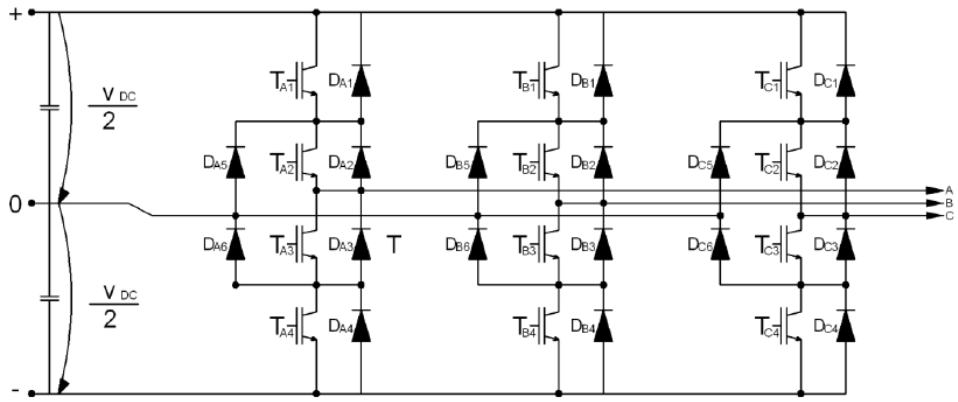


Figure 5-3 Three-level NPC converter schematic

As it can be seen in Figure 5-3, this converter has the neutral point clamped to the mid-point of the DC-link. This configuration uses fast switching devices (IGBTs) that switch simultaneous and generate a high dv/dt at the output terminal of the converter. The IGBTs are connected in series, and hence the stress on the devices is reduced. The neutral point is used to generate three output voltage levels $V_{dc}/2$, 0, $-V_{dc}/2$, based on the commutation of the twelve switching devices. The combination of these semiconductors allows 27 switching vectors [20]. By means of Pulse Width Modulation (PWM), quasi sinusoidal waveform can be obtained at the output. In order to have a high quality waveform, filtering and high switching frequency is required.

In a three phase m-level NPC converter each leg is composed of 2(m-1) series connected switches and (m-1) DC-link capacitors charged with a voltage equal to $V_{dc}/(m-1)$. Thus Figure 5-3 illustrates the three-level converter with four series IGBTs per leg and two capacitors. The IGBTs include antiparallel diodes, which in real life are comprised inside the switching device module. They are free-wheeling diodes, and their purpose is to eliminate voltage spikes and provide a smooth a current to the load as well as to provide a DC discharge path for the remnant stored energy from an inductive load, which can surge the transistor and hence lead it to breakdown. Consequently this makes the switch bidirectional, at least as far as the current flow is concerned. It is worthy to mention an important disadvantage of the NPC topology, which is the fact that the necessary reverse voltage blocking capability of the clamping diodes is proportional to the level for which they are used to employ clamping action. As a result, series connection of diodes is required, which complicates the design and raises reliability and cost concerns [19].

The presentation of the switching paths of the NPC converter will facilitate the following analysis and modeling procedure. Figure 5-4 illustrates schematically the switching paths per leg.

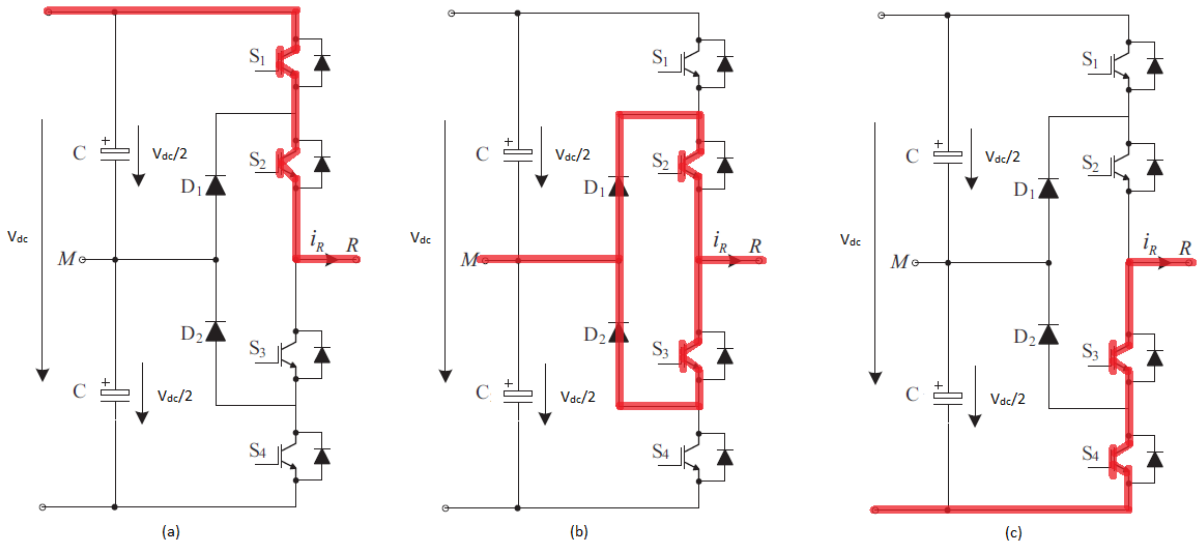


Figure 5-4 Switching paths NPC converter (a) P state, (b) 0 state and (c) N state

In the switching state P (positive) the upper two switching devices are on and the resulting converter leg voltage is $V_{dc}/2$, while n the switching state N (negative) the lower two switching devices are on and the resulting converter leg voltage is $-V_{dc}/2$. When the inner two switches are on the voltage of the leg is zero. The switches T_{1-} T_3 and T_2 -T_4 operate in complementary mode [20], [22].

5.3 Control Architectures

A converter model is divided into two main parts: the electronic part, consisting of the switching devices and the filter, and the control part. A DSP platform is normally used for implementing the control. The control box requires a few input parameters, such as the reference voltage, the simulation time, the sampling time, the switching frequency, the output frequency and the dead time. For simplicity reasons, the dead-time is not taken into consideration in this thesis. Additionally, the first part is developed using components from the Simulink library, which provides sufficient accuracy for the purpose of the project.

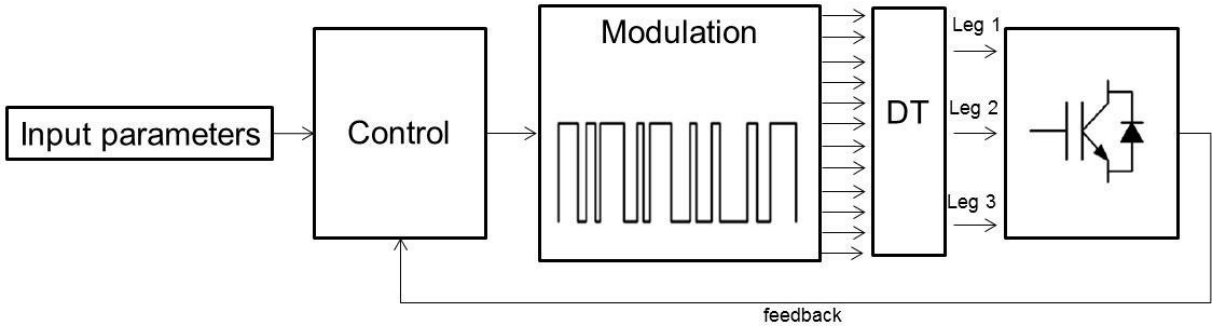


Figure 5-5 Structure of a complete converter model

The last decades a lot of research has been conducted on the development and implementation of accurate control strategies of the VSCs. According to the references, the control can be done either in stationary frame using resonant controller, or in rotating dq0 frame using PI controller. Stationary frame PI current-regulated VSCs are conventionally regarded as unsatisfactory for ac systems

because they cannot eliminate steady state errors. In [23], [24], [25], [26] and [27] the resonant controllers are explicitly explained, while also the advantages over the PI controllers in stationary frame are mentioned as well. More specifically a PI controller is not able to track a sinusoidal reference without steady-state amplitude and phase errors. The need to transform the signals between the stationary and the synchronous reference frames (abc to dq0 transformation and vice versa) makes the implementation of a synchronous frame PI regulator complex. Despite the large calculation effort, this technique remains very popular and is explained in detail in [28], [29], [30], [31] and [32]. A regulator with zero steady-state error in the stationary frame would certainly have implementation advantages.

In the next paragraphs, both control schemes are analyzed and implemented. The load side converter is controlled in stationary frame (PR), while for the control of the AFE, the rotating reference frame has been selected (PI).

5.4 Load-side Converter

As already mentioned this is a three-level NPC voltage-source converter. It can be observed as a medium-voltage test generator. It is used in the FPGL to generate disturbances in MV grids according to standards like IEC 61000, EN 50160 and IEEE 1547.

5.4.1 Topology & Specifications

The topology of a three-level NPC, VSC, is shown in paragraph 5.2. The main specifications of the converter are:

- Power: 1MVA continuous
- Three-phase voltage range: 400 – 3300 $V_{ac\text{-}rms}$
- Maximum current (per phase): 175 A_{rms}
- Frequency range: DC – 75 Hz
- Bandwidth: 2.4kHz

The converter output filter and its specifications are also worthy to be presented in this part, because it plays significant role for the control development.

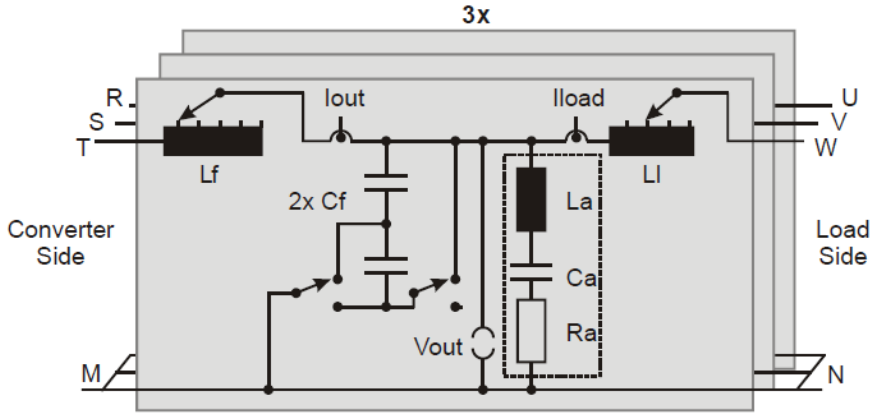


Figure 5-6 Converter Output Filter

As it can be seen in Figure 5-6, it is a T-type L-C-L filter, including an L-C-R resonant absorption filter in star topology. The filter inductance L_f and the line impedance are adjustable, while the filter capacitance consists of two similar capacitors C_f that can be connected either individually or in series or in parallel. The absorption filter LCR is designed to absorb the switching frequency.

Specification		Value
Rated frequency (Hz)	Hz	16+2/3; 50; 60; 75
Inductor Lf	mH	2; 1.5; 1.1; 0.85; 0.6
Inductor Ll	mH	0.5; 0.4; 0.3; 0.2; 0.1
Inductor La	mH	0.125; 0.131; 0.119; 0.08
Capacitor Cf	uF	315±5%
Capacitor Ca	uF	50±5%
Resistor Ra	mΩ	70±30%
Parasitic Resistors RCf, RLf	mΩ	100

Table 5-1 Converter Output Filter Specifications

Taking into account all this information the model is built in Simulink, using components from the SimPowerSystems Toolbox. In APPENDIX E the plant of the system as developed in Simulink is depicted.

5.4.2 State-space representation, modeling & control

Sebastian A. Richter et al, members of Aachen University and AixControl GmbH developed the controller of the FPGL converter. The complete description of that is analyzed in [33]. In this paper the control scheme of the FPGL load-side converter is described and verified through a downscaled prototype.

The converter should be able to generate freely programmable static and dynamic voltage phenomena, such as voltage unbalance, voltage dips, harmonic voltage distortion, voltage flickering and frequency variation.

Two major tasks need to be fulfilled by suitable control architecture for the test generator:

- Zero steady-state error for ac signals (concerning amplitude as well as phase)
- Stabilization of the plant

It is necessary to carry out the following analysis, in order to initialize the plant and aspects of the controller through an m-file and eventually import the data into the Simulink model. The following steps summarize the procedure that was followed for the modeling of the load side converter using MATLAB:

i. Develop the plant model
   - State space representation of the output filter (continuous filter, s-domain)
   - Discretize the transfer function of the filter (z-domain)
   - Include any possible delays that should be taken into account (augment the plant model)

ii. Controller design
   - Design of the output feedback and the compensator
   - Augment the plant model, including the output feedback and the compensator

- Stabilization of the plant
- Determine the feed forward gains

Once all the above gains and transfer functions have been determined and calculated using MATLAB code, then the Simulink variable-based model is ready to be developed. The prior calculation of the gains and transfer functions through a script makes the procedure more generic, convenient and certainly the simulation times much faster.

5.4.2.1 Plant model

Figure 5-7 illustrates the single-phase equivalent circuit of the output filter.

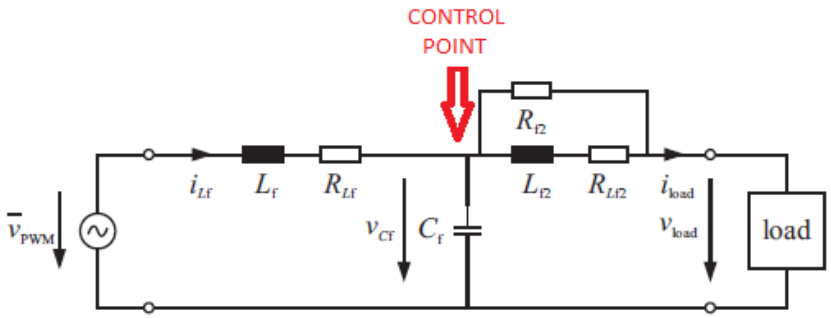


Figure 5-7 Single-phase equivalent circuit of output filter [33]

L_f and C_f (with their parasitic resistances RL_f and RC_f) comprise the LC filter. L_{f2} forms a line impedance that is very lightly damped by its parasitic resistance. It can be either bypassed in order to represent stiff grids, or increased to represent weak grids, such as remote places where the feeders are long and the grid impedance higher. Only the LC-filter itself is taken into account for the control design. Hence the control point is at the terminal of the C_f. The equations of the filter are the following:

$$L_f \frac{di_{Lf}}{dt} = -R_{Lf} \cdot i_{Lf} - R_{Cf} \cdot (i_{Lf} - i_{load}) - U_{Cf} + U_{PWM} \quad 5\text{-}1$$

$$C_f \frac{dU_{Cf}}{dt} = i_{Lf} - i_{load} \quad 5\text{-}2$$

$$U_{out} = U_{Cf} + R_{Cf} \cdot (i_{Lf} - i_{load}) \quad 5\text{-}3$$

The state space representation of these equations is:

$$\dot{x_f}(t) = A_{f,s} \cdot x_f(t) + Bu_{f,s} \cdot u_f(t) + Bz_{f,s} \cdot z_f(t) \quad 5\text{-}4$$

$$y(t) = C_{f,s} \cdot x_f(t) + D_{f,s} \cdot u_f(t) \quad 5\text{-}5$$

Where:

State vector: $x_f(t) = \begin{bmatrix} i_{Lf}(t) \\ U_{Cf}(t) \end{bmatrix}$ and $\dot{x_f}(t) = \begin{bmatrix} {di_{Lf}}/{dt} \\ {dU_{Cf}}/{dt} \end{bmatrix}$

Input vector: $u_f(t) = [U_{PWM}(t)]$

Disturbance input vector: $z_f(t) = [i_{load}(t)]$

Output vector: $y(t) = [U_{out}(t)]$

And hence the system matrix, the command input, the disturbance input, the output and the feed-through matrices are the following:

$$A_{f,s} = \begin{bmatrix} -\frac{R_{Lf} + R_{Cf}}{L_f} & -\frac{1}{L_f} \\ \frac{1}{C_f} & 0 \end{bmatrix}$$

$$Bu_{f,s} = \begin{bmatrix} \frac{1}{L_f} \\ 0 \end{bmatrix}$$

$$Bz_{f,s} = \begin{bmatrix} \frac{R_{Cf}}{L_f} \\ -\frac{1}{C_f} \end{bmatrix}$$

$$C_{f,s} = [R_{Cf} \quad 1]$$

$$D_{f,s} = [0]$$

Inserting these data in the MATLAB Editor, the second-order filter model in continuous (s-domain) state-space representation is developed. For the controller implementation a DSP platform is used and thus digital control is performed. For this reason, the transfer function is transformed into the z-domain. The discretization of the model described above with a sampling time Ts, can be done directly in MATLAB, using *c2d* function and the Zero-Order-Hold method. As a result, the discretized state-space matrices $A_{f,z}$, $Bu_{f,z}$, $Bz_{f,z}$, $C_{f,z}$, and $D_{f,z}$ are obtained[1].

At this point, it important to make clear that the plant operates in the continuous time domain, whereas the operation of the controller takes place in the discrete time domain. Thus, signals have to be converted from the continuous to the discrete time domain and vice versa using Analog-to-Digital Converter (ADC). Special attention should be given at the avoidance of the aliasing phenomena. The aliasing phenomenon is a result of the violation of Shannon's theorem[2]. According to that, a band-limited function can be perfectly reconstructed from an infinite sequence of samples, if the band-

[1] The index *f* of the state space matrices indicates that the matrices refer only to the filter model, while also the indices *s* and *z* refer to continuous and discrete domain respectively.

[2] Shannon's theorem: if a function x(t) contains no frequencies higher than B hertz, it is completely determined by giving its ordinates at a series of points spaced (1/2B) apart.

limit is no greater than ½ of the sampling rate. In other words, there is an upper bound for the sampled signal bandwidth, beyond which perfect reconstruction becomes impossible and aliasing phenomena appear. The limit frequency is called Nyquist frequency and is proved to be equal to a half of the sampling frequency [34]. Hence a filter limits the frequency spectrum, before the ADC, of the sampled signal, so as to make it negligible above the Nyquist frequency. It is a low-pass filter with cut-off frequency $f_s/2$ to eliminate spectrum replicas at higher frequencies.

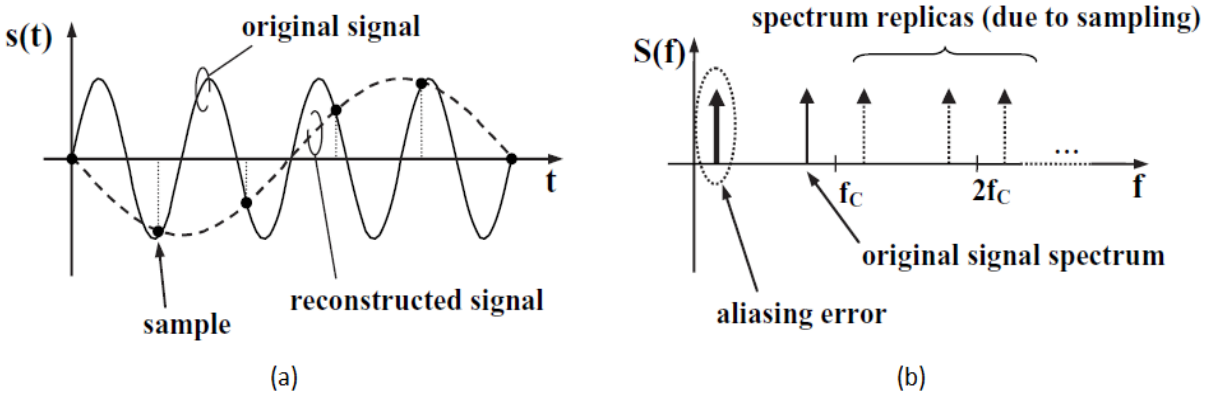


Figure 5-8 (a) Aliasing effect of a too low sampling frequency on the reconstructed signal, (b) Aliasing effect in frequency domain [34]

ZOH method, assumes the control inputs are piecewise constant over the sampling period Ts. This is to say that the modulating signal m(t) is sampled at the beginning of each sampling period and the sampled value kept constant for the whole period. It is now evident that, because of the sample and hold effect, the response of the modulator to any disturbance, can take place only during the modulation period following the one where the disturbance actually takes place. Therefore, even if our signal processing were fully analog, without any calculation or sampling delay, passing from an analog to a digital PWM implementation would imply an increase in the system response delay [34]. The proposed discrete model has been determined using the ZOH equivalent (*ZOH* Matlab method of *c2d* function) and hence, already accounts for this effect.

As for the PWM, a discrete 3-phase PWM generator (3-level type, 12 pulses) is used, which is readily available in the Simulink library. However, the calculation delay that the generator causes should not be neglected. The analog PWM modulator delay can always be considered negligible. In contrast the digital implementations of the PWM determine an appreciable, not at all negligible, delay effect [34].

More specifically, the discrete PWM generator introduces a delay of half a sampling period Ts/2 due to calculation. This delay is between the instance at which the values of the state variables are sampled and the instance at which the duty cycle is updated. In other words, the delay introduced by the PWM modulator represents the time distance between the modulating signal m(t) sampling instant and the instant when the output pulse is completely determined. The figures below show the general block diagram of PWM and the particular case of a triangular carrier modulation. As it is shown, the modulating signal m(t) is discretized by the ZOH block and the output $m_s(t)$ is compared with the triangular carrier. The first case corresponds to single update mode where $T_s = T_{PWM}$ and the second case to double update mode $T_s = {}^{T_{PWM}}/_{2}$.

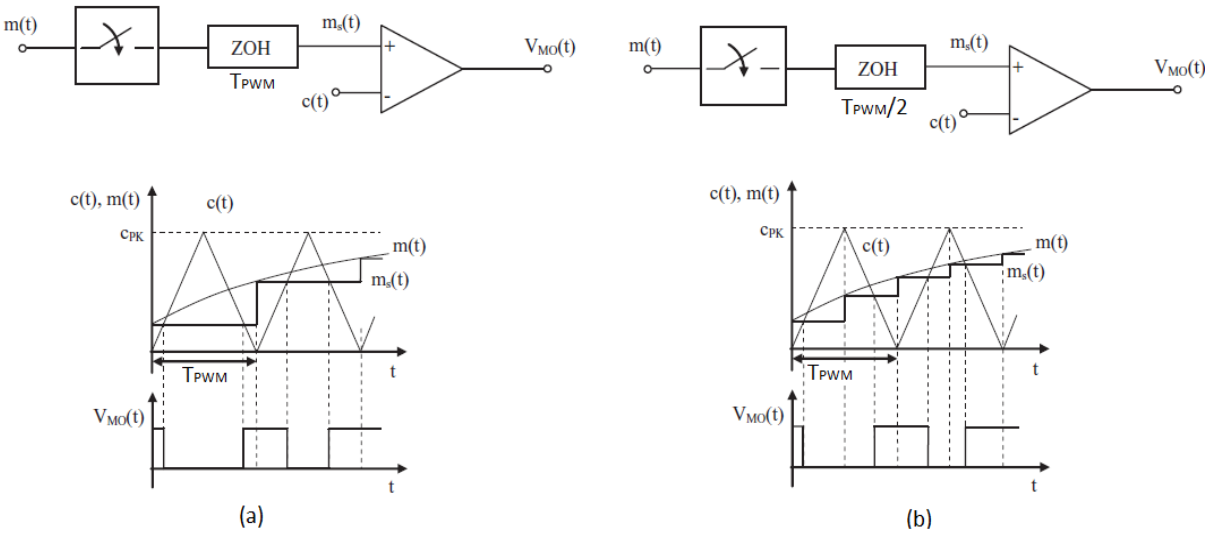


Figure 5-9 Uniformly sampled PWM with (a) single update mode and (b) double update mode [34]

In [34] is given the transfer function between the modulating signal m(t) and output of the comparator $V_{MO}(t)$:

$$PWM(s) = \frac{V_{MO}(s)}{M(s)} = \frac{e^{-sDT_{PWM}}}{c_{PK}} \quad 5\text{-}6$$

Where $V_{MO}(s)$ and M(s) represent the Laplace transforms of $V_{MO}(t)$ and m(t), respectively. Therefore, this result shows that a uniformly sampled modulator presents a delay, the value of which is proportional to the steady state duty cycle D. More specifically, for the triangular carrier modulation, like the FPGL case, the transfer function for single and double update mode respectively becomes:

$$PWM(s) = \frac{V_{MO}(s)}{M(s)} = \frac{1}{2c_{PK}}\left(e^{-s(1-D)^{T_{PWM}}/_2} + e^{-s(1+D)^{T_{PWM}}/_2}\right) \quad 5\text{-}7$$

$$PWM(s) = \frac{V_{MO}(s)}{M(s)} = \frac{1}{2c_{PK}}\left(e^{-sD^{T_{PWM}}/_2} + e^{-s(1-D)^{T_{PWM}}/_2}\right) \quad 5\text{-}8$$

Hence the modulator phase lag for the single and double update modes is $-\omega^{T_{PWM}}/_2$ and $-\omega^{T_{PWM}}/_4$ respectively.

In the FPGL the sampling frequency is twofold the switching frequency. However, the installed PWM generator does not support the double update feature and hence a single duty cycle is generated per PWM period using the average of the two samples in that period. For the purposes of this thesis, the Simulink model is developed ignoring the PWM generator's limitations and the double update feature is considered possible. This feature offers improved control dynamics and simultaneously keeps the modeling procedure less complex but still accurate in respect with the actual performance of the lab. As a result, in the model a $^{T_{PWM}}/_4 = {}^{T_s}/_2$ delay is taken into account.

In [27], S. Richter et al describe the conventional way of introducing one whole sampling period (z^{-1}) delay. However, introducing a delay of less than one whole sampling period is not straightforward and this is explained further in [33]. To introduce such a delay, the second order model should be

augmented to third order. Two different input matrices for the first half of the sampling period and for the second half of the sampling period are calculated:

$$B_{f,z,1} = e^{A_{f,s} \cdot T_s} \cdot \int_0^{\frac{1}{2}T_s} e^{-A_{f,s}\tau} d\tau \cdot B_{f,s} \quad 5\text{-}9$$

$$B_{f,z,2} = e^{A_{f,s} \cdot T_s} \cdot \int_{\frac{1}{2}T_s}^{T_s} e^{-A_{f,s}\tau} d\tau \cdot B_{f,s} \quad 5\text{-}10$$

The entire plant's (output filter including calculation delay) system matrix [3x3], the command input [3x1], the disturbance input [3x1], the output [1x3] and the feed-through matrices are being constructed as follows:

$$A_{plant,z} = \begin{bmatrix} A_{f,z} & B_{f,z,1} \\ 0 & 0 \end{bmatrix}$$

$$Bu_{plant,z} = \begin{bmatrix} B_{f,z,2} \\ 1 \end{bmatrix}$$

$$Bz_{plant,z} = \begin{bmatrix} Bz_{f,z} \\ 0 \end{bmatrix}$$

$$C_{plant,z} = [C_{f,z} \quad 0]$$

$$D_{plant,z} = [0]$$

The state space equations of the plant are:

$$\dot{x_{plant}}(k+1) = A_{plant,z} \cdot x_{plant}(k) + Bu_{plant,z} \cdot u_{plant}(k) + Bz_{plant,z} \cdot z_{plant}(k) \quad 5\text{-}11$$

$$y(k) = C_{plant,z} \cdot x_{plant}(k) + D_{plant,z} \cdot u_{plant}(k) \quad 5\text{-}12$$

Where:

State vector: $x_{plant}(k) = \begin{bmatrix} i_{Lf}(k) \\ U_{Cf}(k) \\ U_{PWM}(k) \end{bmatrix}$

Input vector: $u_{plant}(k) = [U^*_{PWM}(k)] = [U_{PWM}(k+1)]$

Disturbance input vector: $z_{plant}(k) = [i_{load}(k)]$

Output vector: $y(k) = [U_{out}(k)]$

The complete LC filter and PWM generator model has now been developed and the block diagram of that is shown below:

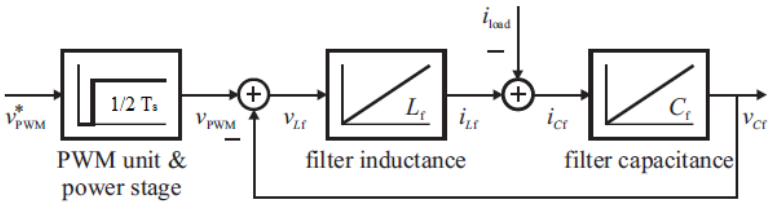


Figure 5-10 Block diagram of plant: LC filter and PWM generator [33]

The corresponding representation in Simulink can be found in APPENDIX E.

5.4.2.2 Controller

The controller should ensure zero steady-state error and a stable system. Figure 5-11 shows the implemented control scheme of the FPGL load-side converter.

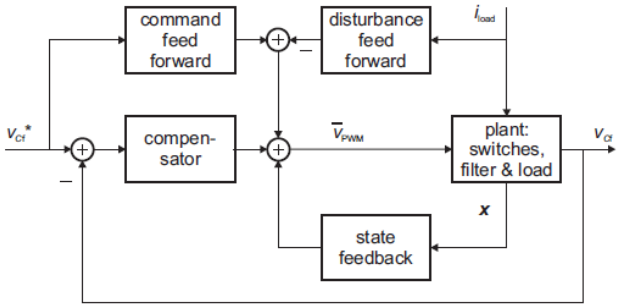


Figure 5-11 Implemented control architecture of the load-side converter [33]

This scheme, as implemented in Simulink, can be found in the APPENDIX E.

- *Zero steady state error*

The FPGL converter is a medium voltage test generator, which means that it should be able to generate, among others, voltage harmonics in order to emulate "bad grid" conditions. Hence, the zero steady state error should be achieved for the fundamental voltage component as well as for selected harmonic components of higher order.

The zero steady state error is achieved through the output feedback and a compensator consisting of either up to ten resonant controllers or an I-controller. Depending on the requirement that need to be fulfilled for each test request, the corresponding compensator configuration is chosen. Thus, for static voltage phenomena the "harmonic mode" compensator (PR controller) is used, whereas dynamic phenomena can be studied turning the compensator to "dynamic mode", which consists of an I-controller to achieve better transient performance.

1. *Harmonic Mode:*

The load side converter, in steady state operation uses resonant controller, because compared to the conventional PI controller, it can overcome two well-known drawbacks of the latter. Apart from the less calculation effort that is needed for the design of a resonant controller, the two advantages are certainly of high importance considering the usage of the FPGL. Firstly, a resonant controller is able to track a sinusoidal reference with zero steady state error and secondly, it has great disturbance rejection capability [24].

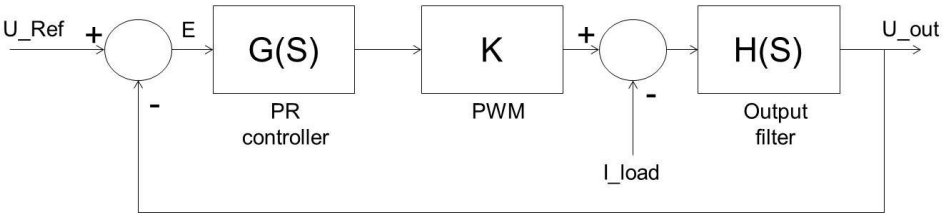


Figure 5-12 Control block diagram including plant and PR controller

With the help of Figure 5-12, the working principle of a PR controller is presented. The second order resonant terms represent sinusoidal signals of the specified frequency. Looking into it from the open-loop transfer function of the system, the resonators introduce theoretically infinite high gain (practically very large finite gain) at the specified resonant frequencies eliminating steady state error at that frequency, and is therefore conceptually similar to an integrator whose infinite dc gain forces the dc steady state error to zero.

$$U_{out} = \frac{K \cdot G(s)}{H(s) + K \cdot G(s)} U_{ref} - \frac{1}{H(s) + K \cdot G(s)} I_{load} \quad 5\text{-}13$$

The open loop transfer function shows that the output voltage depends on both the reference voltage and the load current (disturbance). The transfer functions of the PI and PR controller are the following [24]:

$$G_{PI}(s) = k_p + \frac{k_i}{s} \quad 5\text{-}14$$

$$G_{PR}(s) = k_p + 2k_r \frac{s}{s^2 + \omega_o^2} \quad 5\text{-}15$$

In steady state, the PI controller has finite at the fundamental frequency, and thus the second term of the open loop transfer function of the system cannot be neglected (not perfect disturbance rejection). In contrast the PR which provides an infinite open-loop gain makes the first term to approach the reference value and the second one the zero.

PR controllers can be extended easily to also control higher harmonic voltages with zero error [35]. Consequently, in the FPGL case, besides the single fundamental frequency compensation, selective harmonic compensation can also be achieved by cascading several resonant blocks tuned to resonate at the desired harmonic frequencies to be compensated for. Hence:

$$G_h(s) = \sum_h 2k_h \frac{s}{s^2 + (h \cdot \omega)^2} \quad 5\text{-}16$$

Where h is the harmonic order. It is worth noting that the proportional term is neglected, because the entire proportional part of the controller will be introduced by the Command Feed Forward (CFF). The transfer function of the resonators should be transformed to z-domain:

$$G_h(z) = \sum_h 2k_h \frac{z \cdot \left(z - cos(h \cdot \omega \cdot T_s)\right)}{z^2 - 2cos(h \cdot \omega \cdot T_s) + 1} \quad 5\text{-}17$$

The state space representation of the digital resonator for natural frequency ω_o:

$$A_{comp,z} = \begin{bmatrix} 0 & 1 \\ 1 & 2cos(\omega_o T_s) \end{bmatrix}$$

$$B_{comp,z} = \begin{bmatrix} 0 \\ 1 \end{bmatrix}$$

$C_{res,z}$ will be determined during the pole placement procedure of the state feedback and the feed-through matrix remains zero, because it will be determined from the CFF gain.

$$D_{comp,z} = [0]$$

The figure below is an example of the open loop transfer function of a PR controller, which is represented by the Bode plot. One can observe that at the fundamental frequency 50Hz as well as at the frequencies of 7 harmonics (3rd, 5th, 7th, 9th, 11th, 13th and 15th), the gain is large enough to compensate the error.

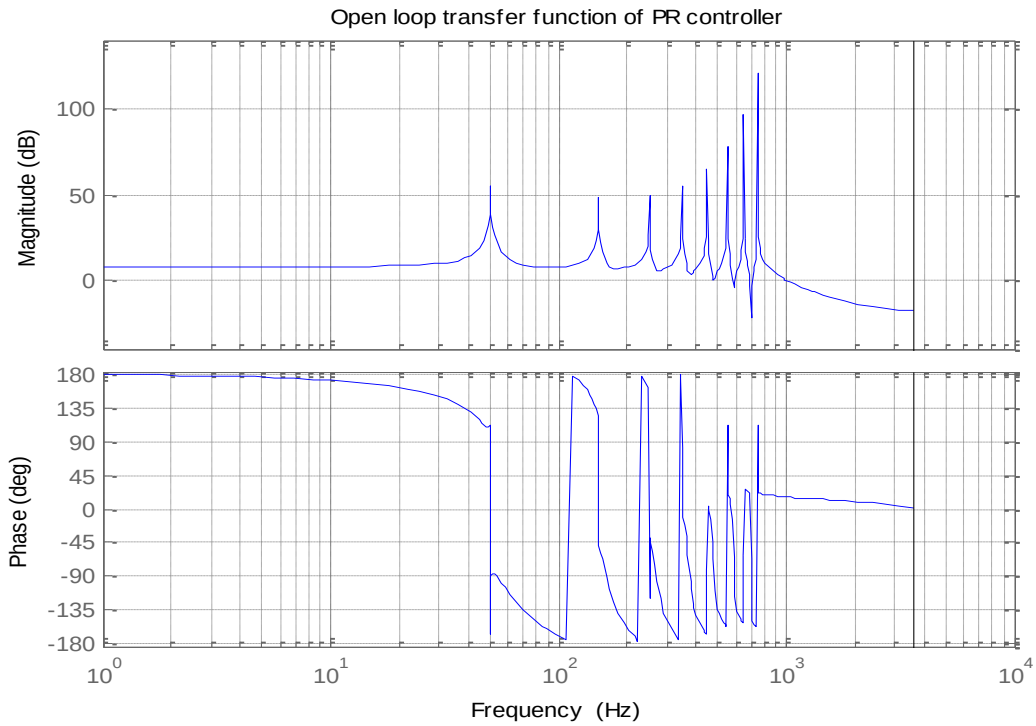


Figure 5-13 Bode plot of the open loop transfer function of a PR controller (fundamental + 7 harmonics)

Moreover, it is also interesting to present the corresponding closed loop command response, which is represented by the Bode plot as well. At the fundamental frequency 50Hz as well as at the higher harmonic frequencies, the Bode plot shows a magnitude of 0dB and phase 0^{o}.

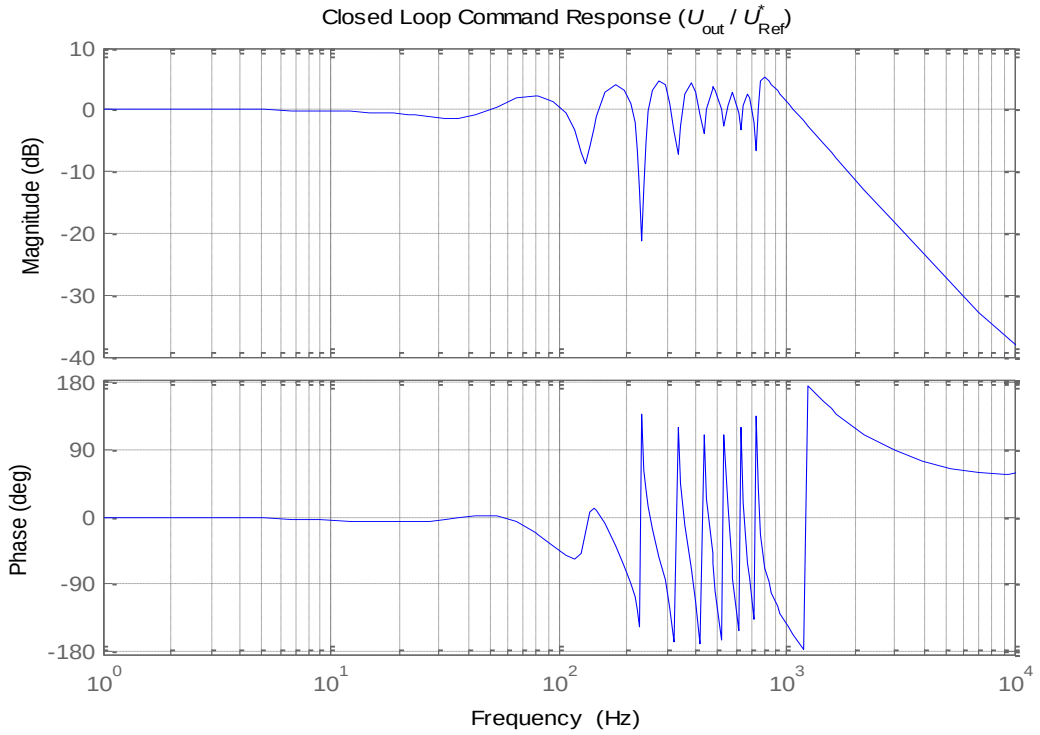


Figure 5-14 Bode plot of closed loop command response in harmonic mode (fundamental 50Hz + 7 harmonics)

2. *Dynamic Mode:*

Respectively, when the purpose of the test is to study on dynamic voltage phenomena, the compensator is turned to a first-order I-controller, whose transfer function in z-domain is:

$$G_{PI}(z) = k_i \frac{z}{z-1} \qquad 5\text{-}18$$

And the state space representation:

$$A_{comp,z} = [1]$$

$$B_{comp,z} = [1]$$

$$D_{comp,z} = [0]$$

The proportional term is neglected again and the output matrix will be determined during the pole placement.

To sum up, in the m-file, the compensator is represented in state-space either in harmonic mode or dynamic mode. Once in the next step of the system stabilization, the output matrix C is determined, then the transfer function of the compensator can also be determined and the compensator itself will be represented in the Simulink model as an LTI system (Linear Time-Invariant system). Bear in mind that the transfer function of the compensator refers to one phase.

- *System Stabilization*

Our system has already been augmented to 3rd order (LC filter including PWM) plus the order of the compensator. This means that in case of use of ten resonant controllers (2nd order each), the order of the systems becomes 23rd. To achieve stabilization of this system two architectures are suitable. The first is the cancellation controller, which inverts the plant model to cancel out the plant's poles by the zeros of their transfer functions and replace the plant's poles with their own ones [33]. The second strategy, which is the selected one, is the state feedback control. This architecture is explained in all modern control theory handbooks, such as the [36], and according to that, proportional feedback of all states is applied to shift the plant's poles to the desired locations. Due to the fact that the compensator increases the order of the system and its dynamics change the structure of the plant, it should be taken into account in the pole placement procedure. Hence, the state space matrices of the plant including the compensator and the output feedback are as follows:

$$A_{pl+comp,z} = \begin{bmatrix} A_{plant,z} & 0 \\ -B_{comp,z}C_{plant,z} & A_{comp,z} \end{bmatrix}$$

The term $-B_{comp,z}C_{plant,z}$ represents the negative unity output feedback.

$$Bu_{pl+comp,z} = \begin{bmatrix} 0 \\ B_{comp,z} \end{bmatrix}$$

$$Bz_{pl+comp,z} = \begin{bmatrix} Bz_{plant,z} \\ 0 \end{bmatrix}$$

$$C_{pl+comp,z} = [C_{plant,z} \quad 0]$$

$$D_{pl+comp,z} = [0]$$

The state space equations of the plant are:

$$\dot{x}_{pl+comp}(k+1) = A_{pl+comp,z} \cdot x_{pl+comp}(k) + \\ +Bu_{pl+comp,z} \cdot w_{pl+comp}(k) + Bz_{pl+comp,z} \cdot z_{pl+comp}(k) \quad 5\text{-}19$$

$$y(k) = C_{pl+comp,z} \cdot x_{pl+comp}(k) + D_{pl+comp,z} \cdot w_{pl+comp}(k) \quad 5\text{-}20$$

Where:

State vector: $$x_{pl+comp}(k) = \begin{bmatrix} i_{Lf}(k) \\ U_{Cf}(k) \\ U_{PWM}(k) \\ \zeta(k) \end{bmatrix}$$

where $\zeta(k)$ describes the states of the resonators or the I-controller, which is actually the control error.

Input vector: $$w_{pl+comp}(k) = [U^*_{REF}(k)] = [U_{REF}(k+1)]$$

Disturbance input vector: $$z_{pl+comp}(k) = [i_{load}(k)]$$

Output vector: $y(k) = [U_{out}(k)]$

Once the entire system to be stabilized has been determined, the next step is to determine the target poles. Obviously, the number of the target poles will be the same as the order of the system. The vector of the target poles of the plant (filter and PWM generator) is generated by choosing a frequency based on two criteria: high enough frequency which achieves sufficient dynamics and low enough frequency in order to keep it well below the dead-beat location [33]. In discrete-time control theory, the dead-beat control problem consists of finding what input signal must be applied to a system in order to bring the output to the steady state in the smallest number of steps. The characteristics that need to be fulfilled are: zero steady state error, minimum rise time, minimum settling time and less than 2% over/undershoot. For N-th order linear system it can be shown that the minimum number of steps will be at most N. The solution is to apply feedback such that all the poles of the closed loop transfer function are at the origin of the z-plane. The FPGL control system operates with chosen target frequency 660Hz, which was found to fulfill the above criteria. This frequency corresponds to following value in z-plane:

$$p_{target,pl,z} = exp\left(-2\pi \cdot f_{target,pl} \cdot T_s\right) \quad 5\text{-}21$$

The pole placement is done in MATLAB, using the *place* function. It is worth noting that this routine is unable to place more than one poles at the same location and consequently the two other poles are a bit displaced; the vector of the target poles of the 3rd order plant is:

$$p_{plant,z} = [p_{target,pl,z} \quad p_{target,pl,z} + 0.01i \quad p_{target,pl,z} - 0.01i] \quad 5\text{-}22$$

The target pole vector should also include the target poles of the compensator, which can be determined by calculating the eigenvalues of the system matrix $A_{comp,z}$. Additionally, the target poles of the compensator are dependent on the time constant T_r (action rate of the resonator) or T_i (integral time constant of the I-controller). This time constant sets the distance of the closed loop poles of the compensator from the unity circle in z-plane [27]. In our converter control this constant is set to 4ms and finally the target poles of the compensator are given by [33]:

$$p_{comp,z} = exp\left({}^{T_s}/_{T_r}\right) \cdot eig(A_{comp,z}) \quad 5\text{-}23$$

Once the target poles vector has been determined (consists of both $p_{plant,z}$ and $p_{comp,z}$), the *place* routine of MATLAB, returns the feedback matrix (state feedback). The gains that comprise this matrix relocate the poles of the closed loop transfer function and keep the system stable. The gains that correspond to the compensator, comprise actually the output matrix of it $C_{comp,z}$, which was not determined before. So, finally the state-space representation of the compensator is complete and hence it is now possible to determine its transfer function and represent it in Simulink using an LTI system (see APPENDIX E). In APPENDIX E the Simulink representation of the state feedback is shown as well. The representation is the result of a simple sum of the three state variables multiplied by the corresponding gains K_1, K_2 and K_3 of the third order system:

$$[K_1 \quad K_2 \quad K_3] \cdot \begin{bmatrix} i_{Lf} \\ U_{Cf} \\ U_{PWM} \end{bmatrix} = K_1 \cdot i_{Lf} + K_2 \cdot U_{Cf} + K_3 \cdot U_{PWM} \quad 5\text{-}24$$

Figure 5-15 illustrates the zero-pole plot of the closed loop system (example fundamental 50Hz + harmonics) in harmonic and dynamic mode. One can observe that all the poles are in the unity circle and thus indeed the system remains stable.

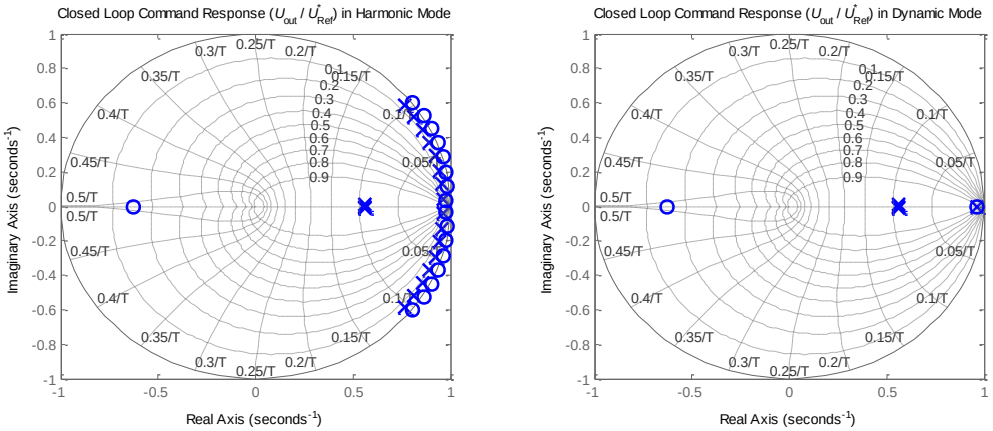


Figure 5-15 Pole zero plots (z-plane) of closed loop command response in Harmonic and Dynamic Mode

- *Command Feed Forward*

So far, in the modeling and control procedure the feed-through matrix remained equal to zero. The command feed forward is now necessary to be determined, in order to correct the dc gain of the plant. The plant's system matrix, with closed state feedback loop is $\left(A_{plant,z} + B_{plant,z} \cdot K\right)$. This system matrix along with $B_{plant,z}$, $C_{plant,z}$ and $D_{plant,z}$ represent the closed state feedback loop plant. In harmonic mode the reciprocal of the dc gain of this system gives the CFF, which is a single gain [33]. The *dcgain* MATLAB function is used for this calculation.

$$k_{cff} = \frac{1}{dcgain(plant\_sf)} \tag{5-25}$$

When the controller operates in dynamic mode the CFF gain is:

$$k_{cff} = \frac{C}{1-p} \tag{5-26}$$

Where C is the gain that results from the pole placement and p the target pole specified for the I-controller.

- *Disturbance Feed Forward*

Finally the last part of the model that needs to be calculated is the DFF, which improves the disturbance rejection. From the above state-space representation (see CFF), the transfer functions for command input Gu_{plant_sf} and disturbance input Gz_{plant_sf} are determined. The *dcgain* function returns the DFF gain [33]:

$$k_{dff} = dcgain\left(\frac{Gz_{plant\_sf}}{Gu_{plant\_sf}}\right) \tag{5-27}$$

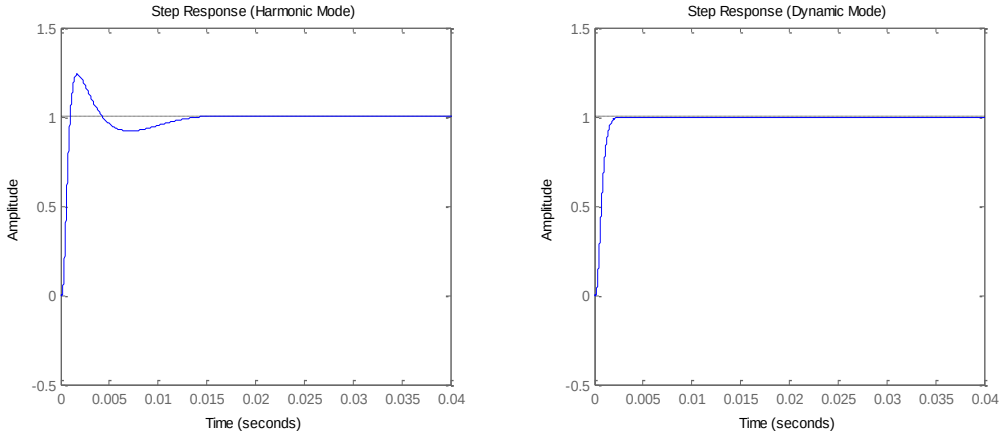


Figure 5-16 Step response of the closed loop system in Harmonic and Dynamic Mode

As expected, in dynamic mode because of the I-controller, the response goes much faster to steady state. However, the figure below ensures the perfect compensation of steady state error in harmonic mode, whereas in dynamic mode the I-controller cannot perfectly eliminate the error (the grey line is the command input and the blue one is the response).

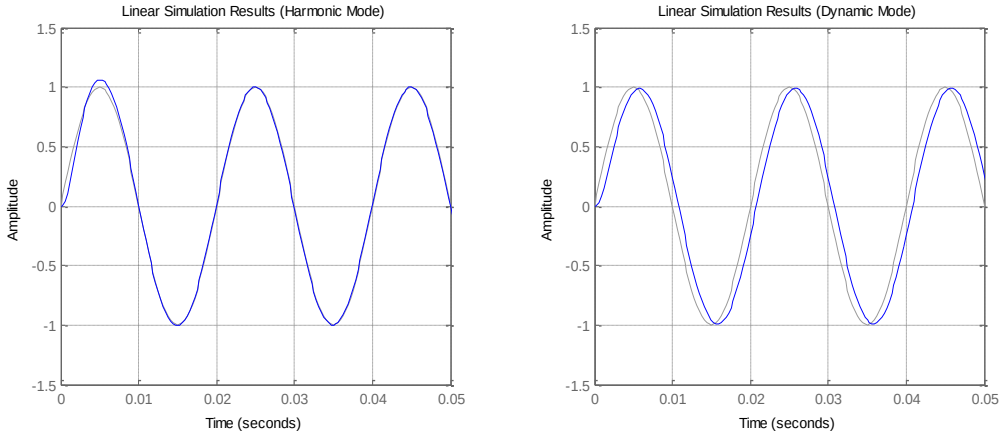


Figure 5-17 Time response of the closed loop system in Harmonic and Dynamic Mode

5.4.3 Simulations & conclusions

The model allows the user to choose the PWM frequency according to their needs, which can go up to 3.6kHz. Through input dialog boxes and subsystem masks that have been developed, the user is able to input the PWM and fundamental frequency, the operation mode, the amount of resonant controllers in case of harmonic mode, the harmonic order for each resonant controller, as well as the amplitude and phase of both fundamental and harmonics.

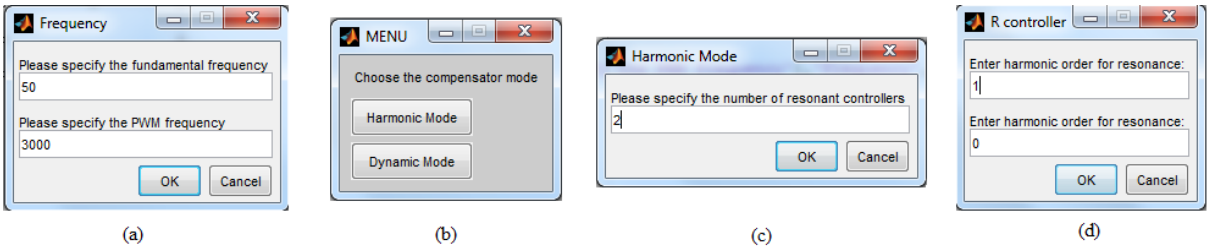


Figure 5-18 Input dialog boxes for (a) fundamental and switching frequency, (b) operation mode, (c) amount of resonant controllers, and (d) order of each resonant controller

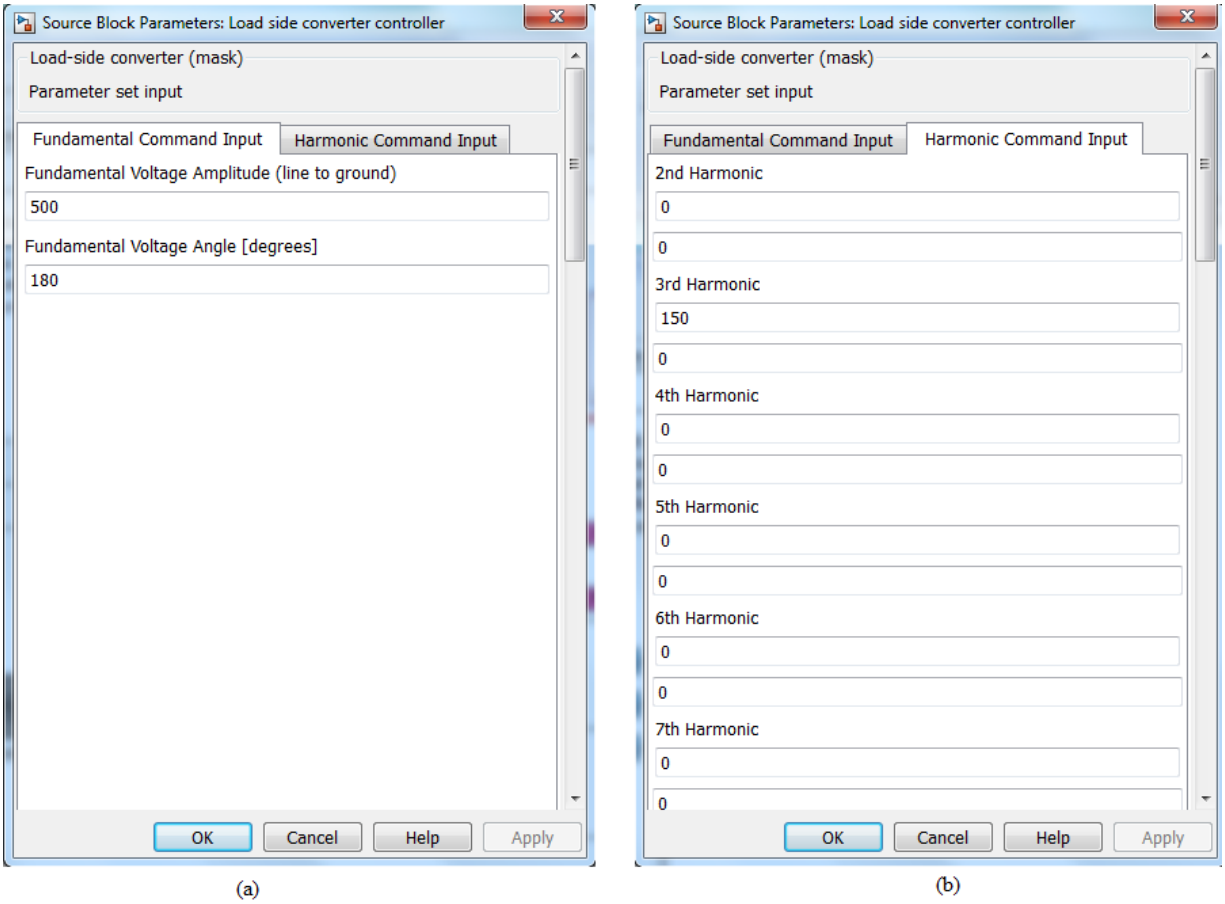


Figure 5-19 Masked load-side controller block – Input interface for (a) fundamental and (b) harmonic command input

The following graphs give a first impression of the controller performance. The switching frequency that is used is 2.4kHz and all the simulations are at full load conditions (1MW). The sampling frequency, apart from the first simulation where the synchronized PWM is shown (single update mode), is chosen to be twofold the PWM frequency (double update mode). Also the nominal frequency is 50Hz.

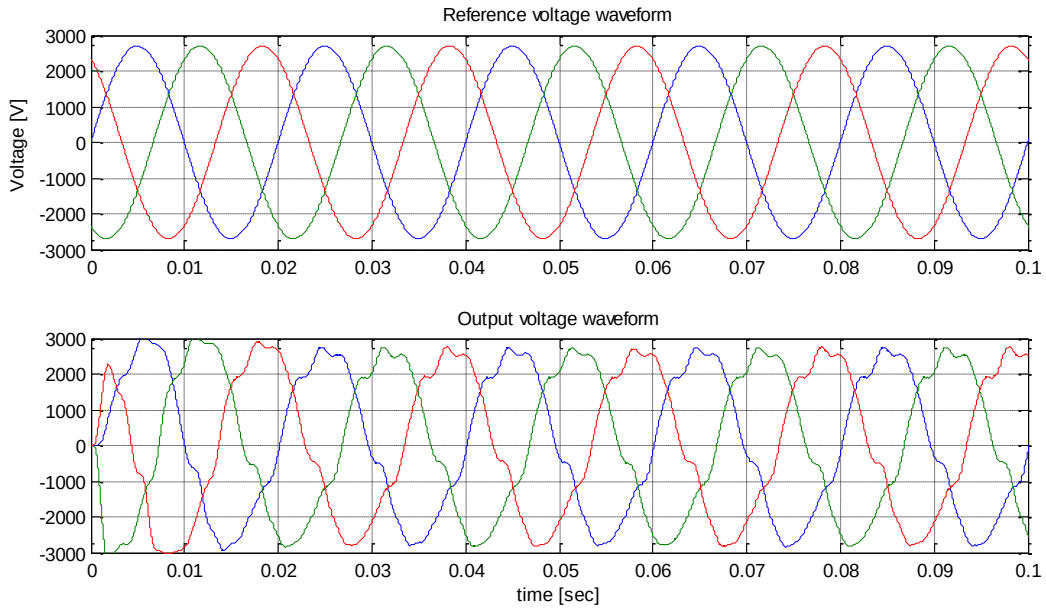


Figure 5-20 Reference and output voltage for symmetrical sampling and PWM

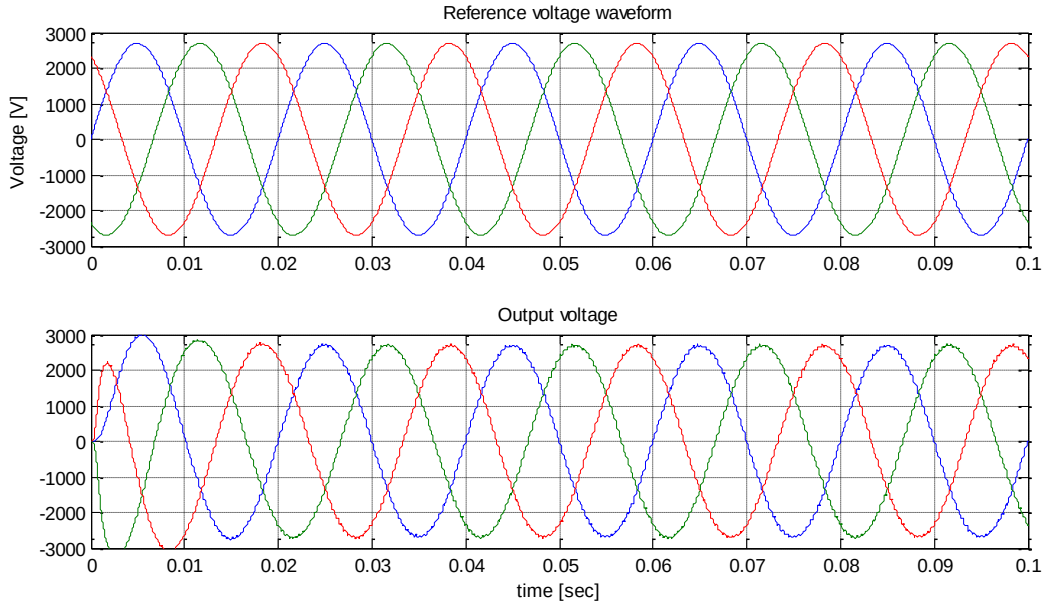


Figure 5-21 Reference and output voltage for asymmetrical sampling and PWM

As expected, Figure 5-20 and Figure 5-21 confirm that the non-synchronized sampling and switching frequency have better performance. It is interesting to present the unfiltered PWM waveforms, where the three levels of the converter are obvious.

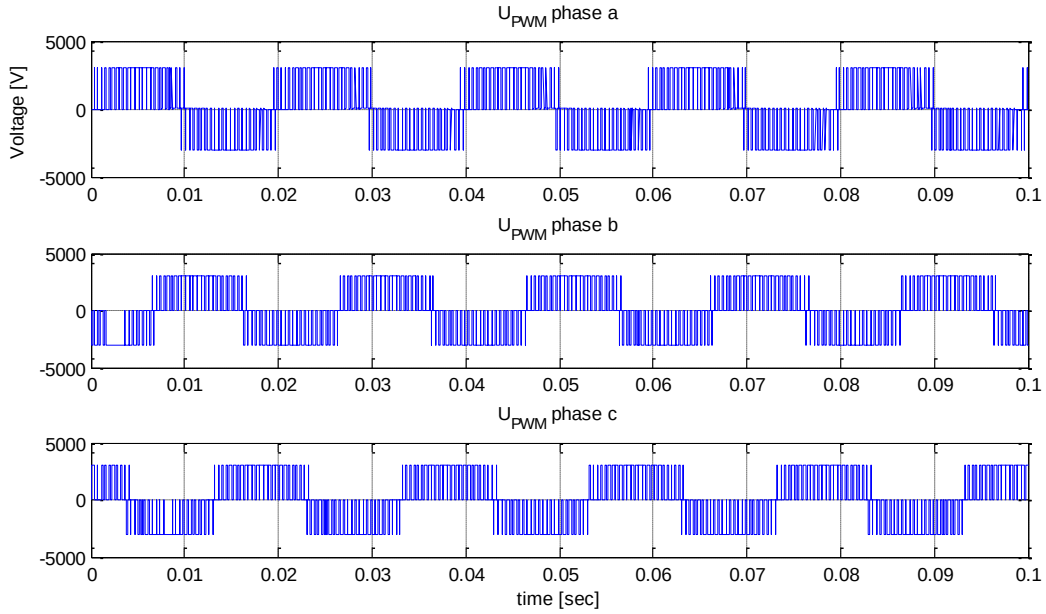


Figure 5-22 Phase PWM output voltage

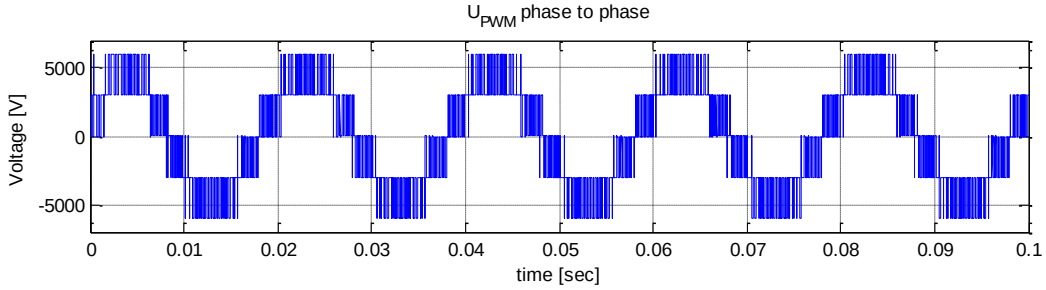


Figure 5-23 Phase to phase PWM output voltage

Figure 5-24 shows the performance of the controller when some harmonics are also included. The PWM frequency and hence the sampling frequency are increased for better performance. All the odd harmonics up to 15^{th} are superimposed on the fundamental 50Hz. The harmonic level is at the maximum values under nominal operating conditions according to EN 50160.

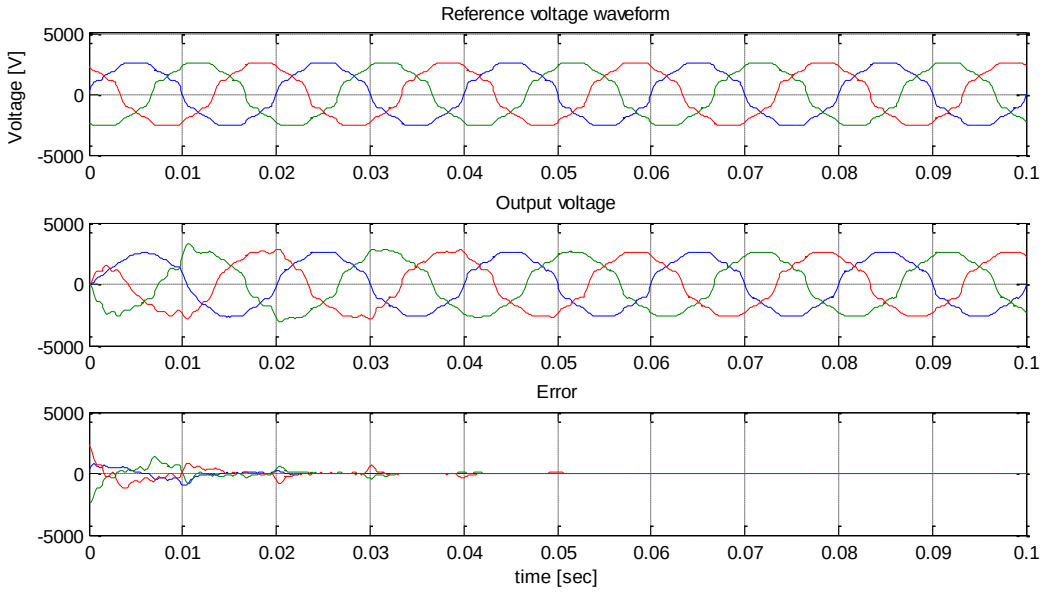


Figure 5-24 Reference, output voltage and error. All measured in discrete domain.

5.5 Grid-side Converter / Active Front End

The FPGL allows regeneration of power back to utility and because of this, a simple, low-cost uncontrolled or semi-controlled rectifier would not be enough. An uncontrolled diode rectifier produces a fixed dc voltage and it has the advantages of its simplicity and low cost. However, it does not offer the possibility of control of the power flow, it generates high harmonics at the input current and moreover it does not allow regeneration of power. A semi-controlled thyristor rectifier has in general the same advantages and limitations as the diode rectifier, but it has the advantage that operating with a firing angle >90^{o} it can regenerate power from the dc load to the ac supply [37].

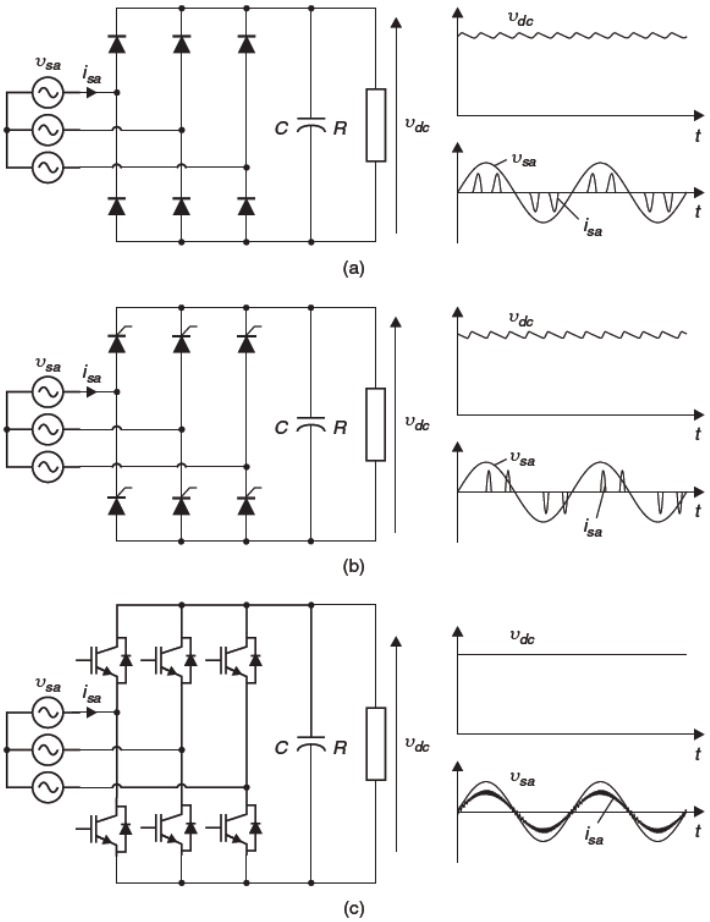


Figure 5-25 Three-phase rectifier (a) diode rectifier (b) thyristor rectifier and (c) AFE [37]

The Active Front End (AFE) utilizes a PWM controlled IGBT converter to allow bi-directional power flow to the AC line. Although nowadays the initial cost of an AFE is higher than a diode bridge rectifier, it has a lot of advantages that finally compensate the cost difference. More specifically the AFE eliminates the need for large resistor banks. When the speed of an inverter-controlled ac motor is reduced, the motor acts as a generator, feeding back energy to the frequency converter. As a result, the voltage in the intermediate circuit of the inverter increases. When a specific threshold is exceeded, the energy must flow to an external breaking system in order to avoid drive failures. Braking resistors are designed to absorb such energy and dissipate it into heating. These resistor banks can create a lot of heat and must frequently be cleaned. Hence, instead of wasting energy with resistor braking technology, regenerative breaking actually puts the energy back into the system to be used by other equipment [38], [39]. Moreover the AFE itself actively controls the power factor regardless the load. The ac current is in phase with voltage and thus the AFE does not exchange reactive power with the line, but exclusively active power. Practically it is possible to say that the AFE usually allows eliminating power factor correction systems. In a nutshell, the AFE has the capability of complete energy reversibility (full regenerative operation), complete control of reactive power (operation with very high power factor), control of harmonics (control of input currents with sinusoidal waveforms) and control of the DC voltage. Moreover, it is worthy to say that the AFE allows input voltage boost operation, which helps protect critical processes from the potentially disruptive effects of input voltage dips and sags.

5.5.1 Topology & Specifications

The AFE input filter and its specifications are presented in this paragraph.

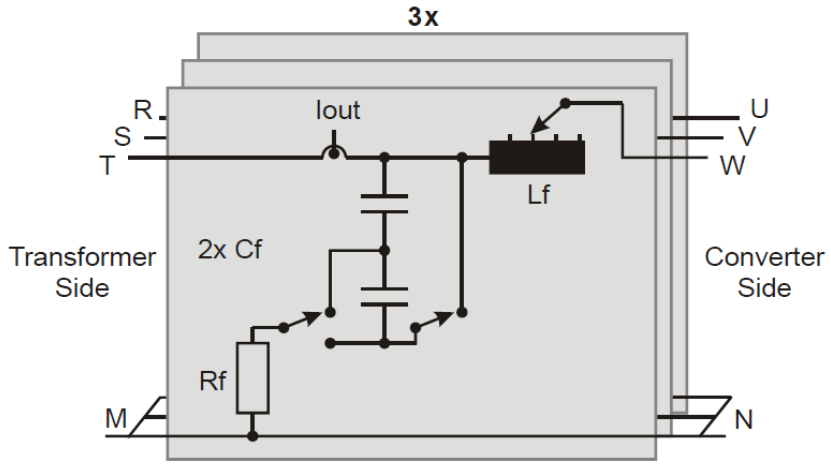


Figure 5-26 AFE input filter

The filter contains three phases and each phase consists of an L-C-R filter in L-connection. The inductance of the filter is used to extract the modulation from the signal and make a sinusoidal voltage and current. The capacitor consists of two capacitors, which can be connected individually, parallel or serial. To support a serial connection, parallel resistors must exist which guarantee equal voltage sharing. The functionality of the capacitor is to protect the transformer insulation of exposing itself in high dv/dt, which could lead it to failure as well as provide a low impedance path for high frequency PWM ripple and thus attenuate the content of current ripple in utility current.

Specification		Value
Rated frequency (Hz)	Hz	50
Inductor Lf	mH	0.5 (0.3; 0.1)
Parasitic Resistance RLf	mΩ	7
Capacitor Cf	nF	50±5%
Parasitic Resistance RCf	mΩ	100
Resistor Rf	Ω	33 (22; 15)

Table 5-2 Input filter specifications

Similar to the output filter, the model is built in Simulink using components from the SimPowerSystems Toolbox. Please refer to APPENDIX E, where the plant of the system as developed in Simulink is depicted.

5.5.2 Mathematical representation, modeling & control

In the beginning of this analysis, the main objectives of the control and the assumptions that have been made during the modeling procedure are stated. As mentioned before, the control scheme of the AFE is being developed in the rotating reference frame using PI controllers. Hence Park transformation is necessary to transform the system from the stationary abc frame to the rotating dq0 frame. You can refer to APPENDIX F for details.

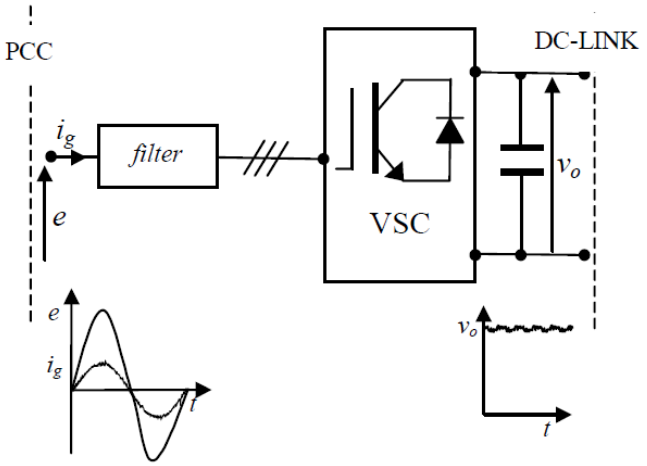


Figure 5-27 VSC used as active rectifier with a sketch of the desired grid current i_g in phase with the grid voltage e and the desired dc voltage v_o [40]

The main objective of the controller is to keep the dc-link voltage to the level that the reference indicates. As it will be explained later, the dc voltage can be controlled by controlling the active power and hence the current at the ac side. However, it is of high importance that the right selection of the control point at the ac side is made. It is not possible to choose the measurement point at the terminals of the converter, because the current at that point is highly distorted by harmonics. A possible point would be the grid side terminals of the input filter. However, depending on the value of the filter inductance the harmonic distortion may still be considerable. In the case of the FPGL, the converter operates always connected to the transformer TR3/T3. This is the step-down transformer that transforms the 10.5kV of the grid to either 3800V or 1900V or 950V (3 tap positions). This fact makes possible the even more efficient control of the input current, as it becomes possible to take the impedance of the transformer into account and set the measurement point at the high voltage side of that, where the Point of Common Coupling (PCC) is also located. Consequently, the input filter of the AFE is an LCL filter. Moreover a Phase Locked Loop (PLL) will be used for the synchronization of the grid-interfaced converter with the utility network.

5.5.2.1 Plant model

The converter is modeled in Simulink using the switching devices of the library. The single phase equivalent circuit of the LCL filter is depicted in Figure 5-28. E represents the high voltage of the transformer TR3/T3 and V_{conv} the voltage at the terminals of the converter.

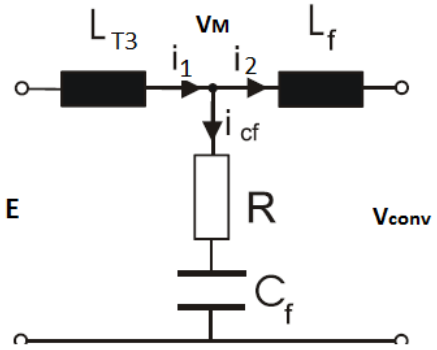


Figure 5-28 Single phase equivalent of the AFE LCL filter.

The system can be represented as a 3rd order transfer function (per phase representation). The equations of the 3rd order system (taking also into account the parasitic resistors of the inductances and the capacitor) in the stationary abc frame are:

$$L_{T3}\frac{di_1}{dt} = E - V_M - R_{T3}\cdot i_1 \quad 5\text{-}28$$

$$C_f\frac{dV_{Cf}}{dt} = i_1 - i_2 \quad 5\text{-}29$$

$$L_f\frac{di_2}{dt} = V_M - V_{conv} - R_{Lf}\cdot i_2 \quad 5\text{-}30$$

Respectively, modeling the LCL filter in a dq reference frame gives:

$$L_{T3}\frac{di_1^{dq}}{dt} = E^{dq} - V_M^{dq} - (R_{T3} + j\omega L_{T3})\cdot i_1^{dq} \quad 5\text{-}31$$

$$C_f\frac{dV_{Cf}^{dq}}{dt} = i_1^{dq} - i_2^{dq} - j\omega C_f V_{Cf}^{dq} \quad 5\text{-}32$$

$$L_f\frac{di_2^{dq}}{dt} = V_M^{dq} - V_{conv}^{dq} - \left(R_{Lf} + j\omega L_f\right)\cdot i_2^{dq} \quad 5\text{-}33$$

It is obvious that in dq frame, the representation of an LCL filter is augmented to 6th order and hence the control and decoupling of such a large system becomes very complex. In low frequency range the LCL filter behaves similar to the L-filter. The control will mostly act in this frequency range (up to 1800Hz which is the switching frequency of the PWM generator of the AFE). Therefore, a designer needs to model the system in the rotating frame of the L filter-based active rectifier for the control [41]. As a result:

$$L_{tot}\frac{di^{dq}}{dt} = E^{dq} - V_{conv}^{dq} - (R_{tot} + j\omega L_{tot})\cdot i^{dq} \quad 5\text{-}34$$

Where L_{tot} is the sum of the transformer and the filter inductance, R_{tot} the sum of the parasitic resistance of the filter and the dc resistance of the transformer windings, i and E are the current and the voltage respectively, at the high voltage side of the transformer. Hence, with this simplified filter scheme, the transfer function of the system is:

$$G(s) = \frac{i^{dq}}{V_{conv}^{dq}} = -\frac{1}{R_{tot} + sL_{tot} + j\omega L_{tot}} \quad 5\text{-}35$$

Multiplication by j maps the d axis on q axis and vice versa. It is important to cancel this cross coupling, because a PI current controller has no satisfactory tracing performance for the coupled system. The decoupled system transfer function is [30], [41], [42]:

$$G(s) = \frac{1}{R_{tot} + sL_{tot}} \quad 5\text{-}36$$

Although the modeling of the plant is done using switching devices and components from Simulink library, the numerical representation of the system helps the controller design process. The figure below provides a better understanding of the abc and dq representation of the electric circuit.

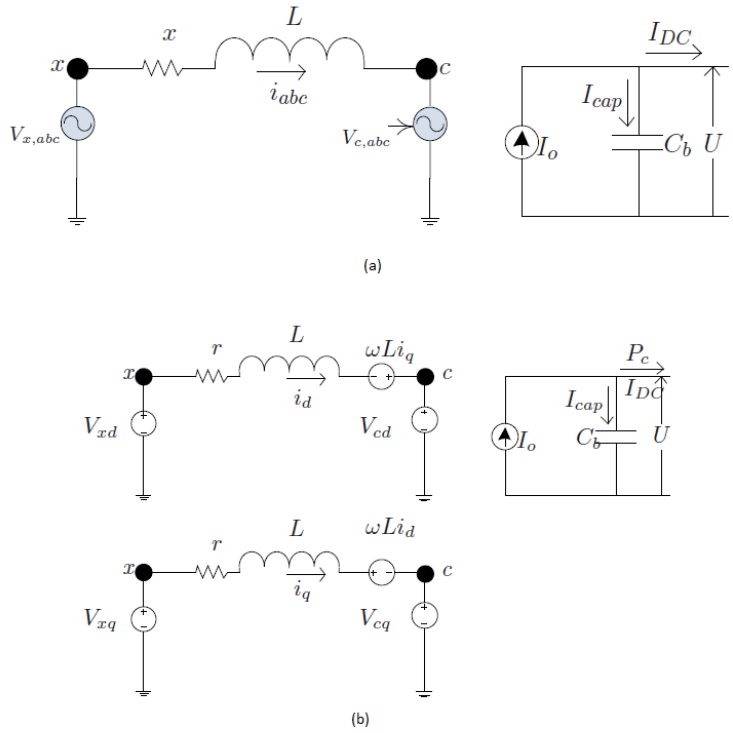


Figure 5-29 Electric circuit of the VSC in (a) abc frame and (b) dq frame [31]

The dc-link is represented by pure capacitance. The dc-link capacitors are 1.5mF (2 of 750uF, 3%, 3.1kV) each and there are 4 in parallel between the (+) and the mid-point M and 4 in parallel between M and the (-) terminal, per converter cabinet. Therefore, in total there is 12mF between +dc and M and 12mF between M and –dc, and in this simple way, with two pure capacitors the dc-link is modeled.

5.5.2.2 Controller

Several different control architectures have been developed, to control the dc-link voltage, the active and reactive power using an AFE. In [37] some of these methods are presented and been compared to each other.

The FPGL controller design of the grid-side PWM converter is based on the vector control method. This method requires modeling of three phase systems by using axis transformations. Nowadays vector theory is probably the most dominant control approach of three-phase PWM converters. In PWM converters for ac applications, vector control systems can be utilized to obtain independent control of the active and reactive power. Vectors of ac currents and voltages occur as constant vectors in steady state and hence static errors in the control system can be avoided by using PI controllers [43].

More specifically, the working principle is based on the vector control, which is carried out in the rotating frame that is being rotated with the angular velocity of the grid. In order to ensure that the rotating frame holds always the frequency of the grid, a PLL is used. The line voltage U_{abc} feeds the

PLL and the angular velocity that is calculated in the PLL is used for the stationary to dq-coordinate transformation of the line current and voltage and vice versa.

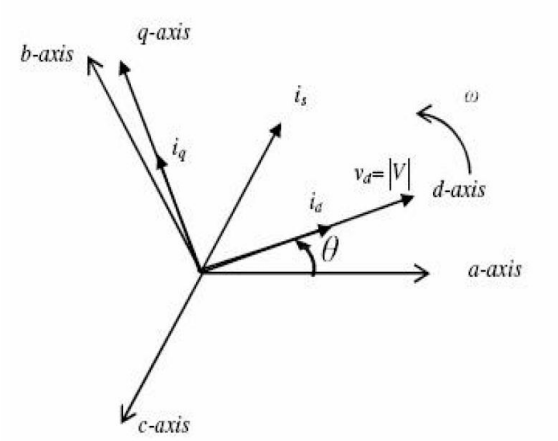


Figure 5-30 The rotating dq reference frame in respect with the reference frame

The analysis of the line current and voltage in dq coordinates is depicted in figure above. To make the analysis easier, it is possible to make the following assumption: the voltage vector coincides with the d-component and as a result $v_d = |V|$ and $v_q = 0$. In order to achieve that, the dq reference frame is selected in such a way that the d-axis is aligned to the voltage phasor of phase-a. In other words the PLL should be phase locked to phase-a voltage phasor of the measurement point (in Figure 5-30, θ=0).

It is known that the instantaneous active power in a three-phase system at the reference point (PCC) is given by:

$$P(t) = v_a i_a + v_b i_b + v_c i_c \tag{5-37}$$

Respectively, in the dq-reference frame the power is given by (amplitude invariant transformation):

$$S = \frac{3}{2} v_{dq} i_{dq}^{*} = \frac{3}{2}(v_d + jv_q)(i_d - ji_q) = \\ = \frac{3}{2}\left[(v_d i_d + v_q i_q) + j(v_q i_d - v_d i_q)\right] \Rightarrow \tag{5-38}$$

Hence

$$P = \frac{3}{2}(v_d i_d + v_q i_q) \tag{5-39}$$

$$Q = \frac{3}{2}(-v_d i_q + v_q i_d) \tag{5-40}$$

Taking into consideration the previous assumption:

$$P = \frac{3}{2} v_d i_d = \frac{3}{2}|V| i_d \tag{5-41}$$

$$Q = -\frac{3}{2} v_d i_q = -\frac{3}{2}|V| i_q \tag{5-42}$$

According to equations 5-41 and 5-42, the active and reactive power, which are transferred from the converter to the grid and the other way around, are functions of the d and q current components

respectively (at the PCC). Hence, regulating the two current components, control of the active and reactive power exchange is possible. Of course the ultimate goal is to control and keep the dc-link voltage constant.

The idea is based on the power balance along the path from the ac to the dc side. The controller consists of two regulators: the inner current regulator and the outer dc-voltage controller. The inner controller is the active current or active power controller. For steady state operation, active power exchange at the PCC, P_{ac}, will be equal to the power exchange at the dc side, P_{dc}. Neglecting the filter and semiconductor losses:

$$P_{ac} = P_{dc} \tag{5-43}$$

$$\frac{3}{2} v_d i_d = V_{dc} I_{dc} \tag{5-44}$$

$$I_{dc} = \frac{3 v_d i_d}{2 V_{dc}} \tag{5-45}$$

In case that the d-component was not aligned with the voltage vector, q-component would also be involved in equation 5-45. Thus, the previous assumption enables fully decoupled control of active and reactive power. The converter, as seen from the dc network side, will be a constant current source of magnitude I_{dc}. As a result, from equation 5-45, it can be deduced that regulating the ac active power at the PCC and hence i_d, it is possible to keep the dc-link voltage constant [31]. Based on this equation along with the differential equation 5-34, the inner current regulator can be formed (see Figure 5-32). The cross-coupling currents as seen in the differential equation are compensated by feed-forward terms.

The reference for the inner current controller, i_d^* comes from the dc voltage controller which is the outer controller of the scheme. The complete power balance at the capacitor of the dc-link is given by:

$$P_{ac} = P_{dc} + P_{cap} + P_{loss} \tag{5-46}$$

Where P_{ac} is the power exchange at the PCC, P_{dc} is the power exchange at the dc side (load), P_{cap} is the power exchange at the capacitor branch and P_{loss} includes the filter and semiconductor losses. Equation 5-46 can be rewritten:

$$\frac{3}{2} v_d i_d = P_{dc} + V_{dc} i_{cap} + P_{loss} \tag{5-47}$$

$$i_{cap} = \left(\frac{3 v_d i_d}{2 V_{dc}} - \frac{P_{dc} + P_{loss}}{V_{dc}} \right) \tag{5-48}$$

The same current in terms of voltage across the capacitor is given by:

$$i_{cap} = C_{dc} \frac{dV_{dc}}{dt} \tag{5-49}$$

Combining the equations 5-48 and 5-49:

$$\frac{dV_{dc}}{dt} = \frac{3v_d i_d}{2C_{dc}V_{dc}}\left(i_d - \frac{2(P_{dc}+P_{loss})}{3v_d}\right) \quad 5\text{-}50$$

This equation shows that regulating the active current, the dc-link voltage is kept constant, or equally $\frac{dV_{dc}}{dt}$ is close to zero. Let's say for example that the power demand at the dc side increases at a certain moment. As a result, instantly $\frac{dV_{dc}}{dt}$ loses its balance from zero and becomes negative. Then the outer voltage controller sees the error and modifies its output which is the reference value for the i_d. Consequently, the dc voltage returns to its initial reference value, while the current is regulated in such a way to provide more active power to cover the demand from the load.

The following scheme shows the entire block diagram, as it is implemented in Simulink (APPENDIX E) including the four main parts of the model: the PLL, the decoupled controller composed by a current and voltage controller, the PWM block and the three-level IGBT converter model including L filter. The measurement point at the ac side is selected to be at the PCC, and the LCL filter is simplified to an L filter, consisting of the inductance of the filter itself and of the transformer TR3/T3 (also including their resistances).

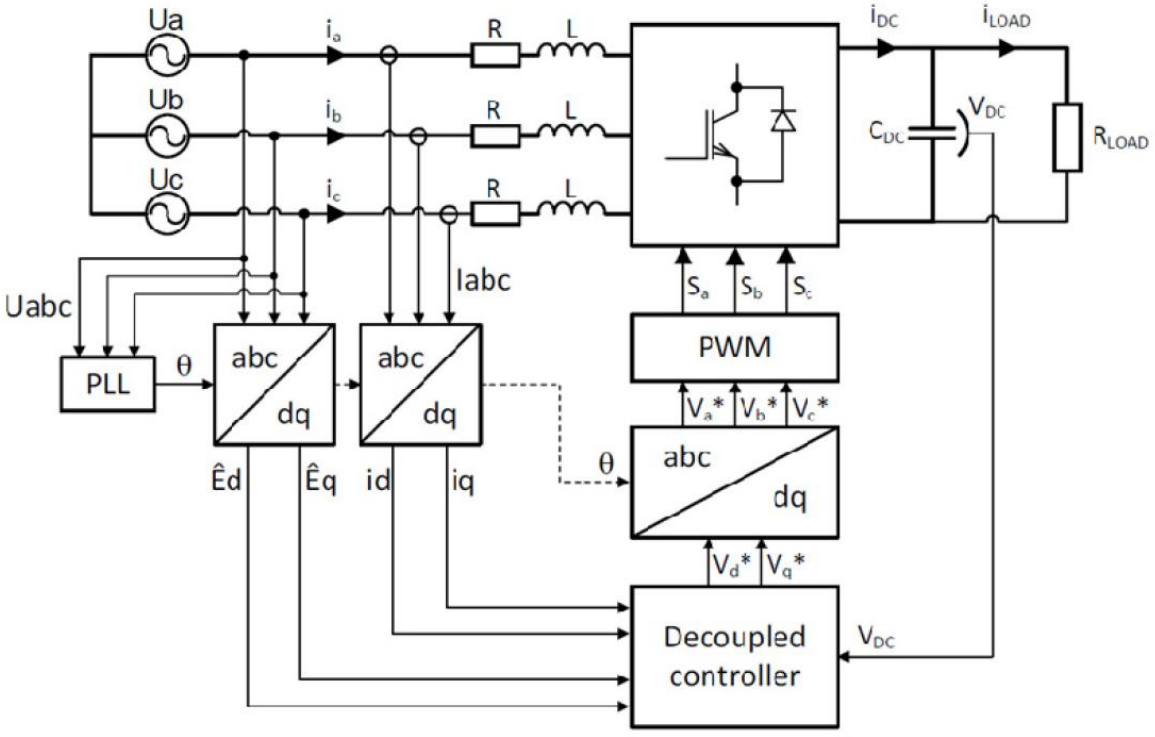


Figure 5-31 Vector control block diagram [30]

In order to maintain the dc-link voltage constant, the controller compares the instantaneous dc voltage with the reference, and the error passes through a PI controller (outer control). The output of the PI controller determines the required current of the d component, which will keep the dc voltage stable and it is called reference current I_d^*. This current will be compared with the actual I_d, which comes from the dq transformation of the current measurement. The result passes from a PI controller and the output is the reference d-component of the voltage, V_d* (inner control). Similarly, it is possible to implement also reactive power controller by regulating the q-component of the

current and determining the I_q*. In this way, through this controller the grid can be supported with reactive power exchange when it is needed (reactive power compensation). Finally, once the two reference voltage components have been calculated, V_d* and V_q*, they are being back-transformed to the stationary abc reference frame. Then V_a*, V_b* and V_c* divided by $V_{dc}/2$ (for 3-level topology) give the modulation indices, which are the required input for the PWM generator. It is worth noting that in FPGL case there is no reactive power control implemented in the scheme and hence I_q*=0. Figure 5-32 illustrates the block diagram of the decoupled controller.

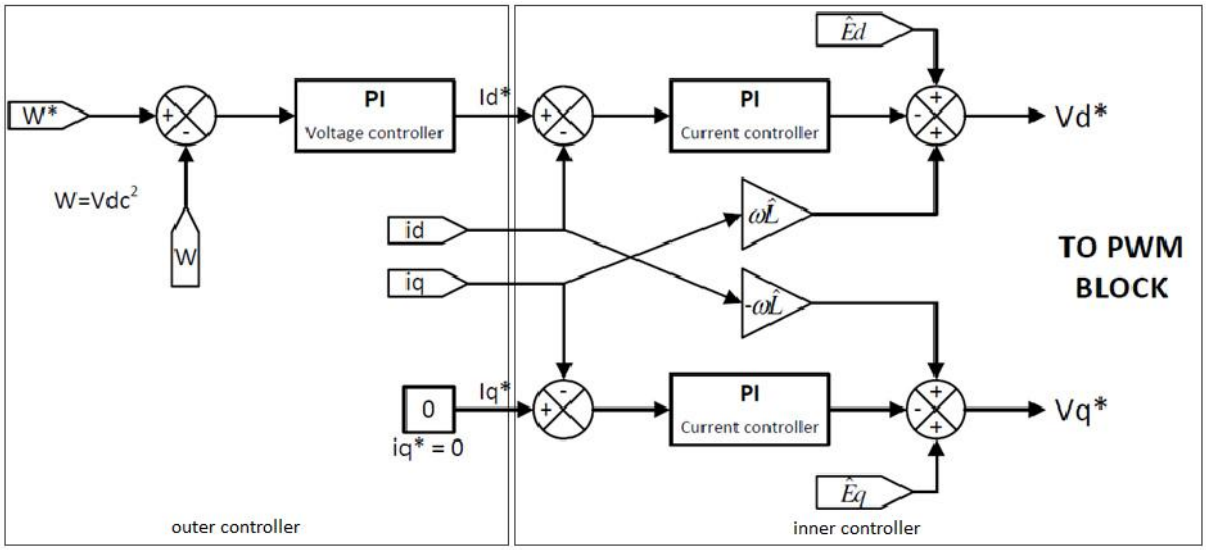


Figure 5-32 Decoupled controller [30]

It is worthy to state the important points and assumptions of the implemented controllers:

1. The reference value for the q-component of the current is set to zero, because it is assumed unity power factor and hence no reactive power exchange.
2. The decoupling of the controller, which is necessary for high tracking performance of the PI controllers, is achieved by the multiplication of the actual measured values of i_d and i_q by the gain ωL. The results of these values are implemented as feed-forwards in the scheme.
3. As mentioned above the measured voltage values at the PCC, E_d and E_q comprise disturbance input for the system. Hence, these values are implemented as DFF. Of course, due to fact that the line voltage vector is aligned to the d-axis, E_q=0.
4. Because the transformer impedance plays a significant role in the system and its control, it is more convenient to implement the controller in per unit. It makes it more generic and misunderstandings due to the two voltage levels of the system are avoided. The per unit values are based on the nominal power of the converter. As for the transformer, the per unit values are already calculated in Chapter 3. However, the already calculated per unit values use as base power the nominal of the transformer. This has to be changed to the base power of the converter. The converter has 3 base power values; one for each tap position of the transformer: (a) high tap position 3800V: S_b=1MVA, (b) mid tap position 1900V: S_b=500kVA, (c) low tap position 950V: S_b=250kVA.
5. The dc-link is modeled as a pure capacitor. This capacitor is an energy storage where the stored electrical energy in Joule is $E_c = \frac{1}{2}CV_{dc}^2$. In the power balance of equation 5-47 the power exchange of the power in the capacitor can equivalently be written as the time derivative of the stored energy $P_{cap} = \frac{1}{2}C\frac{dV_{dc}^2}{dt}$. As a result, it can be observed that the power balance equation is

not linear with respect to V_{dc}. For this reason, a new state variable is chosen $W = V_{dc}^2$ and consequently the equation becomes linear with respect to W [30]. Figure 5-32 shows that indeed the outer voltage regulator has been implemented by the use of the dc voltage squared.

6. Several empirical rules have been developed regarding the tuning of the three PI controllers of the control scheme. Some of them are described in [29] and [30]. However these rules are not always reliable and applicable to all cases. Their implementation in a system with numerical representation has usually more chances to be successful. The tuning of the controllers (inner and outer) was done by means of the "traditional" tuning method, which is trial and error. As a result, the values used were:
   - Current regulator: $k_{pi} = 0.24$ and $k_{ii} = 2.6$
   - Voltage regulator: $k_{pv} = 10$ and $k_{iv} = 1000$
7. The controller is implemented in discrete domain, like in the load-side converter. ZOH blocks, anti-aliasing filter as well as digital PI controller blocks are used in Simulink. The transfer function of a PI controller in z-domain is: $PI(z) = K_p + K_i \frac{T_s}{2} \cdot \frac{z+1}{z-1}$.

5.5.3 Simulations & conclusions

Depending on the transformer tap position, three dc-link voltage levels are available:

- At the highest tap position: 6260 V_{dc}
- At the mid tap position: 3700 V_{dc}
- At the lowest tap position: 1900 V_{dc}

These voltage levels correspond to (+) to (-) of the converter and it is assumed that they are equally distributed with respect to the mid-point.

The switching frequency of the PWM converter is set to 1800Hz, and the sampling frequency twice that of the switching frequency. In reality, the rectification is firstly done naturally (through the diodes) and eventually the switching devices take action. This is necessary to prevent exposing the switching devices and the input transformer to inrush current. More specifically, the protection from inrush current is done by means of inrush resistors and a pre-charge circuit. This is also a way to prevent causing voltage dips in the public grid during the transformer energisation. As it can be seen in Figure 5-33, which is a typical example of the start-up at the lowest dc-link voltage level (1900V_{dc}), a pre-charge circuit of lower voltage (lower than the 10.5kV grid line) is used during the charging of the capacitors. The dc voltage is naturally rectified from the transformed ac voltage. Once the capacitors are fully charged and the voltage reaches the desired level (at ~3sec in the graph), the normal 10.5kV circuit is connected. Natural rectification (using the diodes of the 3-level converter) is applied for a few more seconds and the IGBTs switching starts eventually. It is now clear that for the IGBT operation the capacitors are already charged.

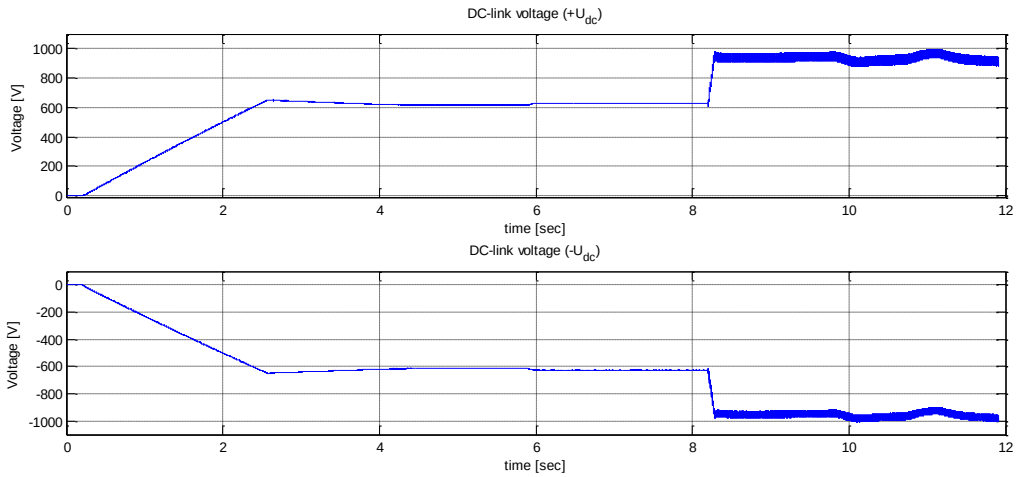


Figure 5-33 FPGL start-up of the AFE in the lowest position (1900Vdc) - Real measurement

For the purposes of this thesis, it is not important to implement the start-up using pre-charge circuit and natural rectification. It is possible though to give an initial voltage to the capacitors and hence consider them fully charged in the beginning of the simulation. Similarly, in reality when the lab is in operation, the first task is to get the desired dc voltage, while keeping the reference of the load-side converter to zero. Once steady-state is reached at the dc-link within a few seconds, it is possible to generate the required voltage at the output of the grid-side converter. Hence for the scope of this report, it is acceptable to assume steady-state and consider pre-charged dc-link capacitors. Nevertheless, it is worthy to see how the Simulink model performs during the start-up, if natural rectification is applied prior the switching operation (Figure 5-34). No pre-charge circuit or inrush resistors are taken into account, hence the fast rectification with respect to the real measurement. The gains selected for the outer controller (dc voltage regulator) in the previous paragraph intend to keep the dc-link voltage stable in steady-state. However, these values are not very realistic, because the high integral gains would cause significant overshoot in the beginning. Adjusting the proportional gains to $k_{pv} = 80$, $k_{pi} = 0.24$ and integral gains to $k_{iv} = 3.5$, $k_{ii} = 0.001$, a more realistic approach of the AFE start-up can be simulated.

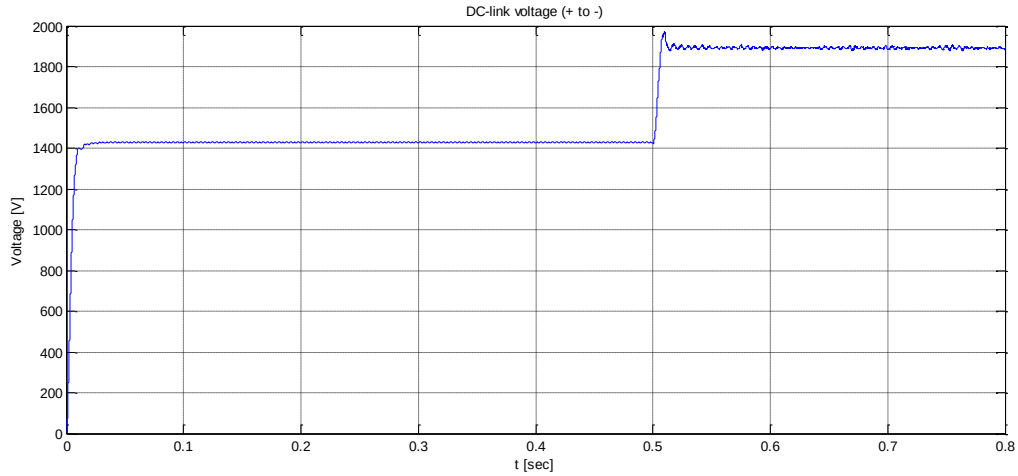


Figure 5-34 Start-up of the AFE in the lowest position (1900Vdc) – Simulation

Figure 5-34 shows that the PWM pattern is applied at 0.5sec. Before that instant only natural rectification takes place.

For the following simulations, it is assumed the capacitors at the dc-link are pre-charged. It is presented the case where the highest tap position of the transformer ($3800V_{ac}$) is selected and hence the full load condition corresponds to 1MVA and the dc link voltage to 6260V. The simulation time of the figures is 6 seconds (300 periods) and the required power at t=0 is 500kVA. At t=3 sec until the end of the simulation the active power is double and corresponds to full load condition. In this way, it is possible to show the performance of the controller in load changes.

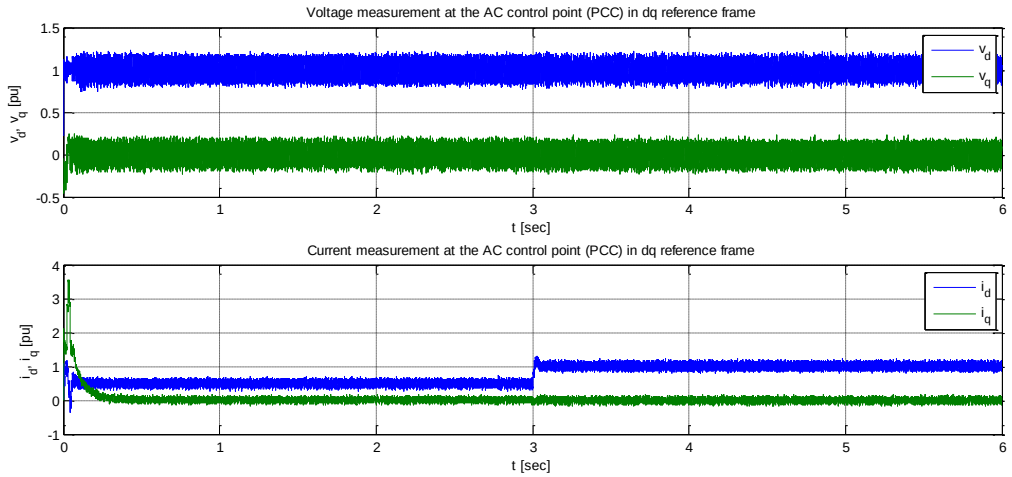


Figure 5-35 Voltage and current measurement in per unit at the AC control point (PCC) in dq reference frame

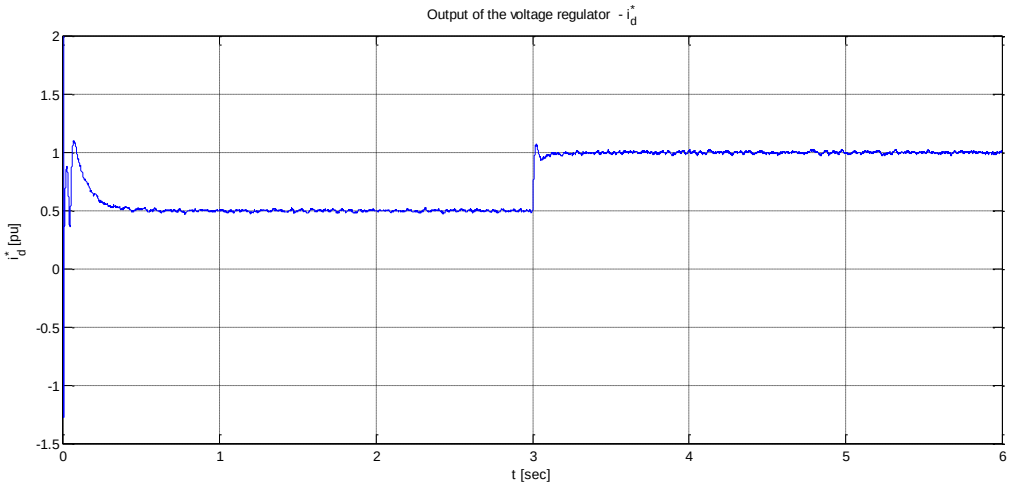


Figure 5-36 Voltage regulator output. Reference of the d-component of current.

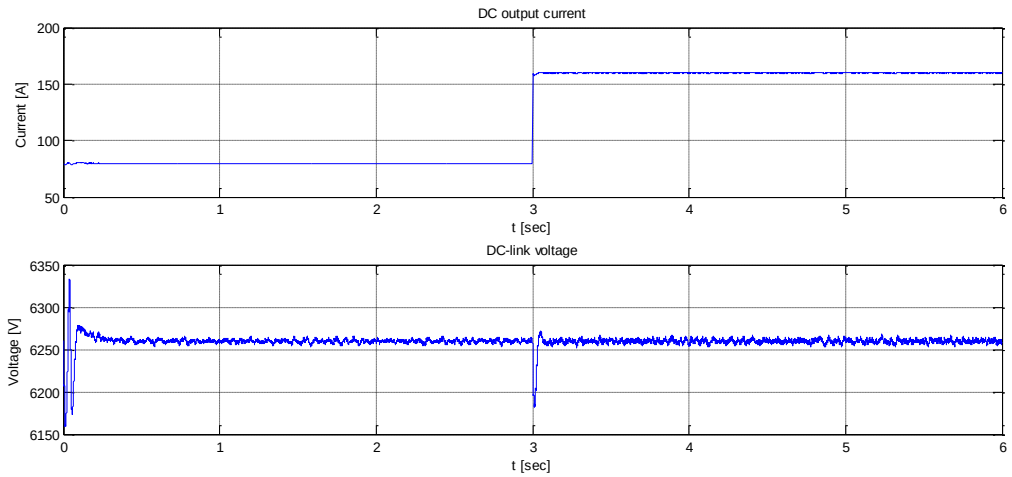


Figure 5-37 DC-link current and voltage

Figure 5-35 confirms that the PLL is locked to phase a voltage phasor and consequently the q-component of the voltage remains zero. Moreover, it is assumed unity power factor and as a result the reference of the q-component of the current is set to zero. Figure 5-35 shows that the measured i_q is zero. In the same figure, the measured d-component of the current is shown to be 0.5pu initially (half load), and at 3sec when the demanded power at the dc-side is 1MVA (full load), the same current increases to 1pu. Figure 5-36 depicts the reference i_d, which changes from 0.5pu to 1pu as well. Finally, Figure 5-37 illustrates the DC-link voltage and DC output current. When the demanded power increases, instantly the voltage decreases. The I-controller brings it back to the reference level 6260V, and the extra power is covered by the increase of the current, which becomes twofold, similar to the change of power.

Last but not least, it is interesting to include also the unfiltered voltage at the ac side of the AFE. For the reader's convenience only 5 periods are plotted.

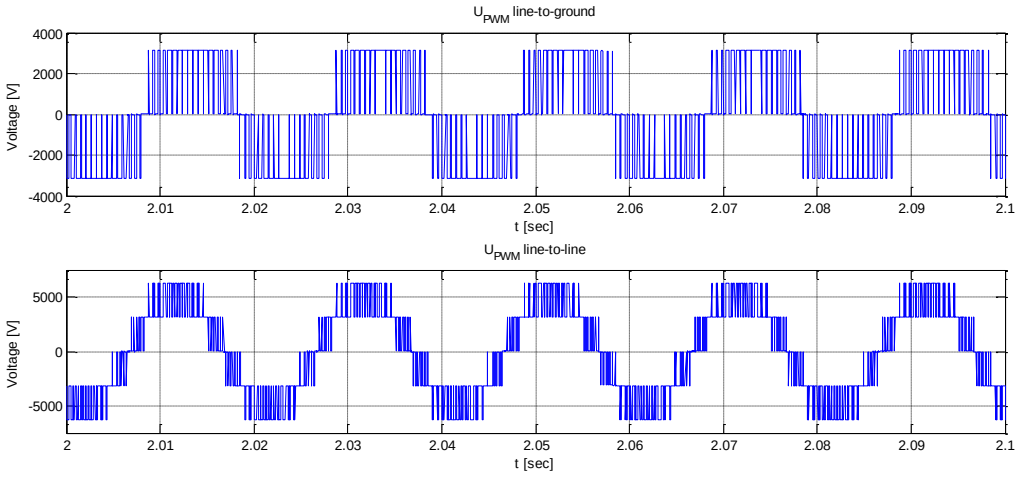


Figure 5-38 PWM voltage at the AC side of the AFE

Chapter 6 : Model Validation

This chapter is dedicated to the presentation and analysis of experimental results. The lab measurements will be used for verification of the accurate performance of the developed model, which will simulate the same scenarios as the tests. All the test configurations consist of the 10.5 kV grid, the TR3/T3 transformer to step-down the available 10.5kV to a lower voltage level, the AFE and the inverter. They have been carried out without the absorption filter connected at the output of the converter, while also the line impedance has been bypassed. Additionally, it is worthy to mention that the lowest tap position - 950V - of the TR3/T3 transformer is selected for all tests. This means that the rating of the converter is 250kVA and the DC-link voltage is approximately 1900V_{dc}.

Prior to each case study a table is attached per test setup, which summarizes the data input per test run. All voltage set-points are given in Vpk line-to-ground. Please bear in mind that the graphs included in this chapter are intended to validate the simulation results. The timings of the lab tests and the simulations are not the same. The time axis shows the duration and can give information only about the graph that corresponds to. No phase shifts can be observed from the following graphs.

6.1 Test 1: Ohmic load at the output of the converter

The test setup is illustrated in Figure 6-1.

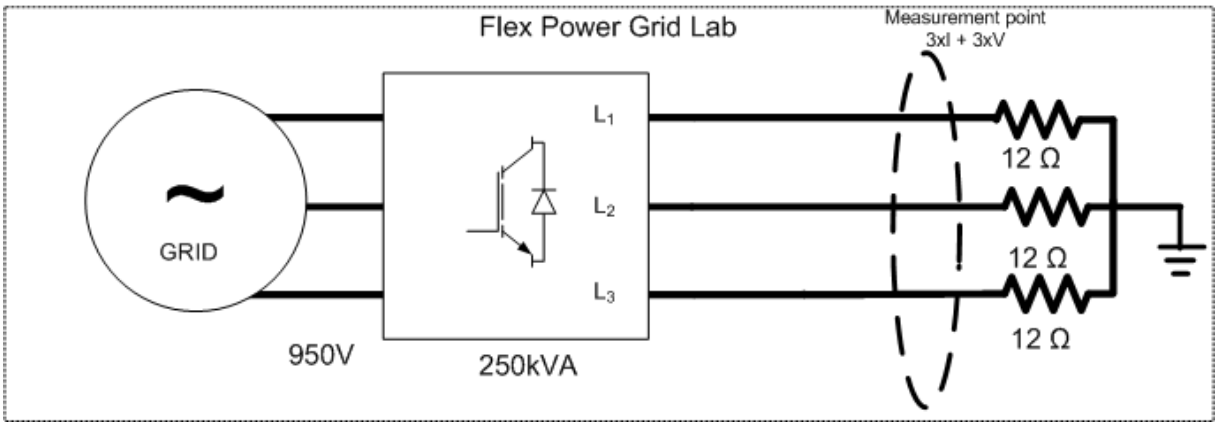


Figure 6-1 Test setup No 1

PWM Frequency [Hz]	Mode	Frequency [Hz]	Voltage set-point [Vpk]
3000	Harmonic	50 (fundamental)	240

Table 6-1 Test 1 - Case study 1: Input data

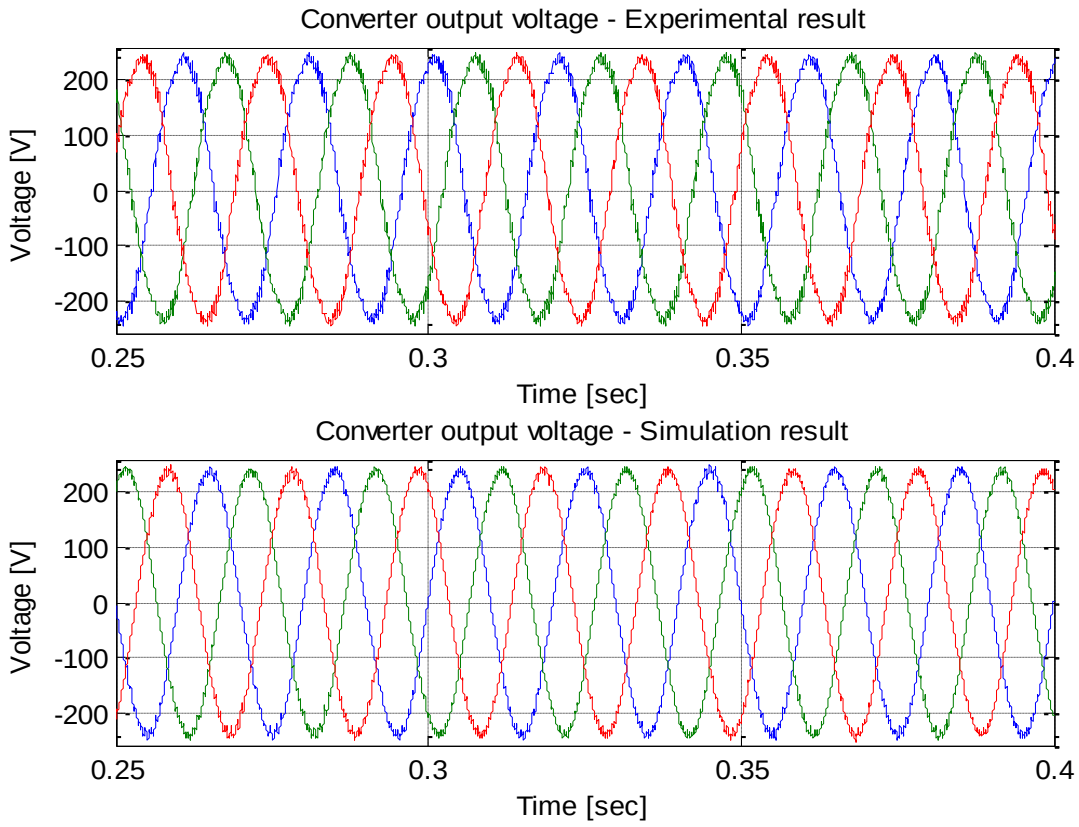


Figure 6-2 Test1 – Case study 1: Converter output voltage: FPGL and Simulation result

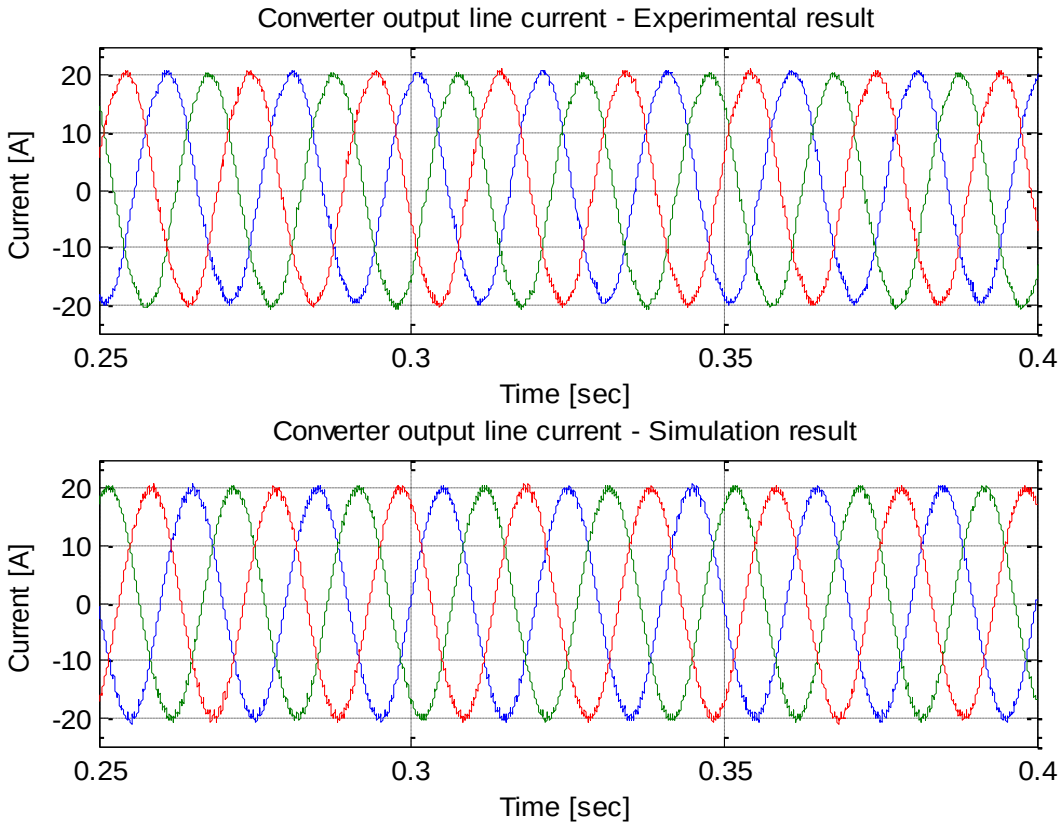


Figure 6-3 Test 1 – Case study 1: Converter output current: FPGL and Simulation result

Both the waveforms of voltage and current give a first view of the accuracy of the model. The rms values of the measurements and simulations quantify the information provided by the graphs. Due to the fact that there is no unbalance in this case, the differences between the three phases are negligible and Table 6-2 includes the average line-to-ground rms voltages and average rms line currents.

	Frequency [Hz]	Set-point	FPGL	Simulation	Error [%]
Voltage [Vrms]	50	169.7	169.86	169.6	-0.15
Current [Arms]			14.3	14.14	-1.1

Table 6-2 Test 1 - Case study 1: comparison table of results

It is worth also observing the voltage waveforms of the 3rd harmonic on the top of the fundamental component. Simulations and lab tests have been carried out for three different phase angles of the 3rd harmonic with respect to the fundamental: 0, 90 and 180 degrees.

PWM Frequency [Hz]	Mode	Frequency [Hz]	Voltage set-point [Vpk]
3000	Harmonic	50 (fundamental)	500
		150 (3rd)	150 <0 ; 150 <90 ; 150 <180

Table 6-3 Test 1 - Case study 2: Input data

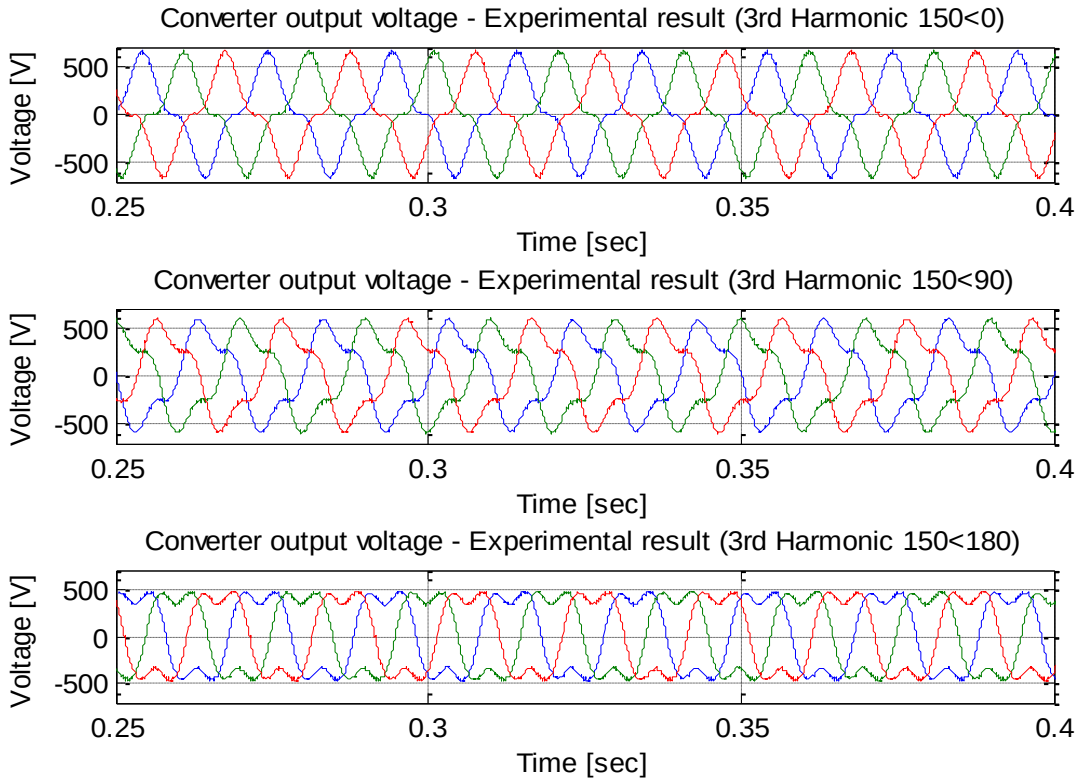


Figure 6-4 Test 1 - Case study 2: Converter output voltage: FPGL result

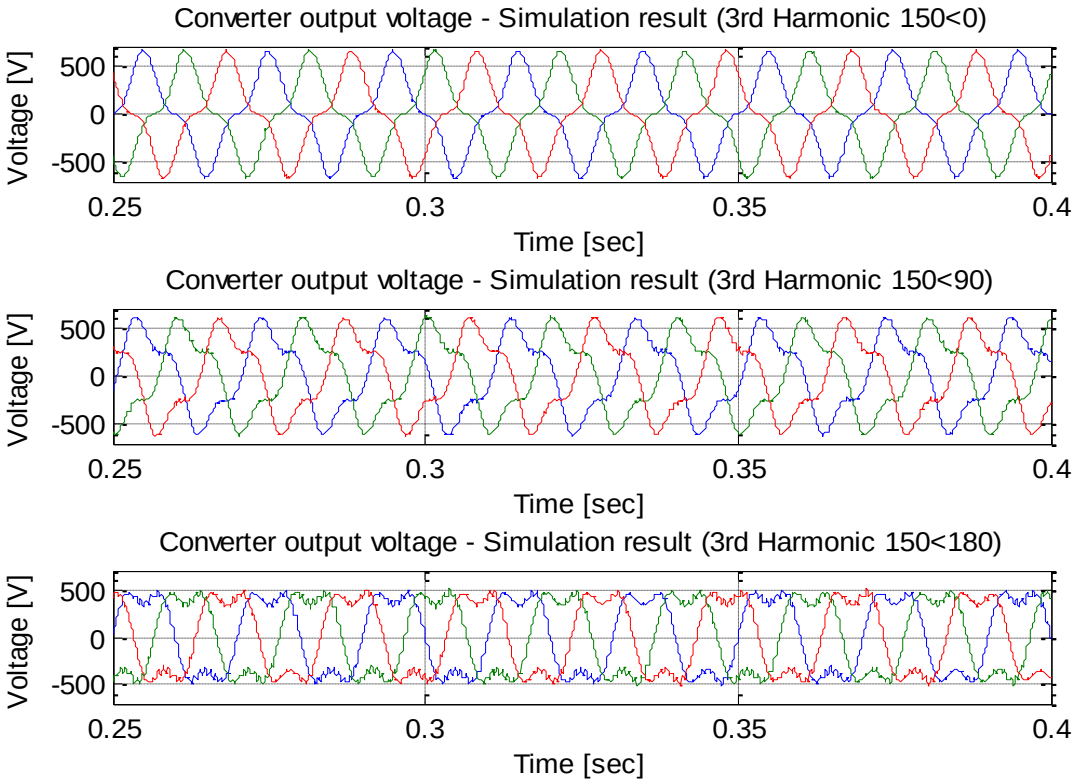


Figure 6-5 Test 1 - Case study 2: Converter output voltage: Simulation result

The graphs confirm the very accurate performance of the model, while from the FFT analysis of both simulation and lab test it is possible to receive the content from each frequency separately.

	Frequency [Hz]	Set-point	FPGL	Simulation	Error [%]
Voltage [Vrms]	50	353.55	351.79	353.5	0.49
Voltage [Vrms]	150	106.06	108.39	106	-2.2

Table 6-4 Test 1 - Case study 2: comparison table of results

6.2 Test 2: Voltage unbalance–Interruption of phase b

In this test, it is intended to create voltage unbalance. More specifically the fundamental command input is 500Vpk line to ground for all three phases. The command input for the second phase is set to 0 and eventually it recovers. The aim of this test is to focus on the dynamic response of the system and observe if the model reacts similarly to the FPGL. The compensator uses the I-controller in this case, hence dynamic mode.

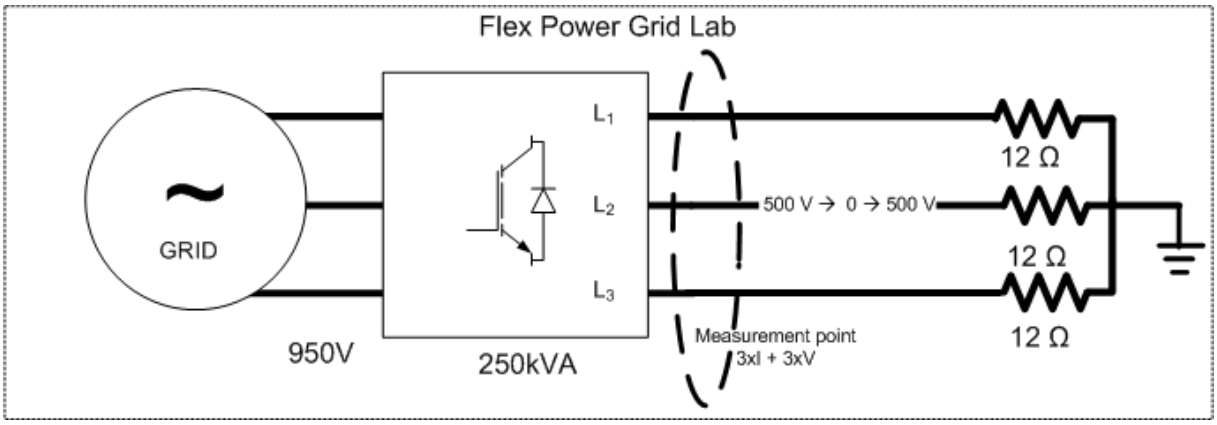


Figure 6-6 Test setup No2

PWM Frequency [Hz]	Mode	Frequency [Hz]	Voltage set-point [Vpk]
3000	Dynamic	50 (fundamental)	500

Table 6-5 Test 2: Input data

Paragraph 6.1 - Test 1 ensures quantitative accurate performance of the model in the current test because of its similar setup. The figures below show the voltage waveforms generated in the FPGL versus the ones generated virtually in the model. It is important to focus on the time instants when the voltage of phase b becomes 0 and when it recovers.

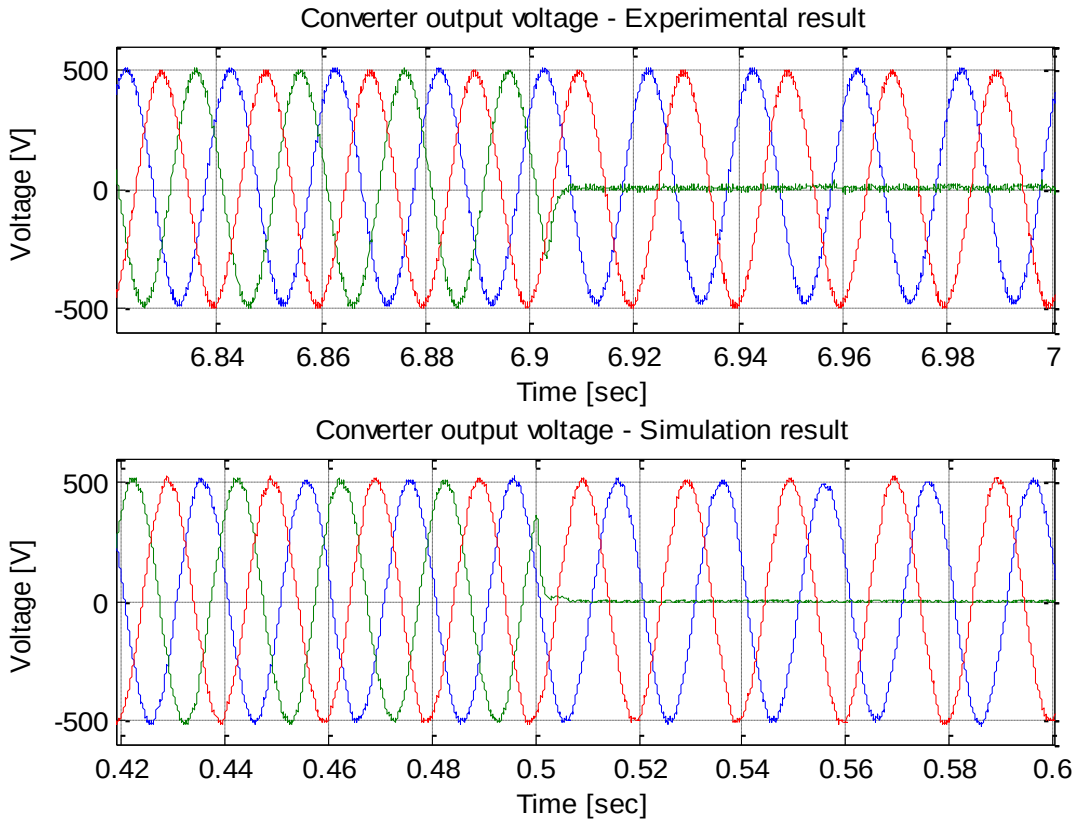


Figure 6-7 Test 2: Converter output voltage at the instant when command input for phase b becomes zero: FPGL and Simulation result

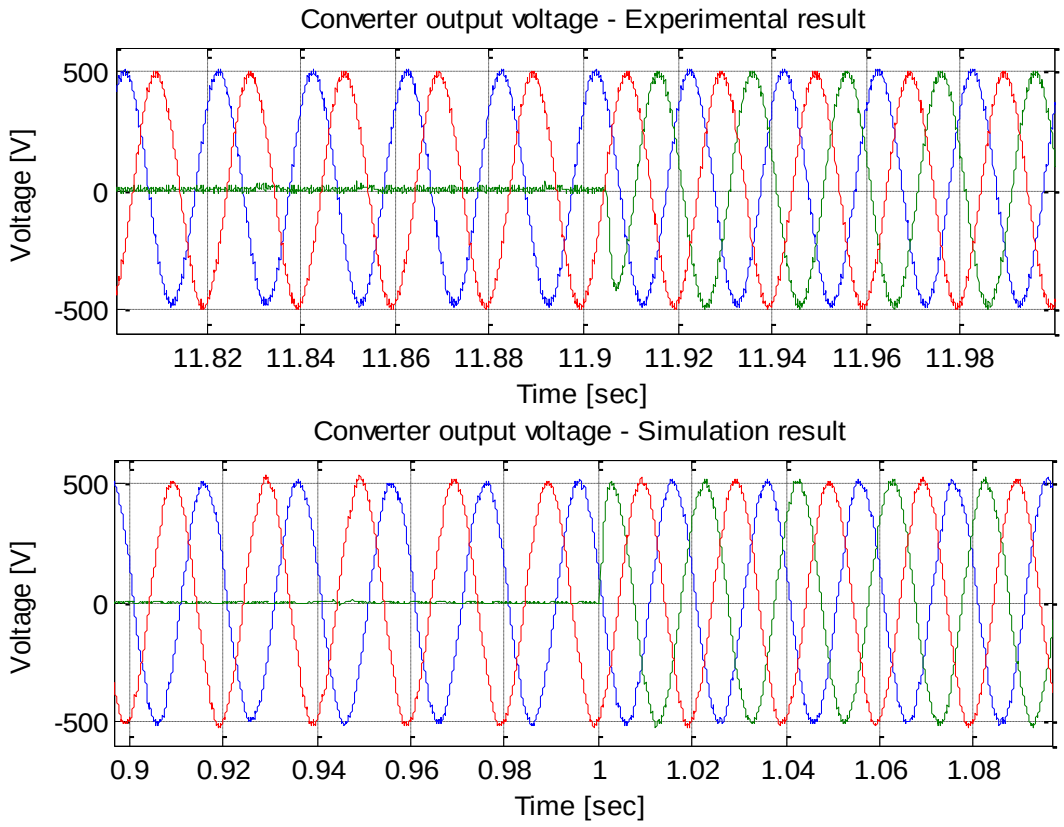


Figure 6-8 Test 2: Converter output voltage at the instant when voltage balance recovers: FPGL and Simulation result

The equivalent proposed Simulink model has similar performance to the FPGL in this test too. However, it is worthy to note that the main difference that one can observe in the figures above is the voltage ripple of the phase which turns to zero. Figure 6-9 depicts the magnification of the previous graphs, focusing only on the ripple when phase b is 0. The ripple, which is generated in the FPGL is at least two times the one generated by the model. This was expected, because the real measurement may have some noise, which affects the result. Experimental measurements are never perfect, even with sophisticated modern instruments. It is not always easy to distinguish the noise from the signal; however this could be an idea for future work.

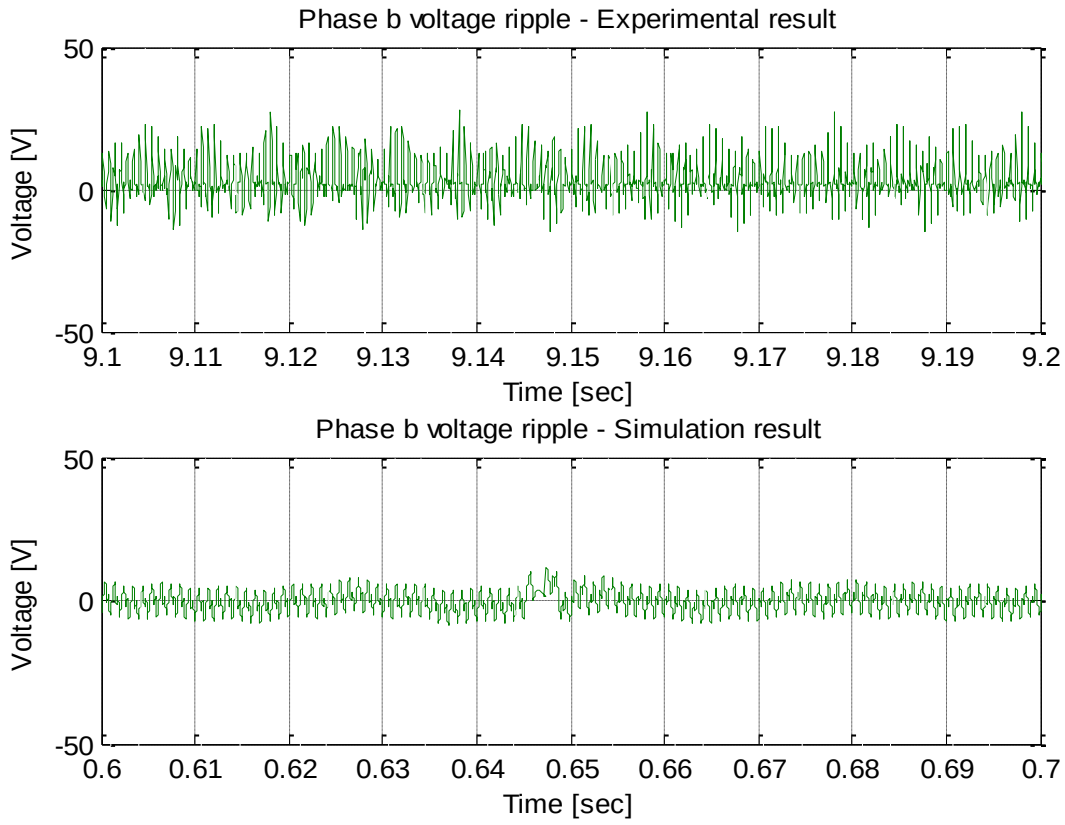


Figure 6-9 Test 2: Phase b output voltage ripple: FPGL and Simulation result

6.3 Test 3: Three-phase jump

This case study focuses on the dynamic grid voltage phenomenon of phase jump. A three-phase instantaneous jump of 180 degrees is commanded as input. The test set-up remains the same as in Figure 6-1, while the input data are presented in the following table.

PWM Frequency [Hz]	Mode	Frequency [Hz]	Voltage set-point [Vpk]
3000	Dynamic	50 (fundamental)	500

Table 6-6 Test 3: Input data

First, it is of high importance to see the system response in both FPGL and Simulink model as well as compare them to each other. Concerning the quantitative accuracy of the model, the results as presented in paragraph 6.1 are representative. The figures below confirm the validity of the model regarding the tracking reference. Figure 6-10 shows very similar voltage waveforms for the FPGL and simulation outcomes.

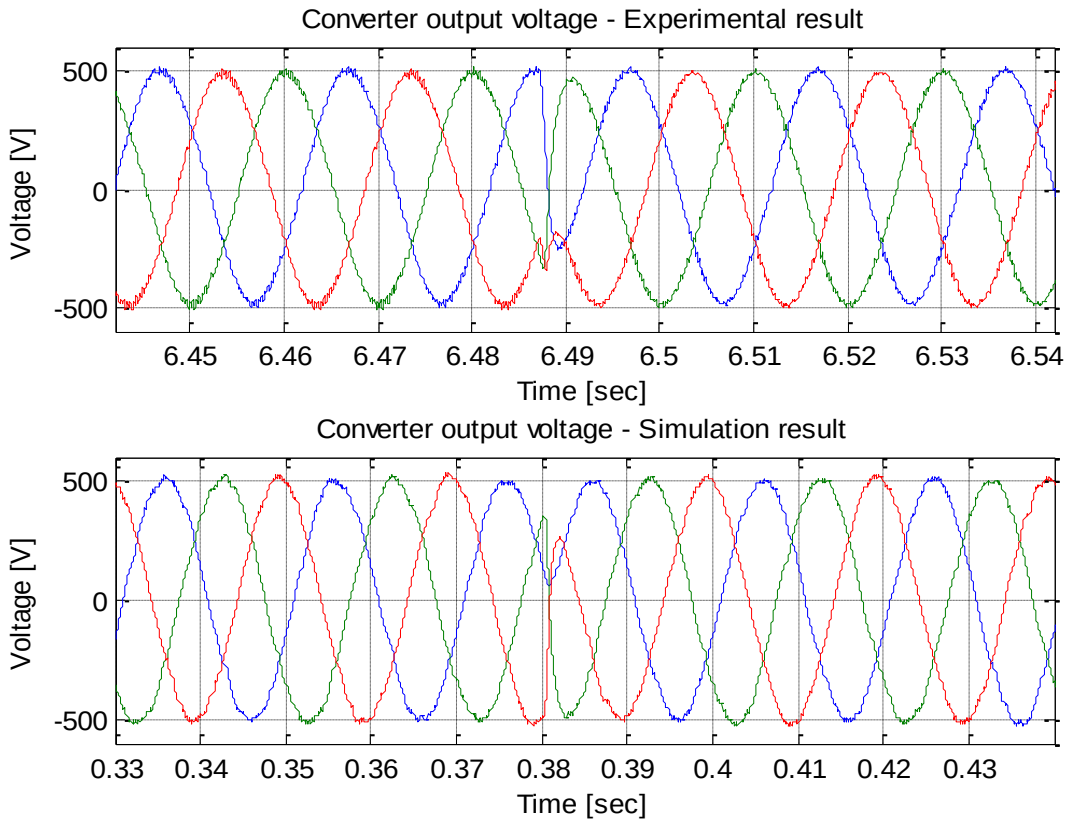


Figure 6-10 Test 3: Converter output voltage at the instant when 180 degrees phase jump occurs: FPGL and Simulation result

Because of the nature of this test, it is extremely interesting to observe and compare the filter and output currents of the load-side converter. Figure 6-11 illustrates the output filter current, which as expected is highly distorted because of the PWM and presents current spikes at the instant that the phase jump occurs. The spikes of the simulation result are a few Amperes sharper than the ones of the reality. Of course these spikes are absorbed by the filter capacitors and the output currents are depicted in Figure 6-12, where there are no spikes at all. Both simulation and real currents are getting reversed relatively fast. However, the FPGL system seems to react a few milliseconds slower than the model predicts. This happens because in reality the phase jump was commanded to be completed in 0.1sec, whereas the phase jump in the model occurs instantly. This might be also the reason why the predicted spikes are higher than the measured spikes.

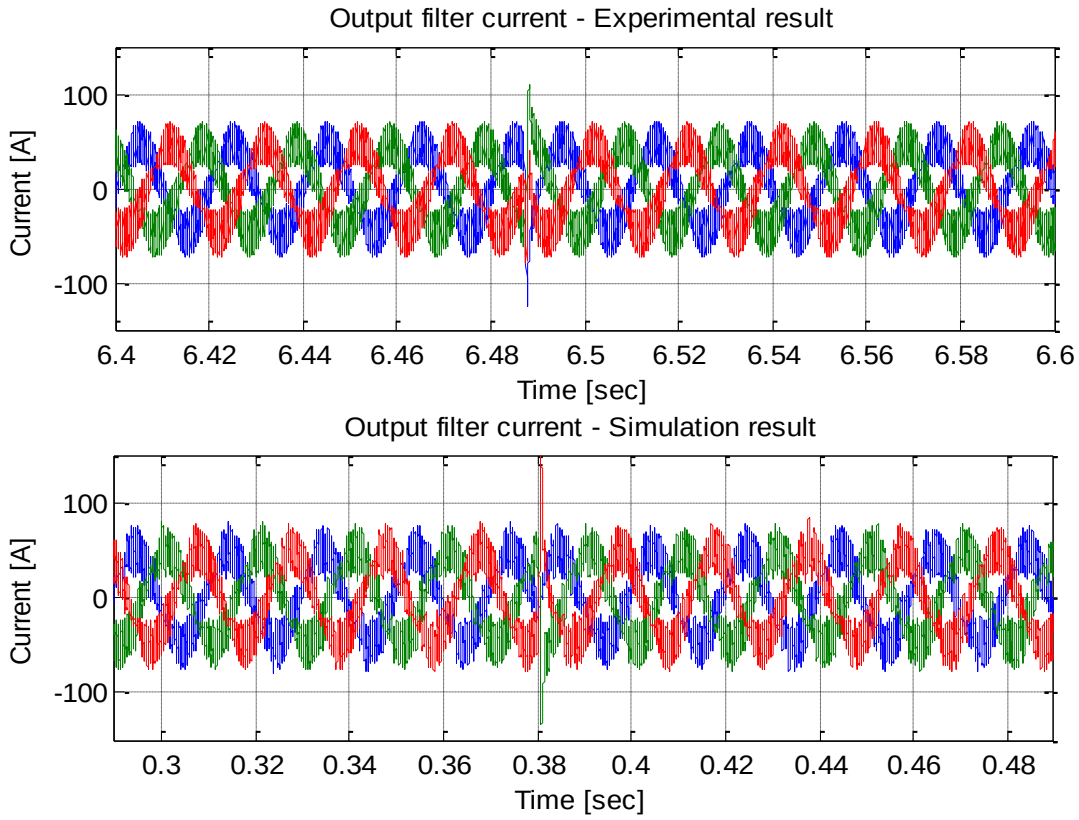


Figure 6-11 Test 3: Output filter current: FPGL and Simulation result

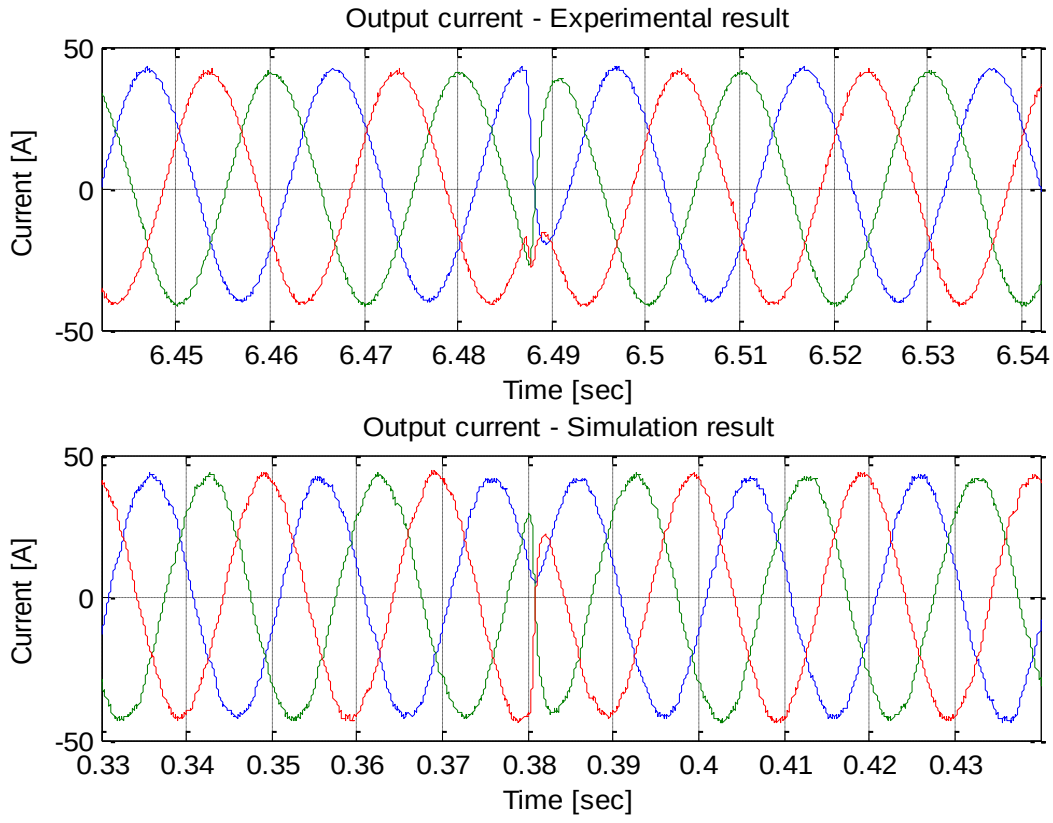


Figure 6-12 Test 3: Output current: FPGL and Simulation result

Although some minor differences exist, the simulation results give a great overview of the lab performance before the actual test takes place. Hence, in such tests when current spikes are expected - in order to avoid getting higher currents than 175Arms, which is one of the converter limitations - the Simulink model is capable of predicting them accurately.

Finally, it is worth including also the DC-link voltage graphs, which show that nothing occurs at the dc-link during the phase jumps, and thus it remains steady to the desired level (1900V_{dc}). Figure 6-13 illustrates the DC-link voltage as measured in the FPGL and in Simulink environment. As mentioned in paragraph 5.5, the tuning of the PI controllers in Simulink was done using a trial and error method. The real values of these controllers were not available during this study and hence some differences were expected. This is the reason why the FPGL DC-link voltage is more rippled with respect to the Simulink DC-link voltage. Of course, measurement noise also plays a significant role in this measurement and explains the difference between the measured and simulated DC voltage.

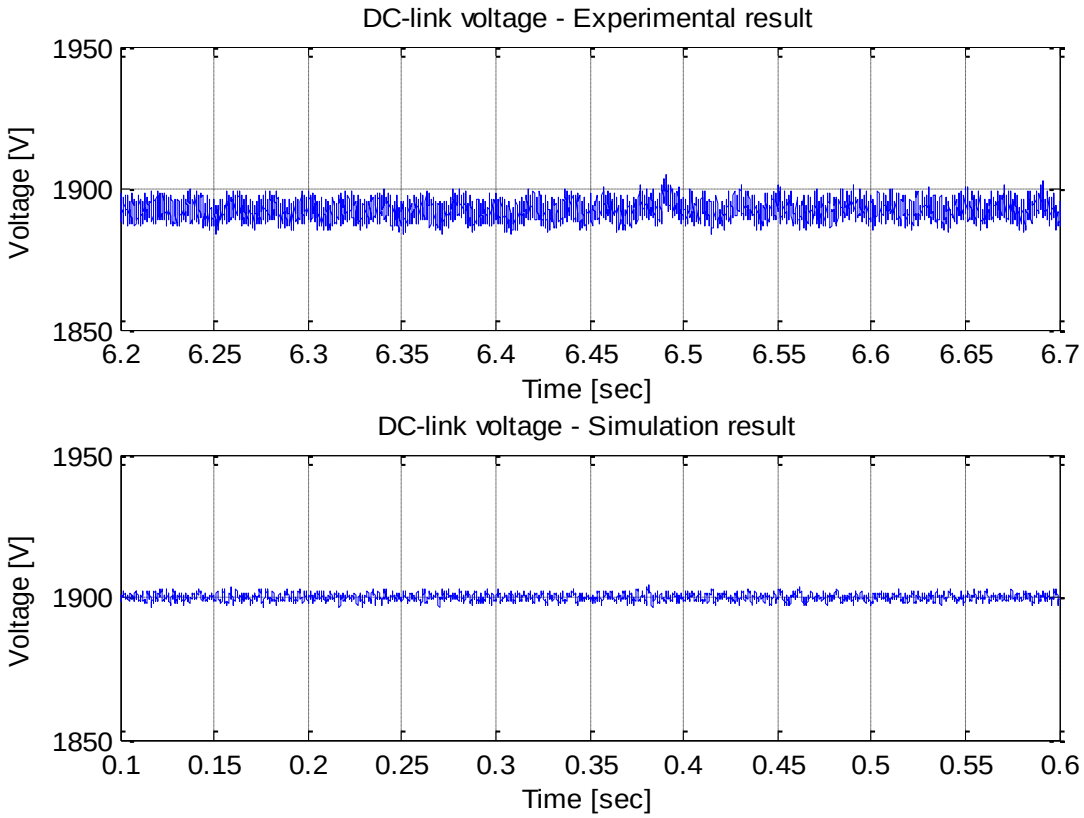


Figure 6-13 Test 3: DC-link voltage: FPGL and Simulation result

6.4 Test 4: Voltage harmonic distortion

The next configuration intends to verify the performance of the converter model in harmonic mode as well as validate the TR3/T4 transformer model at higher frequencies.

In Chapter 3, short- and open-circuit simulations for the transformers verify the simulation results with the witness test measurements. This particular test integrates also the three-phase, three-

winding TR3/T4 transformer, which shows the transformer model performance at higher frequencies. Because of high frequencies the cable impedances cannot be neglected. The converter is connected to the 3.3kV tapping of the transformer with one 95mm^2, 13.8kV cable per phase. It is 5.93m long, its dc resistance is 1.245 mΩ and its linear inductance is 3.65uH/m. Moreover, the low voltage side of the transformer is short-circuited with one 13,8kV cable per phase. Its cross-section is 120mm^2 and its length 2.56m. The dc resistance is 0.42mΩ and the linear inductance 0.928uH/m.

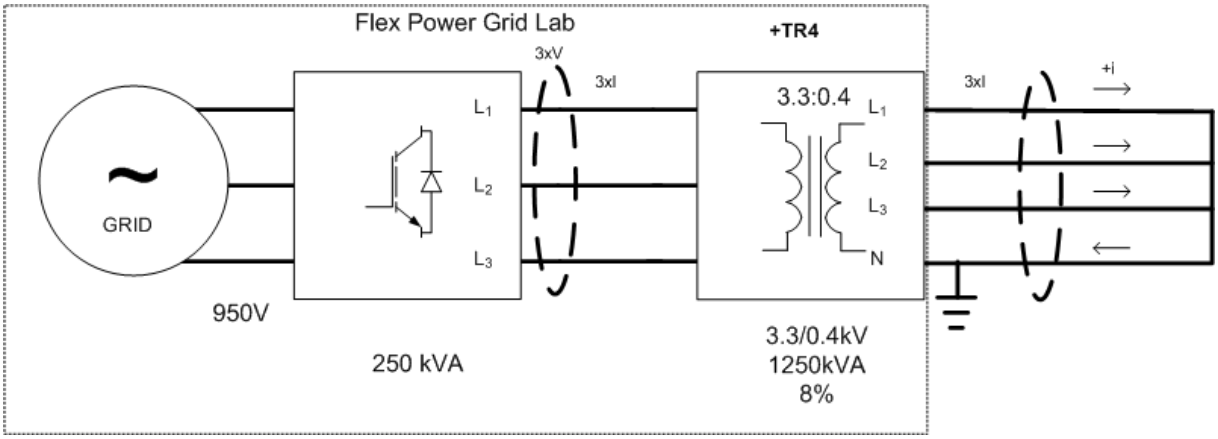


Figure 6-14 Test setup No 4

Two different case studies are being examined with the configuration of Figure 6-14. The first case study includes 4 simulations at 4 different frequencies. Considering that the FPGL is capable of producing fundamental frequencies up to 75Hz, the frequencies of 150Hz, 250Hz, 350Hz and 450Hz are generated as harmonics of 50Hz fundamental frequency. However, the command input of the fundamental voltage is set to 0. The input data of each test run is shown in the Table 6-7.

PWM Frequency [Hz]	Mode	Frequency [Hz]	Voltage set-point [Vpk]
3000	Harmonic	150	105
3000	Harmonic	250	160
3000	Harmonic	350	225
3000	Harmonic	450	300

Table 6-7 Test 4 – Case study 1: Input data

Figure 6-15 to Figure 6-18 show the generated voltage and the current at the short-circuited side of the transformer. Please bear in mind that 150Hz and 450Hz are odd multiples of the 3rd harmonic (3rd, 9th). Triplen harmonics are of particular concern, because they are zero sequence harmonics, unlike the fundamental, which is positive sequence. This can be seen in the corresponding graphs below, which show that although all three phases are plotted, they are not shifted by ±120 degrees. Special attention should be paid to the configuration of the test when triplen harmonics are intended to be generated. More specifically, the transformer winding connections have a significant impact on the flow of triplen harmonic currents. The triplen harmonic currents enter the wye side and since they are in phase, they add up in the neutral. In balanced conditions, the neutral of the star connected windings shall not be left disconnected, whereas the triangular connection of the high voltage winding 24kV (Dyn-yn transformer) needs to be disconnected to avoid circulating the current in the delta configuration.

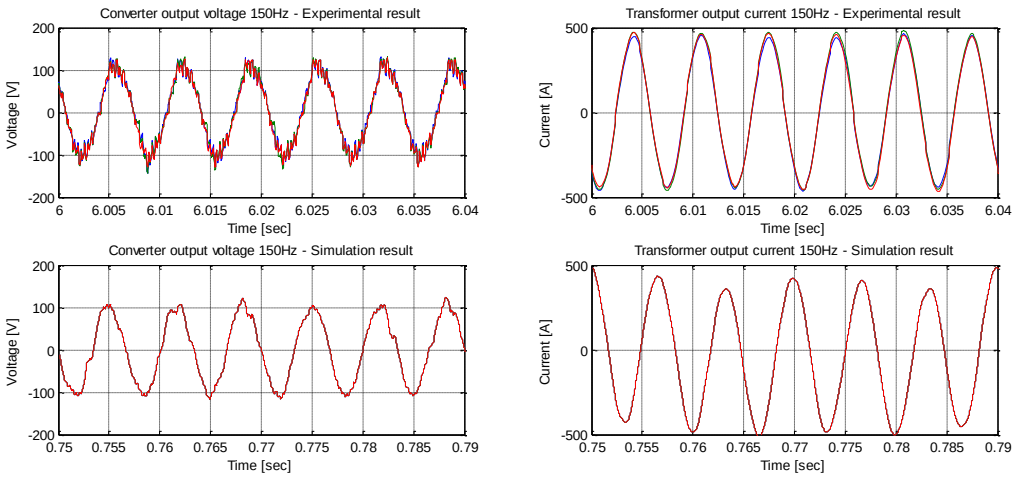


Figure 6-15 Test 4 – Case study 1: Converter output voltage and transformer output current 150Hz: FPGL and Simulation result

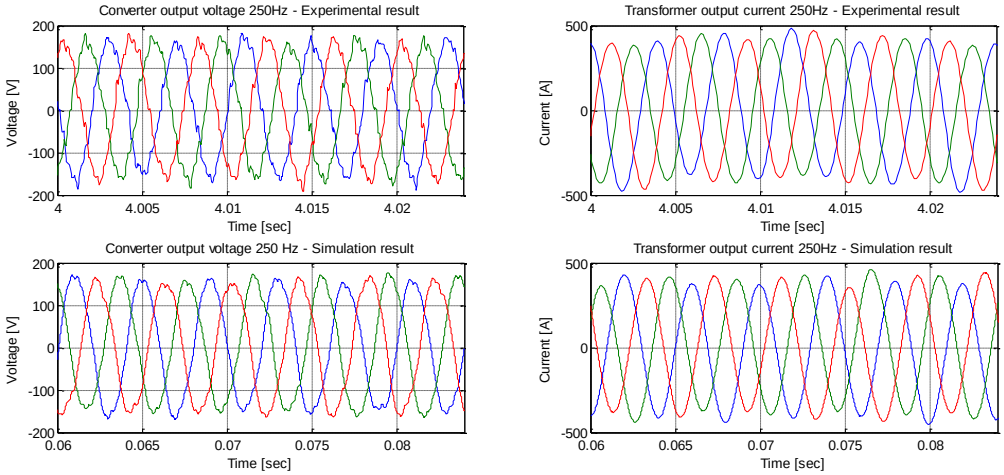


Figure 6-16 Test 4 – Case study 1: Converter output voltage and transformer output current 250Hz: FPGL and Simulation result

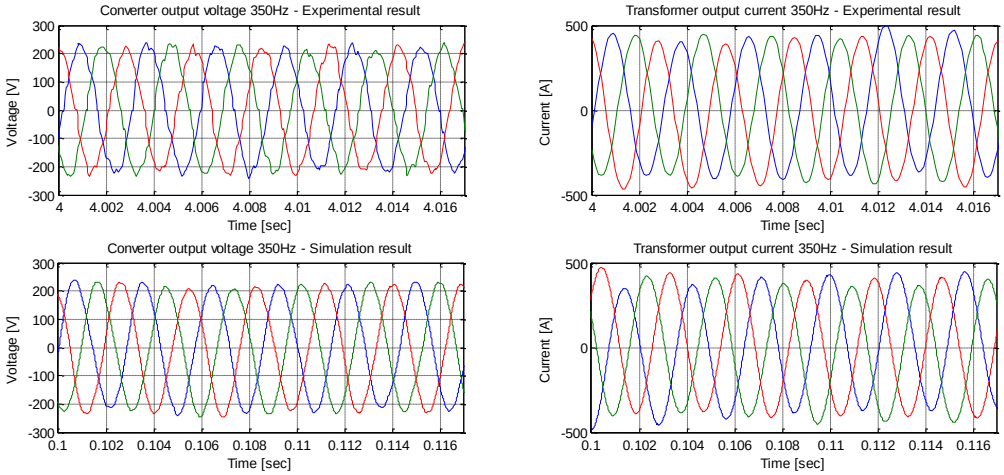


Figure 6-17 Test 4 – Case study 1: Converter output voltage and transformer output current 350Hz: FPGL and Simulation result

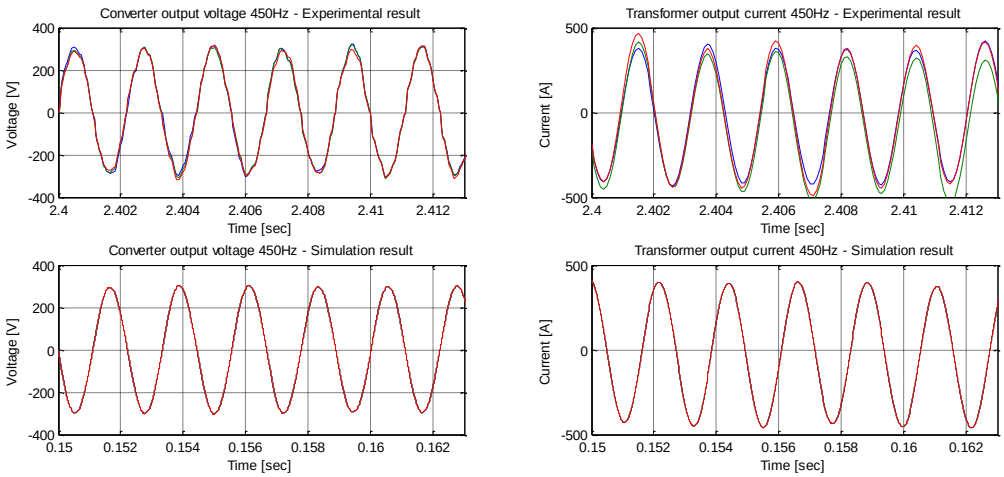


Figure 6-18 Test 4 – Case study 1: Converter output voltage and transformer output current 450Hz: FPGL and Simulation result

The figures above show very similar waveforms between the model simulation and FPGL measurement results. However, the FPGL voltage waveform seems more distorted compared to the simulation plot which is more idealistic. This happens especially in lower voltage set-points, because in lower scales, the noise of real measurement is more obvious. Table 6-8 provides a quantitative overview of the presented results comparing the rms values of converter output voltage and the transformer output current.

	Frequency [Hz]	Set-point	FPGL	Simulation	Error [%]
Voltage [Vrms]	150	74.25	76.16	75.62	-0.71
Current [Arms]	150		313.06	312.54	-0.16
Voltage [Vrms]	250	113.14	113.92	112.7	-1.07
Current [Arms]	250		299.46	285.47	-4.67
Voltage [Vrms]	350	159.10	157.83	158.27	0.28
Current [Arms]	350		296.84	286.34	-3.54
Voltage [Vrms]	450	212.13	211.14	212.10	0.45
Current [Arms]	450		299.08	296.42	-0.89

Table 6-8 Test 4 – Case study 1: Comparison table of results

It can be seen that the results are very encouraging as there no significant differences. The results verify the converter model with regard to the generated voltage and make the transformer model valid for higher frequencies as well. This is a transformer short-circuit test and the outcomes are convincing regarding the correct calculation of the windings' impedances, which are frequency dependent.

The purpose of the second case study is to create a ''dirty'' grid by generating harmonic voltage distortion on the top of the fundamental 50Hz frequency. The harmonics will be 180 degrees shifted with respect to the fundamental. The following spectrum will be created:

PWM Frequency [Hz]	Mode	Frequency [Hz]	Voltage set-point [Vpk]
3600	Harmonic	50 (fundamental)	45
		250 (5^{th})	23<180
		350 (7^{th})	215<180
		550 (11^{th})	485<180
		650 (13^{th})	185<180
		850 (17^{th})	100<180

Table 6-9 Test 4 – Case study 2: Input data

Due to the high harmonic content, it is more convenient to plot only one phase in every graph, and it is assumed that the results and conclusions stated for these graphs are valid for the other two phases as well. This is a safe assumption, because all the phases have been modeled similarly and independently, while the system in this particular case is balanced. The output voltage of the converter is presented first along with its single-sided amplitude spectrum, which will allow us to receive a quantitative view of the result.

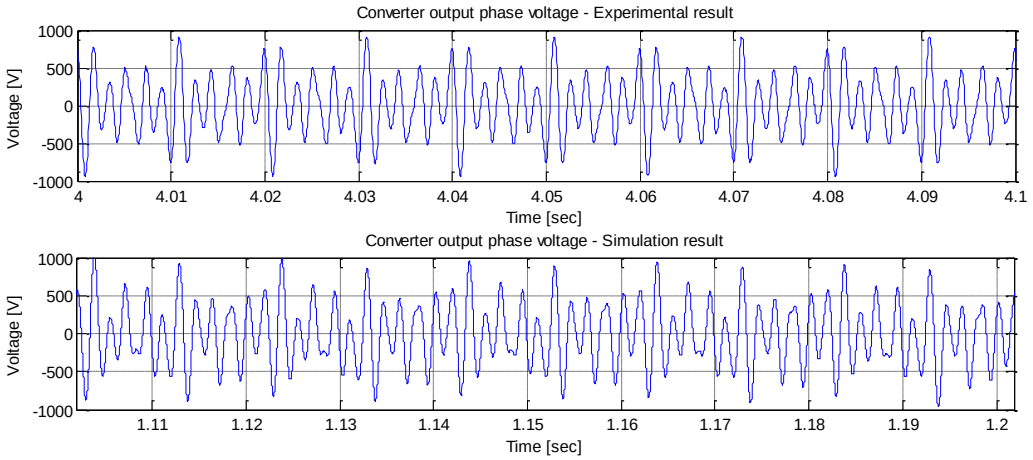


Figure 6-19 Test 4 – Case study 2: Converter output phase voltage: FPGL and Simulation result

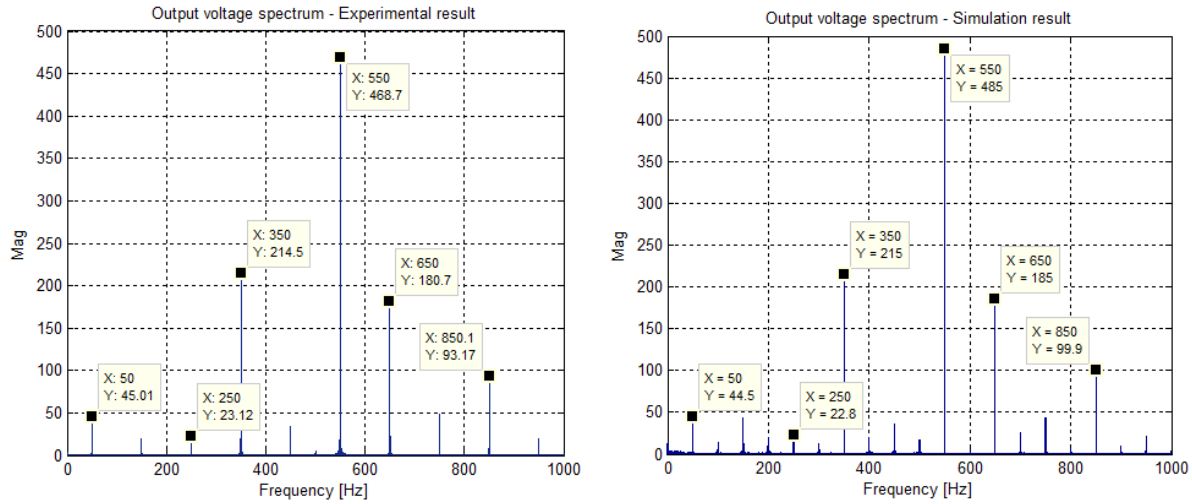


Figure 6-20 Test 4 – Case study 2: FFT amplitude spectrum of the converter output voltage: FPGL and Simulation result

The developed Simulink model has similar performance to the FPGL, regarding the generated voltage waveform. The cursors on the spectrum plots (see Figure 6-20) facilitate the numerical comparison of the generated voltage. Harmonic content of frequencies higher than 1000Hz is considered negligible. Keeping in mind the commanded set-points, the model has high accuracy in respect with the reference. The following table gives a better overview of the results.

	Frequency [Hz]	Set-point	FPGL	Simulation	Error [%]
Voltage [Vpk]	50	45	45.01	44.5	-1.13
Voltage [Vpk]	250	23	23.12	22.8	-1.38
Voltage [Vpk]	350	215	214.5	215	0.23
Voltage [Vpk]	550	485	468.7	485	3.47
Voltage [Vpk]	650	185	180.7	185	2.38
Voltage [Vpk]	850	100	93.17	99.9	7.22
THD [%]		1269.21	1229.53	1307.98	6.38

Table 6-10 Test 4 – Case study 2: Comparison table of results

The table confirms limited error between the FPGL measurement and the model. Apart from the 17th harmonic, the error of which is increased with respect to the others, the differences between the FPGL and the model are very low. The 17th harmonic of the FPGL, as well as the entire real spectrum - in contrast to the FFT analysis of the simulated model - may have some error due to the finite resolution of the recorded sample. The THD of the simulation is 3% higher than the expected according to the set-points, which can be considered as a very accurate result.

Next, it is interesting to present the current at the short-circuited side of the transformer.

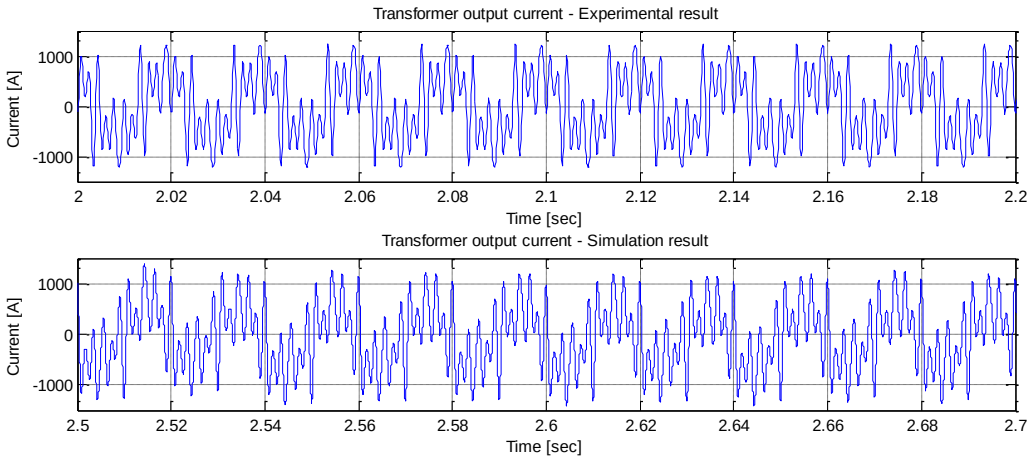


Figure 6-21 Test 4 – Case study 2: Transformer output current: FPGL and Simulation result

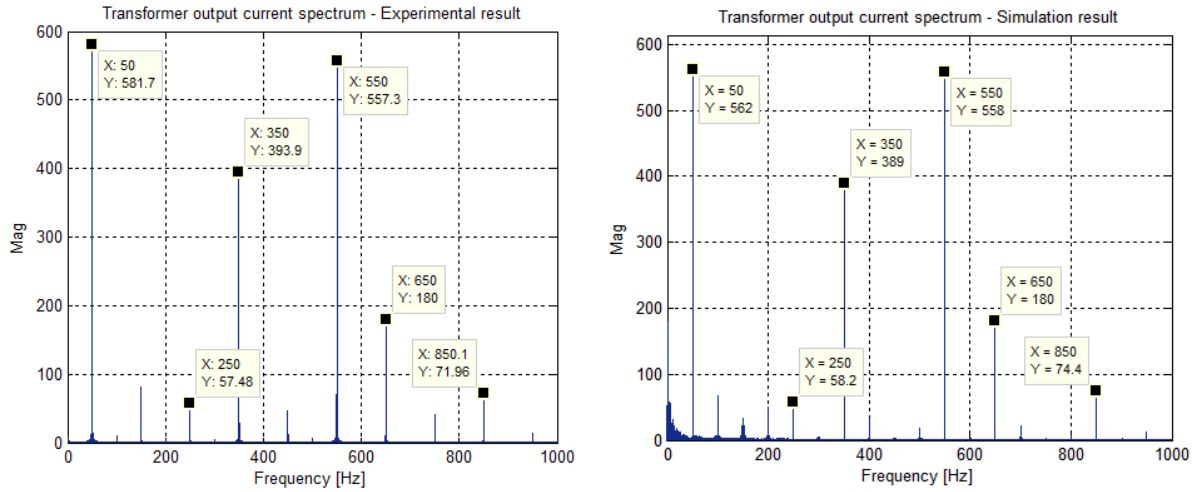


Figure 6-22 Test 4 – Case study 2: FFT amplitude spectrum of the transformer output current: FPGL and Simulation result

The two current waveforms are very similar as well as the differences per harmonic component are not significant. The fundamental current in the simulation is 3.4% lower than the corresponding current in the lab, while all the harmonic currents have even lower differences. Nevertheless, it would be useful to look into the current spectrum before the transformer.

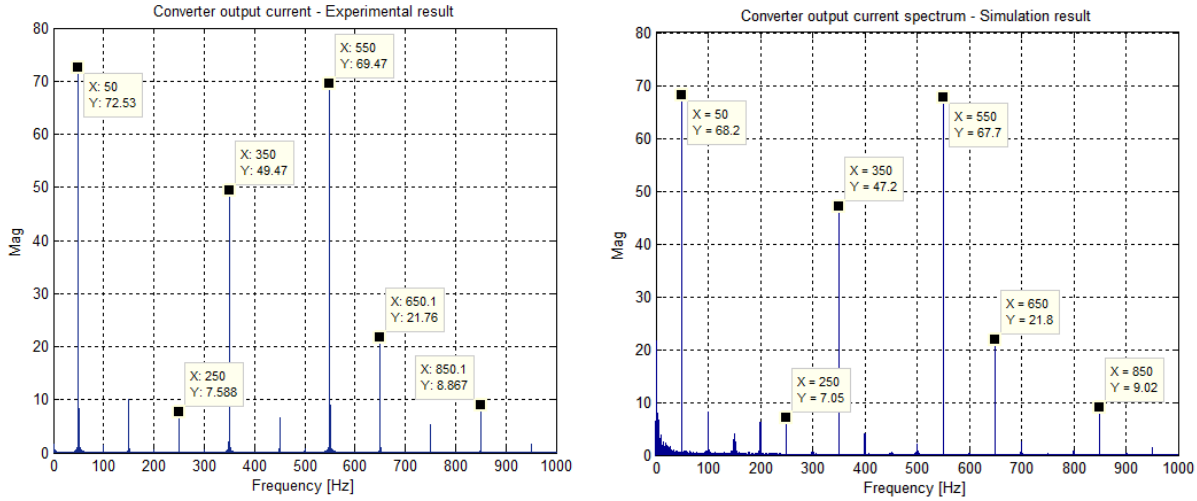


Figure 6-23 Test 4 – Case study 2: FFT amplitude spectrum of the converter output current: FPGL and Simulation result

Figure 6-23 illustrates that even before the transformer these minor differences in the current spectrum exist. The current THD of the FPGL is 124.37%, while the simulated THD is 128.61%. Similarly to Figure 6-22, the fundamental current shows the most significant difference.

All the plots confirm the satisfying accuracy of both the converter and the transformer models. The minor differences at the output voltage of the converter come from the different sampling times of the PWM generators. The Simulink PWM generator uses lower sampling time and hence the more accurate output voltage with respect to the command input and the less un-commanded distortion. In addition to this, the high frequency content, which is more obvious in the real measurements and lower scales and appears on the top of the commanded voltage output, may be noise during the measurement. In Simulink such measurements are not accompanied by noise, in contrast to the FPGL, in which unfiltered measurements would certainly include some noise. Furthermore, it is worth mentioning that the cable impedance values are not provided by their manufacturer, but by our own

measurements. Hence, these low differences that the currents show, it is likely to emanate from the not 100% accurate cable impedance calculation. Last, it is possible that the currents at the output of the transformer may have these low differences, because of the not entirely accurate prediction of the windings temperature. As aforementioned the transformers' models incorporate the temperature of the windings, which can roughly be predicted depending on the test. For the tests presented in this chapter, it is assumed that the temperature does not exceed the 30^{o}C because of the very short duration of each test.

Chapter 7 : Conclusions

7.1 Thesis Outcomes

This Master Project successfully fulfills all the goals that were set initially. The complete FPGL has been modeled in MATLAB/Simulink environment, while the model can be considered as a reliable representation of the lab, at least concerning the aspects that have also been validated.

Although some minor assumptions have been made, for simplicity reasons or due to lack of information, the model integrates all the functionalities of the existing FPGL. The validation test results are certainly very promising and along with more tests that can be carried out in the future - such as measurement of the harmonic injection into the grid or testing the converter in operating conditions close to its limits – the model can be considered as completely verified and may be used with full success. Moreover, regarding the transformers' models, the saturation is not taken into account, while all the data imported in the model were extracted by measurements. Pre-defined adjustable winding temperature is also a feature supported by the model, hence the accuracy increases when long tests are required and temperature is a factor that cannot be neglected. In Chapter 3 and Chapter 6 the calculations and the performance of the model at nominal and higher frequencies are verified by tests.

Undoubtedly, the converters were the most challenging parts to be modeled, especially because of their control. As for the load-side converter, [33] describes in detail the control architecture that is implemented in the FPGL converter. Because of this great advantage, it was possible to avoid many assumptions and the model controller is tuned according to the paper's information. Consequently, the results presented in the validation chapter are very accurate. The discrete implementation of this controller was necessary in order to take the DSP into account. Special attention was paid to different time domains; the converter hardware operates in continuous time domain, and two different frequencies were chosen for the sampling and switching. As explained in Chapter 5, due to hardware limitations, double update of the duty cycle is not supported in the FPGL, and although the sampling frequency is twice the switching frequency, the update occurs once in every PWM period for the averaged value of two samples in that period. However, the PWM generator model supports the double update feature. This assumption was made for simplicity reasons, and as it can be seen in Chapter 6, the error is not significant at all. Of course the double update operation of the PWM generator makes the model more idealistic with respect to the real world, hence the voltages are less distorted. Certainly, some high frequency content that appears in the FPGL measurements, but not in the model results, may emanate from the unfiltered noise during the real measurements. The load-side converter modeling procedure is possibly the most valuable from the scientific point of view, as it describes an innovative control strategy in the stationary reference frame using resonant controllers. It is clear that this control scheme is the most efficient, when not only the fundamental voltage, but several harmonics as well, need to be controlled.

Moreover, as for the grid-side converter another control architecture was followed. Providing that stable dc-link voltage was the main requirement, the control was implemented in the rotational reference frame. It is worth adding that the tuning of the PI controllers was done by trial and error method, because there was no available information about the actual values of the gains in the FPGL during this study and some papers dispute the empirical rules that exist. The dc-link capacitors are modeled, always having initial voltage equal to the required dc-link voltage level, or in other words the dc-link capacitors are considered pre-charged. For this reason, a relatively high value for the outer I-controller eliminates the steady state error and simultaneously there is no concern about the overshoot. The chosen PI gains may differ from the values applied in the FPGL, and their selection has been done with main criterion the zero steady-state error. However in paragraph 5.5.3 a more realistic approach is presented as well.

In a nutshell, the Simulink model is a valuable tool, which is able to perform stability and power quality studies. Through simulations and ultimately emulations of the FPGL, many objects such as power inverters can be tested before they are connected to the grid, to certify that the disturbances are not exceeding the allowable levels as described in the corresponding standards. It is one more step towards the implementation of decentralized power generation, intelligent electricity networks and sustainable development.

7.2 Future Work

As the first release of the FPGL Simulink realization now exists, there are certainly many aspects in which the model can be improved:

- In Chapter 2, it is stated that PSCAD and ATP/EMTP meet also the necessary requirements for the FPGL modeling. Re-modeling of the lab in other platforms will show potential deficiencies of the current model, as well as by comparing results of different interfaces, it is possible to select the most accurate. These two programs have more sophisticated component models and they are Electro-Magnetic Transient Programs (EMTP), which will certainly enable transient studies.
- Moreover, the transformer and especially the converter protection is an aspect that is beyond the scope of this thesis. However, improving the current work by including the FPGL protection system in the model would be an interesting future project. The protection system will allow the FPGL user to push the lab's equipment to its limits, knowing in advance and of course avoiding failures.
- An even more accurate equivalent of the FPGL can be achieved by revising the assumptions stated in the report. The model can be further improved by integrating the saturation curve of the transformers, adjusting the PI gains of the AFE controller to correspond to reality, taking the PWM generator hardware's limitations into account and considering dead-time to make the load-side converter even more realistic.
- As it was mentioned in the beginning of this thesis, an ultimate goal is the use of the model in real-time simulations. Hardware-in-the-loop (HIL) simulations are deemed the future of testing. HIL simulation provides an effective platform by adding the complexity of the plant under control to the test platform. The complexity of the plant under control is included in the test and development by adding a mathematical representation of all related dynamic systems (plant

simulation). The embedded system to be tested interacts with the plant simulation. The sensors and actuators act as interface between the plant simulation and the embedded system under test. The value of each sensor is controlled by the plant simulation through feedback loops. Sometimes, it is more efficient to connect and test an embedded system to the plant simulation instead of the real plant, because it saves time, money and it is safer. Real-time simulations are typically applied at the end of the system design cycle to test the actual, control and protection systems. Several random tests can be performed to test the designed circuit under normal and faulty operation. The control and the protection can be tested under conditions that would be impractical or even dangerous to test when controllers are connected to our real power system. Hence real-time operation of the model is of high importance. MATLAB/Simulink through xPC Target and xPC Target Turnkey system (by Mathworks) create a hard real-time environment for Simulink models. Research in this specific topic and the development of the existing FPGL Simulink model in real-time environment would definitely be a great challenge.

- Power electronic converters are significantly affected by the heat dissipation and the cooling. These are of the main limiting factors for higher level of performance. The main power loss is considered to be at the p-n junction of the semiconductor elements. Not negligible losses emanate from passive elements, wirings and mechanical elements. These losses can be considered as the driving force for a thermal model development [44]. Although most of the practices so far allow the decoupled thermal management and power electronic control, a unified electro-thermal model would optimize the converter model performance, based on both thermal and electrical limitations. As a result, a combined model, the control of which takes into account additional boundaries and parameters, such as thermal bounds, could be the evolution of the existing model. The temperature effect would certainly increase the accuracy of the developed model. This improvement can be done by modeling of the thermal system as an electrical analog system - as described in [44] - or by use of specific software. PLECS blockset (by Plexim) is a tool for high-speed simulations of power electronic systems in Simulink environment. It enables the user to include thermal design with the electrical design in to order to be able to select suitable cooling solution.

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APPENDIX A : Single-line diagram of the FPGL

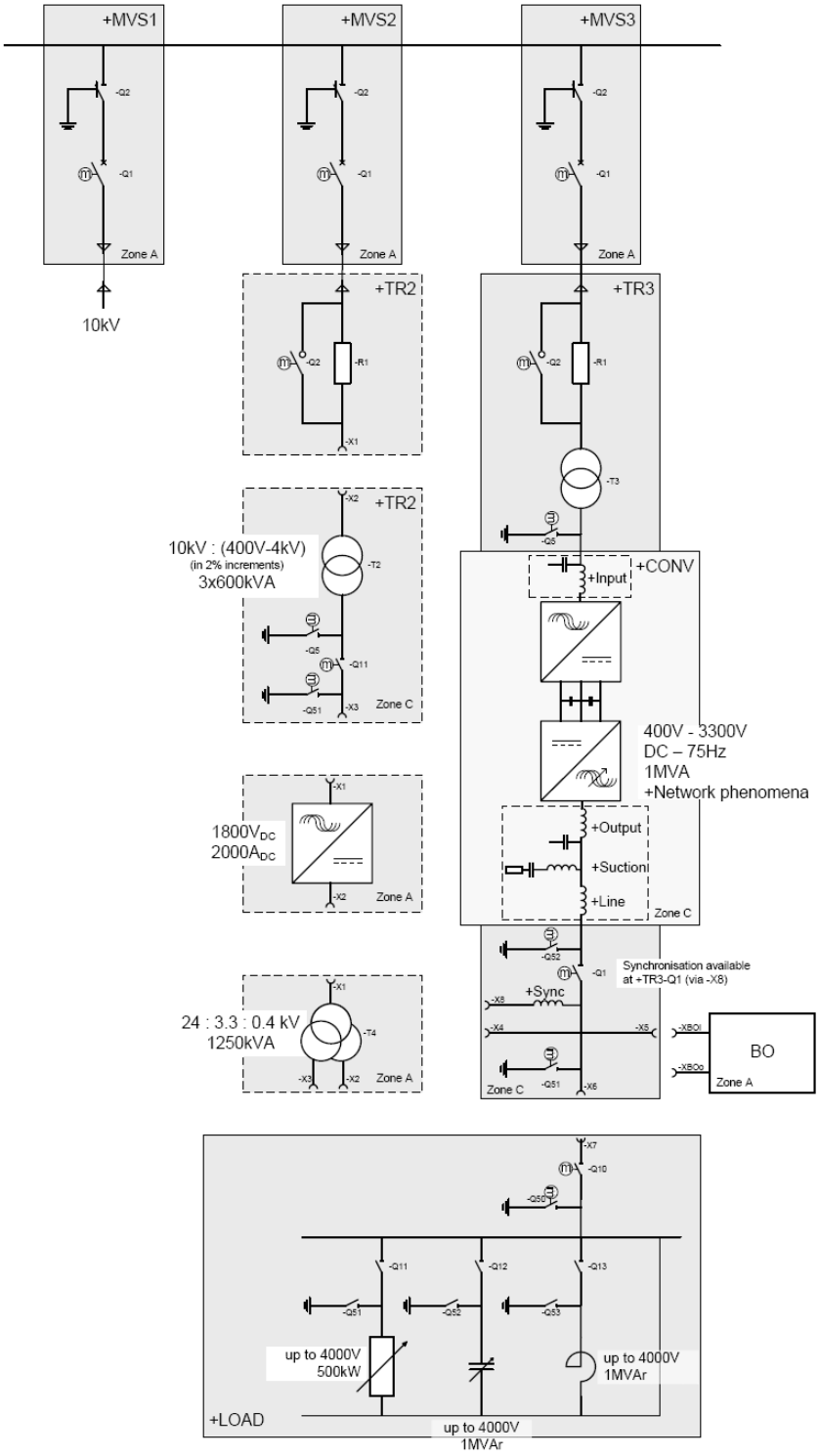


Figure A-1 Single-line diagram of the Flex Power Grid Lab

APPENDIX B : Transformers Tables

B.1 TR2/T2 Transformers

The base power of the transformers TR2/T2 is 600kVA. The voltage, current and impedance base values are shown in the Table B-1. The rest tables include all the useful for the modeling data provided by the witness test reports.

U_{1b} [V]	I_{1b} [A]	Z_{1b} [Ω]	L_{1b} [H]	U_{2b} [V]	I_{2b} [A]	Z_{2b} [Ω]	L_{2b} [H]
12500	48	260.4167	0.828932	2000	300	6.666667	0.021221
12000	50	240	0.763944	1000	600	1.666667	0.005305
11500	52.17391	220.4167	0.701608	500	1200	0.416667	0.001326
11000	54.54545	201.6667	0.641925				
10500	57.14286	183.75	0.584894				
10000	60	166.6667	0.530516				
9500	63.15789	150.4167	0.478791				
9000	66.66667	135	0.429718				
8500	70.58824	120.4167	0.383298				
8000	75	106.6667	0.339531				
7500	80	93.75	0.298416				
6250	96	65.10417	0.207233				
6000	100	60	0.190986				
5750	104.3478	55.10417	0.175402				
5500	109.0909	50.41667	0.160481				
5250	114.2857	45.9375	0.146224				
5000	120	41.66667	0.132629				
4750	126.3158	37.60417	0.119698				
4500	133.3333	33.75	0.10743				
4250	141.1765	30.10417	0.095825				
4000	150	26.66667	0.084883				
3750	160	23.4375	0.074604				

Table B-1 Transformer TR2/T2 base values

System	Connected	Position [V]	f_m [Hz]	U [V]	I_o [A]	I_o [%]	P_o [W]
2	2.1-2.2	1000	50	1000	1.37	0.23	991

Table B-2 Measurements of the no-load loss witness test (TR2/T2.1 - S/N: 0734062)

System	Connected	Position [V]	R [mΩ]	T[°C]
1	1.1-1.2	10000	812.6	18.8
1	1.1-1.2	12500	1037.5	18.8
1	1.1-1.2	7500	593.6	18.8
1	1.1-1.2	5000	203.3	18.8
1	1.1-1.2	6250	259.6	18.8
1	1.1-1.2	3750	148.5	18.8

2	2.1-2.3	-	5.191	18.8
2	2.4-2.5	-	5.199	18.8
2	2.6-2.7	-	5.159	18.8
2	2.2-2.8	-	5.172	18.8

Table B-3 Measurements of the DC resistance witness test (TR2/T2.1 - S/N: 0734062)

Connected	Short-circuited	I_m [A]	U_m [V]	P_m [W]	T[°C]	P_k [W] @75 °C	u_z [%]
10000	2000	30	414.6	5248	18.8	6226	8.31
12500	2000	24	544.9	4612	18.8	5490	8.73
7500	2000	40	281.3	5960	18.8	7161	7.53
5000	2000	60	207.2	5252	18.8	6230	8.31
10000	1000	30	414.1	5256	18.8	6232	8.30
5000	1000	60	207.2	5272	18.8	6246	8.31
10000	500	30	411.5	6200	18.8	7005	8.25
5000	500	60	206.1	6232	18.8	7032	8.26

Table B-4 Measurements of the load loss witness test (TR2/T2.1 - S/N: 0734062)

System	Connected	Position [V]	f_m [Hz]	U [V]	I_o [A]	I_o [%]	P_o [W]
2	2.1-2.2	1000	50	1000	1.45	0.23	986

Table B-5 Measurements of the no-load loss witness test (TR2/T2.2 - S/N: 0734061)

System	Connected	Position [V]	R [mΩ]	T[°C]
1	1.1-1.2	10000	814.3	18.6
1	1.1-1.2	12500	1040	18.6
1	1.1-1.2	7500	594.9	18.6
1	1.1-1.2	5000	203.7	18.6
1	1.1-1.2	6250	260.3	18.6
1	1.1-1.2	3750	149	18.6
2	2.1-2.3	-	5.185	18.6
2	2.4-2.5	-	5.177	18.6
2	2.6-2.7	-	5.154	18.6
2	2.2-2.8	-	5.166	18.6

Table B-6 Measurements of the DC resistance witness test (TR2/T2.2 - S/N: 0734061)

Connected	Short-circuited	I_m [A]	U_m [V]	P_m [W]	T[°C]	P_k [W] @75 °C	u_z [%]
10000	2000	30	417.9	5256	18.6	6238	8.38
12500	2000	24	547.9	4600	18.6	5485	8.78
7500	2000	40	282.9	5832	18.6	7063	7.57
5000	2000	60	209	5264	18.6	6245	8.38
10000	1000	30	417.9	5288	18.6	6264	8.38
5000	1000	60	208.8	5296	18.6	6271	8.37

10000	500	30	415.2	6172	18.6	6987	8.32
5000	500	60	207.8	6200	18.6	7011	8.33

Table B-7 Measurements of the load loss witness test (TR2/T2.2 - S/N: 0734061)

System	Connected	Position [V]	f_m [Hz]	U [V]	I_o [A]	I_o [%]	P_o [W]
2	2.1-2.2	1000	50	1000	1.44	0.23	971

Table B-8 Measurements of the no-load loss witness test (TR2/T2.3 - S/N: 0734060)

System	Connected	Position [V]	R [mΩ]	T[°C]
1	1.1-1.2	10000	817.5	19
1	1.1-1.2	12500	1043.5	19
1	1.1-1.2	7500	597.7	19
1	1.1-1.2	5000	204.7	19
1	1.1-1.2	6250	261.3	19
1	1.1-1.2	3750	149.7	19
2	2.1-2.3	-	5.175	19
2	2.4-2.5	-	5.155	19
2	2.6-2.7	-	5.171	19
2	2.2-2.8	-	5.205	19

Table B-9 Measurements of the DC resistance witness test (TR2/T2.3 - S/N: 0734060)

Connected	Short-circuited	I_m [A]	U_m [V]	P_m [W]	T[°C]	P_k [W] @75 °C	u_z [%]
10000	2000	30	417.1	5256	19	6235	8.36
12500	2000	24	548.6	4508	19	5406	8.79
7500	2000	40	283.3	5986	19	7187	7.58
5000	2000	60	208.8	5272	19	6250	8.37
10000	1000	30	417.9	5280	19	6254	8.38
5000	1000	60	208.9	5292	19	6266	8.37
10000	500	30	415.1	6260	19	7057	8.32
5000	500	60	207.4	6272	19	7069	8.31

Table B-10 Measurements of the load loss witness test (TR2/T2.3 - S/N: 0734060)

B.2 TR3/T4 Transformer

The base power of the transformer TR3/T4 is 1.25MVA. The voltage, current and impedance base values are shown in the Table B-11. The rest tables give the measured outcomes of the witness tests.

	U_b [V]	I_b [A] line current	Z_b [Ω]	L_b [H]
System 1	24000	30.1	1382.4	4.4
System 2	3300	219	8.712	0.0277
System 3	400	1804	0.128	0.000407

Table B-11 Transformer TR3/T4 base values

System	Connected	U[V]	f_m [Hz]	I_u [A]	I_v [A]	I_w [A]	I_o [A]	I_o [%]	P_o [W]
3	3U-3V-3W	400	50	10.44	7.09	9.96	9.16	0.51	3154

Table B-12 Measurements of the no-load loss witness test (TR3/T4)

System	Connected	Position [V]	U-V [mΩ]	V-W [mΩ]	W-U [mΩ]	T[°C]
1	1U-1V-1W	24000	6067	6057	6069	23.5
2	2U-2V-2W	3300	70.95	71.06	70.97	23.5
3	3U-3V-3W	400	0.5407	0.5405	0.5629	23.5

Table B-13 Measurements of the DC resistance witness test (TR3/T4)

Connected	Short-circuited	I_m [A]	U_m [V]	P_m [W]	T[°C]	P_k [W] @75 °C	u_z [%]
24000	3300	15.05	826.3	14048	23.5	16590	6.92
24000	400	15.05	1672	13136	23.5	14944	13.94
3300	400	109.5	112.8	8828	23.5	10208	6.85

Table B-14 Measurements of the load loss witness test (TR3/T4)

B.3 TR3/T3 Transformer

The power, voltage, current and impedance base values are shown in the Table B-15. The rest tables give the measured outcomes of the witness tests.

System	P_b [VA]	U_b [V]	I_b [A] line current	Z_b [Ω]	L_b [H]
1	1700000	10500	93.476	194.56	0.62
2	1700000	3800	258	8.49	0.027
1	850000	10500	46.74	389.12	1.24
2	850000	1900	258	4.25	0.014
1	425000	10500	23.37	778.24	2.124
2	425000	950	258	2.477	0.00676

Table B-15 TR3/T3 transformer base values

System	Connected	U[V]	f_m [Hz]	I_u [A]	I_v [A]	I_w [A]	I_o [A]	I_o [%]	P_o [W]
2	2U-2V-2W	3800	50	0.48	0.35	0.55	0.46	0.02	2368

Table B-16 Measurements of the no-load loss witness test (TR3/T3)

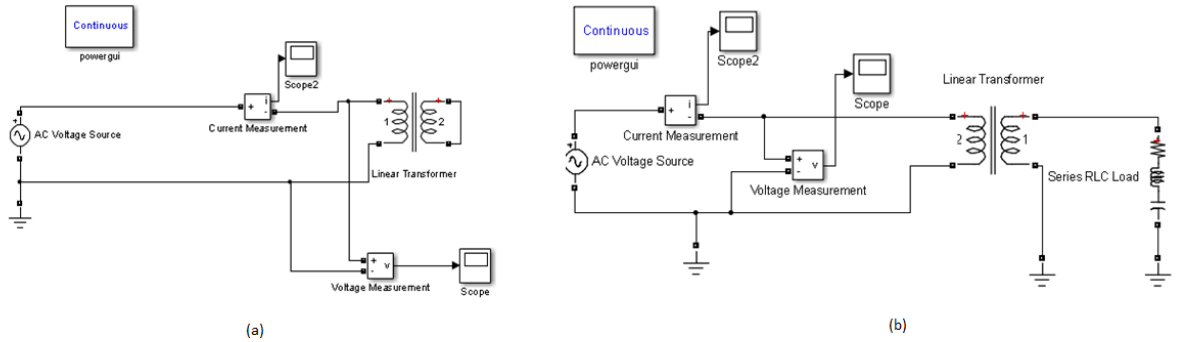
System	Connected	Position [V]	U-V [mΩ]	V-W [mΩ]	W-U [mΩ]	T[°C]
1	1U-1V-1W	10500	588	589	590	19.1
2	2U-2V-2W	3800	37.27	37.33	37.28	19.1
2	2U-2V-2W	1900	17.11	17.11	17.13	19.1
2	2U-2V-2W	950	8.725	8.704	8.731	19.1

Table B-17 Measurements of the DC resistance witness test (TR3/T3)

Connected	Short-circuited	I_m [A]	U_m [V]	P_m [W]	T[°C]	P_k [W] @75 °C	u_z [%]
10500	3800	46.7	337.7	12304	19.1	14662	6.45
10500	1900	23.4	223.6	3936	19.1	4688	4.27
10500	950	11.7	118.4	1444	19.1	1728	2.27

Table B-18 Measurements of the load loss witness test (TR3/T3)

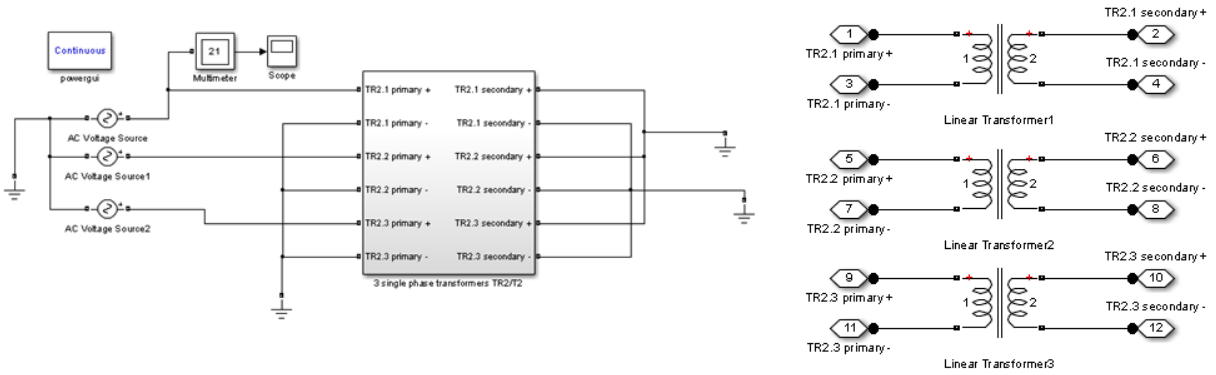
APPENDIX C : Transformers' Simulink models



(a) (b)

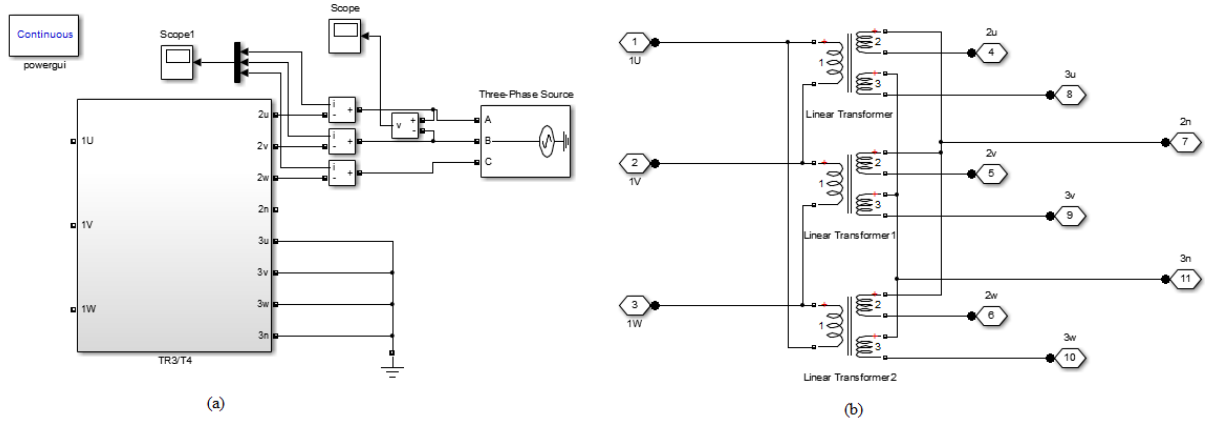
Figure C-1 TR2/T2 Simulink model (a) short circuit implementation, (b) open circuit implementation

Since in Simulink environment, all elements must be electrically connected, the System 1 of the transformer cannot be left open and a load has to be connected. In order to simulate no-load condition, constant impedance model to reflect loading is used, and the resistance and inductance values are set to very large numbers while the value of the capacitor is set to a very small number. The resulting secondary current will be approximately zero.



(a) (b)

Figure C-2 TR2/T2 three-phase Simulink model (a) masked (short circuit implementation, (b) unmasked



(a) (b)

Figure C-3 TR3/T4 three-phase Simulink model (a) masked short circuit implementation, (b) unmasked

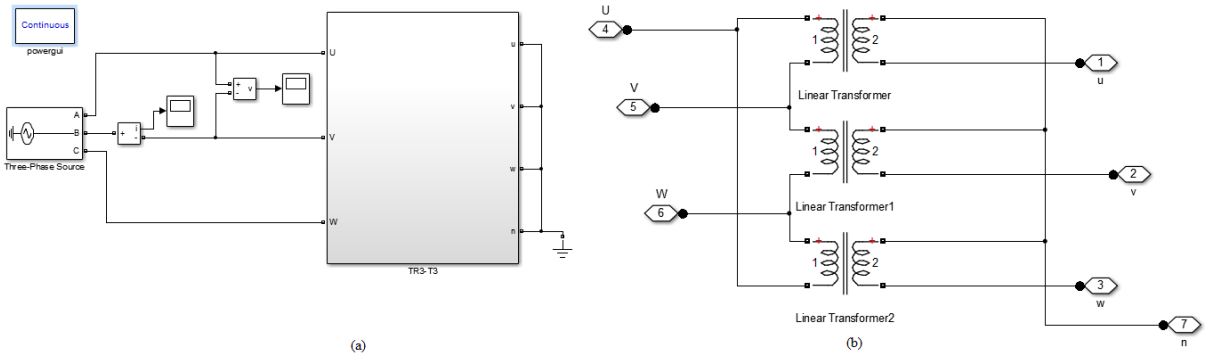


Figure C-4 TR3/T3 three-phase Simulink model (a) masked short circuit implementation, (b) unmasked

APPENDIX D : Grid line Simulink model

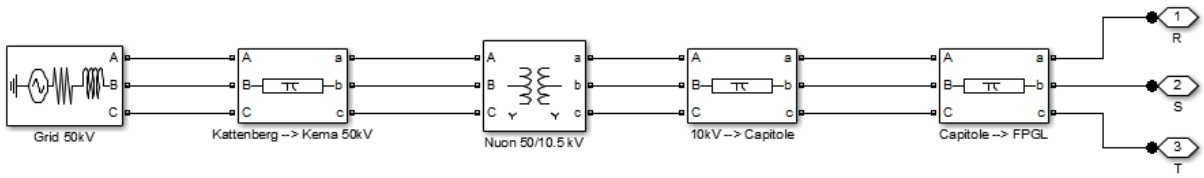


Figure D-1 50kV grid to FPGL bus-bar equivalent model

APPENDIX E : Converter's Simulink models

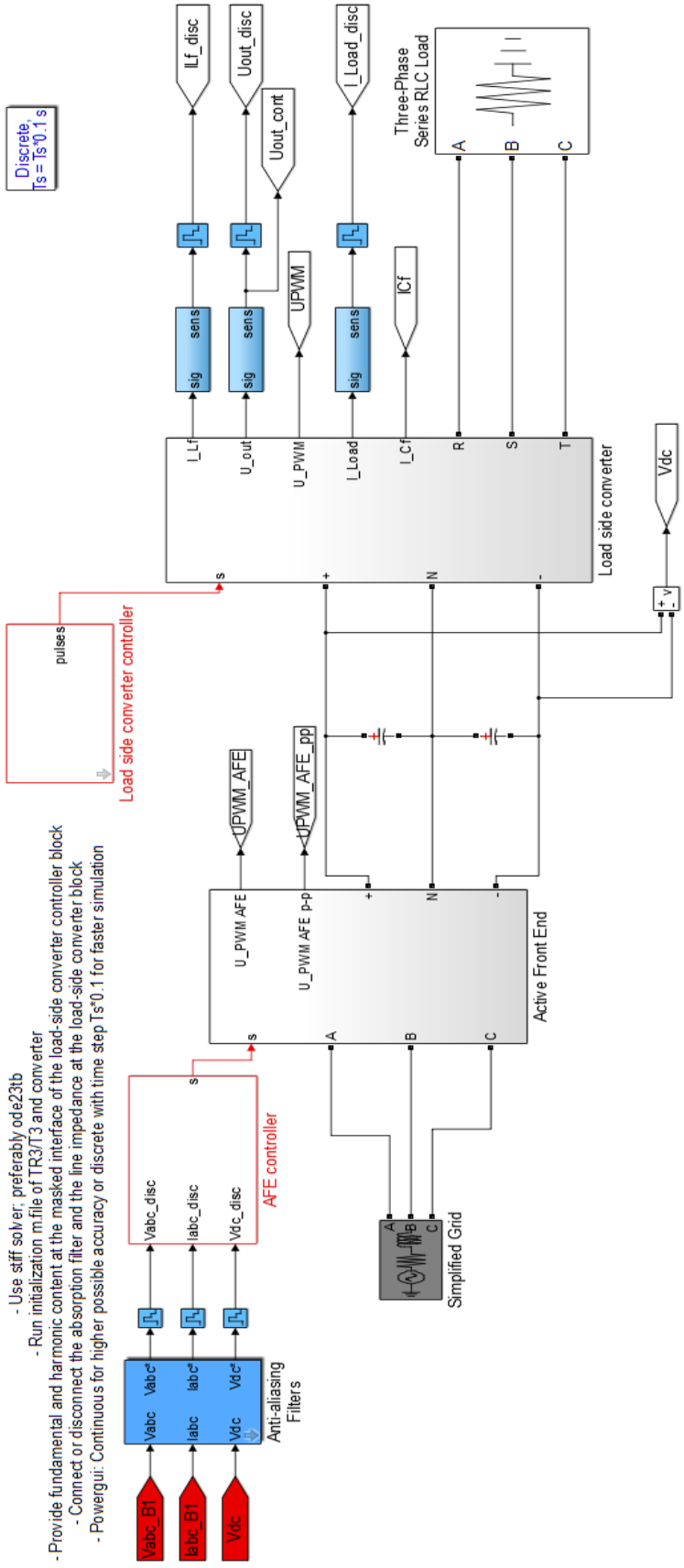


Figure E-1 Complete converter model including the grid-connected AFE, the load side converter and their controllers

E.1 Load-side converter

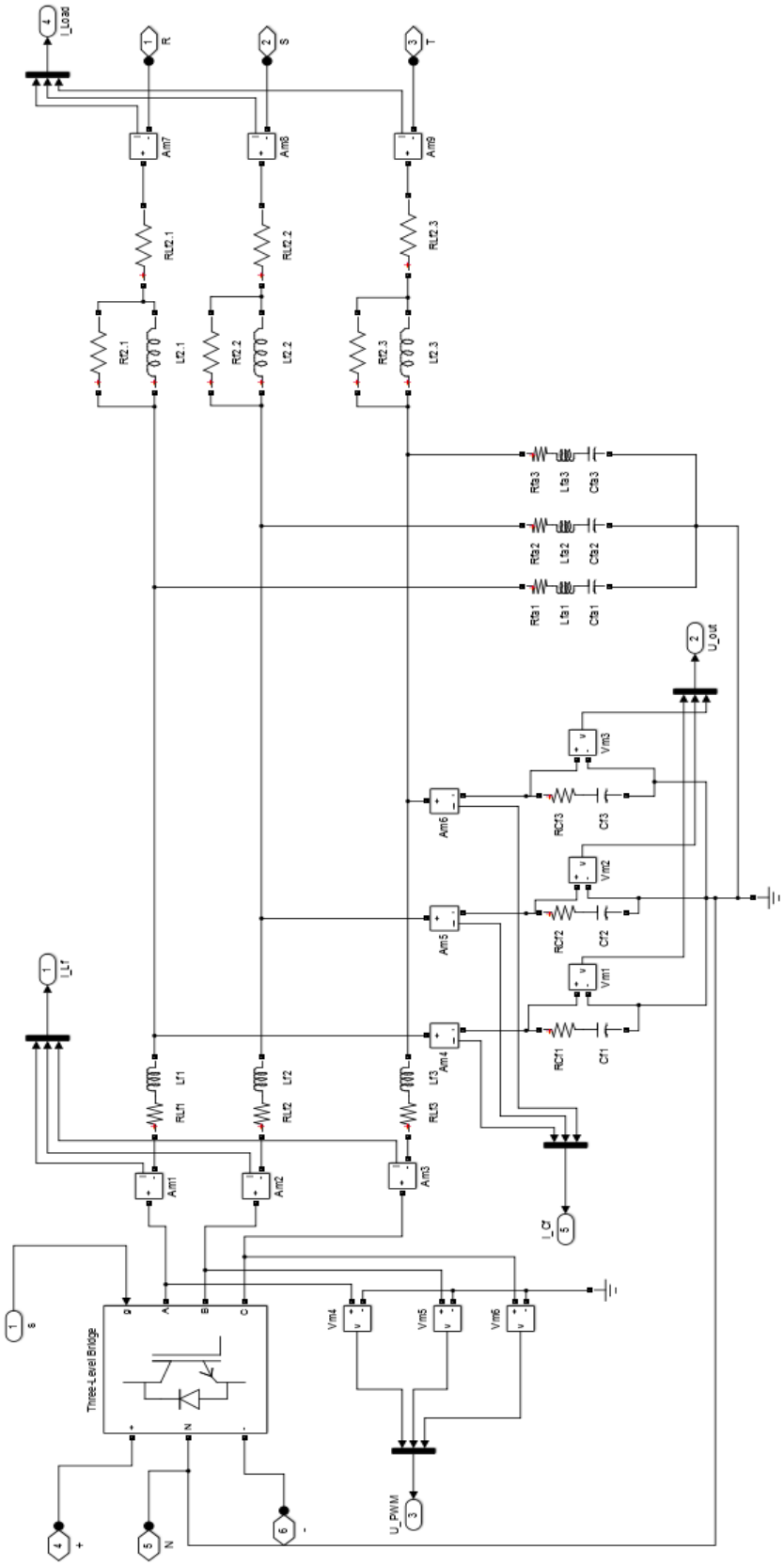


Figure E-2 Plant of the system - Three-level converter including LC filter, absorption filter and line impedance

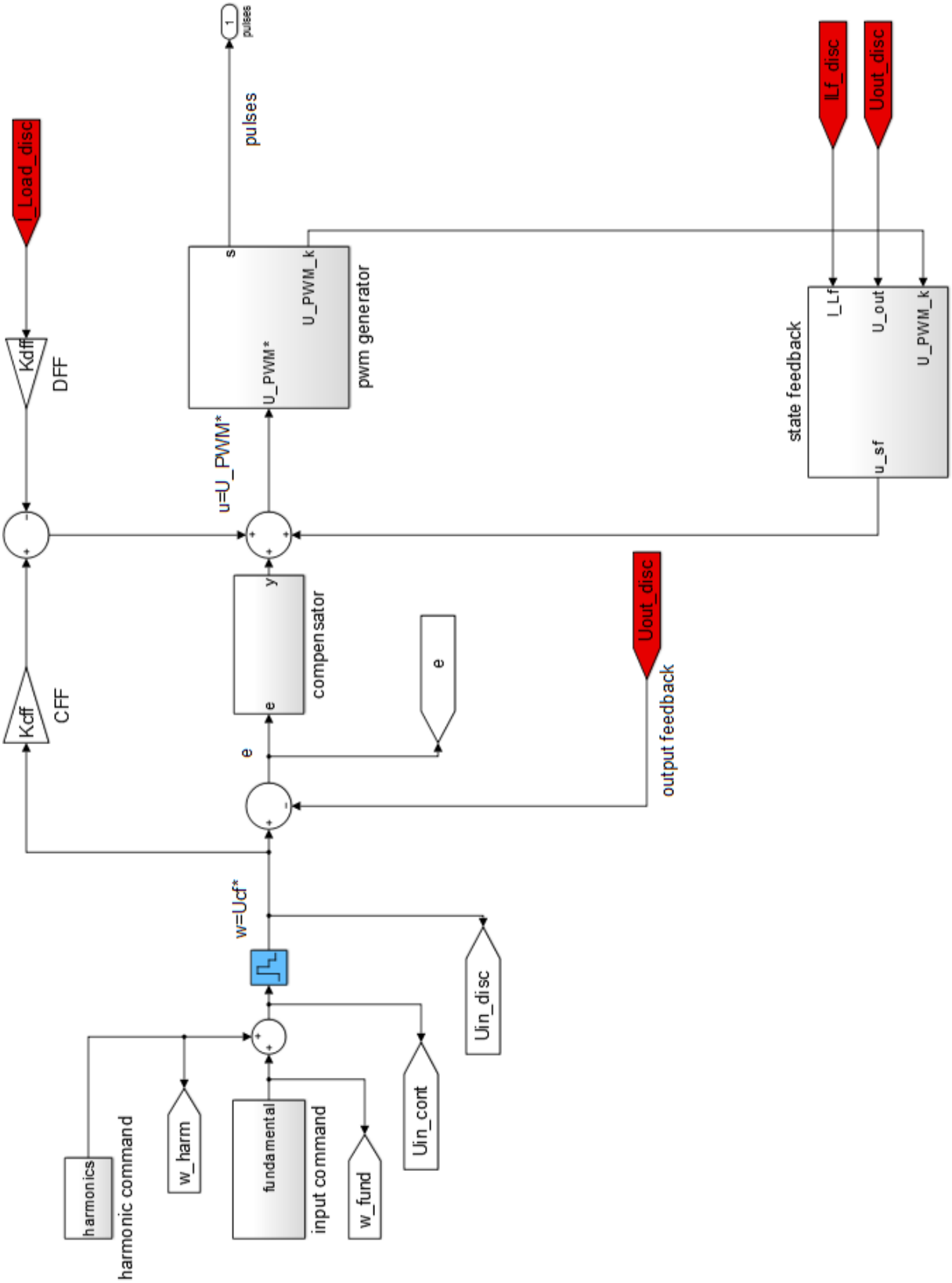


Figure E-3 Overview of the controller

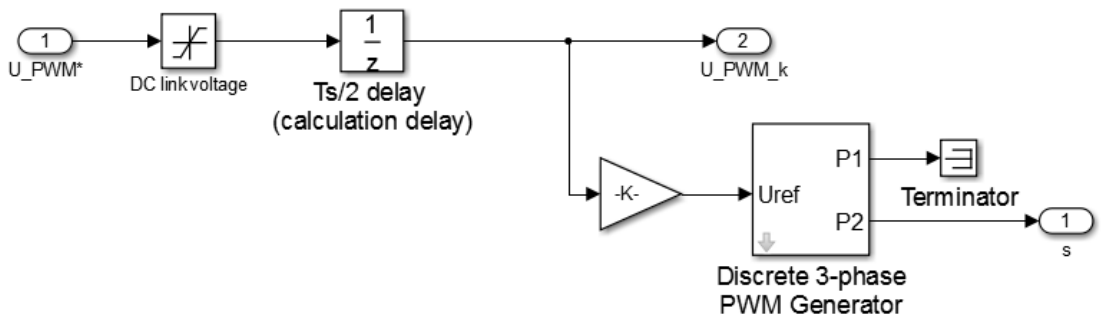


Figure E-4 PWM generator including calculation delay

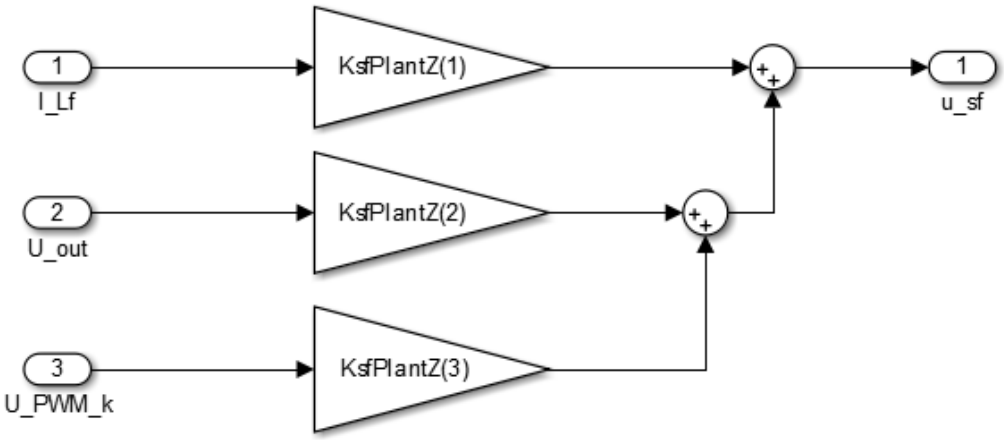


Figure E-5 State-feedback block

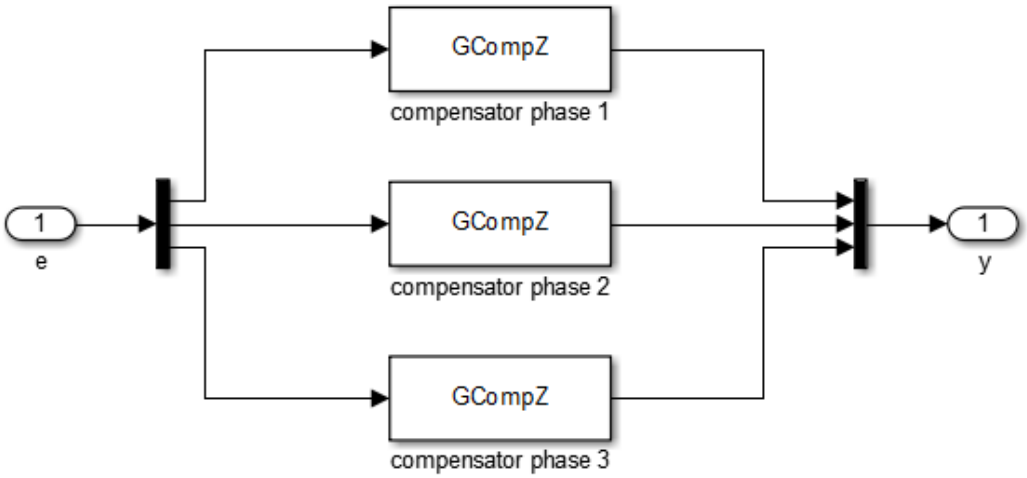


Figure E-6 Compensator implemented as LTI system

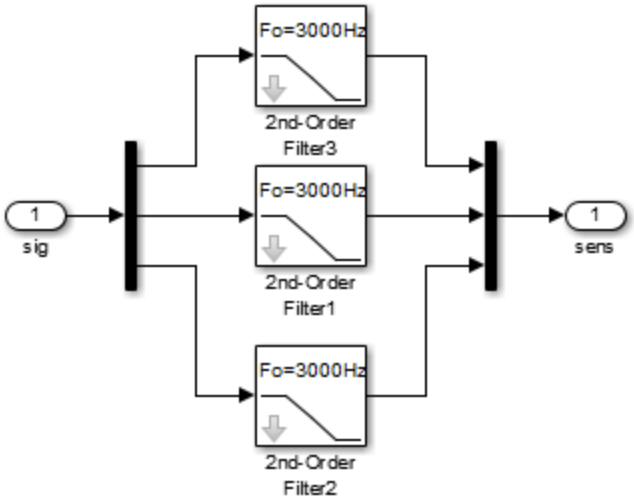


Figure E-7 Anti-aliasing filter (implemented as 2nd order low-pass filter)

E.2 Grid-side Converter (Active Front End)

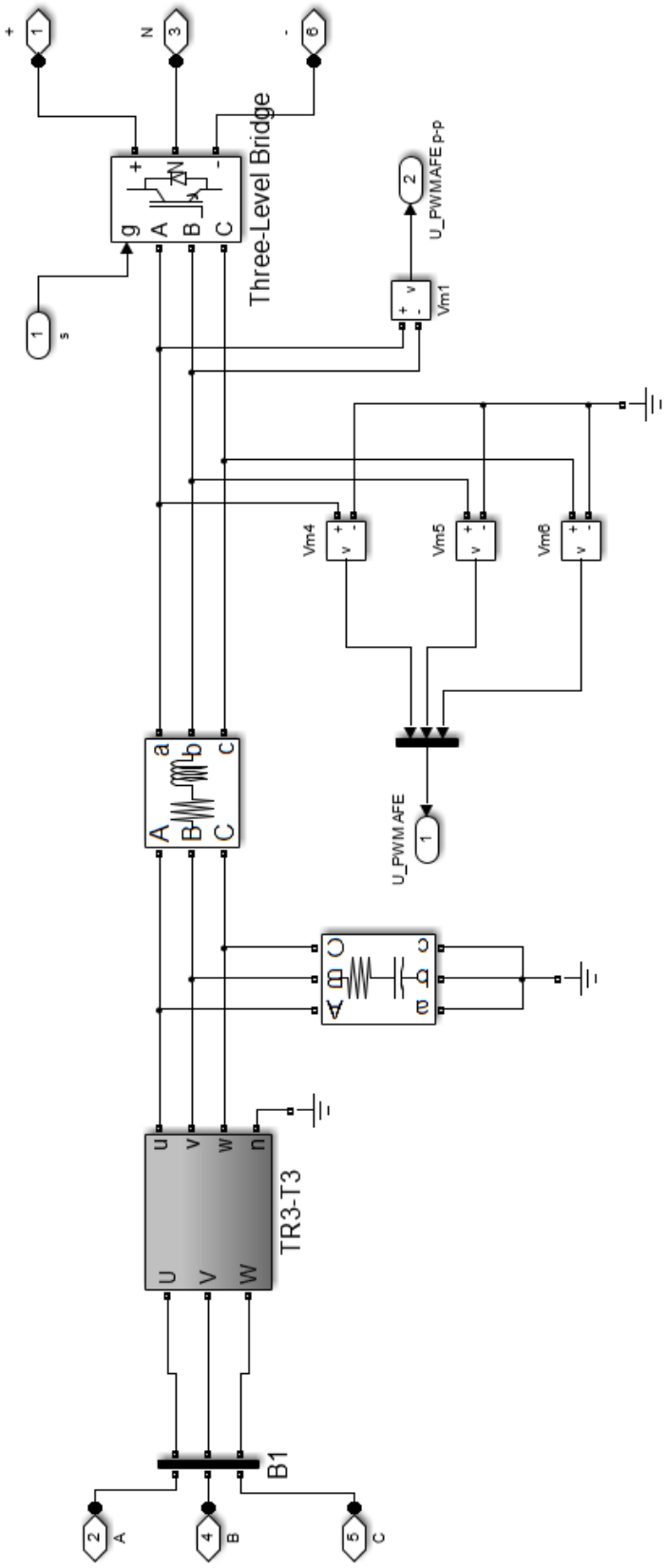


Figure E-8 Plant of the system – Three-level converter including LC filter, TR3/T3 transformer and B1 measurement point

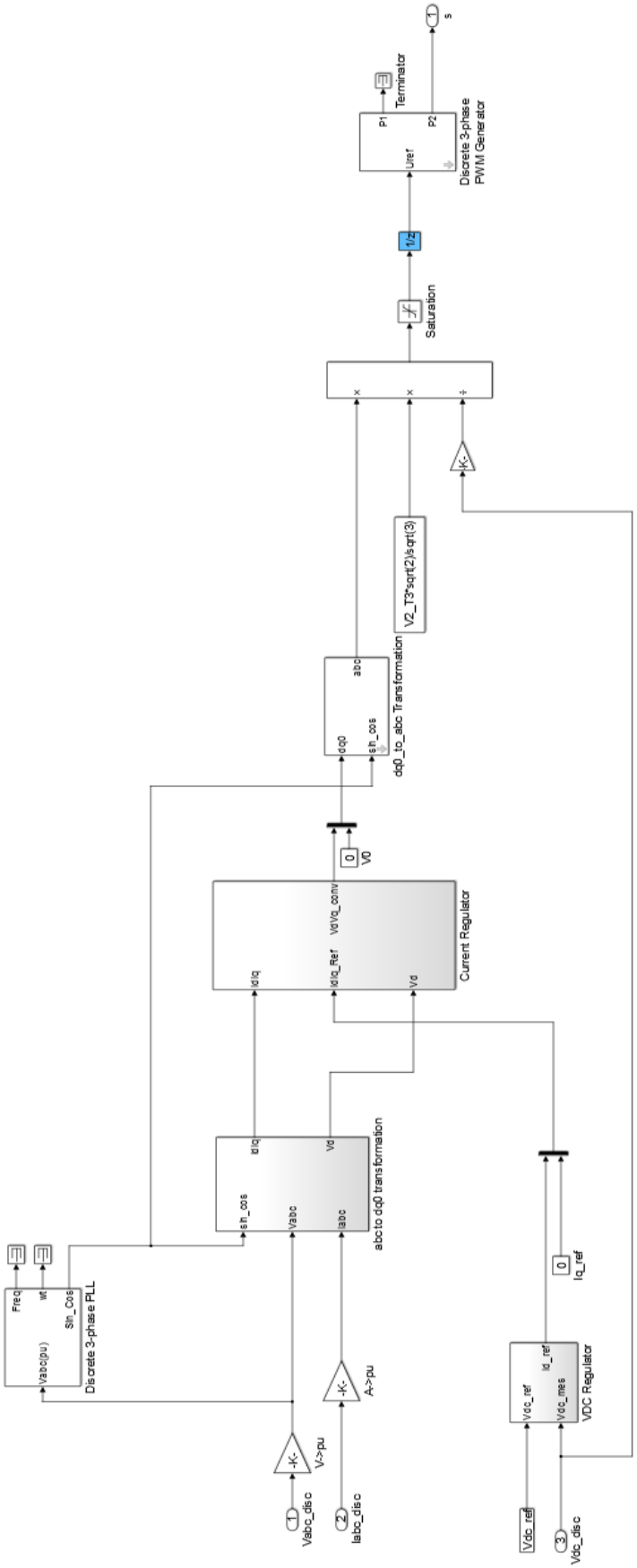


Figure E-9 Overview of the controller

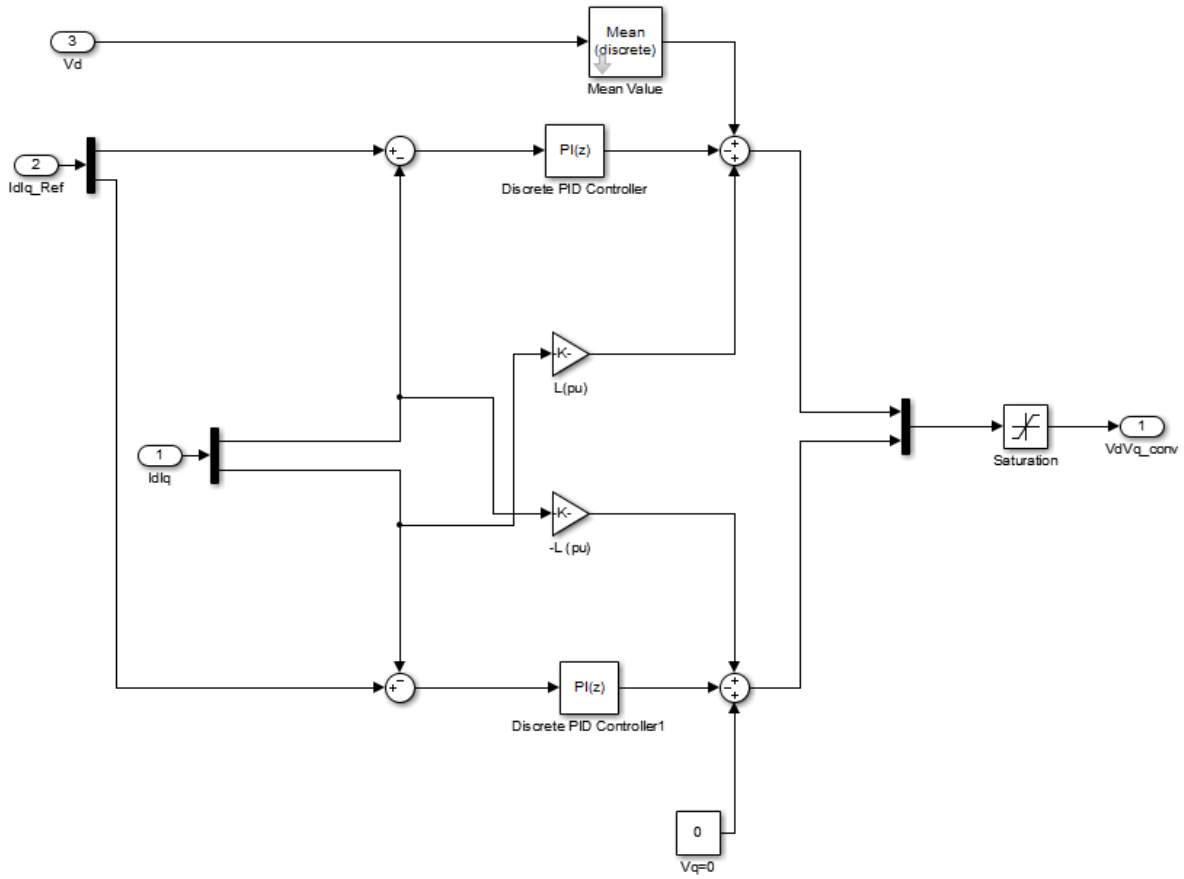


Figure E-10 Current regulator

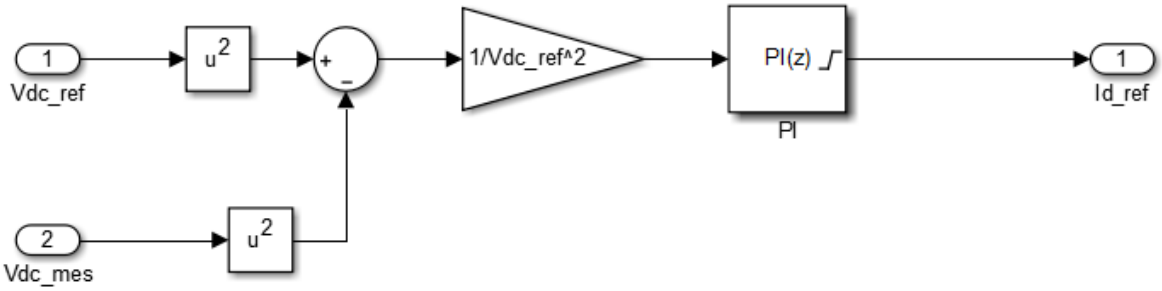


Figure E-11 DC Voltage regulator

APPENDIX F : Three-phase system – Coordinate transformations

- **3-phase system definition**

Positive sequence:

$$u_a = E_m \cos(\omega t) \quad \text{F-1}$$

$$u_b = E_m \cos\left(\omega t - \frac{2\pi}{3}\right) \quad \text{F-2}$$

$$u_c = E_m \cos\left(\omega t + \frac{2\pi}{3}\right) \quad \text{F-3}$$

For any three-phase system composed of positive and negative sequence:

$$u_a(t) + u_b(t) + u_c(t) = 0 \quad \text{F-4}$$

If the system presents any asymmetry, a zero sequence appears:

$$u_0(t) = \frac{u_a(t) + u_b(t) + u_c(t)}{3} \quad \text{F-5}$$

- **Equivalent 2-phase system – αβ transformation (Clarke)**

A three-phase system can be described by only two components; the real α and the imaginary β.

$$u_s(t) = u_\alpha(t) + j \cdot u_\beta(t) = \frac{2}{3}\left(u_a(t) + u_b(t) e^{j\frac{2\pi}{3}} + u_c(t) e^{-j\frac{2\pi}{3}}\right) \quad \text{F-6}$$

The transformation from abc to αβ, Clarke transformation, can be done according to equations F-7 and F-8:

$$\begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ 0 & 1/\sqrt{3} & -1/\sqrt{3} \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad \text{F-7}$$

$$\begin{bmatrix} a \\ b \\ c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} \alpha \\ \beta \end{bmatrix} \quad \text{F-8}$$

- **Synchronous coordinate – dq transformation (Park)**

The rotating dq0 reference is now defined as: $u_{dq} = u_s e^{-j\theta}$, where $\theta = \omega t$. This coordinate is the space vector rotating with the frequency ω (synchronous).

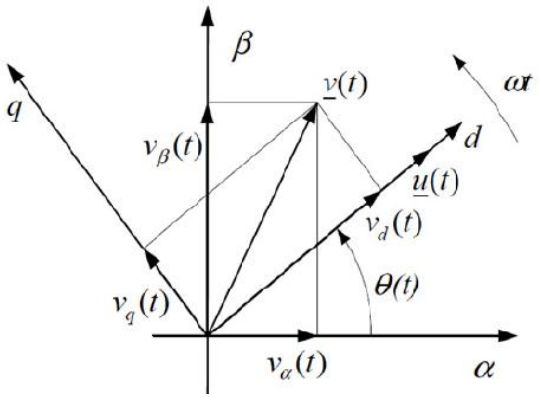


Figure F-1 αβ and dq reference frames

The transformation from αβ to dq reference, Park transformation, can be done as follows:

$$\begin{bmatrix} d \\ q \end{bmatrix} = \begin{bmatrix} cos\vartheta & sin\vartheta \\ -sin\vartheta & cos\vartheta \end{bmatrix} \begin{bmatrix} \alpha \\ \beta \end{bmatrix} \quad \text{F-9}$$

$$\begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \begin{bmatrix} cos\vartheta & -sin\vartheta \\ sin\vartheta & cos\vartheta \end{bmatrix} \begin{bmatrix} d \\ q \end{bmatrix} \quad \text{F-10}$$