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***Abstract*—This work presents the design and simulation of a PVT-robust x16 gain dynamic open-loop inverter-based Gm-ratio residue-amplifier for high-speed SAR-assisted pipeline ADCs. The amplifier is designed in a 28 nm standard bulk CMOS process with a regulated 0.9 V power supply and simulated across a -20°C to 85°C temperature range. It achieves a power dissipation of 1.67 mW at 1.3 GHz, corresponding to a power-speed ratio of 1.28 mW/GHz, with less than $\pm 5\%$ gain variation throughout all temperature corners in typical conditions.**

***Index Terms*—pipeline analog-to-digital converter (ADC), PVT-robust residue amplifier, gm-ratio residue amplifier**

I. Introduction

Successive-approximations-register (SAR) assisted pipeline analog-to-digital converters (ADCs) enable moderate-to-high resolution and conversion-rate applications while improving the energy efficiency that pipeline ADCs typically exhibit [1]. A first-stage with higher resolution enabled by a fast SAR-ADC facilitates the linearity improvement of pipeline ADCs. However, this makes the design of a residue-amplifier (RA) with a accurate DC-gain challenging.

RA DC-gain inaccuracies due to process-voltage-supply-temperature (PVT) variations severely impact the resolution of the ADC. Digital calibration techniques can compensate for PVT-variations, but require the interruption of the conversion process, limiting conversion-rates. It also requires additional circuitry, increasing complexity and power dissipation [2], [3]. Analog PVT compensation schemes using DC bias sensing and control provide an alternative to digital calibration. Classic closed-loop static OTA designs offer PVT-robust RAs through negative feedback but have lower energy efficiency at high conversion rates [4]. Dynamic open-loop amplifiers achieve higher energy efficiency and conversion speeds but are more sensitive to PVT-variations due to the lack of common-mode control. Additional analog circuitry can be used to implement PVT-dependent settling time at the expense of introducing device mismatch issues [5–7]. Multistage closed-loop dynamic amplifier topologies, such as ring amplifiers and floating-inverter amplifiers (FIAs), offer PVT-robust RA architectures but have lower energy efficiency and stability issues at high speeds [2], [3], [8]. Open-loop dynamic gm-ratio residue-amplifiers (GGRA) enable energy-efficient high-speed RAs with accurate gain but still require digital reference-trimming strategies to mitigate the lack of DC gain accuracy throughout PVT corners [9], [10]. Additionally, due to the devices' lower output impedance, achieving moderate-to-high DC gains in GGRAs requires aggressive power dissipation and area trade-offs at advanced technology nodes. Power dissipation can be minimised through the use of minimum channel-length ($\mathrm{L_{ch}}$) devices in high-speed channels, but requires disproportional channel-width ($\mathrm{W_{ch}}$) ratios within GGRA architectures to compensate for the lack of DC gain, leading to additional distortion, power dissipation, and die-area. Increasing the output impedance of each stage within GGRAs can thus lead to lower power-dissipation and smaller die area. Three approaches can be used to increase the output impedance of inverter-based OTAs: 1) sacrificing bandwidth and power dissipation for longer channel lengths, 2) sacrificing voltage headroom and output swing for the use of cascode devices, 3) using a harmonic-injection cross-coupled pair (HXCP) as a negative resistor at the output of the inverter-based OTA at the expense of additional power-dissipation [11].

This work presents a PVT-robust $\times 16$ gain dynamic open-loop inverter-based GGRA. It comprises common-mode feed-forward (CMFF) and feedback (CMFB) networks to address PVT-variations-related CM shifts and DC gain errors. An HXCP is used to lower the RA's output conductance without reducing its output voltage swing, leading to higher DC gain with lower power-dissipation and die area, while also compensating for the additional output load caused by CMFF and CMFB networks. The document is divided into five sections: overall pipelined-SAR ADC architecture and RA specifications (Section II), study and design methodology of the proposed RA (Section III), discussion of the simulation results (Section IV), and conclusions and a comparison with the current state-of-the-art (Section V).

II. SAR-Assisted Pipeline ADC Architecture Overview

A 12-bit SAR-assisted 2-stage pipeline ADC is shown in Fig.1 a). It comprises a 6-bit front-end SAR-ADC quantizer

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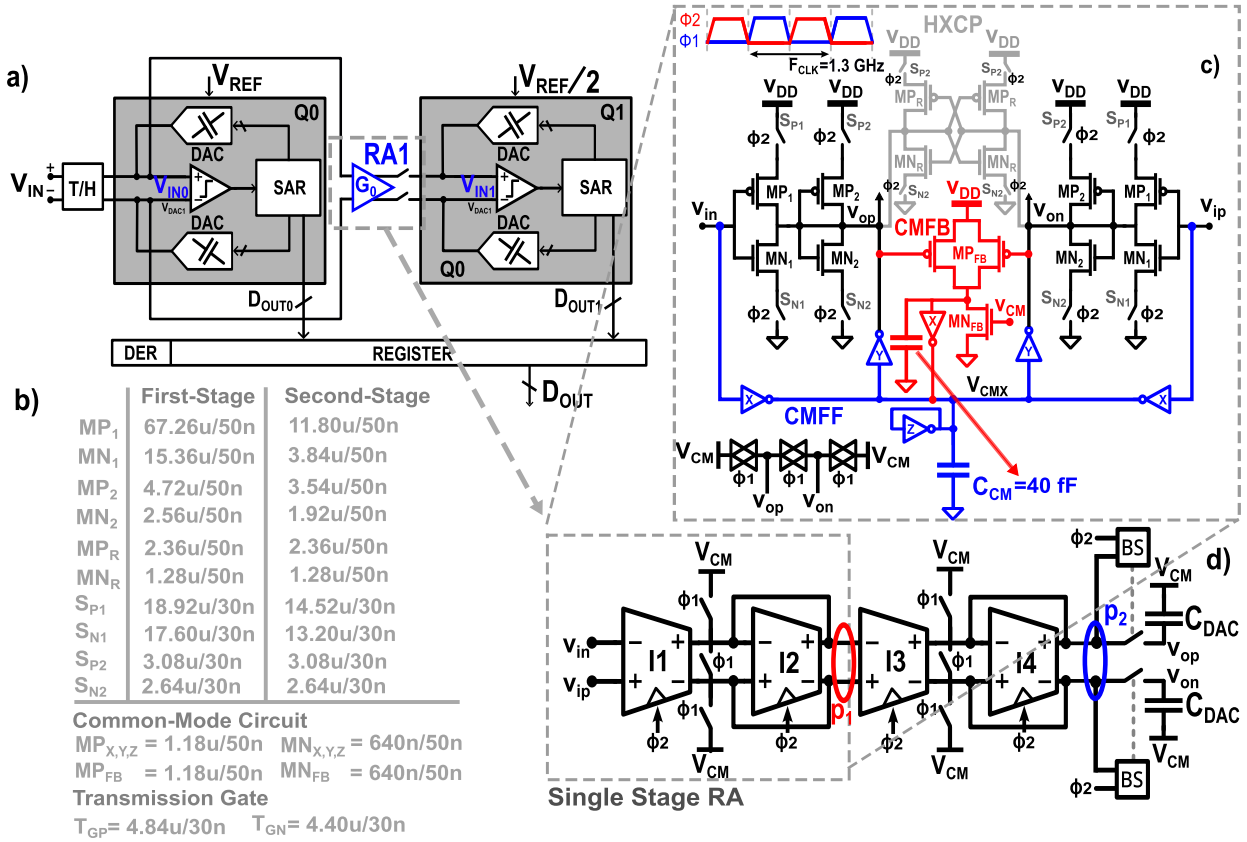

Fig. 1. a) 12-bit SAR-Assisted Pipeline ADC architecture, b) Gm-Ratio two-stage RA sizings, c) Proposed inverter-based Gm cell using common-mode feedback and feedforward circuits, d) Gm-Ratio two-stage RA block-architecture. The non-explicit bulk terminals of the PMOS and NMOS devices indicate that the bulks are connected to V_{DD} and V_{SS}, respectively.

(Q0) with 1-bit redundancy, followed by a 7-bit back-end quantizer (Q1). The $\times 16$ DC gain of the RA complements with the $\times 2$ gain of Q1's DAC to achieve the required $\times 32$ gain. Limitted by the $\mathrm{kT/C}$ noise constraints to ensure the target effective number of bits (ENOB) of > 9.0 bits, the total load capacitances of Q0 and Q1's DAC are 640 fF and 40 fF, respectively. Accounting for voltage supply variations, the gain-error-ratio (GER) limits for the RA are bound to $\pm$ 5% (3σ), to facilitate the achievement of the target ENOB.

III. Proposed Residue Amplifier

A. Common-mode Feedback and Feedforward

The RA (Fig.1 d)) is implemented by cascading two GGRA stages (Fig.1 c)). The design features core devices only. The common-mode feedforward circuit (CMFF) and common-mode feedback circuit (CMFB) are represented in Fig.1 c) in blue and red, respectively. The CMFF and CMFB circuits provide a negative CM feedback directly applied to the $\mathrm{V_{op}}$ and $\mathrm{V_{on}}$ nodes through the Y inverters (IY). CM voltage variations due to PVT-variations are compensated through the shared V_{CMX} node, as depicted in Fig.2 c). The CMFF is implemented through inverters X (IX), cancelling out their output AC currents at the $\mathrm{V_{CMX}}$ node, as represented in Fig.2 b). The CMFB is implemented through devices $\mathrm{MP_{FB}}$ and $\mathrm{MN_{FB}}$, operating in the saturation region and cancelling out their channel AC currents, as shown in Fig.2 a). The resulting DC current establishes a $\overline{\mathrm{V_{CMO}}}$ DC voltage with the opposite dynamic of the output CM voltage ($\mathrm{V_{CMO}}$) at the drain of $\mathrm{MN_{FB}}$. The Z inverter (IZ) introduces a CM pole $s_{P_{CM}} \approx -g_{m_Z}/C_{CM}$, filtering out unwanted, switching-related, high-frequency harmonics from V_{CMX}.

B. Single-Stage Analysis

1) PVT-Variations Sensitivity Analysis: The gain of a single stage k of the RA ($A_{V\,k}(s)$) is shown in (1), obtained using the small-signals model circuit in Fig.1 c).

$$A_{V\,k}(s) = -2\frac{G_{m\,k,1} - C_{dg\,k,1}s}{G_{m\,k,2} + g_o - G_{m\,k,R} + s\,(C_{L\,k} + C_{P\,k})} \quad (1)$$

where $G_{m\,k,1}$ and $G_{m\,k,2}$ are the transconductances of the first and second inverter of the RA, respectively, g_o is the total output conductance of the stage, $G_{m\,k,R}$ is the transconductance of the HXCP's IR inverter, $C_{L\,k}$ is the load capacitance of the stage and $C_{P\,k}$ is the total parasitic capacitance at the output node.

The sensitivity of $A_{V\,k}(0)$ against channel transconductance (G_m) variations of each OTA is shown in (2). This result was

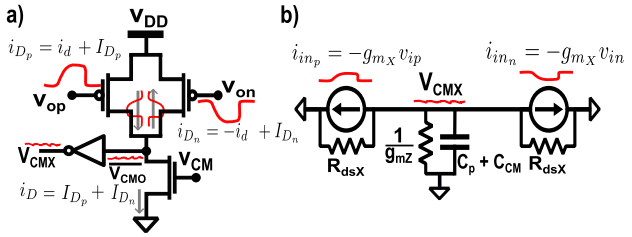

Fig. 2. a) Common-mode feedback circuit, b) Equivalent small-signal model of the common-mode feedforward circuit.

used to study the impact of PVT-variations on the DC gain of the RA.

$$S_{G_m}^{A_{V\,k}(0)} = \frac{\partial A_{V\,k}(0)}{\partial G_{m\,k,1}} \frac{G_{m\,k,1}}{A_{V\,k}(0)} + \frac{\partial A_{V\,k}(0)}{\partial G_{m_K}} \frac{G_{m\,k,2}}{A_{V\,k}(0)} + \\ + \frac{\partial A_{V\,k}(0)}{\partial G_{m\,k,R}} \frac{G_{m\,k,R}}{A_{V\,k}(0)} = \frac{g_o}{G_{m\,k,2} + g_o - G_{m\,k,R}} \tag{2}$$

Equation (2) shows that reducing the output conductance g_o by increasing $\mathrm{L_{ch}}$ or boosting $G_{m\,k,2}$ by enlarging the OTA's $\mathrm{W_{ch}}$ decreases $|S_{G_m}^{A_{V\,k}(0)}|$, being in conformity Pelgrom's Law [12]. However, increasing $G_{m\,k,R}$ increases PVT variations in each stage's DC gain. Moderately scaling up HXCP's devices is needed to reduce die area and power-dissipation, allowing scale-down of the RA's main devices $(\mathrm{M1-M4})_{\mathrm{A,B}}$.

2) Non Linear Distortion and Noise: Careful CM pole placement and proper reset transmission gate sizing facilitates differential DC offset spur cancelling. Even harmonics are eliminated from the differential output signal. In such conditions, a single RA stage's total harmonic distortion (THD) is dominated by the third-order harmonic distortion (HD3) within its bandwidth, as expressed (3).

$$HD_3 \approx \left| \eta \Big/ \left(3\,\eta + \frac{4\left(G_{m\,k,2} - G_{m\,k,R} + \frac{G_{m\,k,1}}{A_{V\,k}(0)} \right)}{\left(A_{in} A_{V\,k}(0) \right)^2} \right) \right| \tag{3}$$

where $\eta = G_{m\,k,2}^{(3)} - G_{m\,k,R}^{(3)} + \frac{G_{m\,k,1}^{(3)}}{(A_{V\,k}(0))^3}$, $G_{m\,X}^{(3)} = \frac{1}{3}\left(g_{m3_{N\,X}} + g_{m3_{P\,X}} \right)$ and $g_{m3_{N\,X}}$ is modelled using the EKV transistor model.

Eq. (3) shows that increasing the transconductance of each inverter will extend the bandwidth of the stage, decreasing the settling-time, and consequently decreasing HD3. On the other hand, increasing the DC gain of each stage (either by increasing $G_{m\,k,R}$ or the L_{CH} of the CMOS devices) will limit its bandwidth, leading to an increase in HD3.

$$Vn_i^2 = \int_0^\infty \frac{S_{V_o}(f)}{|A_{V\,k}(f)|^2} df \approx \frac{S_{V_o}(0)}{|A_{V\,k}(0)|^2} \left[\Delta f\right]_0^{\frac{\pi}{2} GBW} = \\ = \frac{T k_B \left(\gamma_n + \gamma_p\right)}{C_{L\,k} + C_{P\,k}} \left(1 + \frac{\left(G_{m\,k,2} + G_{m\,k,R} \right)}{G_{m\,k,1}} \right) \ (V^2) \tag{4}$$

The total input-referred output noise of a single stage is shown in (4), where γ_n and γ_p are the thermal noise coefficients of the NMOS and PMOS devices, respectively,

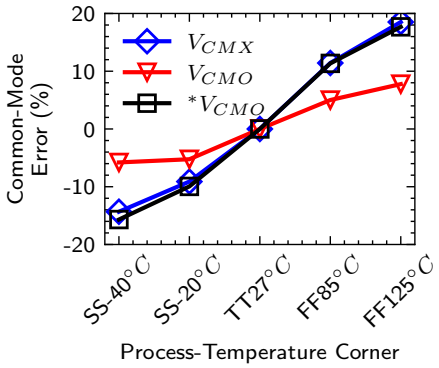

Fig. 3. Simulation behaviour of the CMFB and CMFF circuits. $*\mathrm{V_{CMO}}$ is the uncontrolled output CM voltage, $\mathrm{V_{CMO}}$ is the controlled output CM voltage and $\mathrm{V_{CMX}}$ is the resulting CM node controlling the output CM voltage.

T is the temperature in Kelvin, k_B is the Boltzmann constant. While the dynamic RA is not immune to jitter noise, it amplifies a sampled input residue voltage with a much lower frequency than the RA's clock phases (F_{CLK}). Hence, jitter noise is disregarded in this analysis. Flicker noise contributions ($v_{\mathrm{nf}}^2 \propto (WLF_{\mathrm{CLK}})^{-1}$) are also negligible due to the high F_{CLK} and wide gate area used for each main inverter device. Thus, the main noise contribution is due to sampled thermal noise multiplied by an excess noise factor (ENF) $\Gamma = \left(1 + \frac{(G_{m\,k,2} + G_{m\,k,R})}{G_{m\,k,1}}\right)$. Increasing $G_{m\,k,R}$ to boost the DC gain of each stage results in a higher ENF. Careful sizing of the HXCP's devices is thus required to avoid excessive distortion and noise contributions.

C. Design Methodology

The proposed RA presents a total open loop gain of $G(s) = A_{v,1}(s)\ A_{v,2}(s)$, featuring a pole at the first and second stage's output, s_{p1} and s_{p2} respectively. The GBW of the RA is determined using a dominant pole approximation $\mathrm{GBW} = |G(0)| f_{\mathrm{p2}}$, where f_{p2} denotes the second stage's pole frequency. In this scope, $\mathrm{GBW} \geq 10 f_{\mathrm{p2}}$ and $f_{\mathrm{p2}} \geq [1.5 - 2.5]\, F_{CLK}$ are the specifications used to establish the required settling-time at $\mathrm{F_S}/2$.

A minimum channel length of $\mathrm{L_{CH}} = 50$ nm is used for inverter devices, offering the best balance between intrinsic gain, gain accuracy, and speed under PVT conditions. NMOS and PMOS switches have a minimum channel length of $\mathrm{L_{CH}} = 30$ nm. Key design steps involve creating a minimum-size inverter $\mathrm{I_U}$ with dimensions that align its trip-point (V_{Trip}) with the common-mode voltage ($V_{CM} = \frac{V_{DD}+V_{SS}}{2}$). A scaling factor M_X can thus be used to represent a scaled-up version of $\mathrm{I_U}$, simplifying the design of the system.

To minimize Vn_i^2 and achieve a dominant pole approximation, the first stage's weights must be scaled higher than the second stage's to ensure $f_{\mathrm{p1}} \geq [1.5 - 2.0]\,\mathrm{GBW}$. Increasing the gain of the first stage in relation to the second reduces the power-dissipation and noise contribution of the RA. The DC gain is designed to achieve a $[-20\%; -15\%]$ gain error, further corrected by increasing $\mathrm{W_{ch}}$ of HXCP devices.

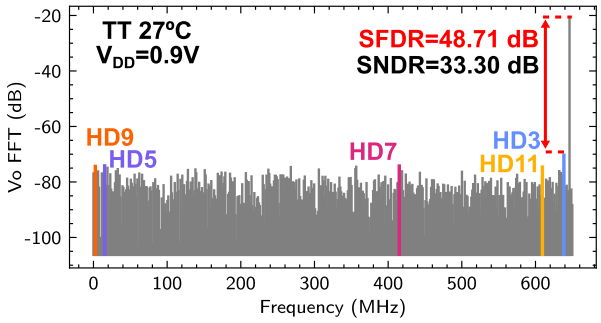

Fig. 4. 1024 points FFT simulation results, obtained for a nominal $\mathrm{V_{DD}} = 0.9$ V at $f_{in} = F_S/2$ Hz, for a typical process corner (TT) at the temperature of $\mathrm{T} = 27°\mathrm{C}$.

Two bootstrapped switches are added to the RA outputs to allow ADC pipelining operations and maintain linearity during its tracking and amplification-phase (phase $\Phi 2$) [13]. Precise design of S_P and S_N switches is crucial to limit the supply voltage deviation from the devices' sources to under 10 mV, preventing differential DC offset, common-mode ripple, and distortion.

IV. Simulation Results Discussion

A 1.3 GHz clock signal with a 50% duty cycle generated non-overlapping RA clock phases. DC gain and GER were determined from samples taken at the end of RA amplification (phase $\Phi 2$). A fast fourier transform (FFT) analysis of the differential output voltage provided SNDR, SFDR, and gain measurements within a simulation time window of 0.8 ns to 807.7 ns using 1024 frequency bins (Fig. 4). The proposed RA dissipates 1.67 mW at 1.3 GHz in typical conditions, yielding a power-to-speed ratio of 1.28 mW/GHz. This ratio is the lowest among RAs with DC gain above $\times 10$ in channels exceeding 1 GS/s, as shown in Table I.

A. PVT-variations simulation results

Schematic PVT simulations covered all extreme NMOS-PMOS process corners for three supply voltages (0.85V, 0.9V, 0.95V) and temperatures ranging from -40°C to 125°C. The gain error ratio (GER) was computed through the relative error in relation to the RA's nominal gain of $\times 16$. The RA achieved an SFDR of 48.71 dB, with stable SNDR above 28.85 dB, removing the ADC linearity bottleneck, enabling it to achieve an ENOB above 9.5 bits (Fig.4 and Fig.5). The DC gain only collapses at the lowest voltage supply and temperature, due to the collapse of the transconductances. However, it remains within $\pm 5\%$ limits for the FF, SS, and TT process corners across temperature for the nominal voltage supply. FS and SF corners showed higher and lower DC gain, respectively, but are still within a 2σ GER threshold. High NMOS charged-carriers mobility and a large $\mathrm{M_{N1}}$ to $\mathrm{M_{N2}}$ ratio for high open-loop DC gain severely impact the RA's settled DC gain. Lower DC gains with reduced transconductance ratios enhance process variation robustness.

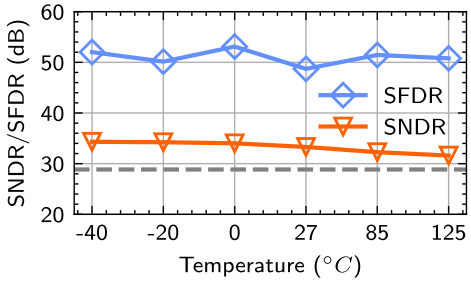

Fig. 5. Simulated spurious-free dynamic-range (SFDR) and signal-to-noise and distortion ratio (SNDR), obtained at $f_{in} = F_S/2$ Hz for a typical process-voltage-supply-temperature corner (TT, $\mathrm{V_{DD}} = 0.9$ V, $\mathrm{T} = 27$ °C).

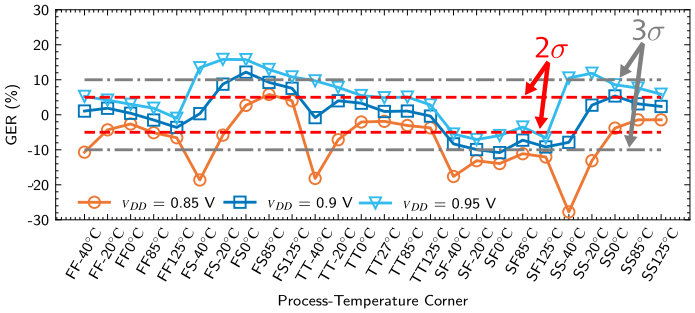

Fig. 6. Simulation results of the GER of the proposed RA across PVT corners at $f_{in} = F_S/2$ Hz.

V. Conclusions

This work introduces a $\times 16$ gain PVT-robust open-loop inverter-based Gm-ratio RA for high-speed pipelined ADCs. It's implemented in a 28 nm standard CMOS process with a 0.9 V power supply. It employs HXCP to minimize output conductance's impact on DC gain, achieving nominal gain with more relaxed die area and power-dissipation tradeoffs. Simulations across PVT corners ranging between the target design temperature of -20°C to 85°C show less than $\pm 5\%$ gain variation under typical conditions. The RA dissipates 1.67 mW at 1.3 GHz, yielding a power-speed ratio of 1.28 mW/GHz, setting a benchmark for RAs with a DC gain above $\times 10$.

TABLE I
State-of-the-art comparison.

	[6]*	[9]**	[10]**	**This Work***
Process (nm)	28	40	28	**28**
Supply Voltage (V)	0.9	1.2	1.0	**0.9**
Nominal Gain (V/V)	6	12	8	**16**
Temp. Range (°C)	[-40, 125]	[-40, 125]	[-40, 125]	**[-20, 85]**
GER-Temp. Ratio (%/°C)	0.018	0.121	0.010	**0.028**
Power-Speed Ratio (mW/GHz)	0.55	4.30	4.59	**1.28**
Calibrated	No	No***	No***	**No**

* Simulation results ** Measurement results *** Reference-trimming

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