Control of a DC Microgrid

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By

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Abstract

The growth of distributed Renewable Energy share in the total electricity production as wells as technological advancements in power electronics and increase of DC loads, point towards the development of the DC microgrid (DCMG) concept as a valid model for future energy systems especially for operations and locations where the existing grid cannot satisfy.

A DC microgrid consist of distributed sources, load and storage connected to a DC bus through converters. The two main issues in a DCMG operation is the power balance between supply and demand and its implementation through the interfacing converters, who in turn must be able to facilitate these operations. Many grid control strategies can be used but whatever the strategy may be, control is achieved through regulation of the DC bus voltage.

In this thesis a decentralized primary controller is selected, analyzed and modelled for power balance operations in an islanded 48V-LVDC microgrid, consisting of a renewable energy source, an electronic load and storage capability. Control is achieved through dc bus voltage monitoring and control operations on the interfacing converters, based on predefined voltage set points. As an interfacing converter, a cascaded half bridge buck and boost converter is used and controlled. Two different control modes are implemented: buck operation for the start-up of the grid and a special constant frequency modulation for soft switching and increased efficiency of the converter.

Furthermore, its use as multi-purpose converter, its low level control schemes and the co-operation with the high-grid level control are studied. Physical switching models are used to account for the real operation of the converter, when operating under higher level control, aiming at grid stability and optimal power flow.

Acknowledgements

This master thesis is the culmination of my studies in Sustainable Energy Technology at TU Delft. The object of this research was within my sphere of interests and I gladly undertook it.

However in the process I came across many adversities and obstacles both having to do with the research itself and some personal contingencies. Nevertheless, through this process there are people, whom I would like to thank from the bottom of my heart, as they have stood by me all the way. They have been very supporting and encouraging and never refused to spare their time in order to provide me with guidance and advice.

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But this thesis would never have been completed if it weren't for PhD. Laurens Mackay, my PhD. supervisor. He deserves my deepest gratitude for his immense assistance, his patience and the long hours he spent on discussing all little details and questions I had, without showing any indisposition.

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Lastly, I would like to thank my family for all the support during my studies and on the difficulties I coped.

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1 Introduction

1.1 Background

The gradual depletion of fossil fuels along with the increased awareness of the pollution of the environment, the climate change and the increase of energy demand globally, are pointing towards the growth of the renewable energy sources (RES) like Photovoltaic panels, wind turbines, biomass generators etc. leading to an increased share of the electricity production [1]–[4].

EU has set the goal of 20% of total energy consumption to come from RES for the year 2020 with this percentage to be increased to 27% in the year 2030 while in 2015, the EU-wide share of electricity from renewable sources (RES-E) amounted to 28.8 %. [5]. Meanwhile the same trend can be observed globally. In 2016 the net added total power capacity was provided at 62% by RES, increasing the percentage of renewable generation to the total capacity of 30% supplying approximately 24.5% of global electricity production [6]. Renewable energy would be more useful in the developing world, where the use of RES is promoted by new business models, where bottom-up customer demand is motivating hundreds of millions of households to generate their own modern energy, to provide services through off-grid units or community-scale mini-grids, instead of the old paradigm of energy access through grid expansion [6].

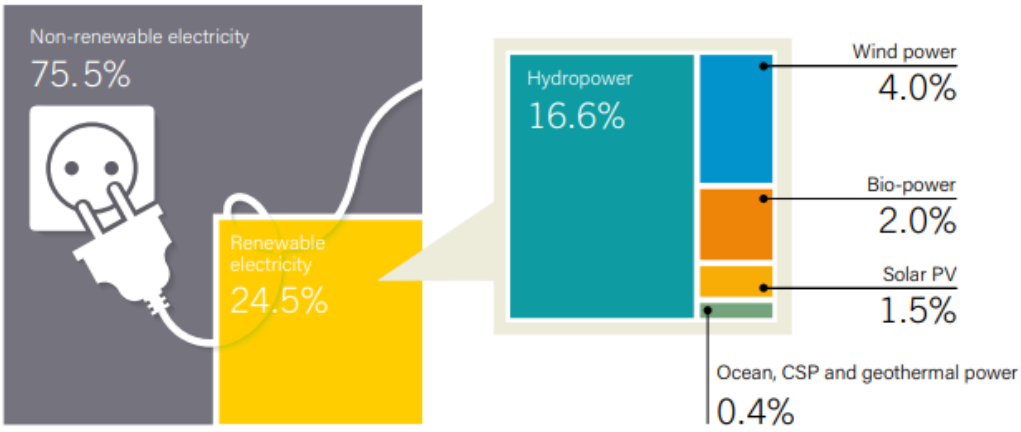


Figure 1.1:Estimated Renewable Energy Share of Global Electricity Production, End-2016 [6]

According to all the above, renewable energy generation is expected to continue to grow in size and market share. But renewable energy sources are distributed by nature [7] and so they are scattered through the power network producing power at a distribution voltage level [8]. For this reason their interconnection with existing power grid must be evaluated.

The conventional AC power network can be perceived as a one-way system with a unidirectional power flow from bulk power generators to substations through the transmission system and then to the distribution system and the loads [9]. These characteristics of the existing power grid make it unsuitable for incorporating distributed power generators, like renewable energy sources, since the variable power production can cause voltage and frequency fluctuation to the grid making it susceptible to voltage and frequency instability and protection, reliability and power quality issues that come along [3]. This is exaggerated also by the inability of the existing grid to accommodate demand side control due to the unidirectional power flow.

This may pose as disadvantage, since power balance between supply and demand must always be satisfied [1], [9].

To address these issues of the growth and efficient integration of the distributed generation with intermittent renewable energy sources, the increase in electrical demand, the need of cleaner, more reliable and diversified power production and the inabilities of the existing power grid, the microgrid concept is promoted as a solution [3], [10]. The micro-grid is an autonomous, low-voltage power system, which consists of distributed renewable energy sources, distributed storage devices like batteries, super capacitors and distributed-local loads and new technologies [8]–[10]. The microgrid mainly serves to balance the local demand and supply, but it can also operate in conjunction with the existing distribution grid or other microgrids to allow for power exchange when needed or it can be operated in an off-grid, islanded mode, when faults occur in the main grid or at all times. Then, it can control the demand locally with storage units and dedicated converters [9], [10]

Due to these benefits, the microgrid can relieve the additional stress and problems that the Distributed RES cause to conventional grids and become a more reliable, efficient means of distribution, as it takes into account the geographical location of sources, loads and storage units to optimize the power balance between supply and demand, reduce losses and increase power quality. Also it is economically beneficial for consumers with no or poor access to power in regard with a grid expansion of the existing grid [7].

Initially MG research and studies were carried out to fit to the traditional AC grid standardization and to cope with the ac-power associated problems like power quality. This was mainly due to the technological barriers and conditions of the time [3]. The most important component of the traditional AC grid is the transformer, which was the reason for the adaptation of the AC power as the norm in power systems, due to the ability of the transformer to change the voltage levels efficiently in order to move the centrally bulk produced power to the transmission voltage level and then to the distribution level voltage again. DC was mainly used in HVDC systems to connect different AC networks or for industrial purposes [11].

But many reasons today point towards the adaptation of the DCMG as the new norm in the LVDC power systems.

First of all the progress made in power electronics has enabled low cost, efficient DC/DC converters which due to their higher switching frequency (-100 KHz) in contrast to the AC counterparts (50-60Hz), leads to smaller components since frequency is inversely proportional to component sizing and therefore to reduced size, losses, harmonics and therefore costs [1]–[3]. Furthermore, microgrid components like distributed renewable energy sources, operate in DC (e.g. PV) or use a DC link in their power converter interface towards the grid to decouple rotational dynamics from the frequency of the AC grid as in the case of wind turbines [3]. This is also true for the distributed energy storage units (ESS) like batteries and Fuel Cells which also operate in DC [1]–[3], [10]. Finally, the increase in electronic loads like computers, smartphones etc. are naturally DC or use a built in rectification (ac to dc) stage to operate to the required dc voltage or require a dc link to the grid. Such loads are LED lighting, variable frequency machines like refrigerators, heaters consumer electronics, and variable-frequency drive machines (refrigerators, heaters, air conditioners, washing machines, etc.) [3], [11]–[13].All these will benefit from a direct dc connection as fewer conversion stages are needed.

As it can be concluded it makes sense to operate a microgrid in DC and connect every component to the common DC bus through DC converters creating a DCMG. A DCMG offers increased reliability due to smaller component sizes, high efficiency with appropriate voltage level due to fewer conversion steps and better control due to the lack of synchronization for

frequency and phase, reactive power management and fewer harmonics. These grids can operate in conjunction with the main grid through bidirectional AC-DC converters increasing the reliability of the upper main grid, as they can facilitate supply and demand power balance.

DCMG can be a smart solution for islanded operation of a power system where grid expansion is either impossible or non-profitable[5]. In an islanded mode the DCMG is not interconnected with the main grid and the power balance must be guaranteed locally. Beneficial to this direction could be the progress made in electrical vehicles, which have a built in capacity like batteries, which run in DC and can accommodate the role of storing the excess power, thus reducing the costs of acquiring a lot of extra storage capacity, which is of especially high importance for off grid power systems, in order to provide power in case of need and cope with the control issues as well as stability of the grid due to fluctuation in RES power production [1], [3], [9]–[11].

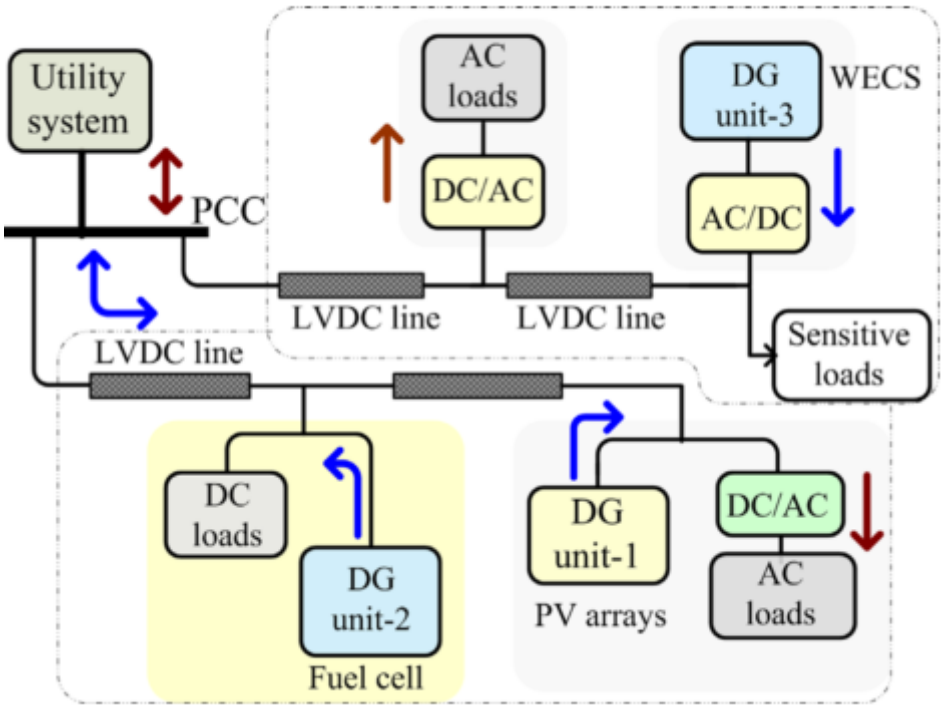


Figure 1.2: A DC microgrid with various Loads[11]

1.2 Motivation

The main purpose of control in any power system and of course in the DCMG is the power balance between supply and demand, ensuring constant voltage in the common bus. But the stochastic nature of renewable energy sources, along with the changing load may cause unbalances that can lead to voltage fluctuation in the DC bus [14], [15]. When connection of the DCMG to a strong grid is present, the voltage fluctuations can be suppressed with adequate power transfer from or to the grid as necessary to satisfy the demand [11].

But in islanding operation of the DCMG large voltage fluctuations may occur due to the absence of a strong power source, so the DC bus voltage regulation and thus the power balance must be done locally. A solution could be to install sufficient storage capacity on the supply side of the DCMG, to cope with the variations in power generation and consumption and thus reducing the voltage fluctuations. However, this option comes with high installation and maintenance

costs [3], [14]–[16]. But DCMG's can facilitate demand side control allowing for optimal power balance and quality in the DCMG [1], [11]. Demand side voltage-control is translated as switching off non critical loads or if allowed shading them when power supply is not enough [14], [15] and thus DC bus voltage is dropping below some critical value [1].

Different control strategies can be employed to address the issue of power balance and sharing between the devices in a DCMG. Nevertheless, whatever strategy may be used, control is achieved through voltage control of the DC bus. In turn, this is possible through the converters that interface the power sources, the storage units and the loads to the common DC bus of the DCMG. Therefore, the DC-DC converter is one of the most important components in the DCMG since it allows the control operation to take place, interconnects sources, storage units and loads with different voltage levels to the common bus and simultaneously isolates sensitive devices, like batteries, from voltage fluctuations, allowing for plug-and-play activity [3]. So each converter must be able to effectively regulate the local voltage, track the reference signals fast to meet the power demands, allow for control methods of load sharing.

From the discussion so far, it is obvious that DC microgrids are a promising concept as far as future energy systems are concerned. In this context, a study on one of the most important issues as the control can assist in better understanding and standardization. More specifically coordination between control strategies of the DCMG and converters- the basic modules of control implementation-, should be investigated. In the context of these considerations, in this thesis a 48V-islanded DCMG is going to be analyzed and controlled to cope with the power balance issue rising from the intermittent nature of RES, the changing loads and the storage limitations as well as the interactions with the low level control of the converters.

1.3 Research Objectives

This research aims to refine and solve power balance issues in a DC micro grid consisting of distributed RES in dynamic conditions taking into consideration the real operation and characteristics of converters, while cooperating with power flow control techniques. Also this thesis aims to further study the main component of a DC microgrid, the DC converter. For this reason, a bidirectional cascaded buck and boost converter will be studied, analyzed and simulated under various operations in order to evaluate its performance under dynamic conditions as well. Addressing these issues contributes forward to a further research on DC micro grids and their gradual integration into the bigger and more complex systems.

1.4 Research Questions

1. How can the control of the Synchronous Buck Converter can be realized and utilized in a DC microgrid?
2. How is the ZVS-modulation method implemented in the cascaded buck and boost converter and how this control performs under dynamic conditions?
3. How can the hybrid control technique for power balance be integrated with a low level control and implemented for real converters?

1.5 Methodology

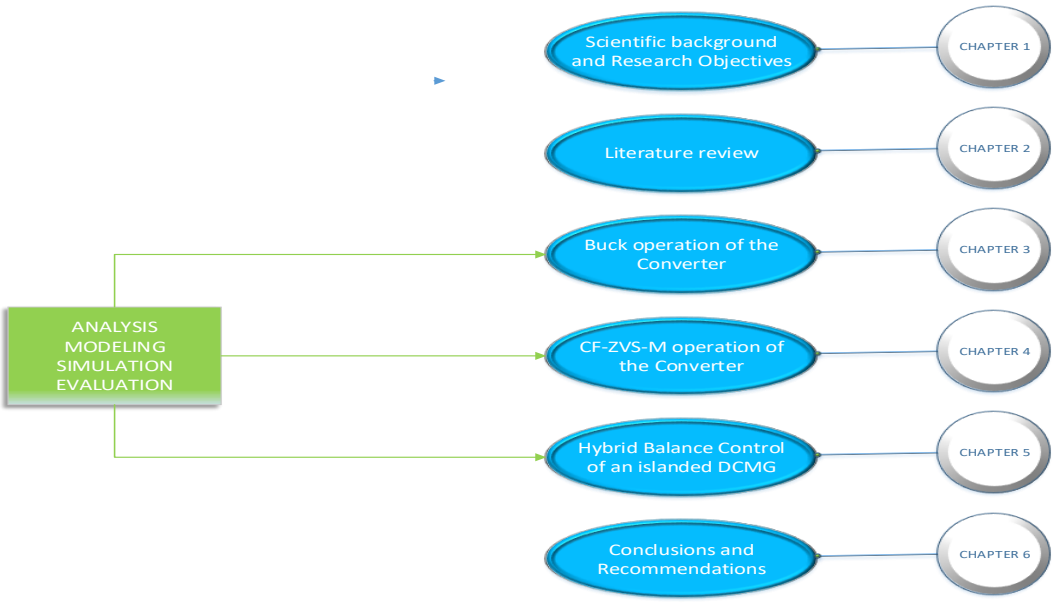


Figure 1.3: Research Methodology

This thesis will be organized in 6 Chapters as can be seen in fig 1.3:

In chapter 1, the background concerning the DC microgrids is set in addition to the questions to be answered by this thesis.

In chapter 2, previous work done and the basic context of the control schemes and converter topologies through which the research questions will be attempted to be addressed are presented. A thorough review of many different aspects concerning the DC microgrid in general are presented also to highlight key concepts and techniques that will be used in this thesis.

In chapter 3, the buck operation of the cascaded buck and boost converter is going to be studies. The theoretical background will be set, the converter will be modelled and low level controllers will be constructed. Two models will be created one based on the mathematical equations and one on the physical characteristics of the converter and their results will be evaluated and presented.

In chapter 4, the Constant Frequency ZVS modulation technique will be applied on the converter in study as presented in [17]. Again the theoretical approach of this control will be presented and two models both mathematical and switching are going to be constructed. Simulations will be carried to evaluate the behavior of this technique for efficiency upgrade.

In chapter 5, the converter with the low level control as implemented in chapter will be integrated in a 48-islanded DCMG comprising one PV module, one controlled load and one storage device. In this chapter power balance control will be implemented and its cooperation with the low level control will be evaluated and tested.

Finally in chapter 6, the conclusion of this thesis are going to be reviewed and recommendation for future work will be provided.

2 Literature Review

2.1 DC Microgrid Structure and Voltage Level

As we saw in the previous section, DC microgrid rises as a viable solution for integrating distributed generation and storage units, while satisfying the increasing demand of DC loads with higher efficiency, as now fewer conversion steps are needed both on the supply side and the load/demand side. A DCMG can be connected to other DCMG's forming a DC distribution system, but also to the main utility grid increasing its resilience and reliability, while accommodating structures for emerging energy market models. But also DCMG's can operate autonomously, through the inclusion of distributed storage units like batteries, super capacitors, flywheels etc. making them invaluable for remote locations, where grid expansion is either not cost efficient or even impossible. This specific characteristic along with the increased reliability in regard with to ac system is obvious in the telecommunication sector, where DC microgrids have been used to power up remote telecom stations.

Telecom sector has been rapidly growing in the past few years and is one of the most power demanding sectors while emitting high amounts of CO_2 [10]. For these reasons, it is one of the most known examples for DCMG with renewable energy systems. A typical layout of a 48V-DCMG for telecommunication stations can be seen below [3] .

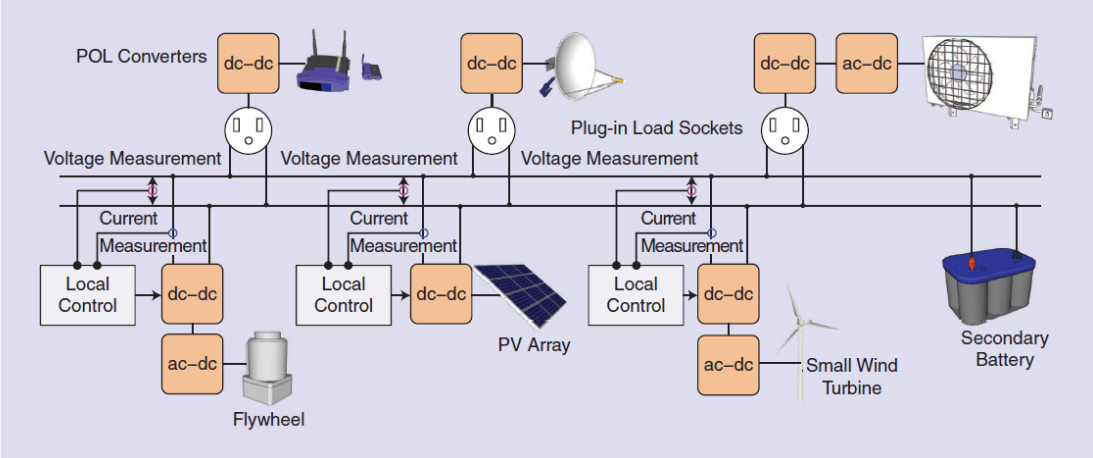


Figure 2.1: A 48V DC Microgrid for Telecommunication Station [3]

The voltage standard for these stations was set at 48V. All components are interfaced with appropriate converters to the common DC bus, except for batteries. Load converters are supplying the operating voltage for the loads by utilizing the battery voltage. Meanwhile, the sources operate, depending on the voltage level, either at Maximum Power Point Tracking (MMPT) mode or at voltage regulating mode, where part of the produced power is discarded to control the charging of the battery. Due to the success of this model's control scheme, plug-and-play capability and stability, it has been used as a prototype for telecommunication systems and expanded to other activities, since supporting devices for this voltage level and use were readily available [3], [18].

As we mentioned, use of DCMGs is promoted to fit other uses with higher power needs and different load profiles, such as residential and commercial buildings, electrical vehicles charging stations, data stations, ship networks, industrial applications etc. The selection of the DC bus voltage level is important for a number of reasons like costs, efficiency, reliability,

safety and compatibility of connected units. There is currently a lot of research underway on optimal voltage level for different applications. For example EPRI developed a voltage standard of 380V DC for data centers, together with the Lawrence Berkeley National Laboratory [2], [19], while EMerge Alliance proposed a 24V DC microgrid for interior spaces and uses like lighting, since most DC loads operate at 12-24V voltage range. So the optimal voltage level depends on the power needs and voltage operating ranges of the applications to be used in. In the table below typical values for various applications can be seen [10].

`	Applications	Voltage (DC)
1	USB and other small electronic equipments	≤ 5 V
2	Cars, desktop computer	12 V
3	LED lights, trucks, fans	24 V
4	Future PV installation	48 V
5	Telecom	-48 V
6	Power over Ethernet	50 V
7	Energy Strorage System (Batteries)	110 V/ 220 V
8	Data center	380 V
9	EV charging	400 V
10	Future residential and commercial building distribution	350- 450 V
11	Industry and transportation (metro, light rail transit)	600- 900 V
12	Traction system, marine and aircraft system	1000- 1500 V

Table 2.1: DC Power Application and Preferred Voltage level[10]

It has been shown by [18]–[20] that a 48V DC microgrid provides a good voltage level for residential applications, due to higher efficiency obtained and safety , even with direct contact with the bus, provided for these low power applications. Also, the availability of supporting devices for this voltage level, which was inherited by extensive use of this DCMG in the telecommunication sector makes it an appropriate choice for LVDC for residential and interior applications generally. Under this voltage level, battery operation is safer and more efficient than higher voltage battery stack. In addition low power and voltage PV modules are safer from sustaining arcing, have minimal shading effect issues and the converter efficiency is increased, since there is no great voltage difference, as we will see later in this section [20]. Lower voltage levels (i.e. 12V or 24V) are suffering from increased costs and big losses, because of the higher currents. Higher voltage levels like 380V provide increased efficiency but are better for high power essential loads (>1KW), requiring adequate safety measures.

The stand- alone DC microgrid of this thesis comprises a PV array, a battery stack and a load like LED lighting or other electronic loads typical for low power applications of residential or commercial buildings (e.g. LED lighting, variable speed drives of household appliances), so selecting the 48V voltage level is more appropriate due to high safety, backup battery requirements, converter selection and increased reliability with regard to different voltage levels [3]- [21].

2.2 Control in DC Microgrids

This high reliability of DC microgrids comes, as in the case of the telecommunication DCMG, from the connection of the battery to the DC bus. This was adequate so far, but in the face of the expansion of the DCMG to different applications, becomes a problem ,mainly due to the voltage variations of the battery and because the dc bus voltage cannot adequately and directly be controlled [3]. As we discussed in the introduction, control of the DC bus voltage facilitates the power balance control of the DCMG. Thus, connecting the battery to the common bus through a storage DC-DC converter, allows for increased controllability of the DC bus voltage and flexibility, through controllable charging and discharging operations. This modularity

though comes with stability problems, as now the capacitance (battery) that supported the bus is replaced by the smaller converter output/input capacitors. In addition to that, the dc bus voltage now needs to be controlled by other converters as well, when the battery converter is in charge /discharge operation mode [3],[11].

Generally, the control of DC microgrids should provide good load sharing capability between the sources, by adjusting the current drawn or fed by their respective interfacing converters and suppress voltage deviations, while allowing for a high degree of modularity. In case of grid connected DCMG's control should also allow for optimal power flow in the microgrid [8]. From the above, it can then be derived that control of DCMG's should be approached as a multi-level process, where each level is responsible for different control issues. This results in hierarchical control scheme, where three main control levels can be recognized [8], [11], [22]:

A. Primary control: responsible for regulating the local power, voltage and current parameters through the interface controllers and thus achieving the load sharing,
B. Secondary control: responsible for suppressing voltage deviations and performing microgrid wide range control action like power quality, synchronization and finally,
C. Tertiary control: responsible for power flow exchange with other grids, optimization and cost efficient operation. These levels can be seen in the figure below[22]:

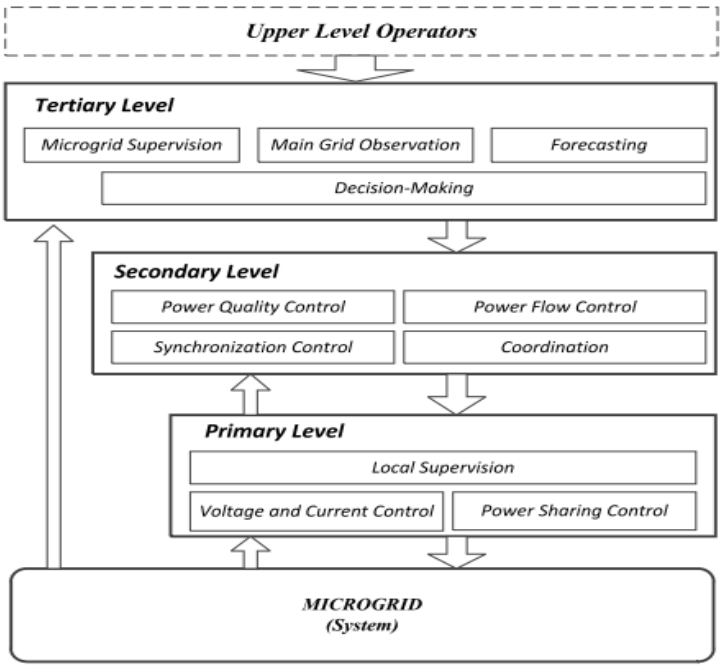


Figure 2.2: Hierarchical Control Structure in a DCMG[22]

Figure 2.2 also highlights another classification of control in DCMG, but this time based on whether communication infrastructure is used in the system and to what extent. With this in mind control structures can be classified into [3], [22]–[25]

a) Centralized: Usually a central controller gathers information of all DCMG components and accordingly manages the data and performs control operations by transmitting reference values and data to each component. This achieves efficient operation and control in the cost of decreased modularity, costs and reliability as is susceptible to communication faults.

b) Decentralized: Here no communication is needed since the control is based on local measurements and data to achieve load sharing and voltage regulation between converters. It offers high modularity but at the cost of poor accuracy.

c) Distributed: Here communication exists only between the controllers of different units and thus control is based both on information between distributed units and local measurements.

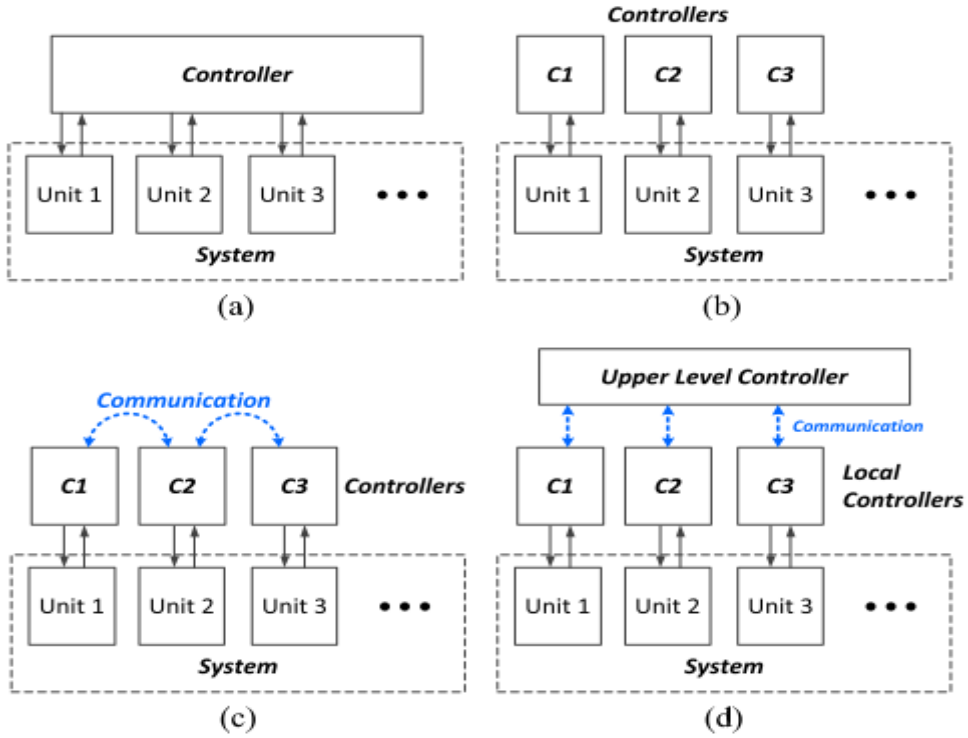


Figure 2.3: Basic Control Structures. (a) Centralized. (b) Decentralized. (c) Distributed. (d) Hierarchical

In Figure 2.3 we can see the different control structures described. Each technique comes with both advantages and disadvantages. A recent trend points towards utilizing the best elements each scheme has to offer leading to a hierarchical control (Figure 2.3d). In this scheme, secondary and tertiary control levels are usually implemented in a centralized fashion, where primary control for voltage regulation (and therefore power balance) and power sharing is implemented locally in a decentralized or distributed way through local controllers on each converter [22]. In [25], a hierarchical control of this manner is implemented, where a secondary centralized controller is adjusting the primary distributed controllers of each source converter interface to achieve low voltage regulation and simultaneously, thanks to the distributed primary control, to ensure safety in case of failure in the centralized controller.

2.2.1 Control in Islanded DC microgrids

In case of an islanded DCMG with few components, as in this thesis, higher level control is not essential. The main issue, as we discussed, in this operation is the power balance, which is

achieved by proper voltage regulation and current sharing among the parallel converters of the power sources, storage units and in special condition even loads, operations implemented by the primary/local control [22], [26].

Typically, depending on the way the voltage regulation and current sharing is achieved, two methods are recognized: active current sharing and droop [8], [22], [26], [27].

In active sharing methods, communication is needed to allow sufficient load sharing between the converters by utilizing a proper control and error sensing scheme. In [27], a review of different methods and sensing schemes is made. The most common is the master-slave control method, where one master converter is operating as a voltage source and assumes control of the DC bus voltage, while signaling current references to the other converters, rendering them current controlled sources [8], [22], [26]. This method, although achieving good voltage regulation and power sharing, suffers from the demerits of centralized control structure. To improve it circular chain control is suggested where a distributed control based on adjacent converter information may be used [8], [22], [27].

To get rid of the failures and high costs of communication, droop control may be more attractive for primary control operation in isolated DCMG's. Droop control is a method developed to enhance the low DC output resistance of power converters, which is the main reason for poor load sharing [27]. The main operating norm of droop control is to decrease the converter voltage output, when the current is increased. In this way, a resistive behavior is introduced to the system. Droop control can be implemented with a series resistor in every paralleled converter as presented in [27] but at the cost of high power losses. The most common droop technique is the virtual output resistance as described by:

$$V_{output} = V_{ref} - I_{output} \times R_{droop} \quad (2.1)$$

where V_{output}, V_{ref}, I_{output} and R_{droop} are the voltage output of the converter (reference to the voltage controller), the voltage at no load-reference value, the output current and the droop coefficient respectively. It can derived that the droop coefficient represents a virtual resistance, which enables voltage regulation and current sharing in the DCMG. In this way the converter of the microgrid operates as voltage source converter and can therefore assume control of the dc bus voltage. The operating principle can be seen in Figure 2.4:

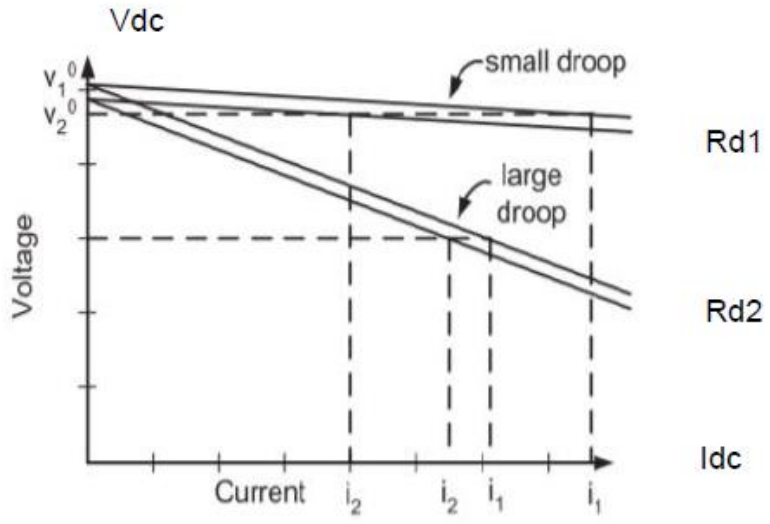


Figure 2.4: Small and Large Coefficient Droop Control

The droop coefficient represents the slope of the curve. Small droop coefficient is translated according to (2.1) in small deviation of the DC bus voltage, but at the cost of poor current sharing between converters. In contrast, large droop coefficient results in better load sharing, but in large voltage deviations also as seen in Figure 2.4. This is mainly due to error sensing in the voltage measurement and to load distribution structure, where usually unequal cable resistances superimpose over the droop coefficient leading to different droop equations. In [23] and [28], a distributed secondary control is employed to suppress the voltage deviation by shifting the droop voltage equation accordingly. A secondary control loop, in which a controller communicates the load information through low –bandwidth communication, to all the other converters and using average current sharing techniques, processes the required voltage shift for the voltage equations. Another solution can be the non-linear droop, where

$$V_{output} = V_{ref} - I_{output} * K(I_{outptut}) \quad (2.2)$$

The droop coefficient *K* varies, depending on load conditions (I_{output}) as in work done in [29]–[31], but communication is also needed. The adaptive droop technique based on SoC of each storage unit in the system falls under this category. In [32] the droop coefficient of each storage unit is adjusted in a way that the batteries with the highest SOC will provide more current, achieving a better load sharing.

In case, though, of a small system like our own, proper selection of droop coefficients should be sufficient to properly ensure power balance and adequate load sharing by prioritizing each unit accordingly.

Major focus should be put on the cooperation between the voltage droop method and the converter controllers. The droop control should provide the reference set-point for the dc bus voltage to the converter control in order to adjust the switching of the converter and thus produce the desired voltage. In [33], two droop control schemes are presented: the current sensing droop, which must be utilized in the voltage controller of the converter and the voltage sensing droop, suitable for the current controller of the converter. In the latter case, the outer voltage controller is omitted. In the figures below, the two different methods can be seen.

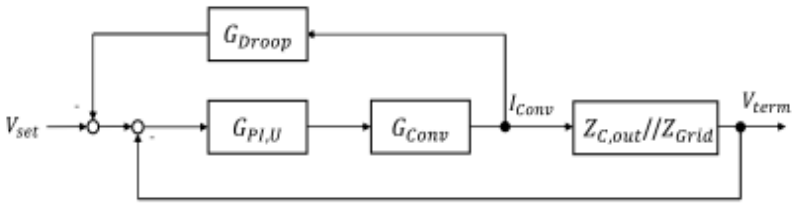


Figure 2.5: Voltage Droop Control with Current Feedback for a Converter[33]

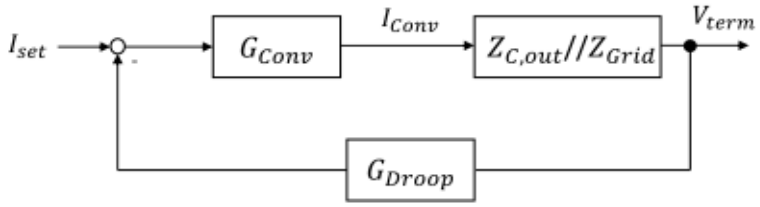


Figure 2.6: Voltage Droop Control with Voltage Feedback for a Converter [21]

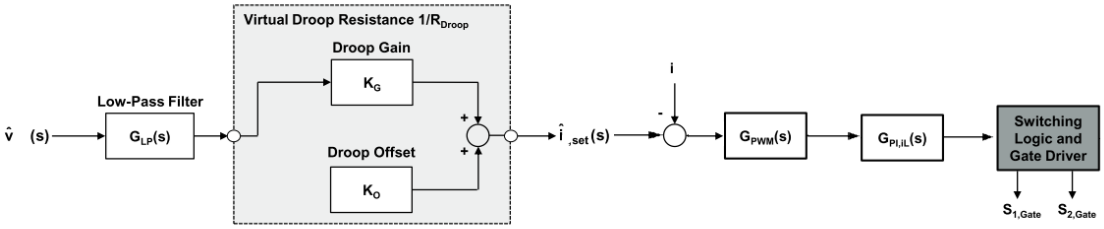
In [33], the voltage sensing method was confirmed to produce one less integrator in the output converter transfer function than the current sensing method, since the outer voltage control loop is absent and therefore the converter is behaving as a voltage dependent current source. This

can be seen by comparison of Figure 2.5-Figure 2.6, where the voltage controller is omitted in the case of voltage feedback. At the same time the output current of the converter (and so the loading of the grid) is directly controlled.

The current control loop has a higher frequency bandwidth than the voltage control loop leading to faster response of the converter to the load changes and prioritization of the sources according to droop [27], [33] . Crucial to the control is also the selection of the low pass filter of the voltage sensing as it affects the dynamics and the capacitor selection of the converter [34]. So the voltage droop controller is important to be well designed to ensure good cooperation with the converter current or voltage controller. Since it has an ohmic behavior, then also the line resistance must be taken into account [33], [34]. The droop control equation (2.1) can now be reshaped into:

$$I_{ref} = \frac{V_{ref}}{R_{droop}} - \frac{V_{output}}{R_{droop}} = K_g + K_o * V_{output} \quad (2.3)$$

Where K_g is an offset current and K_o has impedance characteristics. In [34] piecewise linear droop based on Look up tables can be employed to prevent over-voltages by segmenting the voltage into ranges. The control lop for the current controller can be seen in



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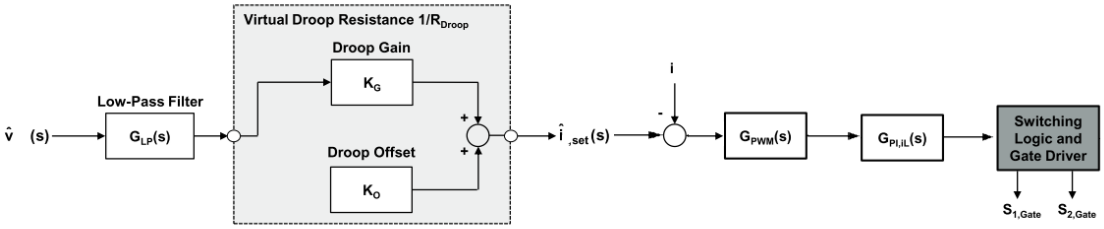


Figure 2.7: Droop Control with voltage sensing and Inner Current PI controller [34].

This is a hint for another control method for dc bus voltage regulation referred in the literature as DC bus signaling (DBS). From sources side of view, three operation modes are identified: utility dominating mode, storage dominating mode, and generation dominating mode depending on which device is controlling the DC bus voltage. This depends on the voltage measurement and some predefined voltage range levels set in each individual interfacing converter [22]. If one converter is controlling the DC bus voltage and therefore, the power balance, then the other units of the system may change their operation mode. For example PV can operate under MPPT algorithms to extract as much power as possible or be in voltage regulating mode. Loads can work under constant power, be turned off or if a possible droop depending on the voltage. Batteries commonly used for the voltage regulation may enter a fast charging mode [3], [24].

These modes can be realized by specifically predefined voltage levels on each interfacing converter. In [24], a hierarchical control is implemented, where in the primary control level , voltage thresholds are predefined based on which, operation modes for each source or storage device of the microgrid are selected to keep the voltage under specific limits. Also higher levels of control are implemented for optimization. In [35], a microgrid with renewable and conventional power sources, battery storage units and ac and dc loads, is controlled through voltage level predefined operation modes set on each interfacing converter according to the type component. Especially for battery units, SOC is also taken into account. The same principle is used in [14], [15] for the sources and storage units in an islanding DCMG, but here also controllable loads operate according to voltage levels in different modes. Here, also, these controllable loads can assume, through droop, the DC bus voltage regulation if needed.

Typically though when tightly regulated converters are used for loads they can be regarded as Constant Power Loads (CPL). Also the MPPT operation converters of renewable sources can be viewed as Constant Power Sources (CPS). This introduces the main stability issue for the power balance control of DCMG's, since they represent a negative impedance towards the rest of the DCMG converter input terminals, as when voltage increases, current decreases and vice versa [24], [36]–[38]. Negative Impendence can be seen as an oscillator which causes instabilities [38].Thus in this paper a stabilization loop as presented in (HBC) will be used and will thoroughly be examined in chapter 5.

2.3 Converters in a DC Microgrid

As we discussed above, a DCMG consists of renewable energy sources, storage units like batteries and super capacitors and controlled or uncontrolled loads, cables etc. all connected to a common DC bus. All these units, though, operate at different voltage levels and modes of operations and have different characteristics. In addition to that, control operations in the system are realized by power electronic converters, which interface the devices. Sometimes they are part of the device and the only way through which they can be controlled [39]. So DC converters are of paramount importance to the optimal operation and control of DCMG especially in islanded operation. Generally converters depend on the characteristics of the unit they connect to the grid but all of them need to exhibit low ripple in voltage and current input and output, high efficiency, low costs and allow external control signals [39].

2.3.1 PV module Converters

Renewable energy sources like PV need suitable converters to match the voltage range of the source, due to fluctuations in power production, to the DC bus voltage level and simultaneously allow both Maximum Power Point (MPP) operation and bus voltage regulation depending on the control strategy. Typically they don't need insulation. Low efficiency of PV under partial load due to shading can be countered by modular design, where each converter performs MPPT operation on each individual PV module and not on the whole PV installation, leading to higher efficiency redundancy and safety [18], [40], [41]. In literature typically boost converters are used with various differences [39], [42]. In [43], a thorough research on various topologies for power converters is made and a non-isolated two inductor boost topology is proposed for high voltage gain converters. In [41], different topologies like buck, boost, buck-boost and Cuk converters are compared with boost yielding the higher gains. In [44], also a boost converter based on the chopper circuit is used in the cascaded dc converter between series connected modules.

Another topology found in literature and of high importance to this thesis is the cascaded buck-boost half-bridge converter, as presented in Figure 2.8. This converter can operate either in

buck or boost mode and therefore is compatible with a wide range of voltage and furthermore, it enables MPP operation even when partial shading of the PV is present. In [40], this power stage is digitally controlled in buck, boost and a special bridge mode to achieve a high efficiency gain even in the transition between buck and boost modes and simultaneously allow for MMPT operation. The Digital Control is made of two loops with the inner being a fast current loop and the outer a slow MMPT algorithm producing the current reference for the inner control, which uses a two pole, two zero compensator (Figure 2.8).

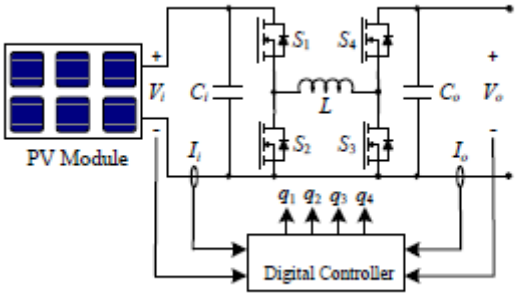


Figure 2.8:Cascaded Buck-Boost Converter with Controller[40]

In [45], the same topology is used for MPPT operation of a PV installation with many PV modules connected in series, but instead of bridge mode operation, near the nominal operation point of each module, a pass through mode with unity voltage ratio is implemented to achieve high efficiency.

The partial shading and the MMPT operation of each PV module in a PV installation is a widely addressed issue in literature and although of no direct interest in the scope of this thesis, it is useful to see the types of converters used in PV installations to get an insight into the problems that the converter needs to address in the control aspects of the DCMG itself.

2.3.2 Converters for Storage Devices in a DC microgrid

Next we are going to examine the converters for another major component of the DCMG, the storage units, which are the most important elements for control operations in the system. Converters need to take care of their specific characteristics, whether they are batteries, flywheels, super capacitors or fuel cells. If we also take into account the increasing penetration of Electrical Vehicles (EV), Hybrid-EV (HEV), or Fuel Cell Vehicles (FCV), which have storage elements like the above mentioned, interfacing them to the DC bus through converters, inserts concerns regarding the slow dynamics and response of these systems [3], [46]. Nevertheless, either as part of the systems storage capacity or of an EV, storage units' converters need to operate bidirectionally and since different batteries or other storage units may be used, whose voltage may overlap the DC bus voltage, the bidirectional converter needs also to operate both in buck and boost mode [17]. In addition to that, converters must be compact, of low cost, but also, as in the case of the PV converters, highly efficient over a wide range of voltage and loading(e.g. peak power during acceleration of EV, partial load in battery energy management actions) to satisfy reliability and other restrictions as EMI interference [17], [46].

In literature many suitable converter topologies are found. One major distinction is whether isolation is used or not in the converter. In [47], it is reported that isolated full bridge buck and full bridge boost converters are widely used, with the buck topology presenting high efficiency for low voltages, where boost presents higher efficiency in high voltage operations. But non-isolated dc-dc converters are more suitable for low voltage operations, where galvanic

insulation may not be needed. Furthermore, they are of lower cost, simpler structure and efficiency. In [46], boost converter is referred to as the most favorable due to high voltage gains.

In [48], different non-isolated converter topologies are compared. Some of the most predominant are presented in the figure below.

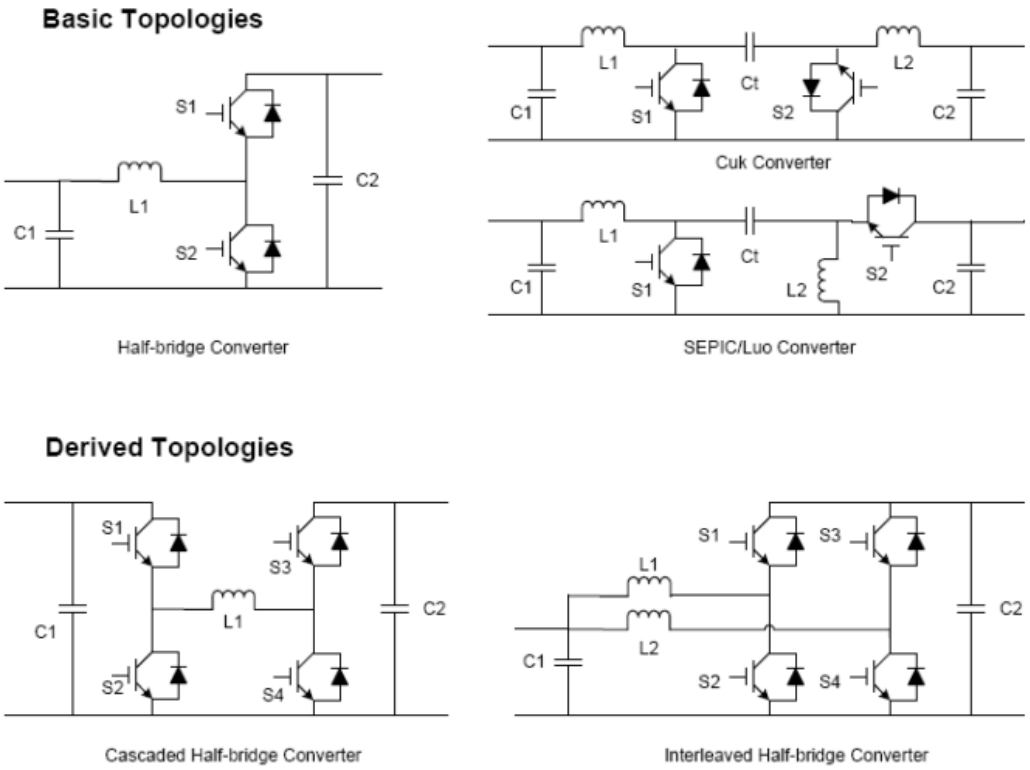


Figure 2.9: Common Non-Isolated Bidirectional DC converters[48]

According to this paper, the half bridge converter, that can work in buck or boost mode and the derived cascaded half bridge converter that can operate in both modes bidirectionally, present significantly higher efficiency and lower losses due to fewer number and size of components, in regard to the other topologies. As expected though, low efficiency is reported, when the charging of the battery is done under low battery voltage (boost mode), worsening with low power conversion, due to increased currents on the inductor and switches. In [17], [49], [50], also the cascaded buck and boost converter is chosen as the most predominant topology due to the wide range of capabilities. Nevertheless, low efficiency problems are identified when operated in PWM, mainly due to increased reverse recovery losses on the complementary switch's antiparallel body diode during turn-on of the switch.

2.3.3 Efficiency Optimization

Reverse recovery is the dominant loss component of switching losses in a converter. Reverse recovery losses of the diode happen due to the minority stored charge, during the forward bias of the diode (during the off state of the switch), which takes some time to remove when the diode turns off (switch turns-on). The turn-off time interval of the diode refers to the required time for this store charge to be removed and the diode to pass to the reverse biased mode [38]. During this interval, power is dissipated in the diode, which is a direct switching loss proportional to the switching frequency. On the other hand high switching frequency is required because size component is reversely-proportional to switching frequency [17], [38], [49]. So, there is a trade-off between efficiency and power density [49].

One first approach would be to replace the antiparallel diodes with silicon carbide diodes, which exhibit lower recovery losses at a wide voltage range [38], [42], [43], [46], but at the cost of increase EMI interference due to the large voltage change rate, increased costs and higher voltage drop. In [48], a variable frequency PWM operation is implemented where in low battery voltages , the switching frequency is lowered to reduce the switching losses and therefore increase efficiency in the low voltage range. However, this comes with the problem of increased EMI issues [17].

Another solution to cope with switching losses could be soft switching techniques more importantly zero-voltage switching (ZVS), zero-current switching (ZCS) and therefore low switching losses. More specifically, it is preferable to have zero voltage switch-on of MOSFETS and switch off of diodes. With these techniques, it is possible to lower the switching losses, while voltage change ratio is reduced to allow for lower EMI and simultaneously increase the switching frequency to allow for smaller components and costs [17], [46], [49].

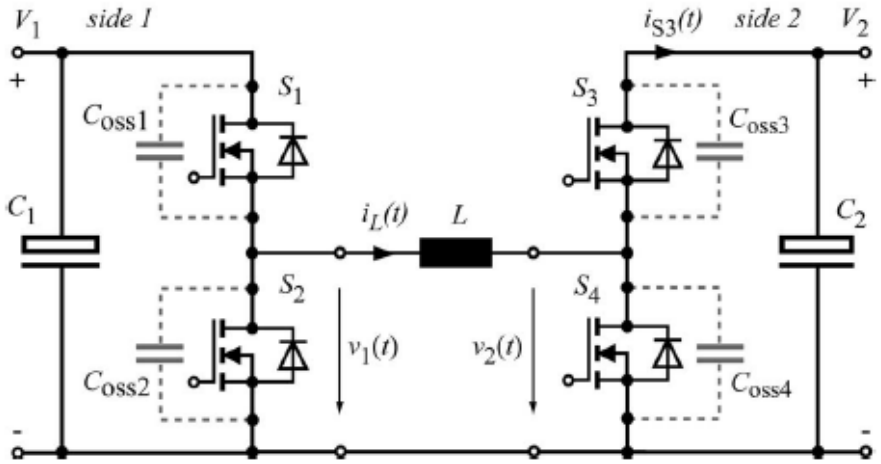


Figure 2.10: Cascaded Bidirectional buck-boost Converter for ZVS operation (CF-ZVS-M) with MOSFET parasitic capacitances which allow shaping of the inductor current for ZVS [17], [50]

Soft switching techniques can be divided into two types: PWM operated converters with auxiliary resonant circuits and resonant soft switching converters. Resonant converter utilize switch cells with resonant elements, instead of PWM for switching. If these resonant elements are placed suitably, soft-switching under ZVS or ZCS can be achieved [38]. Some bidirectional resonant converters in [17], [49] are presented, like the constant-frequency ZVS quasi-square-wave (CF-ZVS-QSC) converter, the single ended primary inductor converter (SEPIC) and the zero-voltage zero-current switching (ZVZCS). The main issues with these are increased induction losses due to larger component size, the large number of passive components and the variable frequency operation, which increases EMI. PWM with auxiliary circuits are also referred to [17], [49]. The main idea is that ZVS or ZCS is achieved by modulating the inductor current properly into resonant auxiliary circuits. But also these suffer from the need of additional active or passive components and PWM restrictions due to the resonant transition time requirements. We see that these well-established methods suffer from either low efficiency or increased costs or complex circuitry.

In [17], the author presents a software only soft switching method for constant frequency ZVS modulation without additional components or circuitry based on the cascaded buck and boost converter. Here instead of utilizing only one half bridge each time (buck or boost operation), all switches are turned on and off once per period in order to regulate the inductor current accordingly and to allow for ZVS turn-on of the switches. For this operation, a negative offset

current in the beginning of each operation is needed. It was shown that this approach exhibited high efficiency over both peak and partial power operation with no additional circuitry needed compared to other state of the art converters [17], [49].

Based on these remarks, along with the literature pointing towards the cascaded buck and boost converter not only for storage elements but also for PV modules, we deduct that this cascaded buck and boost converter with the soft switching method (CF-ZVS-M) presented in is capable of high efficiency and wide power and voltage applications both for PV (MPPT) and for storage devices and thus suitable for an autonomous DCMG. Also a converter prototype was already developed in the context of the Laboratory of DC Systems, Energy Conversion & Storage group of TU DELFT [51]. This converter was designed for input voltage range of 20-50V and output of 32-52V, which is suitable for the 48V DCMG and will be analyzed in this thesis. In order to sufficiently analyze and evaluate its operation in the control operations of the DCMG, first its operation in buck mode and under the special modulation strategy will be checked and controllers will be designed for each operation.

3 Buck Operation of the Converter

3.1 Introduction

As we discussed in the previous section, the cascaded buck-boost converter with the software soft switching approach, as presented in [17] and developed in [51], is going to be considered as the basic and general purpose converter of our DC microgrid. The converter is presented in the figure below:

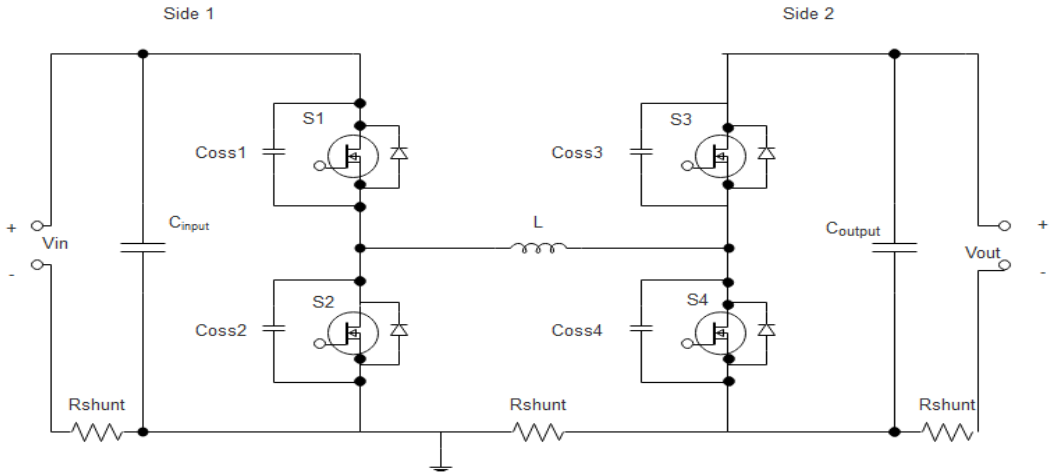


Figure 3.1: Cascaded Buck-Boost Converter

The converter voltage operational ranges were set at 0-50V for the input voltage and 32-52V for the output voltage of the converter. The maximum output current (full load) was set at 10A. According to these then, the power range of the converter is in the region of 0-520W. These limits concern the nominal operation of the converter under soft switching conditions. To fit these ranges and the constraints as set in [17], calculations and sensitivity analysis were carried out in [51] to define the component values. The components and their respective values can be seen in the table below:

Component	Name	Characteristics	Manufacturer
Inductor L1	IHTH-1125KZ-5A	2.2 μH, 0.77mΩ	VISHAY
Filter Capacitor (C1,C2)	2x60ER5470(1)40(2)	2X47μF each=94μF	KEMET
MOSFET(S1-S4)	IPB065N15N3G	150V,130A,6.5mΩ	Infineon
Capacitors(Coss1-Coss4)	ECWU1102JX5	1000pF	PANASONIC

Table 3.1:Converter Components

In contrast with [17], where the parasitic capacitance of the MOSFET is used, in [51] an additional capacitor in parallel with each MOSFET is connected, since MOSFET parasitic capacitances are not constant but depend on voltage and switching frequency. Analysis of this converter and its operation under the soft switching modulation of [17], will be analytically presented in the next chapter. It is though necessary to mention again, that this modulation is applicable only to the operating voltage ranges presented above. To start up the converter from

zero voltage up to these voltage ranges, the converter must be operated in buck mode in order to build up the output voltage.

Consequently, in this chapter the buck operation of the converter is going to be presented and analyzed. Since the converter was not designed to operate in buck mode, it is important to see its behavior and control issues in this mode. To achieve buck operation, the right half bridge switches of the converter Figure 3.1 are applied with constant control signals in their gate. More specifically S3 is constantly turned ON and S4 is turned OFF. In contrast to that, the left hand switches (S1 and S2) are actively controlled. The converter is then reduced to a buck converter as in Figure 3.2.

First, the operation and the equations of the Buck Converter will be presented. Two switching models were implemented, one based on the equations of the converter for faster simulations and one with the physical electrical components to confirm the results. For the controller design a small signal analysis was also carried out. Simulation results will also be presented and the overall performance evaluated.

It should be mentioned that the converter will be operated in Discontinuous Conduction Mode (DCM) in synchronous buck topology. This is mainly done for two reasons. The first has to do with the design specifications that require some off-time to take place for the parallel to the MOSFET capacitors to get discharged. Secondly, since there may be a wide load variation and the transmitted power is low, it is more beneficial to operate in DCM. Furthermore PWM-DCM in synchronous buck converter yields both good efficiency and transient behavior at light load conditions.

3.2 Buck Converter Operation

3.2.1 Theoretical Analysis

In Figure 3.2 the topology of a basic buck converter is presented. As discussed in the previous section, the cascaded converter can be reduced to this topology, if static signals are applied to the gates of the right half bridge (S3 and S4). Also it is should be noted that for the analysis of the converter and the extraction of the equations in DCM, we will initially assume that S2 is always turned off. In this case the current is conducted by antiparallel body diode of the S2 switch. The antiparallel body of S4 is reversed biased.

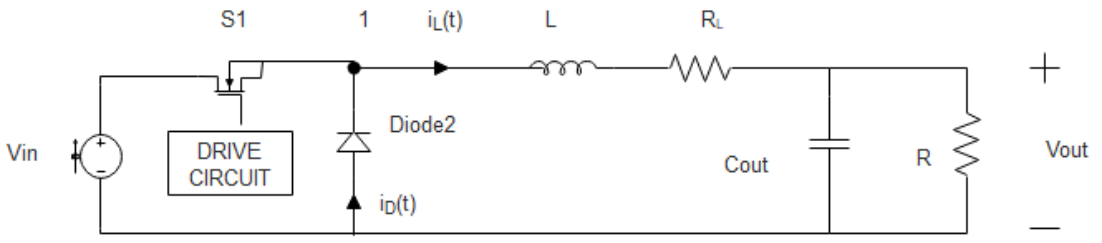


Figure 3.2: Buck Converter

In its basic form, the converter consists of a MOSFET switch (S1), which switches on and off according to the drive logic and creates a pulsating voltage waveform in the point denoted as 1 in Figure 3.2. This voltage is then attenuated by a L/C filter to supply with DC Voltage (V_{out}) the load (R). Since the filter has a cut off frequency a lot lower than the switching frequency, the output voltage can be seen as the averaged value of the pulsating voltage of the common coupling of the MOSFET S1, the diode and the inductor (point 1) [52]. Despite the filtering though, some amount of switching harmonics pass into the output signal. So the output voltage can be written as the sum between a DC component and a high frequency ripple component. It

should be noted that the analysis that follows derives from [38] and follows the denomination of the book. So, DC components will be denoted with upper case letters where ac ones with lower case. For the output voltage it holds that:

$$v_{out}(t) = V_{out}^{dc} - v_{out}^{ripple}(t) \tag{3.1}$$

In well-designed converters the ripple is small and thus can be neglected, leading to the small ripple approximation $v_{out}(t) \approx V_{out}$. Based on this remark, when S1 switch conducts, then diode 2 is in off mode and current increases with slope:

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_{in} - V_{out}}{L} \tag{3.2}$$

In contrast to that, when S1 is turned off the diode 2 conducts and the current is decreased with slope:

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = -\frac{V_{out}}{L} \tag{3.3}$$

Thus, the inductor current can also be considered as consisting of a DC component (I_L) and a ripple component (Δi_L):

$$i_L(t) = I_L + \Delta i_L \tag{3.4}$$

The above can be seen in the figures below. It should be noted that the losses in the circuitry due to non-ideal components have been disregarded.

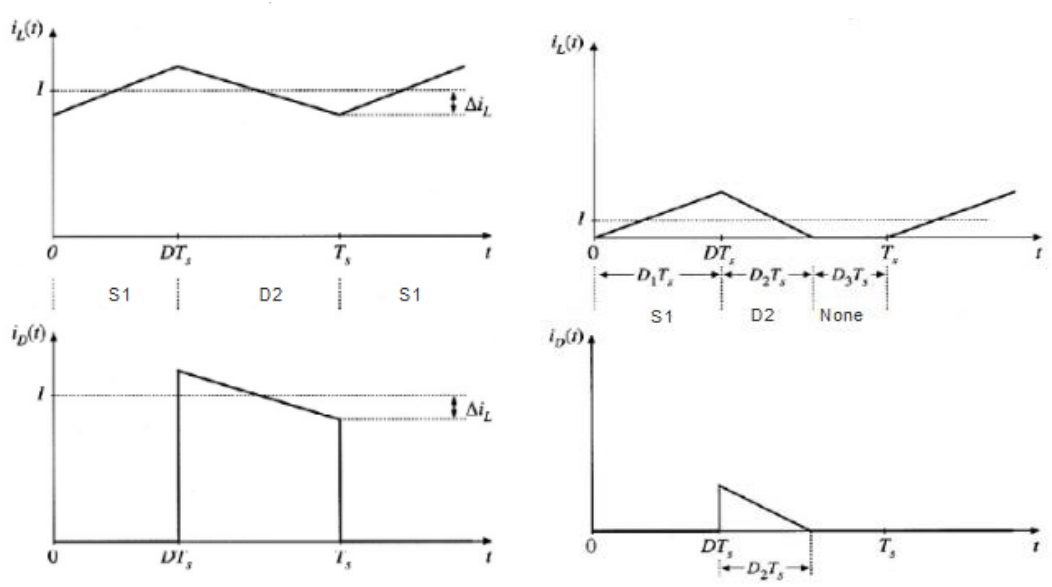


Figure 3.3: Inductor and Diode 2 Current Waveforms in a) Continuous Conduction Mode and b) Discontinuous Conduction Mode

In Figure 3.3a, the inductor current can be seen. In this operation, the ripple is smaller in regard to the DC component and current flows continuously in the circuit. In this case we are in the Continuous Conduction Mode and now (3.4) can be reduced to:

$$i_L(t) = I_L = I_{out} = \frac{V_{out}}{R}, \quad I_L \gg \Delta I_L \tag{3.5}$$

For the buck converter, based on the results of [38], the current ripple is given by:

$$\Delta i_L = \frac{V_{in} - V_{out}}{2L} D_1 T_s \tag{3.6}$$

where T_s is the switching period and D_1, the duty cycle of the switch S_1, which for the buck converter is given by:

$$D_1 = \frac{V_{out}}{V_{in}} \tag{3.7}$$

As we can see from (3.5)-(3.6), the DC component of the inductor current depends on the loading of the converter in contrast to the inductor ripple current, which depends only on converter characteristics and the applied input and output voltages. But if the load R increases, then the output current $I_{out} = V_{out}/R$ decreases, while the ripple current remains the same. It can be seen in figure 3.3b, that I_{out} may become so small that the ripple is now greater than the DC component of the current and now eq. 3.5 is not a valid assumption. From (3.3)-(3.4), we can see that now the inductor current may become negative when S1 is turned off. But since in this time interval the diode conducts, this is impossible since diode 2 is a unidirectional switch, not allowing for negative currents when it is conducting. Again from figure 3.3b, the diode and therefore the inductor current remain zero for a part of the switching period. This is the Discontinuous Conduction Mode and arises from light load conditions and unidirectional switches as explained in [38].

The boundary condition between DCM and CCM operations is given by [38], [53]:

$$\Delta i_L > I_L \tag{3.8}$$

Substituting (3.5)-(3.7), in (3.8), we get:

$$\frac{2L}{RT_s} < 1 - D \text{ or } R > \frac{2L}{(1-D)T_s} \leftrightarrow K < Kcrit(D) \text{ or } R > Rcrit(D) \tag{3.9}$$

Where $K = \frac{2L}{RT_s}$, $Kcrit(D) = 1 - D$, $Rcrit(D) = \frac{2L}{(1-D)T_s}$ and $R = \frac{V_{out}}{I_{out}}$.

R is the effective load resistance of the converter, valid for any type of load. Inequality (3.9) states that if the R value exceeds the critical load value, R_{crit} then the converter will operate in DCM. Also they tell us that DCM exists typically with lower duty cycles.

3.2.2 DCM Operation of the converter

In DCM operation, the conversion ratio becomes load dependent in contrast to CCM, where it depends only on the voltages as expressed in (3.7). To find out the conversion ratio in DCM, we have to look into the converter over one switching period. Again the analysis follows the steps of [38].

When the drive circuit of the buck converter of fig. 3.2, applies a voltage over the gate of switch S1, it turns on and the MOSFET conducts. The MOSFET has a low drain to source resistance during conduction represented by Ron. The inductor voltage drop is also represented in the figure. Diode 2 is reversed biased, because a negative voltage is applied on it ($v_1 = v_{in} - i_L \times (R_L + R_{on})$ and thus is not conducting. Then the buck converter reduces to the circuit of fig 4.

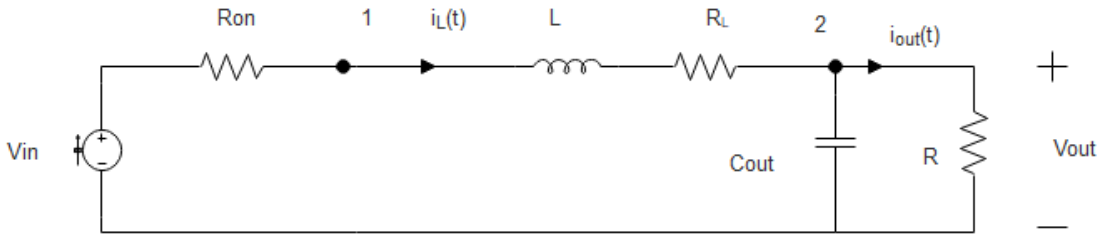


Figure 3.4: Buck converter when S1 conducts

The inductor voltage and capacitor current during this subinterval, when S1 conducts ($0 \leq t \leq D_1T_s$) are given by:

$$\begin{aligned} v_L(t) &= V_{in} - v_{out}(t) - i_L(t)(R_{ON} + R_L) \\ &\approx V_{in} - V_{out} - i_L(t)(R_{ON} + R_L) \end{aligned} \tag{3.10}$$

$$i_C(t) = i_L(t) - \frac{v_{out}(t)}{R} = i_L(t) - \frac{V_{out}}{R} \tag{3.11}$$

In the above circuit the small ripple approximation for the output voltage of (3.1) was used. It should also be noted that the same cannot hold for the current, as in DCM eq. (3.8) is true.

When the drive circuit signals S1 to switch off, the inductor current shifts from S1 to the antiparallel Diode of MOSFET 2 (Figure 3.1), since it cannot change its value instantaneously [52]. The voltage in the left of the inductor becomes negative since the inductor voltage becomes negative and the diode thus becomes forward biased (positive voltage over diode 2) and conducts. v_1 now is $v_1 = -V_d - i_L \times R_L$,where V_d is the forward voltage drop of the diode. V_2 has the value of the output voltage. The inductor current now decreases under the negative inductor voltage with slope given in eq. 3 (if losses are neglected) until it reaches zero as in fig. Figure 3.3b (D_2T_s). The circuit in this interval ($D_1T_s \leq t \leq (D_1+D_2)T_s$) is seen in the figure below:

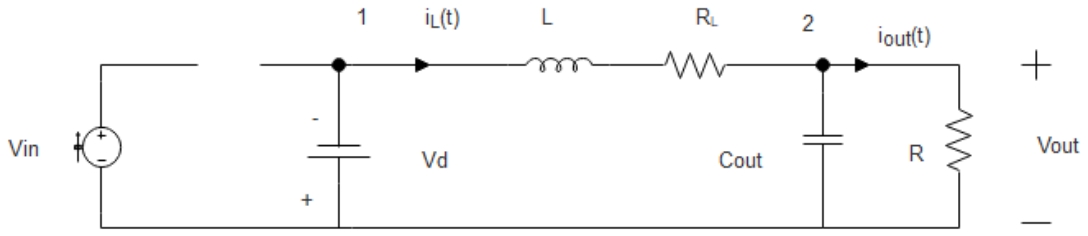


Figure 3.5: Buck Converter when Diode 2 conducts

It should be noted that the antiparallel diode of S4 in Figure 3.1 doesn't conduct since the voltage across it is negative ($0 - v_2 = -v_{out}$) and thus is reversed biased. The inductor voltage and capacitor current equations are now given by:

$$v_L(t) = -V_d - v_{out}(t) - i_L(t)R_L = -V_d - V_{out} - i_L(t)R_L \tag{3.12}$$

$$i_C(t) = i_L(t) - \frac{v_{out}(t)}{R} = i_L(t) - \frac{V_{out}}{R} \tag{3.13}$$

Finally, due to the large current ripple, there is also a subinterval $(D_1+D_2)T_s \leq t \leq T_s$, where no current flows.

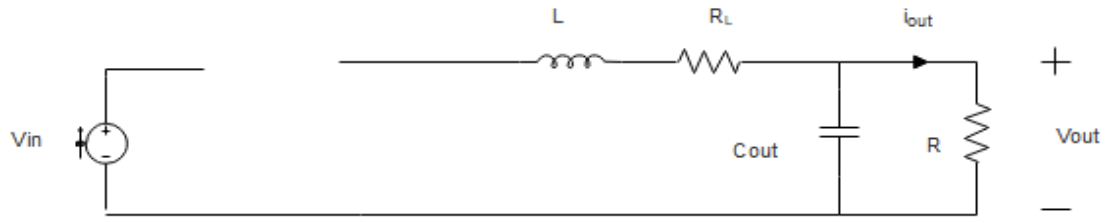


Figure 3.6: Buck Converter when no device conducts

It can easily be derived that:

$$v_L(t) = 0 \tag{3.14}$$

$$i_C(t) = -\frac{v_{out}(t)}{R} = -\frac{V_{out}}{R} \tag{3.15}$$

Now, we can use as in [38], the principles of inductor voltage-second balance and capacitor charge balance. These principles declare that the DC component of the voltage applied to an inductor and current applied to a capacitor respectively, must be zero over one switching period. Mathematically these principles can be expressed as:

$$\frac{1}{Ts}\int_0^{Ts} v_L(t)dt = 0 \tag{3.16}$$

$$\frac{1}{Ts}\int_0^{Ts} i_c(t)dt = 0 \tag{3.17}$$

Equations (3.16)-(3.17) can be solved now over one switching period. The loss elements of the converter though insert into the equations the ac component of $i_L(t)$, since in DCM the small ripple approximation cannot be used in contrast with CCM, where more analytical solution could be drawn. But typically, these elements are very small and thus can be safely ignored. Neglecting losses and substituting (3.10), (3.12) and (3.14) in (3.16) and (3.11), (3.13) and (3.15) in (3.17) we get:

$$D_1T_s(V_{in} - V_{out}) + D_2T_s(-V_{out}) + D_3T_s(0) = 0 \tag{3.18}$$

$$\frac{1}{Ts}\int_0^{Ts} i_L(t)dt = I_L^{dc} = \frac{V_{out}}{R} \tag{3.19}$$

where D_3 is the fraction of the switching period where no device conducts. It can easily be derived that $D_1 + D_2 + D_3$=1. Equation (3.18) yields:

$$\frac{V_{out}}{V_{in}} = \frac{D_1}{D_1+D_2} \tag{3.20}$$

In this, D_1 is considered known since it is the control variable from the PWM gate drive circuit. Equation (3.19) informs us that the DC capacitor current is zero and thus the output current is supplied by the DC component of the inductor current. The integral part is the area below the inductor current waveform in one switching period as can be seen in Figure 3.3b. This area is given by:

$$\int_0^{Ts} i_L(t)dt = \frac{1}{2} i_L(D_1 T_{s)} \, (D_1 + D_2)T_s \tag{3.21}$$

The inductor current at $D_1 T_s$, which is the peak current, can be found by integrating (3.3):

$$i_L(D_1 T_{s)} = \frac{V_{in} - V_{out}}{L} D_1 T_s \tag{3.22}$$

Combining (3.20), (3.21) and (3.22) the conversion ratio for DCM is given by:

$$M = \frac{V_{out}}{V_{in}} = \frac{2}{1 + \sqrt{1 + \frac{4K}{D_1^2}}} = \frac{2}{1 + \sqrt{1 + \frac{4R_e}{R}}} \tag{3.23}$$

Where:

$$K = \frac{2L}{RT_s} \, , Re = \frac{2L}{D_1^2 T_s} \tag{3.24}$$

3.2.3 Synchronous Buck Operation in DCM

In the analysis done in the previous section, a static PWM signal was set to have S2 switch always turned-off. In this case as was discussed, the antiparallel body diode of the S2 MOSFET, conducts the current. Since diode is a unidirectional component, DCM operation can be observed in light load conditions.

But instead of using the antiparallel body diode, we can actively control switch S2 to decrease losses associated with diode conduction. The power dissipated in a MOSFET switch and a diode in Continuous Conduction mode are given by [54]:

$$P_{diode} = V_d \times I_{out} \times (1 - M) \tag{3.25}$$

$$P_{FET} = R_{on} \times I_{out}^2 \times (1 - M) \tag{3.26}$$

Typically power loss in MOSFETs is lower than in the diodes. For our converter, based on the Datasheet of the MOSFET, for a load current of 6.4A and a conversion ratio of M=32/48V=0.67, the above equations yield $P_{diode} = 1.9W$ where $P_{FET} = 0.09W$. So, from efficiency point of view S2 should be actively controlled to conduct the current, leading to a synchronous buck converter operation. Similar arguments can be extracted for the DCM operation. According to [55], the conduction losses of the S2 MOSFET and for the diode can be given by :

$$P_{FET} = R_{on} \times \frac{\Delta I_L^2}{3} \times \frac{T_{off}}{T_s} \tag{3.27}$$

$$P_{diode} = V_d \times \frac{\Delta I_L}{\sqrt{3}} \times \frac{T_{off}}{T_s} \tag{3.28}$$

where T_{off} is the fraction of time either the diode or the switch conducts. By dividing both equations we get:

$$P_{FET} = P_{diode} \times \frac{\sqrt{3}R_{on}}{3V_d} \times \Delta I_L \quad (3.29)$$

As in the case of the previous example of M=32/48V=0.67, now $P_{FET} \approx 0.05 Pdiode$. In other words, by utilizing a second actively control FET with lower forward voltage drop than that of the diode, losses are reduced.

The synchronous buck converter though consists of two bidirectional switches. This means that the inductor current may go to negative values at light load conditions, exhibiting a CCM behavior. This in an unwanted situation as power is dissipated when reverse current is flowing as it is conducted by the antiparallel diode of S1 resulting in lower efficiency. A solution to this can be to operate synchronous buck in DCM through actively controlling the PWM switching of S2 by an independent control signal. This control signal is no other than the duty cycle D_2 or the fraction of the switching time where the diode of S2 was conducting in the analysis of the previous section.

From (3.20) and (3.23) it can be deducted that:

$$D_2 = \frac{MK}{D_1} = \frac{V_{out}}{V_{in}} \frac{K}{D_1} \quad (3.30)$$

Equation (3.30) states that D_2 is derived by properly manipulating the control signal D_1 of the PWM controller to S1. The other variables of (3.30) all depend on the loading and the voltages applied. By applying this PWM control signal to S2, it turns on for exactly the time needed for the current to reach zero, thus increasing the efficiency of the converter.

It should be mentioned that special care by the controller must be taken to prevent simultaneous conduction of both S1 and S2 MOSFET's, since in this case a source to ground short circuit can occur. For this reason a dead-time between the switching of S1 and S2 must be implemented. Current could still flow through the antiparallel body diode of S2 for the delay on and off time of the diode but the power dissipation is negligible since it depends on these very small times.

In the case of the non-synchronous buck converter another major loss component is the reverse recovery loss of the diode. When S1 turns on, for a small amount of time the antiparallel diode of S2 remains forward biased, due to minority charge stored in its pn junction, until it is removed either by the negative current flowing or through recombination. The time it takes for the diode to turn off, the reverse recovery loss, is a major loss component [38].

In synchronous buck, when S1 turns-off, the antiparallel diode of S2 conducts for some time which is the dead-time and the turn-on delay of S2. Then S2 turns on and the antiparallel diode turns off. If though $D_1 \rightarrow 1$, that means $D_2 \rightarrow 0$ and S2 may not turn on at all and thus the diode of S2 may still conduct, when S1 MOSFET is turned on again, leading to the mechanism of reverse recovery losses as explained above. So if the turn on delay is neglected ($\sim 25ns$), the proper selection of the dead-time that would both ensure that no cross conduction is taking place and low power dissipation is significant [52]. The same doesn't hold for S1 turn on since the current then is zero. According to [55] , in DCM the losses due to the diode conduction during the dead-time can be described by:

$$P_{diode} = V_d \times \Delta I_L \times \frac{T_{deadtime}}{T_s} \quad (3.31)$$

In [55] , formulas for the transitional switching time are also provided but they cannot be adjusted to our current setup as they depend on time delays of the MOSFETs.

3.3 Dynamic Analysis

Typically dc converters need to supply a constant voltage output in spite of load and input voltages variations or fluctuations. For this reason a control loop with feedback is required. A typical control loop for a converter can be seen in the figure below.

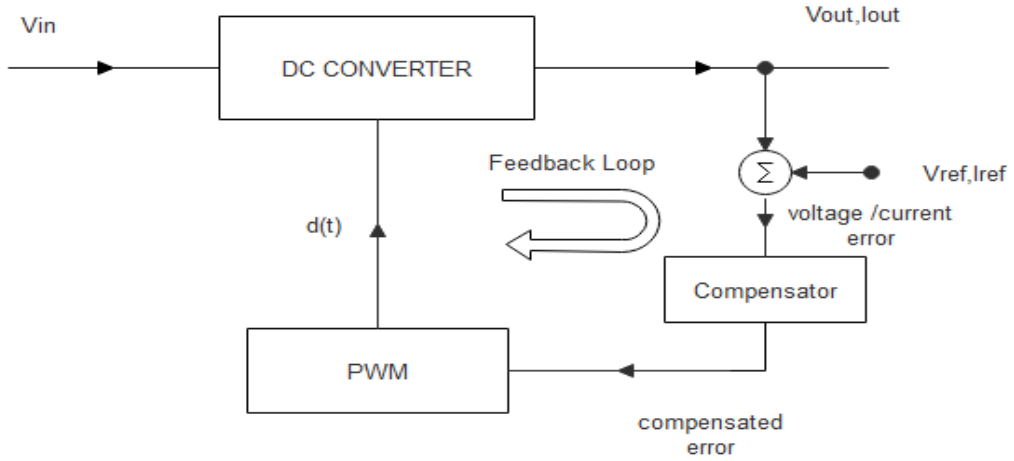


Figure 3.7: Converter Control Loop

In the figure above, we see that two inputs are identified towards the converter i) the control input $d(t)$, which controls the switching actions and thus the output voltage and ii) the input voltage V_{in}. This control system must regulate the output voltage or current sufficiently close to the reference values and reject disturbances on the input signals, while being stable and adequately fast. To achieve this the dynamic model of the converter must be constructed.

Usually due to switching, high frequency components are added to the signals like voltage or current of the converter, through the control input $d(t)$. But what is needed is the low frequency ac response of the system and therefore averaging over the switching period removes the high frequency components. What is left is a set of averaged non-linear equations due to the non-linear elements of a dc converter, like MOSFETs and diodes. But linear systems are easy to analyze, therefore, linearization around an operating point is done. To demonstrate this clearly, in figure 3.8, the boost converter's conversion ratio to duty cycle to is sketched.

If a conversion ratio M around 3 is chosen, this correlates to a duty cycle of about 0.7. For small variations of $d(t)$ around 7, the converter can be approached by the linear curve tangent to the operating point, meaning the effect of the variations in the conversion ratio can be approached by the slope of this curve linearly. In the same manner, the linearized small signal model of the converter around an operating point can accurately predict the dynamic behavior of the nonlinear converter to disturbances (perturbation).

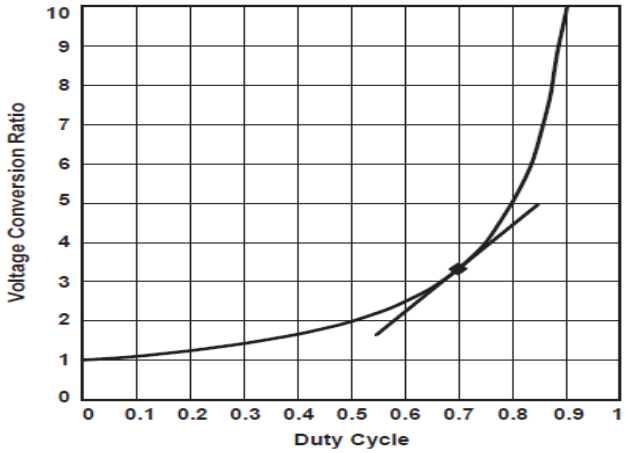


Figure 3.8: Boost Converter Voltage Conversion Ratio to duty cycle(control input) [52].

Since the buck converter is operated in DCM, the DCM small signal will be presented. The analysis is based on the work done on [38] and here only the basic concepts and the results will be presented. It should be noted that CCM models are completely different than the DCM.

3.3.1 DCM Small Signal Model of the Buck Converter

As discussed in [38], the switch network of the buck converter (switches S1 and diode of S2) is replaced by an averaged PWM model, based on the equations of voltage and current in the input and output of the switch network. Thus, the averaged non-linear model of the buck converter is constructed as seen in figure 3.9.

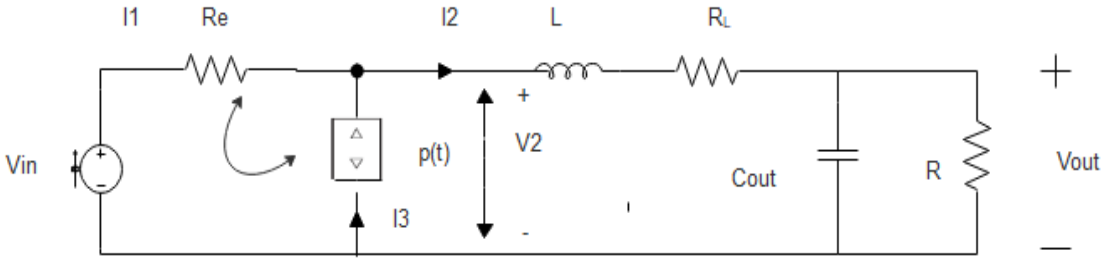


Figure 3.9: The averaged large signal model of the Buck Converter in DCM.

We can see that the input port of the converter (switch S1) has been replaced by a resistance Re, while the output port (diode of S2) has been replaced by a dependent power source equivalent to the power dissipated in Re. This is due to the fact that the switch network averaged equations of the input port exhibit a resistive behavior while the output port averaged network equations exhibit power source characteristics equal to the power dissipated in Re. The same model of the loss-free resistor can be used for any two-port switch network where the waveforms of the input port of the switch network are independent of the external circuit characteristics connected to the output port. So the same analysis is valid for S2 I place of the diode. All signals are averaged over one switching period and denoted with capital letters. The averaged values of inductor voltage and capacitor current over one switching period are zero as expressed by (3.16) and (3.17). The steady state value of Re is given by the above if large signal averaged model if L is short-circuited and C open circuited around a quiescent point expressed by (V_{in}, V_{out}, D_1):

$$R_e = \frac{2L}{D_1^2 T_s} \tag{3.32}$$

So, for the power source it holds:

$$p(t) = I_3 \times V_2 = \frac{(V_1 - V_2)^2}{R_e} \tag{3.33}$$

From [38], $V_1 = V_{in}$ and for the current we have from Kirchhoff's law:

$$I_3 = I_2 - I_1 = \frac{V_{out}}{R} - \frac{V_{in} - V_2}{R_e} \tag{3.34}$$

Using the voltage divider we get (V_L and I_C are zero, since we are in steady state-DC):

$$V_{out} = V_2 \frac{R}{R + R_L} \tag{3.35}$$

Combining (3.32)-(3.35), the voltage conversion ratio is found:

$$M = \frac{V_{out}}{V_{in}} = \frac{R}{R + R_L} \times \frac{2}{1 + \sqrt{1 + \frac{4K}{D_1^2} \times \frac{R}{R + R_L}}} = \frac{R}{R + R_L} \times \frac{2}{1 + \sqrt{1 + \frac{4R_e}{R + R_L}}} \tag{3.36}$$

So we reach the same result as the DCM steady state analysis (eq. 3.24) of the previous section if $R_L \to 0$. In order to extract the small signal model the switch network averaged equations ($\langle v_1(t)\rangle_{T_s}, \langle v_2(t)\rangle_{T_s}, \langle i_1(t)\rangle_{T_s}, \langle i_2(t)\rangle_{T_s}$) are perturbed and linearized around a quiescent point, defined above (V_{in}, V_{out}, D_1), as performed in [38]. For simplicity the resulting model is given in the next figure:

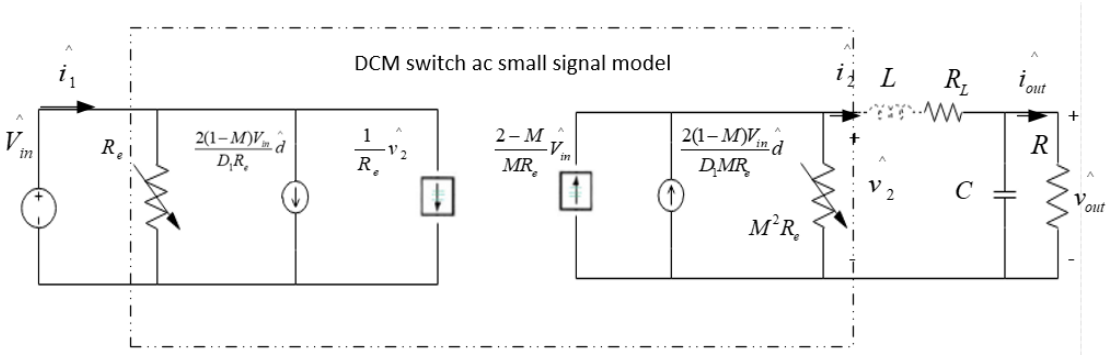


Figure 3.10: Buck Converter DCM Small Signal Model

This model accurately predicts the low frequency dynamics of the Buck converter in DCM. It should be noted that high frequency dynamics of the inductor cannot adequately be predicted through this model but nevertheless, the inductor induced pole is near the switching frequency while the capacitor induced pole is responsible for the low frequency dynamic behavior. For this reason the inductor is short circuited. In this model also the inductor ohmic losses can be included. It should be noted here that the notation $\hat{x}$, refers to ac small signal models. Without the losses, the converter output can be replaced by:

$$Z_{conv} = \begin{cases} R||\left(\frac{1}{sC}\right) = \frac{R}{1+sCR}, & R_L = 0 \\ (R|\left|\frac{1}{sC}\right) + R_L = \frac{R}{1+sCR} + R_L = \frac{(R+R_L)+sCRR_L}{1+sCR}, & R_L \neq 0 \end{cases} \quad (3.37)$$

Here $\hat{v}_2 = \hat{v}_{out}$. So we see that the ohmic losses of the inductor introduce a zero on the converter impedance, though due to the low value of R_L, this is pushed to very high frequencies exceeding the switching frequency. In this case $\hat{v}_2 = \hat{v}_{out} \times (1 + \frac{R_L}{R} + sCR_L)$.

As we saw in figure 3.7, the converter has two inputs $d(t)$ and v_{in}. So the two transfer functions that describe the low frequency dynamics are a) the control to output (G_{vd}) and line to output (G_{vv}) transfer functions. The control to output transfer function can be found by the small signal model of fig. 3.10 by setting $\hat{v}_{in} = 0$. Then:

$$G_{vd}(s) = \left.\frac{\hat{v}_{out}}{\hat{d}}\right|_{\hat{v_{in}}=0} = (Z_{conv}||M^2R_e) \times \frac{2(1-M)V_{in}}{D_1 M R_e} \quad (3.38)$$

For the line to output transfer function, the same procedure is followed, only this time $\hat{d} = 0$:

$$G_{vv}(s) = \left.\frac{\hat{v}_{out}}{\hat{v}_{in}}\right|_{\hat{d}=0} = (Z_{conv}||M^2R_e) \times \frac{(2-M)}{MR_e} \quad (3.39)$$

If $R_L \to 0$, then replacing (3.32), (3.36) and (3.37) into (3.38) and (3.39), they following are derived:

$$G_{vd}(s) = \frac{2V_{out}}{D_1}\frac{1-M}{2-M}\frac{1}{1+\frac{sCR(1-M)}{2-M}} \quad (3.40)$$

$$G_{vv}(s) = M\frac{1}{1+\frac{sCR(1-M)}{2-M}} \quad (3.41)$$

We can see that both transfer functions have a pole due to the capacitor at $\omega_p = \frac{2-M}{RC(1-M)}$ and therefore are first order transfer functions.

In the following figure, the Bode diagrams of G_{vd} both with inductor losses and no losses are drawn based on the data of the buck converter of table 1, for $R = 5\Omega$ and $V_{in} = 48V$, $V_{out} = 32V$, which is a nominal operational point for our converter.

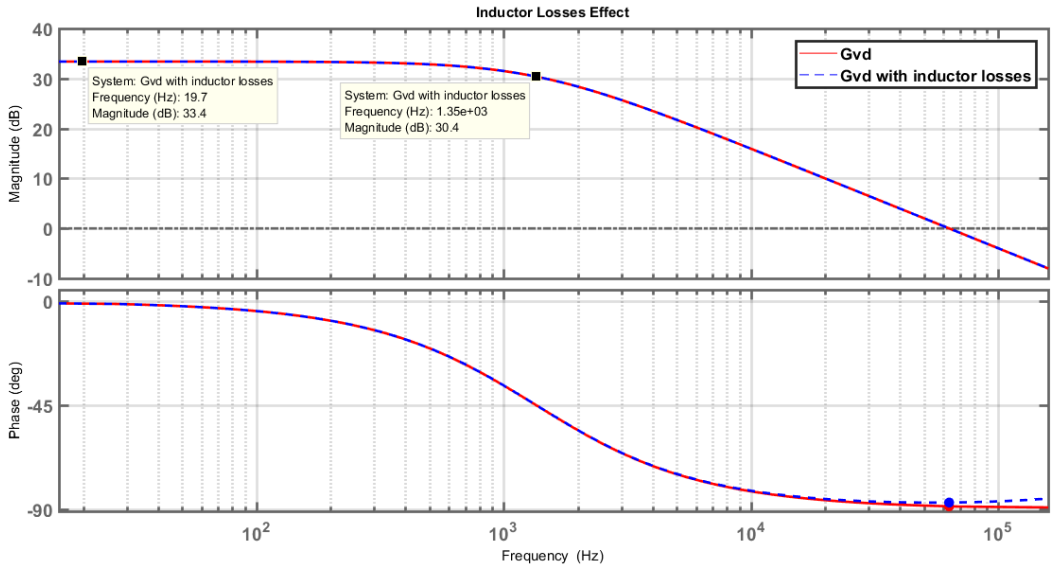


Figure 3.11: Converter Transfer Function Bode Diagrams.

The single pole present in both transfer functions is at $\omega_p = \frac{2-M}{RC(1-M)} = 1356Hz$ with a dc gain of $\frac{2V_{out}}{D_1}\frac{1-M}{2-M} = 46.77/33.4$dB, which is confirmed by the bode plots. At 1356Hz the magnitude decreases by 20db/decade due to the pole there (-3dB from the DC gain) and the phase drops by 45° at the same frequency up to -90 at$10 \times f_p$. In the case of R_L included, this induces a zero into the transfer function as can be seen by (3.37) at frequency $\omega_z = \frac{R+R_L}{CRR_L} = 2.2MHz$. The zero increases gain by 20db/decade above this frequency and also induces a phase shift up to 90° from $0.1 \times f_z = 220KHz$ as can be seen, but these frequencies are even higher than the switching frequency and thus of no importance.

In the previous analysis the inductor was omitted to find out the low frequency dynamics of the buck converter. In the drawing of the large signal model the average inductor voltage over one switching period was assumed zero to simplify the two port model equations. According to [38], the ac voltage over the inductor due to the disturbances in the inputs of the converter is not zero. In the drawing of the large signal model the average inductor voltage over one switching period was assumed zero. and therefore the high frequency dynamics of the DCM buck converter are affected. The inductor as explained in [38], inserts a high frequency pole into the converter transfer function at frequency given by :

$$\omega_p^{hf} = \frac{2Mf_s}{D_1(1-M)} \tag{3.42}$$

We can see from (3.42) that this pole is in the vicinity of the switching frequency and thus the high frequency dynamics induced by the inductor can be neglected. Indeed, a HF pole is induced due to the inductor at frequency for our data at $f_p^{hf} = \frac{2Mf_s}{2\pi D_1(1-M)} \approx 186KHz > fs$. The high frequency pole exhibits the same behavior as ω_p and starts reducing the phase at around $0.1 \times f_p = 18{,}6KHz$ and at $186KHz$ the phase is at -135° as can be confirmed by the bode diagram that follows

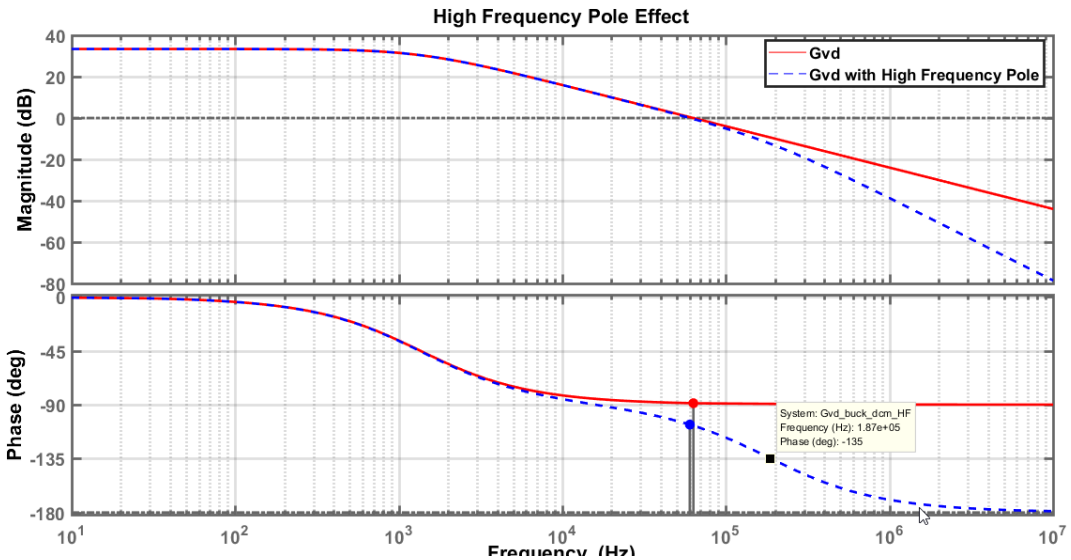


Figure 3.12: High Frequency Pole Effect on Transfer Functions.

3.3.2 Input Filter/Capacitor Effect on Buck Converter Dynamics

Finally, we should consider the effect of the input capacitor and line or source resistance on the buck converter dynamics. According to [38], and based on Middlebrooks's Extra Element Theorem, a component with impedance $Z_o(s)$ placed on the input of the converter changes its control to output transfer function as follows:

$$G_{vd}(s) = G_{vd}(s)|_{Z_o(s)=0} \frac{1 + \frac{Z_o(s)}{Z_N(s)}}{1 + \frac{Z_o(s)}{Z_D(s)}} \tag{3.43}$$

Where $Z_N(s), Z_D(s)$ are the input impedances of the converter, when $\hat{v}_{out}$ and $\hat{d}$ are set to zero respectively. $Z_D(s)$ can be seen as the open loop input impedance of the converter when the control loop doesn't work, while $Z_N(s)$ is the input impedance, when the controller perfectly regulates the output. In this case the load power is constant and from the source point of view can be seen as a negative incremental resistance toward the converter, as power is constant and supplied by the input an increase in input voltage will result in a decrease in input current and vice versa. This negative impedance can have destabilizing effects on the system according to (3.43).

To find out these impendences, the small signal model of the DCM buck converter is examined. First, to find out$Z_D(s)$, $\hat{d}$ is set to zero, and thus

$$Z_D(s) = R_e = \frac{R(1-M)}{M^2} \tag{3.44}$$

For $Z_N(s)$ a current source $\hat{\imath}_{test}(s)$ is connected to the input terminal. $\hat{v}_{out}$ is set at zero and thus $\hat{\imath}_{out} = \hat{\imath}_2 = \hat{v}_2 = 0$.Therefore, the small signal model is as seen in the figure below:

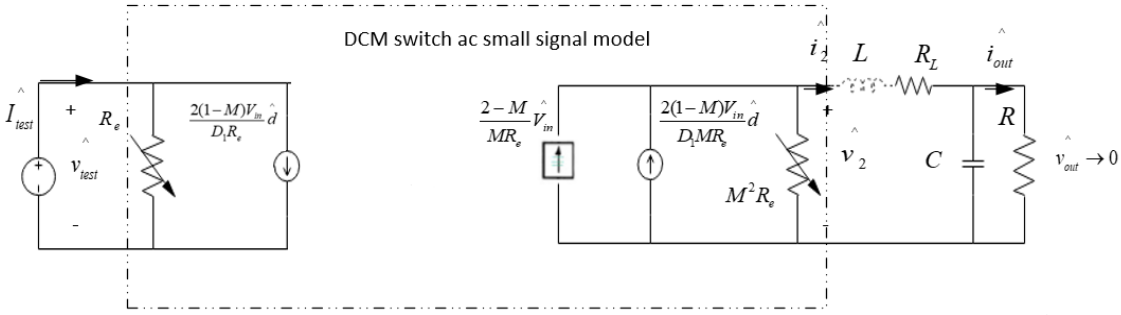


Figure 3.13: Small Signal Model when V_{out}=0.

From the figure, $\hat{v}_{test} = \hat{v}_{in}$ and from KCL, we can deduct that:

$$\hat{\mathrm{i}_2} = \frac{2-\mathrm{M}}{\mathrm{MR_e}}\hat{\mathrm{v}}_{\mathrm{test}} + \frac{2(1-\mathrm{M})\mathrm{V_{test}}}{\mathrm{D_1MR_e}}\hat{\mathrm{d}} = 0 \tag{3.45}$$

$$\hat{\mathrm{i}}_{\mathrm{test}} = \frac{\hat{\mathrm{v}}_{\mathrm{test}}}{\mathrm{R_e}} + \frac{2(1-\mathrm{M})\mathrm{V_{test}}}{\mathrm{D_1R_e}}\hat{\mathrm{d}} \tag{3.46}$$

Now $Z_N(s)$ can be found by the above:

$$\mathrm{Z_N(s)} = \frac{\hat{\mathrm{v}}_{\mathrm{test}}}{\hat{\mathrm{i}}_{\mathrm{test}}} = -\frac{\mathrm{R_e}}{1-\mathrm{M}} = -\frac{\mathrm{R}}{\mathrm{M}^2} \tag{3.47}$$

As we can see, it represents a negative incremental resistance as expected. Generally, we can see from (3.43) that if $|Z_o(s)| \ll |Z_N(s)|$, $|Z_o(s)| \ll |Z_D(s)|$, then the effect of the added component is of no significance to the converter dynamics.

An input capacitor by itself can have a dramatic destabilizing effect on the buck converter. Applying the same data as in the previous section, we get $Z_N = -11.25\Omega$ and $Z_D = 3.75\Omega$. From (3.44), in case of a capacitor filter $Z_0 = \frac{1}{sC}$, the effect of the input filter on G_{vd} is that it introduces a phase shift of 180° in the phase of the converter's transfer function, which is destabilizing for the closed control loop . This phase shift arises from the insertion to the transfer function of a RHP zero, as well as a negative dc gain of -0.33, as can be derived by (3.43).

This problem though can be addressed by damping. The simplest way to damp an input filter is by introducing a small resistance in parallel with the capacitor at a value a lot lower than the absolute value of Z_N [38], [56]. The presence of a resistance should though be taken as granted, since the line connecting to the capacitor has a resistive value or even the internal resistance of the source. For a value about $R_f = 0.1\Omega$ the input filter becomes $Zo(s) = \frac{R_f}{1+sCR_f}$ and the effect on the transfer function as derived by (3.443), is negligible as the DC gain is approximately 1. This behavior is highlighted below:

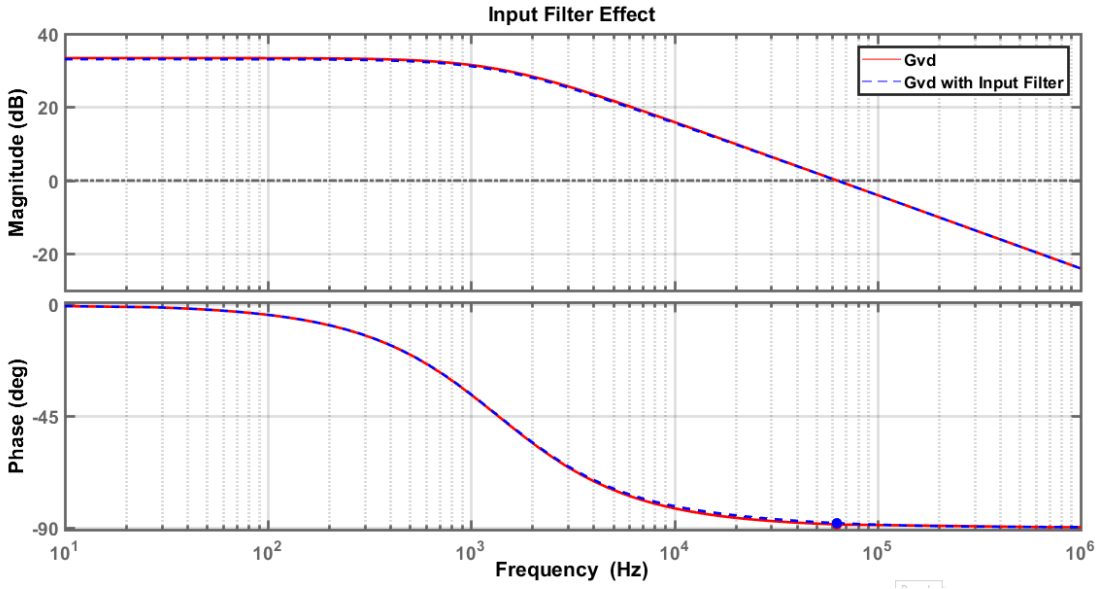


Figure 3.14: Input Filter Effect on Converter Transfer function Gvd.

3.4 Controller Design

Now that the dynamic response of the system with the open loop transfer functions was presented, the closed feedback loop response will be examined. The basic control diagram of the buck converter was presented in Figure 3.7. The negative feedback loop will be responsible for adjusting the duty cycle $d(t)$ to maintain the desired output, while rejecting any disturbances in v_{in} or in component values [38].

Now that the converter small signal transfer functions have been established the following control loop can be drawn.

$$\hat{v}_{out} = G_{vd}(s)\hat{d} + G_{vv}(s)\hat{v}_{in} \tag{3.48}$$

For the duty cycle variation around an operating point, from figure 3.7:

$$\hat{d} = G_{comp}(s) \times (\hat{v}_{ref} - \hat{v}_{out}) \tag{3.49}$$

Where G_{comp} is the controller/compensator transfer function which we need to design in order for the control to meet the design criteria. The output voltage response of the closed feedback loop to changes or disturbances in v_{ref} and v_{in} can be given by eliminating $d(t)$ in (3.50):

$$\begin{aligned}\hat{v}_{out} &= \frac{G_{vd}(s) \times G_{comp}(s)}{1 + G_{vd}(s) \times G_{comp}(s)}\hat{v}_{ref} + \frac{G_{vv}(s)}{1 + G_{vd}(s) \times G_{comp}(s)}\hat{v}_{in} \\ &= \frac{T(s)}{1 + T(s)}\hat{v}_{ref} + \frac{G_{vv}(s)}{1 + T(s)}\hat{v}_{in}\end{aligned} \tag{3.50}$$

Where $T(s) = G_{vd}(s)xG_{comp}(s)$ is the open loop gain of the control scheme.

This equation tells us how accurately and fast the output responds to a change of its reference value and the input voltage. We can see that this response is based on the loop gain $T(s) = G_{vd}(s)xG_{comp}(s)$, so the control system can be designed through proper selection of the compensator. This equation holds true for the DC values as well or in other words for dc regulators. For example, V_{out} follows V_{ref}^{dc} accurately, provided that $T(0)$ is large, so $V_{out} = V_{ref}$.

Since we want control of the current, we will implement the controller design for a current inner loop and then a voltage control will be implemented as an outer loop towards the current control loop. So the converter transfer functions will be manipulated to express the current. Also we will make a cascaded outer voltage and inner inductor current loop to showcase the use of the inductor current as well.

We will also assume the same operational point of $M = \frac{V_{out}}{V_{in}} = \frac{32V}{48V}$, and a resistance of 5Ω. Under these conditions our converter operates in DCM.

3.4.1 Control of Output Current

When the output current is controlled then the transfer functions of the converter are modified as:

$$G_{id}(s) = \left.\frac{\hat{i}_{out}}{\hat{d}}\right|_{\hat{v}_{in}=0} = \frac{1}{R}G_{vd}(s) = \frac{1}{R} \times \frac{2V_{out}}{D_1} \times \frac{1-M}{2-M} \times \frac{1}{1+\frac{sCR(1-M)}{2-M}} \quad (3.51)$$

$$G_{iv}(s) = \left.\frac{\hat{i}_{out}}{\hat{v}_{in}}\right|_{\hat{d}=0} = \frac{1}{R}G_{vv}(s) = \frac{1}{R} \times M \times \frac{1}{1+\frac{sCR(1-M)}{2-M}} \quad (3.52)$$

and the open loop gain towards i_{ref} is $T = G_{id}(s)xG^{i}_{comp}(s)$. Initially we set $G^{i}_{comp}(s) = 1$ to investigate the uncompensated response of the control feedback loop. Then, the open loop gain is described by $G_{id}(s)$. The closed loop response towards i_{ref} is given by (3.50) and the closed loop gain is described by $T(s)/(1+(T(s))$, substitutingG_{vd}, G_{vv} with the respective current transfer functions of (3.51)-(3.52).

Both open and closed loop gain frequency responses are shown in the next figure:

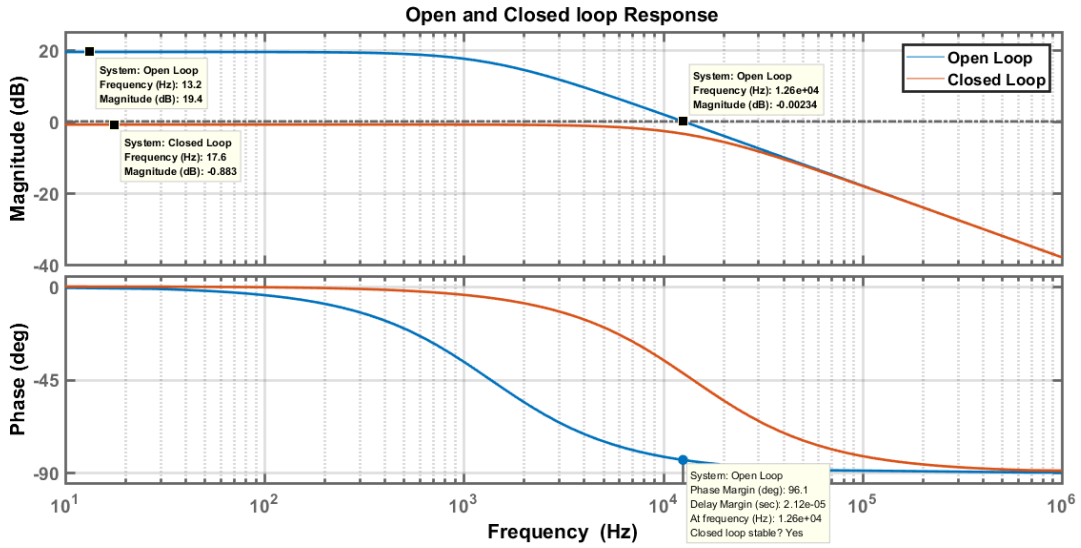


Figure 3.15: Open and Closed Loop Bode Diagram.

The closed loop response for frequencies $f \ll f_c$, where the gain of the open loop is large, tends to 0db or absolute magnitude of 1, and for $f \gg f_c$ where the gain is low, the closed loop follows the open loop curve. In other words [38]:

$$\hat{i}_{out} = \frac{T(s)}{1+T(s)}\hat{i}_{ref} = \begin{cases} \hat{i}_{ref}, & f \ll fc \text{ where } |T| \text{ is large} \\ T(s) \times \hat{i}_{ref}, & f \ll fc \text{ where } |T| \text{ is small} \end{cases} \quad (3.53)$$

$$\hat{\imath}_{\text{out}} = \frac{1}{1+\text{T(s)}}\hat{V}_{\text{in}} = \begin{cases} \hat{\imath}_{\text{ref}}/\text{T(s)}, & \text{f} \ll \text{fc where |T| is large} \\ \hat{v}_{in}, & \text{f} \ll \text{fc where |T| is small} \end{cases} \quad (3.54)$$

As expected by (3.51), the open loop exhibits a pole at frequency $f_p = \frac{2-M}{RC(1-M)} = 1356Hz$ and a dc gain of $\frac{1}{R}\frac{2V_{out}}{D_1}\frac{1-M}{2-M} = 9.354/19.4\text{dB}$ and with these data a crossover frequency of $f_c = 12600Hz$. The closed loop gain for $f \ll fc$ has a dc value of -0.88db and then follows the open loop gain. We see that these data are following the theoretical values quite satisfying.

As far as stability is concerned, and according to the diagrams presented in the previous chapters, the effect of the input filter, the inductor ohmic resistance and the HF pole are of no importance as most of them occur at frequencies higher than the switching frequency. So it is safe to assume that T contains one dominant left plane real pole as seen in (3.51). So it is inherently stable. This is also highlighted by the phase margin, which stands at 96 degrees. According to stability based on phase margin criterion, if the open loop phase (T(s)) is higher than $-180°$, the system is stable. The further from $-180°$ the phase is, the further the system is away from frequency inversion. According to [38], there is a relationship between phase margin and oscillations. The smaller the phase margin, the more unstable the system and the higher the overshoot. But with high margin the control becomes slower. Generally for a phase margin greater than 76°, the system has only real poles and exhibits no overshoot.

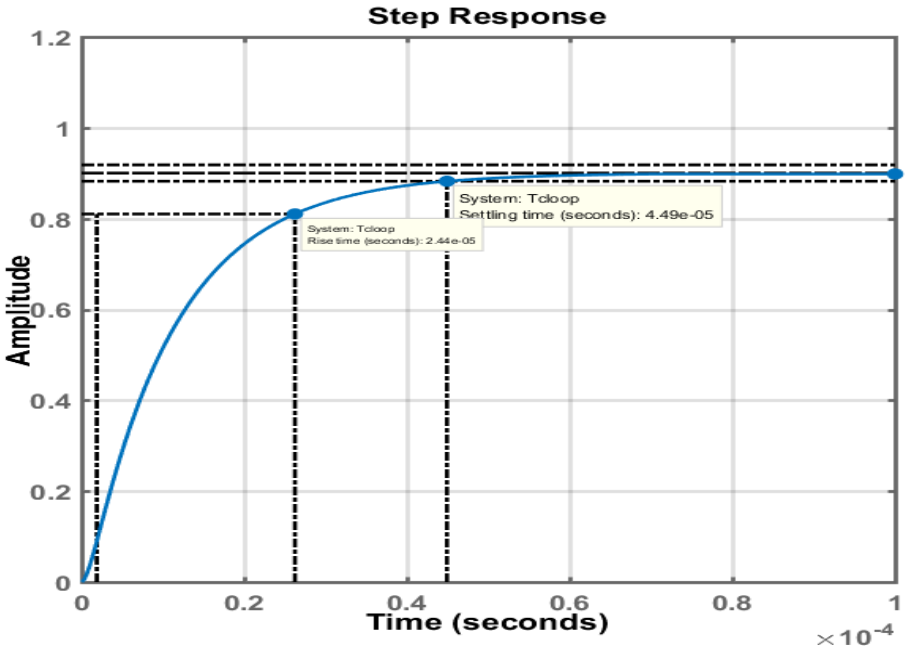


Figure 3.16: Reference tracking of the Uncompensated Closed Control Loop.

As we can see from the step response diagram above, the closed loop exhibits no overshoot, but the reference isn't followed as accurately (amplitude is less than 1). So the controller has to increase the low frequency gain of the closed loop for better reference tracking. Higher values of loop gain for low frequency will also lead to better attenuation and response to voltage input variations and changes according to (3.54). Furthermore, relative small rise and settling times as well as minimal overshoot should be assured. One controller to achieve this is the PI controller which is described by:

$$G_{comp}^{i} = K_P + \frac{K_I}{s} = K_P\left(1 + \frac{{K_I}/{K_P}}{s}\right) \tag{3.55}$$

The PI controller induces a zero at frequency $\omega_z = {K_I}/{K_P}$ in the control loop, below which the loop magnitude gain is increased. If ω_z is sufficiently lower than the crossover frequency then then the phase margin is hardly changed making them suitable for one pole systems as in our case [38]. By using this information and with the help of MATLAB Software, a zero was set at about 1470Hz, lower enough than the 12300Hz crossover frequency, to achieve minimal overshoot and good rising time, while increasing the magnitude at low frequencies and of course the reference tracking preciseness. Simultaneously, we want the crossover frequency of the compensated system to remain relatively unchanged to allow for faster control as high crossover frequencies lead to faster response. Since the uncompensated crossover frequency rests at about 10% of the switching frequency, which is a typical design criterion to allow for really low gain at switching frequencies and therefore the switching harmonics are not enhanced, we should not increase the crossover frequency. Under these considerations $K_P = 0.99$ and $K_I = 9127$ were selected. The compensated open and closed loop frequency response are presented in the figures below.

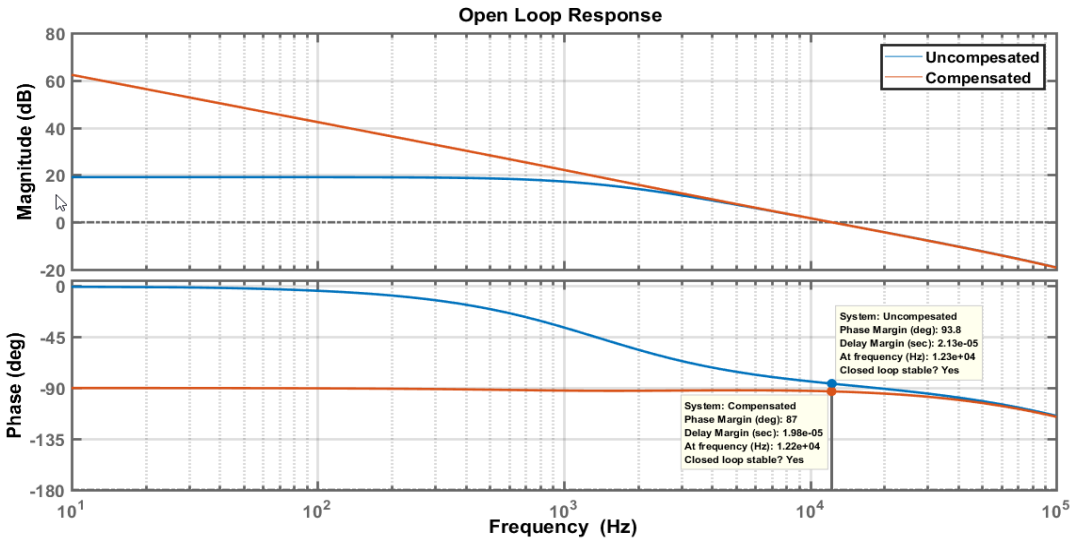


Figure 3.17: Bode Diagrams of the Compensated Open control Loop.

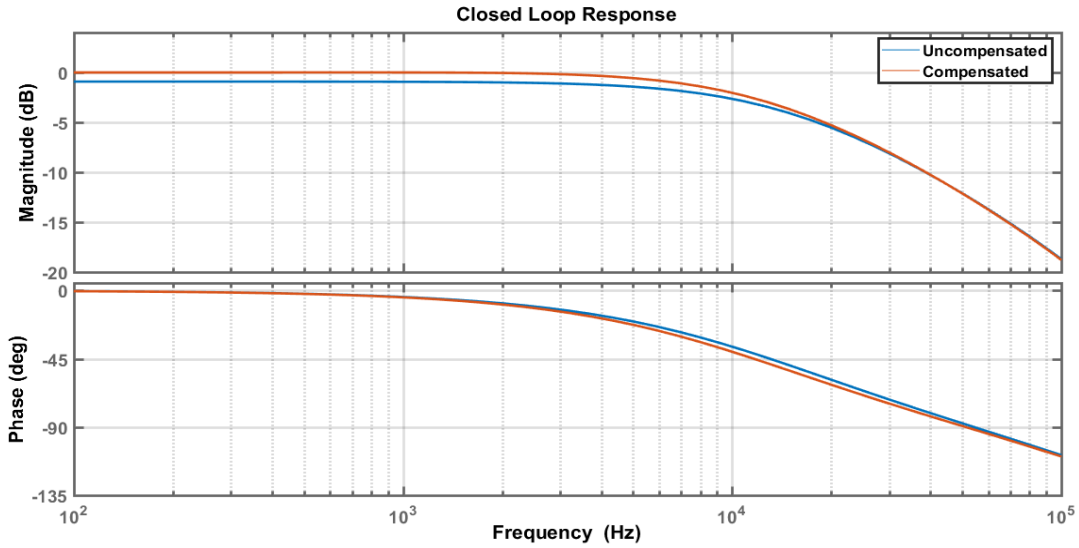


Figure 3.18: Compensated Closed control Loop Bode Diagram

Indeed the crossover frequency is retained while the low frequency gain increases dramatically, which leads to better reference tracking ($\frac{T(s)}{1+T(s)} = 1$ or 0Db) and response to input voltage variations ($\frac{1}{1+T(s)} \ll 1$).While at low frequencies down to dc the phase is decreased to -90° due to the zero induced, but near the crossover frequency a phase margin of 87° is attained which implies no overshoot and oscillations.

To validate this claim and to see the response times the step plot of the closed loop is presented below.

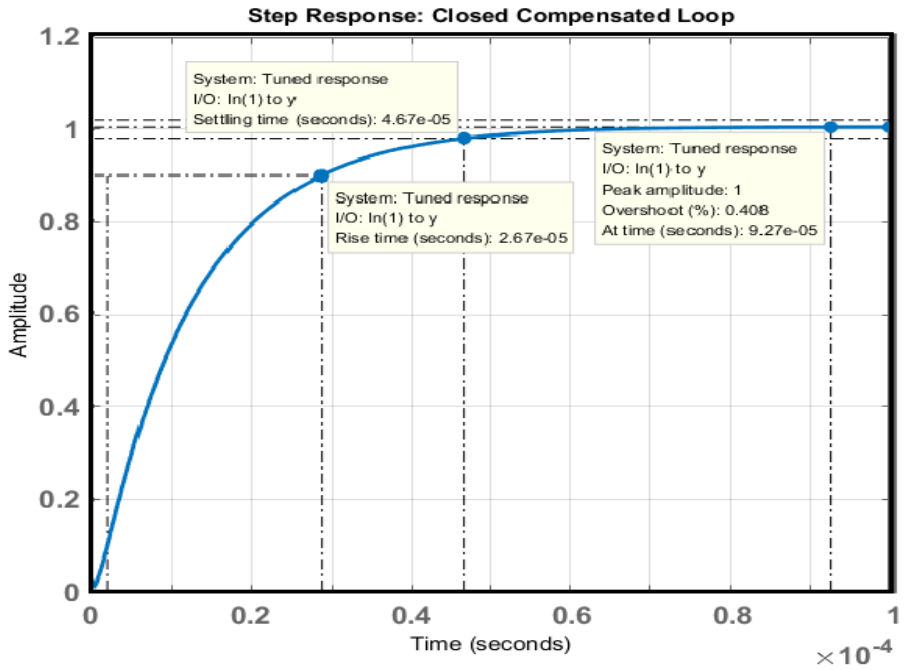


Figure 3.19: Reference Tracking and Step Response of the Compensated Control Loop

We see from the above that overshoot is kept under check, while rising and settling times are fast as before. This time, though the reference is tracked accurately with the compensation chosen.

It is worth mentioning that the controller was designed to regulate the output sufficiently and thus a large phase margin and no overshoot were design criteria. In the next section an outer voltage control will be introduced. Usually then, the inner control loop is designed to give fast response, while the outer is used for stability. So, we could make the inner controller faster and use the outer to stabilize it. This though would not yield that faster results as was found out and furthermore the crossover frequency should not increase further (faster response) to allow practically very small gains at switching frequency.

3.4.2 Outer Voltage Control Loop

In order to keep output current under regulation and protect the converter from over-currents, while being able to actively control the output voltage, an outer voltage loop is also designed. This may be redundant in this case, as the output current is linearly connected to the output voltage. With an outer control loop, output voltage can be directly controlled, while allowing for tighter current regulation and system stability.

Usually the outer control loop is set at 10 times slower than the input loop. This is done to decouple control loop dynamics from one another. Especially in buck converter, the inductor current is commonly controlled along with the output voltage which is coupled with the slow response of the capacitor. So the voltage control loop should be slower. But in case of current output control both outputs are linearly connected.

Nevertheless, the reference of the inner current controller is supplied by the voltage controller and in order for the inner controller to operate smoothly this value must be considered relatively constant. Thus the outer control loop will be designed to be quite slower than the inner. In this case the inner current controller is seen as a transfer function with a small time constant towards the outer loop.

With these considerations, the outer voltage control loop frequency is set at 1200Hz, although this could be made faster due to the linearity as discussed above. For this reason, the PI gains were selected at $K_P = 0.005$ and $K_I = 1507$. The loop response and step reference tracking are seen below:

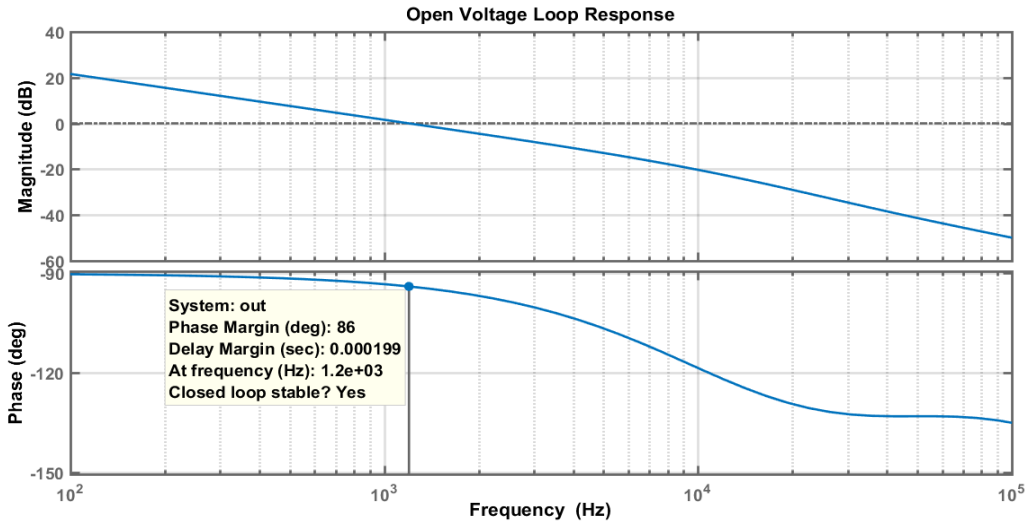


Figure 3.20: Bode Diagram for the Cascaded Open Control Loop.

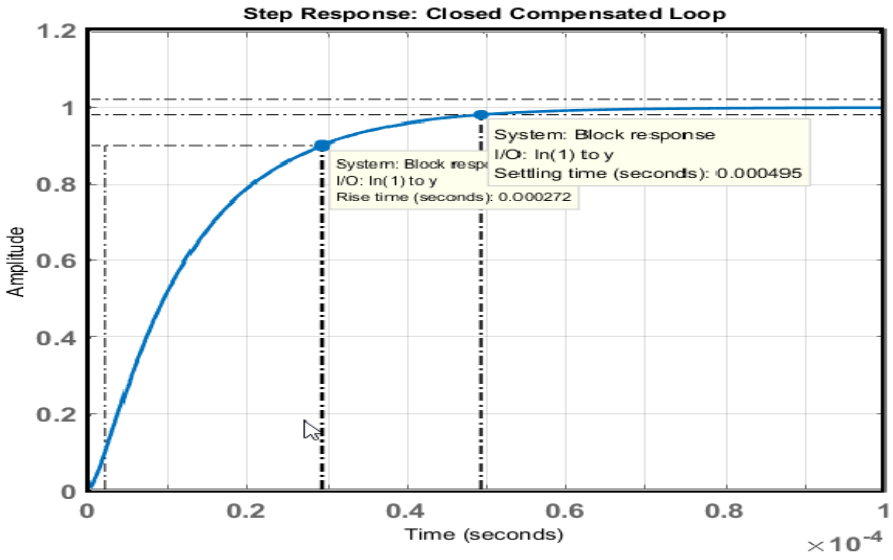


Figure 3.21: Step Response of the Cascaded Control Loop.

The rise time is expected to be at about 0.272 ms, while the settling time is predicted at about 0.5ms with no overshoot.

3.4.3 Cascaded Control of Inductor Current and Output Voltage

In this section a cascaded control scheme is made where the inductor current and the output voltage are controlled to also showcase the possibility of control also in this way. We will make the assumption that the output current is the filtered inductor current, when passed through the capacitor as approached by [38], [57]. So we can say that:

$$G_{id}(s) = \frac{\hat{i}_L}{\hat{d}}\Big|_{\hat{v_{in}}=0} = \frac{(1+sRC)}{R} \times G_{vd}(s) \tag{3.56}$$

Carrying out the procedure as outlined in the previous section, the PI gains were selected at $Kp = 0$ and $Ki = 3535$ for the inner inductor current controller and at $Kp = 1.18$ and $Ki = 2871$ for the outer voltage loop. We can see from these values that the inner controller consists only of an integrator. Indeed, this is valid if we consider that the capacitor is an integrator. With this in mind the inner loop can be made arbitrarily fast. The outer controller though should also be 10 times slower. To keep consistency with the previous control and design criteria, the outer loop was designed aiming at 2 KHz. The open loop response as well as the step response of the cascaded control can be seen below:

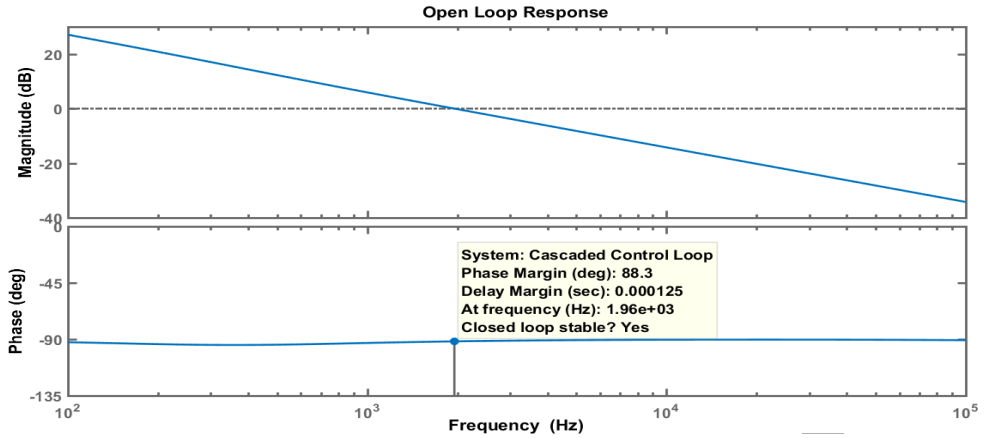


Figure 3.22: Bode Diagram for the Inductor current-Voltage output Cascade Control.

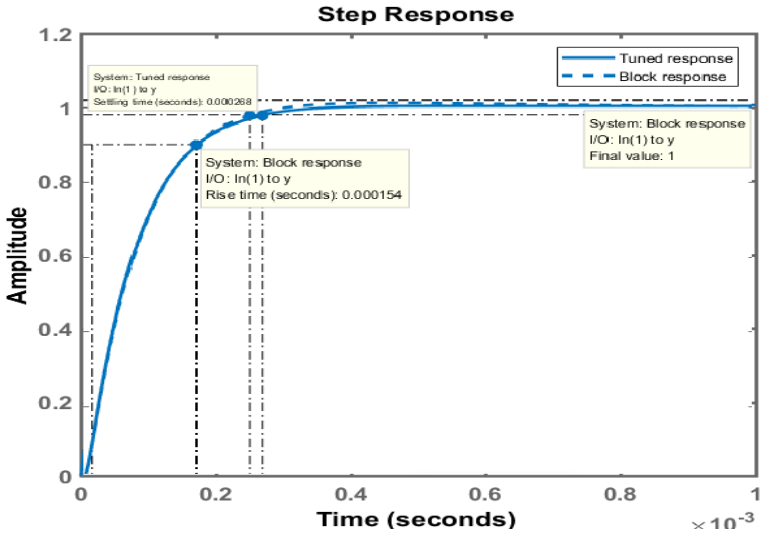


Figure 3.23: Step Response of the Cascaded Inductor Current Voltage output Control Loop.

We see that the rise time is predicted at 0.1ms while the settling time at 0.3ms, which is faster than the previous control loop as expected, due to the higher cut off frequency of the control loop in regard to the cascaded control of the output current and voltage.

3.5 Simulations

The above analysis ended with the controller design and specifications for the converter of figure 1, when operated in buck discontinuous mode. In order to verify the validity of our results, the converter is going to be simulated and the results be presented here.

For simulations two switching models were implemented. The first model was based on the mathematical equations of the buck converter as presented in the analysis of section 3.2.2 and as simulations are faster in this model and a more in depth understanding is gained. Then a model based on the physical system of the converter was constructed to confirm the results and to see all the phenomena associated with the physical system operation.

The mathematical model is described by the following equation set with the Laplace transformation:

$$
\begin{aligned}
V_{inductor} &= S_1 \times V_{L1} - S_3 \times V_{L2} - i_{inductor} \times R_{inductor} \\
V_{L1} &= 1/(R_{cable} \times C_{in}) \times V_{in} \\
V_{L2} &= V_{out} \\
V_{inductor} &= sL\, x\, i_{inductor} \\
V_c &= i_{inductor} - i_{out} \\
i_{out} &= \frac{V_{out}}{R}
\end{aligned}
\tag{3.57}
$$

In the table below the parameters of the converter and the nominal operation conditions can be seen:

Table 3.2: Simulation Data

Component	Value
Input Voltage ($\boldsymbol{Vin}$)-Nominal	48V
Output Voltage ($\boldsymbol{Vout}$)- Nominal	32V
Load ($\boldsymbol{R}$)	5Ω
Inductor ($\boldsymbol{L}$)	2.2μH
Inductor Losses ($\boldsymbol{R_L}$)	0.77mΩ
Input/ Output Capacitor ($\boldsymbol{C_{in}/C_{out}}$)	94μF
Switching Frequency ($\boldsymbol{f_{sw}}$)	100KHz
Cable Resistance ($\boldsymbol{R_{cable}}$)	0.01Ω
MOSFET On-Resistance ($\boldsymbol{R_{on}}$)	6.5mΩ
Internal Diode Forward Voltage Drop ($\boldsymbol{V_d}$)	0.9V

From equation (3.9), we see that $K = 0.09$, so for $D < 0.91$, converter is in DCM. We see that for output voltage up to 43.7V, the system will remain in DCM. In nominal operation in case of the smart-grid, we need to start up the system up to 32V, as we discussed in the introduction, well below the boundary condition.

First we are going to see the cascaded control of the output current and voltage. The main operation is to start up the system up to 32V. The control signal of switch 3, S3 is set always on while of switch 4 to always off. Since a lot of talk was done on reference tracking also the response to reference change will be examined as well as its stability and operation under voltage input change. These are shown below in both models.

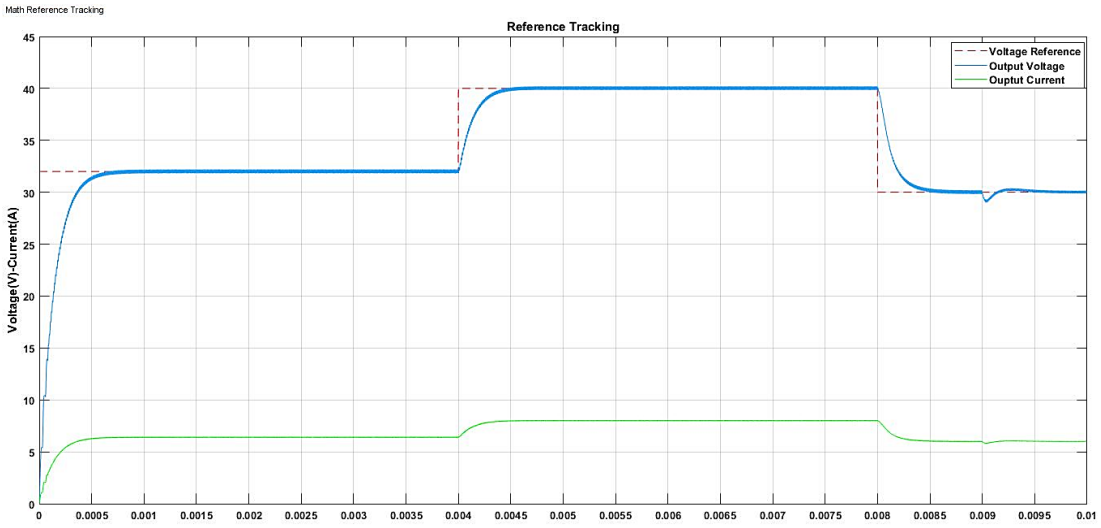


Figure 3.24: Reference Tracking of Cascaded Control Math Model

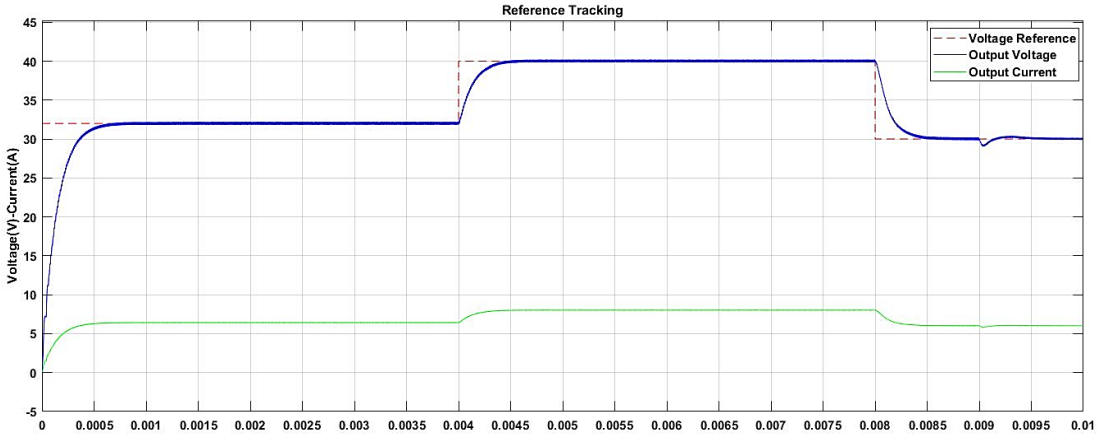


Figure 3.25: Reference Tracking of Cascaded Control Electrical Model

As we can see both models yield identical results. We see that during startup the control needs about 0.5ms to reach the value of 32V, which confirms the analysis done in the previous section which predicted similar settling time. We also see that during changes in the reference signal, the output voltage and current control respond quickly enough, as it assumes the reference value after only 0.5 ms , during the changes from 32 to 40V and then at 0.8ms to 30 Volts. Also it is confirmed that there is no overshoot which is one design specification we set. Another significant characteristic can be seen at 0.9ms. At this point a step decrease from 48V to 36V in input voltage is taking place. Nevertheless we confirm that the controller accurately follows the voltage reference in 0.5ms, which again confirms the settling time of the theoretical analysis.

A more in depth look into the switching action of the converter over one switching period can be highlighted in the next figures.

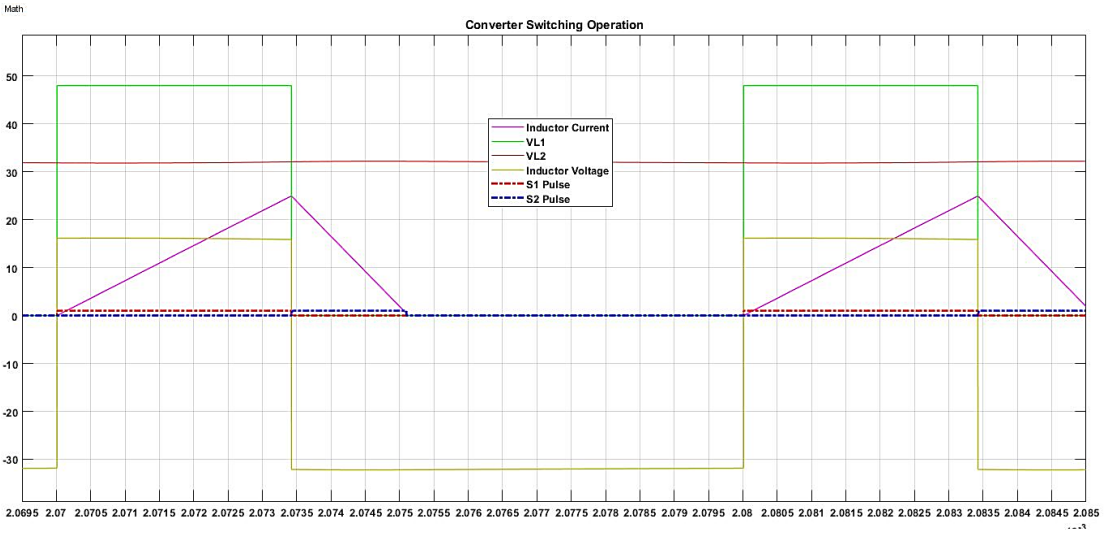


Figure 3.26: Switching period of Converter-Math Model

First we take a look into the mathematical switching model and the basic operation. This is a steady state operation point where the converter has assumed the nominal voltage of 32V. We see that when S1 switch conducts the inductor current is increased and when S1 switches off the current decreases under the negative voltage induced until it reaches zero. In this time S2 is conducting for exactly the specific time needed for the current to extinguish. Indeed for the operational condition M=0.667, which according to (3.36) yields a D1 of 0.3425, according to

(3.30) a D2 of 0.173 and a peak current of 24.9 (3.20), which are all confirmed by the simulations.

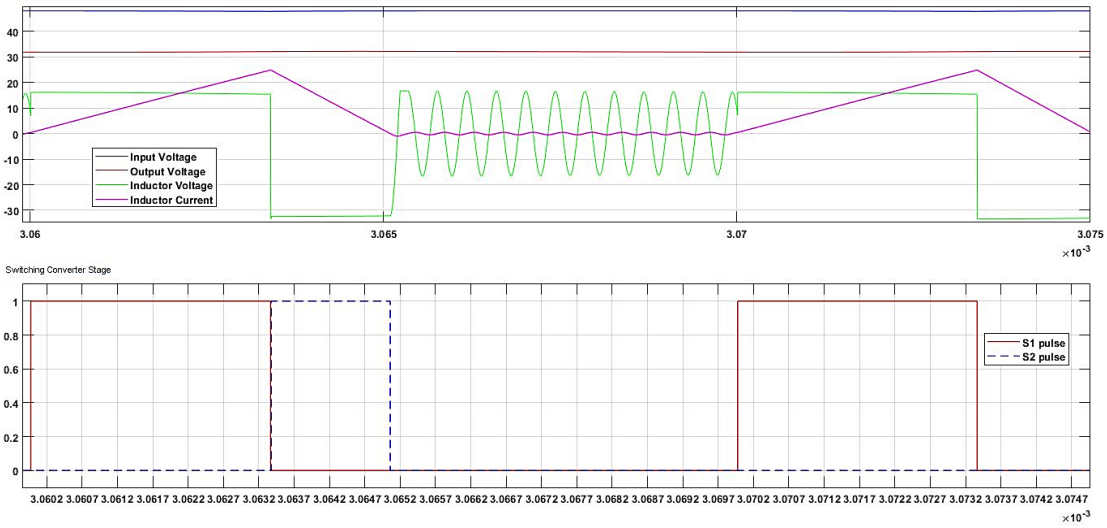
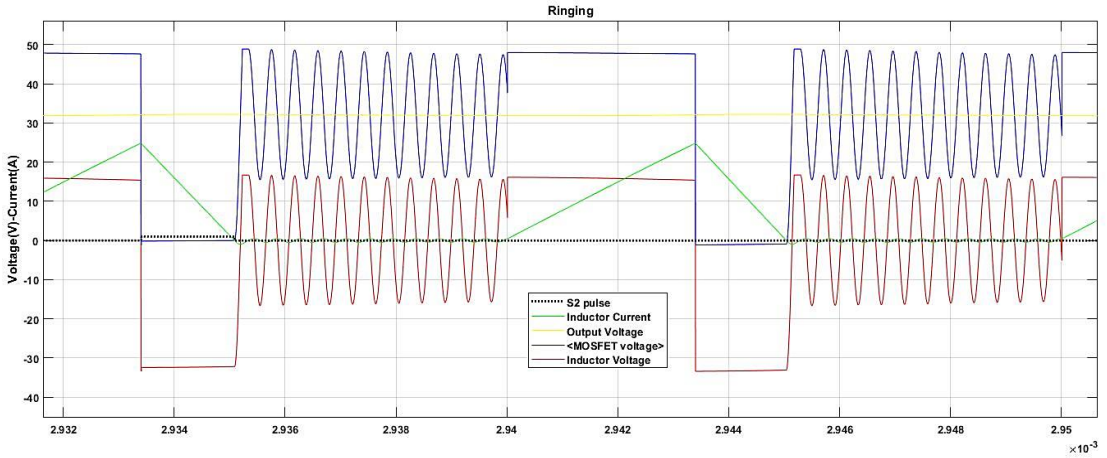


Figure 3.27: Switching period of Converter-Electrical Model

In the above figure the same can be seen for the converter but in the electrical converter model. The same as above can also be confirmed here. But this model highlights two important characteristics. The first has to do with the effect of the synchronous DCM operation. We can see two switching periods one with the S2 as an active controlled switch and the next period where S2 is deactivated and the antiparallel diode of S2 conducts. It can be observed, that while the antiparallel diode conducts, then according to (3.12), $V_{inductor} \approx -V_d - V_{out} = -0.9V - 32V = -32.9V$. But when S2 is actively controlled, the $V_{inductor} \approx -32V$. This is highlighted also in the figure below:



Figre 3.28: Ringing in the Converter

Another important phenomenon that can be revealed in both figures Figure 3.27 and Figre 3.28 is the ringing of the current during the period when both S1 and S2 are off. This is due to the capacitances placed in parallel to each MOSFET, for the operation of ZVS as will be described in the next chapter. According to [38], the diode minority charge stored during deadtime between switching, cannot be extinguished instantaneously, when inductor current reaches zero, so the diode remains forward biased for some time after D_2Ts time period, when S2 is switched off. This can be seen by the -0.9V value of the voltage. So it conducts the inductor current and it goes to negative values extinguishing the minority charge of the diode. When the

diode becomes reversed biased due to minority charge depletion, this negative current flows through the capacitor and together with the inductance of the converter forms a resonant circuit, which creates this oscillation in the current and consequently the switch node voltage and the inductor voltage. This phenomenon, though doesn't induce additional losses as the oscillations aren't damped, which would mean losses to resistive elements. The frequency of ringing oscillations is given by:

$$f = \frac{1}{2\pi\sqrt{LC_{oss}}} = 3{,}4Mhz \tag{3.58}$$

which is comparable to the results of the simulation.

Finally, the cascaded control of the inductor current and the output voltage is implemented and the simulation of the physical model will be presented.

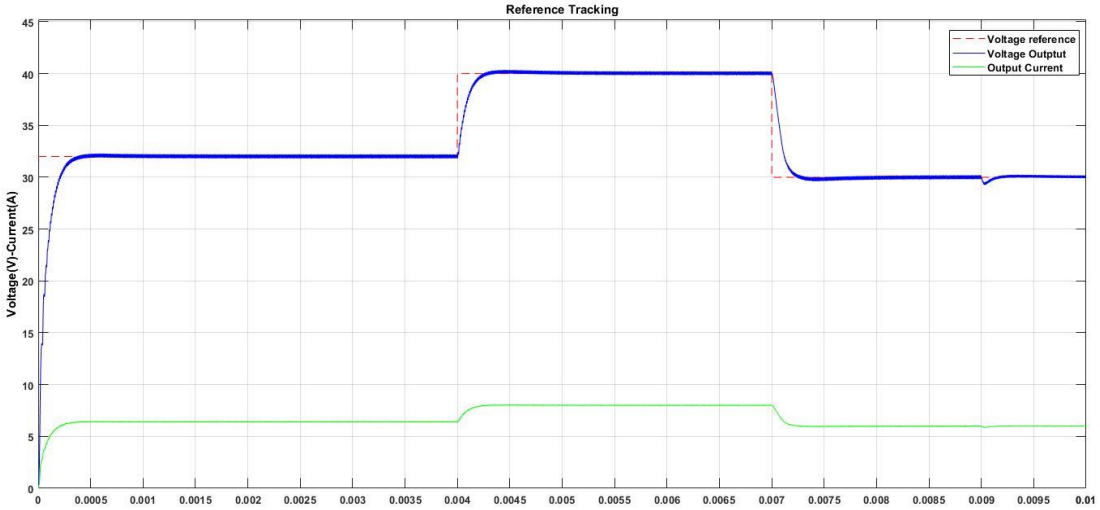


Figure 3.29: Reference Tracking of Cascaded control of Inductor Current

We can see that this control is also accurately tracking the reference and more specifically faster than the previous controller, since a 2KHz control loop was implemented in this case in contrast to the 1200KHz of the previous control loop. This time the settling time is at 0.3ms consistent with the theoretic analysis of this loop that was made before.

4 CF-ZVS operation of the converter

4.1 Introduction

In the previous chapter the cascaded converter was operated in buck mode in order to highlight its use as a startup of the 48V DCMG we are going to examine in the next chapter. But the components of the DCMG may operate over a wide range of operational voltages. Thus buck and boost mode of operation is needed. Instead of implementing separate controller for both buck and boost operation, a buck-boost modulation strategy as presented in [17] is selected. This control not only allows for higher utilization and power density but also enables zero voltage switching of the MOSFETs, both during-turn on and turn -off transitions (CF-ZVS-M). Furthermore, this modulation strategy allows nominal operation when input and output voltages are equal and smooth transitions from buck to boost mode operation in contrast to other control techniques, where special transition modulations must take place, as we discussed in the literature review[40], [45].

As we saw in the previous chapters, a hardware cascaded converter for this mode of operation was implemented in Laboratory of DC Systems, Energy Conversion & Storage group of TU DELFT as presented in[51]. This converter was only tested though in steady state condition with predefined calculated switching times as proposed by [17], [50].

In this thesis, a control scheme for the above mentioned modulation strategy is going to be implemented and simulated to determine its dynamic behavior and suitability as the universal converter for the DCMG. Due to the need for interfacing different components, it will also be controlled bidirectionally. It should be noted that the operational voltage ranges of this converter are set at 20-50V for the input voltage and 32-52V for the output. Due to this characteristic, a cooperative control where buck operation is used for the startup and then the modulation strategy will be presented.

4.2 Theoretical Analysis

For ease of reference the cascaded buck and boost converter is shown below:

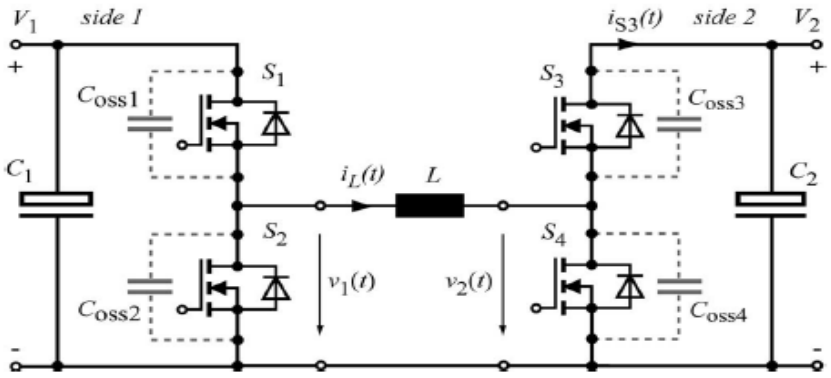


Figure 4.1: The cascaded Buck-Boost Converter

As explained in [17] and shortly presented in this section, in this modulation strategy every MOSFET is switched once per period. Turn on under zero voltage (ZVS) is ensured, by

switching on the MOSFET, when the antiparallel body diode of each switch conducts the inductor current. At the same time the antiparallel body diode of the complementary half bridge switch is reversed biased and therefore doesn't conduct the current. For this reason, the inductor current is modulated in way that will allow for ZVS in all instances. It is obvious that in order for an antiparallel body diode to conduct in the beginning of each cycle, a negative inductor current is needed. Turn off ZVS is achieved through the capacitances C_{oss} in parallel with each MOSFET (Figure 4.1), which have the effect of delaying the voltage rise on the MOSFET, thus enabling it to turn off at low voltage.

In more detail, the switching period can be divided into four time intervals, depending on whether a switch conducts or not. The inductor current waveform as well as the switching intervals can be seen in the figures below[17]:

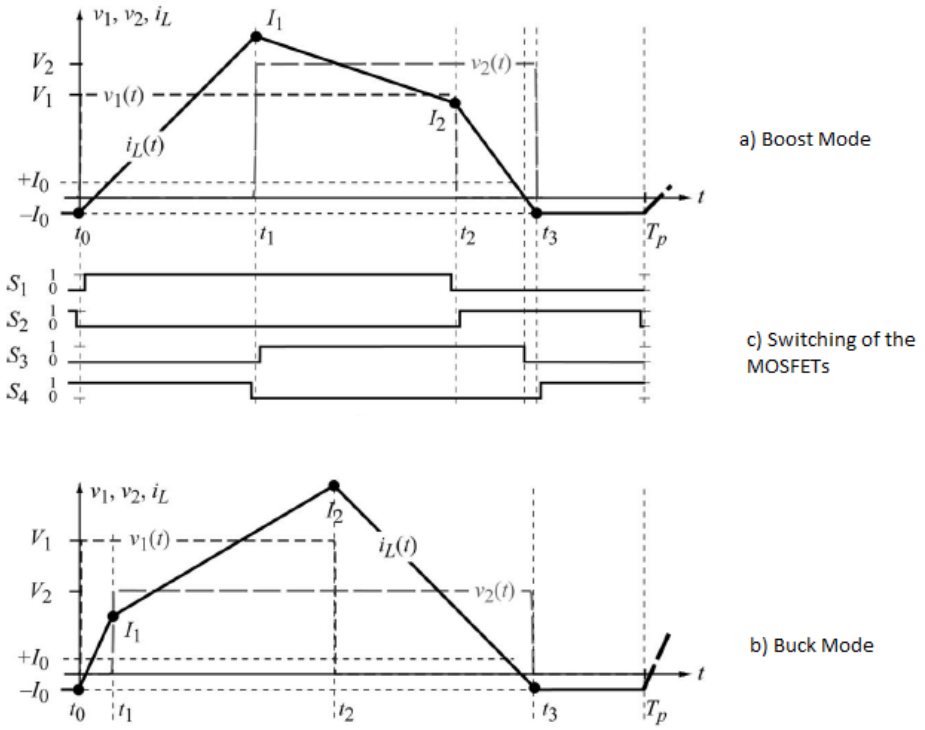


Figure 4.2: Inductor Current Waveform and Switching Intervals

Before the start of a new period ($t < t_0$), S2 and S4 switches are conducting the inductor current, which has a negative value by demand for ZVS to take place in the beginning. More specifically at $t = t_0$, S2 can turn off under ZVS since C_{oss2}, delays the voltage rise across it. During the interval between S2 turn-off and S1 turn-on, the inductor current with the negative value is conducted between the inductor and the parallel capacitances of the two switches, discharging C_{oss1} and charging C_{oss2}, as can be seen in Figure 4.3a. After this is done, the current switches from Coss1 to the antiparallel body diode of S1. This is the condition for ZVS so now S1 can switch on and since it has a lower resistance path than the diode, it conducts the inductor current.

In the next time interval ($t_0 < t < t_1$) , S1 and S4 conduct (Figure 4.3b) and the inductor voltage becomes $v_L = V_1$, so the current increases (Figure 4.2). At t_1, S4 can turn off under ZVS due to Coss4, which delays the voltage rise again, since first it must be charged. At the interval between S4 switch off and S3 switch on, the inductor current is flowing from the inductor towards the parallel capacitances of S3 and S4, charging C_{oss4} and discharging C_{oss3}. When the voltage drops due to discharging, the antiparallel body diode starts conducting the

current. Now S3 can be switched on under ZVS and conduct the inductor current, since it presents a lower resistance path (low voltage drop) in respect to the antiparallel diode forward voltage drop.

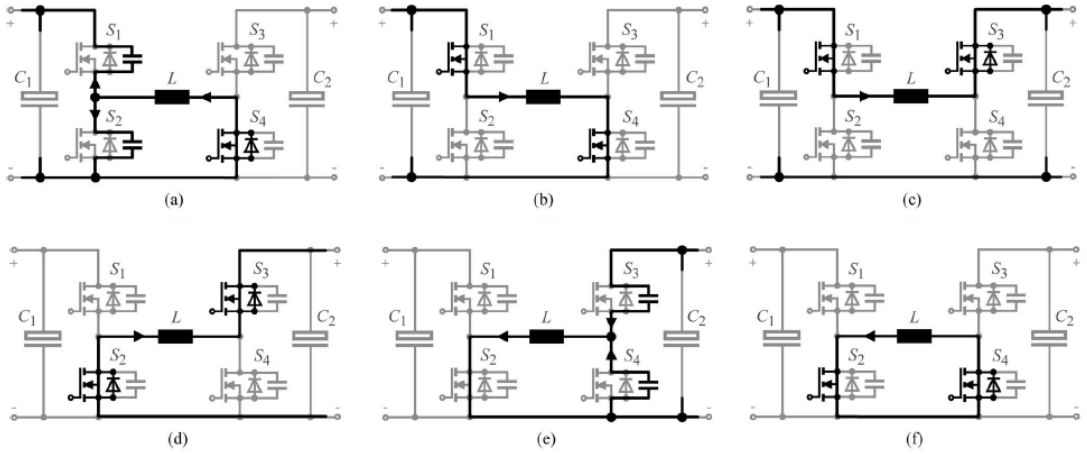


Figure 4.3: Circuit Topology at different time instances and intervals

In this interval ($t_1 < t < t_2$), S1 and S3 conduct (Figure 4.3c) so the inductor voltage is given by $v_L = V_1 - V_2$ and depending on the operation (Buck with M<1 or Boost M>1) mode the current may increase or decrease. At t_2 again, S1 can now switch off under ZVS and in the corresponding subinterval, C_{oss2} is discharged while C_{oss1} is charged, but now the current transfers energy from the capacitances of S1 and S2 to the inductor. Again, when C_{oss2} is discharged, the antiparallel body diode conducts and S2 is turned-on under ZVS.

During the next interval ($t_2 < t < t_3$), S2 and S3 conduct so the inductor voltage is $v_L = -V_2$ and thus the current decreases. Since both S2 and S3 conduct the current due to their lower voltage drop in respect to the antiparallel diodes, the current is allowed to go to negative values. The next period has to do with setting the negative offset current necessary for the next period. Thus at t_3 S3 can be switched off under ZVS, since C_{oss3} will delay voltage rise. The negative current during the dead-time between S3 and S4 will now charge C_{oss3} and discharge C_{oss4}, while it transfers energy from the capacitances towards the inductor (Figure 4.3e). Again, when the interval finishes, the antiparallel body diode of S4 conducts the negative current and therefore S4 can be switched-on under ZVS (Figure 4.3f).

Finally during ($t_3 < t \leq T_p$) , it is obvious that $v_L = 0$ so the current will stay at its negative value. Also in this way frequency is kept constant, since no other switching occurs in the period.

In order to calculate the timings of the converter operation, the inductor voltage will be solved for each time interval as seen in Figure 4.2. The inductor voltage equation then concludes to the following equations:

$$t_1 - t_0 = L\frac{I_0 + I_1}{V_1} \tag{4.1}$$

$$t_2 - t_1 = L\frac{I_2 - I_1}{V_1 - V_2} \tag{4.2}$$

$$t_3 - t_2 = L\frac{I_0 + I_2}{V_1 - V_2} \tag{4.3}$$

The average power from input to output and vice versa is given by:

$$P_{tr} = \frac{1}{T_p}\int_{t_0}^{T_s} v_1(t) \times i_1(t) \tag{4.4}$$

And by assuming constant voltage in the input and solving for the time interval where S1 is switched-on we get:

$$P_{tr} = \frac{V_1}{T_p}\int_{t_0}^{t2} i_L(t)\,dt = \frac{V_1}{2T_p}((I_1 + I_2) \times t_2 - (I_0 + I_2) \times t_1) \tag{4.5}$$

This set of equations constitutes the control modulation. In this analysis, losses were disregarded. According to [50], losses in the system could be represented as an equivalent resistor compromising the R_{on} resistances of the switches as well as the inductor losses. Then the system would become a set of differential equations which would be more difficult to be computed in a simulation, where computation of the equations is happening in real time. Generally though, as [17] suggests the system is adequately described by (4.1-4.5).

These 4 equations have five unknowns. Therefore one of the above variables needs to be selected with a degree of freedom for an operating point of the converter described by V_1, V_2 *and* P_{tr}. The system needs to transfer power from the input to the output and is analogous to the area below the inductor current waveform of Figure 4.2. Under this consideration in order to increase this amount to match the required power, either t_1 or t_2 must be adjusted, while t_3 is kept constant or t_3 is moved towards the end of the switching period as can be seen in Figure 4.2. If t_3 is selected with a degree of freedom, then this results to lower RMS currents and therefore to lower losses in ohmic resistances of the converter.

So in order to determine the timings the following procedure is implemented, as depicted in the graph below:

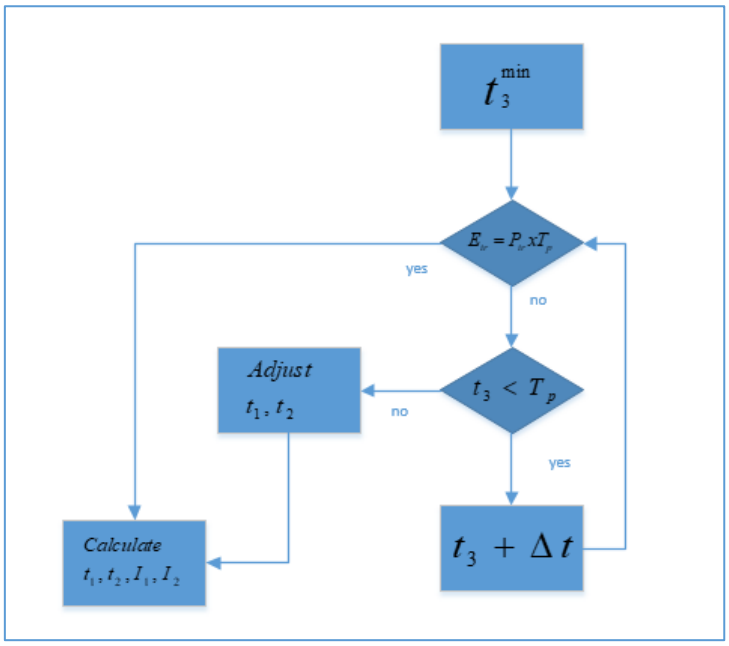


Figure 4.4: Algorithm procedure for Switching Times calculation.

As depicted in the chart, first a minimum t_3 is calculated by taking into account the limitations of the soft switching operation. So from (4.3), by setting $I_1 = I_0$ for a buck operation and $I_2 = I_0$ for boost mode, we get:

$$t_3^{min} = \frac{2I_0L(V_1 + V_2)}{V_1V_2} \tag{4.6}$$

For this value of t_3, the set of equations (4.1-4.5) is solved. If P_{tr} is not achieved with this value, then t_3 is increased in step in the range $t_3^{min} \leq t \leq T_p$, until the power condition is satisfied. If $t_3 = T_p$ without the condition having been met, then t_1 and t_2 are adjusted accordingly. The maximum power that can be transferred then is given by:

$$\mathrm{P_{tr}^{max}(t_3) = \frac{V_1V_2(I_0^2L^2 - 2I_0L(V_1 + V_2)t_3 + V_1V_2t_3^2)}{2LT_p(V_1^2 + V_1V_2 + V_2^2)}} \tag{4.7}$$

This maximum power should not be exceeded, because then the soft switching conditions will not be met. Another important parameter for ZVS is the proper selection of the offset current I_0. Before turn-on of S1 the current circulates between the parallel capacitances of the half bridge and the inductor forming a resonant circuit (Figure 4.3a). I_0 should be sufficiently large, in order for the energy stored in the inductor during the turn off transitions, be able to transfer the charge from one capacitor (C_{oss2}) to the other (C_{oss1}) and allow the switching take place under ZVS. The same holds true for S4. From the energy balance equation in the resonant circuit we get:

$$\frac{1}{2}C_{oss} \times V^2 = \frac{1}{2}L \times {I_0}^2 \underset{max}{\Longleftrightarrow} I_0 \geq max(V_1^{max}, V_2^{max}) \times \sqrt{\frac{C_{oss}}{L}} \tag{4.8}$$

In reality I_0 should be higher due to the additional charge built in the body diode to compensate for the losses. But errors in the timings could lead the inductor current to decrease below $-I_0$. So additional measures must be taken to stop the current from going below I_0 which in turn would increase ohmic losses in the non-ideal components of the converter. Of course the condition (4.8) must apply during all switch turn-ons. S3 turns on at t_1 and S2 at t_2. In these times the inductor current must be at least as the value above, so:

$$\mathrm{I_1 \geq I_0 \text{ and } I_2 \geq I_0} \tag{4.9}$$

In [51], a sensitivity analysis based on (4.7)-(4.8) was carried out to estimate the required inductor value in order for the soft switching conditions to hold true for a specific voltage range and power. More specifically in order for (4.7) not to be surpassed, the inductor L is chosen with the minimum values of the operating ranges and the maximum power that can be transferred from (4.7) for t_3=T_p. Also according to [58], the output and input capacitor values can be selected from :

$$\mathrm{C_1 = C_2 = \frac{T_p}{\hat{u}_{ripple}}\left(\frac{P_{max}}{V_{max}} + \frac{2LP_{max}^2}{T_pV_{max}^3} - \frac{6\sqrt{14\frac{L}{T_p}P_{max}^3}}{7V_{max}^3}\right)} \tag{4.10}$$

It should be noted that instead of using the parasitic capacitances of the MOSFETs as in [17], additional capacitors were used in parallel with each MOSFET. This was done because the parasitic capacitances exhibit non-linear characteristics. So the values were selected as in the following table[51]:

Table 4.1: Calculated Converter Parameters

Parameter	Value
Inductor	2.2μH
Input-Output Capacitor	94μF
MOSFET Capacitance	1nF

4.3 Control of the Converter with the ZVS modulation

4.3.1 Control Structure

In [51], the converter was only tested in steady state conditions, with static signals applied on the gate of the MOSFETs, while the switching times were estimated by trial and error. In this work, a control model with the live calculation of the timings and control of the input and output voltage and currents will be created. Also selection of the proper offset current will be selected and the dead-time value will be more closely estimated.

The same model implemented for the buck converter, the electrical switching model is also employed in this chapter. The basic control structure in this operation is of course the timings calculation algorithm. In [50] the equations set were solved for the a range of operational points defined by three parameters, V_1, V_2 and P_{tr}. The solutions t_1, t_2 and t_3 were then predefined and incorporated into a three dimensional look-up table. During operation of the converter, timings were extracted by this look-up table through linear interpolation, in order to minimize the computation effort for the controller.

In this thesis though, the computation of the exact solutions for the set of equations is taking place simultaneously with the converter operation. This was done for two reasons. The first has to do with validating that the operation of the soft switching modulation control in dynamic conditions, yields the same results as expected by the equations. The second has to do with the linear interpolation. As stated in [17], the partial derivatives of the interpolation in the look up table must be continuous to allow for small errors. If discontinuities exist, then small variations in the input parameters can cause significant calculations errors. It is more preferable for timings thus to change in a continuous way to allow for more exact solutions.

To decrease the computation effort, the set of equations was solved analytically towards the variables t_1, t_2, I_1, I_2, which depend on the operational point conditions as described by V_1, V_2 and P_{tr} and t_3. As explained in the previous section t_3 is calculated and set at a minimum value (4.6) and then increased by a very small step of 10nsec, as in the flow chart of Figure 4.4, until the power (4.5) and the current conditions (4.9) are met. The algorithm developed is run in the beginning of each period, so the values are refreshed every $T_p = 10\mu s$. The process is illustrated in the figure below:

It should be noted that the signals towards the gates of the switches are the duty cycles produced by the algorithm based on the exact timings. As we can see from the switching logic of figure 4.2, it holds that:

$$D_1 = \frac{t_2 - t_0}{T_s}$$

$$D_3 = \frac{t_3 - t_1}{T_s} \tag{4.11}$$

$$\text{phase} = t_1$$

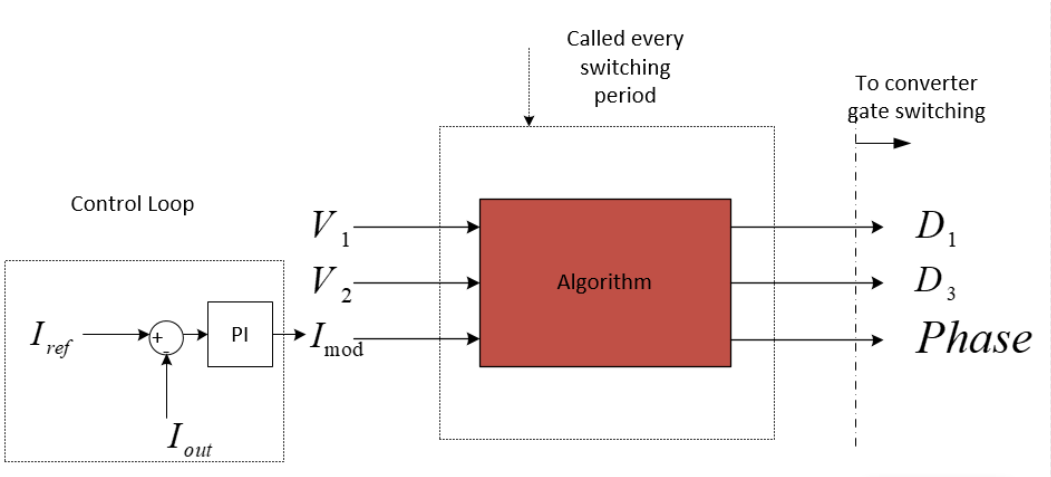


Figure 4.5: Control Diagram of the CF-ZVS Modulation Strategy

where D_1, D_3 are the duty cycles of S1 and S3 switches respectively, while phase is the delay after, which D3 pulse is activated, since all these calculations take place simultaneously but of course S3 must be switched after t1. The duty cycles and the respective pulses for S2 and S4 are the complementary of the above.

Another major point of focus regards the operating conditions as seen in the figure 4.5. As we can see the operating point for the converter is described by V_1, V_2 and I_{mod} instead of P_{tr}. This current acts as the carrier of the power P_{tr} that is transferred to the output, a measurement of the required power through which the inductor current is shaped. This current is the new control input toward the algorithm and is the control output of our PI control loop, which acts like an open loop control, since output current is not the directly controlled variable and acts as a representative value of the power to be transferred. In the figure the output current control loop is presented but of course an extra outer loop for the output voltage can also be implemented. In this case the desired output power P_{tr}, necessary for the set of equations is given by $P_{tr} = V_2 \times I_{mod}$. In this way the power is a control variable and can be controlled by setting the desired output current reference of the PI loop. The PI controllers make the system slower, but offer increased capabilities of regulating more accurately and tightly the desired output. The main reason here is to maintain the voltage and the current under the required limits. Of course the power then depends on the output load.

4.3.2 Offset current Control and Deadtime Selection

As stated in [17], [50], the inductor current must reach the value of $-I_0$ in the $t_3 < t \leq T_p$ subinterval, to allow the switching of S1 under ZVS in the next period. Some methods are proposed in [50] to address this issue. As a first approach in this thesis the inductor current is monitored during the $t_2 < t \leq t_3$ subinterval. If it reaches the required offset value, then S3 is switched off immediately and the resonant process of switching S4 begins. During the commutation interval, the output capacitances are charged and discharged and the current attains the minimum required value for ZVS for the next period. This technique is simple to implement and yields satisfying results. The main problem is that during the commutation interval between S3 and S4 the inductor current will drift below the required value of Io due to the conduction of the diode resonant circuit formed and the energy stored in it. It is dependent on the duration of the commutation interval-the deadtime. This can lead as explained in [50] to increased ohmic losses in the inductor and other ohmic elements of the converter.

For this reason a second approach was implemented to minimize the inductor current during $t_3 < t \leq T_p$ subinterval to its predefined value. Based on the ideas presented in [50], a step

algorithm was developed, which adjusts time t_3 (when S3 switches-off), to ensure that the current will stay at its nominal offset value and ZVS will be maintained. More specifically, when $V_1 > V_2$ (buck mode), the inductor current is measured when S2 switches-off and is compared to the required offset value. If it is lower than the required (higher negative value), then t_3 is decreased by a step value in the next period, while it increases if it is higher, in order to attain exactly the required value of the offset current, while ZVS is ensured also for the output since $V_1 > V_2$. The same can be done with a PI control loop, where the current value is compared to the desired one and the error is processed by a PI controller with respect to the minimum and maximum t_3 values.

In boost mode ($V_1 < V_2$) the same procedure is followed but this time, the current at the switch-on of S4 is measured and t_3 is adjusted accordingly [50]. ZVS is assured for the input as I_0 assumes the required value. But during switch-off of S3, the inductor current may have positive values, which means that the diode will conduct increasing the voltage that the capacitor has to build across S3 and discharge across S4 in the commutation interval. In [50], this is addressed through a hysteresis loop, but here this can be taken care by proper selection of the deadtime as we will examine next.

Regardless of the control method of I_0 to ensure ZVS, the control method of the converter assumes the following structure:

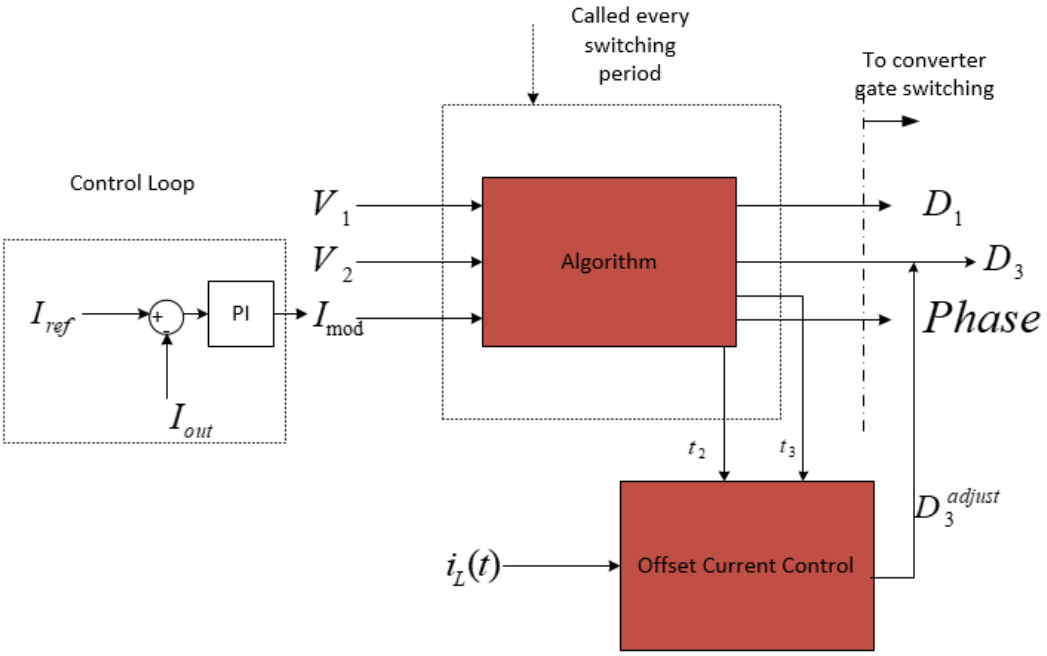


Figure 4.6: Control Diagram of the CF-ZVS Modulation Strategy with Offset Current Control

The last thing then that needs to be taken care of is the dead time or the commutation interval between the switching-off and switching-on of the half bridge switches. Deadtime must be carefully selected for each switch as it is crucial to allow for ZVS to take place. The deadtime depends on the voltage level across the MOSFET and the inductor current during the commutation interval and of course the parallel capacitance of the MOSFET. Under these considerations the deadtime can be approached as:

$$2xC_{oss}\frac{dV}{dt} = i_L(t) \tag{4.12}$$

The double value for the capacitor has to do with the resonant process during the commutation interval because the inductor current is split between the two MOSFET capacitors, which may be regarded as parallel connected (Figure 4.3a). During the commutation intervals, the inductor current i_L is not constant, but if approached as such, then (4.12) yields:

$$t_{deadtime} = \frac{2xC_{oss} \times V}{i_L} \tag{4.13}$$

The capacitor has to be charged up to this voltage for the switch that turns-off and discharged from this value for the switch that turns-on. In other words, it is the input or output voltage of the converter, depending on which side each switch lies. In this thesis the deadtime is implemented for the worst case scenario. This scenario happens when the voltage is at maximum level and the current is minimum according to (4.13). The current can be approached by its value at the beginning of the commutation interval. For S1 this is the I_0 current as well as for S4 with the offset current control of the first method, while for S2 and S3 can be approached by I_2 and I_1 respectively. With the algorithm I_0 control, since t_3 is adjusted, then S3 is then turned off at a lower absolute inductor current value than I_0, leading to an increased value for the deadtime. For the previous reason as well as for low power conditions where I_1 and I_2 are small , the offset value of the current is going to be used for all switches and a safe margin will be added to account for uncertainties like ohmic losses reverse recovery of the diodes conduction, miscalculations of the exact timings and the changing inductor current.

4.4 Evaluation of the proposed control structure.

4.4.1 Study case under nominal voltage and power conditions

In order to evaluate and validate the ZVS modulation technique as described in the previous section, simulations will be carried out in Simulink. The model that will be used is the same as in the electrical model used in the previous chapter of the buck operation. For this reason the same resistance value of 5Ω will be used as a first step for the simulations. Under the operating voltage ranges of the converter, 20-50V for input and 32-52V for output, will yield a maximum current of 10.4A or 540.8W, which come in accordance with the specifications of maximum power and current as set in [51]. This will also lead though to a minimum current of 6.4A or a minimum transferred power of 204.8W. Although these values are well in accordance with the operating power rating of the DCMG, as we will examine in the next chapter, simulations under low power and current conditions will also be carried out.

The offset current for the ZVS operation was selected at 1.6A based on (4.8). This value satisfies the minimum required value for soft switching conditions and compensating for uncertainties of the timing calculations and offset current control specifications. The deadtime was selected according to the worst case scenario according to (4.13) for the highest voltage and the lowest current. The lowest current is present in low power conditions, but as simulations showed, approximation by the offset current yields good results. Again a 50% margin was also added to compensate for miscalculations of the proper timings, losses in the system and uncertainties during the resonant process. All the above parameters are presented in the table below:

Table 4.2: Simulation Parameters

Parameter	Value
Input Voltage Range	20-52V
Output Voltage Range	32-52V
Offset Current	1.6A
Deadtime	100nsec
Switching Frequency/Period	100Khz/10μsec
Maximum Power	540.8W
Maximum Current	10.4A

First the validity of the ZVS modulations is going to be highlighted in the limits of the operating range with the 5Ω resistance with both the offset current control methods. In the following figure the switching of the converter and the inductor current, with the first control method can be seen:

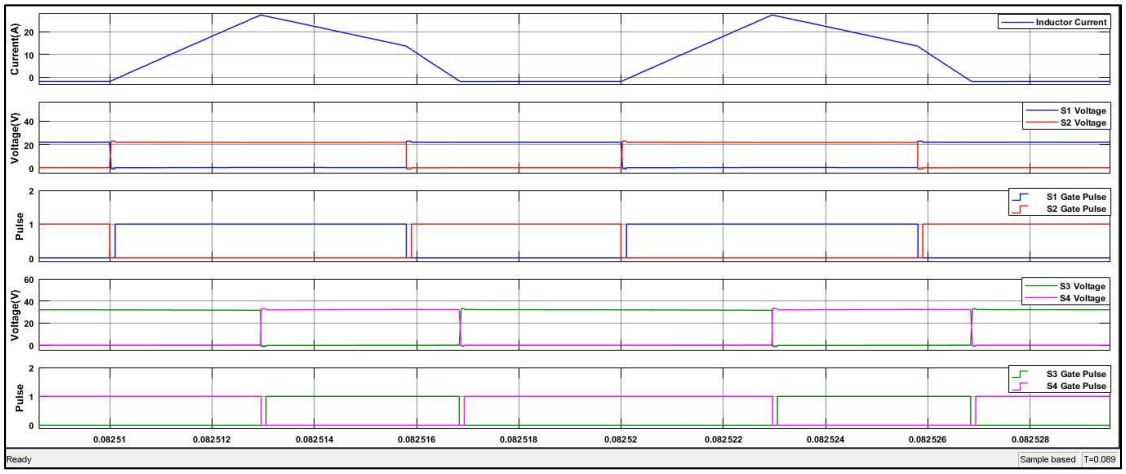


Figure 4.7: Vin=50V, Vout=32V, Power=204.8W

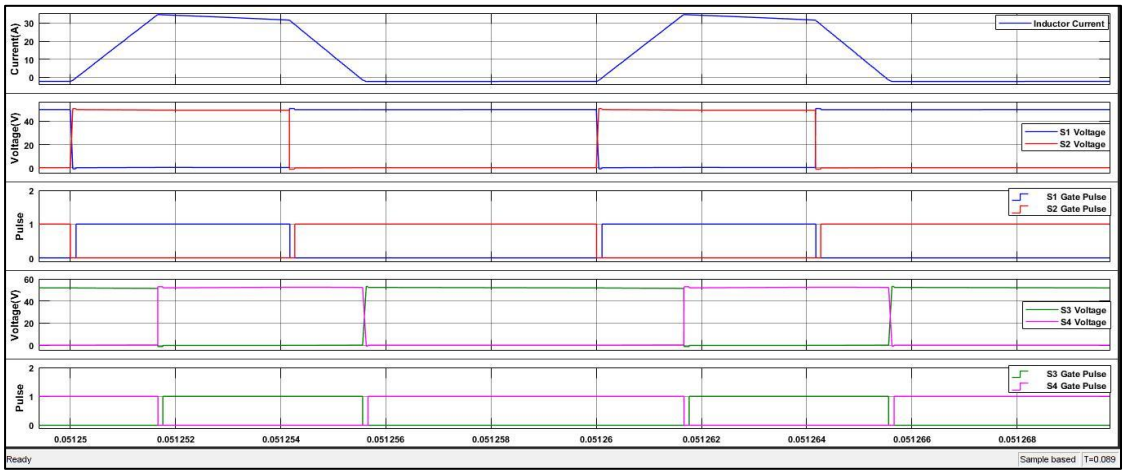


Figure 4.8: Vin=50V,Vout=52V, Power=540.8W

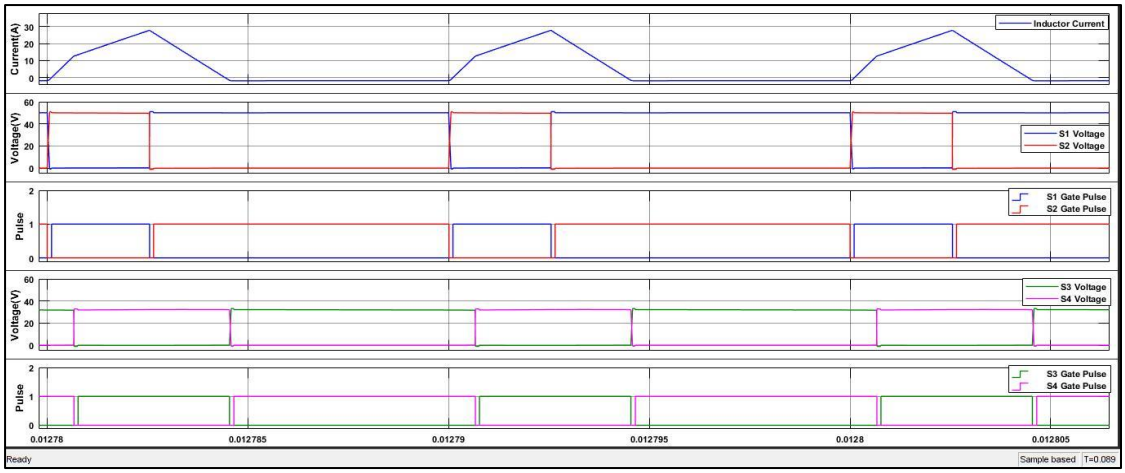


Figure 4.9:Vin=20V,Vout=52V, Power=540,8W

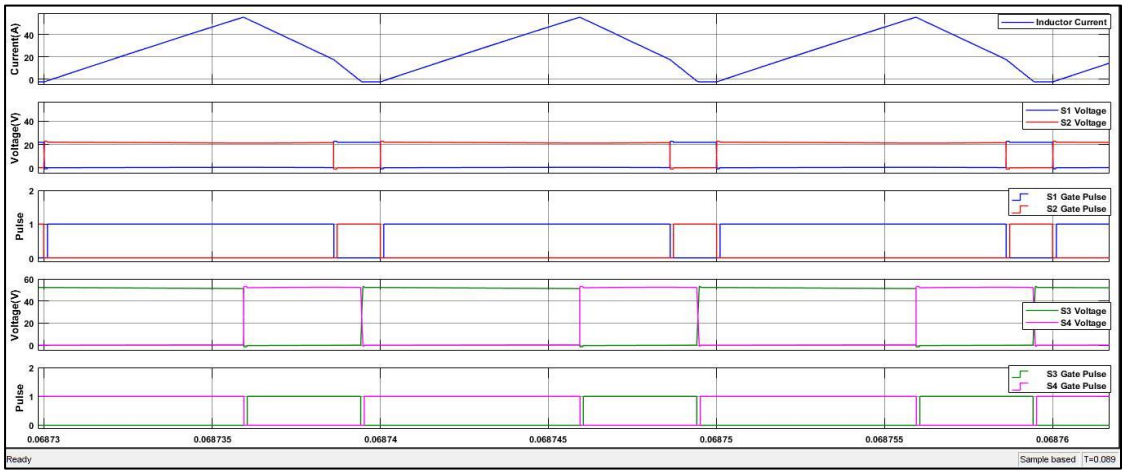


Figure 4.10: Vin=20V,Vout=32V,Power=204.8W

In the above figure all the limit cases for this situation are presented. We can see that in all situations, all switches switch on under ZVS. This is obvious since the voltage built in each MOSFET before it switches on, drifts to zero during the deadtime. When it reaches zero, the diode starts conducting. This is obvious from the drift of the MOSFET voltage below zero to $-0.9V$, which is the forward voltage drop of the diode. After the diode starts conducting then the MOSFET turns-on under ZVS. Soft switching is also attained for the turn off of the switches. As it can be seen from the figures, when the switch conducts the voltage is zero. According to the analysis of section 4.2, then it can turn off under ZVS. The capacitor delays the buildup of the voltage across the MOSFET, charging it while it discharges the capacitor of the complementary switch. It is obvious that S3 and S2 switches can use a lower deadtime, to decrease the conduction time of the diode, since the current at this point is higher than the offset current. But the deadtime is calculated based on low current or power conditions in the system, while here the minimum output current is 6.4A. One solution to that could be to implement a deadtime function based on the current measurement and voltage at the specific time but was not further investigated in this thesis, since the deadtime is still low for the worst cases.

The inductor current waveforms for various operations can be seen in the graphs below:

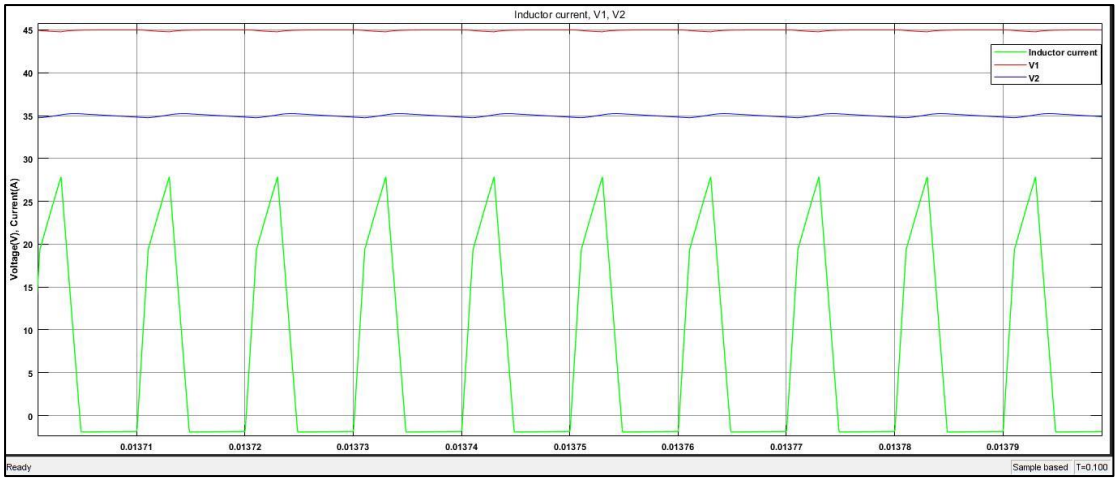


Figure 4.11: Buck stage Operation, Power=245W.

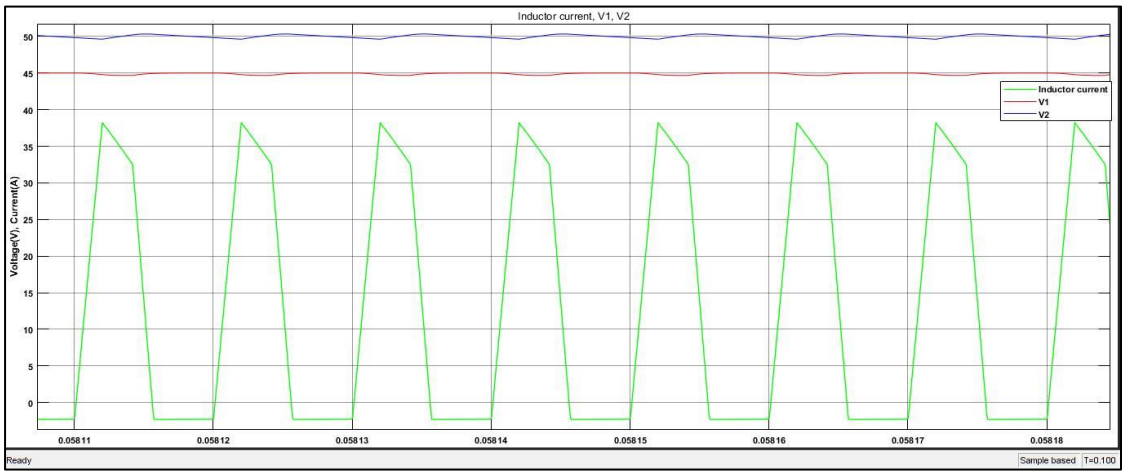


Figure 4.12: Boost Stage Operation, Power=500W.

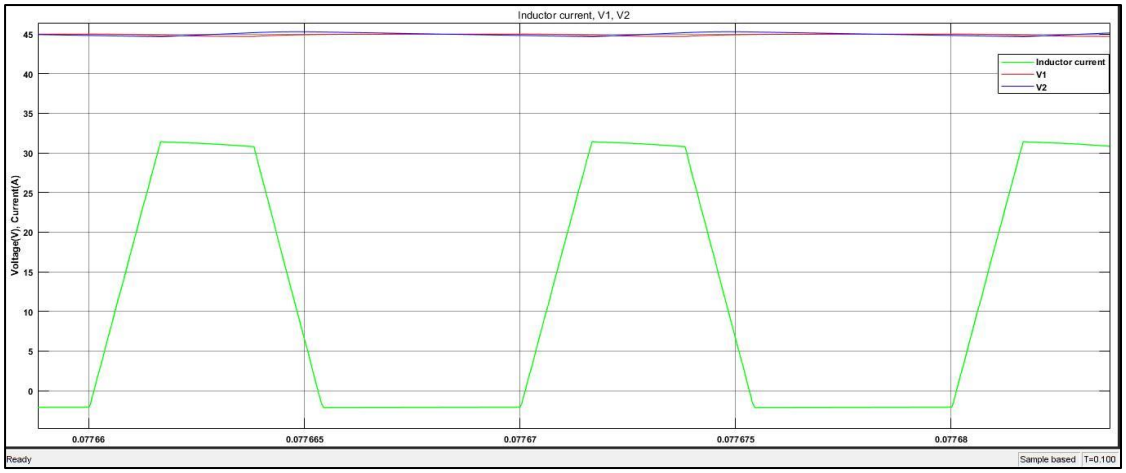


Figure 4.13: Equal voltages, Power=405W.

The inductor current waveforms follow the expected patterns. Both buck and boost stages of this control modulation are more advantageous than the pure buck or boost modes, since the power that can be transferred now is analogous to the area under the inductor current waveform, meaning that a wider area is utilized. Special note should be given to the case of figure 4.13, where the voltages are equal. This is a major advantage of this control method, since both buck

and boost control suffers when the input and output voltages are close. Here the transition between buck and boost mode can be made seamlessly as it will be shown.

Up to this point the simulations were carried under the first control method of the offset current as described in §4.3.2. The major disadvantage of this control of offset current can be seen in the figure below.

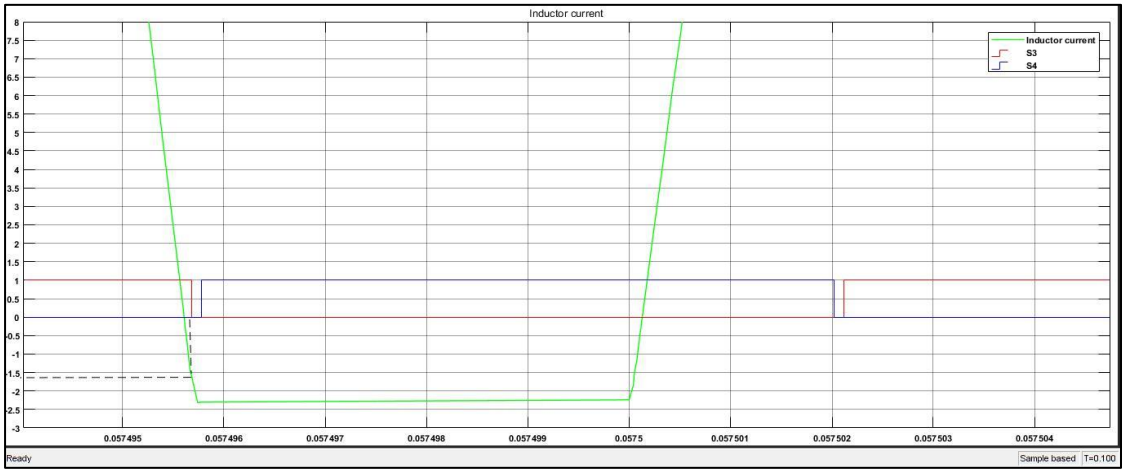


Figure 4.14: Offset current Drift below the minimum value.

We can see that although S3 switch is turned off at I_0=-1.6A, the current drifts below this value, since in the commutation interval the energy stored in the capacitors of S3 and S4 is transferred to the inductor, as i_L is discharging C_{oss4} and charging C_{oss3}. This offset current is more than enough to drive the ZVS of S1 the next period, but induces higher ohmic losses during $t_3 < t \leq T_p$ in the ohmic elements of the inductor and the MOSFETS. Higher voltages can lead to a drift well below this value. For this reason the second offset method as explained in §4.3.2 is implemented.

This offset control method is based on correcting the t_3 value in steps (S3 switch off), in order to attain the required minimum value of Io next period. In other words, based on the value of the current at specific points as explained in 4.3.2, t_3 is changed by a small step time next period, until the minimum required value of I_0 is attained. The proposed control method can be evaluated through the figures below.

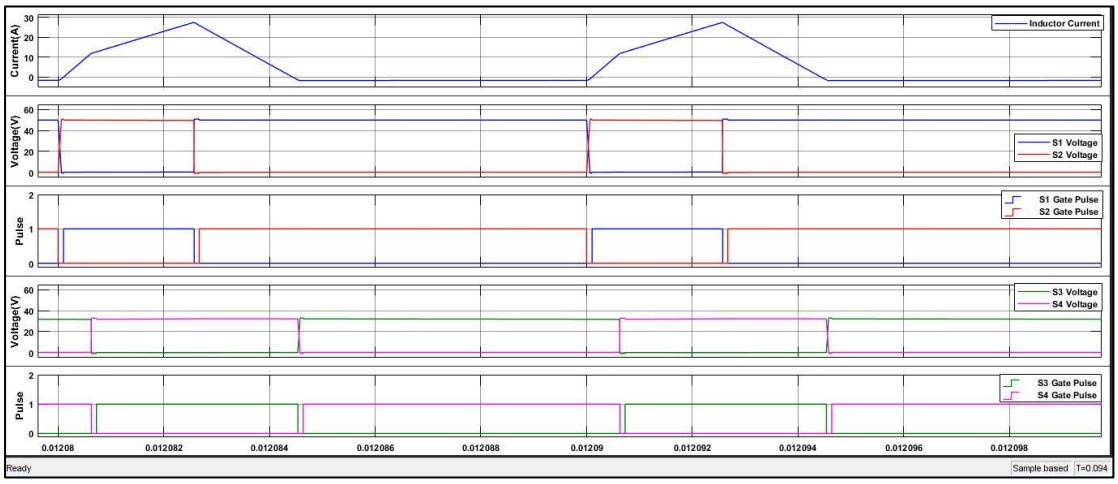


Figure 4.15: Vin=50V,Vout=32V,Power=204.8W

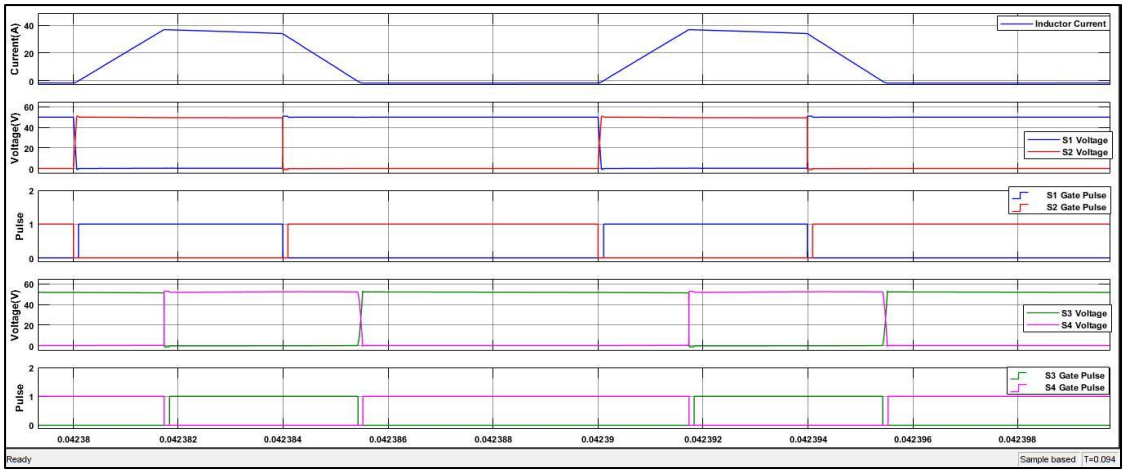


Figure 4.16: Vin=50V, Vout=52V, Power=540.8W.

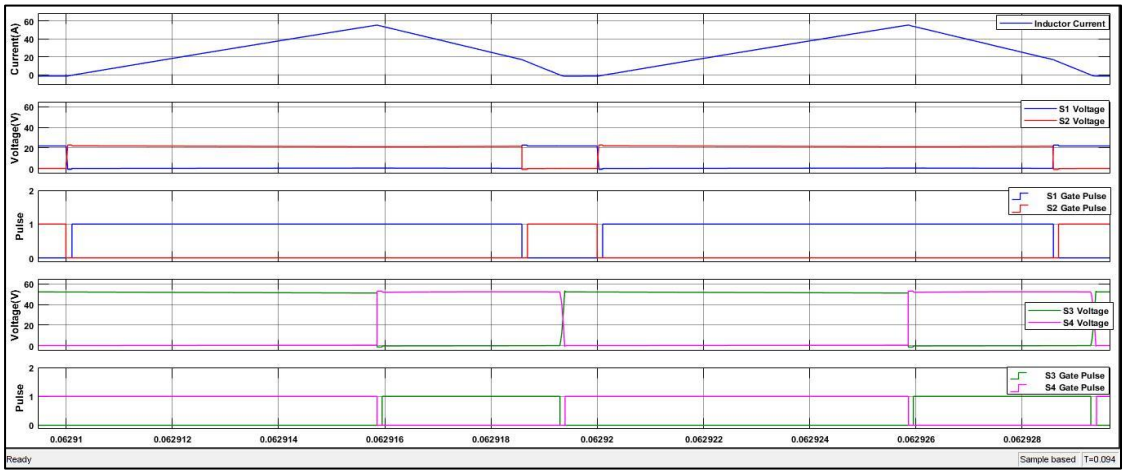


Figure 4.17:Vin=20V,Vout=52V,Power=540.8W

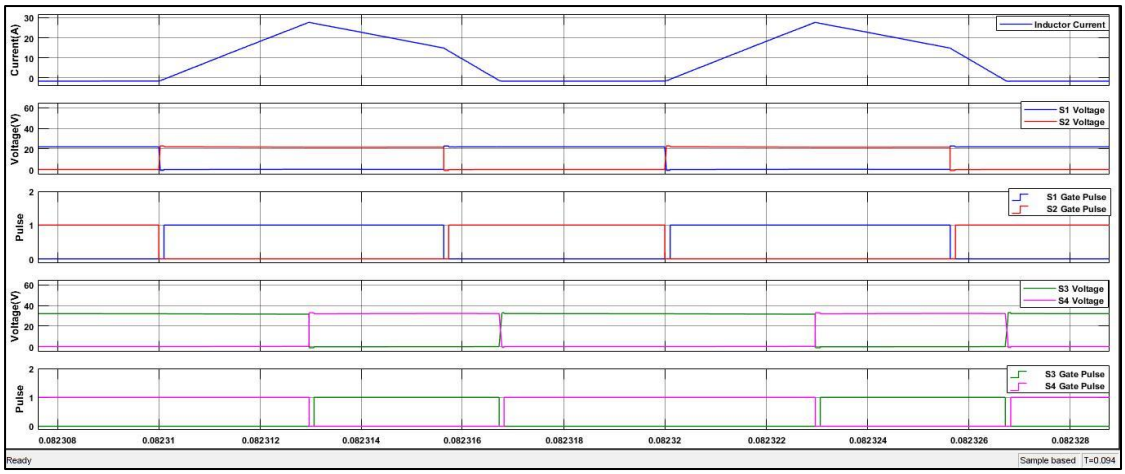


Figure 4.18: Vin=20V, Vout=32V, Power=204.8W.

Again the same behavior is attained as in the previous case. Soft switching conditions are ensured for all switches, both at turn on and turn off. Again the steady state operation of the converter can be seen below:

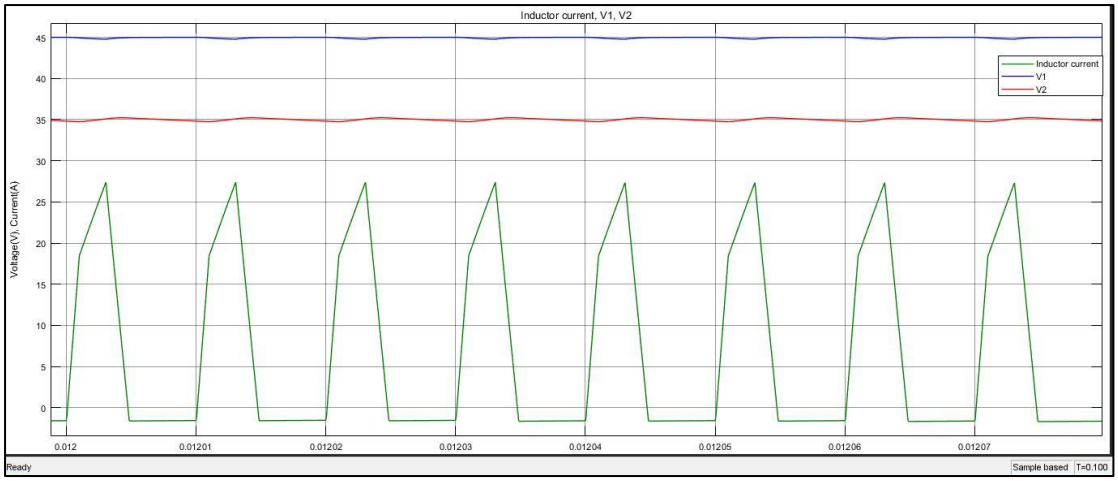


Figure 4.19: Buck Stage Operation, Power=245W.

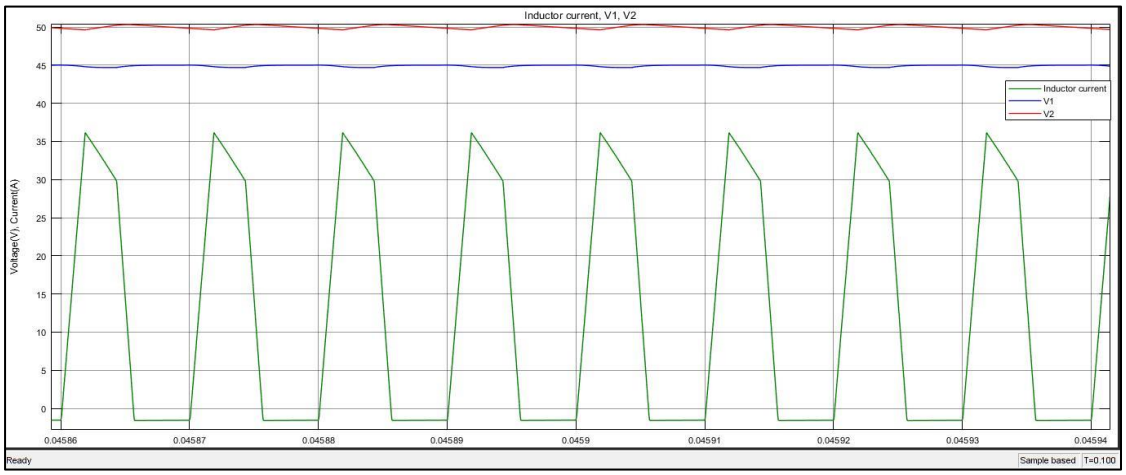


Figure 4.20: Boost Stage Operation, Power=500W.

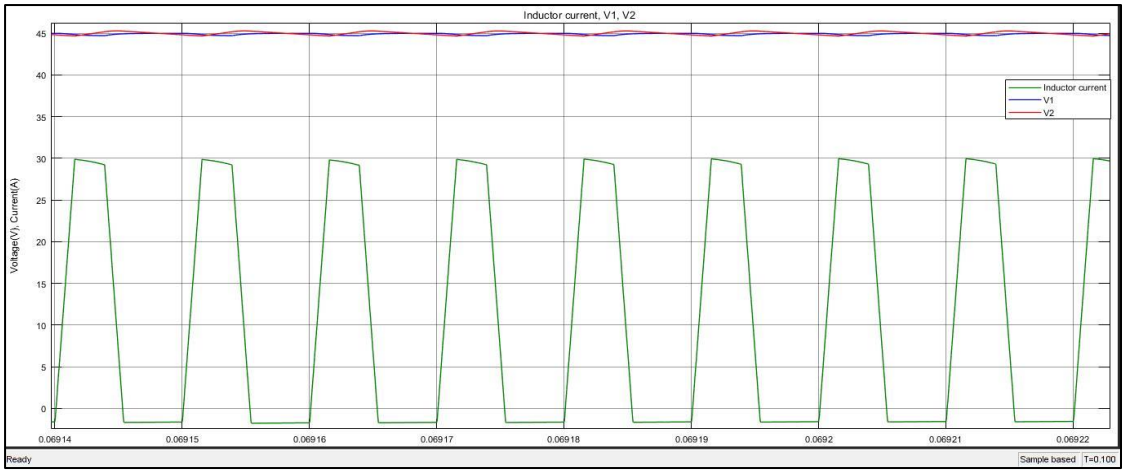


Figure 4.21: Equal Voltages, Power=405W.

It is validated that the converter operates as expected. The difference this time lies with the minimization of the offset current to the minimum value of -1.6A, as seen below:

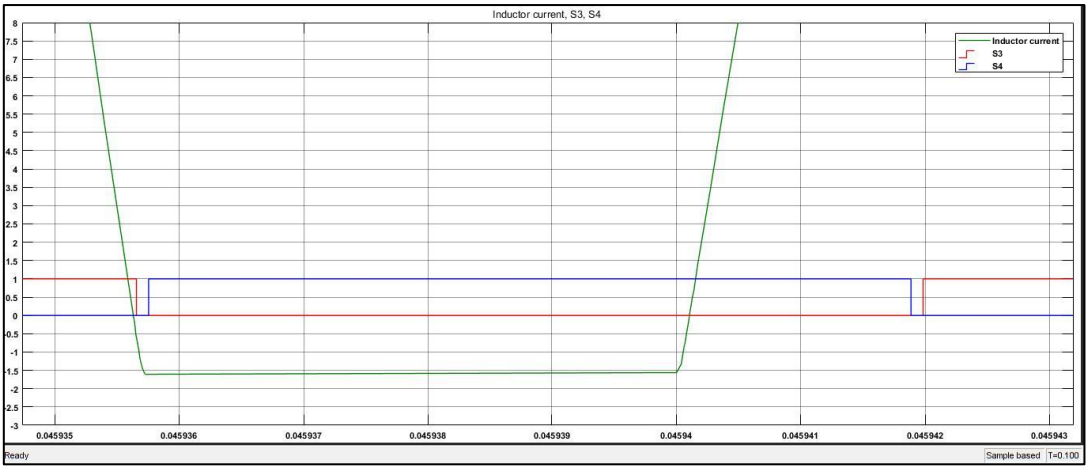


Figure 4.22: Offset current minimization

It is observed that in order to acquire the minimum offset value, switching-off of S3 is adjusted. S3 now switches-off under a lower absolute current value. But still ZVS of S4 is not violated, even for the worst case, since the deadtime is designed with respect to the worst case scenario, that the current at t_3 is very small or even zero. If it is positive though, it means that the diode of S3 conducts, until i_L reaches zero, increasing the voltage due to its forward drop value and the charging and discharging of the capacitors cannot start until i_L<0.Thus a portion of the deadtime is not used to begin the commutation interval. This situation may occur during transitions, where the minimum value of I_0 is not reached. If i_L is positive meaning the diode conducts and the offset current is higher than the absolute of the minimum required, then t_3 is adjusted to increase more rapidly, while the deadtime increases to account for this lower minimum current. This is the equivalent of a function to adjust deadtime according to operational conditions.

This algorithm offset current control is setting the steady state value of the offset current to its minimum required value sufficiently well, but due to the small step change that is applied every period is slower to responses during transients, in regard to the first control method and therefore the current during transitions may drift well below –Io increasing ohmic losses. The first control method though is faster and although Io may drift below Io minimum, this value will be attained for sure. So a combination between the two methods will increase both steady state Io control and lead to better dynamic behavior.

These considerations are highlighted in the figure below:

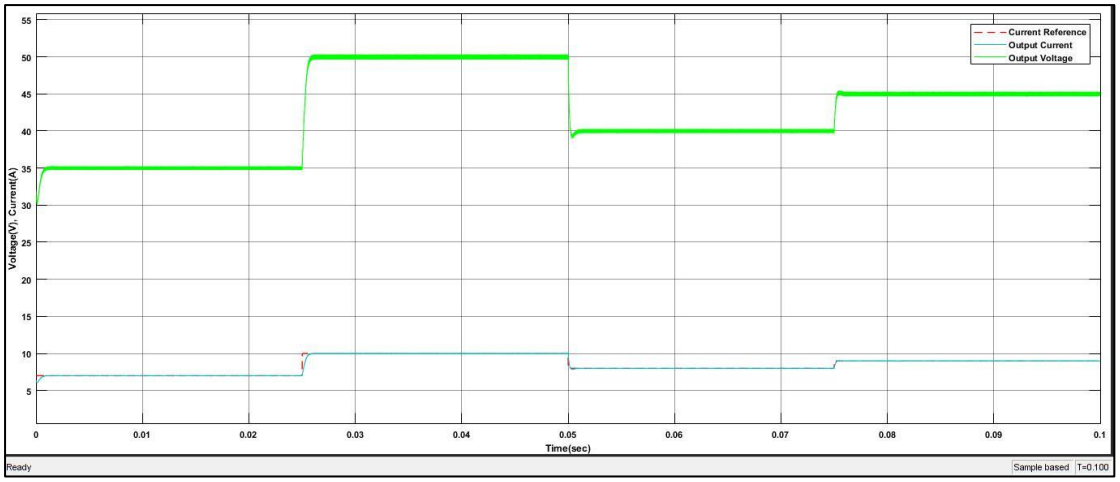


Figure 4.23: Reference Tracking

In the above figure the control response to changes in the reference value is given. Operational conditions change and transitions between modes take place. The question here is the dynamic behavior of the converter's total control loop. We can see from fig. 4.23 the total control loop of the output current PI and the algorithm, as visualized in fig. 4.6, assumes the desired values fast and with now overshoot or oscillations. At 0.025sec the controller switches from buck to boost mode. The question now shifts to whether offset current and ZVS is retained. This can be extracted by the following figures (fig 4.24 and 4.25).

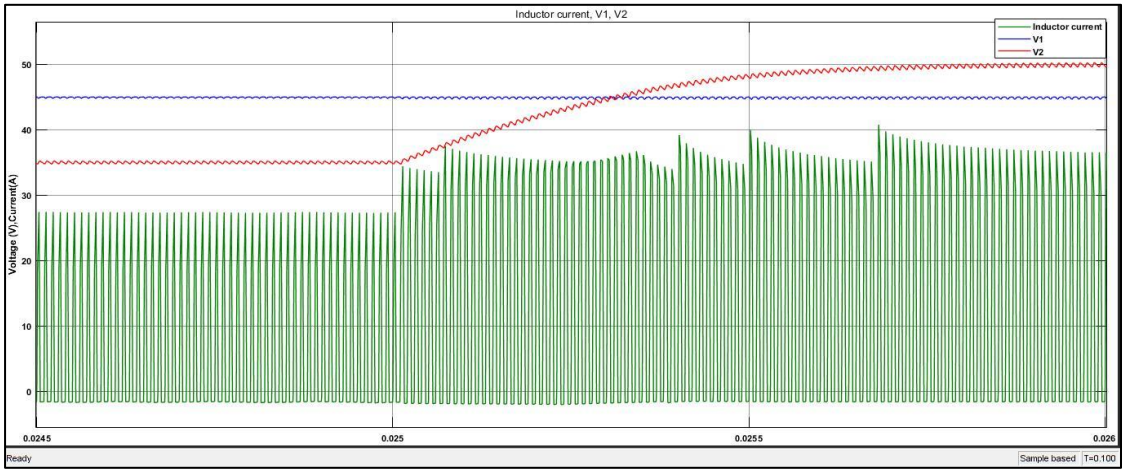


Figure 4.24: Buck to Boost Transition: Inductor Current

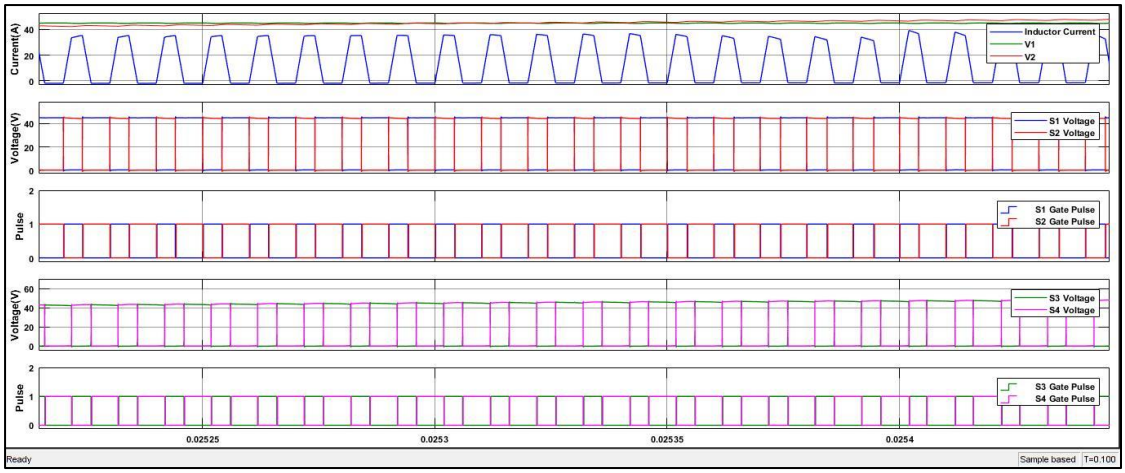


Figure 4.25: ZVS during Buck to Boost Transition

As can be seen above during this transition from buck to boost operation, ZVS is ensured and the offset current attains the minimum offset value quite fast.

Same arguments hold true for the transition taking place at 0.05sec from boost to buck operation. Here the controller increases both the deadtime and t3 value rapidly to account for the positive inductor current, when S3 switches off if that is necessary:

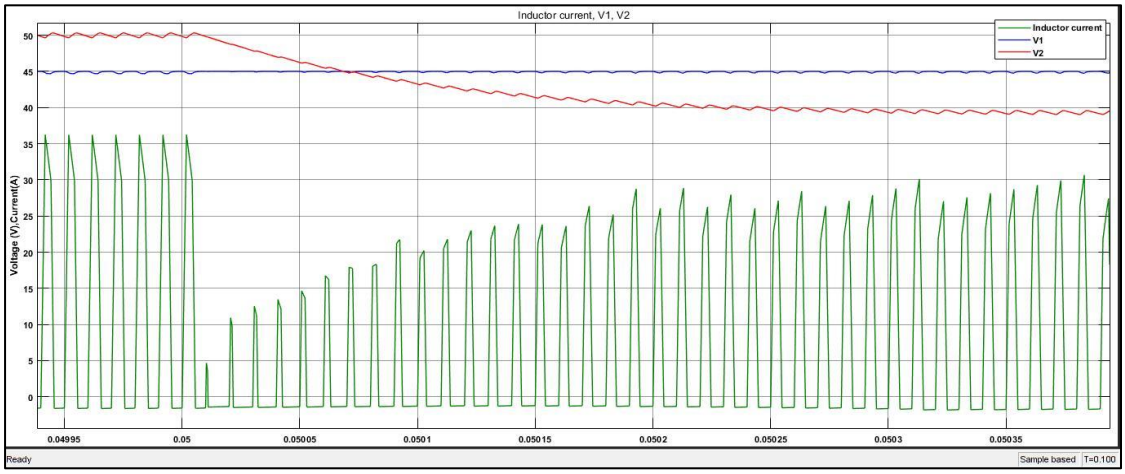


Figure 4.26: Boost to Buck Transition: Inductor Current

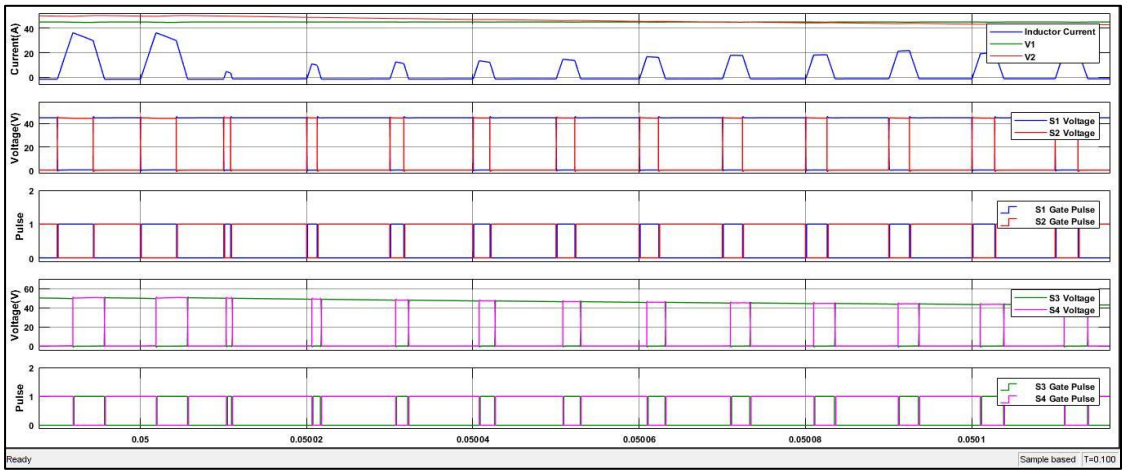


Figure 4.27: ZVS for Boost to Buck Transition

In both transitions between modes of operation the dynamic behavior of the whole control scheme to variations in operational conditions is validated. Not only the control works fast and without stability issues but also ZVS is retained in all cases in these nominal power conditions.

4.4.2 Low Power Condition

The above study case simulated the system under the nominal voltage ranges for sufficient amount of power. But we also need the converter to achieve soft switching in these voltages even at very low power conditions. For this reason a simulations will be carried out at low output current of 0.1A, and therefore power as low as P=3.2W at the lower voltage range. This will be useful as this converter is going to be used in a DCMG where low values of current and transferred power are attained.

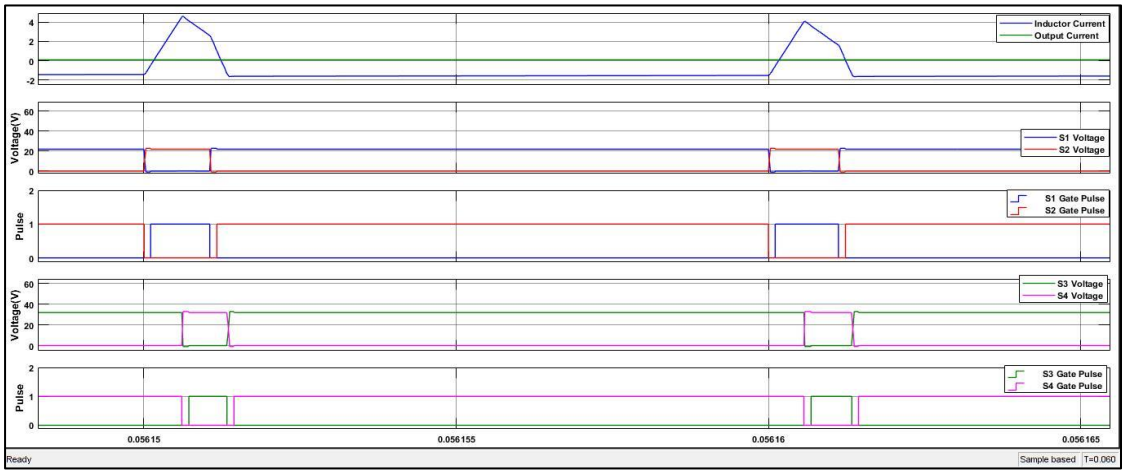


Figure 4.28: Vin=20V, Vout=32, Power=3.2W

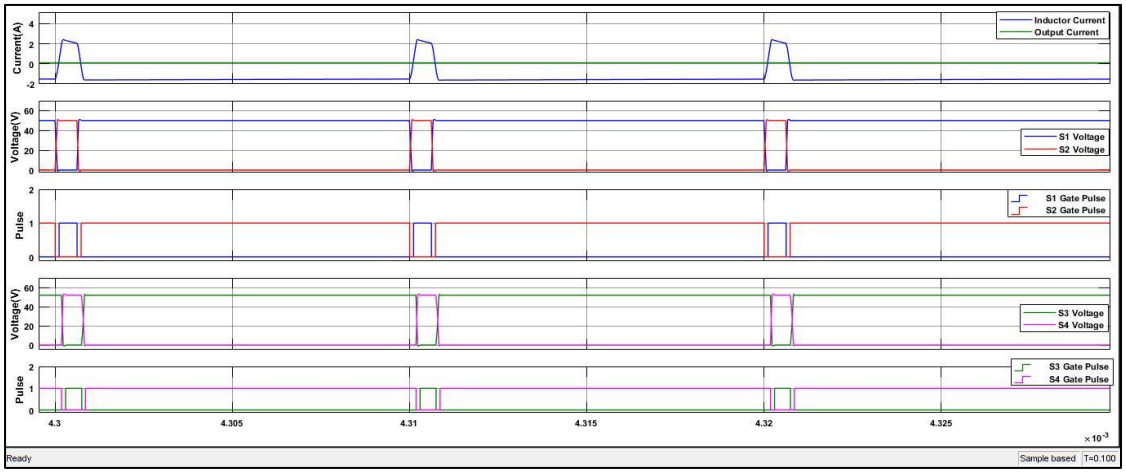


Figure 4.29:Vin=50V, Vout=52V, Power=5.2W

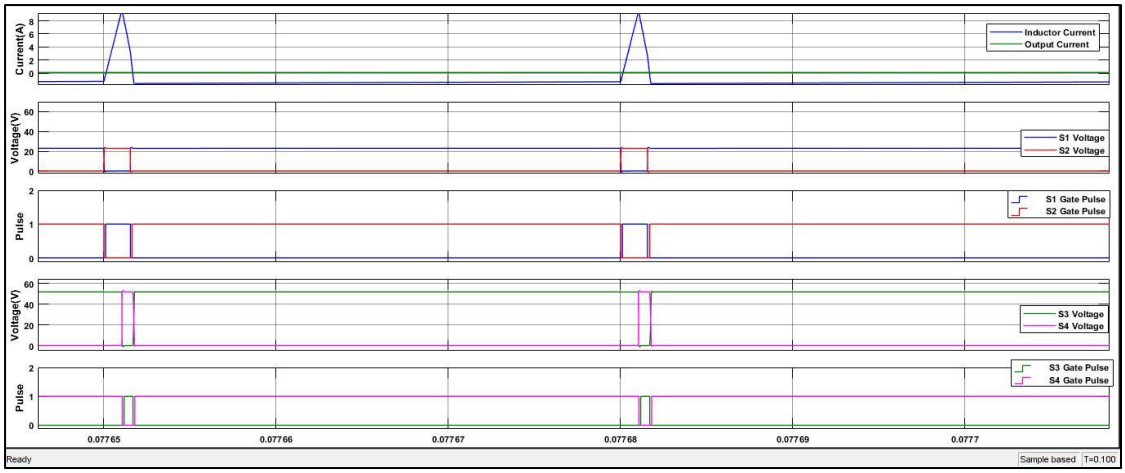


Figure 4.30: Vin=20V,Vout=52V, Power=5.2W

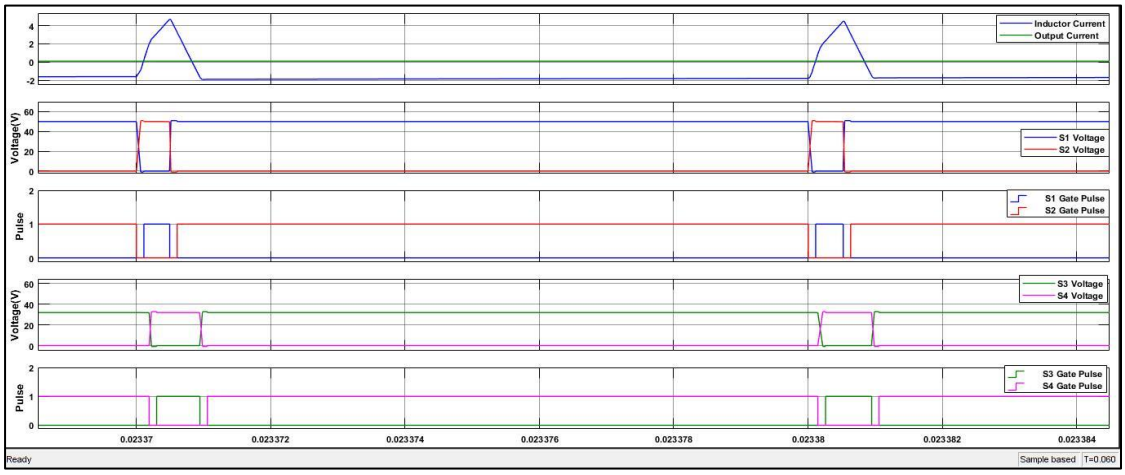


Figure 4.31:Vin=50V,Vout=32V,Power=3.2W

We can see from the above that even for a very low current of 0.1A which corresponds to a low power output of 3.2W-5.2W, soft switching of every switch is assured in every limit condition of the control modulation unlike to standard ZVS techniques, where ZVS is not achieved at low power conditions [17]. The usefulness of deadtime implementation for the worst case scenario is seen here, where I_1 and I_2 have low values comparable to the offset current value.

4.4.3 Cooperation with Buck operation for startup.

In the previous simulations the output capacitor was considered initially charged to the operating voltage range. The algorithm was implemented for specific voltage ranges and not for startup operation, where output voltage is zero. For this reason, the buck operation and control, as described in the previous chapter, is going to be employed to startup the system from zero voltage up to the minimum output voltage of 32V. As soon as this value is achieved then the control switches to the ZVS modulation control.

Thus a combined control method was implemented which combines the above mentioned operation and is shown in the figure below:

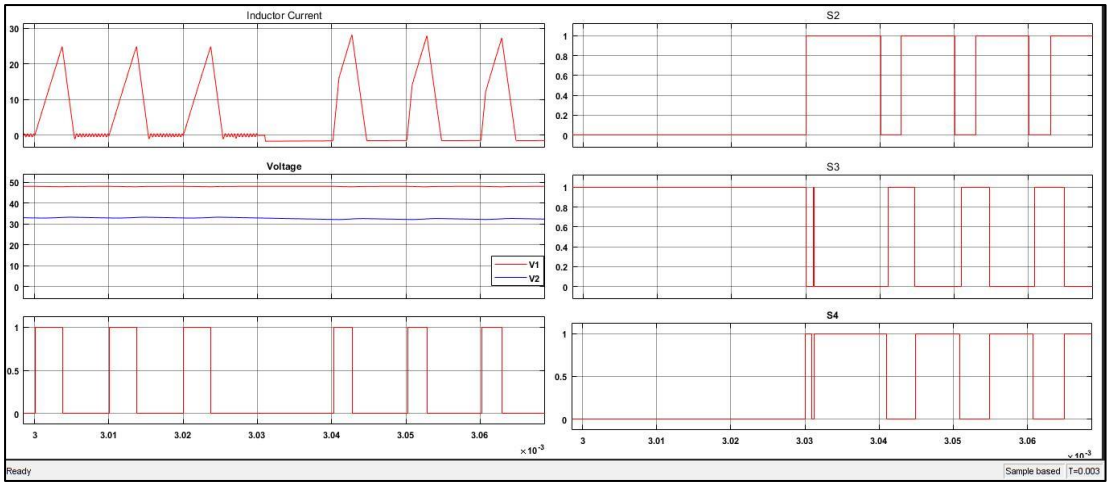


Figure 4.32: Transition Between Buck Operation for start-up and ZVS nominal operation.

As can be seen from the figure, between the two modes of operation a special signal is applied on S3 to decrease the current to the minimum offset current so the ZVS modulation strategy can start under ZVS immediately for the first switch. Also it is obvious that bumpless control transfer between the two modes is achieved through proper implementation of PI tracking.

4.5 Bidirectional Mode of Operation.

The cascaded buck and boost converter can be used to transfer power in both directions. This is necessary if this converter is to be used as a universal converter for the DCMG since it can support then charging and discharging storage operation.

When the power direction changes the gate signals of the two half bridges of the converter must be exchanged and the mode of operation must change from buck to boost or vice versa since now the input side becomes the output side. More specifically since now the voltages input and output have switched sides, S1-S3 and S2-S4 are exchanged respectively.

To attain ZVS when the power direction reverses, a special modulation signal for the inductor current must be introduced in a period before the direction change takes place. Since the reversion of power transfer is denoted by a negative current, now during this special modulation period, the offset current must swift from $-I_0$ to $+I_0$. For this reason the input voltage V_1 must be applied on the inductor for time $t = 2 \times I_0 \times L/V_1$. As soon as the value of $+I_0$ is attained, S2 and S4 are switched on and in the next period ZVS can be ensured [17]. The previous procedure is highlighted in the figure below:

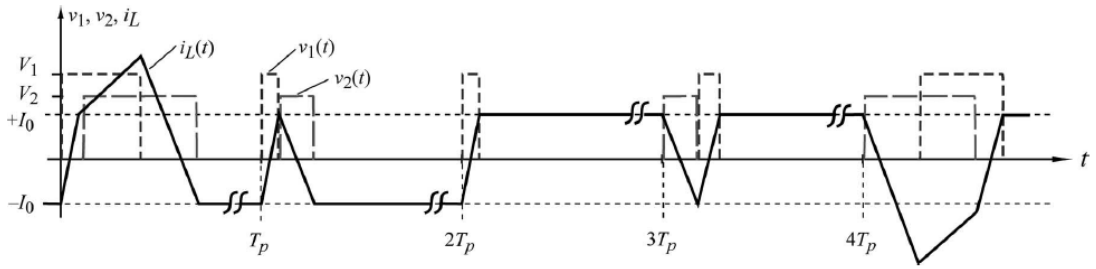


Figure 4.33: Special Modulation of the Inductor current for Power direction Change [17].

As it can be seen at $2T_p < t < 3T_p$, S1 is switched as long as needed to attain the positive value of the offset current, and then S2 and S4 to allow for I_0 to circulate in the circuit and enable

soft switching next period. The operation also changes from buck to boost as now the input-output ports have been exchanged.

The above sequence was implemented in this thesis to allow bidirectional power conversion as well as soft switching. The offset current control methods were also adopted to fit the negative direction of the current. Also the PI controller gains are shifted to negative values to compensate the negative current controlled, when the power direction changes and to maintain universality of the algorithm method. To test the bidirectional mode the current reference of the output current is changed from 2A to -2A at 0.03s and back to 2A at 0.06s as seen in the following figure:

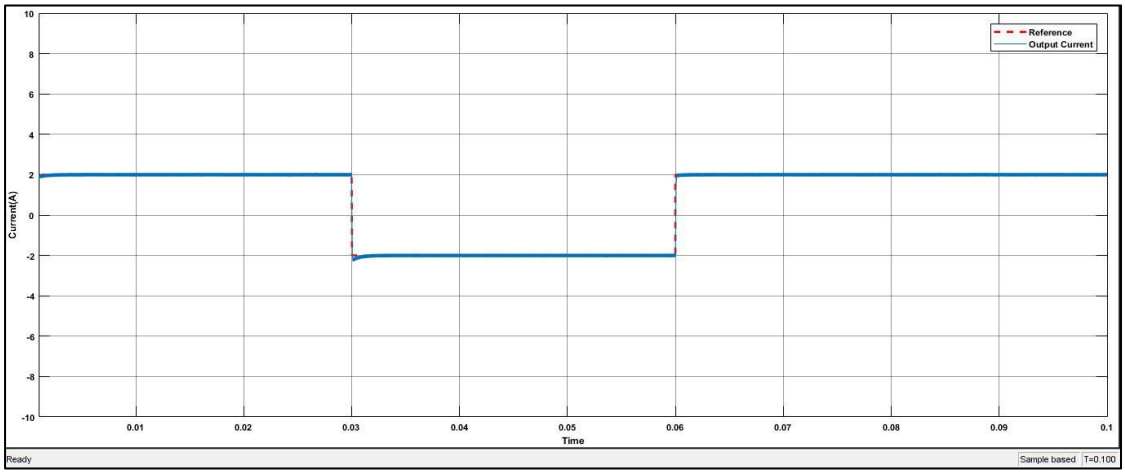


Figure 4.34: Reference Tracking of the Bidirectional Converter.

The control responds fast to the reference change and the current and therefor the power direction reverses. A close up of the inductor current during the transitions is shown below:

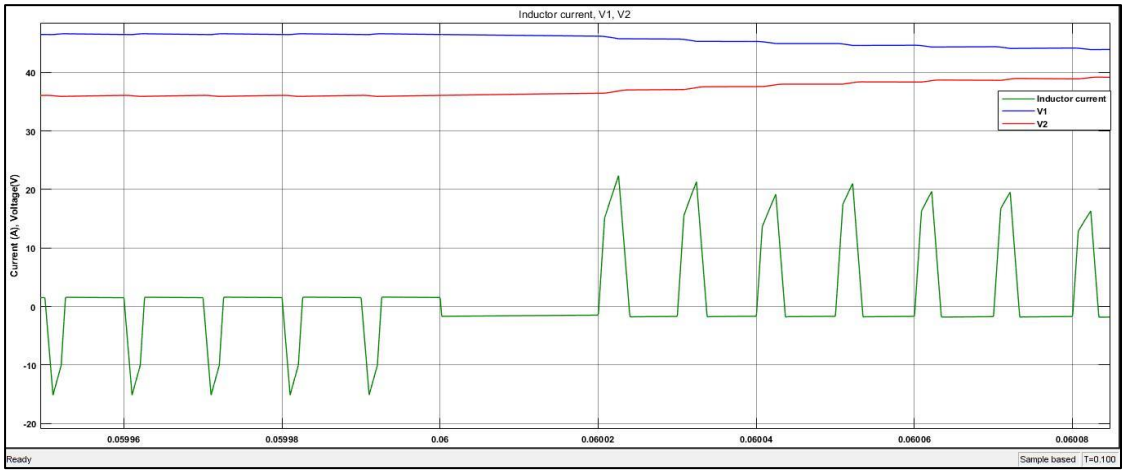


Figure 4.35: Inductor Current during Power direction Reverse (2A/-2A)

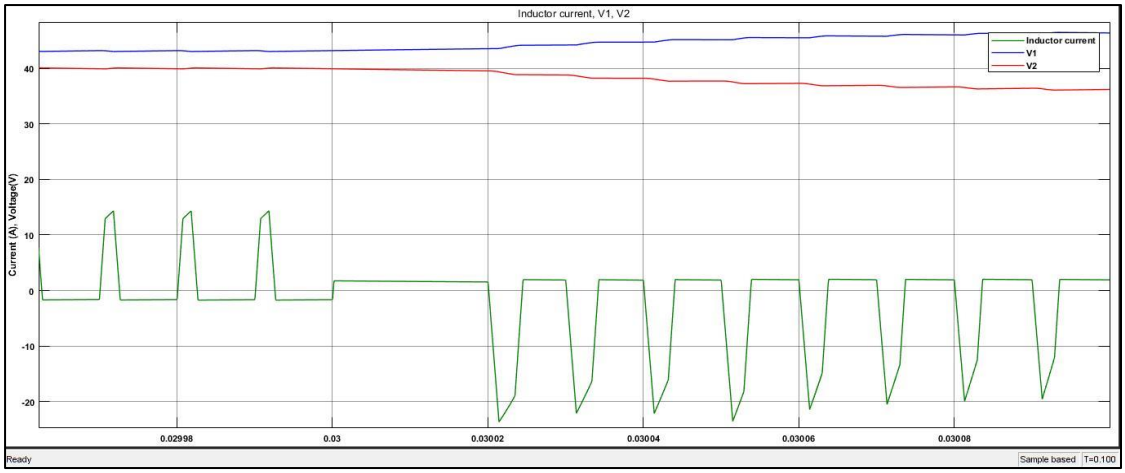


Figure 4.36: Inductor Current during Power direction Reverse (-2A/2A)

We can see that during transitions the offset current changes polarity when the power direction changes. More specifically from figure 4.35, it is observed that the offset current shifts during the transition from -1.6A to 1.6A, while from figure 4.36, the opposite shift is seen. Another significant note is that the input and output port voltages reverse, so the converter and thus the inductor current waveform shifts from buck to boost operation in figure 4.35 and vice versa in figure 4.36. The switching during both power direction reverses can be seen in the figures below:

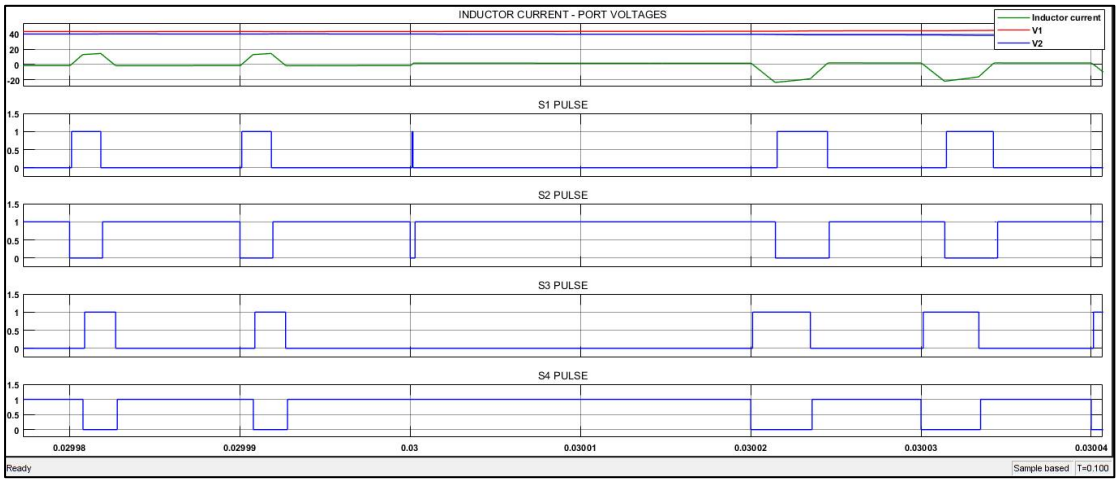


Figure 4.37: Switching during Power Direction reverse (2A/-2A).

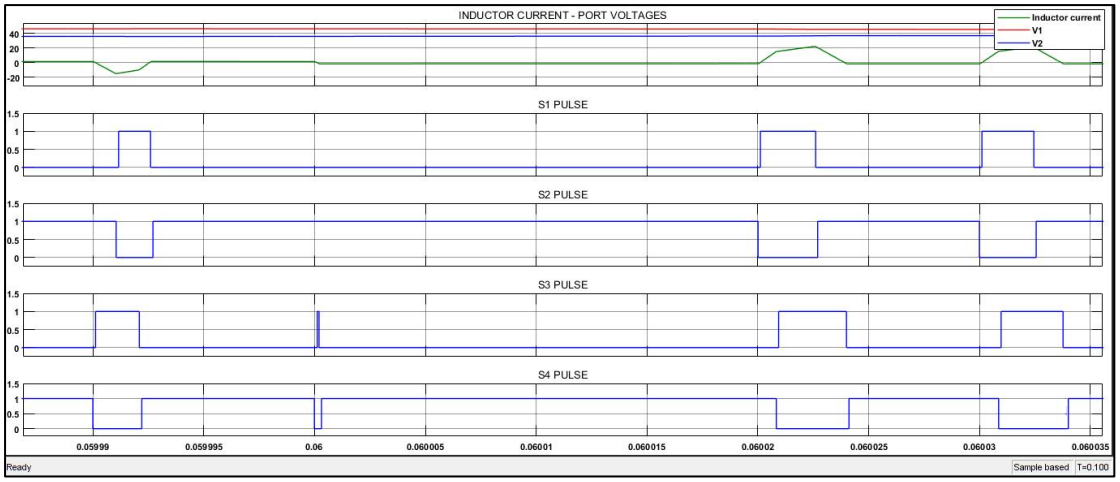


Figure 4.38: Switching during Power Direction reverse (-2A/2A).

From figure 30, during current direction change from 2A to –2A at 0.03, we see that S1 is switched on for $t = 2 \times I_0 \times L/V_1$, to allow for Io to reach 1.6A. Then S2 and S4 are switched on and ZVS of S3 next period is ensured. In figure 31, the reverse procedure is followed. S3 is now switched on for $t = 2 \times I_0 \times L/V_2$, since now V_2 is the input voltage for the converter. After the inductor current reaches the negative offset value of -1.6A, S2 and S4 are switched on to allow the offset current to circulate in the circuit and allow ZVS of S1 next period. The validation for the ZVS is shown in the next figure:

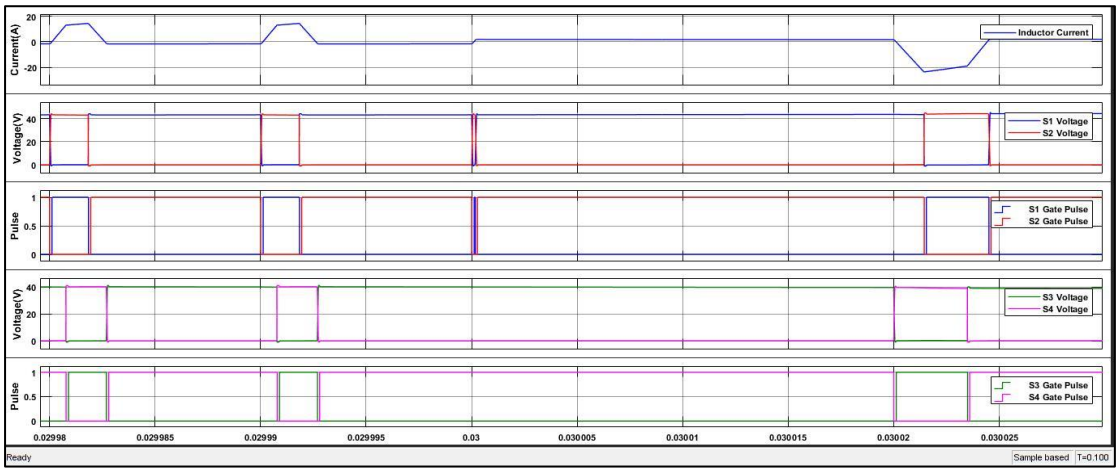


Figure 4.39: ZVS during Power Direction Reverse

We can validate that S3 switches on under ZVS immediately after the power direction reverses, since S3 voltage drifts to zero before S3 turns on. This can be highlighted more closely in the following figures:

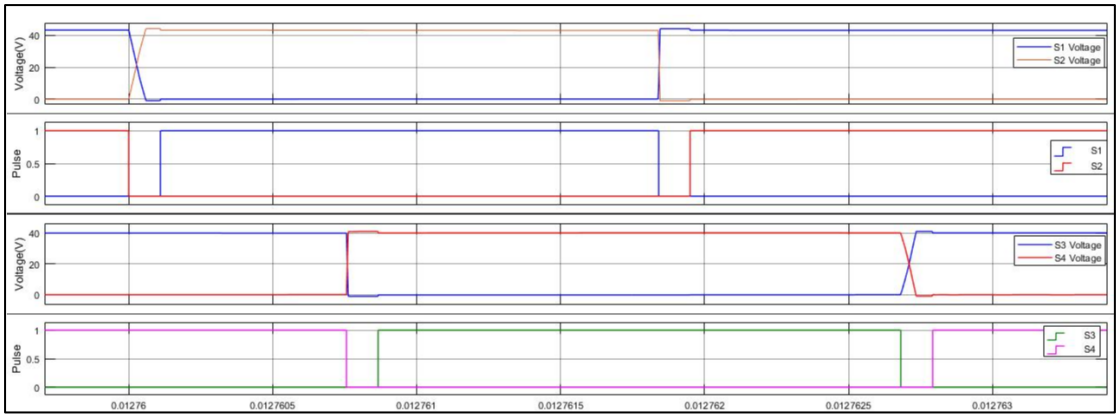


Figure 4.40: Close Up of ZVS during Buck operation (2A).

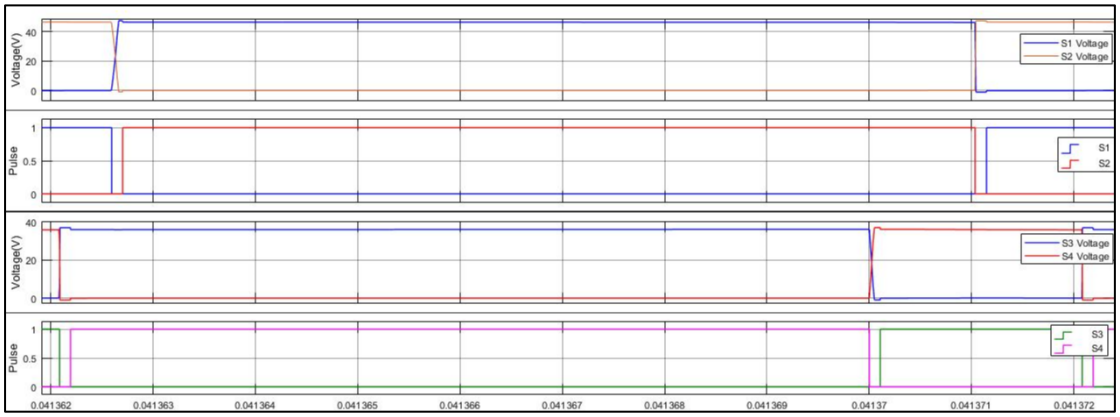


Figure 4.41: Close Up of ZVS during Boost Operation (-2A).

In the above figures the ZVS of buck operation of the converter, which coincides with the 2A of the previous example and the boost operation, as in -2A, are shown with more detail. It is obvious that each switch turns on under ZVS, since the antiparallel body diode has turned on. This is highlighted by the voltage drop below 0 by 0.9V, which is the diode forward voltage drop. Also during turn off the voltage is slowly built across each switch as expected by the operation. These figures highlight the successful operation once more. One note should be given to the quite long conduction of the diode. The switches could be turned earlier. This though is done due to the fact that the deadtimes are calculated for the limits of the voltage and power limits. A deadtime function based on the voltages could be a good improvement.

This paragraph not only demonstrates the suitability of the converter and the control scheme for bidirectional operations but again verifies the stability and fast control operation of the control under dynamic conditions. With this consideration in mind the converter can be used for power balance control in LVDC networks as will be discussed in the next chapter.

5 Control Operations in a LV DC microgrid

In the previous chapters the low level control of the cascaded buck and boost converter was designed, implemented and evaluated. In this chapter the converter will be evaluated and used in the context of the DCMG control operations. An islanded 48V- DCMG consisting of a PV panel, a storage-battery and a DC load of LED lights will be implemented. All components are connected to the common DC bus through the cascaded buck and boost converter under the CF-ZVS modulation analyzed and implemented in the previous chapter. This DCMG can be used to provide lighting in streets, houses or office applications without additional protection schemes as presented in chapter 2. The structure of the DCMG is shown in the figure below:

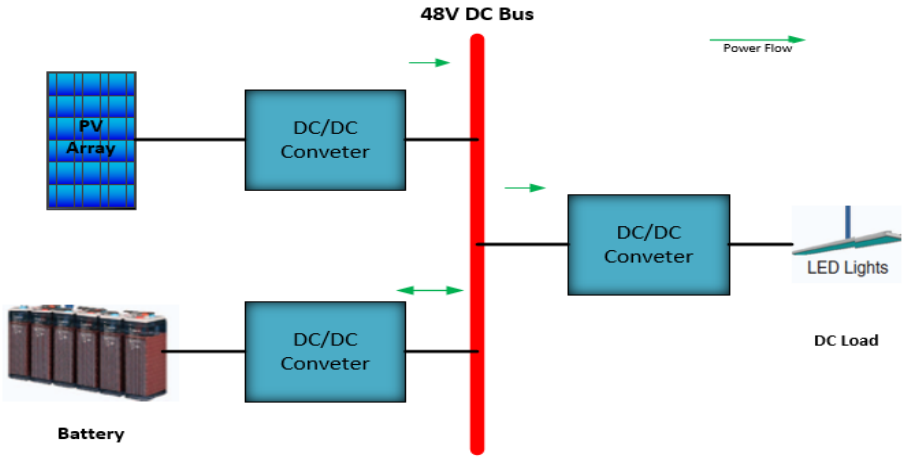


Figure 5.1: The studied 48V DC Microgrid.

As discussed in Ch. 2, power balance must always be satisfied in a DCMG and especially an islanded one, where support from a large grid doesn't exist. Power balance can be realized by voltage regulation of the common DC bus. One of the most popular ways for voltage regulation and power balance is droop control.[3], [26], [59]. Battery usually assumes control of the voltage through charging and discharging operations[3], [36]. Renewable energy sources should be operated in MPPT to extract the maximum amount of power available [3], [36], [60]. As long as one source converter assumes the control of the dc bus voltage all other converters can be operated in Constant Power mode [59].

But in isolated systems the power produced by RES should be monitored to prevent overcharging of the battery system. Batteries usually come along with specific charging and discharging power limits adding complexity to the control of the DCMG[35], [60]. When necessary RES converters can also droop to decrease power and assume command of the voltage in case of battery inability to regulate it instead of switching off[36]. Apart from the sources issues, DC loads with tightly controlled converters usually behave as constant power loads (CPL). CPL introduce instability to the system[37]. Finally, in order to facilitate demand response, since we saw it is an advantage of DCMG, load could be also dimmed, as in the case of LED lighting, instead of switching off [36].

To address these issues originating from the nature of the components and the parallel connected DC converters, a decentralized primary controller consisting of the control strategies mentioned above will be analyzed and implemented to allow for power balance and stabilization of the DCMG[36]. This hybrid balance controller (HBC) satisfies the need for good control, low costs and maintenance and universal plug and play capabilities and it will be tested under various scenarios. Models for the PV, Battery and LED light will be constructed. Finally cooperation between the converter low level control (CF-ZVS-M) and the DCMG aforementioned primary controller (HBC) will be highlighted.

5.1Hybrid Balance Controller

The Hybrid balance controller consists of three common controllers commonly used: a constant current control setting the output current limit described by:

$$I = I_{max} \tag{5.1}$$

a droop control for voltage regulation and power flow control described by the droop equation:

$$V = V_{ref} - I \times R_{droop} \tag{5.2}$$

Where V_{ref} is the desired voltage output of the converter, usually its nominal voltage output, and R_{droop} the virtual resistance/droop coefficient of the droop control mode.

Finally, a constant power control describing the constant power loads and MPPT operations of RES is also utilized, denoted by:

$$P = V \times I \tag{5.3}$$

All these different controllers combine to create the Hybrid Balance Controller as seen in the figure below:

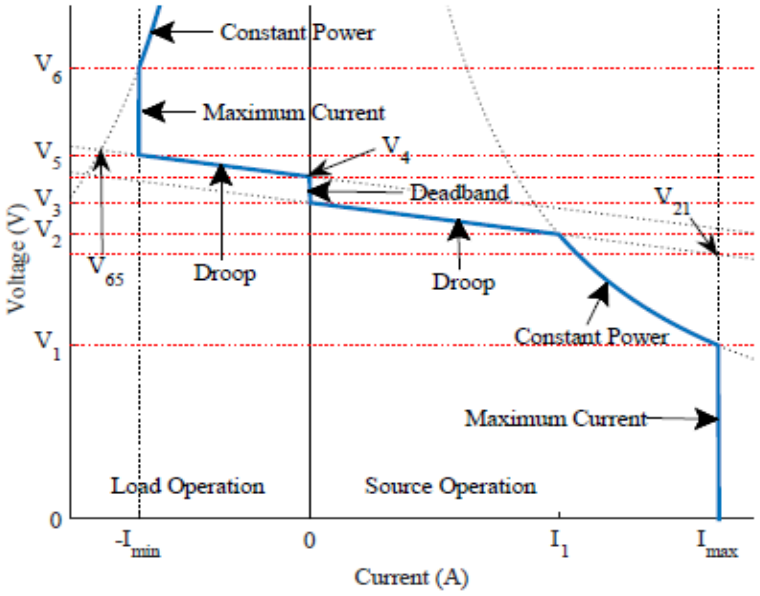


Figure 5.2: Hybrid Balance Controller Voltage set-points for selection of Control Mode[36].

The control mode is based on the output voltage measurement of each converter. The right half-plane denotes the operation of the converter as a source, while the left one describes the load operation of the converter. The operating ranges of each control mode are created by some voltage set-points denoted by $V_0 - V_6$ and two special condition voltage set-points denoted by

V_{65} and V_{21} as seen in figure 5.2, which are the intersection points between the different control modes.

More specifically in the range of $0 \leq V \leq V_1$ the controller sets the converter in constant current mode meaning that converter operates in the maximum allowed current. Voltage set-point V_1 is the intersection between constant current and power regions and can be found by equalizing equations (5.1) and (5.3):

$$V_1 = \frac{P_{max}}{I_{max}} \tag{5.4}$$

In the next region $V_1 \leq V < V_2$ the converter operates under constant power. This constant power depends on the maximum available power generated by the source at a specific moment. The upper voltage limit of V_2 is the intersection between the Constant Power control region and the droop control and can be found by eq. (5.2) and (5.3):

$$V_2 = \frac{V_{ref} - \sqrt{V_{ref}^2 - 4 \times P_{max} \times R_{droop}}}{2} \tag{5.5}$$

Then the control for $V_2 \leq V < V_3$ shifts to droop control. As voltage increases, current decreases. At V_3 the current is set to zero and is given by (5.2):

$$V_3 = V_{ref} \tag{5.6}$$

which is the nominal output voltage or , in other words the maximum allowable voltage for this source converter, when the current becomes zero.

Under certain conditions like low power, the Constant power conditions may not be met. In this case the control swifts directly from constant current mode to droop control mode. This special condition is defined by V_{21} in figure 5.2. Two new voltage ranges describe the hybrid balance controller in source operation now: $0 \leq V \leq V_{21}$ for constant current mode and $V_{21} \leq V < V_3$ for droop control mode. This condition is true if $V_{21} > V_1$. The voltage set-point V_{21} is given by (5.1) and (5.2):

$$V_{21} = V_3 - I_{max} \times R_{droop} \tag{5.7}$$

Similar arguments hold for the load operation of a converter. In the range of $V_4 \leq V < V_{65}$ as can be seen in fig. 5.2, the converter operates in droop control mode. This is the case when the loads can be throttled or dimmed like LED lighting load, instead of being switched off. V_4 is the voltage of the load converter, when the current is zero. In other words, it is the minimum allowable voltage for the operation of the load converter. The upper limit V_{65} is the intersection between the droop control region and the Constant Power mode of the load converter. This is given again by (5.2) and (5.3):

$$V_{65} = \frac{V_{ref} + \sqrt{V_{ref}^2 - 4 \times P_{max} \times R_{droop}}}{2} \tag{5.8}$$

Where P_{max} and R_{droop} now refer to maximum load power (negative value) at the specific time and load droop coefficient respectively. From this voltage set point and above, $V \geq V_{65}$, the load operates under constant power continuously, which is usually the required.

As in the source operation the constant power condition may not be met. This is the case of high power needs. In this case the control shifts from droop control to constant current mode. This case is denoted by the voltage set-point of V_5 and is given by (5.1) and (5.2):

$$V_5 = V_{ref} - I_{max} \times R_{droop} \tag{5.9}$$

where I_{max} is the maximum negative current (load current) allowed by the load converter. This operation is present when $V_{65} \geq V_5$, when the load power is high enough and the current limit is reached. If voltage increases beyond V_6, constant power mode is attained:

$$V_6 = \frac{P_{max}}{I_{max}} \tag{5.10}$$

Of course in this region current will decrease from the maximum value as power is kept constant and voltage increases.

In case of unidirectional converters interfacing either pure sources (PV) or pure loads (LED lights), only the respective operational half-plane of the hybrid balance controller is used. In case of bidirectional converter operation though, like the battery converter, both planes are used. Depending on the voltage, the battery may be in load operation, where it charges or in source operation, where it discharges. In the case of bidirectional operation a dead-band voltage range, between the two operations is used. When the voltage is within the dead-band range limits, then the battery is turned off. This is done to prevent multiple transitions between charging and discharging modes, when the grid voltage is in this range [36]. This voltage dead-band can be approached by the maximum range of allowed voltage deviation in the DCMG [35]. Then voltage set-points V_3 and V_4 are modified as follows:

$$V_3 = V_{ref} - \frac{V_{deadband}}{2} \tag{5.11}$$

$$V_4 = V_{ref} + \frac{V_{deadband}}{2} \tag{5.12}$$

5.2 Controller implementation

The hybrid balance controller measures the output voltage and based on its value it selects the control mode for the converter according to the voltage ranges described in the previous section. The control diagram of the converter under CF-ZVS modulation was described in the previous section but is presented again below for ease of reference.

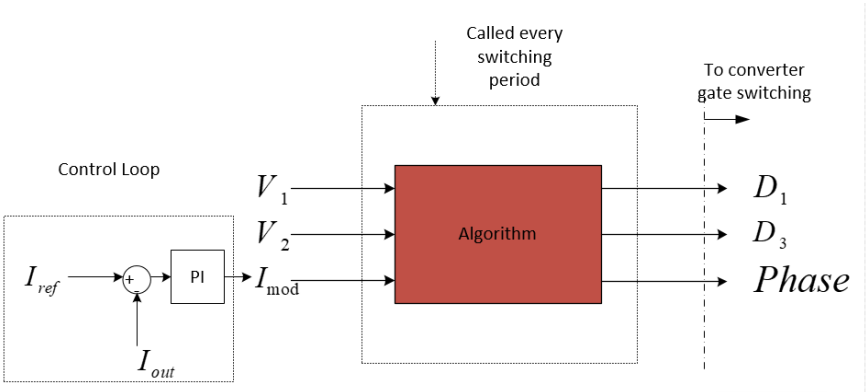


Figure 5.3: CF-ZVS modulation control of the cascaded buck-boost converter

This control scheme controls the inductor current of the converter by shaping it through the algorithm based on the values of V_{in}, V_{out} and P_{tr}. It must be noted that I_{mod} is a variable that carries the required power information P_{tr}. In other words I_{out} is not directly controlled but it is a measurement of the required power to shape and control the inductor current accordingly. Nevertheless, the required operational point is determined by I_{ref} as can be seen in figure 5.3.

Thus the necessary information for control mode of the converter based on the output voltage measurement is passed from the Hybrid Balance controller to the converter controller through I_{ref}. In other words, Hybrid balance controller calculates the output current value based on the specific mode of operation associated with the output voltage measurement and sets it as a reference operation point for the low level control of the converter.

5.2.1 Droop Controller

The droop controller equation is given by (5.2). This controller adds a virtual resistance to the output of the converter and in this way it influences the output impedance, which in turn influences the output voltage, thus controlling the power flow to the rest of the grid. In classic droop control approach, the current measurement of the output provides the information of the converter's loading and is used to set the voltage reference towards the voltage controller of the converter.

Another possibility that complies with the configuration of the hybrid balance controller, utilizes the output voltage measurement of the converter and sets the current reference in respect with the selected droop coefficient, towards the current PI of the low level controller [33], [34]. This comes with the advantage of omitting a voltage control loop and is faster since one less integrator is present in the control loop. This second droop controller comes in accordance with the configuration of our converter and hybrid balance controller. The control loop diagram for this mode can be seen in the figure below:

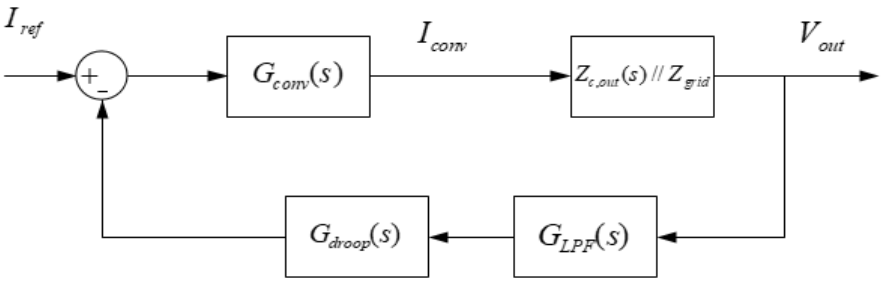


Figure 5.4: Converter Control Diagram with Voltage measurement droop control.

The converter current can be seen given now in the Laplace domain as:

$$I_{conv} = G_{LPF}(s) \times G_{conv}(s) \times G_{droop}(s) \times V_{out} \tag{5.13}$$

where G_{LPF} is a low pass filter for the output voltage measurement to protect against oversensitive reactions of the droop controller at high frequency harmonics and fast oscillations of the dc bus voltage [26], [33]. The droop transfer function $G_{droop}(s)$ has impedance characteristics of $1/R_{droop}$ to account for the voltage measurement impact on the output current and $G_{conv}(s)$ can be assumed as a first order transfer function with unity gain below the crossover frequency f_{PI} of the current controller of the converter. This assumption is based on the fact that the low level control implemented, works ideally and thus the closed low-level control loop can be substituted by a first order TF [33]. The above equation can be manipulated into:

$$I_{conv} = Z_{droop}(s) \times V_{out} \tag{5.14}$$

Where

$$Z_{droop}(s) = \frac{R_{droop}}{G_{conv}(s) \times G_{LPF}(s)} \tag{5.15}$$

is the converter's output impedance modified due to the droop controller. As it can be seen from (5.14), the converter now can be represented as a voltage dependent current source. The output converter impedance and the bus impedance can now be given by:

$$Z_{out}(s) = Z_{droop}(s)//Z_{c,out}(s) \tag{5.16}$$

$$Z_{bus}(s) = Z_{out}(s)//Z_{grid}(s) \tag{5.17}$$

Z_{grid} includes the line resistances and the output impendences of the other components in the DC microgrid. In order for the system to be stable then the complex bus impedance must not have Right Half Plane (RHP) zeros or alternatively, its phase should be in the range of –90° to +90°.

Instability in the DCMG can arise from tightly controlled parallel connected load converters. Load converters display then constant power characteristics. This can be expressed mathematically as:

$$P_{in} = P_{out} = V \times I = constant \tag{5.18}$$

This leads to:

$$dP = v \times di + i \times dv = 0 \leftrightarrow \frac{dv}{di} = -\frac{v}{i} \leftrightarrow r = -\frac{v}{i} \tag{5.19}$$

This shows that although the instantaneous resistance is positive ($\frac{V}{I} > 0$), the incremental resistance or the slope of the V-I curve has a negative value. When a CPL is connected to a capacitor like the case of the output capacitor of a converter then it holds true that [61]:

$$v_c = \frac{P}{i}, \qquad -i = C\frac{dv_c}{dt} \tag{5.20}$$

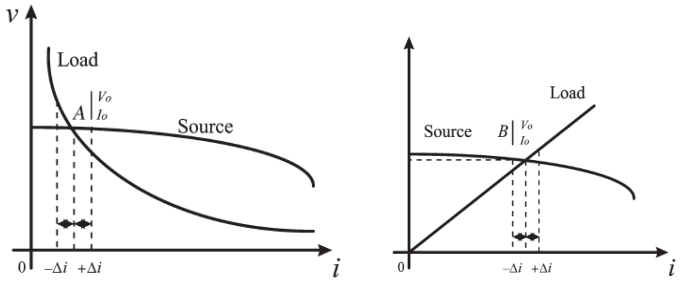


Figure 5.5: Source Converters and loads exhibiting a) CPL b) Resistive characteristics

The instability due to the CPL can be understood as follows: the system is stable if $V_{out} = V_{load}$. If a small disturbance occurs and V_{load} reduces, then due to the constant power behavior (eq. 5.20), the load current will increase as in fig. 5.5a. This will discharge the capacitor and the output voltage will decrease further going away from the stable operating point, leading to oscillations and dc bus voltage collapse. In converter terms, this means that the transfer function(eq. 5.16) exhibits right half plane zeros or the negative incremental resistance introduces a phase shift at -180°, violating the stability criterion [34].

In contrast to that, if the load exhibits resistive behavior, then a decrease on the load voltage will lead to decrease of the load current and an increase of the converter output voltage going towards the stable operational point (fig. 5.5b). This is exactly the behavior the droop control introduces on the converter output. According to eq. (5.2), if the load current increases, then

the output converter voltage decreases and equilibrium is restored, like having an added resistance, which damps the input CPL negative resistance effect towards the converter [61].

So closed control loop with droop can lead to system stability as it decreases the output characteristic impedance of the converter, therefore improving damping and stability [61]. By proper design of the droop control stability can be ensured. The converter output impedance is given by (5.16). From (5.15), $Z_{out}(s) = R_{droop}/G_{LPF}(s)$, assuming the frequency of the low pass filter is much smaller than the frequency of the closed current control loop of $G_{conv}(s)$. This is validated when we accepted that $G_{conv}(s) = 1$ for frequencies below f_{PI}. Then, the output impedance can be described by [33], [34]:

$$Z_{out}(s) = -R_{droop}\frac{1+\frac{s}{\omega_{LPF}}}{1+\frac{s}{\omega_{droop}}+\frac{s^2}{\omega_{droop}\times\omega_{LPF}}} \tag{5.21}$$

Where $\omega_{droop} = 1/(-R_{droop}\times C_{out})$. From [38], a second order system is described by :

$$G(s) = \frac{1}{1+\frac{s}{\omega_0\times Q}+\frac{s^2}{{\omega_0}^2}} \tag{5.22}$$

And so $Q = \sqrt{\frac{\omega_{droop}}{\omega_{LPF}}}$. As explained in [38], the damping factor Q points to overshoot and oscillations. By selecting a proper value of Q (e.g. 0.5 which means phase margin >76°) then the output impedance of converter can be properly shaped and the response become without oscillations. The low pass filter and the Droop value are then linked by:

$$\omega_{LPF} = \frac{1}{R_{droop}\times C_{out}\times Q} \leftrightarrow R_{droop} = \frac{1}{\omega_{LPF}\times C_{out}\times Q} \tag{5.23}$$

For frequencies below the closed current control loop, the output impedance is dominated by the droop control. In low frequencies, we saw that $G_{conv}(s) = 1$ and $Z_{out}(s) = R_{droop}$, so the converter output impedance displays an ohmic behavior and 180° phase is added due to the droop control, which leads the phase to 0°. For high frequencies $Z_{out}(s) = Z_{c,out}(s)$. This behavior can be seen in an example in the figure below:

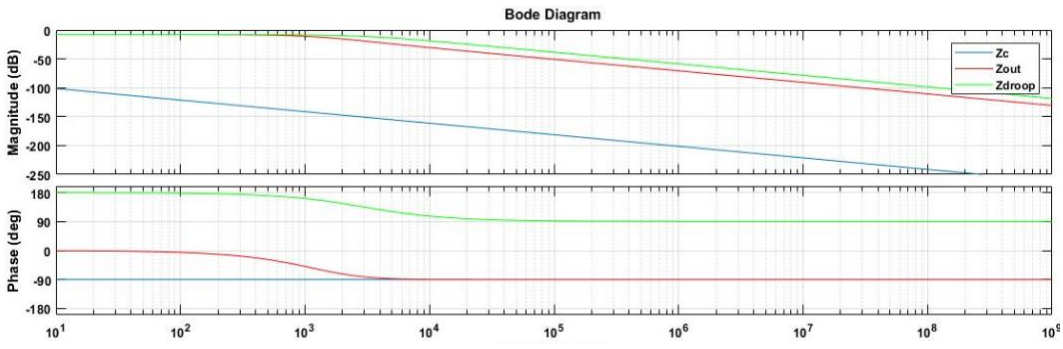


Figure 5.6: Bode Diagram for a Converter with Voltage Droop Control.

The same holds true if $G_{conv}(s)$ is taken into account. Then in low frequencies the droop control and the current controller will dominate. With the design of the converter based on (5.23), highlighted in fig. 5.6, the phase is at 0° for low frequencies, which signifies a constant value or resistive behavior. This is very important for the current sharing in the DCMG, as now the

effect of the line resistance can be attenuated by incorporating its value into the droop coefficient value and mitigate the voltage drop as we will see in the design process.

If equation (5.23) is affirmed in the design then the dynamic response of the converter is without overshoots or ringing. The CPL will not affect the converter, if no gain intersection takes place between Z_{grid} and Z_{out} at a 180° phase difference [34]. This is because the negative resistance a CPL introduces will lead Z_{grid} phase to -180° and from Nyquist the complex Z_{out}/Z_{grid} phase must be between +90° and -90°. Generally increasing the droop coefficient leads to increased stability as the poles are pushed towards the stability region [62].

This comes in accordance with the analysis done on chapter 3. Assuming ideal control of the voltage, the input impedance of the converter is given by $Z_N = -\frac{R}{M^2}$. Then for a stable system it holds that $|Z_{out}| \ll \left|-\frac{R}{M^2}\right|$, meaning that if R_{droop} is selected accordingly no intersection takes place. Apart from that, since phase margin is selected to be high, the system will be without oscillations when in droop. Since at least one converter operates in droop in the system at any time stability can be ensured.

After this analysis has been carried out, the droop controller can be seen in the figure below:

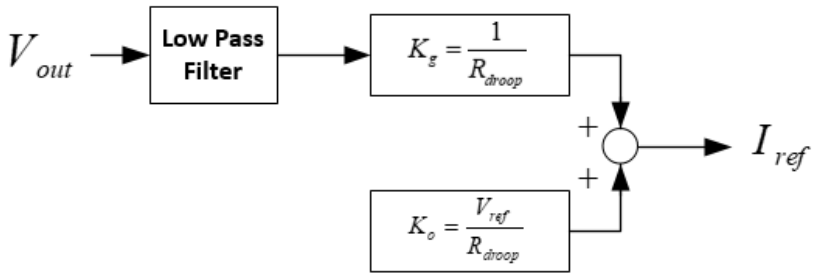


Figure 5.7: Droop Controller with Voltage Measurement.

5.2.2 Constant Power controller

The constant power controller receives the maximum power information from each component in a specific time and forwards the required set point for the current controller. This power may change for every converter. In the case of PV, it is the maximum available power according to the environmental conditions. In case of battery it depends on the battery charge and discharge characteristics. For the load, it may vary depending on the additional load added or switched off. The notation though for load or charging operation follows the negative sign. Whatever the case the set point can be described by (5.3) and the control diagram can be seen below:

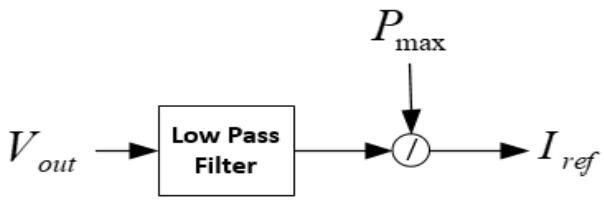


Figure 5.8: Constant Power Controller

5.2.3 Constant Current Controller and Charge/Discharge Controller

The constant current controller is implemented through the hybrid balance controller setting the maximum allowable current for the converter. This limit can be implemented in the current PI

controller of figure 5.3 as a saturation limit. Of course it can be implemented as a current reference by the hybrid balance controller.

Finally, another controller that is implemented in addition to the above is a charge/discharge controller for the battery. When the SOC level of the battery during charging exceeds a threshold, then the battery stops charging to prevent overcharging. Similarly during discharge, the battery stops feeding power, if the SOC value drops below a low threshold value. Both operations can be implemented through the constant current controller, by setting the maximum or minimum value at zero and therefore modifying the Hybrid balance controller set points.

5.2.4 Complete Controller Structure

Now that each controller has been analyzed and modeled, the total control scheme of the DCMG with the hybrid balance controller and the current control of each converter can be visualized in the figure below:

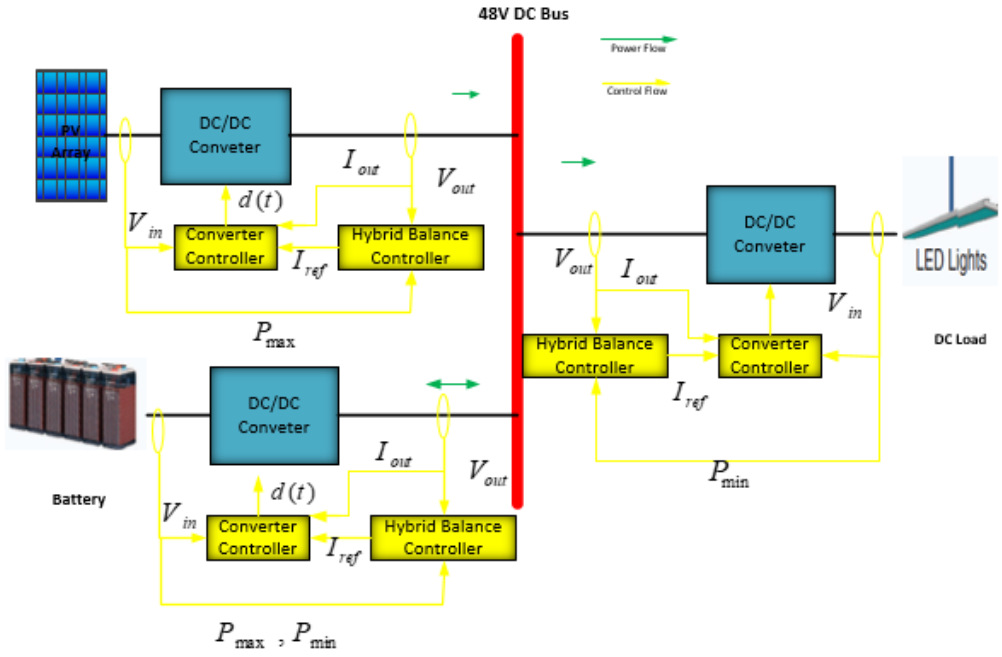


Figure 5.9: Total Control Scheme of the DC microgrid.

5.3 Component Modelling and Sizing

In this section the modelling of the DCMG's components and their respective values is going to be presented. It must be noted that due to the complexity of the converter switching model, simulations require a lot of time. Furthermore, the main object of this thesis is on the converter operation as well as its performance with a higher level DCMG control such as the Hybrid Balance Controller. Control efforts are thus concentrated on the DC bus side of the converters. For this reason components are modeled by simple models as voltage sources and resistances. Despite that, effort was made that values and key parameters selected are sufficiently representing the operation of each component.

5.3.1 Load

The DCMG of this thesis is feeding a load of LED lighting for office or house applications. LED lighting is gaining increased market share due to low power consumption, higher life time and higher luminosity per watt compared to conventional lighting like bulbs or fluorescent lamps. LED lighting is inherently DC which makes it ideal for interconnection with a DC grid

and renewable energy sources like PV. In addition to that LED lights can be dimmed and thus can support intelligent lighting systems for power reduction [13].

In [63], a three level driver is used to power the led stack. The first is a boost rectifier, the second an insulation level with ZVS capability and the third a buck converter for voltage regulation. In the 48V DMCG, insulation and rectification are not needed. Comparable driver topology with resonant ZVS is also presented in [64]. The cascaded buck and boost converter can therefore assume the role of the LED driver.

As stated in [65], the energy consumption of a LED light when dimmed can be given by:

$$E = v \int_0^t di \tag{5.24}$$

Where E is the energy consumption of the LED lamp when it operates for t. The voltage is kept constant and the energy consumption and luminosity depends on the current drawn by the LED. So it makes sense to represent the load with a voltage source with a small resistance in series. In this way the power required by the LED and the current may be given as a parameter towards the HB controller. In other words the load is simulated in a way that will allow us to support all control operations on the DC bus side of the load converter and its power requirement is a variable towards the hybrid balance controller.

For typical offices of 80m2 according to [65],[66] a LED light load of 300W accounting for losses in the interconnecting cables is sufficient. For simplicity the load here is considered as concentrated. The voltage is selected to match the operating range of the converter and result in acceptable currents. For example led strip lights of voltage around 48V are commonly found in the commerce.

It is obvious that with this modelling approach any DC load with a nominal voltage of 48V that can be dimmed can be represented in the DCMG.

5.3.2 PV Model

A common modeling technique found in literature [67]–[70] regarding the PV module is the five parameters model as expressed through:

$$I = I_{ph} - I_o \left\{ exp\left[\frac{V + I \times R_s}{V_T \times a} \right] - 1 \right\} - \frac{V + I \times R_s}{R_p} \tag{5.25}$$

Where $I, V$the PV module output current and voltage, I_{ph} the photovoltaic saturation current, I_o is the diode saturation current, V_T is the thermal voltage of the module with N_s series connected cells and R_s, R_p are the equivalent series and parallel resistances of the PV module. More specifically, R_s refers to the total of internal resistances of the PV module, while R_p describes the pn-junction behavior (leakage currents) [67], [68]. Coefficient a refers to the diode ideality and can assume a value in the range$1 \leq a \leq 1.5$. The model of the PV module can be seen below:

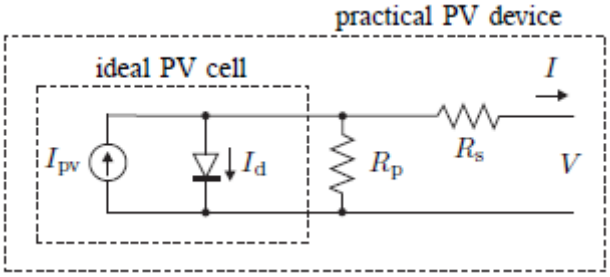


Figure 5.10: PV module equivalent[68].

The data required by eq. 5.24 are usually unknown. Data regarding the PV module are limited to the information provided by the manufacturer. This information regards some operational points like open-circuit voltage, short circuit current, maximum power, voltage and current in this point as well as some temperature coefficients, all given for STC or NOCT conditions. Based on these data, the five parameters of the model above are calculated. There are different approaches identified in literature [67]–[71]. For example R_p can be neglected as it is usually very high.

But in the context of this thesis, the main objective lies in the cooperation and behavior of the converter under a DCMG level control like the Hybrid balance controller. The above models are more accurate for MPPT algorithm studies and behavior of the PV model itself. In this thesis control, as we have already discussed, is applied on the DC bus side of the converter since the hybrid balance controller refers to the voltage of this side, while MPPT control should be applied on the component-PV side of the converter. In order to decouple maximum power from the component modeling, the same approach of a voltage source in series with a resistance is going to be used. A basic assumption is made that maximum power can be extracted from the PV module any time.

Based on the analysis made in [68], an algorithm is developed and based on the manufacturer data provided the five parameter model is derived. Equation (5.24) is solved for the open circuit, short circuit and Maximum Power point operation of the PV. R_p *and* R_s are estimated through an iterative process in order to match the experimental maximum power provided by the manufacturer with the model's maximum power. As soon as the experimental I-V curves are matched and the validity of the model is confirmed, then this model can be used to extract the I-V and P-V curves under different irradiation and ambient temperature conditions. Finally, a look up table is implemented, where the maximum power and the voltage of the PV module under different environmental conditions are calculated. The process is illustrated in the figure below:

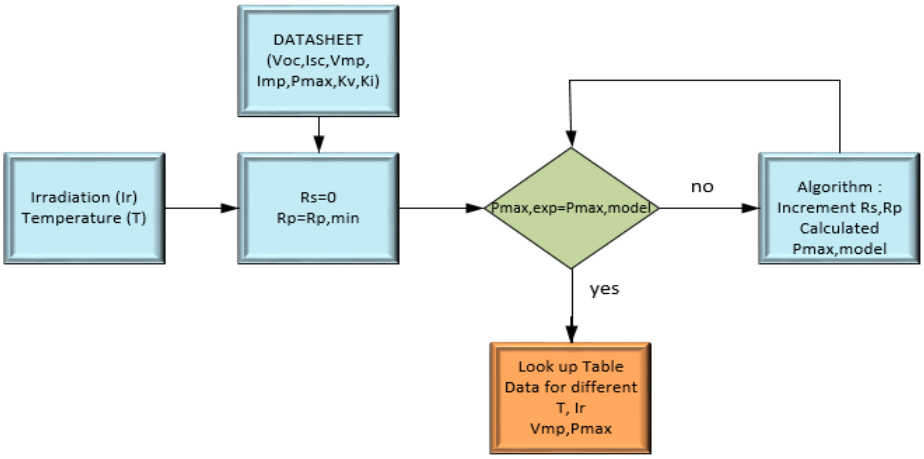


Figure 5.11: Process to determine Pmax, Vmp for different environmental conditions.

The look up table is used in the Simulink model to change the voltage source value of the PV model and supply P_{max} to the Hybrid Balance Controller depending on the irradiation and temperature conditions.

As far as sizing is concerned, a logical assumption should be that the PV module should be enough to cover the peak amount of load. So the peak load demand sets the PV capacity. Since we chose a peak load of 300 W, then it makes sense to have at least this value. This comes in accordance with the IEEE standard that a 48V DCMG should be less or equal to 400W [72].

A PV module of 350Wp was chosen for this thesis to account for losses in the system as well as sufficient battery charging. The Data provided by the manufacturer can be seen in the table below:

Table 5.1: PV model Parameters.

Parameter	**STC(Irradiance=1000W/m^2,T=25°C,AM1.5)**
Maximum Power($\boldsymbol{P_{max}}$)	350W
MPP Voltage($\boldsymbol{V_{mpp}}$)	38.8V
MPP Current($\boldsymbol{I_{mpp}}$)	9.02A
Open Circuit Voltage($\boldsymbol{V_{OC}}$)	47.1V
Short Circuit Current($\boldsymbol{I_{sc}}$)	9.49A
Temp. Coefficient of Voltage ($\boldsymbol{K_V}$)	-0.39%/K
Temp. Coefficient of $\boldsymbol{I_{sc}}$ ($\boldsymbol{K_I}$)	0.04%/K
Number of Cells($\boldsymbol{N_s}$)	60

In the figures below the manufacturer and the model I-V curves are presented for comparison.

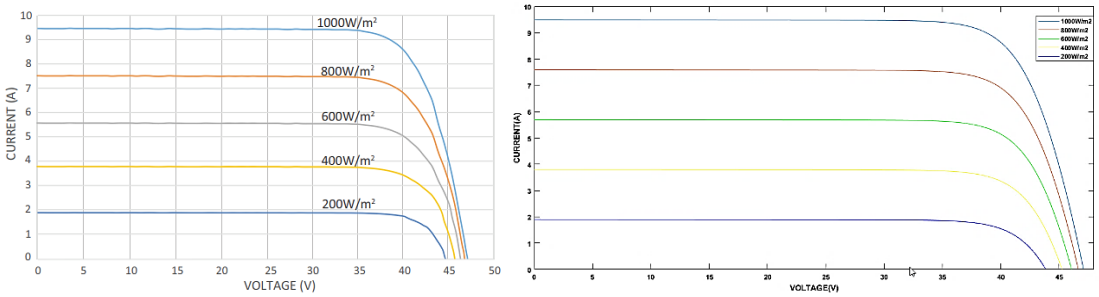


Figure 5.12: a) Experimental and b) Model I-V curve.

We can see that the model accurately follows the experimental data. For this reason the look up table can now be constructed based on this model. The P-V model curves can now be constructed for different irradiances and temperatures.

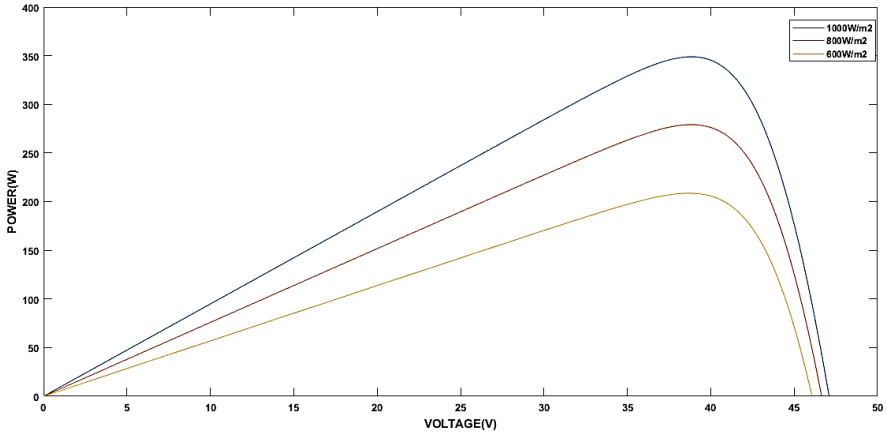


Figure 5.13: P-V model curve

The look up table can now be fed with environmental data and therefore change the model voltage and maximum power that can be delivered to the DCMG.

5.3.3 Battery

For the battery model, we could also use the voltage source model. But in this case, a power integrator simulating the state of charge (SOC) of the battery should be implemented. Furthermore battery voltage changes depending on the SOC level and also depending on whether it is in charge or discharge mode. For these reasons the Simulink Model for the battery is chosen, which can be seen in the figure below:

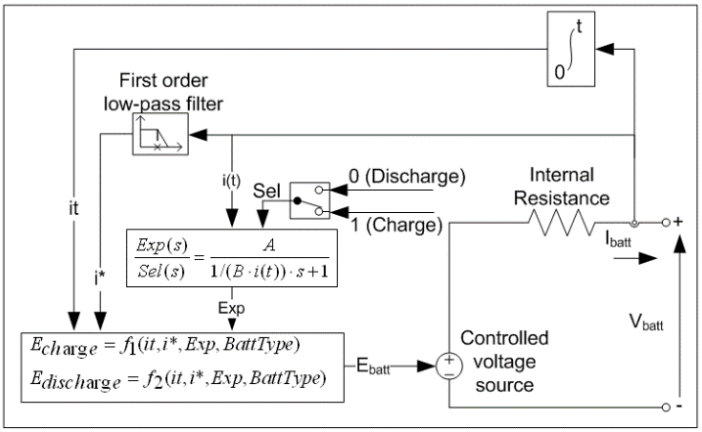


Figure 5.14: Simulink Battery Model[73]

Depending on the type of battery different equations apply. The Simulink battery model accurately represents the battery voltage behavior under different SOC levels and mode of operation even with the exponential characteristics.

Every battery is described by a maximum charging and discharging current. These currents are setting the limit of how fast a battery can be charged or discharged respectively. These limits can be seen from the bus side of the battery converter as power limits given by:

$$P_{charge}^{max} = I_{charge}^{max} \times V_{batt} \tag{5.26}$$

$$P_{discharge}^{max} = I_{discharge}^{max} \times V_{batt} \quad (5.27)$$

These power limits are the reflection of the battery charge and discharge limits towards the DC bus and are the power variables towards the HBC. These currents are set by the battery manufacturer and can be found on datasheets. It doesn't though mean that these currents cannot be exceeded for rapid charge or discharge. Another limit for the converter currents are set by the converter itself. So if the charge/discharge currents exceed the converter maximum current, then these currents are limited to the maximum allowed converter current. So the maximum power that can be fed or drawn out of the converter is given by $P_{max} = max(V_{batt}) \times I_{converter}^{max}$. To prevent the battery voltage collapsing at low SOC levels, and to prevent overcharging an additional control is implemented as described in the current limiter controller.

It should also be noted though that in our simulations the SOC level cannot change significantly and neither can the voltage, since simulations are run for very short times. For this reason different SOC levels will be simulated.

The battery capacity is chosen based on the load energy consumption and the autonomous time it needs to satisfy, when the PV is not producing any power. With regard to the office use, it should be able to satisfy the demand for at least 8h, a working day.. A first estimation would be to have a battery supplying the peak load demand for 8h, yielding a required battery capacity of at least: $300W \times 8h = 2400Wh$. But according to [65], the real consumption is lower and if a dimming operation control is used it can go even below. Based on [65], a value of $435Wh$ is closer to reality.

The nominal battery voltage is chosen at 36V. Although it makes sense to use a 48V nominal voltage, due to the exponential voltage characteristics of the battery, the battery voltage may exceed the converter voltage range of 20-50V. Furthermore charging is taking place under higher voltages than the nominal. With this in mind a $\frac{435Wh}{36V} = 12Ah$ battery is needed. Keeping in mind a maximum allowed battery capacity (80%) is commonly used to prevent overcharging or over discharging of the battery this capacity will increase. Therefore a $20Ah$ will be used. The data of the battery used can be seen in the table below:

Table 5.2: Battery Model Parameters.

Parameter	Value
Nominal Voltage	36 V
Maximum Charge Voltage	43.5 V
Maximum Discharge Voltage (when SOC is at 100%)	42 V
Capacity	20 Ah
Max Discharge Current-Max discharge power	10A-360 W
Max Charge Current-Max charge Power	5A-180 W
Impedance	200 mΩ

As discussed above, to prevent overcharging and depletion of the battery capacity, a SOC based controller is implemented. If SOC level is above 90%, then the battery converter stops any further charging setting the current to zero. Similar to this, when SOC level drops below 10%, the battery stops discharging.

5.3.4 Line Resistances

Finally it should be noted that all the components are connected to the common DC bus through cable lines that exhibit line resistances described by:

$$R_{line} = \rho \times \frac{l}{A} \tag{5.28}$$

Where ρ the electrical resistivity of cable material, l is the cable length and A is the cable cross section area. We suppose that all components are at equal distances from the DC bus and therefore their line resistances are equal. Then the voltage drop of each output is $I \times R_{line}$, so the total voltage difference between two components can be given by $(I_i + I_j) \times R_{line}$ and the total power loss is $\sum_{i=1}^{3}(I_i^2 \times R_{line})$, where i a DCMG component and I_i its respective output current. Usually $A = 2.5mm^2$ copper cables are used. With $\rho_{copper} = 17{,}2\ n\Omega \cdot m$ and a length of 15m for each cable, then $R_{line} = 0.1\Omega$. As described in [23], this line resistance leads to poor load sharing between sources and should be taken into account when designing the droop coefficients. In the specific DCMG though only one converter is in droop mode at any time and to guarantee this, the voltage drop is accounted, when setting the voltage set points of the hybrid balance controller or by added the R_{line} into the droop coefficient to mitigate its effect, as we discussed in section 5.2.1.

5.4 DC Microgrid Operation.

The next step lies in setting the voltage set-points for the Hybrid balance controller for each component. The nominal DC voltage of the DC microgrid is set at 48V. The bus voltage is allowed to exhibit a 5% deviation as set by LVDC standards [74] and commonly found in literature [23], [35], [75], [76]. As we discussed, the battery is assuming the control of voltage bus in nominal conditions through charging and discharging operations. So the voltage reference for the battery converter is set at 48V. The battery is controlling the dc bus voltage in the range of 47-49V and droop control is applied. When these limits are exceeded, then it shifts to constant power region at the maximum power it can charge or discharge with.

The upper voltage limit of the DCMG is set by the converter voltage range at 52V. Since PV source is the power generator in the DCMG it is set at the highest voltage and therefore priority in the DCMG. So the reference voltage for the HBC of the PV converter is set at 52V. The PV module should operate under maximum power, which continuously changes depending on the environmental conditions. When the upper limit of the voltage bus deviation is exceeded, then to prevent stability issues and overcharging of the battery, the PV source droops up to the maximum voltage of 52V, instead of switching off.

Finally the load converter voltage reference is set at lower voltages in the DC microgrid, because the load should operate under CP conditions within the nominal operating voltage ranges of the DCMG and only droop when the DC bus voltage is reduced significantly. Generally, voltage droop should start under the minimum limit of the allowed voltage deviation, or at least when the sources operate at their maximum power output.

Finally the maximum and minimum currents are set by the converter. For this converter these are set at $\pm 10A$. These values describe extreme conditions that may be exhibited in the system, during start up or failures but during nominal operating conditions should not be observed.

Based on equations (5.4-5.12), the parameters of each component and the analysis above, the Hybrid balance control voltage set-points and parameters for each operation are presented in the table below. It should be noted that the voltage drop on each component is taken into account. If the maximum current is set at 10A then a 2V drop from component to component may be exhibited ($I_{max}(R_{line} + R_{line})$. Since we don't want to have simultaneous droop of components, then this voltage drop should be accounted for. Normally the cable resistance is not known and neither is the voltage drop on each one. Another approach could be the inclusion

of R_{line} to the R_{droop} coefficient. But allowing for a margin on the set points is necessary in any case. Under these considerations the set points can be seen below:

Table 5.3: Hybrid Balance Voltage Set-Points.

Voltage Set-point	PV	Battery	Load
$\mathbf{V_1}$	35V	36V	-
$\mathbf{V_2}$	51.1V	47V	-
$\mathbf{V_{21}}$	50.7V	45V	-
$\mathbf{V_3}$	52V	47.75V	-
$\mathbf{V_4}$	-	48.25V	40V
$\mathbf{V_5}$	-	(53.8V)	(49.87V)
$\mathbf{V_6}$	-	(18V)	(32.5V)
$\mathbf{V_{65}}$	-	49V	44V

Voltage set-points V_{21}, V_6, V_5 are not affecting the normal operation. For example V_{21} is the set-point for transition from constant current to droop control mode. This transition is satisfied only when $V_{21} < V_1$, which can be attained only for high power values greater than 507W, which cannot be met by the PV module. Same arguments hold for the load. In order to have constant current $V_6 > V_{65}$. For this to happen power must exceed 460W. This is though a possible scenario if more load is added to the DCMG. If power of the PV drops below the maximum rated power, then the voltage set point value for the droop controller will increase. This is though acceptable as we don't want simultaneous droop of the components. The load starts shedding, when both battery and PV are at constant power mode meaning that they supply as much power as possible but the voltage keeps decreasing due to higher load demands.

The operational ranges with the current reference produced by the Hybrid Balance Controller can be seen in the table below:

Table 5.4: Hybrid Balance Controller Parameters.

Voltage Range	Mode of Operation	Flag of Operation	Current Reference	PV	Battery	Load
$\boldsymbol{V \leq V_1}$	Constant Current	1	I_{ref}	I_{max}	I_{max}	–
$\boldsymbol{V_1 < V \leq V_2}$	Constant Power	2	I_{ref}	$\frac{P_{max}}{V}$	$\frac{P_{max}}{V}$	–
$\boldsymbol{V_2 < V < V_3}$	Droop	3	I_{ref}	$\frac{V_3 - V}{R_{droop}}$	$\frac{V_3 - V}{R_{droop}}$	–
	Droop Coefficient		R_{droop}	0,1314	0.0979	–
$\boldsymbol{V_3 \leq V \leq V_4}$	Zero Current	4	I_{ref}	0	0	0
$\boldsymbol{V_4 < V \leq V_{65}}$	Droop	-5	I_{ref}	–	$\frac{V_4 - V}{R_{droop}}$	$\frac{V_4 - V}{R_{droop}}$

	Droop Coefficient		R_{droop}	–	0.2042	0.5867
$\boldsymbol{V > V_{65}}$	Constant Power	-6	I_{ref}	–	$\frac{P_{max}}{V}$	$\frac{P_{max}}{V}$

The filters chosen along with the droop values for the sources above satisfy equation (5.23) for stability. For the nominal load values at dc, no gain intersection takes place between the source and load converter. The hybrid balance graph for each component converter with respect to output voltage can be seen in the figure below:

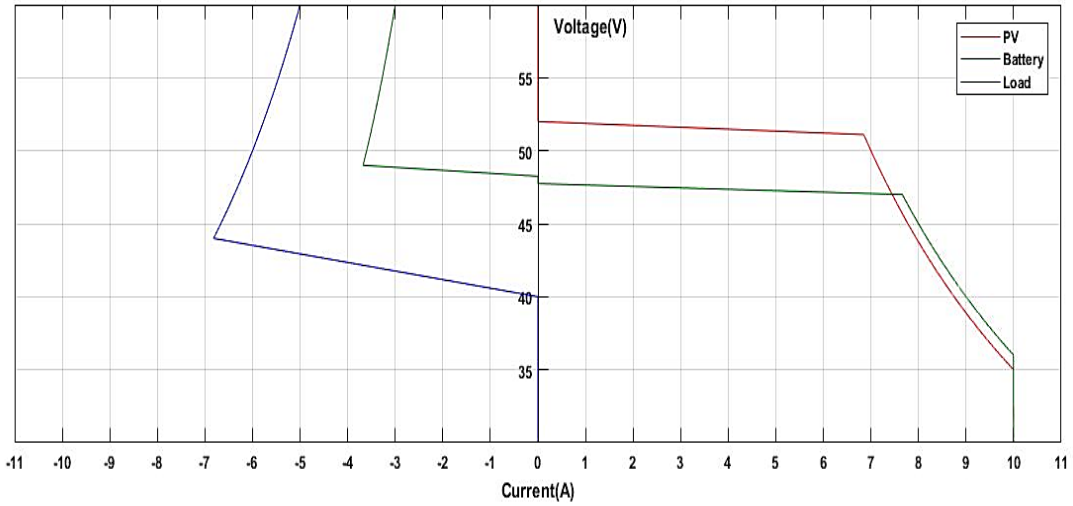


Figure 5.15: Hybrid Balance V-I curves for the DCMG components.

5.5 Simulations

In this section the simulation of the DC microgrid is going to be presented. It should be noted that the aim is to examine the operation of the converter under the Hybrid balance controller. Simulations are carried out for small amount of time, since simulations require too much time and therefore a real solar profile or load variation cannot take place. For this reason simulation will be carried out to highlight characteristic scenarios for the Hybrid Balance controller.

5.5.1 Operation Under different PV power output.

First the Hybrid Balance controller under different PV power output is going to be examined. For the simulations four different values of irradiance were used. The results can be seen in the figures below. The battery is set at 50%.

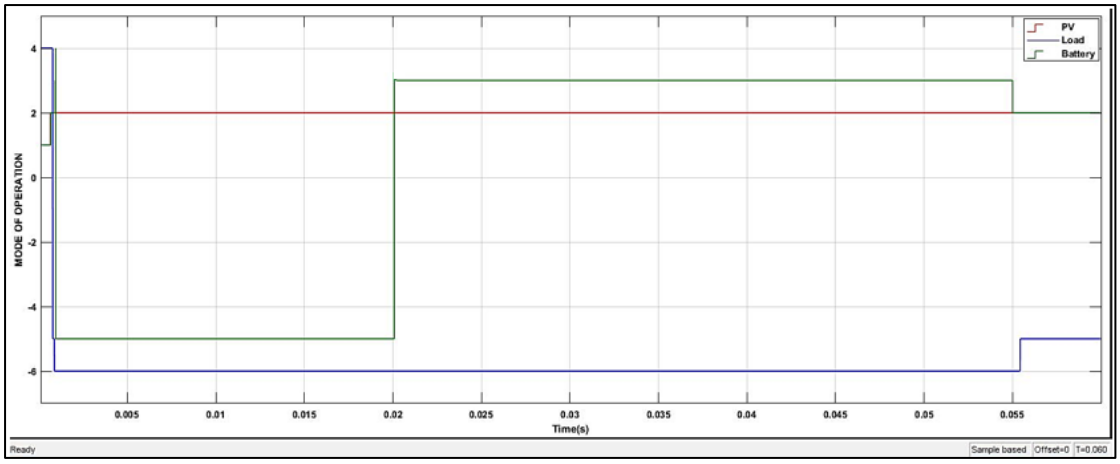


Figure 5.16: Mode of Operation of each Converter under different irradiances and PV power outputs.

Initially the irradiance value is at 1000W/m2, which corresponds to a maximum output power of 350W. Both the PV and the battery start up the system sharing the initial high current and stress, and are operating at maximum current operation (mode 1) as can be seen in figures 5.16 and 5.18 at the start of the simulation. As the voltage is build up in the beginning, the load passes into droop mode (mode -5) but quickly shifts to constant power operation (mode -6) of 300W. The PV is operating under constant power (mode 2), while the excess of power produced is supplied to the battery, which simultaneously regulates the bus voltage as it is in droop operation (mode -5). At time 0.02s the irradiance value is set at 500W/m2, which yields a maximum power of 173W. This value is not sufficient to cover the load, so the battery shifts to source droop operation (mode 3) supplying the necessary amount of power supporting both the voltage and the load. At 0.03 the irradiance drops at 200W/m2 resulting in even lower PV output. The battery still remains in droop operation and the load still works under constant power mode. The battery though increases its current output to supply the necessary load current, since the PV current decreases (fig. 5.17). It should be reminded that everything is controlled on the DC bus side. At 0.04s, the PV isn't producing anything and the power is zero. The operation modes of the battery and the load still don't change as the battery can adequately supply the load power. The PV operation is denoted by mode 2 in this time, although its output is zero. This is to differentiate from mode 4, where again current is set to zero, but in this case is due to surpassing the maximum voltage of 52V of the Hybrid balance controller as denoted in table 5.4.

Next at 0.05 the PV starts producing again under an irradiance of 600W/m2. The load now is served by both sources again and the battery still regulates the DC bus voltage. The above irradiance values can be exhibited in different times in a day. The transitions of course between different values are not as abrupt as in these simulations and the control could therefore cope even better, but these examples showcase the behavior under different conditions and abrupt changes, and the cooperation between the two levels of control is fast. Finally at 0.055s the battery is switched off assuming that its SOC value drops below 10% and the current charge/discharge limiter implemented through the constant current controller as explained in the respective section(mode 2). With this controller the battery stops supplying power under 10% of SOC value to prevent depletion. Therefore, the battery current drifts to zero (fig 5.17). The PV power is not enough to supply the current and the voltage drops as attested in figure 5.18. Therefore the load enters droop mode (mode -5) as seen in figure 5.16 and balance is restored in the system. It should be noted that the PV slightly increases in current due to the voltage drop and the constant power operation.

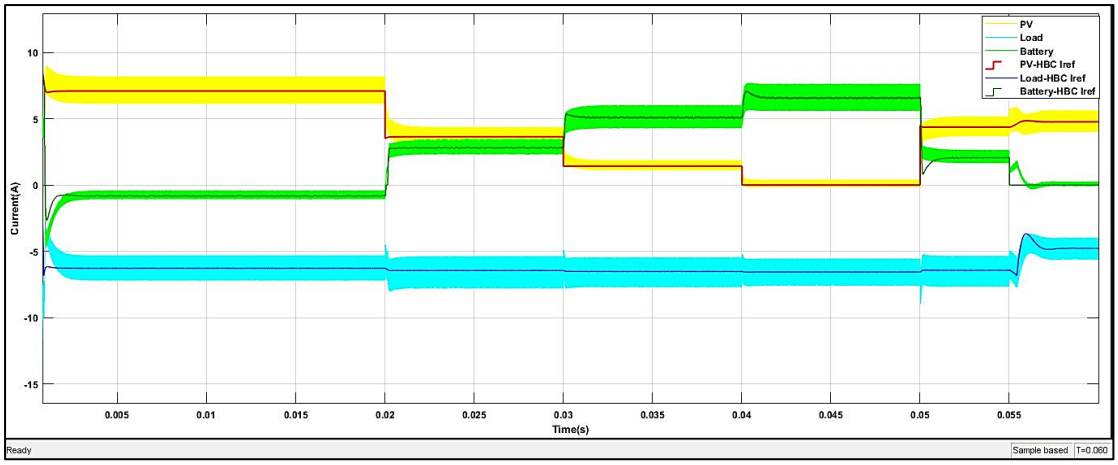


Figure 5.17: Output converter currents and Hybrid Balance current references for each component of the DCMG under PV power output variation.

In addition to these, the most relevant aspect examined in the context of this thesis is how the converter output tracks the reference signals set by the Hybrid Balance controller. We can see from figure 5.17 that each converter responds quite quickly to the reference signals. The delays have to do with the ZVS switching special technique and the fact that the algorithm is run at every period to calculate the required switching times. Faster results could be succeeded with the pre-calculation of the switching times, which could be loaded in a look-up table as described in [50], although not implemented in this thesis as the focus was on confirming the operation of the algorithm. Nevertheless, satisfying operation was achieved even under these abrupt changes.

Special note should be given to the output current ripple. The ripple observed is not really an issue as this is a by-product of the Simulink simulation. As the algorithm is run every switching period continuously, the voltage is acquiring a ripple characteristic due to the simulation algorithms of Simulink. This small ripple of the voltage is creating this current ripple due to the small value of the line resistance.

Despite that, the low level control is regulating the output current at the reference value accordingly. As seen in fig 5.17, when the PV output power reduces successively to 0.02s, 0.03s and 0.04 the PV current reduces, while the battery current increases at the same time. The load current is not changing much, since it is in constant power mode and the voltage variation is small. It is preferable that the load be supplied with constant power all the times and the hybrid balance controller was designed under this consideration giving the load the lowest voltage reference. Thus, when the voltage decreases as seen in figure 5.18, the current slightly increases (fig. 5.17) to satisfy the constant power demand. The negative current value of the battery indicates that the battery is charged. Finally the ripple around the zero value of the PV has to do with the ripple in the other currents at the specific moment and not due to operation of the PV converter, which sets the output to zero according to its HBC reference. The same behavior can be observed during start up where the PV and battery are ramping the voltage up, while load is at zero. Nevertheless its output resistance is circulated by current but no current flows to the component side of the converter.

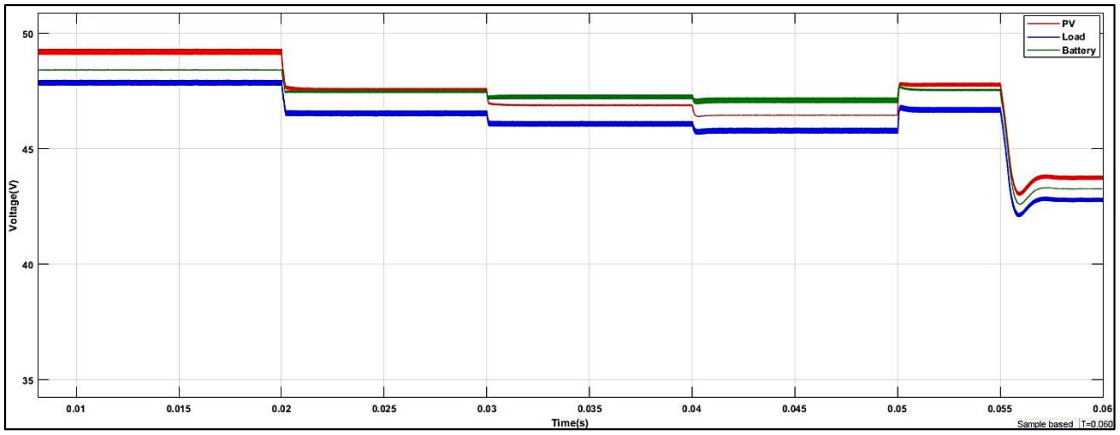


Figure 5.18: Converter output voltages of each DCMG component under PV power output variation.

Finally in the figure above, the voltages of each component's output are presented and can be compared to the mode of operation of figure 5.16 and table 5.4. It should also be mentioned that filters are used to cut-off the ripple of the voltage due to simulations that come also in accordance with the filter needed by the droop controller as described by eq. (5.23). If the voltage is not filtered, then constant switching between operations may be exhibited due to the ripple component, which is must be taken care of as the filter protects against small changes in the voltage waveform and to respond only to large (compared to ripple) changes. This situation may be present if the voltage is near the set point value, but still this behavior is only transitional.

5.5.2 Operation under different Load Conditions

In order to showcase different Hybrid Balance Controller operation modes, the behavior of the system under different load conditions is simulated and presented in the figures below. As before, at the beginning both battery and PV ramp up the voltage of the grid. They are both at constant current mode (mode 1), while the load is switched off (mode 4) as seen in figure 5.19. When the DC voltage reaches the operational ranges the 300W load is switched on and operated under constant power (mode -6), while the PV is in constant power mode and the battery in load droop mode as in the previous simulations.

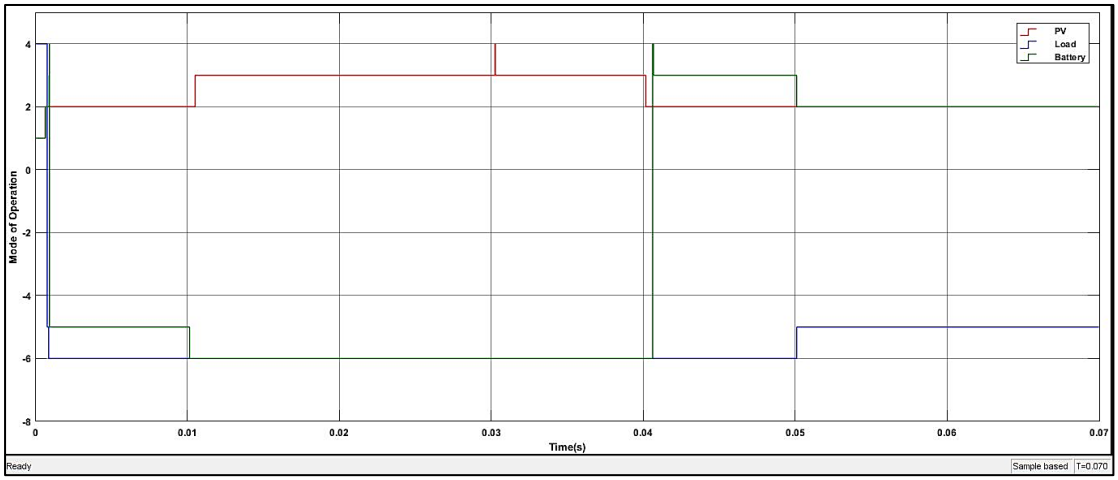


Figure 5.19: Mode of Operation of each Converter under different Load conditions.

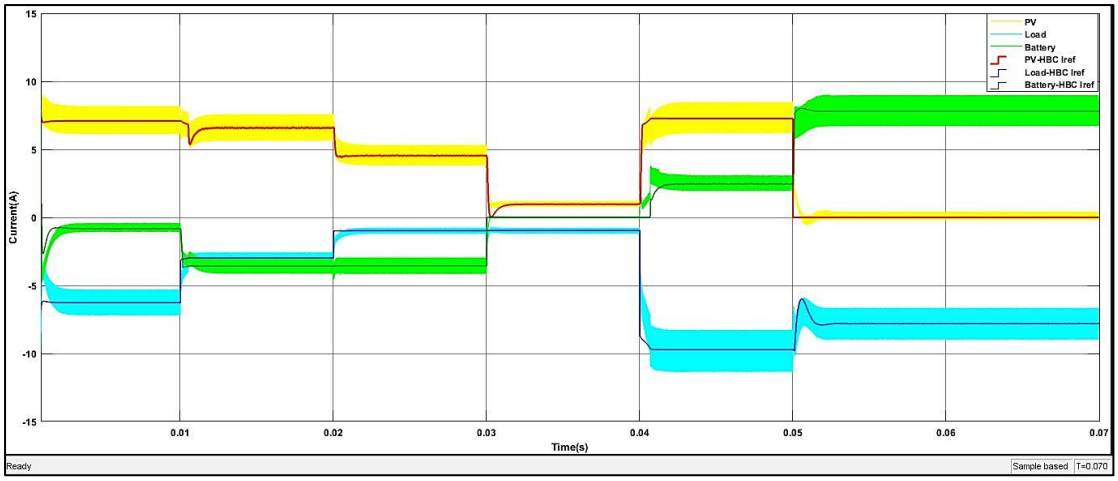


Figure 5.20: Output converter currents and Hybrid Balance current references for each component of the DCMG under Load Variation.

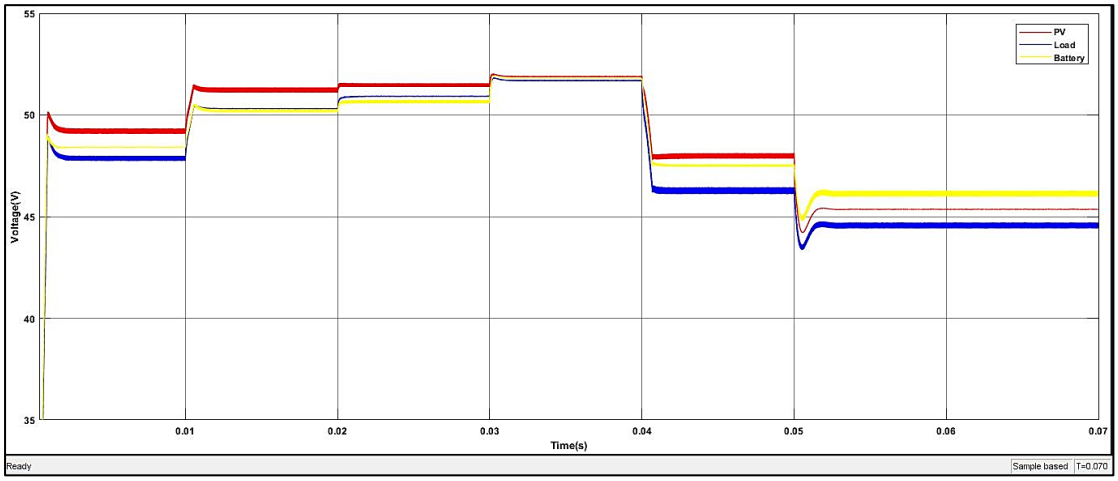


Figure 5.21: Converter output voltages of each DCMG component under Load Variation.

At 0.01s the load decreases to 100W, while the PV is producing the maximum power of 350W. The voltage increases and thus the battery enters constant power mode (charge under constant power, mode -6) and the PV instead of switching off enters droop mode (mode 3), therefore remaining in operation while regulating the DC bus voltage. In this way all components acquire operational points even under these conditions, which is the purpose of the HB controller. Further decrease in load is observed at 0.02s, without a change in operating modes though for any component but a decrease in current for the PV, due to the subsequent decrease in load power and a slight increase in voltages. The battery continues constant power charging.

At time 0.03s the battery is assumed to be charged over 90% SOC and therefore the current/charge limiter switches off the battery. Now the PV current has to decrease significantly as the excess power produced cannot be fed elsewhere. Now the PV supplies just the required load current (fig. 5.20) and the voltages rise even further. We see now that the battery current is zero that the voltages of both battery and PV are identical (fig 5.21). Still DCMG operation is maintained as the PV still droops and regulates the DC bus voltage (mode 3) as seen in figure 5.19. Battery operation although at zero power is still at mode -6 of constant load power to distinguish from mode 4, where power and current are set at zero due to voltage ranges of the HBC.

At 0,04s load demand increases to 450W. We see that the PV enters constant power mode (fig. 5.19), while the battery is discharging also to supply the new load demand that cannot be covered by the PV alone. Although it discharges uncontrollably for a very small period of time, immediately the HBC of the battery is controlling the discharge by setting the battery in source droop mode (mode 3). The PV and the battery are enough in this case to supply the full load and therefore operation under constant power is maintained.

At 0.05 though, the PV panel stops producing power, which is the case in night. Therefore the voltages drop (fig. 5.21) and battery enters constant power discharge (mode 3). This is though not enough to convert the 450W load and therefore the load starts drooping (mode -5), contributing to the DC bus voltage regulation. The load current therefore decreases up to the current the battery can supply and balance is restored in the system. The PV voltage now is not identical to the battery voltage since although nothing is produced by the module, the small ripple circulating in the output side due to the ripples in the other currents, creates this difference. Finally at 0.06 the load power increases even further. As though seen from figures 5.19-5.21, this doesn't change anything, since the battery is already supplying as much as it can and the load droop control is setting the load current demand accordingly.

5.5.3 Special Case

A special transition between droop and constant current control modes is shown in this section. As in the previous example PV is producing the maximum amount of power, while the load has its nominal value of 300W. At time 0.01s the battery is disconnected. Therefore the PV moves into droop mode (mode 3), to account for the increase in the voltage, reducing its current output. At t=0.02, the load is increased to 500W. This forces the load to move into constant current mode of operation (mode -65), since now V5>V65 as the power exceeds the limits. But since the PV power cannot support the increased amount of power and current needed, the voltage drops and shifts into droop mode of operation (mode -5). The battery operation may seem to swift to CPS and Deadband but this is due to the voltage of the dc bus. The battery doesn't supply anything as can be seen by the current reference after 0.01s. The current during the load transition that is visible on the battery current waveform is not due to the battery but due to the current change in the grid and drifts to zero when PV and load currents reach stable OP.The above can be seen below:

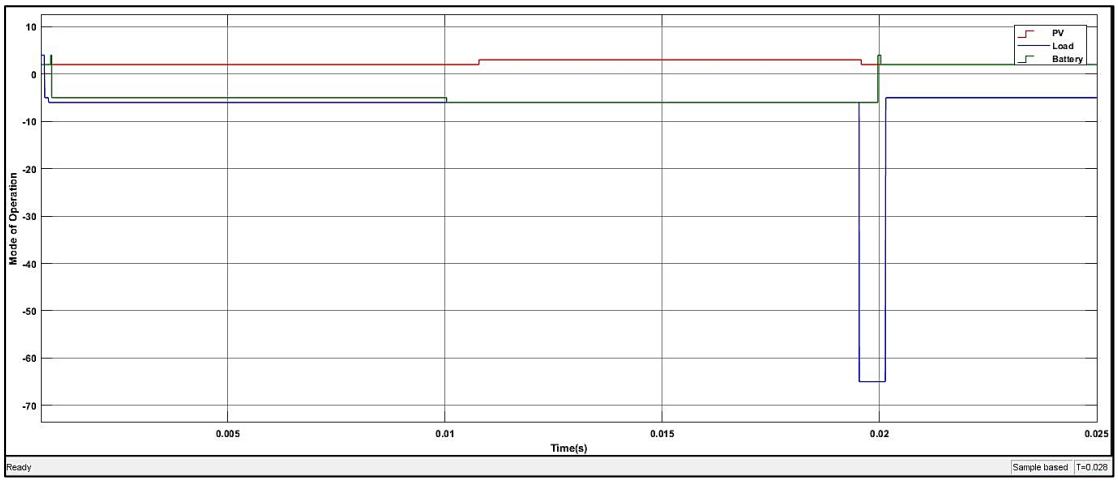


Figure 5.22: Mode of Operation under special conditions.

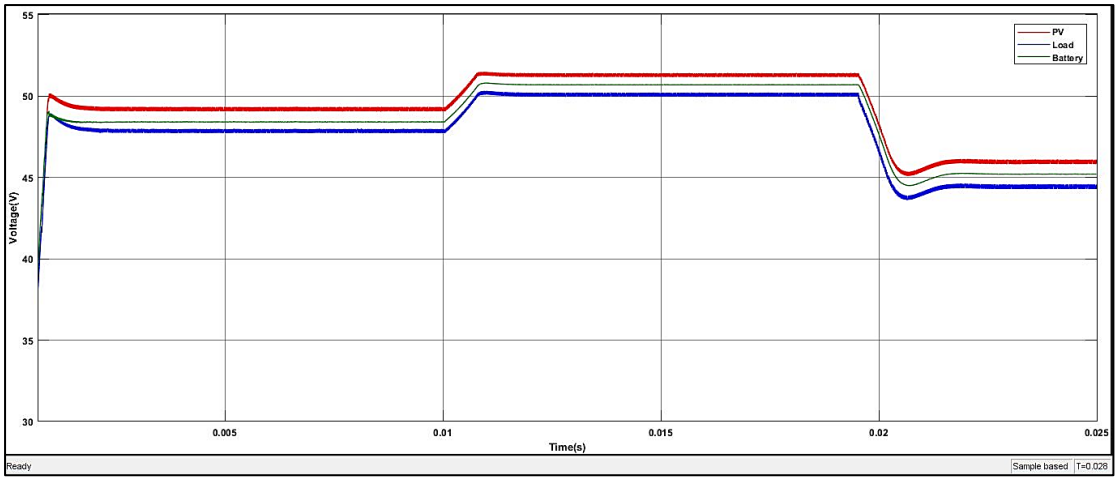


Figure 5.23: Voltages under special conditions.

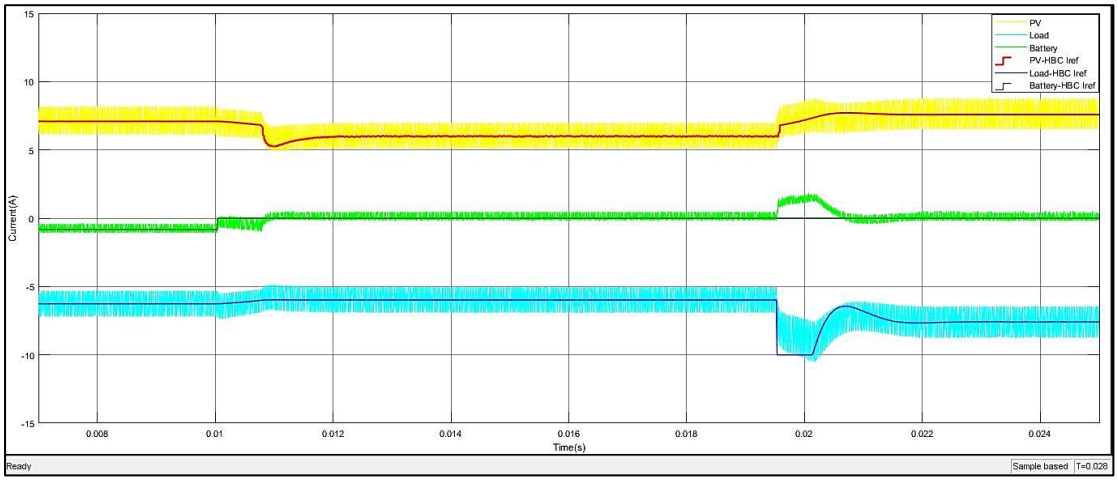


Figure 5.24: Currents under special conditions

6 Conclusions and Recommendations

6.1 Conclusions

This thesis was carried out as an attempt to study the cascaded half bridge buck and boost converter, as the building block of a DC microgrid, evaluating its usefulness as a universal multi-purpose interfacing converter for the DC components of a low voltage DC grid.

The converter was studied as a physical, real component with its switching actions considered. PI controllers were design to address the control of the converter's voltage and current, both in buck operation and in the CF-ZVS operation by controlling the gate signals and thus the switching actions of the converter. Especially the CF-ZVS modulation, as presented in Chapter 4,was implemented for live calculation of the switching timings, instead of the pre-calculation method presented in [50] and used by [51] on the converter prototype in the DC Systems, Energy Conversion & Storage Laboratory of TU Delft. This was mainly done to validate its correct operation and performance. Furthermore, this thesis adds to existing work done previously in the context of the Laboratory by analyzing and proposing control schemes for the converter (in buck and CF-ZVS modes of operation), something that was not done before as the converter was studied to operate statically and not in dynamic conditions.

Apart though from the implementation of the aforementioned low level control, the Hybrid Balance Control proposed by [36] as a DC microgrid decentralized controller was studied and implemented in a modeled DCMG. One major contribution of this thesis is the study and evaluation of the co-operation of this grid level control with the low level control loops of the converter, as most of the literature and previous work in the context of the laboratory, regarded the converter component, mainly as an ideal source-black box, not taking into the consideration the switching, real operation of the converter. Here however, complete control schemes were implemented for each component combining grid and converter level control operations.

Under the scope of the above considerations, this thesis aims to contribute in the efforts of the DC Systems, Energy Conversion & Storage department for a DC future by adding more insight into control operations in DCMG's. Therefore the questions set at the beginning of the thesis can now be answered:

- ***How can the control of the Synchronous Buck Converter can be realized and utilized in a DC microgrid?***

The cascaded buck and boost converter was selected as it offers a wide range of uses and possibilities. In chapter 3, its operation as a buck converter was evaluated. This is done since the buck converter is a widely used and can help in start-up processes. A low level control was designed based on the well-known theoretical small signal analysis. Also a synchronous DCM operation was achieved by independent control of the duty cycles of the half bridge of the cascaded converter. Simulations confirmed the expected performance of control operations and its use in start-up operations of components in a DCMG, where the ZVS modulation of the cascaded converter cannot cope with due to low voltage levels

- ***How is the ZVS-modulation method implemented in the cascaded buck and boost converter and how this control performs under dynamic conditions?***

In chapter 4, the ZVS modulation control technique was analyzed and implemented. With this control soft switching both in turn-on and turn-off of all switches is achieved. ZVS switching of the converter was confirmed as well as its ability to perform exceptionally at unity conversion ratios. Good performance of the control was also confirmed during the transitions from buck to boost modes and vice versa. Soft switching was also achieved during bidirectional operations. The implemented control performs quite satisfying when subjected to changes and ZVS operation is maintained. Thus its suitability as a multipurpose converter for DCMG components can be realized.

- ***How can the hybrid control technique for power balance be integrated with a low level control and implemented for real converters?***

In chapter 5, the above cascaded buck and boost converter with the ZVS modulation as described in chapter 4 was used to interconnect a PV panel, a load and a battery into a 48V DC microgrid. The decentralized Hybrid balance controller was analyzed and selected as the primary microgrid-level control for power flow and balance operations in the DCMG. The hybrid balance controller incorporates a droop controller, constant power controller and a constant current controller which set the required current reference for each component based on the converter output voltage value and some voltage set points based on the components characteristics. These current references are fed to the low level control implemented in the previous chapters and drive the converter output.

Good cooperation and control performance between the Hybrid balance controller and the low level converter controllers was confirmed. The control of the DCMG was tested under various operating conditions and scenarios and the control was found to perform as expected. The hybrid balance controller can guarantee stable system operation and operating points for each component even under extreme case scenarios of low power production. Satisfying transitional behavior was also observed as the system was tested under changes in power production and consumption as well as different SOC battery levels. Such sudden changes are not normal conditions but still the control coped with everything. In every case and scenario the low level control of the converters responded quite fast to the signals set by the Hybrid balance controller.

6.2 Recommendations

In this work a step was taken towards the implementation of the Hybrid balance controller with switching model of the converter. In the following section some suggestions for further study are suggested.

In chapter 4, an offset current control was implemented, which is tightly though connected to the suggested voltage levels and operating conditions. A more accurate and versatile offset current control could be implemented such as voltage dependent deadtime or even some hysteresis controller as suggested in [50] , which needs accurate analog comparators for the half-bridge voltage measurements. Furthermore in order to decrease the computational effort of microcontrollers in real converters, the timings of the ZVS modulation method should be pre-calculated based on the operating conditions (V1, V2, Ptr) and fed into a look-up table. Then during the operation and through linear interpolation the exact timing can be extracted. This will also be beneficial for faster control operations in the DCMG.

Another suggestion would be the implementation of more realistic model for the PV, the battery and the load. In this thesis simple representation by voltage sources was used. More realistic models would yield better results of the total control structure.

In the control structure implemented in the DCMG, everything is controlled on the DC bus side. A better approach would be to switch control sides depending on the hybrid balance mode of operation. For example charging control operations should be performed on the battery side of

the converter to take into account the constant voltage or current charging characteristics of the battery. The PV panel MPPT algorithm control actions take place on the PV side of the converter. Finally load control of LED should take place in the load side to control the current fed in the devices.

Finally due to the vast amount needed, simulations were carried out to show some scenarios that may be present in the DCMG. It would be more accurate to develop a real-time solar profile and realistic load profile to see how the control operates under more probable conditions and to decide the battery capacity more accurately.

Bibliography

[1] L. Mackay, T. Hailu, L. Ramirez-elizondo, and P. Bauer, “Towards a DC Distribution System – Opportunities and Challenges,” pp. 215–220, 2015.

[2] L. Mackay, T. G. Hailu, G. C. Mouli, L. Ramirez-Elizondo, J. A. Ferreira, and P. Bauer, “From DC nano- and microgrids towards the universal DC distribution system - A plea to think further into the future,” *IEEE Power Energy Soc. Gen. Meet.*, vol. 2015–Septe, no. November, 2015.

[3] T. Dragicevic, J. C. Vasquez, J. M. Guerrero, and D. Skrlec, “Advanced LVDC Electrical Power Architectures and Microgrids: A step toward a new generation of power distribution networks.,” *IEEE Electrif. Mag.*, vol. 2, no. 1, pp. 54–65, 2014.

[4] S. Chowdhury, S. P. Chowdhury, and P. Crossley, *Microgrids and Active Distribution Networks*. 2009.

[5] P. Komor and T. Molnar, “Background Paper on Distributed Renewable Energy Generation and Integration,” *Prep. TEC-UNFCCC, Bonn, Ger.*, no. February 2015, 2015.

[6] REN21, *Renewables 2017: global status report*, vol. 72, no. October 2016. 2017.

[7] R. Viral and D. K. Khatod, “Optimal planning of distributed generation systems in distribution system: A review,” *Renew. Sustain. Energy Rev.*, vol. 16, no. 7, pp. 5146–5165, 2012.

[8] M. Gulin, “Control of a DC Microgrid,” 2012, pp. 1–6.

[9] C. Buccella, C. Cecati, and H. Abu-rub, “An Overview on Distributed Generation and Smart Grid Concepts and Technologies,” in *Power Electronics for Renewable Energy Systems, Transportation and Industrial Applications*, Wiley, 2014, pp. 50–68.

[10] D. Kumar, F. Zare, and A. Ghosh, “DC Microgrid Technology: System Architectures, AC Grid Interfaces, Grounding Schemes, Power Quality, Communication Networks, Applications, and Standardizations Aspects,” *IEEE Access*, vol. 5, pp. 12230–12256, 2017.

[11] J. J. Justo, F. Mwasilu, J. Lee, and J. W. Jung, “AC-microgrids versus DC-microgrids with distributed energy resources: A review,” *Renew. Sustain. Energy Rev.*, vol. 24, pp. 387–405, 2013.

[12] L. Mackay, L. Ramirez-Elizondo, and P. Bauer, “DC ready devices - Is redimensioning of the rectification components necessary?,” *Proc. 16th Int. Conf. Mechatronics, Mechatronika 2014*, pp. 1–5, 2014.

[13] M. Hulsebosch, P. Willigenburg, J. Woudstra, and B. Groenewald, “Direct current in public lighting for improvement in LED performance and costs,” *Proc. Conf. Ind. Commer. Use Energy, ICUE*, 2014.

[14] K. Kurohane *et al.*, “An Islanding Operation of DC Smart Grid,” *Control*.

[15] H. Matayoshi, T. Senjyu, and T. Funabashi, “Islanding operation of DC smart grid under DC distribution line faults,” *Proc. - 2015 Int. Symp. Smart Electr. Distrib. Syst.*

Technol. EDST 2015, pp. 313–317, 2015.

[16] Y. Hamdaoui and A. Maach, “Smart islanding in smart grids,” *2016 4th IEEE Int. Conf. Smart Energy Grid Eng. SEGE 2016*, pp. 175–180, 2016.

[17] S. Waffler and J. W. Kolar, “A Novel Low-Loss Modulation Strategy for High-Power Bidirectional Buck- Boost Converters,” *Power Electron. IEEE Trans.*, vol. 24, no. 6, pp. 1589–1599, 2009.

[18] S. Anand and B. G. Fernandes, “Optimal voltage level for DC microgrids,” *IECON Proc. (Industrial Electron. Conf.*, pp. 3034–3039, 2010.

[19] W. Li, X. Mou, Y. Zhou, and C. Marnay, “On voltage standards for DC home microgrids energized by distributed sources,” *Conf. Proc. - 2012 IEEE 7th Int. Power Electron. Motion Control Conf. - ECCE Asia, IPEMC 2012*, vol. 3, pp. 2282–2286, 2012.

[20] R. Panguloori, P. Mishra, and V. Prabu, “Investigation on Choice of DC Electrical Distribution System with Lab Test Results for Office and Commercial,” *Proc. Int. Conf. Control. Commun. Power Eng. Investig.*, p. 6, 2013.

[21] Cong Wang and P. Jain, “A quantitative comparison and evaluation of 48V DC and 380V DC distribution systems for datacenters,” *2014 IEEE 36th Int. Telecommun. Energy Conf.*, pp. 1–7, 2014.

[22] L. Meng *et al.*, “Review on Control of DC Microgrids,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 5, no. 3, pp. 1–1, 2017.

[23] S. Anand, B. G. Fernandes, and J. M. Guerrero, “Distributed control to ensure proportional load sharing and improve voltage regulation in low-voltage DC microgrids,” *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1900–1913, 2013.

[24] C. Jin, P. Wang, J. Xiao, Y. Tang, and F. H. CHOO, “Implementation of Hierarchical Control in DC Microgrids,” *IEEE Trans. Ind. Electron.*, vol. PP, no. 99, p. 1, 2013.

[25] J. M. Guerrero, J. C. Vasquez, J. Matas, L. G. de Vicuna, and M. Castilla, “Hierarchical Control of Droop-Controlled AC and DC Microgrids-A General Approach Toward Standardization,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 158–172, 2011.

[26] R. A. F. Ferreira, H. A. C. Braga, A. A. Ferreira, and P. G. Barbosa, “Analysis of voltage droop control method for dc microgrids with Simulink: Modelling and simulation,” *10th IEEE/IAS Int. Conf. Ind. Appl.*, pp. 1–6, 2012.

[27] Shiguo Luo, Zhihong Ye, Ray-Lee Lin, and F. C. Lee, “A classification and evaluation of paralleling methods for power supply modules,” *30th Annu. IEEE Power Electron. Spec. Conf. Rec. (Cat. No.99CH36321)*, vol. 2, pp. 901–908.

[28] Q. Shafiee, T. Dragičević, J. C. Vasquez, and J. M. Guerrero, “Hierarchical Control for Multiple DC-Microgrids Clusters,” *IEEE Trans. Energy Convers.*, vol. 29, no. 4, pp. 922–933, 2014.

[29] F. Pilo, G. Pisano, and G. G. Soma, “Optimal Coordination of Energy Resources With a Two-Stage Online Active Management,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 10, pp. 4526–4537, 2011.

[30] C. M. Colson, M. H. Nehrir, R. K. Sharma, and B. Asghari, “Improving Sustainability of Hybrid Energy Systems Part I: Incorporating Battery Round-Trip Efficiency and Operational Cost Factors,” *IEEE Trans. Sustain. Energy*, vol. 5, no. 1, pp. 37–45, 2014.

[31] C. L. Su, K. L. Lin, and C. J. Chen, “Power Flow and Generator-Converter Schemes Studies in Ship MVDC Distribution Systems,” *IEEE Trans. Ind. Appl.*, vol. 52, no. 1, pp. 50–59, 2016.

[32] X. Lu, K. Sun, J. M. Guerrero, J. C. Vasquez, and L. Huang, “State-of-charge balance using adaptive droop control for distributed energy storage systems in DC microgrid applications,” *IEEE Trans. Ind. Electron.*, vol. 61, no. 6, pp. 2804–2815, 2014.

[33] L. Ott *et al.*, “An advanced voltage droop control concept for grid-tied and autonomous DC microgrids,” *INTELEC, Int. Telecommun. Energy Conf.*, vol. 2016–Septe, no. October, 2016.

[34] L. Ott, B. Wunder, D. Systems, and F. Iisb, “Design Guidelines for Droop Controlled Power Electronic Converters in LVDC Microgrids,” *2nd IEEE Int. Conf. DC Microgrids (ICDCM 2017)*, pp. 1–36, 2017.

[35] H. J. Kim, Y. S. Lee, J. H. Kim, and B. M. Han, “Coordinated droop control for stand-alone DC micro-grid,” *J. Electr. Eng. Technol.*, vol. 9, no. 3, pp. 1072–1079, 2014.

[36] S. Chaudhuri, L. Mackay, T. G. Hailu, L. Ramirez-elizondo, and P. Bauer, “Hybrid Power Balance Controller for DC Microgrids,” *PES Gen. Meet.*, no. 3, 2016.

[37] A. Emadi, A. Khaligh, C. H. Rivetta, and G. A. Williamson, “Constant power loads and negative impedance instability in automotive systems: Definition, modeling, stability, and control of power electronic converters and motor drives,” *IEEE Trans. Veh. Technol.*, vol. 55, no. 4, pp. 1112–1125, 2006.

[38] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Springer US, 2001.

[39] P. Biczel, “Power Electronic Converters in DC Microgrid,” in *2007 Compatibility in Power Electronics*, 2007, pp. 1–6.

[40] R. K. Hester, C. Thornton, S. Dhople, Z. Zhao, N. Sridhar, and D. Freeman, “High efficiency wide load range buck/boost/bridge photovoltaic microconverter,” *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, pp. 309–313, 2011.

[41] G. R. Walker and P. C. Sernia, “Cascaded DC–DC Converter Connection of Photovoltaic Modules,” *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 1130–1139, 2004.

[42] M. Nymand, “High efficiency power converter for low voltage high power applications,” *Danish Tech. Univ. PhD Thesis, ISBN*, no. January, 2010.

[43] M. Power, E. Converters, and P. Range, “Modular Power Electronic Converters in the Power Range 1 to 10 kW by Aalborg University , Denmark Institute of Energy Technology November 2009,” 2009.

[44] J. Ferrieux and Y. Lembeye, “Optimization and Design of a Cascaded DC / DC Converter Devoted to Grid-Connected Photovoltaic Systems,” vol. 27, no. 4, pp. 2018–2027, 2012.

[45] L. Linares, R. W. Erickson, S. MacAlpine, and M. Brandemuehl, “Improved energy capture in series string photovoltaics via smart distributed power electronics,” *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, pp. 904–910, 2009.

[46] Z. Zhang, R. Pittini, M. A. E. Andersen, and O. C. Thomsena, “A review and design of power electronics converters for fuel cell hybrid system applications,” *Energy*

Procedia, vol. 20, pp. 301–310, 2012.

[47] M. Nymand, R. Tranberg, M. E. Madsen, U. K. Madawala, and M. a. E. Andersen, "What is the best converter for low voltage fuel cell applications- a Buck or Boost?," *35th Annu. Conf. IEEE Ind. Electron.*, pp. 962–970, 2009.

[48] Y. Z. Du Xiaohu; Bai, Sanzhong; Lukic, Srdjan; Huang, Alex, "Review of Non-isolated Bi-directional DC-DC Converters for Plug-in Hybrid Electric Vehicle Charge\rStation Application at Municipal Parking Decks," *IEEE Appl. Power Electron. Conf. Expo.* , no. 1, pp. 1145–1151, 2010.

[49] S. Waffler and J. W. Kolar, "Comparative evaluation of soft-switching concepts for bi-directional buck+boost dc-dc converters," *Power Electron. Conf. (IPEC), 2010 Int.*, pp. 1856–1865, 2010.

[50] S. Waffler and J. W. Kolar, "Efficiency optimization of an automotive multi-phase bi-directional DC-DC converter," *2009 IEEE 6th Int. Power Electron. Motion Control Conf. IPEMC '09*, pp. 566–572, 2009.

[51] T. Ioannis, "DC – DC Converter for Bidirectional Power Flow Applications."

[52] E. Rogers, "Understanding Buck Power Stages in Switchmode Power Supplies Application Report," no. March, p. 36, 1999.

[53] A. Mohan, D. Mathew, and V. M. Nair, "A Control Strategy for a Distributed Power Generation Microgrid Application," vol. 25, no. 12, pp. 395–402, 2013.

[54] R. Nowakowski and Nin, "Efficiency of synchronous versus nonsynchronous buck converters," *Analog Appl. J. Texas Instruments Inc. 4Q*, pp. 15–18, 2009.

[55] W. Fu, S. T. Tan, and A. Fayed, "Switching and conduction loss analysis of buck converters operating in DCM-only scenarios," *Proc. - IEEE Int. Symp. Circuits Syst.*, no. d, pp. 921–924, 2013.

[56] Synqor, "Input System Instability," 2017. [Online]. Available: www.synqor.com.

[57] L. Ibarra *et al.*, "On DC/DC voltage buck converter control improvement through the QFT approach," in *New Developments in Circuits, Systems, Signal Processing, Communications and Computers*, 2015, pp. 183–190.

[58] S. Waffler and J. W. W. Kolar, "Comparative evaluation of soft-switching concepts for bi-directional buck-boost dc-dc converters," *Power Electron. Conf. (IPEC), 2010 Int.*, vol. 24, no. 6, pp. 1856–1865, 2010.

[59] M. Gulin *et al.*, "Control of a DC Microgrid," *IEEE Trans. Ind. Electron.*, vol. 4, no. 3, pp. 395–402, 2015.

[60] T. Dragičević, J. M. Guerrero, J. C. Vasquez, and D. Škrlec, "Supervisory control of an adaptive regulated {DC} microgrid with battery management capability," vol. 29, no. 2, pp. 695–706, 2014.

[61] M. K. AL-Nussairi, R. Bayindir, S. Padmanaban, L. Mihet-Popa, and P. Siano, "Constant power loads (CPL) with Microgrids: Problem definition, stability analysis and compensation techniques," *Energies*, vol. 10, no. 10, 2017.

[62] C. Li, T. Dragicevic, M. G. Plaza, F. Andrade, J. C. Vasquez, and J. M. Guerrero, "Multiagent based distributed control for state-of-charge balance of distributed energy storage in DC microgrids," *IECON Proc. (Industrial Electron. Conf.*, pp. 2180–

2184, 2014.

[63] D. G. Assistant, S. Madhuri, G. K. Shanthi, B. Aparna, and P. Keerthana, “Design and Simulation of an Efficient LED Driver for Street Light Application,” *Int. J. Res. Appl. Sci. Eng. Technol.*, vol. 4, no. Iv, pp. 576–582, 2016.

[64] A. Shrivastava and B. Singh, “LLC series resonant converter based LED lamp driver with ZVS,” *2012 IEEE 5th Power India Conf. PICONF 2012*, 2012.

[65] L. H. Koh, Y. K. Tan, Z. Z. Wang, and K. J. Tseng, “An energy-efficient low voltage DC grid powered smart LED lighting system,” *IECON Proc. (Industrial Electron. Conf.*, pp. 2883–2888, 2011.

[66] D. E. LLC, “How to Reduce Office Energy Costs.” [Online]. Available: https://www.myledlightingguide.com/blog-how-to-reduce-office-energy-costs.

[67] A. a El Tayyan, “PV system behavior based on datasheet,” *J. Electron Devices*, vol. 9, no. January 2011, pp. 335–341, 2012.

[68] M. G. Villalva, J. R. Gazoli, and E. Ruppert Filho, “Modeling and circuit-based simulation of photovoltaic arrays,” *2009 Brazilian Power Electron. Conf. COBEP2009*, no. November, pp. 1244–1254, 2009.

[69] A. Bouraiou, M. Hamouda, A. Chaker, M. Sadok, M. Mostefaoui, and S. Lachtar, “Modeling and Simulation of Photovoltaic Module and Array Based on One and Two Diode Model Using Matlab/Simulink,” *Energy Procedia*, vol. 74, pp. 864–877, 2015.

[70] J. Park, H. Kim, Y. Cho, and C. Shin, “Simple Modeling and Simulation of Photovoltaic Panels Using Matlab / Simulink Modeling of Photovoltaic Module,” *Adv. Sci. Technol. Lett.*, vol. 73, no. Fgcn, pp. 147–155, 2014.

[71] A. Obbadi, Y. Errami, A. Elfajri, M. Agunaou, M. Benhmida, and S. Sahnoun, “Photovoltaic (PV) parameter estimation of a multicrystalline panel using developed iterative and non-iterative methods,” *Proc. 2015 IEEE Int. Renew. Sustain. Energy Conf. IRSEC 2015*, no. December, 2016.

[72] E. Rodriguez-Diaz, F. Chen, J. C. Vasquez, J. M. Guerrero, R. Burgos, and D. Boroyevich, “Voltage-Level Selection of Future Two-Level LVdc Distribution Grids: A Compromise Between Grid Compatibiliy, Safety, and Efficiency,” *IEEE Electrif. Mag.*, vol. 4, no. 2, pp. 20–28, 2016.

[73] Mathworks, “Battery,” 2018. .

[74] D. J. Becker and B. J. Sonnenberg, “DC microgrids in buildings and data centers,” in *2011 IEEE 33rd International Telecommunications Energy Conference (INTELEC)*, 2011, pp. 1–7.

[75] P. Biczel, S. Anand, B. G. Fernandes, S. Waffler, and J. W. W. Kolar, “Power Electronic Converters in DC Microgrid,” *2007 Compat. Power Electron.*, vol. 24, no. 6, pp. 1–6, 2010.

[76] T. Morstyn, B. Hredzak, and V. G. Agelidis, “Cooperative Control of DC Microgrid Storage for Energy Balancing and Equal Power Sharing,” no. October, pp. 1–6, 2014.