A Fill-In Technique for Robust IMD Suppression in Chopper Amplifiers

Rooijers, C.T.; Karmakar, S.; Kusuda, Y.; Huijsing, J.H.; Makinwa, K.A.A.

DOI
10.1109/JSSC.2021.3107350

Publication date
2021

Document Version
Final published version

Published in
IEEE Journal of Solid State Circuits

A Fill-In Technique for Robust IMD Suppression in Chopper Amplifiers

Thije Rooijers, *Member, IEEE*, Shoubhik Karmakar, *Student Member, IEEE*, Yoshinori Kusuda, *Member, IEEE*, Johan H. Huijsing, *Life Fellow, IEEE*, and Kofi A. A. Makinwa, *Fellow, IEEE*

***Abstract*— In chopper amplifiers, the interaction between the input signal and the chopper clock can give rise to intermodulation distortion (IMD). This chopper-induced IMD is mainly due to amplifier delay, which causes large pulses at the output of the amplifier's output chopper. This article proposes the use of a so-called fill-in technique to eliminate these pulses, and thus the resulting IMD, by multiplexing the outputs of two identical amplifiers that are chopped in quadrature. A prototype chopper-stabilized amplifier was implemented in a 180-nm CMOS process. Measurements show that the fill-in technique suppresses chopper-induced IMD by 28 dB, resulting in an IMD of −126 dB for input frequencies near $4F_{CH}$ (=80 kHz). It also improves the amplifier's two-tone IMD (with 79 and 80 kHz inputs) from −97 to −107 dB, which is the same as that obtained without chopping.**

***Index Terms*— Auto-zeroing, chopping, dynamic offset compensation (DOC), fill-in technique, intermodulation distortion (IMD), offset.**

I. Introduction

CMOS amplifiers suffer from offset (several millivolts), offset drift (several μV/°C), and $1/f$ noise corner (tens of kilohertz). Dynamic offset compensation (DOC) techniques, such as auto-zeroing and chopping, are often used to achieve low offset (microvolt level), offset drift (<20 nV/°C), and $1/f$ noise corners (several hertz). However, these techniques also have drawbacks. Some of these, such as the introduction of glitches, increased input current, and residual offset due to the charge-injection (mismatch) of switches, have been well studied [1], [2] and can be effectively mitigated [3]–[8]. This has led to precision CMOS amplifiers with no visible spectral content at the auto-zero/chop frequencies [6]–[8], very low input current (1 pA untrimmed, 0.2 pA trimmed [8]) and very low residual offset (100 nV [3]). This article focuses on the mitigation of a lesser-known drawback of DOC techniques: the generation of intermodulation distortion (IMD). In the presence of an ac input at a fixed input frequency (F_{in}), IMD will occur at the sum and difference of F_{in} and multiples of the DOC frequency F_{DOC}, i.e., at $F_{in} \pm nF_{DOC}$ and $nF_{DOC} \pm F_{in}$, where n is integer. In the case of auto-zeroing, this is due to its inherent sample and hold operation, which causes noise folding and large odd-order ($n = 1, 3, 5, \ldots$) IMD tones [8], [17], [18]. In the case of chopping, the main cause of even-order ($n = 2, 4, 6, \ldots$) IMD is amplifier delay, as will be discussed later in more detail.

In many chopper amplifiers, the chopping frequency (F_{CH}) is much higher than F_{in}. The resulting input-referred amplitude spectrum is shown in Fig. 1(a). It may be seen that the ripple caused by the up-modulated offset and $1/f$ noise can then be suppressed by a simple low-pass filter (LPF). The same filter will also suppress the tones near $2F_{CH}$ due to charge-injection

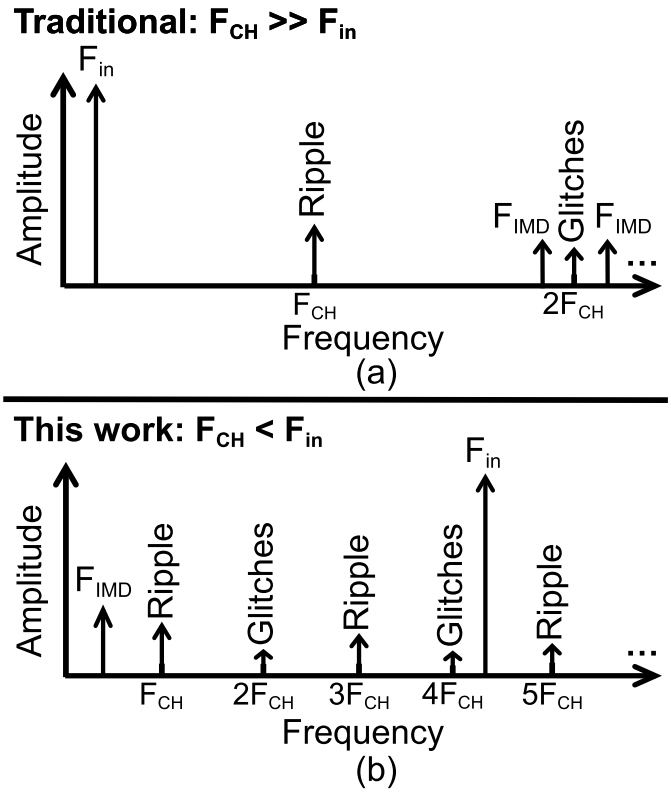

Fig. 1. Amplitude spectrum for: (a) traditional choice of F_{CH} ($F_{CH} \gg F_{in}$) and (b) the choice in this work ($F_{CH} < F_{IN}$), showing the resulting ripple, spikes, and IMD tones.

Manuscript received May 10, 2021; revised July 21, 2021; accepted August 20, 2021. Date of publication September 6, 2021; date of current version November 24, 2021. This article was approved by Associate Editor Man-Kay Law. *(Corresponding author: Thije Rooijers.)*

Thije Rooijers, Shoubhik Karmakar, Johan H. Huijsing, and Kofi A. A. Makinwa are with the Department of Microelectronics, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: c.t.rooijers@tudelft.nl).

Yoshinori Kusuda is with Analog Devices, Inc., San Jose, CA 95134 USA.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2021.3107350.

Digital Object Identifier 10.1109/JSSC.2021.3107350

glitches and chopper-induced IMD. However, to achieve a large tone-free signal bandwidth (BW), F_{CH} must be quite high, and will certainly be higher than the amplifier's original $1/f$ corner frequency. However, increasing F_{CH} results in lower effective gain, higher input current, and residual offset. For example, in [9], $F_{CH} = 333$ kHz, which results in 50 μV offset, 0.25 μV/°C offset drift, and 550 pA input current. In [10], inter-leaved 800 kHz clocks are used to achieve an effective $F_{CH} = 4.8$ MHz. This results in 5 μV offset and 0.02 μV/°C offset drift, but trimming is required to lower its input current to acceptable levels (from 1.5 nA to 150 pA).

This work focuses on chopper amplifiers in which F_{CH} is set only slightly higher than the $1/f$ corner frequency, and so will typically be lower than F_{in}. This choice results in the lowest residual offset, lowest input current, and largest effective gain, while still effectively suppressing $1/f$ noise. For example, in [11], F_{CH} is 30 kHz, which results in 1 μV offset, 22.5 nV/°C offset drift and an input current of 110 pA. However, as shown in Fig. 1(b), a simple LPF can no longer be used to filter out chopper ripple, and so other techniques are required, such as the use of a ripple-reduction loop [11], trimming [12] or auto-zeroing [13]. In addition, chopper-induced IMD tones will now be in-band and so cannot be easily filtered out.

In prior art [14]–[19], spread-spectrum chopper clocks were used to lower the magnitude of IMD tones by dithering F_{DOC}. This turns IMD tones, as well as chopper ripple, into noise-like signals, thus suppressing IMD tones (by ~10–20 dB) but increasing the noise floor around F_{DOC}. However, since this approach does not solve the underlying problem, the IMD is still visible in the time domain [15].

In this article, a novel fill-in technique is proposed to address the underlying cause of chopper-induced IMD [20]. When used in a prototype chopper-stabilized amplifier, it decreases IMD tones by 28 dB and results in a two-tone IMD of −107 dB for input frequencies near $4F_{CH}$ (=80 kHz), which is the same as that obtained without chopping.

The rest of the article is organized as follows. The origin of chopper-induced IMD is discussed in Section II. The operation of the proposed fill-in technique and the resulting amplifier architecture are discussed in Section III. Measurement results are shown and discussed in Section IV, and the article ends with the conclusions.

II. Origin of Chopper-Induced IMD

The cause of chopper-induced IMD can be understood by examining the signals in a chopped operational transconductance amplifier (OTA) in the presence of a sine-wave input signal V_{in} (Fig. 2). Due to the action of the input chopper (CH_{in}), the OTA's input V_1 will be an up-modulated version of V_{in}. Without loss of generality, the worst case scenario is shown, in which the chopping transition coincides with the peak of the input signal ($\hat{V}_{in}$). At this point, CH_{in} changes the polarity of the input signal, causing a $2\hat{V}_{in}$ step in V_1. This is converted into a current (I_1) by the OTA's transconductance G_m, and delayed by its finite BW (here modeled as a pure delay T_{delay}). As a result, the edges of the chopping clock (CH) will no longer be aligned with the corresponding transitions in I_1. The demodulated current (I_{out}) produced by the output chopper (CH_{out}) will then contain large pulses around the chopping transitions. The amplitude of these pulses ($2G_m\hat{V}_{in}$) is equal to the instantaneous amplitude of the input signal and so can be a significant source of distortion. These pulses are the main cause of chopper-induced IMD.

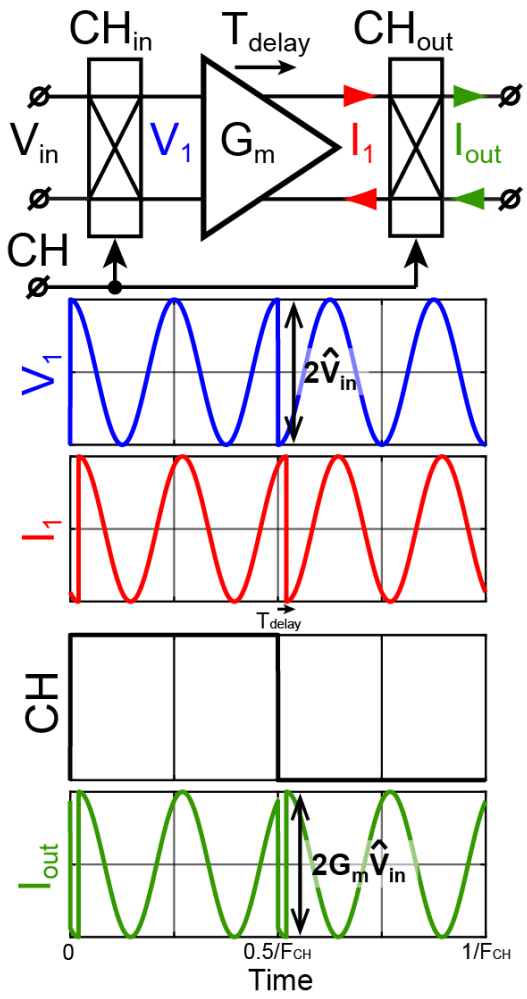

Fig. 2. Chopped OTA with a pure amplifier delay (T_{delay}) and the corresponding time-domain signals. The large pulses in the output current (I_{out}) result in chopper-induced IMD.

In the frequency domain, the effect of these pulses can be better understood by considering the simplified model of the chopped OTA shown in Fig. 3. This consists of a delay-free OTA with an extra input path, shown in red, that models the IMD pulses. In this path, V_{in} is multiplied by a sequence of rectangular pulses (p) with an amplitude of 2, a width of T_{delay}, and a period of $0.5/F_{CH}$. The result (pV_{in}) is then subtracted from V_{in} to model the pulses generated at the chopping transitions.

In the frequency domain, it can be seen that the multiplication in the extra path will fold input signals near multiples of $2F_{CH}$ back to dc. The spectra of the various signals in Fig. 3 are shown in Fig. 4, where the input is assumed to have a narrow-band spectrum ($V_{in}(f)$) centered on $4F_{CH}$. At low frequencies, the spectrum of the rectangular

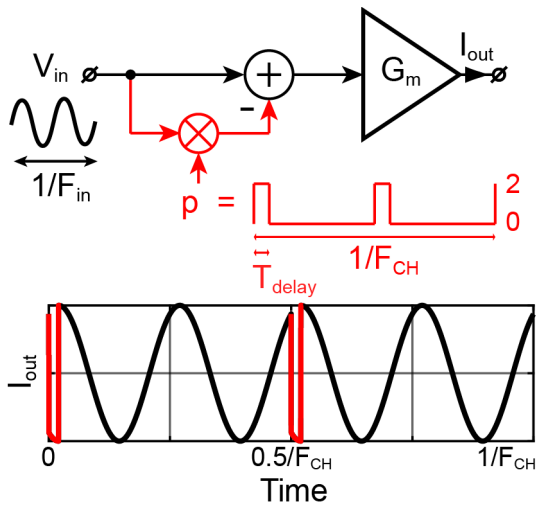

Fig. 3. Simplified model for a chopped OTA with a pure delay and the resulting waveform.

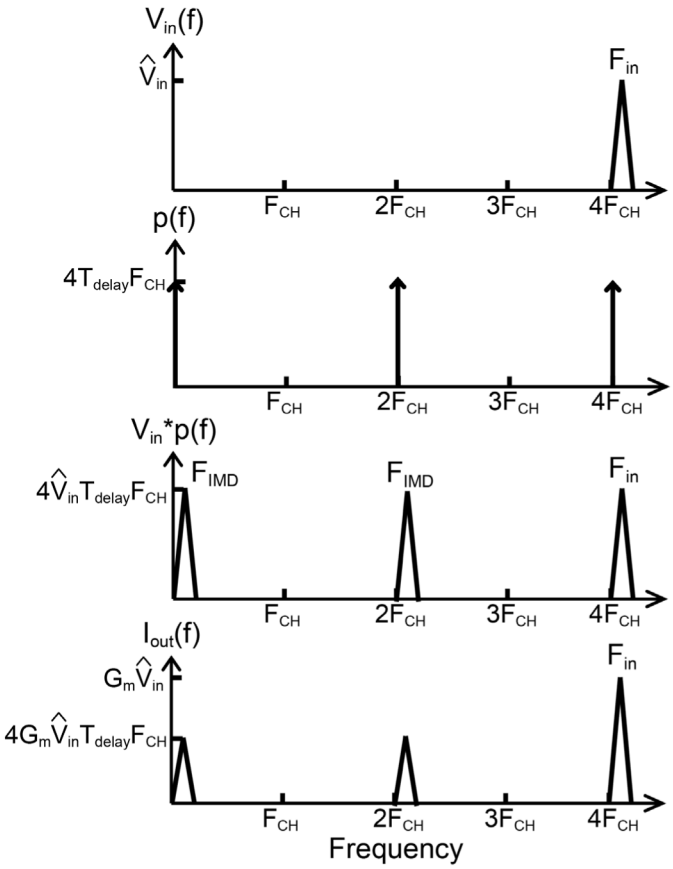

Fig. 4. Amplitude spectra of the different signals in the simplified model of a chopped OTA for a narrow-band triangular input spectrum.

pulses ($p(f)$) consists of impulses at multiples of $2F_{\mathrm{CH}}$ with an amplitude of $4T_{\mathrm{delay}}F_{\mathrm{CH}}$ (see Appendix). As a result, the convolution $V_{\mathrm{in}} * p(f)$ consists of scaled and frequency-shifted versions of the input spectrum, which are subtracted from V_{in} and applied to the ideal OTA. The amplitude of the IMD tones in the resulting output current $I_{\mathrm{out}}(f)$ are then given by

$$\mathrm{IMD} = 20\log\left(4T_{\mathrm{delay}}F_{\mathrm{CH}}\right). \tag{1}$$

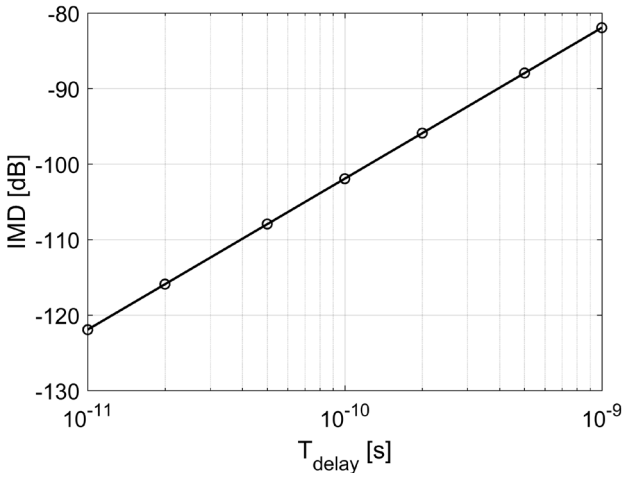

Fig. 5. Chopper-induced IMD tones versus the OTA delay for a fixed F_{CH} of 20 kHz.

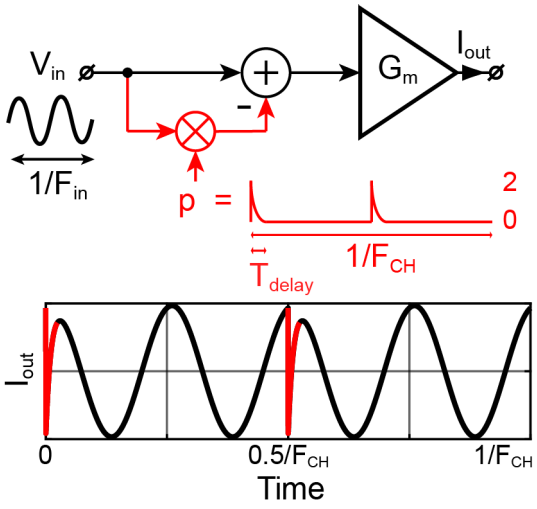

Fig. 6. Simplified model for a chopped OTA with limited BW and the resulting waveform.

For a fixed F_{CH} of 20 kHz, the IMD predicted by (1) is plotted in Fig. 5 for various values of T_{delay}. It can be seen that a delay of only 1 ns results in a chopper-induced IMD of 82 dB. Decreasing the delay causes the amplitude of the IMD tones to roll-off at the rate of 20 dB/decade.

Rather than the rectangular pulses considered so far, finite OTA BW will cause exponentially settling pulses at the output of $\mathrm{CH}_{\mathrm{out}}$. This can be incorporated in the chopped OTA model (Fig. 3) by modifying the shape of the pulse sequence $p(t)$, as shown in Fig. 6. Noting that $T_{\mathrm{delay}} = 1/(2\pi\,\mathrm{BW})$, (1) can be rewritten in terms of amplifier BW

$$\mathrm{IMD} = 20\log\left(\frac{4F_{\mathrm{CH}}}{2\pi\,\mathrm{BW}}\right). \tag{2}$$

This equation predicts that the IMD can be reduced by increasing the OTA's BW. However, this comes at the expense of significantly higher OTA power dissipation. In this work, an OTA with a noise density of 11 nV/Hz and a 15 MHz BW is employed, which corresponds to a delay of ~10 ns.

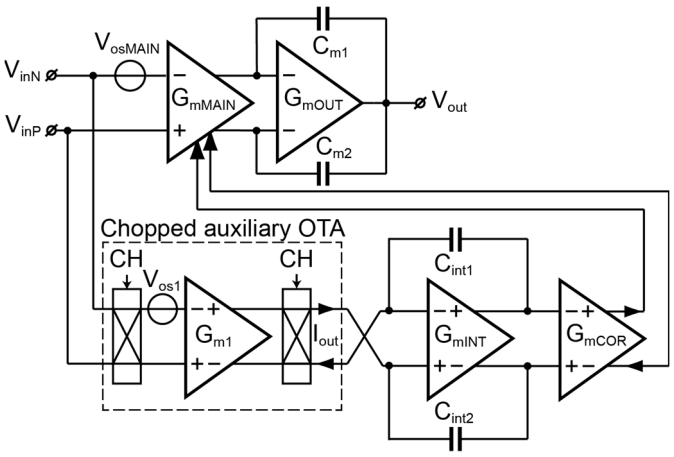

Fig. 7. Simplified block diagram of the chopper-stabilized amplifier.

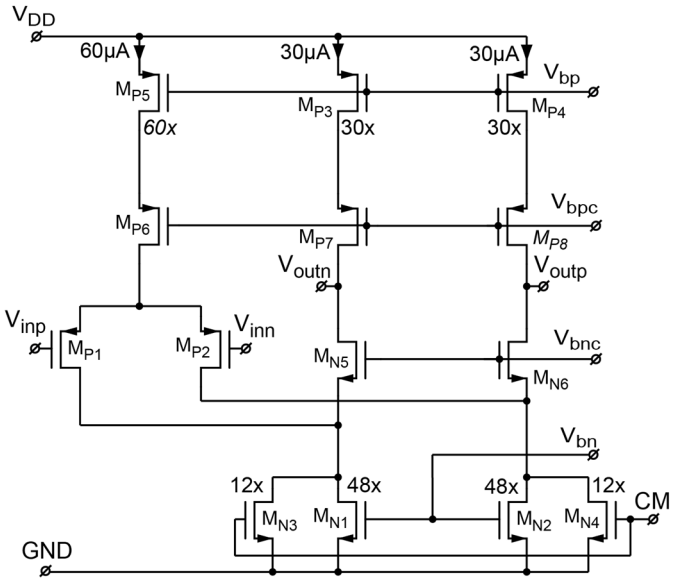

Fig. 8. Schematic of G_{m1} and G_{m2}.

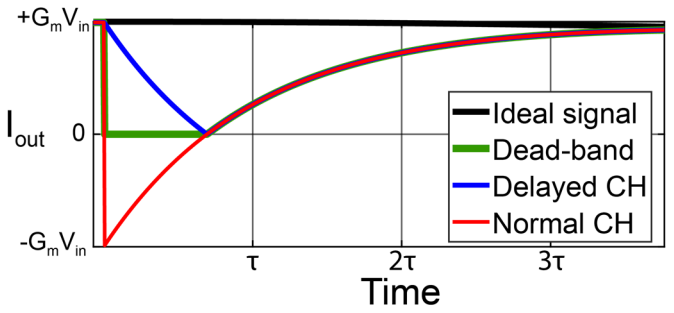

Fig. 9. Zoom-in of the pulse in I_{out} versus time for: ideal signal (no pulse), dead-band chopping, delayed output chopping, and normal chopping.

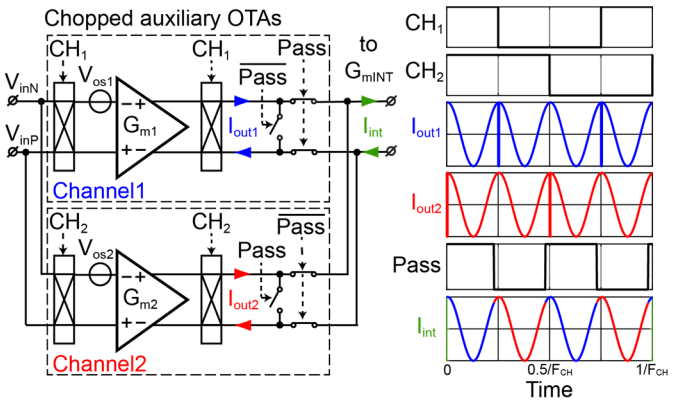

Fig. 10. Fill-in technique for the chopped auxiliary OTA.

To achieve the 28 dB reduction in chopper- induced IMD reported in this work, a 25× increase in BW, and thus power would be required.

III. Proposed Amplifier Topology With Fill-In Technique

A simplified block diagram of the proposed chopper-stabilized amplifier is shown in Fig. 7. It consists of a two-stage main amplifier with a folded-cascode input stage (G_{mMAIN}) and a Class AB output stage (G_{mout}) with Miller compensation capacitors (C_{m1} and C_{m2}, 10 pF each), and Miller-zero compensation resistor (not shown, 5.4 kΩ). The offset and $1/f$ noise of the main amplifier (V_{osMAIN}) are suppressed by a three-stage auxiliary amplifier. To minimize its own offset (V_{os1}) and $1/f$ noise, the auxiliary amplifier employs a chopped OTA (G_{m1}, folded-cascode Fig. 8), followed by an integrator (G_{mINT}, folded-cascode, and $C_{int1-int2}$, each 36 pF), and a correction OTA (G_{mCOR}, telescopic).

When used in a negative feedback configuration, the offset of the main amplifier (V_{osMAIN}) appears at the input of the chopped G_{m1}, whose output current is integrated (G_{mINT}) to generate, via G_{mCOR}, an offset-correcting signal for the main amplifier (G_{mMAIN}). Due to the amplifier's finite gain, the application of an ac input signal will give rise to a finite swing at the input of the chopped auxiliary OTA, whose finite BW then causes chopper-induced IMD in its output current (I_{out}). The resulting tones will be somewhat suppressed by the active integrator. However, input frequencies close to $2F_{CH}$ (or $4F_{CH}$, $6F_{CH}$, etc.,) will cause IMD tones near dc, and so will not be suppressed.

To reduce the effect of near-dc IMD tones, the magnitude of the pulses in I_{out} should be reduced. One possibility would be to introduce a dead-band, as is sometimes done to mitigate the effect of chopping glitches [21]. In other words, make $I_{out} = 0$ for the duration of the pulses (Fig. 9). However, this will only reduce the amplitude of the pulses by about half: to $G_m V_{in}$ from $2G_m V_{in}$. In the case of exponential settling, simulations show that the IMD reduction is limited to about 2 dB for the optimal dead-band, which ends at the zero-crossing of I_{out} (Fig. 9). Another solution would be to delay the clock of the output chopper to compensate for the OTA delay. However, simulations show that the IMD reduction is then limited to about 4 dB for the optimal delay, which again ends at the zero-crossing of I_{out} (Fig. 9). The limited effectiveness of these techniques can be attributed to their inability to compensate for the long settling tail of I_{out} after the zero-crossing.

The goal of the proposed fill-in technique is to suppress chopper-induced IMD by eliminating the pulses in I_{out}. As shown in Fig. 10, this can be done by using *two* identical auxiliary OTAs (G_{m1} and G_{m2}), which are chopped

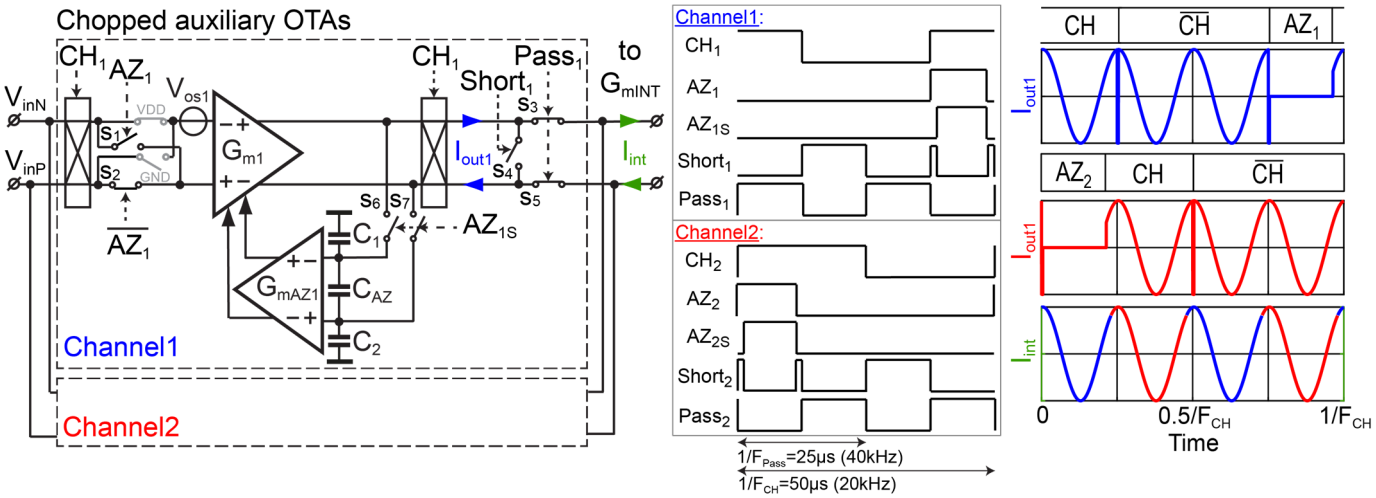

Fig. 11. Fill-in technique combined with auto-zeroing (left), timing diagram (middle), and the corresponding signals (right).

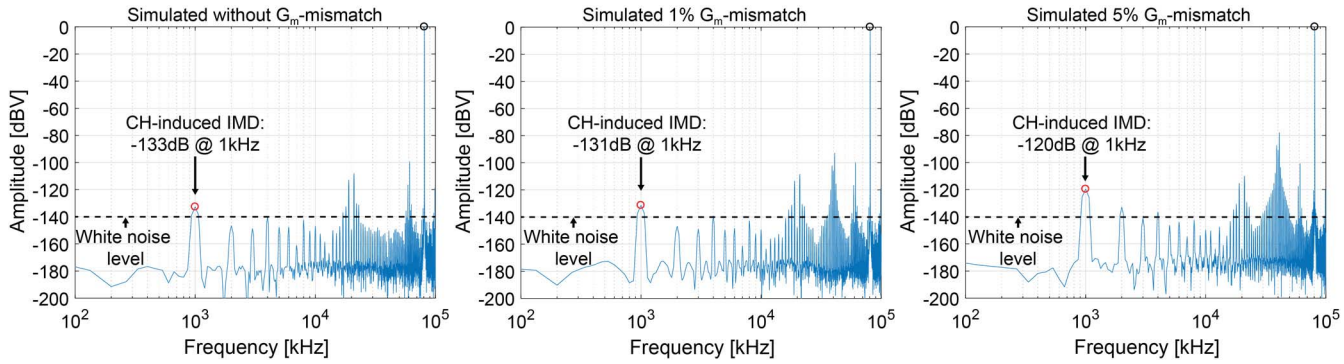

Fig. 12. Simulated amplitude spectrum without G_m-mismatch, 1% of mismatch, and 5%.

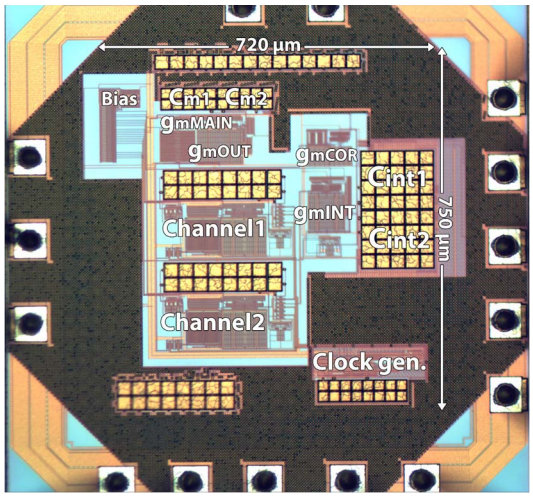

Fig. 13. Die micrograph.

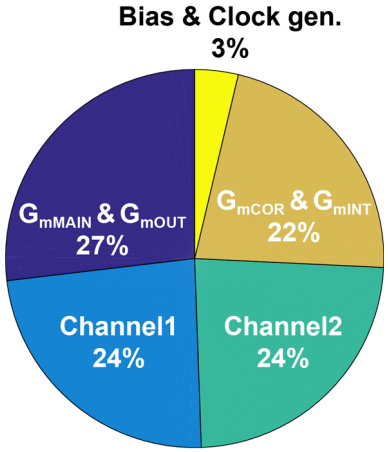

Fig. 14. Power breakdown of the most important blocks.

in quadrature (CH_1 and CH_2). Although the output current of each channel (I_{out1} and I_{out2}) will still contain pulses around the chopping transitions, these will only occur in one channel at a time. The OTAs' output currents ($I_{out1,2}$) are nominally identical, and so, by selecting the appropriate current slightly before each chopping transition, a combined output current can be generated that is free of pulses and, therefore, free of IMD. In other words, the pulses of one OTA are *filled in* by the output current of the other. The key insight is that the required switches can select the OTA's output currents much faster than the OTAs themselves can settle.

However, the chopped offset of G_{m1} and G_{m2} (V_{os1} and V_{os2}) will still cause ripple. To suppress this, the proposed fill-in technique is combined with auto-zeroing (Fig. 11). An AZ loop is added, which is used to AZ the OTA when it is not connected to G_{mINT}. To prevent input common-mode (CM)

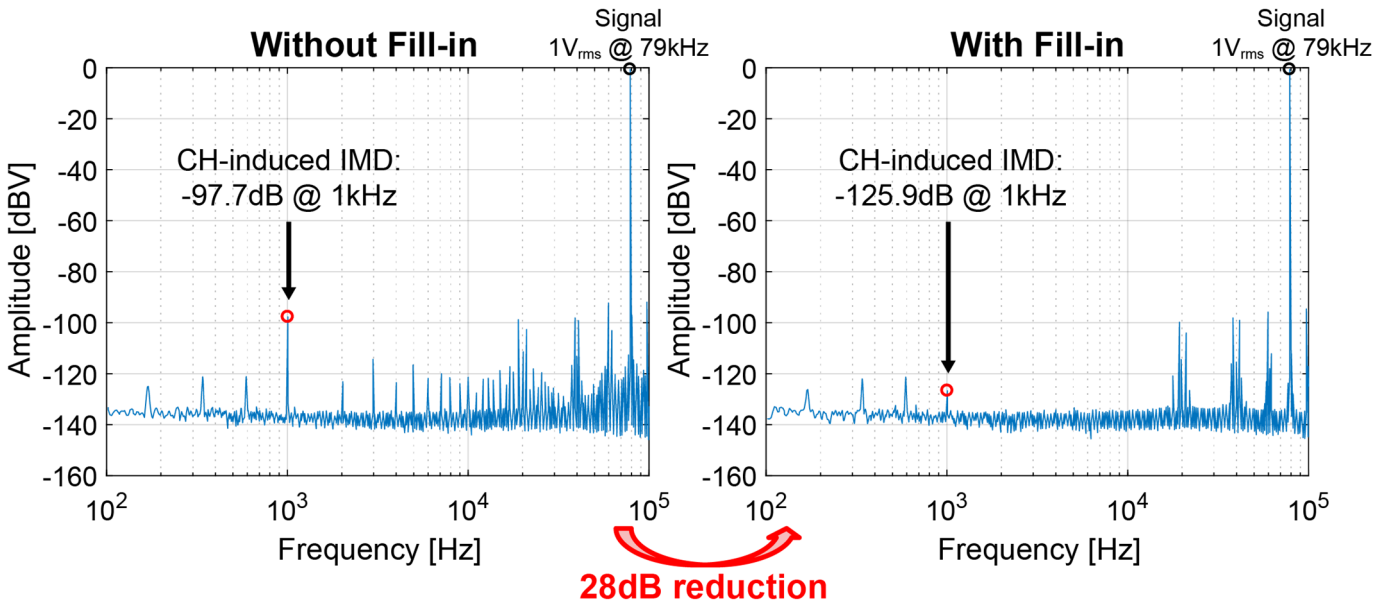

Fig. 15. Measured amplitude spectrum (ten averages) for a one-tone test of 79 kHz 1 V_{rms} for fill-in disabled and enabled.

transients, which would cause additional IMD, the OTA inputs are shorted to one of the input pins during the AZ phase (via S_1). Dummy always-closed and always-open switches (in gray) ensure that the input network formed by the switch resistances and the parasitic capacitance is symmetric. During the AZ phase, C_{AZ} (25 pF) acts as a passive integrator whose output drives G_{mAZ1} (Telescopic) to cancel the OTA's offset. The resulting voltage is held by $C_{1,2}$ (1.8 pF each) during the amplification phase. To minimize noise folding, the noise BW during the AZ phase should be limited by minimizing G_{mAZ1}, but this increases the OTA's worst case output swing. As a compromise, G_{mAZ1} is chosen to be $\sim$50$\times$ smaller than G_{m1}.

At the start of the AZ phase, the output current of the OTA needs to transition from a level that depends on the input signal to a level that is nearly zero. To prevent these transients from reaching the AZ loop and thus causing additional IMD, shorting switch S_4 allows the OTA current to settle before it is connected via switches $S_{6\&7}$ to the integration capacitor C_{AZ} [22]. $S_{6\&7}$ are controlled by the $\text{AZ}_{1\text{S}}$ signal, which includes a dead-band that disconnects C_{AZ} during this settling time. The width of the dead-band is set to 100 ns, which guarantees OTA settling in the worst case corner. Similarly, the AZ phase is ended roughly 100 ns before the next chopping phase, allowing $G_{\text{m1,2}}$ to settle before it is connected to G_{mINT}. To further minimize the voltage transient that occurs when the OTA is connected to G_{mINT}, the shorting switch (S_4) resistance is set to $\sim 1/G_{\text{mINT}}$ (6.8 kΩ). The remaining voltage transients are then mainly due to the charge-injection of the multiplexing switches (S_3 and S_5).

The effectiveness of the fill-in technique is limited by the G_{m} matching of the two input OTAs, as any mismatch will cause additional transients in their composite output current. With a 1 V_{rms} 81 kHz input signal, the results of simulations with various degrees of intentional G_{m} mismatch are shown in Fig. 12. Without mismatch, the simulated chopper-induced IMD is -133 dB, increasing only slightly to -131 dB for 1% mismatch, which is readily achievable. Even with 5% mismatch, -120 dB IMD can still be achieved, showing that in practice, G_{m} mismatch is not an important limiting factor.

IV. Measurement Results

The prototype chopper-stabilized amplifier with fill-in technique was realized in a 0.18 μm CMOS BCD process. The die micrograph is shown in Fig. 13, with the most important blocks highlighted. It occupies an active area of 0.54 mm^2 and draws 550 μA from a 5 V supply. The opamp has a 0–4.5 V input CM range, a 15.4 noise efficiency factor (NEF), and a 4.2 MHz gain bandwidth product (GBW). A power breakdown is shown in Fig. 14. It is equally split between the main amplifier, Channel 1, Channel 2, and the rest of the stabilization loop. The first three all have low noise input stages and so dissipate significant power. Furthermore, at high input frequencies, the signal entering the stabilization loop increases due to the roll-off of amplifier gain. To handle the resulting high current levels output by the input OTAs, the stabilization loop also dissipates significant power.

With the prototype amplifier configured as a buffer, a one-tone test was performed using an Audio Precision APx555 analyzer, which provides a 1 V_{rms} 79 kHz input tone at an input CM level of 2.2 V. To ensure that the IMD tones are well above the $\sim$134 dB noise floor, an input tone near $4F_{\text{CH}}$ (79 kHz) was used rather than one near $2F_{\text{CH}}$ (39 kHz). The resulting output amplitude spectrum is shown in Fig. 15. The 79 kHz input tone, together with the chopping frequency of 20 kHz, leads to an IMD tone at 1 kHz ($4F_{\text{CH}}$–F_{in}). Without the fill-in technique, a large (-97.7 dB) IMD tone is present. With the fill-in technique enabled, this drops by 28 to -125.9 dB. Some power-line interference is also visible below 1 kHz. This is present even in the absence of the prototype chip and is thus caused by the measurement setup. Higher-order IMD tones (>1 kHz) are also partly

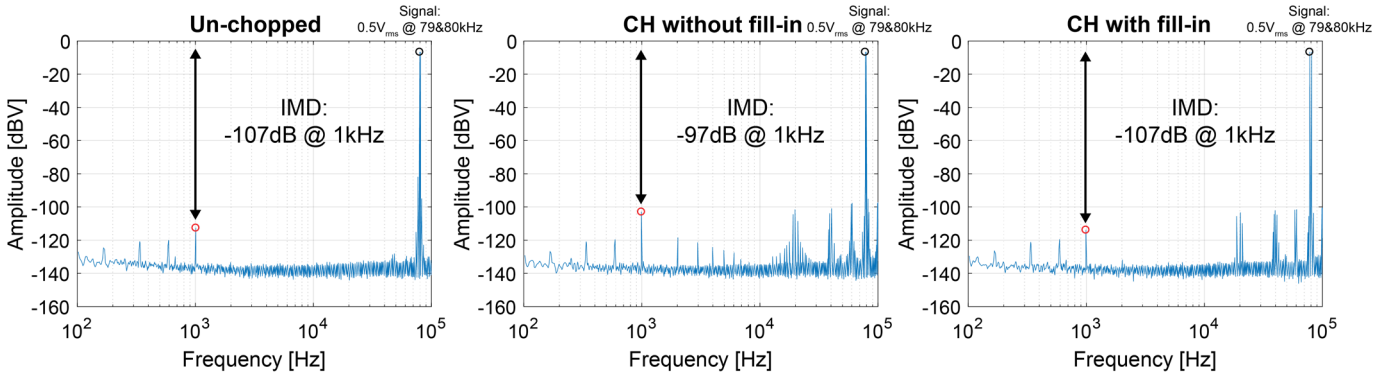

Fig. 16. Measured amplitude spectrum (ten averages) for a two-tone test of 79 and 80 kHz tone 0.5 $V_{\rm rms}$ each, for the case of the un-chopped amplifier, chopped without fill-in, and with fill-in.

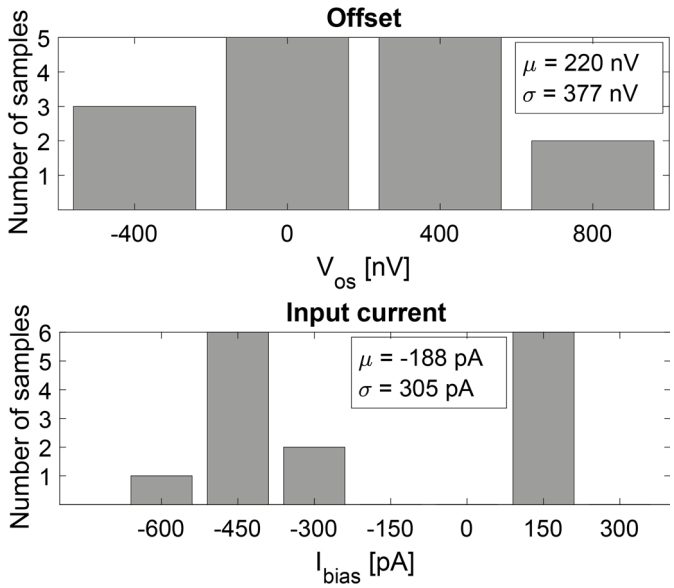

Fig. 17. Histogram of the offset voltage and input current for 15 samples.

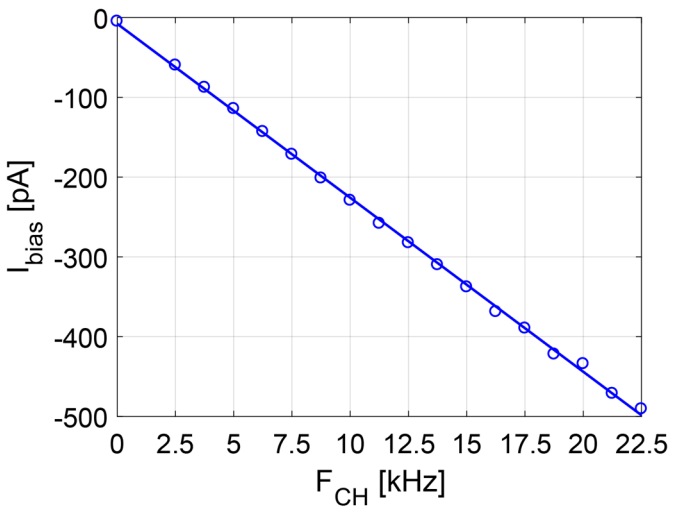

Fig. 18. Input current for different chopping frequencies.

suppressed by the fill-in technique. Some residual ripple is also present at multiples of $F_{\rm CH}$.

A two-tone test was also performed using tones at 79 and 80 kHz, both with an amplitude of 0.5 $V_{\rm rms}$. The resulting amplitude spectrum is shown in Fig. 16. As a baseline, the two-tone IMD was first measured with chopping disabled. Due to the amplifier's own non-linearity, an IMD tone of -107 dB can be seen at 1 kHz. When chopping is enabled, but without the fill-in technique, this tone increases to -97 dB, which is mainly due to chopper-induced IMD. With the fill-in technique enabled, the IMD drops back to -107 dB, demonstrating the effective suppression of chopper-induced IMD.

With a 2.5 V input CM voltage and $F_{\rm CH} = 20$ kHz, measurements on 15 samples show that the offset is less than 0.8 μV, while the input current is less than 600 pA (Fig. 17). The input current was measured by a Keithley 6514 electrometer, and guarding was used to minimize printed circuit board (PCB) leakage. The input current is a linear function of $F_{\rm CH}$ (Fig. 18), indicating that it is mainly due to the charge-injection (mismatch) of the chopper and AZ switches.

The opamp's voltage noise density is shown in Fig. 19. With chopping disabled, its white-noise level is 16 nV$\sqrt{\rm Hz}$ and its $1/f$ corner frequency is $\sim$6 kHz. With chopping, auto-zeroing and fill-in enabled, the $1/f$ corner frequency is less than a few Hertz. The noise folding associated with auto-zeroing each OTA at 20 kHz causes a slight noise bump around this frequency. Some tones can also be seen at the chopping/auto-zeroing frequencies, which is due to PCB-mediated crosstalk between the 5 V reference clock (80 kHz) and the prototype chip.

To verify the amplifier's ability to handle rapidly changing signals, its slew rate was measured by applying a 4 V input step (Fig. 20). For both rising and falling steps, the speed at which the amplifier's output transitions from 10% to 90% of its final value corresponds to a slew rate of 1.7 V/μs.

Fig. 21 shows the measured power supply rejection ratio (PSRR) of the amplifier using a 1 $V_{\rm rms}$ disturbance added to the 5 V supply at different frequencies. At low frequencies, the PSRR is 124 dB, rolling off at higher frequencies.

Table I summarizes the performance of the amplifier and compares it to other DOC amplifiers using chopping, auto-zeroing, or a combination of the two. Table I reports the

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE-OF-THE-ART

	This work	AD8551 [17]	AD8571 [18]	Ivanonv [19]	Rooijers [8]	
Dynamic technique(s)	**Chopper Stabilized with Auto-zeroing**	Auto-zero Stabilized	Auto-zero Stabilized	Chopper Stabilized with ripple-reduction	Auto-zero and Chopped Stabilization	
Chopper-induced IMD tone (dB @ f_{IMD})	**f_{in}=79 kHz -97.7 (No Fill-in) -125.9 (Fill-in) @ 1 kHz**	f_{in}=0.5 kHz -80 (Single)* - @ 4.5 kHz	f_{in}=0.5 kHz - -90 (Spread)* @ 4.5 kHz	f_{in}=1 kHz -103 (Single)** -122.7 (Spread)** @ 156 kHz	f_{in}=1 kHz -91 (Single) - @ 14 kHz	f_{in}=16 kHz -44 (Single) - @ 1 kHz
Offset (Max)	**0.8 µV*** **	5 µV	5 µV	3.5 µV	0.6 µV***	
Input current (Max)	**600 pA*** **	50 pA	50 pA	200 pA	1 pA (untrimmed)*** 0.2 pA (trimmed)***	
Voltage noise density (nV/√Hz)	**16**	42	51	6.5	20	
CH/AZ frequency (kHz)	**20**	4	2-4	50-150	15	
GBW (MHz)	**4.2**	1.5	1.5	10	1.45	
Slew rate (V/µs)	**1.7**	0.4	0.4	5	-	
PSRR (dB)	**124**	130	130	135	125	
Supply voltage	**5 V**	5 V	5 V	1.8 - 5.5 V	1.8 V	
Supply current	**0.55 mA**	0.85 mA	0.85 mA	1.65 mA	0.21 mA	
Technology	**0.18 µm**	-	-	0.6 µm	0.18 µm	
Die Area (mm^2)	**1.25**	-	-	1.626	1.4	

*V_{out}=1 V_{rms}@500 Hz (A=40 dB) [14] **V_{out}=1 V_{rms}@1 kHz (A=1) ***Maximum value of 15 sample

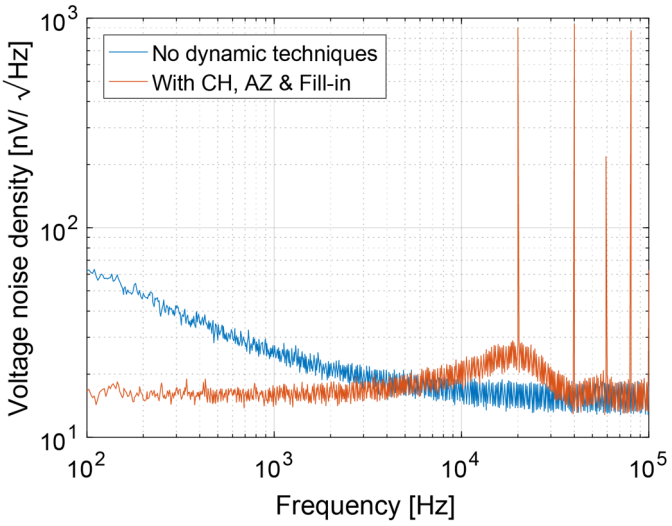

Fig. 19. Voltage noise density versus frequency for the case without any dynamic techniques and with CH, AZ, and fill-in.

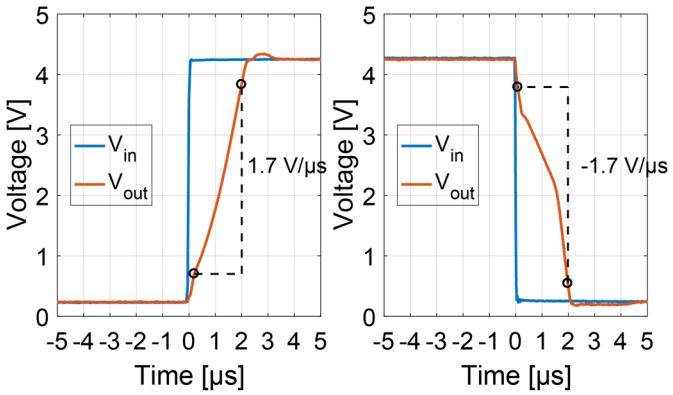

Fig. 20. Slew-rate measurement for a step-up and step-down.

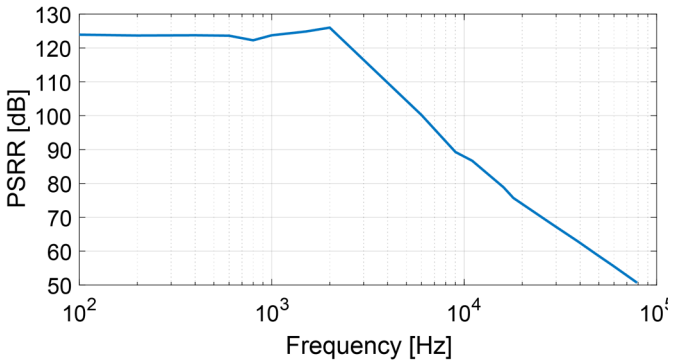

Fig. 21. Measured PSRR versus frequency.

IMD of amplifiers that use both fixed DOC frequencies (Single) [8], [17] and spread-spectrum DOC frequencies (Spread) [18], [19]. For the latter, the IMD with a fixed DOC frequency is also reported (Single), where it should be noted that [17] and [18] describe the same amplifier. Although the reported IMD of the proposed amplifier is obtained from a single sample, the variation between five samples has been measured. Without the fill-in technique, the single-tone IMD varies between −97.2 and −98.2 dB. With the fill-in technique enabled, the IMD varies between −125 and −131 dB. The amplifier achieves the lowest IMD (125.9 dB) at a much higher input frequency (79 kHz), which is more difficult to achieve due to the roll-off of amplifier gain with frequency. Furthermore, at worst case input frequencies ($f_{in} = nf_{AZ}$ with

$n = 1, 3, 5, \ldots$ or $f_{\text{in}} = nf_{\text{CH}}$ with $n = 2, 4, 6, \ldots$), which will cause near-dc IMD tones, an 81.9 dB improvement is obtained. For low input frequencies (<1 kHz), the IMD tones are below the −134 dB noise floor. Even though an additional low-noise input stage is required to implement the fill-in technique, the amplifier's total supply current (0.55 mA) is comparable with that of other designs. Each fill-in channel uses 24% of the power and 10% of the total active area.

V. Conclusion

In chopper amplifiers, finite amplifier delay gives rise to short pulses around the chopping transitions, which in turn give rise to significant amounts of chopper-induced IMD. To address this problem, a novel fill-in technique is proposed, in which two identical amplifiers are chopped in quadrature such that a pulse-free output signal can be obtained by selecting the output of the appropriate amplifier. As a proof of concept, the fill-in technique was used in a chopper-stabilized amplifier, resulting in a 28 dB reduction of its chopper-induced IMD. This corresponds to less than −125 dB of chopper-induced IMD for a single-tone near $4F_{\text{CH}}$ (=80 kHz), while the two-tone IMD (with 79 and 80 kHz tones) is less than −105 dB, mainly limited by the amplifier's own linearity. In addition, the amplifier achieves low offset (<1 μV) and low noise (16 nV$\sqrt{\text{Hz}}$), while its supply current (0.55 mA from a 5 V supply) is comparable with that of other state-of-the-art precision amplifiers.

Appendix

In this appendix, the amplitude spectra for the different signals in Fig. 3 are determined.

The sequence of rectangular pulses (p) can be described by the convolution

$$p(t) = 2\text{rect}(T_{\text{delay}}t) * \sum_{n=-\infty}^{\infty} \delta\left(t - \frac{n}{2F_{\text{CH}}}\right) \tag{3}$$

where the rectangular function represents the short pulse caused by amplifier delay and the impulse train represents its repetition rate (every $0.5/F_{\text{CH}}$). The Fourier transform of the first term is

$$2T_{\text{delay}}\text{sinc}(T_{\text{delay}}f) \tag{4}$$

and the Fourier transform of the second term is

$$2F_{\text{CH}} \sum_{n=-\infty}^{\infty} \delta(f - n2F_{\text{CH}}). \tag{5}$$

The convolution in the time-domain leads to a multiplication in the frequency-domain, which results in

$$p(f) = 4T_{\text{delay}}F_{\text{CH}}\text{sinc}(T_{\text{delay}}f) \sum_{n=-\infty}^{\infty} \delta(f - n2F_{\text{CH}}). \tag{6}$$

The notches of $\text{sinc}(T_{\text{delay}}f)$ occur at n/T_{delay} with $n = 1, 2, 3, \ldots$. At low frequencies, the effect of the sinc function is negligible for a small T_{delay}. The multiplication pV_{in} leads to the convolution

$$\begin{aligned} p * V_{\text{in}}(f) &= 4T_{\text{delay}}F_{\text{CH}}\text{sinc}(T_{\text{delay}}f) \sum_{n=-\infty}^{\infty} \delta(f - n2F_{\text{CH}}) * V_{\text{in}}(\text{f}) \\ &= 4T_{\text{delay}}F_{\text{CH}}\text{sinc}(T_{\text{delay}}f) \sum_{n=-\infty}^{\infty} V_{\text{in}}(f - n2F_{\text{CH}}). \end{aligned} \tag{7}$$

The frequency shifted versions of the input spectrum lead to the IMD tones. pV_{in} is subtracted from V_{in} and multiplied by G_{m}, leading to an output current spectrum ($I_{\text{out}}(f)$) of

$$\begin{aligned} I_{\text{out}}(f) = G_{\text{m}}V_{\text{in}} &- 4T_{\text{delay}}F_{\text{CH}}\text{sinc}(T_{\text{delay}}f) \\ &\times G_{\text{m}} \sum_{n=-\infty}^{\infty} V_{\text{in}}(f - n2F_{\text{CH}}). \end{aligned} \tag{8}$$

References

[1] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization," *Proc. IEEE*, vol. 84, no. 11, pp. 1584–1614, Nov. 1996.

[2] Q. Fan, J. H. Huijsing, and K. A. A. Makinwa, "Input characteristics of a chopped multi-path current feedback instrumentation amplifier," in *Proc. 4th IEEE Int. Workshop Adv. Sens. Interfaces (IWASI)*, Jun. 2011, pp. 61–66.

[3] C. Menolfi and Q. Huang, "A fully integrated, untrimmed CMOS instrumentation amplifier with submicrovolt offset," *IEEE J. Solid-State Circuits*, vol. 34, no. 3, pp. 415–420, Mar. 1999.

[4] A. Bakker, K. Thiele, and J. H. Huijsing, "A CMOS nested-chopper instrumentation amplifier with 100-nV offset," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1877–1883, Dec. 2000.

[5] R. Burt and J. Zhang, "A micropower chopper-stabilized operational amplifier using a SC notch filter with synchronous integration inside the continuous-time signal path," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2729–2736, Dec. 2006.

[6] T. Rooijers, J. H. Huijsing, and K. A. A. Makinwa, "A quiet digitally assisted auto-zero-stabilized voltage buffer with 0.6 pA input current and 0.6 μV offset," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 50–52.

[7] T. Rooijers, J. H. Huijsing, and K. A. A. Makinwa, "An auto-zero stabilized voltage buffer with a quiet chopping scheme and constant input current," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 298–299.

[8] T. Rooijers, J. H. Huijsing, and K. A. A. Makinwa, "An auto-zero stabilized voltage buffer with a trimmed input current of 0.2 pA," in *Proc. IEEE 45th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2019, pp. 257–260.

[9] Texas Instruments. (Oct. 2009). *OPA378 Data Sheet*. [Online]. Available: https://www.ti.com/lit/ds/symlink/opa378.pdf

[10] Y. Kusuda, "A 60 V auto-zero and chopper operational amplifier with 800 kHz interleaved clocks and input bias current trimming," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2804–2813, Dec. 2015.

[11] Q. Fan, J. H. Huijsing, and K. A. A. Makinwa, "A 21 nV/$\sqrt{\text{Hz}}$ Chopper-stabilized multi-path current-feedback instrumentation amplifier with 2 μV offset," *IEEE J. Solid-State Circuits*, vol. 47, no. 2, pp. 464–475, Feb. 2012.

[12] I. Akita and M. Ishida, "A 0.06 mm^2 14nV/$\sqrt{\text{Hz}}$ Chopper instrumentation amplifier with automatic differential-pair matching," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 178–179.

[13] A. T. K. Tang, "A 3 μV-offset operational amplifier with 20 nV/$\sqrt{\text{Hz}}$ input noise PSD at DC employing both chopping and autozeroing," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2002, pp. 386–387.

[14] E. C. J. Brown, "Chopper-stabilized amplifier with spread-spectrum clocking," U.S. Patent 5 115 202 A, May 19, 1992.

[15] A. T. K. Tang, "Bandpass spread spectrum clocking for reduced clock spurs in autozeroed amplifiers," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, vol. 1, May 2001, pp. 663–666.
[16] Maxim Integrated. (Feb. 2018). *MAX4238/MAX4239 Data Sheet*. [Online]. Available: https://datasheets.maximintegrated.com/en/ds/MAX4238-MAX4239.pdf
[17] Analog Devices. (Jun. 2015). *AD8551 Data Sheet*. [Online]. Available: http://www.analog.com/media/en/technical-documentation/datasheets/AD8551_8552_8554.pdf
[18] Analog Devices Inc. (1999). *AD8571 Data Sheet*. [Online]. Available: http://www.analog.com/media/en/technical-documentation/data-sheets/AD8571_8572_8574.pdf
[19] V. Ivanov and M. Shaik, "A 10 MHz-bandwidth 4 μs-large-signal-settling 6.5nV/$\sqrt{}$Hz-noise 2 μV-offset chopper operational amplifier," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016, pp. 88–89.
[20] T. Rooijers, S. Karmakar, Y. Kusuda, J. H. Huijsing, and K. A. A. Makinwa, "A Chopper-stabilized amplifier with -107 dB IMD and 28 dB suppression of Chopper-induced IMD," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2021, pp. 438–440.
[21] Q. Huang and C. Menolfi, "A 200 nV offset 6.5 nV/$\sqrt{}$Hz noise PSD 5.6 kHz Chopper instrumentation amplifier in 1 μm digital CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2001 pp. 362–363.
[22] M. A. P. Pertijs and W. J. Kindt, "A 140 dB-CMRR current-feedback instrumentation amplifier employing ping-pong auto-zeroing and chopping," *IEEE J. Solid-State Circuits*, vol. 45, no. 10, pp. 2044–2056, Oct. 2010.

Thije Rooijers (Member, IEEE) was born in Leiden, The Netherlands, in 1991. He received the B.Sc. and M.Sc. degrees in electrical engineering from Delft University of Technology, Delft, The Netherlands, in 2013 and 2016, respectively, where he is currently pursuing the Ph.D. degree with a focus on reducing the imperfections of dynamic offset compensated amplifiers.

Mr. Rooijers was a recipient of the ADI Outstanding Student Designer Award in 2018, the ProRISC Best Oral Presentation Award in 2019, and the ProRISC Best Poster Award in 2021.

Shoubhik Karmakar (Student Member, IEEE) received the B.E. degree in electrical and electronics engineering from Birla Institute of Technology and Science, Pilani, India, in 2012, and the M.Sc. degree from Delft University of Technology, Delft, The Netherlands, in 2017, where he is currently pursuing the Ph.D. degree.

His current research interests include energy-efficient data converters and high-performance class-D amplifiers for audio applications.

Yoshinori Kusuda (Member, IEEE) received the M.S. degree in physical electronics from Tokyo Institute of Technology, Tokyo, Japan, in 2004, and the Ph.D. degree with a focus on the subject of reducing switching artifacts in chopper amplifiers from TU Delft, Delft, The Netherlands, in 2018.

In 2004, he joined Analog Devices Japan Design Center, Tokyo. From 2015 to 2018, he was a Guest with the Electronic Instrumentation Laboratory, TU Delft. Since then, he has been with Analog Devices and is currently in San Jose, CA, USA, working with the Linear and Precision Technology Group. He has been working on precision CMOS analog designs, including stand-alone amplifiers and application specific mixed-signal products. This work has resulted in presentations and papers at IEEE conferences and journals, as well as 14 issued U.S. patents.

Johan H. Huijsing (Life Fellow, IEEE) received the M.Sc. degree in electrical engineering and the Ph.D. degree from Delft University of Technology, Delft, The Netherlands, in 1969 and 1981, respectively.

He has been an Assistant Professor and an Associate Professor of electronic instrumentation with the Faculty of Electrical Engineering, Delft University of Technology, since 1969. In 1990, he joined the Chair of Electronic Instrumentation, as a Full Professor. He has been a Professor Emeritus since 2003. From 1982 to 1983, he was a Senior Scientist with Philips Research Laboratories, Sunnyvale, CA, USA. From 1983 to 2005, he was a Consultant with Philips Semiconductors, Sunnyvale. Since 1998, he has been a Consultant with Maxim, Sunnyvale. His research work is focused on operational amplifiers, analog-to-digital converters, and integrated smart sensors. He has supervised 30 Ph.D. students. He has authored or coauthored over 300 scientific articles, 40 U.S. patents, and 15 books. In 1992, he initiated the International Workshop on Advances in Analog Circuit Design. He co-organized it yearly until 2003.

Dr. Huijsing was a Program Committee Member of the European Solid-State Circuits Conference from 1992 to 2002. He was awarded the title of Simon Stevin Meester by the Dutch Technology Foundation. He was the Chairman of the Dutch STW Platform on Sensor Technology and the Biannual National Workshop on Sensor Technology from 1991 to 2002.

Kofi A. A. Makinwa (Fellow, IEEE) received the B.Sc. and M.Sc. degrees from Obafemi Awolowo University, Ife, Nigeria, in 1985 and 1988, respectively, the M.E.E. degree from Philips International Institute, Eindhoven, The Netherlands, in 1989, and the Ph.D. degree from Delft University of Technology, Delft, The Netherlands, in 2004.

From 1989 to 1999, he was a Research Scientist with Philips Research Laboratories, Eindhoven, where he worked on interactive displays and digital recording systems. In 1999, he joined Delft University of Technology, where he is currently an Antoni van Leeuwenhoek Professor and the Head of the Microelectronics Department. His research interests include the design of mixed-signal circuits, sensor interfaces, and smart sensors. This has led to 16 books, over 300 technical articles, and over 30 patents.

Dr. Makinwa has been on the program committees of several IEEE conferences, and was the Analog Subcom Chair of ISSCC. He has also served the Solid-State Circuits Society as a Distinguished Lecturer and as an Elected Member of its Adcom. He is currently one of the organizers of the Advances in Analog Circuit Design Workshop and the Sensor Interfaces Meeting. He is an ISSCC top-10 contributor, and a co-recipient of 16 best paper awards, from the JSSC, ISSCC, VLSI, ESSCIRC, and Transducers, among others. He is a member of the Royal Netherlands Academy of Arts and Sciences.