Experimental Controller Design for Modular Interleaved High-Precision Current Amplifiers

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by

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Abstract

A modular approach to high-precision current amplifiers benefits lithography machines by reducing size and increasing efficiency. This research proposes two promising controller structures for a modular topology: a parallel controller structure and a cascaded controller structure. The study evaluates and compares their performance, introduces Delta-Sigma (DS) Analog-to-Digital Converters (ADCs) as a cost-effective alternative, and investigates their limitations in the proposed controller structures. A Feed Forward (FF) strategy is introduced to enhance the frequency response performance of both controllers.

Two methods to increase efficiency, particularly in amplifiers that are using interleaved Pulse-Width Modulation (PWM), are introduced: Phase-Shedding (PS) and Zero-Voltage Switching (ZVS). By estimating power losses it is shown that PS increases power efficiency for lower current setpoints, while ZVS increases efficiency for higher current setpoints. The study investigates how these methods impact controller stability and output current performance.

A hardware implementation validates the operation of the two controller structures. Stability issues with the cascaded controller structure become apparent and are resolved by a method that sacrifices bandwidth. Various measurements are conducted, and their results are compared to analytical expectations. The best frequency response is obtained using the parallel controller structure with a complex FF strategy, which gives a magnitude response of -0.3 dB and a phase shift of -3.6° at a 400 Hz setpoint.

When comparing the two controller structures, each has its own advantages and disadvantages. Choosing between the structures should be based on specific application requirements. If the application requires large bandwidth with high stability, the parallel controller should be selected. If the application requires good modularity, low quantization noise, and disturbance rejection performance, the cascaded controller should be selected.

Preface

This thesis marks the end of my educational journey at the TU Delft. The past eight months have been challenging yet rewarding. It gave me the opportunity to expand my knowledge in power electronics, control systems, and firmware design, as well as developing my personal skills. Conducting research at a high-tech company provided insights into the practical application of theoretical knowledge, and being surrounded by experts helped me grow professionally and personally.

First and foremost, I want to express my gratitude to my company supervisor, Mert Turhan, for all the opportunities and the support over the last months. Our many discussions and often extended meetings provided me with new insights and ideas. He always steered me in the right direction and I would not have come this far without his guidance. Thanks to Mert, I improved my writing and presentation making skills, especially in creating efficient figures, where I improved a lot because of Mert's sharp comments. Secondly, I want to thank my university supervisor, Hani Vahedi, for his academic support. Hani always provided valuable insights during our meetings and motivated me to dive deeper into ideas that were maybe not obvious at first. Whenever I had questions, he was always very quick to respond and helped me through the sometimes difficult process of obtaining my master's degree. Finally, I want to thank my family, friends, and especially my girlfriend for their support during this final part of my studies.

Although this marks the end of my formal education, I am eager to continue learning and look forward to future opportunities as an electrical engineer.

Luuk Pijnenburg
Delft, April 2025

Contents

List of Abbreviations

Abbreviation	Definition
AA	Anti-Aliasing
ADCs	Analog-to-Digital Converters
BRAM	Block Random-Access Memory
DS	Delta-Sigma
EMC	Electromagnetic Compatibility
EMF	Electromotive Force
ENOB	Effective Number of Bits
FF	Feed Forward
FIR	Finite Impulse Response
FPGA	Field-Programmable Gate Array
GM	Gain Margin
HB	Half-Bridge
MMCM	Mixed-Mode Clock Manager
PM	Phase Margin
PS	Phase-Shedding
PWM	Pulse-Width Modulation
RMS	Root Mean Square
SAR	Successive Approximation Register
SiC	Silicon Carbide
ZVS	Zero-Voltage Switching

1

Introduction

Gordon Moore predicted in 1965 that the number of transistors on a given chip doubles every 2 years [28]. This prediction relies on continuous innovations in lithography machines, which provide the patterning required in semiconductor manufacturing. In these machines a pattern from a reticle is projected onto a wafer, that contains the silicon material for the chips. After multiple different processing steps the next layer is printed and this process is repeated for each layer. Modern chips can consist of up to 100 layers, making it a lengthy process.

Stages that hold the wafer and the reticle, containing the pattern, are required to move with nanometer precision to achieve accurate projection. These stages are moved by actuators that are driven by high-precision power electronic current amplifiers. Patterning more and smaller transistors raises the desire for even higher precision. Combined with a need for high production throughput, fueled by a fast-rising demand for computer chips, this calls for continuous innovation in these amplifiers, both in bandwidth and output power, and to a lesser extent, in cost.

In modern lithography machines, two different actuator systems are used to move the stage that holds the wafer [9]. A short-stroke system provides only small movement but has position accuracy with error in the range of picometres. A long-stroke system provides larger movements in the range of meters and position accuracy with errors in the range of nanometers, along with a requirement for fast acceleration. An overview of the control of a long-stroke system is shown in Figure 1.1. The outer position loop obtains a setpoint from a given position profile and receives a position measurement, with which the controller determines a current setpoint that is provided to the current amplifier. This amplifier then generates this current, and the actuator exerts a proportional force on the wafer stage. The term "high-precision" arises from the requirement that current tracking needs to be as accurate as possible, meaning a maximally flat frequency response over the desired bandwidth, as well as minimum noise and distortion at frequencies that cause position error [32].

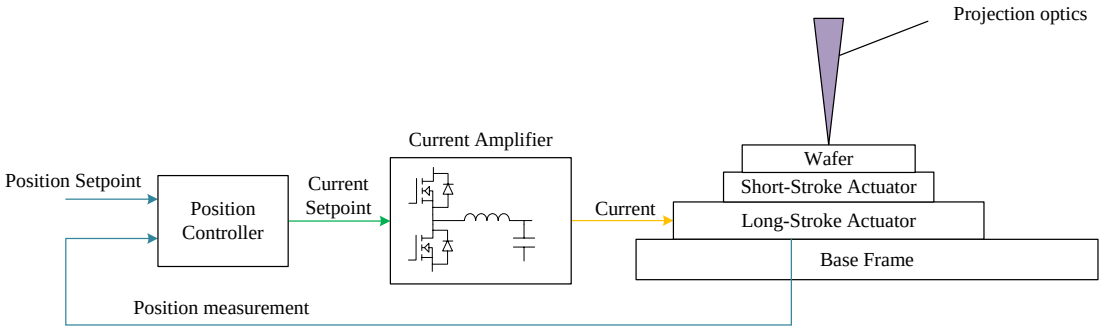


Figure 1.1: Schematic overview of the position loop and current loop of the long-stroke actuator in a lithography machine.

Lithography machines contain numerous of these current amplifier systems, providing current to amplifiers

with different specifications and requirements. With every new machine generation, the amount of amplifiers and their requirements only become more demanding, leading to an increase in physical space occupied by these amplifiers. Therefore, the requirement for higher power output comes together with a request for a more modular solution and higher power densities. A way to achieve this, discussed in this research, is by paralleling multiple amplifiers. In this modular solution the configuration can be changed based on the specific actuator requirements. Two distinct controller structures that have potential to be used in such a modular configuration will be explained and compared in detail. By interleaving the Pulse-Width Modulation (PWM) additional techniques can be implemented that increase power efficiency, and as result, power density even further.

1.1. Research Objectives

The research goals of this work can be summarized in three objectives:

- Compare two different controller structures for modular interleaved current amplifiers evaluating their performance in terms of bandwidth, stability and modularity.
- Investigate the use of Delta-Sigma (DS) Analog-to-Digital Converters (ADCs) as a cost-effective alternative in high-precision current amplifiers.
- Provide and evaluate promising techniques for improving power efficiency in interleaved current amplifiers leading to higher possible power density.

1.2. Thesis Outline

The thesis is structured into six chapters.

- **Chapter 2** introduces the amplifier topology and how it operates in a modular configuration. It explains the technique of interleaved PWM and discusses its advantages and disadvantages. Additionally, an explanation on the operation of DS ADCs, which will be used for this research, will be provided.
- **Chapter 3** presents two different controller structures for interleaved current amplifiers: a parallel controller structure and a cascaded controller structure. Each structure will be explained in detail, with a focus on the implementation and tuning for the particular topology and taking into account group delay limitations of the selected ADCs. Performance will be evaluated using the programs PLECS and MATLAB Simulink for simulations.
- **Chapter 4** describes two techniques that can be used to increase efficiency in interleaved current amplifiers: Phase-Shedding (PS) and Zero-Voltage Switching (ZVS). Their effectiveness in terms of efficiency increase will be evaluated analytically using a power loss model. Simulation results are shown with a particular focus on output current error and the effect on controller stability.
- **Chapter 5** validates the proposed controller structures through hardware implementation. A prototype that uses a low-cost Field-Programmable Gate Array (FPGA) is used to demonstrate the performance of the two proposed structures. The firmware structure is outlined, with particular interest in timing restrictions and clock requirements. Different measurements are shown, and used to verify the analytical and simulation results. The chapter concludes with a comparison of the two different controller structures based on various evaluation criteria.
- **Chapter 6** concludes this thesis by summarizing key findings, and providing a tradeoff table for comparison. Finally, this chapter will provide recommendations for future research.

2

Amplifier Overview

In this chapter, a general overview of the current amplifier will be provided. The circuit topology will be introduced, along with the proposed modular configuration. From this topology, a simplified circuit can be derived, from which state-space equations can be obtained that are used for modeling. Next, an explanation will be given regarding the operation and benefits of using interleaved PWM. Finally, DS ADCs will be introduced, discussing their advantages and disadvantages, providing a foundation for their limitations that need to be taken into account while designing the controllers.

2.1. Circuit Topology

The circuit topology of the amplifier is shown in Figure 2.1. It consists of a Half-Bridge (HB) followed by an LC-filter, consisting of an inductor and a capacitor. This gives it a similar topology to what is often used in class-D amplifiers for audio applications. The LC-filter is added for two main reasons. The first reason is that it filters out the switching frequency and its harmonics, in order to get a cleaner output with minimum switching ripple. The second reason is to improve Electromagnetic Compatibility (EMC). Fast switching creates high-frequency voltage ringing on the switches. This has the potential, in combination with long machine cables acting as antennas, to interfere with sensitive electronics. The LC-filter suppresses this interference. The actuator load connected to the amplifier is modelled as an inductor in series with a resistor.

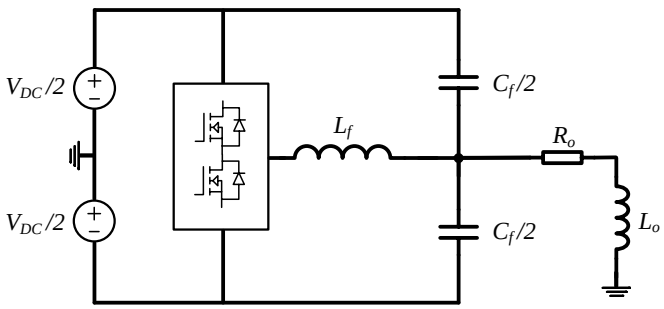
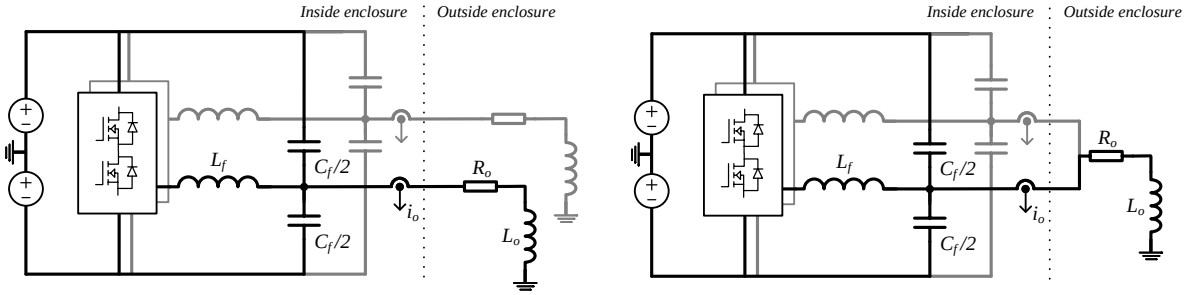


Figure 2.1: Circuit topology of the current amplifier.

The amplifier is connected to a symmetric power supply, in order to deliver both positive and negative currents to the load. This is also the reason that the filter capacitor is divided into parts that connect to the positive rail and the negative rail. The focus of this research will be on a 1-phase amplifier implementation. If the position loop requires 3-phase operation, using three of these topologies the system can be extended to a 3-phase system, provided that a control strategy for the midpoint voltage is added.

A modular topology can be created by allowing multiple amplifiers to work in parallel, from now on referred

to as parallel branches. In this way, the configuration can be changed depending on the required power specifications. When operating individually, each branch controls its own load, as shown in Figure 2.2a. The branches are located inside the same enclosure and share the same DC supply. Figure 2.2b shows the situation when two branches are paralleled, and together are controlling a single load. Since the configuration inside the enclosure cannot change, this parallel connection is created outside the enclosure. Due to this, no total output current can be measured directly, only the individual branch current output can be measured. This is an important constraint to take into consideration when designing the controller, with regards to current sampling. The branches are located in the same enclosure, but should be able to be controlled separately, each by their own FPGA. As a consequence, it is desirable that the information, such as measurements or setpoints, that have to be shared by the controllers of the branches, should be minimized. The reason for this is to have minimal communication channels and to have low communication delay within the controller. On top of this, it is also desirable to keep the necessity for controller parameter changes to a minimum when changing the number of branches to keep the system as modular as possible.



(a) Two branches connected to individual loads.

(b) Two branches connected to a common load.

Figure 2.2: The modular topology of the amplifier.

2.2. Simplified Circuit for Modelling

The characteristics of the LC-filter change when the number of branches is changed. Using Norton's and Thevenin's Theorems, a simplified circuit for designing the controllers can be drawn. This circuit is shown in Figure 2.3, where n defines the number of parallel branches. A resistor is added to represent the series resistance of the filter inductor. The setpoint voltage (v_{PWM}) from the HB is modelled without any switching harmonics. Adding more branches increases the effective capacitance while decreasing the effective induc-

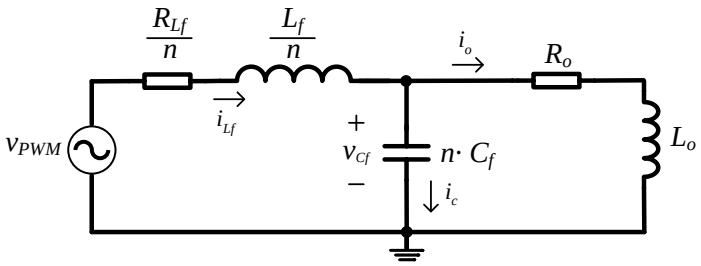


Figure 2.3: Simplified circuit for modelling of n parallel branches.

tance. The resonance frequency (f_r) of the LC-filter does not change with the number of branches and can be expressed as:

$$f_r = \frac{1}{2 \cdot \pi \cdot \sqrt{\frac{L_f}{n} \cdot C_f \cdot n}} = \frac{1}{2 \cdot \pi \cdot \sqrt{L_f \cdot C_f}} \tag{2.1}$$

The damping of the LC-filter is important for controller stability. The damping ratio (ζ) is proportional to the filter components, and changes with the number of branches:

$$\zeta \sim \sqrt{\frac{\frac{L_f}{n}}{C_f \cdot n}} = \frac{1}{n}\sqrt{\frac{L_f}{C_f}} \tag{2.2}$$

To keep the filter inductance small, a low filter damping ratio is unavoidable. To achieve a good transient response while avoiding any oscillations in the output, the aim is to obtain $\zeta = \frac{1}{\sqrt{2}}$. Control techniques that can be used to control the damping ratio will be provided in chapter 3. Using the simplified circuit in Figure 2.3, a state-space equation can be expressed as:

$$\frac{d}{dt}\begin{bmatrix} i_{L_f} \\ v_{C_f} \\ i_o \end{bmatrix} = \begin{bmatrix} -\frac{R_{L_f}}{L_f} & -\frac{n}{L_f} & 0 \\ \frac{1}{n \cdot C_f} & 0 & -\frac{1}{n \cdot C_f} \\ 0 & \frac{1}{L_o} & -\frac{R_o}{L_o} \end{bmatrix} \cdot \begin{bmatrix} i_{L_f} \\ v_{C_f} \\ i_o \end{bmatrix} + \begin{bmatrix} \frac{n}{L_f} \\ 0 \\ 0 \end{bmatrix} \cdot v_{PWM} \tag{2.3}$$

This equation will be used further for the controller design in the following chapters. Throughout this report, analytical, simulation, and experimental results will be shown using the parameter values in Table 2.1. Figure 2.4 shows the frequency response of the circuit. A large resonance is observed due to the LC-filter, which is undesirable for controller stability.

Table 2.1: This table shows the values of the parameters used in this research.

Parameter	Value
L_o	1.37 mH
R_o	220 mΩ
L_f	104 μH
R_{Lf}	28 mΩ
C_f	0.96 μF
f_r	15.8 kHz
f_{PWM}	78.125 kHz

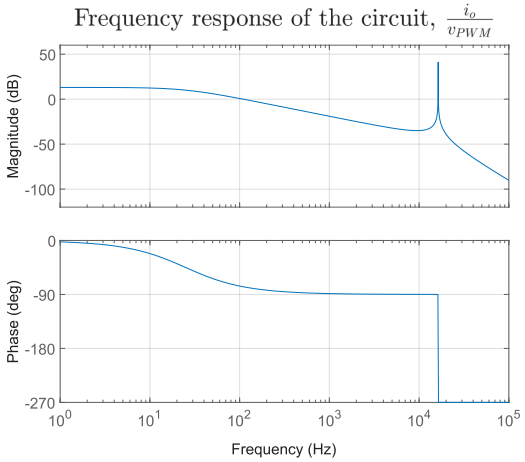


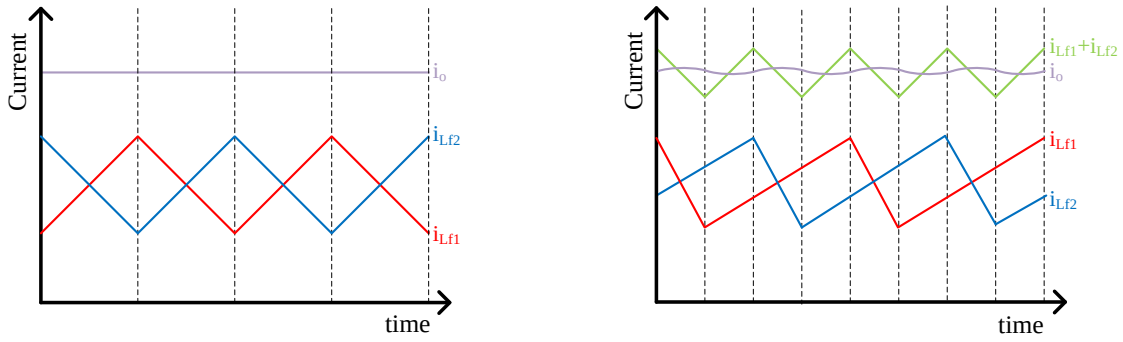
Figure 2.4: The frequency response of the circuit, for number of branches n = 2.

2.3. Interleaved Pulse-Width Modulation

When multiple branches are placed in parallel, interleaved PWM can be implemented. This technique was first extensively researched for its application in DC-DC converters [2, 19], and later also in inverters [1]. It uses phase-shifted carriers to generate the PWM, where the phase-shift between carriers is determined by the total number of parallel branches and can be expressed as:

$$\Delta\phi = \frac{360^\circ}{n} \tag{2.4}$$

As a result, there is also a phase-shift between the inductor current ripple of the different branches. The sum of these ripples determines the output current. For $n = 2$ and a 50% duty cycle, the ripples fully cancel, resulting in zero ripple in the output current. This effect is illustrated in Figure 2.5a. For the case $n = 2$, a maximum output current ripple is present at 75% duty cycle, which is illustrated in Figure 2.5b. For this case, the total added inductor current ripple is half that of an individual inductor current ripple. However, with this technique, the resulting ripple frequency also doubles, leading to higher suppression by the output LC-filter. When accounting for the second-order filtering effect of the LC-filter, the maximum current ripple amplitude



(a) 50% duty-cycle: shows complete ripple cancellation in the output current.

(b) 75% duty-cycle: shows maximum output current ripple.

Figure 2.5: The inductor ripple and output current for interleaved PWM, with number of branches $n = 2$.

when interleaving with $n = 2$ is reduced by a factor of 8, compared to using non-interleaved PWM.

Additional advantages of using interleaved PWM can be summarized:

- It reduces input current ripple, minimizing the required size of input filter capacitors.
- Errors in sampled inductor currents that exists due to timing offset can be canceled. This effect will later be shown in subsection 3.1.2.
- Interleaving reduces average PWM delays, improving control robustness. This effect will be elaborated upon later in section 4.3.
- EMC performance is improved since individual switching happens at a lower current and is spread over time.

A drawback of interleaved PWM is the potential for high circulating currents. In literature, a potential solution for this is the use of coupled filter inductors, which can suppress this high-frequency current flowing between the branches [10, 35]. However, because of the desire for a modular design, this solution is not feasible. The branches should be able to work individually, in which case a coupled inductor would result in interference from one branch to another. Moreover, because of the filter capacitor in the topology, there is already a circulating current present when using non-interleaved PWM. Interleaving will not give any additional circulating currents.

2.4. Delta-Sigma ADCs

Now that the circuit topology and PWM strategy are established, the next step is to determine how to measure the voltage and currents. When selecting the type of ADC that is going to be used, an obvious choice would be a Successive Approximation Register (SAR) ADC. They are widely used because of their good performance for delay and resolution and are the common choice for high-precision current amplifiers. However, for this research, the use of DS ADCs will be investigated. The main reason for this is their significant advantage in terms of cost. DS ADCs operate by converting an analog signal into a high-frequency bitstream, at a sampling frequency much higher than the desired data rate [3]. In this operation, the quantization noise is shifted to frequencies much higher than the desired signal frequency (Figure 2.7). This high-frequency quantization noise can be filtered out by a low-pass filter, leaving the original signal. This filter can be implemented digitally in the FPGA. How much of this quantization noise is removed in the digital filter determines the effective resolution of the sampled signal. A schematic overview of the data acquisition using the DS ADCs is summarized in Figure 2.6.

A common choice for digital filter type is the sinc filter, which is a type of Finite Impulse Response (FIR) filter [27]. This filter requires very few FPGA resources and provides relatively good group delay performance. The filter gives the output at a data rate (f_D) multiples lower than the sample rate (f_S) of the DS ADC, this ratio is

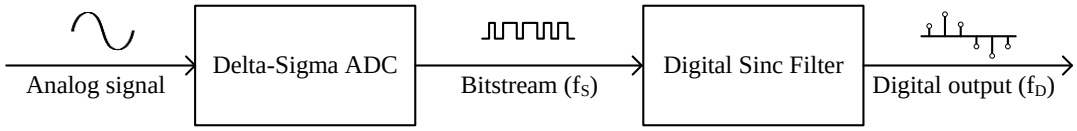


Figure 2.6: This figure shows the operation of the DS ADCs. The analog signal is converted into a bitstream which is digitized by a digital filter.

called the decimation factor (M), and can be expressed as:

$$M = \frac{f_S}{f_D} \tag{2.5}$$

This decimation factor determines stop-band attenuation, which results in lower quantization noise and better signal resolution. Next to the decimation factor, the filter order (K) also determines the stop-band attenuation of the sinc filter. The filter can be represented in the z-domain as:

$$H(z) = \frac{1}{M}\left(\frac{1-z^{-M}}{1-z^{-1}}\right)^K \tag{2.6}$$

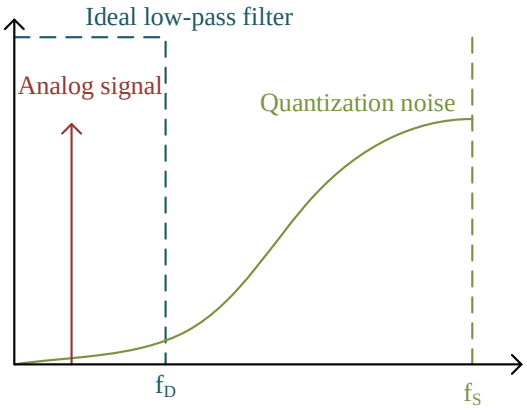


Figure 2.7: The DS ADC moves the quantization noise to close to the sampling frequency. A digital low-pass filter can be used to obtain the original signal.

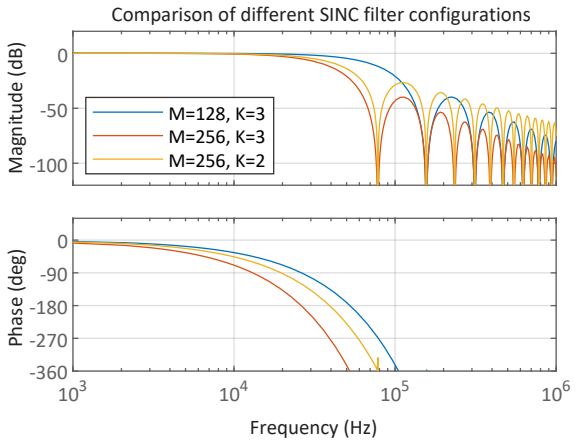


Figure 2.8: A comparison of different sinc filter configurations for different filter orders and decimation ratios ($f_S = 20MHz$).

Figure 2.8 compares the filter frequency response for different values of decimation rate and filter order. What is shown is that there is a trade-off between stopband attenuation and group delay. The higher the stop-band attenuation roll-off, the larger the group delay of the filter. This can be translated to a trade-off in faster ADC readout speeds at the cost of lower effective resolution. This effective resolution can be calculated by integrating the noise and can be expressed as the Effective Number Of Bits (ENOB). These calculations are out-of-scope for this report, but data from [16] will be used to determine this effective resolution. This will be used to compare quantization noise performance for the different controller structures.

Figure 2.8 also shows that the sinc response is equal to zero at integer multiples of the data rate, which appear as notches in the response of the filter. These notches can be used in the design of the controller for the current amplifier, where it is sometimes desirable to remove the PWM frequency component and its harmonics. In that case the exact sampling instance is independent of the PWM carrier, which would be the case for other types of ADCs. However, this comes at a cost of a relatively high decimation ratio and as a result, a higher group delay.

In conclusion the advantages of the use of DS ADCs can be summarized as follows:

- The cost of DS ADCs are much lower compared to other types of ADCs for the same performance.
- DS ADCs don't require additional expensive 2^{nd} order Anti-Aliasing (AA) filters. The very high sampling frequency enables the use of simple first-order passive filters for AA.
- They provide easy galvanic isolation, due to the single bitstream, which is often already integrated into the ADC.
- Digital sinc filters require few FPGA resources for implementation.
- DS ADCs provide flexibility in trade-off between accuracy and group delay. A possibility exist for multiple sinc filters to be run in parallel, each with its own decimation factor.
- Notches in sinc filter response can be used to filter out PWM harmonics.

The main downside of the DS ADCs is the high group delay of the required digital filter compared to the sampling delay in most other types of ADCs. The effect of this delay will be taken into account when designing the controllers. For each measured quantity a trade-off will be provided to determine the preferred decimation rate for the sinc filter.

3

Controller Design

This chapter explores two different controller structures, assessing their implementation in modular interleaved high-precision current amplifiers. The challenges posed by using DS ADCs in terms of group delay and resolution are highlighted. Additionally, a Feed Forward (FF) strategy will be provided to improve frequency response. The chapter will be concluded by showing simulation results and comparing these with the analytical expectations.

3.1. Parallel Controller

The first controller structure will be referred to as the parallel controller structure. An overview of this structure is shown in Figure 3.1. This structure is well-defined in literature for different converter and inverter applications [22, 21, 8], but a definition of a modular configuration using DS ADCs is missing. It consists of a damping loop, a balancing loop, and a tracking loop, all connected in parallel. The output provided to the PWM generator is determined by a subtraction of the individual loops.

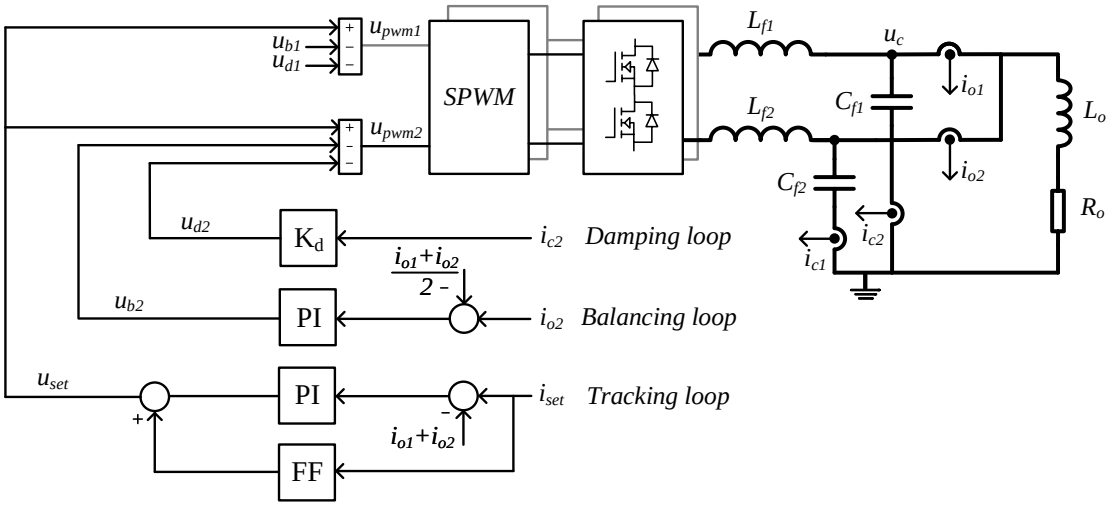


Figure 3.1: Schematic overview of the parallel controller structure. It consists of a damping loop, a balancing loop and a tracking loop. u_{d1} and u_{b1} are calculated similarly to u_{d2} and u_{b2} with their own corresponding branch currents. The tracking loop is common for all branches.

3.1.1. Damping Loop

The objective of the damping loop is to change the damping ratio of the LC-filter, also called active damping. As explained in section 2.2, a consequence of keeping component values small is a small damping ratio. On a pole-zero plot, a small damping ratio means that the complex pole pairs of the LC-filter are closer to the right-half plane, which will result less controller stability. Having the damping ratio too high will cause a slow filter response. This is the reason why a damping ratio of $\zeta = \frac{1}{\sqrt{2}}$ is selected. The damping loop takes the measurement of the filter capacitor value and multiplies this with a damping constant (K_d). This is subtracted from the open-loop voltage setpoint going to the PWM generator. This process can be compared to placing a virtual damping resistor in series with the LC-filter, which is illustrated in Figure 3.2a. Using the total filter capacitor current (i_c), as indicated in Figure 2.3, the value of this damping resistor, which is equal to the value of K_d is calculated as:

$$K_{d,tot} = 2 \cdot \zeta \cdot \sqrt{\frac{\frac{L_f}{n}}{C_f \cdot n}} = \frac{2}{n} \cdot \zeta \cdot \sqrt{\frac{L_f}{C_f}} \tag{3.1}$$

However, provided that the filter capacitances are equal, the individual capacitor current is a function of the total capacitor current (i_c) and the number of branches:

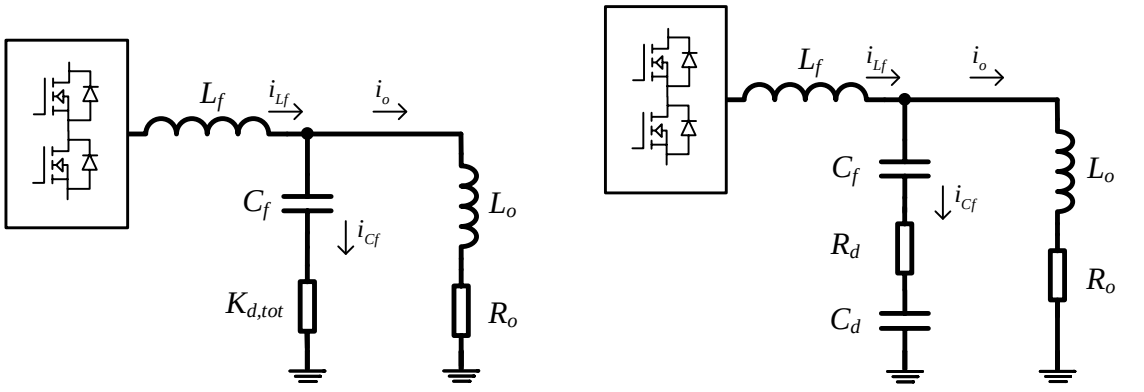
$$i_{c,n} = \frac{i_c}{n} \tag{3.2}$$

The result of this is that if individual branch capacitor current is used the individual branch damping constant ($K_{d,n}$)can be written independent of number of branches:

$$K_d = 2 \cdot \zeta \cdot \sqrt{\frac{L_f}{C_f}} \tag{3.3}$$

For modularity, this is beneficial for two reasons:

- When the number of branches changes, the damping constant remains the same.
- Each controller can run its damping loop locally. This eliminates the need for controllers to share capacitor current information. As will be explained in the next paragraph, for the damping loop, the delay should be minimized, which means there is no margin to communicate capacitor current information between controllers.



(a) Ideal active damping adds a virtual damping resistor in series with the LC-filter.

(b) Due to delays in the digital control, in reality, also a damping capacitor should be included. This capacitor influences the resonance frequency of the filter.

Figure 3.2: Active damping of the LC-filter.

Due to delays introduced when in digital controllers, the virtual damping resistance is not a perfect resistance but a complex impedance, which is illustrated in Figure 3.2b. This effect can be modelled by including a delay in the s-domain to the damping constant:

$$X_d = K_{d,tot} \cdot e^{-T_d \cdot s} \tag{3.4}$$

$$X_d = K_{d,tot} \cdot (\cos(2 \cdot \pi \cdot f \cdot T_d) - j \cdot \sin(2 \cdot \pi \cdot f \cdot T_d)) \tag{3.5}$$

$$R_d = K_{d,tot} \cdot \cos(2 \cdot \pi \cdot f \cdot T_d) \tag{3.6}$$

$$C_d = \frac{1}{K_{d,tot} \cdot 2 \cdot \pi \cdot f \cdot \sin(2 \cdot \pi \cdot f \cdot T_d)} \tag{3.7}$$

The parasitic damping capacitance depends on the frequency. To give a graphic illustration using a MATLAB, an approximation of the delay can be given using a Padé approximation [38]. The dependency of the complex pole pair position of the LC-filter on delay can be shown using a root locus (see Figure 3.3). In the figure, it can be seen that increasing the delay affects both the damping ratio and the resonance frequency. The poles follow a trajectory and eventually end up in the right-half plane, indicating instability.

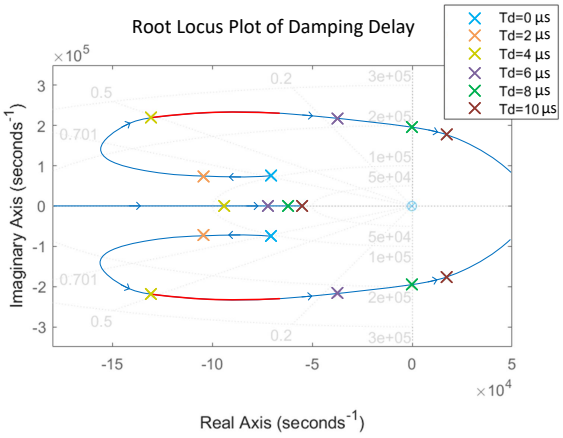


Figure 3.3: The root locus of the poles of the circuit seen in Figure 3.2b with changing damping loop delay. Increasing the delay eventually leads to the poles moving into the unstable right-half plane. Using Equation 3.9 the maximum delay of the damping loop before instability is $T_{d,max} = 8\mu s$. The segment in red indicates the range of delay when using low sinc decimation factor (M=32) for capacitor current measurement and PWM oversampling (N=8).

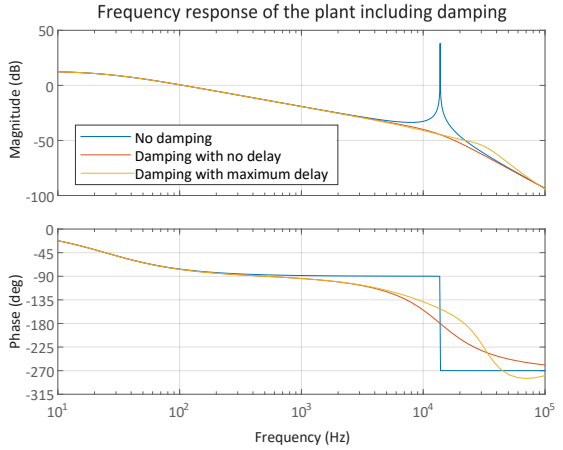


Figure 3.4: The frequency response of the circuit. The case with no damping is compared to the case with ideal active damping where no delay is taken into consideration. Finally, also the case where the damping delay is taken into account is plotted (T_d = 5.4 μs). The delay is minimized by using a low decimation factor (M=32) and PWM oversampling (N=8).

The resonance frequency at the edge of instability will be denoted as f_d. To maintain stability, the effective damping resistance at this frequency should be positive:

$$R_d = K_{d,tot} \cdot \cos(2 \cdot \pi \cdot f_d \cdot T_d) > 0 \tag{3.8}$$

From this, the the maximum damping delay can be expressed as:

$$T_{d,max} = \frac{1}{4 \cdot f_d} \tag{3.9}$$

The damping capacitance, under the condition stated in Equation 3.8, can be expressed as:

$$C_d = \frac{1}{2 \cdot \pi \cdot K_d \cdot f_d} \tag{3.10}$$

To find f_d, Equation 2.1 needs to be adjusted to contain the series damping capacitance:

$$f_d = \frac{1}{2 \cdot \pi \cdot \sqrt{L_f \cdot (C_f || C_d)}} = \frac{1}{2 \cdot \pi \cdot \sqrt{\frac{L_f \cdot C_f}{2 \cdot \pi \cdot K_{d,tot} \cdot C_f \cdot f_d + 1}}} \tag{3.11}$$

This can be solved using a numerical solver. From this analysis and Figure 3.3 it can be concluded that a low controller delay is desired for the damping loop. The control delay is composed of four delay sources:

- The sampling delay of the DS ADC. However, because of the high oversampling of the ADC, this delay is negligibly small compared to other delays and will not be considered.

- The group delay of the sinc filter (T_{sinc}) , as explained in section 2.4.
- The calculation delay (T_{calc}) needed by the FPGA to calculate the PWM generator setpoint.
- The PWM generator delay ($T_{d,PWM}$). It takes a delay for the moving average effect of the PWM filter to significantly change the output voltage. Depending on the position of the carrier relative to the setpoint, the PWM delay ranges from 0 to a certain maximum value [31].

In summary, an equation for the total damping loop delay (T_d) can be written as:

$$T_d = T_{sinc} + T_{calc} + T_{d,PWM} \tag{3.12}$$

Combining Equation 2.3, Equation 3.3, and Equation 3.12, the transfer function of the plant can be written to include damping constant and damping delay:

$$P(s) = \frac{1}{L_f C_f L_o s^3 + \left(\left(K_d e^{-T_d s} + R_{L_f}\right) C_f L_o + L_f C_f R_o\right) s^2 + \left(\left(K_d e^{-T_d s} + R_{L_f}\right) C_f R_o + L_o + \frac{L_f}{n}\right) s + R_o} \tag{3.13}$$

A lower delay can be achieved through two methods. First, the decimation factor of the sinc filter can be decreased. This significantly lowers the group delay of the ADC data-acquisition. However, this comes at the cost of a decreased effective resolution. The quantization current noise of the DS ADC will be amplified by the damping loop and will directly influence the output current. Another consequence of decreasing the decimation ratio is that sinc filter notches will not be positioned at the PWM frequency. However, the Gain Margin (GM) requirements for the damping loop are not as strict as the Phase Margin (PM) requirements, and this ripple is acceptable for stability.

A second method to decrease overall controller delay is to use oversampling in the PWM generator [42, 37]. Most commonly, the setpoint is updated twice per PWM period (N=2), on the peaks and valleys of the carrier, which is called double-update PWM. When oversampling, the PWM setpoint gets updated more often during a PWM period. This decreases the PWM generator delay with factor N:

$$T_{d,PWM,N} = \frac{T_{d,PWM,N=1}}{N} \tag{3.14}$$

It is common practice to have the calculation delay equal to the PWM generator delay, in order to have sampling and updating of the setpoint happen simultaneously. This leads to the calculation delay also decreasing when oversampling:

$$T_{calc,N} = \frac{T_{calc,N=1}}{N} \tag{3.15}$$

An important constraint is that the FPGA should still be able to calculate the setpoint before updating the PWM generator, when this calculation time is decreased. Figure 3.3 also indicates the operating range of the poles for the delay range if these two methods are implemented. Figure 3.4 compares the frequency response of the circuit when using active damping with and without taking the delay into account. Similar to the root locus, this figure illustrates that the delay increases the resonance frequency and decreases the damping ratio.

3.1.2. Tracking Loop

Next, the tracking loop will be discussed. The goal of this loop is to take the setpoint current and provide it as accurately as possible as an output current. This is achieved by measuring the output error current and then compensating for this this using a controller. A simple PI controller is chosen for this research, as the main goal is the comparison of the controller structures, and not the controller itself. To obtain better steady-state tracking a Type-3 compensator could be considered [39]. A PI controller consists of a single pole at the origin and a zero, and can be written as:

$$C(s) = K_p + \frac{K_i}{s} \tag{3.16}$$

For tuning, the numerical bode plot method, proposed by Manke [25], will be used. In this method, magnitude (Mag_{bw}) and phase (θ_{bw}) at the desired bandwidth (f_{bw}) are extracted from the plant transfer function numerically using MATLAB. By selecting a desired PM, the PI parameters are calculated as:

$$K_p = \frac{\cos\left(\frac{PM - 180° - \theta_{bw}}{360°} \cdot 2\pi\right)}{Mag_{bw}} \tag{3.17}$$

$$K_i = -\sin\left(\frac{PM - 180° - \theta_{bw}}{360°} \cdot 2\pi\right) \cdot f_{bw} \cdot 2\pi \tag{3.18}$$

For selecting the PM value, Bergmans [5] suggest a PM of 45° as a good compromise between guaranteed stability and good dynamic response. However, the DS ADC imposes a significant group delay in the control loop. To maintain stability the group delay should be taken into account when defining the PM. As illustrated in Figure 3.1, the tracking loop takes the total output current by adding the individual branch currents (for $n = 2, i_o = i_{o1} + i_{o2}$). If the controllers are implemented on separate FPGA's, also a communication delay should be taken into account for the PM. To achieve sufficient GM, the controller bandwidth of the tracking loop should be a factor lower than the resonance frequency of the LC-filter. Thavaratnam [36] defines this minimum ratio as:

$$f_{bw} \leq \frac{1}{5} f_{res} \tag{3.19}$$

Now that the controller parameters have been established, the open-loop frequency response can be expressed as:

$$G_{OL}(s) = C(s) \cdot P(s) \tag{3.20}$$

The open-loop frequency response is drawn in Figure 3.5, with GM and PM indicated. The closed-loop frequency response is given as:

$$G_{CL}(s) = \frac{C(s) \cdot P(s)}{1 + e^{-s \cdot T_t} \cdot C(s) \cdot P(s)} \tag{3.21}$$

The communication delay and sinc filter delay are also included and are denoted by T_t. Figure 3.6 illustrates the closed-loop frequency response of the tracking loop.

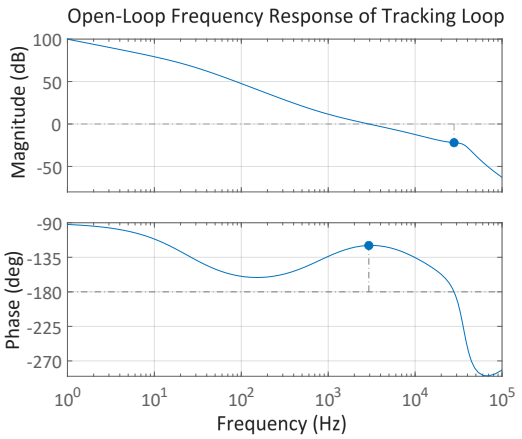


Figure 3.5: The open-loop frequency response. Indicated are the GM = 22 dB and PM = 60.4°, for $T_t = 10\mu s$

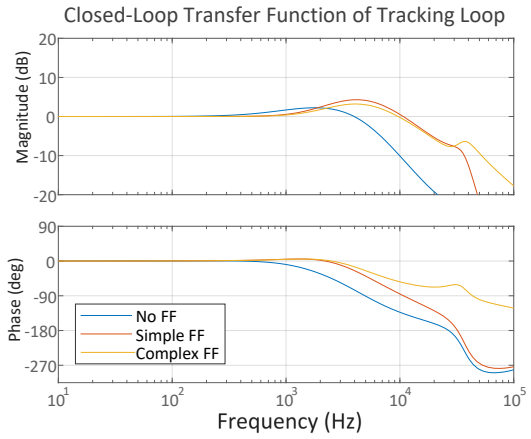


Figure 3.6: The closed-loop response of the tracking controller. A comparison can be made between no FF, simple FF and complex FF ($T_t = 10\mu s$).

Output current sampling

In section 2.1 it was indicated that no total output current measurement is available in the modular configuration, only individual branch current output measurements. Each branch has a separate filter capacitor. This means the PWM ripple will still be present in this measurement, which can be see in Figure 3.7. A notch in the sinc filter can be used to eliminate this ripple. However, this comes with increased group delay of the sinc filter, which is undesirable. A potential solution is to make use of the interleaving in the PWM. Because of the phase-shift, when adding the individual branch currents, the out-of-phase PWM ripples will cancel, and the total output current remains. The group delay of the sinc filters will be equal. This means that the delay of the sampled ripples will also be equal. If the sampling happens simultaneously, these ripples will fully cancel. Figure 3.7 demonstrates this effect, the current that is sampled by the controller will always be the current data from one group delay prior. This method can be easily extended to a topology with n branches, since the sum of the current will always be equal to the total output current, and all phase-shifted ripples will cancel.

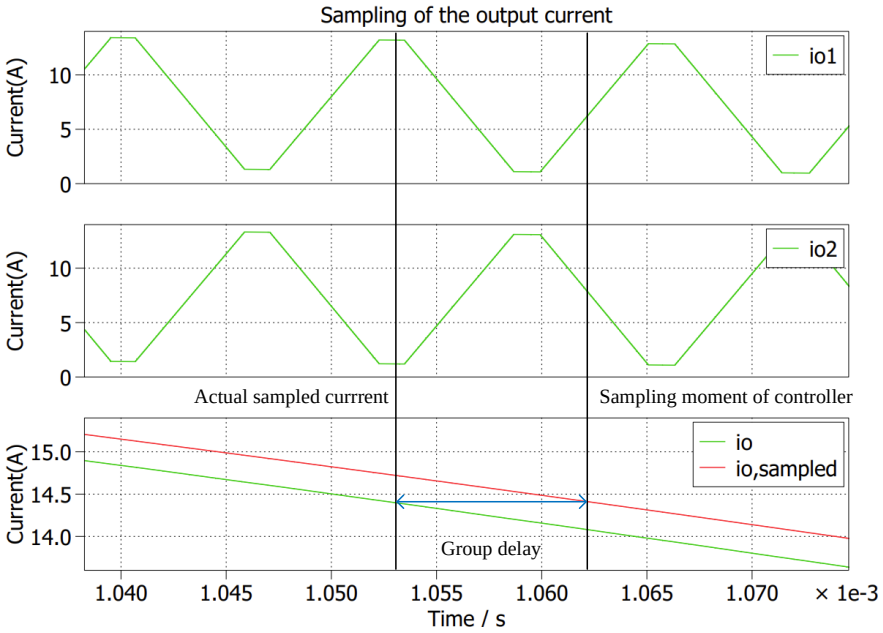


Figure 3.7: This figure demonstrates the ripple cancellation effect if sampling happens simultaneously. When the controller retrieves the current data from the sinc filter, it obtains the data from a group delay prior. This group delay is equal for all frequencies, which means the PWM ripple cancels. This figure was created using PLECS simulation, using sinc filter with $K = 3$ and $M = 128$.

Feed Forward

To improve tracking performance, a FF strategy can be added to the tracking loop. Figure 3.1 shows how this is implemented in the parallel controller structure, where the FF setpoint is added to the output of the controller. Dorf [14] explains this concept in detail. The closed-loop response is modified to:

$$G_{CL,FF}(s) = \frac{FF(s) \cdot P(s) + C(s) \cdot P(s)}{1 + e^{-s \cdot T_t} \cdot C(s) \cdot P(s)} \tag{3.22}$$

The objective is to have the term $FF(s) \cdot P(s)$ as close to 1 as possible. This makes the transfer function in Equation 3.22 approach 1, even for frequencies higher than the bandwidth:

$$FF(s) \approx \frac{1}{P(s)} \tag{3.23}$$

To correctly apply FF, there should be some prior knowledge of system parameters. To keep the FF equation simple, it is undesirable to directly use the full plant definition as stated in Equation 3.13. As a first idea, only the transfer function of the LR-load could be considered. This keeps the function simple with only one zero. To keep the transfer function causal, a high-frequency roll-off pole is also added:

$$FF_{simple}(s) = (L_o \cdot s + R_o) \cdot \frac{1}{\frac{s}{10^5} + 1} \tag{3.24}$$

Boerlage [7] proposes adding a notch filter to the FF to include the behavior of the LC-filter. This will be indicated as complex FF and is expressed as:

$$FF_{complex}(s) = (L_o \cdot s + R_o) \cdot \frac{s^2 + 2 \cdot \zeta \cdot \omega_{res} \cdot s + \omega_{res}^2}{\omega_{res}^2} \cdot \frac{1}{\left(\frac{s}{10^6} + 1\right)^3} \tag{3.25}$$

Again, to keep the equation causal, three high-frequency roll-off poles are added at higher frequencies. The notch parameters ω_{res} and ζ resemble the LC-filter parameters. Two FF approaches are included in the closed-loop transfer function for the tracking controller, their comparison is shown in Figure 3.6. It shows

that FF significantly improves frequency response, with complex FF giving better improvement compared to simple FF.
It is important to note that FF relies on accurate prior knowledge of system parameters. In high-precision systems, such as lithography systems, this is usually the case. For even better frequency response, in an actual system, the back Electromotive Force (EMF) of the actuator should be incorporated into the FF strategy.

3.1.3. Balancing Loop

Ideally, the current provided to the load should be equally divided over all branches. However, due to component variations such as filter inductance, switch parameters and driver delays, a branch current difference can exist [11]. This causes additional circulating current, resulting in extra power losses. In order to solve this, the goal of the balancing loop is to equalize the branch currents. In literature, the difference between two branch currents ($i_{o1} - i_{o2}$) is often taken as the error for the controller [22]. However, for more than n=2 branches, and for modularity purposes this is not desirable. A better approach is to take the difference between the average output current and the individual branch current, this can be expressed as:

$$i_{b,error} = i_{o,b} - i_{o,avg} = i_{o,b} - \frac{i_{o1} + i_{o2} + ...}{n} \tag{3.26}$$

For modularity, this is preferred, since if every controller runs on its own FPGA, it only needs its own individual branch current and the total output current information.The total current is already available since this information was also needed for the tracking loop. This strategy does require information about the total number of connected branches, which should be updated when the number of branches changes. An important note is that for the individual branch current, the ripple cancellation strategy explained in subsection 3.1.2 cannot be used. To obtain the branch current without ripple, the decimation factor of the DS ADC should be increased to move the notch to the switching frequency. To cancel the branch current ripple, the decimation factor of the DS ADC should be increased to move the notch to the switching frequency. The result of this is a higher sampling group delay, which should be taken into account when designing the balancing controller. The balancing setpoint that comes from the balancing controller will be equal in magnitude but different in sign for number of branches n=2. This setpoint voltage will be indicated as $u_{PWM,b}$. A circuit for modeling can be created and is shown in Figure 3.8 for number of branches n=2. Balancing will ideally not influence output voltage, this leads to the filter capacitors being left out of the model. This means that constant output voltage will be assumed for the control of the balancing. Using this circuit diagram, a

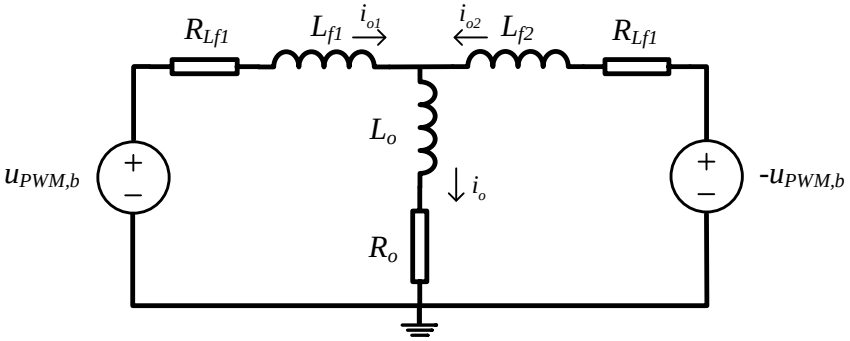


Figure 3.8: Simplified circuit for modelling of the balancing.

state-space representation for the balancing loop can be expressed:

$$\frac{d}{dt}\begin{bmatrix} i_{o1} \\ i_{o2} \\ i_o \end{bmatrix} = \begin{bmatrix} -\frac{R_{Lf1}}{L_{f1}} & 0 & 0 \\ 0 & -\frac{R_{Lf2}}{L_{f2}} & 0 \\ 0 & 0 & -\frac{R_o}{L_o} \end{bmatrix} \cdot \begin{bmatrix} i_{o1} \\ i_{o2} \\ i_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{f1}} \\ -\frac{1}{L_{f2}} \\ 0 \end{bmatrix} \cdot u_{PWM} \tag{3.27}$$

From this equation, the frequency response of the balancing plant can be derived, this is shown in Figure 3.9. Using this plant, the balancing controller can be designed. For the balancing loop, similar to the tracking loop, a PI controller is chosen to improve steady-state balancing error. The procedure to determine controller

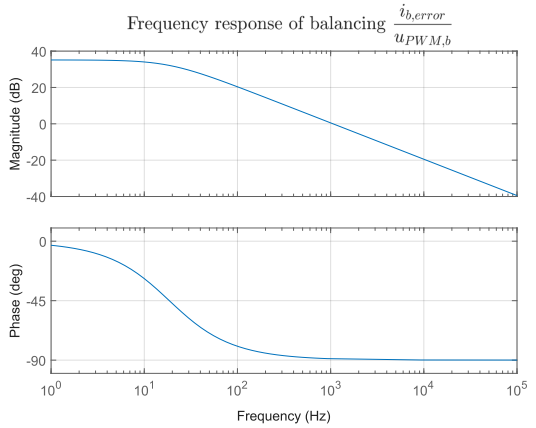


Figure 3.9: The frequency response of the balancing error current to an input of the balancing control.

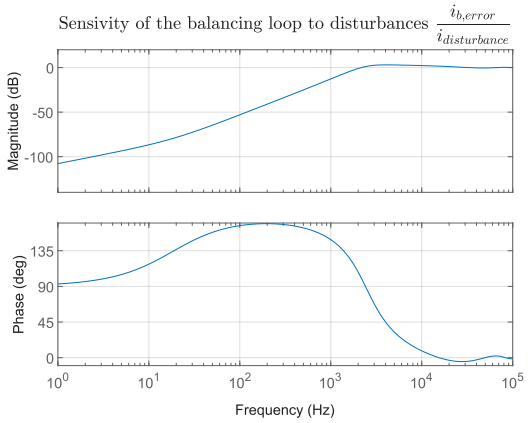


Figure 3.10: The sensitivity of the balancing loop to disturbances ($f_b = 3\,kHz$, $T_b = 25\,\mu s$). Up to the bandwidth, disturbances are rejected by the balancing controller.

parameters is the same as before, taking into account the higher PM requirement due to the higher sinc filter decimation factor for the individual branch output current sampling. The bandwidth is selected to be equal to the tracking loop bandwidth, to compensate for disturbance harmonics at setpoint frequency. Since the goal of the controller is to always keep the balancing error current close to zero, the closed-loop response is of less interest. More interesting is how the controller rejects disturbances. This can be represented by the sensitivity function as explained by Dorf [14]. Including the balancing loop delay (T_b), it can be expressed as:

$$S_b(s) = \frac{1}{1 + e^{-s \cdot T_b} \cdot P_b(s) \cdot C_b(s)} \tag{3.28}$$

The sensitivity function is shown Figure 3.10, in which it can be seen that the controller is good at rejecting balancing disturbances up to the balancing bandwidth.

3.2. Cascaded Controller

The second controller structure that will be discussed is a cascaded controller structure, which is shown in Figure 3.11. This structure is not as commonly found in literature as the parallel controller structure [23], but it is nevertheless defined for its application in high-precision current amplifiers [39, 26]. However, a modular approach lacks, and sampling is assumed to be instant and continuous, lacking a practical, cost-effective implementation, such as with DS ADCs. The structure consists of an outer current tracking loop, a middle capacitor voltage loop and an inner inductor current loop. The main concept is that each controller only controls a single component variable, by decoupling the controllers. For example, the inner current loop controls the current through the filter inductor by controlling the voltage across this component. By adding the capacitor voltage, the total output voltage setpoint to the PWM generator is calculated. Because the controllers are cascaded, bandwidth limitations should be taken into account to maintain stability.

3.2.1. Inductor Current Controller

The first controller is the inner inductor current controller. This controller receives a setpoint for the branch inductor current and then provides a setpoint for the branch inductor voltage. By adding the measured capacitor voltage the total PWM generator setpoint is obtained. This decoupling allows for control of the inductor current independently from the capacitor voltage. Since the PWM component in the capacitor voltage is already filtered by the LC-filter, a notch in the sinc filter is not needed for this measurement, resulting in lower possible group delay. Due to the decoupling the plant can simply be written as the admittance:

$$P_{inner}(s) = \frac{1}{s \cdot L_f} \tag{3.29}$$

By observing this plant (see Figure 3.12a) it would seem that very high controller bandwidth is possible, because phase delay is constant at -90°. However, the achievable bandwidth is determined by the delays in the

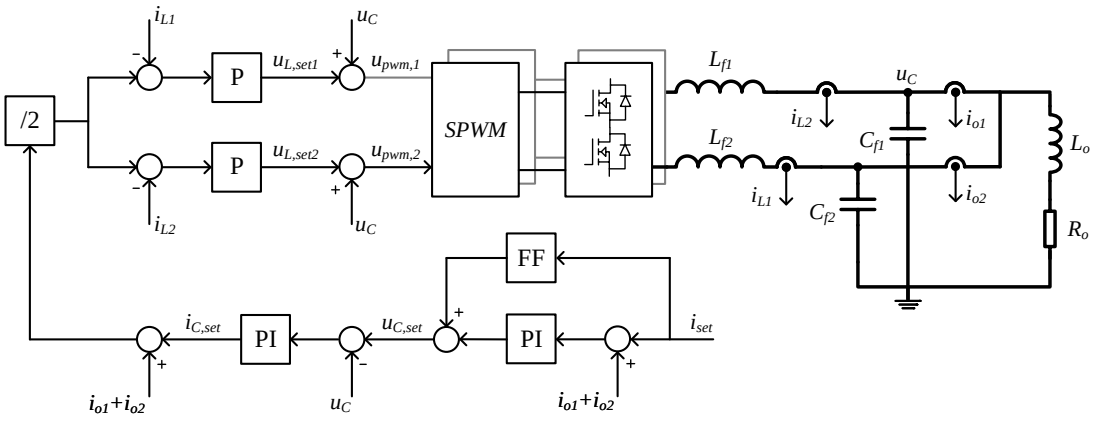


Figure 3.11: Schematic overview of the cascaded controller structure for number of branches n=2. It consists of an inner inductor current loop, a capacitor voltage loop and an outer current loop. Each controller is decoupled such that it only controls one component parameter.

loop of the controller (see Equation 3.12), which limits available PM and GM.

The controller uses a measurement of the filter inductor current to calculate the error for the controller. Since the individual branch current is required, the ripple cancellation strategy provided in subsection 3.1.2 cannot be used. Instead a sinc filter notch is required to filter out the PWM ripple. The consequence of this is a significant group delay in the current measurement. The bandwidth of the inner loop directly determines the achievable bandwidth of the output current tracking loop. Because of this, it is desired to keep the delays in the loop as small as possible, to achieve the highest possible bandwidth. Using four methods, the delay can be reduced, by:

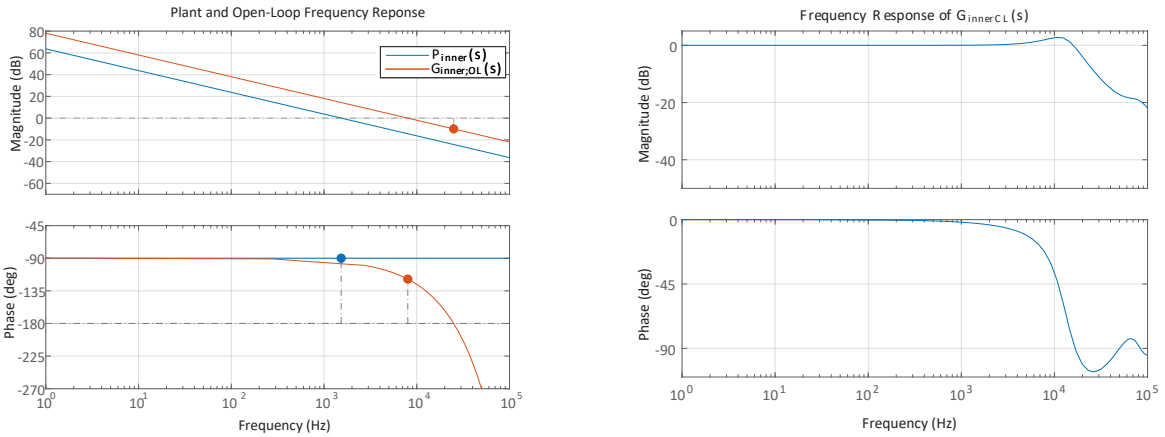
- Using a second-order sinc filter with K=2 (see section 2.4), the sinc filter group delay is reduced. This comes, however, at the price of reduced resolution and increased quantization noise in the filter inductor current measurement.
- Using oversampling in order to reduce the PWM delay. The problem is that because of the high decimation factor of the sinc filter the sampling rate is low. The sampling rate can be increased by using a method that parallels two sinc filters on the same input bitstream from the DS ADC. Giving one sinc filter a sampling time offset increases effective sampling rate and enables oversampling.
- Choosing a simple P-type controller, the calculation delays of the controller can be kept minimal.
- Reducing calculation delay by selecting a simple controller enables a technique where the calculation time in the loop delay can be eliminated [13]. This works by calculating the setpoint right after sampling and making it available to the PWM generator immediately when calculation is finished. This is possible only when it is ensured that PWM generator setpoint will never be very close to the maximum voltage setpoint by using saturation and if calculation delay is much smaller than PWM period. The maximum allowed setpoint voltage for this method is expressed as:

$$u_{PWM,max} = \left(\frac{T_{PWM} - 4 \cdot T_{calc}}{2 \cdot T_{PWM}} \right) \cdot U_{DC} \tag{3.30}$$

By including the delay and the controller gain, the open-loop transfer function can be expressed as:

$$G_{inner,OL} = P_{inner}(s) \cdot C_p \cdot e^{-s \cdot T_d} \tag{3.31}$$

The frequency response is shown in Figure 3.12a. Using Equation 3.21 the closed-loop frequency response $G_{inner,CL}$ is calculated, which is shown in Figure 3.15b.



(a) Plant response and open-loop response. Indicated for the open-loop response are PM=61° and GM= 10 dB

(b) Closed-loop response with bandwidth f_{bw} = 8 kHz

Figure 3.12: Frequency response of the inner inductor current loop (M=256, K=2, N=2).

Since each branch inductor controller controls its own inductor voltage, the cascaded controller structure provides an advantage in terms of modularity. The total filter inductor current setpoint comes from the voltage controller and gets divided by the number of branches. The inner inductor current parameters do not change with a changing number of branches, since they control individual branch filter inductors. Decoupling voltage measurement is the same for all branches. The result of this is that the fast inner loop can be run locally for each branch without needing any communication between branches, with the exception of receiving the setpoint.

3.2.2. Capacitor Voltage Controller

The capacitor voltage loop controls the output voltage by providing a setpoint for the capacitor current. By adding the total output current, a total inductor current reference is created as a setpoint for the inner loop. For the total output current measurement, the ripple cancellation strategy, as explained in subsection 3.1.2, can be used. This means sinc filters with a higher decimation factor and consequently lower group delays are possible for this decoupling current. When controlling the current through the capacitor, the plant can be expressed as the impedance of the total filter capacitor, limited by the frequency response of the inner loop:

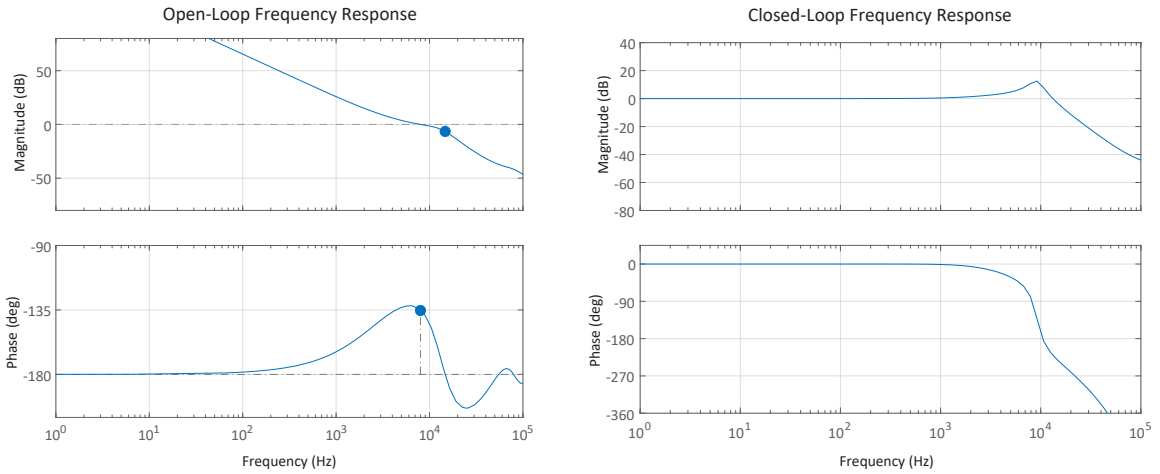
$$P_{voltage}(s) = \frac{1}{s \cdot C_f \cdot n} \cdot G_{inner,CL} \tag{3.32}$$

For the controller, a PI type is selected since the delay requirements are not as strict as for the inner controller. The integrator in the controller will improve steady-state tracking. The open-loop frequency response is shown in Figure 3.13a. The bandwidth is selected to be the same as that of the inner inductor controller. This is possible because of the integrator added by the capacitor to the plant provides an additional 90° phase delay. Subsection 5.3.2 will show that a high bandwidth for the voltage controller is required to reject disturbances, this comes at the cost of thinner stability margins. The closed-loop frequency response of the voltage controller is shown in Figure 3.13b.
The controller controls the capacitor voltage by providing a setpoint for the total capacitor current. However, for modularity, parallel capacitor controllers can be run in parallel each providing a setpoint for a single branch capacitor current.

3.2.3. Outer Current Tracking Controller

The outer current tracking controller regulates the current going to the load. For this controller, no additional decoupling is needed. The controller provides a capacitor voltage setpoint to the voltage controller based on a received setpoint current and the measurement of the output current. The plant can be written as the load admittance, corrected by the frequency response of the capacitor voltage controller:

$$P_{current}(s) = \frac{1}{s \cdot L_o + R_o} \cdot G_{voltage,CL} \tag{3.33}$$

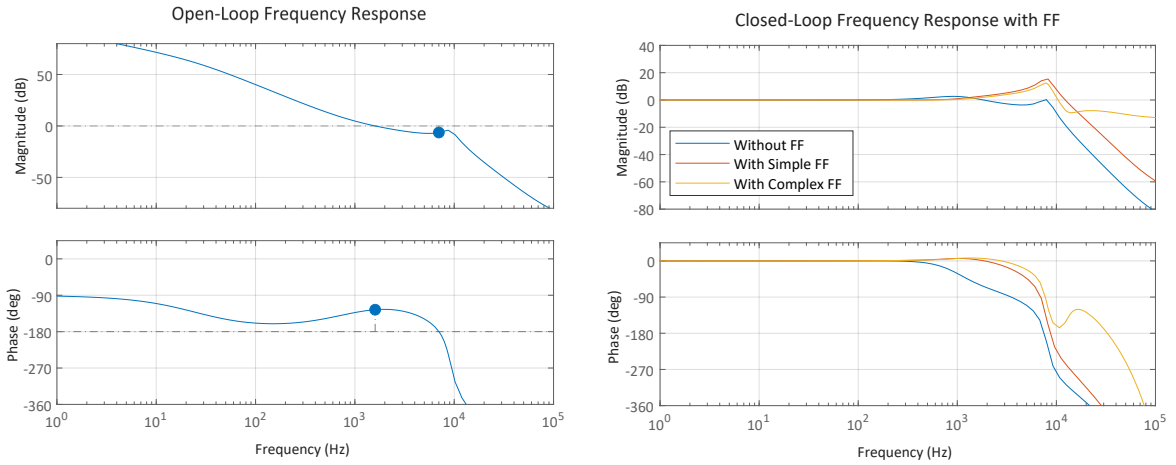


(a) Open-loop frequency response, indicated are PM = 45° and GM = 7 dB

(b) Closed-loop response with bandwidth f_{bw} = 8 kHz. The peak in frequency response is because of relatively high loop delay.

Figure 3.13: Frequency response of the capacitor voltage controller (M=128, K=3, N=2).

To sample the current, the ripple cancellation strategy as explained in subsection 3.1.2 can be used to keep group delay of the sinc filter limited. A PI controller will be used to obtain good steady-state tracking performance. The open-loop frequency response is shown in Figure 3.14a. By using Equation 3.21, the closed-loop response is found, of which the frequency response is shown in Figure 3.14b. The possible bandwidth for this controller is limited by the bandwidth of the voltage controller.



(a) Open-loop frequency response, indicated are PM=54° and GM= 6dB

(b) Closed-loop response with bandwidth f_{bw} = 1.6 kHz. FF provides significant improvements in frequency response.

Figure 3.14: Frequency response of the output current controller (M=128, K=3, N=2).

Feed-Forward Control

Same as for the parallel controller structure, for the outer current loop of the cascaded controller structure, a FF can be added (see subsection 3.1.2). Both the simple FF and complex FF from the cascaded structure are also possible for this structure. For complex FF, the pole pair of the LC-filter should not be taken for the notch filter as was the case for the parallel controller. But instead the pole pair of the closed-loop response of the voltage controller should be taken. In this case, these poles cause some resonance in this closed-loop controller, which can also be seen in Figure 3.13b. Putting the FF notch filter at this frequency improves phase response. The frequency and damping ratio can be found using numerical methods. Figure 3.14b shows the improvements in transfer function after implementing FF. Complex FF provides the best performance in terms of phase and frequency response.

3.3. Simulation

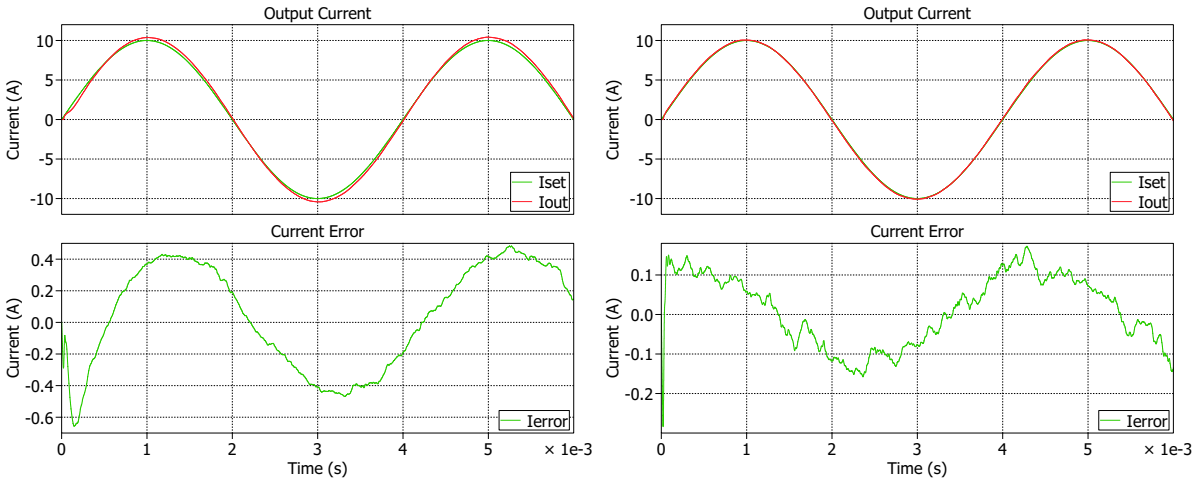
Now that an analytical model is defined for both controller structures, a simulation model can be build for verification. This is done using MATLAB Simulink with PLECS blocksets. PLECS is a tool for modelling circuit behavior with fast simulation speeds. It is used to model the behavior of the circuit and the load. A PWM signal is connected to two interleaved half-bridges consisting of 2 switches. Simulink is used to implement the controller, the sinc filter and the PWM generator. These are implemented digitally running simulation at FPGA clock speed (see section 5.2) to model real world behavior as accurately as possible. The DS ADCs are implemented using the control Toolbox of MATLAB, which convert the analog signals into a bitstreams. To discretize the continuous controller and FF function the forward Euler method will be used. This method provides the best match of continuous to digital domain, while requiring minimum computing power [6]. In this method, the substitute function is used:

$$s = \frac{1 - z^{-1}}{T_s \cdot z^{-1}} \tag{3.34}$$

Finally, the PWM generator is implemented using a counter for the carriers, in order to properly include the quantization error of the PWM generator. The performance will be evaluated by looking at a 250 Hz frequency setpoint with 10 A current magnitude using $V_{dc} = 200$ V.

3.3.1. Parallel Controller

Simulation results of the parallel controller are shown in Figure 3.15. The frequency response of the simulation without FF (0.33 dB and -1.0°) can be compared to the analytical results (0.25 dB and 0.3°). The magnitude estimation is quite accurate. However, the phase is negative instead of positive, which was expected from the analytical results. The simulation results including the FF (0.05 dB and 0.8°) are more accurate compared to the analytical results (0.01 dB and 0.9°), although the magnitude is still slightly different. The differences



(a) Simulation results of controller without FF. On the top figure the setpoint and output current, on the bottom the current error. The magnitude response is 0.33 dB and the phase response is -1.0°.

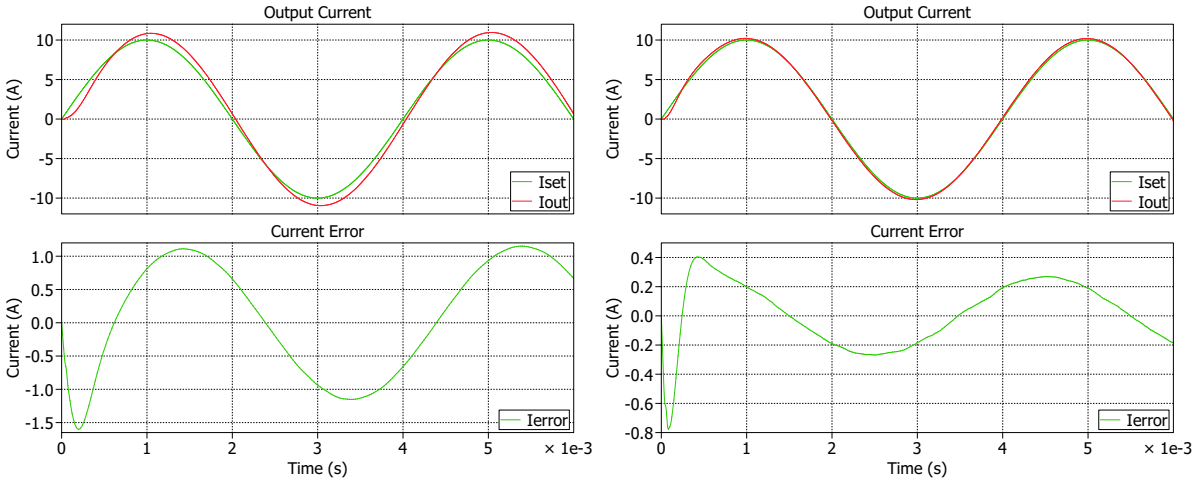
(b) Simulation results of controller using complex FF. On the top figure the setpoint and output current, on the bottom the current error. The magnitude response is 0.05 dB and the phase response is 0.8°.

Figure 3.15: Simulation results of the parallel controller with and without FF, for a setpoint of 250 Hz with 10 A amplitude.

can be explained in two ways:

- The FF is digitally implemented, which is not exactly equal to the continuous implementation used in analytical results.
- The FF function uses the location of the complex pole pair of the LC-filter. However, in subsection 3.1.1 it was shown that the poles depend on the damping delay, which is difficult to exactly determine as was explained in subsection 3.1.1.

Nevertheless, the analytical results give a good approximation of the simulated results.



(a) Simulation results of controller without FF. On the top figure the setpoint and output current, on the bottom the current error. The magnitude response is 0.8 dB and the phase response is -3.4°.

(b) Simulation results of controller using complex FF. On the top figure the setpoint and output current, on the bottom the current error. The magnitude response is 0.17 dB and the phase response is 1.1°.

Figure 3.16: Simulation results of the parallel controller with and without FF, for a setpoint of 250 Hz with 10 A amplitude.

3.3.2. Cascaded Controller

Simulation results of the cascaded controller structure are shown in Figure 3.16. The frequency response of the simulation without FF (0.8 dB and -3.4°) compared to the analytical results (0.5 dB and -0.4°), has relatively similar magnitude response but much higher phase delay. A possible explanation is that the loop delay estimates for the three cascaded loops used for the analytical results have a small deviation in the simulation. Because of the cascaded structure, a mismatch will cause a relatively high deviation in the frequency response.

The results of the FF (0.17 dB and 1.1°) are also different than what was expected from the analytical results (0.001 dB and 1.0°) in terms of magnitude response. The explanation is similar to that given for the cascaded controller structure, with the difference that the poles now depend on the accurate analytical expression of the capacitor voltage controller. A small difference in estimation can easily lead to larger differences in frequency response. As with the parallel controller structure, the simulation results for the cascaded controller structure are still close to the analytical expectations.

When comparing the simulation of the two different controller structures, the quantization noise of the parallel controller structure is higher than that of the cascaded controller structure. This can be explained by the low decimation factor of the damping loop in the parallel controller, which results in lower effective resolution.

This chapter proposed two different promising controller structures for modular interleaved high-precision current amplifiers. A detailed design procedure was provided for both controllers, giving all the analytical results. The chapter concluded by showing simulation results and comparing these with the analytical expectations.

4

Efficiency Increase in Interleaved Current Amplifiers

The introduction stated that the main focus of this research is increasing power density of current amplifiers used in lithographic systems in order to decrease the size of power electronics systems. In the previous chapter, the focus was on defining and comparing promising controller structures that can be used to provide advantages to the application in terms of modularity. Modularity enables the matching of current amplifier capabilities to particular system needs. Building on the controller structures discussed in the previous chapter, this chapter shifts focus to exploring two methods for reducing power losses, by making use of the possibilities that interleaving PWM in a multi-branch configuration offers. Reducing power losses will directly improve power density as components can become smaller, and cooling elements can be reduced in size. The chapter will start with an analytical approach to estimate power losses in the current amplifier. A model is created to define instantaneous power losses. A current profile for evaluation will be presented, which will be used to demonstrate the decrease in power losses for both methods. Next, the first of the two methods will be explained, which is PS. In this method interleaved branches will be turned on and off dynamically depending on the output current setpoint. For a lower setpoint this will reduce losses, since there will be no circulating current in phases that are turned off, eliminating both switch and inductor losses for these branches. A second method for reducing power losses is ZVS. In this method switching frequency is changed dynamically to achieve soft switching in the HB. The proposed interleaved topology gives advantages because of the higher effective switching frequency, maintaining low ripple and stability when changing the frequency. The methods will be implemented in simulation using the parallel controller structure, but could in theory be implemented as well on the cascaded controller structure.

4.1. Model for Power Losses

This section will present equations to estimate the power losses in the current amplifier. The losses can be divided into switch losses and inductor losses. Finally, a current profile to compare losses is presented. The goal is to make a model that provides an approximation of the instantaneous power losses as a term of total output current, number of active branches and switching frequency. To simplify the model, a constant output voltage of 0 V is assumed. Another important assumption is that the temperature remains constant. The inductor ripple is dependent on the switching frequency (f_{sw}) and can be written as:

$$I_{ripple}(f_{sw}) = \frac{V_{dc}}{4 \cdot L_f \cdot f_{sw}} \tag{4.1}$$

The Root Mean Square (RMS) value of the current flowing through a branch can be written [30]:

$$i_{RMS}(i_o, f_{sw}) = \sqrt{\left(\frac{i_o}{n}\right)^2 + \frac{I_{ripple}(f_{sw})^2}{12}} \tag{4.2}$$

Switch Losses

To determine the switch losses, the datasheet of a potential Silicon Carbide (SiC) switch will be used as a reference [17]. The switch losses can be split up into switching losses, conduction losses and deadtime losses. The

switching losses are provided in the datasheet directly for a range of transistor drain currents, and a lookup table is created, according to which interpolation can be used to determine losses. The voltage specified needs to be scaled to the actual voltage. The switching losses can be divided into turn-on and turn-off losses:

$$E_{on}(i_o, f_{sw}, n) = \frac{V_{dc}}{V_{DD_{datasheet}}} \cdot E_{on_{lookup}}(i_D) = \frac{V_{dc}}{V_{DD_{datasheet}}} \cdot E_{on_{look-up}}\left(\frac{i_o}{n} \pm \frac{I_{ripple}(f_{sw})}{2}\right) \tag{4.3}$$

$$E_{off}(i_o, f_{sw}, n) = \frac{V_{dc}}{V_{DD_{datasheet}}} \cdot E_{off_{lookup}}(i_D) = \frac{V_{dc}}{V_{DD_{datasheet}}} \cdot E_{off_{look-up}}\left(\frac{i_o}{n} \pm \frac{I_{ripple}(f_{sw})}{2}\right) \tag{4.4}$$

The drain current depends on the number of active branches, the output current at the moment of switching, and, depending on which quadrant the amplifier operates, the negative or positive amplitude of the ripple current. Calculating the instantaneous power from these quantities is achieved:

$$P_{switching}(i_o, f_{sw}, n) = n \cdot f_{sw} \cdot \left(E_{on}(i_o, f_{sw}) + E_{off}(i_o, f_{sw})\right) \tag{4.5}$$

If the switch operates with soft switching, specifically using ZVS, the turn-on switching loss can be assumed to be zero [15]. Another source of losses in the switches is the conduction loss, which is determined by the on-resistance of the switch and the RMS current flowing through the transistor, multiplied by the number of active branches:

$$P_{conduction}(i_o, f_{sw}, n) = n \cdot R_{ds,on} \cdot I_{RMS}^2 = n \cdot R_{ds,on} \cdot \left(\left(\frac{i_o}{n}\right)^2 + \frac{I_{ripple}(f_{sw})^2}{12}\right) \tag{4.6}$$

Finally, the deadtime losses are defined. These are the losses that are caused by the current flowing through the body diode during the deadtime. These are defined by a lookup table of the forward voltage drop of the diode in terms of current, extracted from the datasheet of the switch. Deadtime is indicated by T_{dt}:

$$P_{deadtime}(i_o, f_{sw}, n) = n \cdot f_{sw} \cdot V_{D_{look-up}}\left(\frac{i_o}{n}\right) \cdot T_{dt} \cdot \frac{i_o}{n} = f_{sw} \cdot V_{D_{look-up}}\left(\frac{i_o}{n}\right) \cdot T_{dt} \cdot i_o \tag{4.7}$$

Inductor Losses

The inductor losses can be divided into conductor losses, both AC and DC, and core losses. The total DC conductor losses are simply written as:

$$P_{inductor,dc}(i_o, f_{sw}, n) = n \cdot R_L \cdot I_{RMS}^2 = n \cdot R_L \cdot \left(\left(\frac{i_o}{n}\right)^2 + \frac{I_{ripple}(f_{sw})^2}{12}\right) \tag{4.8}$$

The AC conduction losses can be divided into losses due to the proximity effect and the skin effect. However, for a large number of turns, the proximity loss is multiple factors higher than the skin effect losses, which can be neglected [29]. Proximity effect losses can be estimated using Dowell's method [43]. The skin depth (d) needs to be defined:

$$d(f_{sw}) = \frac{1}{\sqrt{\pi \cdot \sigma \cdot \mu \cdot f_{sw}}} \tag{4.9}$$

With σ the conductivity and μ the magnetic permeability of the conductor material. The Dowell's curves can then be used to obtain the Dowell factor using a lookup table for the specific number of turns N, which is then used to determine proximity effect power losses:

$$P_{proximity}(i_o, f_{sw}, n) = n \cdot K_{Dowell_{lookup}}(d(f_{sw})) \cdot R_L \cdot I_{RMS}^2 = n \cdot K_{Dowell} \cdot R_L \cdot \left(\left(\frac{i_o}{n}\right)^2 + \frac{I_{ripple}(f_{sw})^2}{12}\right) \tag{4.10}$$

For the core losses, only the losses due to the switching frequency ripple will be taken into consideration, as simplification the low-frequency core losses due to the setpoint will be neglected. The fringing effect will also be neglected for this analysis. The losses are calculated using the Steinmetz equation [18]:

$$P_v(f_{sw}) = K_c \cdot f_{sw}^{\alpha} \cdot B(f_{sw})^{\beta} \tag{4.11}$$

Here, K_c, α and β are material parameters and can be extracted from the datasheet. The magnetic flux density can be expressed as:

$$B(f_{sw}) = \frac{L_f \cdot I_{ripple}(f_{sw})}{N \cdot A_e} \tag{4.12}$$

With A_e the cross-sectional area of the core. By multiplying with the volume of the core (V_e), and taking into account the number of active branches, the total core losses can be expressed as:

$$P_{core}(f_{sw}, n) = n \cdot P_v(f_{sw}) \cdot V_e \tag{4.13}$$

Current Profile
Next, a current profile is defined. This profile will be used both for quantifying improvements in power losses and for simulating the two proposed methods. In lithography machines, the wafer stage is quickly accelerated, after which it is kept at a constant velocity for a longer period of time. This means that a small period of time a large current is required for acceleration after which almost no current is required for the longer constant velocity time. This behavior is represented in the current profile shown in Figure 4.1. Having defined all the individual power losses, the total instantaneous power loss can be calculated by summing all sources of losses. For the analysis in this chapter, a supply voltage of V_{dc} = 800 V will be assumed. It is defined as a function of output current, switching frequency, and the total number of active branches:

$$P_{loss}(i_o, n, f_{sw}) = P_{switching} + P_{conduction} + P_{deadtime} + P_{inductor,dc} + P_{proximity} + P_{core} \tag{4.14}$$

In Figure 4.2 the instantaneous power losses are plotted for the current profile in Figure 4.1. Using integration, the average power loss over the full profile can be determined.

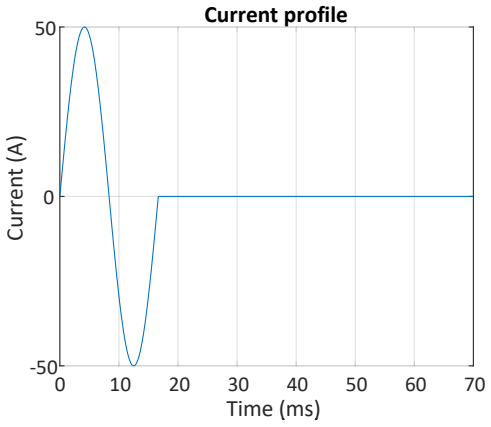


Figure 4.1: The current profile used as a reference to quantify losses.

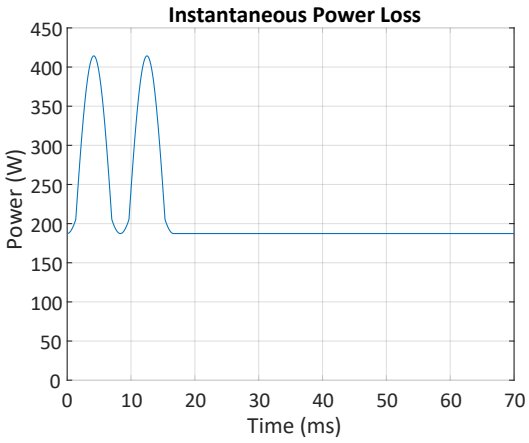


Figure 4.2: A plot of the total instantaneous power loss of the interleaved current amplifier, with f_{sw} = 80 kHz, V_{dc} = 800 V and n = 2.

4.2. Phase-Shedding

In PS, the power losses are decreased by dynamically turning branches on and off depending on the current setpoint. Turning off a branch means both HB switches will not be switching and will remain in the off-state. For low currents, only one branch will be active. When the setpoint reaches a certain value, an extra branch will be turned on, and output current load will be shared by more branches. PS is often used in paralleled DC-DC converters to increase small load efficiency but can also be found in interleaved inverter applications [33, 40]. This method is particularly useful in lithographic machines, which have short periods of high acceleration and thus high current setpoint and long periods of constant velocity, with low current setpoint (see Figure 4.1). The current threshold at which an extra branch should be added depends on power loss calculations and thus on particular component values as explained in section 4.1. It will be determined numerically by looking at the intersection of the power loss curve (see Figure 4.3). The power losses curve when applying PS is created by the combination of these curves, as is shown in Figure 4.4. By integrating this curve and comparing this to the case without PS, the average power loss decreases by 36 %.

4.2.1. Considerations for Control

Starting from a situation where only one branch is active and provides all the current to the output load. When the output current reaches the PS threshold, the second branch is turned on. After this happens, there

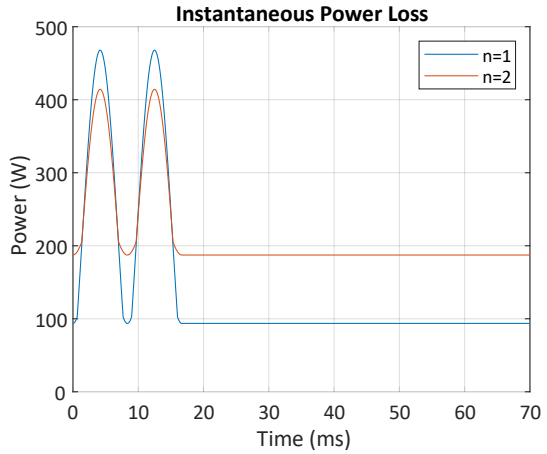


Figure 4.3: A comparison of the power loss for using n=1 and n=2 branches. Intersection point is used to determine PS threshold value, for this case $I_{PS} = 15$ A.

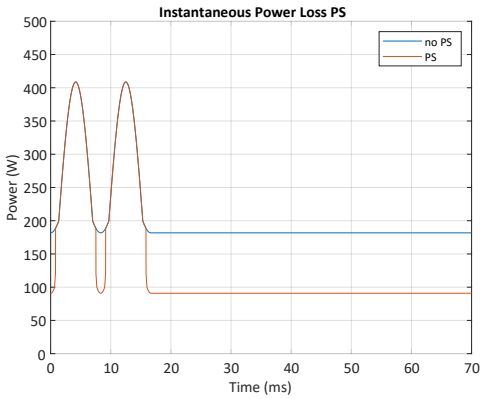


Figure 4.4: Power losses when applying PS. For lower current setpoint losses decrease by only using 1 branch.

is a mismatch in branch output current. This mismatch is corrected by the balancing loop from the parallel controller structure, as was explained in subsection 3.1.3. This loop ensures the branch current converge to be equal. For this reason it is important that the balancing controller has a high bandwidth. The longer it takes for the currents to equalize, the higher the additional power losses are.

Similarly, when the current setpoint goes below the PS threshold, a branch is turned off. However, this should not be done immediately. First, a balancing setpoint equal to the current setpoint is given, in order to achieve a situation where one branch provides all the output current and the other branch provides zero current. This means that in this case, the difference between the two branches diverges to the total output current setpoint. Once the branch current reaches zero, it can be switched off.
A first important consideration is that the balancing controller should be operational only when the second branch is turned on. The reason for this is to avoid having this controller correct for a mismatch in currents between branches that is desired, which is the case with PS, if one branch is turned off. If this is not the case, the balancing loop and tracking loop will counteract, and the output will be distorted.
A second consideration is that, when looking at the circuit topology in Figure 2.2, turning off a branch will eliminate the filter inductor for that branch. The branch capacitor should still be considered, because there is still current flowing through this capacitor. This means that the resonance frequency will decrease, depending on the number of active branches and the total number of branches. Equation 2.1 changes to:

$$f_r = \frac{1}{\sqrt{\frac{L_f}{n_{active}} \cdot C_f \cdot n_{total}}} \tag{4.15}$$

For controller purposes, the damping constant of the damping loop in Equation 3.3 also depends on the number of active branches:

$$K_d = 2 \cdot \zeta \cdot \sqrt{\frac{\frac{L_f}{n_{active}}}{C_f \cdot n_{total}}} \tag{4.16}$$

This means that when dynamically turning off and on the branches, the damping constant of the damping loop needs to dynamically change in order to keep the damping ratio constant. The observation that changing the number of active branches leads to a change in resonance frequency introduces a third control consideration. It was shown in subsection 3.1.2 that available bandwidth, with regards to stability, depends on a ratio of the resonance frequency. Lower resonance frequency with lower number of active branches means this ratio will decrease, which leads to a decrease in the GM. A consideration should be made regarding whether this decrease is acceptable for desired stability or if the bandwidth should be decreased when implementing PS.

4.2.2. Influence on Output Current

It is important to look at the influence on the output current when turning on or off a branch during PS. The influence on the output current should be as low as possible, so as not to compromise the performance of the high-precision current amplifier.
A first important consideration is the exact moment of turning on and off a branch. This should not influence the output current, and for that reason, it is important to switch exactly at the peak of the PWM generator carrier. At this moment the inductor current is exactly equal to the average inductor current, which should at that moment be exactly 0 A. Doing this ensures no influence on the output current, because the circulating current at this moment is also equal to 0 A.
A second consideration is taking into account the influence of the tolerances of the filter inductors on the output current. When applying PS, one filter inductor is providing the output current and the other is conducting 0 A. This will inevitably lead to a difference in filter inductance due to the saturation effect. This difference invalidates the assumption made in subsection 3.1.3, that the output voltage would not be influenced by the balancing loop. Instead, when the balancing loop acts during PS to converge the two branch currents, the output voltage, and thus output current will also be influenced. To model this effect, Equation 3.27 is extended to include the capacitor voltage (u_c), the damping constant (K_d) and the tolerance of the filter inductor of one branch (ϕ):

$$\frac{d}{dt}\begin{bmatrix} i_{L_{f1}} \\ i_{L_{f2}} \\ u_c \\ i_o \end{bmatrix} = \begin{bmatrix} -\frac{-K_d-R_{Lf1}}{L_{f1}\cdot\phi} & \frac{-K_d}{L_{f1}\cdot\phi} & \frac{-1}{L_{f1}\cdot\phi} & \frac{K_d}{L_{f1}\cdot\phi} \\ \frac{-K_d}{L_{f2}} & \frac{-K_d-R_{Lf2}}{L_{f1}} & \frac{-1}{L_{f2}} & \frac{K_d}{L_{f2}} \\ \frac{1}{C_f\cdot n} & \frac{1}{C_f\cdot n} & 0 & \frac{1}{C_f\cdot n} \\ 0 & 0 & \frac{1}{L_o} & -\frac{R_o}{L_o} \end{bmatrix} \cdot \begin{bmatrix} i_{L_{f1}} \\ i_{L_{f2}} \\ u_c \\ i_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{f1}\cdot\phi} \\ -\frac{1}{L_{f2}} \\ 0 \\ 0 \end{bmatrix} \cdot u_{PWM} \tag{4.17}$$

Using this equation the frequency response of the influence of the output current as function of the balancing loop output voltage difference can be plotted and is shown in Figure 4.5. For lower frequencies, the influence is very large, and a response of the balancing loop will result in a large distortion on the output current. For higher frequencies, however, the much higher output inductance relative to the filter inductance ($L_o >> L_f$) limits the distortion on the output current. In the same figure, the sensitivity of the current tracking loop is shown, which illustrates how the disturbances on the output current are rejected. It appears that the lower frequency disturbances created by the balancing controller are very well corrected by this loop. The actual frequency response of the output disturbance as a function of the balancing loop voltage difference is obtained by multiplying these two transfers:

$$S_{dt}(s)\left[\frac{i_{o,error}}{u_{b,PWM}}\right] = S_t(s)\left[\frac{i_{o,error}}{i_{disturbance}}\right] \cdot S_e(s)\left[\frac{i_{disturbance}}{u_{b,PWM}}\right] \tag{4.18}$$

This resulting sensitivity frequency response is shown in Figure 4.6, and has its maximum magnitude response at high frequency. It also shows that higher filter inductor difference results in higher output current distortion. The analytical model can be finalized by including the open-loop response of the balancing controller, as was defined in subsection 3.1.3:

$$S_{eb}(s)\left[\frac{i_{o,error}}{\Delta i_{o,b}}\right] = S_{dt}(s)\left[\frac{i_{o,error}}{u_{b,PWM}}\right] \cdot G_d(s)\left[\frac{u_{b,PWM}}{\Delta i_{o,b}}\right] \tag{4.19}$$

The result is the frequency response of the output current error to a difference in branch currents. At the moment of PS, the difference in filter inductor currents is a step response with magnitude equal to the PS threshold. Figure 4.9 shows the analytical result of the output current error for this step response. It shows that the output current error has a high frequency and is quickly damped by the fast tracking current loop. Application specifications should determine if this output current error is acceptable, but a current error of a high frequency means that the position error will be minimal in high-precision applications [32].

4.2.3. Simulations

Using PLECS simulation, PS can be added to the simulation of the parallel controller structure as defined in section 3.3. The resulting simulated inductor currents are shown in Figure 4.7. When the output current setpoint increases above the PS threshold, the second branch is activated and the branch currents converge due to the balancing loop. After the current drops below this setpoint, the branch currents diverge and the second branch turns off when it reaches zero current.

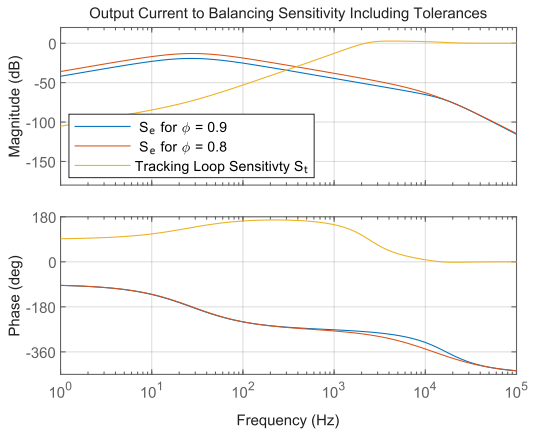


Figure 4.5: This figure shows the sensitivity of the output current to a difference in branch PWM voltage setpoints due to balancing. It shows that higher filter inductor difference leads to higher output current error. The figure also shows the sensitivity of the tracking loop to the output current distortion.

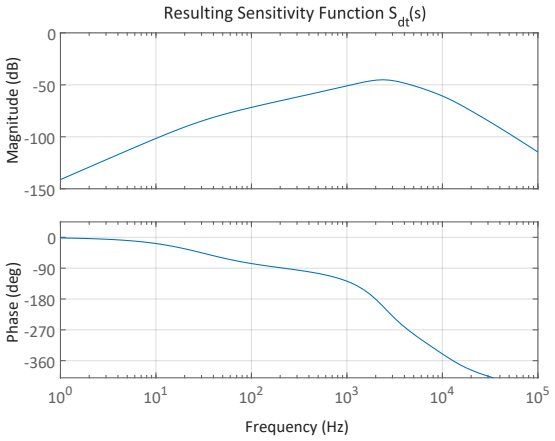


Figure 4.6: This figure shows the resulting transfer function of the balancing PWM setpoint voltage difference to the output current error, for inductor tolerance $\phi = 0.8$

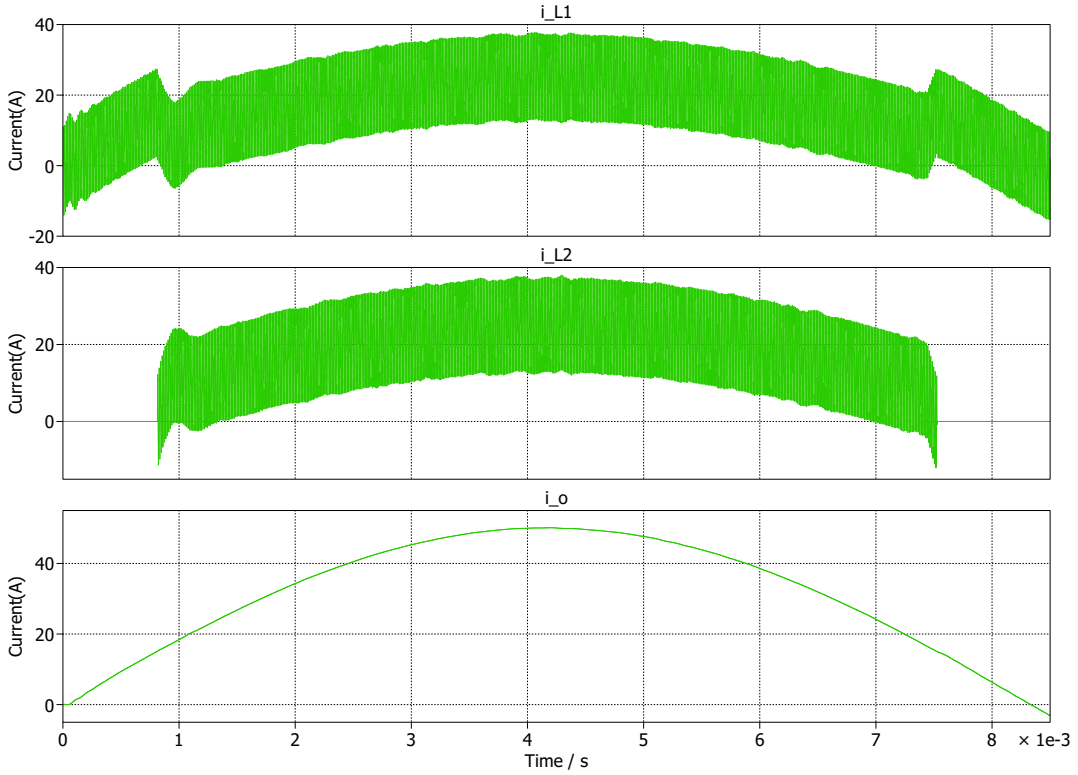


Figure 4.7: The inductor currents when PS is applied for the first part of the current profile. There is some small overshoot due to the fast balancing loop, but this does not influence the output current.

Figure 4.8 shows a zoomed image of the part where the PS is being activated. It shows that if the second branch is turned on at the top of the PWM carrier, the inductor current starts exactly in the middle of the ripple. Figure 4.9 shows the output current error due to tolerance in filter inductors as explained in subsection 4.2.2. The simulation is close to the analytical expectations, although the frequency of the simulated output current error is slightly higher. A possible explanation for this difference is the non-ideal active damping in the parallel controller structure, as was explained in subsection 3.1.1.

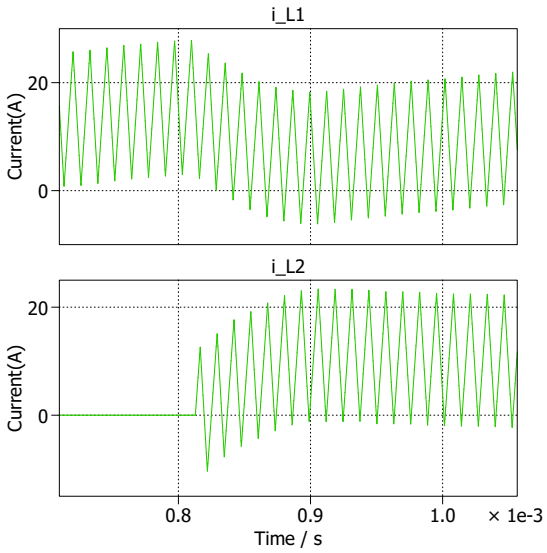


Figure 4.8: A closer look at the inductor currents the moment an extra branch is turned on, the branch currents quickly converge. The second branch is turned on exactly at the moment there is no inductor ripple.

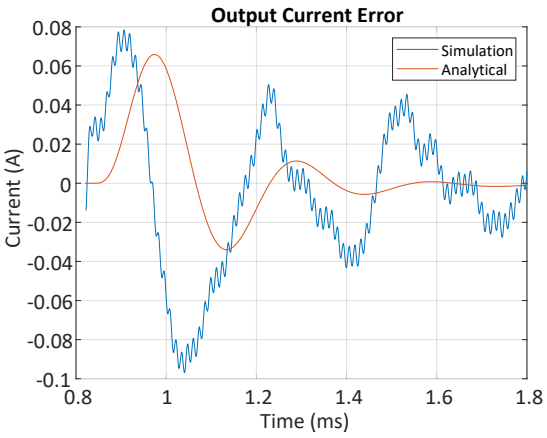


Figure 4.9: Simulated and analytical output current error when activating PS due to filter inductor tolerance ($\phi = 0.8$)

4.3. Zero-Voltage Switching

The next strategy to improve power efficiency in interleaved current amplifiers is ZVS. This strategy takes advantage of the fact that in SiC switches, turn-on losses are multiple times higher than turn-off losses [17]. If the current in the switch is reversed before switching, the voltage over the switch is essentially zero which causes substantially lower switch losses. To ensure that the current reverses, Huang [20] proposes a technique that dynamically changes the switching frequency. The general idea of this strategy is illustrated in Figure 4.10. Decreasing switching frequency increases inductor current ripple which makes sure that inductor current reverses direction before turning on the switch. This is the case as long as the inductor current ripple amplitude is higher than the output current. This always happens at output current near 0 A, but for higher output currents the switching frequency can be decreased.

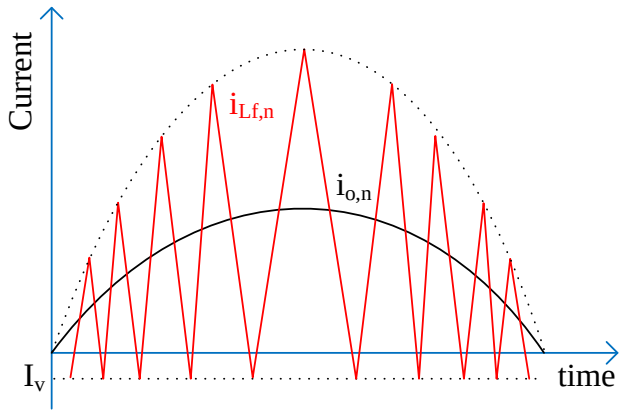


Figure 4.10: Illustration of the selected ZVS technique with dynamically changing switching frequency. Decreasing this frequency increases inductor current ripple.

4.3.1. Dynamic Switching Frequency

The proposed method relies on dynamically changing the switching frequency. To determine this frequency, complex zero-crossing-detection algorithms have been developed such as in [24]. To keep control simple, an easier approach is to use a calculation based on known circuit parameters and a voltage measurement [41]. A valley-current (I_v) is defined (see Figure 4.10), which should be kept as small as possible, but large enough to provide some margin for the current to reverse. Combining this with the current setpoint, an equation for the switching frequency can be expressed as:

$$f_{sw} = \frac{V_{dc} - v_o}{2 \cdot L_f \cdot (i_{set} + I_v)} \cdot \left(\frac{v_o}{V_{dc} + 0.5} \right) \tag{4.20}$$

Using this equation, the optimal switching frequency for ZVS for a given current setpoint can be calculated. The range of switching frequencies cannot extend indefinitely, and limits should be defined. For the upper limit, the switching frequency defined in Table 2.1 is selected, because increasing it further will not significantly reduce losses and would require performance improvement of other hardware elements such as the FPGA. To determine the lower switching frequency limit two aspects are important. First, lowering the switching frequency will increase output current ripple, since ripple attenuation by the LC-filter decreases. This is where the advantage of interleaved PWM for ZVS becomes apparent. In section 2.3, it was explained that the effective switching frequency increases proportionally to the number of phase-shifted branches n. The current ripple should not increase with ZVS compared to a single branch implementation. Following this statement, the lower limit for the switching frequency can be expressed as:

$$f_{sw_{min,n}} = \frac{f_{sw_{n=1}}}{n} \tag{4.21}$$

Another aspect to consider is the influence on controller stability, with particular focus on the damping loop. subsection 3.1.1 defined the stability of this loop to be dependent on the sum of the loop delays. T_{sinc} and T_{calc} can remain constant independent on switching frequency if the sampling frequency remains constant. However, the delay of the PWM modulator $T_{d,PWM}$ is dependent on the switching frequency [31]. Again, interleaved PWM offers an advantage. Cvetanovic [12] states that the modulator delay decreases with increasing number of branches with interleaved PWM as:

$$T_{d,PWM_n} = \frac{T_{d,PWM_{n=1}}}{n} \tag{4.22}$$

This is used to determine that for controlling purposes, Equation 4.21 also provides the lower limit of the switching frequency when implementing ZVS. This means that for both considerations, ripple current and controller stability, increasing the number of interleaved branches gives a higher dynamic switching frequency range for ZVS.

4.3.2. Simulation

Now that the theory of ZVS has been discussed, an estimation of the power losses can be provided. For this, the switching frequency is dynamically changed in the power losses model presented in section 4.1. To give some margin, the lower limit of the switching frequency is set to $0.75 \cdot f_{sw}$ for $n = 2$. Using Equation 4.20, Figure 4.11 shows the optimal switching frequency for the given current profile. The switching frequency saturates at the lower limit, which means from this point, there will be no ideal ZVS. However, since the current through the switch will still be lower, the losses will still decrease compared to no ZVS. This effect is shown in the results of the power simulation in Figure 4.12. Compared to PS, ZVS provides power efficiency increase at higher current setpoints. For the given current profile, the losses only decrease by 2%. The efficiency increase is limited by the increase in filter inductor losses due to a higher ripple current, which results in more losses. This can still have positive effects on the lifetime of the switches, which is largely dependent on the temperature fluctuations in the switches, which are proportional to the losses [4]. Additionally, when setpoints with higher current peaks are used, the increase in efficiency will be more significant.

Using a PLECS simulation, ZVS was implemented in the simulation of the parallel controller structure as defined in section 3.3. The resulting simulated inductor currents are shown in Figure 4.13. It can be observed that the inductor current ripple increases so that ZVS is achieved until the lower limit of switching frequency is reached. Even then, the turn-on losses of the switch are lower due to the lower current at the turn-on instance. The simulation shows that a small resonance occurs when the switching frequency is dynamically

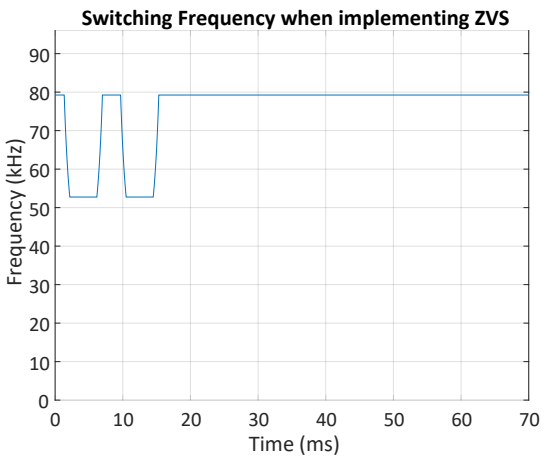


Figure 4.11: The calculated switching frequency for the current profile given in Equation 4.1.

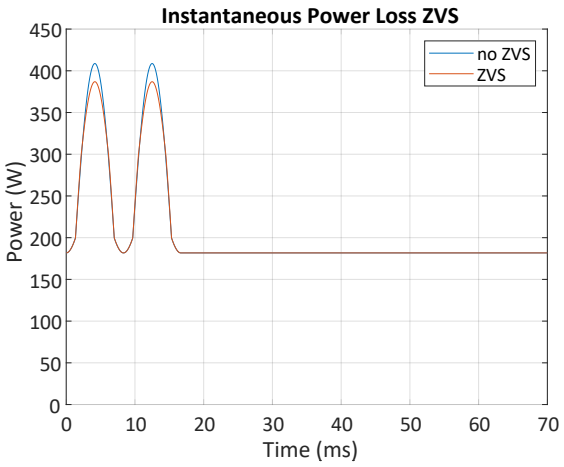


Figure 4.12: Analytically estimated power losses when applying ZVS, the power losses increase become significant only for high current setpoints.

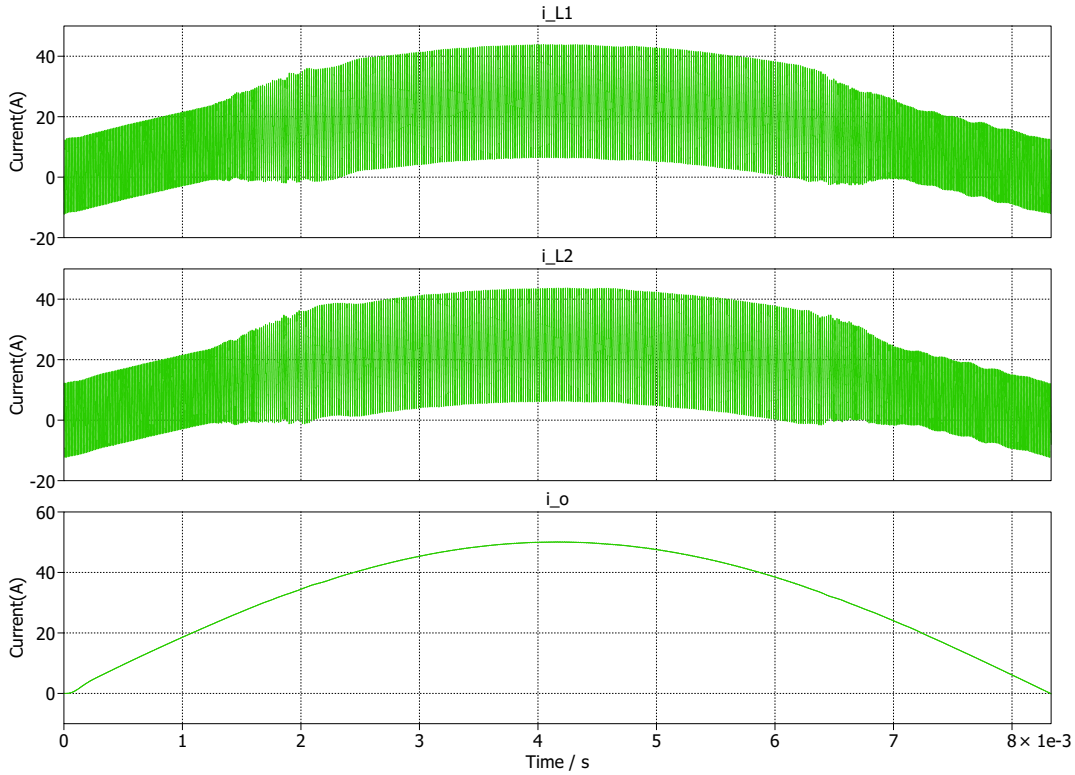


Figure 4.13: The inductor currents when ZVS is applied for the first part of the current profile. The switching frequency increases, which increases the inductor current ripple and decreases switching losses.

changed. This resonance is triggered by the changing output voltage ripple amplitude, which is a consequence of the changing ripple frequency. This resonance is very small and has a high frequency, so it will not have a significant impact on performance.

5

Prototype Implementation and Measurements

This chapter describes the prototype implementation that is used to validate and compare the two designed controller structures. First, an overview of the hardware and the test setup will be provided. Next, the design of the FPGA firmware will be explained and a schematic overview is given. Measurement results are shown, first with an analysis at low current to compare controller behavior, after which measurement waveforms for larger current setpoints at the full voltage are shown for verification. Finally, the chapter concludes by providing a comparison of the different controller structures based on various criteria.

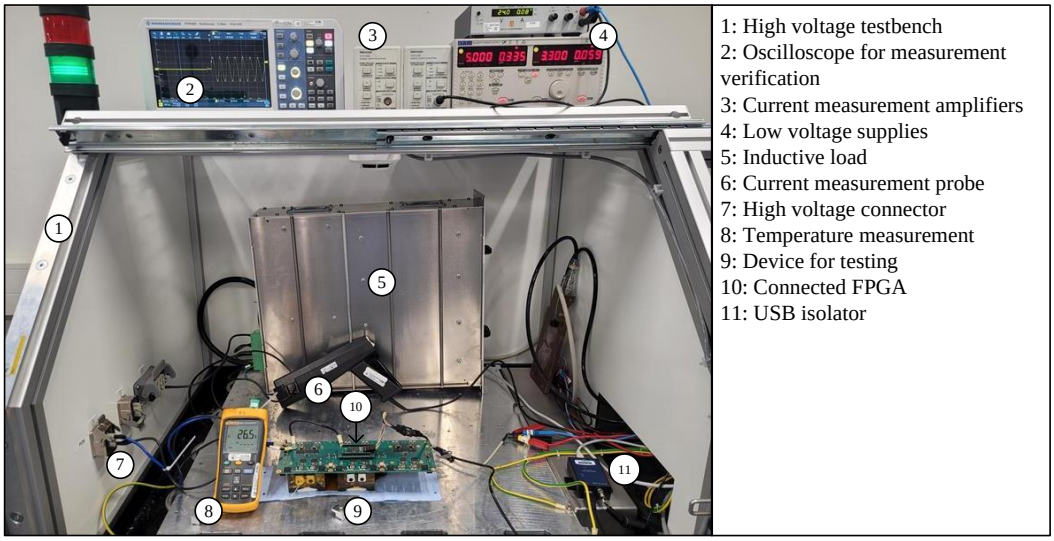


Figure 5.1: Overview of the test setup in the high voltage test bench with indicated parts.

5.1. Hardware Demonstrator and Test Setup

The hardware demonstrator consists of two phases of a three-phase inverter connected to form the circuit topology required for testing the controller structures with two branches, as illustrated in Figure 2.2b. A FPGA of type Spartan-7 is connected to implement the controller structures. The choice of using a FPGA over a microcontroller or digital signal processor was made because of the high number of parallel tasks that can be performed by a FPGA. This requirement arises from the number of sinc filters for data acquisition that need to be run in parallel as well as other tasks such as the controllers and PWM generation. For paralleling tasks, a FPGA provides superior behavior, by at the same time staying a very cost-efficient solution. For this prototype only, a single FPGA is connected to both branches. Figure 5.1 shows the test setup built in a high voltage test

bench for safety reasons. The circuit containing the two branches is connected to a symmetrical high voltage power supply and an inductive load with series resistance, as in the circuit topology. It is important that the high voltage comes from power supplies that can operate in two quadrants in order to handle the bidirectional current flow to the load. The FPGA, gate drivers, and ADCs are connected to low voltage supplies. A JTAG to USB connector is used to communicate with the FPGA. For safety reasons the USB connection is isolated before connecting to the PC. An oscilloscope is connected to a current probe via a current amplifier to validate output current measurements. Finally, the temperature of the switches is monitored using a thermocouple. The switches are not connected to a heatsink in this test setup because only very short current profiles will be tested. A summary of the prototype and test setup parameters is shown in Table 5.1.

Table 5.1: Prototype and Test Setup Parameters.

Parameter	Specification
Input Voltage (Small-Signal)	± 100 V (±24 V)
Low Voltage Supply Voltages	3.3 V, 5 V, 24 V
Max Tested Output Current	10 A_{peak}
Switching Frequency	78.125 kHz
Filter Capacitance	$2 \times 0.47 \mu F$
Frequency of DS ADCs	20 MHz
Filter Inductance	104 μH
Output Inductance	1.37 mH

5.2. FPGA Firmware

In Figure 5.2 a schematic overview of the designed FPGA firmware is provided. The function of each block will be explained separately.

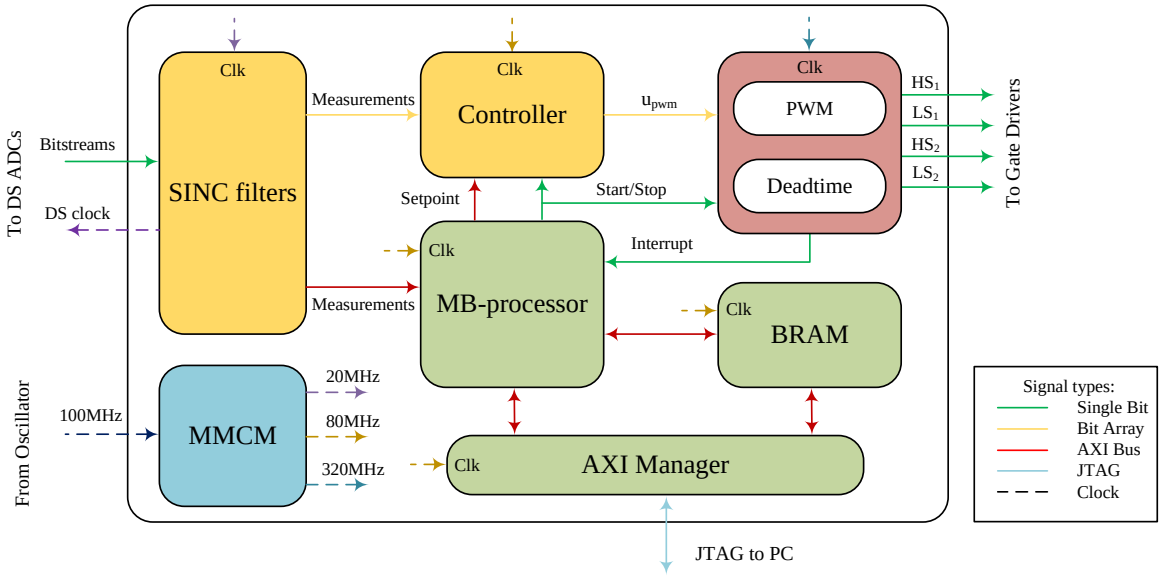


Figure 5.2: A schematic overview of the FPGA firmware. Signal types for the connection between different blocks are highlighted.

AXI manager

The AXI manager enables the FPGA to communicate with Matlab, to load the current setpoint and to extract the measurement data. The JTAG bus has insufficient speed to provide the setpoint data in real-time. For that reason, setpoint data will first be loaded on an internal Block Random-Access Memory (BRAM). A start signal is provided via JTAG indicating to the processor to start running the profile. After the profile has been run,

the PC can extract the measurement data from the BRAM via the JTAG bus. Using this method, setpoint and measurement data can be analyzed and compared, since timing will be synchronized.

BRAM
The internal FPGA BRAM is used to store setpoint data from the PC and measurement data from the sinc filters. The size of the BRAM determines the possible duration of the profile.

MicroBlaze-processor
A soft core MicroBlaze-processor takes care of the communication between the BRAM, the sinc filters, and the controller. This is essentially a small microprocessor that is created on the digital FPGA fabric. It receives a start signal from the PC via the AXI manager, after which it sends a start signal to the PWM generator and the controller. After startup, the first current setpoint is loaded to the controller. Based on an interrupt signal coming from the PWM generator, the next current setpoint is loaded from the BRAM into the controller. At the same time it collects the measurement data from the sinc filters and loads it into the BRAM.

Controller
In this part, the controller structures, as explained in chapter 3, are implemented. It takes the measurements from the sinc filter and obtains the setpoint from the processor to provide an output reference to the PWM generator. For the parallel controller structure, the three controller loops are run in parallel, and the output reference is generated by adding the setpoints. For the cascaded controller structure, the three controllers are run sequentially, where each loop takes the setpoint of the previous loop when it is finished calculating.

Sinc filters
This block contains the digital sinc filters to retrieve the data from the DS ADCs as explained in section 2.4. The 20 MHz clock going to the DS ADC determines the precise value of the PWM frequency:

$$f_{PWM} = \frac{DS_{clk}}{M} = \frac{20\,\text{MHz}}{256} = 78.125\,\text{kHz} \tag{5.1}$$

The current setpoint is provided to the controller at twice this frequency, at 156.25 kHz. Table 5.2 provides a summary of various parameters for sampling using sinc filters for the two controller structures. Unfortunately, it was not possible to implement phase-shifted sampling times, which means that the inner loop of the cascaded controller could not be over-sampled, as explained in subsection 3.2.1, leading to slightly less stability.

Table 5.2: A summary of the different sampling parameters for the different controllers using DS sampling frequency f_S = 20 Mhz.

Controller Loop	**Parameter**	**Data rate (f_D)**	**Over-sampling factor (N)**	**Sinc filter order (K)**	**Decimation ratio (M)**	**Notch at f_{pwm}**	**Group delay**	**ENOB**
Parallel Controller								
Damping Loop	i_c	625 kHz	8	3	32	No	2.4 μs	11.4 bits
Tracking Loop	i_o	156.25 kHz	2	3	128	No	9.6 μs	16.4 bits
Balancing Loop	$i_{o,n}$	78.125 kHz	1	3	256	Yes	19.2 μs	18.9 bits
Cascaded Controller								
Inner Loop	i_{Lf}	156.25 kHz	1	2	256	Yes	12.7 μs	13.5 bits
	u_c	156.25 kHz	2	3	128	No	9.6 μs	16.4 bits
Voltage Loop	i_o	156.25 kHz	2	3	128	No	9.6 μs	16.4 bits
	u_c	156.25 kHz	2	3	128	No	9.6 μs	16.4 bits
Tracking Loop	i_o	156.25 kHz	2	3	128	No	9.6 μs	16.4 bits

PWM generator
The PWM generator receives the setpoint from the controller and generates an output PWM for each of the 4 HB switches. It does this by generating a triangular carrier signal and comparing the input to this carrier. The carrier for each of the 2 branches is 180° out of phase to create interleaved PWM. The number of quantization steps depends on the clock frequency and on the PWM frequency:

$$n_q = \frac{f_{clk}}{2 \cdot f_{PWM}} = \frac{320\,\text{MHz}}{2 \cdot 78.125\,\text{kHz}} = 2048\,\text{steps} \tag{5.2}$$

An interrupt signal is generated here to tell to the processor both new measurement sample and the next setpoint can be taken. The reason this interrupt signal is generated in the PWM generator is because it is important that sampling and controller setpoints are aligned with the PWM carriers. Finally, using a counter a predefined deadtime of 100 ns is included into the output gate driving signals.

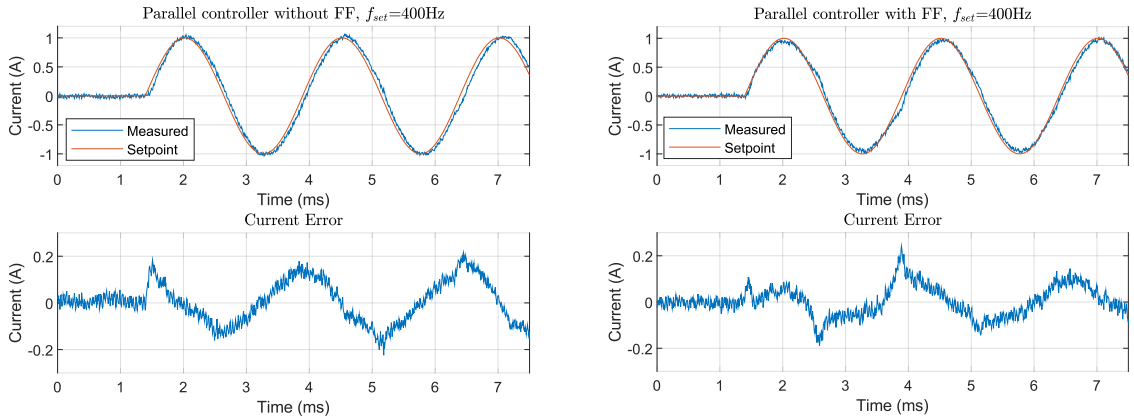
MMCM
A Mixed-Mode Clock Manager (MMCM) is used to convert the 100 MHz oscillator clock signal into the required clock signals for the design. An 80 MHz clock is selected for the processor and controller because it gives good execution performance, but also enough time to finish digital multiplications. The PWM generator does not contain any multiplications, the clock is therefore increased to obtain a high number of quantization steps.

5.3. Measurements

In this section the measurements of the hardware implementation will be shown. First, small-signal measurements will be shown and used to compare with the analytical results. These will be conducted at low voltage (V_{dc} = 48 V) and low current (I_{peak} = 1 A) to limit the effect of non-linear elements in the prototype. Finally, also measurements at full voltage and larger current are shown to validate correct operation under these conditions.

5.3.1. Parallel Controller

Figure 5.3 shows the measurements for the parallel controller structure, as well as the resulting current error. It shows that the current follows the setpoint as expected and there is only small error. When complex FF is added, there is a little more distortion during settling. Overall, the current error decreases significantly.



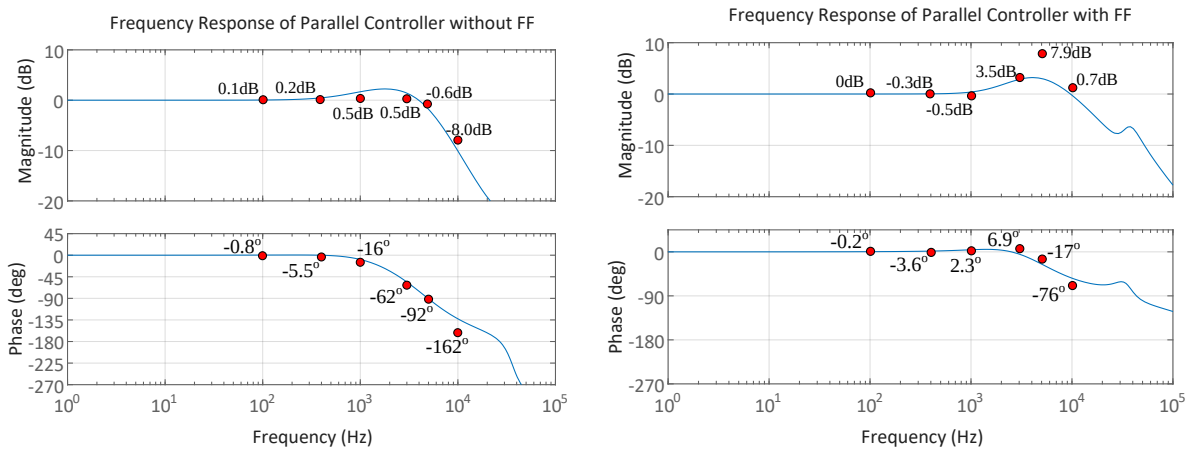
(a) Current measurements without FF

(b) Current measurements with complex FF.

Figure 5.3: Showing the measurements for the parallel controller structure. In the top, the current measurement relative to the current setpoint of 400 Hz with a 1 A amplitude. The figures on the bottom show the resulting current errors.

Using these measurements, the frequency response in terms of magnitude and phase can be derived. By taking measurements at a number of frequencies, a picture can be created for the total frequency response, which is shown in Figure 5.4. The measurements are compared with the analytical results. For the case without FF the magnitude and phase match very well, with the measured values giving a flatter magnitude response than was expected. The frequency response including FF shows that the magnitude deviates a bit

more from the the analytical results, which can be explained by inaccurate damping poles estimation, as explained in section 3.3. However, because of the large improvement in phase response, complex FF gives better overall tracking performance.



(a) Without FF

(b) With FF

Figure 5.4: Frequency response for a set of measurements compared to the analytical results for the parallel controller structure.

To validate the operation of the balancing controller loop, the error in branch currents can be measured. Figure 5.5 shows this measurement for a situation with and without an active balancing controller. The output current setpoint is the same as Figure 5.3. It shows that without any active balancing, a current is flowing between the branches that is multiple times bigger than the output current. This can be explained by non-idealities such as tolerances in the circuit elements. The balancing control is able to suppress this current, in order to reduce subsequent losses.

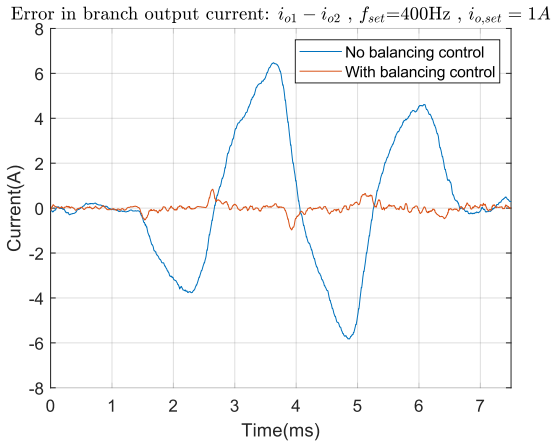


Figure 5.5: Measurements of the error current between the branches to show the impact of the balancing loop.

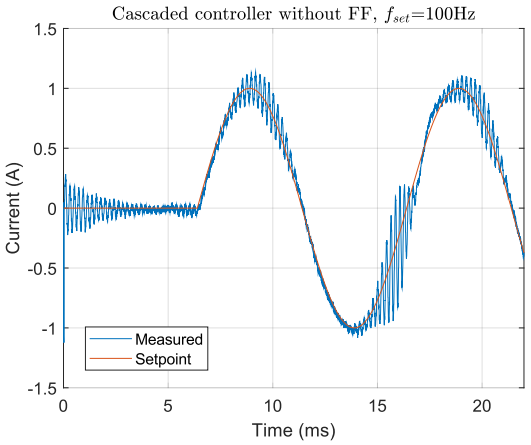


Figure 5.6: The initial testing of the cascaded controller structure causes undesired oscillations.

5.3.2. Cascaded Controller

Next, the cascaded controller structure was implemented in the hardware demonstrator according to the design. However, when running at low voltage, a problem was encountered. Figure 5.6 shows that when running a current setpoint, undesired oscillations occur. These oscillations originate from the capacitor voltage decoupling for the inner loop. When the inner control loop was disconnected, these oscillations still occurred. An analysis of this capacitor voltage decoupling was conducted using the equivalent circuit in Figure 5.7. The decoupling can be modeled as a delayed voltage addition of the capacitor voltage to the PWM setpoint. It is multiplied by a constant K, to indicate a gain error. This gain error can arise due to non-linearities in the measurement circuit, offset errors, or distortion. T_d indicates the total loop delay for this decoupling voltage

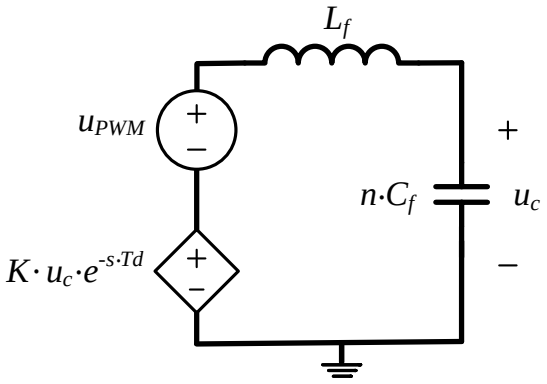


Figure 5.7: Circuit for modelling the decoupling of the capacitor voltage. It includes a gain error factor K and the decoupling loop delay T_d.

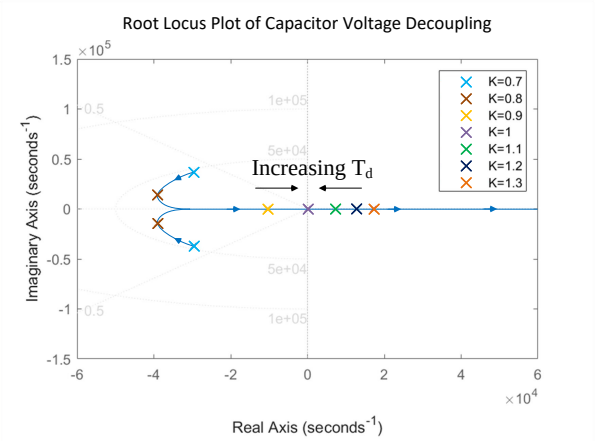


Figure 5.8: Root locus plot for the changing poles of the modelling circuit for capacitor voltage decoupling for different values of gain factor (T_d= 12 μs).

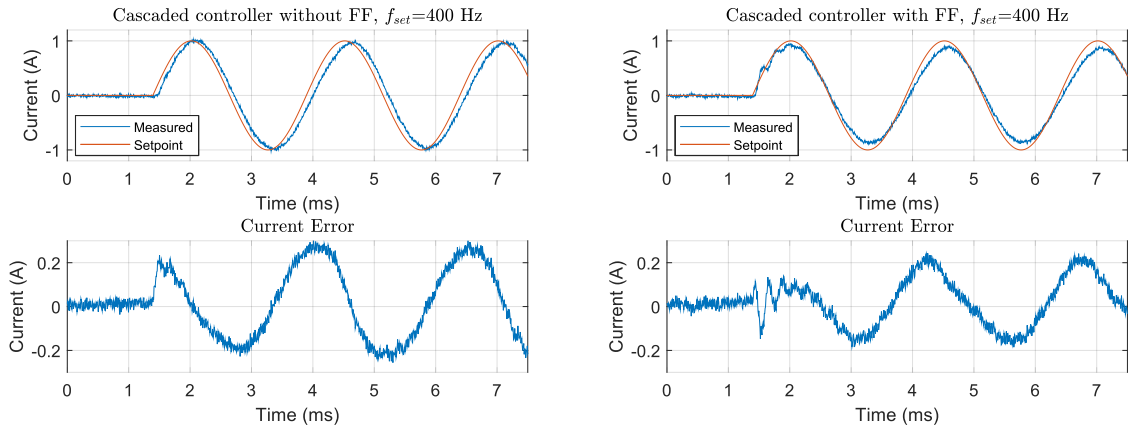
as explained in subsection 3.1.1. Using the equivalent circuit, the transfer function for the capacitor voltage can be expressed as:

$$\frac{u_c}{u_{PWM}}(s) = \frac{1}{s^2 \cdot L_f \cdot C_f \cdot n + 1 - K \cdot e^{-s \cdot T_d}} \tag{5.3}$$

In an ideal case this decoupling leads to a double pole in the transfer function at the origin. However, Figure 5.8 shows that the location of these poles depends on both K and T_d. It shows that for a gain larger than unity ($K > 1$) the poles will move into the unstable right-half plane. For gain smaller than unity ($K < 1$), the poles will move further into the stable left-half plane. An increase in decoupling delay will push the poles closer to the origin. This means that selecting a gain smaller than unity creates a margin in capacitor voltage gain before the pole moves into the right-half plane.
Two design considerations were made based on these results. First, for the implemented cascaded controller a gain value of K=0.95 was selected to keep sufficient stability margin. The consequence of this is that decoupling will not be ideal, and this will influence the closed-loop response. A second design consideration explains the high bandwidth of the capacitor voltage controller that was selected in subsection 3.2.2. Better sensitivity performance will result in greater suppression of any oscillations.
Figure 5.9 shows the measurements for the cascaded controller structure, as well as the resulting current error. It shows that the current follows the setpoint as expected and there is only small error. However, the error is not as small as with the parallel controller structure. When FF is added, there is a little more distortion during settling, which appears to be similar to the distortion for the cascaded controller due to the decoupling loop. Overall, the current error decreased when implementing complex FF. Similar as with the parallel controller, these measurements were used to validate the analytical frequency response. In Figure 5.10a, this is shown for the case without FF. It follows the analytical estimation well in terms of bandwidth. However, there is significant peaking for frequencies around the bandwidth of the voltage controller. This can be explained by the estimation of the delays in the controllers. A small deviation in delay estimation will result in a large deviation in frequency response. The same applies to the case without FF, which is shown in Figure 5.10b. Another possible explanation for the deviations is the lower gain factor $K = 0.95$, which was expected to reduce bandwidth.

5.3.3. Large-Signal Verification

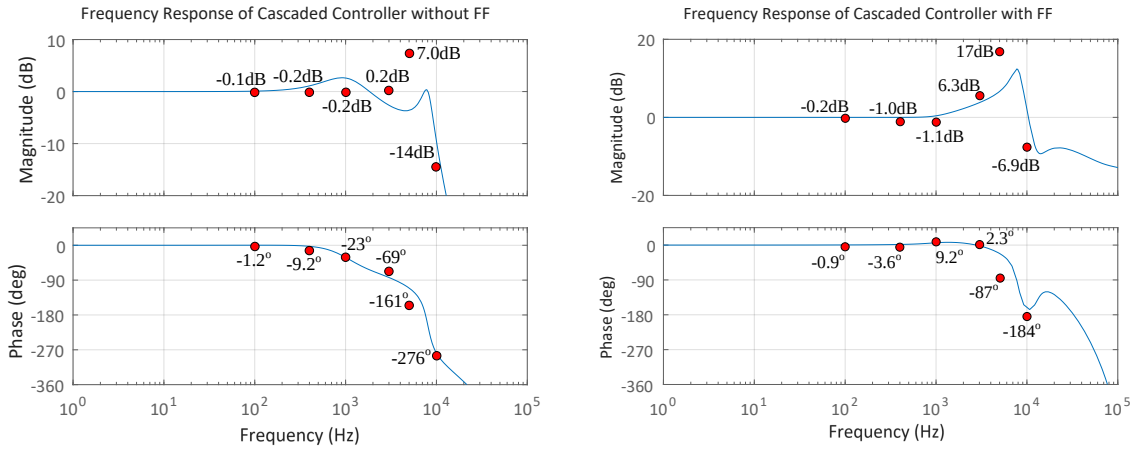
To finalize, measurements for larger setpoints were conducted to show behavior at these condition. This is done by increasing the supply voltage to $V_{dc} = 200$V and the current setpoint to 10 A peak. The measurements were conducted for the cases without FF and can be seen in Figure 5.12. It can be concluded that for larger signals, the parallel controller behaves better than the cascaded controller. For the cascaded controller, the magnitude is much lower than expected. For both signals, a small resonance can be seen in the signal, which is expected because of non-ideal damping. For the cascaded controller, this is at a lower frequency, at the



(a) Current measurements without FF

(b) Current measurements with complex FF.

Figure 5.9: Showing the measurements for the cascaded controller structure. In the top, the current measurement relative to the current setpoint of 400 Hz with a 1 A amplitude. The figures on the bottom show the resulting current errors.



(a) Without FF

(b) With FF

Figure 5.10: Frequency response for a set of measurements compared to the analytical results for the cascaded controller structure.

poles of the capacitor voltage controller. Since the controller is designed to behave linearly, deviations from the small-signal measurements can be explained by nonidealities in the circuit elements.

5.4. Controller Comparison

Now that the controller structures have been explained in detail and measurements have been conducted for verification, a comparison can be made. Note that this comparison is not a general comparison of the particular controller structures, but of controllers specifically tuned for the modular approach using DS ADCs.

Bandwidth

The maximum possible bandwidth of the parallel controller is higher than that of the cascaded controller. The reason for this is that the bandwidth of the cascaded controller is limited by the available bandwidth of the inner loop and voltage loop. The inner inductor loop bandwidth is mainly limited by the high delay of the DS ADC, which requires a notch at the PWM frequency. The bandwidth of the parallel controller is limited by the resonance frequency of the LC-filter. Increasing the bandwidth results in thinner stability margins.

Frequency response

A comparison of the analytical frequency response for the two controller structures is shown in Figure 5.13. The measurements show that there is small deviation from these analytical expectations, but they can still be

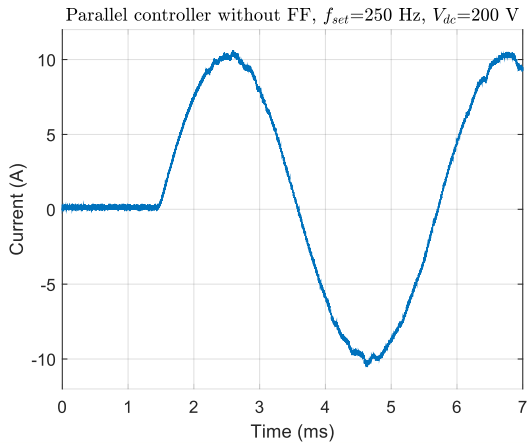


Figure 5.11: Large-signal measurement of the parallel controller structure, captured using the oscilloscope.

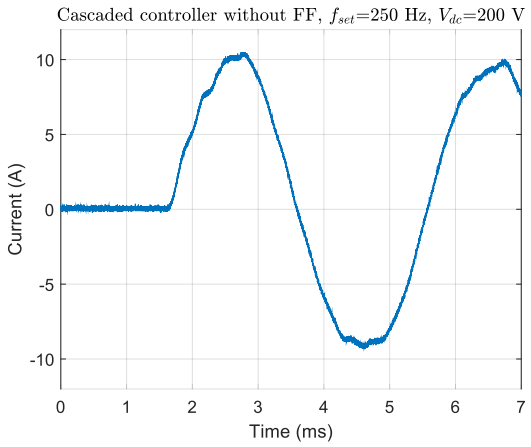
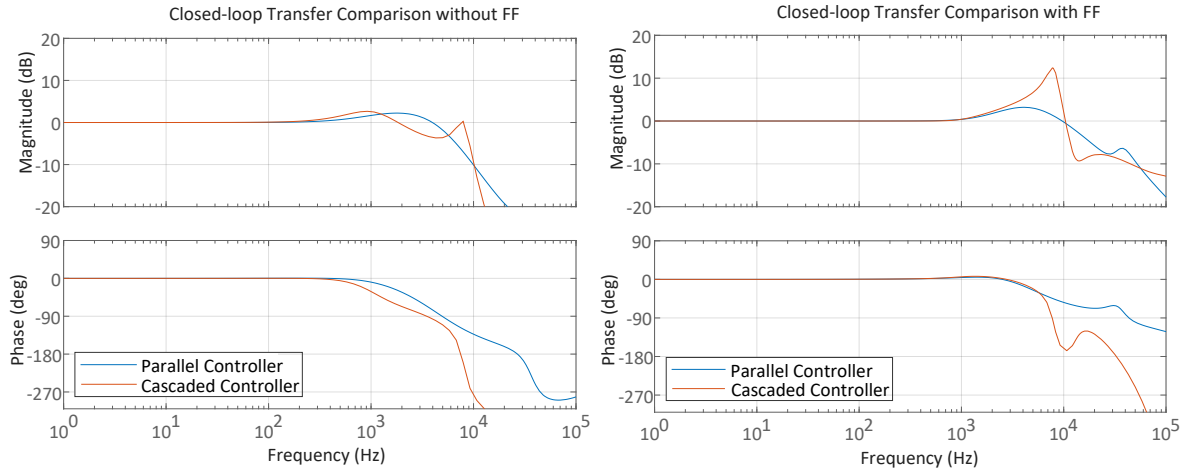


Figure 5.12: Large-signal measurement of the cascaded controller structure, captured using the oscilloscope.

used for a general comparison of the two structures. When looking at the comparison without FF, the results are as expected. Due to the higher bandwidth of the parallel controller structure, the response drops of at a higher frequency compared to the cascaded controller. The cascaded controller shows a resonance peak at high frequency due to the voltage controller. This limits the drop in magnitude response, but the phase still drops off sharply.
Looking at the comparison including FF, the frequency response of the two controller structures is more comparable for frequencies up to the bandwidth. The reason for this is explained in section 3.3. Poles for FF are more predictable for the cascaded controller than for the parallel controller. This makes it more suitable for complex FF. However, the resonance peak for the cascaded controller is much higher.



(a) Without FF

(b) With complex FF

Figure 5.13: A comparison of the analytical closed-loop frequency response of the parallel controller structure and the cascaded controller structure.

Stability
The bandwidth of the parallel controller structure has sufficient distance from the frequency of the resonance poles of the LC-filter on the frequency spectrum. This means a high GM is achieved for this controller, resulting in good stability. The stability of the damping loop in this structure depends on the controller delay. A larger delay could make the controller unstable.
On the other hand, in the cascaded controller structure, the three cascaded loops make stability margins thinner. The bandwidth of each loop needs to be close to the frequency of the poles of the inner loop to maintain

acceptable bandwidth. This results in the GM being much smaller compared to the GM of the parallel controller structure, resulting in less stability. Moreover, it was shown that decoupling could also easily cause stability issues and that additional margins needed to be incorporated for a practical implementation.

Sensitivity
Sensitivity indicates how well the controller reacts to disturbances. For the parallel controller structure, disturbances are only rejected by the tracking loop, and are limited by the bandwidth of this loop. In contrast, in the cascaded controller structure, disturbances present in the inductor current or capacitor voltage can be corrected by the inner loops. These loops are much faster than the output current loop and thus disturbance rejection will be faster. An example is a disturbance in the supply voltage, which will be corrected by the capacitor voltage loop. If the disturbance only occurs in the output current, as is the case for dynamic load variations, the disturbance will only be rejected by the outer tracking loop.

Ease of Tuning
For tuning the parallel controller structure, knowledge of the entire plant is needed, including the influence of the damping loop delay on the frequency response. On the other hand, in the cascaded controller structure, tuning the controllers is done separately for each controller, using only single component parameters, adjusting for bandwidth limitations of the previous loop. It can be concluded, that therefore the cascaded controller structure tuning is more intuitive.

Quantization noise
section 2.4 explained that for DS ADCs there is a trade-off between group delay and effective resolution. In the design of the controllers, suitable group delay was selected. The effect of these choices on effective resolution is seen as higher quantization noise at the output. The low group delay requirement of the controller results in lower effective measurement resolution, which translates into higher quantization noise at the output. What is derived from both measurements and simulation, is that the noise of the parallel controller structure is higher than that of the cascaded controller. This is because of the damping loop in the parallel controller. Strict group delay requirement resulted in high quantization noise added by this loop Table 5.2. However, because of the high frequency of this quantization noise section 2.4, it will have a marginal effect on performance in high-precision applications.

Modularity
To compare modularity, two aspects are important. First, how much communication is needed between two branches, and second, how many parameter changes are needed for the controller when the number of branches changes. The measurement communication requirement is equal for both controller structures. Only the output current measurement needs to be shared between the branches. Measurements for capacitor current and inductor current, for respectively the damping loop and the inner inductor current loop, can be taken in each branch individually. The same applies to the capacitor voltage measurement.
For changing controller parameters, the cascaded controller is a better candidate, since the outer loop tuning is based on load impedance only. This was a specific aspect of this controller structure where each component parameters is controlled separately. This is only valid if the voltage controller is controlling each branch capacitor current separately, as was explained in subsection 3.2.2. For the parallel controller, parameter data of the full plant is needed, which depends on the number of branches.

6

Conclusion and Outlook

This study has explored the design and implementation of two promising controller structures for modular interleaved high-precision current amplifiers used in lithography machines. A modular approach provides benefits in power density by matching amplifier specifications to actuator requirements and by enabling strategies to increase power efficiency. The first research objective was to evaluate and compare the performance of the parallel controller structure and the cascaded controller structure. The second objective was to introduce and implement DS ADCs as a cost-effective alternative for these amplifiers and explore their limitations. Finally, two ways to increase efficiency by making use of the interleaved PWM were explored, and possible implementation challenges were elaborated upon.

The design of each loop of the controller structures was provided in detail using analytical expressions. Two FF strategies were presented to increase closed-loop performance of both of the controller structures, of which complex FF gave superior results. Extra controller challenges arose from the group delay of the DS ADCs. In the parallel controller structure, limitations on the damping loop delay enable stable implementation with low decimation rates, which increase quantization noise. For the cascaded controller structure, limitations in the controller delay of the inner inductor loop directly causes output current bandwidth to be limited. A summary of the comparison of the controller structures is shown in Table 6.1. This summary can be used when selecting a suitable controller. If the highest possible bandwidth is desired, with high stability margins, the parallel controller structure should be chosen. On the other hand, if there is no high bandwidth requirement, and the focus is more on good sensitivity, modularity and quantization noise, the cascaded controller structure can be selected.

Table 6.1: Trade-off table to compare two controller structures.

Comparison	**Parallel Controller Structure**	**Cascaded Controller Structure**
Bandwidth	Higher possible bandwidth, limited by LC-filter	Lower possible bandwidth, limited by bandwidth of the inner controllers
Frequency Response	Good frequency response with and without FF	Complex FF provides relatively better improvements in frequency response
Stability	Better stability	Stability limited
Sensitivity	Disturbance rejection only by outer current loop	Disturbance rejection possible by faster inner loops
Ease of Tuning	Tuning depends on full plant model	Tuning depends on individual component values
Quantization Noise	Higher quantization noise because of fast damping loop	Lower quantization noise
Modularity	Worse for modularity	Better for modularity

The efficiency improvement techniques PS and ZVS were analyzed and simulated for the cascaded controller structure. By dynamically turning off and on branches, PS showed a significant reduction in power losses at lower current setpoints. ZVS improved efficiency at higher current setpoints by achieving soft switching

through dynamic adjustment of the switching frequency. Considerations for the control and output current were explored for both techniques and quantified. A choice for implementation can be made based on application-specific requirements.

Finally, a hardware demonstrator connected to a FPGA was used to validate the theoretical and simulation results. Firmware was created to efficiently implement and test the two different controller structures. For the cascaded controller structure, the implementation showed a problem with stability in the decoupling. This problem could be solved at the cost of bandwidth. Measurements of the frequency response were compared to the analytical expectations. A short summary is shown in Table 6.2.

Table 6.2: Summary of important results for a setpoint with a frequency of 400 Hz and with current magnitude 1 A.

	Parallel Controller structure		**Cascaded Controller Structure**	
	No FF	**Comlex FF**	**No FF**	**Complex FF**
Analytical	0.54 dB / -2.0°	0.06 dB / 0.5°	2.0 dB / -2.7°	0.004 dB / 1.6°
Simulation	0.66 dB / -3.1°	0.17 dB / 1.2°	1.1 dB / -9.6°	0.6 dB / 1.7°
Measurement	0.2 dB / -5.5°	-0.3 dB / -3.6°	-0.2 dB / -9.2°	-1.0 dB / -3.6°

6.1. Future Recommendations

The research objectives of this research are accomplished, but there are still a number of research topics left for future work. Some suggestions are outlined below:

- Throughout this research, effort has been put into providing a scalable approach, generalizing the analysis for an arbitrary number of branches. However, some challenges remain for a practical implementation. An example is how to deal with peaks and valleys of the PWM generator not taking place simultaneously for a higher number of branches. This leads to the challenge on how to deal with sampling and updating the setpoint in this case. The simulation and implementation should be extended to validate the operation with a higher number of branches.

- For this prototype, both branches were controlled by only a single FPGA. To increase modularity, it is preferred that each branch is controlled by its own FPGA. This work attempted to provide solutions to challenges that arise in the design of the controller for this situation. However, further research is needed for a practical implementation, for example how to synchronize the PWM, how to synchronize the sampling, and how to implement fast communication.

- Further investigation can be conducted on the use of DS ADCs. Sorensen [34] proposes a technique where the error to the proportional and integrator parts of a PI controller are provided by sinc filters with different decimation factors. Extending this analysis to the two proposed controller structures can improve bandwidth and stability performance. The analysis of DS ADCs can also be further extended by looking into more complex types of digital filters other than the sinc filter. These may provide different group delay to resolution trade-off at the expense of higher hardware implementation costs.

- Finally, the analysis of the methods to increase power efficiency can be extended. Combining both methods can result in even greater power efficiency improvements. For this, the analysis of practical limitations should be extended. Moreover, further research could be focused on implementing the strategies in a hardware demonstrator and validating the power loss estimates provided in this research.

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