# A 40.68-MHz Fully-Integrated Voltage/Current-Mode Dual-Output PMU for Wireless Neural Implants

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***Abstract*—This paper presents a fully-integrated single-input dual-output power management unit operating both in voltage/current modes for powering mm-scale wireless neural implants. The chip operates in voltage mode most of the time, using an active full-wave rectifier to regulate a low-voltage, high-load output with high power efficiency and low output ripple (<32 $\mathrm{mV_{pp}}$). It switches to current mode rectification when generating a high-voltage, low-load output. This dual-mode operation allows for flexible power distribution and configurable voltage ratios between the two outputs. The selected 40.68 MHz operating frequency reduces the required capacitances for input impedance matching and output filtering, enabling on-chip integration; the only external component is the receiver coil. A novel resonance breakup switch compatible with full-wave rectification ensures a smooth cold start-up of the chip without any external voltage supply. The chip was fabricated using 40-nm CMOS technology with an active area of 1.18 $\mathrm{mm^2}$ and was tested in a wireless power link. Measurement results demonstrate that the chip can simultaneously regulate two outputs, $V_{LV}$ = 1 V and $V_{HV}$ = 2 V, with a tested maximum output power of 10 mW and 32.6 µW on $V_{LV}$ and $V_{HV}$, respectively. At the optimal output power condition ($P_{LV}$ = 4.4∼6.7 mW), the system achieves a peak power conversion efficiency of 85.87% and a peak end-to-end efficiency of 17.32% when regulating $V_{LV}$. The end-to-end efficiency drops by only 2.38% when regulating both outputs with $R_{LV}$ = 225 Ω and $R_{HV}$ = 400 kΩ.**

***Index Terms*—Dual output rectifier, voltage mode, current mode, dual-mode, full-wave rectification, active rectifier, wireless power transfer, neural implants.**

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## I. Introduction

MODERN neuromodulation implants record neural signals for decoding brain activities and stimulate neurons for targeted and personalized treatments in a closed-loop fashion [1], [2], [3], [4], [5], [6], [7] - see Fig. 1. Three key blocks - recording, stimulation, and data telemetry/processing - are typically needed in such systems, each with different voltage/power requirements. As a result, such applications often require a power management unit (PMU) that can provide various output voltages—including a high-voltage supply ($V_{HV}$) and a low-voltage supply ($V_{LV}$)—from a single AC input while maintaining high power efficiency. $V_{HV}$ drives the stimulation circuit to allow sufficient voltage headroom, while $V_{LV}$ powers the recording, processing, and control circuits. In conventional neural implant systems, $V_{HV}$ experiences the highest load as stimulation is delivered continuously in an open-loop fashion [5], [8], [9], [10], [11]. Recent advances in on-chip neural signal processing, driven by the need to overcome data transmission bottlenecks, have enabled real-time closed-loop neural stimulation, drastically reducing the charge delivered to the tissue [12], [13], [14], [15], [16]. Furthermore, advances in electrode design, stimulation parameters optimization, and implantation techniques [17], [18], [19] reduced the required stimulation intensity to elicit a neural response. These improvements lead to a reduced load on $V_{HV}$, with power levels reported in the microwatt range in [20], [21]. Instead, the need for continuous multi-channel recording and on-chip signal processing to monitor brain activity results in a larger load on $V_{LV}$ [20], [21], [22], [23], [24], [25]. This marks a new trend in neuromodulation implants, where the PMU is required to provide both a high-power supply ($V_{LV}$) and a low-power supply ($V_{HV}$). Furthermore, because $V_{LV}$ is used in precision circuits such as analog front ends, it has stricter voltage ripple requirements than $V_{HV}$. Finally, since stimulation is not performed continuously, $V_{HV}$ does not need to be constantly regulated. Future wireless power transfer (WPT) systems for closed-loop neuromodulation should consider these requirements to exploit power and area efficiency.

Modern PMU structures have gradually evolved from cascaded power conversion stages [26], [27], [28], [29], [30], [31],

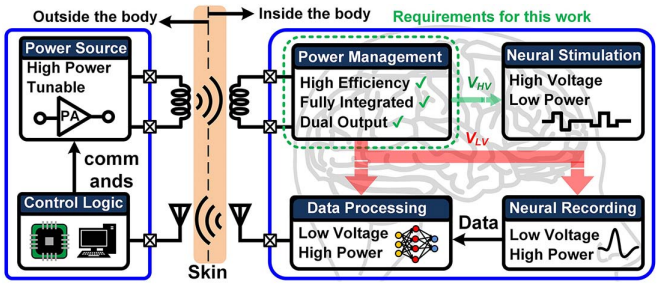



Fig. 1. The general structure of a wireless closed-loop neuromodulation implant.

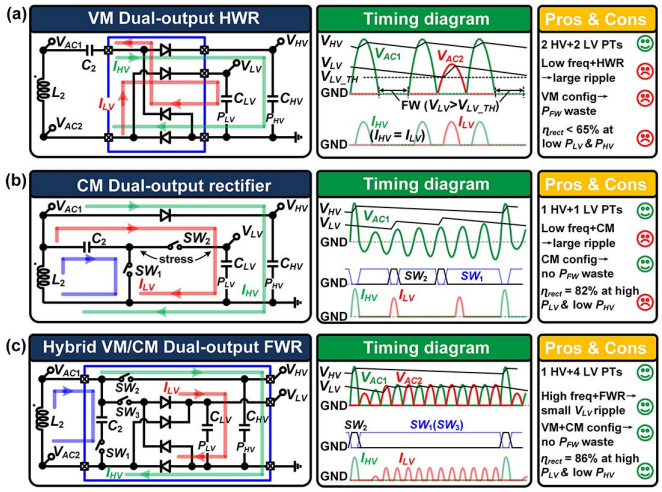



Fig. 2. Existing and proposed PMU topologies for dual-output applications with highlighted current flow paths: (a) Dual-output Half-Wave Rectifier (HWR) with VM charging [35], (b) Dual-output rectifier with CM charging [43], and (c) Proposed Full-Wave Rectifier (FWR) with dual VM/CM charging.

[32] and multi-tapped rectifiers [11], [33] to more compact and advanced topologies. In recent years, several dual-output voltage-mode (VM) rectifiers based on a single resonant *LC* tank have been proposed, operating in either half-wave or full-wave rectification modes [22], [34], [35], [36], [37], [38], [39], [40], [41], [42] (Fig. 2(a)). Dual-output regulation is achieved through time-interleaved switching of multiple power transistors connected to different loads. However, since the charging current for each output is identical, these structures are only efficient when the load currents at both outputs are comparable and when $V_{HV}$ draws the majority of power. In emerging neuromodulation implants, where $V_{LV}$ dominates overall power consumption, significant regulation losses appear at $V_{HV}$. For example, the tested power conversion efficiency (PCE) in [35] reduces by 8% when $V_{LV}$ dominates the power consumption and further decreases by 19% due to voltage regulation. In addition, the output voltage ratio of the VM rectifier is strongly dependent on the corresponding loads [35] and the switch controller accuracy [36], [42]. Particularly, [22] achieves an output voltage ratio of seven by employing series and parallel resonant configurations for each output; however, its efficiency is relatively lower compared to other works due to strict load requirements and passive rectification.

Current-mode rectifiers (CM) [23], [44], [45], [46], [47], or resonant current-mode rectifiers (RCM) [43], [48], [49], [50], [51], [52], are boost converter structures that can generate high voltage level outputs from an AC input signal resonating at a low amplitude, based on the principles of charge accumulation and charge transfer. These structures typically achieve a voltage gain exceeding two ($V_{HV}/|V_{AC1}| > 2$), as shown in Fig. 2(b), offering a promising solution to the efficiency bottlenecks of dual-output VM designs. However, dual-output generation using a CM charging scheme inherently introduces significant voltage ripple on both outputs, as it requires multiple resonant cycles before each subsequent charge transfer can commence. To address this issue, bulky off-chip filtering capacitors are required [23], [43], [44], [45], [46], [47], [48], [49], [50], [51], [52], which restricts implant miniaturization. Furthermore, the breakup switch $SW_1$, which plays an essential role in the *LC* tank loop, degrades the power transfer efficiency (PTE) of the link and complicates the startup procedure, as the switch control requires $V_{LV}$ or $V_{HV}$ before it becomes available. As a result, all prior works implementing CM operation achieve only half-wave rectification and suffer from power switch stress due to the negative swing of $V_{AC}$. This issue can be addressed by using thick-oxide devices, albeit at the cost of reduced PCE. In particular, [52] introduced a voltage doubler structure capable of full-wave rectification with zero negative swing, similar to its VM counterpart structure [40], [41]; however, it requires two identical off-chip capacitors (2 µF each), and fixes the output voltage ratio at two, restricting its applications.

To address the aforementioned new challenges in WPT for neuromodulation implants, this paper introduces a fully on-chip, single-input dual-output (SIDO) PMU with dual-mode powering (Fig. 2(c)). By incorporating two distinct operation modes, the proposed SIDO PMU can provide two supplies without compromising efficiency or voltage ripple: a low-level, low-ripple voltage ($V_{LV}$) with high output power, and a high-level high-ripple voltage ($V_{HV}$) with low output power. Unlike prior monolithic-mode designs, this work eliminates bulky passive components, achieving high power and area efficiency, low output ripple, and fully independent startup. To the best of the author's knowledge, this is the first work that fully exploits the advantages of a dual-mode charging strategy to realize all these features within a miniaturized implant system. As an intended application, a next-generation retinal prosthesis [53] has been investigated, as it demands two distinct voltage levels with load-driving capabilities ranging from the microwatt to milliwatt scale. The organization of this paper is as follows: Section II discusses the operation principle of the dual-mode PMU. Section III describes the detailed circuit implementation of the main components. Section IV presents the measurement results of the fabricated chip and a comparison with the state-of-the-art. Finally, conclusions are drawn in Section V.

## II. Operating Principle

The wireless link operates at 40.68 MHz to reduce the size of the on-chip resonance and filter capacitors, and to increase the

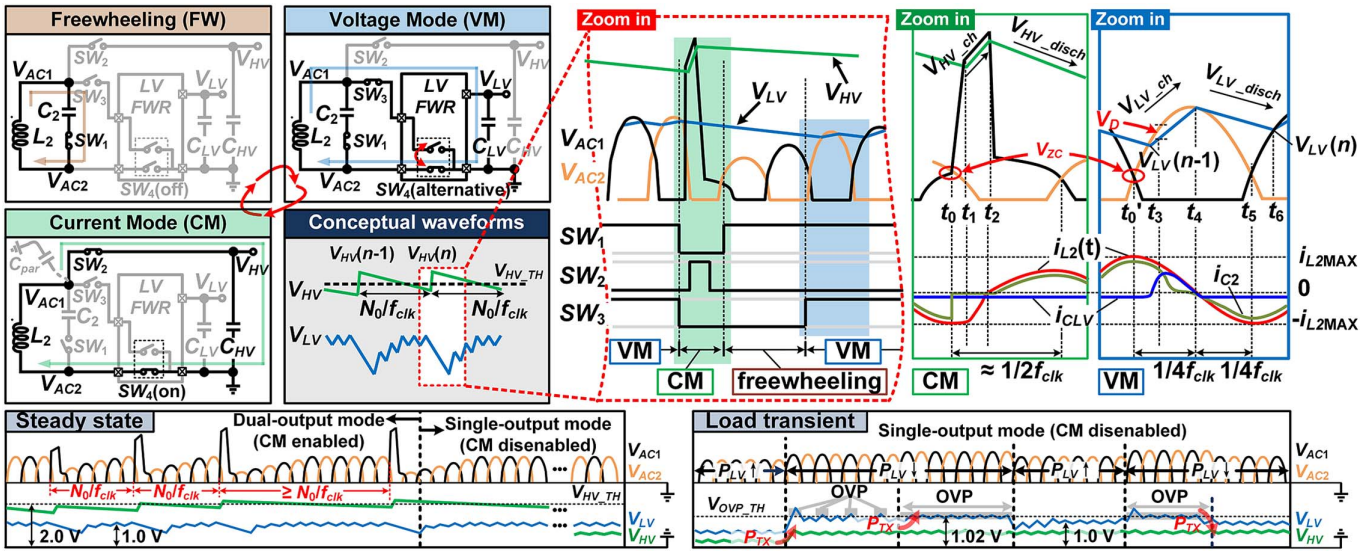



Fig. 3. Mode configurations and their conceptual transient waveforms.

Q-factor of the coils for better PTE. The receiver resonates at a low AC voltage ($V_{AC} \simeq V_{LV}$) to maximize power delivery in VM for $V_{LV}$; while the CM rectifier can boost the AC voltage to generate $V_{HV}$ when needed. Both VM and CM phases are realized using active switch control for higher PCE.

The proposed dual-mode PMU for dual-output WPT systems operates in three phases controlled by a mode-switching algorithm: the freewheeling phase, the VM charging phase, and the CM charging phase. The circuit configuration and their conceptual waveforms are shown on the left and right sides of Fig. 3, respectively. The following sections explain the operation of each phase and the mode-switching algorithm.

### A. Freewheeling Phase

The freewheeling (FW) phase builds up the resonance in the parallel-connected *LC* tank and accumulates energy within the loop (Fig. 3, the mode labeled 'FW'). During this phase, the switch $SW_1$ is closed while switches $SW_2$, $SW_3$ and $SW_4$ are open. Energy starts to accumulate within the *LC* resonator and $V_{AC}$ gradually increases. The FW phase is activated at startup and after the CM charging phase to ensure that VM charging is performed only when $V_{AC} > V_{LV}$. This condition may not always be satisfied without the FW phase, as an offset is introduced to $V_{LV}$ for delay compensation. Consequently, the FW phase avoids the potential reverse charging issue. Moreover, the FW phase incurs no power penalty, since the energy accumulated during this phase is fully transferred to the load in the subsequent VM phase.

### B. Current Mode Charging Phase

In the CM phase, the energy stored in the *LC* resonator is delivered to the $V_{HV}$ load (Fig. 3, the mode labeled 'CM'). $SW_1$ disconnects $C_2$ and $L_2$ to break the resonance; meanwhile, $SW_3$ is open to disconnect the VM rectifier, and $SW_2$ is closed to allow the $L_2$ current to flow into the $V_{HV}$ load and output capacitor $C_{HV}$. $SW_4$ remains closed, connecting $V_{AC2}$ to the ground and providing the current return path (the green line). When the resonance breakup switch opens, the $V_{AC1}$ node is boosted to a high voltage to charge $V_{HV}$. Although CM charging mitigates the need for a large AC voltage amplitude, it has a lower PCE than VM charging [44], [45].

The activation timing of the CM phase should be carefully chosen to maximize energy transfer to the $V_{HV}$ load, thus a sufficiently high $V_{HV}$ can be achieved. Consider an inductive coil link as in Fig. 4(a), where $V_S$ is a voltage source that can be modeled as $|V_S|\cos(wt)$ at the Tx side, $V_{12}$ and $V_{21}$ are the induced voltage at the transmitter (Tx) and the receiver (Rx) sides, respectively, $\omega$ is the angular frequency, $k_{12}$ is the coupling coefficient between $L_1$ and $L_2$, and $M_{12}$ is the mutual inductance, given by $M_{12} = k_{12}\sqrt{L_1 L_2}$. $R_{SW}$ represents the breakup switch resistance, while $R_1$ and $R_2$ are the equivalent series resistances of $L_1$ and $L_2$, respectively. The energy $E(t)$ stored in the $L_2C_2$ tank can be derived as:

$$E(t) = \frac{1}{2}L_2 I_{L2}^2(t) + \frac{1}{2}C_2 V_{C2}^2(t) \tag{1}$$

where $I_{L2}$ is the current flowing through $L_2$ and $V_{C2}$ is the voltage across $C_2$. According to Eq. (1), the maximum current $I_{L2}$ in the receiver coil can be found when $V_{C2} = V_{AC2} - V_{AC1}$ is zero. Breaking the resonance loop at this point yields the maximum $\Delta V_{HV}$.

It is important to quantify the voltage change $\Delta V_{HV}$ in each CM charging step. According to Kirchhoff's Voltage Law:

$$V_{21}(t) = L_2\frac{di_{L2(t)}}{dt} + \frac{1}{C_2}\int_0^t i_{L2}(t)dt + (R_2 + R_{SW})i_{L2}(t) \tag{2}$$

where $V_{21}(t)$ can be expressed as $|V_{21}|\sin(wt)$. In steady state, $V_{21}$ in the receiver side can be derived as [49]:

$$|V_{21}| = \left|\frac{j\omega V_S M_{12}}{R_1 + \frac{\omega^2 M_{12}^2}{R_2 + R_{SW}}}\right| = \frac{\omega |V_S| M_{12}}{R_1 + \frac{\omega^2 M_{12}^2}{R_2 + R_{SW}}} \tag{3}$$

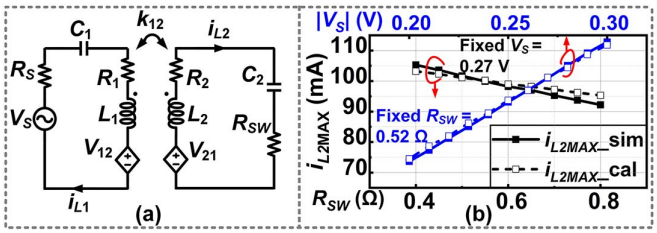



Fig. 4. (a) The equivalent model of a series-parallel Tx-Rx inductive link, (b) Comparison between the simulated and calculated result of $i_{L2\mathrm{MAX}}$ vs. $R_{SW}$ and $|V_S|$.

Given the initial conditions $i_{L2}(0) = 0$ and $\left.\frac{di_{L2}(t)}{dt}\right|_{t=0} = 0$ at startup, the solution of Eq. (2) leads to the complete form of $i_{L2}(t)$ and its maximum value $i_{L2\mathrm{MAX}}$ in steady state, as shown in Eq. (4) and Eq. (5), respectively:

$$i_{L2}(t) = \frac{|V_{21}|}{R_2 + R_{\mathrm{SW}}}\sin(\omega t) - e^{-\alpha t}\frac{\omega|V_{21}|}{\omega_d(R_2 + R_{SW})}\sin(\omega_d t) \tag{4}$$

$$i_{L2\mathrm{MAX}} = \frac{|V_{21}|}{R_2 + R_{\mathrm{SW}}} = \frac{\omega|V_s|M_{12}}{R_1(R_2 + R_{\mathrm{SW}}) + \omega^2 M_{12}^2} \tag{5}$$

where $\alpha = \frac{R_2 + R_{\mathrm{SW}}}{2L_2}$ represents the neper frequency and $\omega_d = 1/\sqrt{L_2 C_{\mathrm{par}}}$ is the undamped natural angular frequency. Fig. 4(b) compares the simulated and calculated results of $i_{L2\mathrm{MAX}}$, demonstrating a close agreement between them. Increasing the transmitter side voltage or reducing the breakup switch resistance can lead to a higher $i_{L2\mathrm{MAX}}$.

The derived expressions for $i_{L2}(t)$ and $i_{L2\mathrm{MAX}}$ can be further used to estimate the achievable $V_{HV}$ after $n$ cycles of CM operation. In the Appendix, we present the analytical derivation of the charging and discharging voltages, $V_{HV,\mathrm{ch}}(n)$ and $V_{HV,\mathrm{disch}}(n)$, respectively, as functions of $i_{L2}(t)$, $R_{HV}$, and $C_{HV}$. Based on these expressions, the cumulative result of $V_{HV}(n)$ can be calculated accordingly:

$$V_{HV}(n) = \sum_{i=0}^{n}\left(V_{HV\_ch}(i) - V_{HV\_disch}(i)\right) \tag{6}$$

### C. Voltage Mode Charging Phase

The VM phase starts once the resonating AC voltage amplitude reaches the desired voltage level of $V_{LV}$. Fig. 3 (the mode labeled 'VM') illustrates the simplified configuration for VM operation with full-wave rectification. Only the positive $V_{AC1}$ cycle is shown for simplicity. During this phase, the switch $SW_1$ is closed to enable energy accumulation in the *LC* resonator (similar to the FW phase). The switch $SW_2$ is open to disable the CM rectifier. The switch $SW_3$ closes to conduct current into the FWR. $SW_4$ represents the cross-coupled NMOS transistor within the FWR that grounds $V_{AC2}$ and provides the current return path (the blue line).

The VM charging phase performs high-efficiency charging from the *LC* resonator to the $V_{LV}$ load and output capacitor $C_{LV}$. It performs full-wave voltage rectification to reduce the output ripple approximately by half compared to conventional half-wave rectification used in dual output rectifiers [43], [44].

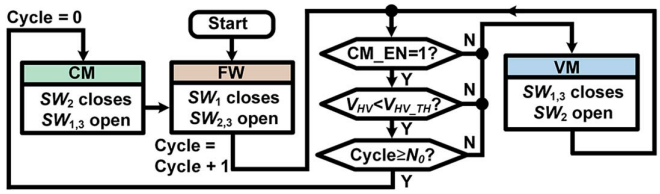



Fig. 5. The flowchart of the mode-switching algorithm.

Similar to Eq. (6), the achievable $V_{LV}$ after $n$ switching cycles in the VM can be recursively calculated based on the voltage expressions derived in the Appendix:

$$V_{LV}(n) = \sum_{i=0}^{n}\left(V_{LV\_ch}(i) - V_{LV\_disch}(i)\right) \tag{7}$$

Eq. (6) and Eq. (7) can be used to determine the optimal time interval for the transition between the VM and CM phases, as further discussed in the following section.

The regulation mechanism for $V_{LV}$ is depicted in Fig. 3 (labeled 'load transient'). Unlike $V_{HV}$, which employs a self-adaptive charging scheme, $V_{LV}$ is regulated by an over-voltage protection (OVP) circuit with a trigger voltage near 1.0 V. Under light load, excess power is dissipated by the OVP, while under heavy load, the DC voltage level is maintained, ensuring robust operation across dynamic load conditions.

### D. Mode-Switching Algorithm

Fig. 5 illustrates the mode-switching algorithm implemented by the control logic on chip. The algorithm starts from the FW mode to build up the AC signal swing and store energy within the *LC* resonator. Once the amplitude of the AC signal reaches the target level of $V_{LV}$, the system transitions to VM. To enable dual-output rectification, the transition from VM to CM is required. Three conditions must be satisfied for the system to switch from VM to CM: (i) the CM control flag CM_EN is active. If CM_EN = 0, the system works as a single output rectifier to generate only $V_{LV}$, (ii) $V_{HV}$ is below the regulation threshold $V_{HV\_TH}$, and (iii) there have been sufficient cycles ($N_0$) since the last CM charging operation, ensuring adequate time for the AC signal swing to rebuild and preventing consecutive CM charging operations that could disrupt $V_{LV}$ regulation.

If all three conditions are satisfied, the system performs CM charging for one cycle before switching to FW mode to build up the resonance again. Notably, an optimal $N_0$ exists that is constrained by both a lower and an upper limit.

The lower limit for $N_0$ is decided by the acceptable PCE degradation in VM for the high-load output $V_{LV}$ - see Fig. 6(a). If $N_0$ is too small, then the system does not spend sufficient time in VM charging the high output load $V_{LV}$. To evaluate the power degradation of the proposed dual-mode charging scheme under different $N_0$, the corresponding PCE is formulated in Eq. (8):

$$\mathrm{PCE} = \frac{P_{LV}}{P_{LV} + P_{Loss,total}} \tag{8}$$

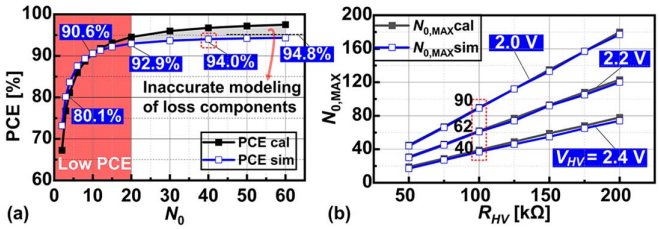



Fig. 6. The comparison between the calculation and behavioral simulation results of (a) PCE versus $N_0$, and (b) $N_{0,\mathrm{MAX}}$ versus $R_{HV}$ with achievable $V_{HV}$ from 2.0 V to 2.4 V.

$$P_{LV} = \left[\frac{1}{n+1}\sum_{m=0}^{n=\infty}\left(V_{LV}(0) + \sum_{i=1}^{m}\Delta V_{LV}(i)\right)\right]^2 / R_{LV} \tag{9}$$

where $P_{LV}$ is the output power, $\Delta V_{LV}(i)$ is the voltage accumulation on $V_{LV}$ at step $i$ based on Eq. (7), and $P_{Loss,total}$ is the power loss as derived in [54]. Notably, ensuring $N_0 > 20$ limits the PCE degradation to less than 2.0%.

The upper limit for $N_0$ is decided by the desired output voltage $V_{HV}$ for a given load $R_{HV}$. When $N_0$ is too large, the CM charging ($V_{HV\_ch}$) may not fully compensate for the discharging in between CM cycles ($V_{HV\_disch}$). For a given output level and load, there exists a maximum $N_{0,max}$ that can sustain proper CM operation - see Fig. 6(b)). For our target specifications ($V_{HV} = 2$V and $R_{HV} = 100$kΩ), the calculated theoretical $N_{0,\mathrm{MAX}} = 90$. However, considering the potential losses due to imperfect switching timing and power leakage, selecting $N_0 = 40$ provides a sufficient margin.

Considering both lower and upper limits, this work uses $N_0 = 40$. Notably, this number significantly exceeds those previously reported in CM-based schemes [43], [50], mainly because the majority of power is delivered to the $V_{LV}$ output in the high-efficiency VM charging phase. The conceptual waveform showing the mode switching and $V_{HV}$ regulation is depicted in Fig. 3 (labeled 'steady state'). The CM rectification starts at the zero-crossing point. A high voltage is induced on $V_{AC1}$, and current flows into the $V_{HV}$ load capacitor $C_{HV}$. During the CM rectification and the subsequent FW mode, $V_{LV}$ is not being charged, which leads to a larger ripple and reduced power efficiency in VM. However, the system operates in the high-efficiency VM to drive the heavy load on $V_{LV}$ most of the time. Hence, the overall efficiency in VM is not affected significantly. For example, with $V_{HV}$ connected to a 225kΩ load, the end-to-end efficiency in VM charging only drops by 2.38% in this work (detailed in Section IV).

## III. Hardware Implementation

Fig. 7 illustrates the proposed VM/CM PMU system architecture that regulates a 40.68 MHz inductive wireless link to generate dual outputs. The chip simultaneously achieves rectification, regulation, bias generation, and overvoltage protection using only the Rx coil as an external component. The 240 pF resonance capacitor $C_2$ (consisting of 80 pF $C_{2a}$, 80 pF $C_{2b}$, and 80 pF parasitic capacitance seen from node connections), the 250 pF filtering capacitor $C_{HV}$ and the 2 nF $V_{LV}$ filtering capacitor $C_{LV}$ are integrated on-chip. $C_{LV}$ and $C_{HV}$ use a stacked structure with a metal-on-metal (MOM) capacitor on top of a thick-oxide low-leakage varactor (2.5 V voltage rating) to achieve high capacitance density and low power leakage, while $C_2$ uses a MOM capacitor to ensure minimal variation and low resistance. The PMU comprises three main blocks: the VM rectifier, the resonance breakup switch, and the CM rectifier with the control logic.

### A. VM Rectifier

The VM rectifier uses active PMOS diodes ($M_{1,2}$) with a cross-coupled NMOS pair structure ($M_{3,4}$). The active diodes are controlled by a common-gate comparator and a gate driver, both optimally sized to minimize switching losses. The rectifier uses thin-oxide devices to minimize power losses.

*High-Voltage Protection Switch:* $SW_3$ (Fig. 8(a)) protects the rectifier core devices during CM by turning off before $V_{AC1}$ exceeds 1.25 V (40-nm CMOS limit), and remains ON during VM. To fully turn off $SW_3$ during CM, the switch buffer (Fig. 8(b)) supplies $V_{AC1}$ and ground to the PMOS and NMOS gates, respectively. Conversely, to turn on $SW_3$ during the VM phase, the switch buffer supplies ground and $V_{LV}$ voltage rails to the transmission gate. $V_{HV}$ is not used as the supply since CM operation is not always enabled. $SW_3$ is upsized to reduce conduction loss during VM charging (PCE decreases by 1.2% when assuming 0.5Ω resistance), at the cost of notable parasitic capacitance at $V_{AC1b}$. As a result, the delayed switching of pull-down transistor $M_4$, increases switching loss due to the negative swing at $V_{AC2}$. To mitigate this, a dummy capacitor, $C_{d1} = 24$ pF is placed at $V_{AC2}$. This solution effectively compensates for asymmetrical loading of $V_{AC1b}$ and $V_{AC2}$, offering area advantages over a dummy switch and has a negligible impact on matching. Simulation results show a 2.27% improvement in rectifier PCE at the $R_{LV}$ load of 200 Ω, without degrading link PTE.

*Common Gate Comparator:* The common-gate (CG) comparator used in this work (Fig. 8(c)) can accommodate a high input common-mode voltage and has a low static power consumption [55]. It operates in the VM comparison when the FW control signal ($V_{FW}$) is not enabled. To compensate for the turn-on delay, this design uses comparator offset compensation [54], [56]. The offset is introduced through a programmable mismatch in the current mirror $M_6$ and $M_8$ to accommodate process variations, and functions well in the steady state when $V_{LV} > V_{th,M5} + V_{th,M6}$ (strong inversion). However, the generated offset is dependent on the working region and varies with $V_{LV}$ during startup, reducing the effective power transferred to the load. Apart from the late turn-on problem, this technique also has a reverse current problem during startup [54], [57]. Although the fixed delay problem can be solved using a voltage-controlled delay cell with a feedback loop design, it cannot properly compensate the turn-on delay during startup [57], which increases startup power and may risk device breakdown [39]. To prevent the AC voltage from exceeding safety limits during startup, an auxiliary coupling voltage $V_{os}$

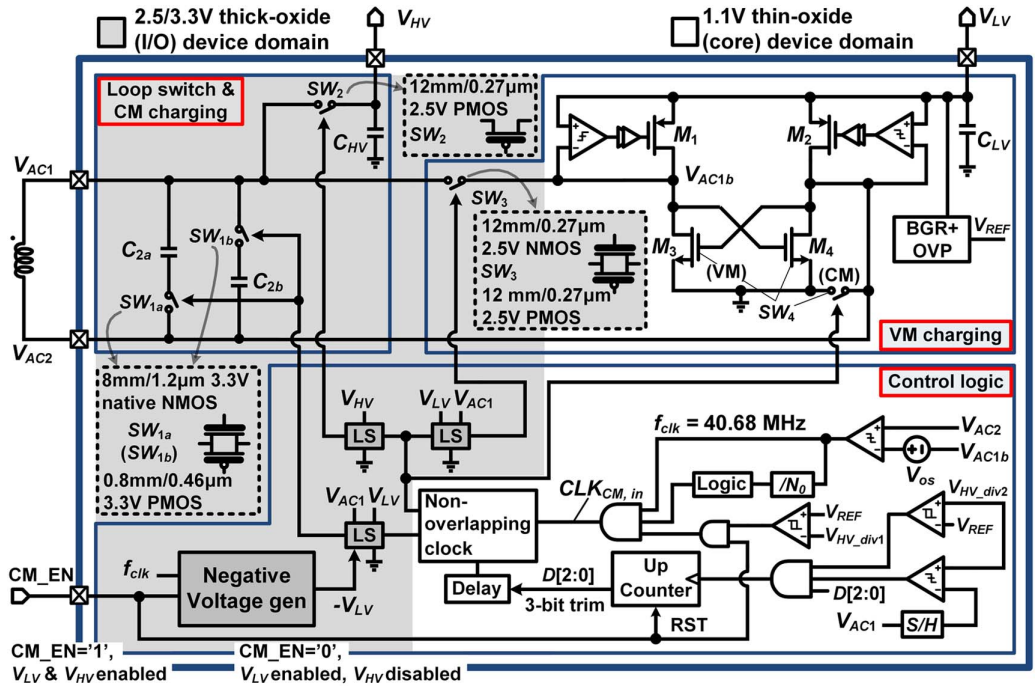
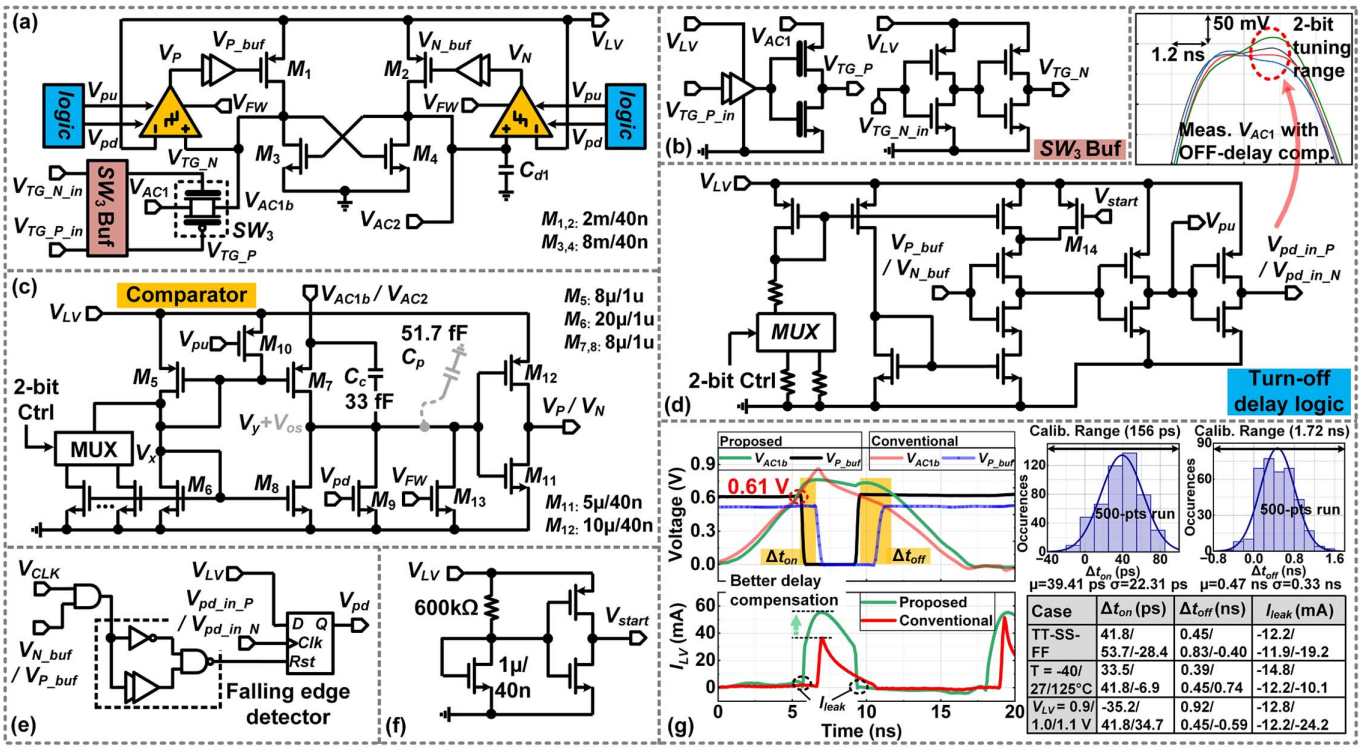



Fig. 7. The overall structure of the proposed design.




| Case | $\Delta t_{on}$ (ps) | $\Delta t_{off}$ (ns) | $I_{leak}$ (mA) |
|---|---|---|---|
| TT-SS-FF | 41.8/ 53.7/-28.4 | 0.45/ 0.83/-0.40 | -12.2/ -11.9/-19.2 |
| T = -40/ 27/125°C | 33.5/ 41.8/-6.9 | 0.39/ 0.45/0.74 | -14.8/ -12.2/-10.1 |
| $V_{LV}$= 0.9/ 1.0/1.1 V | -35.2/ 41.8/34.7 | 0.92/ 0.45/-0.59 | -12.8/ -12.2/-24.2 |

Fig. 8. The circuit implementation of (a) active voltage rectifier, (b) driving circuits for the high-voltage protection switch, (c) common gate comparator, (d) pulse duration time control circuit, (e) digital logic to prevent multiple-pulsing, (f) startup auxiliary circuit, and (g) the simulated waveform of the turn-on delay compensation using the conventional mismatch-based scheme ($M_6$ size = 100/1 µm for a fair comparison) and proposed coupling capacitor-based scheme. The robustness of the proposed scheme is verified through a 500-point Monte Carlo simulation and PVT analysis.

at $V_y$ is introduced by a coupling capacitor $C_c$. The capacitive divider between $C_c$ (33 fF) and the total parasitic capacitance $C_p$ (51.7 fF) at the node $V_y$ sets the value of $V_{os}$ as a function of $V_{AC}$. It can operate at $V_{LV}$ as low as 0.61 V. Consequently, the proposed design accelerates startup by reducing reverse current at low $V_{LV}$ (Fig. 8(g)). In this work, the $C_c$-induced

coupling voltage compensates for 0.2 ns delay (typical value), while the input pair programmable offset (2 bits) compensates for up to 0.25 ns (typical value). Monte Carlo and corner simulations show robustness of this method across PVT variations (Fig. 8(g)).

The comparator's turn-off delay leads to reverse current loss. This design uses a current-starved delay cell (Fig. 8(d)) to create a delayed signal ($V_{pd}$) of the turn-on signal ($V_{P\_buf}$) to switch off the power transistor ($M_{1,2}$) in the rectifier at the right time. $V_{pd}$ pulls $V_y$ in the comparator to ground through $M_9$, while $V_{pu}$ pulls $V_x$ to $V_{LV}$ through $M_{10}$, causing the comparator to generate a high signal and switch off $M_{1,2}$. The delay time can be manually controlled by a 2-bit resistor array that adjusts the bias current of the delay cell, as verified by the measurement $V_{AC1}$ waveform (shown above Fig. 8(d)). To prevent the multiple pulsing issue [58] which increases switching losses, this design uses digital logic as shown in Fig. 8(e) to latch the $V_{pd}$ signal until the next comparison cycle starts. To prevent excessive power demand during startup, an auxiliary circuit (Fig. 8(f) [59]) is designed to shorten the startup delay by providing additional current to the delay cell through $M_{14}$ (Fig. 8(d)). When $V_{LV}$ reaches its stable state, $V_{start}$ transitions from low to high, disabling the current path.

### B. Resonance Breakup Switch

The resonance breakup switch ($SW_1$) is an essential part of this design that affects both the CM and VM operation. When $SW_1$ is OFF during CM operation, it should completely block the conduction path within the $LC$ tank to maximize $\Delta V_{HV}$. When $SW_1$ is ON during VM operation, it should have a small equivalent resistance to reduce the losses in the link. For example, assuming an on-resistance of 0.5 Ω, $SW_1$ degrades the PTE by 2.2%.

A transmission-gate structure is used to allow full-wave rectification in VM. A thick-oxide native (normally-on) NMOS device enables self-startup when $V_{LV}$ has not yet reached its stable value. A negative supply voltage $-V_{LV}$ (Section III-D3) is used to turn the native NMOS switch OFF during CM. The thick-oxide PMOS switch is driven between ground (ON in VM) and $V_{AC1}$ (OFF in CM), similarly to the one in $SW_3$.

Fig. 9(a) shows the circuit implementation of the resonance breakup switch ($SW_1$) during VM in conventional structures with an FWR. This structure suffers from a significant increase in ON resistance during the $\Phi_2$ phase, when $V_{AC2} > V_{AC1}$. In the $\Phi_1$ phase, where $V_{AC2} = 0$, $R_{eq}$ is only $0.52\Omega$ due to a fixed $V_{GS}$ applied to the NMOS switch. However, when $V_{AC2} > 0$, $R_{eq}$ increases due to the reduced gate drive voltage, especially during $V_{AC2} < V_{th,P}$. As a result, rather than charging the intended resonant capacitor $C_2$ through the high-impedance path, the inductor current is diverted to an unintended low impedance path formed by the parasitic capacitance and the rectifier power transistor ($M_3$ in Fig. 8(a)), which increases switching losses and degrades PCE.

To reduce $R_{eq}$ to an acceptable value based on simulation results, it would require a PMOS switch ∼20 times larger. Instead, this work addresses this problem by splitting the switch-capacitor pair into two anti-parallel structures - Fig. 9(b). When

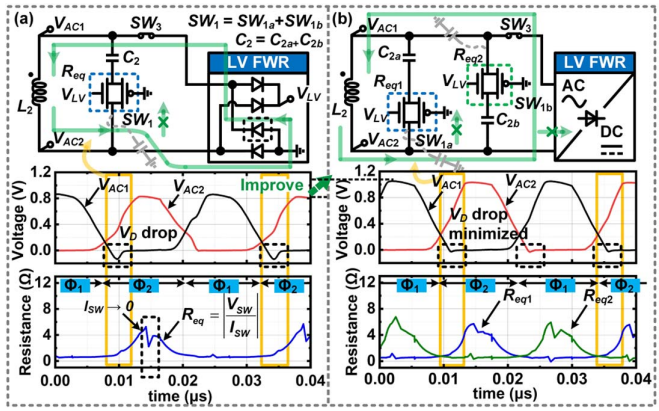



Fig. 9. The VM configuration of the resonance breakup switch and its equivalent resistance in (a) the conventional half-wave and (b) proposed full-wave scheme. The size of $SW_1$ in (a) is double that of $SW_{1a}/SW_{1b}$ for a fair comparison.

$V_{AC2}$ increases, the equivalent resistance ($R_{eq,a}$) of $SW_{1a}$ increases as before, while $R_{eq,b}$ of $SW_{1b}$ remains small. Hence, in this phase, the majority of the current flows through $SW_{1b}$. Vice versa, when $V_{AC1}$ increases, current flows through $SW_{1a}$. This way, the overall ON resistance is low over the full cycle, leading to lower power losses in the breakup switch. In addition, the negative voltage swing in $V_{AC1}$ is eliminated, which mitigates the switching losses in the NMOS power transistor pair and further improves the rectifier PCE by 5.7% under the nominal load condition of 200Ω. The proposed topology avoids the need for complex bias schemes or excessive use of transistors and capacitors [52].

### C. CM Rectifier

The CM rectifier in Fig. 10(a) uses an active diode ($SW_2$) with a dynamic body bias to prevent leakage current to the substrate [60]. The active structure minimizes the voltage drop across the diode to maximize efficiency, as shown in Fig. 10(b). During CM, the resonance-breakup switches $SW_{1a}/SW_{1b}$ and the protection switch $SW_3$ are open. The pull-down switch $SW_4$ connects $V_{AC2}$ to ground to provide current return path. A negative voltage $-V_{LV}$ is applied to the native NMOS transistors in $SW_{1a}/SW_{1b}$. $V_{AC1}$ directly drives the PMOS transistors in $SW_{1a}/SW_{1b}$ and $SW_3$, while the NMOS transistor in $SW_3$ can be grounded.

As mentioned above, this work focuses on applications where most of the power is required for $V_{LV}$, while $V_{HV}$ has a light load. Hence, the resonance breakup switches $SW_{1a}/SW_{1b}$ and the protection switch $SW_3$ are optimized to reduce conduction losses during VM. The drawback is that they contribute a large parasitic capacitance to the $V_{AC1}$ node. If passive charging with a diode voltage drop (∼0.7 V) is adopted [43], [45], [46], [50], [61], most of the current in the inductor is used to charge the parasitic capacitance at node $V_{AC1}$, and $V_{HV}$ cannot be properly regulated to the expected high voltage. This can be a significant bottleneck, especially in low-power, high-frequency applications, because both the available power and the charging

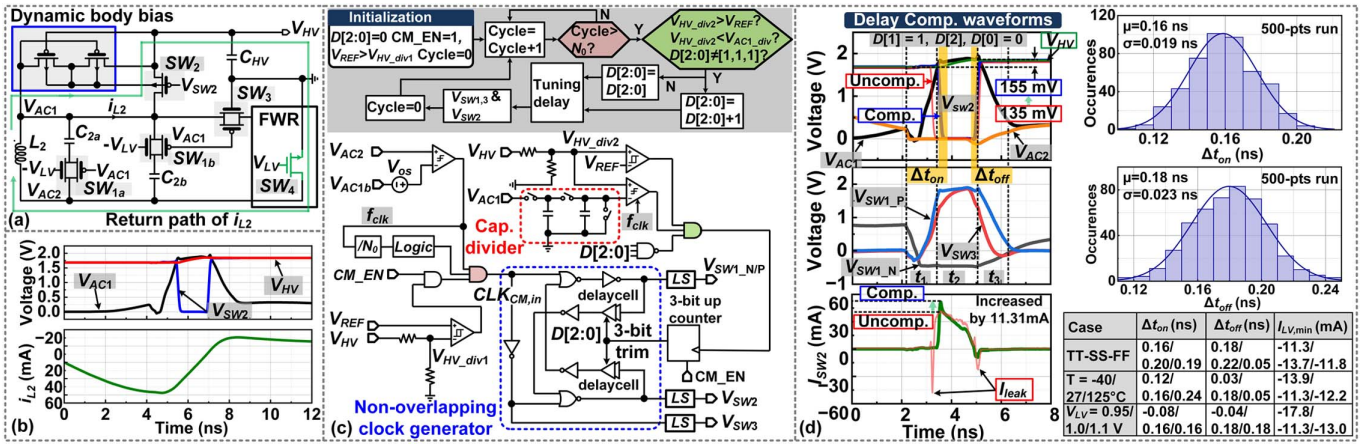



Fig. 10. (a) The circuit implementation of the CM charging rectifier, (b) Simulated charging waveforms, (c) the operation flowchart and the circuit implementation of the non-overlapping clock generator, and (d) simulated CM charging waveform with uncompensated/compensated non-overlapping clock signals. The robustness of the proposed scheme is verified through a 500-point Monte Carlo simulation and PVT analysis.

time are insufficient for conducting the CM charging. To overcome this passive mode charging limitation, this work proposes an active charging structure to reduce the voltage drop between $V_{AC1}$ and $V_{HV}$.

The following requirements have to be satisfied: (i) $SW_3$ needs to open before the CM phase starts to protect the core devices in the VM rectifier, (ii) $SW_1$ needs to open when $V_{AC1} = V_{AC2}$ to maximize the current coming from the inductor, and (iii) $SW_2$ needs to close when $V_{AC1} \geq V_{HV}$ to start charging the output capacitor $C_{HV}$. Similarly to the VM rectifier, the early switch-ON or the late switch-OFF of $SW_2$ when $V_{AC1} < V_{HV}$ can introduce a reverse current from $V_{HV}$ to $V_{AC1}$. Also, the late switch-ON or the early switch-OFF of $SW_2$ when $V_{AC1} > V_{HV}$ ($SW_1$ in OFF state) can generate large spikes on $V_{AC1}$ [36] and cause stress problems since there is no low-impedance path for the inductor current.

To address these issues, the CM control logic uses a non-overlapping clock with adaptive delay. The operation principle is illustrated in the flowchart in Fig. 10(c). Initially, a comparator recovers the system clock in phase with the zero crossing point (ZCP). This clock is sent to the digital control unit along with the CM_EN signal and the output of the $N_0$ counter (Section II-D) to generate the enable signal for the CM charging periodically ($CLK_{CM,in}$). The comparator is offset compensated to minimize its delay and maximize the inductor current when the *LC* tank is opened (details in Section III-D2).

First, $CLK_{CM,in}$ derives the overlapping clock signal to open the protection switch $SW_3$ before $SW_1$ opens. $SW_2$ is closed only when $SW_1$ (and $SW_3$) are open. The required non-overlapping time demands dynamic adjustment, as it increases proportionally with $V_{HV}$. This is realized using a programmable delay line controlled by a 3-bit counter. At every CM charging cycle, $V_{AC1}$ is sampled when $SW_2$ closes and compared with $V_{HV}$. If $V_{AC1} < V_{HV}$, the non-overlapping time is increased by incrementing the counter output bits. If $V_{AC1} > V_{HV}$, the counter is not updated. Fig. 10(d) shows the delay compensation for the control signal of $SW_2$. When $V_{SW2}$ turns on before $V_{AC1} > V_{HV}$, the counter continues to increase until the cross-point reaches its optimal timing. Monte Carlo and corner simulations confirm that the proposed CM delay compensation scheme can effectively suppress reverse current under PVT variations (Fig. 10(d)).

### D. Auxiliary Circuits

*1) Bandgap Reference and Overvoltage Protection:* A low-voltage bandgap reference circuit [62] generates the 0.55V reference voltage ($V_{REF}$) for the control logic and the OVP circuit (Fig. 11(a)). The OVP circuit ensures that $V_{LV}$ remains within the safe operating range and also enables voltage regulation. When $V_{LV}$ exceeds the 1.02V threshold voltage (decided by $V_{REF}$, the resistive divider, and the hysteresis window), the output of the hysteresis comparator $V_{\mathrm{OVP}}$ goes high. As a result, the NMOS transistor ($M_1$) conducts and discharges $V_{LV}$ through a 100Ω resistor ($R_1$) connected to the ground. This local voltage regulation can regulate $V_{LV}$ across a wide range of Tx power (31.6 mW to 63.1 mW when $R_{LV} = 200\Omega$, and 50.1 mW to 112.2 mW when $R_{LV} = 100\Omega$). By implementing a global power control scheme through backward data telemetry [63], [64], the $V_{\mathrm{OVP}}$ can also be used to regulate the Tx power ($P_{TX}$) level. In this configuration, the OVP circuit can protect $V_{LV}$ against high Tx power up to approximately 158.5 mW.

*2) Clock recovery and Zero-Crossing Detection:* The 40.68 MHz system clock is recovered from the AC signals using a comparator. However, the conventional latch-based comparator [65] suffers from a significant comparison delay, leading to losses during CM charging as explained in Section II-B. This work uses a delay-compensated comparator (Fig. 11(b)) [66] to achieve clock recovery and zero-crossing detection. The unbalanced sizing in the PMOS input pair ($M_{1,2}$) introduces an offset voltage $V_{os}$ ($V_{AC1b} + V_{os} = V_{AC2}$) of approximately 250 mV to account for the delay between the cross point of the AC signals and the rising edge of the comparator output ($f_{clk}$), resulting in a 25% increase in inductor current during the CM operation. Additionally, the $M_3$ transistor, sized identically

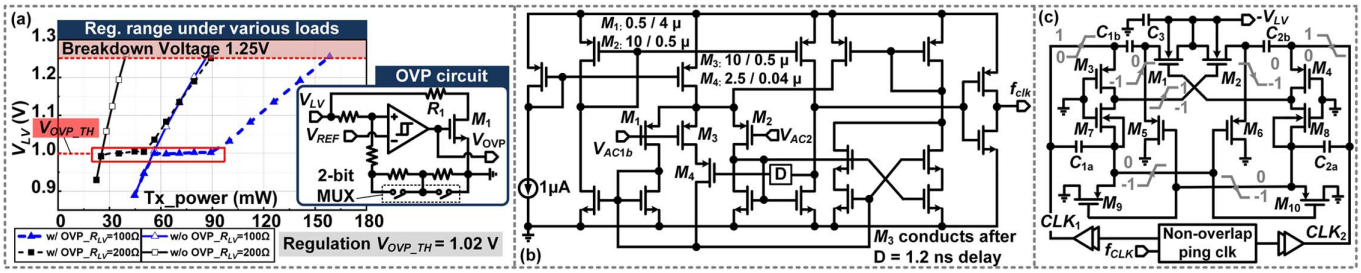



Fig. 11. (a) The circuit implementation of the OVP and the simulated $V_{LV}$ w/ and w/o OVP versus different Tx powers, (b) Comparator with a mismatched input pair, and (c) Negative voltage generator.

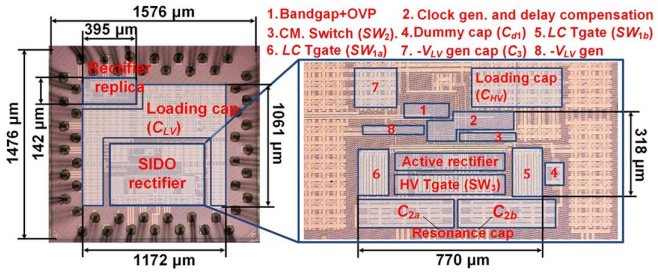
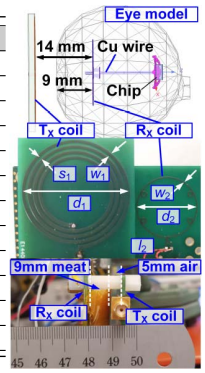



Fig. 12. Die photograph of the 40-nm CMOS PMU chip.

TABLE I
THE POWER COIL PARAMETERS USED FOR THE WPT SYSTEM

| Item | Tx($L_1$) | Rx($L_2$) |
|---|---|---|
| Outer diameter $d$ [mm] | 26.8 | 16 |
| # of turns | 4 | 1 |
| Trace width $w$ [mm] | 0.8 | 0.25 |
| Trace spacing $s$ [mm] | 0.6 | - |
| 28-AWG Cu wire $l_2$ [mm] | - | 8 |
| Inductance [nH] | 595.41 | 74.06 |
| Quality factor | 186.82 | 24.76 |
| Frequency [MHz] | 40.68 | |
| Cu trace thickness | 35 µm | |
| Substrate thickness | 1.57 mm Fr4 | |
| Distance [mm] | 14 (air+tissue) | |
| Coupling coefficient $k_{12}$ | 0.0523 | |




to $M_2$, is placed alongside $M_1$ to generate the falling edge of $f_{clk}$, thereby maintaining the duty cycle of the 40.68 MHz clock close to 50%.

*3) Negative Voltage Generator:* A negative supply ($-V_{LV}$) is required to strongly turn OFF the native NMOS transistor used in resonance breakup switches $SW_{1a}/SW_{1b}$ during CM operation. This supply is provided by the negative voltage generator illustrated in Fig. 11(c), which consists of two charge pumps (formed by $M_3 \sim M_{10}$ and $C_{1a} \sim C_{2b}$) working in time-interleaved mode and two output switches ($M_1$ and $M_2$). The charge pumps are controlled by the non-overlapping 40.68 MHz clock outputs $CLK_1$ and $CLK_2$, to continuously charge the output capacitor $C_3$ through the output switches. The nominal output voltage when CM is activated is -0.5 V.

## IV. EXPERIMENTAL RESULTS

The proposed dual-output PMU was implemented using standard 40-nm CMOS technology. The chip micrograph (Fig. 12) shows that the design occupies a core area (active circuit area, w/o test I/O pads) of 1.18 $\mathrm{mm}^2$, and a total area of 2.28 $\mathrm{mm}^2$. A replica rectifier circuit (not included in the core area) without the on-chip resonance capacitor is also integrated to measure the rectifier input power for PCE.

The measurements of the PMU chip use a custom-designed coil link, following the design methodology introduced in [67]. The Tx/Rx coils are separated by 14 mm, a typical separation distance for retinal prostheses applications. The coil dimensions are optimized to meet the strict surgical constraints, and its parameters have been characterized using a vector network analyzer (Keysight P9374A) - details in Table I. The Tx *LC* resonator is matched to the 50Ω impedance of an RF power source (Agilent N5183B MXG), and the Tx power is adjusted to regulate $V_{LV} = 1$ V according to the load $R_{LV}$.

### A. Cold Startup Measurement

Fig. 13 presents the measured cold start-up waveforms of the Rx chip under a 250Ω load at $V_{LV}$ with a transmitter power of 13.6 dBm (22.91 mW). The rectifier initially operates in a passive-mode configuration, formed by the transistors $M_1(M_2)$, with uncertain gate voltage, and the body diode of $M_4(M_3)$. As $V_{LV}$ increases, the uncompensated comparator begins to generate digital control signals to drive $M_1(M_2)$. After approximately 0.4ms of passive rectification, $V_{LV}$ reaches 0.6 V, activating the OVP while $V_{REF}$ gradually increases. The OVP phase lasts for 0.88 ms until $V_{REF}$ exceeds 0.3 V, and the chip starts operating normally to regulate $V_{LV}$.

### B. Voltage-Mode (Single) Output Measurement

Fig. 14(a) shows the setup for measuring the voltage conversion ratio (VCR) in the VM rectifier and presents the AC-in and DC-out waveforms during VM operation. The phase differences between different channels on the oscilloscope have been calibrated to ensure accuracy. With a 250Ω load at $V_{LV}$, the measured mean value of $V_{LV}$ is 0.99 V, with a ripple of 31.67 mVpp. The peak-to-peak amplitude of $V_{AC}$ is 2.11 V, yielding a VCR of 93.84%.

Since this design incorporates an on-chip resonant capacitor ($C_2$), a replica circuit without the integrated resonant capacitor

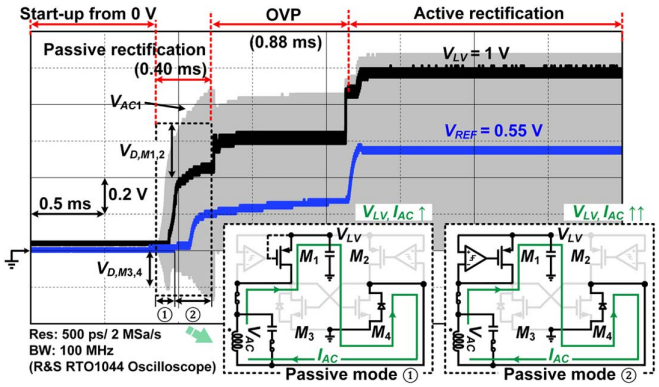



Fig. 13. Measured cold start-up procedure at $R_{LV} = 250\ \Omega$ and $P_{TX} = 22.91$ mW. The passive mode configuration at one of the conduction phases is shown in the lower right corner.

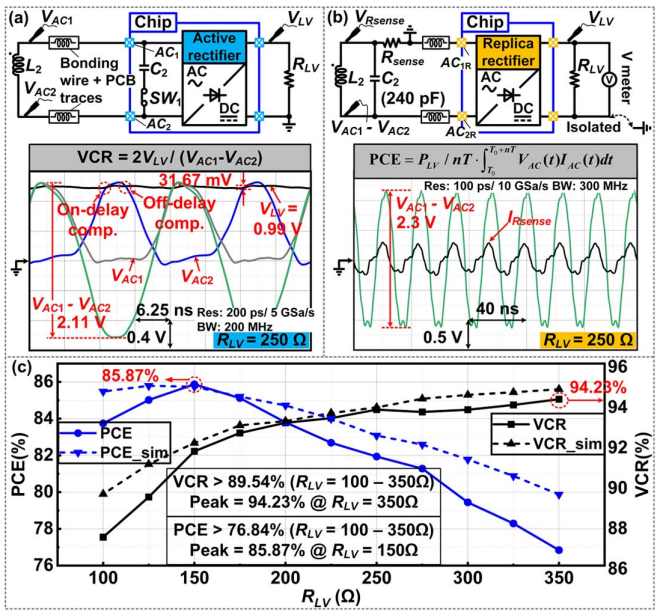



Fig. 14. (a) VCR measurement diagram with measured waveforms of $V_{LV}$, $V_{AC1}$, and $V_{AC2}$ for VCR calculation at $R_{LV} = 250\Omega$, (b) PCE measurement diagram with measured waveforms of $V_{AC2}$ - $V_{AC1}$ and $V_{Rsense}$ for PCE calculation at $R_{LV} = 250\Omega$, (c) Measured PCE and VCR versus $R_{LV}$.

is used to measure the rectifier PCE, avoiding the need for complicated current measurements in the *LC* tank. Fig. 14(b) illustrates this setup, based on [36], [58]. A 10Ω current-sensing resistor captures the input current, which is then multiplied by $V_{AC}$ to calculate the average input power across several cycles. Meanwhile, the average output power at $V_{LV}$ is measured using an isolated voltage meter. For a 250Ω load, the measured input power is 4.02 mW with $V_{LV} = 0.91$V, resulting in a PCE of 82.5%.

Fig. 14(c) provides a summary of the simulated and measured VCR and PCE across all loads, ranging from 100Ω to 350Ω. The measured VCR peaks at 94.23% at $R_{LV} = 350\Omega$, while the PCE reaches 85.87% at $R_{LV} = 150\Omega$.

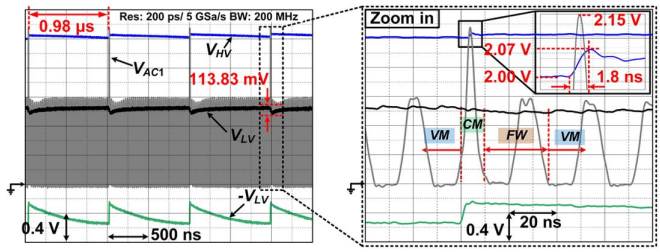



Fig. 15. Measured dual VM/CM operation waveforms under the conditions of $R_{HV} = 400$ kΩ and $R_{LV} = 150\ \Omega$.

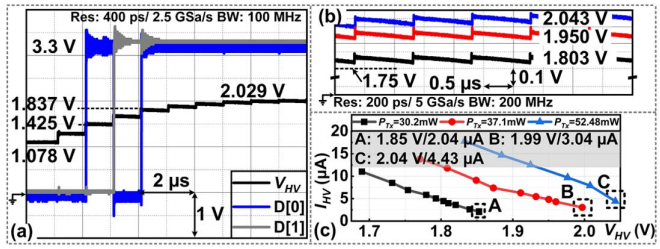



Fig. 16. (a) Measured $V_{HV}$ charging and delay compensation logic (3.3V I/O) waveforms with $R_{HV} = 1$ MΩ, (b) Measured steady state $V_{HV}$ with $R_{HV} = 400$ kΩ under different $P_{TX}$, (c) Measured maximum $I_{HV}$ and $V_{HV}$ under different $P_{TX}$.

### C. Dual-Mode (Dual) Outputs Measurement

Fig. 15 shows the measured transient waveforms to validate the dual VM/CM operation. The test conditions are set to $R_{HV} = 400$ kΩ and $R_{LV} = 150\Omega$, with a transmitter power of 17.2 dBm. The negative voltage generator operates as intended, producing -0.5 V to disconnect the *LC* resonator and enable the CM operation every 0.98 µs ($N_0 = 40$). As a result, $V_{AC1}$ rises above $V_{HV}$ (2.0 V), leading to an undershoot in $V_{LV}$ of 113.83 mV due to the lack of charging in the CM and FW phases. Thanks to the FWR structure, the undershoot only lasts for one cycle. This is acceptable since $V_{LV}$ has more relaxed requirements during HV stimulation.

Fig. 16(a) shows the measured charging procedure of $V_{HV}$ alongside the delay compensation logic outputs, validating the CM charging concept. The test conditions are set at $R_{HV} = 1$ MΩ and $R_{LV} = 200\Omega$, with a transmitter power of 15.7 dBm. During $V_{HV}$ charging, the voltage rises from 1.078 V to 2.029 V within 7 µs. The delay compensation logic $D[1:0]$ ($D[2]$ not shown) automatically changes as $V_{HV}$ increases according to the functionality described in Section III-C. The maximum achievable $V_{HV}$ depends on the transmitter power (Fig. 16(b)) and the load current $I_{HV}$. When $I_{HV}$ increases to 4.88 µA, $V_{HV}$ can be regulated to 1.95 V. Fig. 16(c) illustrates the correlation between $V_{HV}$ and the maximum current load, as a function of the transmitter power. High output current can be achieved by increasing $P_{TX}$.

### D. Load Transient Measurement

Fig. 17(a) and (b) present the load transient responses of $V_{LV}$ and $V_{HV}$, respectively. As the Tx power increases from

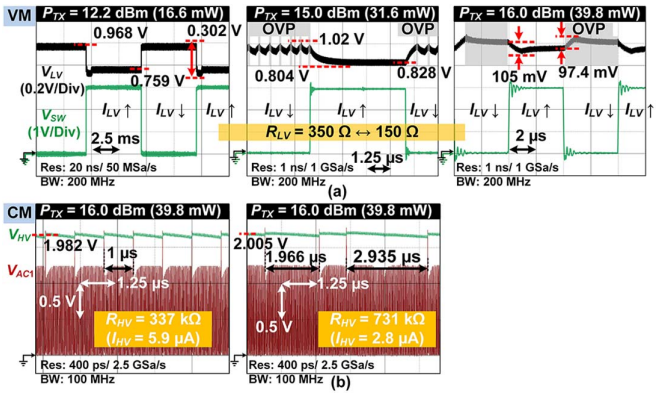



Fig. 17. Measured load transient response waveform of (a) $V_{LV}$ with $R_{LV}$ switching between 150 Ω ∼ 350 Ω and (b) $V_{HV}$ with $R_{HV}$ switching between 338 kΩ and 731 kΩ.

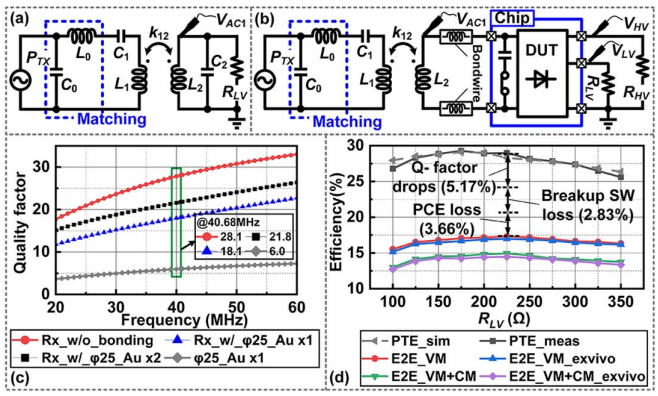



Fig. 18. (a) PTE measurement setup, (b) E2E efficiency measurement setup, (c) Simulated Q-factors of the receiver coil w/ and w/o the bonding wires connections, and (d) Measured system-level PTE/E2E vs. $R_{LV}$ with $R_{HV}$ fixed at 400 kΩ.

12.2 dBm to 16.0 dBm, $V_{LV}$ is regulated around 1.0 V under both light and heavy load conditions, exhibiting a 105 mV undershoot and a 97.4 mV overshoot at 20 ns rise/fall load step. The $V_{HV}$ regulation is achieved through a self-adaptive scheme that adjusts to varying load conditions. Under the light load condition, the slower discharge rate requires less frequent recharging, validating the proposed mode-switching concept.

### E. System-Level Efficiency Measurement

Fig. 18(d) presents the system-level efficiency results, covering both PTE and end-to-end (E2E) efficiency using the Tx/Rx coils in Table I. The PTE is measured using an external resonant capacitor $C_2$ terminated with a resistive load $R_{LV}$ without the chip (Fig. 18(a)). The measured PTE matches the simulated PTE closely, achieving 28.98% at 225Ω load. The E2E efficiency is measured using the PMU chip with the integrated resonant capacitor and a resistive load for each output, $R_{LV}$ and $R_{HV}$ (Fig. 18(b)). The peak E2E efficiency for VM and dual VM/CM are 17.32% and 14.94%, respectively, when $R_{LV} = 225\Omega$. Notably, the E2E efficiency decreases at most by 2.7% across all loads when regulating also $V_{HV}$. The E2E efficiency was measured using a 9-mm pork sample with a 5-mm air gap between the Tx/Rx coils to simulate biomedical implant conditions (see Table I, bottom-right). The *ex vivo* experiment results show negligible efficiency degradation, with E2E efficiency decreasing by less than 0.48% across all loads.

The difference between the PTE and E2E efficiencies is due to three main reasons: (i) The rectifier PCE accounts for 3.66% losses, (ii) The breakup switch in the *LC* resonator accounts for 2.83% losses, (iii) The impedance of the bonding wires (gold, 1.5 mm long, 25 µm diameter, two parallel-connected wires per AC input) and PCB traces between the Rx coil and the on-chip resonance capacitor account for 5.17% losses. This is due to the quality factor drops of the receiver from 28.1 to 21.8 (simulated result, see Fig. 18(c)). This issue can be mitigated using parallel bonding wires to lower their equivalent resistance and adjust the PCB/coil designs.

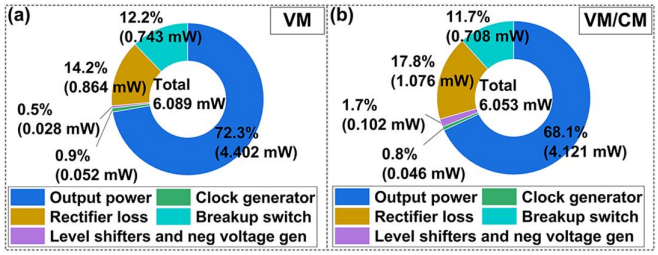



Fig. 19. Simulated power breakdown of the chip working at $R_{LV} = 250\Omega$ in (a) VM operation, (b) VM/CM operation.

### F. Power Breakdown

Fig. 19 shows the simulated power breakdown of the proposed Rx chip design operated in the VM and dual VM/CM under the load condition of $R_{LV} = 250\Omega$. The dual VM/CM operation achieves an output efficiency of 68.1% on $V_{LV}$, which is slightly less (4.19%) than that of the VM operation. The lower power efficiency is mainly due to the extra power consumption for the level shifters and the negative voltage generation block in Fig. 7(b), in addition to the cycles used for the CM and FW phases, during which $V_{LV}$ is not charged.

### G. Comparison With State-of-the-Art

The performance of the proposed PMU is summarized and compared with the state-of-the-art in Table II. Most designs using voltage-mode charging [34], [35], [36], [37] assume that $V_{HV}$ has the largest load, thus $V_{AC} > V_{HV}$ most of the time. While other works adopt current-mode charging to mitigate the need for large $V_{AC}$, their performance in terms of voltage ripple and voltage rating (by using thick-oxide devices) remains constrained by using HWM charging [11], [23], [48]. Additionally, the large off-chip output capacitors (several $\mu$F) hinder system integration for implantable devices.

In contrast, the proposed SIDO PMU is the only design that prioritizes delivering the main portion of power to $V_{LV}$ while achieving high power efficiency. This represents a significant advantage over previous VM rectifier designs that prioritize

TABLE II
COMPARISON TO STATE-OF-THE-ART DUAL-OUTPUT RECTIFIER DESIGNS

| Item | TBioCAS'19 [23] | TBioCAS'20 [34] | JSSC'21 [35] | JSSC'22 [11] | TCAS-I'23 [48] | JSSC'24 [36] | JSSC'24 [37] | This work |
|---|---|---|---|---|---|---|---|---|
| **Process** | 350-nm | 180-nm | 180-nm | 180-nm HV BCD | 180-nm | 65-nm | 65-nm | 40-nm |
| **Frequency (MHz)** | 1 | 1-10 | 6.78 | 40.68 | 6.78 | 40.68 | 13.56 | **40.68** |
| **Structure** | CM | Full-wave VM | HWM[2] | HWM + CM | CM | Full-wave VM + HWM | Full-wave VM | **Full-wave VM + CM** |
| **Cold-startup** | No | No | Yes | Yes | Yes | Yes | Yes | **Yes** |
| **Output voltage** | 2.6 V & 3.9 V | 1.5 - 3 V & 1.5 - 3 V | 1.8 V & 3.3 V | 10 V & 4.7 V & 2 V | 1.8 V & 3 V | 1.1 V& 2.2 V | 1.2 V & 2.5 V | 1.0 V & 2.0 V |
| **Power $P_{OUT}$ (mW)** | 4.7 (mainly $P_{LV}$) | ≤65 (mainly $P_{HV}$) | ≤1020 (mainly $P_{HV}$) | 186 (mainly $P_{HV}$) | ≤ 7 (mainly $P_{HV}$) | ≤60.5 (mainly $P_{HV}$) | ≤ 20 (mainly $P_{HV}$) | ≤ 10 **(mainly $P_{LV}$)** |
| **PCE@$P_{HV}$ (mW) & $P_{LV}$ (mW)** | 75.3%@N/A & 4.7 | 90.75%@62.5 & 1<br>83%@6.25 & 1.0 | 91.9%@660 & 360<br>65%@66 & 36 | 81%@186 & N/A & N/A | 85.1%@1 & 1 | 90.1%@55 & 1.1<br>76%@5.5 & 5.5 | 88%@8 & 8 | **85.87%@0.011 & 6.7** |
| **Active area** ($mm^2$) | 1.35 | < 6 | < 0.601 | < 4.6 | 2.7 | < 0.74 | 0.145[4] | **1.18 & 0.24**[5] |
| **Tx/Rx diameter ratio** | 70 mm / 22 mm | N/A (cap. coupling) | N/A | 33 mm / 24 mm | 41 mm / 23 mm | 16.5 mm / 4 mm | 35 mm / 30 mm | 26.8 mm / 16 mm |
| **Coil distance (mm)** | N/A | N/A | 15 | 12 | 10 | 2 | 6-15 | 14 |
| **Link efficiency** | N/A | N/A | N/A | 86.6% | N/A | N/A | N/A | 25.59% - 29.28% |
| **End-to-end efficiency** | N/A | N/A | N/A | 69.66% | 31.3% @ $P_{OUT}$ = 2 mW | N/A | 32.4-62.7% | VM: 17.32%, VM + CM: 14.94% |
| **Output voltage ripple** | N/A | < 6 $mV_{pp}$ | 42 - 60 $mV_{pp}$ | N/A | CM: 180 $mV_{pp}$ | 90 $mV_{pp}$ | N/A | **VM: 31.67 $mV_{pp}$, VM + CM: 113.83 $mV_{pp}$** |
| **No. of off-chip capacitors**[1] | 4 (0.1 µF / 4.7 µF / 4.7 µF / 100 µF) | 2 (0.47 µF / 1 µF) | 3 (1.1 $nF^3$ / 4.7 µF / 4.7 µF) | 4 (N/A) | 3 (N/A) | 3 (194 $pF^3$ / 220 nF / 470 nF) | 3 (238 $pF^3$ / 1 µF / 1 µF) | **0** |

[1] Including the resonant capacitor [2] Half-wave mode [3] Calculated from the resonant frequency [4] Including the on-chip decoupling capacitor [5] w/ & w/o on-chip capacitors

identical currents to charge both outputs. With all resonant and output capacitors integrated on-chip, the proposed design occupies only 1.18 $mm^2$ of active chip area. The measured voltage ripple on $V_{LV}$ remains competitive with other designs that rely on off-chip capacitors ($100 \sim 500\times$ higher than the on-chip capacitor used in this work), thanks to the FWR structure and high resonance frequency.

## V. CONCLUSION

This paper presents a fully integrated SIDO PMU for wirelessly powering modern closed-loop neuromodulation implants. The proposed SIDO PMU is configurable to operate in either single-output ($V_{LV}$) or dual-output mode ($V_{LV}$ and $V_{HV}$). In the dual-output configuration, it uses a combined voltage/current-mode strategy to simultaneously generate $V_{LV}$ for high-power loads and $V_{HV}$ for low-power loads. The chip operates at 40.68 MHz and requires only an external Rx coil while achieving a peak E2E efficiency of 14.94% when enabling the dual VM/CM charging. The wireless power link can provide a maximum output power of 10 mW on $V_{LV}$ and drive µA load levels on $V_{HV}$. These advantages make this work attractive for applications requiring distinct power levels and precision on different outputs.

## APPENDIX

In this section, we derive Eq. (6) and Eq. (7) for the optimal resonant cycle analysis using rectifier waveforms in Fig. 3.

*1) CM Operation:* The CM operation begins at $t = t_0$. $i_{L2}$ first charge the parasitic capacitor $C_{\text{par}}$ until $V_{AC1}$ exceeds $V_{HV}$ ($t = t_1$). Neglecting the inductor resistance $R_2$, and assuming the initial condition of $i_{L2}(t_0) = i_{L2\text{MAX}}$ and $\frac{di_{L2}(t)}{dt}\big|_{t=t_0} = 0$, the nodal equation can be derived as:

$$L_2 \frac{di_{L2}(t)}{dt} + \frac{1}{C_{\text{par}}} \int_{t_0=0}^{t_1} i_{L2}(t)dt = 0 \tag{10}$$

At $t_1$, $C_{\text{par}}$ is charged to $V_{AC1} = V_{HV}(n)$, where $n$ is the current CM charging cycle. Across two consecutive charging cycles (from $t_2$ to the next $t_1$, approximated as $\Delta T \approx \frac{N_0}{f_{clk}}$, $V_{HV}$ decreases by Eq. (11), due to the absence of charging:

$$V_{HV\_disch}(n) = V_{HV}(n-1)(1 - e^{-\Delta T/\tau}) \tag{11}$$

where $\tau = R_{HV}C_{HV}$ is the time constant formed by the load and filtering capacitor at $V_{HV}$, $f_{clk}$ is the resonant frequency, and $N_0$ is the number of AC periods in between CM charging cycles. Hence, $V_{HV}$ at step $n$ can be derived as (neglecting the zero crossing voltage, $V_{ZC}$, for simplicity):

$$V_{HV}(n) = V_{HV}(n-1)e^{-\Delta T/\tau} = \frac{1}{C_{\text{par}}} \int_{t_0=0}^{t_1} i_{L2}(t)dt \tag{12}$$

By solving Eq. (10) and Eq. (12), the solution for $t_1$ and the corresponding current $i_{L2}(t_1)$ can be obtained:

$$t_1 = \frac{1}{\omega_d} \arcsin\left[\frac{\omega_d C_{\text{par}} V_{HV}(n-1)e^{-\Delta T/\tau}}{i_{L2,\max}}\right] \tag{13}$$

$$i_{L2}(t_1) = i_{L2,\max}\cos(\omega_d t_1) \tag{14}$$

During the CM charging transfer phase ($t_2$), $i_{L2}(t)$ decreases approximately linearly with a slope of $i'_{L2}(t_1)$ due to the short charging time ($t_2 < 2$ ns). Hence, $i_{L2}(t_2)$ can be derived as:

$$i_{L2}(t_2) = i_{L2}(t_1) + i'_{L2}(t_1) \cdot (t_2 - t_1) \tag{15}$$

Finally, the voltage increase per charging cycle can be analytically approximated using Eq. (16):

$$V_{HV\_ch}(n) = \frac{\int_{t_1}^{t_2} i_{L2}(t)dt}{C_{HV}} \simeq \frac{i_{L2}(t_1) + i_{L2}(t_2)}{2} \cdot \frac{t_2 - t_1}{C_{HV}} \tag{16}$$

$V_{HV}(n)$ can be derived recursively based on Eq. (11) and (16).

*2) VM Operation:* The VM operation begins at $t = t'_0$. $i_{L2}(t)$ first charge the resonant capacitor $C_2$, and the parasitic capacitance $C_{\text{par}}$, until $V_{AC2}$ exceeds $V_{LV}$ plus the rectifier power switch drop $V_D$ at $t = t_3$:

$$\frac{1}{C_2} \int_{t'_0=0}^{t_3} i_{L2}(t) \frac{C_2}{C_2 + C_{\text{par}}} dt + V_{ZC} = V_{LV}(n-1) + V_D \tag{17}$$

By solving Eq. (17), the expression for $t_3$ is derived as follow:

$$t_3 = \frac{1}{\omega} \arcsin \left\{ \frac{\omega(C_2 + C_{\text{par}}) \left[ V_{LV}(n-1) + V_D - V_{ZC} \right]}{i_{L2,\max}} \right\} \tag{18}$$

Similar to Eq. (11) and Eq. (16), the precise charging and discharging voltages of $V_{LV}$ in each half-period cycle can be calculated as follows:

$$V_{LV\_ch}(n) = \frac{1}{C_{LV}} \int_{t_3}^{t_4} i_{L2}(t) dt \tag{19}$$

$$V_{LV\_disch}(n) = [V_{LV}(n-1) + V_{LV\_ch}(n)](1 - e^{-\Delta T'/\tau'}) \tag{20}$$

where $t_4 = 1/4f_{clk}$, $\tau' = R_{LV}C_{LV}$ is the time constant formed by the load and filtering capacitor at $V_{LV}$, $\Delta T' = t_6 - t_4 \simeq t_3 + 1/4f_{clk}$. $V_{LV}(n)$ can be derived recursively based on Eq. (19) and Eq. (20).

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## REFERENCES

[1] S. S. Ghoreishizadeh, D. Haci, Y. Liu, N. Donaldson, and T. G. Constandinou, "Four-wire interface ASIC for a multi-implant link," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 12, pp. 3056–3067, Dec. 2017.

[2] Y. Jia et al., "A trimodal wireless implantable neural interface system-on-chip," in *Proc. IEEE Int. Solid-State Circuits Conf. - (ISSCC)*, San Francisco, CA, USA, 2020, pp. 414–416.

[3] V. W. Leung et al., "Distributed microscale brain implants with wireless power transfer and Mbps Bi-directional networked communications," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Austin, TX, USA, 2019, pp. 1–4.

[4] A. Zhou et al., "A wireless and artefact-free 128-channel neuromodulation device for closed-loop stimulation and recording in non-human primates," *Nature Biomed. Eng.*, vol. 3, no. 1, pp. 15–26, Jan. 2019.

[5] S. Reich, M. Sporer, M. Haas, J. Becker, M. Schüttler, and M. Ortmanns, "A high-voltage compliance, 32-channel digitally interfaced neuromodulation system on chip," *IEEE J. Solid-State Circuits*, vol. 56, no. 8, pp. 2476–2487, Aug. 2021.

[6] U. Shin et al., "A 256-channel 0.227μJ/class versatile brain activity classification and closed-loop neuromodulation SoC with 0.004mm2-1.51 μW/channel fast-settling highly multiplexed mixed-signal front-end," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, 2022, pp. 338–340.

[7] M. A. Shaeri, U. Shin, A. Yadav, R. Caramellino, G. Rainer, and M. Shoaran, "A 192/512-channel 2.46mm0x000B2 miniaturized brain-machine interface chipset enabling 31-class brain-to-text conversion through distinctive neural codes," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, 2024, pp. 546–548.

[8] A. Akinin et al., "An optically addressed nanowire-based retinal prosthesis with wireless stimulation waveform control and charge telemetering," *IEEE J. Solid-State Circuits*, vol. 56, no. 11, pp. 3263–3273, Nov. 2021.

[9] A. Burton et al., "Fully implanted battery-free high power platform for chronic spinal and muscular functional electrical stimulation," *Nature Commun.*, vol. 14, Nov. 2023, Art. no. 7887.

[10] S. F. Cogan, "Neural stimulation and recording electrodes," *Annu. Rev. Biomed. Eng.*, vol. 10, pp. 275–309, Aug. 2008.

[11] E. So, P. Yeon, E. J. Chichilnisky, and A. Arbabian, "An RF-ultrasound relay for adaptive wireless powering across tissue interfaces," *IEEE J. Solid-State Circuits*, vol. 57, no. 11, pp. 3429–3441, Nov. 2022.

[12] H.-G. Rhew, J. Jeong, J. A. Fredenburg, S. Dodani, P. G. Patil, and M. P. Flynn, "A fully self-contained logarithmic closed-loop deep brain stimulation SoC with wireless telemetry and wireless power management," *IEEE J. Solid-State Circuits*, vol. 49, no. 10, pp. 2213–2227, Oct. 2014.

[13] H. Wu et al., "Conceptualization and validation of an open-source closed-loop deep brain stimulation system in rat," *Scientific Rep.*, vol. 5, Apr. 2015, Art. no. 9921.

[14] M. T. Salam, J. L. Perez Velazquez, and R. Genov, "Seizure suppression efficacy of closed-loop versus open-loop deep brain stimulation in a rodent model of epilepsy," *IEEE Trans. Neural Syst. Rehabil. Eng.*, vol. 24, no. 6, pp. 710–719, Jun. 2016.

[15] J. E. Fleming, E. Dunn, and M. M. Lowery, "Simulation of closed-loop deep brain stimulation control schemes for suppression of pathological beta oscillations in Parkinson's disease," *Frontiers Neurosci.*, vol. 14, Mar. 5, 2020, Art. no. 166.

[16] W. Kang, C. Ju, J. Joo, J. Lee, Y.-M. Shon, and S.-M. Park, "Closed-loop direct control of seizure focus in a rodent model of temporal lobe epilepsy via localized electric fields applied sequentially," *Nature Commun.*, vol. 13, no. 1, pp. 7805–7818, 2022.

[17] R. Lycke et al., "Low-threshold, high-resolution, chronically stable intracortical microstimulation by ultraflexible electrodes," *bioRxiv*, Feb. 21, 2023, doi: 10.1101/2023.02.20.529295.

[18] T. Guo et al., "Closed-loop efficient searching of optimal electrical stimulation parameters for preferential excitation of retinal ganglion cells," *Frontiers Neurosci.*, vol. 12, Mar. 2018, doi: 10.3389/fnins.2018.00168.

[19] G. K. Wu, Y. Ardeshirpour, C. Mastracchio, J. Kent, M. Caiola, and M. Ye, "Amplitude- and frequency-dependent activation of layer II/III neurons by intracortical microstimulation," *Science*, vol. 26, no. 11, Nov. 2023.

[20] Y.-J. Lin et al., "A 3.1-5.2GHz, energy-efficient single antenna, cancellation-free, bitwise time-division duplex transceiver for high channel count optogenetic neural interface," *IEEE Trans. Biomed. Circuits Syst.*, vol. 16, no. 1, pp. 52–63, Feb. 2022.

[21] D.-H. Choi and D.-W. Jee, "A 1984-pixels, 1.26 nW/pixel retinal prosthesis chip with time-domain in-pixel image processing and bipolar stimulating electrode sharing," *IEEE J. Solid-State Circuits*, vol. 58, no. 10, pp. 2757–2766, Oct. 2023.

[22] N. U. Hassan, S.-W. Hong, and B. Lee, "A robust multioutput self-regulated rectifier for wirelessly powered biomedical applications," *IEEE Trans. Ind. Electron.*, vol. 68, no. 6, pp. 5466–5472, Jun. 2021.

[23] H. S. Gougheri, P. Graybill, and M. Kiani, "A dual-output reconfigurable shared-inductor boost-converter/current-mode inductive power management ASIC with 750% extended output-power range, adaptive switching control, and voltage-power regulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 5, pp. 1075–1086, Oct. 2019.

[24] B. Lee et al., "An inductively-powered wireless neural recording and stimulation system for freely-behaving animals," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 2, pp. 413–424, Apr. 2019.

[25] J. Lim, B. Lee, and M. Ghovanloo, "Optimal design of a resonance-based voltage boosting rectifier for wireless power transmission," *IEEE Trans. Ind. Electron.*, vol. 65, no. 2, pp. 1645–1654, Feb. 2018.

[26] T. Sun, X. Xie, G. Li, Y. Gu, X. Li, and Z. Wang, "An omnidirectional wireless power receiving IC with 93.6% efficiency CMOS rectifier and Skipping Booster for implantable bio-microsystems," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Jeju, Korea (South), 2011, pp. 185–188.

[27] J. Kim, J. Kim, M. Sim, S. Kim, and C. Kim, "A single-input four-output (SIFO) AC–DC rectifying system for vibration energy harvesting," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2629–2633, Jun. 2014.

[28] Y. Lu, M. Huang, L. Cheng, W.-H. Ki, S. -P. U, and R. P. Martins, "A dual-output wireless power transfer system with active rectifier and three-level operation," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 927–930, Feb. 2017.

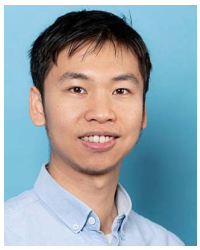
[29] S. Fan, Z. Xue, H. Lu, Y. Song, H. Li, and L. Geng, "Area-efficient on-chip DC–DC converter with multiple-output for bio-medical applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 11, pp. 3298–3308, Nov. 2014.

[30] K. Noh, J. Amanor-Boadu, M. Zhang, and E. Sánchez-Sinencio, "A 13.56-MHz CMOS active rectifier with a voltage mode switched-offset comparator for implantable medical devices," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 10, pp. 2050–2060, Oct. 2018.

[31] Y. Wang, D. Ye, L. Lyu, Y. Xiang, H. Min, and C.-J. R. Shi, "A 13.56 MHz wireless power and data transfer receiver achieving 75.4% effective-power-conversion efficiency with 0.1% ASK modulation depth and 9.2 mW output power," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 142–144.

[32] F.-B. Yang, D.-H. Yao, and P.-H. Chen, "A quad-mode structure-reconfigurable regulating rectifier with shared-inductor DC–DC energy

recycling in a wireless power receiver," *IEEE J. Solid-State Circuits*, vol. 59, no. 2, pp. 574–582, Feb. 2024.
[33] M. R. Islam, M. A. Rahman, K. M. Muttaqi, and D. Sutanto, "A new magnetic-linked converter for grid integration of offshore wind turbines through MVDC transmission," *IEEE Trans. Appl. Supercond.*, vol. 29, no. 2, pp. 1–5, Mar. 2019.
[34] R. Erfani, F. Marefat, and P. Mohseni, "A dual-output single-stage regulating rectifier with PWM and dual-mode PFM control for wireless powering of biomedical implants," *IEEE Trans. Biomed. Circuits Syst.*, vol. 14, no. 6, pp. 1195–1206, Dec. 2020.
[35] J. Lin, Y. Lu, C. Zhan, and R. P. Martins, "A single-stage dual-output regulating rectifier with hysteretic current-wave modulation," *IEEE J. Solid-State Circuits*, vol. 56, no. 9, pp. 2770–2780, Sep. 2021.
[36] Z. Luo, J. Liu, and H. Lee, "A high-efficiency 40.68-MHz single-stage dual-output regulating rectifier with ZVS and synchronous PFM control for wireless powering," *IEEE J. Solid-State Circuits*, vol. 59, no. 8, pp. 2418–2429, Aug. 2024.
[37] Y. Liu, Y. Yao, and W.-H. Ki, "A 13.56-MHz single-input dual-output wireless power and data transfer system for bio-implants," *IEEE J. Solid-State Circuits*, vol. 59, no. 8, pp. 2557–2567, Aug. 2024.
[38] H.-S. Lee and H.-M. Lee, "A 92.7%-efficiency 6.78-MHz energy-resuscitating resonant regulating rectifier with dual outputs for wirelessly powered devices," *IEEE J. Solid-State Circuits*, vol. 59, no. 10, pp. 3204–3217, Oct. 2024.
[39] Z. Luo, J. Liu, and H. Lee, "A 40.68-MHz active rectifier with cycle-based on-/off-delay compensation for high-current biomedical implants," *IEEE J. Solid-State Circuits*, vol. 58, no. 2, pp. 345–356, Feb. 2023.
[40] T. Lu, K. A. A. Makinwa, and S. Du, "A single-stage dual-output regulating voltage doubler for wireless power transfer," *IEEE J. Solid-State Circuits*, vol. 59, no. 9, pp. 2922–2933, Sep. 2024.
[41] K. Zheng, Y. Hou, X. Wang, and Y. Liu, "A single-stage dual-output regulating rectifier with sequential pulse frequency modulation control for wireless biomedical applications," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 71, no. 10, pp. 4566–4570, Oct. 2024.
[42] H.-S. Lee, K. Eom, and H.-M. Lee, "A single-input multi-output resonant regulating rectifier generating three outputs in a half cycle for wirelessly powered biomedical devices," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 72, no. 6, pp. 2956–2969, Jun. 2025.
[43] J. Lim, B. Lee, and M. Ghovanloo, "A multiphase resonance-based boosting rectifier with dual outputs for wireless power transmission," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2680–2689, Mar. 2020.
[44] H. Sadeghi Gougheri and M. Kiani, "An inductive voltage-/current-mode integrated power management with seamless mode transition and energy recycling," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 874–884, Mar. 2019.
[45] Y. Engür, H. A. Yigit, and H. Külah, "13.56 MHz triple mode rectifier circuit with extended coupling range for wirelessly powered implantable medical devices," *IEEE Trans. Biomed. Circuits Syst.*, vol. 15, no. 1, pp. 68–79, Feb. 2021.
[46] C.-J. Kuo and S.-I. Liu, "A 13.56 MHz current-mode wireless power receiver with energy-investment capability," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 67, no. 2, pp. 205–209, Feb. 2020.
[47] H. Kim, Y. Park, C. Sung, J. Cho, S. Park, and C. Kim, "DiTTO: A distance adaptive over 100-mW wireless power transfer system with 1.695-Mb/s uplink telemetry and a shared inductor two-output regulating rectification," *IEEE J. Solid-State Circuits*, vol. 59, no. 8, pp. 2568–2580, Aug. 2024.
[48] D.-H. Yao, T.-N. Liu, M. Takamiya, and P.-H. Chen, "A 6.78-MHz wireless power transfer system with dual-output resonant current-mode regulating rectifier and transmission power regulation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 12, pp. 4986–4998, Dec. 2023.
[49] H.-S. Lee et al., "A power-efficient resonant current mode receiver with wide input range over breakdown voltages using automated maximum efficiency control," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 8738–8750, Jul. 2022.
[50] M. Choi, T. Jang, J. Jeong, S. Jeong, D. Blaauw, and D. Sylvester, "A resonant current-mode wireless power receiver and battery charger with -32 dBm sensitivity for implantable systems," in," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2880–2892, Dec. 2016.
[51] T. Lu and S. Du, "A switching-mode single-stage dual-output regulating rectifier achieving 92.33% efficiency and extended range for wireless power transfer," in *Proc. IEEE Eur. Solid-State Electron. Res. Conf. (ESSERC)*, Bruges, Belgium, 2024, pp. 169–172.
[52] T. Lu and S. Du, "A coupling-adaptive wireless power transfer system with voltage-/current-mode receiver and global digital-PWM regulation," *IEEE J. Solid-State Circuits*, vol. 59, no. 12, pp. 4175–4187, Dec. 2024.
[53] D. G. Muratore and E. J. Chichilnisky, "Artificial retina: A future cellular-resolution brain-machine interface," in *NANO-CHIPS 2030. The Frontiers Collection*, B. Murmann and B. Hoefflinger, Eds., Cham, Switzerland: Springer-Verlag, 2020, pp. 443–465.
[54] H.-M. Lee and M. Ghovanloo, "An integrated power-efficient active rectifier with offset-controlled high speed comparators for inductively powered applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 8, pp. 1749–1760, Aug. 2011.
[55] H.-C. Cheng, C.-S. A. Gong, and S.-K. Kao, "A 13.56 MHz CMOS high-efficiency active rectifier with dynamically controllable comparator for biomedical wireless power transfer systems," *IEEE Access*, vol. 6, pp. 49979–49989, 2018.
[56] C.-Y. Wu, X.-H. Qian, M.-S. Cheng, Y.-A. Liang, and W.-M. Chen, "A 13.56 MHz 40 mW CMOS high-efficiency inductive link power supply utilizing on-chip delay-compensated voltage doubler rectifier and multiple LDOs for implantable medical devices," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2397–2407, Nov. 2014.
[57] L. Cheng, X. Ge, L. Hu, Y. Yao, W.-H. Ki, and C.-Y. Tsui, "A 40.68-MHz active rectifier with hybrid adaptive on/off delay-compensation scheme for biomedical implantable devices," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 2, pp. 516–525, Feb. 2020.
[58] Y. Lu and W.-H. Ki, "A 13.56 MHz CMOS active rectifier with switched-offset and compensated biasing for biomedical wireless power transfer systems," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 3, pp. 334–344, Jun. 2014.
[59] X. Li, C.-Y. Tsui, and W.-H. Ki, "A 13.56 MHz wireless power transfer system with reconfigurable resonant regulating rectifier and wireless power control for implantable medical devices," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 978–989, Apr. 2015.
[60] P. Feng and T. G. Constandinou, "Robust wireless power transfer to multiple mm-scale freely-positioned neural implants," in *Proc. IEEE Biomed. Circuits Syst. Conf. (BioCAS),* Cleveland, OH, USA, 2018, pp. 1–4.
[61] H. S. Gougheri and M. Kiani, "Current-based resonant power delivery with multi-cycle switching for extended-range inductive power transmission," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 9, pp. 1543–1552, Sep. 2016.
[62] H. Banba et al., "A CMOS bandgap reference circuit with sub-1-V operation," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 670–674, May 1999.
[63] C.-Y. Wu, S.-H. Wang, and L.-Y. Tang, "CMOS high-efficiency wireless battery charging system with global power control through backward data telemetry for implantable medical devices," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 12, pp. 5624–5635, Dec. 2020.
[64] X. Bai, Y. Lu, C. Zhan, and R. P. Martins, "A 6.78-MHz wireless power transfer system with inherent wireless phase shift control without feedback data sensing coil," *IEEE J. Solid-State Circuits*, vol. 58, no. 6, pp. 1746–1757, Jun. 2023.
[65] H.-M. Lee, H. Park, and M. Ghovanloo, "A power-efficient wireless system with adaptive supply control for deep brain stimulation," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2203–2216, Sep. 2013.
[66] H. Wang, Y. Du, X. Jia, and Y. Fan, "A low-power continuous-time comparator with enhanced bias current at the flip point," in *Proc. IEEE 11th Int. Conf. ASIC (ASICON)*, Chengdu, China, 2015, pp. 1–4.
[67] U. Jow and M. Ghovanloo, "Design and optimization of printed spiral coils for efficient transcutaneous inductive power transmission," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 3, pp. 193–202, Sep. 2007.



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