Ferroelectric Materials and Artificial Dielectric Layer Structures for Microwave Integrated Circuit Technologies

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Ferroelectric Materials and Artificial Dielectric Layer Structures for Microwave Integrated Circuit Technologies

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Contents

Chapter 1

Introduction

1.1 Motivation and background

The emergence of monolithic microwave integrated circuits (MMICs) in the past two decades has caused a dramatic change in our everyday life and experience. Today, MMIC technology is a multi-billion dollar industry and the backbone of our information and communication society. With the efforts of thousands of microwave scientists and engineers, cell phone has gone from an expensive, heavy and large item to a portable communication tool in everyone's pocket, even as small as a wrist watch (see Fig.1.1), which allows people to communicate from almost anywhere. The impact of the MMIC revolution, however, has not remained confined to the sphere of personal communication. Modern ultra-compact communication systems provide a wide variety of services from high-quality audio and video to high-speed internet and wireless access. The transfer of such high data rates requires high-speed data links which could not have been realized without miniature MMIC transceivers. Well known examples are local area networks (WLAN) and wireless personal area networks (WPAN) used by modern personal digital

assistants (PDAs) and notebook computers.

The advent of low-cost commercial radar for sensing and position detection is another major driver of the MMIC technology. Automotive wireless (e.g., radar) sensors are revolutionizing driving safety and automated traffic control [1-5]. Already, radar-based systems providing adaptive cruise control are being fitted to luxury cars, and this market alone is expected to witness a nearly 20-fold increase in near future [6]. The ever increasing popularity of cheap, light and compact navigation instruments utilizing the global positioning system (GPS) is another application area where MMICs are indispensable.

Figure 1.1: One of world's first cell phones held by inventor Martin Cooper, as compared to the wrist watch mobile phone packing a 1.5-inch touchscreen with tiny built-in stylus, bluetooth 2.0, MP4 and MP3 players.

Historically, the origin of the MMIC technology can be traced back to the development of planar transmission lines and solid state devices [7]. Over the last 50 years, driven by the IC-technology trend of smaller size, lighter weight, lower cost and increased complexity, huge amounts of research interests have been attracted in this direction [7,8]. Initially, GaAs was the substrate of choice for microwave integrated circuits because of its high electron mobility, leading to faster transistors, and its semi-insulating electrical characteristics, making it a suitable vehicle for microwave passive components. However, GaAs device manufacturing is very difficult and transistors on GaAs are very fragile and easily damaged by overheating or electrical overload [9].

Due to these shortcomings and the already existing enormous market for digital silicon-based ICs, silicon has been replacing GaAs as the mainstream MMIC technology. The maturity of silicon technology makes it extremely cost effective for mass production [10] and offers the further possibility to combine microwave circuits with digital circuits on the same chip. Moreover, excellent microwave device characteristics have been demonstrated with silicon-based SiGe and CMOS transistors with cut-off frequencies exceeding 500 GHz [11]. These results are very promising for active devices to operate at microwave frequencies, while being manufactured on a low cost, highly integrated silicon platform. Nevertheless, the shift towards silicon technology has come at a price. What distinguishes microwave integrated circuits from digital VLSI circuitry is the extensive use of passive components such as capacitors, inductors and transmission lines to implement various functions like impedance matching, phase shifting, and filtering [9]. But the migration of integrated passive microwave components to silicon has caused a number of serious hurdles.

First, unlike CMOS transistors, passive components do not readily shrink with each new generation of processing technology. Lumped inductors and capacitors are per se energy storage devices, which by nature consume relatively large chip area. Besides, the length of transmission lines used in microwave circuit, such as quarter wavelength impedance transformer, is normally comparable with the wavelength at frequencies of interest, sometimes even comparable or larger than the chip size. In addition, integrated passive components on ordinary silicon suffer from substrate loss and crosstalk due to the electromagnetic filed penetration into the conductive silicon, which results in severe performance degradation at microwave frequencies [12]. Finally, compared to conventional logic application, the new functionality of electrical tuning is required for microwave integrated circuits. Tunable components like varactors are widely used in impedance matching, voltage controlled oscillators (VCO), filters and phase arrayed antennas. Although silicon-based semiconductor varactors are available for tuning purposes, their quality factors (Q) typically decrease with increasing frequency. As a result, semiconductor varactors with sufficiently high Q and tunability are still a big challenge for frequencies above 10-20GHz [13].

Over the past decade, various solutions have been proposed to address these issues. In particular, attention has been focused on reducing the loss and crosstalk caused by the conducting silicon material through the use of high-resistivity substrates [14-16], local

removal of silicon (silicon micromachining) [17,18], substrate transfer]19,20], and the use of esoteric technologies such as very thick dielectric layers [21-23] and proton bombardment [24]. Micromachining techniques have also been employed to realize micro-electro-mechanically tunable components (MEMs) [25,26] and potentially to improve the quality of conventional silicon-based varactors.

Nevertheless, by comparison, much less attention has been paid to the use of materials with extraordinary electromagnetic properties as a potential remedy for the issues mentioned above. One exception is the recent effort to reduce the area consumption of on-chip inductors and transmission lines by the implementation of integrated ferromagnetic thin films with high permeability. Such films have been demonstrated to significantly increase the inductance of on-chip solenoid [27] and spiral [28,29] inductors compared with their air core counterparts. Integrated microstrip transmission lines with thin ferromagnetic cores have also been shown to exhibit a shorter propagation wavelength, therefore leading to a smaller device size [30,31].

The objective of this thesis is to explore the application of two other classes of materials in integrated microwave passive components: ferroelectrics and artificial dielectrics. The interest in ferroelectric materials in microwave integrated circuits is primarily due to a high dielectric constant which also depends on the electric field. With dielectric constant possibly as high as a few hundreds even in thin film form, the metal-insulator-metal (MIM) capacitor can be made substantially small while still maintaining an adequate capacitance density value. The recognition of potential applications of ferroelectric materials for microwave tunable devices dates back about fifty years ago. It's until the last decade that intensive research efforts were made in this direction, driven by the miniaturization of microwave components and possible integration in microwave integrated circuits, due to the development of ferroelectric thin and thick film deposition technologies [32].

Likewise, the utilization of artificial dielectrics in microwave engineering is not a new concept. Since the 2nd world war, artificial dielectrics have been studied for use in light weight lenses for antenna beam shaping [33-38]. These materials comprise three dimensional arrays of miniature metallic particles immersed in an insulating dielectric medium [39]. Their dielectric constant can be (locally) engineered by changing the size, shape, and spacing of the particles. However, monolithic integration of artificial dielectrics offers the additional benefit of enhancing the range of material constants and

realizing novel media by exploiting the (sub-) micron patterning and thin film deposition techniques. As such, the exploration of integrated artificial dielectrics and devices based on them is a very new research area which will be explored in this work.

1.2 Ferroelectrics and their applications in microwave engineering

1.2.1 Dielectrics and ferroelectrics

In the so-called dielectric materials, when an electric field is applied, the ions (cations and anions) move in different directions and/or electron clouds deform, causing electric dipole moment (see Fig.1.2). This phenomenon is known as electric polarization of the dielectric, and the polarization (***P***) is expressed quantitatively as the sum of the electric dipole moments per unit volume. According to Poisson's equation, free charges are sources of the electric displacement (***D***) field

$$\nabla \cdot \boldsymbol{D} = \rho_{\text{free}}, \tag{1.1}$$

where ρ_{free} is the density of free charges. The electric displacement ***D*** is related to the electric field (***E***) and polarization ***P*** by the following expression:

$$\boldsymbol{D} = \varepsilon_0 \boldsymbol{E} + \boldsymbol{P}. \tag{1.2}$$

Here, ε_0 is known as the permittivity of vacuum. Most dielectric materials polarize linearly with external electric filed, nonlinearities are negligible. This is usually expressed mathematically as:

$$\boldsymbol{P} = \varepsilon_0 \chi_{ij} \boldsymbol{E}, \tag{1.3}$$

where χ_{ij} is called the dielectric susceptibility of the material and is generally a constant second rank tensor. It follows from (1.2) and (1.3) that

$$\boldsymbol{D} = \varepsilon_0 \boldsymbol{E} + \boldsymbol{P} = \varepsilon_0 \boldsymbol{E} + \varepsilon_0 \chi_{ij} \boldsymbol{E} = \varepsilon_0 (\delta_{ij} + \chi_{ij}) \boldsymbol{E} = \varepsilon_0 \varepsilon_{ij} \boldsymbol{E}, \tag{1.4}$$

where $\varepsilon_{ij} = \delta_{ij} + \chi_{ij}$ is called the relative permittivity or relative dielectric constant and δ_{ij} is Kronecker's delta (ie. $\delta_{ij} = 1$ for $i = j$ and $\delta_{ij} = 0$ for $i \neq j$). In homogeneous isotropic materials, both χ_{ij} and ε_{ij} reduce to scalar constants known as χ and ε_r respectively, which appear in most textbooks [40].

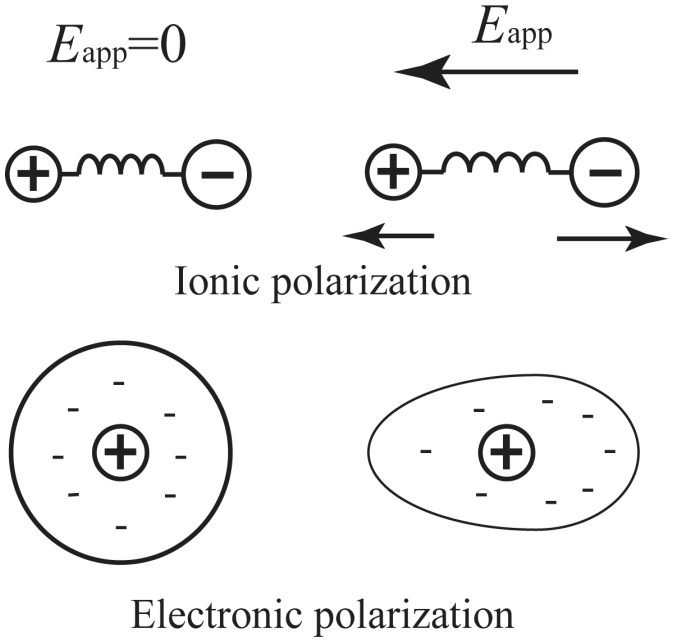

Figure 1.2: Schematics of ionic polarization and electronic polarization.

Depending on the crystalline structures, the positive and negative charge centers of certain materials may not coincide with each other even without an external electric field. Such materials are said to possess electric spontaneous polarization. Ferroelectric materials are commonly defined as crystals which show an electric spontaneous polarization and in which the direction of the polarization can be reversed by an external electric field, yielding a hysteresis loop. The term 'ferroelectric' is used in analogy to

'ferromagnetic', in which the material possesses permanent magnetic moment. Historically, this is because ferroelectricity was first experimentally identified in Rochelle salt ($KNaC_4H_4O_6 \cdot 4H_2O$) by Valasek in 1920, when ferromagnetism was already known. Although the prefix ferro means iron, most ferroelectric materials do not have iron atoms in their lattice. Besides the hysteretic polarization similarity, also akin to ferromagnetic materials is the phase transition temperature of ferroelectrics, denoted by the Curie point T_C. Most ferroelectric materials undergo a structural phase transition from a high-temperature (above the Curie point) non-ferroelectric (also known as paraelectric) phase into a low-temperature (below the Curie point) ferroelectric phase (Fig.1.3). The crystalline symmetry of ferroelectric phase is always lower than the paraelectric phase. Above the Curie point, the relative dielectric constant ε_r falls off with temperature over a wide range in the paraelectric phase according to Curie-Weiss law

$$\varepsilon_r = \frac{C}{T - T_0}, \tag{1.5}$$

where C is the Curie-Weiss constant, T_0 is Curie-Weiss temperature which is equal or slightly lower than the exact phase transition temperature T_C.

Ferroelectric phase transitions are often characterized as of being either displacive or order-disorder type, though often phase transitions will have behavior that contains elements of both types. The distinction is made in terms of whether the paraelectric phase is microscopically non-polar (displacive) or only non-polar in a macroscopic or thermally average sense (order-disorder). Among the many different ferroelectric materials, the ones with perovskite crystal structure are of particular interest for practical applications. Taking $BaTiO_3$ as an example, which is a typical displacive type and is well studied, Fig.1.4 shows both the cubic perovskite structure of paraelectric phase and tetragonal structure of ferroelectric phase (although cubic $BaTiO_3$ crystal transforms successfully to three ferroelectric phases as the temperature goes down, only the first one below the Curie point with tetragonal structure is shown here). In the cubic phase, there is obviously no spontaneous polarization from the symmetry consideration. In the tetragonal phase, the Ti and O ions move relative to Ba at the origin from their cubic positions, thus spontaneous polarization along [001] direction occurs [40].

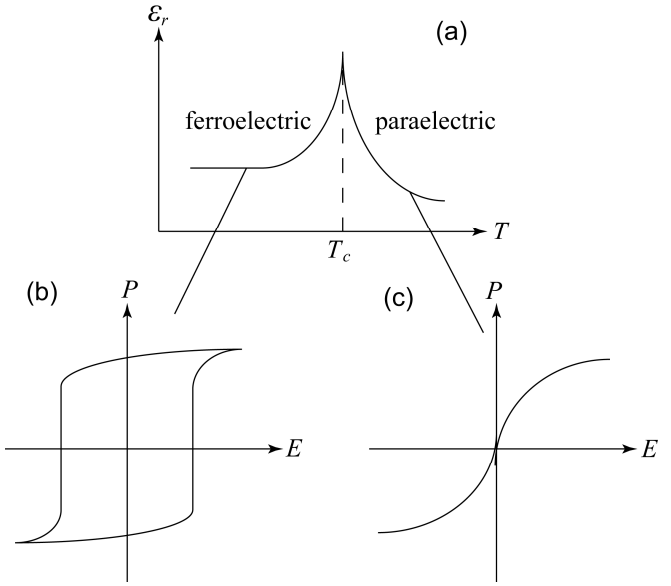

Figure 1.3: Schematics of (a) relative dielectric constant as a function of temperature in different phases; (b) hysteresis loop of polarization-electric filed in a ferroelectric phase and (c) nonlinear polarization-electric field relation in a paraelectric phase.

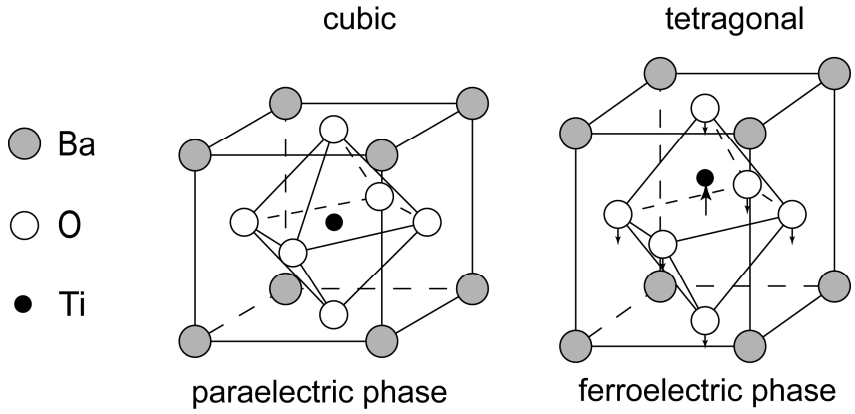

Figure 1.4: Crystal structure of $BaTiO_3$ for a cubic paraelectric phase without spontaneous polarization and a tetragonal ferroelectric phase with spontaneous polarization along [001] direction.

1.2.2 Applications of ferroelectrics

Ferroelectric materials are widely used in various devices especially in modern integrated circuits. A brief summary of applications of ferroelectric materials with an emphasis of thin film and IC technology is presented below.

The first impressive property of ferroelectric material to come to mind is perhaps the high permittivity. For example, single crystal $BaTiO_3$ shows a relative dielectric constant of more than 5000 at room temperature. Although dielectric constant of only a few hundred is observed for thin film form, it is still much higher than that of typical dielectric materials like SiO_2 (with a relative dielectric constant of around 4) widely used in IC technologies. It is the high dielectric constant that makes ferroelectric thin film very attractive for dynamic random access memory (DRAM) applications. As is well known, DRAM capacitor gets physically smaller with scaling, yet adequate capacitance per cell has to be maintained to get enough charge storage ability. For trench capacitor, it means deeper trench must be formed to increase the capacitor surface area, which substantially increase the process complexity and cost. For stacked capacitor, it is difficult to make the surface area indefinitely, therefore, ferroelectric materials like Barium Strontium Titanate (BST) are considered as candidates to replace SiO_2 as the dielectric layer in DRAM capacitor [41].

Ferroelectric materials in ferroelectric phase show hysteresis loop as depicted in Fig. 1.3(b). Basically, two different polarization states of different polarization directions can be identified. Because these two polarization states can be switched between each other with an external electric field, these two states can be used to represent binary states. Furthermore, since a ferroelectric maintains a remanent polarization at zero bias, this memory would require no refreshing, leading to non-volatile ferroelectric memory. A device incorporating a ferroelectric film as a capacitor to hold data is called ferroelectric random access memory (FeRAM). Lead zirconate titanate (PZT) has been proposed to be a good candidate for FeRAM applications [40]. However, both the PZT ferroelectric layer and the noble metals used as electrodes are not compatible with CMOS process integration and may cause contamination issues. Other applications of ferroelectric materials include piezoelectric devices, pyroelectric sensors, electrooptic devices etc. These are beyond the interests of this thesis and will not be discussed here.

1.2.3 Microwave ferroelectric components

Over the last twenty years, with the fast development in IC technologies, ferroelectric materials were extensively investigated and implemented in modern MMICs, mainly due to their extraordinary properties of high permittivity and/or strong field dependence of dielectric constant. One major application of ferroelectric materials in microwave regime is for lumped capacitors. As energy storage devices, capacitors are not readily scaled with logic circuit elements, therefore consume relatively large chip area. The implementation of ferroelectric materials with very high permittivity could potentially solve the problem since the stored electric energy in a material is proportional to its dielectric constant. In conventional GaAs MMIC's, off-chip large capacitors were provided with additional pins, leading to higher pin count and larger package size [42,43]. By integrating these capacitors on chip using conventional SiN as dielectric, the chip size would be extremely large. In contrast, on-chip BST thin film employed by metal organic decomposition (MOD) technique has been demonstrated to have a relative dielectric constant of 300, which is 50 times higher than that of SiN [43]. Therefore, substantial area reduction and more compact package size can be achieved with on-chip BST capacitors, resulting in miniaturization of the RF front-end block of mobile phone sets [43]. The comparisons of area consumption and package size of aforementioned technologies are illustrated in Fig.1.5.

As shown in Fig.1.3, nonlinear relations between electric polarization and electric field are observed in both ferroelectric phase and paraelectric phase, resulting in field dependant permittivity. This characteristic is commonly described by the material tunability, which is defined as the ratio of material permittivity at zero applied electric field to its permittivity at the maximum electric field [32]. This property, combined with relatively low loss at high frequencies, makes ferroelectrics attractive for tunable microwave devices, which is another major application of ferroelectric materials at microwave frequencies. In principle, all forms of ferroelectric materials, *i.e.* bulk, thick film and thin film, can be used for microwave tunable applications. Bulk or single crystalline ferroelectrics are preferred for tunable disc resonators where the largest permittivity can be achieved [44,45]. Thick ferroelectric films can be processed on common microwave substrates like Al_2O_3, in a cost effective way, by screen printing techniques or low temperature co-fired ceramics (LTCC) technology [46,47]. This is attractive to phase arrayed antennas where thousands of phase shifters can be easily

implemented by ferroelectric transmission lines. However, devices based on bulk or thick film ferroelectrics require very high voltages for effective tuning, *i.e.* of the order of hundreds of volts to tens of kilovolts, which hinders their integration in modern MMICs

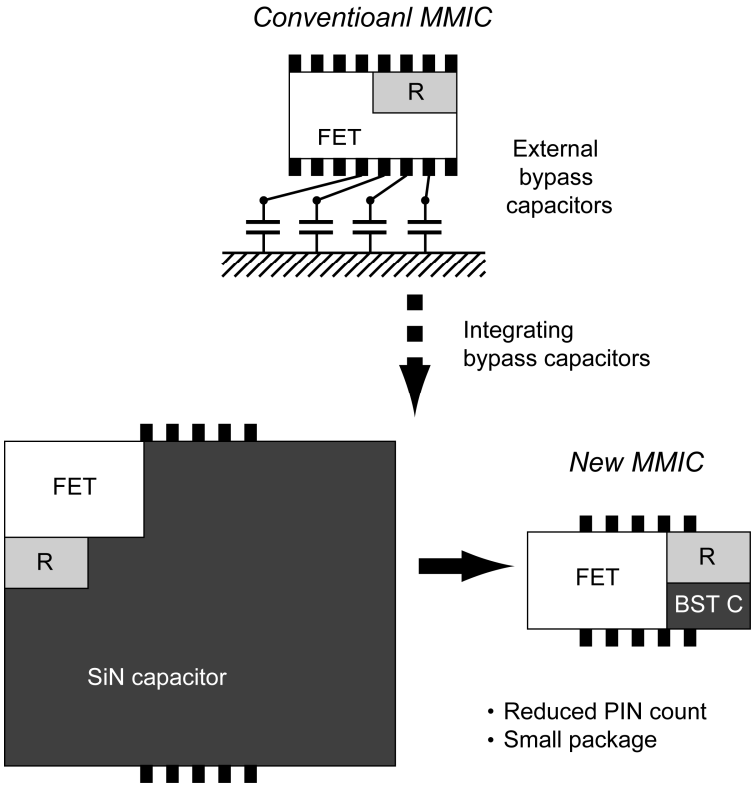

Figure 1.5: Area comparison of MMIC in case of using SiN and BST capacitors. Adapted from [43].

Over the last decade, ferroelectrics in thin film form have attracted high research interest because of its low tuning voltage and its compatibility with modern IC technologies. Microwave tunable components, including varactors, tunable filters, voltage controlled oscillators, phase shifters and delay lines, have been realized already by using thin film ferroelectric materials [32]. Among the various ferroelectric materials, BST thin film has been investigated extensively. Compared to other ferroelectric

materials, BST thin film offers high tuning range (a tunability greater than 13 has been demonstrated [48]), low microwave losses (loss tangent could be as low as 0.005 at 20 GHz [49]), various standard thin film deposition technologies available on different substrates, and Curie temperature control by simply changing the Ba/Sr ratio.

In many works, BST thin film microwave tunable devices have been fabricated on single crystal substrates such as MgO, $LaAlO_3$ and sapphire (see for example [50] and [51]). This is because these substrates have extremely low loss at microwave frequencies. Epitaxial growth of BST thin film on these substrates offers the best quality of the film. However, these substrates are expensive and often only available at small sizes, in contrast silicon is the substrate choice for mass production. Besides, silicon also offers the possibility to co-integrate microwave and digital logic circuits. Recently, much effort has been made to realize BST thin film tunable devices on silicon.

The performance of BST thin film tunable microwave devices (tunability and loss) on silicon depends on various factors, *i.e.,* substrate conductivity, film property, stress, film-electrode interface, device topology and electrodes. Since ordinary silicon loss features high loss at microwave frequencies, high resistivity silicon (HRS) is usually chosen to minimize substrate loss contribution, and thus to achieve high quality factors. Large efforts have been made to optimize BST based tunable devices while considering the aforementioned aspects. For example, the film property can be optimized, from processing aspect, through morphology control [52], compositional design [53] and post deposition treatment [54]. Normally, the electrodes of parallel plate BST varactors are made by platinum (Pt) to withstand high temperature processing step and to offer minimal lattice mismatch. However, Pt has a relatively high resistivity which contributes to high conductor loss. It has been shown that by using a thick bottom electrode consisting of Pt(50nm)/Au(0.5μm), the microwave losses associated with metal layers can be substantially reduced. BST varactors based on this technique have shown record Q factors of about 40 at 45 GHz, which is much higher than that of a silicon abrupt junction varactor diode [55]. Delay lines, phase shifters and voltage controlled oscillator (VCO) based on the high-Q BST varactor technologies have been demonstrated [56-58]. Due to the enormous progresses made, ferroelectrics are gaining attention for microwave tunable applications and becoming commercialized [13]. However, the deposition of ferroelectric materials mostly requires high temperature process steps and platinum as electrode material, which are not well compatible with modern CMOS back-end-of-line (BEOL)

technologies. Another issue related to ferroelectric based tunable components, especially when a thick ferroelectric film is used or a planar capacitor structure is adopted, is the high DC bias voltage (tens to hundreds of volt) required to gain a reasonable tuning range.

1.3 Artificial dielectric materials

Artificial materials, from a broad point of view, are man-made materials in contrast to natural materials which are products of nature. Plastics are perhaps the most well known man-made materials and are surrounding us in our everyday life.

In a narrow sense, artificial materials, sometimes also called metamaterials, are man-made structured composite materials that exhibit electromagnetic properties not available in natural materials. (It is interesting that the term metamaterial is even narrowly referred to artificial material with negative refractive index.) Artificial materials thus gain their electromagnetic properties from their structure rather than directly from their composites. In this thesis, we adopt this narrow meaning of artificial materials.

It is well known that the response of a system to an electromagnetic excitation is strongly dependent on the properties of the materials involved. Normally, we use the macroscopically defined parameters of permittivity and permeability to characterize materials under an electromagnetic field. In an ordinary material, the permittivity and permeability per se originate from the induced electric and magnetic dipole moment at the atomic level respectively by an external electromagnetic field. These two parameters are in general frequency dependent. In artificial materials, well-designed microscopic structures, which could generate electric and/or magnetic dipole moment (such as metal spheres in a three dimensional lattice), are embedded in another natural material. Although these structures are generally much larger than the size of an atom, as long as the wavelength of the electromagnetic wave is far more than the dimension of the individual structure, the induced dipole moments behave very similar to their atomic counterpart. As a result, the artificial material globally can be viewed as a continuous medium with averaged (effective) permittivity and permeability. The microscopic structures are easily realized by today's micro-fabrication technologies. The essence of artificial materials is to ignore the detail of electric and magnetic field distribution of the individual elements, but to consider the system as a continuous medium under electromagnetic field.

The first attempt of artificial materials may date back to the late nineteenth century [59]. The artificial materials today are widely investigated for a large frequency range, from radio-frequency to visible light, and can be roughly categorized according to their response to incident electromagnetic field as artificial dielectrics and artificial magnetics. Some artificial media, such as the so-called “double negative (DNG)” metamaterials (also the terms of “left-handed”, “negative refraction index” and “backward-wave” media are commonly used for this kind of metamaterials), are both artificial dielectrics and artificial magnetics, this is because both the macroscopic permittivity and the permeability of these composites are originated from the structures rather than from the materials [39]. Furthermore, since the microscopic elements introduced as metallic spheres normally generate both electric and magnetic dipole moments under high frequency electromagnetic field, the differences between these two kinds of artificial materials are not stringent. Nevertheless, within a suitable frequency range, it is still valuable to make these distinctions to emphasize certain aspect of the artificial media in reaction to external electromagnetic field. Related to the scope of this thesis, only a short review of artificial dielectric is given below.

It is commonly recognized that Kock first developed artificial dielectrics in the late 1940s [39]. An artificial dielectric is physically a large scale model of a real dielectric. Normally, it consists of a large number of identical conducting elements periodically arranged in a three-dimensional or two-dimensional pattern within a host conventional dielectric. Under an electric field, the positive and negative charges within each single conducting obstacle displace with one another. Since the conducting obstacle is overall electrically neutral, the dominant part of the induced field by the displacement of the charges is a dipole field. Thus, each obstacle simulates the behaviors of an atom or a molecule in a natural dielectric and exhibits an electrical dipole moment [39].

Typical artificial dielectric structures include metallic spheres or disks in a three dimensional lattice, and metallic strips or rods in a two dimensional periodic pattern [39]. It should be noticed that, unless the metallic obstacles are of spherical shape and are embedded in a cubic or random lattice pattern, the induced polarization value is different for a fixed applied electric field in different directions. Thus artificial dielectrics in general are anisotropic.

Artificial dielectrics are extensively applied in microwave engineering. As for Kock’s work, the early period of the development of artificial dielectrics is for lens antenna

applications. Compared with a lens antenna using conventional dielectrics, a lens antenna based on artificial dielectrics offers the advantages of low cost and low weight [39]. In recent years, the DNG metamaterials have attracted attention of a wide audience. In a sense, a DNG metamaterial is an artificial dielectric as well as an artificial magnetic, showing both negative value of permittivity and permeability in a certain frequency range [59]. Recently, artificial dielectric resonator, composed of small metal strips and put in a waveguide type cavity, was proposed by Kubo's group [60]. A Q factor over 1000 and effective permittivity over 800 of the artificial dielectric resonator was demonstrated. On chip $\lambda/4$ transmission line resonator built on top of artificial dielectric was demonstrated by Huang et al., and was shown to substantially reduce the chip area occupied by the resonator because the high permittivity of the artificial dielectric and thus a short wavelength of the transmission line [61].

In this thesis, a new type of artificial dielectric structure is introduced. The building blocks are small metal squares embedded in conventional dielectrics. The structures can be easily realized by modern micro-fabrication technologies. We will show that an in plane effective dielectric constant of tens of thousands (could be called super high-k) can be achieved by the proposed structures. Applications of the artificial dielectric structure to on-chip microwave passives shield and on-chip high-Q resonator will be demonstrated.

1.4 Outline of the thesis

This thesis focuses on: firstly, tunable functionality of microwave passive components based on ferroelectric materials, including both the material preparation and possible device realization; and secondly, loss reduction of on-chip passive components with artificial dielectric structure. The contents of the thesis can be summarized as follows:

Chapter 2 describes chemical solution deposition (CSD) method for BST thin film preparation. The microstructure of deposited BST thin film is characterized by atomic force microscopy (AFM) and scanning electron microscopy (SEM). The dielectric constant as a function of applied voltage is obtained by C-V measurement of parallel plate capacitor. It also presents possible tunable device designs based on BST thin film. A device fabrication flow based on substrate transfer technology is proposed. Issues related to the device performance are analyzed.

Chapter 3 presents a new ferroelectric based varactor design by implementing nano-dot electrodes which is aimed to enhance the tunability of the varactor at relatively low bias

voltage. Theoretical studies of single dot varactor and nano-dot varactor arrays are carried out. It is shown that near the dot electrode, the electric field distribution is determined by the dot dimension rather than the ferroelectric material thickness. The large value of electric field adjacent to the dot gives rise the high tuning range.

Chapter 4 introduces a new artificial dielectric structure consisting of a conventional dielectric thin film sandwiched between two patterned metal layers. It is shown that substrate losses of on-chip microwave passive components, such as CPW transmission lines and spiral inductors, built on ordinary medium resistivity silicon substrate can be effectively reduced by the proposed structure. The artificial dielectric structure acts as an electric shield to substantially reduce undesired electric field penetrating into the conductive silicon substrate.

Chapter 5 presents a new design of on-chip artificial dielectric resonator coupled with a metallic ring. Simulations using effective media parameters of the artificial dielectric structure yield promising high Q on microwave substrate like glass and HRS. The artificial dielectric resonator is theoretically studied and experimentally verified, although the achieved Q is less than expected.

Chapter 6 provides a summary of conclusions of the presented research topics, along with a number of recommendations for future research.

Appendix A provides a short introduction of basic physics of ferroelectric phase transition.

Appendix B presents the flowchart for the fabrication of BST thin film based tunable devices used in this work.

Appendix C and D presents detail calculations and derivations which have not been included in the main text for brevity reasons.

Finally, **Appendix E** describes details of transmission line parameters extraction procedures.

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Chapter 2

Ferroelectric Materials for Integrated Tunable Microwave Components

2.1 Introduction

Electrically tunable microwave devices, such as varactors and phase shifters, are indispensable in modern microwave integrated circuits. Taking a multi-band, multi-mode transceiver as an example, simple adaptive blocks employing tunable components offer the advantages of compact size and low loss [1] in comparison with the traditional method of using parallel, non-adaptive circuit blocks. For next generation wireless communication systems to support high data transfer rates, the operating frequency is desired to rise to broadband channels at Ku-band (12-18 GHz), K-band (18-26 GHz) and even higher [2]. In spite of the progress in transistor technologies, no semiconductor varactors with high enough quality factor (Q-factor) and tunability are available for

frequency range higher than 10-20 GHz [3].

Due to the electric field dependence of the permittivity, ferroelectric (FE) materials have been proposed for tunable microwave devices over 40 years ago [4]. However, extensive research on FE devices is fairly recent [5]. In theory and practice, all forms of FE materials, bulks, thin films and thick films can be used in tunable microwave devices. Particularly, FE thin films have attracted large amount of interests due to their broad tuning range, low tuning voltage, high breakdown voltage and especially low loss at microwave frequencies. Already thin-film based varactors with a Q-factor of ~40 at 45 GHz have been demonstrated [6]. Besides, cost effective deposition methods for FE thin film are readily available and the strong potential for integration into existing IC processes make it a competitive candidate for high frequency applications.

Even though FE materials in ferroelectric phase can not be completely ruled out for microwave applications, it is commonly believed that only in the paraelectric phase the desired properties of high tunability and low loss can be achieved simultaneously [5]. Moreover, it has been verified that only near the Curie point does a FE material show highest tunability [5]. Therefore, it is desired that FE material has a Curie point T_c slightly below the normal operating temperature, *i.e.* at room temperature. Among the various FE materials, Barium Strontium Titianate (BST) is the most widely investigated one for tunable microwave applications [7]. BST is a solid solution of $BaTiO_3$ and $SrTiO_3$ and is commonly denoted as $Ba_xSr_{1-x}TiO_3$, where x represents the relative concentration of the two composites. By the formation of the solid solution, the Curie point can be shifted to any value between about 400K (T_c of $BaTiO_3$) and 105K (T_c of $SrTiO_3$), depending on the x value [5]. As an example, $Ba_{0.7}Sr_{0.3}TiO_3$ (x=0.7) bulk ceramic undergoes a paraelectric-ferroelectric phase transition near room temperature. Although in contrast to its bulk form, BST thin film shows much lower permittivity due to fine grain size, interfacial capacitance and residual stress [8], reasonable tunning range and dielectric loss suitable for microwave tunable applications can still be realized.

In this chapter, different techniques for BST thin film deposition are discussed and compared. Chemical solution deposition (CSD) method is chosen for preparation of BST thin film in the lab facilities of Delft Institute of Microsystems and Nanoelectronics (DIMES). Results for structural and electrical characterization of deposited films are given.

From the device point of view, ferroelectric thin-film based tunable components are

widely investigated for a variety of applications in microwave (sub-)circuits, such as phase shifters [9,10], tunable filters [11], matching networks [12] and voltage controlled oscillators (VCO) [13]. The tunable components roughly fall into two categories: lumped elements like varacors and distributed components such as tunable transmission lines (this classification depends on the wavelength of electromagnetic waves compared to the device dimensions). In both cases, either a parallel-plate or a planar structure can be adopted for fabrication of tunable devices.

Planar configurations, like finger print varactors and coplanar waveguide (CPW) transmission lines, with both electrodes on the top of the ferroelectric film are easy to fabricate, but at a disadvantage. The electric field in a planar device is applied over lateral distances of the order of microns [14]. The dc bias voltage required for changing the dielectric constant of the ferroelectric film (and, thus, the electric characteristics of the device) should now be applied over such distances. Given the dc fields required for a significant modification of the dielectric constant of typical ferroelectric materials (tens of V/μm in the case of BST thin film), relatively high dc voltages (hundreds or even thousands of Volt) are needed to realize a reasonable tuning range.

On the other hand, tunable components using ferroelectric thin films in a parallel-plate configuration offer low tuning voltages since the voltage is now applied over the small thickness of the ferroelectric layer, inducing high electric fields (as shown in Fig.3.1). However, the on-chip integration of parallel-plate ferroelectric devices faces a major difficulty: in order to be able to grow ferroelectric films of microwave quality on top of the bottom electrode, the latter should satisfy stringent requirements. Proper crystal growth of the ferroelectric film requires small lattice mismatch as well as small thermal expansion coefficient mismatch between the ferroelectric and the underlying metallic electrode. Besides, the electrode should withstand the high temperatures required for the ferroelectric deposition and annealing. The integrated ferroelectric varactors reported so far mostly use Platinum (Pt) electrodes which satisfy these requirements. However, Pt is not compatible with a modern silicon (Si) integrated circuit (IC) process where Aluminum and Copper are the metals of choice.

In this chapter, substrate transfer technology (STT) is also proposed for the fabrication of BST thin film varactors and tunable microstrip transmission lines with parallel-plate configuration. The use of STT circumvents the restriction of Pt electrodes since the high temperature process step for BST deposition precedes the formation of the

two electrodes. In principle, based on STT, BST thin film can be deposited on any substrate as far as the whole or part of the substrate materials can be removed later. However, lattice mismatch and thermal expansion coefficient mismatch between BST and substrate should also be taken into consideration for choosing a substrate material. As a preliminary step, oxidized Si wafer was used as the substrate since due to the relatively mature STT process based on Si wafer. However, devices fabricated were found to be short circuited. Possible causes are investigated which indicating that BST deposition on silicon oxide is likely not a feasible solution. Comments on future works are finally given.

2.2 Chemical solution deposition of Barium Strontium Titanate (BST) thin film

A variety of deposition techniques for BST thin films, including pulsed laser deposition (PLD), RF sputtering, metalorganic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE) and chemical solution deposition (CSD), are available. A comparison of the advantages and limitations of these methods is given in Table 2.1.

CSD methods have been widely investigated for perovskite thin films since the mid-1980s, mainly aimed at FE thin films for electronic applications [17]. One major advantage of CSD methods over other deposition techniques is an easier stoichiometry control as different film compositions (Ba/Sr ratio in the case of BST deposition for example) can be readily achieved by changing the composition of starting chemicals. Besides, the compositional homogeneity of deposited film can be guaranteed by using an appropriate mixture of starting chemicals. Therefore, high quality samples with different compositions can be quickly tested in a cost effective way. In addition, the low investment capital makes it attractive not only for device fabrication but also for scientific research.

Conventionally, the morphology, or micro structure of BST thin films deposited by CSD method is a randomly oriented polycrystalline structure. However, the device performances (dielectric constant, tunability and loss) are generally considered to degrade from the grain boundaries in the film. Therefore, especially in the case of parallel plate tunable capacitors, the morphology control is normally regarded as a drawback of CSD method. Nevertheless, Hoffman and co-workers have shown that by controlling the precursor chemistry and deposition parameters, it is possible to change the microstructure

of BST thin films from a randomly oriented polycrystalline configuration to a columnar structure [18]. Based on these characteristics, we establish CSD method for BST thin film deposition by using the facilities of DIMES.

Normally, CSD deposition of BST thin film includes (1) precursor preparation, (2) film deposition and (3) pyrolysis and crystallization by high temperature annealing. The precursor preparation generally involves dissolving metalorganic compounds (typically metal alkoxide compounds) into a common solvent. The solution is then deposited on a substrate by spin coating. The as-deposited film is amorphous in nature and contains a significant organic fraction. To convert the amorphous film to a crystalline one, either the so called *two-step* or *one-step* pyrolysis and crystallization processes will follow. In the *two-step* case, the as-deposited film is subject to a separate pyrolysis step for bake out of the organic species, at relatively low temperature (normally 200-400 ºC), prior to a high temperature crystallization annealing. In the *one-step* method, the film is directly sent to a pre-heated furnace at crystallization temperature, which results in both organic pyrolysis and crystallization.

Based on works of Hoffmann [18] and Hasenkox [19], a process flow for $Ba_{0.7}Sr_{0.3}TiO_3$ is developed as sketched in Fig.2.1. The composition (Ba/Sr ratio) is chosen so that the Curie point is shifted to room temperature, where the film is believed to possess highest dielectric constant at zero bias voltage. Since the trend “the higher the dielectric constant, the higher the tunability” is observed in many dielectrics, highest value of dielectric constant is therefore favorable for microwave tunable applications [5]. The reason of choosing Ba acetate and Sr acetate as starting materials is the formation of an intermediate carbonate phase [18]. The acetylacetone (AcAc) is reacted with titanium-tetra-n-butoxide or $Ti(OBu)_4$ in Fig.2.1 to prevent the formation of nanosized TiO_2 particles in the solution, which will degrade the film performance [19]. The mixed starting materials are diluted to 0.1M in 2-methylpropionates (2MOE). A crystallization step is taken after every single spin coating which will result in a thickness of ~10 nm per layer. According to Hoffmann, it is the intermediate phase, suitable concentration of the final solution (resulting in thinner film per layer) and the crystallization strategy that produce a columnar structure of the final BST film, which is favorable for tunable devices with a metal-insulator-metal (MIM) structure like parallel plate varactors and microstrip transmission lines.

Table 2.1 Advantages and limitations of process techniques for BST thin film deposition [15,16]

Method	Advantages	Limitations
PLD	Rapid sampling of materials Quickly produce new materials Low temperature epitaxial growth	Morphology Point defect concentration Limited sample scale Uniformity High residual stress
RF Sputtering	Cost Uniformity Low temperature Scalability Standard IC processing	Point defect concentration Residual stress Stoichiometry control Slow deposition rate for oxide
MOCVD	Uniformity Morphology Composition control Low point defect concentration Scalability	Immature technology Precursor stability Precursor availability Expensive Down-time
MBE	Uniformity Composition control Precise atomic layering Extreme flexibility Scalability	Expensive Complexity Immature for oxide
CSD	Inexpensive, low capital investment Rapid sampling of materials Homogeneity Stoichiometry control Simple preparation route	Phase control Morphology Reproducibility

2.3 BST thin films characterization

2.3.1 Structural characterization

BST thin films are developed by CSD method following the aforementioned process flow

(Fig.2.1) on 100nmPt/20nmTi/SiO_2/Si substrate. Titanium is added for good adhesion between Pt and SiO_2. 40 nm-thick BST thin films, deposited by four coating-crystallization cycles, were investigated in a FEI XL30 scanning electron microscopy (SEM) to characterize the micro-structure during the film evolution. The SEM sample was coated by a thin gold layer to prevent charge accumulation during experiment. Atomic force microscopy (AFM) (NTEGRA, NT-MDT) operating at semi-contact mode was used to study the surface morphology and roughness of BST thin film after fifteen coating-crystallization cycles.

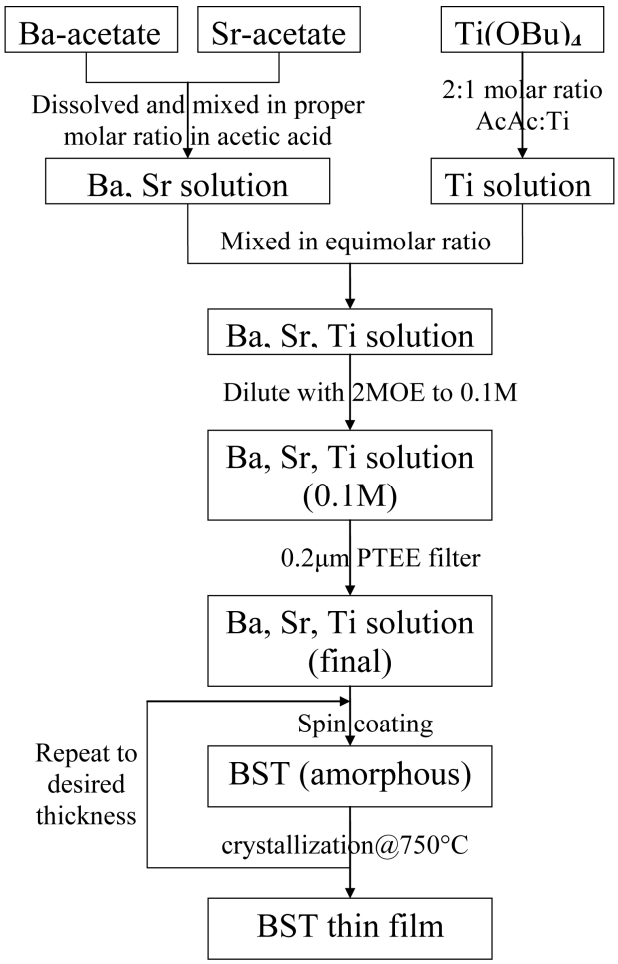

Figure 2.1: Process flow of BST thin film preparation by CSD method.

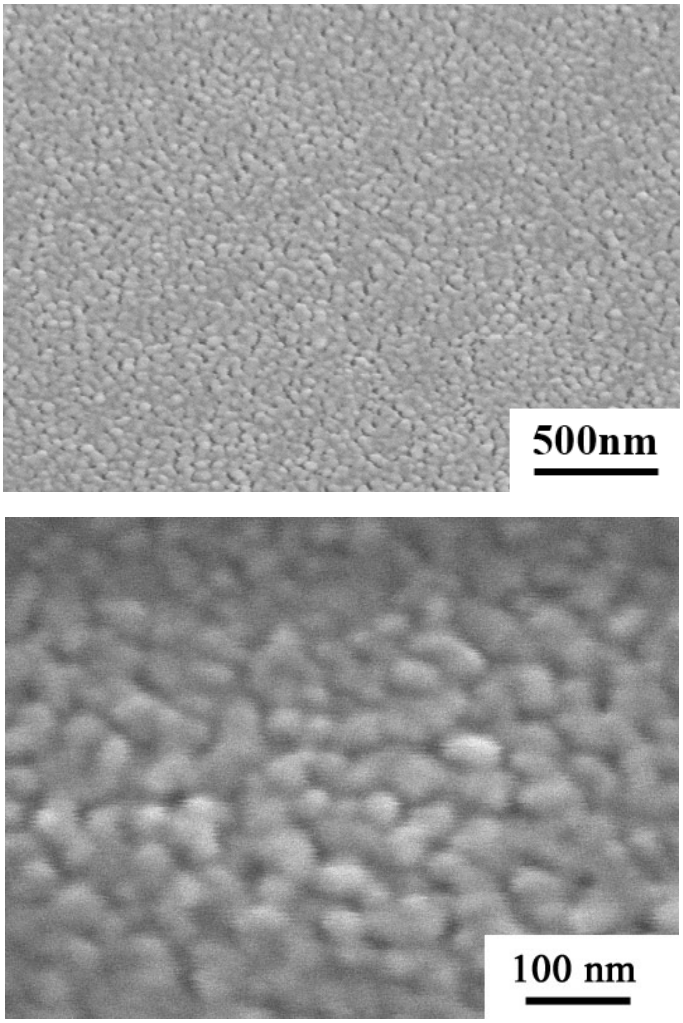

Figure 2.2: SEM images of ~40nm BST thin films by CSD method. The film is dense and without crack and fine grain size (30-50nm) is clearly demonstrated.

Fig.2.2 shows the SEM images of the 40 nm-thick BST films at different magnifications. The films are dense and crack-free with grain sizes in the 30-50 nm range.

In Fig.2.3, the AFM image of BST thin film after fifteen coating-crystallization cycles is shown. The thickness of the film is measured by Tencor alpha step surface profiler after patterning the film in 2.5%HF solution and is found to be 150±5 nm. Therefore, approximately a 10 nm layer is obtained for each coating-crystallization cycle. The films are again homogeneous and crack-free and the surface roughness is found from the AFM measurement to have a root mean square value of 0.96 nm.

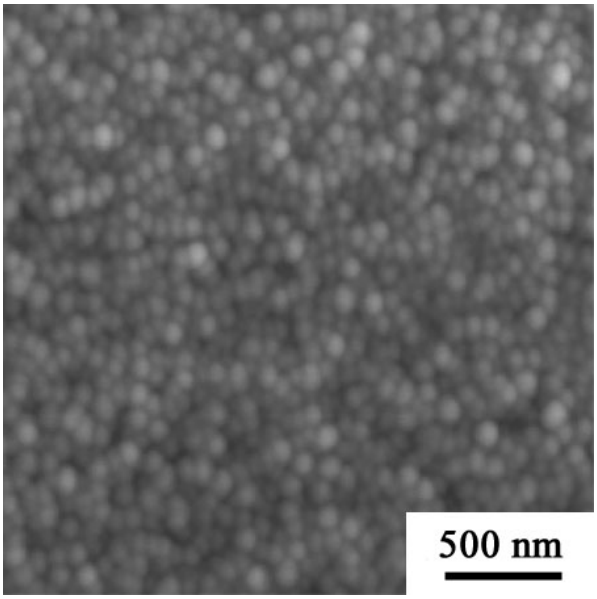

Figure 2.3: Surface morphology of 150 nm BST thin film by AFM. Smooth surface is identified.

2.3.2 Electrical characterization

To characterize the tunable properties of BST thin films, *i.e.* the dielectric constant as a function of applied bias voltage, parallel plate capacitors were fabricated for the 150 nm BST thin films on a platinized wafer. A Pt layer of 100 nm in thickness was used as the bottom electrode with 20 nm Ti film as adhesion layer between Pt and Si substrate. After the BST deposition, a layer of 1.4 μm Aluminum (Al) was sputtered on top of it. The Al layer was then patterned and etched to form the top electrode of the parallel-plate capacitor. (Fig.2.4).

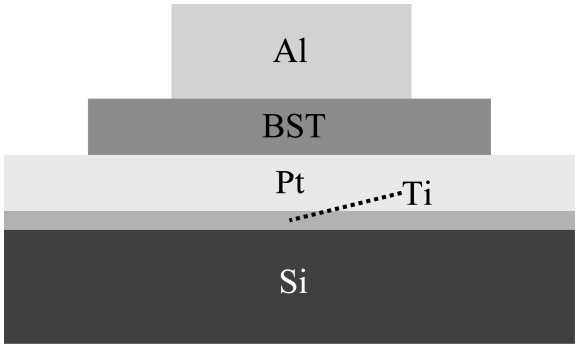

Figure 2.4: Cross section view of of Al/BST/Pt thin film varactor.

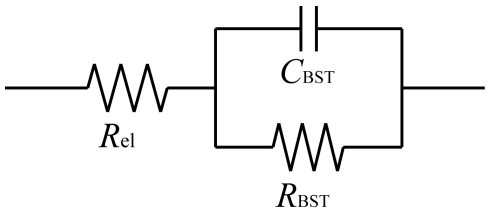

Figure 2.5: Equivalent circuit model of BST thin film capacitor.

Impedance measurements as a function of bias voltage at room temperature (25 ºC) and -30 ºC were performed with a HP4156A precision semiconductor parameter analyzer on a Cascade probing station equipped with a thermo-chuck at 1 MHz. An equivalent circuit model of BST parallel capacitor is developed and shown in Fig.2.5, in which R_{el} represents the resistances of the two electrodes as well as the contact resistance, R_{BST} models the losses of BST thin film capacitor due to dielectric loss and leaky current, and C_{BST} is the capacitance of the film. The values of R_{BST} and C_{BST} are calculated from the impedance measurement based on the equivalent circuit model by assuming R_{el} equals to 1.5 Ω.

Fig. 2.6 shows the capacitance density and the capacitor loss which is represented by the inverse of the device quality factor ($1/Q$). The capacitor is built using a 150 nm-thick BST film sandwiched between a bottom Pt electrode and a top Al electrode. The applied voltage is varied from -5 V to +5 V (bottom with respect to top electrode). The

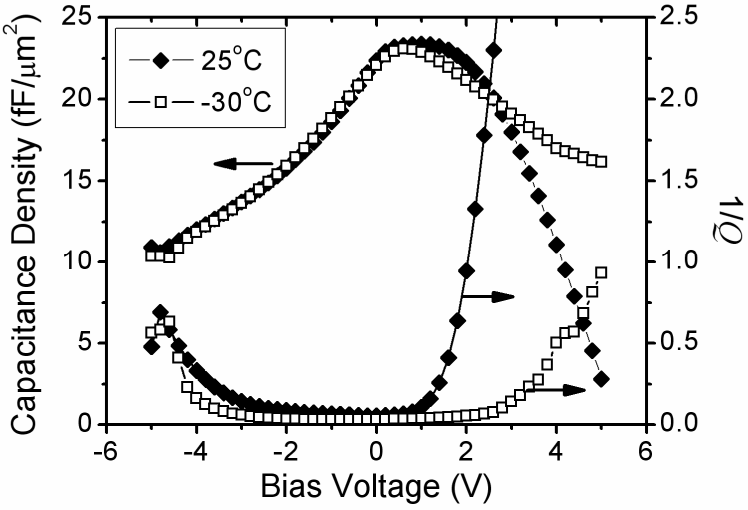

Figure 2.6: Capacitance density and capacitor losses of Al/BST/Pt thin film varactor as a function of applied bias voltage on Pt electrode.

measurements were carried out under two different temperatures: room temperature (25 °C) and -30 °C. From the figure, we can clearly identify the asymmetry of both capacitance and loss with respect to the bias voltage. Furthermore, the following observations can be made:

(1) At most negative bias voltages, the temperature does not affect the capacitance and quality factor of the capacitor. The effect of temperature at positive bias voltages, however, is significant.

(2) The maximum capacitance value at room temperature is obtained at bias voltage of 1 V instead of 0 V.

(3) The loss at negative bias voltage is relatively flat. It slightly increases with increasing the voltage.

(4) At positive bias voltage, the losses increase much faster with the applied (positive) voltage. This is especially significant at room temperature.

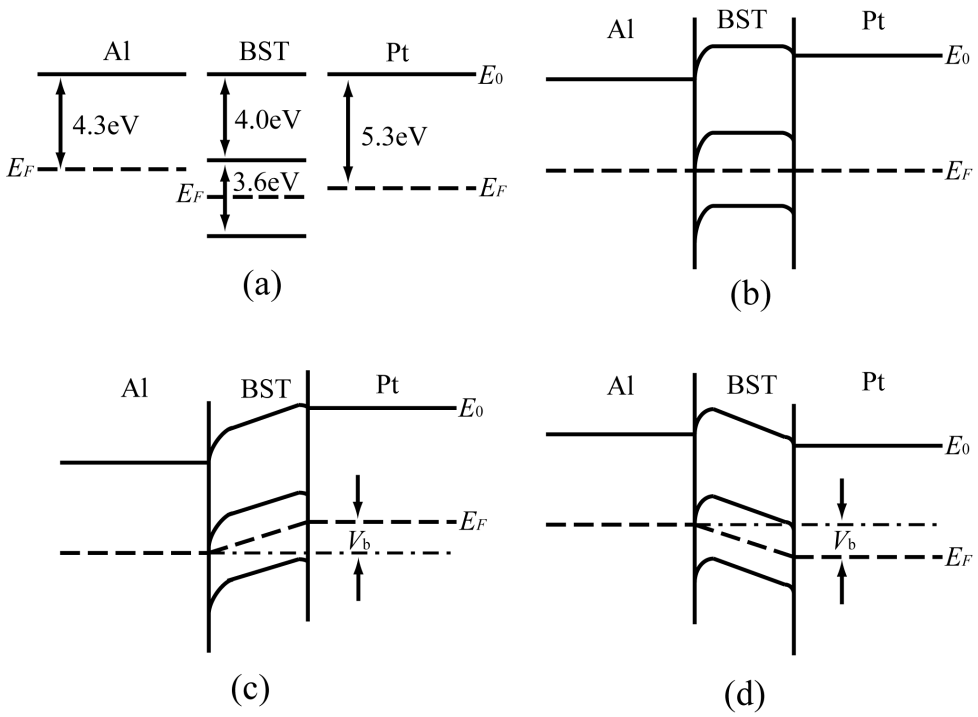

Figure 2.7: Band diagrams of Al/BST/Pt capacitor, (a) the work functions of Al and Pt, the electron affinity and band gap of BST; (b) band diagram of Al/BST/Pt when contacts are formed and equilibrium is established; (c) band diagram of Al/BST/Pt when negative bias voltage is applied at Pt; (d) band diagram of Al/BST/Pt when positive bias voltage is applied at Pt.

Note, that by increasing and then decreasing the bias voltage, no hysterisis was observed. Therefore, the film is in its paraelectric phase and the polarity behavior is not due to the possible formation of ferroelectric phase of the film. Thus, the observed asymmetry may be attributed to the different electrodes used (Pt vs. Al), and can be understood by the band structure of Al/BST/Pt layers which is shown in Fig.2.7. As shown in Fig.2.7 (a), Al and Pt have work functions of 4.3 eV [20] and 5.3 eV [21] respectively, while BST has an electron affinity of 4.0 eV and a band gap of 3.6 eV [21]. The Fermi level of BST is normally believed to be lightly above the center of the band gap [21]. When the three materials form the capacitor structure with zero bias voltage and thermal equilibrium is achieved, the Fermi levels of the three regions must be equalized.

As shown in Fig.2.7 (b), due to the small differences of the work function of Al and the electron affinity of BST, an ohmic contact is formed at the Al/BST interface. While in case of Pt/BST, a Schottky barrier is formed. Therefore space charge regions are developed in BST at both interfaces and an interfacial voltage (V_{int}) is built under zero bias. This voltage can be expressed as

$$V_{int} = V_{bi(Al/BST)} + V_{bi(BST/Pt)} = \frac{1}{e}(\phi_{Pt} - \phi_{Al}), \qquad (2.1)$$

where $V_{bi(Al/BST)}$ and $V_{bi(BST/Pt)}$ are the built-in voltage at the Al/BST and Pt/BST interfaces, respectively, and ϕ_{Pt} and ϕ_{Al} are work functions of Pt, respectively, Al [22]. Taking the values of $\phi_{Pt} = 5.3\text{eV}$ and $\phi_{Al} = 4.3\text{eV}$, the interfacial voltage is calculated to be 1.0 V, which is consistent with the measurement result, where the maximum value of the capacitance occurs when 1 V is applied on Pt electrode to annihilate the interfacial voltage V_{int}. When negative bias voltage is applied on Pt electrode, the energy band is bended as shown in Fig.2.7 (c), the leakage current is controlled by the Schottky barrier at Pt/BST interface. Therefore, the losses at low negative bias voltage are expected to be dominated by the dielectric loss due to the 1.4 eV potential barrier [20]. However, if the Pt electrode is positively biased, as shown in Fig.2.7 (d), much leakage current will flow due to the ohmic contact at the Al/BST interface. As the bias voltage increases, the potential barrier is reduced by the Schottky effect [23]. The thermally excited electrons will now easily overcome the potential barrier and flow across the BST film into the Pt electrode, resulting in a rapid growth of the capacitor loss at room temperature. At -30 °C, the concentration of thermally excited electrons is much less than that at room temperature, therefore the losses due to leakage current are lower as clearly exhibited in Fig.2.6.

The relative dielectric constant and the loss tangent of the BST thin film is extracted from the calculated R_{BST} and C_{BST} in Fig.2.5 for negative bias supplies, where the capacitor loss is mainly due to the dielectric loss of the BST thin film. Since the thickness of the film (150 nm) is much less than the device dimensions, the fringe field is safely ignored in the extraction of dielectric constant from capacitance value. The dielectric constant of 380 and loss tangent of 0.05 are obtained at zero bias, and a tunability of 2.05

is achieved with a bias voltage as low as 5 V for 150 nm BST thin film. However, compared to the results of Hoffmann [18], the dielectric constant is still lower and the dielectric loss higher than their reported values, which makes our prepared BST thin film not of sufficient quality for tunable microwave applications. One possible reason is the use of atmospheric ambient in the crystallization step where an oxygen ambient environment is preferred to reduce oxygen vacancies in the film. The quality of the solution precursor is another important factor determining the film properties. For example, the more particles in the precursor, the more defects in the deposited film. Extensive efforts are needed to determine the optimized conditions to prepare and purify the precursors. Furthermore, the possible contamination of the annealing environment, the wafer cleaning before each coating steps, the annealing strategies, etc. should also be taken into consideration to identify the optimal conditions to prepare BST thin films for making good quality devices.

2.4 Tunable components by substrate transfer technology (STT)

2.4.1 Introduction

As mentioned in Section 2.1, parallel-plate BST tunable devices normally require Pt as bottom and/or top electrodes. However, Pt is not IC compatible and is difficult to etch. Therefore, we propose an alternative method to fabricate parallel-plate components which utilize metals common in IC technology. The method is based on the substrate transfer technique (STT).

STT was first introduced by Dekker *et al.* in 1990's [24] for radio frequency (RF) circuit applications. The motivations behind STT are lower power consumption of the RF circuits, higher quality of passive components, and suppression of cross-talk between adjacent devices at RF frequencies [25]. STT achieves this by substituting the major part of the silicon substrate by a glass substrate. Already, low-power, highly integrated GPS receiver frontends [25] and high-performance varactor diodes [26] have been demonstrated using the STT. The bio-compatibility of glass has triggered new research on STT in integrated bio-electronic circuits [27], in addition to its (initially intended) RF application.

Essentially, STT consists of gluing the silicon wafer, face down, onto an alternative

substrate like glass. The process can be summarized as follows: First, active devices are fabricated on silicon wafer using ordinary silicon IC technologies. After that, both surfaces of silicon and glass substrate are treated with special primer to promote the adhesion between the substrate and glue. Then both substrates are glued together. The wafer sandwich is then cured by ultraviolet (UV) light. The silicon wafer is now partially or completely removed depending on the type of silicon substrate, bulk or silicon on isolator (SOI). After cleaning, the wafer is now ready for further processing, such as the formation of passive components and interconnects.

2.4.2 STT process for ferroelectric tunable components

The use of STT allows one to carry out the inevitable high temperature annealing in the deposition of BST thin films prior to the metallization of the film on both sides. As a result, IC compatible metals such as Al and Cu can be used to form electrodes or signal/ground layers of tunable devices. The process flowchart of fabrication of BST tunable microwave devices is designed (see Appendix B) and summarized in Fig.2.8.

The process starts with BST thin film deposition by CSD method on an oxidized Si substrate (step #1). Notice that the high temperature (750 °C) annealing is contained within this step. Step #2 involves patterning of BST thin film by 2.5% HF solution as well as the deposition and structuring of the first metal layer (Al is shown in the figure). This metal layer will serve, e.g., as the bottom electrode of the parallel-plate varactors and ground plane of microstrip transmission lines. The gluing of Si on the glass (Schott AF45 in this case) substrate followed by UV light curing is done in step #3. The Si substrate is then completely removed by wet etching in 33% Tetramethylammonium hydroxide (TMAOH) solution at 85 °C (step #4). Due to the high etching selectivity of SiO_2 over Si in the TMAOH solution, the etching will stop at the Si oxide layer. Finally, the Si oxide layer is patterned for contacting the BST film with the second metal to complete the device fabrication.

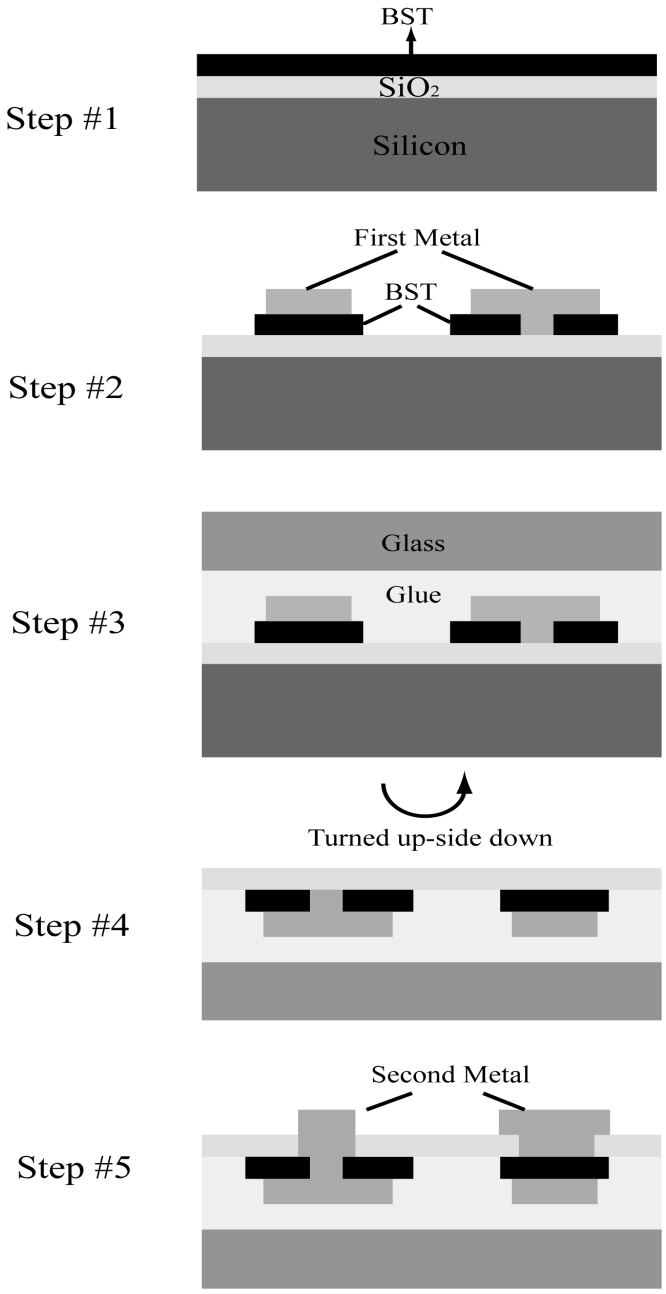

Figure 2.8 Sketch of STT process flow of ferroelectric tunable devices.

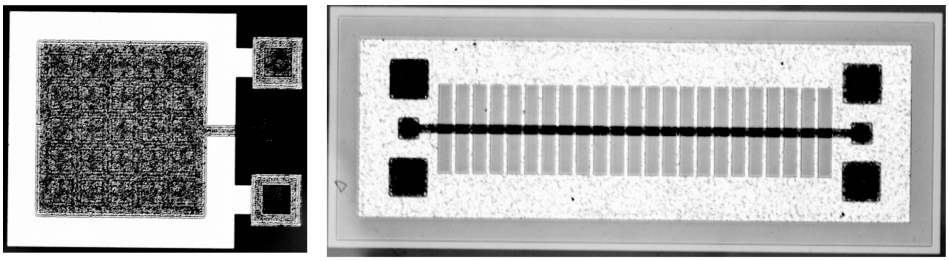

Figure 2.9: Micrographs of as-fabricated (a) parallel plate varactor and (b) microstrip transmission line.

2.5 Experimental results and discussions

Following the STT process flow described in the previous section, BST thin film tunable parallel-plate capacitors and microstrip transmission lines were fabricated at the DIMES cleanroom facilities. The thickness of BST thin film is 200 nm which is deposited by 20-fold repetition of the coating-crystallization cycles, as described section 2.2. Micrographs of fabricated tunable devices are shown in Fig.2.9. The ground plane of the microstrip is patterned to a defected ground structure to reduce the induced current flow in the ground layer, therefore to increase the inductance per unit length value (L')[28-30]. On the other hand, the capacitance per unit length value (C') is reduced due to the patterning of the ground since the overlap area of signal line and ground is apparently reduced by the patterning. Since the characteristic impedance of a transmission line (Z_0) is given by

$$Z_0 = \sqrt{\frac{L'}{C'}}, \tag{2.2}$$

Z_0 can be significantly increased by patterning of the ground, which overcomes one major drawback of microstrip configuration of transmission line with thin film between two metal layers, *i.e.* the very low characteristic impedance. Besides, by ignoring the dielectric loss (which is valid in most cases), the quality factor of the transmission line is

$$Q = \frac{\omega L'}{R}, \tag{2.3}$$

where ω is the angular frequency. It can be seen that, by patterning of the ground layer, the quality factor of the transmission line is also increased.

However, the electrical measurement of these devices showed that they were short circuited. Hence, we then analyzed the surface of the BST film (those potions which are open to the air after device fabrication) by AFM. Micro-cracks in the micrometer range, uniformly distributed over the whole BST film, were identified (Fig.2.10). Therefore, the two metal layers are in contact with each other through these micro cracks resulting in direct connection between two electrodes of the varactor or between the signal and ground lines of the microstrip line.

To trace the origin of the aforementioned micro cracks of the BST thin film, AFM was used to monitor the surface morphology of the deposited film after every three coating-crystallization cycles (Fig.2.11). Fig.2.11 (a-c) shows the AFM images of BST thin film after 3, 6 and 9 coating-crystallization cycles. Notice that in Fig.2.11c, bright line segments were observed. These segments form a network throughout the sample as revealed by a larger area scan (Fig.2.11d). The dimensions of the line segments were in the micron range, which were at the same level as the micro crack in Fig.2.10. The sample was then etched in 0.55% HF solution for one minute to partly remove a certain thickness of BST at the surface. AFM image (Fig.2.11e) then showed clearly micro cracks coincided with the position of the bright line segments.

From the AFM images of Fig.2.11, it can be seen that the micro cracks are formed at the SiO_2/BST interface. After each annealing step, the temperature of the wafer will drop from 750 ºC to room temperature before the next coating. Due to the large thermal expansion coefficient mismatch between SiO_2 ($5x10^{-7}$ K^{-1} [31]) and BST thin film ($7.8x10^{-6}$ K^{-1} [32]), the former and the latter will experience compressive and tensile stress respectively. If the thickness of BST thin film is higher than a critical value, cracks will originate at the interface between SiO_2 and BST to release the stresses. Although at the beginning, as in Fig.2.11a and Fig.2.11b, the cracks are not observable at surface, further experiments have shown that the micro cracks already exists in 40 nm thick BST thin film (with 4 coating-crystallization cycles). As a new BST layer is deposited on top of the existing ones, continuous film can be formed on the top, which is verified by Fig2.11c and Fig.2.11d, where only bright line segments instead of cracks are observed. However, the micro cracks underneath will grow and propagate. Therefore, after removing the top surface layer of BST by wet etching, micro cracks are exposed as can

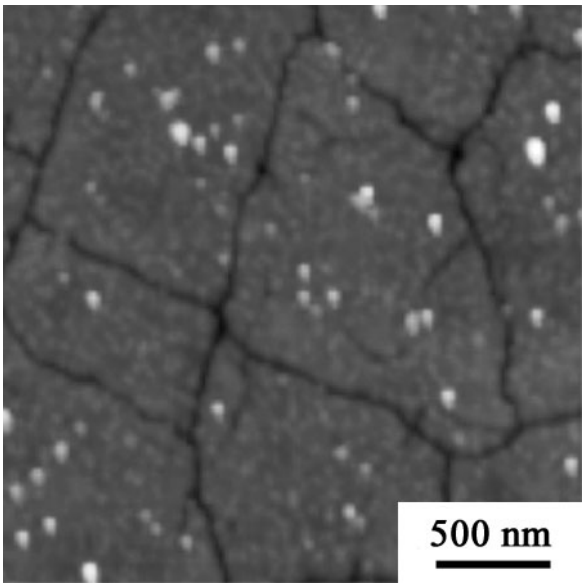

Figure 2.10: AFM image of BST thin film surface after STT processing shows micro cracks.

be seen in Fig2.11e.

As the process flow of Fig.2.8 shows, the SiO_2 layer is patterned after substrate transfer and Si removal in order to contact the BST film with the second metallic electrode. Micro-cracks at this moment are exposed to the air and have developed through the whole thickness of BST thin film during former processing steps (for example, the dry etching of SiO_2). Therefore, the second metal layer will directly contact with the first metal layer, leading to short circuited devices.

The above discussions assert that to realize BST-based tunable devices by STT processing, it is critical to obtain crack-free BST films of practical thickness. From this point of view, the use of SiO_2 as the buffer layer for BST deposition is not appropriate due to the large thermal expansion coefficient differences between the layers. To overcome this problem, a seed layer with small lattice and thermal expansion coefficient mismatch to BST is required to prevent the formation of cracks during the CSD processing steps. On the other hand, this seed layer must allow for selective etching with respect to the BST material in order to implement the second metal contact. Aluminium

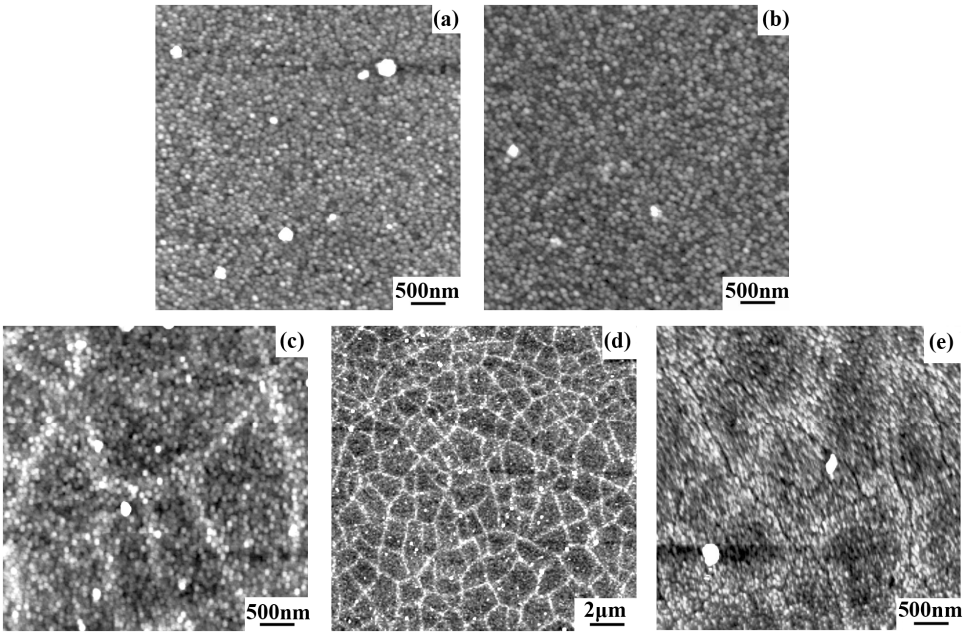

Figure 2.11: AFM images of surface morphologies of BST thin film after (a) 3 times, (b) 6 times, (c) 9 times coating-crystallization cycles; (d) large area scan of 9 layers shows network of bright line segments; (e) the line segments were identified to be micro-cracks after wet etching in 0.55HF solution.

oxide (Al_2O_3) and titanium oxide (TiO_2) are possible candidates, while further experiments are necessary for verification.

It is worth mentioning that the essential idea of STT could also be applied to substrates other than Si. Normally, high quality ferroelectric thin films, such as BST, are grown epitaxially on substrates like MgO and $LaAlO_3$ (LAO) [33]. By virtue of STT, the substrate (MgO or LAO) can be removed if a suitable etchant is found. After processing the top surface of the epitaxial ferroelectric material (e.g. deposition and patterning of the top metal layer) the whole wafer can again be glued onto glass, the substrate can be removed, and the second metallic electrode can be implemented. In this way, high quality ferroelectric thin films can be included in IC-compatible glass (or even Si) processes.

2.6 Conclusions

In summary, crack-free and smooth surface BST thin films have been successfully prepared by CSD method on platinum coated silicon substrates. Tunable parallel plate capacitors with Al/BST/Pt structure were fabricated and characterized by impedance measurement at 1 MHz. The measured asymmetric characteristics of both capacitance and loss with respect to the bias voltage applied between the Pt and Al electrodes is attributed to the formation of an ohmic contact and a Schottky barrier at the Al/BST and Pt/BST interfaces, respectively. A dielectric constant of 380 at zero bias voltage, and a tuning range of 2.05 at only 5 V were observed for the BST thin film.

Besides, ferroelectric thin film tunable microwave devices in parallel-plate configuration are proposed to be realized by substrate transfer technology to lift the stringent requirement on the metallic electrodes. Varactors and microstrip transmission lines with BST thin film sandwiched between two Al layers were fabricated using STT, starting from oxidized Si wafer. Unfortunately, the devices were found to be short circuited. This was casued by micro cracks originating from the SiO_2/BST interface due to the large thermal expansion mismatch.

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Chapter 3

Tunability Enhancement of Ferroelectric Varactors Using Nano-dot Electrodes

3.1 Introduction

In Chapter 2, we focused on the fabrication of parallel-plate varactors based on ferroelectric thin films. There, we proposed the substrate transfer technique to lift off the stringent requirement of Pt as the bottom electrode. Given the technological complexity of this process, a more conventional alternative would be to realize planar varactors with both electrodes on the top of the ferroelectric layer. The ferroelectric could then be grown on any suitable substrate and no restrictions would be imposed on the layer thickness.

The problem with this apparently straightforward solution is that, in a conventional IC process, the lateral distance between coplanar metallic electrodes cannot be made very small due to technological restrictions. These include the lithography resolution as well as

the high aspect ratio involved in etching steps. By contrast, in a parallel-plate varactor this distance is essentially the thickness of the ferroelectric film which may be as small as several nano-meters. Besides, the electric field distribution in a coplanar capacitor is essentially different from that of a parallel-plate device. As a result, compared to parallel-plate varactors, a coplanar varactor requires a high dc voltage to realize reasonable tuning range. A similar issue hinders the integration of tunable microwave components utilizing thick ferroelectric films [1-3]. While tunable resonators and phased-array antennas have already been demonstrated using thick ferroelectric single crystals and ceramics [3,5], these components require very high voltages, of the order of hundreds of volts to tens of kilovolts, for effective tuning.

To address this issue, in this chapter, we propose and theoretically investigate planar ferroelectric varactors and thick-film devices based on nano-dot metallic contacts. The key idea here is that, for any given voltage, the intensity of the electric field surrounding a metallic electrode is dictated by its dimensions if they are small compared to the ferroelectric film thickness or inter-electrode separation. For sub-micron sized electrodes this electric field can become very large and, since the dielectric constant of the ferroelectric is a function of the field intensity, high degrees of tunability can be achieved. This is in sharp contrast with typical parallel-plate configurations where the electric field and, thus, tunability, is governed by the film thickness. The method proposed can potentially be applied to all ferroelectric materials. It is worth mentioning that the recent literature on integrated ferroelectric devices is mostly focused on the optimization of ferroelectric material aspects, while mush less attention has been paid to the role of the device structure [6].

Using realistic material parameters, we will calculate the tuning range of planar nano-dot varactors as function of dot size and film thickness. We show that devices built from electrodes with diameters below 100 nm can exhibit a higher than two-fold change of capacitance under application of relatively low DC bias voltages (<10 V) even when thick ferroelectric films (>5 μm) are used. Since the capacitance of an individual nano-scale device is usually too small for realistic applications, we extend our analysis to arrays of nano-dots, and investigate the effects of dot size and separation on the overall tunability of the device. We show that below a critical inter-dot separation the enhanced tuning is washed out as the electric field profile starts to resemble the parallel-plate case. Furthermore, in designing the arrays, care has to be taken as to how the individual dots

are contacted with each other. The metallic pad connecting the dots should not be placed too close to the ferroelectric film, but should be separated from the latter by a conventional dielectric film with a thickness exceeding the diameter of each dot.

3.2 Basic principles of the ferroelectric nano-dot varactor

In characterizing the behavior of ferroelectric materials, tunability (also called tuning factor) is a commonly used parameter, which is defined as the ratio of the permittivity of the ferroelectric material at zero electric field to its permittivity at a finite field value,

$$n = \frac{\varepsilon(0)}{\varepsilon(E_0)}. \tag{3.1}$$

For a linear medium this ratio would be simply equal to unity. Thus, the tunability of a ferroelectric material originates from the non-linear relationship between the applied electric field and the polarization density. However, from a more practical viewpoint, a different definition of tunability for a varactor can be given in terms of the ratio of the capacitance at zero voltage to the capacitance at some nonzero voltage:

$$n_c = \frac{C(0)}{C(V_0)}. \tag{3.2}$$

For a parallel plate capacitor, if the fringe field effects are ignored, n and n_c have the same value since the electric field is constant and simply proportional to the voltage. In other configurations, such as the coplanar and interdigited capacitors, the field distribution is not necessarily linearly related to the applied voltage. In such applications, only the tunability of the capacitor (n_c) is of practical importance. However, one should bear in mind that it is the electric field which dictates the (local) value of the dielectric constant in the medium and, in the end, determines the tuning factor. It is the latter consideration which lies at the basis of the idea on using nano-dot electrodes: one may enhance the device tunability by dramatically increasing the electric field locally.

One possibility is to shrink the electrode(s) to sub-micron or even nanometer range (nano-dot contact). Fig.3.1 schematically shows a planar, nano-dot contact (NDC) ferroelectric varactor built from a metallic nano-dot (of radius R_d) and a much larger ground electrode placed above a ferroelectric/Si substrate. A conventional parallel-plate device has also been shown for comparison. Unlike the parallel-plate varactor, the distribution of the electric field in the NDC varactor is highly non-uniform. The electric

field is expected to be very high near the metallic dot, but to drop rapidly into the substrate, in analogy with the problem of a metal-semiconductor nano-junction [7,8]. Furthermore, the intensity of the field near the dot is expected to be mainly determined by the dot size rather than the thickness of the ferroelectric film, in sharp contrast with the parallel-plate configuration. The high intensity of the electric field near the dot contact lies at the basis of the high tunability of the proposed NDC varactor. Applying a relatively small dc bias voltage will cause a major change in the field-dependent dielectric constant of the ferroelectric material directly beneath the dot. Due to the high concentration of the electric field in this region, and the high dielectric constant of the ferroelectric, a significant change of the device capacitance can thus be achieved.

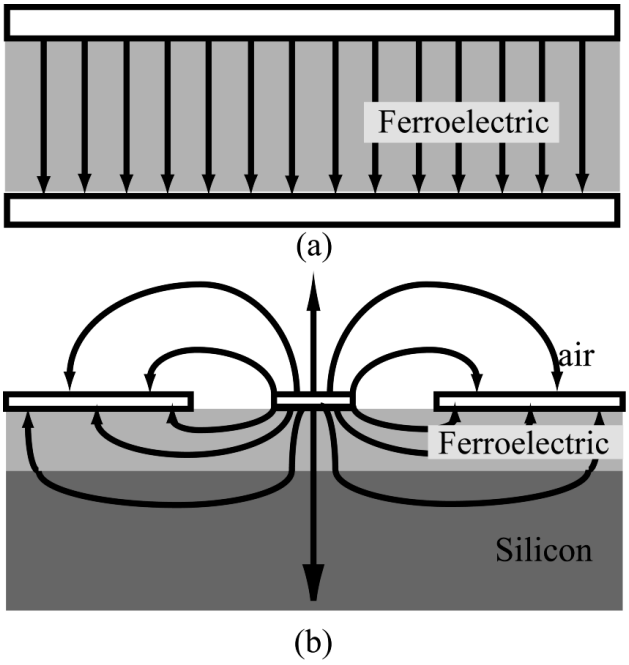

Figure 3.1 Schematic view of electric field distribution of a ferroelectric material based (a) parallel plate and (b) planar NDC varactor.

Because of the nonlinear relationship between the electric field and polarization inside a ferroelectric material, the use of numerical techniques is indispensable for an

exact analysis of the NDC varactor. However, by making a number of approximations, a semi-analytic model can be derived which offers a qualitative picture of the electric behavior of the NDC varactor. To derive the model we assume that the lateral separation between the dot contact and the ground electrode is much larger than the dot size. The varactor can then be viewed as the series connection of the two capacitances C_d and C_g, representing the self-capacitance of the dot and the ground contact, respectively (Fig.3.2a). Since the area of the ground electrode is taken to be much larger than that of the nano-dot, one has $C_g \gg C_d$ so that the overall varactor capacitance approximately equals C_d itself.

Next, we note that C_d is predominantly determined by the ferroelectric and Si layers because of their high relative dielectric constants. (The thickness of these layers is denoted by t_F and t_{Si}, respectively.) Neglecting the contribution of air above the substrate, one can now make the approximation $C_d \sim C_s / 2$ where C_s is the self capacitance of the same dot when sandwiched between the original substrate and a reversed, but identical substrate as shown in Fig.3.2b. Finally, C_s is approximated by mapping the system unto the spherically symmetric structure of Fig.3.2c, where the metallic dot is replaced by a metallic sphere with the same total area, i.e. with the radius $R_a = R_d / \sqrt{2}$, embedded in a sphere of ferroelectric material with the radius $R_b = R_a + t_F$ (Fig.3.2c), followed by a shell of Si material with the radius $R_c = R_b + t_{Si}$.

At not too high frequencies (<35 GHz, as long as the ferroelectric material does not show much dispersion [9]), electrostatic field analysis can be employed to compute the self capacitance of the structure of Fig.3.2c. Suppose that a total charge of Q resides on the metallic sphere. Employing the rotational symmetry of the structure, the electric displacement can be written as $\boldsymbol{D} = D_r \hat{\boldsymbol{r}}$, where $\hat{\boldsymbol{r}}$ is the unit vector in the radial direction, and

$$D_r(r) = \frac{Q}{4\pi r^2}, \tag{3.3}$$

with r is the radial distance from the center of the spherical system. Inside the ferroelectric region

$$\boldsymbol{D} = \varepsilon_0 \boldsymbol{E} + \boldsymbol{P}, \tag{3.4}$$

where ε_0 is the vacuum dielectric constant, $\boldsymbol{E}$ is the electric field, and $\boldsymbol{P}$ is the polarization density which is a nonlinear function of $\boldsymbol{E}$, most simply described by a power series expansion of the free energy in terms of $\boldsymbol{P}$ (the order parameter) [10]. For tunable microwave applications, ferroelectric materials of the displacive type in their paraelectric phase are commonly considered since it is believed that only for this case, both high tunability and a relatively low loss can be achieved.6 Following the Landau-Ginzburg-Devonshire (LGD) theory [11], if a homogeneous and isotropic ferroelectric material is assumed for simplicity, the non-linear *P-E* relationship can be expressed by the equation

$$\boldsymbol{E} = \alpha \boldsymbol{P} + \beta P^2 \boldsymbol{P}, \tag{3.5}$$

where $\alpha = (\varepsilon_0 \chi_f)^{-1}$ with χ_f the zero-field susceptibility of the material, β is a (positive) dielectric stiffness constant, and $P^2 = \boldsymbol{P} \cdot \boldsymbol{P}$.

Because of the isotropic nature of Eq. (3.5), and the spherical symmetry of the structure, the polarization density only has a radial component, i.e., $\boldsymbol{P} = P_r \hat{\boldsymbol{r}}$, which is given by the implicit equation

$$\left(\varepsilon_f / \chi_f\right) P_r + \varepsilon_0 \beta P_r^3 = \frac{Q}{4\pi r^2}, \tag{3.6}$$

as can be seen from Eqs. (3.3)-(3.5). Here $\varepsilon_f = 1 + \chi_f$ is the zero-field relative dielectric constant of the ferroelectric material. Using the same equations, the electrostatic potential of the metallic sphere (with respect to the infinity) can now be written as

$$V = \int_{R_a}^{\infty} E_r(r) dr = \frac{Q}{C_0} + \frac{\chi_f \beta}{\varepsilon_f} \int_{R_a}^{R_b} P_r^3(r) dr \tag{3.7}$$

$$\frac{1}{C_0}=\frac{1}{4\pi\varepsilon_0}\left[\frac{1}{\varepsilon_f}\left(\frac{1}{R_a}-\frac{1}{R_b}\right)+\frac{1}{\varepsilon_{Si}}\left(\frac{1}{R_b}-\frac{1}{R_c}\right)+\frac{1}{R_c}\right], \tag{3.8}$$

where E_r is the radial component of the electric field. To arrive at this result we have used the fact that inside the Si and air layers $D_r=\varepsilon_0\varepsilon_{Si}E_r$ and $D_r=\varepsilon_0 E_r$, respectively, with ε_{Si} the relative dielectric constant of Si. Note that C_0 is the zero-field self-capacitance of the structure, i.e., when the nonlinear term in Eq. (3.5) becomes negligibly small.

To further develop the right hand side of Eq. (3.7), we change the integration variable from r to P_r, apply partial integration, and use Eq. (3.3) to arrive at

$$V(Q)=\frac{Q}{C_0}+\frac{\chi_f\beta}{\varepsilon_f}\left[P_b^3(Q)R_b-P_a^3(Q)R_a\right]+2I(Q)\sqrt{Q} \tag{3.9}$$

$$I(Q)=\frac{3}{4\varepsilon_0}\sqrt{\frac{\chi_f P_0}{\varepsilon_f\pi}}\int_{P_b(Q)/P_0}^{P_a(Q)/P_0}\frac{u^{3/2}du}{\sqrt{1+u^2}}. \tag{3.10}$$

Here $P_0=\sqrt{\varepsilon_f/(\varepsilon_0\beta\chi_f)}$, and $P_a(Q)=P_r(R_a,Q)$, $P_b(Q)=P_r(R_b,Q)$ are found by solving (3) for the charge Q. The self-capacitance of the sphere for a given total charge can now be computed as

$$\frac{1}{C_s(Q)}=\frac{dV}{dQ}=\frac{1}{C_0}+\frac{I(Q)}{\sqrt{Q}}. \tag{3.11}$$

Note that from Eq. (3.7) Q can be found as function of the voltage V which, subsequently, can be used to determine C_s from Eq. (3.11).

Returning to the NDC varactor with the capacitance $C\sim C_d$, and keeping in mind that $C_d\sim C_s/2$, the overall capacitance as function of the applied bias voltage V can be expressed as

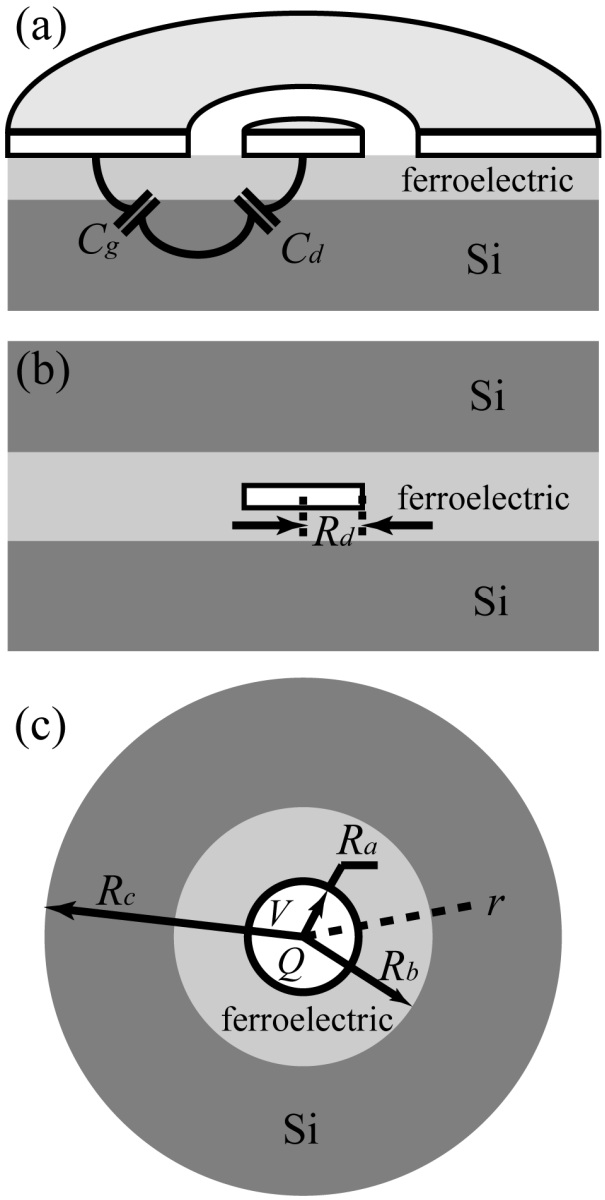

Figure 3.2: (a) Schematic view and simplified equivalent lumped element model of a planar NDC varactor; (b) Self capacitance of the NDC varactor is simplified to a system with a dot sandwiched between two identical ferroelectric/silicon substrate; (c) The system in (b) is further mapped to a spherical model for semi-analytical analysis.

$$\frac{1}{C(V)} = 2\left\{\frac{1}{C_0} + \frac{I[Q(V)]}{\sqrt{Q(V)}}\right\}, \tag{3.12}$$

where we have neglected the voltage drop over the ground electrode. In the limit $V \to 0$ where the nonlinearity of the *E-P* relation become negligible, one has $C \to C_0 / 2$. Increasing *V* leads to an increase in the 2nd term on the right hand side of Eq. (3.12), resulting in a decease in *C*.

The normalized capacitance $C(V)/C(0)$ of the ferroelectric NDC varactor on a ferroelectric/Si substrate is shown in Fig.3.3a as function of voltage for various radii of the nano-dot contact. In the calculation, the constants α and β in Eq. (3.5) were chosen to be $\alpha = 2.4 \times 10^{10}$ cm/F and $\beta = 0.75 \times 10^{20}$ cm^5/C^{2}F from Acikel's work [11]. These values are typical for Barium Strontium Titanate (BST) film, the most widely investigated ferroelectric material for RF/microwave tunable applications. (The same values of α and β are assumed throughout the whole chapter.) The thickness of the ferroelectric film was 5 μm. As shown in Fig.3.3a, reducing the dot size results in a larger tuning factor [$C_0 / C(V)$] with the same applied bias voltage. With a dot radius below 75 nm, a tuning factor above 1.5 can be achieved by applying a voltage of merely 10 V. It is worth mentioning that a parallel plate varactor built using an identical ferroelectric film with the same thickness (5 μm) would require more than 100 V to achieve a tuning factor higher than 1.5.

Note, however, that the degree of tunability of a NDC varactor decreases with decreasing ferroelectric film thickness (Fig.3.3b). With a relatively thin ferroelectric film, the drop of the electric field surrounding the dot-contact mainly takes place inside the Si under-layer. The continuity of the electric displacement across the ferroelectric-Si interface, and the much higher dielectric constant of BST ferroelectric compared to Si (370 vs. 12 at zero field), leads to a high electric field in Si just below the interface. Thus, the overall capacitance of the structure becomes dominated by the Si region whose dielectric constant is independent of the applied dc bias field. To better clarify these results, in Fig.3.4 we have plotted the dependence of the capacitance and tuning factor of the varactor on the dot radius and ferroelectric film thickness for a given bias voltage of 10 V.

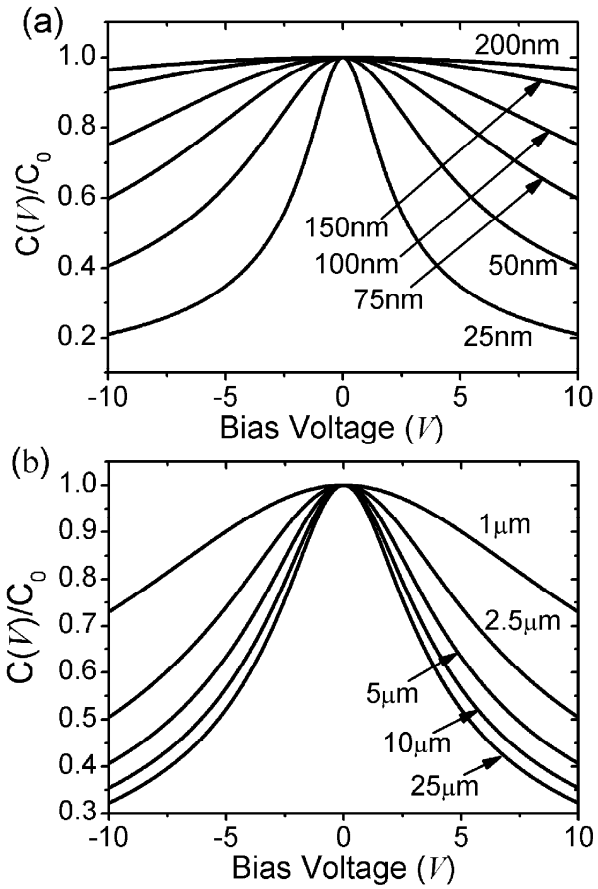

Figure 3.3: Calculated *C-V* curves of a planar NDC varactor: (a) as function of the dot radius (R_a) for a ferroelectric film thickness of 5 μm, and (b) as function of the ferroelectric film thickness (t_F) for a dot radius of 50nm.

At this stage it is also instructive to consider the case where a ground plane is placed below the ferroelectric layer. This situation is highly relevant for microwave devices such as tunable microstrip transmission lines and phased-array patch antennas which require a thick ferroelectric substrate on a metallic ground plane. In such cases the conventional parallel-plate configuration demands a very high bias voltage (several hundreds or even a few thousands volts) to gain effective tuning. By contrast, the use of nano-contacts will drastically reduce this voltage as shown in Fig.3.5. For the calculation we used the

approximation outlined above, but replaced the Si substrate by a perfect conductor. In effect, the same formula's can be applied except for the fact that the zero-field capacitance given by Eq. (3.8) should now be replaced by

$$\frac{1}{C_0} = \frac{1}{4\pi\varepsilon_0\varepsilon_f}\left(\frac{1}{R_a} - \frac{1}{R_b}\right). \tag{3.13}$$

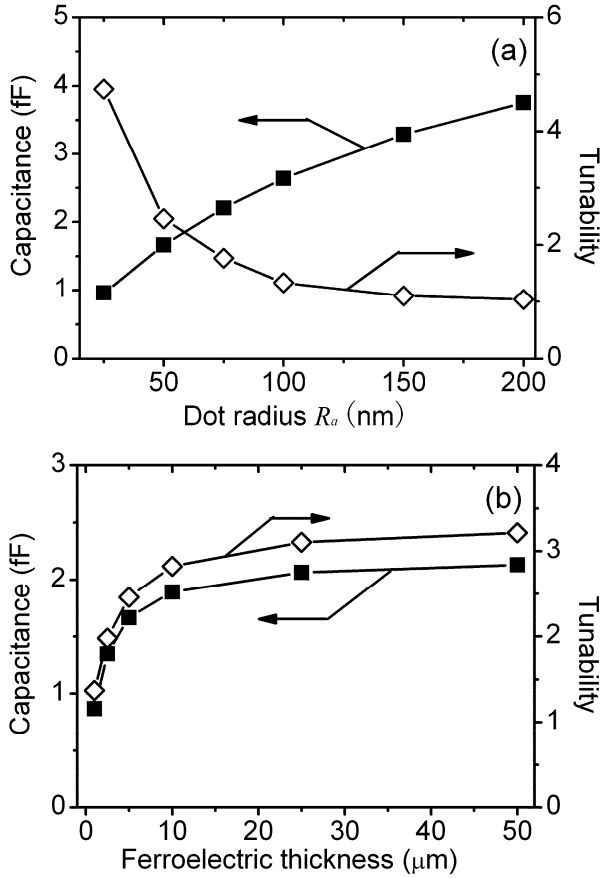

Figure 3.4: Calculated capacitance and tunability of a planar NDC varactor on silicon (a) as function of the dot radius (R_a) for a ferroelectric film thickness of 5 μm, and (b) as function of the ferroelectric film thickness (t_F) for a dot radius of 50 nm. The applied dc bias voltage was 10 V in both cases.

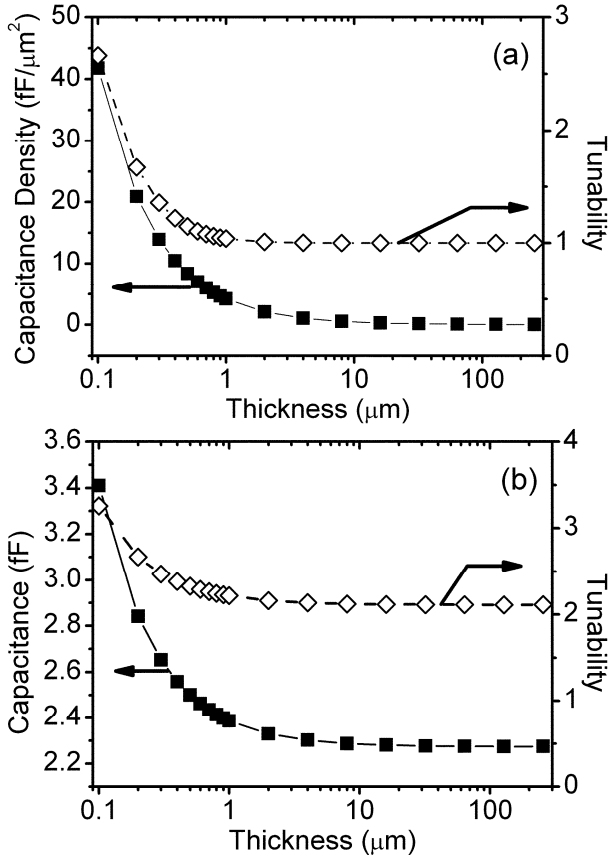

Figure 3.5: Calculated capacitance and tunability vs. ferroelectric material thickness for (a) a parallel plate capacitor and (b) a NDC capacitor built from a metallic dot (radius 50 nm) placed above a grounded ferroelectric layer. The applied dc bias voltage was 5 V in both cases.

As shown in Fig.3.5, with a nano-dot electrode with a radius of 50 nm, one can even reach a tuning factor higher than 2 at just 5 V, even on ferroelectric films with a thickness exceeding 50 μm.

It should be mentioned that the calculation presented above is not strictly rigorous since, due to the high electric field near the nano-dot electrode, higher order of polarization should be included in Eq.(3.5) according to LGD theory [10]. Nevertheless,

it is sufficient to illustrate the essential characteristics of the NDC varactor. For practical applications, however, one should bear in mind that the capacitance of a single NDC varactor is too small due to the latter's small radius (Fig.3.5). To achieve a sufficiently high capacitance while maintaining a high tunability, arrays of nano-contacts should be used, which is the subject of the next section.

3.3 Nano-dot varactor arrays

A realistic nano-dot varactor array is schematically shown in Fig.3.6. The ferroelectric film is covered by a conventional dielectric material such as SiO_2, which is perforated by an array of holes with diameters of the order of tens of nanometers. Once deposited on top of the dielectric, the metal layer directly contacts the ferroelectric film through these holes, forming nano-contacts. At the same time, the metal connects the individual nano-contacts together, forming a capacitor composed of the shunt connection of individual nano-dots. The second electrode of the capacitor may be built on the same layer (as in Fig.3.2a), or as a ground plane below the ferroelectric. In this section, we restrict ourselves to the latter case.

To analyze the capacitor array, we consider an infinite, 2D lattice of nano-dots in the x-z plane, and compute the capacitance per unit area of the structure. This assumption is justified if the number of dots in the array is large. The analysis can then be reduced to that of a unit cell containing a single dot, provided that appropriate boundary conditions on electric field are imposed on the vertical walls of the unit cell. For 2D lattices which are symmetric under reflections with respect to lines forming the boundary of a unit cell (e.g. triangular and square lattices), it can be shown that the normal component of the electric field should vanish on the boundary walls.

Let us now focus our attention on a triangular array of nano-dot varactors with a hexagonal unit cell (Fig.3.6a). To further simplify our calculations, a rotational symmetry with respect to the axis of one single dot is supposed. This is based on the fact that close to the dot, the field and potential almost preserve the rotational symmetry of the dot. As we see in the previous section, the capacitance is mainly determined by the field near the dot. Therefore, this approximation has little impact on the total capacitance results. Combined with the previous approximation, one ends up with a 2D problem which will

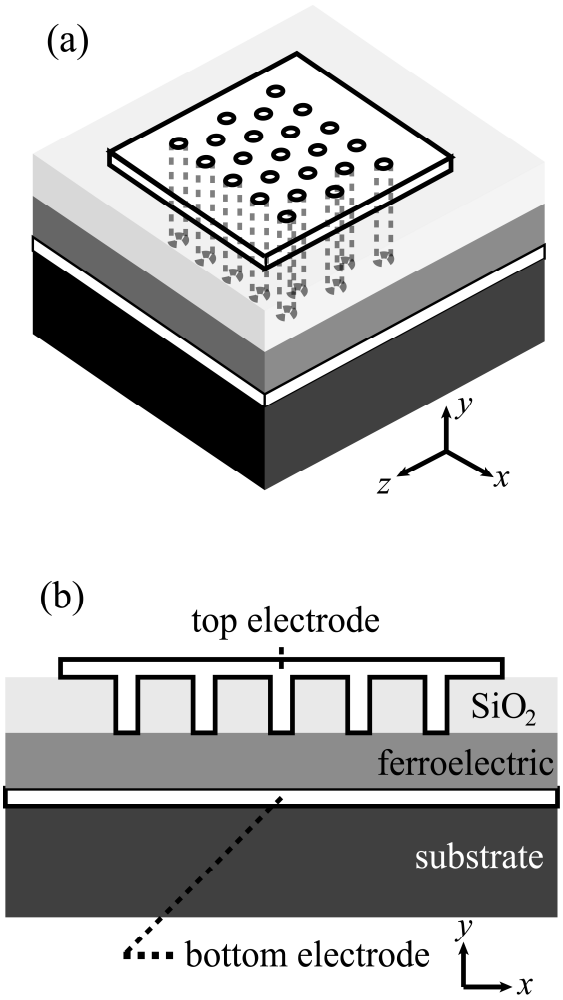

Figure 3.6: (a) 3D and (b) cross section view of arrayed NDC varactor.

be once again studied using the electrostatic approximation. The 2D geometry in consideration is sketched in Fig.3.7. Here, symmetry about the y-axis helps to further simplify the domain by half (only the right half is shown). As shown in Fig.3.7, the radius of the nano-dot is r, the thickness of ferroelectric film is t_F, the thickness of SiO2 is d, and the separation of two adjacent dots (center to center distance) is $2l$. For electrostatic problem, the electric field is usually expressed as the gradient of an electrostatic potential φ. During the calculation, a voltage $\varphi = V$ is applied to the top electrode, the bottom

electrode is kept at $\varphi = 0$. Zero Neumann boundary conditions for the potential, which implies the normal components of electric field along the boundary walls vanish, is applied to boundary walls (x=0, 0≤y≤t_F) and (x=l, 0≤y≤t_F+d) by symmetry consideration.

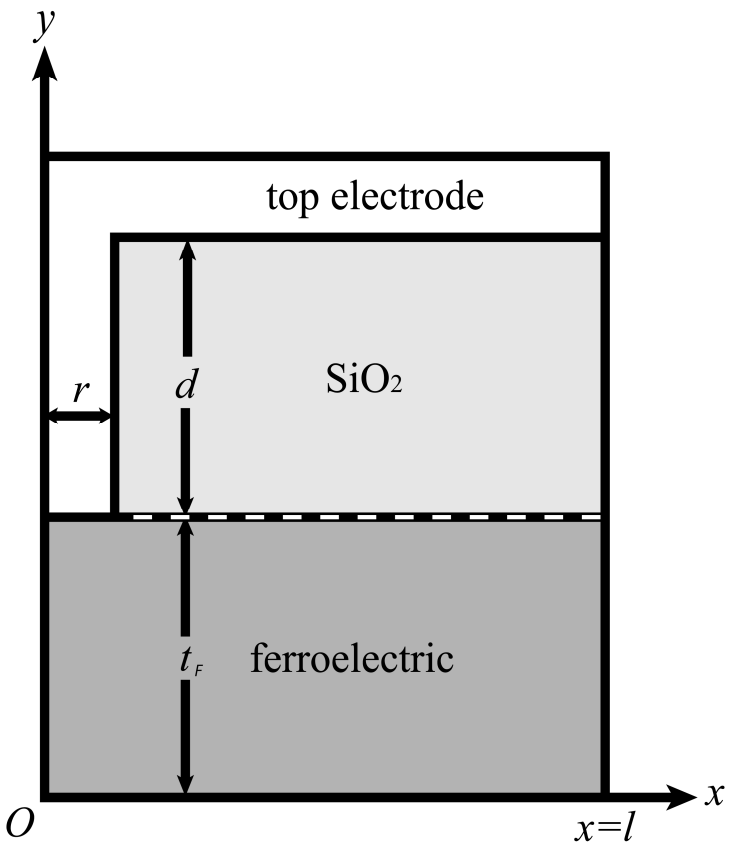

Figure 3.7: Cross section geometry of a unit cell (only right half is shown) of arrayed NDC varactor.

The Laplace equation

$$-\nabla\bullet(\varepsilon\,\nabla\varphi) = 0 \qquad (3.14)$$

is applied to both ferroelectric and SiO_2 regions. In SiO_2 region, the dielectric constant term ε is given by $\varepsilon_0\varepsilon_r$, where ε_0 is again the vacuum dielectric constant and ε_r is the relative dielectric constant of SiO_2, which is taken as 4. In ferroelectric region, we

define ε as a local, field-dependent dielectric constant which is given by

$$\varepsilon = \frac{|\boldsymbol{D}|}{|\boldsymbol{E}|} = \varepsilon_0 \left(1 + \frac{\varepsilon_f - 1}{1 + \varepsilon_0 \chi_f \beta P^2} \right). \tag{3.15}$$

Notice that ε is a function of electric field, thus a function of the potential. The electrostatic potential was solved iteratively using finite element method. At the beginning, the local dielectric constants in the ferroelectric region were assumed to be a constant value. The potential at every point is then solved based on this uniform dielectric constant value by Eq.3.14. Taking the gradient of the potential, electric field can be calculated. Using this electric field value and Eq.3.3, a new local dielectric constant can be derived by Eq.3.15. Substituting the new local dielectric constants into Eq.3.14, potential is again solved at every point. The whole procedures are repeated until the electrostatic potential converges to certain accuracy. A program was developed to carry out the calculation.

The total amount of charge Q_c for one unit cell is found by integration of the perpendicular component of the electric displacement $\boldsymbol{D}$ on the surface of the bottom electrode over its area A. The capacitance per unit cell is defined as

$$C(V) = (1/A)\left(dQ_c / dV\right), \tag{3.16}$$

which is evaluated using numerical differentiation. In what follows, we present the calculation results for the capacitance and tunability of a NDC array as function of the radius of the nano-dot electrodes, inter-dot separation (center to center distance), and thickness of the conventional dielectric layer (here SiO_2) separating the top global electrode from the ferroelectric. As in the previous section, we assume the ferroelectric to be BST. Since model calculations for a single NDC varactor show practically no change once the thickness of the (grounded) ferroelectric layer exceeds 1 μm (see Fig.3.5), the same value was used in the numerical simulations to reduce the computation time.

Fig.3.8 shows the calculated tuning factor at a bias voltage of 15 V, as a function of the dot radius (the calculated zero-bias capacitance density is also shown). The thickness of the SiO_2 layer and the separation between two neighboring dots were assumed to be d = 1 μm and $2l$ = 2 μm, respectively (see Fig.3.7). As shown in Fig.3.8, a tuning factor of 2.02 is obtained with a dot radius below 50 nm. In comparison, a parallel plate varactor with the same BST film thickness and applied bias voltage yields a value of 1.30. This

can be seen from Fig.3.8, as the limit $R_d \to l$ (l = 1 μm) corresponds to the parallel-plate case (Fig.3.7). Note also that the parallel-plate varactor exhibits an almost twice higher capacitance density compared to a NDC array composed of dots with a radius of 50 nm. The higher tunability is, therefore, obtained at the cost of a lower capacitance density. Nonetheless, in the majority of applications, varactors are intended for providing adjustability, not high capacitance.

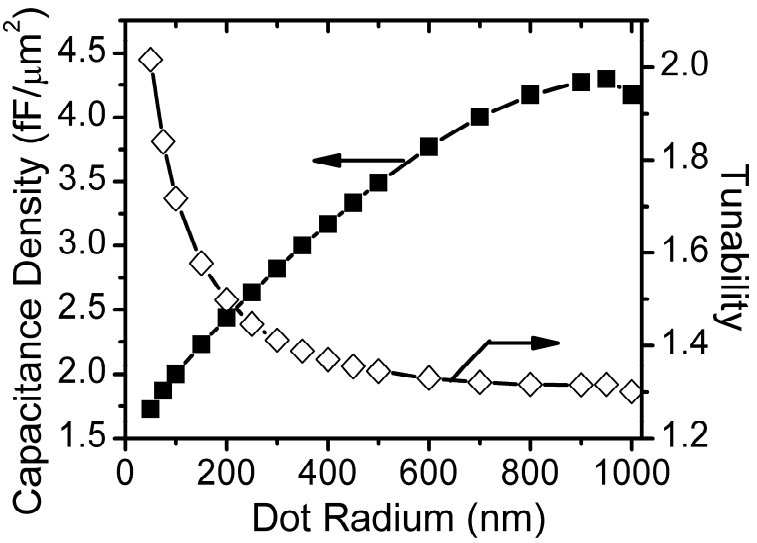

Figure 3.8: Calculated capacitance density (at zero voltage) and tuning factor (at 15 V) of a NDC array as function of dot radius. The BST and SiO_2 layers were both 1 μm-thick, and the inter-dot separation was $2l$ = 2 μm in the calculations. A curvature of 30 nm was assumed at the bottom corner of the metallic dot to prevent the electric field exceeding the break down field of the BST ferroelectric.

Figure 3.9 shows the dependence of the tuning factor (and zero-voltage capacitance density) of the NDC array on the inter-dot separation ($2l$). At small values of $2l$, when the dot-separation becomes comparable to the dot radius, the NDC array varactor behaves like a parallel-plate capacitor. This is because of the strong electric coupling between adjacent dots: the enhanced tuning is washed out as the electric field profile starts to

resemble the parallel-plate case. At sufficiently large separation, the inter-dot coupling becomes weak, and the tuning factor of the NDC array approaches that of a single dot.

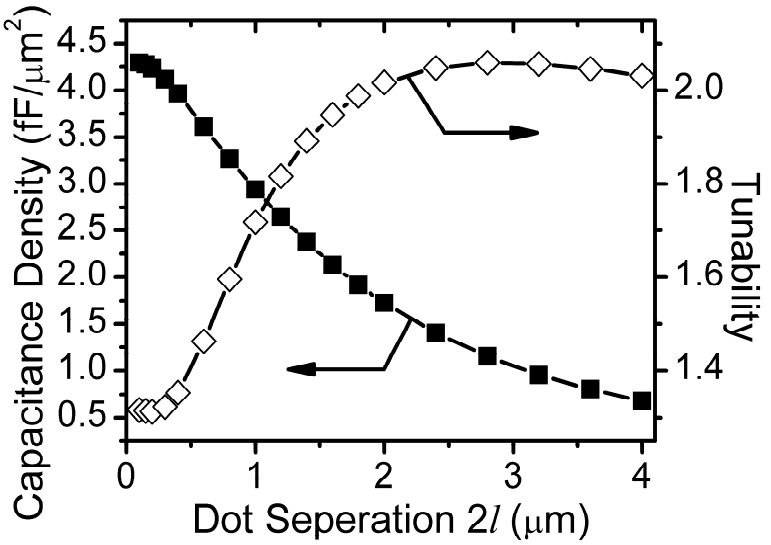

Figure 3.9: Calculated capacitance density (at zero voltage) and tuning factor (at 15V) of a NDC array as function of inter-dot separation. A BST and SiO_2 layer thickness of 1μm, and a dot radius of 50nm were assumed in the calculations.

Finally, consider the behavior of the NDC array as function of the thickness of the isolating SiO_2 layer, as shown in Fig.3.10. Reducing the SiO_2 layer thickness increases the capacitance density, but yields a lower tuning factor. This can again be understood in terms of the electric field distribution near the dot contact. When the SiO_2 layer is sufficiently thick, the electric field is mostly concentrated near the dot. This is because, away from the dot, the dc bias applied between the top electrode and the ground plane mostly drops over the SiO_2 layer due to the latter's much lower dielectric constant compared to that of the ferroelectric. The high concentration of the electric field near the dot contact ensures a high tuning factor as we saw before. However, decreasing the SiO_2 layer thickness leads to a more uniform field distribution since, now, a larger portion of the electric field reaches the ferroelectric. Eventually, in the limit where the SiO_2 layer thickness becomes zero, a parallel-plate field profile results.

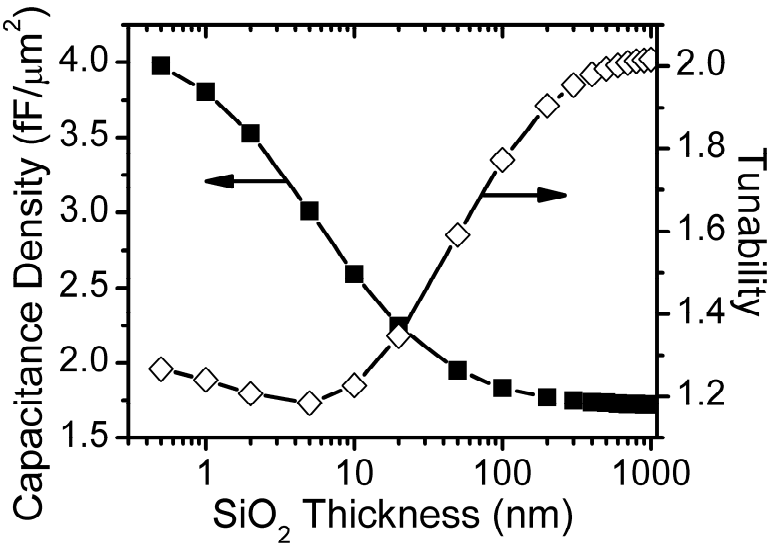

Figure 3.10: Calculated capacitance density (at zero voltage) and tuning factor (at 15 V) of a NDC array as function of the SiO_2 layer thickness. The BST layer was 1μm-thick, the dot radius was 50 nm, and the inter-dot separation was $2l$ = 2 μm in the calculations.

3.4 Discussion and conclusion

We proposed a method for increasing the tunability of ferroelectric varactors utilizing thick (>1 μm) ferroelectric films. The method was based on metallic nano-dot electrodes deposited on a ferroelectric layer. Using a semi-analytic model, it was found that the tuning factor of a single nano-dot varactor built on a thick BST layer can reach values higher than 2, even with a dc bias voltage as low as 5 V. To achieve sufficiently high capacitance density, we then considered arrays of nano-dot varactors and studied their behavior as function of the dot radius and separation, as well as the thickness of the isolating layer. It was found that the nano-dot array can maintain the high tuning factor of a single dot, provided that the inter-dot distance does not become too small.

While our focus has been on ferroelectric varactors, the application of nano-dot electrodes can be extended to other types of tunable microwave components utilizing

thick ferroelectric films. In particular, one can consider tunable transmission lines which form the basis of phase shifters and electrically adaptable filters. As an example, consider a microstrip line built on a thick, grounded ferroelectric substrate. By covering the ferroelectric with a conventional dielectric layer (e.g. SiO_2) perforated by an array of sub-micron holes and, subsequently, depositing the microstrip line, a highly tunable transmission line can be formed. The capacitance per unit length and tunability of such a microstrip can be calculated using the static field analysis method presented earlier at not too high frequencies (as far as a quasi-TEM approximation is valid). The detailed results are beyond the scope of this work and will not be presented here.

The proposed nano-dot varactor may offer another potential benefit in comparison with conventional devices. As is well known, one of the major sources of dielectric loss in a ferroelectric is the oxygen vacancies within the grain boundaries of the ferroelectric film [12]. Because the electric field rapidly drops away from the metallic nano-electrode, only a few grains are expected to be involved in determining the capacitance and loss of the device (BST thin film for example has a typical grain size of 60-70 nm). Therefore, lower loss can be expected from nano-dot capacitors and capacitor arrays. However, experiments are required to confirm this argument.

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Chapter 4

On-chip Passives with Artificial Dielectric Layer (ADL) Shields

4.1 Introduction

Transmission lines are extensively used in microwave circuits, not only as wave guiding structures to transfer signal power from one point to another, but also as passive elements used for processing the microwave signal. Examples are λ/4 transformers, transmission line resonators, power dividers, and filters [1].

Most people are familiar with coaxial transmission lines which have been widely applied in microwave systems. Over the past 40 years, the development of solid state circuits and IC technology has dramatically changed microwave engineering. With the availability of high quality microwave solid state transistors, the focus of wave guiding components has changed to planar transmission line structures, such as microstrip and coplanar waveguides (CPW). With the current trend and enormous focus on monolithic microwave integrated circuits (MMIC), development of high-quality on-chip planar

transmission lines has attracted much attention from the scientific and engineering community [2].

Nonetheless, monolithic integration of high-quality microwave transmission lines still remains a challenge due to performance degradation caused by losses in the underlying silicon (Si) substrate, the main vehicle of the contemporary radio-frequency integrated circuits (IC). It is the conductive nature of Si which allows the flow of electric conduction currents in the substrate in response to the electric field surrounding the transmission line conductors. In turn, the dissipation of microwave power brought about by these currents is manifested as a rise in the overall device loss [3-5].

To illustrate the substrate loss effects, the attenuation of typical CPW lines, with signal line width of 30 μm and signal to ground width of 30 μm, was simulated in a microwave simulator, Advanced Design System (ADS). Since our interest is the substrate loss effect, the metallic signal line and ground are assumed to be perfect metal in simulations. In Fig.4.1, the simulated substrate losses are shown as a function of frequency with different values of Si substrate resistivity. With lower substrate resistivity, the line shows higher substrate loss, especially at high frequencies. Although substrate loss can be suppressed by using insulating substrates [3], micromachining [4], and substrate transfer techniques [5], such methods involve modification of the core device integration process, leading to significantly higher fabrication costs.

Electric shields built from metal or poly-silicon layers offer an IC-compatible alternative. Inserted beneath the device, the shield blocks the electric field from entering the conductive Si substrate, preventing the flow of unwanted currents [6-8]. Already coplanar waveguide (CPW) transmission lines with shields built from floating metal strips perpendicular to the line have been demonstrated to have very low substrate loss [8]. However, the inherently large parasitic capacitance between the CPW and the conductive shield substantially reduces the line characteristic impedance. Consequently, shielded lines with high characteristic impedance require narrow signal lines or large signal to ground spacing, which increase the line attenuation or device area. For example, in Cheung's work [8], the signal line width of a shielded line is smaller than un-shielded line by a factor of 3, with the same values of signal to ground space and characteristic impedance. This is a crucial disadvantage in the implementation of resonant tanks, impedance matching networks and couplers, where a wide range of characteristic impedances (30-300 Ω) is required.

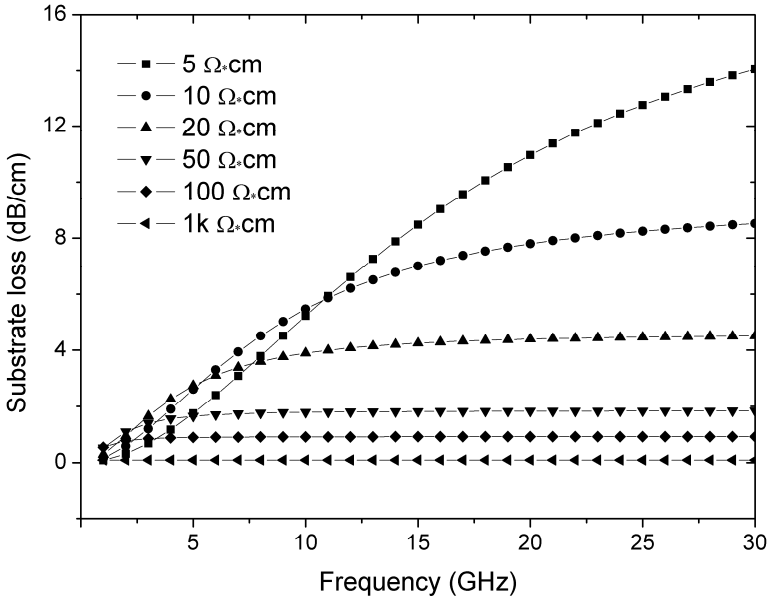

Figure 4.1: ADS Simulation results of CPW line attenuation as a function of frequency for different substrate resistivity.

In this chapter we describe a new IC-compatible shielding method for integrated CPW's utilizing an artificial dielectric layer (ADL) consisting of a conventional, thin dielectric film sandwiched between two patterned metal layers [9]. The ADL effectively behaves as a thin homogeneous dielectric with a very high dielectric constant. Using the concept of surface impedance, it can be shown that an ADL layer possesses a very high in-plane dielectric constant. This property of the ADL leads to the prevention of the electric field of the CPW from entering the Si substrate. Our experiments show the ADL shield to yield an up to three-fold reduction of the line attenuation below 30 GHz. Furthermore, the effect of the ADL on the characteristic impedance of the CPW is much smaller than that of conventional shields, allowing the realization of a broad range of characteristic impedances without the need for narrow signal lines or large signal-ground spacing. An additional benefit of the ADL, compared to conventional shielding structures, is the independence of its design of the individual CPW layout, simplifying the mask design and fabrication process [9].

Moreover, we will also show that the shielding effect can be further improved by

micro-patterning the shielding structures [10], i.e. the metal blocks used in ADL, or by using multi-layer ADLs. The former method is aimed at reducing the eddy current loss in the metal blocks which can contribute significantly to the total loss at high frequencies. The latter technique, one the other hand, is employed to increase both the effective dielectric constant and thickness of the ADL. Finally, we will investigate the application of the ADL shield to on-chip spiral inductors, another important and widely used microwave passive component.

In the next section, we describe the principle of shielding by a high-k (high dielectric constant) for integrated transmission lines on lossy substrates.

4.2 Integrated coplanar waveguide (CPW) transmission lines with ultra-high-k dielectric shields

The most widely used transmission lines in microwave IC technology are the microstrip line and the coplanar waveguide transmission line (CPW), which are schematically shown in Fig. 4.2. The microstrip line consists of a narrow stripe of metal placed on top of a grounded substrate. While the microstrip line is common in traditional hybrid circuits built on insulating dielectric substrates, its use in modern silicon ICs is problematic. The conductive nature of conventional silicon material will cause significant losses due to the flow of substrate conduction currents. Moreover, making connections to the metallic ground plane on the back of the silicon wafer requires the use of vertical, through-wafer vias whose implementation in silicon IC's is technologically involved.

An alternative is to implement both the microstrip and ground plane on the wafer front side by using the metal-dielectric stack of a modern IC process. The ground plane in this construction shields the electric field of the microstrip from the silicon substrate, and is easily accessible through commonly used metallic vias [11]. But, due to the small thickness of the dielectric (several um's), the characteristic impedance of such lines is rather small. The only remedy is to reduce the microstrip width which, in turn, causes the resistance per unit length and line attenuation to rise significantly.

In view of these issues, coplanar waveguides constitute a more viable option when it comes to chip integration. The signal and ground conductors of a CPW are built on a single metal layer which is placed above a Si substrate isolated by a silicon oxide layer of a few microns in thickness. Due to its open nature, however, a CPW line is also prone to

substrate loss, albeit to a lesser degree compared to conventional microstrip lines as the electric field lines remains close to the conductors and do not traverse the whole substrate thickness. Despite this shortcoming, integrated CPW lines remain popular due to their ease of fabrication and the wide range of characteristic impedances realized.

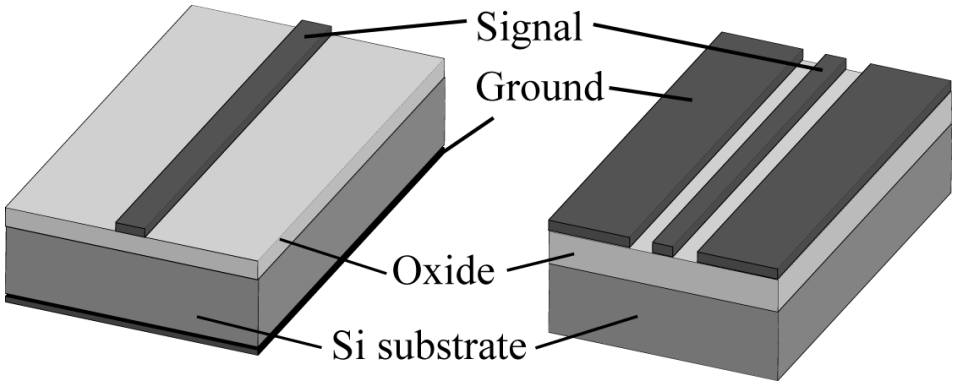

Figure 4.2 Schematic view of on-chip transmission lines with microstrip (left) configuration and coplanar-waveguide (CPW) configuration (right).

An IC compatible technique to reduce the substrate loss of CPW lines is to use electric shields built underneath the transmission line. Already coplanar waveguide (CPW) transmission lines with shields built from floating metal strips perpendicular to the line have been demonstrated to have very low substrate loss [8]. However, the large parasitic capacitance between the CPW and the conductive shield substantially reduces the line characteristic impedance. Therefore, shielded lines with high characteristic impedance require narrow signal lines or large signal to ground spacing, which increase the line attenuation or device area.

In this section we theoretically investigate an alternative shielding method based on a thin, ultra-high-k dielectric film which is inserted between the CPW and the silicon substrate. To demonstrate the shielding effect, we simulate the electric field distribution on the cross section of CPW line. For CPW lines at not too high frequency, quasi-TEM approximation can be made. Therefore, we look at the quasi-static field distribution by solving two dimensional Laplace's equation for the electric potential on the cross section

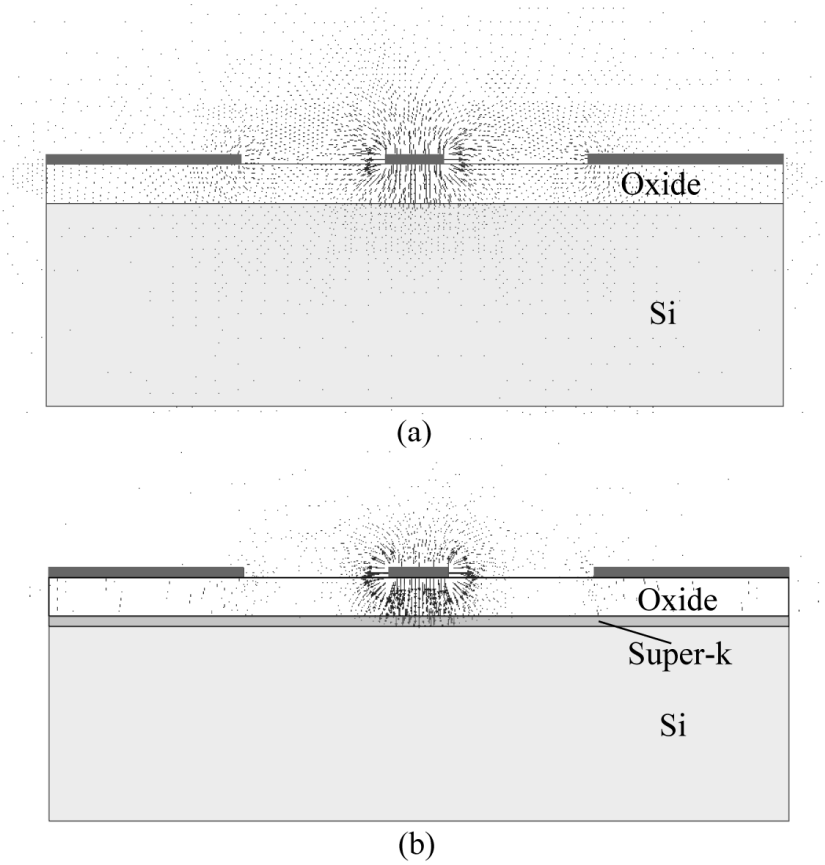

Figure 4.3 Schematic view of electric field distribution of a CPW transmission line (a) without and (b) with super-k shield.

of the structure. This has been done in Ansoft's Maxwell SV. Fig. 4.3 shows the calculated electric field distribution without (a) and with (b) high-k shield. As shown in Fig. 4.3a, without the high-k shield, a significant portion of electric field lines, and therefore electromagnetic energy will penetrate into Si substrate, leading to substrate losses. With the high-k shield inserted (Fig.4.3b), the electric displacement field, and therefore electric field, tends to be confined in the high-k thin film. As a result, much less electromagnetic energy will leak into Si. The shielding effect can be also understood from a circuit theory point of view: the high-k film can be modeled as a large capacitance and provides an alternative low impedance, low loss route for RF current to flow instead of

entering into the lossy Si substrate. The equivalent circuit model of CPW with high-k shield will be discussed in more detail later.

To better verify the picture presented, simulations were performed for CPW lines on a Si substrate with the high-k shield using the microwave simulator in ADS. In the simulations, CPW lines with signal line width of w=30 μm and signal-ground space of s=15 μm were assumed. The substrate stack consists of a 10 Ωcm Si substrate of 500 μm in thick, covered by a 1 μm-thick high-k film 4 μm of SiO_2. For comparison, simulations were also performed on a reference CPW line with the same geometric configurations (w and s), but with the shield replaced by 1 μm of SiO_2. Since we are interested the substrate shielding effect, the conductors and the dielectrics were assumed lossless. The dielectric constants of the super-k layer were chosen to be 500, 1000, 2000 and 5000. The attenuations of the lines were extracted from S-parameter simulations and a comparison of the simulated line attenuations as a function of frequency for different values of dielectric constant is shown in Fig.4.4.

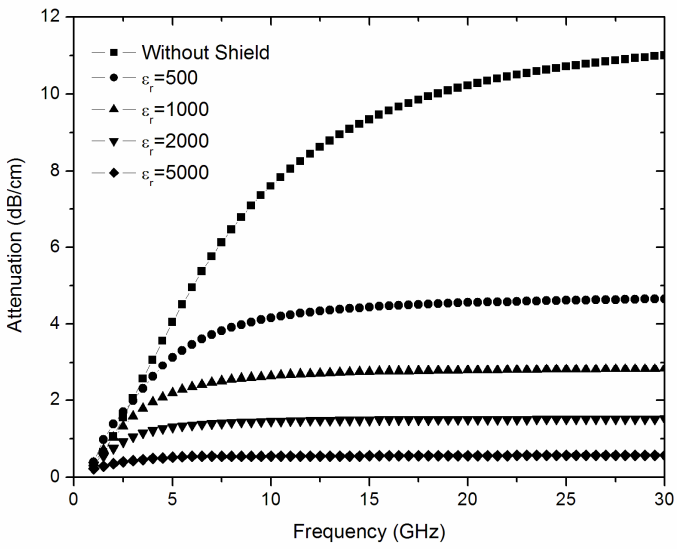

Figure 4.4: ADS Simulation results of CPW line attenuation as a function of frequency with super-k thin film shield for different dielectric constant values. For comparison, CPW line attenuation without shield is also shown.

As shown in Fig.4.4, the ultra-high-k thin film shield can significantly suppress the substrate loss and, thus, reduce line attenuation. The degree of suppression directly depends on the dielectric constant of the shield. At 30 GHz, 1μm thick super-k thin film with a dielectric constant of 500 can reduce the substrate loss by more than 2-fold, and 20-fold reduction of substrate loss can be achieved by super-k film of the same thickness with a dielectric constant of 5000.

Although the simulation shows promising results for loss reduction by super-k materials, the realization of super-k thin films shield on Si is prohibited currently by technological difficulties. Ferroelectric materials are well known to have extremely high dielectric constant values (on the order of 10^5), which make them attractive for this application. However, in thin film forms, ferroelectric materials exhibit much lower value of dielectric constant (3 orders lower) compared to their bulk ceramic forms, especially on Si substrates. Besides, unlike in the simulation presented, realistic ferroelectric films may exhibit high dielectric loss at microwave frequencies which might partially reduce the shielding efficiency. Nevertheless, the idea of electric shield by thin film with super high dielectric constant is still a solid one. This can be accomplished by artificial materials as presented in the next section.

4.3 ADL as a shield

4.3.1 Concept of ADL

As introduced in Chapter 1, an artificial dielectric is a special kind of man-made material which exhibit electromagnetic properties similar to a dielectric material. Physically, it is a large scale model of a real dielectric. Normally, it consists of a large number of identical conducting elements periodically arranged in a three-dimensional or two-dimensional pattern in a host conventional dielectric. A typical structure of artificial dielectric is metallic spheres or disks in a three dimensional lattice. Here we introduce a new kind of artificial dielectric formed by isolated metallic squares embedded in a conventional dielectric material. Since this new kind of artificial material manifests itself as an effective dielectric thin film, we nominate this new structure artificial dielectric layer, or simply, ADL as abbreviation.

Figure 4.5 shows the ADL built from two thin metal layers vertically separated by a thin dielectric film with the thickness t_d and dielectric constant ε_d. Each metal layer is patterned to form a lattice of disconnected, but closely spaced squares. The lattices on the

two metal layers are shifted with respect to each other so that each square on the top lattice partially faces four squares on the bottom lattice and vice versa [9, 12-13]. To reduce the flow of eddy currents inside individual patterns at high frequencies, their dimension is chosen in the micrometer range.

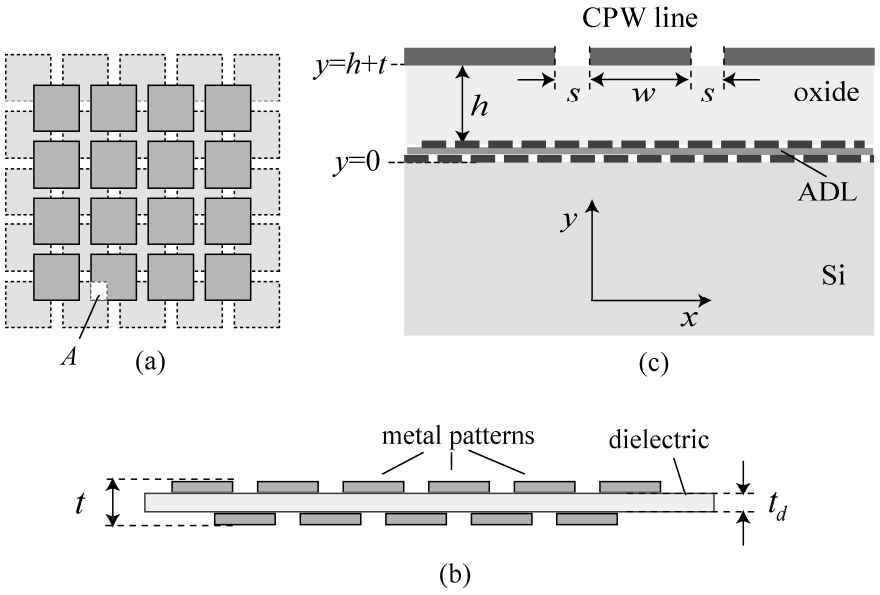

Figure 4.5 (a) and (b): Geometrical layout of the ADL consisting of two thin, patterned metal layers isolated by a thin dielectric. The lattices of squares on the two metal layers are shifted with respect to each other so that each square on the top lattice partially faces four squares on the bottom lattice and vice versa. (c): Cross section of an integrated CPW line shielded by an ADL inserted between the Si and oxide (thickness h) layers.

To describe the dielectric properties of the ADL we use an effective medium approach which is justified at the frequencies of interest in this work (<30 GHz) where the electromagnetic wavelength exceeds by several orders of magnitude the dimension and spacing of metallic squares (both in the micrometer range).

The effective properties of the ADL can be determined by modeling the latter as a two-dimensional network of identical capacitors C in series with resistors R (Fig.4.6).

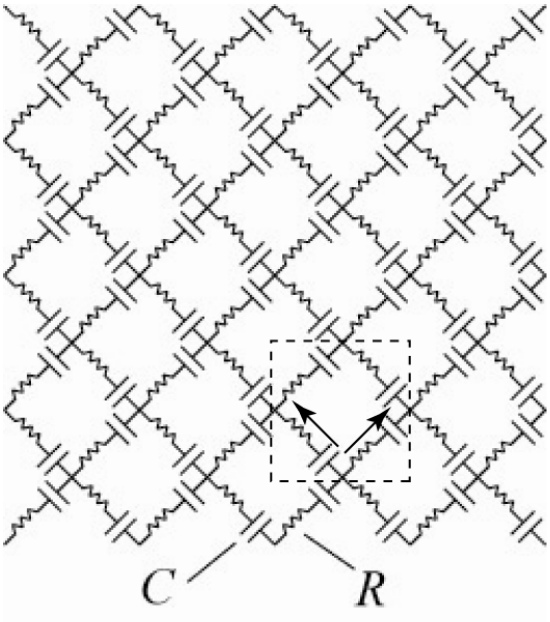

Figure 4.6 Network theoretical model of the ADL based on identical capacitors *C* and resistors *R*.

The capacitors are formed between overlapping metallic squares whereas the resistors take account of the series resistance of the patterns. Using the electric network theory and applying the continuum approximation, one finds the surface impedance of the ADL (ratio between the in-plane electric field and the surface density of the RF electric current flowing on the layer) to be given by $Z_S = R + (1/j\omega C)$. This can be understood by the following arguments. Consider the complex power delivered to a unit cell of the ADL network (as shown in Fig.4.6) and suppose the RF current of *I* flowing into node A. By symmetry consideration, the RF current of each segment is *I*/2. Therefore, the complex power is given by adding up the complex power in each segment, resulting in $P = (R + 1/j\omega C)I^* I$. This can be equated to $P = ZI^* I/2$, where *Z* is the impedance of this unit cell. It is immediately seen that the impedance of the unit cell is given by $Z = R + (1/j\omega C)$. Due to the symmetry of the circuit network, the surface impedance (the impedance per unit area) can be shown to equal to the impedance per unit cell as given by the result presented above. Because a thin dielectric film with an in-plane

permittivity $\epsilon_{\|}$ and thickness t has a surface impedance $1/j\omega\epsilon_{\|}t$, it follows that the effective in-plane permittivity of the ADL is given by

$$\epsilon_{\|} = \varepsilon_{\|} / (1 + j\omega\tau), \tag{4.1}$$

where $\varepsilon_{\|} = C/t$, $\tau = RC$, and t is the overall thickness of the ADL. In the structures studied in this thesis, it can be shown that the product $\omega\tau$ is negligible in the frequency range of interest so that $\epsilon_{\|} \approx \varepsilon_{\|}$. The $\omega\tau$ term actually contributes to the loss tangent of the ADL as will be discussed later. For now, we are interested in the real part of the dielectric constant and just safely ignore this term. Since the thickness t_d of the dielectric layer is extremely small (several tens of nanometers), one can neglect the fringe field and estimate the value of *C* according to

$$C = \varepsilon_d A / t_d, \tag{4.2}$$

where ε_d is the dielectric constant of the dielectric layer and A is the overlap area between two squares partially facing each other (Fig.4.3). As a result,

$$\varepsilon_{\|} = C/t = \varepsilon_d A / t_d t. \tag{4.3}$$

It is important to note that A is in square microns whereas t_d and t do not exceed several tens, respectively, hundreds of nanometers. Therefore, $\varepsilon_{\|}$ is typically several orders of magnitude larger than ε_d. The high value of $\varepsilon_{\|}$ can be exploited to shield the Si substrate from RF electric fields induced by a CPW transmission line as discussed in the previous section.

The effective dielectric constant $\varepsilon_{\perp}$ of the ADL in the direction normal to its plane can be easily estimated when the spacing between the patterns is much smaller than their size. For perpendicular electric fields, the ADL then practically behaves as two continuous metal layers separated by a dielectric film. Here we consider a general situation where *N* dielectric layer with dielectric constant of ε_d is sandwiched by *(N*+1) metal layers (as shown in Fig.4.7). The total capacitance of the structure is just N capacitors in series and is given by $C = \varepsilon_d A / Nt_d$, where A is the overlap area and td is the thickness of one dielectric layer. On the other hand, the total capaciance can also be

calculated by defining an effective dielectric constant ε_{eff} of the overall structure, and resulting in $C = \varepsilon_{eff} A / t$ where t is the thickness of the complete structure. By comparing the two expressions, one finds $\varepsilon_{eff} = \varepsilon_d t / N t_d$. In our ADL case, N is simply equal to 1 and this results in $\varepsilon_\perp \approx \varepsilon_d t / t_d$. Since t and t_d do not differ by orders of magnitude, $\varepsilon_\perp$ is much smaller than $\varepsilon_\parallel$.

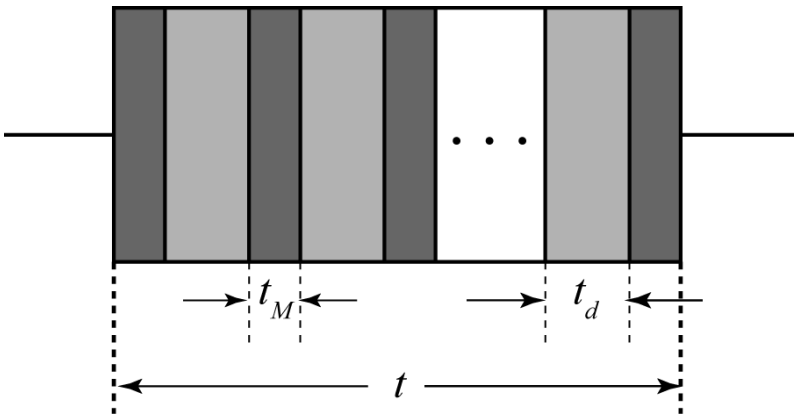

Figure 4.7: A simple model to calculate the perpendicular effective dielectric constant of general ADL structure.

The dielectric loss of the ADL is characterized by the total loss tangent which includes the dielectric loss of the insulating dielectric material as well as the pattern resistance (R in Fig.4.4). Substituting ε_d by $\varepsilon_d(1 - j\tan\delta_d)$ in Eq. (4.2) and combined with Eq. (4.1), it can be shown that the total dielectric loss of the ADL is given by

$$\tan\delta = \tan\delta_d + \tan\delta_M , \qquad (4.4)$$

where $\tan\delta_M = \omega\tau = \omega RC$ is the loss brought by the pattern resistance.

Now consider the magnetic losses. Under influence of a magnetic field perpendicular to the patterns, planar eddy currents start to flow in the plane of the patterns. Such currents, in turn, generate a dipolar magnetic field which opposes the original field. This effect can be represented by an effective susceptibility $\chi_\perp$, i.e. the ratio between the volume average of the induced magnetic dipoles and the original field. For patterns with

a thickness far below the skin depth inside the metal, an approximation assuming a constant magnetic field yields

$$\gamma = \frac{\chi_\perp}{1+\chi_\perp} = -j\eta_M f \omega \mu_0 \sigma_M D^2 , \tag{4.5}$$

where D is the diameter of the patterns, f is their volume filling factor, and η_M is a dimensionless, geometry-dependent factor. For square patterns $\eta_M \sim 1/32$. Detailed derivation is shown in Appendix C.

4.3.2 Shielding effect of ADL

The shielding effect of the ADL on the electric field of a Si-based CPW line (Fig. 4.3c) can be demonstrated using the quasi-TEM approximation [14] where the (transverse) electric field is expressed as the gradient of an electrostatic potential $\varphi(x,y)$ on the line cross section. To simplify the analysis we assume an unbounded substrate and an infinitely thick Si layer. Solving the spectral domain Laplace equation (see Appendix D), the Fourier transform (in the x-direction) of φ inside the Si layer (y<0) can be expressed as

$$\tilde{\varphi}_{\mathrm{si}}(k,y) = \frac{\exp(|k|y)\int_{-\infty}^{\infty} V(x)\exp(ikx)dx}{A(k)\cosh(|k|h) + B(k)\sinh(|k|h)} , \tag{4.6}$$

where $V(x) = \varphi(x, h+t)$ is the potential on the (top) oxide surface, h is the oxide layer thickness (see Fig.4.3c), and

$$A(k) = \cosh(|q|t) + (\varepsilon_{\mathrm{si}} / \varepsilon_{\mathrm{e}})\sinh(|q|t) \tag{4.7}$$

$$B(k) = \varepsilon_{\mathrm{ox}}^{-1}\left[\varepsilon_{\mathrm{si}}\cosh(|q|t) + \varepsilon_{\mathrm{e}}\sinh(|q|t)\right] \tag{4.8}$$

where $\varepsilon_{\mathrm{ox}}$ is the dielectric constant of the oxide layer, $\varepsilon_{\mathrm{e}}=(\varepsilon_{\|}\,\varepsilon_\perp)^{1/2}$, $q=k(\varepsilon_{\|}/\varepsilon_\perp)^{1/2}$, and $\varepsilon_{\mathrm{si}}=\epsilon_{\mathrm{si}} - j\sigma_{\mathrm{si}}/\omega$ with ϵ_{si} the dielectric constant and σ_{si} the conductivity of Si. The (Fourier transformed) electric field inside Si is $(\tilde{E}_x, \tilde{E}_y) = (ik, -|k|)\tilde{\varphi}_{\mathrm{si}}$.

Eqs. (4.6-4.8) show that, for any non-uniform field ($k \neq 0$), a high value of $\varepsilon_{\|}$ reduces $\tilde{\varphi}_{\mathrm{si}}$ and, therefore, the electric field and power dissipated inside the conductive Si. In particular, since the lateral variation of the field over distances comparable to the ADL

thickness (<1 μm) is negligible in typical CPW configurations, it suffices to consider the limit $kt<<1$, where

$$A(k) \approx 1 + (\varepsilon_{si} / \varepsilon_{\perp}) |k| t \,, \tag{4.9}$$

$$B(k) \approx \varepsilon_{ox}^{-1} (\varepsilon_{si} + \varepsilon_{||} |k| t) \,. \tag{4.10}$$

Evidently, increasing $\varepsilon_{||}$ leads to an increase in $B(k)$ and, therefore, a reduction of $\tilde{\varphi}_{si}$. (Although $V(x)$ is given below the CPW conductors, a rigorous treatment of this problem requires its self-consistent computation inside the CPW slots. But the argument presented is sufficient to show the shielding effect.)

Note that the magnetostatic equations of the quasi-TEM approach [14] are not influenced by the dielectric properties of the medium. Therefore, as long as the quasi-TEM approximation holds (i.e. at not too high frequencies), the effect of the ADL on the magnetic field of the CPW is expected to be negligible.

4.4 Experimental results of CPW lines

4.4.1 CPW with ordinary ADL shields

CPW transmission lines were fabricated on a 5-10 Ω·cm n-type silicon wafer in a standard aluminum CMOS production line. The ADL shields were built using two 100 nm-thick aluminum layers isolated by a 30 nm-thick PVD-sputtered aluminum oxide film with a relative dielectric constant of 10. For each CPW line, three different ADL structures were implemented by patterning the metal layers into 3 x 3, 5 x 5, and 7 x 7 μm^2 squares. In all cases the squares were laterally separated by 1 μm-wide gaps. Taking the 7 x 7 case as an example, this structure yields an overlap area of A = 9 μm^2, resulting in an effective in-plane dielectric constant of $\varepsilon_{||} = \varepsilon_d A / t_d t \approx 13000$ for the ADL.

The ADL was isolated from the silicon substrate by a 0.75 μm thermally grown silicon oxide layer which is the typical distance from substrate to the first metal layer in CMOS integration. On top of the shield structure, a 9 μm PECVD silicon oxide was deposited and the CPW line was fabricated using the top metal level (3 μm-thick aluminum). The micrograph of one CPW line after processing is shown in Fig.4.8. The shield structure is shown in the enlarged area. CPW lines with different signal line width

(w) and signal to ground spacing (s) were designed to achieve different characteristic impedances.

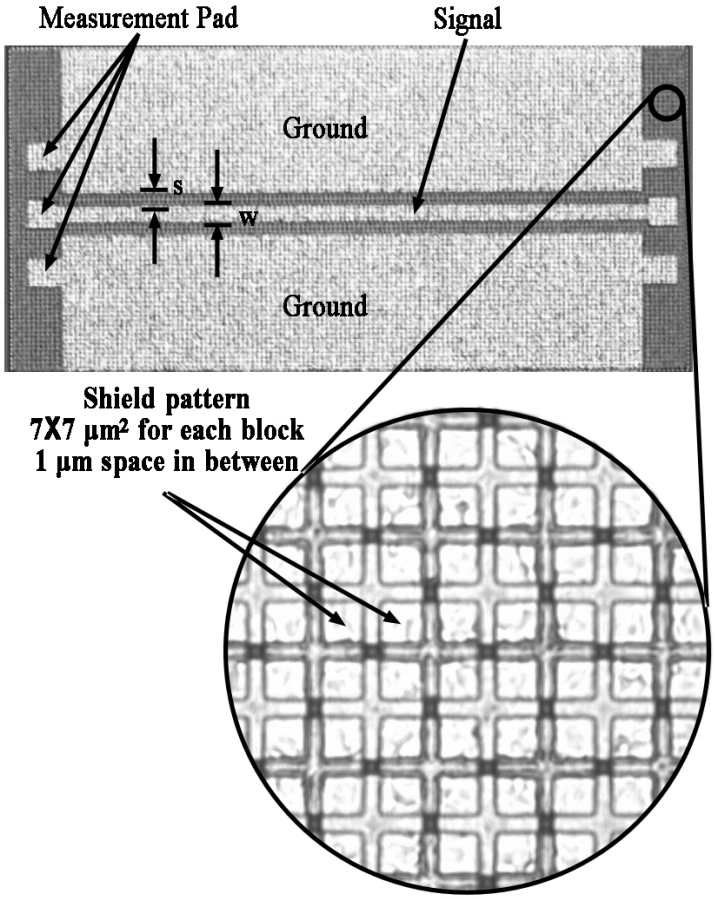

Figure 4.8: Micrograph of a CPW transmission line with an ADL substrate shield. The signal line width and signal to ground spacing of the CPW are denoted by w and s, respectively. The enlarged portion of the ADL shield clearly shows the two (overlapping) metallic square lattices.

The propagation constant (γ) and characteristic impedance (Z_0) of the CPW lines (of length l) were found from (see Appendix E)

$$\gamma = (1/l)\ \text{arctanh}\left(\sqrt{Z_{\text{short}} / Z_{\text{open}}}\right) \qquad (4.11)$$

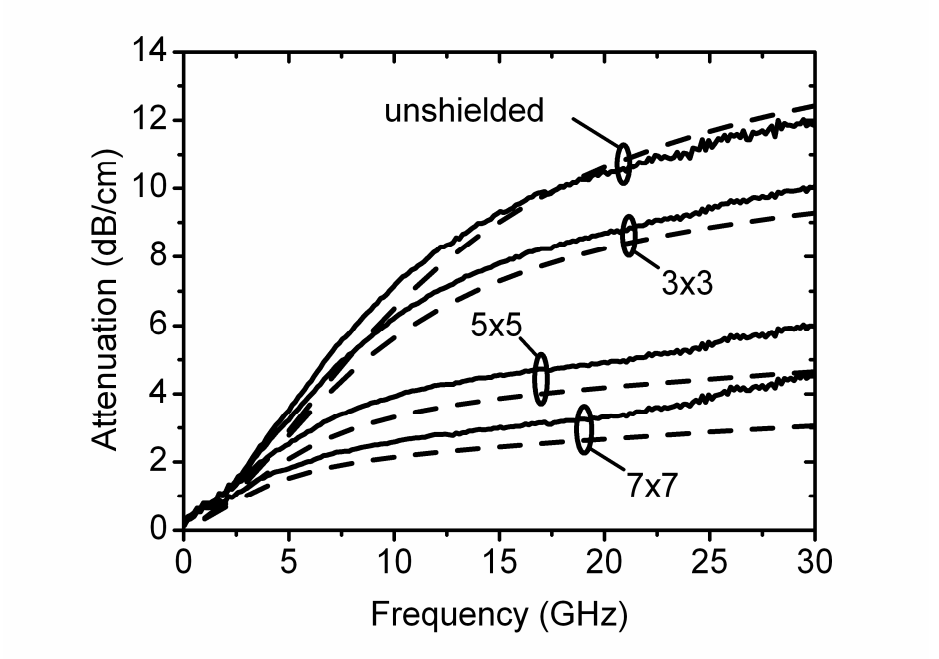

Figure 4.9: Attenuation vs. frequency of a CPW line (w=30 μm, s=30 μm) shielded by ADL's with 3x3, 5x5, and 7x7 μm^2 patterns. Results for an unshielded line are shown for comparison. Dashed lines show the HFSS simulation results with the ADL modeled as an anisotropic dielectric. Taking into account a ~0.3 μm reduction of the ADL pattern size due to lithography issues, a value of $\varepsilon_{\parallel} \sim 700$, 4200, and 10000 was calculated for the three shields, respectively, and used in the HFSS simulations. $\varepsilon_{\perp} \sim 75$ in all cases. A Si resistivity of 7 Ωcm was assumed in the simulations.

$$Z_0 = \sqrt{Z_{\text{open}} \cdot Z_{\text{short}}}\,, \tag{4.12}$$

where Z_{open} and Z_{short} denote the impedance of the open- and short terminated lines, respectively, extracted from S-parameter data obtained using a HP8510C vector network analyzer. Other transmission line parameters (i.e. capacitance per unit length C, inductance per unit length L, serious resistance per unit length R and shunt conductance per unit length G) can also be extracted from S-parameter measurement as derived in

Appendix E. As shown in Appendix E, for integrated CPW line, the metal loss is modeled as the serious resistance per unit length and the substrate loss is modeled as the shunt conductance per unit length.

Fig.4.9 shows the attenuation constant $\alpha = (20 \log e)\,\mathrm{Re}\gamma$ of a shielded CPW (w=30 μm, s=30 μm) in comparison with that of an identical, but unshielded line. The effectiveness of shielding clearly increases with the ADL pattern size. At frequencies below 30GHz, the ADL with the largest patterns (7 x 7 μm^2) yields a nearly three fold reduction of α compared to the unshielded device. HFSS simulations based on the effective description of the ADL yield lower values of α compared to the experimental data (Fig.4.9). Especially at high frequencies, this can be attributed to the inability of the dielectric model to account for the frequency dependant eddy current loss inside the individual patterns of the ADL. Nevertheless, the overall agreement is reasonable below 20 GHz.

Fig.4.10 compares other extracted transmission line parameters of shielded CPW lines with the same geometric configurations (w=30 μm, s=30 μm), but different ADL pattern sizes. Unshielded line results are also shown for comparison. As shown in Fig.4.10(a), ADL shield manifest itself by significantly reducing the substrate loss. The substrate loss reduction effect increases with the ADL pattern size. A six-fold substrate loss reduction near 30 GHz can be achieved by applying the ADL with a 7x7 μm^2 pattern size. Fig.4.10(b) compares the inductance per unit length among different CPW lines. As mentioned in section 4.3.2, the ADL behaves mainly like an effective dielectric layer, the magnetostatic equations of the quasi-TEM approach are not influenced by the existence of ADL. Effect of ADL on the magnetic field, i.e. the extracted inductance per unit length, of the CPW line is expected to be negligible. Therefore, as illustrated in Fig.4.10(b), different CPW lines show almost identical inductance per unit length values throughout the whole frequency range.

The effect of ADL on the capacitance per unit length value is shown in Fig.4.10(c) and can be understood with the help of a simplified lumped element model. Fig.4.11 shows the resistive-capacitive equivalent network of a CPW line with and without a shield. The oxide capacitance is denoted by C_{ox} whereas C_{sub} accounts for the capacitance due to electric field penetrating into Si. The resistors R_{sub} account for the substrate conductivity and are responsible for the substrate loss. In the case of CPW with the ADL shield, the substrate network is shunted by equivalent ADL capacitors. Because of the

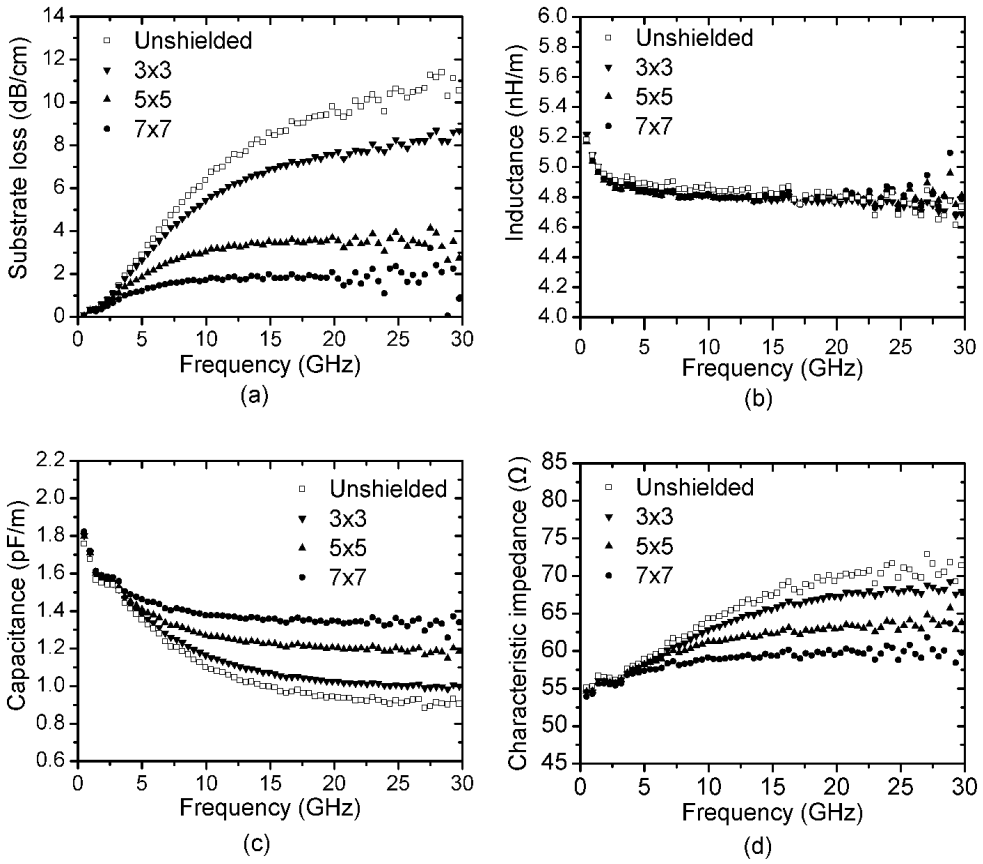

Figure 4.10: Extracted (a) substrate loss, (b) inductance per unit length, (c) capacitance per unit length and (d) characteristic impedance vs. frequency of a CPW line (w=30 μm, s=30 μm) shielded by ADL's with 3x3, 5x5, and 7x7 μm^2 patterns. Results for an unshielded line are shown for comparison. It shows that the substrate loss alone has about six-fold reduction of a 7x7 μm^2 ADL shielded CPW line compared with the unshielded line at high frequencies. The ADL has little effects on the inductance per unit length value due to the mainly dielectric properties of the ADL. In contrast, ADL modifies the capacitance per unit length value as expected by its different effective in-plane dielectric constant. As a result, the characteristic impedance also changes at high frequencies due to the insertion of the ADL.

high effective (in-plane) dielectric constant of the ADL, this capacitance may be much larger than the Si capacitance. This will reduce the current flowing through the substrate resistors (shielding effect) but will also lead to an increase in the total capacitance of the CPW line. Note that the inductance per unit length is not affected by the inclusion of a high-k shield. Consequently, the inclusion of the shield will cause the characteristic impedance, which can be simplified as $\sqrt{L/C}$ when the losses are low, of the line to drop. This effect will become stronger with increasing of the pattern size, as shown in Fig.4.10(d).

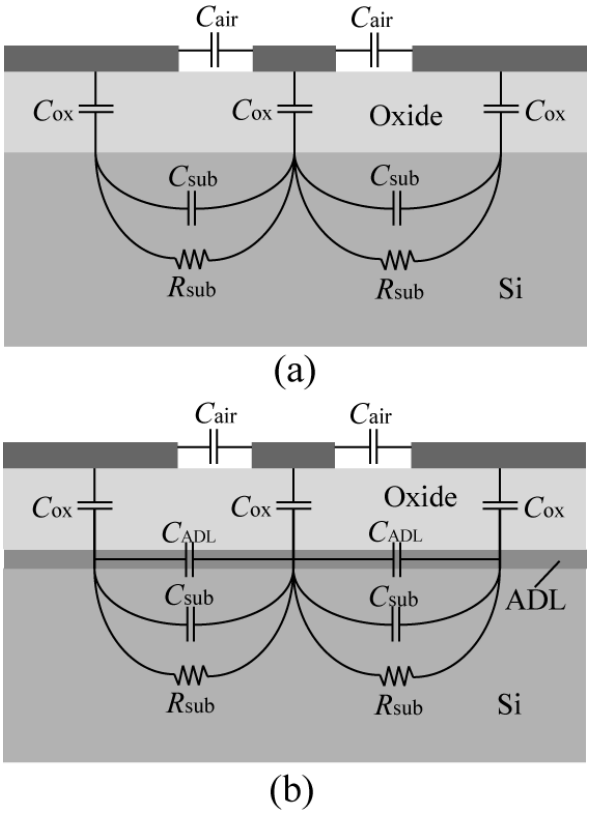

Figure 4.11: Cross section view and simplified lumped-element models of a CPW line on silicon with (a) and without (b) ADL shield.

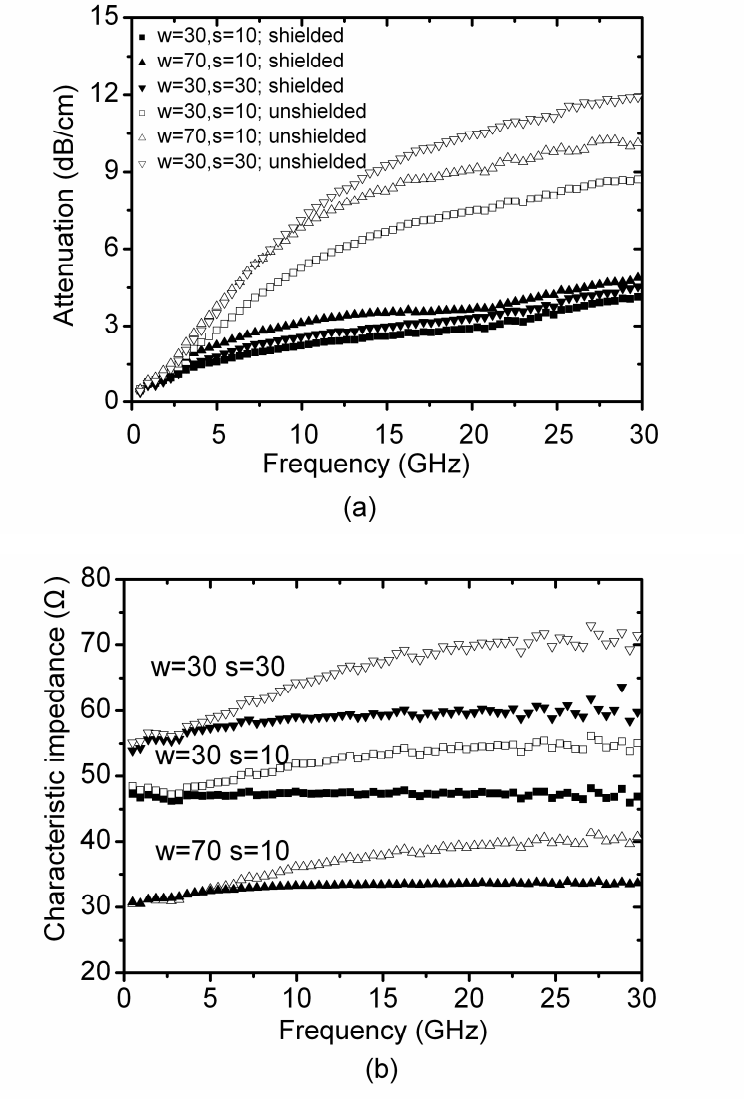

Figure 4.12 Attenuation (a) and real part of the characteristic impedance (b) of shielded (solid markers) and unshielded (hollow markers) CPW lines with the signal line width *w* and signal to ground spacing *s*.

Fig.4.12(a) shows the attenuation versus frequency for three shielded CPW lines with different values of *w* and *s*. Results for identical, but unshielded lines are also shown for

comparison. A two- to three fold reduction of line attenuation is observed for all lines up to 30 GHz. Note that Fig.4.12(a) shows the total line attenuation including the conductor loss. Otherwise, results for the substrate loss show an up to six-fold reduction due to insertion of the ADL (for example the one shown in Fig.4.10a). These results are comparable with those found by Cheung et al [8].

Fig.4.12(b) compares the characteristic impedances of the shielded and unshielded lines with different geometric configurations. All the shielded lines have an ADL with 7 x 7 μm^2 patterns. In contrast with the unshielded lines, the characteristic impedance of the shielded CPW's changes little as function of frequency and has a very small imaginary component. This is due to the ADL masking the influence of the complex permittivity $\varepsilon_{si}=\epsilon_{si} - j\sigma_{si} / \omega$ of silicon which has a large, frequency-dependent imaginary part. Note that, even in presence of the ADL, a wide range of characteristic impedances can be realized without the need for extremely narrow signal lines or large signal-ground spacing. This is in contrast with results obtained using a floating metallic shield [8]. In both cases, the shield structures introduce a low impedance path, which are the ADL and the metallic stripes respectively, between the parasitic capacitances formed between the CPW conductors and the shields, leading to an increase of capacitance per unit length of the CPW line and a decrease of the characteristic impedance. However, due to its high conductivity, the latter has a much bigger effect on the characteristic impedance. As a result, CPW lines with high characteristic impedance are difficult to be realized using conventional metallic shield while still keeping the metallic loss or signal to ground space low. For ADL shielded CPW lines, a tradeoff between high efficiency of shield and high characteristic impedance can be made. Note that, in our experiments, the ADL lowers the characteristic impedance of the CPW lines up to ~15% due to an increase in the line capacitance per unit length. Therefore, ADL-based CPW lines with a wide range of characteristic impedances can be realized without the need for extremely narrow signal lines or large signal-ground spacing.

Based on the experimental results, it is clear that the shielding effectiveness of the ADL can be further increased by increasing its in-plane dielectric constant $\varepsilon_{||}$. This can be achieved by increasing the pattern size, provided that the flow of parasitic eddy currents inside individual patterns can be effectively suppressed, which will be the content of the next section (section 4.4.2). $\varepsilon_{||}$ can also be increased by reducing the thickness of the

dielectric layer, or using a dielectric with a high intrinsic dielectric constant such as TiO_2. Finally, in view of the many metallization layers available in modern IC processes, one can stack several ADL's on top of each other to increase the shielding effect (see section 4.4.3).

It is worth mentioning that, unlike conventional shielding structures [6-8], the geometrical patterning of an ADL does not depend on the layout of individual CPW lines (e.g. their direction). Therefore, a predefined uniform ADL shield can be built underneath the whole passive (sub-) circuit, which simplifies the mask design and fabrication process.

4.4.2 CPW with micro-patterned ADL shields

Although the application of ADL shields results in significant reduction of the substrate loss, the overall performance gain is limited by the eddy currents generated inside the metallic patterns of the ADL itself. At microwave frequencies, eddy currents flow inside the individual metallic particles of the ADL in response to the perpendicular component of the magnetic field of the CPW. These currents, which undergo ohmic dissipation inside the metallic patterns, manifest themselves by increasing the conductor loss (i.e. resistance per unit length) of the transmission line. This effect, which becomes more prominent at higher frequencies, is not accounted for by the dielectric model of the ADL (see Fig.4.9). Using smaller patterns reduces the eddy current loss, but at the expense of a lower effective dielectric constant and, thus, less effective shielding.

In this section, a new type of ADL will be demonstrated. The new type of ADL shield, while maintaining a very high shielding efficiency, is much less prone to eddy current loss. This is achieved by micro-patterning the individual metallic elements of the ADL as shown in Fig.4.13. Employing these shields, we have realized CPW lines on an ordinary Si substrate with an overall attenuation comparable to identical lines built on a high resistivity Si (HRS) wafer. This provides an alternative to the expensive high-resistivity substrates as the vehicle for high-quality microwave transmission lines.

The principles of the eddy current loss reduction by micro-patterning of the metallic elements can be understood by considering the eddy current distribution in a metallic square under influence of a perpendicular magnetic field. Fig. 4.14 shows simulation results of current density distribution of metallic squares with and without

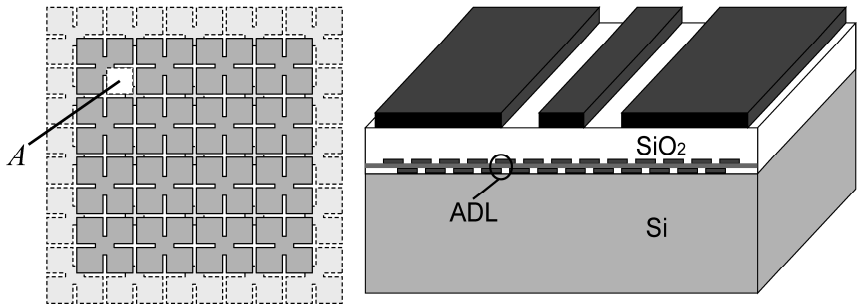

Figure 4.13: Top view (left) of a micro-patterned ADL. The micro-patterned ADL is realized by etching slots near the edges of each square pattern (dashed lines in the left figure). The schematic layout of an integrated CPW line equipped with an ADL shield is shown as well (right).

micro-patterning under uniform magnetic field perpendicular to the paper. As shown in the figure, the current density is relatively large near the edges where it dominates the ohmic loss (which is quadratic in current). Cutting narrow slots close to the edges of the metallic square reduces the flow of these edge currents, resulting in a lowering of the total ohmic dissipation inside the pattern. Note that by placing the slots outside the overlap area between squares on different lattices, the in-plane dielectric constant of the ADL will not be affected.

Integrated CPW lines with ADL shields were fabricated using similar processing steps as described in the previous section. The CPW lines were made by 3 μm-thick aluminum (Al) metallization on a standard 5-10 Ω·cm Si wafer, isolated by a 9 μm-thick silicon oxide (SiO_2) layer. The ADL shields were built on top of Si using a 30 nm-thick, sputtered aluminum oxide (Al_2O_3) film sandwiched between two 100 nm-thick, patterned Al layers. Both conventional and micro-patterned ADL shields were fabricated for comparison. In the first case, conventional ADL was built using 15x15 μm^2 Al squares laterally separated by 1μm-wide gaps. In the latter case, each 15x15 μm^2 square was additionally patterned by etching slots perpendicular to its sides (Fig.4.13). In both cases the overlap area between metallic elements on the two lattices was $A = 49\ \mu m^2$ which, with $\varepsilon_d \sim 10$, yields a relative in-plane dielectric constant of $\varepsilon_{||} \sim 70000$.

To compare the performance of the shielded lines to those implemented on a

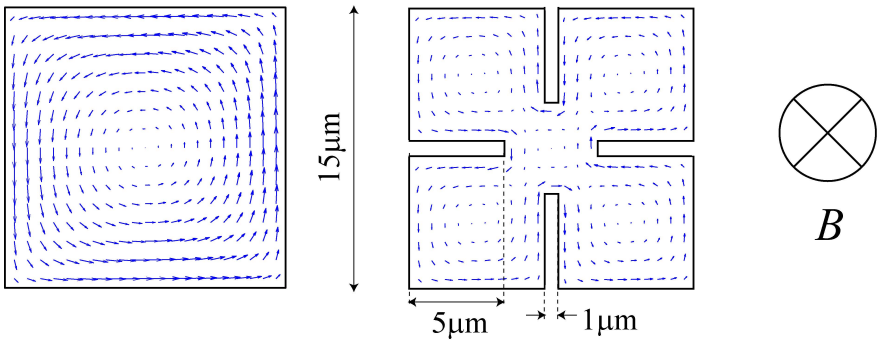

Figure 4.14: Calculated eddy current density distribution in a single, 100 nm-thick metallic (Al) element of a conventional (left) and micropatterned (right) ADL in response to a perpendicular, magnetic field (*B*). The field is assumed to be uniform for simplicity. Calculations were based on the quasi-static approximation which is applicable to elements much smaller than the electromagnetic wavelength. At the frequency range of interest in this work (<25 GHz) the element thickness remains smaller than the skin depth in the Al metal (>500 nm), leading to an almost frequency-independent current distribution.

high-resistivity substrate, identical CPW lines were fabricated on a HRS wafer (1-5 kΩ·cm) with surface passivation [15]. The surface passivation of the HRS wafer was carried out by Ar implantation to amorphorise the surface of the HRS substrate. As a result, the detrimental effects of conductive surface channels can be minimized [15]. A 0.5 μm PECVD silicon oxide was used as the isolation layer between the CPW conductors and the substrate. The line parameters (characteristic impedance, attenuation) were extracted using the formula in Appendix E from the S-parameter measurements carried out on a HP8510 network analyzer.

The total attenuation, substrate loss, real part of characteristic impedance and phase velocity of a CPW line with a signal line width of 30 μm, and signal to ground spacing of 10 μm are shown in Fig.4.15 up to 25 GHz. Compared to an unshielded line on standard Si (U-CPW in Fig.4.15), significant reduction of total attenuation is observed with the ADL, both with (μADL-CPW) and without (ADL-CPW) micro-patterning, as shown in Fig.4.15(a). Fig.4.15(b) presents the substrate loss of the CPW line and shows more than a ten-fold reduction within most of the measurement frequency range, due to the use of the ADL. At relatively low frequencies (<5 GHz), ADL-CPW and μADL-CPW exhibit

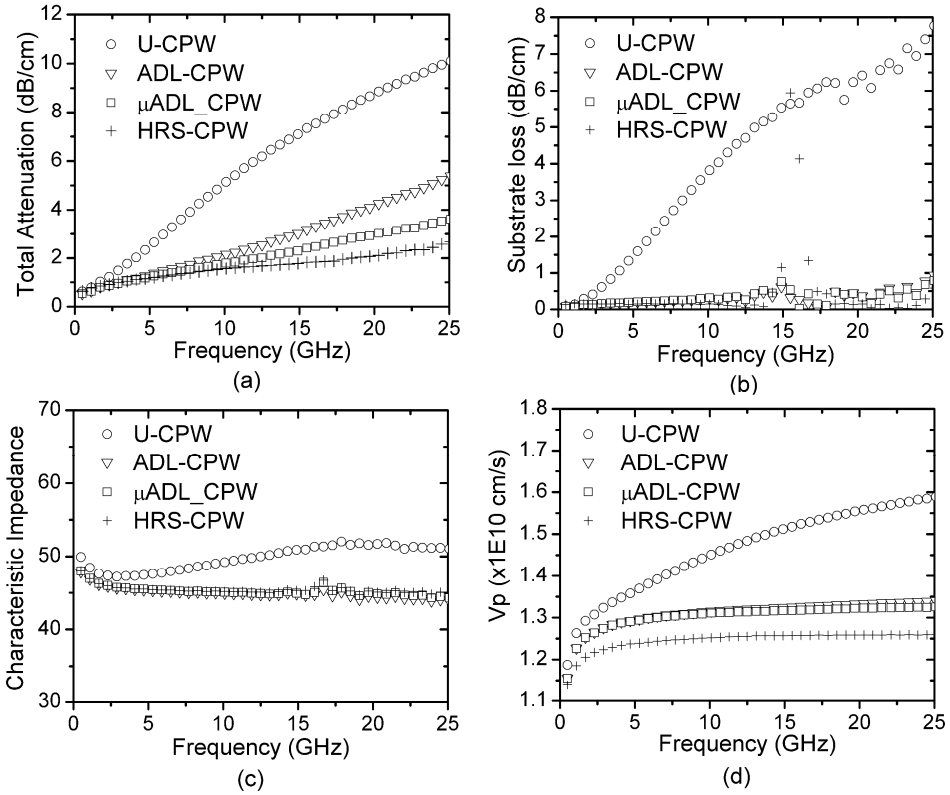

Figure 4.15: Measured (a) total attenuation, (b) substrate loss, (c) characteristic impedance and (d) phase velocity as a function of frequency for an unshielded CPW (U-CPW), a CPW with a conventional ADL shield (ADL-CPW), and a CPW with a micropatterned shield (μADL-CPW), all built on a 5-10 Ω·cm Si substrate. Results for an identical line on a HRS wafer are shown for comparison (HRS-CPW). The line has a signal width *w* of 30 μm and a signal to ground space *s* of 10 μm.

similar attenuation values. However, as the frequency increases, the μADL-CPW shows remarkably lower attenuation, despite the fact that the substrate losses are almost identical as clearly illustrated in Fig.4.15(b). This deviation is due to the suppression of the eddy current loss of the ADL by micro-patterning, which leads to the reduction of the conductor loss of the line. Fig.4.15(a) also shows the attenuation of the HRS-based CPW (HRS-CPW) which is only slightly lower than that of μADL-CPW (2.7- vs. 3.6 db/cm at

25 GHz) despite the latter being built on a standard Si substrate. Note that the characteristic impedances of the shielded and HRS-based lines were all close to ~46 Ω, as shown in Fig.4.15(c) so that a comparison of attenuation values is justified. The conductor loss of the μADL-CPW was found to be reduced by 40% at 25 GHz compared to the ADL-CPW which proves the efficiency of micro-patterning in reducing the eddy current loss of the ADL. This, in combination with the high shielding efficiency of the ADL, causes the overall loss of μADL-CPW to be low and comparable to the HRS-based device.

It is also noticed that the phase propagation velocity of the shielded lines (not shown here) is almost constant over the whole frequency range. This is in contrast with the dispersive behavior of the unshielded line which is caused by the losses in the standard Si substrate and leads to a rising phase velocity as function of frequency. Compared to the unshielded line, the shielded lines exhibit a phase velocity which is slightly lower (up to 15%) because of the increase in the effective dielectric constant of the environment brought about by the insertion of the ADL.

4.4.3 CPW with multi-layered ADL shields

As mentioned in section 4.4.1, the shielding effect can be enhanced by stacking several ADL layers on top of each other. Fig.4.16 shows schematically the cross section view of the multi-layered ADL. On one hand, the stacking of ADL increases the total thickness of the ADL media. And on the other hand, it also increases the effective in-plane dielectric constant as we shall discuss below.

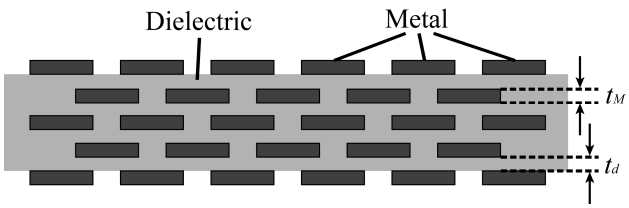

Figure 4.16: Cross section view of multi-layered ADL.

The thickness dependence of the shield efficiency can be understood by considering Eq. (4.6-4.10). By increasing the thickness *t* of the ADL, both $A(k)$ and $B(k)$ increase, resulting in a decrease of $\tilde{\varphi}_{\mathrm{si}}(k,y)$ and therefore the electric field $(\tilde{E}_x,\tilde{E}_y)$ in Si. For a

multi-layer ADL, the effective in-plane dielectric constant can be estimated by considering a 3D lumped-element equivalent circuit, which is similar to the one shown in Fig.4.4 (In Fig. 4.6, a 2D lumped-element network is used to model single ADL with two metal layers and one ordinary dielectric in between. While for a equivalent lumped-element circuit model of multi-layer ADL, the 2D network is stacked on top of each other to form a 3D equivalent circuit.) The effective in-plane dielectric constant of a multi-layer ADL is then given by

$$\varepsilon_{\parallel} = \frac{NC}{t} = \frac{N\varepsilon_d A}{t_d[(N+1)t_M + Nt_d]} \quad , \tag{4.13}$$

where N is the total number of ordinary dielectric layers and t is the overall ADL thickness, ε_d and t_d denote the dielectric constant and thickness of the isolating layers, A is the overlap area between metallic patterns, and t_M is the thickness of the metallic layers. In the above equation we have used $C = \varepsilon_d A / t_d$. If the number of isolating layers is 1, i.e. the ADL structure we have considered in the previous sections, one finds

$$\varepsilon_{\parallel} = \frac{C}{t} = \frac{\varepsilon_d A}{t_d(2t_M + t_d)}, \tag{4.14}$$

which is exactly Eq. (4.3), based on the fact that the total ADL consist 2 metal layers and one dielectric layer. By dividing both the numerator and denominator on the right side of Eq. (4.13), one has

$$\varepsilon_{\parallel} = \frac{\varepsilon_d A}{t_d(\frac{N+1}{N}t_M + t_d)}. \tag{4.15}$$

By comparing Eq. (4.14) and Eq. (4.15), it is obvious that by increasing N, or equivalently the number of ADL layers, one has larger value of the in-plane effective dielectric constant. Substituting the values of t_M and t_d in our experiments, it is found that a ~28% percent increase of $\varepsilon_{\parallel}$ can be achieved by adding only one metal and one dielectric layers (N=2 in this case) on single ADL.

The fabrication of CPW lines with multi-layered ADL is straight-forward and similar to the processing presented in the previous sections, except for repeating the patterned metal and isolating dielectric layer certain times. CPW lines with single ADL shield

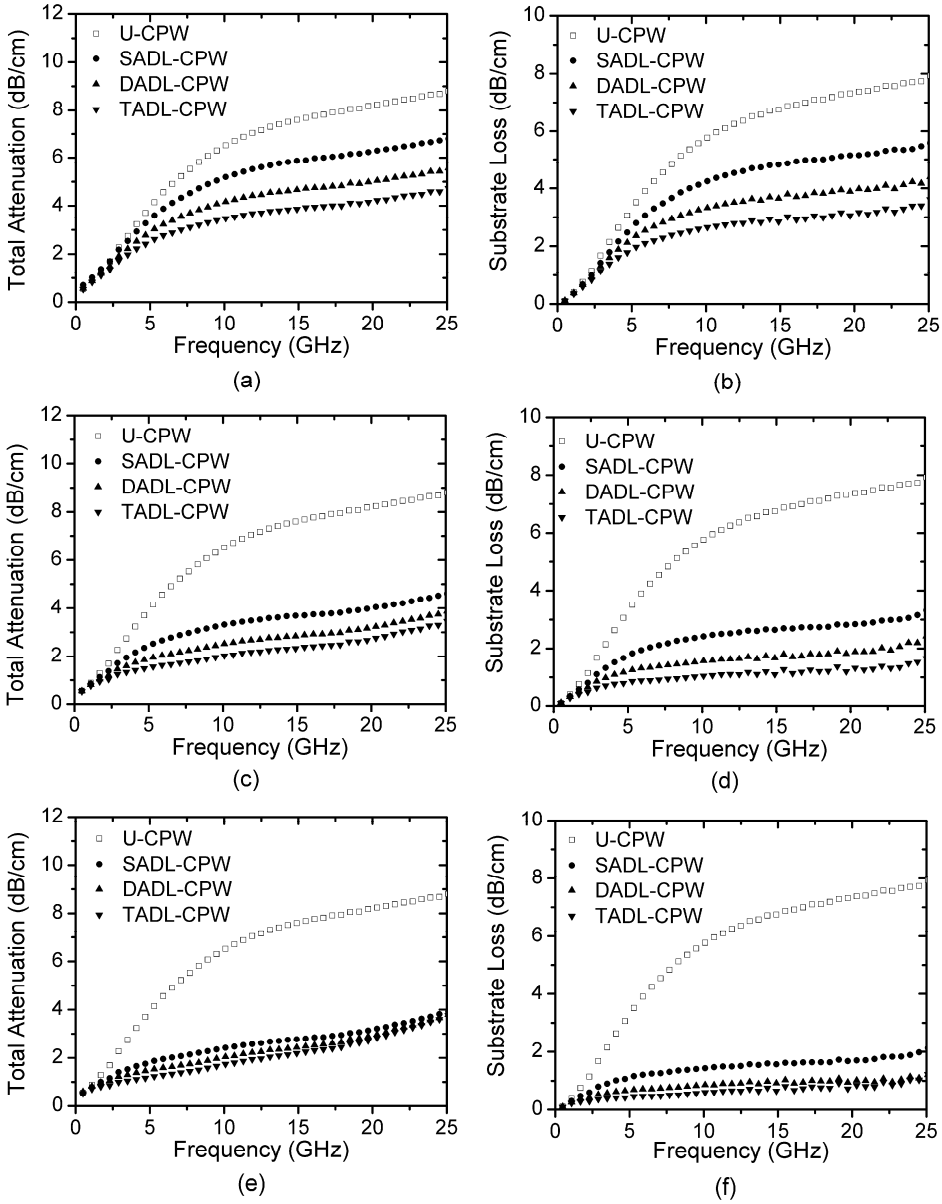

Figure 4.17: Extracted total attenuation (left column) and substrate loss (right column) for CPW lines (w=30 μm, s=30 μm) with different number of ADL shield layers. The ADL metal pattern sizes are 3x3 (a-b), 5x5 (c-d) and 7x7 (e-f) μm^2.

(SADL-CPW, *N*=1), double ADL shield (DADL-CPW, *N*=2) and triple ADL shield (TADL-CPW, *N*=3) were fabricated on the same wafer. For comparison, unshielded lines (U-CPW) were made as well. The ADL metal square sizes were chosen to be 3 x 3, 5 x 5, and 7 x 7 μm^2. Still transmission line parameters were extracted from S-parameter measurement on a HP8510 network analyzer.

Fig. 4.17 compares total attenuation and substrate losses of CPW lines with different ADL pattern sizes and different number of ADL layers. In most of the cases, the total attenuation decreases with increasing the number of ADL layers, which is attributed to the decreases of substrate losses. Apparently, by stacking more ADL layers, the shield is more effective, as expected, due to the higher in-plane effective dielectric constant and higher thickness of the ADL media. However, at high frequencies, as shown in the figure, for the case of 7x7 μm^2, the total loss increases slightly with the number of ADL layers. This is mainly due to the contribution of the eddy current losses in ADL patterns. As can be understood by the aid of Fig. 4.16, the number of metal blocks per unit volume increases with ADL layer numbers, resulting in more eddy current losses per unit volume. This effect becomes more prominent when the pattern size of ADL is large, as in the case of 7x7 μm^2, and can be ignored for the pattern sizes of 3x3 and 5x5 μm^2. Therefore, by applying multi-layered ADL shields with relatively small pattern sizes, the shield efficiency can be increased at high frequencies while keeping the eddy current loss insignificantly. This is demonstrated by comparing Fig. 4.17 (c) and (e), CPW line with 5x5 μm2 TADL shield shows less loss at 25GHz than all CPW lines with 7x7 μm^2 ADL shield.

4.5 Applications of shielded CPW lines

Transmission lines are building blocks of a wide range of microwave components including branch-line couplers, quarter wavelength transformers and transmission line filters [1]. With the ADL shield developed, the losses of these devices can be, in principle, significantly reduced. In this section, we focus on branch-line couplers and ring hybrids built from shielded CPW lines to demonstrate the loss reduction effects.

4.5.1 Principles of directional couplers

Directional couplers are passive reciprocal four-port networks [1]. The operation of a directional coupler can be illustrated with the aid of Fig. 4.18. As shown in the figure, among the four ports, one (port 1) is regarded as the input, one (port 2) is regarded as the

through port (where most of the incident signal exits), one (port 3) is regarded as the coupled port (where a fixed fraction of the input signal appears), and an isolated port (port 4), which is usually terminated. All four ports are ideally matched, and the circuit is ideally lossless. Directional couplers can be realized in transmission line (microstrip, stripline, coax and CPW) and waveguide forms. They are used for sampling a signal, sometimes both the incident and reflected waves which is an important part of a network analyzer [1].

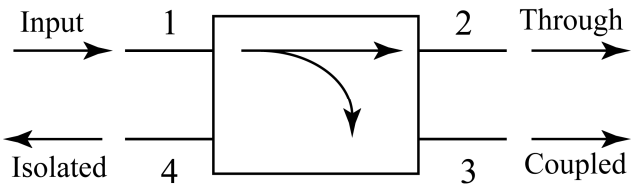

Figure 4.18: Schematic view of directional couplers and power flow conventions.

It can be shown that, for an ideal directional coupler, its S-parameter matrix takes the form

$$[s]=\begin{bmatrix} 0 & S_{12} & S_{13} & 0 \\ S_{12} & 0 & 0 & S_{24} \\ S_{13} & 0 & 0 & S_{34} \\ 0 & S_{24} & S_{34} & 0 \end{bmatrix}. \tag{4.16}$$

In real case, since the directional couplers are required to operate over a certain frequency range, it is not possible to obtain an ideal performance over the whole frequency range. The following S-parameter based quantities are commonly used to characterize a real directional coupler [1]:

$$\text{Coupling} = C = 10\log\frac{P_1}{P_3} = -20\log|S_{13}|\,\text{dB}, \tag{4.17}$$

$$\text{Directivity} = D = 10\log\frac{P_3}{P_4} = 20\log\frac{|S_{13}|}{|S_{14}|}\,\text{dB}, \tag{4.18}$$

$$\text{Isolation} = I = 10\log\frac{P_1}{P_4} = -20\log|S_{14}|\,\text{dB}, \tag{4.19}$$

$$\text{Insertion loss} = IL = 10\log\frac{P_1}{P_2} = -20\log|S_{12}|\,\text{dB}. \tag{4.20}$$

Hybrid couplers are special cases of directional couplers that are designed for a 3dB coupling. Hybrids come in two types, 90° or quadrature hybrids and 180° hybrids. The two kinds of hybrids are simulated and experimentally realized by CPW lines with ADL shields to demonstrate the loss reduction effects and will be the contents of the following two sections.

4.5.2 Branch-line couplers

90° or quadrature hybrids are hybrid couplers with a 90° phase difference in the outputs of the though and coupled ports. They are often made in microstrip or stripline forms as shown in Fig. 4.19, and are also known as branch-line couplers. The operation of an ideal branch-line coupler is as follows. With all ports matched, power entering port 1 equally distributes to port 2 and 3, with no power coupled to port 4. Thus the S-parameter matrix has the form of

$$[s] = \frac{-1}{\sqrt{2}}\begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix}. \tag{4.21}$$

The frequency response of an ideal branch-line coupler with central operation frequency of 20 GHz is shown in Fig. 4.20. Here only the magnitudes of S-parameters (in dB) are shown. Without losses, at design frequency (20 GHz), powers inputted at port 1 are equally (3 dB) split between port 2 and port 3, as can be read from the $|S12|$ and $|S13|$ values at 20 GHz in the figure. Also perfect isolation ($|S14| = -\infty\text{dB}$) and return loss ($|S11| = -\infty\text{dB}$) are achieved at design frequency. All of these quantities, however, degrade quickly as the frequency departs from the central design frequency.

In reality, however, especially for branch-line couplers built on Si, losses are inevitable which results in significant deviation from the ideal behavior. To see the effect of substrate loss, branch-line couplers built from Si-based CPW lines were simulated in

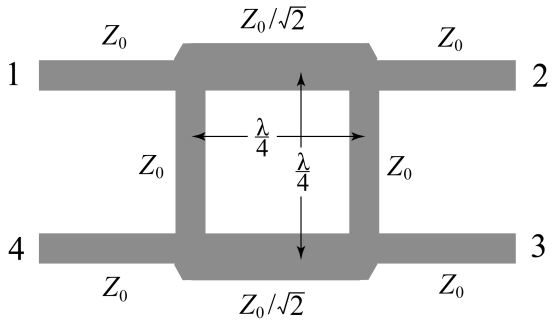

Figure 4.19: Geometry of a branch-line coupler in microstrip form. Power entered at port 1 are equally distributes to port 2 and 3, with no power coupled to port 4.

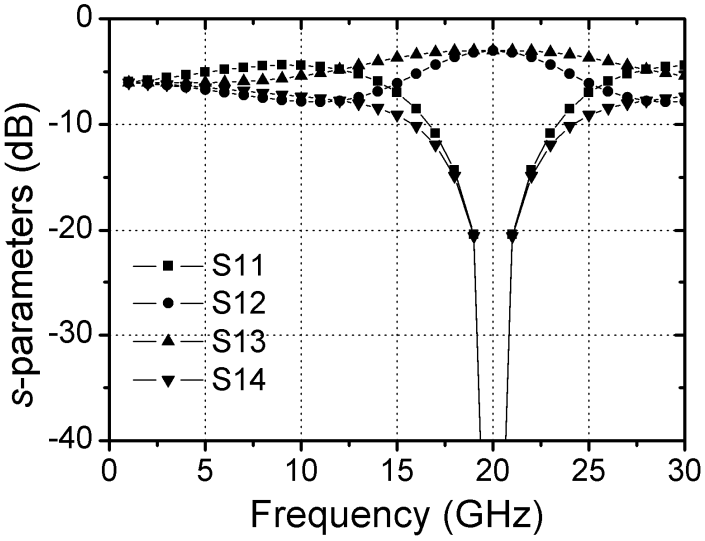

Figure 4.20: Magnitudes of *s*-parameters (in dB) of an ideal branch-line coupler as a function of frequency.

ADS both with and without the high-k ADL shield. The design frequency was 20 GHz. The system characteristic impedances (characteristic impedance of the transmission lines)

in both cases were 50 Ω. Due to modifications of characteristic impedance and phase speed by application of ADL shields, the geometric layouts are slightly different in the two designs. The layout of the branch-line coupler in its CPW form is schematically shown in Fig. 4.21. As illustrated in the cross sectional view, an additional metal layer of 0.6μm in thickness, which is 3μm away from but connected to the top CPW metal layer by metallic vias, is implemented to prevent floating of the central, rectangular-shaped ground conductor. In the S-parameter simulation, the resistivity of the Si substrate is supposed to be 10 Ωcm.

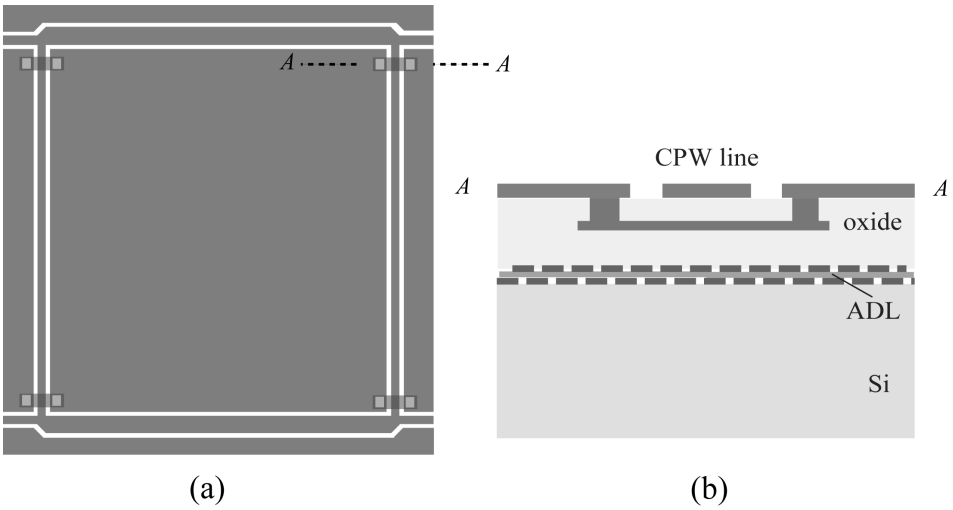

Figure 4.21: Schematic top view (a) and cross section view (b) of directional coupler with CPW configuration.

Fig. 4.22 compares the simulated S-parameters of the branch-line coupler with (solid markers) and without (hollow markers) the ADL shield. Without the ADL shield, the coupler shows an insertion loss of 6.3 dB and coupling of 7.4 dB respectively at 20 GHz. Compared with the ideal coupler behavior, 3.3 dB and 4.4 dB of loss is generated during the power transfer from input port (port 1) to through port (port 2) and coupled port (port 3), which is caused by the substrate loss and metal loss of the CPW lines. With the ADL shield in place, an insertion loss of 4.3 dB and a coupling of 4.4 dB at 20 GHz can be achieved. The 2 dB loss reduction at the through port and 3 dB loss reduction at the

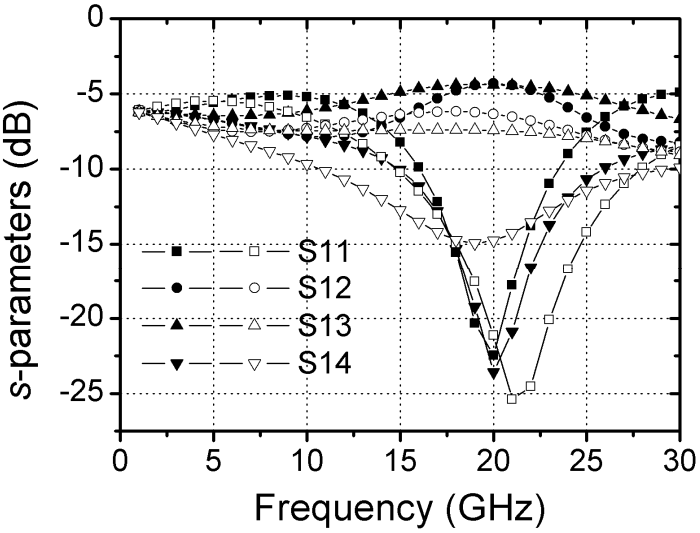

Figure 4.22: Simulated magnitudes of *s*-parameters (in dB) of CPW branch-line couplers on Si with (solid markers) and without (hollow markers) ADL shields.

coupled port are due to the shielding effect of the ADL.

Based on the simulation results, CPW based branch-line couplers with and without ADL shields were designed and fabricated on ordinary Si wafer. The fabrication processes are similar to the ones described in section 4.4.1, except that the 9 μm PECVD oxide layer was deposited in two steps. After the first 6 μm oxide deposition, a metal layer of 0.6 μm in thickness was grown and patterned to form the underneath bridge as shown in Fig. 4.21(b). The other 3 μm oxide was then formed and vias were opened before the last metallization step to form the CPWs. Due to the limitation of our measurement facilities, 2-port S-parameter measurement could be performed with the other two ports open. However, it can be shown that, under this circumstance, with z-parameters of each pair of two ports, the four port z-parameter matrix can be easily constructed by simply combining the two port z-parameters. The four port z-parameter matrix was then converted back to S-parameter matrix to extract the characteristic quantities of the branch-line couplers.

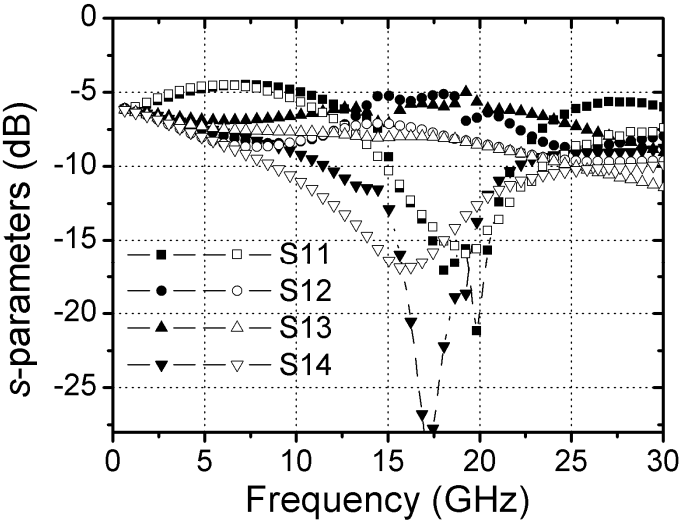

Figure 4.23: Measured magnitudes of *s*-parameters (in dB) of CPW branch-line couplers on Si with (solid markers) and without (hollow markers) ADL shields.

Fig. 4.23 shows the extracted magnitudes of S-parameters from measurements. Due to the uncertainty in the substrate resistivity (nominal value: 5-10 Ωcm, 10 Ωcm was assumed in simulation), deviation of characteristic impedances as well as phase velocities from simulations can be expected. Therefore, in the experiments, the minimum values of S11 and S14 were achieved at different frequencies. Nevertheless, the loss reduction by applying ADL shields is clearly demonstrated if one looks at S12 and S13 values in a certain bandwidth near the central design frequency.

4.5.3 Ring hybrids

180° or quadrature hybrids are hybrid couplers with a 180° phase difference in the two output ports. It can also be operated so that the outputs are in phase. Ideally, referred to Fig. 4.18, a signal applied to port 1 is equally split into two in-phase components at ports 2 and 3. While input at port 4 will be evenly split into two components at ports 2 and 3 with 180° phase differences. 180° hybrids are often used as a combiner. With input signals at ports 2 and 3, the sum of the inputs will be formed at port 1, while the difference will be formed at port 4. Therefore, ports 1 and 4 are also referred to as the sum and difference ports. The scattering matrix for an ideal 180° hybrid takes the following form:

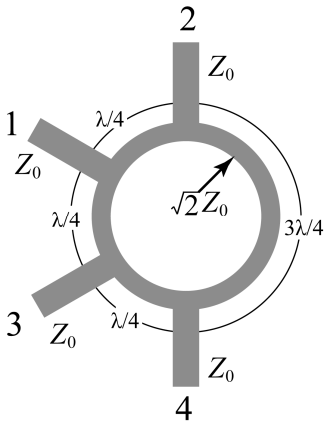

Figure 4.24: Geometry of a ring hybrid in microstrip form. Power entered at port 1 are equally distributes to port 2 and 3, with no power coupled to port 4.

$$[s] = \frac{-j}{\sqrt{2}} \begin{bmatrix} 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & -1 \\ 1 & 0 & 0 & 1 \\ 0 & -1 & 1 & 0 \end{bmatrix}. \tag{4.22}$$

The 180° hybrids can be realized in different forms. In silicon technologies, the ring hybrid, also known as rat-race, is usually the choice of fabrication due to its planar structure. A ring hybrid in microstrip form is schematically shown in Fig. 4.24 and the frequency response of an ideal ring hybrid is shown in Fig. 4.25. At design frequency (20 GHz), power inputted in port 1 is evenly (3 dB) split into port 2 and 3 without any power returned back. Also port 4 is perfectly isolated. It is also shown in Fig. 4.25 that S-parameters are symmetric about the design frequency.

Ring hybrids using CPW lines were designed and simulated in ADS to demonstrate the loss reduction effect of ADL shields. The layout is schematically shown in Fig. 4.26, where, similar to the branch-line coupler, additional metal bridge and through dielectric vias are implemented. Fig. 4.27 compares the magnitudes of simulated S-parameters of ring hybrids with (solid markers) and without (hollow markers) ADL shields. In the unshielded case, the insertion loss and coupling are found to be 6.7dB and 6.1dB at 20 GHz, respectively. Also notice the obvious asymmetry of all S-parameters about the

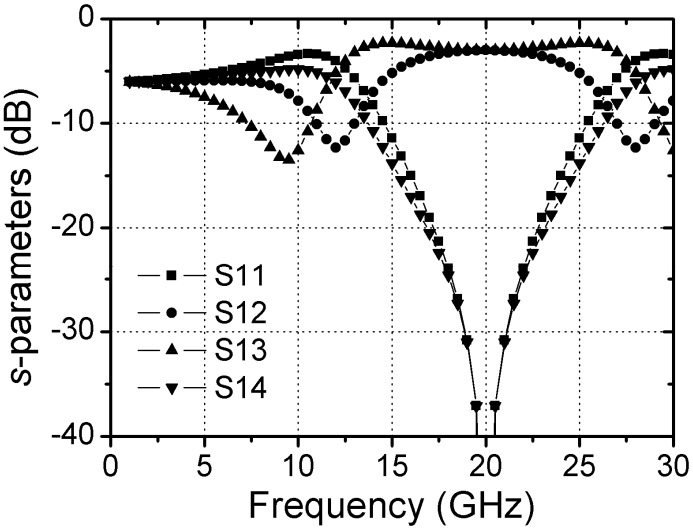

Figure 4.25: Magnitudes of *s*-parameters (in dB) of an ideal ring hybrid as a function of frequency.

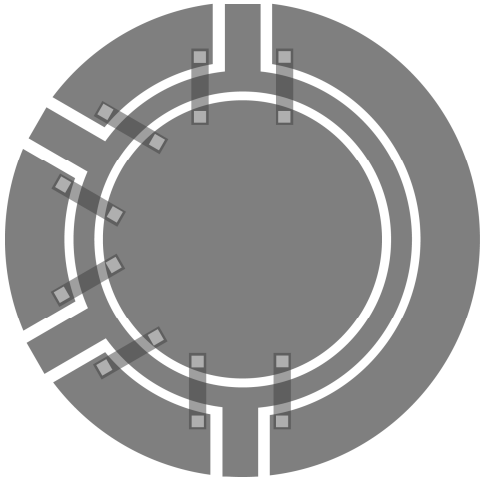

Figure 4.26: Schematic top view of the layout of a ring hybrid in CPW form. Additional metal bridge under the CPW layer is added and connected to CPW grounds by through dielectric vias.

central design frequency, which is due to high substrate loss at high frequencies. When ADL shields are inserted between the Si substrate and the CPW lines, the ring hybrid shows a 4.0dB insertion loss and 3.8dB coupling, which are 2.7dB and 2.3dB lower than the unshielded case. Besides, the shielded ring hybrid shows a more symmetric behavior about the design frequency.

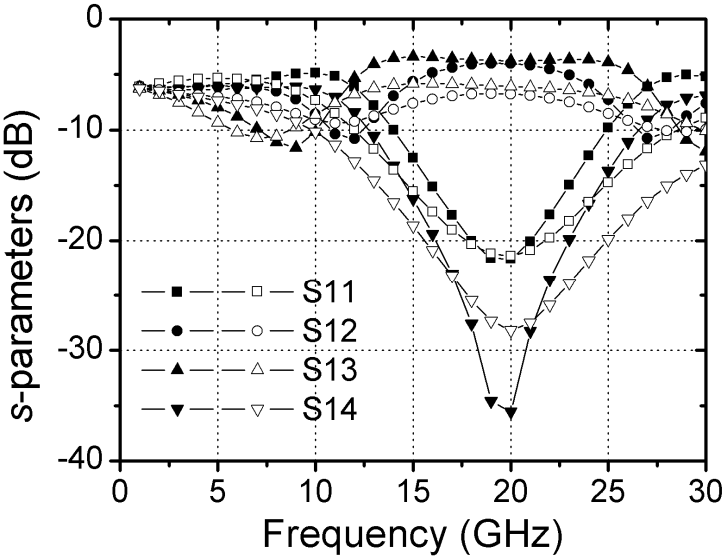

Figure 4.27: Simulated magnitudes of *s*-parameters (in dB) of CPW ring hybrids on Si with (solid markers) and without (hollow markers) ADL shields as a function of frequency.

4.6 Application of ADL shields to spiral inductors

On-chip spiral inductors are nowadays viewed as key components in monolithic RF/microwave circuits. But, as the same time, they are one of the main performance limiting components of integrated RF circuits. The quality factor (Q-factor) of spiral inductors is limited by the conductor loss in the spiral coils as well as substrate loss primarily caused by the unwanted currents flowing in the conductive Si substrate [16]. Similar to the integrated transmission lines, efforts have been made to reduce the substrate loss by using electric shields [17]. In this section, we investigate the application of the high-k ADL shields for the reduction of the substrate loss of integrated spiral coils..

4.6.1 Principles of operation

Substrate loss reduction of spiral inductors by applying ADL shields can be understood by considering the simplified equivalent lumped element model of Fig. 4.28 [16, 18-19]. which also shows the geometry (cross sectional view) of the inductors with and without the ADL shields. The spiral coil itself is represented by the inductance L_s and series resistance R_s which accounts for the conductor loss. C_{ox} represents the oxide capacitance between spiral coil and the substrate. The Si substrate is modeled by C_{si} and R_{si} with the latter accounting for the losses in the substrate. For simplicity, here we ignore the inter-wire capacitance. It should be pointed out that due to its inherent asymmetry of spiral inductor layout, the shunt elements in the π-type model are not necessarily symmetric (i.e. for example, C_{ox1} is not equal to C_{ox2}). The quality factor (Q) of the spiral inductor is defined as the ratio between the imaginary part and real part of input impedance at port 1 when port 2 is grounded [15]. When the ADL layer is inserted between the spiral coil and the substrate, extra shunt capacitances represented by C_{ADL} in Fig. 4.28(d) is added to the lumped element model. This provides a low impedance route for RF current to flow through, bypassing the substrate resistance. However, a side effect of this extra capacitance is that it will also decrease the self resonance frequency of the inductor. Therefore, a tradeoff has to be made to get sufficient shield effect while keeping the self resonance frequency far enough from the working frequency.

4.6.2 Results and discussions

To test the effectiveness of ADL shields for spiral inductors, simulations were carried out in ADS. First, a conventional spiral inductor built on a SiO_2/Si substrate was simulated and the values of the lumped elements in Fig. 4.28(c) were extracted from the simulated S-parameters. Different values of C_{ADL} in a certain range (which can be estimated by the geometry of the spiral coil and the in-plane dielectric constant of ADL) were then assigned in Fig.4.28(d). The quality factor (Q) as a function of frequency was then calculated from the S-parameter simulations with and without C_{ADL}.

Fig.4.29 shows the simulated quality factor Q as a function of frequency for different values of C_{ADL}. Without the shield, the maximum value of quality factor (Q_{max}) is 13.6 at 1.9 GHz. When C_{ADL} is 0.1 pF, a Q_{max} of 15.5 (14% increase), is obtained at 2.4 GHz. With C_{ADL} of 0.5 pF, we have a Q_{max} of 23.9 at 3.9 GHz, an almost 76% improvement. It is noticed that the frequency at which Q_{max} is reached increases with increasing C_{ADL}. It can also be observed from Fig.4.29 that the self resonance frequency of the inductor (the frequency at which Q=0) decreases with increasing ADL capacitance. This is because the

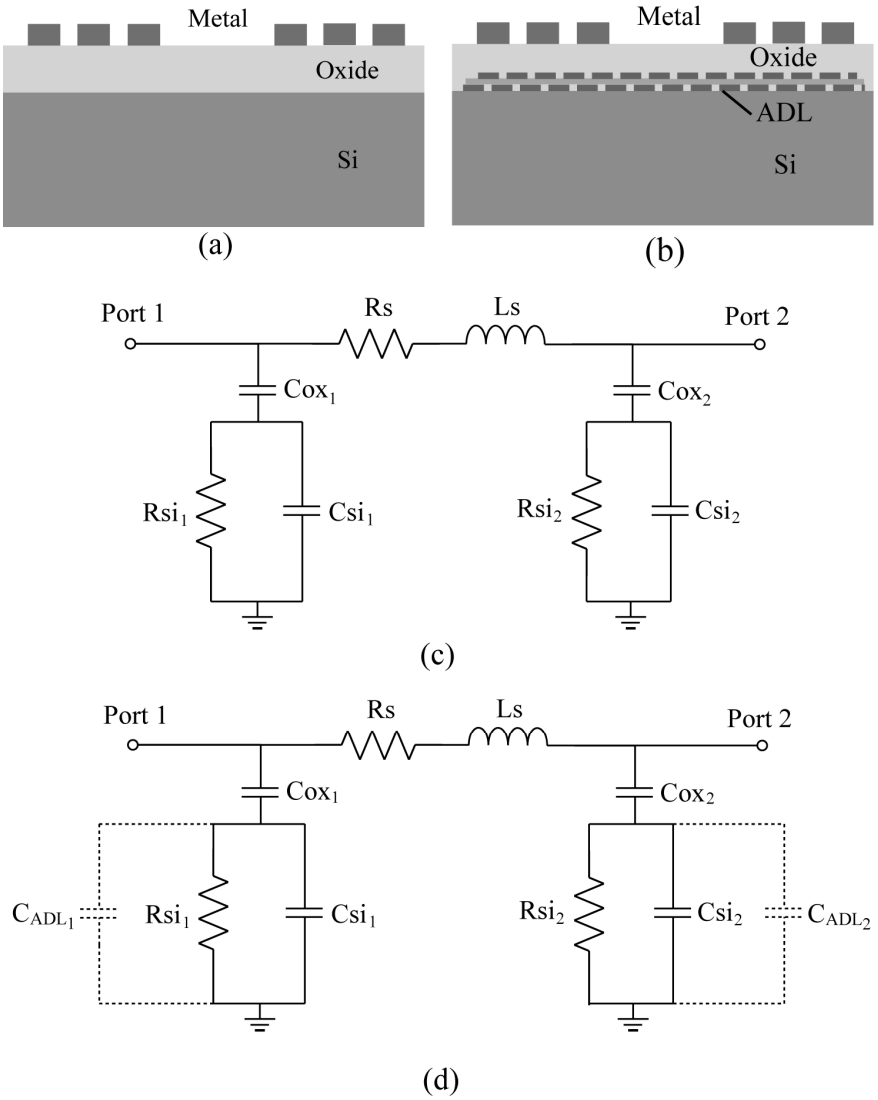

Figure 4.28: Cross section views of spiral inductors (a) on Si substrate without ADL shields and (b) with ADL shields. Also shown simplified equivalent lumped element models of spiral inductors (c) on Si substrate without ADL shields and (d) with ADL shields.

total shunt capacitance in the π-type equivalent model of Fig.4.28 increases as C_{ADL} increases.

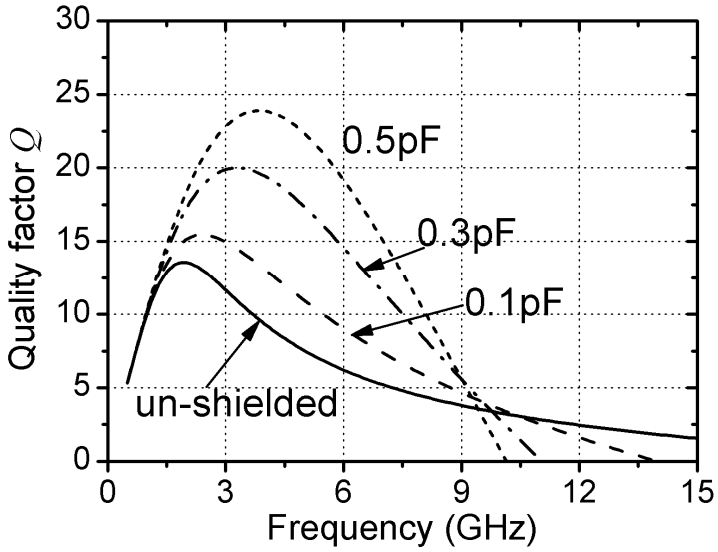

Figure 4.29: Simulated quality factor of a 1.5nH spiral inductor as a function of frequency with different values of C_{ADL}.

For experimental verification, spiral inductors with square shape coils and equipped with ADL shields were fabricated on a 5-10 Ωcm Si substrate. The metallic element size of the ADL shield was chosen to be 15x15 μm^2 to achieve a high in-plane dielectric constant . Due to the strong magnetic field generated by the spiral, which is expected to induce relatively large eddy currents in the ADL patterns, spiral inductors with ordinary ADL (ADL-Ind) and micro-patterned ADL (μADL-Ind) were fabricated for comparison (refer to Fig. 4.14). The ones without any ADL shield (U-Ind) were made as well on the same wafer.

Fig. 4.30 shows the extracted quality factor and inductance values for a ~2 nH inductor. Compared with unshielded coil, the shielded devices show an improvement of the Q-factor in a wide frequency range. In particular, a 17% increase of the Q_{max} is achieved by the use of micro-patterned ADL shields. This can be understood by considering the equivalent lumped element model as shown in Fig. 4.28. The quality factor Q of an inductor without ADL shields can be expressed as

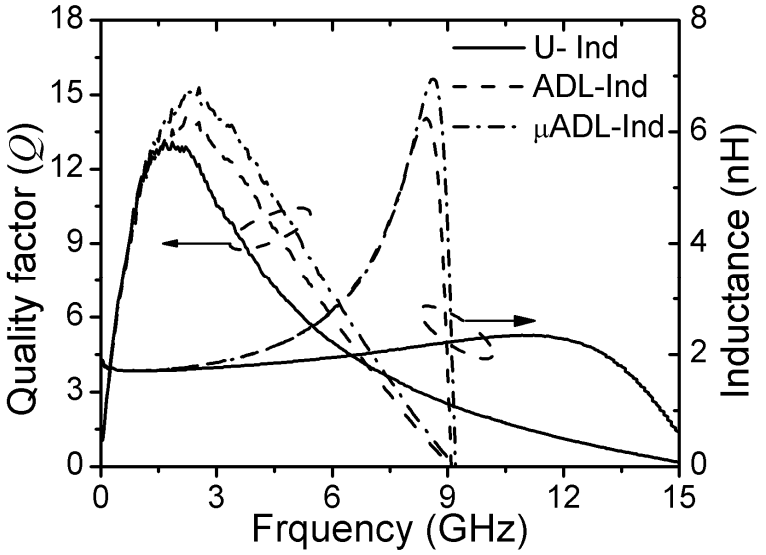

Figure 4.30: Measured quality factor and inductance value of a 2nH spiral inductor as a function of frequency with ordinary (ADL-Ind) and micro-patterned (μADL-Ind) ADL shields. Results for un-shielded spiral inductor (U-Ind) are shown as well for comparison.

$$\frac{1}{Q} = \frac{1}{Q_s} + \frac{1}{Q_c}, \tag{4.23}$$

where $Q_s = \omega L_s / R_s$ and

$$Q_c = \frac{1 + \omega^2 R_{\mathrm{si}}{}^2 C_{\mathrm{si}} (C_{\mathrm{ox}} + C_{\mathrm{si}})}{\omega R_{\mathrm{si}} C_{\mathrm{ox}}}. \tag{4.24}$$

Since we ground port 2 when calculating the quality factor, the resistance and capacitance values are taken from the left shunt branch in Fig. 4.28(b). At relatively low frequencies (roughly speaking, below 1 GHz), the overall quality factor is limited by the conductor loss which is represented by Q_s and has a small value. Therefore, in this frequency range, inclusion of the ADL shield does not strongly affect Q. As frequency ramps up, Q_s increases and becomes comparable to Q_c so that the influence of Q_c on the overall Q becomes more predominant. The effect of the ADL shields can be modeled as an extra

capacitance C_{ADL} added to C_{si} in Eq. 4.24. It is apparent that this will lead to an increment of Q_c and therefore an improvement of Q. It is also noticed in Fig. 4.30 that, compared with the original ADL shield, the micro-patterned one has slightly higher Q over most of the frequency range. This again can be understood from the equivalent circuit model shown in Fig. 4.28. The ohmic loss due to eddy current flow inside the ADL metallic patterns can be lumped into the series resistance R_s in Fig.4.28(c). By cutting slots in the metallic element, eddy current flow is effectively suppressed, leading to a reduction of R_s as compared to ordinary ADL shields. Therefore, the quality factor Q_s of the series branch is improved, so as to the overall quality factor Q of the inductor. The frequency at which Q_{max} is achieved shifts to higher values when ADL shields are applied, which is in agreement with our simulation results. It is also clear from the figure that the self-resonance frequencies of the spiral inductors are reduced by applying ADL shields as expected.

4.7 Conclusions

In this chapter, we presented and investigated a novel method for reducing the substrate loss of Si-based integrated transmission lines. The method exploits the shielding effect of an ADL with a high in-plane dielectric constant. The ADL comprises two patterned metal layers separated by a thin conventional dielectric, and can be readily built in a standard IC process. It was found that the ADL shield significantly lowers the attenuation, but only moderately changes the characteristic impedance of the transmission lines. The shield effectiveness of ADL was experimentally shown to be improved by increasing the metallic element size, while micro-patterning the ADL to suppress the eddy current loss. By this way, CPW built on ordinary conductive silicon showed comparable total attenuation as the one fabricated on HRS substrate. We also showed that the shield effectiveness can be improved by stacking a few ADL layers. Loss reduction of CPW based microwave devices, i.e. branch-line coupler and ring hybrid, by applying ADL shields were demonstrated by simulation and experiment. Application of ADL shields to spiral inductors was also analyzed with the help of a simplified lumped element model and was experimentally demonstrated.

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Chapter 5

On-chip Artificial Dielectric Resonators for Microwave Applications

5.1 Introduction

Microwave resonators are important components in microwave circuits, and are used in a variety of applications, including filters, oscillators, frequency meters and tuned amplifiers [1]. From a physical point of view, energy is stored inside a resonator through electromagnetic fields. Resonance occurs at certain frequencies when the time average stored electric and magnetic energies are equal. The input impedance of a resonator at resonance is purely real since the reactance is proportional to the difference between electric and magnetic energy storage.

The quality factor (Q-factor or simply Q) is an important figure of merit to characterize a resonance circuit, and is defined as

$$Q = \omega \frac{\text{average energy stored}}{\text{power loss}} = \omega \frac{W_e + W_m}{P_i}, \tag{5.1}$$

where ω is the angular frequency, W_e and W_m denote average electric and magnetic energy stored in the resonance circuit respectively, and P_i is power dissipated in the resonance circuit itself[1]. To a very good approximation, the quality factor can also be expressed as

$$Q = \frac{f_0}{\Delta f} = \frac{f_0}{|f_1 - f_2|}, \tag{5.2}$$

where f_0 is the resonance frequency, f_1 and f_2 are half power frequencies.

In order to be applied in a microwave circuit, a microwave resonator must deliver power to an external load. The power loss due to the presence of an external load results in the external quality factor Q_e, which is defined as

$$Q_e = \omega \frac{W}{P_e}, \tag{5.3}$$

where W is the total electric and magnetic energy stored in the resonance circuit, and P_e is the power delivered to the external load. We can also define the loaded quality factor, Q_L, which is the total Q of the system including power losses both internal and external to the resonator. Since the total power loss is simply the sum of the internal power loss of P_i and the external power loss P_e, one obtains

$$\frac{1}{Q_L} = \frac{1}{Q_e} + \frac{1}{Q_0}, \tag{5.4}$$

where Q_0 is the quality factor of the resonator itself as defined in Eq. (5.1), also known as unloaded Q.

Microwave resonators can be realized in different forms, i.e. lumped element resonators (*RLC* resonant circuit), transmission line resonators, cavity resonators (also known as waveguide resonators) and dielectric resonators. The lumped element resonators are simply the parallel or series *RLC* resonant circuits where lumped inductor and capacitor are parallel or series connected to form the resonant circuit. This realization is normally simple and gives a compact circuit. In microwave integrated circuits the

quality factor of the resonator is limited by the lumped inductor, especially at high frequencies [2]. Therefore, lumped element resonators are normally realized on low loss substrates [3] and/or at relatively low frequencies [4], where substrate loss is small [2]. Even in that case, however, the quality factor of the integrated inductor (and, thus, the resonator) can hardly exceed a value of 50 due to conductor loss which is further enhanced by the skin effect at high microwave frequencies. An alternative to lumped-element resonator is provided by distributed element resonators which are usually based on transmission lines. From transmission line theory, it follows that a short- or open-circuited transmission line can resonate at frequencies where its electric length becomes a multiple of a quarter of the propagation wavelength on the line. The unloaded quality factor for such a resonator is given by

$$Q_0 = \frac{\beta}{2\alpha}, \tag{5.5}$$

where β is the propagation constant and α is the attenuation constant of the line [1]. For MMIC application on Si, on-chip transmission lines can be realized by a microstrip or coplanar waveguide (CPW). However, the quality factor of these lines is limited by substrate loss in conductive Si and metal loss mainly in the signal line, especially at high frequencies (tens of GHz) As shown in Cheung's work, the quality factor of a 50 Ω microstrip line on a 10 Ω·cm Si substrate is below 15 at 30 GHz. And even on a semi-insulated alumina substrate, a CPW line of 50 Ω shows a quality factor not exceeding 40 below 40 GHz [6].

In term of quality factor, nothing can surpass the cavity resonator, which is constructed by using a section of a rectangular or cylindrical waveguide. Because of radiation loss of an open-ended waveguide, waveguide resonators are usually short circuited at both ends, forming a closed, hollow box which stores electric and magnetic energies. Although power is dissipated in the metallic walls of the cavity, very high *Q*-factors (tens of thousands) can be obtained [1]. However, although cavity resonators are extensively used in discrete or a hybrid microwave system, they are difficult to integrate with the standard IC technology. This is because the lateral dimensions of a cavity resonator should at least equal have the electromagnetic wavelength in air which is quite large compared to chip dimensions. Besides, their fabrication requires substrate micromachining techniques [7,8] which significantly complicates the process integration and therefore increases the fabrication cost.

Whereas in a cavity resonator the metallic walls are responsible for the field confinement, a dielectric resonator employs the high (relative) dielectric constant of a small disc or cube of low loss dielectric material. The high dielectric constant of the resonator material ensures that most of the electromagnetic field is contained within the resonator, with little fringing or leakage from the sides and ends of the dielectric resonator. Due to the high dielectric constant, the size of dielectric resonator is considerably smaller than that of an empty resonant cavity operating at the same frequency. Conductor losses are absent in a dielectric resonator and therefore Q of up to several thousand can be achieved [1]. Dielectric resonators are usually sealed on solid state devices to form certain microwave systems such as wireless front-end transceivers. Because of their high Q factor, dielectric resonators are needed in such system to have low insertion loss, high out of band rejection, and high channel to channel isolation. However, compared with the solid state devices, dielectric resonators are much more expensive and area consuming. Therefore, for MMIC applications, it will be attractive if one could integrate dielectric resonator on chip and shrink the size significantly, while still keep the high Q factor.

The size of the dielectric resonator is approximately proportional to the wavelength at resonance frequency, which is inversely proportional to the square root of dielectric constant. Obviously, to make the dielectric resonator compact, dielectric materials with very high dielectric constant are needed. However, even for ferroelectric materials, in their thin film form, a dielectric constant of 1000 is hardly achieved. Besides, as we remarked in the previous chapter, there is no guarantee that the dielectric loss of these materials remains low at microwave frequencies.

Could we then use artificial dielectric constructions, as we did in the previous section, to emulate high-k dielectrics? In this chapter, we will try to answer this question by investigating a new type of on-chip resonator, based on artificial dielectric layer (ADL) disk. The resonator may be excited by a conventional metallic structure, i.e., a metal ring surrounding the ADL disk. To better understand the operation of the device, a physical model based on Maxwell's equations will be deduced, in which we model the ADL as an effective material, i.e. a continuous anisotropic media with effective permittivity and permeability tensors. It will be shown that every resonance mode of the ADL disk can be modeled as a normal parallel *RLC* resonator and coupled to the self inductance of the metal ring through a mutual inductance. We will then compare the results obtained with the full-wave numerical calculations carried out using HFSS (High Frequency Simulation

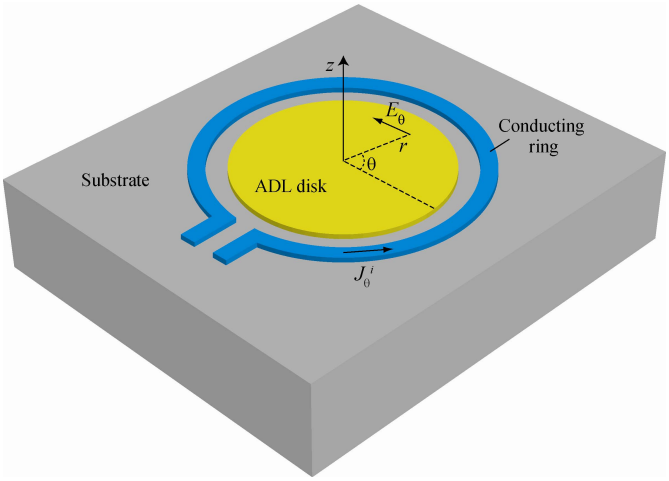

Figure 5.1: schematic of the ADL disk resonator. A conductive, current-carrying ring encloses a thin disk of artificial dielectric with the radius *R*. The ring and the disk are placed on top of a substrate which is assumed to be unbounded in the horizontal plane. The current flowing through the ring is considered as an impressed source, inducing an electromagnetic field with the components E_θ, H_r, H_z in the system.

System), as well as experimental data from ADL disk resonators fabricated on a low-loss substrate (AF 45 glass wafer).

5.2 Theoretical analysis of artificial dielectric resonator

5.2.1 Configuration and theoretical model

As shown in Fig. 5.1, we assume a cylindrically symmetric configuration comprising a dielectric (ADL) disk of radius *R* encircled by a metallic ring carrying a current with the density

$$\boldsymbol{J}^i = J_\theta^i(r,z)\hat{\boldsymbol{\theta}} \qquad (5.6)$$

with $\hat{\boldsymbol{\theta}}$ the unit vector in the azimuthal direction. We neglect the influence of the ADL disk on $\boldsymbol{J}^i$, viewing the latter as an impressed source. The ring and the disk are assumed to be placed above a laterally unbounded, stratified substrate.

Inside the ADL disk the distribution of the electric (***E***) and magnetic (***H***) fields is

governed by the Maxwell equations

$$\frac{\partial E_\theta}{\partial z} = j\omega\mu_0 H_r \tag{5.7}$$

$$\frac{\partial}{r\partial r}\left(rE_\theta\right) = -j\omega\mu_\perp H_z \tag{5.8}$$

$$\frac{\partial H_r}{\partial z} - \frac{\partial H_z}{\partial r} = j\omega\varepsilon_\parallel E_\theta + J_\theta^i, \tag{5.9}$$

where the indices r,θ,z represent the field components in the radial, azimuthal, and vertical directions. Here we model the ADL disk as an effective material with its effective in-plane dielectric constant $\varepsilon_\parallel$, and effective perpendicular permeability $\mu_\perp$. The latter differs from the vacuum permeability μ_0 because of the flow of local eddy currents in the individual metallic patterns comprising the ADL. For the moment, we neglect the effect of $\mu_\perp$, and assume the latter to be equal to μ_0.

Instead of directly solving the Maxwell equations inside the ADL, we view the latter as a volume source of electric polarization currents given by

$$J_\theta^P = j\omega(\varepsilon_\parallel - \varepsilon_0)E_\theta. \tag{5.10}$$

Assume now that $(-j\omega\mu_0 r')G(r,z\,|\,r',z')$ is the Green's function describing the azimuthal electric field induced at r,z by an infinitesimally thin ring of current placed above the substrate at r',z' (in the absence of the ADL disk). At any point in space, the total electric field generated by the impressed and polarization currents can be written as

$$E_\theta(r,z) = -j\omega\mu_0 \int_{\Omega_D} G(r,z\,|\,r',z')J_\theta^P(r',z')ds' + E_\theta^i(r,z) \tag{5.11}$$

$$E_\theta^i(r,z) = -j\omega\mu_0 \int_{\Omega_i} G(r,z\,|\,r',z')J_\theta^i(r',z')ds', \tag{5.12}$$

where Ω_D and Ω_i denote the cross sections of the disk and the current source in the *r-z* plane (as shown in Fig. 5.2), respectively, and $ds' = r'dr'dz'$. In the above equation E_θ^i is the (external) field generated by the impressed source alone. Note that G is frequency dependent, but this is not explicitly shown. By considering the points inside the ADL, and combining Eqs.(5.10-5.11), one obtains the two-dimensional integral

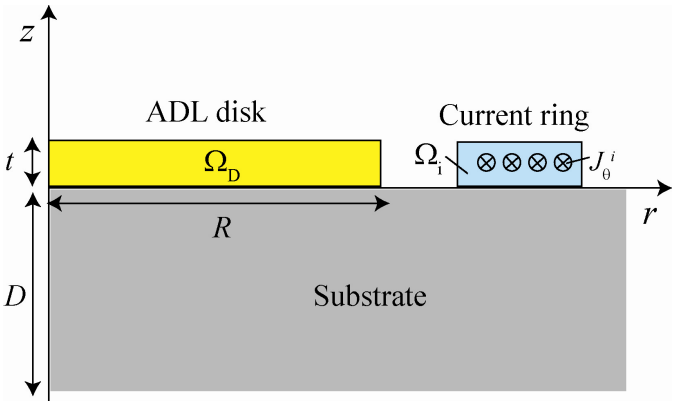

Figure 5.2: Cross section of the system in the r-z plane. The cross section of the ADL disk and the current-carrying ring are denoted by Ω_D and Ω_i, respectively.

equation:

$$E_\theta(r,z) = \omega^2 \mu_0 \Delta\varepsilon \int_{\Omega_D} G(r,z \mid r',z') E_\theta(r',z') ds' + E_\theta^i(r,z), \tag{5.13}$$

where $\Delta\varepsilon = \varepsilon_{\parallel} - \varepsilon_0$. Solving this equation for a given external field yields the distribution of the electric field inside the disk.

Modal expansion

Consider now the eigenvalue problem defined on Ω_D by the equation

$$\int_{\Omega_D} G(r,z \mid r',z') \psi_k(r',z') ds' = \lambda_k \psi_k(r,z), \tag{5.14}$$

where ψ_k and λ_k are the (complex) eigenfunctions and eigenvalues of the integral operator G. (They both depend on frequency as does G.) Since G is symmetric (it does not change under the simultaneous replacements $r \leftrightarrow r', z \leftrightarrow z'$), it follows that ψ_k form an orthogonal set which, upon proper normalization of ψ_k, yields

$$\int_{\Omega_D} \psi_k(r,z) \psi_m(r,z) ds = \delta_{km}, \tag{5.15}$$

where δ_{km} is the Kronecker delta. Furthermore, we assume that the set of the

eigenfunctions ψ_k is complete so that every arbitrary function defined on Ω_D can be expanded as a series in ψ_k. Therefore, we can write:

$$E_\theta(r,z) = \sum_{k=0}^{\infty} c_k \psi_k(r,z) \,. \tag{5.16}$$

Upon substituting Eq. (5.16) into Eq. (5.13), and using Eqs. (5.14-15), solving for a_k, and returning to Eq. (5.16) one obtains

$$c_k = \frac{-j\omega\mu_0 A_k}{1-\lambda_k \omega^2 \mu_0 \Delta\varepsilon} \,, \tag{5.17}$$

where

$$A_k = \int_{\Omega_D}\int_{\Omega_i} \psi_k(r,z) G(r,z \mid r',z') J_\theta^i(r',z') ds ds' \,. \tag{5.18}$$

From Eq. (5.16), we then have

$$E_\theta(r,z) = \left(-j\omega\mu_0\right) \sum_{k=1}^{\infty} \frac{A_k \psi_k(r,z)}{1-\lambda_k \omega^2 \mu_0 \Delta\varepsilon} \,. \tag{5.19}$$

5.2.2 Equivalent circuit model

To have a better understanding of the operation of the ADL-disk resonator, it is instructive represent the latter by an equivalent circuit model. This will be achieved by first calculating the impedance of the ring, from which an equivalent circuit model will be developed.

To calculate the impedance Z of the ring, consider the total complex power P delivered to the system by the impressed source, which is given by

$$P = -\frac{1}{2}\int_{\Omega_i} E_\theta \left(J_\theta^i\right)^* ds = \frac{1}{2} Z \mid I \mid^2 \,, \tag{5.20}$$

where I is the total current flowing through the ring. Using Eqs. (5.10-12, 5.20), the impedance of the ring can be expressed as

$$Z = Z^i + Z^D \quad , \tag{5.21}$$

where

$$Z^i = \frac{j\omega\mu_0}{|I|^2}\int_{\Omega_i}\int_{\Omega_i}\left[J_\theta^i(r,z)\right]^* G(r,z\,|\,r',z')J_\theta^i(r',z')dsds' \tag{5.22}$$

is the self-impedance of the current ring (when no disk is present). The term Z^D represents the contribution of the ADL disk to the impedance, and is given by

$$Z^D = -\frac{\omega^2\mu_0\Delta\varepsilon}{|I|^2}\int_{\Omega_i}\int_{\Omega_D}\left[J_\theta^i(r,z)\right]^* G(r,z\,|\,r',z')E_\theta(r',z')dsds' . \tag{5.23}$$

Using the expansion (5.19), Eq. (5.23) can be written as

$$Z^D = \frac{\omega^2\mu_0\Delta\varepsilon}{|I|^2}\sum_{k=1}^{\infty}\frac{\left(j\omega\mu_0\right)A_k\overline{A}_k}{1-\lambda_k\omega^2\mu_0\Delta\varepsilon}, \tag{5.24}$$

$$\overline{A}_k = \int_{\Omega_i}\int_{\Omega_D}\left[J_\theta^i(r,z)\right]^* G(r,z\,|\,r',z')\psi_k(r',z')dsds' . \tag{5.25}$$

The above result can be represented by the equivalent lumped-element model of Fig. 5.3 as we discuss below. Consider the current carrying ring as the primary winding of a transformer with an infinite number of independent secondary windings (corresponding to different eigenmodes of the disk) all coupled to the primary winding. Let us define the impedance matrix of the transformer as

$$\boldsymbol{Z}_{tr} = j\omega\begin{bmatrix} L_P & M_1 & M_2 & M_3 & \cdots \\ M_1 & L_{s,1} & 0 & 0 & 0 \\ M_2 & 0 & L_{s,2} & 0 & 0 \\ M_3 & 0 & 0 & L_{s,3} & 0 \\ \vdots & 0 & 0 & 0 & \ddots \end{bmatrix}, \tag{5.26}$$

where $L_p = Z^i / j\omega$ is the self inductance of the primary winding, $L_k = \mu_0\lambda_k / t$ is the self inductance of the k-th secondary winding, and $M_k = \mu_0\left(\overline{A}_k A_k / |I|^2\, t\right)^{1/2}$ is the mutual inductance between the latter and the primary winding. (The division by the disk thickness t is to ensure the correct physical dimension for the inductances, but is arbitrary otherwise. Any other length scale could have been used instead of t.) It can

then be shown that the impedance Z (Eq. 5.21) is identical to the impedance seen at the input of the primary winding with all secondary windings terminated by capacitances all equal to $C = t\Delta\varepsilon$. The conductive ring is thus magnetically coupled to an infinite number of parallel *LC* resonators.

Note that the eigenvalues λ_k and, therefore, the inductances L_k are generally complex and frequency-dependent. The imaginary part of $L_k = L_k' - jL_k'' = (\mu_0 / t)(\lambda_k' - j\lambda_k'')$ is related to the polarization loss of the dielectric substrate, as well as radiation into space and surface waves of the substrate. The capacitance C is also generally complex due to the polarization loss of the artificial dielectric disk, i.e. $C = C' - jC'' = t\left[(\varepsilon_{\parallel}' - \varepsilon_0) - j\varepsilon_{\parallel}''\right]$.

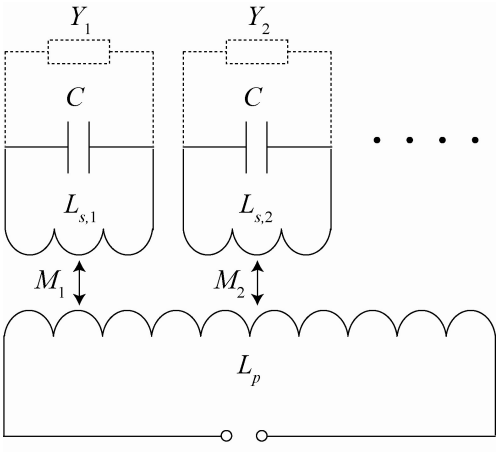

Figure 5.3: Equivalent circuit of an ADL disk resonator. Note that, in general, all the component values are complex and frequency dependent.

Provided that the losses are small (i.e. $L_k' \gg L_k''$, $C' \gg C''$) each eigenmode of the disk will resonate at a frequency $\omega = \omega_k$ satisfying the equation

$$\omega^2 L_k'(\omega) C' = 1 . \tag{5.27}$$

The quality factor Q of the resonator is then given by

$$\frac{1}{Q} = \frac{1}{Q_k^L} + \frac{1}{Q^C}, \tag{5.28}$$

where

$$Q_k^L = \frac{L_k'(\omega_k)}{L_k''(\omega_k)} = \frac{\lambda_k'(\omega_k)}{\lambda_k''(\omega_k)} \tag{5.29}$$

$$Q^C = \frac{C'}{C''} = \frac{\varepsilon_{\|}' - \varepsilon_0}{\varepsilon_{\|}''} \approx \frac{\varepsilon_{\|}'}{\varepsilon_{\|}''} = \left(\tan\delta\right)^{-1}. \tag{5.30}$$

The approximation in the last equation is justified since $\varepsilon_{\|}' \gg \varepsilon_0$, and $\tan\delta$ is the effective loss tangent of the ADL.

Now we would like to include the effect of the magnetic losses by perturbation theory. To that end, consider the perpendicular magnetization M_z defined by

$$M_z = \chi_{\perp} H_z, \tag{5.31}$$

where $\chi_{\perp} = \mu_{\perp} / \mu_0 - 1$ is the perpendicular susceptibility of the ADL. Like the electric polarization, the effect of M_z can be taken account of by an equivalent current which is now given by $J_{\theta}^M = -\dfrac{\partial M_z}{\partial r}$. The extra electric field generated by this current can once again be represented in terms of the Green's function G:

$$E_{\theta}^M(r,z) = \gamma \int_{\Omega_D} \frac{\partial}{r'\partial r'}\left[r' G(r,z \mid r',z')\right] \frac{\partial}{r'\partial r'}\left[r' E_{\theta}(r',z')\right] ds' \tag{5.32}$$

$$\gamma = \frac{\chi_{\perp}}{\chi_{\perp} + 1} = 1 - \frac{\mu_0}{\mu_{\perp}}, \tag{5.33}$$

where we have used partial integration, together with Eqs. (5.8) and (5.31). The total electric field at any point in space is now given by adding the field E_{θ}^M to the right hand side of Eq. (5.13):

$$E_{\theta}(r,z) = \omega^2 \mu_0 \Delta\varepsilon \int_{\Omega_D} G(r,z \mid r',z') E_{\theta}(r',z') ds' + E_{\theta}^M(r,z) + E_{\theta}^i(r,z). \tag{5.34}$$

We next insert the expansion (5.16) into the above equation, multiply both sides by the

eigenfunctions $\psi_k(r,z)$ and perform an integration over the cross section of the ADL disk on the r-z plane. This results in the matrix equation

$$\sum_{m=1}^{\infty}\left[(1-\lambda_k\omega^2\mu_0\Delta\varepsilon)\delta_{km}-\gamma\lambda_k Q_{km}\right]c_m=-j\omega\mu_0 A_k\ , \tag{5.35}$$

where

$$Q_{km}=\int_{\Omega_D}\frac{\partial}{r\partial r}\left[r\psi_k(r,z)\right]\frac{\partial}{r\partial r}\left[r\psi_m(r,z)\right]ds\ . \tag{5.36}$$

If γ is small, the second term on the l.h.s. of Eq. (5.35) can be considered as a perturbation.[1] Up to the first order in the latter, the solution to the above equation can be written as

$$c_k=\frac{\left(-j\omega\mu_0\right)}{1-\lambda_k\omega^2\mu_0\Delta\varepsilon-\gamma\lambda_k Q_{kk}}\left(A_k+\gamma\lambda_k\sum_{m(\neq k)}\frac{Q_{km}A_m}{1-\lambda_m\omega^2\mu_0\Delta\varepsilon-\gamma\lambda_m Q_{mm}}\right). \tag{5.37}$$

In order to calculate the impedance of the ring, we once again use Eq. (5.20). The contribution of the field generated by the electric polarization currents can again be found using Eq. (5.23). However, one should not forget the effect of the field generated by the magnetization which yields the additional impedance

$$Z^M=-\frac{1}{|I|^2}\int_{\Omega_i}E_\theta^M\left(J_\theta^i\right)^*ds\ . \tag{5.38}$$

Using Eqs. (5.16) and (5.32), the above expression can be rewritten as

$$-\frac{\gamma}{|I|^2}\sum_{k=1}^{\infty}a_k\int_{\Omega_i}\int_{\Omega_D}\left[J_\theta^i(r,z)\right]^*\frac{\partial}{r'\partial r'}\left[r'G(r,z\,|\,r',z')\right]\frac{\partial}{r'\partial r'}\left[r'\psi_k(r',z')\right]dsds'\ . \tag{5.39}$$

[1] Actually numerical results show that $\lambda_k\sim c_k Rt$ where c_k of the order of one or smaller. On the other hand, $Q_{mk}\sim d_{mk}/R^2$ where d_{mk} is again of the order of one or smaller. The perturbation is thus of the order of $\gamma(t/R)$. Therefore, for thin films, i.e. $t\ll R$, perturbation theory remains valid even if γ may not be so small.

Since r', z' belong to Ω_D, the function G for $r, z \in \Omega_i$ can be expanded as

$$G(r,z \mid r',z') = \sum_m \psi_m(r',z') \int_{\Omega_D} G(r,z \mid r'',z'')\psi_m(r'',z'')ds'' , \tag{5.40}$$

which, after substitution in Eq. (5.39), leads to

$$-\frac{\gamma}{|I|^2}\sum_{k=1}^{\infty}\sum_{m=1}^{\infty}\bar{A}_m Q_{mk} c_k . \tag{5.41}$$

Adding up Z^D and Z^M, and using Eq. (5.37), one finds that up to the first order in γ:

$$Z^D + Z^M = \frac{(j\omega\mu_0)}{|I|^2}\sum_{k=1}^{\infty}\frac{\left(\omega^2\mu_0\Delta\varepsilon + \gamma Q_{kk}\right)B_k\bar{B}_k}{1-\lambda_k\left(\omega^2\mu_0\Delta\varepsilon + \gamma Q_{kk}\right)} \tag{5.42}$$

$$B_k = A_k + \frac{(\gamma/2)}{\omega^2\mu_0\Delta\varepsilon + \gamma Q_{kk}}\sum_{m(\neq k)}\frac{Q_{km}A_m}{1-\lambda_m\left(\omega^2\mu_0\Delta\varepsilon + \gamma Q_{mm}\right)} \tag{5.43}$$

$$\bar{B}_k = \bar{A}_k + \frac{(\gamma/2)}{\omega^2\mu_0\Delta\varepsilon + \gamma Q_{kk}}\sum_{m(\neq k)}\frac{Q_{km}\bar{A}_m}{1-\lambda_m\left(\omega^2\mu_0\Delta\varepsilon + \gamma Q_{mm}\right)} . \tag{5.44}$$

The circuit interpretation of this result is straightforward. The coupling between the primary and secondary turns of the transformer is now given by $M_k = \mu_0\left(\bar{B}_k B_k / |I|^2\, t\right)^{1/2}$. But, most important, in addition to the capacitance C, each secondary turn sees a shunt admittance (refer to Fig. 5.3)

$$Y_k = -\frac{\gamma Q_{kk} t}{j\omega\mu_0} \quad . \tag{5.45}$$

The real part of $Y_k = Y_k' - jY_k''$ represents a shunt conductance, accounting for the magnetic losses of the resonator. The overall quality factor Q of the device is then given by

$$\frac{1}{Q} = \frac{1}{Q_k^L} + \frac{1}{Q^C} + \frac{1}{Q_k^M} , \tag{5.46}$$

where

$$Q_k^M = \frac{\omega C'}{Y_k'} = \frac{\omega(\varepsilon_{\|}' - \varepsilon_0)t}{Y'}. \tag{5.47}$$

5.2.3 Numerical simulations

On any substrate, the Green's function G can be written as

$$G(r,z \mid r',z') = \int_0^\infty \left[e^{-p_0|z-z'|} + \Gamma(k) e^{-p_0(z+z')} \right] J_1(kr) J_1(kr') \frac{kdk}{2p_0}, \tag{5.48}$$

where $p_0^2 = k^2 - k_0^2$ with $k_0^2 = \omega^2 \mu_0 \varepsilon_0$, $J_1(z)$ is the first order Bessel function of the first kind, and $\Gamma(k)$ describes the reflection coefficient of a wave with the in-plane wave number k impinging on the surface of the substrate at $z = 0$. In case of a homogeneous substrate with the thickness D and dielectric constant ε_s, we have

$$\Gamma(k) = \frac{k_s^2 - k_0^2}{p_0^2 + p_s^2 + 2p_0 p_s \coth(p_s D)}, \tag{5.49}$$

where $p_s^2 = k^2 - k_s^2$ in which $k_s^2 = \omega^2 \mu_0 \varepsilon_s$. If the substrate is bounded from below by a ground plane (which is assumed to be perfectly conductive for simplicity), then

$$\Gamma(k) = \frac{p_0 \tanh(p_s D) - p_s}{p_0 \tanh(p_s D) + p_s}. \tag{5.50}$$

Our aim is now to solve the eigenvalue problem (5.14). This will be numerically carried out employing the Galrekin's technique. To that end, we consider a finite set of test functions $f_n(r,z)$ defined on the cross section of the ADL, and expand each eigenfunction as

$$\psi_k(r,z) = \sum_n u_n^k f_n(r,z). \tag{5.51}$$

We substitute this expansion into (5.14), multiply both sides by $rf_m(r,z)$, and carry out an integration over the disk cross section Ω_D. The result is the (generalized) matrix eigenvalue problem

$$\sum_n \bar{\bar{G}}_{mn} u_n^k = \lambda_k \sum_n \bar{\bar{W}}_{mn} u_n^k \ , \tag{5.52}$$

where

$$\bar{\bar{G}}_{mn} = \int_{\Omega_D} \int_{\Omega_D} f_m(r,z) G(r,z \mid r',z') f_n(r',z') ds ds' \tag{5.53}$$

$$\bar{\bar{W}}_{mn} = \int_{\Omega_D} f_m(r,z) f_n(r,z) ds \ . \tag{5.54}$$

To simplify the calculation we divide the cross section of the disk in rectangular segments and use the test functions

$$f_m(r,z) = \begin{cases} r^{-1} & \text{if } (r,z) \in \Omega_m \\ 0 & \text{otherwise} \end{cases} , \tag{5.55}$$

where Ω_m is the surface of the *m*-th rectangular segment.

Using this method, we have computed ψ_k and λ_k for different disk geometries, and on different substrates. We restrict ourselves to ADLs with a thickness t not exceeding several microns. Even with in-plane dielectric constants of the order of 10^4-10^5, the electromagnetic wavelength in such a material exceeds by several orders of magnitude the film thickness. Thus the variation of the field over the ADL thickness is negligible. We focus on the eigenvalue with the largest real part corresponding to the mode with the largest partial inductance and, thus, lowest resonance frequency. This we call the first mode or the dominant mode designated by the subscript 1, from which we extract the equivalent inductance and quality factor of the lowest resonance mode of the ADL resonator. Fig. 5.4 and Fig. 5.5 show the extracted inductance (real part) and quality factor of the dominant resonance mode of the ADL resonator as a function of frequency on high resistivity silicon (HRS) substrates. There several remarks to be made:

The disk diameter should be limited to few millimeters at most for on-chip applications. Especially for small disks, λ_1' and, thus, the (real) inductance L_1' only slightly changes at frequencies below 50 GHz (the range of interest in this work). Disks of larger dimensions show a drop in L_1' at higher frequencies. The imaginary component λ_1'', by contrast, increases rapidly with frequency in all cases, leading to a

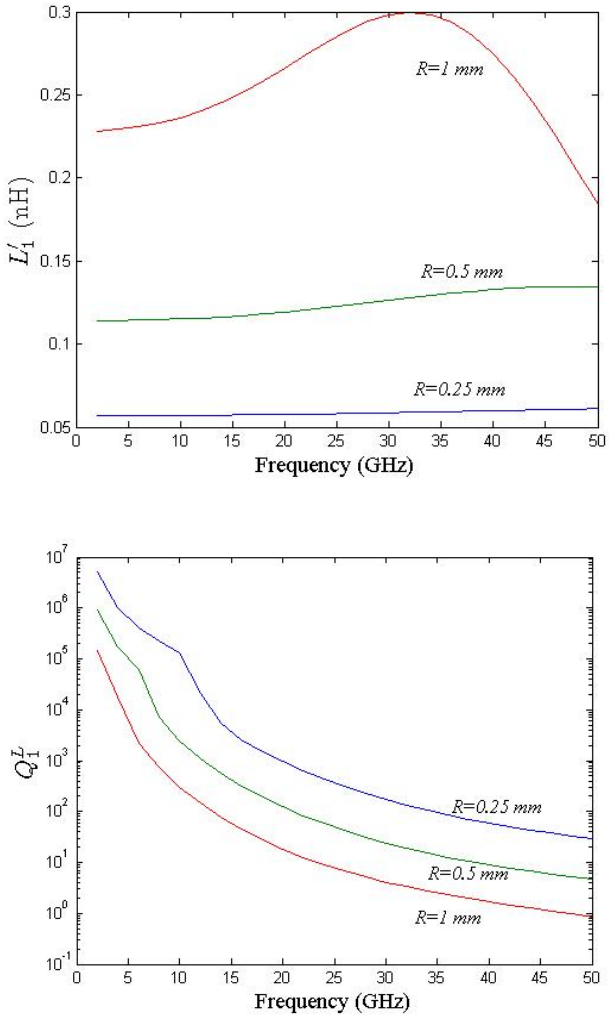

Figure 5.4: Equivalent inductance (left) and quality factor (right) of the lowest mode of the ADL disk resonator as a function of frequency for different values of the radius (*R*). Simulations were carried out assuming a high-resistivity silicon substrate ($\varepsilon_s = 12$) with a thickness of 0.5 mm. No ground plane was assumed.

sharp drop in the inductive quality factor $Q_1^L = \lambda_1' / \lambda_1''$.

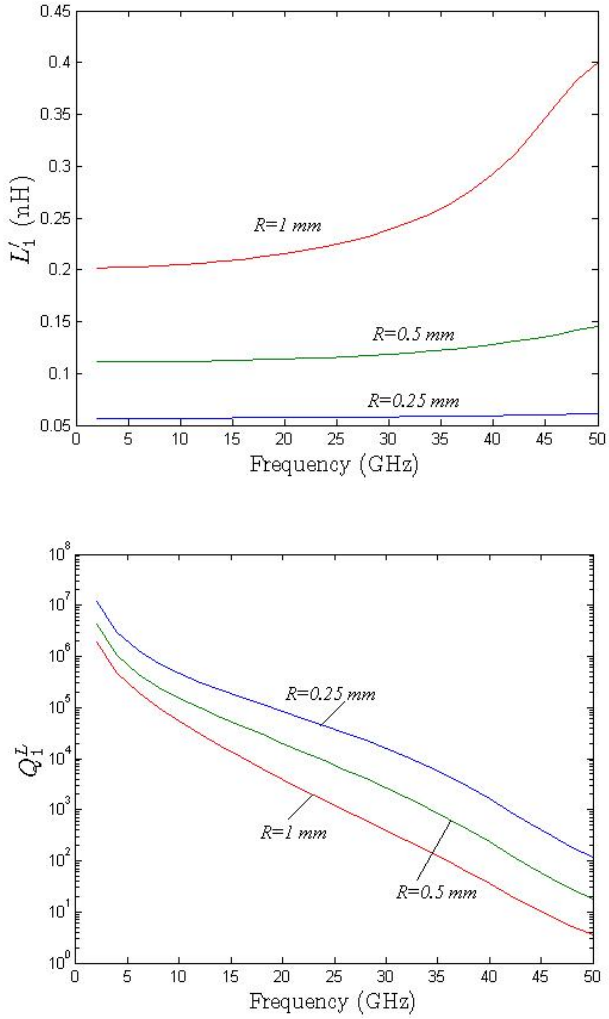

Figure 5.5: Equivalent inductance (left) and quality factor (right) of the lowest mode of the ADL disk resonator as a function of frequency for different values of the radius (R). Simulations were carried out assuming a grounded high-resistivity silicon substrate with a thickness of 0.5mm. The thickness of the ADL disk was 1 μm.

The imaginary part λ_1'' is related to the losses caused by radiation into free space, leakage of microwave power into the surface-wave modes of the substrate, and the

polarization loss inside the substrate. The last factor is found to be negligible on insulating substrates with a small loss tangent (<10^{-2}). By far the most important loss contribution, however, comes from the surface wave effects. The ADL resonance is caused by the formation of TE standing waves inside the disk. Such modes naturally couple to the TE modes of the underlying substrate. If the substrate is not grounded, the cutoff frequency of the lowest TE mode is just zero, and TE waves can freely propagate on the substrate at any frequency, carrying away the energy stored inside the resonator. By contrast, if a ground plane is inserted underneath, a finite cutoff results (>100 GHz in 0.5mm-thick silicon) below which no propagation takes place. By comparison of Fig. 5.4 and Fig. 5.5, it is clear that grounding the substrate yields a major increase in the inductive quality factor Q_1^L. It also decreases L_1' due to the image currents in the conductive ground plane. But this effect is not remarkable when the disk radius is less than the substrate thickness.

If the substrate is not insulating, i.e. it has a finite resistivity, the inductive quality factor can be severely limited. Fig. 5.6 shows the inductive quality factor of an ADL resonator on silicon substrate as a function of frequency with different resistivity. In this case the major loss contribution comes from the generation of eddy currents, and their ohmic dissipation inside the substrate. For disk resonators built on silicon with a radius less than 1 mm, this effect becomes observable when the substrate resistivity becomes less than 100 Ωcm. The interesting point, however, is that even on low resistivity silicon substrates (10 Ωcm) Q_1^L values above 50 can be achieved if the frequency is not too high. Given the difficulty of the realization of conventional lumped elements with quality factors exceeding even 20 on a low-resistivity wafer, this result is particularly promising.

We next consider the resonance frequency $f_1 = \omega_1 / 2\pi$ of the first mode as function of the ADL (in-plane) dielectric constant for different values of the disk radius (as shown in Fig. 5.7). As expected, f_1 increases with increasing ε'. With 1μm-thick ADL films, resonance frequencies below 50 GHz can be obtained by using a $\varepsilon_{||}'$ above a few thousand. Comparison of Fig. 5.5 and Fig. 5.6 shows that the inductive quality factors above 1000 can be easily achieved by choosing the right disk dimension. In practice, this means that the overall quality factor of the resonator is mainly limited by the dielectric and magnetic losses of the ADL material which should be evaluated from its tangent loss and complex susceptibility.

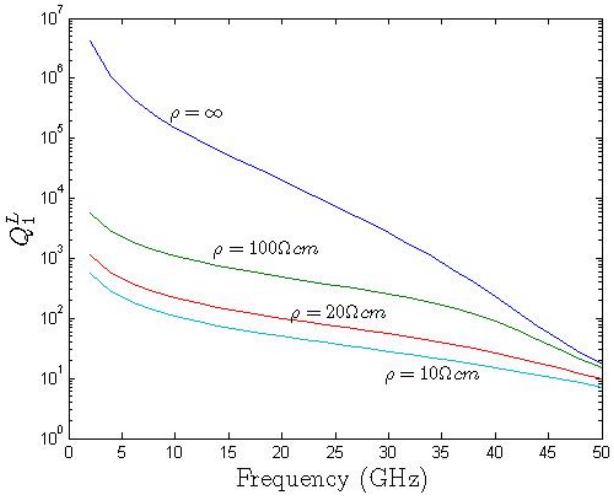

Figure 5.6: Inductive quality factor of the first mode of an ADL disk (radius 0.5 mm, thickness 1μm) on a silicon substrate (0.5 mm-thick, with a ground plane) as function of frequency for different vaues of substrate resistivity ρ.

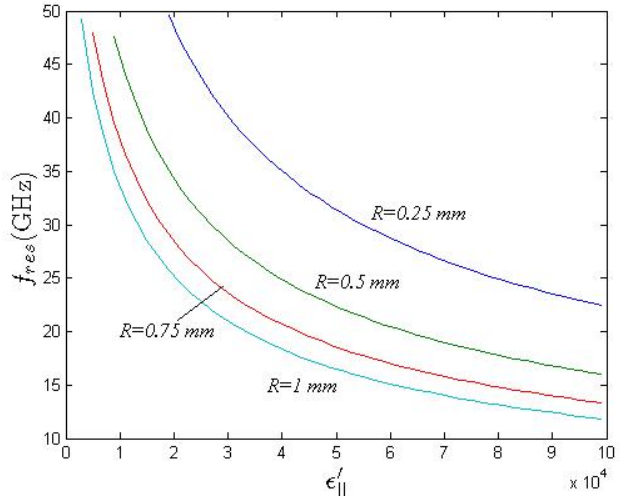

Figure 5.7: Resonance frequency of the first mode of the ADL disk as function of the in-plane dielectric constant $\varepsilon'_{||}$ for different disk radii. A grounded high-resistivity silicon substrate with a thickness of 0.5mm was assumed. The ADL thickness was 1 μm.

5.2.4 Effects of electric and magnetic polarization loss of ADL

The electric polarization loss of the ADL can be estimated using a 3D lumped-element equivalent circuit consisting of capacitors *C* and series resistors *R*, as described in section 4.3.1 and section 4.4.3. The series resistance describes the ohmic loss arising inside the metallic patterns as (RF) current travels along the patterns and the capacitances coupling them. The effective in-plane dielectric constant of the ADL is given by

$$\varepsilon'_{\parallel} = \frac{(N-1)C}{t} = \frac{(N-1)\varepsilon'_d A}{t_d[Nt_M + (N-1)t_d]}, \tag{5.56}$$

where *N* is the total number of metal layers and *t* is the overall ADL thickness, ε'_d and t_d denote the dielectric constant and thickness of the isolating layers, *A* is the overlap area between metallic patterns, and t_M is the thickness of the metallic layers. In the above equation we have used $C = \varepsilon'_d A / t_d$. If the number of layers is large, one finds

$$\varepsilon'_{\parallel} \approx \frac{\varepsilon'_d A}{t_d(t_M + t_d)}. \tag{5.57}$$

The loss tangent of the ADL is given by

$$\tan\delta = \tan\delta_d + \tan\delta_M, \tag{5.58}$$

where $\tan\delta_d$ is the loss tangent of the isolating dielectric layers and

$$\tan\delta_M = \omega RC \tag{5.59}$$

is the loss brought about by the pattern resistance. Since

$$R = \frac{\eta}{\sigma_M t_M}, \tag{5.60}$$

with η a geometrical factor and σ_M the metal conductivity, one has from Eqs. (5.56-59):

$$\tan\delta_M = \eta(1 + t_d / t_M)\frac{\omega\varepsilon'_{\parallel}}{\sigma_M}. \tag{5.61}$$

Now consider the magnetic losses. Under influence of a magnetic field perpendicular to the patterns, planar eddy currents start to flow in the plane of the

patterns. Such currents, in turn, generate a dipolar magnetic field which opposes the original field. This effect can be represented by an effective susceptibility $\chi_\perp$, i.e. the ratio between the volume average of the induced magnetic dipoles and the original field. For patterns with a thickness far below the skin depth inside the metal, an approximation assuming a constant magnetic field yields (see Appendix C for a detail derivation)

$$\gamma = \frac{\chi_\perp}{1+\chi_\perp} = -j\eta_M f \omega\mu_0\sigma_M D^2 , \tag{5.62}$$

where D is the diameter of the patterns, f is their volume filling factor, and η_M is a dimensionless, geometry-dependent factor. Fig. 5.8 shows some pattern geometries and their associated geometrical factors η_M. The quantity η_M can be significantly reduced by micro-patterning the individual metallic squares. Note, however, that while η_M decrease, the pattern series resistance and, thus, η increases. Careful calculations are required to optimize the pattern shape.

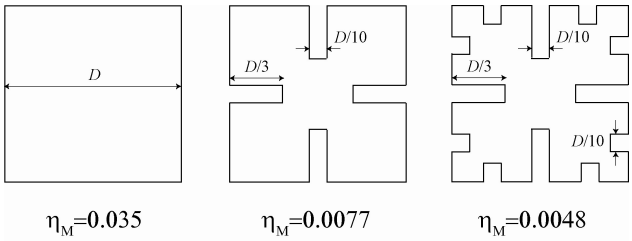

Figure 5.8: Some patterns and their associated susceptibility coefficients.

From Eq. (5.45),

$$Y_k = -\frac{\gamma Q_{kk} t}{j\omega\mu_0} = \left(\eta_M f\right)\sigma_M D^2 Q_{kk} t . \tag{5.63}$$

The magnetic quality factor becomes

$$Q_k^M = \frac{\omega C'}{Y_k'} = \frac{\omega(\varepsilon_\parallel' - \varepsilon_0)}{\eta_M f D^2 \,\mathrm{Re}\left[Q_{kk}\right]\sigma_M} \approx \frac{1}{\eta_M f D^2 \,\mathrm{Re}\left[Q_{kk}\right]}\left(\frac{\omega\varepsilon_\parallel'}{\sigma_M}\right), \tag{5.64}$$

where Eq. (5.47) has been used plus the fact that $\varepsilon_\parallel' \gg \varepsilon_0$. Note that the capacitive

quality factor is proportional to $\sigma_M / \omega\varepsilon'$, while the magnetic quality factor is inversely proportional to this quantity. Thus (if the frequency dependence of $\mathrm{Re}\,Q_{kk}$ can be neglected, as was the case in our numerical experiments), Q^C decreases with frequency, whereas Q_k^M increases with frequency. The combined quality factor Q^{CM} is found from

$$\frac{1}{Q^{CM}} = \tan\delta_d + \frac{1}{Q^C} + \frac{1}{Q_k^M}, \tag{5.65}$$

and has a maximum value given by

$$Q_{\max}^{CM} = \left(\tan\delta_d + 2\sqrt{\eta_M \eta f (1 + t_d / t_M) D^2 \,\mathrm{Re}\left[Q_{kk}\right]}\right)^{-1}, \tag{5.66}$$

which is reached when

$$\frac{\omega\varepsilon'_{\|}}{\sigma_M} = \sqrt{\frac{\eta_M f D^2 \,\mathrm{Re}\left[Q_{kk}\right]}{\eta(1 + t_d / t_M)}}. \tag{5.67}$$

Note that the volume filling factor of the metallic patterns (*f*) can be written as

$$f = f_a \frac{t_M}{t_M + t_d}, \tag{5.68}$$

where f_a is the surface filling factor of those patterns. Therefore, Eq. (5.66) can be written as

$$Q_{\max}^{CM} = \left(\tan\delta_d + 2\sqrt{\eta_M \eta f_a D^2 \,\mathrm{Re}\left[Q_{kk}\right]}\right)^{-1}. \tag{5.69}$$

Numerical experiments show that, for the lowest mode of the resonator, if the frequency is not too high, $\mathrm{Re}[Q_{11}] \sim \nu_1 / R^2$ where ν_1 is almost a constant (~6). This yields

$$Q_{\max}^{CM} = \left[\tan\delta_d + 2(D/R)\sqrt{\eta_M \eta f_a \nu_1}\right]^{-1}. \tag{5.70}$$

It shows that the highest attainable quality factor is only determined by the geometrical

factors and not the material constants. Note, however, that this conclusion is only valid within the perturbative description of the magnetic losses and the approximate result Eq. (5.62).

5.2.5 Restrictions of the model

Since it assumes an impressed current source, the model presented above does not account for ohmic loss in the current-carrying ring. This can be accounted for by adding a resistance R_p in series with the primary winding of the transformer in the equivalent circuit model of Fig. 5.3. R_p can be approximately calculated by considering the flow of the electric current inside an isolated ring, since we neglect the effect of the environment on the ring current distribution anyway. This resistance includes the effect of the non-uniform distribution of current at high frequencies (skin effect) and is frequency-dependent.

A more serious shortcoming of the model used, however, is the assumption of a constant current along the metallic ring. In reality, the excitation current does not remain constant and charges accumulate along the ring. This does not affect the intrinsic behavior of the eigenmodes of the ADL disk discussed above. But a current varying along the ring breaks the rotational symmetry of the system. Thus, additional modes with an electric field varying in the azimuthal direction may also be excited. These modes (similar to whispering gallery mode or WGM of cylindrical dielectric rods [9]) have a very high resonance frequency compared to the low-lying rotationally symmetric modes considered in the previous section. Nevertheless, their resonance tails may still affect the resonator at low frequencies.

Although the model presented in the previous sections can be generalized to include the WGMs, this will significantly complicate the calculation. Instead, to account for the role of charge accumulation, we employ a perturbative approach. Consider the situation with a constant current flowing through the ring as the zero'th order (unperturbed) solution of the problem. Due to the symmetry of the system, this current brings about an electric potential along the ring which linearly varies with distance. From this potential distribution, we can calculate the accumulated charge on the ring and, subsequently, its effect on the impedance. Yet, even this calculation is not straightforward at high frequencies: charges on the ring will induce polarization charges on the ADL disk which, at high frequencies, generate polarization currents. A full description of the latter again needs the inclusion of rotationally non-symmetric eigenmodes. Therefore, to simplify the

calculation, we adopt an electrostatic approach and include the effect of the charges by adding a shunt capacitance at the input of the resonator. Strictly speaking, this approach is valid at low frequencies only, but we will later justify its use by comparison with full wave simulations performed using commercial software. But before performing this calculation, let us see what the consequences will be for the behavior of the resonator.

Consider the ADL resonator close to its first resonance. A shunt capacitance C_p has now been added to its input to account for the charging effects. A series resistance R_p accounts for conductor loss in the ring. For simplicity, we neglect the effect of the higher modes. The resulting equivalent circuit is now given by Fig. 5.9 (the subscript 1, denoting the lowest mode, has been dropped). It consists of two *LC* resonators coupled by a mutual inductance.

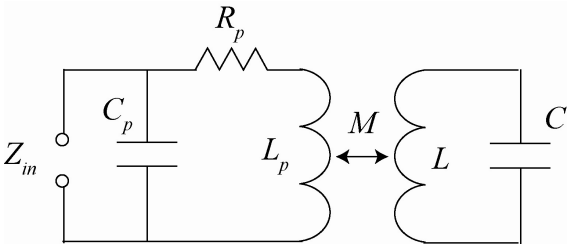

Figure 5.9**:** Equivalent circuit of the ADL resonator including a shunt capacitance C_p.

If the imaginary parts of L,C,L_p,C_p,M as well as the resistance R_p are small, the resonance frequencies of this circuit follow from the solution of the simple algebraic equation:

$$\left(1-\frac{\omega_D^2\omega_p^2}{\omega_M^4}\right)\omega^4-\left(\omega_D^2+\omega_p^2\right)\omega^2+\omega_D^2\omega_p^2=0\,, \tag{5.71}$$

where $\omega_D{}^2=\omega_1{}^2=1/L'C'$ is the intrinsic frequency of the resonance of the lowest mode of the ADL disk,

$$\omega_p^2=1/L_p'C_p' \tag{5.72}$$

is the resonance frequency of the primary inductor in parallel with the shunt capacitance, and

$$\omega_M^2=1/\left(M'\sqrt{C_p'C'}\right). \tag{5.73}$$

Eq. (5.71) has two solutions corresponding to the two coupled resonators. They are given by

$$\omega_{\pm}^2 = \frac{\omega_D^2 + \omega_p^2 \pm \sqrt{(\omega_D^2 - \omega_p^2)^2 + 4\omega_D^2\omega_p^2\kappa^2}}{2(1-\kappa^2)}, \tag{5.74}$$

where

$$\kappa = \frac{\omega_D\omega_p}{\omega_M^2} = \frac{M'}{\sqrt{L_p'L'}} \tag{5.75}$$

is the magnetic coupling factor of the transformer. It is instructive to introduce the coupling factor k between the two resonator, i.e.,

$$k = \frac{2\omega_D\omega_p\kappa}{\omega_D^2 - \omega_p^2}, \tag{5.76}$$

which depends not only on the magnetic coupling factor κ, but also on the differences between the resonance frequencies of the two resonators, and consider the cases of weak coupling (k^2<<1) and strong coupling (k^2>>1).

Weak coupling (k2<<1)

Expansion of the solution (5.74) then shows that the resonances of the ADL disk and the primary ring are shifted to

$$\begin{aligned} \omega_D^2 &\approx \frac{\omega_D^2}{1-\kappa^2} + \frac{k^2(\omega_D^2 - \omega_p^2)}{4(1-\kappa^2)} \\ \omega_p^2 &\approx \frac{\omega_p^2}{1-\kappa^2} - \frac{k^2(\omega_D^2 - \omega_p^2)}{4(1-\kappa^2)} \end{aligned}. \tag{5.77}$$

Thus, if $\omega_p > \omega_D$ ($\omega_p < \omega_D$), the disk resonance frequency will be shifted to lower (higher) values. This shift is reduced if the magnetic coupling becomes smaller, or if the difference between the resonance frequencies of the two LC resonators becomes large.

Strong coupling (k2>>1)

In this limit, the magnetic coupling is high and/or the resonance frequencies of the two resonators are very close to each other. Solving Eq. (5.74) in this circumstance yields

$$\omega_{\pm}^2 \approx \frac{\omega_D^2 + \omega_p^2 \pm 2\omega_D\omega_p\kappa}{2(1-\kappa^2)}. \qquad (5.78)$$

When κ is close to one, the two resonance frequencies are highly separated and could be far different than the original ones.

5.3 Full wave simulations of ADL resonators

To verify the validity of the theoretical model developed in previous section, full wave simulation was carried out using commercially available simulation software, HFSS, which employs the finite element method. The ADL disk is modeled as an anisotropic effective material, with the in-plane dielectric constant $\varepsilon_{\parallel}$ and the out-of-the-plane dielectric constant $\varepsilon_{\perp}$ which we calculated in section 4.3.1. The magnetic properties of the ADL can be derived as follows. Because the thickness of the metallic layer is much smaller than its lateral dimensions and the magnetic field is mainly perpendicular to the ADL disk, the eddy current loss due to horizontal magnetic field is negligible for the dominant resonance mode, which implies that the relative permeability and magnetic loss tangent parallel to ADL disk are 1 and 0 respectively. It can be shown that the magnetic loss tangent perpendicular to ADL disk is given by the negative imaginary part of Eq. (5.62). And therefore, the real part of perpendicular permeability is given by $\mu_{\perp}' = 1/(1+\tan^2\delta_{\text{Mag}})$, where $\tan\delta_{\text{Mag}}$ is the magnetic loss tangent of ADL. In the HFSS simulation, we first assume a magnetic loss tangent value of 1. The choice of this value is based on Eq. (5.62) which is repeated here for convenience.

$$\gamma = \frac{\chi_{\perp}}{1+\chi_{\perp}} = -j\eta_M f\omega\mu_0\sigma_M D^2 = -j\tan\delta_{\text{Mag}}$$

Here a micro-patterned ADL structure is assumed to minimize the magnetic loss, i.e. η_M taking the value of 0.0077 (Fig.5.8). The volume filling factor *f* is calculated based on ADL structure described in chapter 4 with ADL metallic pattern size of 5x5 μm^2, and the same pattern size is assigned to *D*. The frequency is fixed at 30 GHz and the conductivity of Al film is assumed to be $3x10^7$ S/m. This yields a value of the magnetic loss tangent to be 0.73. Therefore, the choice of 1 for magnetic loss tangent is justified in this case. However, for larger pattern size and/or ADL without micro-patterning, the magnetic loss

will be higher than this value. For example, for ADL pattern of 11x11 μm^2, without micro-patterning, the magnetic loss tangent could be as high as 19. (We will come back to this point later, but the simulation presented here will suffice to study the performance of ADL resonator in a more or less optimized scenario.) The magnetic properties of the ADL disk can thus be expressed by the permeability tensor:

$$\mu = \mu_0 \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0.5(1-j) \end{bmatrix}. \tag{5.79}$$

To characterize the ADL resonator from simulations, we first transform the resulting *S*-parameters into *Z*-parameters and then calculate $Z_s = Z_{11} + Z_{22} - Z_{12} - Z_{21}$, which is the input impedance seen with the resonator excited differentially. This is to eliminate the un-wanted impedance through the substrate and can be understood by considering the T-network representation of the resonator [10]. The *Q*-factor is calculated using Eq. (5.2), while the resonance frequency f_0 is determined by the frequency at which the real part of input impedance Z_s reaches its maximum value, f_1 and f_2 are frequencies where Re(Z_s) has half of the peak value. This is justified by considering the input impedance for a parallel *RLC* resonator (our ADL resonator can be modeled as a parallel *RLC* resonator as shown in the previous section). Near the resonance, the input impedance can be approximated by the following expression [1]:

$$Z_{\text{in}} \simeq \frac{R}{1 + 2jQ\Delta f / f_0}, \tag{5.80}$$

where Δf is the frequency deviation from the resonance and f_0 is the resonance frequency. The real part of Z_{in} is

$$\text{Re}(Z_{\text{in}}) = \frac{R}{1 + 4Q^2(\Delta f / f_0)^2}. \tag{5.81}$$

At resonance, the input impedance is just *R*. By setting the Re(Z_{in}) to *R*/2, and solving Eq. (5.81), one finds two Δf values which correspond to two frequency values of f_1 and f_2 respectively. The quality factor Q is therefore expressed as in Eq. (5.2).

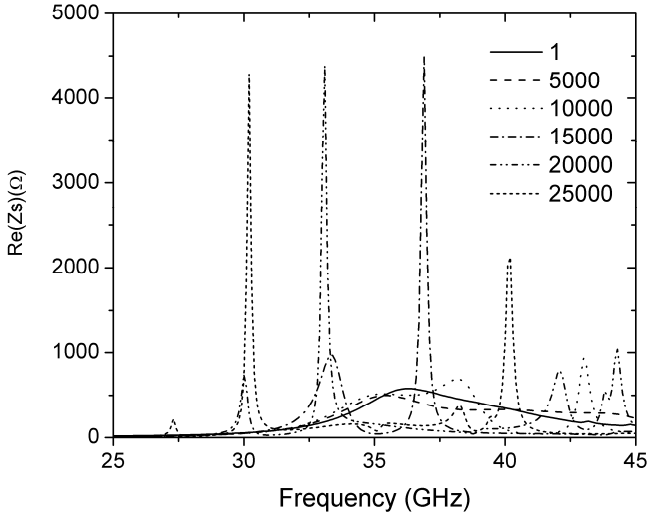

Figure 5.10: HFSS simulation results for ADL disk resonators (R=0.75 mm) with different values of in-plane effective dielectric constants, coupled with ring inductor.

Fig. 5.10 shows the simulated real parts of Z_s (=Z_{11}+Z_{22}-Z_{12}-Z_{21}) as a function of frequency for different in-plane dielectric constants $\varepsilon_{||}$ of the ADL for disk resonators with R=0.75mm coupled with a ring inductor (Fig. 5.1). Clear resonances can be identified in the simulation frequency range for $\varepsilon_{||}$ higher than 10000. The trend of lower resonance frequency for higher $\varepsilon_{||}$ is observed as expected. The Q-factor of 140 is achieved for $\varepsilon_{||}$ equals to 20000 with magnetic loss tangent $\tan\delta_{\text{Mag}} = 1$, and dielectric loss tangent $\tan\delta = 0.002$ for ADL material. To verify our theoretical models developed in the previous section, we compare the resonance frequencies obtained from the HFSS simulations and those from calculation based on the physical model. To that end, we re-calculate the resonance frequencies for different ADL disk geometries on AF45 glass substrate, which is shown in Fig. 5.11. By a comparison between Fig. 5.10 and Fig. 5.11, it is observed that the first resonance frequencies of ADL resonator with different in-plane dielectric values are all shifted to higher end. Taking the case of $\varepsilon'_{||} = 20000$ as an example, the first resonance frequency of ADL disk resonator with

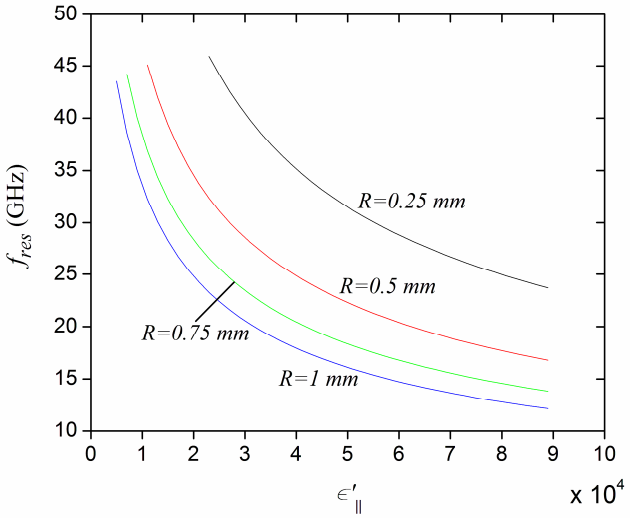

Figure 5.11: Resonance frequency of the first mode of the ADL disk as function of the in-plane dielectric constant for different disk radii. A grounded AF45 glass substrate with a thickness of 0.7 mm was assumed. The ADL thickness was 1 μm.

R=0.75 mm is around 28.3 GHz, while in Fig. 5.10 it is found to be 33.1 GHz from the HFSS simulation result, more than 15% differences. This discrepancy is related to the shift in resonance frequency caused by the magnetic coupling between the current-carrying ring and the ADL disk as discussed in 5.2.5. Notice that the geometric configurations of ADL disk coupled with the ring inductor intrinsically implies a not weak magnetic coupling. To illustrate the influence of magnetic coupling factor on the two resonance frequencies, calculation of the resonance frequency shifts by solving Eq. (5.74) is carried out. In this calculation, we assume the ADL disk and the ring inductor have their first resonance frequencies at 30 GHz and 12 GHz respectively and sweep the magnetic coupling factor. Result is shown in Fig. 5.12. It is inferred from the figure that the ADL disk (ring inductor) resonance frequency shifts to higher (lower) end as the magnetic coupling factor increases. When the magnetic coupling factor is 0.5, the shift of ADL disk resonance frequency could be as high as ~20%, while the ring inductor has a shift of only ~2%. The small shift of the resonance frequency of the ring inductor is also observed (not shown here) in the HFSS simulation.

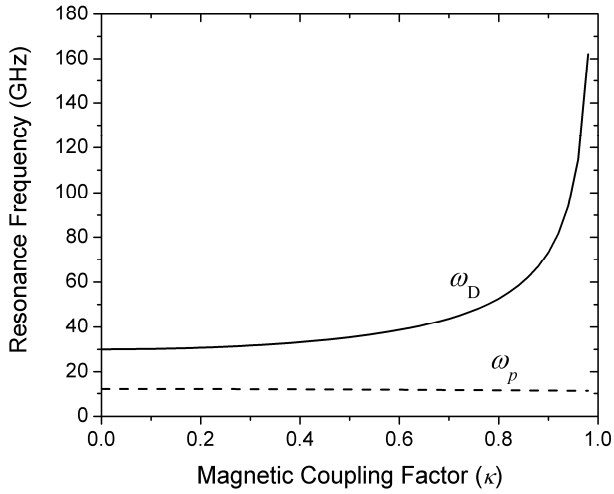

Figure 5.12: Calculated resonance frequency shifts as a function of magnetic coupling factor. Assume the ADL disk and the ring inductor have a first resonance frequency of 30 GHz and 12 GHz respectively.

To demonstrate the 'real' resonance frequency of the ADL disk, we look into a weak magnetic coupling structure. This could be implemented by a dipole, a microstrip transmission line or putting the ring outside the ADL disk. Here for simplicity, we choose to couple the ADL disk with a dipole as schematically shown in Fig. 5.13. A full wave HFSS simulation is carried out for ADL disks of R=0.5 mm and R=0.75 mm with the same ADL material parameters and results are shown in Fig. 5.14. In both cases, clear resonances are observed. Notice that the peak impedances at resonance frequencies are much lower than the ring coupled ones due to the very weak coupling as expected. Besides the first resonance mode, higher modes corresponding to the WHG modes are also clearly visible. By a comparison with Fig. 5.11, it is found that the first resonance frequencies of ADL disks with the two different radii well match the results obtained from the theoretical model. Taking two cases for illustration, the first resonance mode of ADL disk with R=0.5 and an in-plane dielectric constant of 25000 is found to be 31.1 GHz, while it is exactly 31.1 GHz from the calculation (Fig. 5.11). For R=0.75 mm with in-plane dielectric constant of 20000, the simulation and calculation results for the first resonance frequencies are both around 28.3 GHz. Therefore, the theoretical model fits

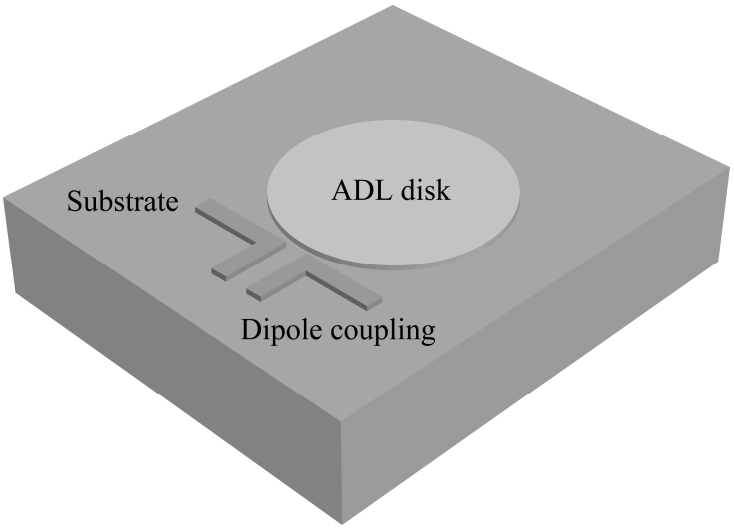

Figure 5.13: Schematic view of a weakly coupled ADL disk resonator, i.e., coupled with a dipole structure.

very well with the HFSS simulation results, which indicates the validity of the physical model presented in the previous section and can be used as a guideline for ADL disk resonator design.

Besides the major resonances, we also notice that minor resonance peaks are also present in Fig. 5.10 for the ring coupled ADL resonator. By comparison Fig. 5.10 with Fig. 5.14, some of the minor peaks at higher frequency end can be explained as the higher resonance modes of the disk resonator. However, the resonance lower than the first disk resonance frequency can not be explained this way. Taking the case of $\varepsilon_{\parallel}$=20000 as an example, the major resonance which corresponds to the first resonance mode of the ADL disk occurs at ~33.1 GHz, while a weak resonance peak at ~30 GHz also be observed. Since the ring itself has its second resonance at around 37 GHz (as indicated by the curve with in-plane dielectric constant of the ADL to be one), this minor peak might be related to the coupling between ADL resonator and this higher mode of the ring. To verify this hypothesis, a HFSS simulation is performed by modifying the ring geometry which has lower second self-resonance frequency. The result (not shown here) shows that this modification has little influence on the ADL disk resonance, but shifts the minor peak to its lower end. Therefore, the hypothesis mentioned above is justified.

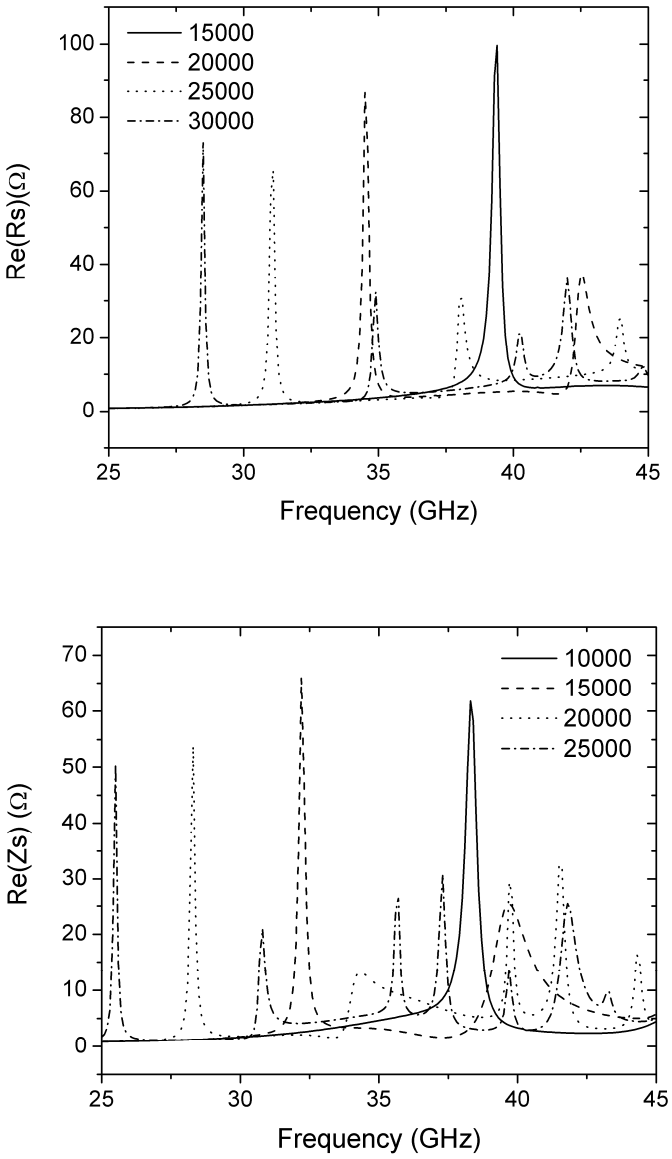

Figure 5.14: HFSS simulation results for ADL resonators of R=0.5 mm (top) and R=0.75 mm (bottom) with different values of in-plane effective dielectric constants, coupled with a dipole structure.

5.4 Experimental results and discussions

Preliminary experiments were carried out to demonstrate the possibility of realizing high-Q ADL resonators. ADL resonators were built on a 500 μm glass substrate (AF 45) to minimize the substrate loss in the first place. The fabrication process is quite similar to the multi-layer ADL shields which were described in section 4.4.3. Here we have 8 Al layers (100 nm for each layer) isolated by 7 PVD sputtered Aluminum oxide films (30nm for each layer). This gives an ADL material of ~1 μm in thickness. The sizes of metallic squares were chosen to be 3x3, 5x5, 7x7, 9x9 and 11x11 μm^2 to achieve different values of effective in-plane dielectric constant of the ADL material. Using Eq. (5.56), these pattern sizes yield effective in-plane dielectric constant values of approximately 2300, 9300, 20000, 37000 and 58000 respectively. Based on our numerical experiments, ADL disks with radii of 0.25, 0.5 and 0.75 mm were fabricated. After the formation of ADL disks, a 1 μm silicon oxide layer was deposited to form an etching stop layer. Finally an Al layer of 3 μm thick was sputtered and patterned to form the conducting ring shown in Fig. 5.1 which can excite resonance of the ADL resonator. To suppress the undesired surface-wave mode in the substrate, 1.4 μm Al is applied on the backside of the glass wafer which will be grounded during the measurement. For comparison, micro-patterning ADL was also fabricated on the same wafer.

Two port S-parameter measurements were performed on a HP8510 vector network analyzer. To eliminate the influence of the measurement pads, open and short structures were fabricated on the same wafer and de-embedded. The extraction of the resonance frequency and quality factor is quite similar as that of HFSS simulation and will not be repeated here.

Fig. 5.15 shows the measured Re (Z_s) as a function of frequency for selected different ADL patterns. The dominant resonance mode of ADL resonator with larger ADL metallic pattern size is clearly observed. The resonance frequencies of the ADL resonators with and without micro-patterning with the same metallic pattern sizes are close to each other, which implies that the effective in-plane dielectric constants are more or less the same. However, the quality factor, as computed for the pattern size of 9x9 μm^2, is estimated to be 25, which is in sharp contrast with the results shown in the HFSS simulations of Fig 5.10. This could be resulted from an under-estimation of the magnetic and/or dielectric loss of the ADL material. As mentioned in the previous section, the magnetic loss tangent for large ADL pattern without mciro-patterning could be as high as 19. A HFSS

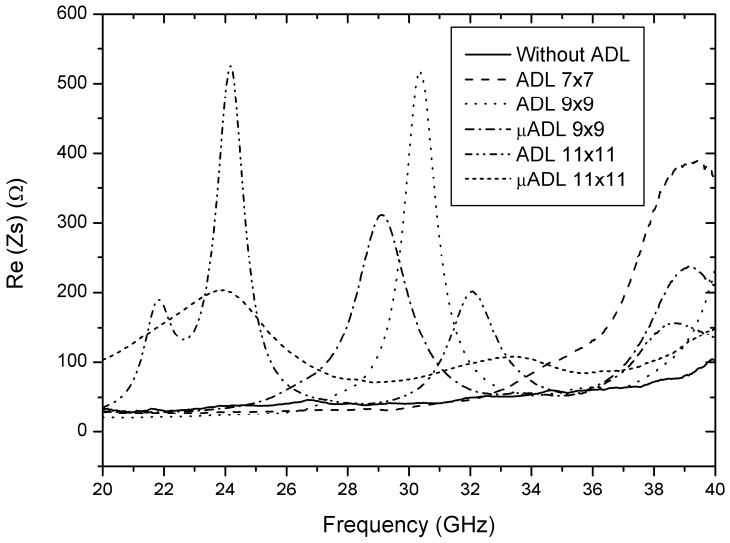

Figure 5.15: Measurement results for ADL resonators (R=0.75 mm) with different ADL patterns.

simulation shows that, with magnetic loss tangent $\tan\delta_{\text{Mag}} = 15$ while the dielectric loss tangent is the same ($\tan\delta = 0.002$) as calculated in Fig. 5.10, the Q-factor of ADL disk (R=0.75 mm, $\varepsilon_{\parallel}' = 20000$) is as low as ~25. On the other hand, with ADL dielectric loss tangent $\tan\delta = 0.02$, while keeping the magnetic loss tangent the same ($\tan\delta_{\text{Mag}} = 1$) as calculated in Fig. 5.10, the Q-factor is around 30, which is also comparable with our experimental result. However, note also that micro-patterning the ADL elements does not yield a higher Q-factor as expected (it even lowers the Q-factor!). This implies that the eddy-current loss is not a dominant factors in the devices investigated. The low Q-factor observed should then be mainly due to dielectric loss which comprises the dielectric loss of the insulating dielectric (RF sputtered aluminum oxide in our case) and the pattern resistance [see Eq. (5.58)]. The higher than expected effective dielectric loss of the ADL may be related to a number of factors as argued below.

Normally, aluminum oxide has a very low tangent loss at microwave frequencies (~0.0002 or lower for alumina substrate [11]). However, the aluminum oxide in our experiment is prepared by reactive RF sputtering of Al target with O_2 plasma, which has poor step coverage especially near the edges of the metallic ADL patterns. This results in very thin Al oxide film near these edges which can introduce electron tunneling effects between two Al layers. This effect plus the fact that the film is extremely thin (30nm) (there is little data in literature on the microwave loss tangent of Al oxide thin film) may lead to an increase of tangent loss of the film. A separate measurement of the loss tangent of the aluminum oxide film will be helpful to identify this issue.

The tangent loss induced by the pattern resistance is given by Eq. (5.59). ADS simulations give a pattern resistance of ~1 Ω assuming 9x9 μm^2 patterns and an Al conductivity of 3.3×10^7 S/m (which is the conductivity of bulk sputtered Al in our sputtering system) This yields a loss tangent of 0.009 at 30 GHz. However, a close look at the SEM images of the cross section of the ADL resonator (Fig. 5.16), shows local narrowing effect of the metallic layer caused by the crystallization and grain growth during the film deposition. This effect can lead to significant decrease of local conductivity of Al and increase of the pattern resistance R. Therefore, the loss tangent $\tan\delta_M$ due to pattern resistance will be higher than 0.009, The above arguments are further justified by the fact that with micro-patterning, the quality factor becomes even less. This can be qualitatively explained by considering the pattern resistance R when cutting slots in the square patterns. Since R is also proportional to a geometric factor η as shown in Eq. (5.60), the micro-patterning in ADL manifests itself by increasing R due to local narrowing near the center of the metallic pattern, as can be seen from Fig. 5.8. Therefore, a higher tangent loss due to metallic pattern resistance can be expected for micro-patterned ADL resonator, which overwhelms the eddy current loss reduction when compared with an un-patterned ADL resonator.

To overcome this problem and achieve higher quality factor, one obvious solution is to increase the conductivity of the metal layer by using copper for example. Another way is to make the metallic layer thicker. The geometry of the metallic pattern in ADL can also be further optimized, however a tradeoff between a lower geometric factor η for pattern resistance R and a sufficient suppression of eddy current loss has to be made. It is also suggested to use dielectric material which has higher dielectric constant (such as TiO_2 or ferroelectric materials) as the isolating material in ADL structure, substituting the

Al oxide film. One obvious benefit by using such material is that the film thickness can be a few times higher than the Al oxide case, to obtain the same in-plane dielectric constant of ADL. This will eliminate the possibility of local electron tunneling as mentioned before. On the other hand, the metallic pattern size can also be decreased which leads to less pattern resistance as well as less eddy current loss.

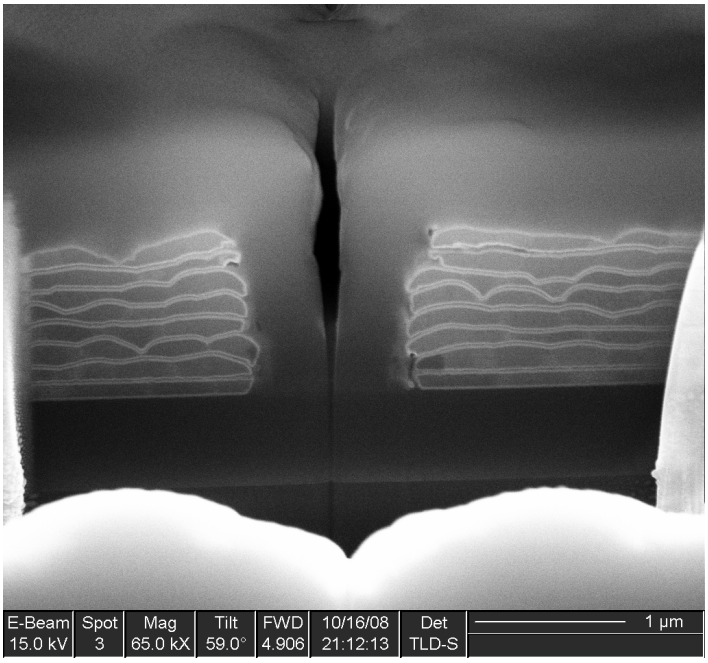

Figure 5.16: SEM image of cross section of ADL resonator. Eight layers of the metallic patterns in ADL are resolved. The local narrowing of the metallic layer is also shown.

5.5 Conclusions

In this chapter, a novel type of on-chip microwave resonator was proposed based on a thin disk of artificial dielectric material, which can potentially achieve very high quality factor. Based on an effective material description of ADL, we developed a theoretical model to analyze the resonance modes of the disk resonator. The dielectric loss (due to the insulating dielectric inside the ADL as well as the resistance of the ADL metallic patterns) and the magnetic loss (caused by the eddy currents inside the patterns) were taken into account in the model. Numerical simulations show that very high quality factor

can be realized on semi-insulating substrates. This prediction was further verified by full wave simulations carried out by in commercially available software HFSS. Results show quality factors exceeding 100. However, although the resonance behavior of the ADL disk was also seen in the experiments carried out, a much lower quality factor was observed. We attribute this degradation to the higher than expected resistance of the individual metallic patterns of the ADL.

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Chapter 6

Conclusions and Recommendations

6.1 Conclusions

The applications of ferroelectric materials and artificial dielectric materials in monolithic microwave integrated circuit (MMIC) have been proposed and investigated. For ferroelectric materials, both material development and device optimization have been addressed. It is for the first time, to the best of our knowledge, that a special kind of artificial dielectric material is designed and implemented in MMIC. Applications of this artificial dielectric in MMIC are proposed and realized experimentally.

In the following, the main results of this work are summarized. Recommendations to future work will be proposed as well.

- It was shown that crack free and smooth surface barium strontium titanate (BST) thin film have been successfully prepared by chemical solution deposition (CSD)

method on platinum coated silicon substrates. Based on the impedance measurement of parallel plate tunable capacitor with Al/BST/Pt configuration, asymmetric characteristics of both capacitance and loss with respect to the bias voltage applied between the Pt and Al electrodes is observed and is found to be attributed to the formation of an ohmic contact and a Schottky barrier at the Al/BST and Pt/BST interfaces, respectively. (*chapter 2*)

- It was proposed to realize ferroelectric thin film tunable microwave devices in parallel-plate configuration, to maximize its tunablity, by substrate transfer technology (SST) to lift the stringent requirement on the metallic electrodes. However, varactors and microstrip transmission lines fabricated in this way were found to be short circuited. This was found to be resulted by micro-cracks originating from the SiO_2/BST interface due to the large thermal expansion mismatch. (*chapter 2*)

- The tunability of ferroelectric varactors utilizing thick (>1μm) ferroelectric films can be increased by implementing nano-dot electrodes. Using a semi-analytic model, it was found that the tuning factor of a single nano-dot varactor built on a thick BST layer can reach values higher than 2, even with a dc bias voltage as low as 5V. Arrays of nano-dot varactors were then proposed to achieve sufficient capacitance densities. Their behavior as function of the dot radius and separation, as well as the thickness of the isolating layer were studied and it was found that the nano-dot array can maintain the high tuning factor of a single dot, provided that the inter-dot distance does not become too small. (*chapter 3*)

- A novel method for reducing the substrate loss of Si-based integrated CPW transmission lines was introduced by exploiting the shielding effect of a thin film layer with a high in-plane dielectric constant. This can be realized either by ferroelectric material with super high dielectric constant or an artificial dielectric layer proposed by us which can be modeled as an effective media with extremely high dielectric constant. The ADL comprises two patterned metal layers separated by a thin conventional dielectric, and can be readily built in a standard IC process. It was found that the ADL shield significantly lowers the attenuation, but only moderately changes the characteristic impedance of the transmission lines. (*chapter 4*)

- It was experimentally shown that the shield effectiveness of ADL can be improved by increasing the metallic element size, while micro-patterning the ADL to suppress the eddy current loss. By this way, it was demonstrated that CPW built on ordinary conductive silicon can achieve comparable total attenuation as the one fabricated on HRS substrate. We also showed that the shield effectiveness can alternatively be improved by stacking a few ADL layers. Loss reduction of CPW based microwave devices, i.e. branch-line coupler and ring hybrid, by applying ADL shields were demonstrated by simulation and/or experiment. The ADL shield was also shown, by simulation and experiment, to potentially be applied to on-chip spiral inductors to optimize their quality factors. (*chapter 4*)

- On-chip microwave resonator based on ADL was proposed and theoretically investigated. It was shown by full wave simulation that the quality factor of ADL resonators can potentially be as high as more than 100. The ADL resonators were also experimentally demonstrated with clear resonance characteristics. The degradation of quality factor in experiment was attributed to high resistance loss in ADL metallic patterns. (*chapter 5*)

6.2 Recommendations

Since BST a very good candidate material for tunable microwave devices, and by substrate transfer technology, the complete use of the tunability of BST can be achieved, further investigation to eliminate micro-crack formation during deposition is highly recommended. Applying seed layers other than SiO_2, which has lower lattice mismatch with BST such as titanium oxide, is one candidate to obtain crack free BST film. Yet it has to be verified by further experiments.

Although the tunability enhancement of ferroelectric thick film varactors is theoretically investigated, experiments have to be designed and carried out to verify this effect. However, to fabricate the dot arrays in nanometer scale, advanced lithography, such as e-beam lithography, has to be applied. One possible quick way of test is to use an atomic force microscopy (AFM) working at its capacitance measurement mode. Since the head of the cantilever in an AFM system is usually in tens of nanometer range, if one can

apply certain bias voltage on it, the varactor characteristic can be obtained by measuring capacitance as function of DC bias. It should be mentioned that, however, the dot array varactor can not be tested in this way.

In addition to the discussed micro-patterning and multi-layered ADL shield to enhance the shielding efficiency, the insulating dielectric can also be substituted by material with higher dielectric constant such as TiO_2. Another benefit to implement TiO_2 is that for the same effective in-plane dielectric constant value, a smaller ADL pattern size will be chosen, therefore, reducing the eddy current loss. Furthermore, the micro-patterning ADL is not optimized. Calculation is necessary to find the best patterning shape to minimize the eddy current loss and also minimize the metallic pattern resistance.

Although ADL resonators with clear resonances have been successfully fabricated, it is just a proof of principle. Compared with simulation results, the quality factor is substantially low. To diagnose this issue, further investigation has to be carried out. First, it is necessary to measure the dielectric loss of the insulating dielectric, i.e. the 30nm aluminum oxide layer. To gather a complete understanding of the ADL media, devices have to be designed to measure the effective dielectric constant and loss tangent of the ADL with certain accuracy. Furthermore, ADL resonators on HRS substrate were not successfully demonstrated with unknown reasons. More efforts need to be given to find the root causes, because Si is such an important substrate for future MMIC.

Appendix A

Ferroelectric Phase Transition

In this appendix, a brief introduction to the phenomenological theory, also known as Landau-Ginzburg-Devonshire (LGD) theory [1] of ferroelectric phase transition is given. This is indeed a macroscopic theory without regard to any atomic structure. Nevertheless, it is helpful to understand the macroscopic phenomena related to spontaneous polarization and ferroelectric phase transitions.

In general, many approaches can be taken to understand the origin of spontaneous polarization and the ferroelectric phase transition. From a lattice dynamics point of view, a displacive ferroelectric transition occurs if a transverse optical phonon mode "softens" until its frequency reaches zero and wavelength becomes infinite at Curie temperature [2]. In another word, the soft mode vibration locks in a displacive distortion, which creates spontaneous polarization necessary for ferroelectricity.

In contrast to the microscopic theory of soft phonon mode, another way to look at the same problem is through phenomenological or macroscopic theory. The phenomenological theory of ferroelectrics is indeed thermodynamic. In general, the thermal, electrical and mechanical properties of a crystal are related to each other. The main task of a phenomenological theory is to explain the properties of a crystal by as few parameters as possible, in order to clarify the relationship between observed properties. Among the possible thermodynamic functions, the elastic Gibbs energy G_1, which is obtained from the internal energy U by the following transformation $G_1 = U - TS - X_i x_i$, is usually used for ferroelectric phase transition, where T is

temperature, S is entropy, X_i and x_i are strain and stress of the crystal respectively [3].

For simplicity, in the following discussion, only a one dimensional problem is considered. It will nevertheless reveal the essential characteristics of ferroelectric phase transition. Following Landau, the elastic Gibbs free energy can be expressed as a power series of the order parameter, the electric polarization P (the order parameter is the macroscopic parameter that appears in the less symmetric phase in a symmetry-breaking phase transition):

$$G_1 = G_{10} + \tfrac{1}{2}\alpha P^2 + \tfrac{1}{4}\beta P^4 + \tfrac{1}{6}\gamma P^6 , \tag{A.1}$$

where G_{10} is the elastic Gibbs free energy when polarization is zero and α, β, γ depend, in general, on temperature. The use of G_1 is because, in the first place, it gives the relations between E and P under ordinary experimental conditions (constant temperature and constant stress) and, in the second place, is related to the Gibbs free energy G by the expression of $G_1 = G - E \cdot P$. In the absence of the electric field, i.e., $E = 0$, the two are the same. Notice that the series only contains even powers of P because the free energy does not change with polarization reversal. It should also be mentioned that the value of γ should be positive since otherwise the state of infinite spontaneous polarization will be the stable phase. This formulation should be applied for both the paraelectric and ferroelectric phase over the whole temperature range [3].

It then can be shown that the electric field E can be found by the first derivative of G_1:

$$E = \frac{\partial G_1}{\partial P} = \alpha P + \beta P^3 + \gamma P^5 . \tag{A.2}$$

Particularly, when E=0 one obtains

$$P(\alpha + \beta P^2 + \gamma P^4) = 0 . \tag{A.3}$$

whose solution is given by

$$P_s^2 = \frac{-\beta \pm \sqrt{\beta^2 - 4\alpha\gamma}}{2\gamma} , \tag{A.4}$$

If the right hand side of the above relation is positive, and if the substitution of P_s in Eq. (A.1) leads to a free energy less than G_{10}, then one has a stable spontaneously polarized state. Otherwise, the paraelectric phase is the stable state of the system [3].

Depending on whether β is positive or negative, a second order or first order phase transition will be found (the *n*th order phase transition is one in which the (*n*-1)th derivative of Gibbs energy is continuous while the *n*th shows a jump at the transition temperature).

In the case of $\beta>0$, (A4) yields an acceptable solution only if $\alpha<0$ and

$$P_s^2 = \frac{-\beta + \sqrt{\beta^2 - 4\alpha\gamma}}{2\gamma}. \tag{A.6}$$

If $|\alpha|\gamma << \beta^2$, which is the case of most real ferroelectric crystals, we obtain:

$$P_s^2 = -\alpha / \beta. \tag{A.7}$$

By substituting this equation into the power series for the elastic Gibbs energy, and taking $G=G_1$ when $E=0$ and $G_0=G_{10}$ into consideration, we have

$$G - G_0 = -\frac{\alpha^2}{4\beta}. \tag{A.8}$$

Therefore, we see that the above solution of P_s gives a smaller Gibbs free energy than when $P_s=0$, and thus the spontaneously polarized phase becomes stable.

As stated earlier, the coefficients of the power series are generally temperature dependent. One frequently expresses α as a function of temperature in the form of Taylor expansion of temperature including only the first order term:

$$\alpha = \frac{1}{\varepsilon_0 C}(T - T_0). \tag{A.9}$$

The requirement for the occurrence of spontaneous polarization is that $\alpha<0$, and so that $T<T_0$. In this case, we have $T_0=T_c$. When the temperature is above the Curie temperature, for weak electric fields, we can express the reciprocal of dielectric susceptibility as

$$\chi^{-1} = \varepsilon_0 \left(\frac{\partial E}{\partial P}\right)_{P=0} = \varepsilon_0 \alpha = \varepsilon_0 \frac{T - T_0}{\varepsilon_0 C} = \frac{T - T_0}{C}. \tag{A.10}$$

And the relative dielectric constant is given by

$$\varepsilon_r = 1 + \chi = 1 + \frac{C}{T - T_0}. \tag{A.11}$$

Since normally in ferroelectric materials $\chi >>1$, we can ignore the 1 term, which just

gives the Curie-Weiss law.

Besides, by substituting Eq. (A.9) into Eq. (A.7), one finds for $T<T_0$

$$P_s = \sqrt{\frac{T_0 - T}{\varepsilon_0 \beta C}}\,, \tag{A.12}$$

which implies a continuous change of spontaneous polarization to zero at the Curie point. Furthermore, substituting Eq. (A.9) into Eq. (A.8), one obtains

$$G - G_0 = -\frac{1}{4\beta}\left(\frac{1}{\varepsilon_0 C}\right)^2 (T - T_0)^2\,, \tag{A.13}$$

which clearly shows a second order transition as defined previously.

For the case of $\beta<0$, a similar analysis can be carried out. Here we restrict ourselves to a brief outline of the results : (1) The Curie-Weiss law is still valid; (2) The Curie point or phase transition temperature T_c does not coincide with the Curie-Weiss temperature T_0, but given by

$$T_c = T_0 + \frac{3}{16}\cdot\frac{\beta^2 \varepsilon_0 C}{\gamma}\,; \tag{A.14}$$

(3) The phase transition is first order and the spontaneous polarization changes abruptly near T_c. [3]

Finally, it is worth mentioning that the phenomenological theory can also be used to discuss the influence on polarization by strain and stress and is also applied to thin ferroelectric films.

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Appendix B

Process Flow for the Fabrication of Microwave Ferroelectric Devices

The following steps are on silicon wafer:

1. **Substrate**: Silicon wafer; in this work: p-type (100) Si, resistivity=2-5Ω-cm, thickness=525±15μm; but other common Si substrates can be used as well.
2. **Coating and baking**: 1.4μm Shipley SPR 3012 photoresist, 95°C, 1 min.
3. **Alignment and exposure**: Define the alignment mark for substrate transfer.
4. **Developmen**t: 115°C 1 min, Shipley MF322 developer, 100°C 1 min.
5. **Alignment and exposure**: Define the alignment mark.
6. **Development**: 115°C 1 min, Shipley MF322 developer, 100°C 1 min.
7. **Si etching**: 1μm Si trench etching, Trikon Omega 201 plasma etcher.
8. **Cleaning**: Photoresist strip in oxygen plasma, clean in 100% HNO_3, 10 min,

rinse in demineralized water, clean in 65% HNO_3 (110°C), 10 min, rinse in demineralized water, dry.

9. **Thermal oxidation**: 500nm oxidation of silicon, 1100°C, 200 min.
10. **Ferroelectric layer deposition**: 100nm BST by CSD method.
11. **Coating and baking**: 2μm Shipley SPR 3017 photoresist, 95°C, 1 min.
12. **Alignment and exposure**: Open the ground metal contact.
13. **Development**: 115°C 1 min, Shipley MF322 developer, 100°C 1 min.
14. **Ferroelectric layer wet etching**: 100nm BST wet etching, 2.5% HF.
15. **Cleaning**: Photoresist strip in acetone (40°C), clean in PRS 3000 (90°C), 20 min, rinse in demineralized water, dry.
16. **First metallization**: 4μm Al sputter deposition, room temperature, Trikon Sigma sputter coater.
17. **Coating and baking**: 2μm Shipley SPR 3017 photoresist, 95°C, 1 min.
18. **Alignment and exposure**: Define the ground pattern.
19. **Development**: 115°C 1 min, Shipley MF322 developer, 100°C 1 min.
20. **Al etching**: 4μm Al etch, 25°C, Trikon Omega plasma etcher.
21. **Cleaning**: Photoresist strip in oxygen plasma, clean in PRS 3000 (90°C), 20 min, rinse in demineralized water, dry.

The following steps are on AF45 glass wafer:

1. **Cleaning**: Clean in 100% HNO_3, 10 min, rinse in demineralized water, dry.
2. **Al sputtering**: 100nm Al sputtering, Trikon Sigma sputter coater.
3. **Coating and baking**: 1.4μm Shipley SPR 3012 photoresist, 95°C, 1 min.
4. **Alignment and exposure**: Define the alignment mark for substrate transfer.
5. **Development**: 115°C 1 min, Shipley MF322 developer, 100°C 1 min.
6. **Al wet etching**: 100nm Al etch, Merck selectipur, 45 sec.
7. **Cleaning**: Photoresist strip in acetone (40°C), clean in 100% HNO_3, 10 min,

rinse in demineralized water, dry.

8. **Oxide deposition**: 3μm PECVD SiO2 deposition on both sides, 400°C. Novellus PECVD system.

The following steps are substrate transfer processing:

1. **Oxide deposition**: 1μm PECVD SiO2 deposition on Si wafer, 400°C. Novellus PECVD system.
2. **Primer treatment**: Coat primer on both Si and AF45 wafers, keep in close box for 24 hours.
3. **Glueing**: Manually spread glue on Si wafer.
4. **Stick wafers**: Manually stick AF45 wafer on Si wafer. Visually inspect the alignment marks on both wafers.
5. **Pressure on wafers**: Supply 0.2 bar pressure on the wafers, 5 min.
6. **UV light treatment**: Supply UV light on the wafers, 5 min.
7. **Cleaning**: Acetone, room temperature, 1 min.
8. **Baking**: Bake the wafers on hotplate, 250°C, 2min.
9. **Cleaning**: Clean in 100% HNO_3, 10 min, rinse in demineralized water, dry.

The following steps are on the backside of the silicon side of the glued wafer unless specified:

1. **Coeating and baking (on front side – AF45)**: 2μm Shipley SPR 3017 photoresist, 95°C, 1 min.
2. **Oxide removal**: 500nm SiO2 etch, BHF (1:7), rinse in demineralized water, dry.
3. **Cleaning**: Photoresist strip in acetone (40°C), clean in 100% HNO_3, 10 min, rinse in demineralized water, dry.
4. **HF dip**: Dip in 0.55% HF, 30 sec, rinse in demineralized water, dry.
5. **Si etching**: Etch completely the Si wafer, 25% TMAOH (80°C), 14 hours, rinse in demineralized water, dry.

6. **Cleaning**: Clean in PRS 3000 (90°C), 20 min, rinse in demineralized water, dry.
7. **Al coating on front side**: For wafer detection in the following steps. 1.8µm Al sputtering, Trikon Sigma sputter coater.
8. **Coating and baking**: 1.4µm Shipley SPR 3012 photoresist, 95°C, 1 min.
9. **Alignment and exposure**: Open the contact for second metal layer.
10. **Development:** 115°C 1 min, Shipley MF322 developer, 100°C 1 min.
11. **Oxide etching**: 500nm SiO2 wet etching, BHF (1:7).
12. **Cleaning**: Photoresist strip in acetone (40°C), clean in PRS 3000 (90°C), 20 min, rinse in demineralized water, dry.
13. **Second metallization**: 1.4µm Al deposition, using low thermal budget recipe, Trikon Sigma sputter coater.
14. **Coating and baking**: 1.4µm Shipley SPR 3012 photoresist, 95°C, 1 min.
15. **Alignment and exposure**: Define the top metal patterns.
16. **Development**: 115°C 1 min, Shipley MF322 developer, 100°C 1 min.
17. **Al etching**: 1.4 µm Al wet etching, Merck selectipur, rinse in demineralized water, dry.
18. **Cleaning**: Photoresist strip in acetone (40°C), clean in PRS 3000 (90°C), 20 min, rinse in demineralized water, dry.

Appendix C

Derivation of effective magnetic susceptibility of ADL

In this appendix, we derive the approximate effective magnetic susceptibility of ADL by using the quasi-static approximation of Maxwell's equations. Consider a thin metallic pattern of arbitrary shape under a uniform RF magnetic field. The assumption of uniformity of the magnetic field is justified as the size of the ADL patterns does not exceed the micron range which is several orders of magnitude smaller than the (effective) electromagnetic wavelength at microwave frequencies. Note also that this magnetic field may be the superposition of an externally applied field (e.g., by other current-carrying structures) and an internal field induced by the currents in the patterns themselves.

Due to the magnetic field, currents will be induced inside the metallic pattern according to the Lenz's law. Suppose the thickness of the metallic layer is much smaller than the skin depth at frequency of interest, like the thin Al layer in our ADL structure. The density of the eddy currents induced will be uniform along the thickness of the metal. Besides, one may neglect the vertical component of the current density vector so that a two dimensional approximation will suffice. In Fig. C.1, we show a single micro-patterned ADL under a uniform RF magnetic field. The coordinate system used in

the following derivation is also shown.

Next, consider the Maxwell equations in frequency domain. By combining the curl equation of electric field and the ohm's law inside the metallic pattern, we have,

$$\frac{\partial J_y}{\partial x} - \frac{\partial J_x}{\partial y} = -j\omega\sigma_M B_z , \tag{C.1}$$

where $\boldsymbol{J} = \hat{\boldsymbol{x}} J_x + \hat{\boldsymbol{y}} J_y$ is the current density within the metallic region, ω is the angular frequency, σ_M is the conductivity of the metal and B_z is the normal component of the magnetic field. Inside the metallic region (Ω in Fig. C.1) where there are no volume charges, the current continuity equation reads,

$$\nabla \cdot \boldsymbol{J} = \frac{\partial J_x}{\partial x} + \frac{\partial J_y}{\partial y} = 0 . \tag{C.2}$$

Since $\boldsymbol{J}$ is divergence free and has only x and y components, it can be represented in terms of a scalar potential ψ:

$$\boldsymbol{J} = \hat{\boldsymbol{x}} \frac{\partial \psi}{\partial y} - \hat{\boldsymbol{y}} \frac{\partial \psi}{\partial x} . \tag{C.3}$$

Substituting eq. (C.3) into eq. (C.1), one ends up with a Poison equation for ψ:

$$\left(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} \right) \psi = j\omega\sigma_M B_z . \tag{C.4}$$

In order to find a unique solution, this equation has to be supplemented by boundary conditions for the potential function at the edges of the metallic pattern. Since the structure is small compared to the electromagnetic wavelength, we adopt the quasi-static approximation in which the accumulation of electric charge on the surface of a conductor are neglected. Thus, we require the normal component of the current density vector to vanish on the boundary curve of the pattern which we denote as *C*. Now we define two direction unit vectors $\hat{\boldsymbol{n}}$ and $\hat{\boldsymbol{\tau}}$, which are the unit vectors normal and along the boundary C, as shown in Fig. C.1. By doing so, the boundary condition reads,

$$\hat{\boldsymbol{n}} \cdot \boldsymbol{J} = 0 \qquad \text{along } C. \tag{C.5}$$

Substituting eq. (C.3) into eq. (C.5) and using the relation between the two unit vectors, one finds,

$$\hat{\boldsymbol{\tau}} \cdot \nabla \psi = 0 \quad \text{or} \quad \frac{\partial \psi}{\partial \tau} = 0 \qquad \text{along } C. \tag{C.6}$$

This implies that the potential function ψ does not change on C, thus it can be taken to be a constant on this boundary curve. For a single pattern, the value of this constant will be arbitrary as it will neither affect the Poisson equation nor the current density. To simplify the calculation we demand $\psi = 0$ on C. The Poison's equation eq. (C.4) combined with this boundary condition can then be solved numerically.

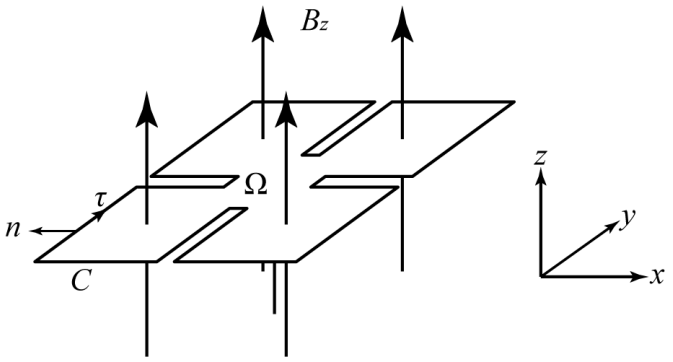

Figure C.1 A single ADL pattern under normal magnetic field. Also the coordinate system is shown.

Once this equation is solved, we consider the magnetic moment induced by the flow of the eddy current calculated above in a single metallic pattern, which is given by [1],

$$\boldsymbol{m} = \frac{1}{2}\int_V \boldsymbol{r} \times \boldsymbol{J} dv \,. \tag{C.7}$$

Substituting eq. (C.3) into eq. (C.7), one finds,

$$\boldsymbol{m} = -\hat{\boldsymbol{z}}\frac{t}{2}\int_\Omega \boldsymbol{r} \cdot \nabla\psi \, dA \,, \tag{C.8}$$

where dA is differential area on Ω. Using the fact that $\boldsymbol{r} = \frac{1}{2}\nabla r^2$, and Green's first identity [1] combined with eq. (C.4), we have

$$\boldsymbol{m} = -\hat{\boldsymbol{z}}\frac{t}{4}\left[\oint_C r^2(\hat{\boldsymbol{n}} \cdot \nabla\psi) dl - j\omega\sigma_M B_z \int_\Omega r^2 dA\right]. \tag{C.9}$$

Note that in this equation, $\boldsymbol{m}$ linearly depends on B_z as ψ linearly depends on B_z

which was considered to be uniform.

Next, we calculate the magnetization of ADL. To that end, we define a volume filling factor *f*, which is the ratio of the volume of one ADL pattern to that of a unit cell. The magnetization then reads,

$$\boldsymbol{M} = f\frac{\boldsymbol{m}}{V_s}, \tag{C.10}$$

where V_s is the volume of a single ADL pattern and is given by

$$V_s = t\int_{\Omega} dA\,. \tag{C.11}$$

The magnetization is also in the z-direction and a linear function of B_z. Let γ denote the ratio $\mu_0 M_z / B_z$. For a square pattern with the side D, $\gamma = -j\eta_M f\omega\mu_0\sigma_M D^2$ where η_M is a dimensionless, geometry-independent factor which is calculated by solving the Poison's equation.(C.4)

We now have a relationship between the volume magnetization of an ensemble of patterns on the one hand, and the normal component of the RF magnetic field on the other hand. The effective susceptibility of ADL in ***z*** direction $\chi_\perp = M_z / H_z$ can now be evaluated with the help of

$$\boldsymbol{B} = \mu_0\left(\boldsymbol{H} + \boldsymbol{M}\right). \tag{C.12}$$

which leads to $\chi_\perp = \gamma/(1-\gamma)$.

Note that we did not consider the case where the magnetic field is tangential to the plane of the pattern. This is because the patterns are very thin and the eddy current induced will not be significant in this case.

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Appendix D

Derivation of shielding effect of ADL

In this appendix, we theoretically investigate the substrate shielding effect of an artificial dielectric layer (ADL) inserted in between a CPW transmission line and the Si substrate. The geometry of the problem is illustrated in Fig. (D.1). The calculation is based on the quasi-TEM approximation in which the electric and magnetic fields surrounding the transmission line are separately treated using the electro-, respectively, magneto-static approximations. This is justified for CPW lines at not too high frequencies, i.e. the frequency range of our interest.

In the quasi-TEM approach the transverse electric field can be expressed as the gradient of an electrostatic potential $\varphi(x,y)$ on the line cross section, which is governed by Laplace equation,

$$\nabla \cdot (\overline{\overline{\varepsilon}} \cdot \nabla \varphi) = 0 , \qquad \text{(D.1)}$$

where the second rank permittivity tensor $\overline{\overline{\varepsilon}}$ has been used for the sake of generality. In the Si and oxide regions, where permittivity is a scalar, eq. (D.1) reads

$$(\frac{\partial^2}{\partial x^2}+\frac{\partial^2}{\partial y^2})\varphi(x,y)=0, \qquad (y\le 0, t\le y\le t+h) \tag{D.2}$$

where t is the thickness of the ADL and h is the thickness of the oxide layer. In ADL, due to its anisotropy of the dielectric properties, the permittivity is represented as a second rank tensor, and Laplace equation (D.1) reads,

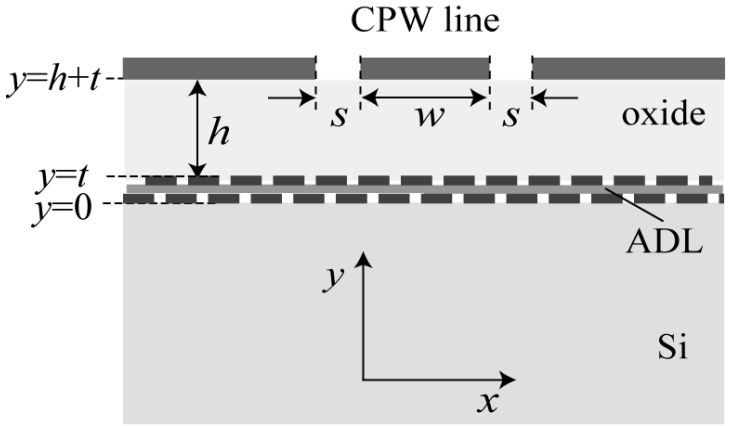

Figure D.1 Geometrical layout of CPW with ADL shield. The thickness of the ADL and oxide are t and h respectively.

$$(\frac{\varepsilon_{\parallel}}{\varepsilon_{\perp}}\frac{\partial^2}{\partial x^2}+\frac{\partial^2}{\partial y^2})\varphi(x,y)=0, \qquad (0\le y\le t), \tag{D.3}$$

where $\varepsilon_{\parallel}$ and $\varepsilon_{\perp}$ are the in-plane (in x-direction) and out-of-plane (in y direction) permittivity respectively.

To simplify the analysis, we assume an unbounded substrate (in x-direction) and transform eq. (C.2-3) to the spectral domain by applying a Fourier transform with respect to x to the potential:

$$\tilde{\varphi}(k,y)=\int_{-\infty}^{\infty}\varphi(x,y)\exp(jkx)dx \tag{D.4}$$

where k is the wave number, The equations for the Fourier transformed potential

$\tilde{\varphi}(x,y)$ are

$$(-k^2+\frac{\partial^2}{\partial y^2})\tilde{\varphi}(k,y)=0, \qquad (y\le 0, t\le y\le t+h) \tag{D.5}$$

$$(-q^2+\frac{\partial^2}{\partial y^2})\tilde{\varphi}(k,y)=0, \qquad (0\le y\le t) \tag{D.6}$$

with $q=k(\varepsilon_{\|}/\varepsilon_{\perp})^{1/2}$. The Fourier transformed electric field can be written in terms of $\tilde{\varphi}(k,y)$ as

$$(\tilde{E}_x,\tilde{E}_y)=(ik,-\frac{\partial}{\partial y})\tilde{\varphi}(k,y)\,. \tag{D.7}$$

Since the thickness of the Si substrate (>500μm) is much larger than the signal line width and signal to ground spacing of the CPW lines under consideration (tens of μm), the Si substrate is assumed to be infinitely thick for simplicity. This leads to the following boundary condition for the potential

$$\tilde{\varphi}(k,y=-\infty)=0 \tag{D.8}$$

Let us denote the electrostatic potential on top of the oxide surface by $\varphi(x,t+h)=V(x)$ which reads in its Fourier transformed form,

$$\tilde{\varphi}(k,t+h)=\int_{-\infty}^{+\infty}V(x)\exp(jkx)dx\,. \tag{D.9}$$

By combining eq.(D.8-9) and the boundary conditions of the continuity of tangential electric field $\tilde{E}_x$ and normal electric displacement field $\tilde{D}_y$ at Si/ADL and ADL/oxide interfaces, one can solve the spectrum domain Laplace equation (D.5-6) in the three regions. The Fourier transformed electrostatic potential $\tilde{\varphi}_{\mathrm{Si}}(k,y)$ in Si substrate then reads,

$$\tilde{\varphi}_{\mathrm{si}}(k,y)=\frac{\exp(|k|y)\int_{-\infty}^{\infty}V(x)\exp(ikx)dx}{A(k)\cosh(|k|h)+B(k)\sinh(|k|h)} \tag{D.10}$$

$$A(k)=\cosh(|q|t)+(\varepsilon_{\mathrm{si}}/\varepsilon_{\mathrm{e}})\sinh(|q|t) \tag{D.11}$$

$$B(k) = \varepsilon_{ox}^{-1}\left[\varepsilon_{si}\cosh(|q|t) + \varepsilon_{e}\sinh(|q|t)\right], \qquad \text{(D.12)}$$

where ε_{ox} is the dielectric constant of the oxide layer, $\varepsilon_e=(\varepsilon_{\|}\,\varepsilon_{\perp})^{1/2}$, and $\varepsilon_{si}=\epsilon_{si} - j\sigma_{si}/\omega$ with ϵ_{si} the dielectric constant and σ_{si} the conductivity of Si.

Appendix E

Extraction of Transmission Line Parameters

In this appendix, the method we adopt to extract the transmission line parameters from the scattering (S-) parameter measurements or simulations throughout this work is briefly outlined. For the measurement, a HP-8510 network analyzer, after a line-reflect-match (LRM) calibration procedure, was used to obtain two-port S-parameters. The S-parameters were transformed to impedance (Z-) parameters by the following relation

$$[Z] = Z_s([U]+[S])([U]-[S])^{-1}, \qquad \text{(E.1)}$$

where Z_s is the system impedance (50Ω in our case), $[Z]$, $[U]$ and $[S]$ are the 2x2 impedance, unitary and S-parameter matrices respectively [1]. The 2x2 admittance matrix

$[Y]$ is just the inverse of the impedance matrix [1], i.e.

$$[Y] = [Z]^{-1} . \tag{E.2}$$

For a transmission line of length l with characteristic impedance of Z_0 and the complex propagation constant γ, we define two impedance values of interests, i.e., Z_{open} and Z_{short} to be the input impedances from one port when the other port is open and short circuitry respectively. It is trivial to show that Z_{open} and Z_{short} can be extracted from the impedance and admittance matrices of the transmission line respectively as

$$Z_{\text{open}} = Z_{11} = \frac{Z_0}{\tanh(\gamma l)} , \tag{E.2}$$

$$Z_{\text{short}} = \frac{1}{Y_{11}} = Z_0 \tanh(\gamma l) . \tag{E.3}$$

Therefore, the characteristic impedance Z_0 and the propagation constant γ can be expressed as [2]

$$Z_0 = \sqrt{Z_{\text{short}} \cdot Z_{\text{open}}} , \tag{E.4}$$

$$\gamma = \frac{1}{l} \text{arctanh}(\sqrt{Z_{\text{short}} / Z_{\text{open}}}) . \tag{E.5}$$

The attenuation (α) and propagation (β) constants can then be found from

$$\gamma = \alpha + j\beta , \tag{E.6}$$

while the attenuation constant α is usually translated into dB form, i.e.

$$\alpha = (20 \log e) \operatorname{Re} \gamma . \tag{E.7}$$

Fig. E.1 shows an equivalent circuit model of a transmission line. Its parameters can be extracted from

$$\gamma = \sqrt{(R + j\omega L) \cdot (G + j\omega C)} , \tag{E.8}$$

$$Z_0 = \sqrt{(R + j\omega L) / (G + j\omega C)} , \tag{E.9}$$

by

$$R = \text{Re}(\gamma \cdot Z_0), L = \text{Im}(\gamma \cdot Z_0) / \omega, G = \text{Re}(\gamma / Z_0), C = \text{Im}(\gamma / Z_0) / \omega . \tag{E.10}$$

where ω is the angular frequency. The transmission line parameters thus can be extracted from S-parameter measurement. It is worth mentioning that, for CPW transmission line on Si, the series resistance R models the metal loss of CPW signal line and the substrate loss is counted by the shunt conductance term G.

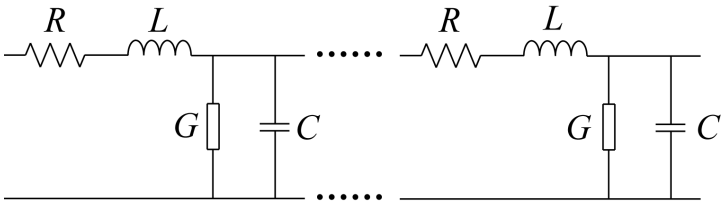

Figure E.1: Equivalent circuit model of a transmission line. L, R, C and G denote the series inductance, resistance and shunt capacitance, conductance (all per unit length), respectively.

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Summary

Title: Ferroelectric Materials and Artificial Dielectric Layer Structures for Microwave Integrated Circuit Technologies

By: Yue Ma

In traditional hybrid microwave circuits, microwave passive components like capacitors and inductors are directly built on the interconnect board. This leads to high total cost of microwave circuits and hinders their miniaturization. For that reason, monolithically integrated passive components are gradually replacing the discrete ones, but are limited by their large chip area consumption, high RF/microwave losses and limited functionality. This thesis is dedicated to address these issues by applications of ferroelectric materials and artificial dielectrics.

Chapter 1 provides an overview of challenges associated with passive components implemented within the standard Silicon (Si) IC technologies. Ferroelectric materials and artificial dielectric materials are then introduced and applications to microwave components are reviewed.

In Chapter 2, the preparation of BST ferroelectric thin films by the chemical solution deposition method is presented. Morphological and electrical characteristics of deposited BST thin films on a platinized Si substrate are experimentally studied. Substrate transfer technique is proposed for microwave tunable components which eliminates the use of platinum, a metal which is incompatible with the mainstream Si technology. Possible causes of the short circuited devices fabricated by the substrate transfer method are discussed and recommendations for further research are given.

Chapter 3 deals with the tunability enhancement of ferroelectric-based components by

smart device structure design, i.e. the implementation of nano-dot electrodes. Physical principles and theoretical models are presented for nano-dot varactors based on an electrostatic approximation. It is shown that the electric field near the nano-dot electrode is mainly determined by the dot size, rather than the voltage applied to it. Therefore, the tunability is enhanced by the large electric field near the nano-dot electrode. A more realistic varactor design by forming a nano-dot array is proposed and numerical simulations are carried out which show a high tuning range with a relatively low applied voltage.

In Chapter 4, a new artificial dielectric layer (ADL) structure is introduced which contains a conventional thin dielectric film sandwiched between two patterned metal layers. An effective medium model of the ADL structure is derived. The principles of the shielding effect of ADL on CPW transmission lines are shown by solving the Fourier transformed Laplace equations, which is based on a quasi-TEM approximation. It is also experimentally shown that by micro-patterning of ADL or stacking a few ADL layers, the shielding effect can be further increased. Applications of ADL shield, such as directional couplers and spiral inductors are also experimentally studied.

In Chapter 5, a new microwave resonator based on ADL is proposed and theoretically investigated. An equivalent circuit model is developed by solving the Maxwell's equations using Green's functions. Experimental results are compared with full wave simulation of the proposed ADL resonator. The degradation of the quality factor achieved by experiments compared with simulation is attributed to the resistance loss within ADL.

Chapter 6 outlines the major conclusions of this work and recommendations for possible future research topics related to this thesis.

Samenvatting

Titel: Ferroelectric Materials and Artificial Dielectric Layer Structures for Microwave Integrated Circuit Technologies

Door: Yue Ma

Passieve microgolf componenten, zoals condensatoren en inductoren, worden in traditionele hybride microgolf circuits direct op de printplaat geplaatst. Dit gaat gepaard met hoge kosten en bemoeilijkt miniaturisatie. Om deze reden vervangen monolithisch geïntegreerde passieve componenten steeds meer de discrete componenten. Echter, monolithisch geïntegreerde passieve componenten vereisen een groot chip oppervlak, hebben een groot RF/microgolf verlies en hebben beperkte functionaliteit. Deze thesis beschrijft hoe door het toepassen van ferroelektrische materialen deze nadelen kunnen worden voorkomen.

Hoofdstuk 1 geeft een overzicht van de uitdagingen voor passieve componenten die gemaakt worden met standaard IC technologie op basis van silicium (Si). Ferroelektrische materialen en kunstmatige diëlectrica worden vervolgens geïntroduceerd en hun toepassingen in microgolf componenten besproken.

In hoofdstuk 2 wordt de fabricage van dunne BST ferroelektrische lagen met chemical solution deposition gepresenteerd. Morfologische- en elektrische karakteristieken van gedeponeerde BST lagen op een platinized silicium substraat worden experimenteel bestudeerd. Voor variabele microgolf componenten wordt een substraat overdracht techniek voorgesteld die het gebruik van platinized silicium substraten voorkomt. Platina is namelijk een metaal dat niet compatibel is met gangbare Si technologie. Mogelijke oorzaken van kortsluiting in devices die zijn gefabriceerd met de substraat transfer techniek worden besproken. Ook worden aanbevelingen gedaan voor toekomstig

onderzoek.

Hoofdstuk 3 gaat over de vergroting van de verstelbaarheid van ferroelektrische componenten door slim device ontwerp, bijvoorbeeld door de implementatie van nano-dot elektrodes. Fysische principes en theoretische modellen gebaseerd op een elektrostatische benadering worden gepresenteerd voor nano-dot varicaps. Aangetoond wordt dat het elektrische veld bij de nano-dot elektrode voornamelijk wordt bepaald door de dot-grootte en in mindere mate door de aangelegde spanning. De instelbaarheid van de varicap wordt hierdoor vergroot. Een ontwerp van een nano-dot varicap array wordt voorgesteld met een capaciteit groot genoeg voor praktische toepassing. Numerieke simulaties laten een groot instelbereik zien bij een relatief klein spanningsbereik.

Hoofdstuk 4 introduceert een nieuwe kunstmatige diëlectricum laag (artificial dielectric layer, ADL) die bestaat uit een conventioneel diëlectricum tussen twee gepatroneerde metaallagen. De ADL structuur wordt gemodelleerd met een macroscopische beschrijving. Gecombineerd met een oplossing van Fourier getransformeerde Laplace vergelijkingen gebaseerd op een quasi-TEM benadering beschrijft dit model het afschermingeffect van de ADL structuur op CPW transmissielijnen. Experimenteel wordt aangetoond dat met het patroneren van de ADL, of het stapelen van een verscheidene ADL lagen, de afscherming verder kan worden verhoogd. Verder worden toepassingen van ADL afscherming in één-richtings transmissie koppelingen en spiraalinductoren experimenteel bestudeerd.

In hoofdstuk 5 wordt een nieuwe op ADL gebaseerde microgolf resonator voorgesteld en theoretisch onderzocht. Een model van een equivalent circuit wordt ontwikkeld middels het oplossen van de Maxwell vergelijkingen met behulp van Green's functies. Experimentele resultaten worden vergeleken met simulatie van de voorgestelde ADL resonator. Het verschil tussen de experimenteel bepaalde kwaliteitsfactor en de gesimuleerde kwaliteitsfactor wordt toegeschreven aan het weerstandsverlies binnen de ADL.

Hoofdstuk 6 geeft een overzicht van de belangrijkste conclusies en geeft aanbevelingen voor mogelijk toekomstig onderzoek dat is gerelateerd aan deze thesis.

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Yue Ma was born on October 16, 1976 in Tianjin, P. R. China. He received the bachelor and master degrees both in materials science and engineering from Tsinghua University in 2000 and 2003 respectively. He worked for Applied Materials China as a process support engineer afterward. In January 2005, he joined the High-frequency Technologies and Components Group in Delft University of technology as a PhD candidate. There he worked on the implementation of ferroelectric and artificial dielectric materials in monolithic microwave integrated circuit technologies. He is working for MAPPER Lithography B.V. as an experimental physicist since March 2009.