AN INTEGRATED HIGH-VOLTAGE PULSER WITH IMPROVED HD2 AND PROGRAMMABLE AMPLITUDE

by

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ABSTRACT

Miniature ultrasound probes increasingly employ Application-Specific Integrated Circuit (ASIC) that drive the transducer elements with High Voltage (HV) pulses and process the received echo signals. Due to size constraints, the HV pulsers tend to be relatively simple circuits, in which HV MOS transistors pull the transducer element to a HV supply and back to ground. An important disadvantage of existing designs is that the rising and falling edges of the generated pulses are not well matched, which leads to second-harmonic components in the generated pulse. This makes these design unsuited for harmonic imaging. Moreover, the pulse amplitude typically cannot be controlled, making it difficult to apply apodization techniques that are often desired to reduce sidelobes.

This work presents an ASIC design that addresses these disadvantages. The content discussed in this thesis includes the circuit architecture, circuit implementation and analysis of simulation results for an integrated HV pulser with improved Second Order Harmonic Distortion (HD2) and programmable amplitude enabling apodization.

The design consists of two parts: a transmit driver and the HV pulser. The transmit driver, composed of a negative feedback loop with a replica pulser, a level shifter and other components, can generate a lower HD2 by auto-calibrating the pull-up and pull-down time. It can be shared by multiple HV pulsers that drive the transducer elements. A combination of duty-cycle modulation and slew-rate modulation is proposed for pulse-amplitude control.

Finally, an experiment aimed to explore the effective acoustic power of transducer under high and low impedance drive modes is proposed. These drive modes are first investigate by simulating the transducer driven by an ideal current and an ideal voltage source. Then, an experimental circuit is proposed in which the transducer is connected to an OpAmp in different ways to achieve similar impedance conditions as in the ideal situation to verify whether there is a large gap in the acoustic power.

Keywords: harmonic imaging, HD2, apodization, HV pulser.

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ACRONYMS

HV High Voltage . . . iii
CT Computed Tomography . . . 1
MRI Magnetic Resonance Imaging . . . 1
PRF Pulse Repetition Frequency . . . 2
DSP Digital Signal Processor . . . 3
LV Low Voltage . . . 3
TX Transmit Circuitry . . . 3
RX Receive Circuitry . . . 3
T/R Transmit/Receive . . . 3
LNA Low Noise Amplifier . . . 3
ADC Analog-to-Digital Converter . . . 3
HI Harmonic Imaging . . . 4
SNR Signal-to-Noise Ratio . . . 3
HV BCD HV Bipolar-CMOS-DMOS . . . 4
HD2 Second Order Harmonic Distortion . . . iii
ASIC Application-Specific Integrated Circuit . . . iii
PWM Pulse Width Modulation . . . vii
SRM Slew Rate Modulation . . . vii
V_{OV} Overdrive Voltage . . . 15
V_{GS} Gate-Source Voltage . . . 22
V_{DS} Drain-Source Voltage . . . 23
I_D Drain Current . . . 22

1 INTRODUCTION

With the improvement of social economy and people's living standards, the aging of the population, and the transformation of the medical service system, the need for safe, effective and minimally-invasive or non-invasive diagnosis and treatment methods continues to increase.

Medical ultrasound imaging brings one of the solutions to satisfy people's expectations. It provides a safe, cost-effective, portable, relatively fast and radiation-free method compared to Computed Tomography (CT), X-ray and Magnetic Resonance Imaging (MRI). Therefore, biomedical ultrasound imaging has become one of the most popular modalities for clinical examinations [4; 5; 6; 7].

This thesis aims to improve ultrasound imaging quality with a relatively small area and low power consumption. In this chapter, the background of ultrasound imaging and challenges from pulse transmission phase will be introduced. Next, the prior arts will be reviewed which will lead to the objectives of this thesis.

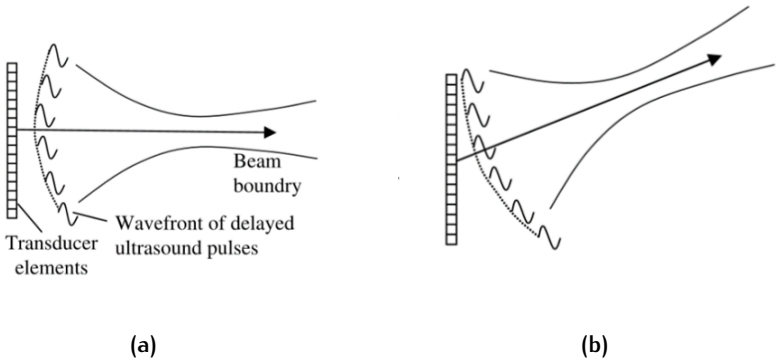


Figure 1.1: Ultrasound imaging functions. (a) Focused beam (b) Focusing and steering [8]

1.1 BACKGROUND OF ULTRASOUND IMAGING

1.1.1 Principle and Function of Ultrasound imaging

Acoustic impedance, which is a characteristic of each tissue, is the product of the speed of sound and the tissue density. Since the speed of sound is nearly constant at 1540 m/sec, the acoustic impedance of most soft tissue is mainly dependent on the tissue density [8]. The unique acoustic impedance of each tissue will produce impedance mismatch. The greater the mismatch, the larger the reflected sound wave. Corresponding to the final imaging stage, the brightness of the area will be higher in the case of large acoustic impedance mismatch [9].

To obtain a processable electrical signal, it is necessary to build a bridge to connect the electrical and acoustic characteristics. The key component is the transducer. Nowadays, the majority of ultrasound scanning probes employ a transducer array to achieve the ability of steering and focusing. They are realized by the relative phasing delays of the elements in the array. Focusing, as shown in Figure 1.1a, is to image a certain area clearly, and steering can change the angle of each beam to adjust the position of the focus, thereby expanding the scanning area. Typically, both functions are operated simultaneously as shown in Figure 1.1b [8].

1.1.2 Transmit/Receive Phase of Ultrasound Imaging

Figure 1.2 intuitively shows the complete process of obtaining a single beam. At the beginning of that is the configuration period. It aims to configure the control data for the transmit driver. After that, the overall circuit will enter the transmit phase. At this stage, the pulsers in the array will be activated sequentially according to the phase delay that has been set. The receive phase starts following the completion of the transmit phase and will last until all of the echoes have returned from the body. The echoes with different energy generated by tissues propagate back and will be converted into electrical signals through the transducer array. Pulse Repetition Frequency (PRF) indicates the number of transmission by the transducer per second. Typically,

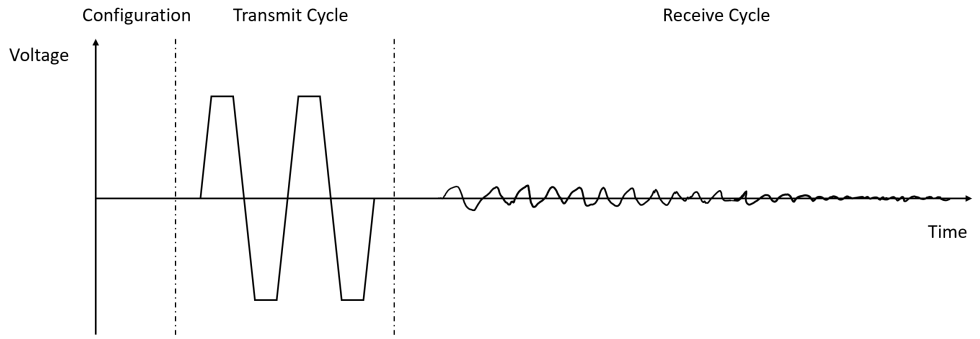


Figure 1.2: Voltage at the transducer during configuration, transmit and receive phase

cardiology imaging is operated at a PRF of around 10 kHz while abdominal imaging requires a PRF of $3-4$ kHz. Therefore, the transmit driver in the transmit phase does not have to keep working during the entire process. This is a benefit to the overall power consumption of the circuit [8; 10].

1.1.3 Ultrasound Imaging System

Figure 1.3 shows a simplified block diagram of an ultrasound imaging system. Clock and data are generated by a Digital Signal Processor (DSP). According to them, Low Voltage (LV) signals will be sent to the transmit driver to generate the relevant HV signals for the pulsers. Then the pulser drives the transducer array with a HV voltage. These pulses can excite the transducer array to produce a focused acoustic beam [11]. The Transmit Circuitry (TX) works in the HV domain, while the Receive Circuitry (RX) in the LV domain. It implies that RX needs to be isolated from TX. Therefore, a Transmit/Receive (T/R) switch is applied. During the transmit phase, the T/R switch will be connected to TX and disconnected from RX. And vice versa in the receive phase. Following the transmit phase, the receive phase begins. A Low Noise Amplifier (LNA) in the receive path is used to boost the weak signal received from the transducer array. The Analog-to-Digital Converter (ADC) following the LNA digitizes the signal amplified by the LNA so that it can be processed by the DSP [12; 13].

1.2 CHALLENGES WITH PULSE TRANSMISSION

1.2.1 High Transmit Voltages for SNR

The transmit power should be high enough to acquire a sufficiently high signal-to-noise ratio Signal-to-Noise Ratio (SNR) at the largest imaging depth, because the acoustic signal will be attenuated by the propagation through tissue. Therefore, pulsers should be capable of withstanding generating HV for instance 30 Vpp [14]. Since the standard CMOS technologies cannot withstand such a HV in the circuitry during the pulse transmission period. Thus,

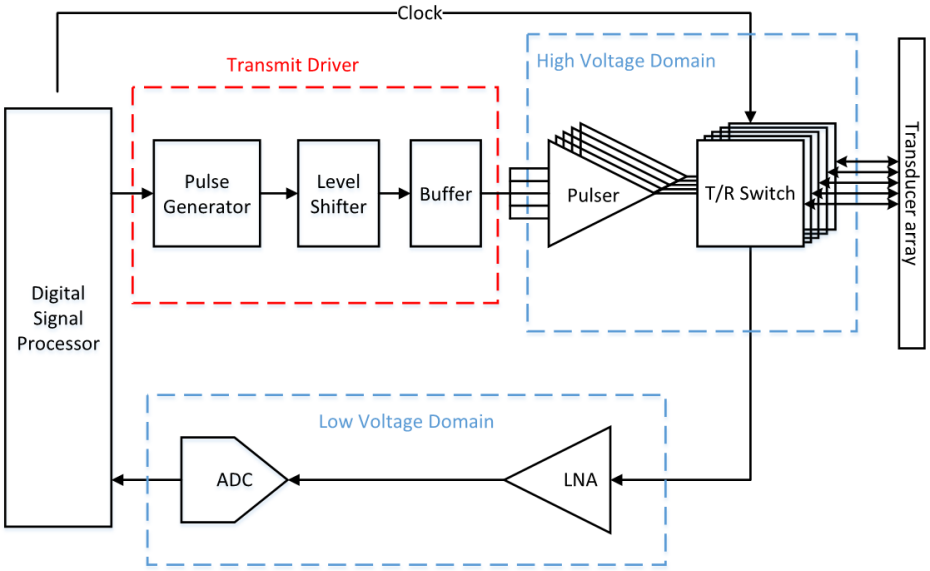


Figure 1.3: Block diagram of a typical ultrasound imaging system

another technology called HV Bipolar-CMOS-DMOS (HV BCD) is adopted [15; 16; 17]. However, compared to the standard CMOS technologies, HV transistors will occupy a larger die area, which will sacrifice a part of the available area in exchange for the HV endurance. In the guided invasive intervention miniaturized ultrasound probes, such as catheter-based probes, the available area for implementing the chip is limited. As the catheter-based systems will be inserted into the patient's body, comfortability is a key issue. In other words, the miniaturization of probes is an important development trend.

1.2.2 Pulse Amplitude Control for Apodization

The diffraction of ultrasonic waves leads to the appearance of sidelobes. Because time sidelobes in a pulse can appear to be false echoes, strong reflectors in a beam profile sidelobe region can interfere with the interpretation of on-axis targets. In the transmit phase, the sidelobes of the output signals should be reduced. Apodization is a method to lower the "sidelobes" on either side of the main beam. There are many ways to realize the apodization. In transducer arrays, apodization is accomplished by simply exciting individual elements in the array with different voltage amplitudes [18].

1.2.3 Low Harmonic Distortion for Harmonic Imaging

Harmonic Imaging (HI), as shown in Figure 1.4[1], is an ultrasonic pulse transmitted at the fundamental frequency and receives echo signals that are generated by the nonlinear propagation of waves in tissue at the harmonics of the frequency (usually the second harmonic) [19; 1]. Compared with fundamental imaging, HI has plenty of advantages. Such as reduced reverberations; better contrast to noise ratio; higher lateral resolution, and lower

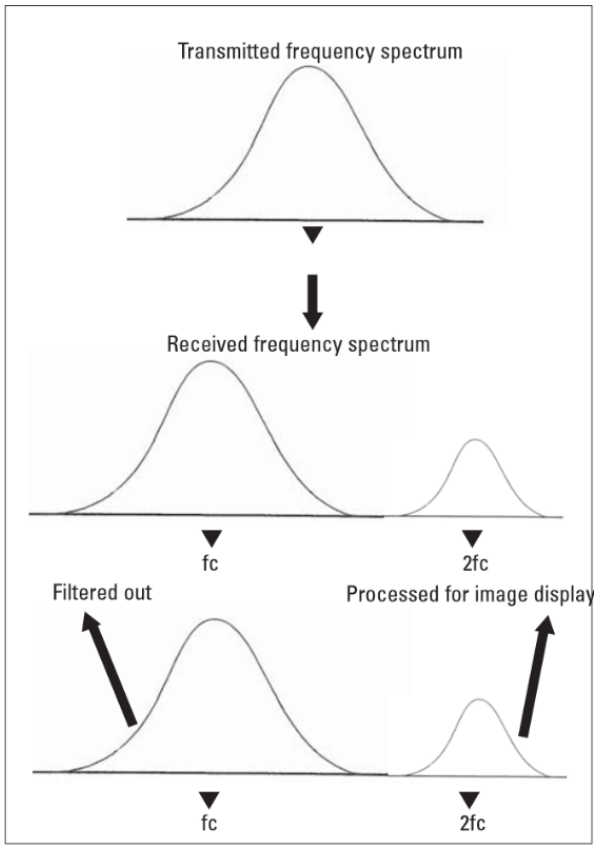


Figure 1.4: Harmonic imaging mechanism [1]

sidelobes[20; 21]. Besides, harmonics originate in the body while fundamental echoes must pass through the body twice, therefore harmonics are less subject to distortion [22; 23]. However, the harmonic power is much lower than the fundamental power, the problem of low SNR becomes more obvious. Therefore, the high transmit voltage is more necessary in HI.

1.3 PRIOR ART

In the effort to improve the quality of imaging, several contributions addressing the challenges discussed in the previous section have already been published. A HV pulser [24] which includes a HV H-bridge driver and an input stage for the signal conditioner, can provide a low HD_2 (40 dB) with a high frequency (> 10 MHz) and low power consumption (< 3.6 mW/per channel). [9] presents a HV integrated bipolar pulser which employs high-speed level shifters to achieve the -40 dB HD_2 in a transmission signal. Recently, a 64-channel transmit beamformer with programmable bipolar pulsers for catheter-based ultrasound probes is proposed [25]. However, there is some slew-rate mismatch between the rising and falling edges of the pulses. The associated second-order harmonic content of the pulse can be an issue in HI.

	This work	[9]	[25]
Process	TSMC 0.18μm HV BCD	0.5μm CMOS SOI	TSMC 0.18μm HV BCD
Supply voltage (V)	1.8	4	1.8
Max.transmit amplitude (Vpp)	30	150	60
Amplitude modulation range (V)	$2-18$	n/a	n/a
HD2 (50% Duty Cycle)(dB)	<-40	<-40	n/a
Transducer center freq. (MHz)	7.5	2.5	2.5
Pulse freq. (MHz)	5	2	9
Power (mW/ch)	<1	<50	<1

Table 1.1: Design Specifications of the pulser

1.4 OBJECTIVES

According to the findings from the analysis mentioned above, in transmit, an output signal with low HD2 and controllable amplitude should be generated. Meanwhile, low power consumption and miniaturization are important considerations as well. To alleviate the problems above and achieve the high quality of HI, for the transmit stage, two solutions are proposed:

1. For low HD2: Analyze harmonic components of trapezoidal waveforms by Fourier analysis, and explore the possibility of lower HD2 [26]. Combine feasible methods with the circuit.

2. For apodization: According to the introduction of apodization in the transducer array above, the circuit needs to establish an adjustable output voltage mechanism

Table 1.1 lists the target specification of the pulser targeted in this thesis. An initial block diagram of the entire system is shown in Figure 1.5. Similarly, the LV control signal is converted to the HV level through the pulse generator, level shifter, etc.. In addition, two new modules have been added to the transmit driver to achieve the purpose of reducing HD2 and Apodization. The block diagram shows the functions of the ASIC inside the multiple-channel pulsers and a shared transmit driver to interface with the pulser side. An initial block diagram of the entire system is shown in Figure 1.5. The block diagram shows the functions of the inside the multiple-channel pulsers and a shared bias circuit to interface with the pulser side.

1.5 THESIS ORGANIZATION

This thesis presents the steps taken to design an integrated HV pulser with improved HD2 and programmable amplitude for miniaturized ultrasound probes. The chapters are organized in chronological order, starting with

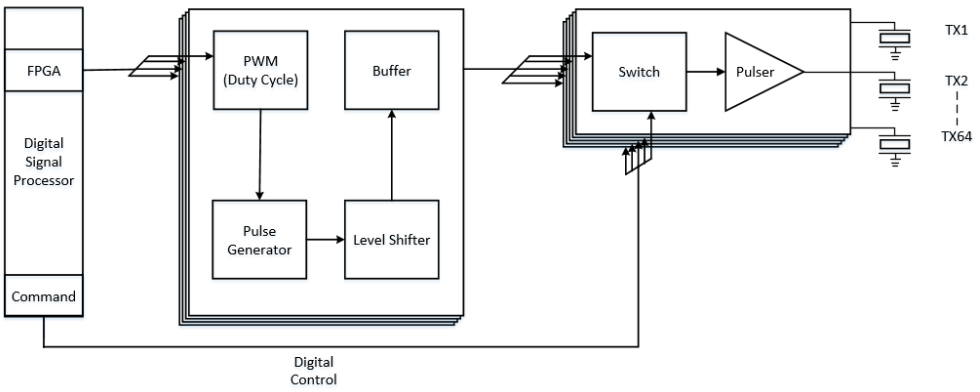


Figure 1.5: Block diagram of the entire system

the concept ideas and discussions on possible circuit topologies converging towards a good circuit implementation

Chapter 2 will discuss the architecture of the circuit from HD2 and sidelobes aspects and propose a possible solution

Chapter 3 discusses the circuit implementations to realize the architecture

Chapter 4 analyze the simulation results of the circuits

Chapter 5 explore the power consumption of the transducer in different drive modes

Chapter 6 concludes the thesis by the overall simulation results and discusses the feasibility of the final circuit and propose some future work.

2 ARCHITECTURE

In this chapter, an analysis of the HD2 of a non-ideal square wave is presented. Simulations in MATLAB show how the duty cycle and transition time of a square wave affect the HD2. Besides, a way of controlling the pulse amplitude is proposed for the apodization of a transducer array.

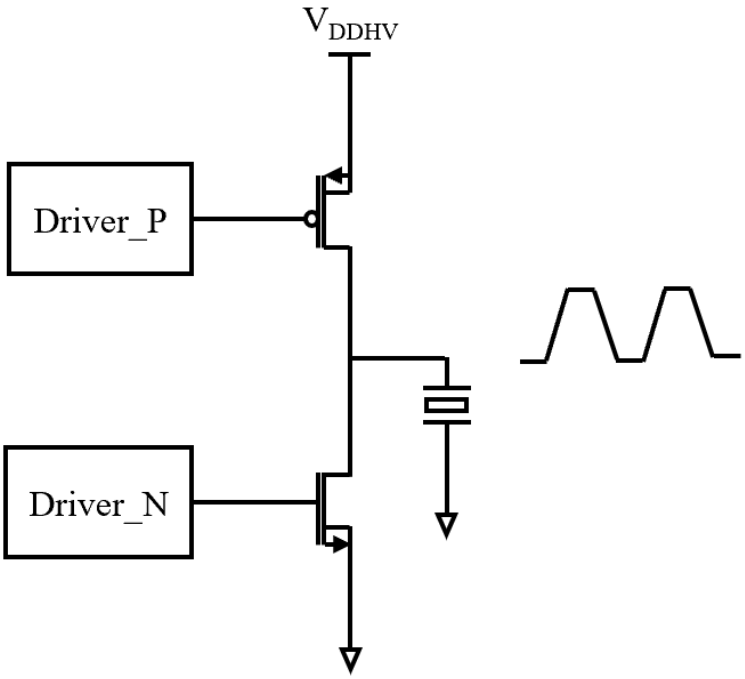


Figure 2.1: Simplified circuit diagram of a unipolar pulser

2.1 PULSER

In the typical ultrasound imaging system shown in Figure 1.3, the pulser generates proper HV pulses according to the control signals from the DSP. Figure 2.1 shows a simplified circuit diagram of a unipolar pulser. Two HV transistors are controlled by drivers to switch the transducer from V_{DDHV} to ground. The transducer can be modelled as a capacitor in parallel with a RLC branch [2] as illustrated in Figure 2.2. Normally, the capacitance will dominate the impedance of the transducer. An ideal square wave with 50% duty cycle should have no second-order harmonics. However, the non-idealities of the MOSFETs and drivers will lead to distortion of the square wave, and thus introduce HD2. In the next section, we will evaluate the HD2 of a non-ideal square wave.

2.2 HD2 OF NON-IDEAL SQUARE WAVE

2.2.1 Effect of Duty Cycle

Figure 2.3 shows an ideal continuous square wave with infinitely-fast rising and falling edges. It has an amplitude of A, a period of T, an on-time of T_{on} and an off-time of T_{off}. This waveform can be expressed in a Fourier series:

$$f(t) = C_0 + \sum_{n=1}^{\infty} C_n \cos(n\omega_0 t) \tag{2.1}$$

$$C_n = \frac{1}{T}\int_{t_0}^{t_0+T} f(t)e^{-jn\omega_0 t}dt \tag{2.2}$$

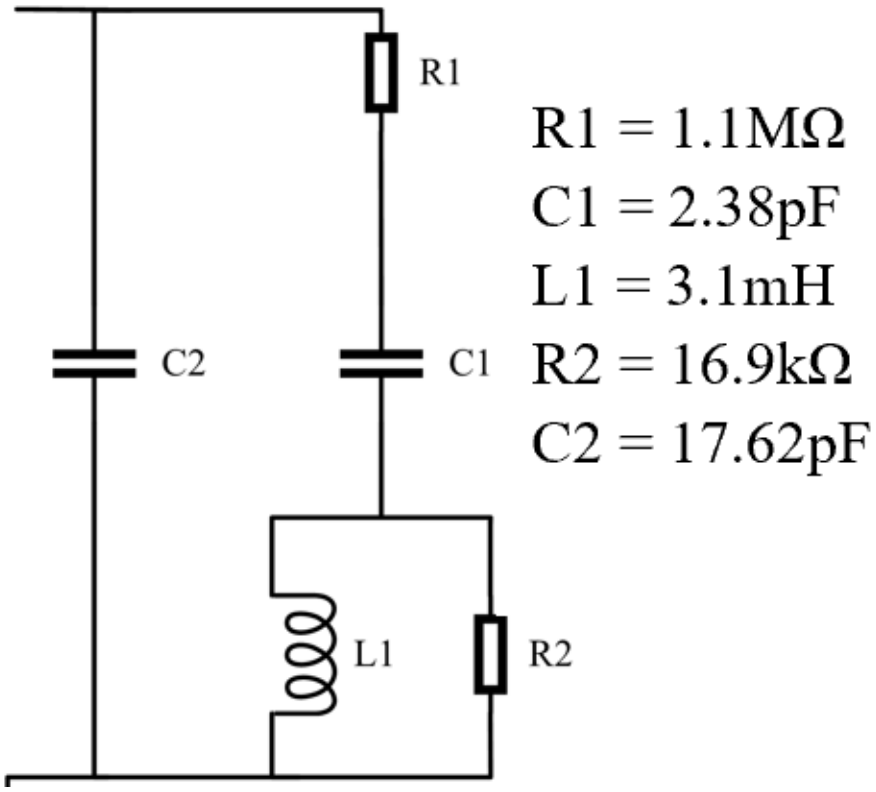


Figure 2.2: Transistor model [2]

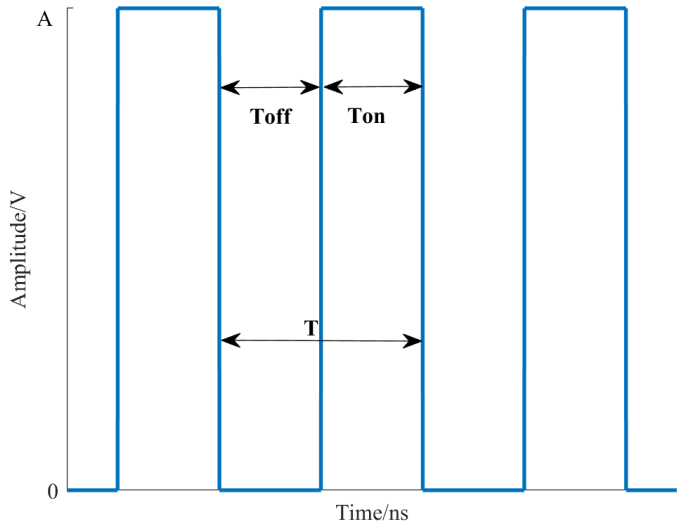


Figure 2.3: A square wave with infinite rising and falling edges

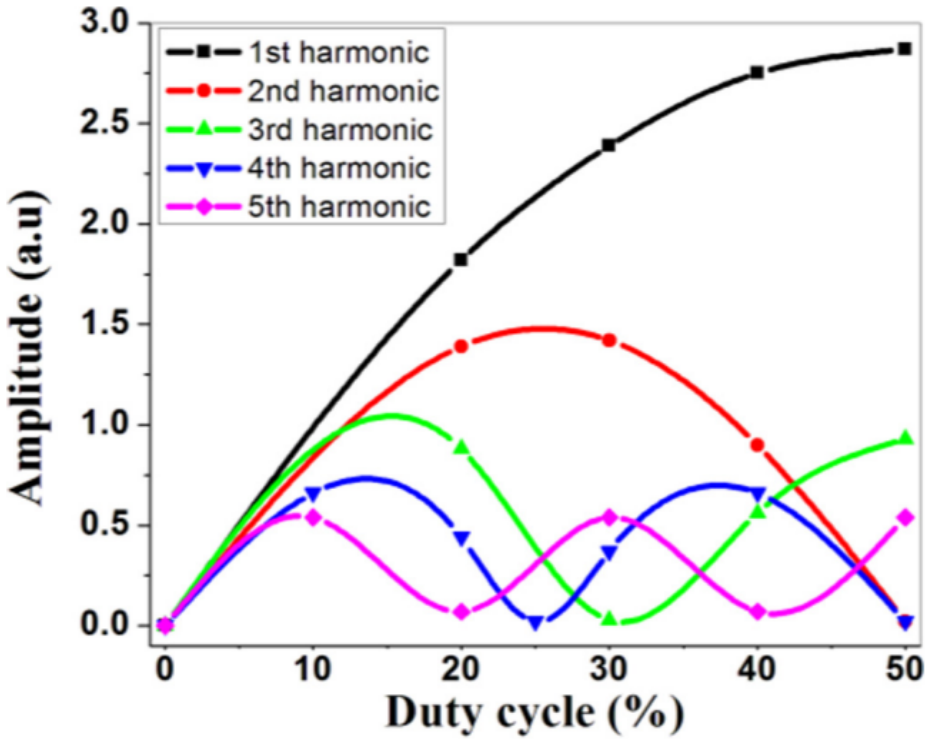


Figure 2.4: Harmonic content of square wave with different duty cycle [3]

$$C_0 = \mathrm{A}\frac{\mathrm{T_{on}}}{T} \tag{2.3}$$

$$C_n = \frac{2A}{n\pi}\sin\left(\frac{n\pi T_{on}}{T}\right) = 2\mathrm{A}\frac{T_{on}}{T}\left|\frac{\sin\left(\frac{n\pi T_{on}}{T}\right)}{\frac{n\pi T_{on}}{T}}\right| \tag{2.4}$$

where C_n is the amplitude of the harmonics and C_0 is the amplitude of the first-order harmonics. In order to minimize the HD2, C_2 should be as small as possible for even n. Equation 2.4 shows that the minimum value of C_n will be obtained when the duty cycle is 50%, that is ,

$$T_{on} = T_{off} = \frac{1}{2}T \tag{2.5}$$

Ideally, Equation 2.4 is equal to zero for even n orders if $T_{on} = T/2$. According to that, the goal of reducing the HD2 can be achieved by tweaking the duty cycle of output waveforms which means adjusting the operation time of pulser.

Figure 2.4 shows the harmonic content of the square wave with different duty cycles. The difference between the 1st and 2nd harmonic represents the HD2 in the simulation, which is similar to the derived result [3]. If the propagation delay from the pull-up and pull-down paths are equal, the duty cycle can be fixed to 50% when the control signals on both sides have a half-period phase delay.

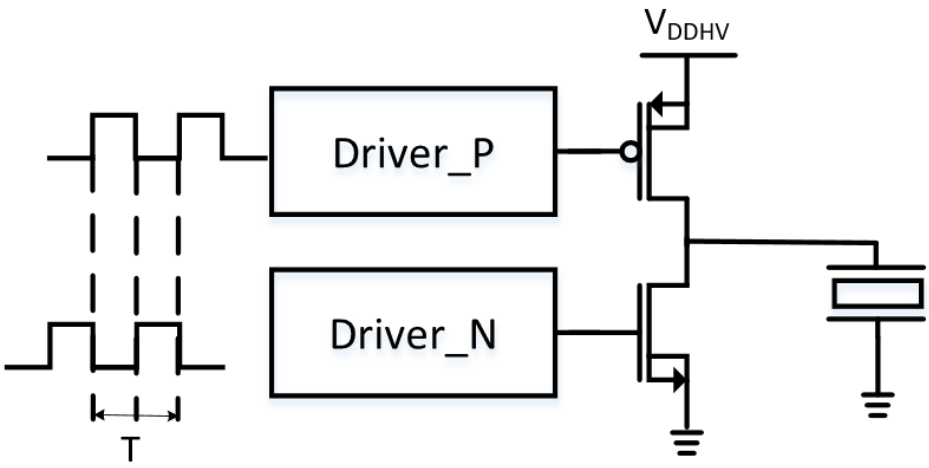


Figure 2.5: Balanced duty cycle control of pulser

Figure 2.6 shows a square wave with finite rise and fall time, T_r and T_f. The on-time T_{on} and off-time T_{off} are defined by the time difference between the mid-point of the pulse edges. C_0 can be derived as [24]:

$$C_0 = \frac{AT_{on}}{T} - \frac{A}{2} \tag{2.6}$$

If $T_r = T_f$, the magnitudes of the Fourier coefficients, C_n ($n \geq 1$), is given by:

$$C_n = 2\frac{AT_{on}}{T}\left|\frac{\sin\left(\frac{n\pi T_r}{T}\right)}{\frac{n\pi T_r}{T}}\right|\left|\frac{\sin\left(\frac{n\pi T_{on}}{T}\right)}{\frac{n\pi T_{on}}{T}}\right| \tag{2.7}$$

Similar to Equation 2.4, the harmonic energy at amplitude of even-order frequencies harmonics is still zero in theory when the duty cycle is 50%, while the rising edge or falling edge will also affect the harmonic energy. Figure 2.7 shows simulated HD2 vesus the duty cycle for a symmetrical trapezoidal when with a 10ns rise time (period is 300ns). The HD2 is minimum when the duty cycle is 50% while it starts to increase with the increase or the decrease of the duty cycle. To show how the HD2 is affected by the rise and fall time, Fourier analysis of a periodical trapezoidal waveform with a $30V_{PP}$ amplitude and 300ns period is done in the MATLAB. The HD2 of the trapezoidal signals with different normalized transition time when the duty cycle is equal to 50% is plotted in Figure 2.8, where the transition time T_r and T_f is equal to maintain the 50% duty cycle.

2.2.2 Effective of Slew-Rate Mismatch

The transducer, which can be seen as a capacitor, will be charged by the slewing current through the pulser. The slewing current is proportional to the capacitor and the slew rate,

$$\mathrm{SR} = \left|\frac{dv_{\mathrm{out}}(t)}{dt}\right| \tag{2.8}$$

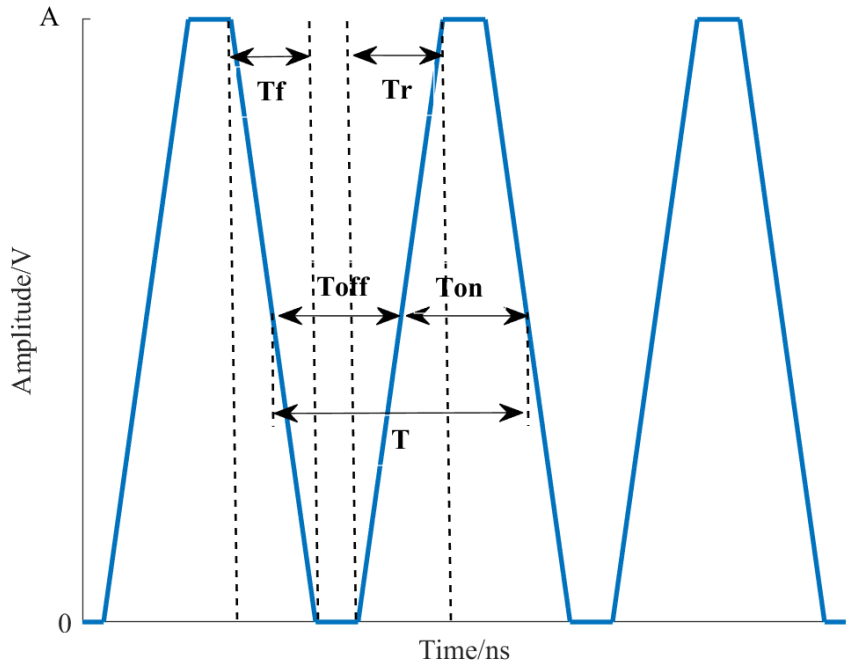


Figure 2.6: Square wave with finite rising and falling edges

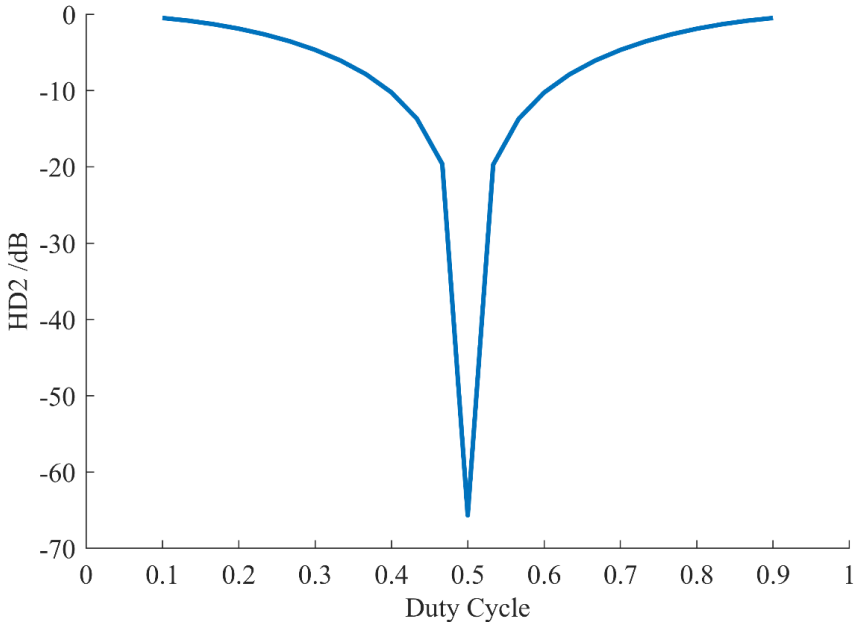


Figure 2.7: HD2 of the ideal trapezoidal wave with different duty cycles

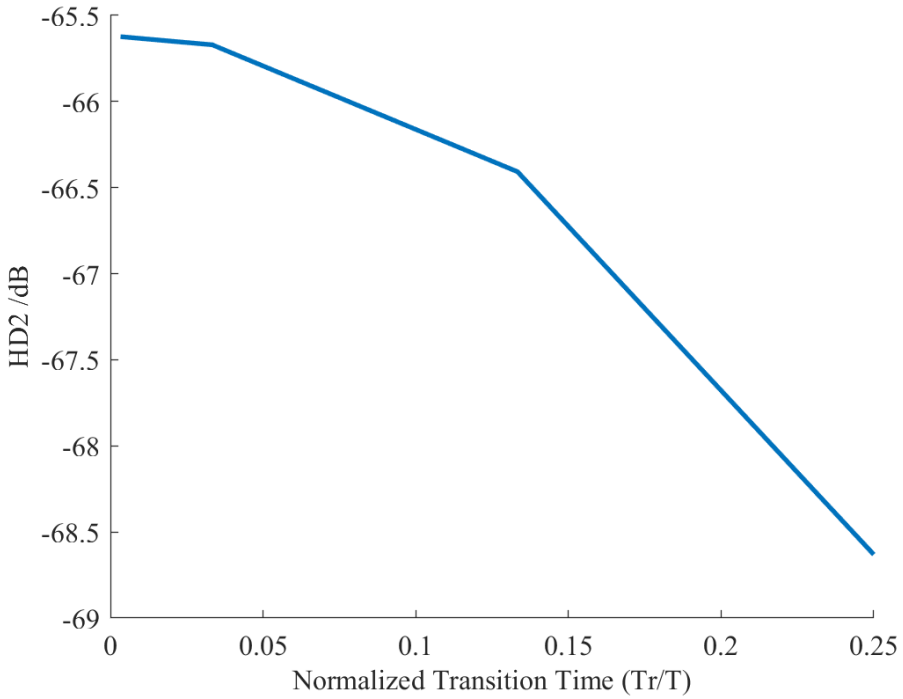


Figure 2.8: HD2 of the ideal trapezoidal wave with different transition time

$$I_{SR} = C\frac{dV}{dt} \tag{2.9}$$

In the actual pulser, the pull-up and pull-down transistors cannot provide exactly the same current to the transducer during the slewing, which will introduce the slew-rate mismatch between T_r and T_f. It can be defined in Equation 2.10.

$$\text{SRMismatch} = \frac{|T_r - T_f|}{T_f} \times 100\% \tag{2.10}$$

The slew-rate mismatch will produce non-zero harmonic energy at even harmonic frequencies of output signals. Figure 2.6 shows that the mid-point of the pulse edges is used to define the duty cycle. Hence, if there is a mismatch between the rising and falling edge, the actual duty cycle will be shifted from 50%. Since the HD2 is very sensitive to the duty cycle, it will also be affected by the slew-rate mismatch. Figure 2.9 demonstrates how the HD2 changes with the slew-rate mismatch.

To balance the currents, one way is to adjust the overdrive voltage of each transistor in the pulser as shown in Equation 2.11,

$$I_{D(sat)} = \frac{\mu \cdot C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tag{2.11}$$

where, V_T is the threshold voltage of the transistor. The Overdrive Voltage (V_{OV}) is,

$$V_{OV} = V_{GS} - V_T \tag{2.12}$$

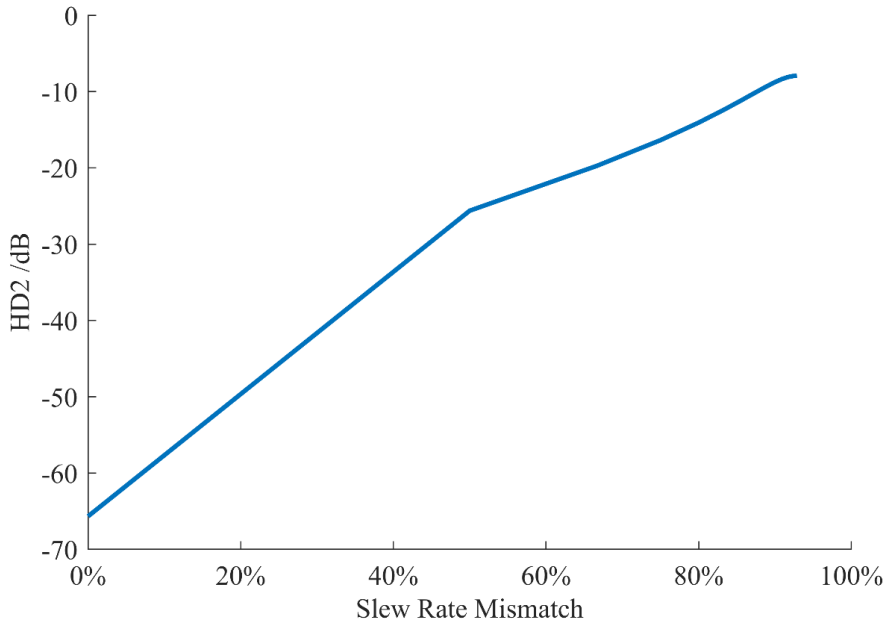


Figure 2.9: HD2 of the ideal trapezoidal wave with different relative slew-rate mismatch

Because multichannel pulsers connect to the shared driver, the slewing current on both sides should be automatically calibrated. Otherwise, each channel needs to be trimmed separately. A replica pulser structure is proposed in Figure 2.10, where the output is clamped at the mid-supply reference voltage (V_{REF}). Therefore, both M1 and M2 in replica pulser work in the saturation region with a similar operating point. Driver_N provides the overdrive for M1 to generate a certain drain current I_{DN}. The overdrive voltage of M2 can be adjusted by the negative feedback loop to get an identical drain current I_{DP} with I_{DN}. Then, apply the same overdrive voltage to the main pulsers, more balanced slewing currents can be obtained, which means the SRMismatch is extremely reduced and the HD2 is much lower.

In conclusion, to generate a better output waveform with lower HD2, the duty cycle is the key factor. Therefore, in the circuit, the turn-on and turn-off time of the pulse should be accurately controlled by the clock signal. Meanwhile, the pull-up and pull-down currents flowing through the transducer should be as equal as possible.

2.3 APODIZATION

When a 1D or 2D transducer array is driven by pulsers with the same excitation amplitude, a rectangular aperture is generated. [8] shows that a sidelobe level of -13 dB down from the main lobe appears in the transmit beam. False echos can appear in the image because of the sidelobes in the rectangular aperture. A way of reducing the sidelobes is to apodize the transmit beam, which can be done by varying the excitation amplitude across the array. Considering that the transducer element can be seen as a bandpass

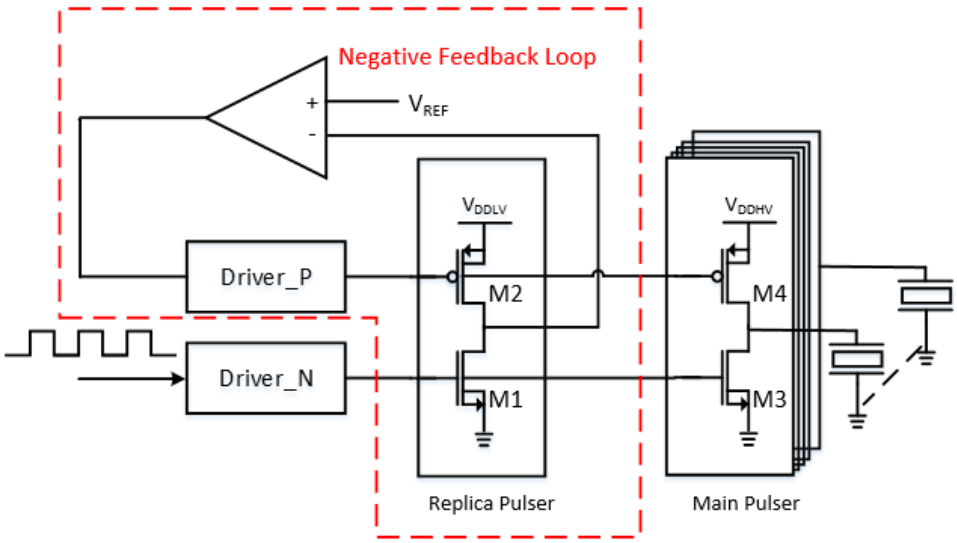


Figure 2.10: Block diagram of automatic calibration replica pulser

filter, the excitation amplitude can be tuned by changing the pulse width or slew rate of the pulses applied to the transducer.

2.3.1 Pulse Width Modulation

The last part of Equation 2.7 illustrates that the amplitude reaches its peak value when the duty cycle is equal to 50%. As shown in Figure 2.11, the amplitude of the fundamental with different duty cycles is simulated when the output swing is 30 V_{PP} and the slew rate is 3 GV/s. However, because the timing logic frequency that generates the switch control signals cannot be infinite, the time resolution of the PWM cannot infinitely small. Therefore, it is difficult to obtain an accurate amplitude modulation

2.3.2 Slew Rate Modulation

To get a better amplitude control accuracy a fine-adjustment method should be considered on top of the coarse-adjustment implemented by the PWM. Equation 2.7 shows that when the duty cycle is 50%, the amplitude increases as the transition time become shorter, which is the same with the simulation results shown in Figure 2.12. From Figure 2.12, the total variation range of fundamental frequency amplitude is roughly equal to 4 V (28% of the amplitude variation by PWM) when the normalized transition time on both sides changes from 0.01 to 0.35 ns, where the normalized transition time is defined as (T_r/T). This method can be regarded as the SRM because the slew rate is inversely proportional to transition time. Compared to the range shown in Figure 2.11, the adjustment range is more than 3 times lower than PWM although it still presents a non-linear relationship.

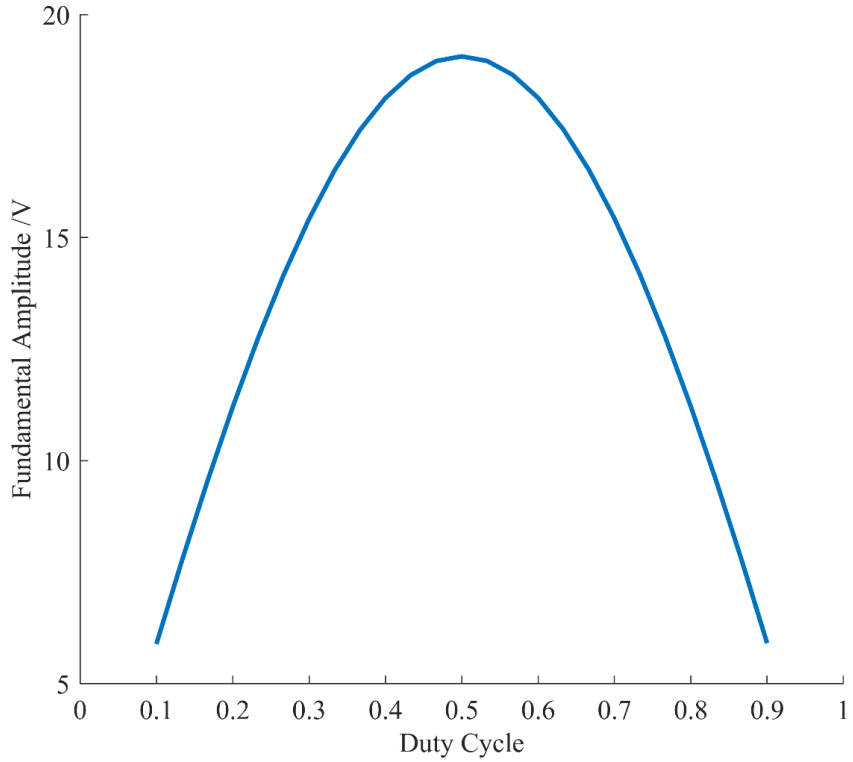


Figure 2.11: Fundamental Frequency Amplitude of ideal 30V trapezoidal wave with different duty cycles

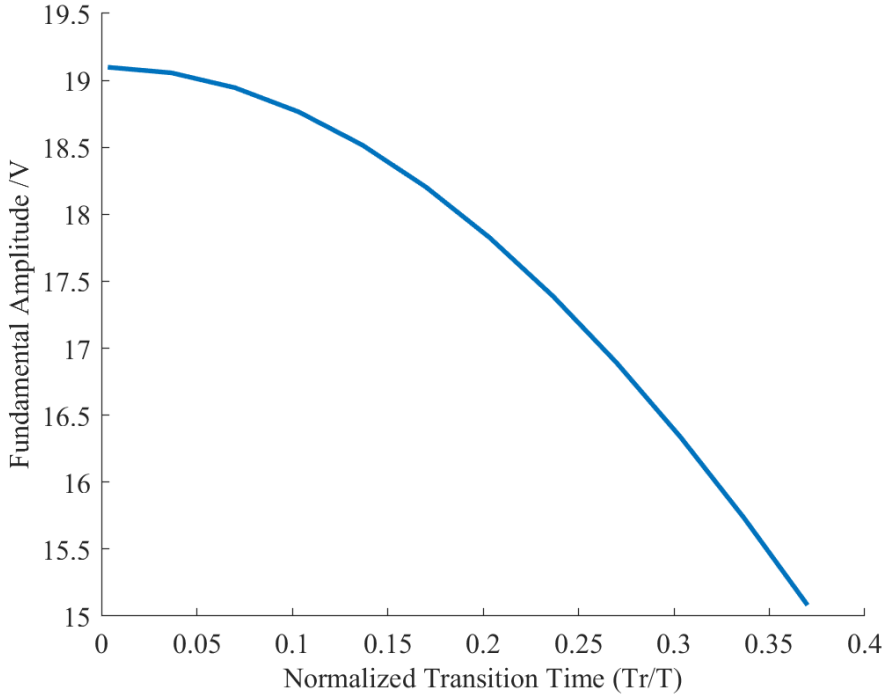


Figure 2.12: Fundamental Frequency Amplitude of ideal 30V trapezoidal wave with different duty cycles

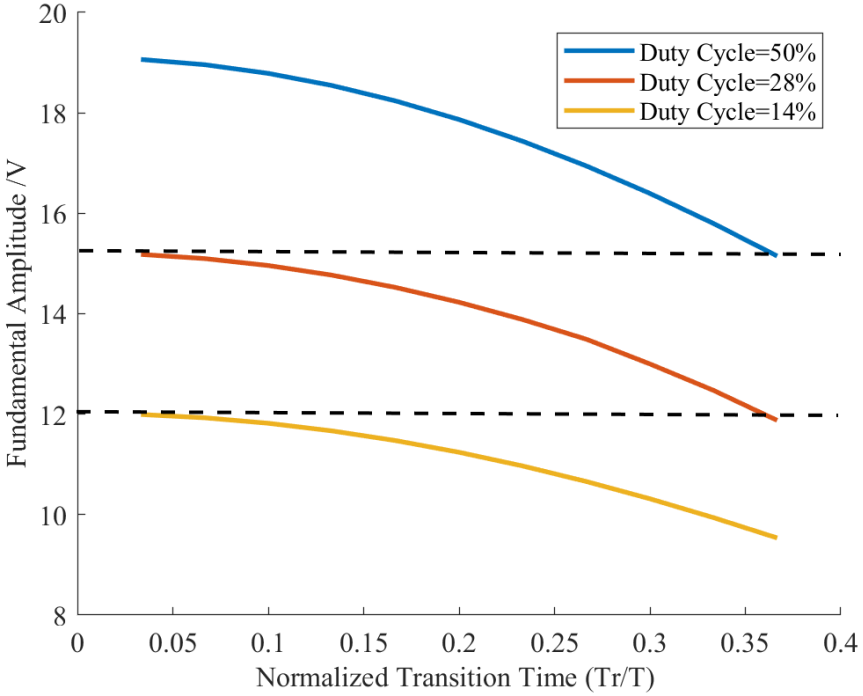


Figure 2.13: Combined graph

2.3.3 Combination of PWM and SRM

Combine SRM with PWM, a more accurate control of the pulse amplitude in the fundamental frequency can be obtained with a large enough range, as shown in Figure 2.13.

Different elements in a transducer array should get different amplitudes to realize Apodization. Therefore, pulse-width and slew-rate programming should be able to employ for every pulser. A timer circuit can control the PWM with finite time resolution by generating the LV pulses to the transmit drivers. Moreover, the slew rate, which can be controlled by the replica circuit, is identical in all main pulsers because the replica circuit is a shared block. Therefore, the SRM for individual pulser can not be achieved. An alternative method for this problem is to build multiple bias circuits, each provides different slewing currents and uses switches to select which slew rates should be connected to each pulser.

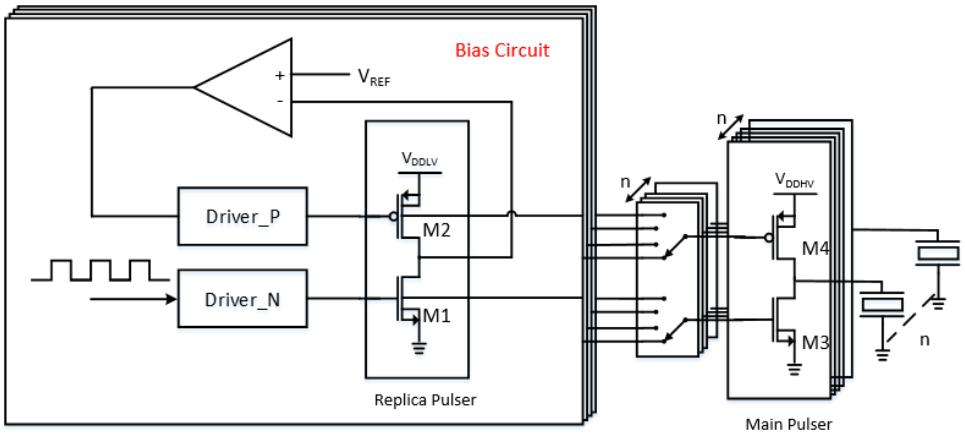


Figure 2.14: Multiple bias circuit with different slewing currents of the pulser

3 CIRCUIT DESIGN

This chapter discusses the circuit implementation and component sizing of the functional blocks of the ASIC. First, the design of the main pulser and replica pulser is presented. Next, the level shifter structure for the pull-up path of the pulser is discussed. Then, the loop stability of the loop amplifier in the replica pulser and the dimensioning of loop amplifier are discussed. Finally, the buffers and switches for driving multiple channel pulsers are presented.

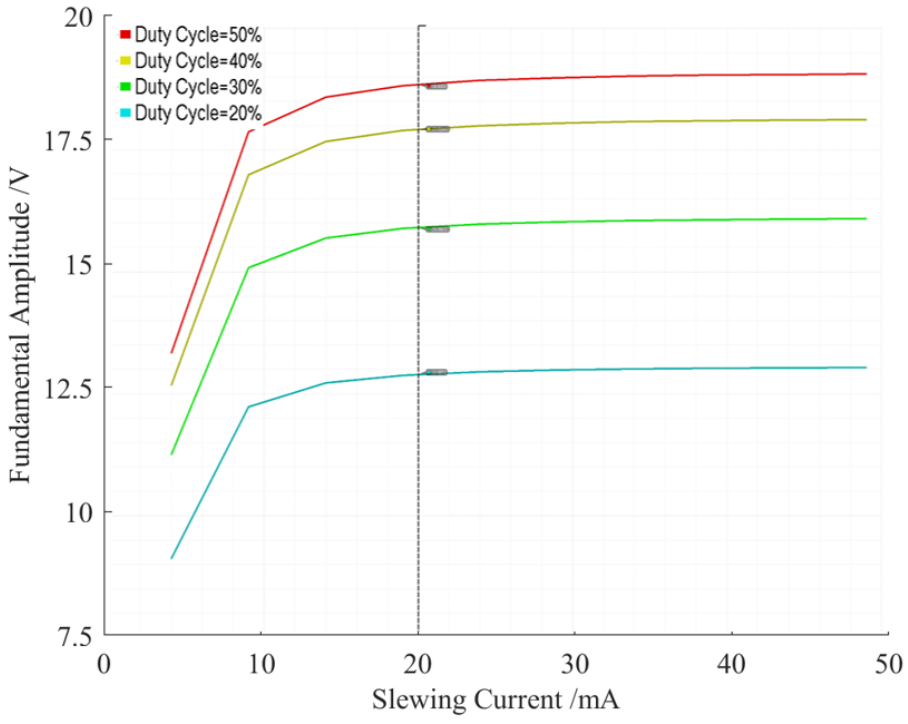


Figure 3.1: Fundamental frequency amplitude of non-ideal trapezoidal wave with different slewing current and duty cycles

3.1 PULSER DIMENSIONING

3.1.1 Range of the slewing current

Two goals of the ASIC, low HD2 and apodization, are both related to the slewing current of the main pulser. For HD2, the slewing current should be perfectly matched. For apodization, the slewing current should be adjustable within the tolerance range of the main pulser. Therefore, to determine the size of pulser, the first thing is to acquire a reasonable current range. In Chapter 2, the influence of the slewing current and duty cycle on the fundamental frequency amplitude in an ideal trapezoidal wave has been discussed. To determine the size of a transistor, the Drain Current (I_D) is an important parameter. As shown in Figure 2.12, the fundamental frequency amplitude increases as the normalized transition time decreases and then saturates when the normalized transition time is smaller than 0.06. The transducer shown in Figure 2.2 can be regarded as a 18 pF capacitor initially. Therefore, the maximum slewing current of a pulse wave with a 30 V_{PP} is around 20 mA. As shown in Figure 3.1 four curves that represent different duty cycles changing from 50% to 20% share the same trend. Hence, the slewing current range is chosen from 5 mA to 20 mA.

3.1.2 Range of Bias Current

The maximum Gate-Source Voltage (V_{GS}) of the HV transistors in 0.18 µm HV BCD technology is 5.5 V. The size of the transistor can be determined

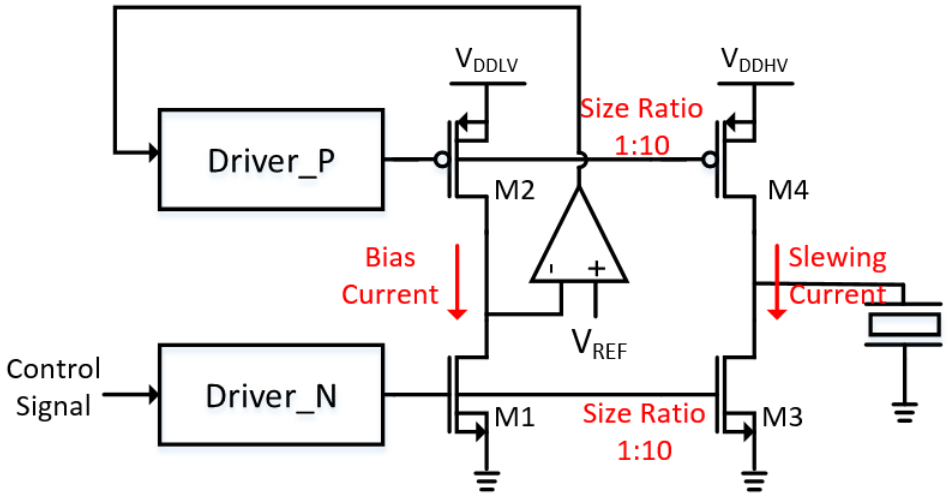


Figure 3.2: Size ratio of replica and main pulser

by Equation 2.11 where considering the maximum required slewing current (20 mA) and maximum allowed gate oxide breakdown voltage (5.5 V).

In Chapter 2, a replica pulser has been introduced to control the gate voltage of the PMOS and NMOS to balance their slewing current. To reduce the power consumption of the replica pulser, the bias current through the replica pulser can be a fraction of the slewing current at the output of main pulser if the size of the replica pulser is scaled down proportionally as well. In Figure 3.2, the size scale ratio is set to be 10. Corresponding to the slewing current, the bias current should range from 0.5 mA to 2 mA.

As mentioned in Chapter 2, the supply voltage of the main pulser should be 30 V because the output swing is from 0 V to 30 V. In addition to the proportional reduction in current, the transmit driver can also operate in a LV domain to further reduce power consumption. But if it is so low that cannot provide enough margin of Drain-Source Voltage (V_{DS}) in replica pulser, M1 and M2 will go into triode region which affects the whole loop gain. Therefore, the supply voltage at the transmit driver is 7 V, as shown in Figure 3.2. The LV supply could be further reduced to further reduce power consumption.

3.1.3 Control signal of Driver_N

In the replica pulser, the feedback network generates an appropriate overdrive voltage for M2 corresponding to I_{DN} flowing through M1. If the gate of M1 is directly driven by a voltage source, the uncertainty of the threshold voltage will introduce errors in the slewing current. Therefore, a current mirror with a reference current source is necessary to make the current insensitive to the threshold voltage which is shown in Figure 3.3. In addition, because the voltage at the output of the main pulser changes dynamically, it is impossible to keep V_{DS3} and V_{DS4} equal, which means there would be some errors caused by the channel length modulation effect. However, be-

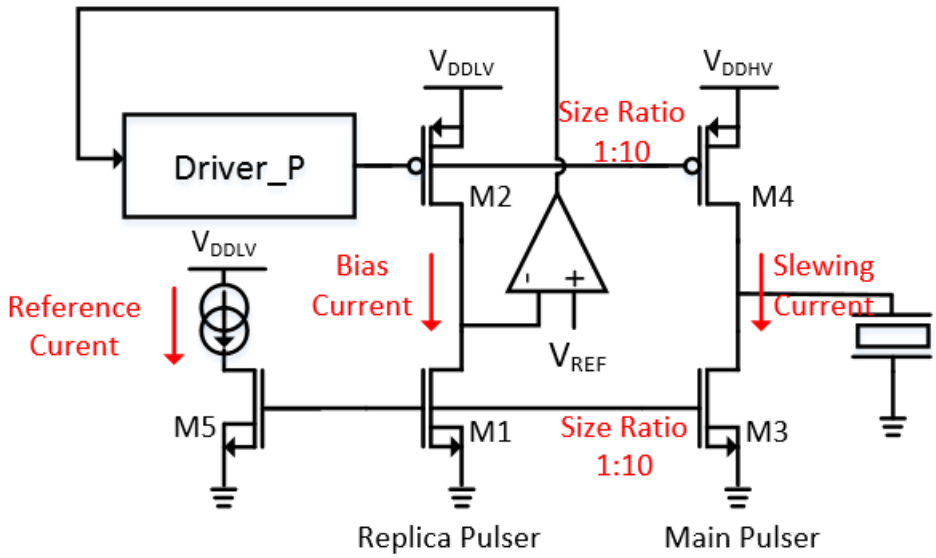


Figure 3.3: Current mirror to bias the replica and main pulser

cause the HV transistor is adopted and its length is longer than LV transistors, the error caused by this effect is acceptable.

3.1.4 Design of Pulser

The previous section introduces several requirements for dimensioning of the pulser. In this section, the specific transistor size will be determined through simulation.

In order to reduce the side effect caused by channel length modulation, the length of transistors in the main pulser is set to $1.5\mu m$. Initially, the width of M3 can be set to $100\mu m$, $150\mu m$ and $200\mu m$. Figure 3.4 shows the linearity of the current multiplication of M3 when the reference current changes from 0.5 mA to 2 mA. In Figure 3.5, a similar simulation has been done between the reference current and bias current, where the size of replica pulser is 10 times lower than the main pulser. Obviously, when the reference current increase above 1.5 mA, the linearity of red line, which represents the W/L of $10\mu/1.5\mu$, is worse than the other two lines. This problem can be explained that when the size of M1 is too small and the bias current is relatively large, V_{GS} goes up. If V_{GS} continues to increase, M1 will go into triode region. In this case, the operating point in the replica pulser and the main pulser becomes different. Figure 3.6 demonstrates the analysis above, the red line represents the smallest size of M1, its V_{GS} at the maximum bias current is around 4.66 V and the threshold voltage is 1.04 V. V_{OV} is 3.6 V which is a bit larger than V_{DS} of M1. In order to minimize the die size, the size of M3 is chosen to be $150\mu/1.5\mu$ and M1 is set to $15\mu/1.5\mu$.

Because the mobility in PMOS is lower than NMOS, the size of PMOS should be larger than NMOS. Normally, the factor is range from 2 3. Based on the size of M3, the size of M4 is initially assumed as $350\mu/1.5\mu$, $400\mu/1.5\mu$ and $450\mu/1.5\mu$.

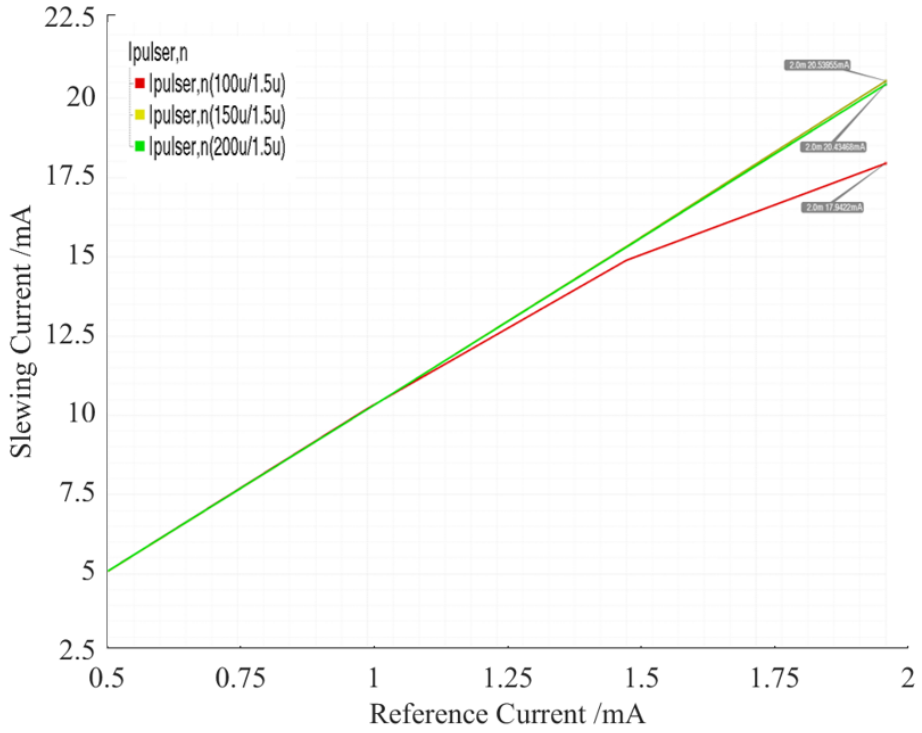


Figure 3.4: The linearity of the slewing current with different size of M3

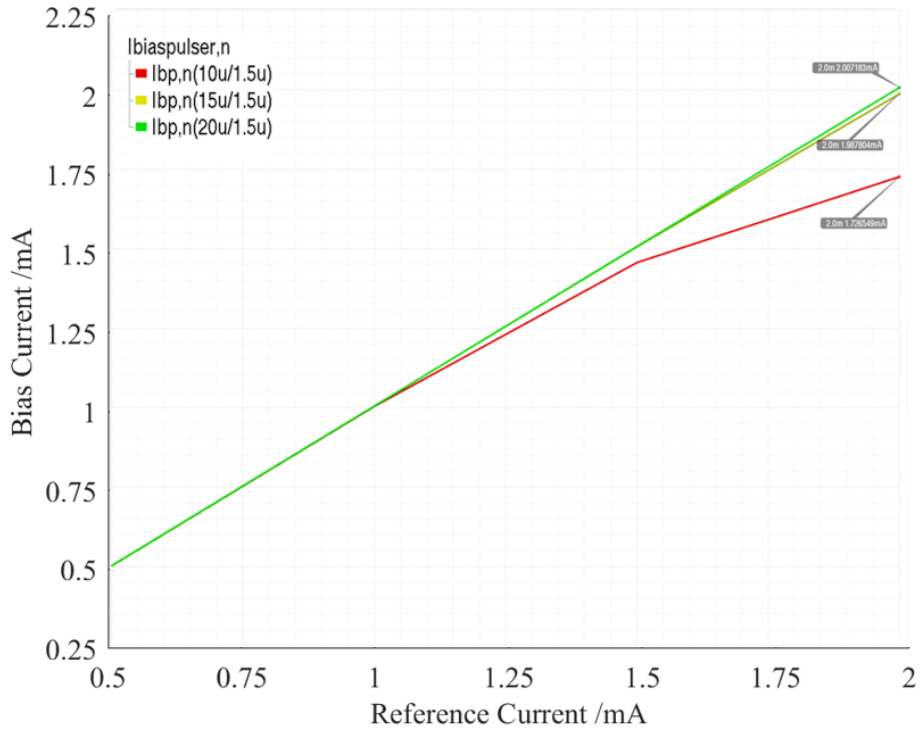


Figure 3.5: The linearity of the bias current with different size of M1

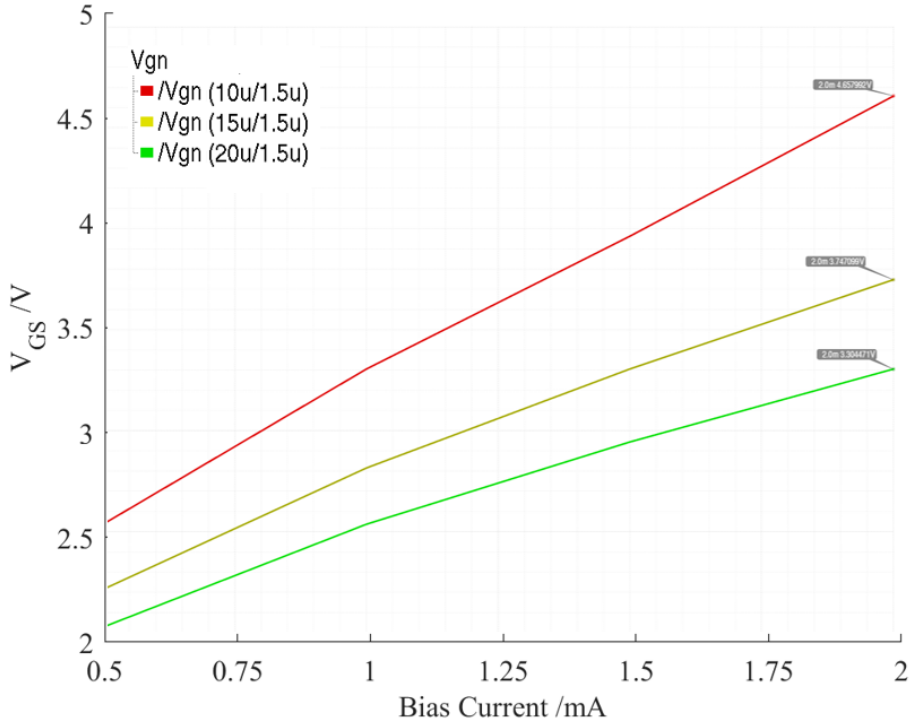


Figure 3.6: The relationship between V_{GS} of M1 and bias current in replica pulser under different size conditions

Use the same method to determine the size of M2 and M4. All cases have good linearity of as shown in Figure 3.7 and Figure 3.8. To check whether the M2 works in the saturation region or not, Figure 3.9 shows the relationship between V_{SG} of M2 and bias current in replica pulser under different size conditions. Similar to Figure 3.6, M2 stays at the edge of the saturation under the size of $35\mu/1.5\mu$. Finally, the size of M2 and M4 is $40\mu/1.5\mu$ and $400\mu/1.5\mu$ respectively.

3.1.5 For Pull-Up Side

Since the source of the M4 is tied to 30 V, its gate voltage must be shifted up to at least 24.5 V to ensure that V_{SG} is within a safe range. Therefore, it is necessary to add a level shifter to transfer from the LV domain to the HV domain.

Three common level shifter circuits are illustrated in Figure 3.10 [27]. Figure 3.10a occupies the smallest area, but there will be static power dissipation. The main advantage of Figure 3.10b and Figure 3.10c is the reduced or eliminated static power dissipation with minimal sacrifice in terms of speed. However, They need two inputs which means they can not transfer the V_{OV} of M2 accurately to M4. Therefore, Figure 3.10a is chosen as the level shifter architecture. Figure 3.11 shows the level shifter used in the pulser based Figure 3.10a. Trade-offs between speed and power consumption can be found in the level shifter structure shown in Figure 3.11. To maximize the speed, R1 and R2 should be small, whereas the total resistance in the level shift

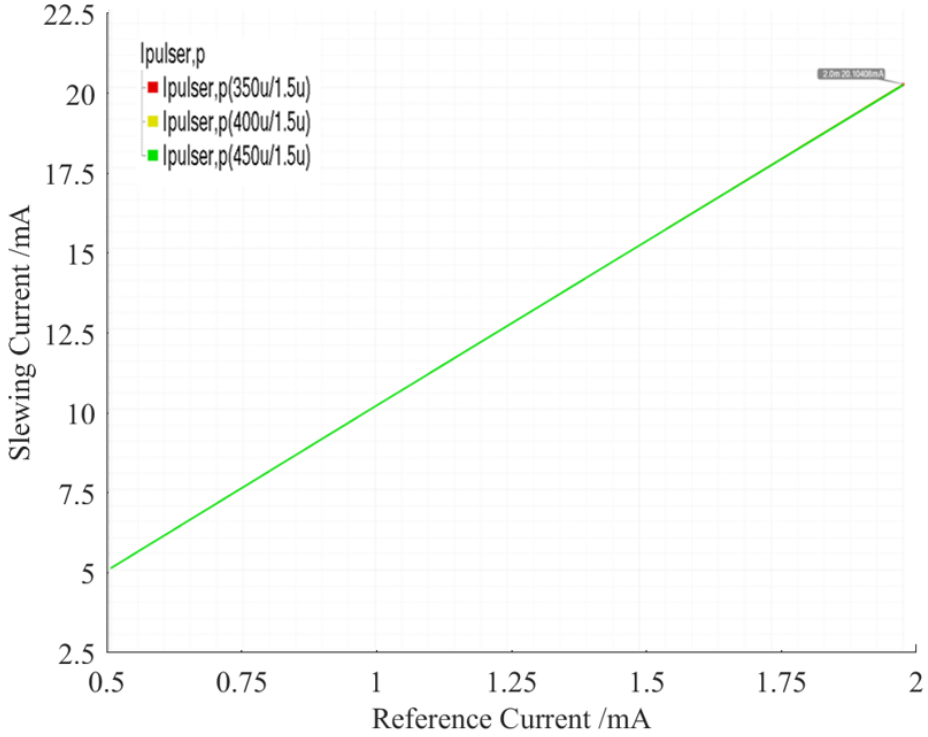


Figure 3.7: The linearity of the slewing current with different size of M4

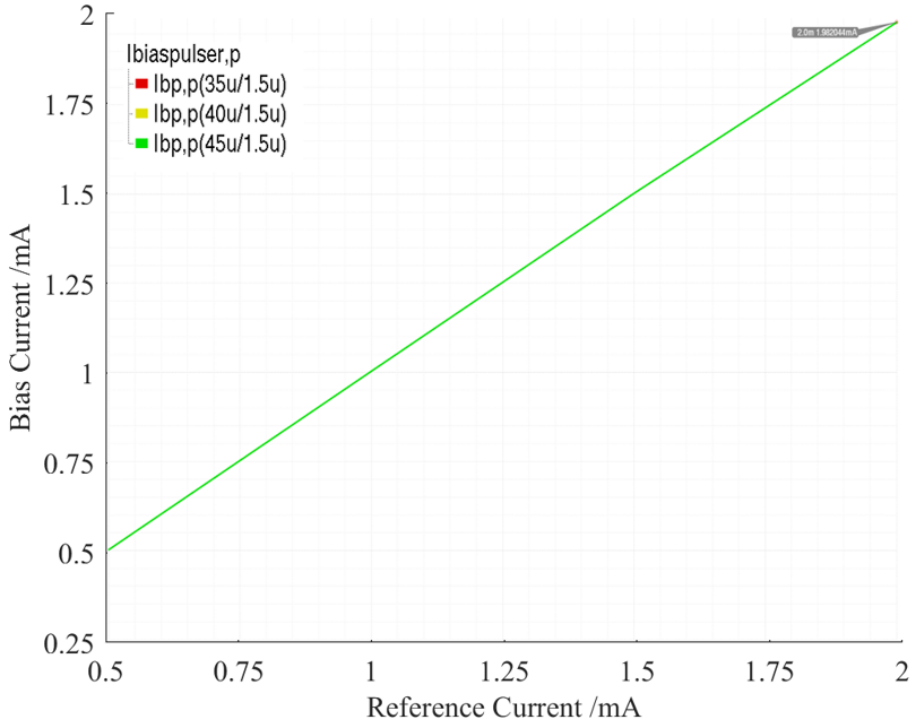


Figure 3.8: The linearity of the bias current with different size of M2

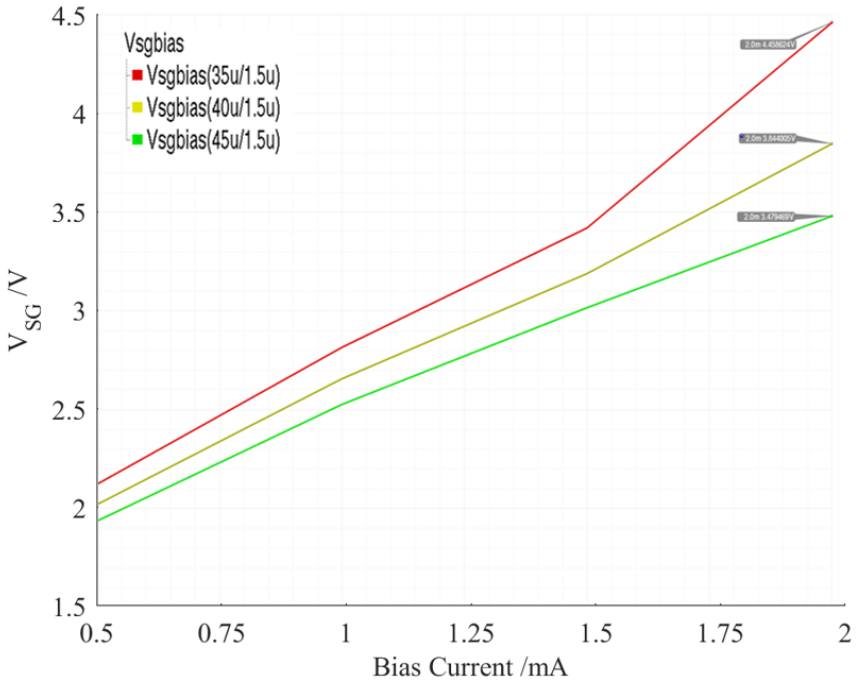


Figure 3.9: The relationship between VSG of M2 and bias current in replica pulser under different size conditions

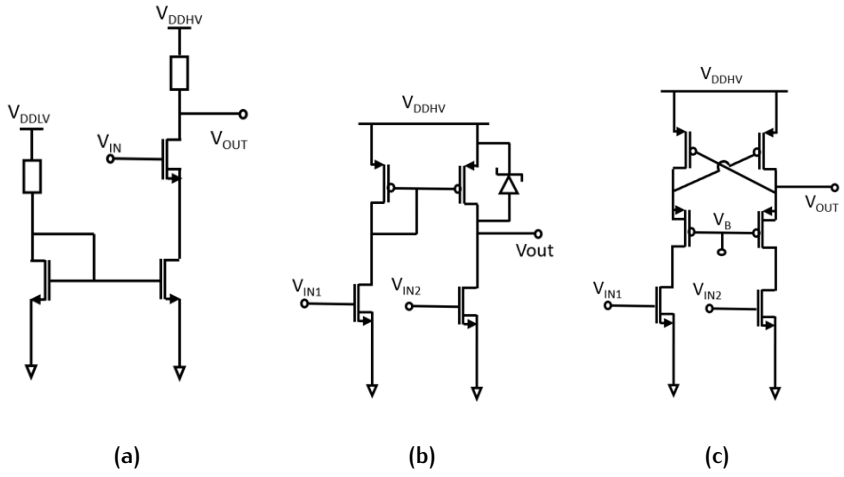


Figure 3.10: Three common level shifter structures

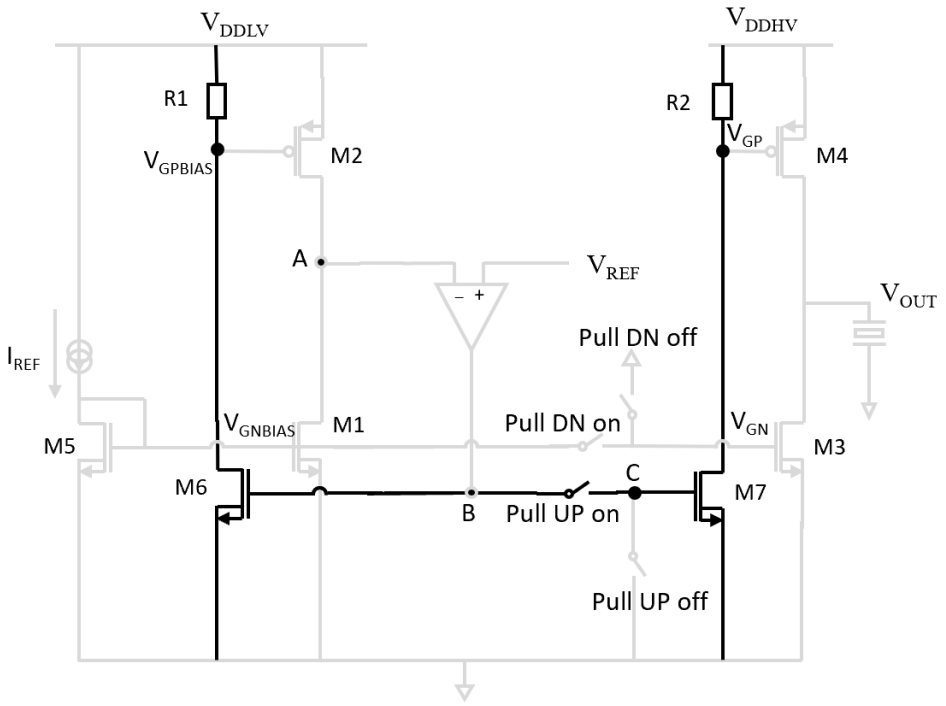


Figure 3.11: Improved level shifter with less static power consumption based on Figure 3.10a

branch should be large enough to decrease the power consumption. The power dissipated by main pulser can be calculated based on Equation 3.1 .

$$P = CV^2fN \tag{3.1}$$

where C is the load capacitance (17.62 pF), V is the peak-peak output voltage (30 V), f is PRF (3.3 MHz) and N is the number of transmission pulses during one complete transmit phase. When N is equal to 1, the power consumption of the main pulser is 54 mW. Therefore, to avoid the DC power consumption of the entire replica pulser exceeding the main pulser, the current through level shifter brunch should be smaller than 1.7 mA, where the maximum V_{GS} is 3.4 V. Hence, R1 should be larger than 2 $k\Omega$.

As bias current changes, the voltage at node B will swing up and down. To keep M6 and loop amplifier work in saturation region, voltage of node B should be low but at least higher than V_{GS6}. Therefore, the size of M6 is $20\mu/1.5\mu$. According to Figure 3.12, when R1 is equal to 1 $k\Omega$, though it has the smallest time delay, the V_{SG} is around 6 V which exceeds the tolerance voltage of 5.5 V. There is a dip in the rising edge as shown in Figure 3.12, which is because the voltage B needs time to settle when the switch turns on.

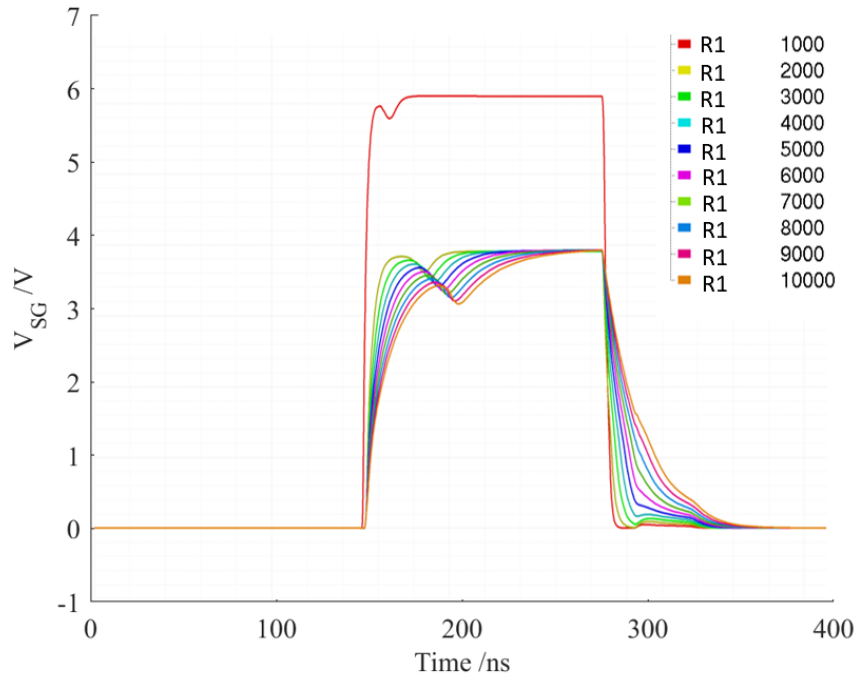


Figure 3.12: Settling performance at V_{SG} of PMOS with different values of R1

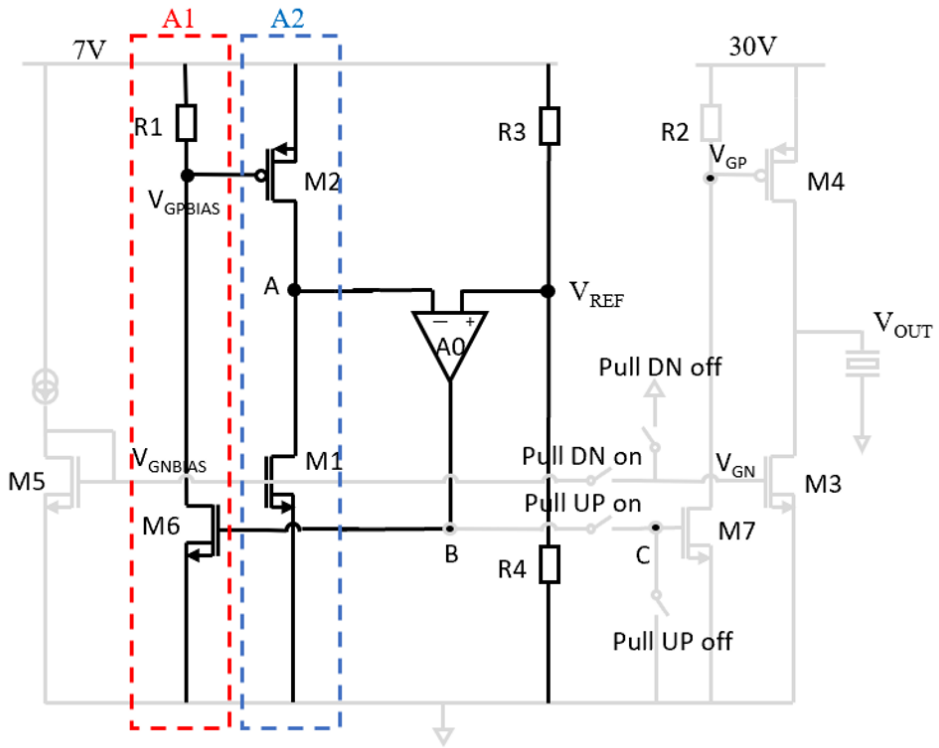


Figure 3.13: Negative feedback loop in replica pulser

3.2 LOOP STABILITY ANALYSIS AND AMPLIFIER SPECIFICATION

The reference voltage is provided by the voltage divider, here R3 is equal to R4. Before discussing the specific parameters of the amplifier in that loop, it is necessary to analyze the stability of this feedback. The bold part in Figure 3.13 represents the feedback loop in the replica pulser. There are three stages $A0$, $A1$ and $A2$ involved in the feedback loop, each of which introduces a pole at node B, node V_{GPBIAS} and node A respectively. Compared with node V_{GPBIAS}, poles at node A and B are located at relatively low frequency because of their high impedance and large load capacitor, that affects the stability of the negative feedback loop. Moreover, the transconductance and output impedance of a single transistor can be represented in Equation 3.2 and Equation 3.3 respectively.

$$g_m = \sqrt{2\mu_n C_{ox}(W/L)I_D\,(1+\lambda V_{DS})} \tag{3.2}$$

$$r_O = \frac{1}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}\,(V_{GS}-V_{TH})^2\cdot\lambda} \approx \frac{1}{\lambda I_D} \tag{3.3}$$

Hence the intrinsic gain of a single transistor is given by Equation 3.4.

$$A = g_m r_0 \approx \sqrt{2\mu_n C_{ox} WL\frac{1}{I_D}} \tag{3.4}$$

The intrinsic gain will increase as I_D decreases. To make the error between node A and the reference voltage of less than 1%, the total loop gain should be greater than 40 dB. Moreover, as mentioned in Chapter 1, duty-cycling of the entire transmit/receive phase can effectively reduce the power consumption of the system. To minimize the time window in which the transmit circuitry has to be active, the start-up time should be as small as possible. A start-up time of less than 500 ns would indicate that the unity-gain bandwidth of this loop should be higher than 2 MHz. Initially, an ideal amplifier with 40 dB gain and 20 MHz unity-gain bandwidth is used to represent the $A0$ stage.

The bode plot of the loop gain with different bias currents is shown in Figure 3.14. As the decrease of bias current, the loop gain increases dramatically and the second pole shifts towards the origin, which will affect the stability of the feedback. Since an ideal loop amplifier with 40 dB gain is used, the change of the loop gain should come from $A1$ and $A2$. In Figure 3.15, the red curve represents gain from $A1$ stage (composed by M6 and R1), and the yellow one shows the change of gain of $A2$ formed by M2 and M1. The gain of $A1$ does not experience a large variation, this is because the impedance at this stage is dominated by R1, which is a constant value. The loop gain variation and phase shift is due to the change of the drain-source transconductance (g_{DS}) in M1 and M2. In order to shift the pole to a higher frequency while narrow the variation range, the impedance at node A should be fixed

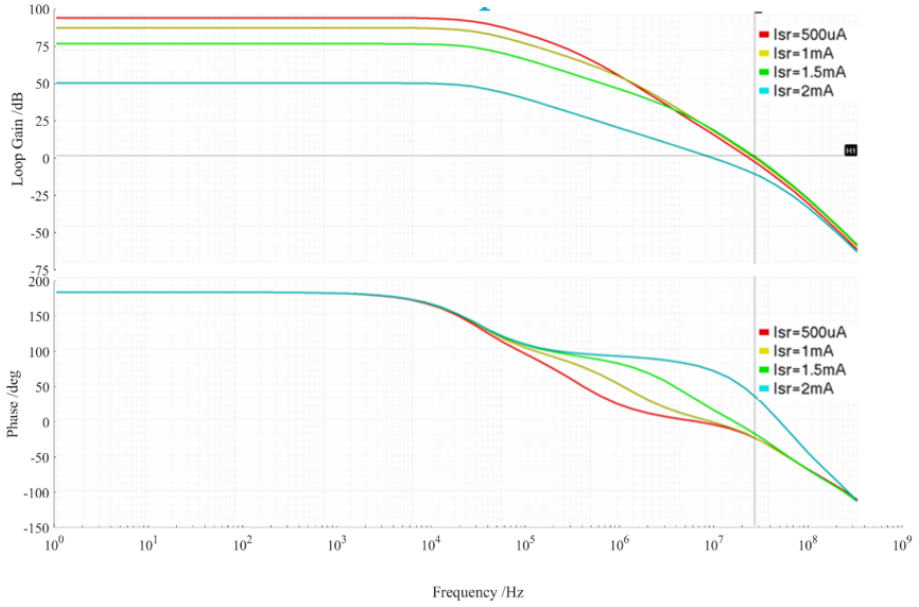


Figure 3.14: Bode plot of the loop gain for different bias currents

at a lower value. This can be achieved by a technique called resistive broadbanding as shown in Figure 3.16, which is the load resistors (R5 and R6) with low impedance connected to node A. In this way, the output impedance at node A is dominated by these load resistors. Considering the power consumption at the replica pulser and the pole frequency, the resistance of R5 and R6 are set to $10k\Omega$.

It is worth noting that when the bias current exceeds 1.5 mA, the gain shows a downward trend. This is because as the current increases, the overdrive voltage of M2 rumps up, and thus g_m of M2 also decreases. Figure 3.18 shows that the loop gain and the second pole variation range become very small under the same bias conditions. The phase margin and gain margin are both sufficiently large to ensure the loop stability under different bias conditions.

3.3 LOOP AMPLIFIER

In Section 3.2, a stable feedback loop with an ideal loop amplifier has been obtained. In the this section, the ideal amplifier will be replaced by a real amplifier and its specific parameters will be discussed to achieve similar results as before.

The gain of $A0$ is set to 40 dB and the unity gain bandwidth is 2 MHz which is same with the ideal case. Besides, the variable bias current will cause the amplifier's output voltage to swing up and down, so it is necessary to have enough margin to prevent the amplifier from working in the wrong operating region.

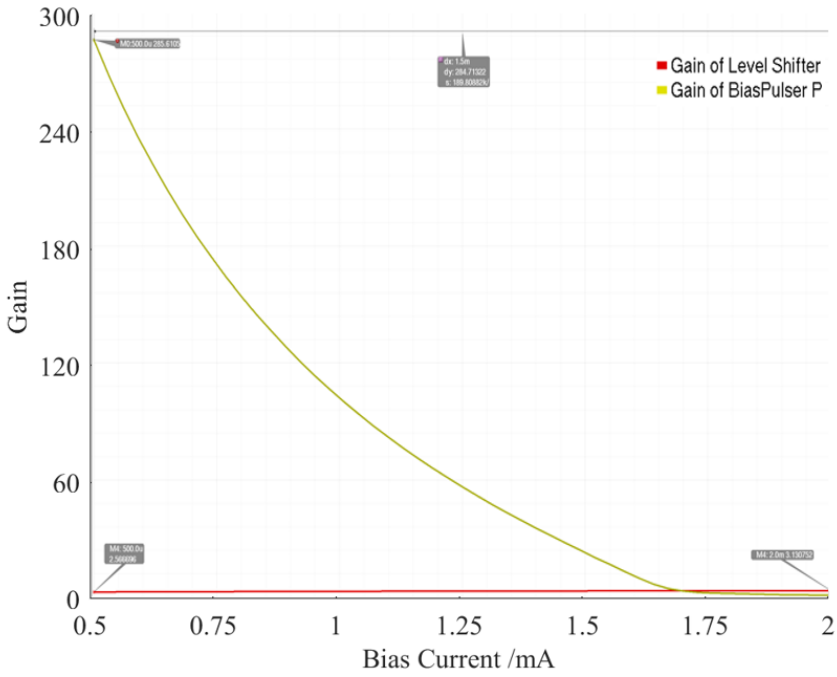


Figure 3.15: The variable gain of level shifter and replica pulser with the bias current changes

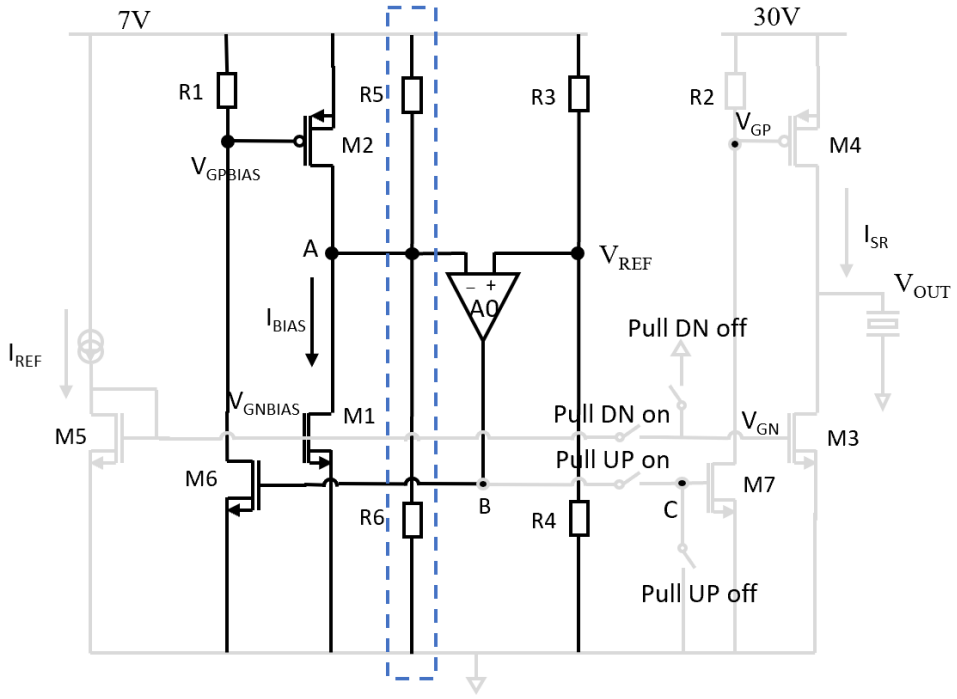


Figure 3.16: Negative feedback loop with resistive broad-banding

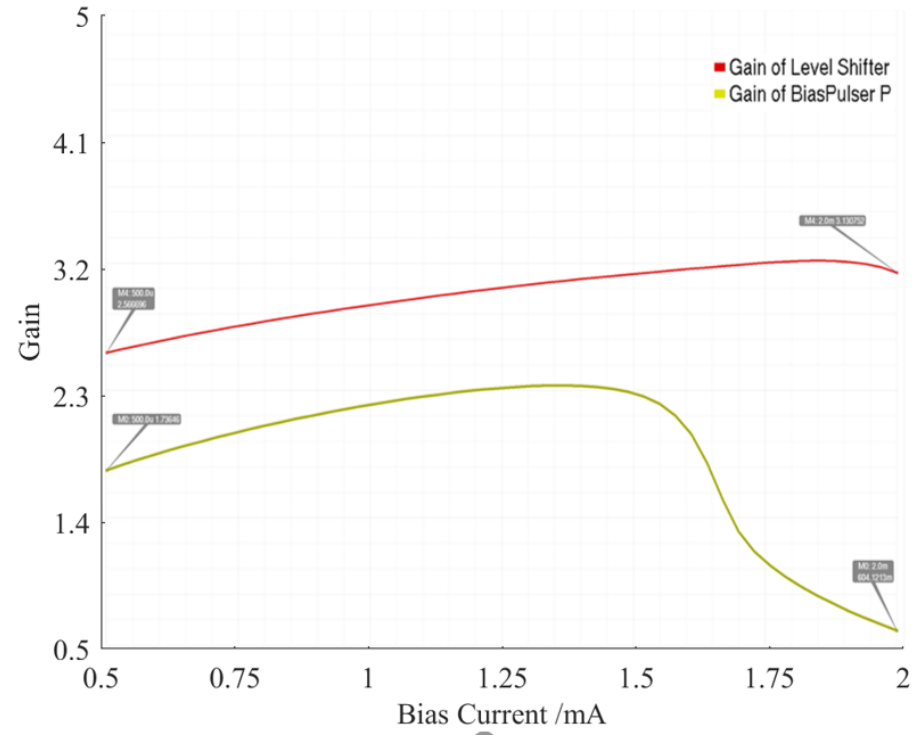


Figure 3.17: The gain performance of level shifter and replica pulser with the resistive broad-banding

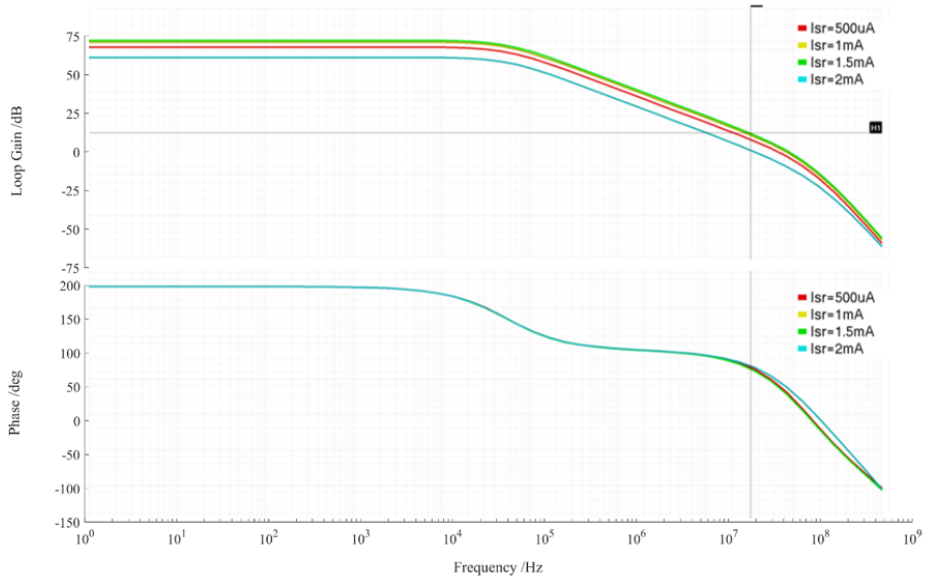


Figure 3.18: Bode plot of the modified negative feedback with an ideal amplifier

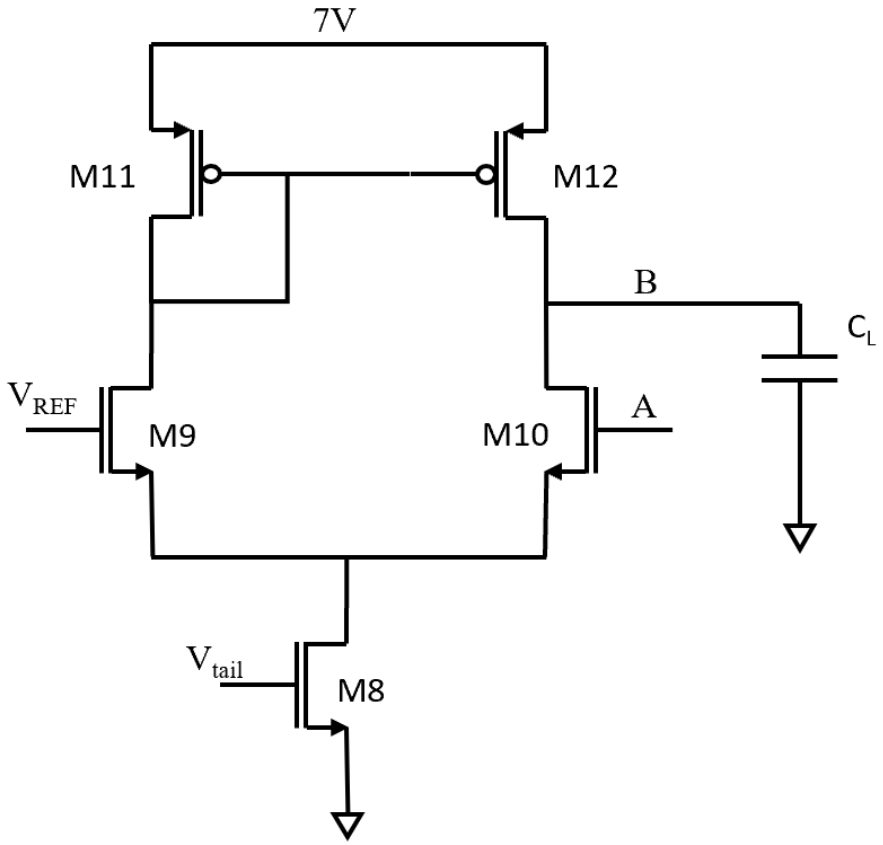


Figure 3.19: Circuit diagram of the loop amplifier

The circuit diagram of the amplifier is determined as a differential pair with active current mirror, as shown in Figure 3.19 In order to reduce power consumption while maintaining a certain speed. The size of transistors can be determined by the g_m/I_D method.

$$GBW = 2\pi f_{unity} = \frac{g_m}{C_L} \tag{3.5}$$

$$BW = \frac{2\pi f_{unity}}{A_o} = \frac{g_m}{A_o C_L} \tag{3.6}$$

The required bandwidth and open-loop gain have been discussed before, according the Equation 3.5 and Equation 3.6, g_m can be calculated. In order not to increase too much power, the power consumption of the amplifier should be much smaller than the power consumption on the level shifter. The W/L ratio can be determined as Equation 3.7

$$I_\square = I_D / \left(\frac{W^*}{L^*}\right) \tag{3.7}$$

A larger $I_\square$ should be chosen to minimize the area, which means the g_m/I_D should be smaller. Finally, the $g_{m9,10}/I_D = 5$ and $g_{m11,12}/I_D = 6$. The value of $I_\square$ can be determined according to the plot shown in Figure 3.20. The

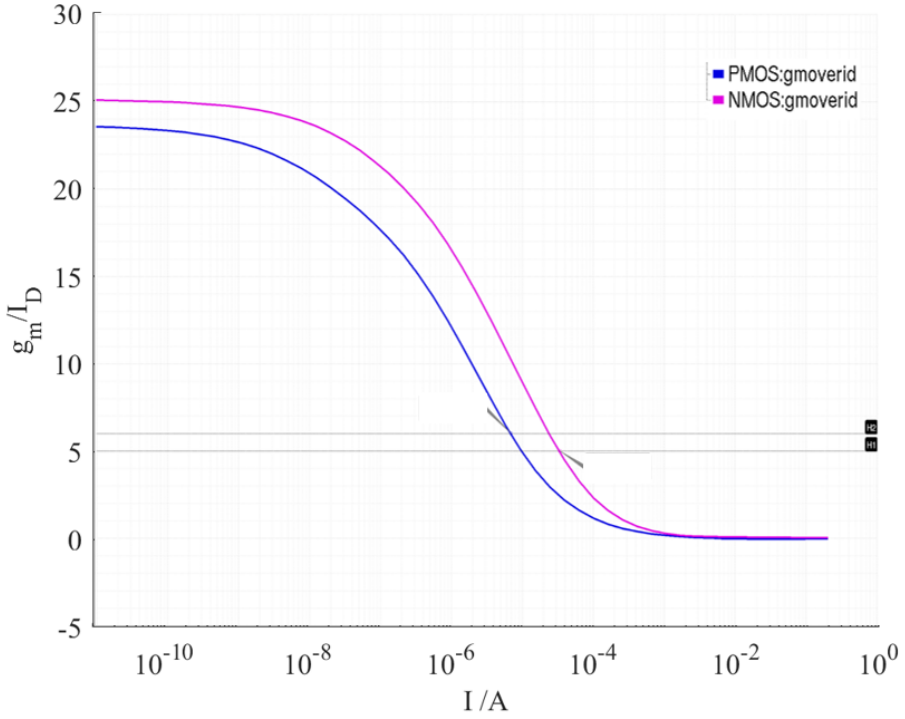


Figure 3.20: g_m/I_D vs $I_\square$ plot

size of each transistor in the loop amplifier can be determined according to Equation 3.8.

$$W/L = \frac{I_D}{I_\square} \tag{3.8}$$

The bode plot based on the calculated loop amplifier is shown in Figure 3.21. The figure shows that the open-loop gain and -3 dB bandwidth of the amplifier are close to the expectations. The amplifier shown in Figure 3.19 replaces the ideal loop amplifier in Figure 3.16. The bode plot of the loop gain is shown in Figure 3.22. It shows a similar DC gain, phase margin and gain margin compared to Figure 3.18.

3.4 SWITCH

In multi-channel pulsers, each channel needs a switch to control the connection to the transmit driver and choose the different slewing currents. The switching circuit is illustrated in Figure 3.23. Some voltage drop will inevitably occur on the switches. If these voltages are too large, they will have a non-negligible impact on the settling time, which will cause a higher propagation delay mismatch between pull-up and pull-down paths. To reduce the error, the transmission gate is used as the switch to minimize the on-resistance. On the other hand, when the gate of M7 and M3 need to be connected to the ground, the source of the switch is tied to the ground. Therefore, a single transistor is sufficient.

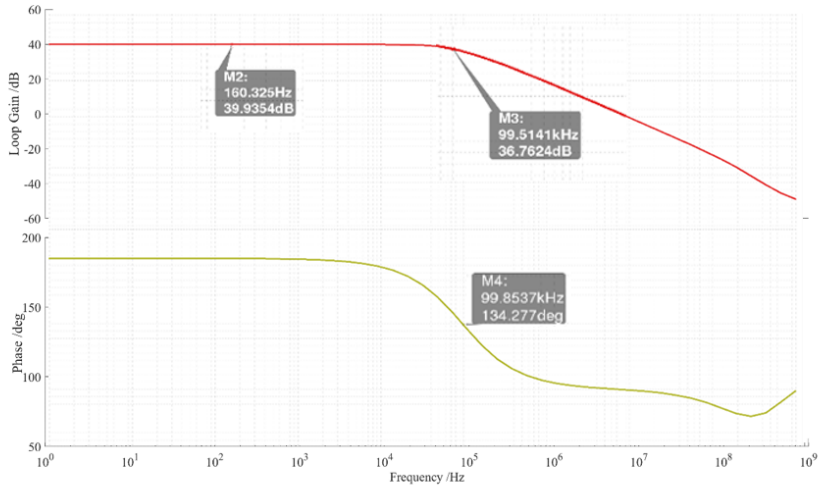


Figure 3.21: Bode plot of the loop amplifier

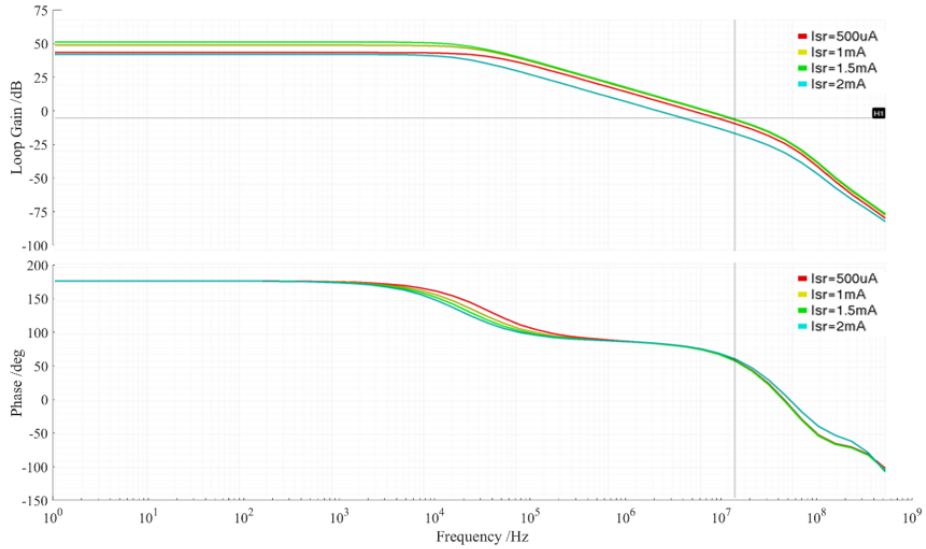


Figure 3.22: Bode plot of the negative feedback with a real amplifier

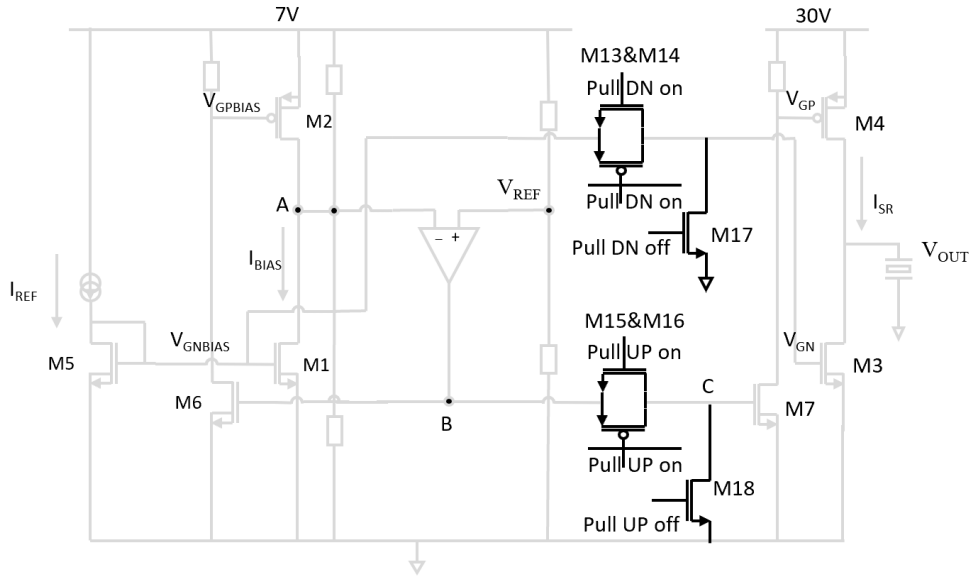


Figure 3.23: Block diagram of the entire circuit with switch circuit

3.5 BUFFER

Up to now, the functions mentioned in Chapter 1 have been accomplished, and the circuit diagram is shown in Figure 3.23. However, if the transmit driver is connected to multi-channel pulsers simultaneously, the load of the loop amplifier will be multiple times higher than the single-channel case, which means the bandwidth will also be multiple times lower. This causes that the voltage at node B cannot completely settle within the switching period, which can be seen from Figure 3.24. C_D is the decoupling capacitor at node B. It is necessary to add buffers to decouple the load capacitance from the node B and V_{GN} on both sides of pulser such that the loop amplifier will only see the gate capacitance of the buffers.

For the buffer of V_{GN}, two source followers M19 and M20 are added above the original current mirror, V_{GN} and V_{GNBIAS} nodes are connected to the source terminal of M19 and M20 respectively. In this case, the output impedance becomes $1/(g_m + g_{mb})$. Finally, the size of M19 and M20 chooses to $8\mu/600n$.

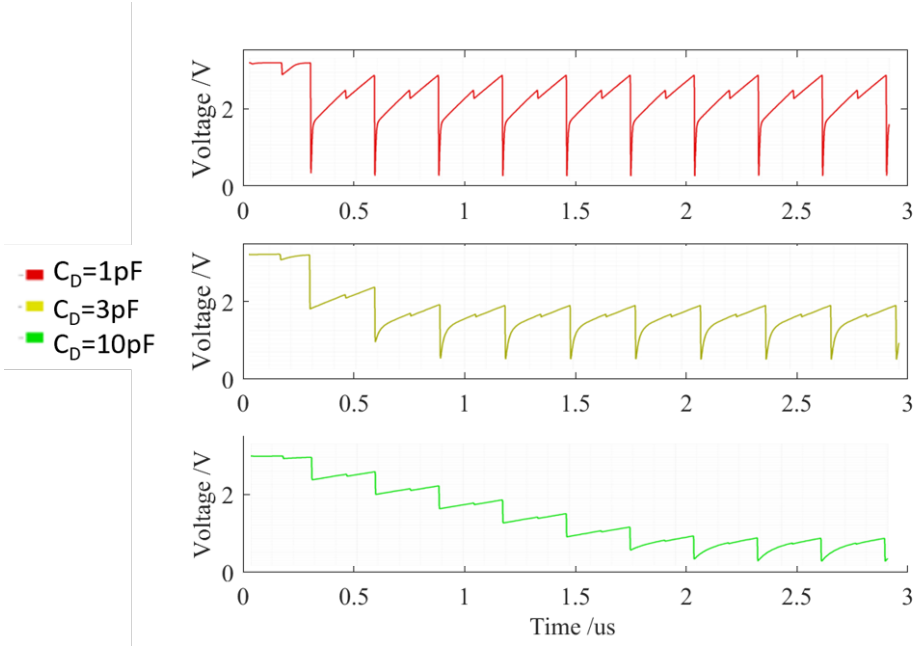


Figure 3.24: Settling behaviour of the entire circuit without buffer

4 SIMULATION RESULTS ANALYSIS

In this chapter, the simulation results of the circuit mention in Chapter 3 are illustrated. HD2 reduction by matching the slew rate and amplitude modulation by the combination of slew rate tuning and pulse width modulation are verified.

4.1 SLEWING CURRENT

To realize the fine adjustment (SRM) of the pulse amplitude at the fundamental frequency, the adjustable slewing current is necessary. Therefore, the slewing current needs to have an accurate proportional relationship with the reference current, otherwise, it will introduce additional errors to the fundamental frequency amplitude modulation. As discussed in Chapter 3, the reference current is equal to 0.5 mA, 1 mA, 1.5 mA and 2 mA respectively. Ideally, the slewing current is ten times larger than the reference current. However, since the transmit driver and the pulser do not work in precisely the same operating point because of the different supply voltage domain, the overdrive voltage on both stages can not be mirrored completely. Compared to the ideal case, there are some inevitable errors of four levels of slewing current. These errors can be ignored if the impact on HD2 is small, more details will be discussed in Section 4.3. Figure 4.1 the slewing current during pull-up and pull-down respectively.

4.2 PWM AND SRM

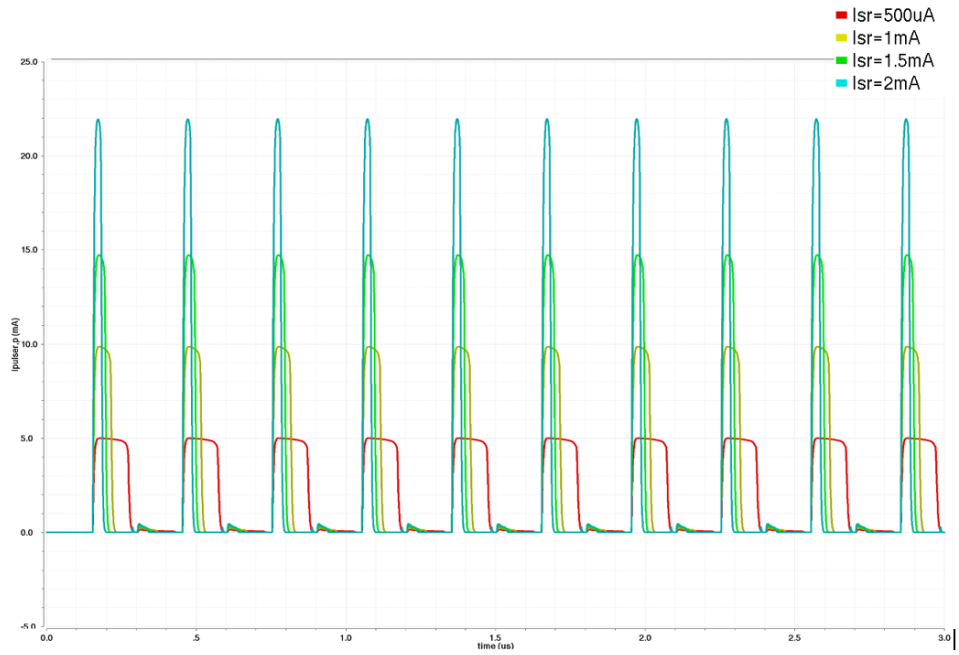
Assuming a 200 MHz central clock is provided , the pulse width can be adjusted with a 5 ns resolution. Meanwhile, the slew rate modulation is accomplished by the four-set slewing current mentioned in Section 4.1. Figure 4.2 shows a combination of both methods.

4.3 PERFORMANCE OF HD2

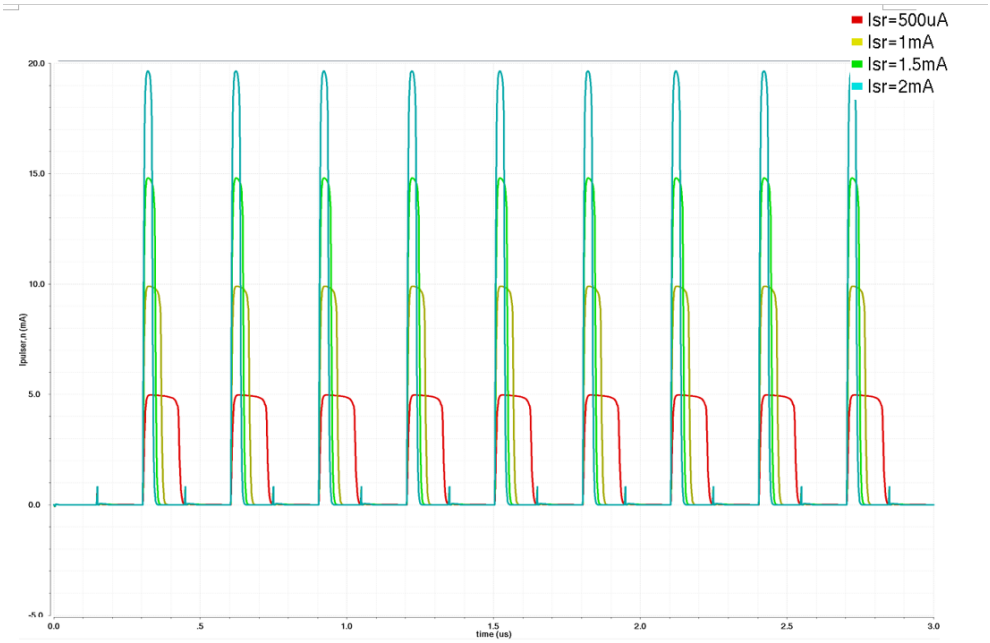
The objective of HD2 has been defined in Chapter 1, which should be smaller than -40 dB under 50% duty cycle without any trimming. The HD2 of the pulser output with four slewing currents is plotted in Figure 4.3, all of them are below -40 dB as expected. The time delay in the pull-up side is longer than the pull-down side because of an additional level shifter in the pull-up side. Therefore, to make the duty cycle much closer to 50%, the slewing current on the pull-up side should be higher than the pull-down side. The difference between the slewing currents on both sides is minimal when the bias current is 1.5 mA. Therefore, HD2 shows in Figure 4.3 increases from 0.5 mA to 1.5 mA and drops again at 2 mA.

4.4 PULSE AMPLITUDE MODULATION

As shown in Figure 4.2, pulse amplitude is modulated by combining the PWM and SRM. The goal is to adjust of the fundamental frequency amplitude while maintaining linearity as much as possible. Figure 4.4 shows the fundamental pulse amplitude of the pulser output. A tunable range of the fundamental frequency amplitude from $1.5V$ to $19V$ is obtained. The maximum fundamental amplitude of the 28% duty cycle is almost equal to the

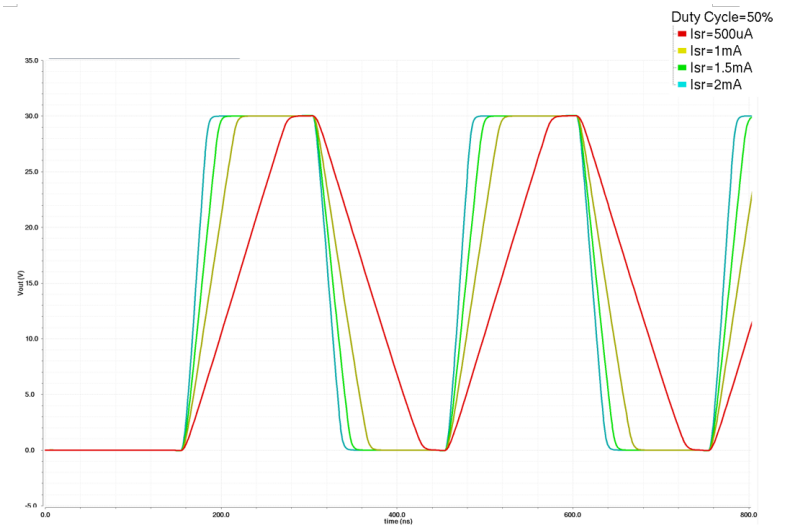


(a)

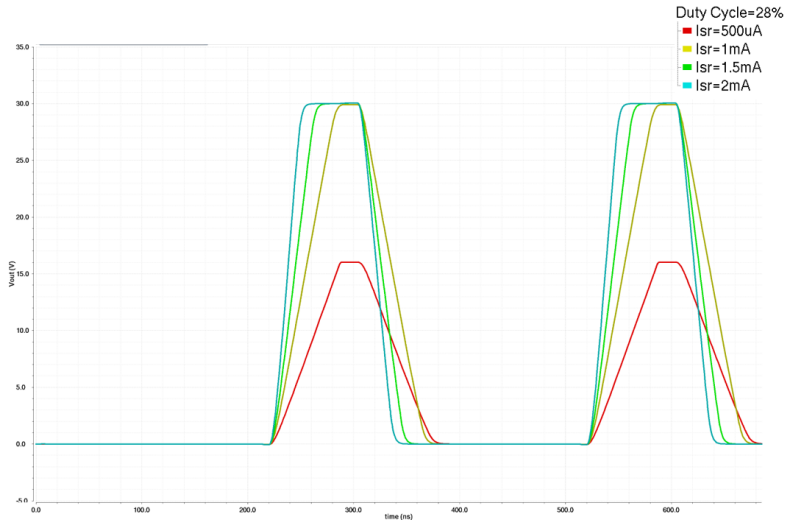


(b)

Figure 4.1: Slewing current corresponding to the different reference current during pull-up and pull-down period. (a) Pull-up slewing current (b) pull-down slewing current



(a)



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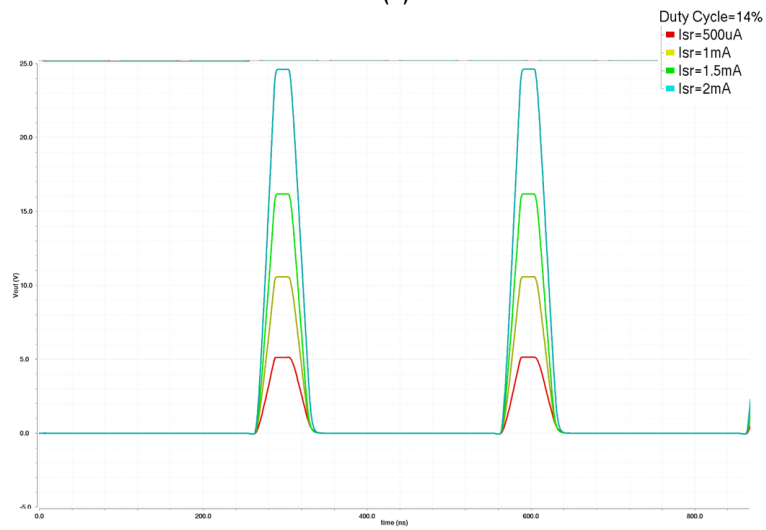


(c)

Figure 4.2: Four slewing currents under different duty cycles. (a) 50% Duty Cycle; (b) 28% Duty Cycle; (c) 14% Duty Cycle

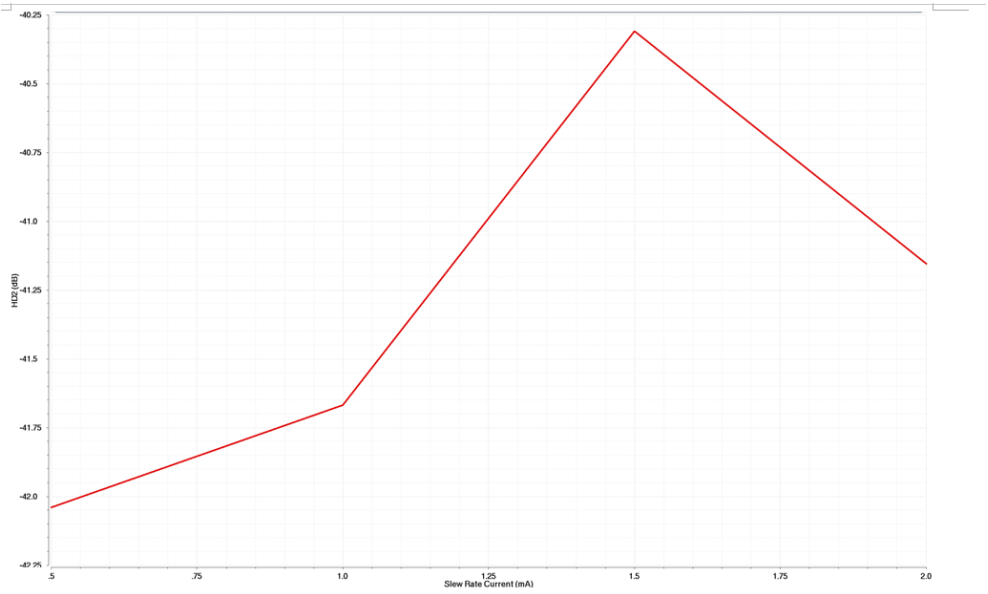


Figure 4.3: HD2 performance of four slewing currents at 50% duty cycle

minimum amplitude of the 50% duty cycle, and so on. If the interval between the duty cycles is reduced, the linearity can be further improved.

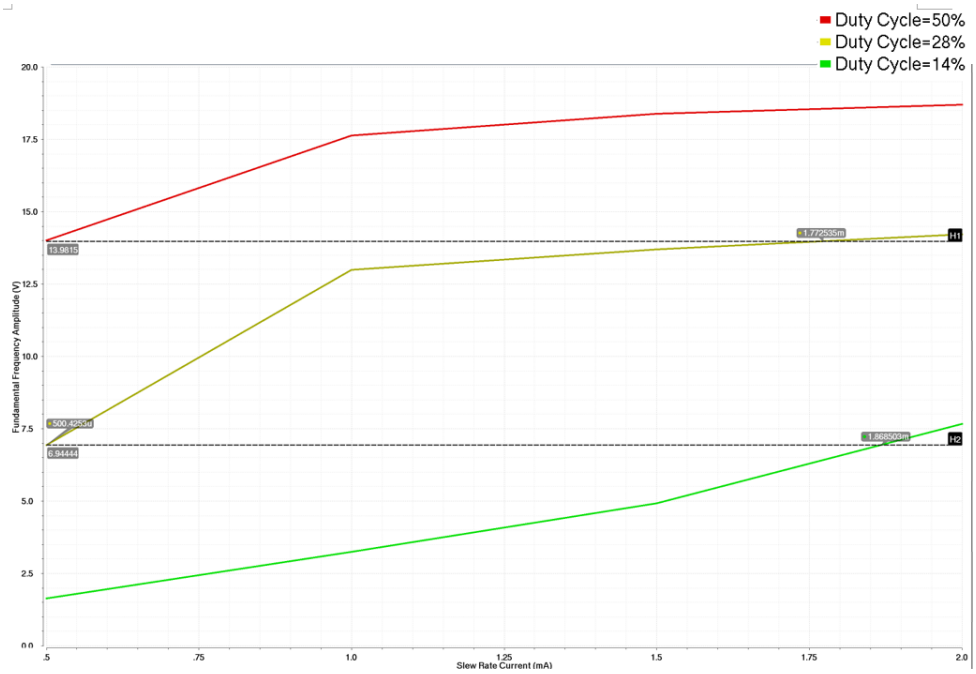


Figure 4.4: Apodization capability

5 EXPERIMENTS SET-UP

In this chapter, the HD2 comparison of bipolar pulse and unipolar pulse is presented. Moreover, different driving modes for the transducer are investigated by means of simulation with ideal signal sources and opamp-based circuits are proposed that can facilitate this comparison in a future experiment.

5.1 COMPARISON OF UNIPOLAR AND BIPOLAR PULSER

Figure 5.1 shows the waveform of unipolar pulses and bipolar pulses. Up to now, all simulation results have been acquired based on a unipolar pulser that requires a small number of HV transistors [[28]. However, this comes with several disadvantages. In comparison to bipolar pulses, unipolar pulses contain more low-frequency out-of-band amplitude and spend more dynamic power consumption with the same peak-to-peak output voltage [29]. Meanwhile, it is much easier to implement image-enhancing techniques by using bipolar pulses [30]. Moreover, the even-order harmonics of unipolar pulses are sensitive to pulse width modulation. Hence, if the fundamental amplitude is controlled by PWM, it will inevitably have a great impact on HD2. This means it is hard to achieve a very low HD2 in the case of apodization while it can be extremely alleviated in bipolar pulser. Assuming that there is no slew rate mismatch, low even-order harmonic distortion can be obtained duty cycle is equal to 50%.

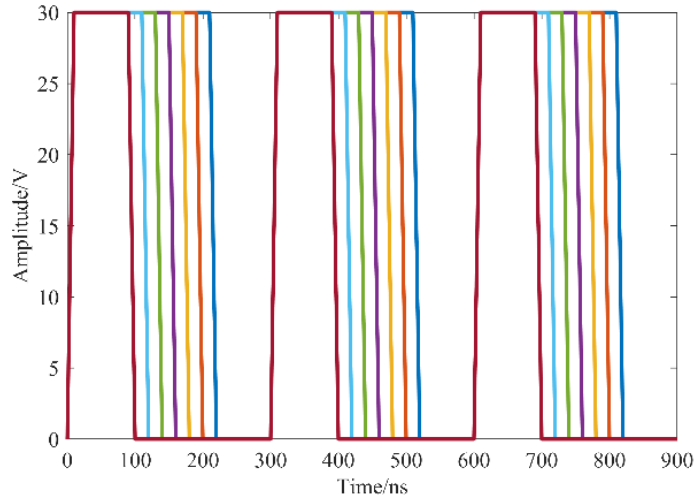
5.2 DIFFERENT DRIVING MODE OF TRANSDUCERS

As shown in Figure 5.2, when the transducer is driven by a pulser, the operation region of the transistors in the pulser changes periodically. That leads the output impedance of the pulser to change as well. During the transition period, the transistors in a pulser work in the saturation region and the output impedance is high which is called the current-driving mode. The rest of time is referred to the voltage-driving mode, because the transistors work in the triode region, which means the output impedance becomes small. As visible in Figure 5.2, $T_{up} and T_{down}$ represent the current driving mode period whereas the rest of the whole period is the voltage driving mode.

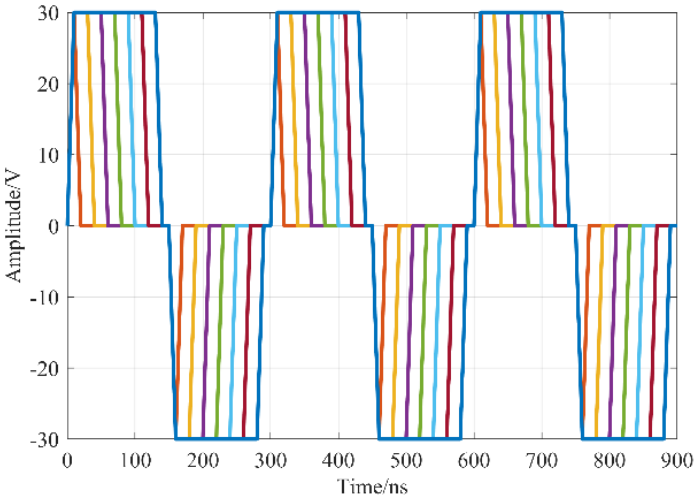
Figure 4.2 illustrates that if the duty cycle becomes so small that the output voltage does not have enough time to be charged to its supply voltage, this means even if the output voltage reaches the peak value, the pulser may still work in the saturation region. The transducer works in current driving mode for more than half of the cycle. The question of whether the different driving modes of the transducer will lead to different acoustic power efficiency caught our attention. On the one hand, a more efficient driving mode can be selected when the difference is very significant. On the other hand, if the difference is not obvious, transducers can work in the current driving mode, which makes it is possible to realize the bipolar pulse wave in the unipolar pulse generator. Therefore, we proposed an experiment to explore the acoustic power efficiency of the transducer under different driving modes.

Before the experiment, the circuit needs to be simulated with ideal components. The simulation will be explored from the following two aspects:

- Pure voltage mode: The transducer is driven by the ideal voltage source.



(a)



(b)

Figure 5.1: Unipolar and bipolar with pulse width modulation (a) Unipolar waveform (b) Bipolar waveform

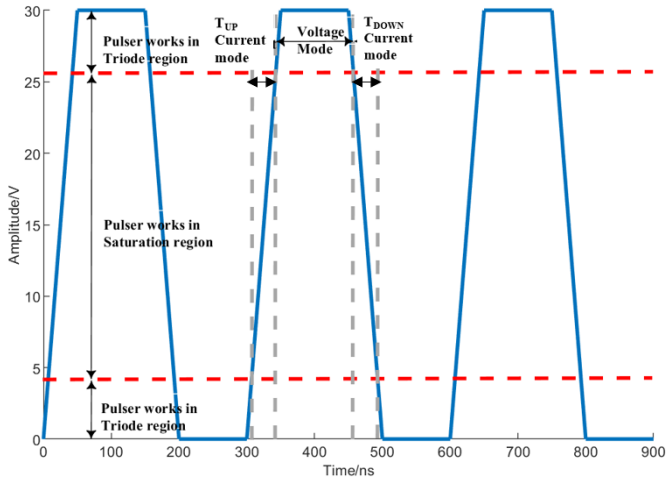


Figure 5.2: Driving mode of a unipolar pulser

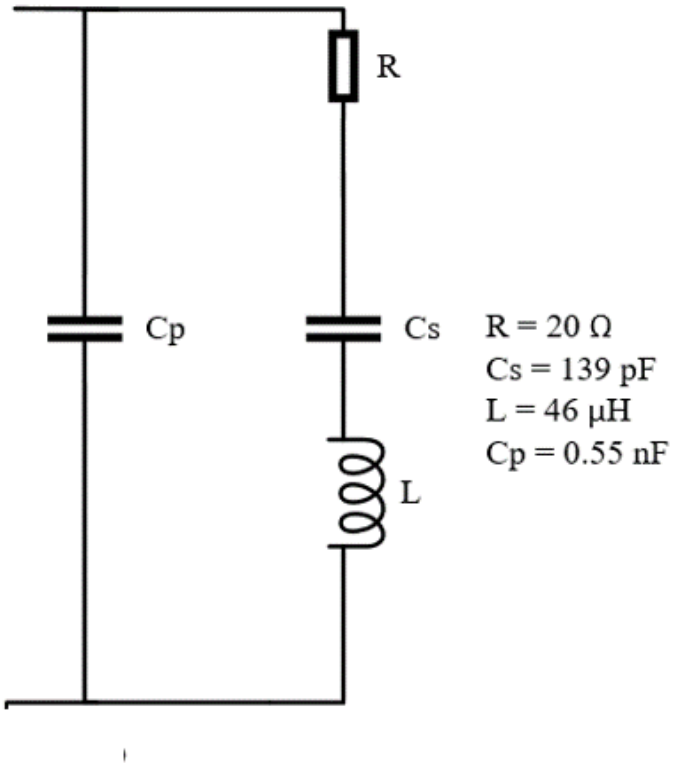


Figure 5.3: Transducer model

- Pure current mode: The transducer is driven by the ideal current source during the transition time. The output floats after reaching the peak value.

5.3 SIMULATION WITH IDEAL POWER SOURCE

This simulation uses an existing transducer model with the equivalent circuit diagram shown in Figure 5.3. Based on the two simulation strategies, the output voltage waveform is illustrated in Figure 5.4, where the time period, slew rate and voltage swing are all the same. In the transducer model shown in Figure 5.3, the branch consisting of R, C_S, L represents the mechanical part, and the electrical part is represented by C_P. The power dissipated in R represents the acoustic power emission into the medium. The parallel resonance frequency of this transducer is 2 MHz, while the series resonance frequency is around 2.2 MHz. The output voltage drops because of the discharge of the capacitor, but the current stored in the inductor will charge the capacitor and make the output voltage rise again. The average power of two driving modes with 2 MHz input signal is listed in Table 5.1 below.

According to the simulation with the ideal current and voltage sources, it can be preliminarily considered that the difference in the driving modes has

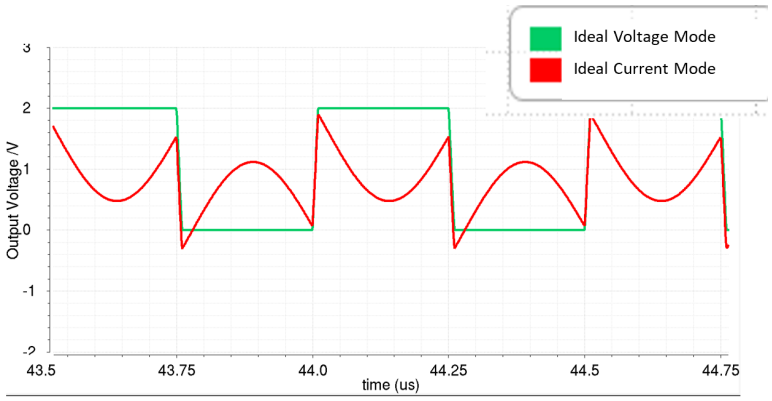


Figure 5.4: Output waveform of voltage mode driving and current mode driving with 2 MHz input signal

Driving Mode	Average Power(mW)
Voltage Mode	33
Current Mode	0.853

Table 5.1: Average acoustic power of two driving modes with 2MHz input signal

a great impact on acoustic power output. The huge difference in average power is due to the gap between parallel and series resonance frequency. Under the current driving mode, one side of transducer is connected to the high impedance node, the other side is connected to ground, which means the branches of C_P and RLC branch are in series. In contrast, these two branches are in parallel when the voltage mode is employed because C_P is shunted by the low-impedance voltage source. From Figure 5.5, the peak value of average power in current mode is 33 mW under 2.2 MHz input frequency. The output amplitude and the power in the current mode gradually increase when the frequency changes from 2 MHz to 2.2 MHz. This is because the current stored in the inductor will not be completely discharged due to the shorter pulse width. If the frequency continue to increase, the current through the transducer decreases as the equivalent impedance of the transducer increase, which leads to the decrease of power.

5.4 SIMULATION WITH ACTUAL OPAMP

In this section, an opamp-based circuit is proposed to experimentally verify the acoustic power difference between current and voltage modes. As shown in Figure 5.6, the difference between the two circuits is where the transducer is placed. Figure 5.6a is the current driving mode in which the transducer is connected in parallel with a large resistor and placed in the feedback loop such that the terminal connected to the virtual ground sees low impedance and the terminal connected to the output sees the high impedance. Figure 5.6b is the voltage driving mode in which the transducer is placed at the output of OpAmp such that the transducer is interfaced with low impedance source.

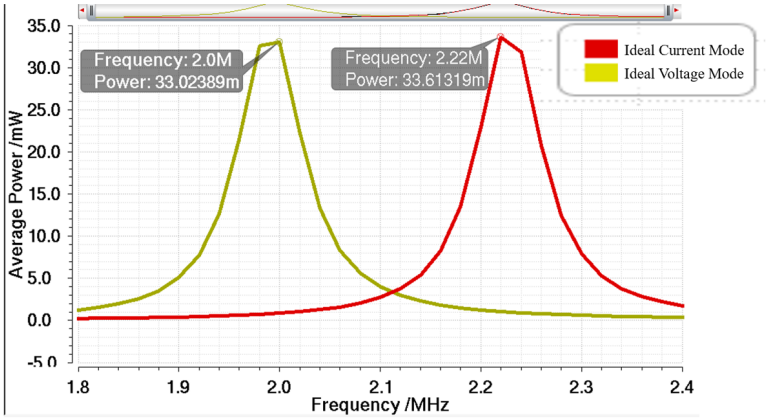
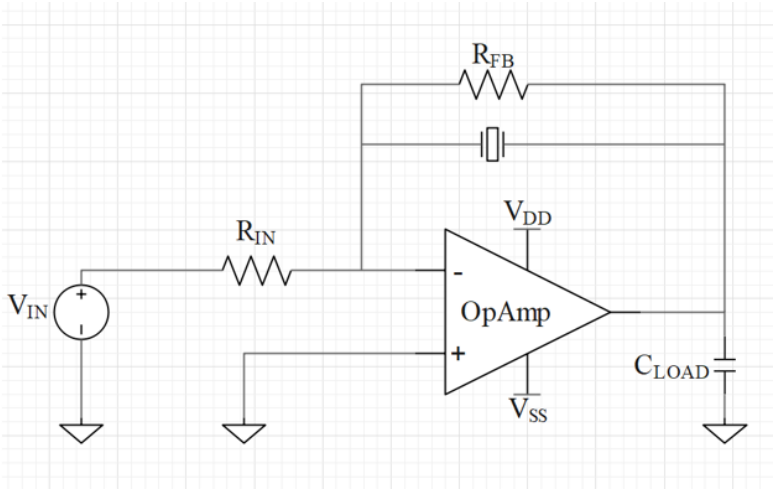
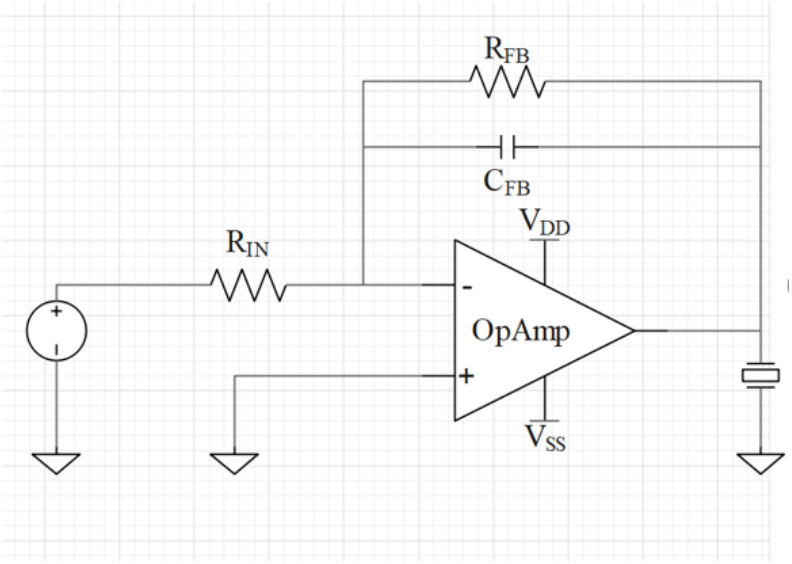


Figure 5.5: Average power under current and voltage modes



(a)



(b)

Figure 5.6: OpAmp configuration for current mode and voltage mode drive (a) Current mode (b) Voltage mode

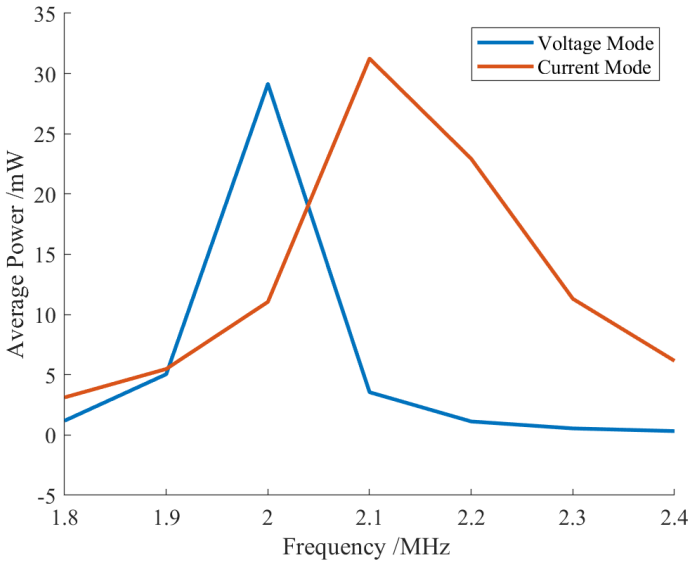


Figure 5.7: Average power under current and voltage modes with OpAmp

The average power in the two driving modes implemented by OpAmp are comparable with implementation using ideal voltage and current source as shown in Figure 5.7.

6 CONCLUSION AND FUTURE WORK

	This work	[9]	[25]
Process	TSMC 0.18μm HV BCD	0.5μm CMOS SOI	TSMC 0.18μm HV BCD
Supply voltage (V)	1.8	4	1.8
Max.transmit amplitude (Vpp)	30	150	60
Amplitude modulation range (V)	$2-18$	n/a	n/a
HD2 (50% Duty Cycle)(dB)	<-40	<-40	n/a
Transducer center freq. (MHz)	7.5	2.5	2.5
Pulse freq. (MHz)	5	2	9
Power (mW/ch)	<1	<50	<1

Table 6.1: Performance summary and comparison with the prior art

6.1 CONCLUSIONS

The goal of this thesis is to design an integrated HD2 pulser with improved HD2 and programmable amplitude, which can be used for harmonic ultrasonic imaging and apodizing the transducer array.

To do so, several techniques have been implemented:

- A transmit driver circuit with a small area and low power consumption has been implemented, making it possible to drive multi-channel pulsers with programmable pulse width and slew rates.
- The programmable amplitude has been achieved via PWM and SRM. PWM (coarse adjustment) is realized with a 5 ns time resolution. SRM (fine adjustment) is achieved by employing multiple transmit driver circuits, which can improve the amplitude modulation resolution to roughly three times smaller than the PWM.
- A negative feedback loop with a replica pulser structure has been implemented in the transmit driver circuit, which can obtain a balanced slewing current to achieve an improved HD2
- Every HV pulser is connected to selected transmit drivers by transmit switches. These transmit switches are controlled by the timing logic circuit.

Besides, an experiment to compare the effective acoustic power efficiency of the transducer under different driving modes (current mode voltage mode) has been proposed. Preliminary simulation work has done for the implementation of the experiment, the simulation results show that when the transducer is working at the parallel resonance frequency, the efficiency in the voltage driving mode is higher than that in the current driving mode.

Table 6.1 summaries the performance of the ASIC and compares it to the prior art.

6.2 FUTURE WORK

The main goal of the project was to design an ASIC to improve ultrasound imaging without consuming significant power consumption and area. Up to the present design, several aspects of the circuit can be further improved.

- The transmit driver and pulser level shifters are working in different supply domains, which leads to mismatch of the transistors' operating points. The overdrive voltage in the replica pulser can not be accurately copied to the pulser and thus affect the performance of HD2. Reducing mismatch will effectively improve the HD2.
- This design is based on unipolar pulsers. Due to the PWM function, the duty cycle will shift from 50% and HD2 becomes worse. The bipolar pulser structure can be adopted to guarantee low HD2 when PWM is operated
- The current project is still at the stage of circuit design. Layout and post-layout simulation still need to be done to check whether the performance can meet the specifications. In the end, the chip will be taped-out and measured.
- Finally, current-mode driver and voltage-mode driver will be implemented on the PCB board to compare their driving efficiency.

BIBLIOGRAPHY

[1] Talat Uppal. Tissue harmonic imaging. *Australasian Journal of Ultrasound in Medicine*, 13(2):29, 2010.

[2] Eunchul Kang, Mingliang Tan, Jae-Sung An, Zu-Yao Chang, Philippe Vince, Nicolas Sénégond, Tony Mateo, Cyril Meynier, and Michiel AP Pertijs. A variable-gain low-noise transimpedance amplifier for miniature ultrasound probes. *IEEE Journal of Solid-State Circuits*, 2020.

[3] M Ranjbaran, MM Tehranchi, SM Hamidi, and SMH Khalkhali. Effects of square-wave magnetic fields on synchronization of nonlinear spin precession for sensitivity improvement of mx magnetometers. *Journal of Magnetism and Magnetic Materials*, 441:718–723, 2017.

[4] Richard SC Cobbold. *Foundations of biomedical ultrasound*. Oxford university press, 2006.

[5] Parisa Behnamfar and Shahriar Mirabbasi. Design of a high-voltage analog front-end circuit for integration with cmut arrays. In *2010 Biomedical Circuits and Systems Conference (BioCAS)*, pages 298–301. IEEE, 2010.

[6] İhsan Cicek, Ayhan Bozkurt, and Mustafa Karaman. Design of a front-end integrated circuit for 3d acoustic imaging using 2d cmut arrays. *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, 52(12):2235–2241, 2005.

[7] Igal Ladabaum, Xuecheng Jin, Hyongsok T Soh, Abdullah Atalar, and BT Khuri-Yakub. Surface micromachined capacitive ultrasonic transducers. *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, 45(3):678–690, 1998.

[8] Krzysztof Iniewski. *Medical Imaging*. Wiley Online Library, 2009.

[9] Yen-Chung Huang, Chin Hsia, and Guo-Zua Wu. A high-voltage integrated bipolar pulser for medical ultrasound scanner applications. In *2017 IEEE International Conference on Consumer Electronics-Taiwan (ICCE-TW)*, pages 33–34. IEEE, 2017.

[10] Vincent Chan and Anahi Perlas. Basics of ultrasound imaging. In *Atlas of ultrasound-guided procedures in interventional pain management*, pages 13–19. Springer, 2011.

[11] Ira O Wygant, Nafis S Jamal, Hyunjoo J Lee, Amin Nikoozadeh, Ömer Oralkan, Mustafa Karaman, and Butrus T Khuri-Yakub. An integrated circuit with transmit beamforming flip-chip bonded to a 2-d cmut array for 3-d ultrasound imaging. *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, 56(10):2145–2156, 2009.

[12] Robert Chebli and Mohamad Sawan. Fully integrated high-voltage front-end interface for ultrasonic sensing applications. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 54(1):179–190, 2007.

[13] Yashodhan Moghe, Torsten Lehmann, and Tim Piessens. Nanosecond delay floating high voltage level shifters in a 0.35\μu m hv-cmos technology. *IEEE Journal of Solid-State Circuits*, 46(2):485–497, 2010.

[14] Robert Wodnicki, Bruno Haider, and KAIE THOMENIUS. Electronics for diagnostic ultrasound. *Medical Imaging: Principles, Detectors, and Electronics, edited by Krzysztof Iniewski*, pages 167–220, 2009.

[15] Yutaka Igarashi, Shinya Kajiyama, Yusaku Katsube, Takuma Nishimoto, Tatsuo Nakagawa, Yasuyuki Okuma, Yohei Nakamura, Takahide Terada, Taizo Yamawaki, Toru Yazaki, et al. Single-chip 3072-element-channel transceiver/128-subarray-channel 2-d array ic with analog rx and all-digital tx beamformer for echocardiography. *IEEE Journal of Solid-State Circuits*, 54(9):2555–2567, 2019.

[16] Eunchul Kang, Qing Ding, Maysam Shabanimotlagh, Pieter Kruizinga, Zu-Yao Chang, Emile Noothout, Hendrik J Vos, Johan G Bosch, Martin D Verweij, Nico de Jong, et al. A reconfigurable ultrasound transceiver asic with 24\$\times$40 elements for 3-d carotid artery imaging. *IEEE Journal of Solid-State Circuits*, 53(7):2065–2075, 2018.

[17] Mingliang Tan, Chao Chen, Zhao Chen, Jovana Janjic, Verya Daeichin, Zu-Yao Chang, Emile Noothout, Gijs van Soest, Martin D Verweij, Nico de Jong, et al. A front-end asic with high-voltage transmit switching and receive digitization for 3-d forward-looking intravascular ultrasound imaging. *IEEE Journal of Solid-State Circuits*, 53(8):2284–2297, 2018.

[18] Thomas L Szabo. *Diagnostic ultrasound imaging: inside out*. Academic Press, 2004.

[19] Thong Huynh, Lars Hoff, and Trym Eggen. Sources of 2 nd harmonic generation in a medical ultrasound probe. In *2018 IEEE International Ultrasonics Symposium (IUS)*, pages 1–4. IEEE, 2018.

[20] Kazuaki Tanabe, Marek Belohlavek, James F Greenleaf, and James B Seward. Tissue harmonic imaging. *Japanese circulation journal*, 64(3):202–206, 2000.

[21] Junsu Lee, Eui-Ji Shin, Changyang Lee, and Jin Ho Chang. Development of dual-frequency oblong-shaped-focused transducers for intravascular ultrasound tissue harmonic imaging. *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, 65(9):1571–1582, 2018.

[22] Andrea Trucco and Franco Bertora. Harmonic beamforming: performance analysis and imaging results. *IEEE transactions on instrumentation and measurement*, 55(6):1965–1974, 2006.

[23] Mohamad Hourani, Adrian Basarab, Denis Kouamé, and Jean-Yves Tourneret. Joint deconvolution of fundamental and harmonic ultrasound images. In *2019 IEEE International Ultrasonics Symposium (IUS)*, pages 2067–2070. IEEE, 2019.

[24] Chin Hsia, Yi-Chi Hsiao, and Yen-Chung Huang. A single-chip high-voltage integrated actuator for biomedical ultrasound scanners. *Sensors*, 19(23):5063, 2019.

[25] Mingliang Tan, Eunchul Kang, Jae-Sung An, Zu-Yao Chang, Philippe Vince, Tony Matéo, Nicolas Sénégond, and Michiel AP Pertijs. A 64-channel transmit beamformer with±30-v bipolar high-voltage pulsers for catheter-based ultrasound probes. *IEEE Journal of Solid-State Circuits*, 2020.

[26] Alan V Oppenheim, Alan S Willsky, S Hamid Nawab, and Day Time Room. Ee202 signals and systems fall 2014. 2014.

[27] Johan Borg and Jonny Johansson. An ultrasonic transducer interface ic with integrated push-pull 40 vpp, 400 ma current output, 8-bit dac and integrated hv multiplexer. *IEEE Journal of Solid-State Circuits*, 46(2):475–484, 2011.

[28] Gokce Gurun, Coskun Tekes, Jaime Zahorian, Toby Xu, Sarp Satir, Mustafa Karaman, Jennifer Hasler, and F Levent Degertekin. Single-chip cmut-on-cmos front-end system for real-time volumetric ivus and ice imaging. *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, 61(2):239–250, 2014.

[29] Weibao Qiu, Yanyan Yu, Fu Keung Tsang, and Lei Sun. A multifunctional, reconfigurable pulse generator for high-frequency ultrasound imaging. *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, 59(7):1558–1567, 2012.

[30] Sheng-Wen Huang and Pai-Chi Li. Arbitrary waveform coded excitation using bipolar square wave pulsers in medical ultrasound. *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, 53(1):106–116, 2006.