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Zhang, H.

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High-Performance Multilevel Class-D Audio Amplifiers

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chair of the Board for Doctorates

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by

Huajun ZHANG

Master of Science in Electrical Engineering, University of Michigan, USA

born in Beijing, China

This dissertation has been approved by the promotors.

Composition of the doctoral committee:
Rector Magnificus, chairperson
Prof.dr. K.A.A. Makinwa, Delft University of Technology, promotor
Dr. Q. Fan, Delft University of Technology, copromotor

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Other member:
Dr. M. Berkhout, Goodix Technology

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Chapter 1 Introduction

1.1 Motivation

Loudspeakers are ubiquitous in modern life. In the audio band, they typically have an impedance in the order of a few ohms and, depending on the application, dissipate to several watts to kilowatts, which means they must be driven by a power amplifier. The steady development of consumer electronics and automotive infotainment systems has increased the demand for high-performance and high-efficiency audio amplifiers.

Traditionally, Class-AB amplifiers are used to drive loudspeakers. However, for a sinusoidal input, their power efficiency is limited to a theoretical maximum of 78% [1], since their output stages typically consist of common source (emitter) amplifiers or source (emitter) followers, which must simultaneously handle large voltages and currents. This results in significant heat dissipation, leading to bulky and complicated cooling solutions and reduced battery life in portable applications. Nevertheless, Class-AB amplifiers are still prevalent in low-power (e.g., headphone) applications due to their excellent audio performance. For example, a Class-AB amplifier [2] driven by a standalone DAC [3] achieves a total harmonic distortion plus noise (THD+N) well below −100 dB, together with a dynamic range (DR) above 120 dB. Recent monolithic solutions also achieve similar or even better performance [4], [5].

In high-power applications, however, Class-D amplifiers (CDAs) are taking over from Class-AB amplifiers because their power efficiency is typically greater than 90%, which significantly simplifies their cooling requirements, thereby reducing system cost and size [6]. The advent of bipolar-CMOS-DMOS (BCD) process technology has made monolithic high-

voltage (HV, >10 V) CDAs feasible, thus enabling further miniaturization [7]. However, compared to Class-AB amplifiers, CDAs suffer from several disadvantages, including greater electromagnetic interference (EMI), lower dynamic range, and inferior linearity. In the coming sections, the basic operation of CDAs and the reasons for these disadvantages will be discussed in more detail.

1.2 Background

1.2.1 Principle of Operation

The term "Class-D" refers to a mode of operation in which an amplifier's output transistors function as switches, which, ideally, do not dissipate power. The required output voltage is then approximated by rapidly switching the output between a small number of supply voltages and low-pass filtering the result. Fig. 1.1 illustrates the operation of a typical single-ended (SE) Class-D output stage. This circuit, also known as the half-bridge, is widely used in various power electronics applications. The negative supply is required to ensure that no DC current flows through the speaker.

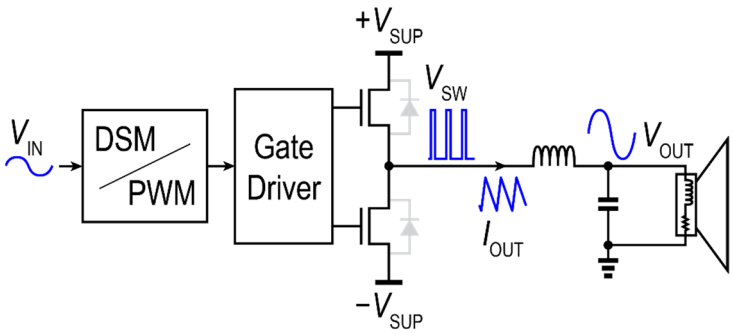

Fig. 1.1. Basic single-ended Class-D output stage.

In Fig. 1.1, the output is switched between discrete voltages, i.e., $\pm V_{SUP}$, which are produced at the switching node (V_{SW}) by the output stage. As a

result, V_{SW}, besides the audio-band content of the input signal V_{IN}, also consists of high-frequency components. The audio signal can be recovered by an LC low-pass filter or, in low-cost applications, by the speaker itself, since this typically behaves like an LR low-pass filter.

To avoid shorting the supply and ground (aka. cross conduction or shoot-through), a dead time is usually implemented to guarantee break-before-make switching of the high-side and low-side output transistors [7], [8]. The inductive load will still force a continuous current through the output stage nevertheless. This current will flow through the body diodes of the transistors (shown in grey in Fig. 1.1), adding a diode drop V_D to the output. The resulting output waveform is shown in Fig. 1.2.

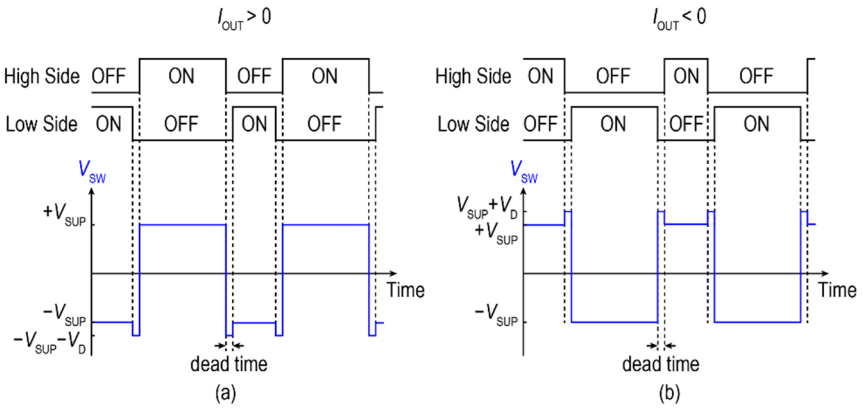

Fig. 1.2. Impact of dead time on the V_{SW} waveform.

To obviate the need for a negative supply, the speaker can be connected between two half-bridges, which is known as the bridge-tied-load (BTL) configuration, and the resulting output stage is called a full bridge or an H-bridge [9] (Fig. 1.3).

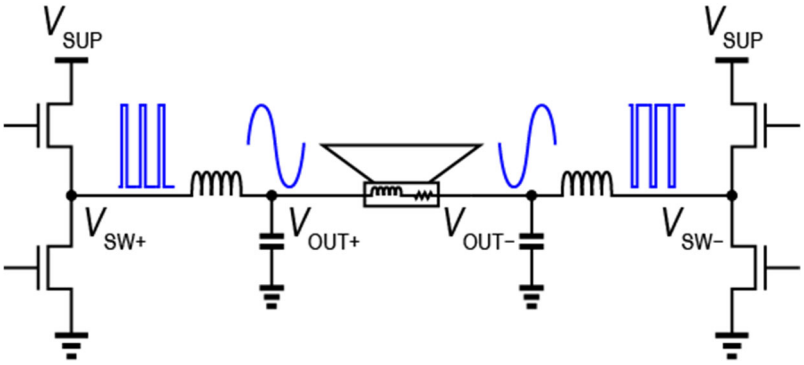

Fig. 1.3. Class-D output stage with bridge-tied-load (BTL) configuration.

1.2.2 Power Loss and Efficiency

The non-zero power dissipation of a practical Class-D output stage can be divided into conduction loss, transition loss, reverse conduction loss, and gate charge loss [10].

Conduction loss occurs in all the resistances that carry the load current, including the output transistors, metallization, bondwire, package, PCB routing, and the external inductor. Wider output transistors thus reduce the conduction loss on the chip at the expense of a larger silicon area.

As illustrated in Fig. 1.4, another source of power loss is due to the output transistor's finite switching speed, which is known as the transition loss. Due to the low-side body diode, when $I_{\mathrm{OUT}} > 0$, V_{SW} will not rise until the output current is completely sourced from the high side. Therefore, during the transition, the high-side transistor's drain-source voltage ($V_{\mathrm{DS,HIGH}}$) and drain current ($I_{\mathrm{D,HIGH}}$) are both nonzero, which implies power dissipation. Transition loss can be reduced by increasing the switching speed. However, this leads to a high di/dt in the output stage, inducing ringings due to parasitic inductances in the system, which could overstress the output transistors and lead to EMI issues. During the dead time, reverse conduction

through the body diode also causes power loss, as shown in the bottom plot of Fig. 1.4.

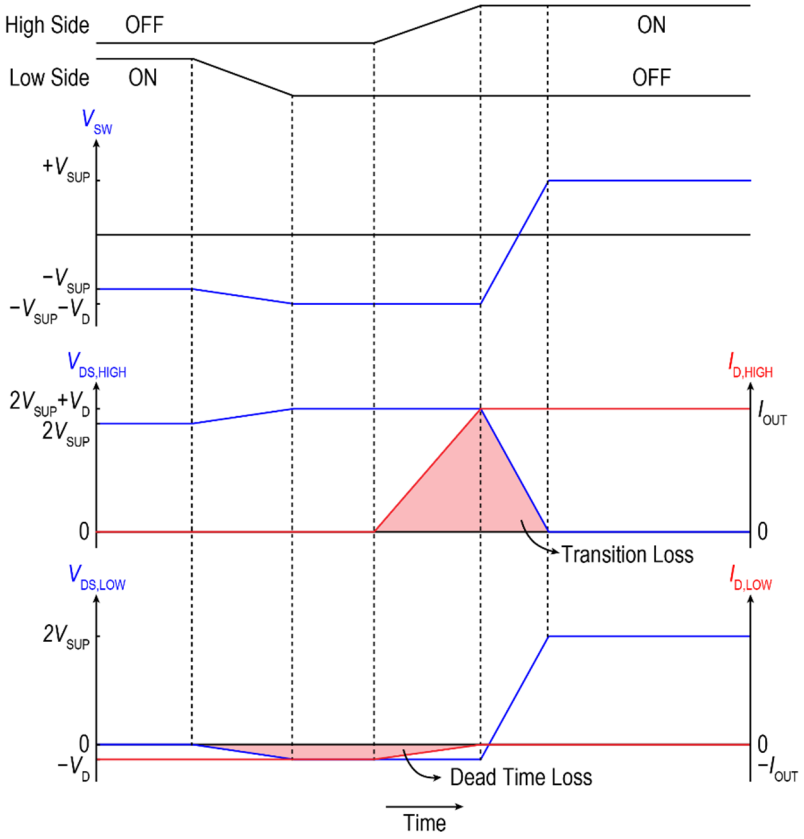

Fig. 1.4. Zoomed-in view of a rising transition in Fig. 1.2(a). For simplicity, the effect of parasitic capacitance is ignored.

Periodic charging of the input and output capacitances of the output transistors also adds to the power loss. The former is called gate charge loss, while the latter adds to the transition loss. They are proportional to the switching frequency and are present even when a zero input is applied to the CDA, and thus $I_{OUT} \approx 0$. The CDA's power consumption, in this case, is defined as the *idle power*. It can be reduced by employing segmented power transistors [11], by choosing a low switching frequency [12], [13], [14], and

by adopting a switching scheme that lowers the switching frequency at low input levels [15], [16].

To quantify the power loss with respect to the power delivered to the speaker, a CDA's efficiency (η) is defined by the ratio between the power delivered to the load (P_{LOAD}) and the power drawn from the supply (P_{SUPPLY}):

$$\eta = \frac{P_{\mathrm{LOAD}}}{P_{\mathrm{SUPPLY}}} \times 100\%. \tag{1.1}$$

It is typically around, or above, 90% for a CDA.

1.2.3 Modulation Schemes

As mentioned above, the modulation scheme of a CDA maps the input audio signal into discrete voltage levels. To maintain high audio quality, it should introduce minimal noise and distortion in the audio band. To achieve this, pulse width modulation (PWM) and delta-sigma modulation (DSM) are commonly used.

1.2.3.1 PWM

PWM produces square-wave pulses whose duty cycle, and thus, whose low-frequency component, tracks the audio input. This can be implemented by comparing the input signal with a triangle wave (aka. a carrier) with a frequency of f_{SW} . This operation is known as natural sampling PWM [9] and is illustrated in Fig. 1.5(a). Fig. 1.5(b) shows the spectrum of V_{SW} , which consists of the input, PWM tones, and sidebands. As shown, natural sampling ideally does not introduce in-band distortion.

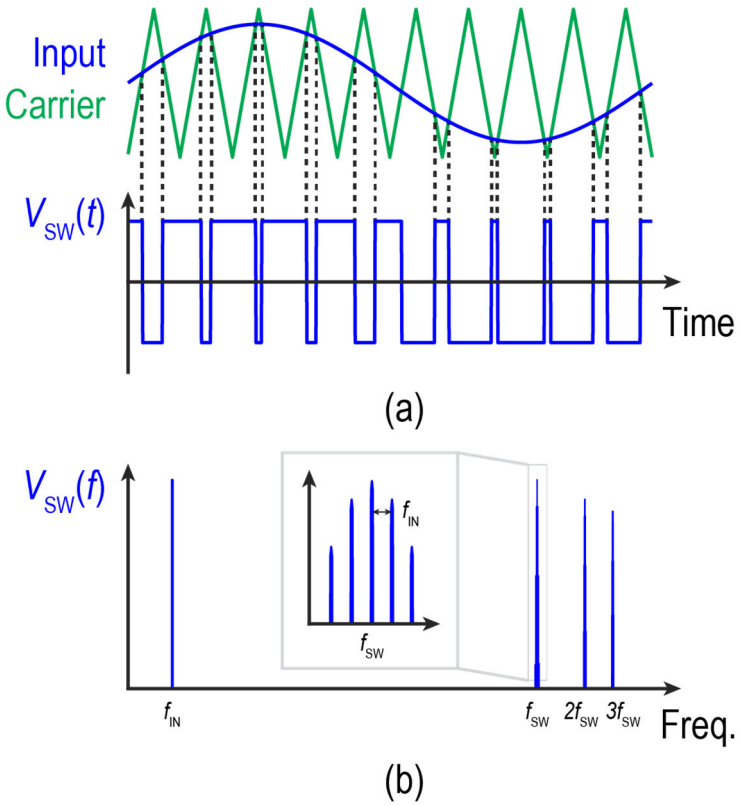

Fig. 1.5. (a) Timing diagram of natural sampling PWM, and (b) spectrum of V_{SW}.

In a BTL output stage, the two half-bridges can be configured to switch in a fully-differential fashion. This is known as the AD mode [Fig. 1.6(a)]. The output thus has no CM content at the switching frequency, which is beneficial for EMI (Section 1.3.1). Alternatively, the two half-bridges can be modulated separately using two triangle waves with opposite phases, which is known as the BD mode [Fig. 1.6(b)]. In this case, no current flows through the load for a zero input, reducing the idle power consumption. For the differential output, it also produces three output levels and doubles the effective PWM frequency. However, the output CM exhibits a rail-to-rail swing, which causes strong tones in the CM spectrum around the switching frequency and its harmonics.

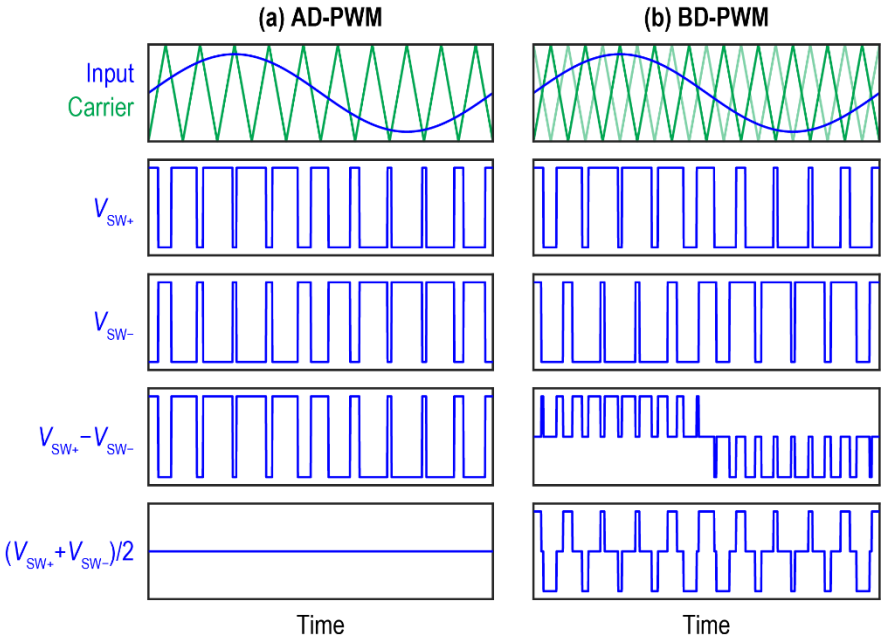

Fig. 1.6. Waveform of (a) AD and (b) BD PWM.

Apart from comparing an input signal with a triangle wave, PWM can also be implemented by a self-oscillating feedback loop based on internal hysteresis or delay [9], as shown in Fig. 1.7. However, the resulting switching frequency varies with the input signal, since the slew rate of the loop filter output is input-dependent, leading to an unpredictable EMI spectrum and potential crosstalk between channels [9], [17].

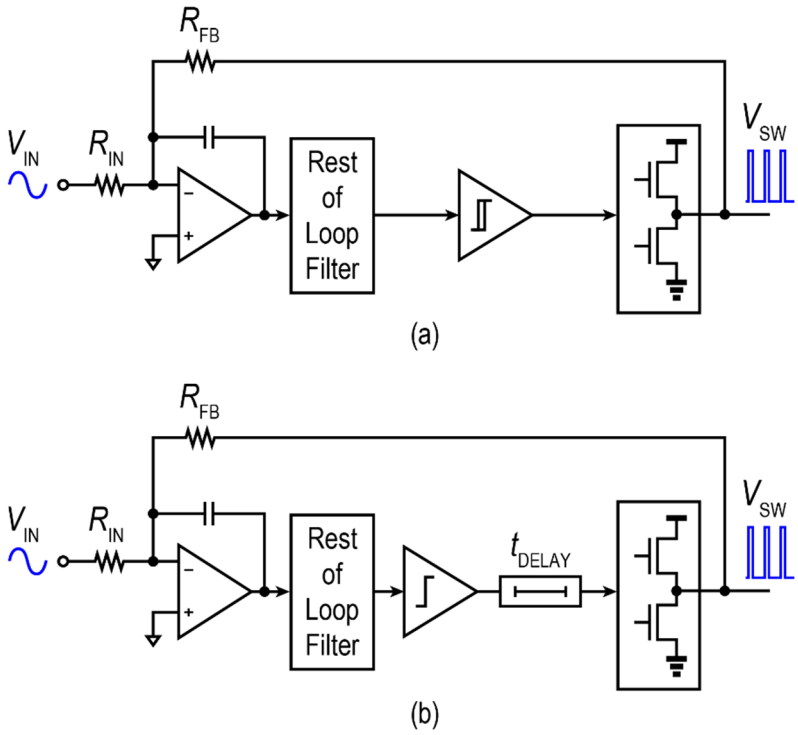

Fig. 1.7. Self-oscillating CDA based on (a) hysteresis and (b) delay.

1.2.3.2 Delta-Sigma Modulation (DSM)

DSM employs oversampling and noise shaping to realize discrete output levels while maintaining a high in-band SNR. Quantization noise is pushed out of the signal band, resulting in a wideband noise spectrum, as shown in Fig. 1.8, which spreads the EMI power and facilitates a filterless configuration [15], [16], [18]. Single-bit DSM is also known as pulse density modulation (PDM). For a BTL output stage, the two switching nodes can be controlled independently as in BD-PWM, resulting in the generation of three differential output levels with a single supply [18], which improves the SQNR.

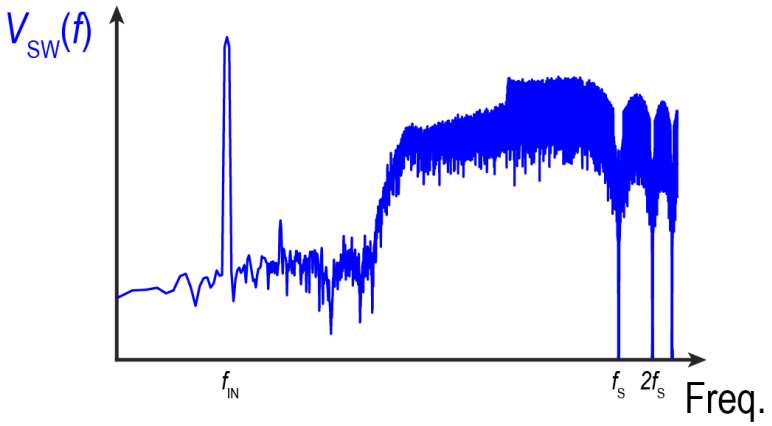

Fig. 1.8. Output spectrum of CDA based on DSM with an input tone at f_{IN} sampled at f_S.

Unfortunately, CDAs based on high-order PDM suffer from instability at large signal amplitudes, so they cannot produce the full output swing offered by the power supply. Dynamically reducing the loop filter order can keep the loop stable up to the full scale (FS) at the expense of lower SNR [15].

1.3 Challenges and Prior Art

1.3.1 EMI

High-frequency switching activities in the output stage are coupled into, and radiated by, the cable harness connecting the power supply, audio amplifiers, and speakers, which is known as radiated EMI. It is particularly problematic in automotive applications, which must comply with strict EMI standards (e.g., CISPR 25 Class 5 [19]). Fully differential switching is preferred to meet this requirement since EMI produced by the 2 output nodes will then partially cancel each other out [17], [20]. The residual EMI must then be suppressed by an LC filter at the output of the Class-D amplifier and/or shielding. Unfortunately, these solutions significantly increase system cost and bulk. In applications with low output power, short speaker cable, and relaxed EMI specifications (e.g., CISPR 32 Class B [21]), the LC filter can

be omitted, which is often referred to as the filterless configuration [18], [22], [23], [24], [25], [26].

Aside from radiated EMI, high-frequency components in the supply current due to the output transitions will cause power-supply ripple, which may interfere with other electronics sharing the same supply. This is known as conducted EMI, which can be mitigated by decoupling and filtering the supply along with careful PCB layout [27]. Another cause of high-frequency current, is the reverse recovery of the body diode. When it conducts, its pn-junction is filled with charge carriers, which are depleted when the diode is suddenly switched to reverse bias. This leads to current spikes in the supply and thus conducted EMI, which can be addressed by using an adaptive gate driver that avoids reverse recovery [28].

To mitigate EMI, multiphase [17] and multilevel output stages [16], [26], [29], [30], [31], [32], [33], [34], [35], [36], [37] have been proposed, as shown in Fig. 1.9.

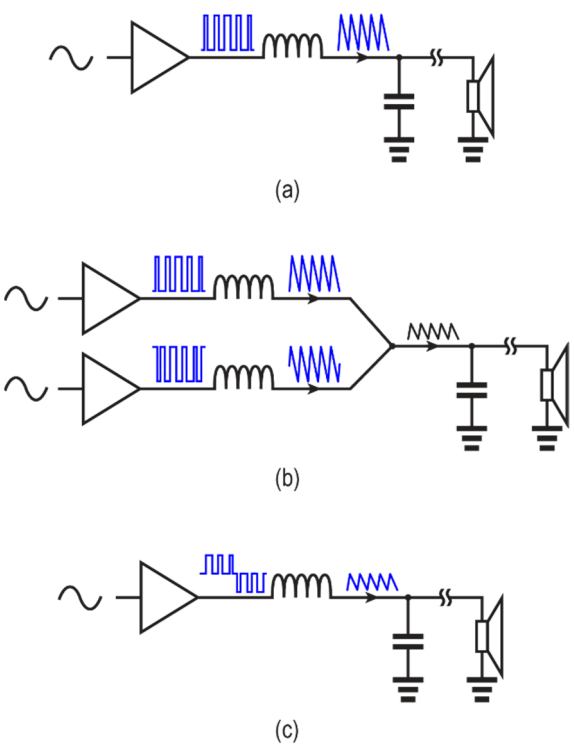

Fig. 1.9. Switching activity in (a) conventional, (b) multiphase, and (c) multilevel CDAs.

In multiphase output stages [17], several output stages drive separate inductors while switching at different moments [Fig. 1.9(b)]. Therefore, the total high-frequency ripple current delivered to the load is reduced, which reduces EMI. However, this increases the number of inductors required, as well as the idle power dissipation caused by the ripple currents circulating in the various output stages. As the number of audio channels increases, the total system cost and idle power dissipation increase proportionally.

Multilevel output stages [Fig. 1.9(c)] reduce EMI by reducing the switching step size. In [29], [30], [31], [32], [33], [34], this is achieved by using multiple supply voltages, which often increases system cost [Fig. 1.10(a)]. Alternatively, this can be done by using (relatively low-cost) external flying capacitors to generate an intermediate output level equal to a

fraction (usually ½) of the supply [35], [36], as shown in Fig. 1.10(b). However, extra control circuitry is then required to regulate the voltage across these capacitors to half of the supply, thus increasing design complexity. In [16], [26], an extra output level is created by simply shorting the load [Fig. 1.10(c)], but it requires zero or even negative dead time for proper operation, resulting in a complicated gate-driving configuration. In [37], independent control of the back-to-back transistors shorting the load is proposed, which obviates zero dead time. However, in both cases, extra circuitry and, thus, idle power is required to robustly define the output CM.

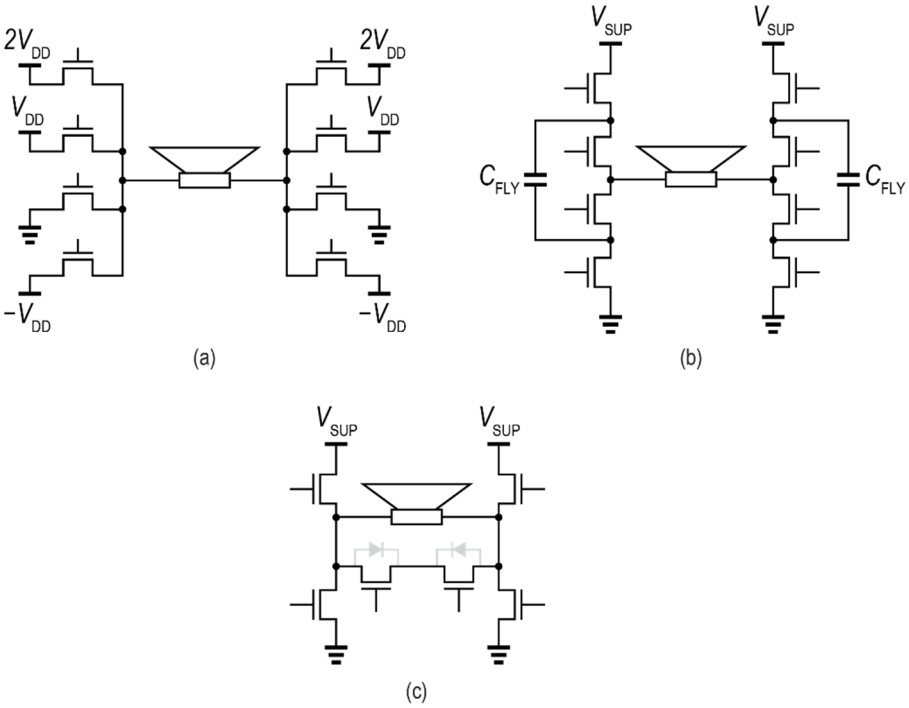

Fig. 1.10. Prior-art multi-level CDA output stages using (a) multiple supplies, (b) flying capacitor, and (c) switches shorting the load.

Another way to meet the EMI challenge is by tailoring it to the requirements of the CISPR 25 EMI mask. Class-D amplifiers employing fixed-frequency pulse-width modulation (PWM) [38] or a hybrid of PWM

and DSM [39] can do this by switching at frequencies above 1.8 MHz where the EMI requirements are relaxed. This also allows the size of the LC filter to be reduced. However, this results in increased switching loss and, hence, higher idle power. On the other hand, Class-D amplifiers employing DSM [15], [18], [34], [37] can reduce EMI peaks by spreading the switching energy, which is useful in consumer applications. However, even with sampling frequencies of several MHz, their out-of-band quantization noise may still fall within the AM band, especially near the lower end of 150 kHz. Hence, an LC filter with a cutoff frequency much lower than 150 kHz may be required, e.g., 41 kHz is used in [15].

1.3.2 Nonlinearity

Nonlinearity in a CDA distorts the signal of interest and should be minimized for optimal audio quality. There are several sources of nonlinearity in a CDA, which will be discussed in this section.

1.3.2.1 Output Stage

Signal-dependent timing errors in the switching of the output stage can introduce distortion. As shown in Fig. 1.2, depending on the direction of the load current, V_{SW} can either make its transition before the dead time (known as soft switching) or after the dead time (known as hard switching) [9], thus causing a signal-dependent delay. This can be mitigated using a “zero” dead time, provided that cross-conduction can be robustly avoided through appropriate sizing [40]. Errors in the pulse shape, due to, e.g., nonlinear on-resistance and the forward voltage drop during body diode conduction, also add extra distortion.

1.3.2.2 Loop Filter

To improve linearity, feedback can be applied around the output stage. Fig. 1.11 illustrates such a closed-loop CDA. Its output is sensed by the feedback resistors R_{FB}, whose distortion is then suppressed by using one or more integrators to realize high loop gain in the audio band. Higher loop gain can be achieved by increasing the unity gain frequency (f_U) of the feedback loop or the loop filter order. However, in constant-frequency PWM-based CDAs, f_U must stay below f_{PWM}/π to maintain correct PWM operation [7], [9] since the slew rate of the PWM modulator's input must be less than that of the triangle wave. Furthermore, residual ripple at the loop filter output, which contains PWM sidebands, can be demodulated back to the audio band by the PWM operation, thus limiting the linearity of closed-loop CDAs [41]. In [12], [13], [14], the PWM ripple is actively canceled to circumvent this limitation.

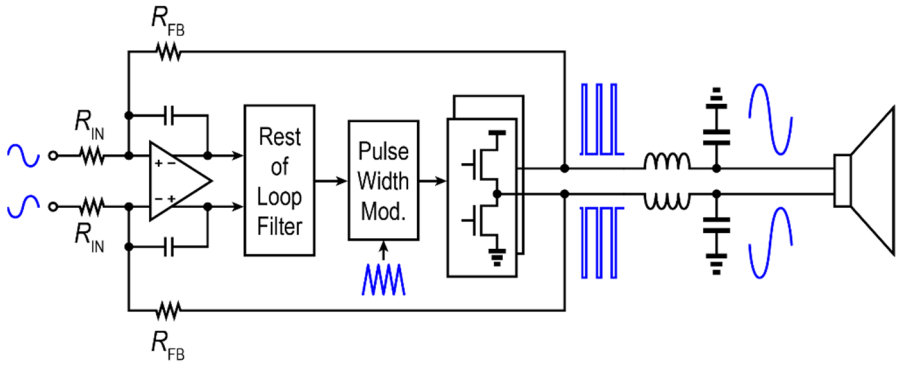

Fig. 1.11. Closed-loop constant-frequency PWM-based CDA.

The loop filter itself can also introduce distortion. The 1st integrator, which is the most critical for noise and distortion, must process the large current pulses coming through the feedback resistors, including PWM tones and sidebands, whose intermodulation products can fall into the audio band and lead to distortion. When using BD-PWM, the large CM swing [Fig. 1.6(b)]

modulates the CM level at the virtual ground of the 1st integrator, posing additional challenges for realizing a low-distortion loop filter.

1.3.2.3 LC Filter

As mentioned in Section 1.3.1, LC filters are often required to suppress EMI. However, practical inductors and capacitors exhibit bias (current and voltage) dependencies, respectively, that cause distortion. This bias dependence can be modeled as follows:

$$L(i_L) = L_0 + \Delta L(i_L) \qquad \text{and} \qquad C(v_C) = C_0 + \Delta C(v_C). \tag{1.2}$$

In (1.2), i_L and v_C are the inductor current and capacitor voltage, respectively; L_0 and C_0 are the nominal inductance and capacitance, respectively. Therefore, their I-V relations can be expressed as:

$$v_L(i_L) = L_0 \frac{di_L}{dt} + \underbrace{\Delta L(i_L)\frac{di_L}{dt}}_{v_{L,nonlinear}} \qquad \text{and} \qquad i_C(v_C) = C_0 \frac{dv_C}{dt} + \underbrace{\Delta C(v_C)\frac{dv_C}{dt}}_{i_{C,nonlinear}}. \tag{1.3}$$

Equation (1.3) shows that the inductor's current dependence can be modeled as a nonlinear voltage in series, which appears low-pass filtered at the LC filter output (Fig. 1.12). Similarly, the capacitor's voltage dependence can be modeled by a nonlinear current in parallel, which is band-pass filtered when V_{SW} is driven by a low-impedance source in the case of a CDA.

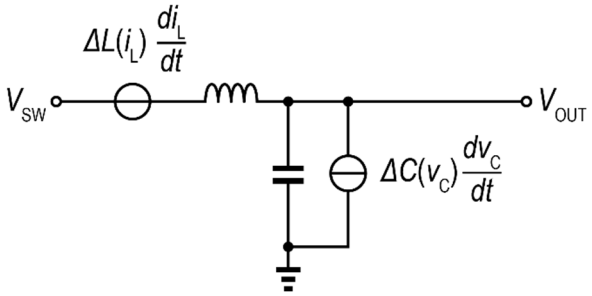

Fig. 1.12. Circuit model for LC filter nonlinearity.

Hence, in audio applications, the LC filter nonlinearity is dominated by the inductor's current dependence and, according to [10], can be estimated by:

$$\mathrm{THD_L} \approx \frac{f_{\mathrm{IN}}}{f_{\mathrm{LC}} Q} \cdot \frac{P_{\mathrm{OUT}}}{6 R_{\mathrm{L}} I_{\mathrm{SAT}}^2}, \tag{1.4}$$

where $f_{\mathrm{LC}} = (2\pi\sqrt{LC})^{-1}$ is the LC filter's cutoff frequency and I_{SAT} is the inductor's saturation current.

From Equation (1.4), an I_{SAT} > 12 A would be required for a THD < −100 dB, while the maximum load current for a CDA with 14.4 V supply and 4-Ω load is only 3.6 A. To verify this, the linearity of LC filters realized with three different inductors (Bourns PQ2614BHA-100K, Würth 7443340330, Murata FDSD0420-H-3R3M=P3) has been measured and listed in Table 1.1. As shown, the use of inductors with a large footprint and high cost is still necessary to guarantee high linearity.

Table 1.1. Selected inductors for CDA application.

			
Dimension (mm)	28 x 20 x 16	8 x 8 x 7	4 x 4 x 2
I_{SAT}	100 A	19 A	3.7 A
THD*	-102 dB	-102 dB	-60 dB
Cost	$$$	$$	$

Source: Bourns, Würth, Murata
*Measured right before clipping across a 4-Ω load.

Feedback-after-LC architectures have been proposed to reduce the impact of LC filter nonlinearity [17], [42], [43], [44], [45], [46]. In such architectures, LC filter nonlinearity is suppressed by the amplifier's overall loop gain. However, implementing this is challenging because the LC filter introduces two additional complex poles into the amplifier's feedback path. Furthermore, practical inductors and capacitors have manufacturing tolerances, as well as bias (current and voltage) dependencies, leading to variations in f_{LC}. In [43], [44], [46], self-oscillating architectures that take advantage of the LC filter's poles have been employed. However, their PWM frequency is signal- and f_{LC}-dependent, leading to an unpredictable EMI spectrum, which restricts their use in EMI-sensitive applications.

In fixed-frequency PWM designs, zeros can be added to the loop filter to compensate for the LC filter's phase shift. However, with a single feedback path, the loop bandwidth (f_U) will be a function of f_{LC}. This limits the allowable f_{LC} tolerance because f_U should not exceed f_{PWM}/π in Class-D amplifiers with fixed-frequency PWM [7], [42]. In [42], the effect of capacitance variation is eliminated by using a current-mode inner loop but f_U still depends on the inductance, and the maximum modulation index is limited to 0.85. To mitigate this, a triple-feedback architecture (Fig. 1.13) is

proposed in [45], where a first feedback path around the output stage and before the LC filter desensitizes the loop bandwidth from f_{LC} variations. A second feedback path after the LC filter is then stabilized with the help of a Type-III compensator. Finally, an outer 1st order feedback path increases the suppression of LC filter nonlinearity. However, due to its limited loop filter order and a low f_{PWM} of 100 kHz, this design only achieves a modest (10 dB) suppression of LC filter nonlinearity at 20 kHz.

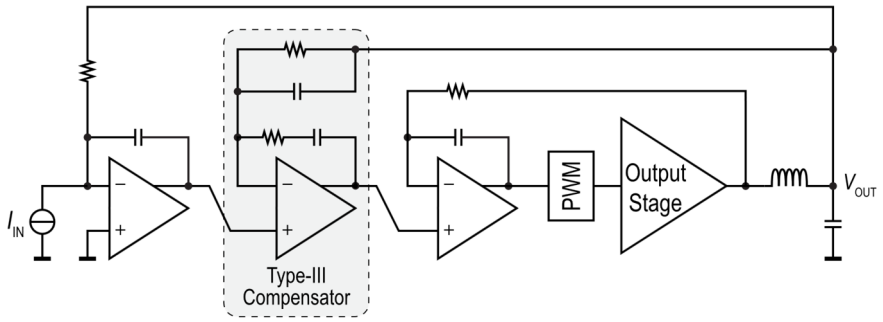

Fig. 1.13. The triple loop architecture of [45].

In [17], a digital feedback architecture is proposed in which a 5th-order digital loop filter provides 50 dB of loop gain around the LC filter at 20 kHz (Fig. 1.14). To maintain stability, the LC filter's poles are nominally canceled by an LC^{-1} filter implemented in the digital domain. This architecture requires a high-performance and low-latency ADC in the feedback path, significantly increasing its complexity. Furthermore, the mismatch between the external LC filter and the digital LC^{-1} filter compromises stability, which is exacerbated by its low loop bandwidth (100 kHz). As a result, the coefficients of the digital LC^{-1} filter have to be adjusted for a given LC filter, resulting in significantly increased application cost.

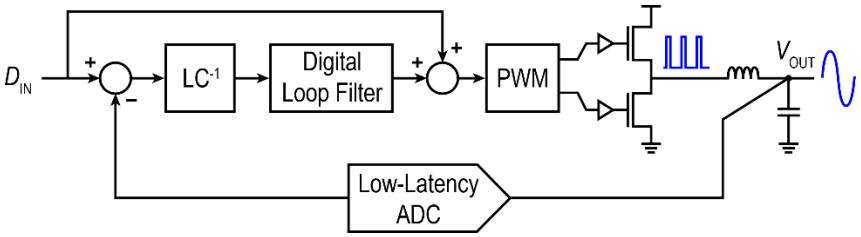

Fig. 1.14. Digital-input CDA with low-latency ADC feedback [17].

1.3.2.4 Digital-Input CDAs

Most audio sources nowadays are digital, so there is a growing trend towards CDAs with digital-inputs. Compared to a monolithic digital-input CDA solution, feeding the input of an analog-input CDA through a standalone DAC increases system size. It also makes the CDA more sensitive to RF interference [47]. Therefore, monolithic digital-input CDAs are preferred.

For a digital-input closed-loop CDA, an analog/digital interface is required so that the analog output can be fed back and compared against the digital input. If the comparison is performed in the analog domain, an upfront DAC will be required, whose noise and distortion will add to that of the CDA itself [16], [48], [49], as illustrated in Fig. 1.15(a).

Alternatively, an ADC can be employed to sense the CDA output, whose linearity will be limited by the internal feedback DAC of the ADC [17], [50], as shown in Fig. 1.15(b). In either case, therefore, the DAC's linearity is crucial to that of the CDA. Major distortion sources here are the unit-element mismatch and intersymbol interference (ISI) [51], [52], [53].

Single-bit PWM DACs [11], [47], [50], [54] do not suffer from unit-element mismatch because quantization is realized in the time domain. Since PWM is implemented in the digital domain, it also obviates the need for a triangle wave generator in the analog domain, further simplifying the design

[11]. However, since the signal is encoded into the pulse width, this type of DAC is more sensitive to clock jitter than a multi-bit DAC [55].

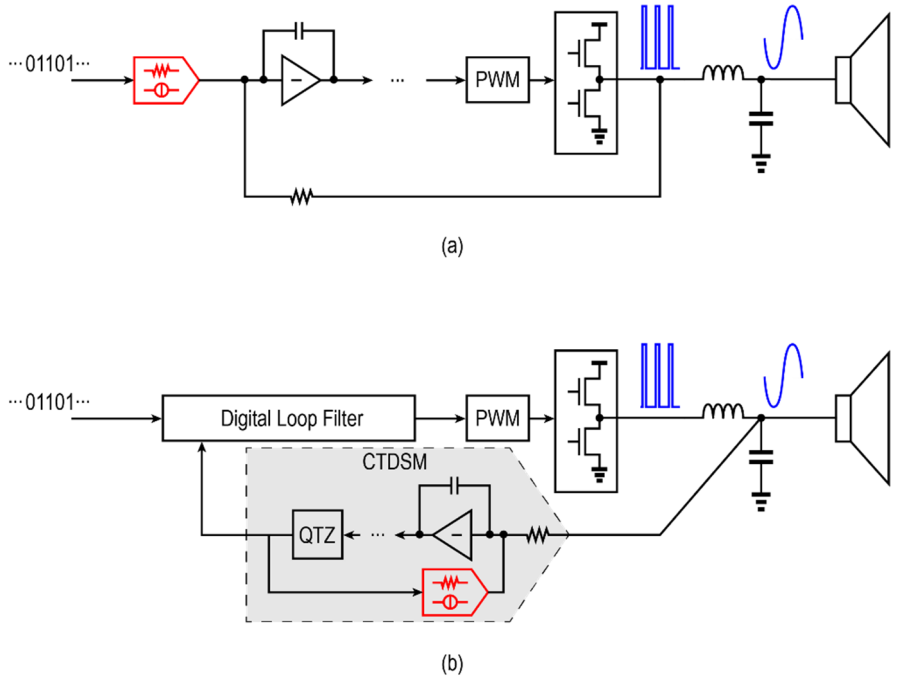

Fig. 1.15. Digital-input CDA architectures using: (a) upfront DAC [48] and (b) feedback ADC [17]. The main sources of distortion are highlighted in red.

1.3.3 Noise

The human ear has a high sensitivity, with a DR of above 120 dB [56], [57]. As mentioned in Section 1.1, audio drivers based on Class-AB amplifiers can achieve a DR higher than 120 dB. As will be discussed in the following, achieving a similar DR with a CDA is quite challenging.

1.3.3.1 Open-Loop CDAs

In an open-loop CDA, the main noise sources are the power supply and clock jitter. At small signal amplitudes, power supply noise appears mostly

as CM across the load and is thus suppressed [58]. On the other hand, clock jitter modulates the timing of output transitions and causes output noise as long as the CDA output keeps switching. The output noise due to the jitter is proportional to the transition step size and RMS value of the jitter (normalized to the switching frequency in the case of PWM [58] and quantizer sampling frequency in the case of DSM [59]).

In [58], an open-loop CDA with 120 dB of DR is reported, in which a digital input is first delta-sigma modulated and then directly used to control the duty cycle of an output stage. As such, its noise performance is limited by supply noise and clock jitter. To achieve the reported 120 dB dynamic range, an integrated clock jitter of less than 2 ps (rms) is required [58], which increases system cost. The open-loop architecture also leads to significant distortion at high power levels and poor power supply rejection.

In [54], the supply voltage is adaptively reduced at low power levels to reduce jitter sensitivity, while feedback is employed at high power levels to reduce distortion and improve supply rejection. However, the additional DC-DC converter required for supply scaling reduces power efficiency, whereas the amplitude-dependent use of resistive feedback causes significant noise floor modulation.

1.3.3.2 Closed-Loop CDAs

For closed-loop CDAs (Fig. 1.11), supply noise and clock jitter in the output stage are suppressed by the loop gain, while the feedback network and loop filter introduce additional noise. Here, the noise floor is typically limited by the thermal noise generated by the resistors that set the CDA's closed-loop gain (or by the resistive or current DAC in a digital-input architecture) and by the amplifier in the 1st stage of the loop filter. The contribution of the latter is usually low since a well-designed active-RC integrator typically satisfies

$g_M R_{IN} >> 1$, where R_{IN} is the integrator's input resistance and g_M is the amplifier's transconductance [51]. Furthermore, in addition to the resistor's thermal noise, the amplifier's flicker noise is also often significant.

To lower the thermal noise floor, R_{IN} must be reduced, and therefore, a larger integration capacitor will be required in the 1st integrator, since the unity-gain frequency of the loop (f_U) is limited by the switching frequency, as mentioned in Section 1.3.2.2. In contrast, Class-AB amplifiers do not suffer from this limitation, allowing the use of f_U 's above 10 MHz [60].

Due to the abovementioned limitations, the dynamic range of conventional monolithic Class-D audio amplifiers is lower than that of their Class-AB counterparts, around 110 dB for analog-input designs [15], [35], [39], [61], [62] and up to about 115 dB for digital-input designs [16], [17], [48], [49].

1.3.4 Power Supply Rejection Ratio (PSRR)

Since the CDA's output transistors operate as switches, supply noise directly couples to the output. For an open-loop CDA, the supply is essentially multiplied by the ideal output waveform. Hence, the rejection of power supply noise depends on the input level, the modulation scheme (e.g., AD vs. BD), and whether an SE or BTL output stage is used. As mentioned in Section 1.3.3, supply noise appears as CM in a BTL configuration when there is no input. However, the PSRR significantly decreases for large input signals and approaches only 3 dB for a full-scale input [58].

For closed-loop CDAs, on the other hand, supply noise at the output is suppressed by the loop gain. Nevertheless, mismatches in the feedback network can cause CM-to-differential leakage and limit the PSRR. Therefore, the PSRR can be improved by regulating the output CM with a CMFB loop

[17], [63]. Digital-input CDAs employing a current DAC also exhibit high PSRR if there is no CM voltage drop across the feedback resistors [16].

1.4 Thesis Goal and Organization

As introduced in Section 1.1, CDAs suffer from greater EMI, inferior linearity, and lower DR than Class-AB amplifiers. Since most audio sources are digital, Table 1.2 summarizes and compares the performance of state-of-the-art digital-input audio drivers at the start of the research described in this thesis. As shown, the THD+N of CDAs is significantly higher than those of Class-AB amplifiers, and few CDAs satisfy the stringent automotive EMI standard of CISPR 25 Class 5 EMI. Although EMI can be improved by advanced PCB layout with extra supply decoupling, filtering, and shielding [64], these mitigation techniques inevitably increase the application cost. Given the necessity for high power efficiency in high-power applications, CDAs with small LC filters are desired to achieve an overall form factor close to that of Class-AB solutions [65].

Table 1.2. Comparison between state-of-the-art Class-AB and Class-D amplifiers.

	TI PCM1794A + TPA6120A2	S.-H. Wen [4] ISSCC'19	E. Cope [49] ISSCC'18	D. Schinkel [17] JSSC'17
Monolithic	No	Yes	Yes	Yes
Amp. Class	Class-AB	Class-AB	Class-D	Class-D
THD+N	−107 dB	−105 dB	−97 dB	−89 dB
DR	>120 dB	120 dB	115.5 dB	115 dB
PSRR (Freq./Hz)	75 dB (N.A.)	-	80 dB ~ 50 dB (20 ~ 20k)	88 dB ~ 60 dB (100 ~ 20k)
$P_{OUT,MAX}$	0.7 W	62 mW	20 W	80 W
Efficiency	-	-	90%	>90%
I_Q	70 mA	3.8 mA	20.5 mA	-
EMI	No	No	Yes	Yes
f_{LC}	No	No	Not reported	~40 kHz

In view of the abovementioned limitation of CDAs, this thesis describes the design and implementation of CDAs that aim to approach the performance

of Class-AB amplifiers in terms of their application cost (mainly for suppressing EMI), dynamic range, and linearity while retaining the characteristic high power efficiency of the CDA.

Chapter 2 presents a CDA with a 4.2 MHz constant-CM multi-level output stage that reduces the radiated EMI, a major issue in automotive applications, thus relaxing the requirements on its LC filter and reducing its size and cost. However, the filter must still be highly linear, which limits further cost and size reductions. To address this issue, **Chapter 3** describes a dual-loop architecture featuring feedback after the LC filter, thus suppressing its nonlinearity and ensuring that it no longer limits the linearity of the CDA. In this architecture, switching components in the feedback signal are also attenuated, enabling the implementation of the capacitively-coupled chopper CDA described in **Chapter 4**, which breaks the dynamic range limitation of conventional CDAs by obviating the need for noisy input resistors. **Chapter 5** extends this architecture to a digital-input CDA and presents design considerations to mitigate distortion due to DAC nonidealities and intermodulation. **Chapter 6** concludes this thesis and discusses potential directions for future works.

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Chapter 2 A −107.8 dB THD+N Low-EMI Multi-Level Class-D Audio Amplifier[1]

2.1 Introduction

As mentioned in Chapter 1, the EMI of CDAs typically has to be suppressed by a bulky LC filter to avoid interfering with AM radios, especially in automotive applications, which have stringent EMI requirements. Setting the PWM frequency above the AM band (150 kHz ~ 300 kHz and 530 kHz ~ 1.8 MHz) allows for a smaller LC filter at the expense of higher idle power [1], [2]. This chapter presents a CDA with a multi-level Class-D output stage. The modulation scheme establishes a fixed output CM voltage, which helps to reduce EMI since the emissions from the pair of output wires partially cancel each other out [3]. In [3], however, a negative dead time was required to ensure correct operation, increasing the gate driver's complexity, and its output CM was defined by a power-hungry resistive divider even with duty-cycling. Moreover, the second and third harmonics of its 500 kHz switching frequency fall within the AM band. As mentioned in Section 1.3.1, several other topologies realizing a multilevel output have been reported [4], [5], [6], [7], [8], [9], [10], [11], which requires external flying capacitors or supply voltages at the expense of a higher application cost.

In this work, an alternative topology is proposed, which does not require a complicated gate driver, power-hungry CM regulation circuitry, or flying capacitors. With a switching frequency of 4.2 MHz, the required LC filter

[1] This chapter is based on the journal paper: H. Zhang *et al*., "A High-Linearity and Low-EMI Multilevel Class-D Amplifier," *IEEE J. Solid-State Circuits*, vol. 56, no. 4, pp. 1176-1185, Apr. 2021.

cutoff frequency is significantly increased. Meanwhile, the increased idle power due to the high switching frequency is mitigated by a modulation scheme that has minimal switching activity during idling and a gate-charge reuse technique.

This chapter is organized as follows. Section 2.2 explains the proposed output stage architecture and modulation scheme. Section 2.3 describes the output stage's circuit implementation. Section 2.4 details the design of the prototype's signal-processing circuitry, including the loop filter and the pulse width modulator. Section 2.4 presents the measurement results, and Section 4.5 summarizes and concludes the chapter.

2.2 Proposed Output Stage

2.2.1 Topology

Fig. 2.1 shows the proposed fully differential multilevel output stage for a bridge-tied-load (BTL) [12]. Four CM output transistors (M1-M4) are added to the conventional H-bridge (M5-M8). A low-power linear regulator generates a voltage PVCM equal to half of PVDD. The output stage then produces three differential output levels ($V_{\mathrm{OUTP}} - V_{\mathrm{OUTN}}$): +PVDD, −PVDD, and 0 in States 1, 2, and 3, respectively.

In State 1, M5, M8, M2, and M4 are turned on; in State 2, M6, M7, M1, and M3 conducts; and in State 3, M1-M4 are switched on. The output CM in all states is maintained at 1/2 PVDD, effectively reducing CM EMI, which is worse than DM EMI since the two output cables' emissions add in phase. The output stage switches between either State 1 and State 3, or State 2 and State 3. During the brief transition between State 1 and State 3, only M2 and M4 are on, and the body diodes of M1 and M3 provide a path for the inductor current to continue flowing. Similarly, the body diodes of M2 and M4 provide a path

for the inductor current during the transition between State 2 and State 3. Compared to [3], the proposed multilevel output stage does not require complex circuitry to avoid both dead time and cross-conduction. In contrast to [10], no complicated capacitor charge balancing circuitry is needed since, in State 3, the signal current only circulates within M1-M4. Thus, no signal current is drawn from PVCM, which can be maintained by a low-power linear regulator. Note that while idling, the output stage is mostly in State 3, which significantly reduces idle power.

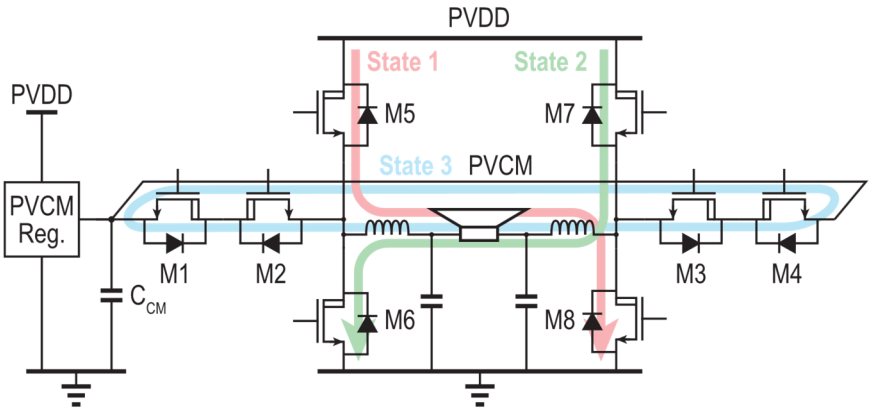

Fig. 2.1. Circuit topology of the proposed multilevel output stage.

Introducing the extra output level reduces the output step size by half compared to traditional two-level PWM modulation, leading to significant EMI reduction. Although it is rather difficult to predict EMI by simulations, the ripple current injected into the load provides a relevant indication. With the same inductor, Fig. 2.2 compares the peak-to-peak output ripple current of a conventional two-level AD mode output stage and that of the proposed multilevel output stage. The conventional output stage generates the most ripple when there is no audio signal, while the proposed output stage produces the least in this situation, with a 2x lower peak amplitude, which is reached at half full-scale. As a result, the proposed output stage should have significantly better EMI performance since most audio signals have a high crest factor.

2.2.2 Modulation Scheme

As mentioned in Section 1.2.3.1, fixed-frequency PWM creates tones at well-defined frequencies in the EMI spectrum, which can be placed above the AM band (150 kHz to 1.8 MHz). Although the CISPR 25 standard does not specify the maximum EMI between 1.8 MHz and 5.9 MHz, a certain limit might still be imposed by the application. Hence, this work employs fixed-frequency PWM switching at 4.2 MHz. For the same amount of attenuation, this allows the LC filter cutoff frequency to be 2x higher than that used in [1], [2], where f_{PWM} was set to 2 MHz. While a f_{PWM} of 4.2 MHz is possible for a CDA employing conventional AD modulation as in [1], [2] in the chosen 180 nm BCD process, analysis shows that the high switching frequency will increase the idle power significantly.

Multilevel operation facilitates low idle power by reducing switching losses. In this work, the voltage step size on the parasitic capacitance C_{PAR} at the output nodes is reduced by half, while C_{PAR} itself is increased by less than 50% since, as will be discussed in Section 2.3.6, M1-M4 are sized smaller than M5-M7. Therefore, the switching loss due to output capacitance, which is proportional to $C_{\mathrm{PAR}}V^2 f_{\mathrm{PWM}}$, is reduced even when f_{PWM} is doubled. Gate charge loss for a small input is also reduced because the on-time of M5-M8 is too short for their V_{GS} to be fully charged; on the other hand, although the V_{GS}'s of M1-M4 are fully charged and discharged at f_{PWM}, they are sized smaller.

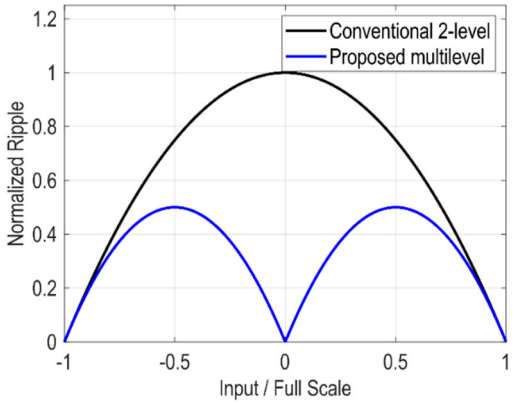

Fig. 2.2. Normalized peak-to-peak output ripple as a function of average output voltage for the proposed multilevel and conventional two-level output stages.

The proposed output stage generates three differential output voltages while the output CM stays at PVDD/2 to minimize CM EMI [3], [13]. To derive them, two triangular-wave carriers are employed, which are equal in amplitude but opposite in phase (Fig. 2.3), as in BD modulation (Section 1.2.3.1), since, differentially, both modulation schemes have three output levels. The loop filter output is then compared to the two triangular waves. When the input signal is above both carriers, the output stage switches to State 1, bringing the differential output to +PVDD; when the signal is between the two carriers, the output stage switches to State 3, creating a zero differential output; and when the signal is below both carriers, the output stage switches to State 2 to provide −PVDD. Since PWM pulses are now generated twice in each carrier cycle, a 2.1 MHz carrier frequency is used to operate the output stage at 4.2 MHz.

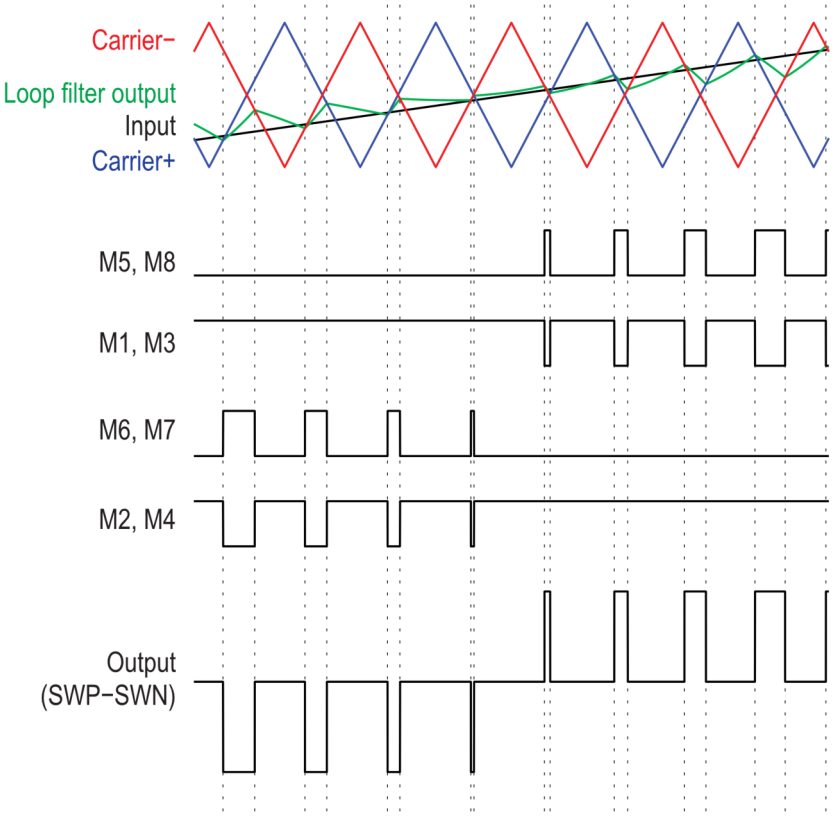

Fig. 2.3. Proposed modulation scheme, the resulting ON/OFF states of the output transistors, and differential output voltage.

2.3 Circuit Implementation

The proposed Class-D amplifier is implemented in a high-voltage BCD process, and its output stage is powered by a 14.4 V supply. To account for the extra voltage stress due to the supply ringing caused by off-chip parasitic inductances, the power transistors are all implemented as n-channel LDMOS transistors with 5 V gate oxide and a 20 V V_{DS} rating. This section describes the circuitry driving the output transistors and then discusses the design details of the gate-charge reuse technique, the power transistor driving

circuits, the sizing of the power transistors, and the implementation of the PVCM regulator.

2.3.1 Overview

As shown in Fig. 2.4(a), the output stage consists of 8 power transistors (M1–M8) and their respective driving circuits, an external capacitor C_{CM} to hold the mid-rail level, and a PVCM regulator to maintain the voltage on C_{CM}. Each output transistor is driven by a PWM signal generated by a 1.8 V PWM modulator (Section 2.4.2). This signal is then used to drive the transistor via a level shifter and a gate driver. The level shifter and the gate driver of each output transistor are powered by a floating regulator that provides a 5V local supply with respect to the source of each output transistor. M2, M3, M5, and M7 require local supplies above PVDD, which are obtained using external bootstrap capacitors C_{BSTP} and C_{BSTN} charged respectively through internal Schottky diodes D_{BSTP} and D_{BSTN}, as in [2], [14], [15], [16]. M2 and M5 (also M3 and M7) employ separate regulators to avoid crosstalk-induced timing errors due to voltage droop at the regulator outputs during gate charging. The gate drive for M1 and M4 is regulated from PVDD, while that for M6 and M8 is derived from PVCM. This configuration allows M6 and M8 to recycle the gate charge from M1 and M4 along with the bias current of their respective floating regulators, as will be explained further in Section 2.3.2. The PVCM regulator is a linear regulator which pre-charges C_{CM} during startup and maintains it at mid-rail during normal operation.

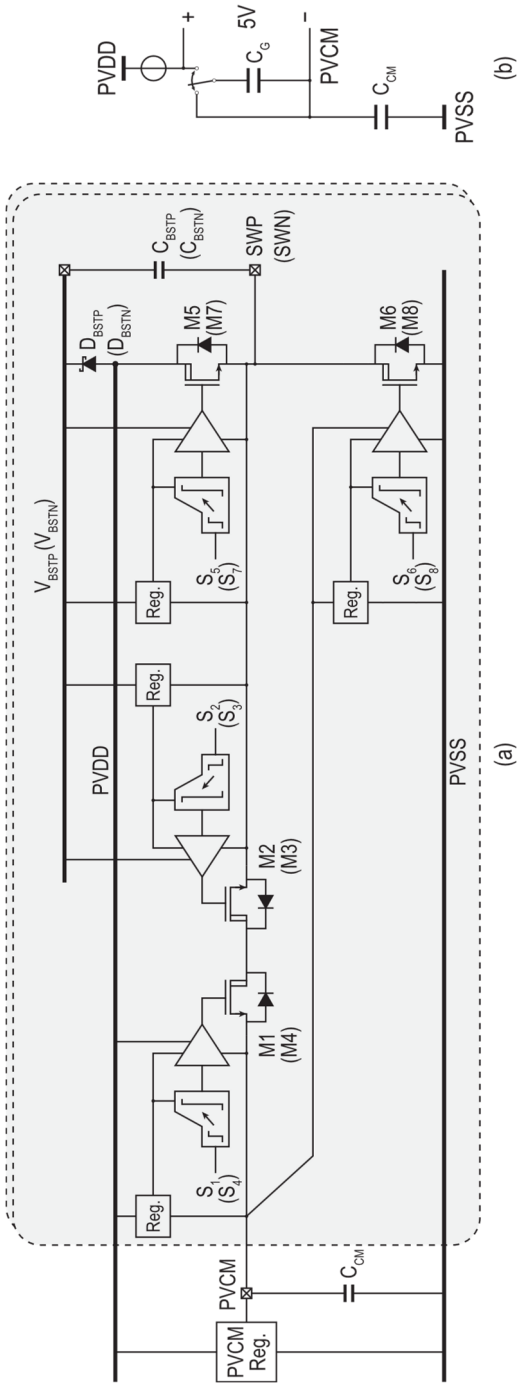

Fig. 2.4. (a) Simplified schematic of the output stage half circuit with floating regulators, level shifters, and gate drivers for the output transistors. (b) Equivalent circuit illustrating the charging of CCM by M1 and M4' s switching.

2.3.2 Gate Charge Reuse

When M1 and M4 are switched on, C_{CM} collects the current charging their gate-source capacitance. Effectively, the periodic charging and discharging of the gate-source capacitance of M1 and M4 create switched-capacitor resistors between PVDD and PVCM, charging C_{CM}. Fig. 2.4(b) shows the equivalent circuit. This charge is then reused for the gates of M6 and M8. The proposed gate-charge reuse scheme not only reduces the gate charging loss but also alleviates the loading on the PVCM regulator, which now only needs to supply the difference between the gate-charge currents of M6, M8, and M1, M4. According to simulations, the idle power would increase by 14 mW if the low-side gate driver's power was simply derived from PVDD.

2.3.3 Floating Regulator

Fig. 2.5(a) shows the schematic of the floating regulator, similar to that in [2]. A current reference I_{REF} is derived by imposing a reference voltage (1.25 V) across a resistor R_{REF}, whose copies are routed to each floating regulator. I_{REF} flows through a 4x larger resistor of the same type in each regulator to create a scaled reference voltage of 5 V with respect to V_{SSF} in the floating domain, which is then buffered by a class-AB source follower that supplies the level shifter and gate driver. The matching of resistors and current source devices guarantees sufficient accuracy of the output voltage [2].

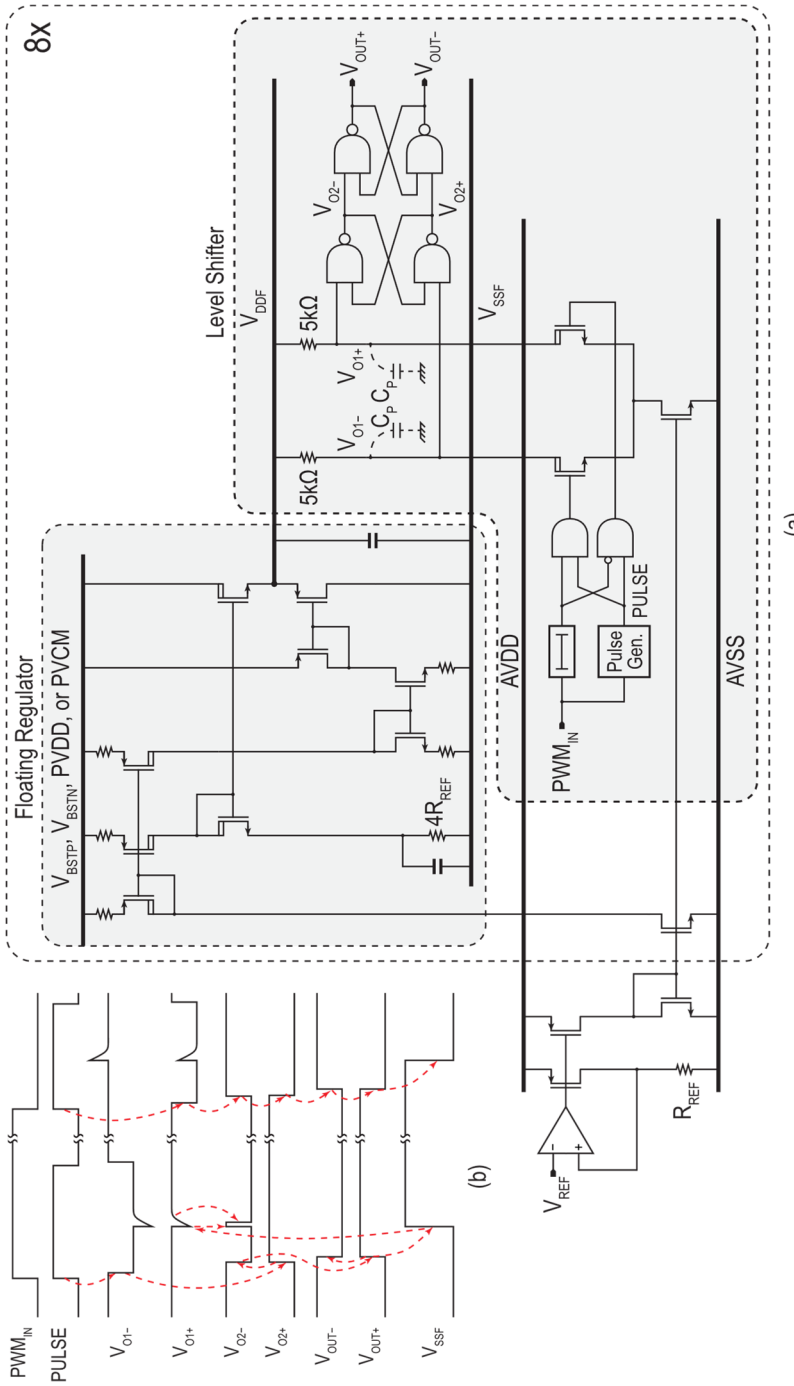

Fig. 2.5. (a) Design of floating voltage regulators and level shifters in the output stage, and (b) Transient waveform on internal nodes of the level shifter.

2.3.4 Level Shifter

Fig. 2.5(a) also shows the level shifter translating the PWM signal from the 1.8 V domain to the floating voltage domains. It consists of a resistor-loaded differential amplifier and a CM-immune two-stage NAND latch. During an output transition, one of the differential pair inputs is pulled high, creating a 5V voltage drop at the respective input of the floating-domain NAND latch, updating its output. The differential pair is only enabled momentarily by a pulse generator to reduce idle power. To avoid pulse width errors due to the pulse generator, a delay line before the AND gates at the input ensures that *PULSE* goes high before the input transition arrives at the differential pair. In the level shifters for M2, M3, M5, and M7, V_{SSF} switches to the new output level with a slew rate of several V/ns after a transition propagates to the output transistor. As shown in Fig. 2.5(b), displacement current through the parasitic capacitance at nodes $V_{\mathrm{O1+}}$ and $V_{\mathrm{O1-}}$ can pull them down and lead to glitches on $V_{\mathrm{O2+}}$ or $V_{\mathrm{O2-}}$. They are blocked by a second NAND latch, and thus, the level shifter output remains constant and correct during the slewing of V_{SSF}. The input pulse is designed to extend beyond the V_{SSF} transition so that the first latch's output is restored after the transition. The pulse generators in all 8 level shifters trigger during each output transition to guarantee the outputs of the 4 level shifters not switching (Fig. 2.3) are not accidentally flipped due to switching noise and bondwire ringing on nodes SWP and SWN.

2.3.5 Gate Driver

Fig. 2.6 shows the gate driver design, which buffers the level shifter output and drives the output transistors. To reduce loading on the floating regulator, most of the gate charge is drawn from the floating regulator's input directly using a source follower $\mathrm{M_{N1}}$ [2], [16]. In the last stage, the pull-down strength

is chosen to be larger than the pull-up strength to avoid cross-conduction and to allow minimal dead time, which reduces the output stage distortion [15].

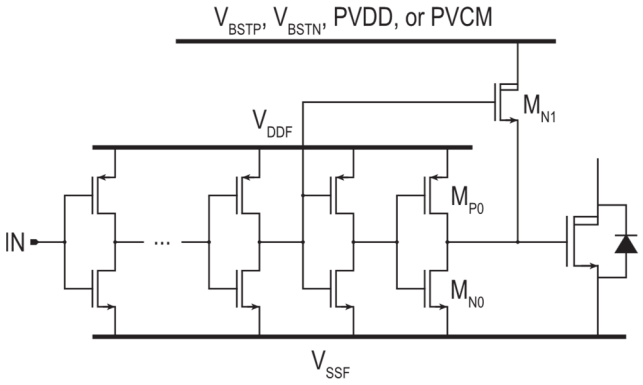

Fig. 2.6. Implementation of the gate driver.

2.3.6 Output Transistor Sizing

Multilevel output stages require additional output transistors that can drastically increase the overall area [3], [4], [6], [10]. At first sight, the on-resistance of M1-M4 should be 2x lower than that of M5-M8, such that the resistance between the output and any of the supply rails (PVDD, PVCM, and PVSS) would be the same. With the same type of transistor used, M1-M4 will occupy a 2x larger area compared to M5-M8. This is mitigated in the proposed output stage architecture. The ON duty cycle of the CM switches (M1-M4) is given by $(1-|V_{IN}|/V_{IN,FS})$, where $V_{IN,FS}$ is the input full scale and V_{IN} is the differential input voltage between $\pm V_{IN,FS}$. Therefore, at high output power, as $|V_{IN}|$ approaches $V_{IN,FS}$, the on-time of M1-M4 approaches zero. Fig. 2.7 shows the conduction loss as a function of relative sizing of M1-M4 and M5-M8 when the amplifier delivers a 10% THD clipped sine wave, representing the worst-case for conduction loss and thermal dissipation. For a certain area budget, the conduction loss is minimized when M5-M8 occupy

60% of the total output transistor area. In this paper, the $R_{DS(ON)}$ of M1-M4 is 210 mΩ, and that of M5-M8 is 140 mΩ.

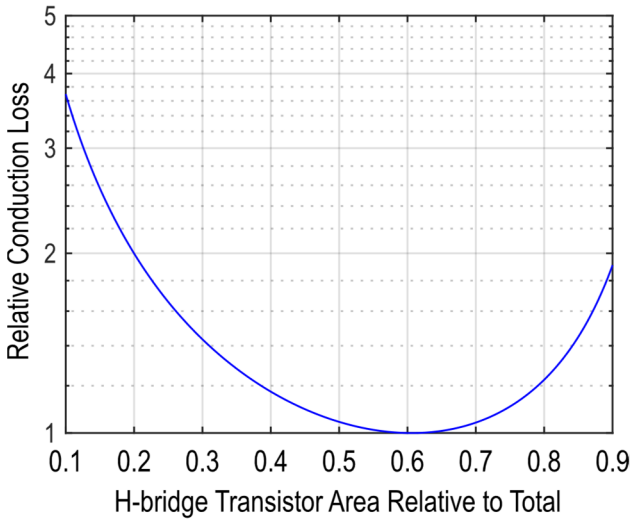

Fig. 2.7. Conduction loss as a function of the area allocated for H-bridge transistors M5-M8 in the output stage when the amplifier delivers a 10%-THD clipped sine wave.

2.3.7 PVCM Regulator

As mentioned in Section 2.2, the PVCM regulator does not supply the load current. However, since M1 and M4 are sized differently from M6 and M8, the regulator must compensate for the difference between their gate charge, which is also signal-dependent. When the duty cycle of M1 and M4 is almost 100%, and the on-time of M6 and M8 is smaller than their gate voltages' rise time, a net current flows into PVCM. On the other hand, when the signal is large and since M1 and M4 have a smaller gate area, their gate charge is not enough to fully charge the gates of M6 and M8, and a net current flowing out of PVCM is required. To stabilize PVCM, the regulator uses a class-AB follower output stage to both source and sink current. Fig. 2.8 shows its implementation, where a resistor divider creates a mid-rail reference voltage,

which drives PVCM through a unity-gain buffer. It only draws 0.5 mA of quiescent current from PVDD.

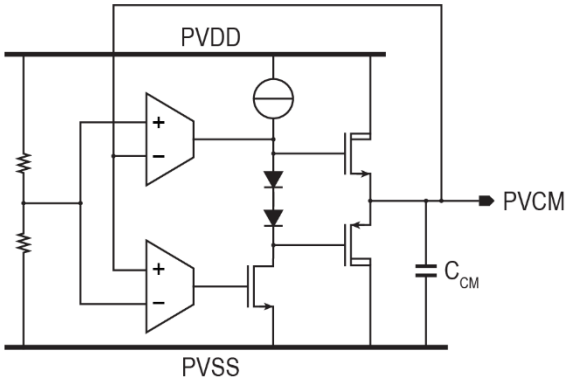

Fig. 2.8. Implementation of the PVCM regulator.

2.4 Prototype Closed-Loop Class-D Amplifier

In closed-loop Class-D amplifiers, distortion in the output stage is suppressed by the loop gain, while noise and distortion introduced in the loop filter directly impact the overall performance. Therefore, the performance of the loop filter and the pulse width modulator is of critical importance. This section presents the design considerations and implementation details of the loop filter and the multilevel pulse width modulator.

2.4.1 Loop Filter

For Class-D amplifiers using fixed-frequency PWM, the maximum allowable bandwidth for stable operation is given by f_{SW}/π, which ensures that the slope of the modulator's input signal is always less than that of the modulating triangular waveform [17]. A loop bandwidth of 800 kHz is chosen to allow for sufficient stability margin, while a 3rd-order loop filter guarantees sufficient loop gain in the audio band. Fig. 2.9 shows a simplified schematic of the loop filter, where active-RC integrators employing polysilicon resistors

and metal-insulator-metal (MIM) capacitors are used for their superior linearity. The integration capacitors are built with switchable banks to compensate for the process variation of the RC time constant. A resonance at around 15 kHz is realized by local feedback through R_{RES} around the 2nd and 3rd integrators to boost the loop gain in the audio band to above 82 dB [18]. Extra input feed-ins into the 2nd and 3rd integrators via R_{FF1} and R_{FF2} guarantee low swing at the output of the first two integrators and improve their linearity. In particular, the 1st integrator processes the difference between the input and feedback signals. The feedback signal contains significant high-frequency components, including the PWM tones, sidebands, and their harmonics. Nonlinearity in the amplifier A1 results in intermodulation among these components, which is directly added to the input and leads to in-band distortion.

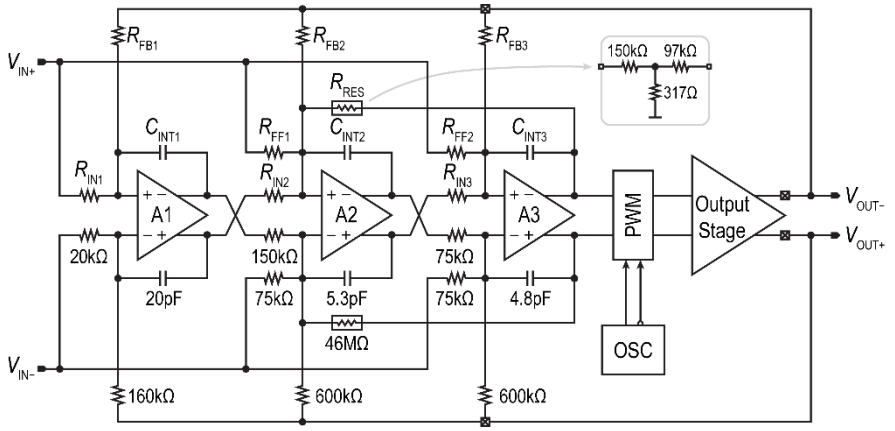

Fig. 2.9. Block diagram of the closed-loop Class-D amplifier.

To mitigate this effect, a two-stage feedforward-compensated OTA instead of a conventional two-stage Miller-compensated OTA is employed, as shown in Fig. 2.10. Feedforward compensation is implemented by ac-coupling the inputs to M_{N3} and M_{N4} in the second stage [2]. This allows for 14 dB of extra gain at the switching frequency to suppress the intermodulation distortion

compared to a conventional Miller-compensated OTA without increasing the power consumption.

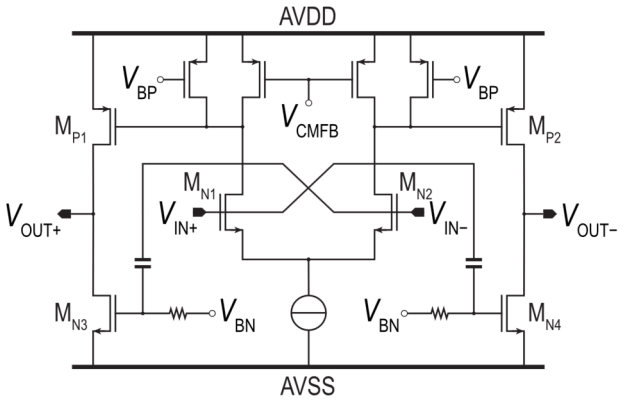

Fig. 2.10. The two-stage feedforward compensated OTA used in the loop filter.

2.4.2 Pulse Width Modulator

As described in Section II, multilevel PWM is realized by comparing the loop filter output with two equal but opposite triangle waves. They are generated by the fully differential oscillator shown in Fig. 2.11, built around a fully differential OTA. When the absolute value of its differential output exceeds $(V_{REFP} - V_{REFN})$, one of the comparators toggles, reversing the polarity of integration using a chopper. The resulting triangle carrier frequency is proportional to $1/(R_{REF}C_{INT})$. C_{INT} is made of trimmable banks to compensate for the process variation of the RC time constant so that the oscillator operates near 2.1 MHz. The same trim codes are then applied to the loop filter to center its transfer function. In the prototype, V_{REF} is provided externally to fine-tune the oscillator to 2.1 MHz.

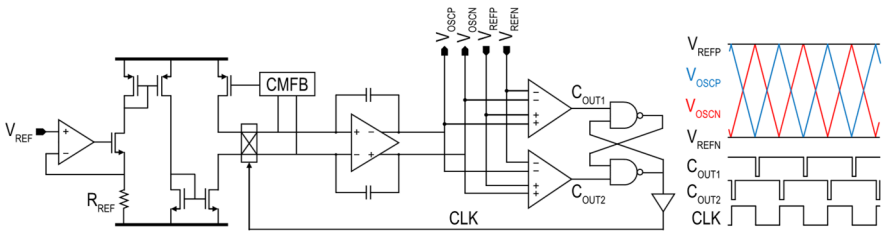

Fig. 2.11. Fully differential oscillator for carrier generation.

The loop filter output ($V_{INT3P} - V_{INT3N}$) is compared with the two triangle waves ($V_{OSCP} - V_{OSCN}$) and ($V_{OSCN} - V_{OSCP}$) using two dual-difference comparators, as shown in Fig. 2.12. To avoid pulse width errors due to parasitic loading by the comparator, the two differential inputs are combined using an all-pass passive network. The fully differential operation offers robustness against CM noise and mismatch (e.g., substrate noise) between the carrier and input compared to single-ended implementations [4], [19], [20]. Here, as in other time-interleaved systems, the mismatch between the two comparators and imbalances in the differential triangle wave result in a residual spur in the spectrum at the carrier frequency (2.1 MHz), which is still above the AM band where the EMI limit is relaxed. The comparator outputs are processed by combinational logic to derive the gate control for each output transistor.

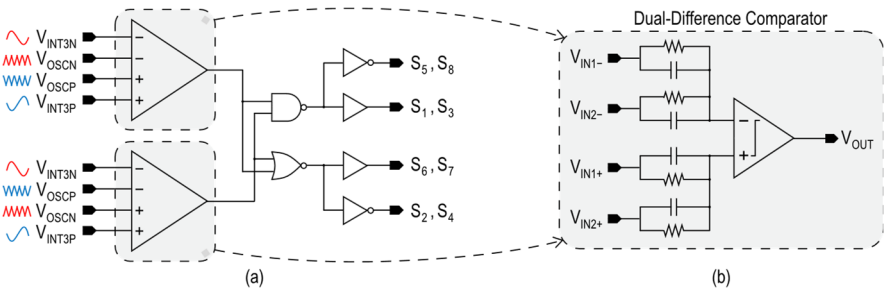

Fig. 2.12. (a) Fully differential multilevel pulse width modulator and (b) Dual difference comparator in oscillator and pulse width modulator.

2.5 Measurement Results

A test chip of the proposed design is fabricated in a 180 nm BCD process and occupies an area of 5 mm^2. Fig. 2.13 shows the die micrograph. The test die is directly mounted and wire-bonded on a test PCB with output stage decoupling capacitors nearby to reduce the loop area of the high-frequency current in the output stage, reducing the ringing and EMI associated with parasitic inductance.

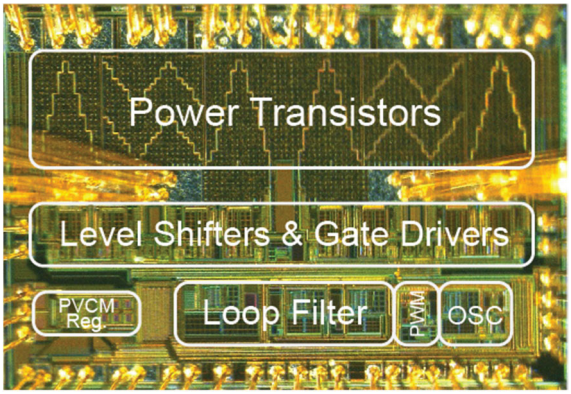

Fig. 2.13. Die micrograph.

Fig. 2.14 shows the measured output waveform during a zero crossing of the differential input signal. When the input crosses zero, there is almost no switching. This feature is beneficial for achieving a low idle power of 94 mW, of which about half is consumed as quiescent current in the floating regulators, while the other half is due to the occasional switching of the output stage driven by noise present at the loop filter output.

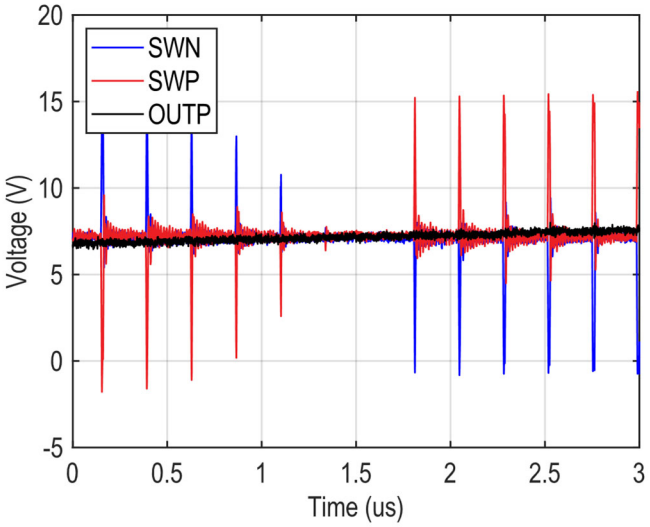

Fig. 2.14. The measured output voltage of the Class-D amplifier before the LC filter (SWP, SWN) and after the LC filter (OUTP).

Audio performance is measured by an Audio Precision APx555 signal source and analyzer connected to the output of the LC filter, which has a cutoff frequency of 580 kHz (L = 470 nH, C = 160 nF). The measured audio band spectrum when the chip delivers 1W into an 8-Ω load is shown in Fig. 2.15. The measured THD+N is −99.7 dB.

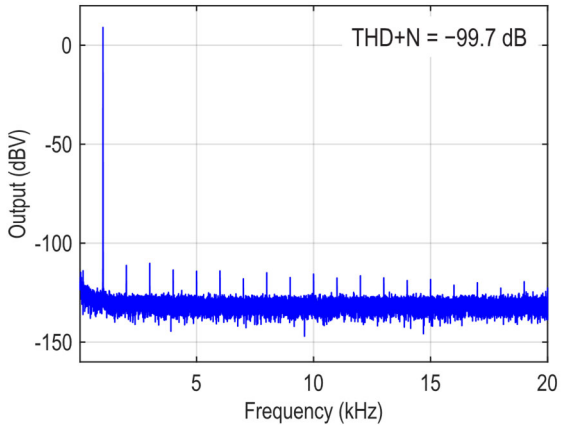

Fig. 2.15. Measured audio band spectrum when the prototype drives a 1W sine wave into an 8-Ω load.

Fig. 2.16 shows the THD+N performance as a function of output power, where the lowest levels are achieved when the signal is near full scale. For an 8-Ω/4-Ω load, the lowest level achieved is −107.8 dB and −102.6 dB, respectively.

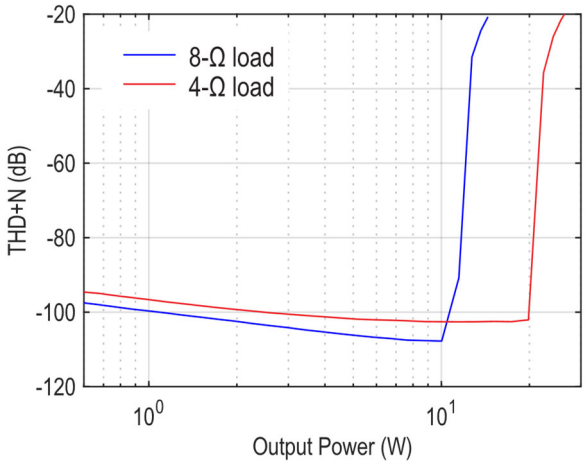

Fig. 2.16. Measured THD+N of the prototype across output power.

The measured peak efficiency is 91% for an 8-Ω load and 87% for a 4-Ω load, as shown in Fig. 2.17.

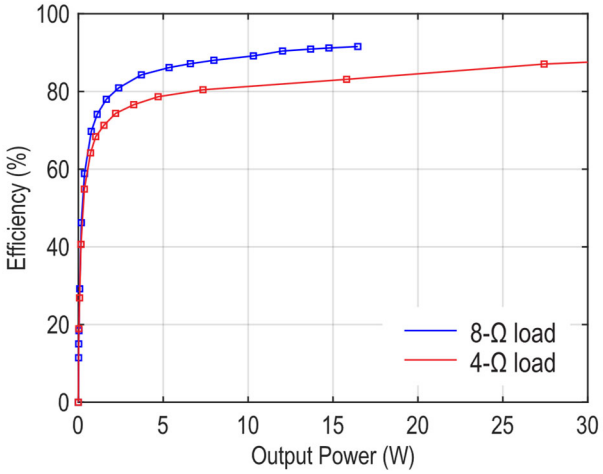

Fig. 2.17. Measured power efficiency at different output power.

According to the CISPR 25 standard, radiated EMI measurements were performed in an anechoic chamber, where a monopole antenna was used for 150 kHz to 30 MHz, a biconical antenna for 30 MHz to 200 MHz, and a log-periodic antenna for 200 MHz to 1 GHz. Fig. 2.18 shows the measured level of radiated EMI from 150 kHz to 1 GHz when the prototype drives 12 W into a 4-Ω load. The prototype meets the Class 5 limit for both peak and average radiated emissions with a 5.7 dB margin.

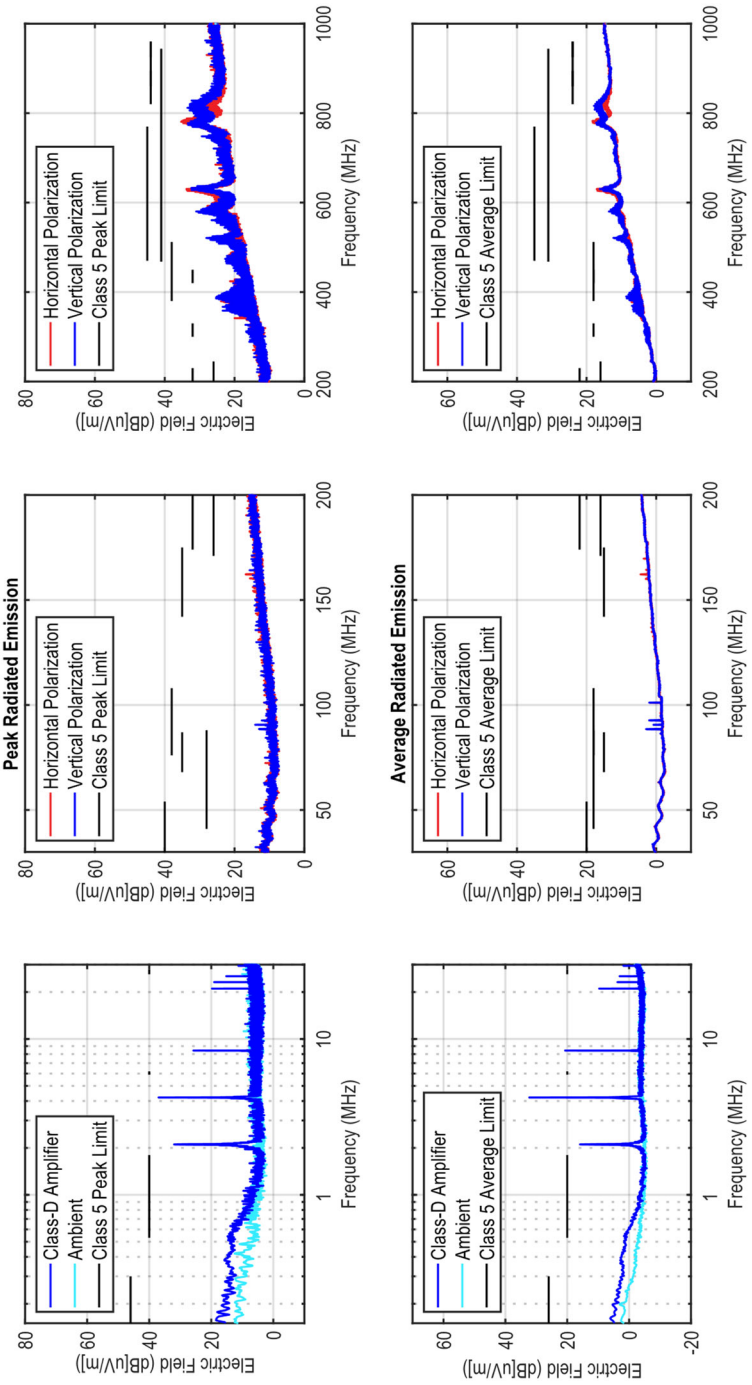

Fig. 2.18. Measured peak and average radiated EMI according to CISPR 25 standard from 150 kHz to 1 GHz.

As a comparison, Fig. 2.19 plots the AM-band EMI spectrum when the CDA is configured to perform AD modulation at 2.1 MHz. The average radiated emission at 2.1 MHz is 28 dB higher, while that at 4.2 MHz is only 2 dB lower, compared to Fig. 2.18.

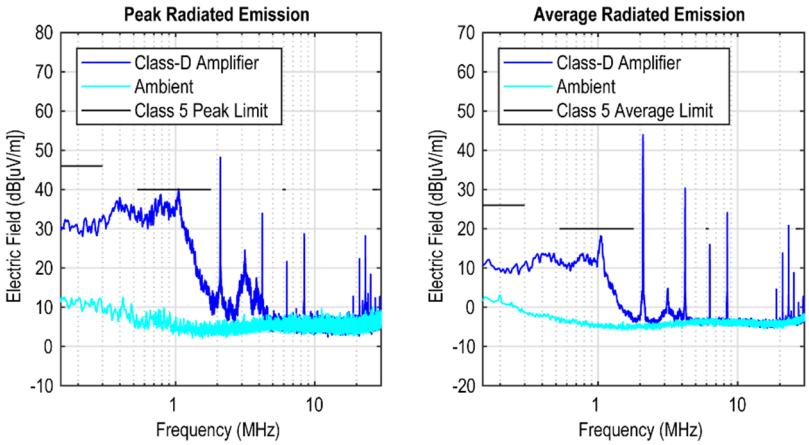

Fig. 2.19. AM-band EMI of the CDA when it outputs 12 W in 2-level AD mode.

Table 2.1 presents a performance summary of the proposed multilevel Class-D amplifier and compares it with other state-of-the-art designs. Thanks to the multilevel operation and high switching frequency, it satisfies the CISPR 25 Class 5 EMI limit while employing a much higher LC filter cutoff frequency (and thus smaller components) compared to other works. Also, the proposed modulation and gate charge reuse scheme result in competitive idle power compared to other Class-D amplifiers that switch above 1 MHz. High loop gain around the output stage and the OTA in the loop filter lead to state-of-the-art THD+N performance.

Table 2.1. Performance summary and comparison.

	This Work		[1]	[2] ISSCC'20	[4] ISSCC'18	[6] JSSC'17	[8] ISSCC'17	[14] JSSC'16	[16] JSSC'09
Architecture	PWM 3 Level		PWM 2 Level	DSPWM 2 Level	PWM 2 Level	PWM 2/4 phase	PWM 7 Level	PWM 5 Level	PWM 3 Level
EMI standard	CISPR 25 Class 5		CISPR 25 Class 5	CISPR 25 Class 5*	-	-	-	-	FCC Class B
f_{sw} (kHz)	4200		2100	2000	400	500	700	165~330	250
f_{LC} (kHz)	580		88	100	-	-	-	-	-
Load (Ω)	8	4	4	8	4	4	8	4	4
Output Power (W)	14	28	75	28	20	80	10	70	20
Efficiency	91%	87%	86%	91%	90%	> 90%	91%	90%	90%
Quiescent Current (mA)	7		180	17	20.5	-	3.5	2.9	-
Idle Power (mW)	94		-	245	-	-	-	70	-
Peak THD+N @ 1kHz	0.0004%	0.0007%	0.02%	0.0008%	0.0013%	0.004%	0.0023%	0.003%	0.1
SNR (A-weighted)	109.7 dB		-	108.6 dB	116 dB	-	106 dB	-	-
DR (A-weighted)	111.2 dB		-	-	115.5 dB	115 dB	-	110 dB	-

*Only 150 kHz to 30 MHz reported

2.6 Conclusion

A low-EMI high-linearity Class-D amplifier employing a multilevel output stage is presented. The fully differential multilevel operation in this work significantly reduces EMI. With a 4.2 MHz switching frequency, the CISPR 25 Class 5 EMI standard is met with an LC filter cutoff frequency of 580 kHz. At idle, the fully differential multilevel operation results in minimal switching activity, leading to an idle power of only 94 mW. The high switching frequency also enables an 800 kHz loop bandwidth and 82 dB of audio band loop gain, suppressing the output stage nonlinearity to below the noise floor and helping the prototype achieve a THD+N of −107.8 dB.

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Chapter 3 A −121.5-dB THD Class-D Audio Amplifier With 49-dB LC Filter Nonlinearity Suppression [1]

3.1 Introduction

The CDA presented in Chapter 2 achieved good linearity. However, since the feedback is taken before the LC filter, its THD may still be limited by the inductor choice. According to Equation (1.5), the THD of an LC filter can be improved by using inductors with a high saturation current or by increasing f_{LC}. Inductors with a high saturation current tend to be bulky and expensive. In Chapter 2, a 580 kHz f_{LC} is enabled by the combination of a multi-level output stage and a 4.2 MHz f_{PWM}. However, as discussed in Section 1.3.2.3, even with such a high f_{LC}, the saturation current of the inductor must be much larger than the maximum load current to achieve linearity commensurate with that of the CDA.

As mentioned in Section 1.3.2.3, CDAs with feedback after the LC filter have been employed to suppress the LC filter nonlinearity [1], [2], [3], [4], [5], [6]. The main challenge is to maintain loop stability with the two additional poles from the LC filter while achieving enough loop gain around the LC filter. This could be realized by the self-oscillating architecture (Fig. 1.7), whose EMI spectrum, unfortunately, varies with the signal and f_{LC}. Therefore, for EMI-sensitive applications, constant-frequency PWM-based CDAs such as [4], [5], [6] are preferred, but their loop bandwidth must stay below f_{PWM}/π to ensure correct PWM operation [4], [7]. In practice, the

[1] This chapter is based on the journal paper: H. Zhang, M. Berkhout, K. A. A. Makinwa, and Q. Fan, "A -121.5-dB THD Class-D Audio Amplifier With 49-dB LC Filter Nonlinearity Suppression," *IEEE J. Solid-State Circuits*, vol. 57, no. 4, pp. 1153-1161, Apr. 2022.

location of these poles inevitably varies due to manufacturing tolerance and the LC components' voltage and current dependency. To ensure robust operation, the stability and loop bandwidth requirements above must be met under these variations. In general, to support a wider range of f_{LC}, the loop filter should be designed more conservatively, leading to a lower loop gain. With a relatively low f_{PWM} as in [4], [5] (< 700 kHz), the loop gain is limited to about 20 dB. In [6], despite an f_{PWM} of about 500 kHz, an aggressive 5th-order digital loop filter achieving 50 dB loop gain is enabled by calibrating the loop filter coefficients for each LC filter, but this comes at the expense of increased application cost.

In this chapter, to reach a THD below −100 dB, a dual-loop architecture is proposed that aims to suppress LC filter nonlinearity by at least 40 dB, based on the data in Table 1.1. It is robust to ±30% variation in LC filter cut-off frequency to accommodate the manufacturing tolerances and bias dependencies of typical components without the need to calibrate per LC filter. This is enabled by the use of a high (1.2 MHz) loop bandwidth, thanks to the 4.2 MHz output stage of Chapter 2. In this architecture, an inner loop desensitizes the loop bandwidth from f_{LC} variations and ensures stability. An outer loop then employs a resonator with optimized in-band poles to maximize the suppression of LC filter nonlinearity.

This chapter is organized as follows. Section 3.2 introduces the proposed architecture and explains the design considerations for the loop filter parameters. Section 3.3 describes circuit implementation details. Measurement results are presented in Section 3.4. Section 3.5 concludes this paper.

3.2 Proposed Architecture

3.2.1 Inner Loop

Fig. 3.1(a) illustrates the proposed architecture. It consists of an inner loop, which incorporates a 1st order RC low-pass filter (LPF) that bypasses a main feedback loop (with a gain of b_0) at high frequencies. The inner loop has three main functions: 1) it compensates for LC filter phase shift and, therefore, stabilizes the overall amplifier; 2) it ensures that the loop bandwidth around the output stage is insensitive to LC filter variation [Fig. 3.1(b)] and satisfies the PWM stability criteria ($f_U < f_{PWM}/\pi$) since the loop gain around f_U is dominated by the 1st order path, 3) it provides the loop gain needed to suppress output-stage nonlinearity.

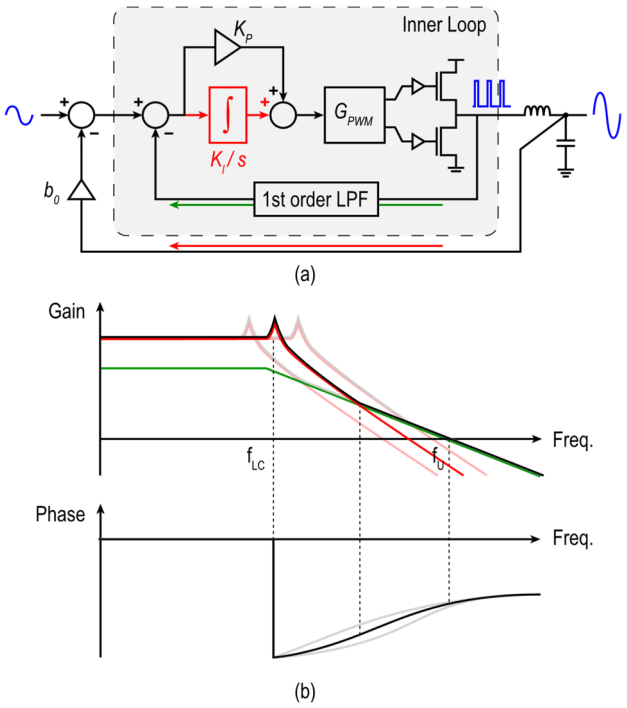

Fig. 3.1. (a) The proposed feedback-after-LC architecture stabilized by the inner loop, and (b) loop gain around the output stage under LC filter variations.

To evaluate the dampening effect of the inner loop on the LC filter's complex poles, its closed-loop gain $H_{\text{CL,inner}}(s)$ will be analyzed. For simplicity, the integral path K_{I}/s (drawn in red) is initially ignored. Then, $H_{\text{CL,inner}}(s)$ can be expressed as:

$$H_{\text{CL,inner}}(s) = K_{\text{P}} G_{\text{PWM}} \cdot \frac{s + \omega_{\text{RC}}}{s + (1 + K_{\text{P}} G_{\text{PWM}})\omega_{\text{RC}}}. \tag{3.1}$$

In (3.1), K_{P} denotes the proportional gain in the forward path, G_{PWM} is the equivalent gain of the output stage (the ratio between its supply voltage and the amplitude of the triangular wave used for PWM generation) [8], and ω_{RC} is the cutoff frequency of the 1st order LPF. From Fig. 3.1, the loop bandwidth f_{U} is given by:

$$\omega_{\text{U}} = 2\pi f_{\text{U}} \approx K_{\text{P}} G_{\text{PWM}} \omega_{\text{RC}}, \tag{3.2}$$

where f_{U} is slightly lower than f_{PWM}/π. Hence, (3.1) can be simplified to:

$$H_{\text{CL,inner}}(s) = \frac{\omega_{\text{U}}}{\omega_{\text{RC}}} \cdot \frac{s + \omega_{\text{RC}}}{s + (\omega_{\text{RC}} + \omega_{\text{U}})}. \tag{3.3}$$

Eq. (3.3) shows that the inner loop acts as a lead compensator with a low-frequency zero at ω_{RC}. Fig. 3.2(a) shows its bode plot, which illustrates how its phase lead can be used to compensate for the phase lag introduced by the LC filter.

The loop gain around the LC filter is given by

$$H_{\text{outer}}(s) = b_0 H_{\text{CL,inner}}(s) H_{\text{LC}}(s), \tag{3.4}$$

where $H_{\text{LC}}(s)$ is the LC filter's frequency response. Fig. 3.2(b) shows the bode plot of $H_{\text{outer}}(s)$. There is a tradeoff between the phase margin and the in-band magnitude of $H_{\text{outer}}(s)$. This is because a smaller ω_{RC} implies a

higher $\left|H_{\text{CL,inner}}\right|$, especially at frequencies above ω_{RC}, so b_0 must be reduced to achieve the extra phase lead.

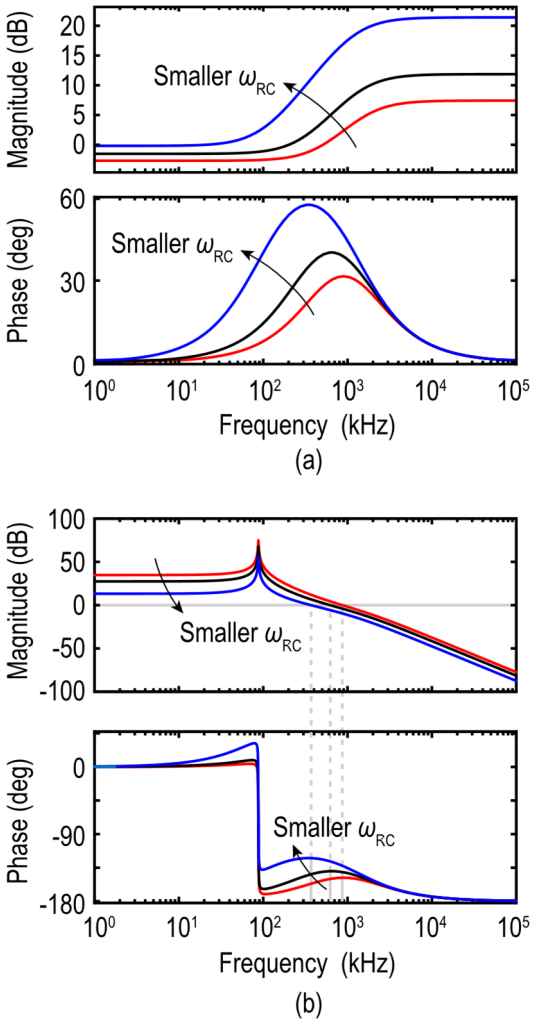

Fig. 3.2. (a) The inner loop's closed-loop response $H_{\text{CL,inner}}$, and (b) the loop gain around the LC filter H_{outer} for the system of Fig. 3.1(a).

Apart from stabilizing the outer loop, the gain of the inner loop also helps to suppress output stage nonlinearity. This can be improved by adding an

integral path in parallel with K_P, forming a PI compensator in the forward path. Then, (3.3) should be modified as follows.

$$H_{CL,inner}(s) = \frac{G_{PWM}H_{PI}(s)}{1 + G_{PWM}H_{PI}(s) \cdot \dfrac{1}{1 + \dfrac{s}{\omega_{RC}}}}, \tag{3.5}$$

where $H_{PI}(s) = (K_P s + K_I)/s$ is the PI compensator's transfer function.

By choosing the PI compensator's zero to coincide with ω_{RC}, i.e., $K_I / K_P = \omega_{RC}$, the loop gain around the output stage reduces to that of an integrator, and (3.5) simplifies to

$$H_{CL,inner} = \frac{G_{PWM}(sK_P + K_I)}{s + G_{PWM}K_I}. \tag{3.6}$$

Thanks to the pole-zero cancellation, the inner loop remains 1st order, and the closed-loop response is still that of a lead compensator. The accuracy of the pole-zero cancellation can be ensured by defining K_I / K_P and ω_{RC} with the same type of RC components on-chip. The loop bandwidth is given by

$$\omega_U = 2\pi f_U = G_{PWM}K_I. \tag{3.7}$$

K_I is defined by on-chip RC components, which can be set with sufficient accuracy by a one-time trim [9]. Consequently, the loop bandwidth becomes insensitive to LC filter variations.

However, as shown in Fig. 3.2(b), the loop gain around the LC filter is still relatively low in the audio band. Also, the loop gain around the output stage does not suppress its nonlinearity sufficiently. These problems are addressed by the addition of an outer loop.

3.2.2 Outer Loop

The outer loop employs two additional stages to increase the suppression of LC filter and output stage nonlinearity, as shown in Fig. 3.3. These stages form a resonator that is designed to maximize the in-band loop gain. A feedforward path (a_1) is used to reduce the output swing of the 1st integrator [10]. A direct input feedforward path (a_0) is used to reduce the output swing of the 2nd integrator [11]. The inclusion of these paths relaxes the amplifiers' specifications and facilitates smooth overdrive recovery (see Section III-B).

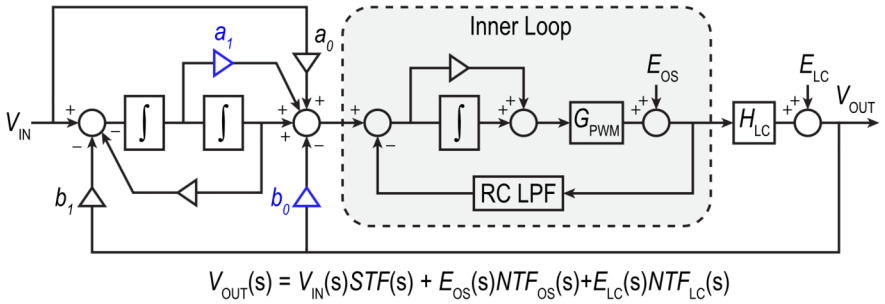

Fig. 3.3. Complete block diagram of the proposed Class-D amplifier.

Besides adding two poles to boost the audio-band gain, the outer loop introduces two zeros due to the presence of the feedforward (a_1) and feedback (b_0) paths highlighted in Fig. 3.3.

In contrast to the zero provided by the inner loop, these two zeros can be arranged as a complex conjugate pair, which pulls the LC filter poles further into the left half-plane (LHP) without compromising loop gain [12], as shown in Fig. 3.4. However, the Q of these zeros cannot be made too high. In this case, shown by the red traces in Fig. 3.4, the LC filter poles no longer move into the LHP but stay close to the imaginary axis, implying excessive ringing in the transient response. In this work, to balance performance and robustness, the Q of these zeros is set to unity. The zero locations of the inner loop and

outer loop are co-optimized in the overall system using Matlab's Control System Designer.

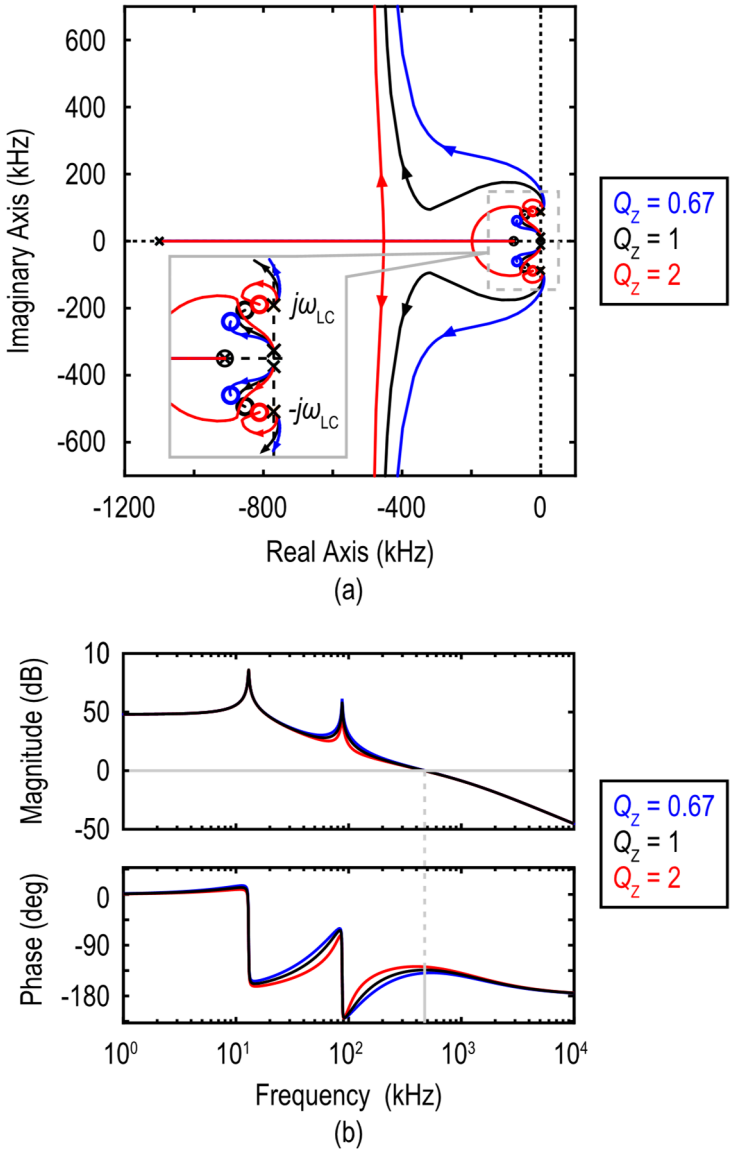

Fig. 3.4. (a) Root loci and (b) loop gain around the LC filter for different Q of the outer loop zeros.

3.2.3 Nonlinearity Suppression

In Fig. 3.3, LC filter and output stage nonlinearity are modeled as additive errors. LC filter nonlinearity is suppressed by the gain of the resonator and the closed-loop gain of the inner loop. This results in the following noise transfer function (NTF):

$$NTF_{\mathrm{LC}}(s)=\frac{V_{\mathrm{OUT}}(s)}{E_{\mathrm{LC}}(s)}=\frac{1}{1+H_{\mathrm{CL,inner}}(s)H_{\mathrm{RES}}(s)H_{\mathrm{LC}}(s)}, \tag{3.8}$$

where $H_{\mathrm{RES}}(s)$ is the open-loop gain of the resonator.

Output stage nonlinearity is suppressed by both the inner loop and the outer loop, resulting in the following NTF:

$$\begin{aligned} NTF_{\mathrm{OS}}(s)&=\frac{V_{\mathrm{OUT}}(s)}{E_{\mathrm{OS}}(s)} \\ &=\frac{H_{\mathrm{LC}}(s)}{1+\dfrac{G_{\mathrm{PWM}}K_{\mathrm{I}}}{s}+H_{\mathrm{LC}}(s)H_{\mathrm{RES}}(s)H_{\mathrm{PI}}(s)}. \end{aligned} \tag{3.9}$$

Fig. 3.5(a) plots $NTF_{\mathrm{LC}}(s)$ and $NTF_{\mathrm{OS}}(s)$. As shown, LC filter nonlinearity is suppressed by more than 47 dB in-band, and output stage nonlinearity is suppressed by more than 80 dB. This is advantageous since $\left|E_{\mathrm{OS}}(s)\right|$ is higher (about −40 dB according to simulations).

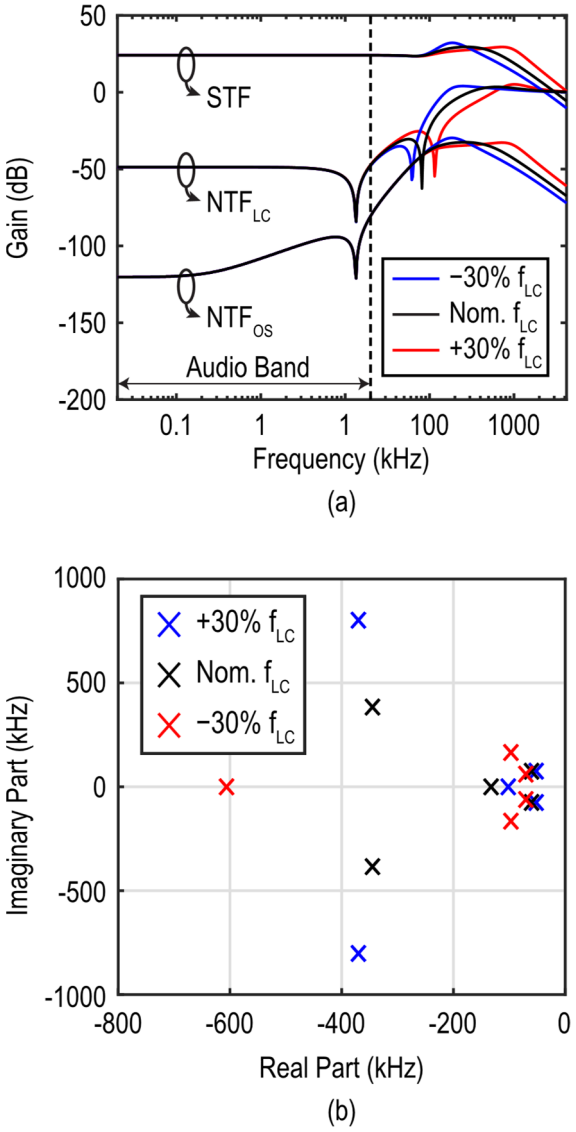

Fig. 3.5. (a) STFs and NTFs and (b) locations of closed-loop poles under fLC variations.

3.2.4 f_{LC} Tolerance

The proposed architecture should be robust to ±30% variations in f_{LC}. As shown in Fig. 3.5(a), such variations do not affect the in-band magnitude of

the NTFs. Furthermore, they do not affect amplifier stability since all the poles remain well within the LHP [Fig. 3.5(b)].

The loop gain around the output stage is plotted in Fig. 3.6. With ±30% variations in f_{LC}, the loop bandwidth varies by only ±12% and remains below f_{PWM}/π. The lower phase margin when f_{LC} increases is not a problem since the resulting STF peaking is far beyond the audio band, as shown in Fig. 3.5(a).

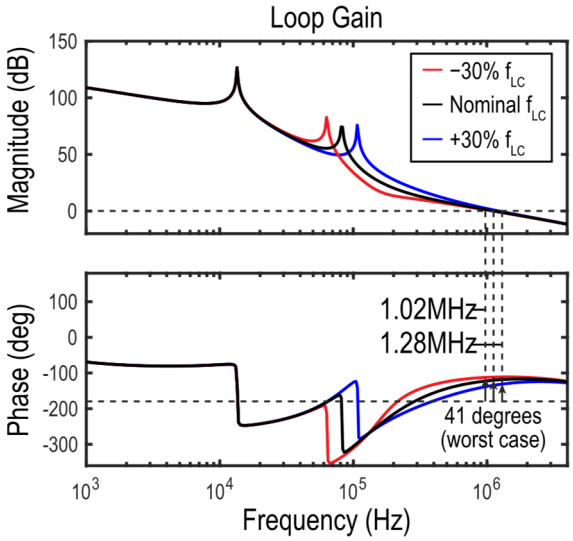

Fig. 3.6. Loop gain around the output stage under ±30% fLC variations.

3.3 Circuit Implementation

3.3.1 Loop Filter

Fig. 3.7 shows a simplified schematic of the loop filter. The implementation is fully differential, and active RC integrators are used for high linearity. Note that in the feedback-after-LC architecture, high-frequency content at the amplifier's output is heavily attenuated by the LC

filter, significantly relaxing the speed and linearity requirements on the outer loop filter. The 1st order LPF in the inner loop is implemented by R_{FILT}, C_{FILT}, and R_{FB3}.

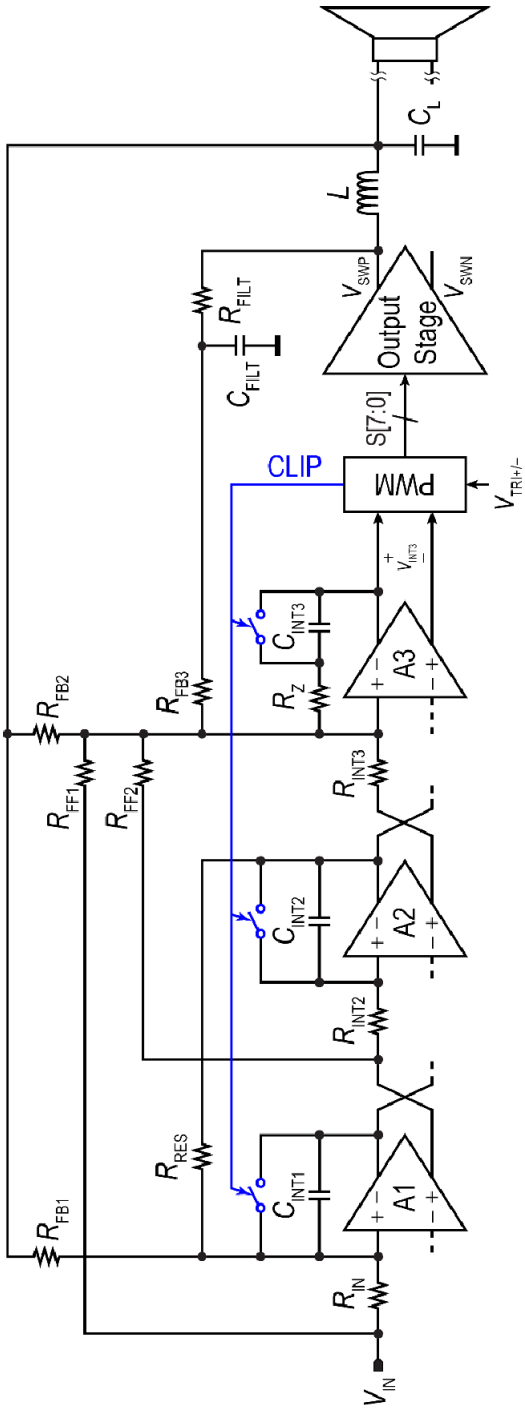

Fig. 3.7. Circuit implementation of the loop filter.

To realize the target RC time constants after a one-time foreground calibration, the loop filter's capacitors are implemented as 2-bit switchable banks. As a result, the tolerable f_{LC} range can be centered around the nominal f_{LC} of 85 kHz despite process variations. In contrast to the coefficient calibration of the digital filter in [6], this calibration does not have to be tailored to a particular LC filter as long as f_{LC} is within the tolerable range.

3.3.2 Overload Detection and Recovery

When the amplifier is overdriven, the integrators in the 5th-order loop will saturate, and their outputs will clip. As a result, an audible settling transient, dictated by the loop dynamics, will occur when the overdrive is removed.

To avoid such transients, an overdrive detection block is implemented in the PWM generator, as shown in Fig. 3.8(a). Due to the feedforward architecture, the integrators in the loop filter only process small error signals during normal operation. Once overdrive is detected, however, the integrator outputs are reset to zero. After the overdrive is removed, they can then return quickly to the small error signals that occur during normal operation, as shown in Fig. 3.9, resulting in smooth overdrive recovery.

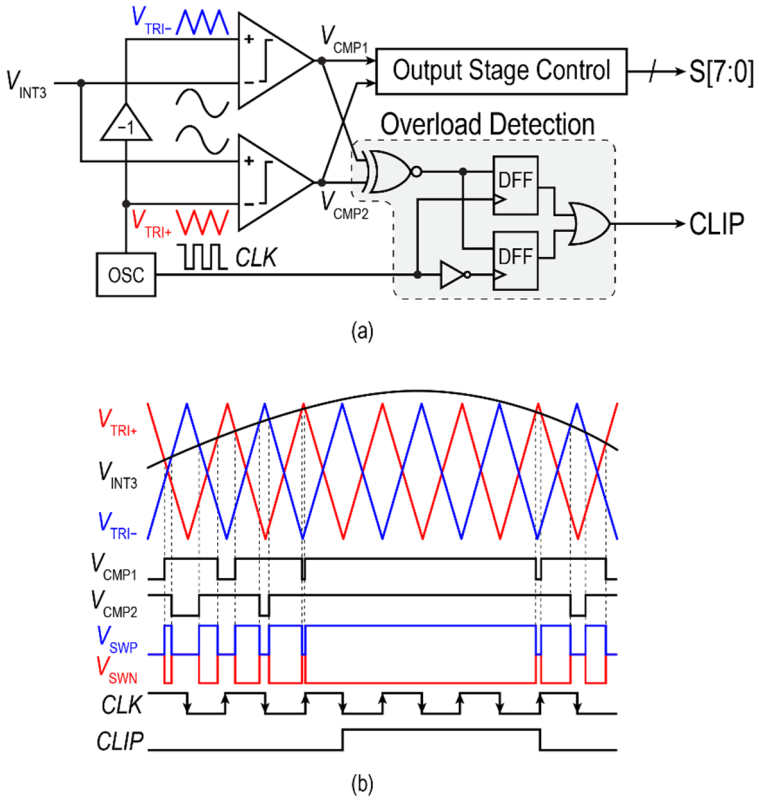

Fig. 3.8. (a) Block diagram of the PWM generation with overload detection and (b) its corresponding waveform.

This Class-D amplifier employs a 3-level PWM scheme that maintains a constant output common-mode voltage (Chapter 2). The waveforms in the pulse-width modulator and the overdrive detection circuit are shown in Fig. 3.8(b). During normal operation, the PWM input V_{INT3} lies between the peaks of the triangular wave, and the two comparator outputs have opposite polarity at the peaks of either triangular wave. Therefore, overdrive can be detected by first XNOR-ing the comparator output and then sampling the result at the peaks of both triangle waves, giving the *CLIP* signal.

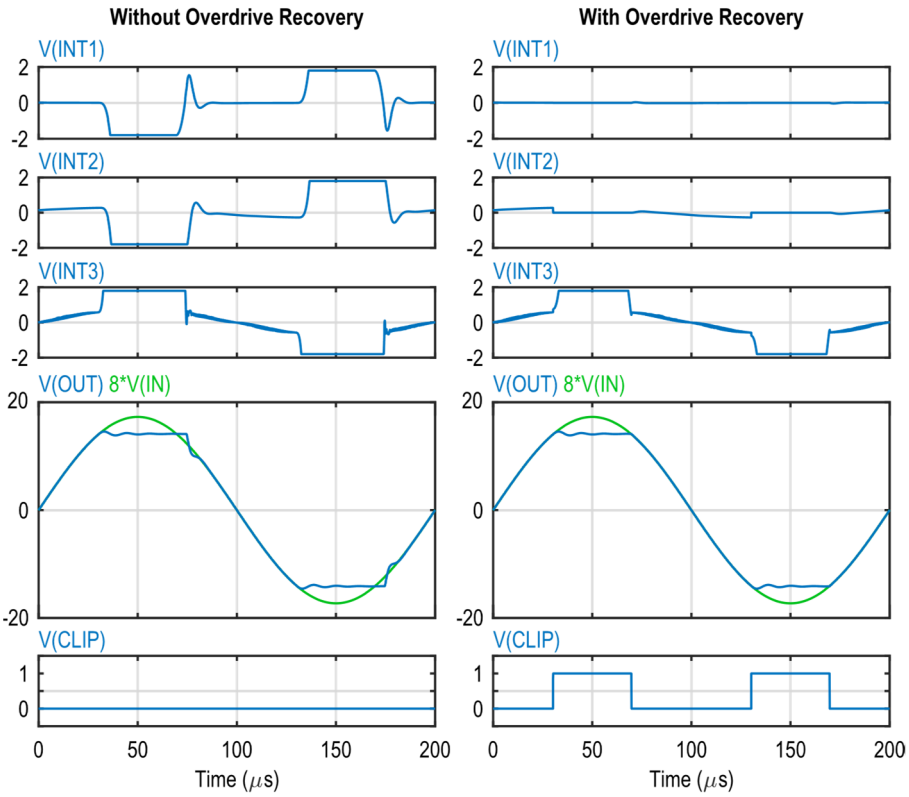

Fig. 3.9. Simulated waveform of the proposed Class-D amplifier with and without overdrive recovery.

3.4 Measurement Results

A prototype chip is fabricated in a 180 nm BCD process and occupies an active area of 5 mm^2 (Fig. 3.10). The output stage employs a 14.4 V supply. The loop filter and PWM operate with a 1.8 V supply.

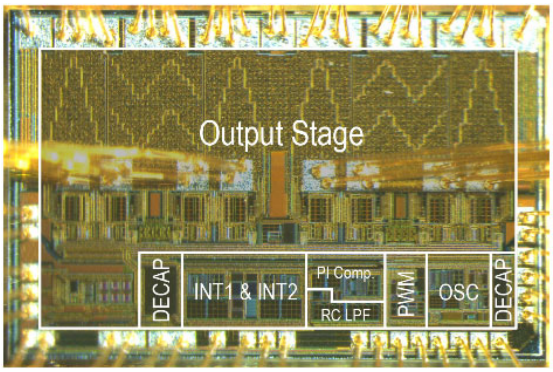

Fig. 3.10. Die micrograph.

3.4.1 Audio Performance

The audio performance is measured with an APx555 analyzer. Fig. 3.11 shows the measurement setup. To estimate the magnitude of LC filter nonlinearity, the THD+N at the LC filter input is measured as well. This waveform includes the pre-distortion applied by the feedback loop to linearize the LC filter output.

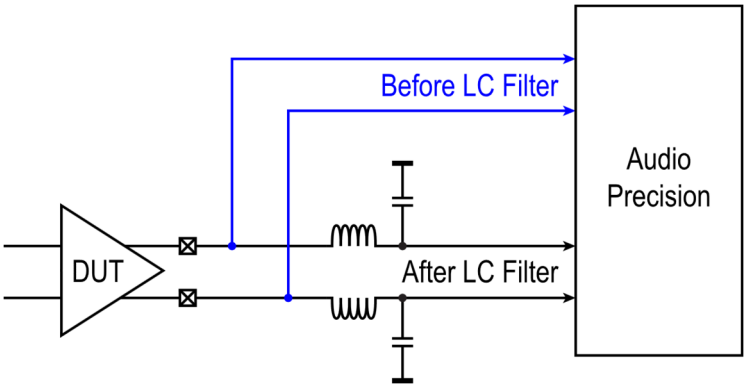

Fig. 3.11. Measurement setup for estimating LC filter nonlinearity.

Fig. 3.12 shows the output spectrum after the LC filter at an output power of 1W with a 1 kHz sine wave input. The amplifier achieves a THD of −121.5 dB and −119.0 dB when driving an 8-Ω load and a 4-Ω load, respectively.

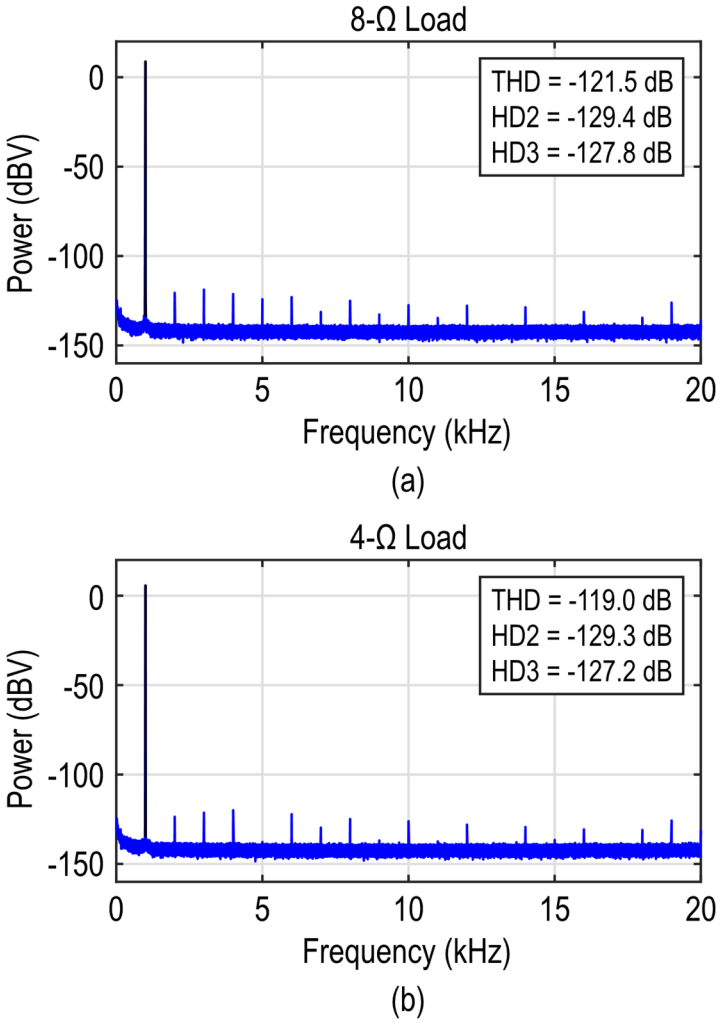

Fig. 3.12. Output spectra for (a) 8-Ω and (b) 4-Ω loads.

The solid lines in Fig. 3.13 show the measured THD+N with a 4-Ω load as the input amplitude is swept. The measurement is repeated for the three inductors listed in Table 3.1, which have different current dependencies, and for input frequencies of both 1 kHz and 6 kHz. The difference in THD+N due to the inductors (measured right before clipping) is only 1.1 dB for the 1-kHz input and 3 dB for the 6-kHz input.

Table 3.1. Inductors used in the measurements for Fig. 3.13.

	 #1	 #2	 #3
Vendor	Würth	Würth	Murata
Part No.	7443340330	74437346033	FDSD0420-H-3R3M=P3
Dimensions (mm)	8.4x7.9x7.2	7.3x6.6x2.8	4.2x4.2x2

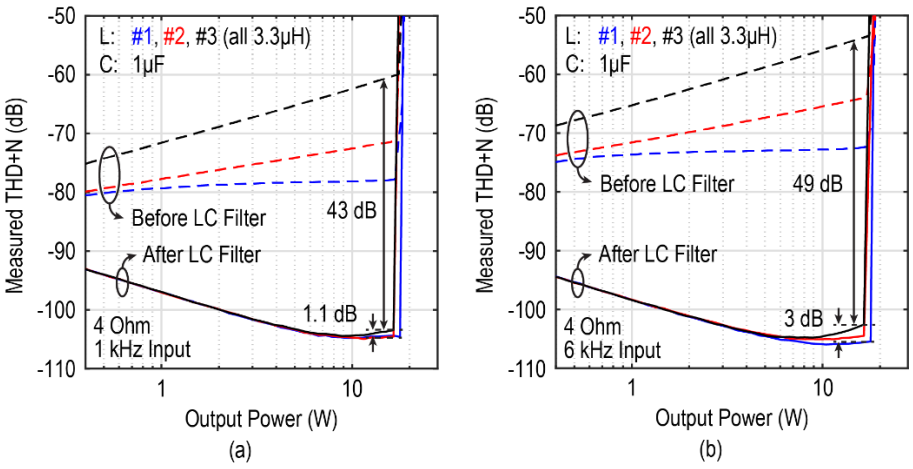

Fig. 3.13. THD+N for (a) 1 kHz input and (b) 6 kHz input.

Fig. 3.14 shows the measured overdrive recovery behavior. The smooth recovery confirms the effectiveness of the overdrive recovery scheme.

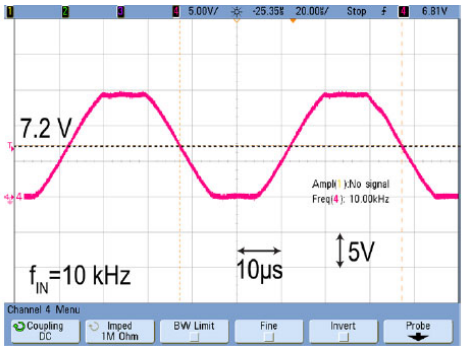

Fig. 3.14. Measured overdrive recovery transient.

3.4.2 Suppression of LC Filter Nonlinearity

As shown in the dashed lines in Fig. 3.13, the nonlinearity of all three LC filters is above −80 dB, with the worst being close to −55 dB for a 6 kHz input. The Class-D amplifier thus suppresses the LC filter nonlinearity by up to 49 dB. As expected, the smallest inductor has the largest nonlinearity, but thanks to the feedback-after-LC architecture, it only degrades the overall THD+N by some 3 dB. Fig. 3.15 shows the spectra of the signals before and after the LC filter obtained from a two-tone test. The signal before the LC filter contains significant intermodulation products that spread across the entire audio band. In a conventional Class-D amplifier, with feedback *before* the LC filter, a similar spectrum would have appeared across the load. In contrast, for the proposed architecture, the intermodulation products at the LC filter output are significantly suppressed, and the residual IM3 is −113.1 dBc.

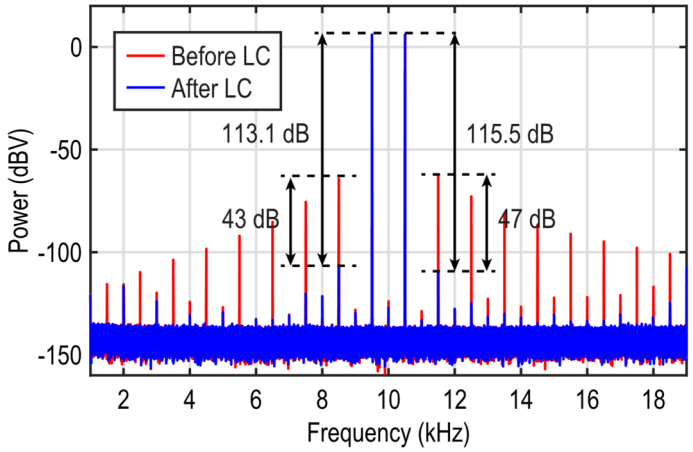

Fig. 3.15. Output spectra from a two-tone test.

3.4.3 Variations in Loading and f_{LC}

Besides load resistance, practical speakers also present an inductive impedance to the Class-D amplifier. To verify the robustness to load impedance variations, the THD+N measurement is performed for load inductances varying from 0 to 330 µH. As shown in Fig. 3.16, the high linearity performance is maintained.

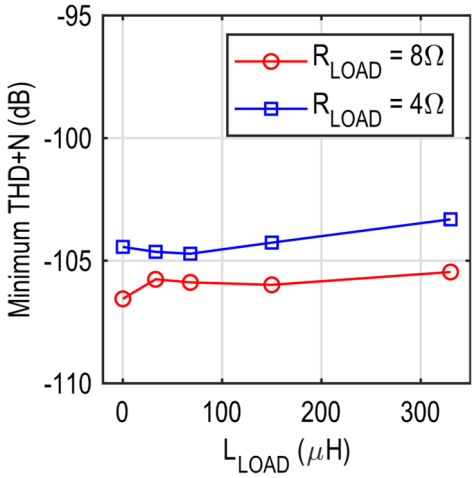

Fig. 3.16. Peak THD+N vs. series load inductance.

Fig. 3.17 shows the robustness of the Class-D amplifier to f_{LC} variation from 62 kHz to 106 kHz, obtained by intentionally varying the LC filter's capacitance. Across six samples, the variation in THD+N is less than 3 dB.

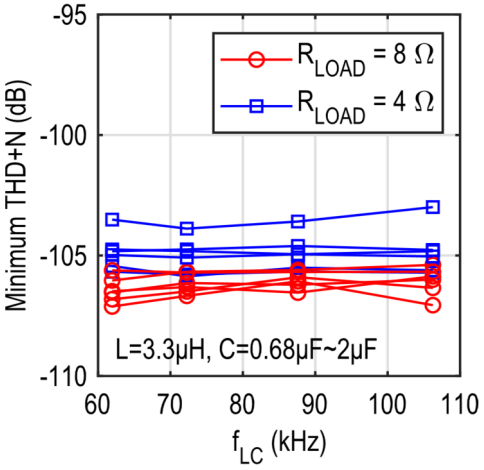

Fig. 3.17. Peak THD+N vs. f_{LC}.

3.4.4 Efficiency and Idle Power

Fig. 3.18 shows the power efficiency of the prototype as a function of output power. It achieves 91% efficiency for an 8-Ω load and 87% efficiency for a 4-Ω load. It can deliver a maximum of 21W, measured at 10% THD, and consumes 120 mW of idle power.

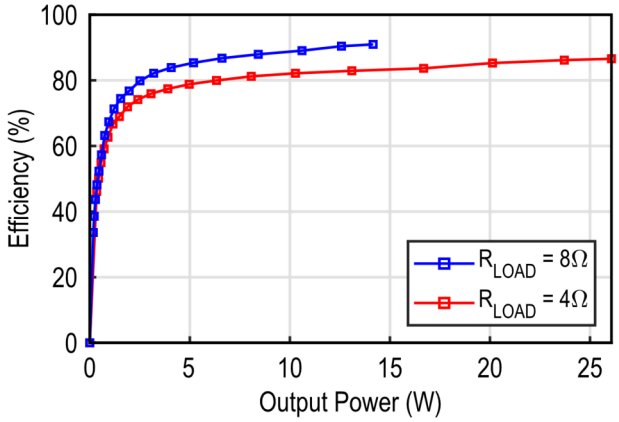

Fig. 3.18. Power efficiency vs. output power (L_{LOAD} = 0).

3.4.5 Comparison with the State-of-the-Art

Table 3.2 summarizes the prototype's performance and compares this work with other state-of-the-art Class-D amplifiers. It achieves the best THD, as well as the best THD+N for a 4-Ω load. Last but not least, it suppresses LC filter nonlinearity by 49 dB while being the only work that is robust to a wide variation in f_{LC}.

Table 3.2. Performance summary and comparison.

	This Work		TAS6424 [1]	Karmakar JSSC'20 [2]	Zhang JSSC'21 [3]		Schinkel JSSC'17 [4]	Adduci J. AES'12 [12]
Supply Voltage (V)	14.4		14.4	14.4	14.4		14.4/25	25
R_L (Ω)	8	4	4	4	8	4	4	4
Efficiency	91%	87%	86%	91%	91%	87%	>90%	89%
THD (dB)	−121.5	−119.0	-	−108.9	-	-	-	-
THD+N at 1kHz (dB)	−107.1	−105.9	−76.5	−102.2	−107.8	−102.6	−87.9	−67.9
THD+N at 1kHz (%)	0.0004	0.0005	~0.015	0.0008	0.0004	0.0007	0.004	0.04
LC error suppression (dB)	49		0	0	0		50*	10
f_{LC} tolerance (kHz)	62 ~ 106		N/A	N/A	N/A		-	-
SNR (dB-A)	110.0		-	109	109.7		-	110
DR (dB-A)	110.8		-	-	111.2		115	108
PSRR (dB) (Frequency Range [Hz])	70 ~ 58 (20 ~20k)		75 ~ 57 (20 ~ 20k)	70 ~ 62 (20 ~ 20k)	-		88 ~ 60 (100 ~ 20k)	-

3.5 Conclusion

A dual-loop analog-input Class-D amplifier with feedback after the LC filter is presented. An inner loop dampens the LC poles, improves f_{LC} tolerance, and suppresses output-stage nonlinearity, while an outer loop further suppresses both LC filter and output-stage nonlinearity. A prototype implemented in a 180 nm BCD process achieves −121.5 dB THD and 49 dB suppression of LC filter nonlinearity. It is also robust to ±30% f_{LC} variation, thereby enabling the use of small and low-cost LC components in high-linearity Class-D amplifiers.

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Chapter 4 A 121.4-dB DR Capacitively Coupled Chopper Class-D Audio Amplifier[1]

4.1 Introduction

As mentioned in Section 1.3.3, the thermal noise of the input resistors or DAC of a conventional closed-loop CDA limits its DR. For low-noise closed-loop amplification, the capacitively coupled chopper amplifier is a good choice [1], [2], [3]. Its capacitive feedback network does not contribute any noise, nor does it consume static power. This enables high energy efficiency, making it popular in biomedical and instrumentation applications. The amplifier's $1/f$ noise is mitigated by chopping, making its thermal noise the dominant contributor.

However, to the best of the author's knowledge, capacitive feedback has not been attempted in CDAs previously since most CDAs take their feedback from the switching nodes, whose sharp edges, when fed back to the virtual ground nodes, would directly saturate the input stage of the loop filter. The use of chopping in CDAs is also rare because it can demodulate PWM sidebands and introduce distortion. If this demodulation is mitigated, chopping can significantly improve the $1/f$ noise and PSRR [4], [5]. In [4], these issues are avoided by extra anti-aliasing filters and by performing chopping only in auxiliary signal paths. In [5], the chopping and PWM timing are then carefully arranged to avoid THD degradation due to intermodulation.

[1] This chapter is based on the journal paper: H. Zhang, M. Berkhout, K. A. A. Makinwa, and Q. Fan, " A 121.4-dB DR Capacitively Coupled Chopper Class-D Audio Amplifier," *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3736-3745, Dec. 2022.

The above issues with using capacitive feedback and chopping in a CDA are significantly mitigated when feedback is taken from the LC filter output since high-frequency components in the feedback signal are heavily attenuated by the LC filter. Building on the work from previous chapters, this chapter describes a capacitively-coupled chopper CDA that achieves 121.4 dB DR. Unlike conventional chopper amplifiers, which process small input and output signals [1], [2] or are used in discrete-time switched-capacitor circuits [3], the proposed audio amplifier must process large continuous-time signals at both its low-voltage (LV) input (±1.8 V) and HV output (±14.4 V). Since the loop filter of the CDA operates in the LV domain, the HV transients coupled into the loop filter via a capacitive feedback network will degrade loop filter linearity and may even damage thin-oxide core devices in input stages. To prevent this, a feedback-after-LC architecture is used to remove HV edges in the CDA output, while the timing and impedance of the switches in the chopped feedback network have been carefully optimized. Residual chopping glitches are blocked by a deadband, so high CDA linearity is maintained.

The rest of this chapter is organized as follows. Section 4.2 introduces the capacitively coupled chopper CDA architecture. Section 4.3 describes the circuit implementation and mitigation techniques to overcome HV transients. Section 4.4 presents the measurement results, and Section 4.5 concludes the chapter.

4.2 Capacitively Coupled Chopper CDA

4.2.1 Overview

To achieve low noise, this work employs a capacitively coupled preamplifier in the loop filter [6]. Fig. 4.1 shows an overview of the proposed

capacitively coupled chopper CDA. The ratio between the input capacitor C_{IN} and the global feedback capacitor C_{FB} sets an overall closed-loop gain of 8. The preamplifier itself has a gain of 16×, which suppresses the noise contribution of the noisy active-RC integrators that comprise the succeeding stages of the loop. The output stage employs 3-level fixed-frequency pulse-width modulation (PWM) with a switching frequency $f_{SW} = 4.2\,\text{MHz}$ and a 14.4 V supply (Chapter 2).

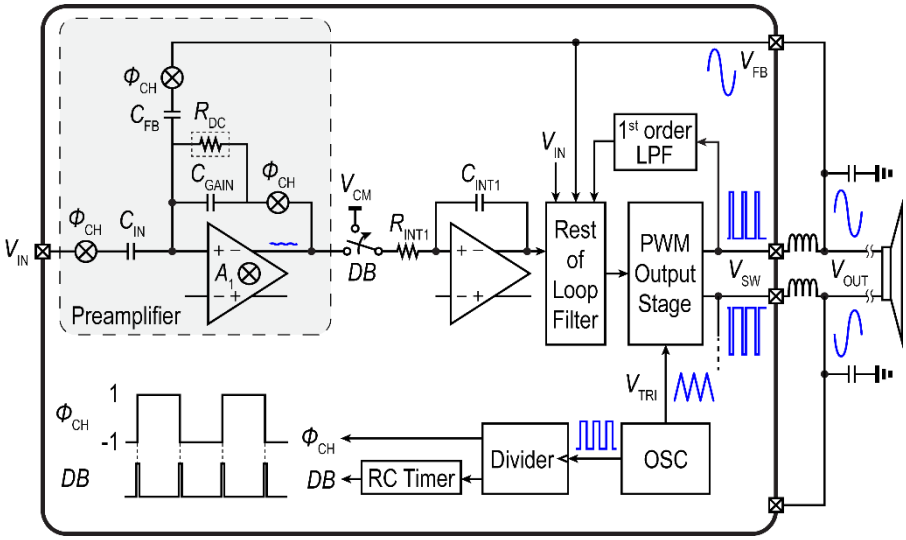


Fig. 4.1. Architecture of the proposed capacitively coupled CDA.

Incorporating the LC into the feedback loop [7], [8], [9] is necessary for the proposed capacitive feedback scheme[2]. Since the output stage generates high-frequency switching signals at V_{SW}, taking feedback from these nodes [4], [11], [12], [13], [14] would result in a residual error signal $(V_{IN} - V_{OUT}/8)$ that would saturate A_1, as illustrated in Fig. 4.2(a). In contrast, due to the LC filter's suppression of the high-frequency components, the error signal is now

[2] The LC filter is required anyway for applications with high output power (> 10 W) or when the speaker cable is longer than a few tens of cm, to suppress the electromagnetic interference (EMI) generated by the CDA's output stage [10].

in the order of millivolts [Fig. 4.2(b)]. To mitigate $1/f$ noise, the input stage of A_1 is chopped. Beneficially, chopping also allows the use of a much smaller resistance to set the dc bias at A_1's virtual ground (R_{DC} in Fig. 4.1), which is more robust to leakage, especially under process and temperature variations. This is because the value of R_{DC} would have to be much larger to push the preamplifier's high-pass corner below 20 Hz, instead of below f_{CH} in the case of chopping. Furthermore, chopping relaxes the matching constraint on the C_{FB} and C_{IN} pairs, thereby improving the common-mode rejection of the preamp and, therefore, the PSRR of the CDA [5].

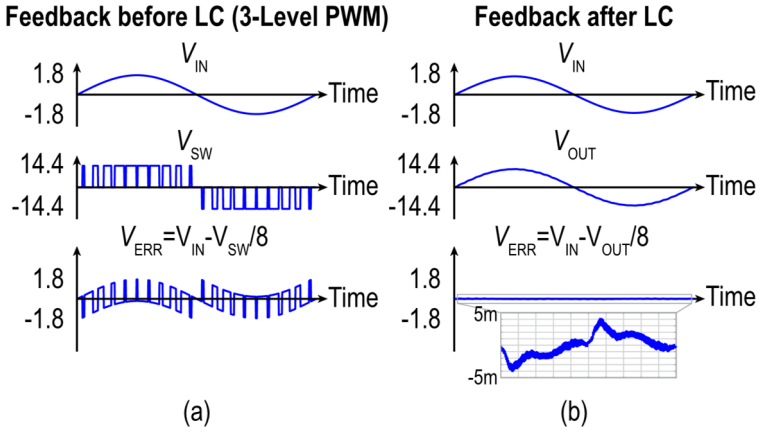
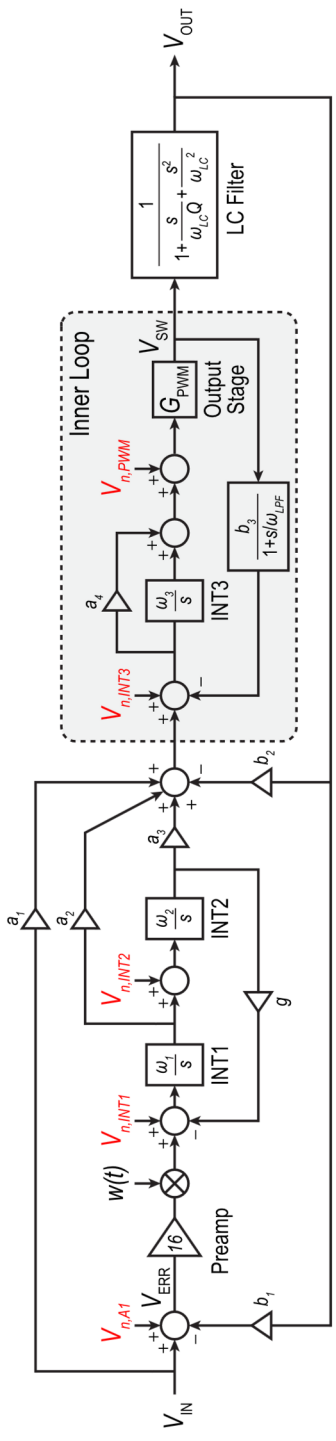


Fig. 4.2 . Error signal waveform for (a) feedback-before-LC and (b) feedback-after-LC CDAs. The closed-loop gain is 8 with a ±1.8 V differential input swing.

However, chopping inevitably also introduces nonlinear glitches due to the large-signal nonlinearity of the chopper switches and the amplifier, limiting the THD of conventional capacitively coupled amplifiers (e.g., to −76 dB in [2]). In signal acquisition applications, the subsequent ADC's sampling time can be carefully chosen to avoid chopping glitches [1], [3]. This is not possible in an audio amplifier. Therefore, a deadband switch is introduced at the output of A_1 to prevent these glitches and the corresponding settling transients of the preamplifier from introducing distortion.

As discussed in [15], [16], propagation delay and parasitic capacitance in a chopper amplifier can demodulate frequency contents from even harmonics of f_{CH} to the baseband. To avoid distortion due to this effect, chopping is performed at $f_{CH} = 200\,\text{kHz}$, an odd subharmonic of f_{SW} [5]. A lower chopping frequency would require a lower $1/f$ corner for A_1, increasing its input capacitance and, thus, its area and power, whereas a higher chopping frequency increases IMD due to the presence of PWM sidebands around even multiples of f_{SW}, and the deadband's noise-folding gain. These considerations will be analyzed later (in Section 4.2.2).

Fig. 4.3 shows a block diagram corresponding to the proposed CDA. The deadband is modeled as a multiplication by a periodic window $w(t)$. As discussed in Chapter 3, the LC filter's 180° phase shift is addressed by a lead compensator, implemented using an inner loop that feeds back the switching node V_{SW} through a 1st-order low-pass filter [7]. The outer loop consists of the preamplifier and a resonator. The latter is built with two integrators and local feedback to place their two poles optimally in the audio band for maximal loop gain.



a_1	a_2	a_3	a_4	b_1	b_2	b_3	g	G_{PWM}	ω_1	ω_2	ω_3	ω_{LC}	ω_{LPF}
1.1875	0.0156	0.0625	21.333	0.1250	0.1250	0.0234	0.0294	28	2.38 Mrad/s	1.49 krad/s	10.5 Mrad/s	503 krad/s	490 krad/s

Fig. 4.3. Simplified block diagram of the proposed CDA.

4.2.2 Noise Analysis

The main sources of thermal noise in the proposed CDA are also shown in Fig. 4.3. Thanks to the 16× gain from the preamplifier, audio-band noise from later loop filter stages is suppressed by 24 dB, and therefore, the CDA's in-band noise floor is mainly determined by the preamplifier. However, the noise of the later stages is not sufficiently suppressed at high frequencies, and the periodic windowing introduced by the deadband partially folds the wideband thermal noise at the preamplifier's output to the audio band. These noise components will be analyzed in the following.

As illustrated in Fig. 4.4(a), the deadband window can be expressed as:

$$w(t;t_d,T)=\begin{cases}0, & |t|<\dfrac{t_d}{2}\\ 1, & \dfrac{t_d}{2}\le|t|<\dfrac{T-t_d}{2}\\ w(t-kT), & \text{otherwise}\end{cases} \tag{4.1}$$

where t_d is the deadband's duration, T is its period [equal to $1/(2f_{\mathrm{CH}})$], and k is a nonzero integer. The Fourier transform of $w(t)$ is given by

$$W(f)=\left[\underbrace{\left(1-\frac{t_d}{T}\right)}_{a_0}+\sum_{\substack{n=-\infty\\ n\neq 0}}^{\infty}\underbrace{-\frac{t_d}{T}\operatorname{sinc}\left(\frac{n\pi t_d}{T}\right)}_{a_n}\right]\delta\left(f-\frac{n}{T}\right), \tag{4.2}$$

whose first few terms are sketched in Fig. 4.4(b).

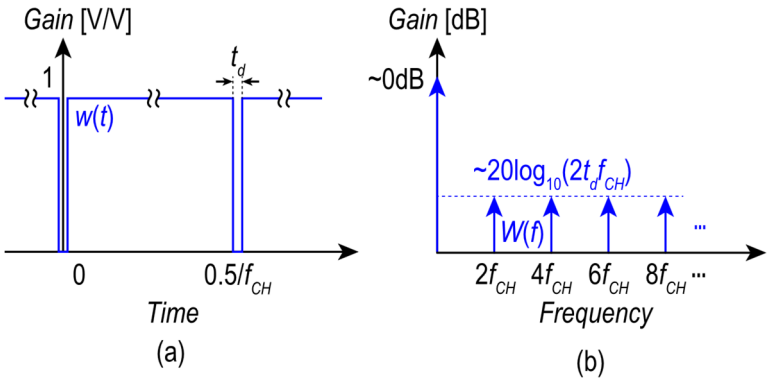


Fig. 4.4. (a) Time-domain waveform of the periodic deadband window $w(t)$, and (b) the first few terms of its frequency-domain representation $W(f)$.

According to (4.2), the deadband marginally attenuates in-band noise by a factor of a_0 but folds frequency components around even multiples of the chopping frequency to DC with a scaling factor of a_n, the magnitude of which is largely determined by the duty cycle of the deadband (t_d / T).

The wideband thermal noise at the preamplifier output includes noise generated by A_1 and the noise present in the feedback signal. Since A_1 is a wideband gain stage, its output noise at different time instants can be assumed uncorrelated. Therefore, the deadband attenuates its noise by a factor of $(1 - t_d / T)$, which can be verified by summing over all noise folding terms:

$$V_{n,A_1,fold}^2 = \sum_{n=-\infty}^{\infty} |a_n|^2 V_{n,A_1}^2 = \frac{1}{T}\int_{-T/2}^{T/2} w^2(t) V_{n,A_1}^2 = \left(1 - \frac{t_d}{T}\right) V_{n,A_1}^2 \tag{4.3}$$

As long as t_d is much smaller than T, the noise folding changes the noise contribution of A_1 by a negligible amount.

On the other hand, the wideband noise present in the feedback signal includes noise contributed by the later stages of the loop filter and the output

stage, shaped by their respective noise transfer functions (NTFs), which are shown in Fig. 4.5. Except for that from A_1, these sources of noise are suppressed in the audio band by the gain of the preceding stages and eventually roll off beyond the unity-gain frequency of the outer loop. However, between 100 kHz and 1 MHz, they appear at the output with much less attenuation.

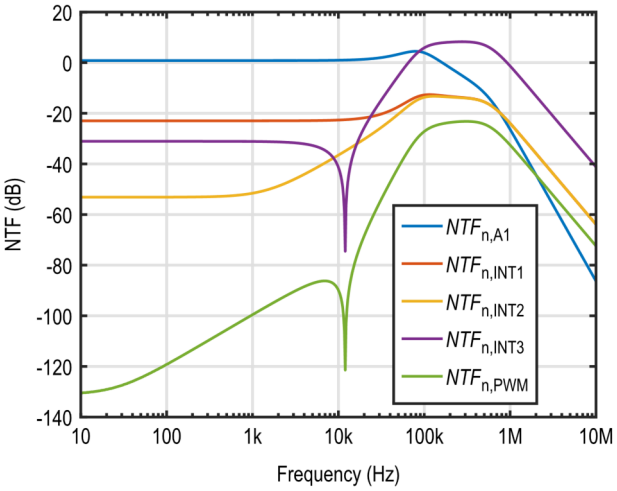


Fig. 4.5. NTFs (normalized to closed-loop gain) of each noise source highlighted in Fig. 4.3.

Fig. 4.6 plots the simulated noise spectral density (NSD) at the output, showing the aforementioned out-of-band noise bump. [The residual $1/f$ noise is mostly contributed by the feedback chopper, which is implemented with LDMOS transistors (Section III-A).]

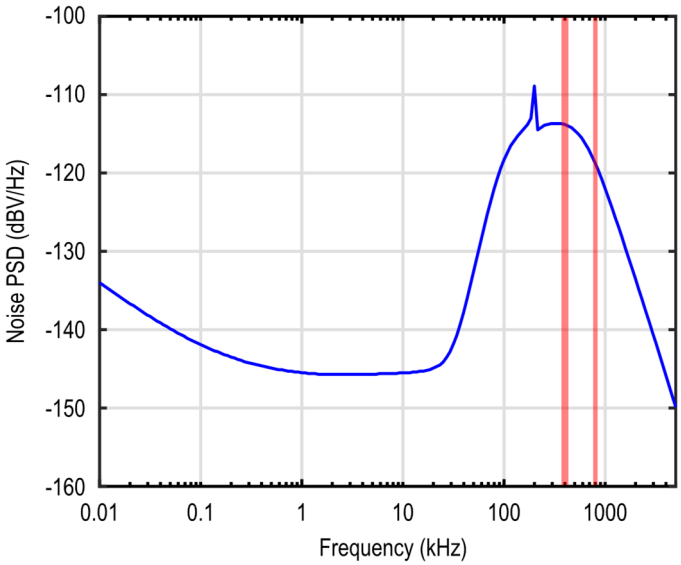


Fig. 4.6. Simulated noise PSD of the CDA output, with the first two bands subjected to noise folding highlighted.

The most significant sources of folded noise are around $2f_{\mathrm{CH}}$ and $4f_{\mathrm{CH}}$, i.e., 400 kHz and 800 kHz. In these two cases,

$$|a_n| \approx \frac{t_d}{T}, \qquad n = 1, 2. \tag{4.4}$$

Reducing the out-of-band noise would require increasing the integrator area as in conventional resistive CDAs. To avoid a significant noise penalty, the deadband's duty cycle is chosen to be 1% $(t_d / T = 0.01)$, thus attenuating the folded noise by 40 dB, corresponding to a deadband duration of 25 ns. The preamplifier is designed to settle sufficiently within this duration. For a higher f_{CH}, the reduced NSD of alias bands is compromised by the increase in $|a_n|$.

In addition, the deadband may also fold back the out-of-band quantization noise of the (typically ΔΣ) audio DAC that drives the CDA. If the DAC has a white out-of-band noise spectrum, sampling 10% of the frequency range per octave (400kHz ± 20kHz, 800kHz ± 20kHz, etc.) will result in the folding

down of approximately −10 dB of the out-of-band noise. For a total out-of-band noise in the order of −40 dBFS [17], [18], and given the aforementioned 40 dB attenuation of folded noise by the deadband, the additional filtering required to keep the folded input noise below −130 dBFS is about:

$$-40\,\text{dBFS} - 40\,\text{dB} - 10\,\text{dB} - (-130\,\text{dBFS}) = 40\,\text{dB}. \tag{4.5}$$

This can be achieved by a 2nd order low-pass filter. Alternatively, quantization noise folding may be avoided by co-designing a DAC to operate at a sampling frequency of $2f_{\text{CH}}$, which places the alias bands at the nulls of the DAC's output spectrum [6].

4.3 Circuit Implementation

4.3.1 Capacitively Coupled Chopper Preamplifier

Fig. 4.7 shows a schematic of the capacitively coupled chopper preamplifier. The input capacitance is chosen to be 3 pF to minimize the attenuation by the parasitic capacitance (~1 pF) at the summing node V_{X}, such that the noise performance is not compromised by the reduced feedback factor due to the parasitics. Monte Carlo simulation indicates a 1-σ mismatch of 0.12% for C_{FB}. Without chopping, this would limit the typical PSRR to about 58 dB.

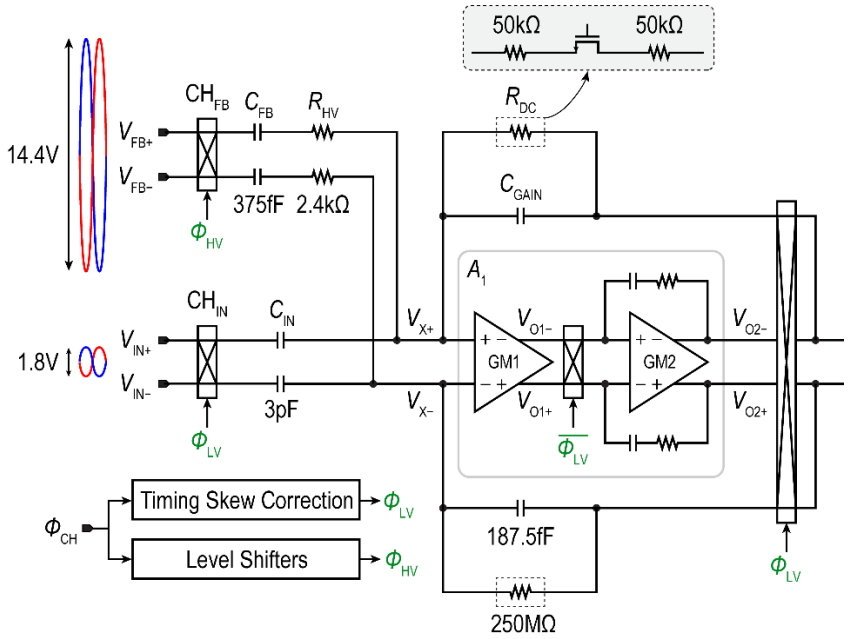


Fig. 4.7. Schematic of the capacitively coupled chopper preamplifier.

The dc bias at V_X is set by a duty-cycled resistor R_{DC} implementing an equivalent resistance of 250 MΩ [6], [19], which ensures a flat gain response around $f_{CH} \pm 20\,\text{kHz}$. In a CDA, temperature fluctuations can be significant and signal-dependent due to the thermal dissipation of the output stage. Therefore, a duty-cycled resistor is chosen over a pseudoresistor for its robustness under temperature variations. The periodic switching of this resistor also introduces some noise folding and IMD, but they are insignificant since the duty cycle (~0.04%) is much smaller than the deadband's.

The preamplifier is built around a two-stage Miller-compensated opamp, shown in Fig. 4.8. The input stage employs a PMOS input pair that achieves a $1/f$ noise corner of about 50 kHz with an input capacitance of around 1 pF to keep its $1/f$ noise contribution below 10%. Its NMOS load is heavily

degenerated to reduce its noise contribution. The input chopper (CH_{IN}) is implemented with conventional bootstrapped switches for high linearity.

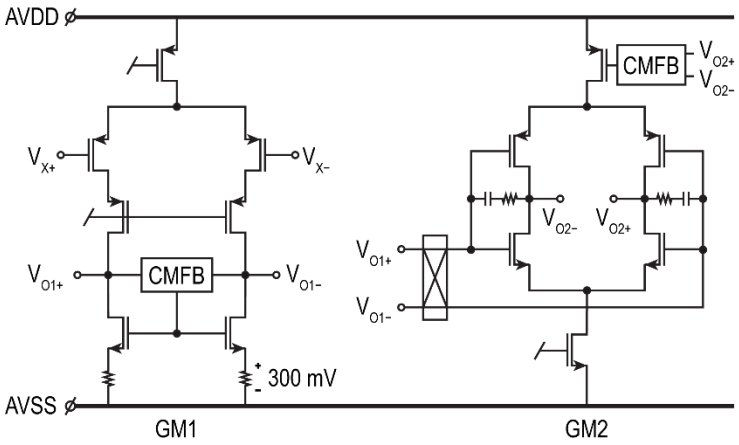


Fig. 4.8. Circuit implementation of amplifier A_1.

4.3.2 HV Chopper[3]

CH_{FB} must handle the 14.4V PWM output. As shown in Fig. 4.9, each switch consists of two back-to-back n-channel LDMOS devices so that they can be completely turned off despite the presence of their body diodes. Level shifters are employed to translate the chopping clock to the floating gate drivers powered from floating regulators bootstrapped to the source nodes of each LDMOS switch. They are supplied by a charge pump that provides a dc voltage V_{CP} near 28 V.

[3] This section is based in part on the journal paper: H. Zhang, N. N. M. Rozsa, M. Berkhout, and Q. Fan, " A Chopper Class-D Amplifier for PSRR Improvement Over the Entire Audio Band," *IEEE J. Solid-State Circuits*, vol. 57, no. 7, pp. 2035-2044, July 2022.

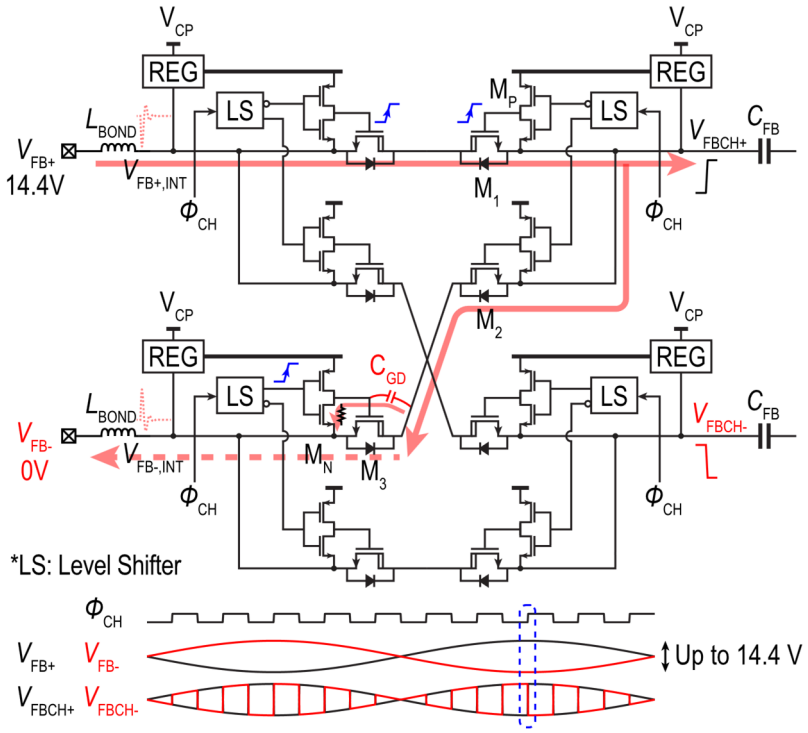


Fig. 4.9. High-voltage chopper (CHFB) and its switching transient during a chopping transition.

In addition, since the output of this work is fed back from the off-chip LC filter, cross conduction through CH_{FB}, even only lasting several hundred ps, can create ringing up to several volts across the parasitic inductance from the bondwire, PCB trace, and the LC filter, adding to the glitches at V_X. The HV chopper transients during a chopping transition are illustrated in Fig. 4.9. Cross conduction happens when coupling through C_{GD} pulls up the gate of a transistor that is supposed to be OFF, e.g., transistor M_3 in Fig. 4.9. This can happen when M_1 is turned on too quickly by its gate pull-up transistor M_P, causing the displacement current through C_{GD} of M_3 to exceed $V_{TH,M_3} / R_{ON,M_N}$, where R_{ON,M_N} is the on-resistance of the gate pull-down transistor M_N. Hence, the ratio of the pull-up and pull-down strength of the switch drivers for CH_{FB}

is sized to 1/7 such that the switches can be kept OFF during such switching events [20].

Fig. 4.10(a) shows the regulator, in which a source follower buffers a Zener-based reference. The charge pump is shown in Fig. 4.10(b), which reuses the circuitry and takes advantage of the switching operation in the Class-D amplifier's output stage. Two off-chip bootstrap capacitors are employed to supply the high-side gate driver of the output stage [12]. They are charged to V_{PVDD} due to the switching operation. Through Schottky diodes D_1 and D_2, they charge V_{CP} to $\sim 2V_{PVDD}$ [Fig. 4.10(c)], which is buffered by a small output capacitor C_{CP} on-chip. Fig. 4.11 shows the level shifter, which is based on Section 2.3.4. During each chopping transition, a current pulse pulls down one of the SR-latch inputs through the corresponding pull-up resistors, thereby updating the level shifter's output.

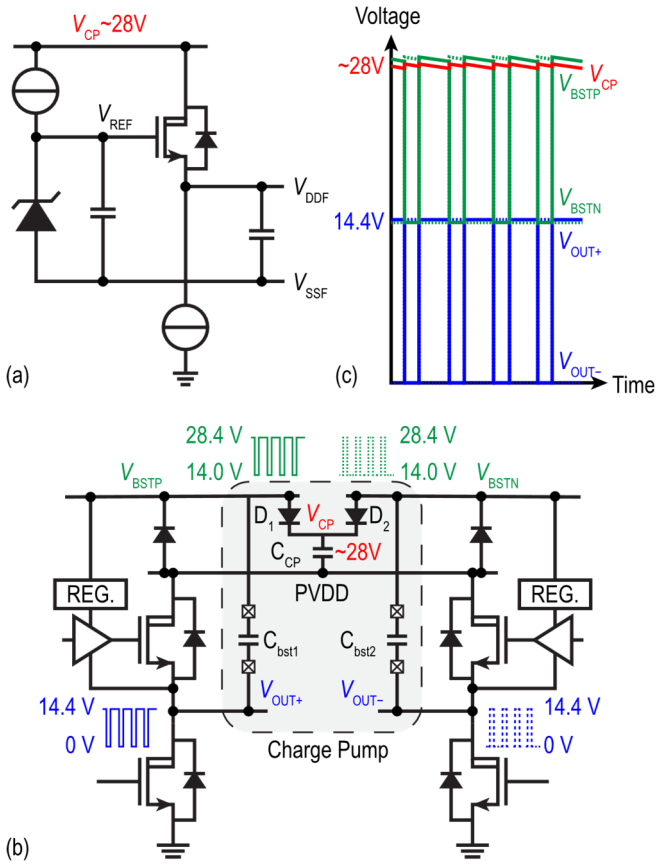


Fig. 4.10. (a) Floating regulator, (b) charge pump, and (c) its timing diagram.

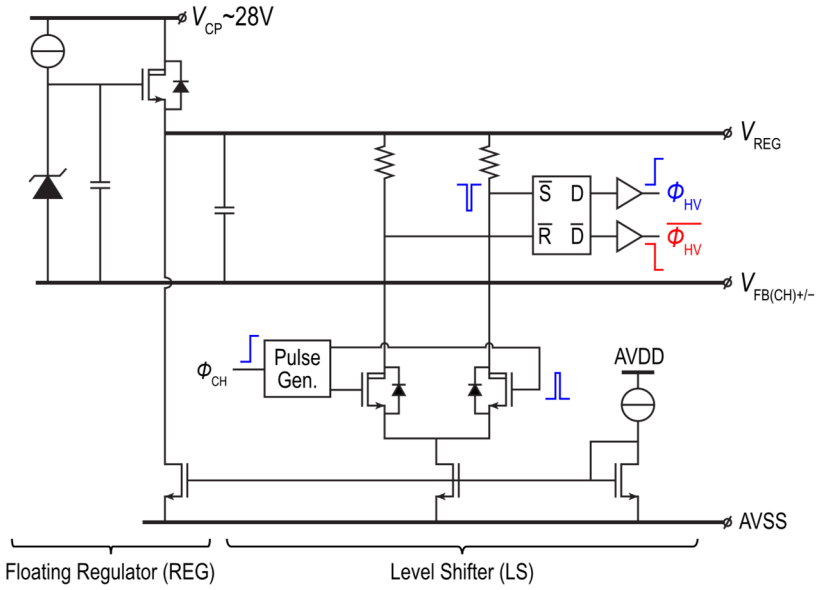


Fig. 4.11. Schematic of the floating regulator and level shifter. A replica of this circuit is used for timing skew correction.

4.3.3 Timing Skew Correction

In this capacitively coupled CDA, the timing skew due to level-shifter delay can cause the voltage across the virtual ground to temporarily exceed the supply range by up to 2 times (ignoring parasitic loading at V_X), as illustrated in Fig. 4.12(a) and Fig. 4.12(b). A replica-based timing skew correction circuit is employed to reduce the timing skew from more than 3 ns to within 200 ps [5].

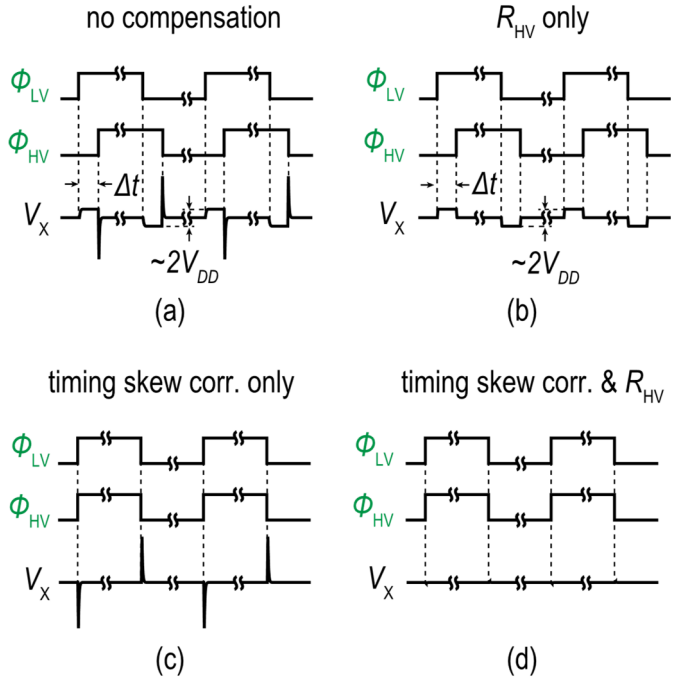


Fig. 4.12. Chopper clock and virtual ground waveform with (a) no timing skew and impedance compensation, (b) impedance compensation only, (c) timing skew correction only, and (d) both timing skew correction and impedance compensation.

4.3.4 Impedance Compensation

The on-resistance mismatch of the two choppers can also cause large transients at V_X, which is exacerbated by the need to upsize CH_{FB} to mitigate the large $1/f$ noise of LDMOS transistors [Fig. 4.12(a) and Fig. 4.12(c)]. The gate length is fixed for n-channel LDMOS transistors in this process, so their width must be increased. According to simulations, an on-resistance of about 10 Ω for each set of back-to-back switches is required to keep their total $1/f$ noise contribution below 10%. This problem is addressed by adding a series resistance R_{HV} (= 2.4 kΩ) to match the resistance ratio of the input and feedback paths to the ratio of their capacitive impedance (1:8), assuming low source impedance ($\ll 300\,\Omega$) at the CDA input. If a source with higher output impedance is used, two external resistors in series with C_{FB} can be employed.

Some residual mismatch is acceptable as long as the swing of the residual glitches at V_X, illustrated in Fig. 4.12(d), does not lead to oxide damage, and the resulting transient at the output of A_1 settles before the deadband ends. The deadband, nominally 25 ns long, is generated by an RC timer, while the same type of component is used in A_1's constant-g_m biasing circuit to ensure settling within the deadband across PVT.

Fig. 4.13 shows the simulated waveform at V_X and the output of A_1 under process and temperature variations during a chopping event. The swing at V_X is well within the supply range, while the glitch at the output mostly settles within 25 ns, which is limited by the bandwidth of the preamplifier.

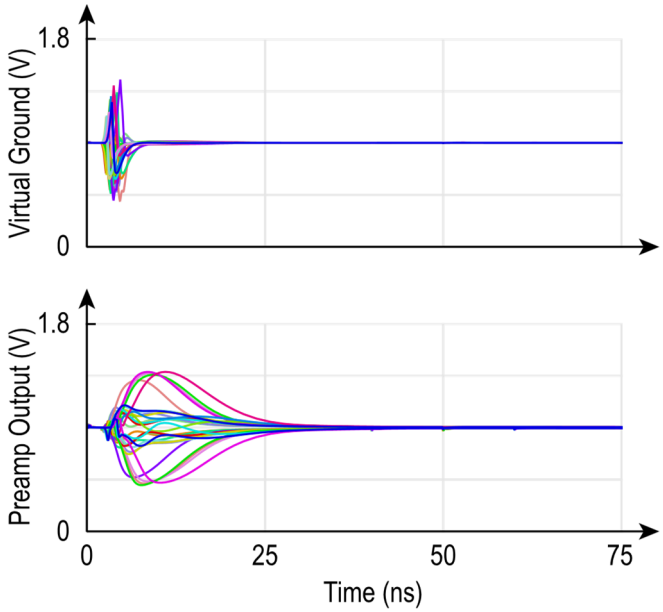


Fig. 4.13. Transient waveform at the virtual ground and output of the preamplifier during a chopping transition.

4.3.5 CDA

As shown in Fig. 4.14, the rest of the loop filter stages employ active-RC topology for high linearity. The 2.1 MHz triangle wave required for PWM is generated by a differential oscillator. The output stage employs a three-level topology with constant output common mode for low idle power. Amplifiers A_2 to A_4 in the loop filter, the differential oscillator, and the output stage are reused from Chapter 2.

The triangle wave's peaks and zero-crossings are extracted to create a 4.2 MHz digital clock, which is then divided by 21 to generate a 200 kHz clock with a 50% duty cycle for chopping.

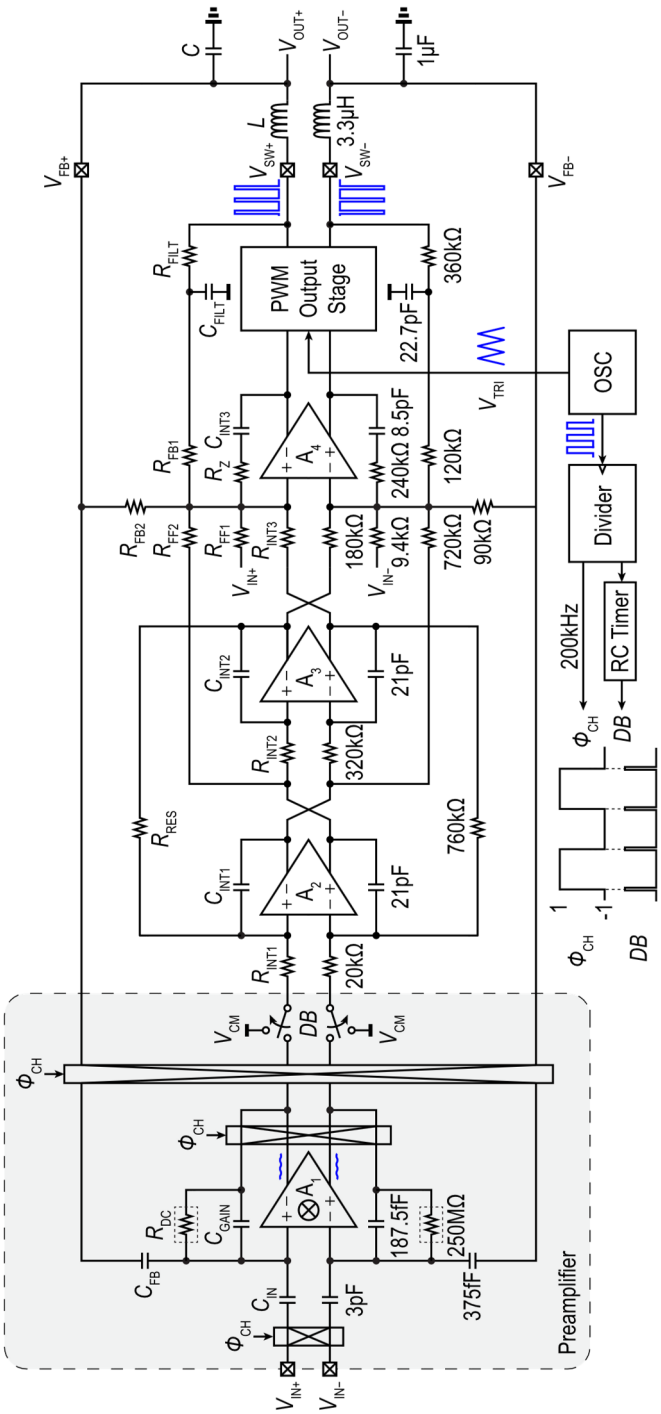


Fig. 4.14. Top-level schematic of the proposed capacitively coupled CDA.

4.4 Measurement Results

A prototype of the proposed capacitively coupled CDA is implemented in a 180 nm BCD process. Fig. 4.15 shows a photo of the die, which occupies 7 mm^2. The output stage employs a 14.4 V supply (PVDD), while the rest, including the loop filter, oscillator, and timing, operates from a 1.8 V supply (AVDD). The quiescent current drawn from AVDD is 7 mA, in which the preamplifier draws 1 mA. The HV chopper draws about 1 mA from PVDD. An Audio Precision APx555 Analyzer generates the input and captures the output of the CDA.

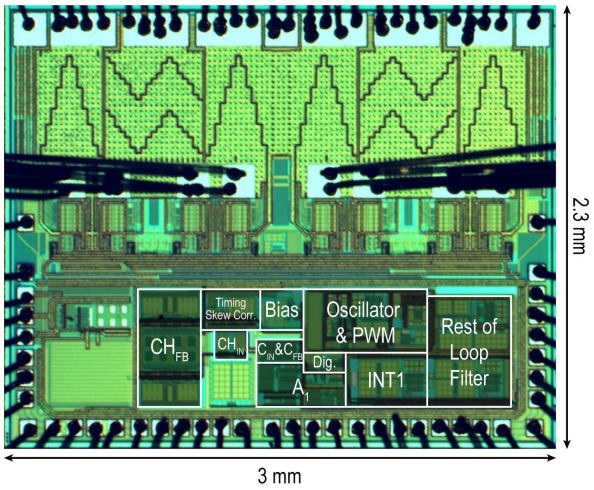


Fig. 4.15. Die photo.

Fig. 4.16(a) shows the measured output spectrum when the CDA delivers 1 W into an 8-Ω load, corresponding to −10 dBFS. In this case, the measured THD+N is −109.6 dB. Fig. 4.16(b) shows the result for a 4-Ω load at the same output swing, where the THD+N is −109.8 dB.

Fig. 4.17 shows the output spectrum with a −80 dBFS input, where the measured SNR is 41.4 dB, indicating that the prototype achieves a DR of 121.4 dB. The measured A-weighted integrated output noise is 8 μV_{RMS}.

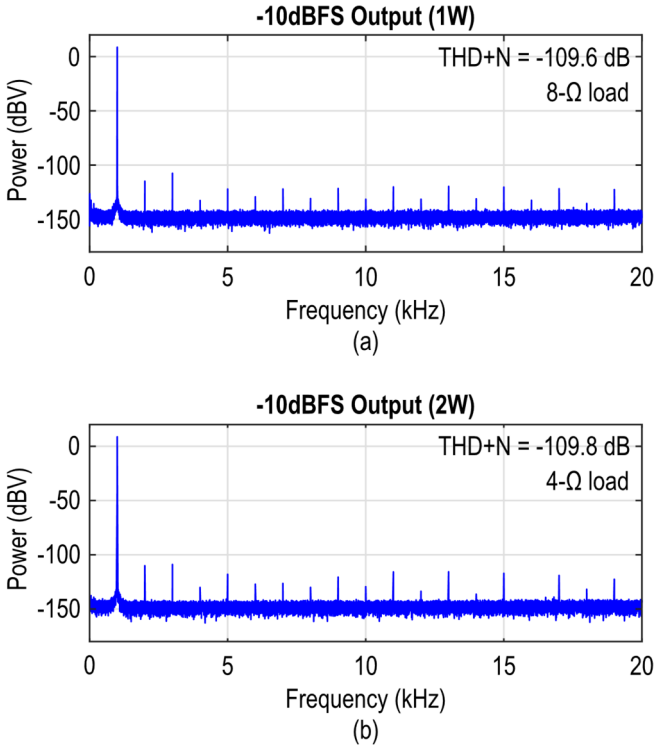


Fig. 4.16. Measured output spectra at −10 dBFS for (a) 8-Ω load and (b) 4-Ω load.

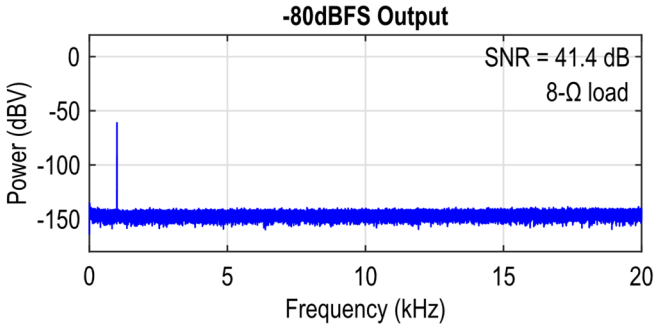


Fig. 4.17. Measured output spectrum at −80 dBFS.

Fig. 4.18(a) shows the measured THD+N across output power levels with both 8-Ω load and 4-Ω load. In both cases, the peak THD+N is about −110 dB. The maximum output power (defined at 10% THD) is 15 W and 26 W for 8-Ω and 4-Ω loads, respectively. The noise floor, which dominates over

distortion at small signal amplitudes, is about 10 dB lower than that contributed by a pair of 20-kΩ resistors, which is common for conventional resistive-feedback CDAs [12], [21]. The THD stays below −100 dB until the point of clipping. Fig. 4.18(b) plots the measured THD+N across input frequency, which is between −108.8 dB and −113.5 dB.

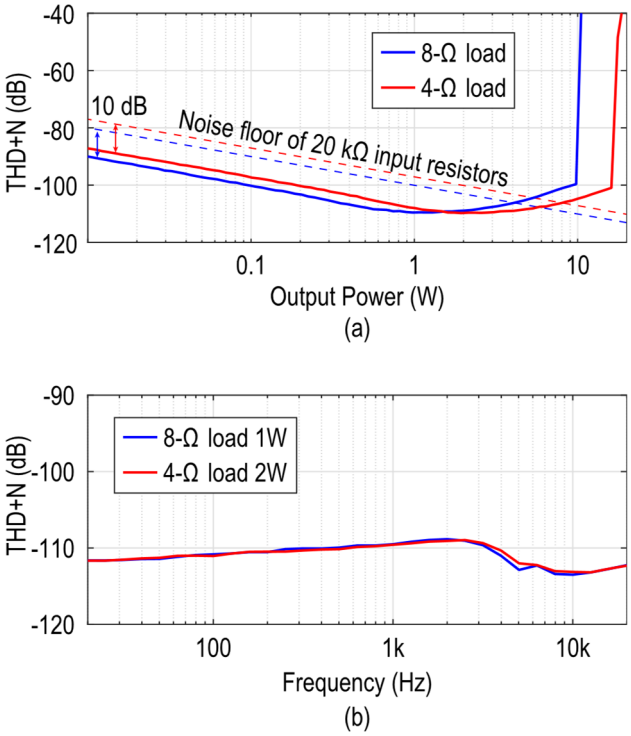


Fig. 4.18. Measured THD+N across (a) output power and (b) input frequency.

Fig. 4.19 shows the spectrum measured from a two-tone test. At an output power of 0.5W, the IM3 is about −110 dB.

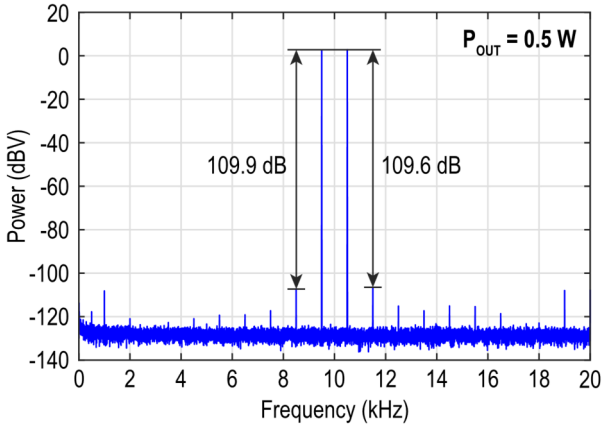


Fig. 4.19. Measured spectrum from a two-tone test.

Fig. 4.20 shows the measured THD+N and DR for 6 samples. The peak THD+N varies by less than 1 dB for an 8-Ω load and less than 2 dB for a 4-Ω load. The DR is within 0.5 dB for all samples.

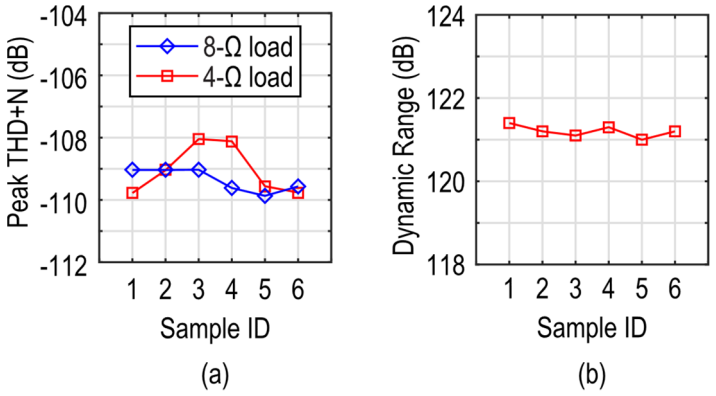


Fig. 4.20. (a) THD+N and (b) DR for 6 samples.

To evaluate the noise folding effect of the deadband, the deadband duration is made programmable. Fig. 4.21 shows the measured THD+N and DR while varying the deadband duration. When the deadband duration is intentionally reduced, linearity degrades as a portion of the nonlinear chopping glitches propagates down the loop filter. On the other hand, when the deadband is

lengthened, the DR degrades due to increased noise folding without much improvement in linearity, as mentioned in Section II-B. Hence, the nominal setting achieves the optimal tradeoff between DR and THD+N.

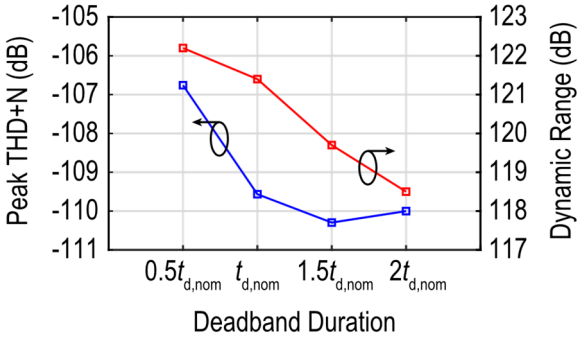


Fig. 4.21. Peak THD+N (left axis) and DR (right axis) for different deadband settings.

Fig. 4.22 shows the measured power efficiency. The peak efficiency is 93% and 88% for 8-Ω and 4-Ω loads, respectively.

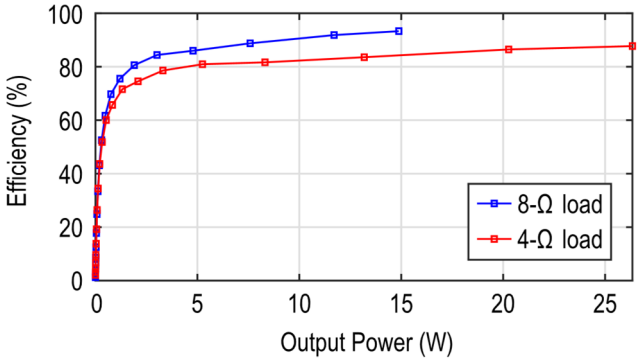


Fig. 4.22. Measured power efficiency across output power.

Fig. 4.23 plots the PSRR measured from 6 samples. The worst-case PSRR is 89 dB at low frequencies. The degraded PSRR compared to [5] was traced to the mismatch of the near-minimum-width resistor pair R_{FB2} (Fig. 4.14). Supply noise thus leaks into the differential signal present at the input of the

3rd integrator, which, in this design, is only suppressed by about 30 dB, as shown in Fig. 4.5.

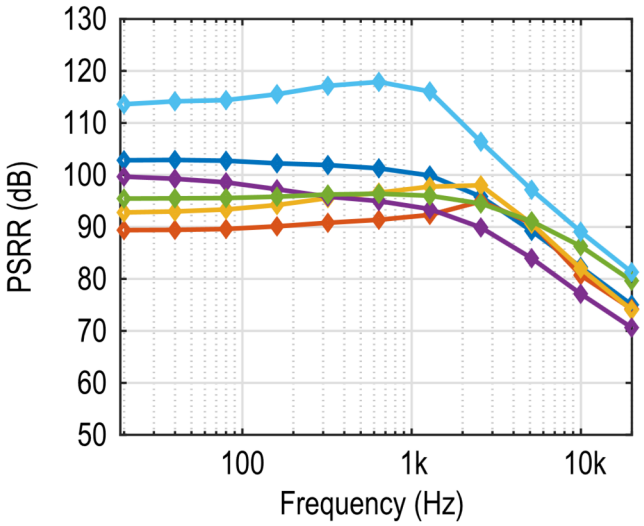


Fig. 4.23. Measured PSRR across the audio band for 6 samples.

Table 4.1 summarizes the prototype's performance and compares it with state-of-the-art CDAs, including both analog-input and digital-input ones. Thanks to the capacitively coupled architecture, this work achieves 5.9 dB higher DR, 2.4× lower A-weighted integrated output noise, and 2.5 dB better peak THD+N. Meanwhile, it achieves competitive efficiency, idle power, and PSRR among HV (>10V) CDAs.

Table 4.1. Performance summary and comparison.

	This Work	TPA3255 [5]	Sun ISSCC'22 [16]	Zhang JSSC'22 [7]	Karmakar JSSC'20 [10]	Cope ISSCC'18 [11]	Schinkel JSSC'17 [12]	Wang JSSC'10 [15]
Process	**180 nm BCD**	-	0.5 µm CMOS	180 nm BCD	180 nm BCD	180 nm BCD	130 nm BCD	65 nm CMOS
Architecture	**Analog-In**	Analog-In	Digital-In	Analog-In	Analog-In	Digital-In	Digital-In	Digital-In
Feedback Network	**Capacitive**	Resistive	Resistive(1)	Resistive	Resistive	Resistive	Resistive	N.A.
Supply (V)	**14.4**	51	0.625~5	14.4	14.4	8~20	14/25	3
R_{LOAD} (Ω)	**8/4**	4	8	8/4	4	8	4	8
$P_{OUT,MAX}$ (W)	**15/26**	315	1.5	12/21	28	20	80	0.4
Efficiency	**93%/88%**	~90%(2)	81	91%/87%	91%	90%	>90%	88
$I_{Q,PVDD}$ / Channel (mA)	**9**	24	2.4	8	17	21	-	2.4
$I_{Q,AVDD}$ / Channel (mA)	**7**	30	-	-	-	-	-	-
THD+N (dB)	**-109.6/-109.8**	-84	-95.4	-107.1/-105.6	-102.2	-97.7	-88.6	-94(2)
DR	**121.4**	113	121	110(3)	109	115.5	115	120
A-wt. Output Noise (μV_{RMS})	**8**	85	3.15	-	31	20	19/34	1.7
PSRR (dB) (Frequency/Hz)	**89~71 (20~20k)**	>65 dB -	100 (217)	-	70~62 (20~20k)	80~50 (20~20k)	90~60** (20~20k)	82 (1k)

(1) Feedback only enabled at high output power
(2) Estimated from graph
(3) SNR number used

4.5 Conclusion

In conclusion, a capacitively coupled chopper Class-D audio amplifier is presented, which enables significant improvement in the DR. To protect thin-oxide devices, HV chopping transients are addressed through timing and impedance matching. Deadbanding is applied to suppress the residual glitches and maintain high linearity. Thanks to the low-noise capacitively coupled chopper preamplifier in the loop filter, the 180 nm prototype achieves 8 μV_{RMS} of A-weighted integrated noise and 121.4 dB DR.

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Chapter 5 A 120.9dB DR Digital-Input Capacitively Coupled Chopper Class-D Audio Amplifier[1]

5.1 Introduction

Due to the digital format of most modern audio sources, digital-input CDAs are preferred to their analog counterparts. Their monolithic integration reduces system size and cost, and their input is much more robust to interference than an analog-input CDA [1]. However, while the dynamic range (DR) and THD+N performance of analog-input CDAs have been significantly improved recently [2], [3], [4], [5], [6], and as described in Chapter 2 to Chapter 4, less progress in these respects has been made for monolithic digital-input CDAs, whose THD+N remains above −100 dB and DR limited to about 115 dB [7], [8], [9], [10].

In prior closed-loop digital-input CDAs, the output is sensed using resistors, which necessitates the use of an IDAC or RDAC in the analog/digital interface, which introduces thermal and $1/f$ noise. Furthermore, since their analog loop filter or feedback ADC is typically implemented in a low-voltage (LV) domain, a resistive divider [8] or common mode regulation loop [7] is required to protect the LV circuitry from the high-voltage (HV) CDA output, which adds more noise. Reducing noise by increasing the DAC's output current would not only increase power consumption but also require larger integration capacitors in the loop filter. To overcome these limitations, the capacitively coupled chopper CDA architecture introduced in Chapter 4 can

[1]This chapter is based on the journal paper: H. Zhang, M. Berkhout, K. A. A. Makinwa, and Q. Fan, "A 120.9-dB DR Digital-Input Capacitively Coupled Chopper Class-D Audio Amplifier," *IEEE J. Solid-State Circuits*, vol. 58, no. 12, pp. 3470-3480, Dec. 2023.

be used, which eliminates the noise contribution from the resistive feedback network. Additionally, the use of chopping largely eliminates the $1/f$ noise from the loop filter, and its feedback-after-LC structure suppresses the LC filter's distortion.

In this chapter, a digital-input CDA based on the capacitively coupled chopper amplifier (CCCA) topology is presented, which achieves a DR of 120.9 dB and a THD+N of −111.2 dB. Several challenges must be overcome to achieve such performance. The capacitive DAC (CDAC), which replaces the chopped capacitor input network in Chapter 4, could introduce distortion due to mismatch and intersymbol interference (ISI). Although similar CDAC structures have been employed in ADCs recently [11], [12], [13], [14], [15], their DR is much lower than the target of this work. Besides, high-frequency components of the DAC output can cause intermodulation distortion due to the presence of chopping and pulse-width modulation (PWM) in the system.

Section 5.2 presents an overview and design considerations of the digital-input capacitively coupled CDA. Section 5.3 presents the techniques adopted to mitigate DAC mismatch and ISI. Section 5.4 describes the circuit implementation of the closed-loop CDA. Measurement results are presented in Section 5.5, followed by a conclusion in Section 5.6.

5.2 Digital-Input Capacitively Coupled Chopper CDA

5.2.1 Overview

Fig. 5.1 presents an overview of the proposed digital-input capacitively coupled CDA. The digital input is upsampled to $f_S = 768\,\text{kHz}$ and truncated to 8-bit by a digital delta-sigma modulator (DSM). The DSM output (D_{IN}) then drives a CDAC, which feeds into the virtual ground of a capacitively coupled chopper CDA. The CDA employs a 14.4-V multilevel PWM-based

output stage and has a closed-loop gain of 8 (as in Chapter 4). Its front end consists of a preamplifier, implemented as a CCCA, which amplifies the error signal ($V_{ERR} = D_{IN}V_{REF} - V_{OUT}/8$), thus suppressing the noise from the subsequent loop filter. However, due to the preamplifier's finite slew rate, chopping and DAC transitions cause nonlinear transients at the CCCA's output. Thus, a 20 ns deadband is introduced to block them from the loop filter. Driving the capacitively coupled CDA by a CDAC presents several additional challenges. The CDA's internal swing is increased by the presence of high-frequency components in the DAC output waveform. Additionally, distortion can arise due to DAC mismatch, intersymbol interference (ISI), and the intermodulation between chopping, DAC, and PWM operations. These issues will be discussed in detail in the following sections.

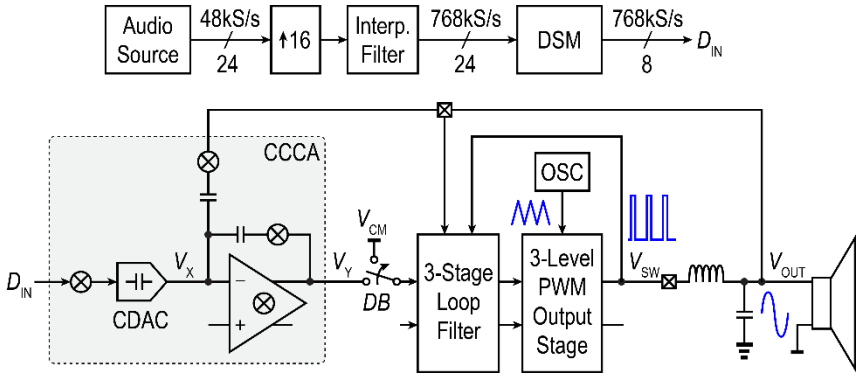

Fig. 5.1. Architecture of the proposed capacitively coupled digital-input CDA.

5.2.2 DAC Sampling Frequency

In this work, a non-return-to-zero (NRZ) DAC is chosen for its high immunity to clock jitter. In contrast to the analog input of the CDA in Chapter 4, the DAC output contains high-frequency components, including out-of-band quantization noise and DAC image, which increases the preamplifier's output swing. While quantization noise can be reduced by increasing the DAC resolution, the DAC image is still amplified by the loop filter's preamplifier,

leading to a sawtooth-like waveform at its output V_Y, as illustrated in Fig. 5.2. To maintain high linearity, the DAC image should not exceed the linear output range of the CCCA.

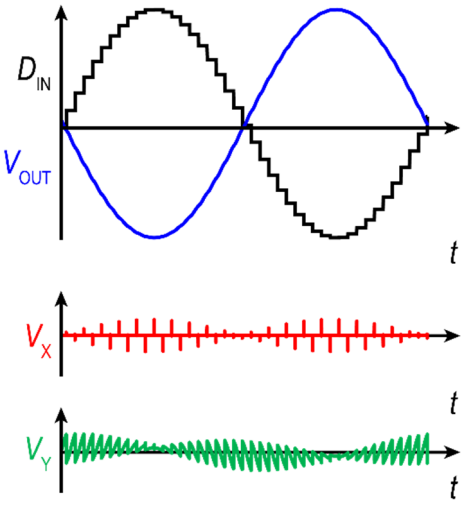

Fig. 5.2. Waveform of the CDA input, output, and CCCA output with respect to the full scale.

For a full-scale sinewave signal $u(t) = \sin(2\pi f_{IN} t)$, the peak swing of the DAC image (before being amplified by the CCCA) can be approximated by:

$$V_{IMAGE,PP} \approx \max\left|\frac{du}{dt}\right| \cdot \frac{1}{f_S} = \frac{2\pi f_{IN}}{f_S} \le \frac{\pi}{OSR}. \tag{5.1}$$

Hence, it can be reduced by increasing the DAC's sampling frequency f_S. Fig. 5.3. Peak-to-peak swing of the DAC image for different choices of f_S and CCCA gain. Fig. 5.3 shows the preamplifier's output swing, normalized to its 1.8 V supply, for different choices of f_S under a worst-case 20 kHz full-scale input, assuming infinite DAC resolution. To ensure enough suppression for the loop filter noise, a gain G of about 8 is required for the preamplifier. While $G = 16$ as in Chapter 4 is also possible, it would require a higher f_S

and thus a higher clock frequency for the dynamic element matching (DEM) logic (Section 5.3.2).

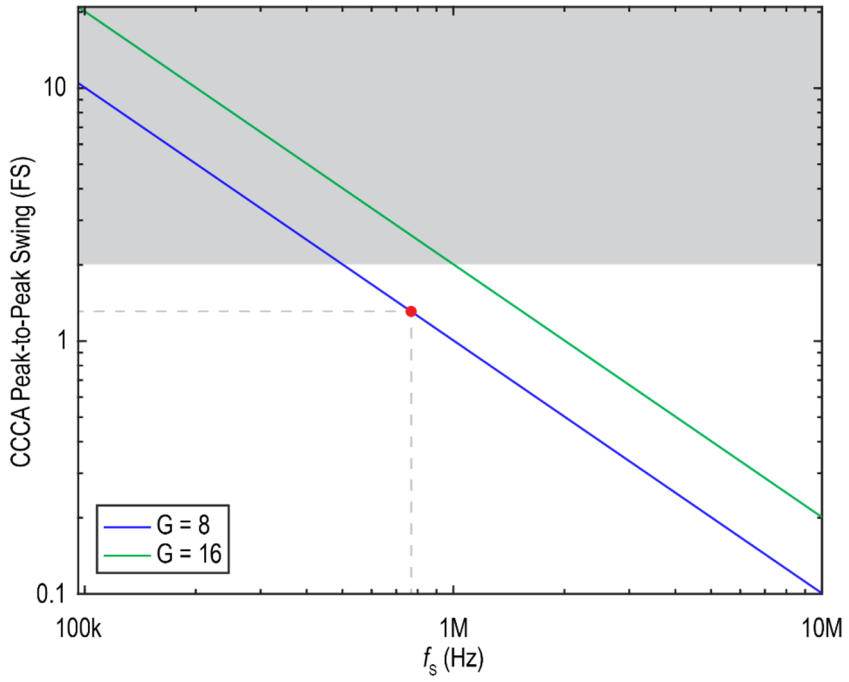

Fig. 5.3. Peak-to-peak swing of the DAC image for different choices of f_S and CCCA gain.

5.2.3 DAC Resolution

Besides the DAC image, shaped quantization noise also consumes the preamplifier's output swing, which is a function of the DAC resolution and out-of-band gain (OBG) of the DSM's NTF [16]. By choosing a relatively low OBG, a peak-to-peak quantization noise swing of 2 LSB can be achieved. Therefore, the extra swing due to quantization noise is given by $G / 2^{N_{\mathrm{DAC}}-1}$ LSB, where N_{DAC} is the DAC's resolution in bits. According to behavioral simulations, the shaped quantization noise can fit into the remaining output swing of the preamplifier as long as the DAC's resolution is more than 6 bits.

However, the DAC's resolution also impacts the linear output range of the overall CDA due to the following. The capacitively coupled CDA employs feedback after the LC filter to suppress the latter's nonlinearity as well as the rail-to-rail switching edges produced by the output stage, which would otherwise saturate the preamplifier. To suppress the LC filter nonlinearity by about 50 dB, a feedback loop with a unity gain frequency of about 500 kHz is employed around the LC filter (as in Chapter 3), whose cutoff frequency is about 88 kHz (L = 3.3 µH, C = 1µF). Fig. 5.4 plots the simulated waveform after a DAC input step. For clarity, the PWM output stage is replaced with a linear model [17]. As shown, the LC filter output follows the DAC input step with a rise time of about 2 µs, requiring an overshoot at the LC filter's input ($V_{SW,AVG}$) that is about 6 times $(\approx 500 \div 88)$ larger, thus consuming part of the output stage's signal range. Since the DAC input can change by up to 2 LSBs at once, for keeping this loss within 0.5 dB (≈ 5.6% FS), the DAC's LSB size must be less than 5.6/2/6 ≈ 0.47% FS. Therefore, $N_{DAC} = 8\,\text{bit}$ is chosen.

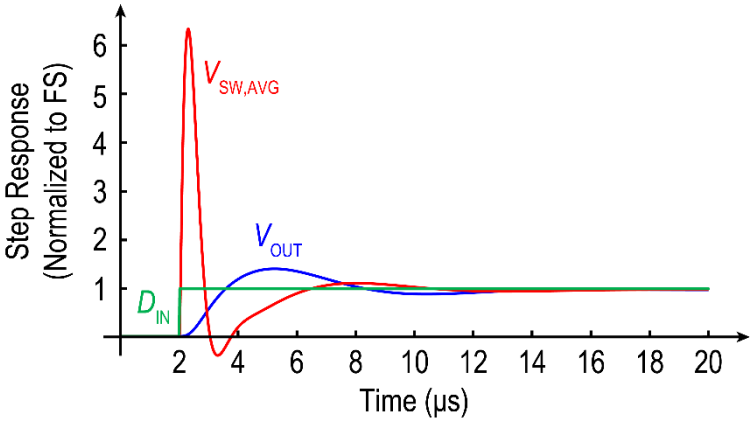

Fig. 5.4. Simulated step response from the input (D_{IN}) to the LC filter input ($V_{SW,AVG}$) and output (V_{OUT}).

5.2.4 Intermodulation

Chopping can demodulate DAC's out-of-band noise at even multiples of the chopping frequency f_{CH}, which can significantly degrade the SNR [11], [12], [18], [19]. In this work, spectral nulls at multiples of f_S are exploited to mitigate chopping-induced noise folding [11] and $f_{CH} = f_S / 2 = 384\,\text{kHz}$ is adopted. This also allows the chopping and DAC transitions to coincide, allowing a simple way to eliminate nonlinear transients due to chopping and DAC settling, which will be explained in detail in Section 5.3. Chopping also demodulates PWM sidebands and degrades the THD, which can be avoided by choosing f_{PWM} to be an odd harmonic of f_{CH}. A factor of 13 is chosen in this work, implying an f_{PWM} of 4.992 MHz.

Given $f_{PWM} = 6.5 f_S$, the DAC's shaped quantization noise in the 6th Nyquist zone is present around f_{PWM}. The PWM operation could potentially demodulate this noise to the baseband. Fortunately, this intermodulation is introduced at the output of the loop filter and thus suppressed by the loop gain, which is above 80 dB (Chapter 3). Hence, the impact on SNR is negligible.

5.3 DAC Implementation

5.3.1 Delta-Sigma Modulator Design

The digital DSM is designed using the Schreier Toolbox [20]. The requirement is to achieve sufficient SQNR while restricting the maximum input step to 2 LSB. Simulations show that, given the abovementioned choice of $f_S = 768$ kHz and $N_{DAC} = 8$ bit, an NTF of 6th order or higher is required. In this work, a 6th-order modulator is used, which has an OBG of 2.4, as shown in Fig. 5.5. A higher-order NTF with a lower OBG could also have been used. To ensure the absence of idle tones, its quantizer is dithered using

an LFSR-based pseudorandom generator, at the expense of 3 dB lower SQNR. The resulting SQNR is 133 dB.

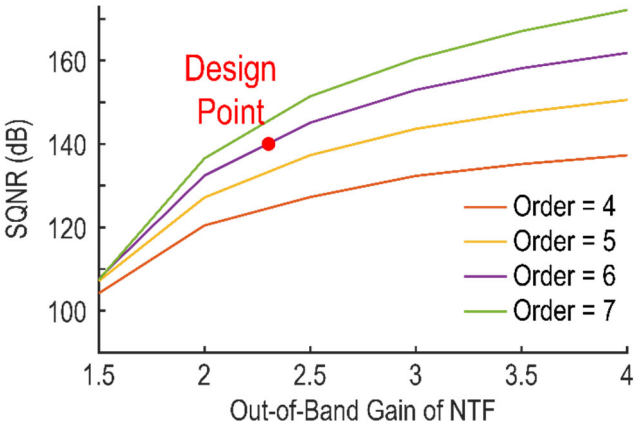

Fig. 5.5. SQNR as a function of the NTF's OBG for an 8-bit DSM with an OSR of 19.2.

5.3.2 Dynamic Element Matching (DEM)

Unit-element mismatch in the 8-bit CDAC causes significant distortion and quantization noise fold-back, so it must be addressed using DEM. Conventional DEM techniques like data-weighted averaging (DWA) are based on unary DAC elements, leading to high digital complexity given the 8-bit DAC resolution. While the segmented tree DEM [13], [14], [21], [22] simplifies the logic, it still offers only 1st-order shaping, introducing significant in-band mismatch noise and degrading the DR. In [15], this limited the DR to below 95 dB at an OSR of 40. In comparison, this work targets 120 dB DR with an OSR of only 19.2. Therefore, 1st order mismatch shaping is insufficient for this work[1], and the real-time DEM (RTDEM) technique [23], [24] is employed instead since it averages out the mismatch error *within* each sample period. However, conventional RTDEM is based on unary

[1] Matlab simulations show that the residual mismatch noise is enough to degrade the DR of this design even using an f_S as high as 10 MHz.

elements, which would require high logic complexity and a clock frequency of about 200 MHz ($\approx 2^8 \times f_S$).

5.3.2.1 Noise-Shaped Segmentation

To reduce the complexity and clock frequency of the RTDEM logic, noise-shaped (NS) segmentation is employed [10], [24], [25], [26]. As shown in Fig. 5.6, the 8-bit DAC input D_{IN} is processed by a second digital DSM to yield a 5-bit word (D_1) that controls an MSB DAC segment. The quantization noise introduced in D_1 is canceled by an LSB DAC segment driven by $D_2 = D_{IN} - D_1$. The total DAC output is given by

$$\begin{aligned} V_{DAC,OUT}(z) &= G_1 D_1(z) + G_2 D_2(z) \\ &= G_1[D_{IN}(z) - D_2(z)] + G_2 D_2(z) \\ &= \underbrace{G_1 D_{IN}(z)}_{\text{ideal output}} + (\underbrace{G_2 - G_1}_{\Delta G}) \cdot \underbrace{D_2(z)}_{-Q_{SEG}(z)\mathrm{NTF}_{SEG}(z)}, \end{aligned} \tag{5.2}$$

where G_1 and G_2 are the normalized gain from D_1 and D_2 to the DAC output, respectively, ΔG is the gain mismatch between the 8x and 1x DACs, Q_{SEG} is the unshaped quantization noise of the DSM in Fig. 5.6, and $\mathrm{NTF}_{SEG}(z)$ is its NTF.

In [10], [24], [25], 1st-order NS segmentation is employed. However, the 1st-order DSM exhibits "frequency-modulated idle tones" [27], causing D_2 to include harmonics of the input, which will degrade the output spectrum. To mitigate this effect, 2nd order NS segmentation [28] is employed in this work, which is less prone to tonal behavior. The 2nd-order $\mathrm{NTF}_{SEG}(z)$ also reduces the in-band power of D_2, hence its contribution to $V_{DAC,OUT}$ by about 20 dB. Since the 2nd-order NTF has higher out-of-band power than a 1st-order one, D_2 spans 32 LSBs, thus requiring a 5-bit LSB DAC.

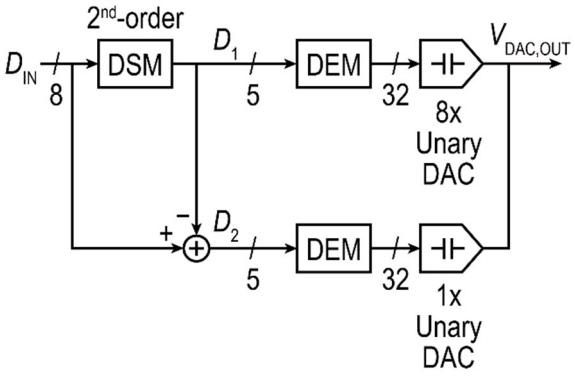

Fig. 5.6. The 2nd-order NS segmentation scheme employed in this work.

5.3.2.2 Real-Time DEM

The mismatch error within each DAC segment is addressed using RTDEM [23], which avoids the idle tone issue and SNR degradation of DWA. Fig. 5.7(a) plots the element selection pattern of RTDEM. The operation of a 3-bit DAC is illustrated for simplicity. In general, for a DAC with N_E unit elements, each sample period is evenly divided into N_E sub-intervals, defined by a high-frequency master clock MCLK. Then, a thermometer code corresponding to the input is rotated at the MCLK frequency. Therefore, a full rotation is completed in a sample period, and each element is turned on for an equal amount of time.

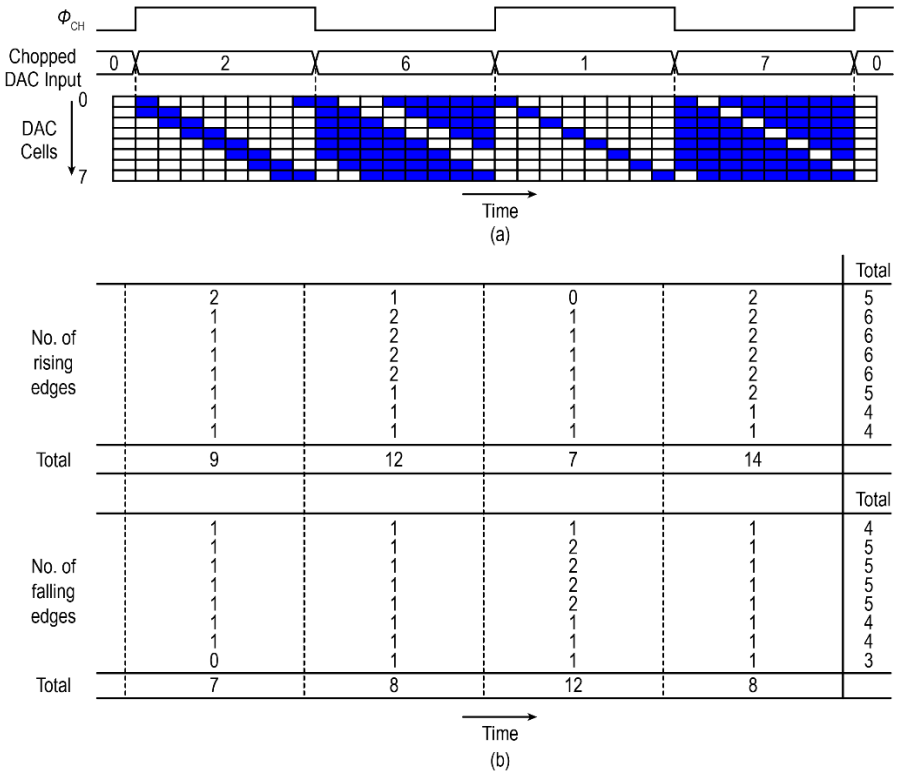

Fig. 5.7. (a) Usage pattern of unit elements with RTDEM (3-bit example), and (b) the number of rising and falling edges.

As shown in Fig. 5.7(b), if the input is chopped, the number of elements switching between two samples can be quite large, and the total number of rising and falling edges will be signal-dependent, causing nonlinear ISI [24]. To illustrate this, Fig. 5.8 shows the simulated output spectra of the MSB DAC for the cases where a unit element's rising edge or falling edge adds a 1% ISI error to its output in the subsequent sub-interval. The ISI clearly causes extra harmonics of the input signal.

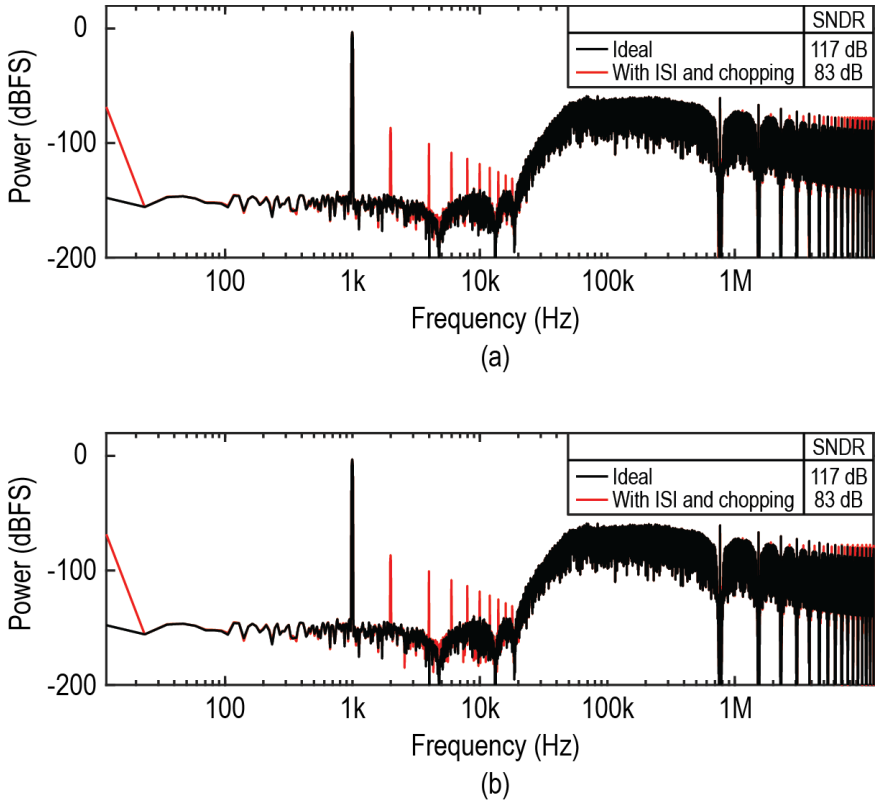

Fig. 5.8. Simulated MSB DAC spectrum of a chopped DAC with RTDEM assuming 1% ISI error on the (a) rising edges and (b) falling edges.

In this work, the dead-band switch at the preamplifier's output can also be used to mitigate this source of distortion since the DAC and the choppers can be configured to switch at the same time. As shown in Fig. 5.9(a), the dead-band is introduced as an additional MCLK cycle at the beginning of each DAC sample when the states of the unit elements are updated based on the new input code. Given the DAC and preamplifier's settling speed, a 20 ns deadband is sufficient, leading to an MCLK of ~50 MHz, which is $\sim 65 f_s$. Therefore, the unit-element inputs are rotated every other MCLK cycle. In the 2 MCLK cycles after the dead-band, the state of the unit elements is not changed. This ensures that they are all still equally used outside the deadband.

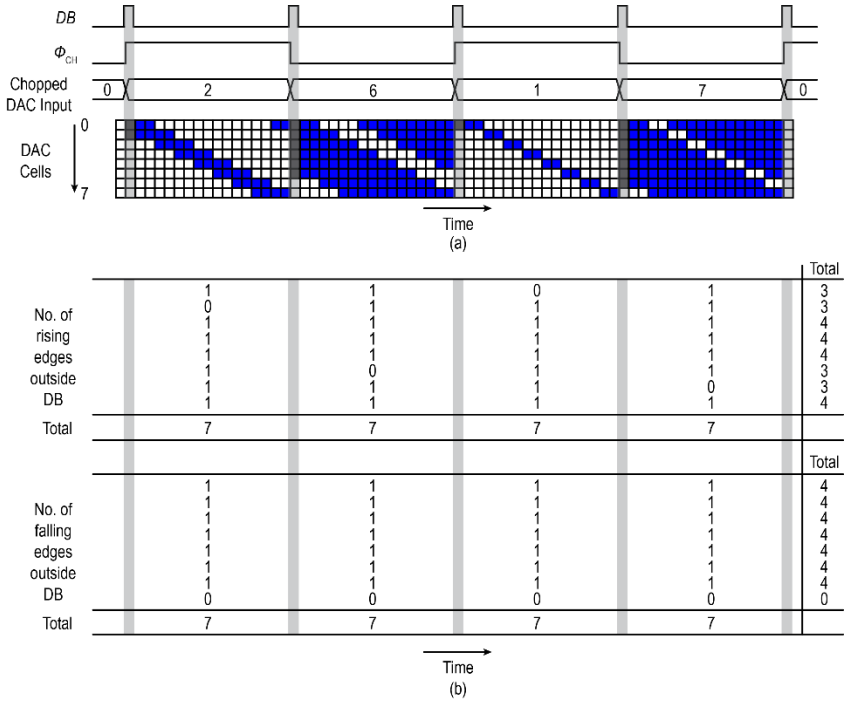

Fig. 5.9. RTDEM with deadband employed in this work (3-bit example), and (b) the number of rising and falling edges outside the dead-band.

With this approach, although the number of rising edges of each unit element outside the dead-band still varies with the input, the total number of transitions in each direction becomes signal-independent, as shown in Fig. 5.9(b). Therefore, the ISI distortion is only limited by the mismatch between the unit elements. According to transistor-level Monte-Carlo simulations, the ISI mismatch is ±0.006% (1σ) with respect to the unit element's output in one MCLK cycle. Therefore, the ISI distortion is reduced significantly, as shown in Fig. 5.10.

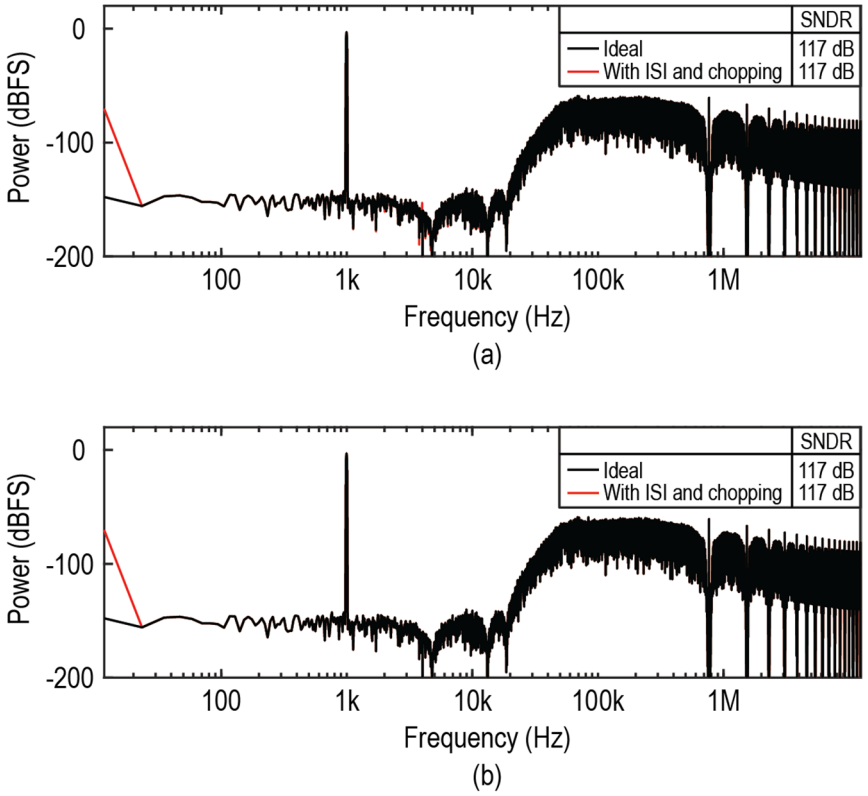

Fig. 5.10. Simulated MSB DAC output spectrum with ISI on the (a) rising edges and (b) falling edges, with the deadband, where the ISI error of each element follows a normal distribution with a mean of 1% and a standard deviation of 0.006%.

Although RTDEM turns on each unit element for an equal amount of time, their mismatch still leads to some residual errors. This is because each unit element is driven by phase-shifted PWM signals that have the same DC value but different spectra. This spectral distortion is inherent to the PCM-to-PWM operation [23], and its magnitude scales with input amplitude and increases with input frequency. In this work, it is about −72 dBc for a −1 dBFS input at 6 kHz. If the DAC had no mismatch and the timing was perfect, these distortion spectra cancel each other out, resulting in the spectrum of a perfect NRZ pulse. In practice, mismatch and timing errors cause a small portion of this distortion to appear at the output.

5.3.3 Clock Jitter

With the timing scheme described in Fig. 5.9, the DAC output effectively becomes a return-to-zero (RZ) waveform. It is well known that RZ DACs are sensitive to clock jitter. Jitter adds noise to the DAC output, which would then be amplified by the CDA. The situation here is, however, different since the deadband is applied to the *error signal* instead of the DAC output. This subsection discusses the impact of clock jitter on this work.

The noise due to the clock jitter can be decomposed into two components: that due to (a) the jitter of the deadband's position and (b) the jitter of the deadband's duration. The former is determined by the MCLK's absolute jitter, while the latter is determined by its period jitter. Note that the dead-band acts on the CCCA output. Therefore, noise introduced by both types of jitter is divided by the CCCA gain of 8 when referred to the input.

Since CCCA output is the amplified difference between the digital input and CDA output, the effect of positional jitter can be analyzed separately and then be evaluated using superposition, as shown in Fig. 5.11(a), which can be analyzed separately for the digital input and CDA output and then evaluated using superposition. As shown in Fig. 5.11(a), the impact on the digital input is much more than that on the CDA output. When the deadband is delayed by jitter, the output sees the previous sample longer and the next sample shorter. This introduces a noise at the DAC output given by:

$$v_{\mathrm{njp,DAC}}[n] = V_{\mathrm{REF}}(D_{\mathrm{IN}}[n+1] - D_{\mathrm{IN}}[n])t_{\mathrm{jp}}[n], \tag{5.3}$$

where $t_{\mathrm{jp}}[n]$ is the positional jitter of the deadband after the n-th DAC sample. This is the same expression as that for a conventional NRZ DAC. Matlab simulation predicts an SJNR of 131.5 dB for 100 ps of positional jitter.

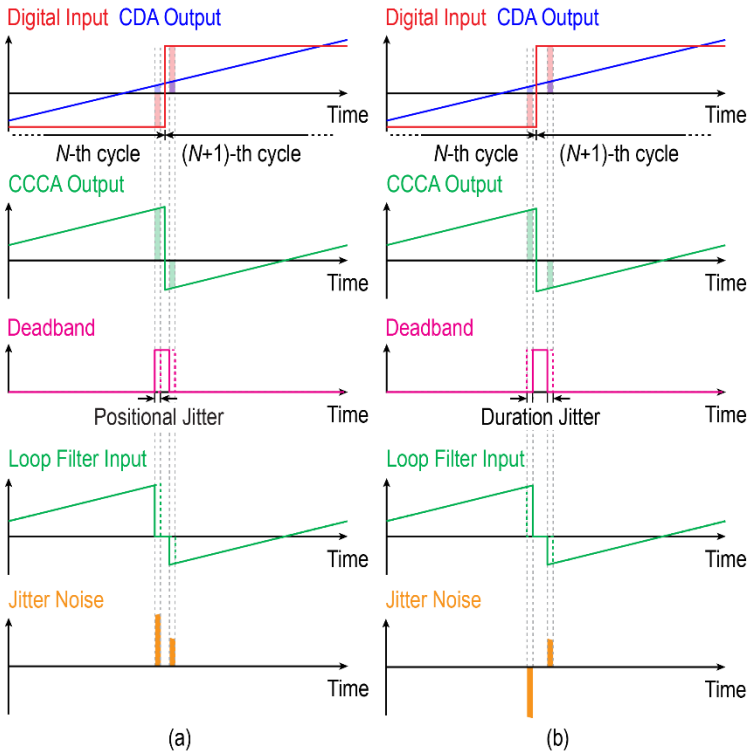

Fig. 5.11. Impact of clock jitter on the proposed DAC with deadband.

The positional jitter also affects when the loop filter sees the CDA output. This introduces a noise component given by:

$$v_{\mathrm{n,OUT,pj}}[n] = [V_{\mathrm{OUT}}(nT_{\mathrm{S}}) - V_{\mathrm{OUT}}(nT_{\mathrm{S}} + T_{\mathrm{MCLK}})]\frac{t_{\mathrm{pj}}[n]}{T_{\mathrm{S}}}$$
$$\approx -\frac{dV_{\mathrm{OUT}}(nT_{\mathrm{S}})}{dt} \cdot \frac{T_{\mathrm{MCLK}}}{T_{\mathrm{S}}} \cdot t_{\mathrm{pj}}[n], \tag{5.4}$$

where $T_{\mathrm{S}} = 1/f_{\mathrm{S}}$ and T_{MCLK} is the period of MCLK and also the duration of the deadband. Approximating the CDA output by a sinewave, the SNR due to this noise is given by:

$$10\log_{10}\left(\frac{\overline{V_{\text{OUT}}{}^2(nT_\text{S})}}{\overline{v_{\text{n,OUT,pj}}{}^2[n]}}\cdot\frac{1}{\text{OSR}}\right)$$
$$=10\log_{10}\left[\frac{1}{(2\pi f_\text{IN})^2\cdot\left(\frac{T_\text{MCLK}}{T_\text{S}}\right)^2\cdot\sigma_\text{pj}^2\cdot\text{OSR}}\right]. \tag{5.5}$$

In this work, $T_\text{MCLK}/T_\text{S}=1/65$ and $\text{OSR}=19.2$. Therefore, for $f_\text{IN}=20\text{kHz}$ and $\sigma_\text{pj}=100\text{ps}$, the SNR is 147 dB, so this source of noise is negligible.

Duration jitter, on the other hand, is more easily analyzed with the CCCA output waveform. As shown in Fig. 5.11(b), if the deadband is wider, error pulses are added to the CCCA output both before and after the deadband. Since the CDA output straddles the DAC input, the two error pulses mostly cancel each other because they often have opposite polarities. Matlab simulation predicts an SNR of 136 dB due to a 100-ps jitter, i.e., 0.5%, of period jitter on MCLK, in the deadband's duration.

Furthermore, in the RTDEM scheme, the jitter on MCLK slightly varies the contribution of each DAC element to the output, potentially impacting its efficacy. As mentioned previously, DAC mismatch and imperfect timing cause a small portion of the PCM-to-PWM distortion to leak into the output. Matlab simulations were performed to evaluate this effect. For a −1 dBFS input, with both 0.5% mismatch and 100 ps of MCLK jitter, the simulated SNR is 126 dB. For a −60 dBFS input, this noise is lower, and the simulated SNR is 72 dB.

5.4 Closed-Loop CDA

5.4.1 Top-Level

Fig. 5.12 shows a top-level schematic of the proposed digital-input capacitively coupled CDA. To stabilize the loop in the presence of the pair of complex poles introduced by the LC filter, the dual-loop structure of Chapter 3 is employed. The overall structure is similar to that of Chapter 4. The feedforward path from the input to the input of the 3rd integrator is omitted in this work to avoid the need for another DAC. As a result, the 2nd integrator must now process the full signal swing, and the 1st integrator's output swing increases by 6 dB/octave with respect to the input frequency. To maintain sufficient linearity for these two stages under the worst case of a full-scale input at 20 kHz, relatively large integration capacitors (80 pF) are employed to limit the swing of these integrators, consuming 6% of the total chip area. Process variations on the RC time constants are addressed by a 2-bit trim of the integration capacitors to keep them within 7% of their nominal values, as in Chapter 3.

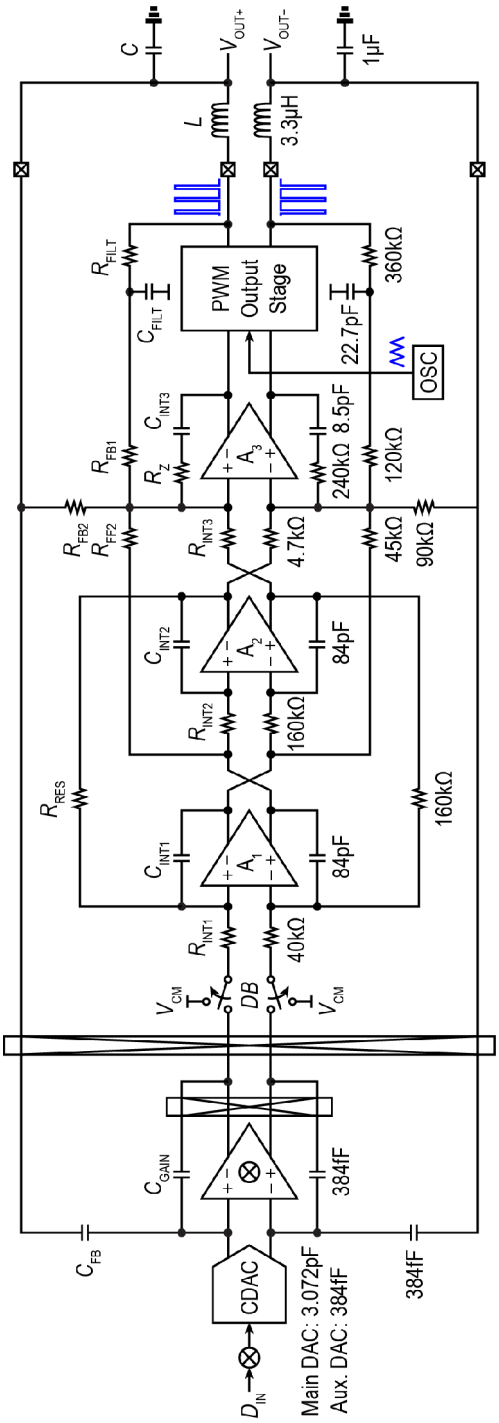

Fig. 5.12. Top-level schematic of the proposed digital-input capacitively coupled CDA.

5.4.2 Timing and RTDEM Logic

A high-frequency clock (MCLK) is required to define the sub-intervals for RTDEM, as shown in Section 5.3.2.2. The MCLK frequency is $f_{\mathrm{MCLK}} = 49.92\,\mathrm{MHz}$, which equals $65 f_{\mathrm{S}}$. For each DAC sample, one MCLK cycle is allocated for the deadband and the remaining 64 for RTDEM. In the prototype, the sampling clock f_{S} and chopping clock f_{CH} are divided down from MCLK using digital counters, as shown in Fig. 5.13. The PWM frequency $f_{\mathrm{PWM}} = f_{\mathrm{MCLK}} / 10$ is ensured by embedding the triangle wave oscillator in Fig. 2.11 into a charge-pump PLL [29]. The timing skew introduced in the HV feedback chopper is mitigated using a replica level shifter (Chapter 4). The RTDEM is realized by cyclic shift registers, as shown in the upper part of Fig. 5.13.

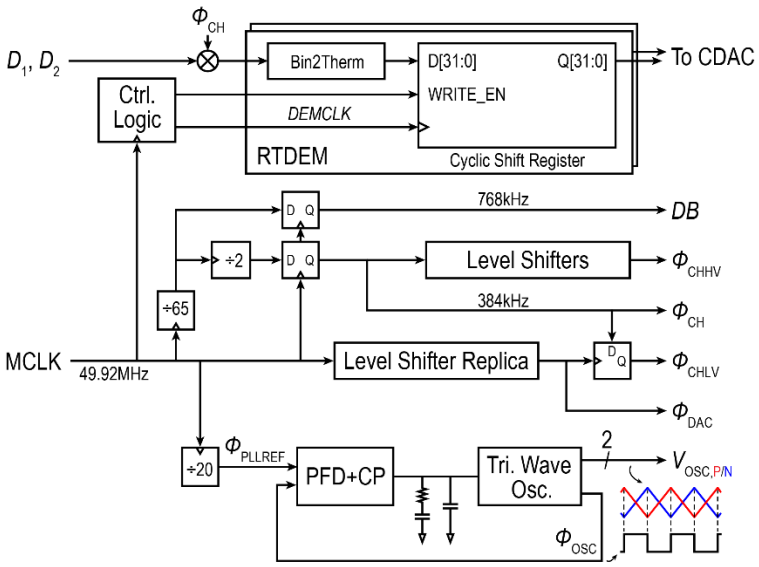

Fig. 5.13. Timing circuitry for chopping, RTDEM, and the deadband.

5.4.3 DAC

Fig. 5.14 shows a schematic of the DAC and CCCA[2]. The cyclic shifter register outputs are retimed by Φ_{DAC}, the output of the level shifter replica, to align the chopping transitions of the DAC output and HV feedback. A unit capacitance of 12 fF is chosen such that the total capacitance corresponding to the signal component $D_1(256C_U)$ dominates over the parasitic capacitance at the summing node. All capacitors connected to the summing node are implemented with custom MOM capacitors for their high voltage ratings and use the same 12 fF unit for good matching. As shown in Fig. 5.9, RTDEM always activates consecutive DAC elements. To minimize the effect of process gradient, a recursive layout pattern is employed for the unit elements [30].

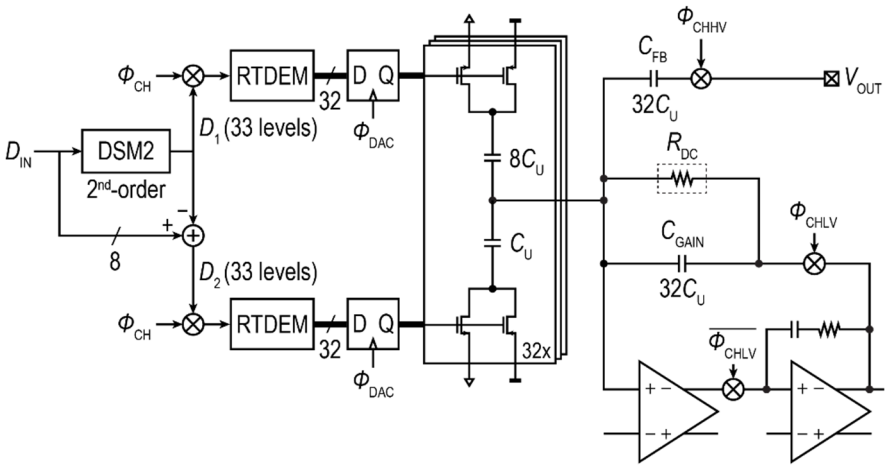

Fig. 5.14. Schematic of the DAC and CCCA.

[2] In Chapter 4, a resistor R_{HV} was added in series with each feedback capacitor C_{FB} to avoid over-voltage conditions at the virtual ground node due to impedance imbalance caused by the relatively high resistance of the input chopper. In this work, the input chopper is replaced with the parallel combination of all DAC switches, which has an equivalent resistance of <1Ω, much less than the on-resistance of the HV chopper. Therefore, a resistor in series with C_{FB} is no longer needed.

5.5 Measurement Results

A prototype of the proposed digital-input capacitively coupled CDA is fabricated in a 180 nm BCD technology. Fig. 5.15 shows a microphotograph of the die, which occupies 7.5 mm^2. During idle operation, it draws 200.2 mW from the 14.4-V output-stage supply (PVDD), 23.4 mW from the 1.8-V analog supply (AVDD, including loop filter, triangle wave oscillator, and PLL), 0.46 mW from the 1.8-V digital supply (DVDD, including timing logic), and 25 μW from the 1.8-V DAC reference. A 10 μF external decoupling capacitor is employed for the DAC reference, and care was taken in the PCB layout to minimize interference to the reference, which is driven by a commercial off-the-shelf linear regulator with a thermal noise floor of $2\text{nV}/\sqrt{(\text{Hz})}$. A commercial off-the-shelf crystal oscillator provides MCLK. For flexibility, the interpolation filter and digital delta-sigma modulators are implemented on an FPGA. Their synthesized area and power in the 180 nm BCD process would be $0.36mm^2$ and 350μW, respectively. An Audio Precision APx555B audio analyzer provides a 24-bit digital input and captures the CDA output.

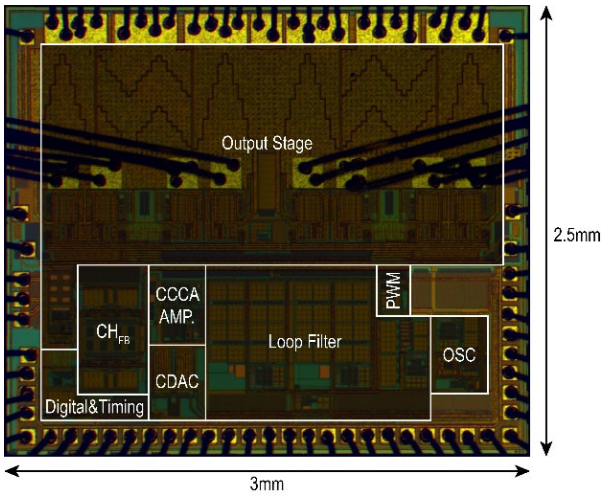

Fig. 5.15. Die micrograph.

Fig. 5.16(a) shows the output spectrum when the CDA drives 1 W into an 8-Ω load, corresponding to about −10 dBFS. The measured THD+N is −108.6 dB, and the SNR is 110.3 dB. Fig. 5.16(b) plots the output spectrum for a −60 dBFS input, showing a clean spectrum. An SNR of 60.9 dB is observed, indicating a DR of 120.9 dB for the CDA[3].

[3] This method of determining the DR is consistent with prior works on digital-input audio drivers [9], [10], [24], [31], [32].

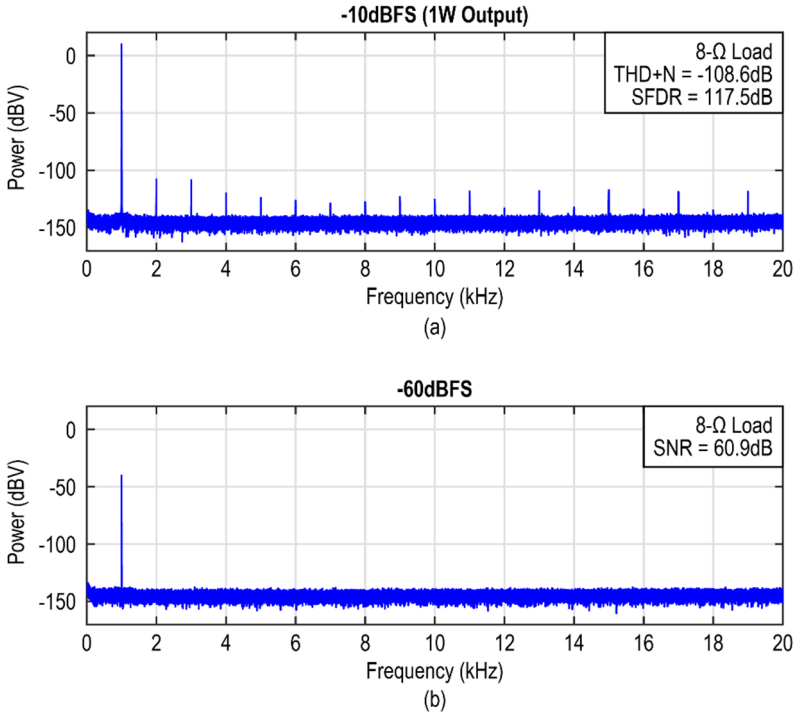

Fig. 5.16. Measured output spectra (256k-point FFT, 4x averaged).

A test mode was implemented to evaluate the effect of 1st-order NS segmentation, whose result is shown in Fig. 5.17. Harmonics at the −80 dBc level due to the “frequency-modulated idle tones” [27] are clearly visible. Although some 20 dB below total integrated noise, [16], [33] suggest they could be discerned by human hearing and thus should be avoided.

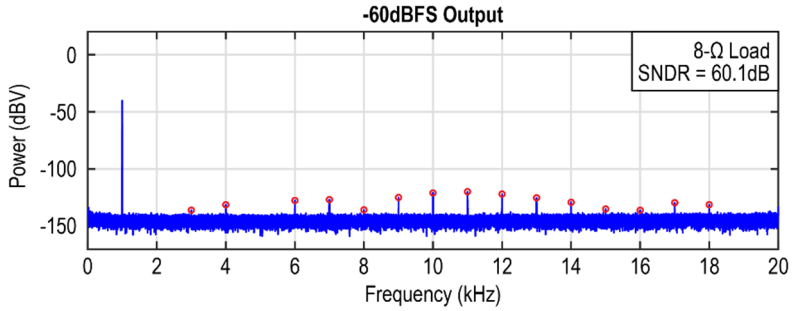

Fig. 5.17. Output spectra when NS segmentation is performed by a 1st-order DSM.

The measured THD+N across output power is plotted in Fig. 5.18, reaching a minimum of −111.2 dB for the 8-Ω load and −106.6 dB for the 4-Ω load. The rise in distortion levels toward high output power is dominated by HD2 (already visible in Fig. 5.16). It is likely due to the magnetic coupling between the CDA output current and the DAC reference traces on the test PCB. According to simulations, −110 dB of coupling can lead to a similar result. Fig. 5.19 plots the THD+N across the audio band for a −10dBFS input.

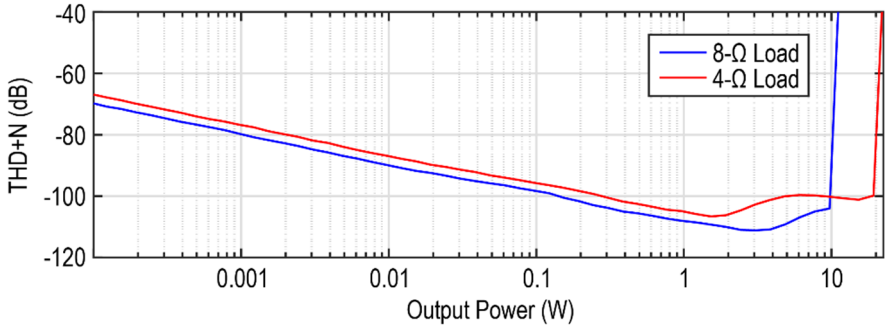

Fig. 5.18. Measured THD+N vs. output power.

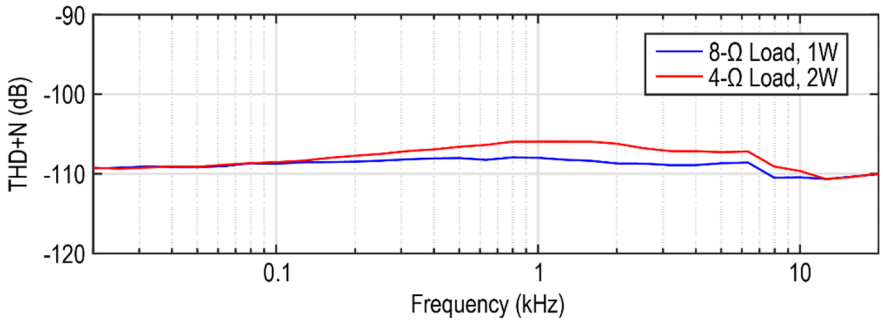

Fig. 5.19. Measured THD+N vs. input frequency.

Fig. 5.20 shows the measured power efficiency across output power up to the point of 10% THD. The peak efficiency is 90% for an 8-Ω and 86% for a 4-Ω load. The degradation compared to that in Chapter 4 is due to the increased output current and switching activities from shaped quantization noise. Fig. 5.21 shows the measured PSRR across the audio band for 3 samples.

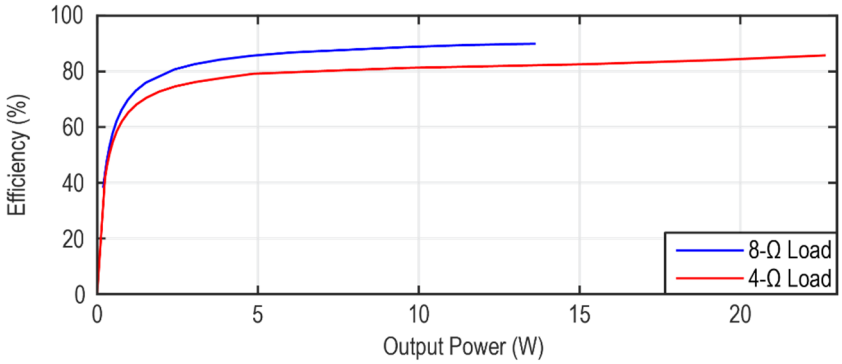

Fig. 5.20. Power efficiency across output power.

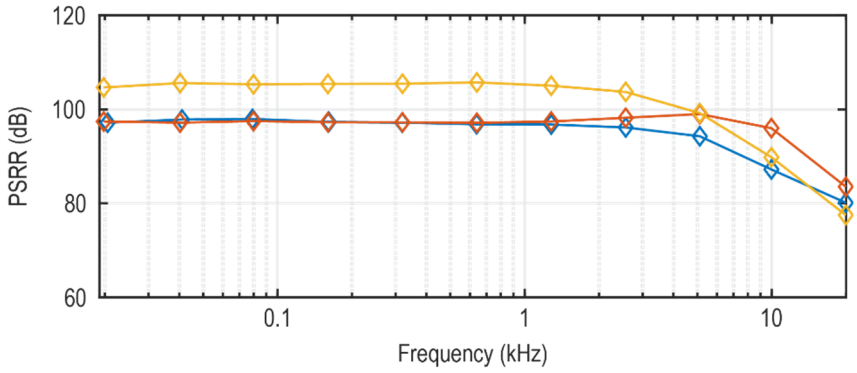

Fig. 5.21. Measured PSRR across the audio band for 3 samples.

Table 5.1 summarizes the performance of this work and compares it with state-of-the-art HV digital-input CDAs [7], [8], [32], [34], [35], [36]. It achieves the highest DR and best THD+N, thanks to the capacitively coupled architecture and proposed mismatch and ISI mitigation techniques. Meanwhile, it features competitive power efficiency, idle power, and PSRR.

Table 5.1. Performance Summary and Comparison with State-of-the-Art Digital-Input HV CDAs.

	This Work	E. Cope ISSCC 2018	D. Schinkel JSSC 2017	J.-M. Liu JSSC 2014	T. Ido ISSCC 2006	ADI SSM3582A	Cirrus Logic CS35L45
Area (mm^2)	**7.5**	4.3	-	-	23[1]	-	6.5
Architecture	**Closed-Loop**	Closed-Loop	Closed-Loop	Open-Loop	Closed-Loop	Closed-Loop	Closed-Loop
DAC Type	**CDAC**	RDAC	IDAC	-	IDAC	-	-
Supply (V)	**14.4**	8~20	25	18	35	4.5~16.5	2.5~15
$I_{Q,PVDD}$ (mA)	**13.9**	20.5	-	9.4	-	12.3	-
R_{LOAD} (Ω)	**8/4**	8/4	4	8	4/6/8	8/4	8
$P_{OUT,MAX}$ (W)	**13/23**	20	80	13	130/99/74[1]	18/32	6.8
Efficiency	**90%/86%**	90%	>90%	88%	81%[1]	94%/91%	88%
Peak THD+N @ 1kHz	**-111.2/-106.6**	-97.2[2]/-93.1[2]	-88.6	-62.5	-94.9	-94[2]	-79
DR (dB)	**120.9**	115.5	115	84	113	109	-
A-wt. Output Noise (μV_{RMS})	**9.3**	20	34	-	-	36	5
PSRR (dB) (Freq./Hz)	**97~78 (20~20k)**	80~50 (20~20k)	88~60 (100~20k)	-	-	88 (1k)	-
Suppress LC Filter Distortion	**Yes**	No	Yes	No	No	No	No

[1] Output stage is off-chip

[2] Extracted from figure

5.6 Conclusion

This chapter presents a digital-input capacitively coupled CDA. Distortion sources due to DAC mismatch and ISI are mitigated using NS segmentation, RTDEM, and deadband. The DAC's intermodulation with chopping and PWM are analyzed so that f_S, f_{CH}, and f_{PWM} are chosen carefully to avoid noise and linearity degradation. Measurement results of the 180 nm prototype show a DR of 120.9 dB and peak THD+N of −111.2 dB, which advances the state-of-the-art in HV digital-input CDAs by 5.4 dB and 14 dB, respectively.

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Chapter 6 Conclusions and Outlook

In this thesis, the design of high-performance multilevel Class-D amplifiers (CDAs) has been explored. This chapter summarizes the main contributions of the CDA designs described in this thesis and benchmarks them against the state-of-the-art. Several directions for future research are also discussed.

6.1 Main Contributions

6.1.1 4.2 MHz Fully-Differential Multilevel PWM Output Stage (Chapter 2)

Conventional CDAs often generate electromagnetic interference (EMI) in the AM band. To satisfy the stringent automotive EMI standard, their output must then be attenuated by a bulky and costly LC filter. To address this challenge, a 4.2 MHz multilevel output stage has been designed, whose extra output level was generated by a low-power on-chip regulator. The choice of a relatively high switching frequency placed the PWM tone above the EMI-sensitive AM band. This was used in a CDA with low idle power that satisfies the CISPR 25 Class 5 EMI standard and enables a 5x increase in the LC filter's cutoff frequency compared to the state-of-the-art.

6.1.2 Dual-Loop Feedback-after-LC Architecture (Chapter 3)

The linearity of conventional closed-loop CDAs is limited by that of the LC filter, since the latter is typically placed outside the feedback loop. This can be addressed by a feedback-after-LC architecture. However, due to LC spread and low PWM frequencies, prior implementations only achieved limited loop gain [1], unless the loop filter coefficients were specifically tailored to match a given LC filter [2]. Taking advantage of the 4.2 MHz

multilevel output stage, a feedback-after-LC CDA was realized that suppressed LC filter nonlinearity by 49 dB and was robust to ±30% variations in the LC components' values. Stability was maintained by an inner loop, which acted as a lead compensator while adding extra loop gain around the output stage. This enables the use of small and low-cost LC filter components in CDAs while still achieving a total harmonic distortion (THD) well below −100 dB.

6.1.3 High-DR Closed-Loop CDA Using Capacitive Feedback (Chapter 4)

The dynamic range (DR) of conventional closed-loop CDAs is limited by the noise in their resistive feedback network. Capacitive feedback has been widely used in instrumentation amplifiers due to its lower noise. However, it cannot be applied to conventional CDAs since the rail-to-rail transitions of the output stage would saturate the loop filter's input stage. The feedback-after-LC architecture attenuates the high-frequency components in the error signal, thus enabling the first capacitively-coupled CDA. Chopping enables the processing of low-frequency audio signals and suppresses the loop filter's $1/f$ noise, and nonlinear chopping glitches were suppressed by using a deadband. It achieved the best-reported DR of 121.4 dB and a peak THD+N of −109.8 dB among integrated CDAs.

6.1.4 Digital-Input Capacitively Coupled CDA (Chapter 5)

Due to its switched-capacitor input interface, the capacitively coupled chopper CDA requires a pre-driver capable of driving a switched-capacitor load with high linearity. In digital audio applications, this would be preceded by another antialiasing filter to avoid the folding of out-of-band quantization noise from the digital-to-analog converter (DAC). The system can be simplified by integrating a capacitive DAC (CDAC) into the CDA. In this

way, the first digital-input capacitively-coupled CDA has been realized, where quantization noise folding was avoided by appropriately choosing its sampling frequency based on the chopping and PWM frequencies. In the CDAC, 2nd-order noise-shaped segmentation and real-time dynamic element matching (RTDEM) were employed to suppress mismatch errors, and the deadband was reused to suppress distortion due to intersymbol interference (ISI). The prototype achieved a DR of 120.9 dB and a peak THD+N of −111.2 dB.

6.2 Main Findings

- The EMI of a CDA can be effectively suppressed by using a multilevel output stage. In addition, with a PWM frequency of 4.2 MHz, the CISPR 25 Class 5 EMI standard can be satisfied with a small LC filter, with a cutoff frequency of 580 kHz (Chapter 2).
- For feedback-after-LC CDAs, a high PWM frequency makes it possible to simultaneously achieve high loop gain and robustness to variations in the LC filter (Chapter 3).
- The DR of a feedback-after-LC CDA can be improved by using capacitive feedback. This can be realized by adding a capacitively-coupled chopper amplifier (CCCA) before the 1st integrator (Chapter 4).
- The use of a deadband in a capacitively-coupled chopper CDA suppresses nonlinearity due to the chopping glitches, but folds high-frequency noise introduced by later stages of the loop filter and the output stage. The folded noise is proportional to the deadband's duty cycle, which, therefore, should be minimized (Chapter 4).
- A capacitive feedback CDA can be driven by a digital input through a CDAC. The deadband can be reused to suppress distortion due to the CDAC's ISI (Chapter 5).

6.3 Comparison with the State-of-the-Art

Fig. 6.1 shows the switching frequency and idle power of all integrated CDAs published in top journals (JSSC and TPE) and conferences (ISSCC, VLSI, ESSCIRC, CICC, ISCAS, AES) [3] since the first report of an integrated CDA in 2003 [4], [5]. A higher switching frequency helps reduce the size of the LC filter required for EMI reduction. Since the idle power is generally higher for a CDA with higher peak output power, their ratio is shown in the plot. The proposed multilevel output stage employs the highest switching frequency. The multilevel operation also enabled the lowest idle power among high-voltage (HV, >5 V)[1] CDAs switching at MHz frequencies, when normalized to the maximum output power.

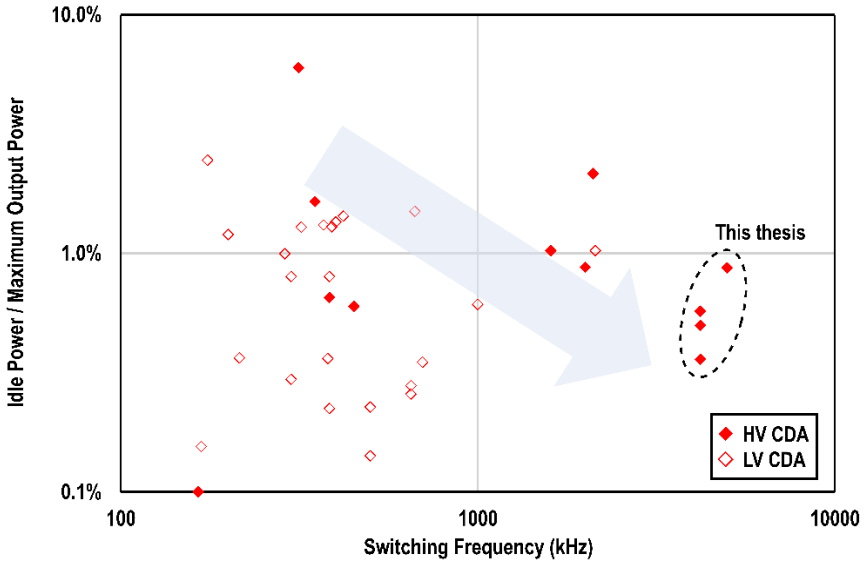

Fig. 6.1. Switching frequency and normalized idle power of all integrated CDAs published in top journals and conferences.

[1] CDAs with output swings less than 5 V typically do not require a floating voltage domain for their high-side gate driver, which consumes extra power.

The DR and THD+N of the surveyed CDAs are compared in Fig. 6.2. As shown, the CDAs presented in this thesis achieved state-of-the-art THD+N. Furthermore, the capacitively coupled CDA architectures described in Chapter 4 and Chapter 5 achieved the best reported DR among HV CDAs.

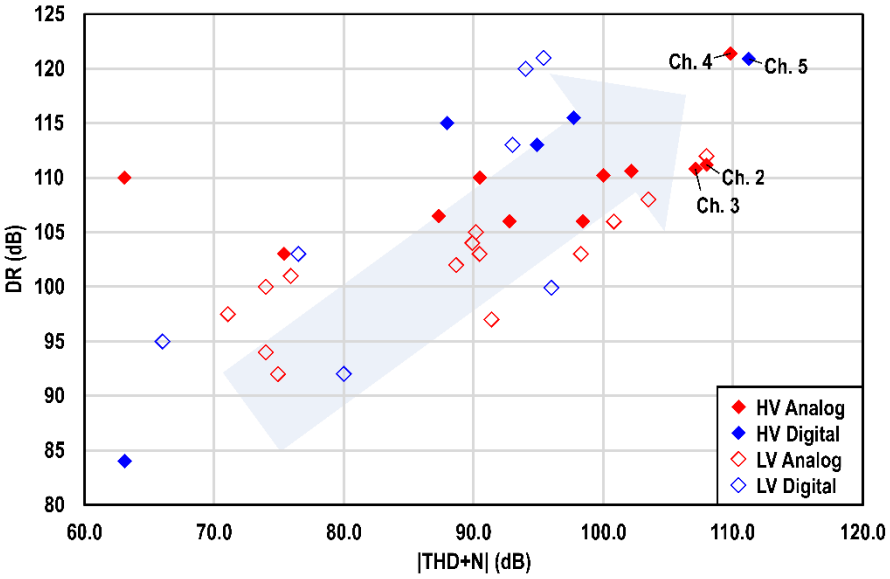

Fig. 6.2. DR and THD+N of integrated CDAs published in top journals and conferences.

6.4 Future Research Directions

6.4.1 Other Feedback-after-LC Architectures

In the feedback-after-LC architecture discussed in Chapter 3, an inner loop is used to realize a lead compensator, which reduces the loop gain around the LC filter at low frequencies. Even though 49 dB of LC filter nonlinearity suppression is realized, this factor would become much less if a lower PWM frequency was used without increasing the loop filter order. To achieve a better tradeoff between loop gain and f_{PWM}, other architectural options can be explored.

For example, DC-DC buck converters are often stabilized by using current feedback, which turns the inductor into a voltage-controlled current source, thereby splitting the complex conjugate poles introduced by the LC filter (Fig. 6.3). This also enables inherent current limiting and, in the case of multiphase converters, inherent current balancing, both desirable features for CDAs. Current feedback has been used in a Class-D piezoelectric speaker driver [6] to damp the LC resonance in a feedback-before-LC architecture. However, it employs a push-pull output stage, which requires only low-side current sensing. Implementing hardware-efficient and sufficiently linear current sensing in a constant-CM output stage would enable the more general application of current sensing to CDAs.

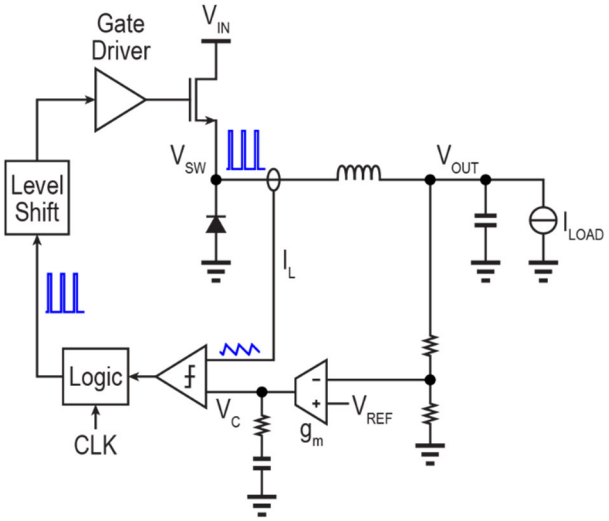

Fig. 6.3. Simplified circuit diagram of a buck converter with current mode control.

6.4.2 Capacitively Coupled CDA with Open-Loop Front-End

As mentioned in Section 4.2, due to the feedback-after-LC architecture, the error signal that drives the CDA loop filter is quite small. This makes it possible to implement the loop filter's front end with an open-loop transconductor (e.g., a differential pair) [7], as shown in Fig. 6.4. Compared

to the capacitively-coupled chopper amplifier (CCCA) front-end used in the designs described in Chapter 4 and Chapter 5, this completely eliminates the noise contribution of the following R_{INT1} (Fig. 5.12) and is particularly helpful in a digital-input design since voltage swing due to the DAC image is immediately suppressed by the integration operation. It also could allow for a much shorter DB, hence less noise folding and better DR. However, the DAC resolution and sampling rate might have to be increased to sufficiently reduce the transconductor's input swing. To avoid a master clock with a very high frequency, a new DEM scheme might also be required, which is challenging when targeting a DR near 130 dB, the state-of-the-art in Class-AB audio driver [8].

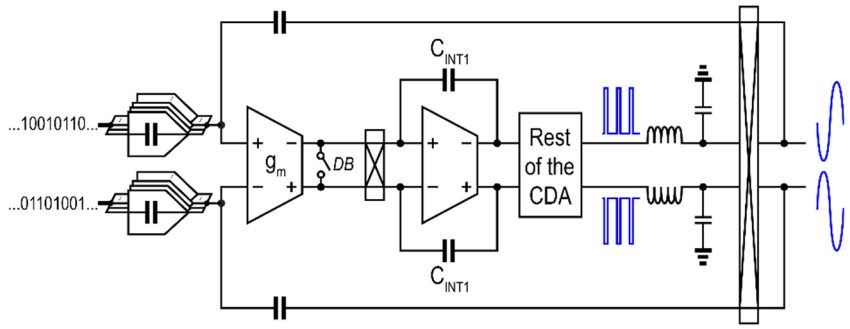

Fig. 6.4. Capacitive feedback CDA with an open-loop transconductor as the input stage.

6.4.3 Ultra-Low-Power CDA for TWS Headphones

True wireless stereo (TWS) headphones have become very popular recently. Each earbud requires a power amplifier, but their small form factor, hence battery capacity, demands ultra-low power consumption. Traditionally, Class-AB amplifiers have been used due to the low (< 100mW) output power requirement. However, Class-D has also been attempted to achieve higher efficiency [9], which could benefit battery life. However, pushing CDA idle power below 1 mW without sacrificing noise and linearity performance

remains challenging. Furthermore, EMI should be carefully managed since the CDA must be placed very close to a wireless transceiver.

6.4.4 GaN-Based CDA

Compared to LDMOS transistors, high-electron-mobility transistors (HEMT) based on Gallium Nitride (GaN) offer much lower gate capacitance for a given on-resistance. Therefore, CDAs employing a GaN-based output stage can potentially achieve higher switching frequencies and lower idle power, enabling the use of smaller LC filters. However, GaN HEMTs exhibit a large voltage drop under reverse conduction, increasing their power loss and causing distortion due to the associated dead time. The absence of p-type transistors in GaN processes also poses significant challenges in circuit design. A possible way forward is a silicon-in-package (SiP) solution combining CMOS mixed-signal circuitry and a GaN-based output stage.

6.4.5 Advanced Packaging Solutions

The multilevel output stage proposed in Chapter 2 requires an internally generated mid-rail supply PVCM. To minimize ringing due to parasitic inductances, it should be decoupled off-chip to both PVDD and PVSS, for each differential half of the output stage, and the area of the current loop formed by these decoupling capacitors and the supply connections should be minimized. Therefore, during measurements, the test chips were directly bonded to the PCB. To reduce ringing and its layout dependence in practical applications, the decoupling capacitors can be integrated inside the package, and flip-chip bonding can be used to further reduce the parasitic inductance. Moreover, since a small LC filter can be used thanks to its feedback-after-LC architecture, it can also be integrated into the package. Nevertheless, a thorough analysis of the EMI and thermal performance should be performed.

6.5 Concluding Remarks

In this thesis, the development of high-performance HV CDAs based on a multilevel output stage has been presented. Their EMI has been significantly reduced, and their THD+N has been improved by >14 dB. In addition, their DR has been extended by >5 dB and is no longer limited by the feedback network of the CDA. However, turning these research prototypes into commercial products will still require additional work to enhance their robustness to external disturbances such as ESD and fault conditions.

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Summary

This thesis describes the analysis, design, prototype implementation, and measurement results of high-performance Class-D amplifiers (CDAs) for audio applications.

Chapter 1 introduces the background of CDAs, key performance metrics, and design challenges. CDAs are characterized by an output stage that switches the output voltage directly to supply rails. No power would be lost in such an output stage if the switches were ideal. However, practical transistors exhibit on-resistance and parasitic capacitances, introducing power losses. Besides, the high dv/dt and di/dt of fast switching causes electromagnetic interference (EMI), which must be kept within certain limits set by various regulations. LC filters are often used to reduce EMI at the expense of extra distortion, cost, and system bulk. Nonideal switching behavior (e.g., non-overlapping to avoid shoot-through currents) also distorts the audio signal, which is often suppressed by a feedback loop around the output stage. However, conventional closed-loop CDAs employ a resistive feedback network, whose noise limits the CDA's dynamic range (DR).

Chapter 1 also reviews existing techniques to mitigate the EMI and improve the noise and linearity of CDAs. EMI can be reduced by a multiphase or multilevel output stage. However, this often requires additional off-chip components or complex timing and output common-mode regulation circuitry. With a low-jitter clock and a low-noise power supply, open-loop CDAs can achieve high DR due to their simple structure and absence of a noisy feedback network. However, their linearity is limited at high power levels. On the other hand, closed-loop CDAs can suppress noise and distortion introduced by the output stage, while the DR is limited by the noise of their input resistors or DAC. The distortion introduced by the LC filter can be suppressed using a

feedback-after-LC architecture, but prior art only achieves a limited amount of suppression or requires digital calibration due to their low switching frequency and, thus, loop bandwidth. Due to these limitations, when this study started, state-of-the-art HV CDAs only achieved a DR of about 115 dB and a THD+N of about −97 dB.

To address the EMI challenge, **Chapter 2** proposes a multilevel CDA with constant output common mode (CM) operating at a PWM frequency of 4.2MHz. Multilevel operation reduces the output step size, hence EMI magnitude, by half compared to the conventional AD modulation scheme, while the high PWM frequency avoids interfering with the AM band. Therefore, the EMI standard can be fulfilled with a relaxed LC filter. Furthermore, the proposed multilevel PWM scheme features reduced switching activity during idle operation, leading to reduced idle power consumption. The high PWM frequency also enables a high bandwidth for the feedback loop, hence a high loop gain to suppress the output stage nonlinearity.

The CDA described in Chapter 2 also can achieve good linearity, which, however, is sensitive to the linearity of external LC filter components. **Chapter 3** proposed a dual-loop architecture to solve this problem. The 4.2 MHz output stage also offers the opportunity to realize feedback after the LC filter with both a high suppression of LC filter nonlinearity and a high tolerance to variations in the LC cutoff frequency. An inner loop is designed to serve as a lead compensator to stabilize the system under ±30% variations in the LC values while also providing extra loop gain to suppress distortion introduced by the CDA's output stage. A resonator is added to the outer loop to further boost the loop gain around the LC filter.

With the feedback-after-LC architecture of Chapter 3, the THD+N of the CDA becomes noise-limited, and the input resistors of the 1st integrator are

the dominant source of noise. This limitation is addressed in **Chapter 4**. The capacitively-coupled chopper amplifier has become a popular amplifier topology for instrumentation and biomedical signal processing due to its noiseless input and feedback network, but it cannot be directly applied to CDAs because of the former's high-pass feedback network and the latter's rail-to-rail switching output. In the feedback-after-LC architecture of Chapter 3, switching edges of the CDA feedback signal are significantly attenuated by the LC filter, thus making it possible to realize the first CDA based on the capacitively coupled chopper amplifier topology. The prototype achieves a DR of 121.4 dB and a THD+N of −109.8 dB.

The CDAs presented from Chapter 2 to Chapter 4 operate with an analog input signal. Since most audio sources are digital, they require an external DAC. Furthermore, for the capacitively coupled CDA of Chapter 4, the use of chopping demodulates out-of-band noise from multiples of the chopping frequency. Therefore, in practice, it also needs to be preceded by an additional anti-aliasing filter. These problems are addressed in **Chapter 5**, where the input capacitor of the capacitively coupled CDA is turned into a capacitive DAC, which is co-designed with the CDA. The intermodulation effect between the DAC, chopping, and PWM is analyzed carefully to prevent extra noise and distortion. DAC mismatch and intersymbol interference (ISI) are addressed with the help of advanced dynamic element matching and timing techniques.

Chapter 6 summarizes the original contributions of this study and concludes this thesis. Future research directions are also suggested, including 1) other feedback-after-LC architectures, 2) capacitively coupled CDA with an open-loop g_m-C input stage, 3) ultra-low-power CDA for true wireless stereo (TWS) earbuds, and 4) GaN-based CDA, and 5) advanced packaging solutions.

Samenvatting

Deze thesis omvat de ontwerp, analyse, prototype-implementatie, en meetresultaten van klasse D versterkers (CDAs) voor audio-toepassingen.

Hoofdstuk 1 introduceert de achtergrond van CDAs, de belangrijkste prestatiegegevens, en ontwerpuitdagingen. CDAs worden gekenmerkt door een uitgangstrap die de uitgansspanning direct aan de voedingsrails verbindt. In het ideale geval gaat zo geen vermogen verloren. Praktische transistoren vertonen echter aan-weerstand en parasitaire capaciteiten die zorgen voor vermogensverlies. Daarnaast zorgen de hoge *dv/dt* en *di/dt* van het snelle schakelgedrag voor Elektromagnetische Interferentie (EMI), die binnen wettelijke kaders moet blijven. LC filters worden vaak gebruikt om EMI te beperken ten koste van extra vervorming, kosten, en systeemgrootte. Niet-ideaal schakelgedrag (zoals overlapvermeiding om doorloopstromen te voorkomen) vervormt ook het audiosignaal, wat vaak wordt onderdrukt door een regelkring rond de uitgangstrap. Conventionele CDAs met gesloten regelkring gebruiken een weerstandsnetwerk, waarvan de ruis het Dynamisch Bereik (DR) van de CDA beperkt.

Hoofdstuk 1 geeft ook een overzicht van bestaande technieken om EMI te verminderen en de ruis en lineariteit van de CDAs te verbeteren. EMI kan worden verminderd door het gebruik van meerdere fasen of schakelniveaus in de uitgangstrap. Dit vereist echter vaak extra componenten buiten de chip of complexe circuits om schakeltijden en het gemeenschappelijke uitgangssignaal te regelen. Door middel van een klok met weinig jitter en een voeding met weinig ruis kan een open-lus CDA een hoog DR halen dankzij de simpele structuur en de afwezigheid van een ruizig terugkoppelnetwerk. De lineariteit is bij hoge vermogens echter beperkt. CDAs met gesloten regelkring onderdrukken daarentegen de ruis en vervorming van de

uitgangstrap, maar hebben een beperkt DR door de ruis van hun ingangsweerstanden of DAC. De vervorming die wordt veroorzaakt door het LC filter kan worden onderdrukt door een terugkoppeling-na-LC architectuur, maar eerder werk haalt slechts een beperkte hoeveelheid ondrukking of vereist digitale kalibratie vanwege een lage schakelfrequentie, en dus regelbandbreedte. Door deze beperkingen werd de stand van de techniek vorafgaand aan dit onderzoek gevormd door hoogspannings CDAs met een DB van ongeveer 115dB en THD+N van ongeveer −97dB.

Om de EMI-uitdaging aan te pakken stelt hoofdstuk 2 een CDA voor met meerdere uitgangsniveaus, een constant gemeenschappelijk signaal (GS), en een Pulsbreedteemodulatie (PWM) frequentie van 4.2MHz. Door te werken met meerdere uitgangsniveaus vermindert de uitgangsstapgrootte, en dus de grootte van de EMI, met een factor 2 ten opzichte van een conventionele AD modulatie structuur, terwijl de hoge PWM frequentie storing van de AM band omzijlt. Daarom kan aan de EMI standaard worden voldaan met een minder hevig LC filter. Verder heeft de voorgestelde meerniveaus PWM structuur een verminderde schakelactiviteit tijdens onbelaste werking, wat leidt tot een vermindert onbelast energieverbruik. De hoge PWM frequentie maakt ook een hoge bandbreedte mogelijk voor de regelkring, en dus een hoge luswinst om de niet-lineariteit van de uitgangstrap te onderdrukken.

De CDA in hoofdstuk 2 kan ook een hoge lineariteit behalen, die echter gevoelig is voor de lineariteit van componenten van het externe LC filter. Hoofdstuk 3 stelt een twee-lussige architectuur voor om dit probleem op te lossen. De 4.2 MHz uitgangstrap geeft ook de mogelijkheid om terugkoppeling na het LC filter te realiseren met een hoge onderdrukking van de niet-lineariteit van het LC filter en een hoge tolerantie voor variaties in de afsnijfrequentie. Een binnenste lus is ontworpen om te dienen als een lead compensator om het systeem te stabiliseren onder ±30% variaties van de LC-

waardes terwijl het ook extra luswinst biedt om vervorming van de uitgangstrap van de CDA te onderdrukken. Een resonator werd toegevoegd aan de buitenste lus om de luswinst rondom het LC filter verder te verhogen.

Met de terugkoppeling-na-LC architectuur van hoofdstuk 3 wordt de THD+N van de CDA ruisgelimiteerd, waarbij de ingangsweerstanden van de eerste integrator de dominante ruisbron vormen. Deze beperking wordt aangepakt in hoofdstuk 4. Een capacitatief gekoppelde hakker versterker is een populaire versterkertopologie geworden voor instrumentatie en biomedische signaalbewerking dankzij het ruisloze ingangs- en terugkoppelingsnetwerk, maar het kan niet direct worden toegepast in CDAs vanwege de hoogdoorlaatkarakteristiek van het terugkoppelnetwerk en het uitgangssignaal dat van voedingsrail naar voedingsrail gaat. In de terugkoppeling-na-LC architectuur van hoofdstuk 3 worden de schakelflanken van het CDA terukoppelsignaal significant afgezwakt door het LC filter, wat het mogelijk maakt om de eerste CDA te realiseren die is gebaseerd op de capacitatief gekoppelde hakker versterker topologie. Dit prototype haalt een DR van 121.4dB en een THD+N van −109.8dB.

De CDAs die worden getoond van hoofdstuk 2 tot hoofdstuk 4 werken met een analoog ingangssignaal. Omdat de meeste audiobronnen digitaal zijn, vereisen ze een externe DAC. Verder zorgt bij de capacitatief gekoppelde CDA van hoofdstuk 4 de hakwerking voor demodulatie van ruis buiten de band op veelvouden van de hakfrequentie. Daarom moet de versterker in praktijk worden voorgegaan door een aanvullend anti-vouvervormingsfillter. Deze problemen worden aangepakt in hoofdstuk 5, waar de ingangscondensator van de capacitatief gekoppelde CDA wordt verandert in een capacitatieve DAC, die samen met de CDA wordt ontworpen. De intermodulatie tussen de DAC, het hakken, en de PWM wordt in detail geanalyseerd om extra ruis en vervorming te voorkomen. Discrepantiefouten

van de DAC en Intersymboolinterferentie (ISI) worden aangepakt met geavanceerde dynamische foutcorrectie- en tijdcontroletechnieken.

Hoofdstuk 6 vat de orginele bijdragen van dit onderzoek samen en sluit dit proefschrift af. Verdere onderzoeksrichtingen worden ook voorgesteld, waaronder 1) andere terugkoppeling-na-LC architecturen, 2) capacitief gekoppelde CDA met een open-lus gm-C ingangstrap, 3) ultra-laag-vermogen CDA for echte draadloze stereo (EDS) oortjes, 4) GaN-gebaseerde CDA, en 5) geavanceerde verpakkingsoplossingen.

List of Publications

Journal Articles

1. S. Karmakar, **H. Zhang**, *et al*., "A 28-W, −102.2-dB THD+N Class-D Amplifier Using a Hybrid ΔΣM-PWM Scheme," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3146-3156, Dec. 2020.
2. **H. Zhang** *et al*., "A High-Linearity and Low-EMI Multilevel Class-D Amplifier," *IEEE J. Solid-State Circuits,* vol. 56, no. 4, pp. 1176-1185, Apr. 2021.
3. **H. Zhang**, M. Berkhout, K. A. A. Makinwa, and Q. Fan, "A -121.5-dB THD Class-D Audio Amplifier With 49-dB LC Filter Nonlinearity Suppression," *IEEE J. Solid-State Circuits,* vol. 57, no. 4, pp. 1153-1161, Apr. 2022.
4. **H. Zhang**, N. N. M. Rozsa, M. Berkhout, and Q. Fan, "A Chopper Class-D Amplifier for PSRR Improvement Over the Entire Audio Band," *IEEE J. Solid-State Circuits,* vol. 57, no. 7, pp. 2035-2044, July 2022.
5. **H. Zhang**, M. Berkhout, K. A. A. Makinwa, and Q. Fan, "A 121.4-dB DR Capacitively Coupled Chopper Class-D Audio Amplifier," *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3736-3745, Dec. 2022.
6. **H. Zhang**, M. Berkhout, K. A. A. Makinwa and Q. Fan, "A 120.9-dB DR Digital-Input Capacitively Coupled Chopper Class-D Audio Amplifier," in *IEEE J. Solid-State Circuits*, vol. 58, no. 12, pp. 3470-3480, Dec. 2023.

Conference Proceedings

1. S. Karmakar, **H. Zhang**, *et al.*, "A 28W -108.9dB/-102.2dB THD/THD+N Hybrid ΔΣ-PWM Class-D Audio Amplifier with 91%

Peak Efficiency and Reduced EMI Emission," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 350-352.

2. **H. Zhang** *et al.*, "A −107.8 dB THD+N Low-EMI Multi-Level Class-D Audio Amplifier," in *Proc. Symp. VLSI Circuits*, June 2020, pp. 1-2.
3. **H. Zhang**, M. Berkhout, K. Makinwa, and Q. Fan, "A -121.5 dB THD Class-D Audio Amplifier with 49 dB Suppression of LC Filter Nonlinearity and Robust to +/-30% LC Filter Spread," in *Proc. Symp. VLSI Circuits*, June 2021, pp. 1-2.
4. **H. Zhang**, N. Rozsa, M. Berkhout, and Q. Fan, "A -109.1 dB/-98 dB THD/THD+N Chopper Class-D Amplifier with >83.7 dB PSRR Over the Entire Audio Band," in *Proc. ESSCIRC*, Sept. 2021, pp. 395-398.
5. **H. Zhang**, M. Berkhout, K. A. A. Makinwa, and Q. Fan, "A 121.4dB DR, -109.8dB THD+N Capacitively-Coupled Chopper Class-D Audio Amplifier," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2022, pp. 484-485.
6. **H. Zhang**, M. Berkhout, K. A. A. Makinwa, and Q. Fan, "A 120.9dB DR, -111.2dB THD+N Digital-Input Capacitively-Coupled Chopper Class-D Audio Amplifier," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2023, pp. 54-55.
7. M. Chen, **H. Zhang**, and Q. Fan, "A 155W −95.6 dB THD+N GaN-based Class-D Audio Amplifier With LC Filter Nonlinearity Compensation," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2023, pp. 1207-1210.
8. S. Karmakar, **H. Zhang**, M. Berkhout, and Q. Fan, "A Class-D Piezoelectric Speaker Driver Using A Quadrature Feedback Chopping Scheme achieving 29dB Large-Signal THD+N Improvement," in *Proc. Symp. VLSI Circuits*, June 2023, pp. 1-2.

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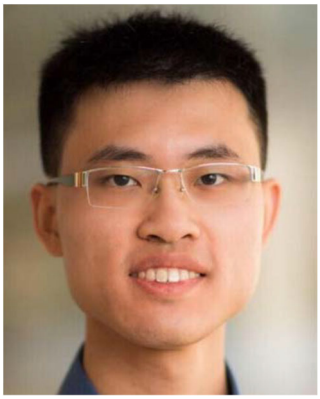
About the Author



Huajun Zhang was born in Beijing, China. He received the B.E. degree in electrical and computer engineering from Shanghai Jiao Tong University, Shanghai, China, in 2015, and the B.S.E. and M.S. degrees in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2015 and 2017, respectively.

In the summer of 2016, he was an Analog/Mixed-Signal Design Intern with Analog Devices, Inc., Wilmington, MA, USA. From May 2017 to February 2019, he was a Mixed Signal Design Engineer with Analog Devices, Inc., Norwood, MA, USA. He joined the Electronic Instrumentation Laboratory, Delft University of Technology, Delft, The Netherlands, in March 2019 to pursue the Ph.D. degree. He holds one U.S. patent. His technical interests include precision analog circuits, Class-D audio amplifiers, and data converters.

Mr. Zhang received the IEEE Solid-State Circuits Society Predoctoral Achievement Award in 2023, the Analog Devices Outstanding Student Designer Award in 2022, and the ESSCIRC Best Student Paper Award in 2021. He has served as a Reviewer for the IEEE OPEN JOURNAL OF THE SOLID-STATE CIRCUITS SOCIETY, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS, ELECTRONICS LETTERS, and the IEEE SENSORS JOURNAL.