Development of an LED Driver for Automotive Lighting Applications

by

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Abstract

Power switches and more specifically MOSFETs are used very often in applications such as industrial (automation, robotics, drives...) and automotive (lighting, heating, motor control...). The main function of these devices is to switch the energy delivered to the load so that power could be transferred in the most optimum way meeting a certain set of requirements.

Due to recent and continuous developments in system-on-chip technologies these power switches can be implemented along with further and further features that turn them into smart devices. These features mainly focus on intelligent diagnosing, measuring and protecting functions that provide the final implementation with improved functionality. This is the case of Infineon's smart technology. With this approach, it will be possible to combine power devices together with highly integrated circuits. In addition, the fitness of this technology for mass-production will culminate in low manufacturing costs.

This thesis focuses on proving the feasibility of using Infineon's smart technology for an LED driver application. Such analysis will be carried out to ultimately build a prototype of the concept together with the implementation of a suitable control scheme. The switch family is currently used in several applications and available for lab testing. However, the suitability of this product line for DC/DC lighting applications has not been evaluated yet.

Starting from an available test-chip which integrates the power device, the feasibility of the solution will be firstly analyzed making use of a simulation approach. The converter will use an asynchronous buck topology. The driver concept and the DC/DC stage will be put together with the MOSFET's detailed model to determine whether the switch family could be used in the conditions given by the application of interest.

The power losses of the system will be computed from simulation results to determine whether the device could handle the required amount of power. Besides this, efficiency calculations of the DC/DC converter will be carried out to obtain gain insight into how energy-saving the system could potentially be.

Once the problem has been tackled from a simulation point of view, a simplified loss model will be derived in order to evaluate the efficiency of the whole system. Coil, capacitor, diode and switch among others will account for the total losses of the solution. Such loss model will be compared to the results obtained during the simulation phase in order to evaluate its accuracy.

The next step towards the physical implementation of the solution will consist in finding a suitable floating gate driver which could deliver the required amount of current to the switch. Two systems will be analyzed and compared in order to determine which would suit the application best. Measurements will be also presented to prove that the theoretical analysis of the solution matches with lab results.

A step further will be taken in order to optimize the prototype setup. The DC/DC converter will be implemented on a PCB to minimize undesired parasitics and improve the results observed at previous measurements. The concept adopted for this system will be presented in detail and the obtained results will be shown and analyzed to demonstrate the validity of the approach.

Besides, a literature study on concepts and strategies to control the system will be introduced and carried out. A comparison between different alternatives will be made in order to choose which would suit the application best. The selection criteria will include aspects such as transient performance and complexity. Once the most suitable control topology has been selected, a practical design for the application of interest will be proposed. Additionally, simulation results will be discussed to evaluate the performance of the final control system.

Lastly, the most suitable control scheme will be implemented on a real system at the lab using a rapid control prototyping tool from dSPACE. The steps of this process will be described and the obtained results will be shown and analyzed in order to draw final conclusions and present future work.

Contents

Acknowledgments

I would like to thank Infineon for giving me the opportunity to be an active part of the company. After completing my internship and master's thesis at the main site in Austria I have gained a lot of insight on how a professional environment works and how the skills learned throughout the years can be put into practice. What is more, I am very glad that our professional relationship will continue in the future after finishing my studies. I am extremely excited and motivated about the challenges and opportunities to come.

I would also like to extend my appreciation to the Delft University of Technology. I decided to embark on an experience abroad to broaden my horizons and I must say that the journey has exceeded my expectations by far. The context and opportunities given by the university have clearly had an impact on my enthusiasm towards learning and improving myself.

I cannot forget to mention all the friends I have met during my stay abroad in both Austria and the Netherlands. Thank you all for listening, offering me advice, and supporting me through this entire process. Thank you for sharing your life stories with me and for your friendship.

Lastly, I would like to extend my deepest gratitude to my family. You should know that your support and encouragement is worth more than I can express on paper. Without your love and understanding I could never have gotten where I am today.

To my mother, who was often in my thoughts on this journey – this dissertation stands as a testament to the unconditional love and encouragement you always showed me. I will be enormously thankful forever.

1 Introduction

The first chapter of this document is aimed to serve as an introduction to the reader for all the work described along the report. Section 1.1 presents the topic of smart power switches to acquaint the reader with the basics of these devices. Section 1.2 focuses on describing the more and more growing role of LED in automotive applications. The importance of DC/DC converter solutions in the automotive field is addressed in section 1.3. A description of Rapid Control Prototyping is presented in section 1.4 to make the reader familiar with the approach used to implement the control on the prototype. Section 1.5 introduces the system that will be analyzed in detail along the report. Section 1.6 focuses on the motivation of this thesis work while section 1.7 sets out the the research questions. Lastly, the outline of the thesis is presented in section 1.7.

1.1. Smart power switches in automotive applications

The importance of power semiconductors in the automobile industry is undoubtedly increasing further and further. Anything that is capable of moving, rotating, sliding, etc. will be deliberately activated by a power switch. This is the trend towards which automotive applications are converging. On top of this, smart switches make life easier by incorporating additional features with respect to traditional semiconductors. A smart device of this kind does not simply stick to performing the switching operation; it takes the application a step further by merging what was traditionally carried out by several different devices into one single piece of hardware. Figure 1.1 shows a comparison between what would be a typical circuit arrangement to switch inductive loads and what could be achieved by simply using a smart power switch. It can be seen how the semiconductor device can perform by itself the tasks commonly carried out by a fuse, a relay, overvoltage protection against electromagnetic interference and diagnosing or sensing elements. What is more, fewer wires and connectors would be needed and fast switching operation, such as PWM, would be possible [1].

Power domain	Application	Supplied by	Overvoltage limit
12 V automotive power net	power switching	generator	> 45/60 V
42 V automotive power net	power switching	generator	> 60/70 V
24 V truck power net	power switching	generator	> 65 V
80 V local high voltage	fuel direct injection	DC/DC converter	> 80 V
12/24/48 V industrial	power switching	power supply	> 80 V

Table 1.1: Smart power switches in automotive and industrial applications with their overvoltage withstanding limit

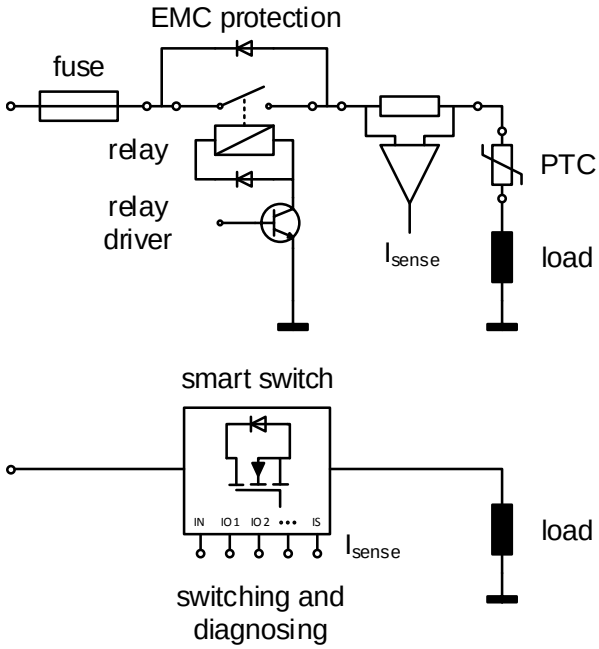

Figure 1.1: Application of a smart switch compared to a traditional discrete solution

Table 1.1 presents a general overview of the most common power domains and their applications in automotive and industrial fields [1]. Voltages of 12, 24, 42 and 48 VDC are typically present. However, due to the voltage generation and storage available in these environments, power semiconductors must be able to withstand a significantly higher voltage levels. These devices are therefore implemented with overvoltage protection features such as active Zener clamping. 12 V applications usually set their overvoltage protection to 45 V. 24 and 42 V systems as well as industrial applications have an overvoltage protection level of 60 V or more. More demanding applications such as rapid opening or closing of valves require a higher overvoltage withstanding rating of approximately 80 V.

Power semiconductors can come in a wide variety of forms. For instance, some of the available technologies at Infineon are:

- *OptiMOS*, a vertical DMOS technology typically used for high-current applications.
- *SMART5*, a CDMOS technology which includes DMOS power transistors together with CMOS logic.
- *SPT5*, a BCDMOS technology which unifies bipolar, CMOS and DMOS fabrication processes.

In the end, the state-of-the-art approach is a monolithic solution which unifies the power silicon and the control and diagnosis circuitry on a single chip. The main advantages are related to improving of reliability and system security, saving of costs (compared to using discrete components) and reducing of footprint. The concept of monolithic devices has become popular for applications which demand currents in the order of 5-10 A. However, if a larger current were required, the ratio between power and logic silicon would not justify such approach as for price and complexity. A chip-on-chip or chip-by-chip approach could be then adopted, that is, putting together semiconductors from different technologies either vertically or adjacently. As a sacrifice of reducing the silicon costs, the price of the assembling process would be increased. Taking all the factors into account, the chip-on-chip concept have enabled the realization of low-ohmic switches in a small package at a relatively low manufacturing cost compared to their monolithic counterparts [1]. Figure 1.2 shows the evolution in size, resistance and cost of high-current switches which have made use of the chip-on-chip approach.

As the name suggest, smart power semiconductors can do more than switching. As described in [1], power switches may include some additional functions such as diagnosing of optional equipment, protecting of load lines against overload and short circuits, failure diagnosing, checking of correct power

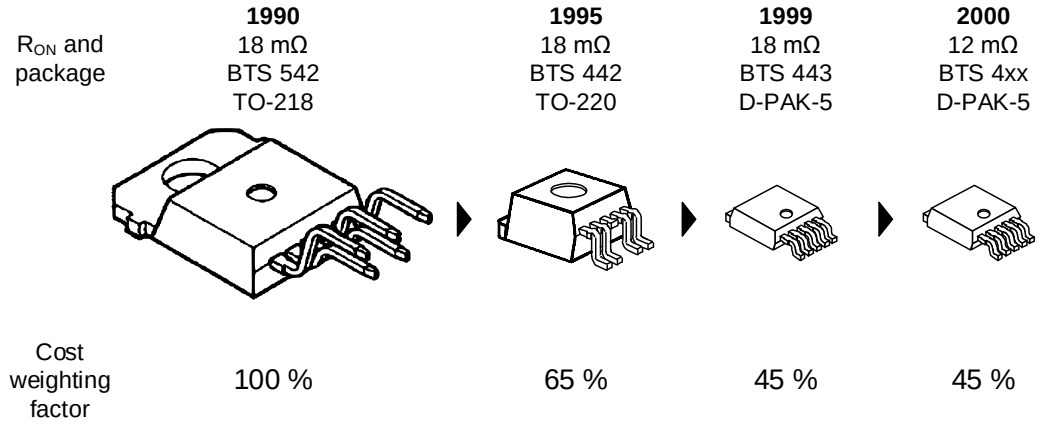

Figure 1.2: Evolution of smart switches due to chip-by-chip concept

ratings, preheating using PWM to extend service life, shaping of switching edges to reduce electromagnetic emissions, etc.

In summary, smart power switches provide very good solutions in the voltage range between 5 and 60 V. However, the overvoltage withstand capability required is high compared to their rated voltage, which results in higher costs. The new 42 V electrical system tries to overcome such limitation. The power switches designed for 42 V would be cheaper and optimally used [1]. In other words, moving the trend towards a higher voltage would lower the current that has to be switched. Consequently, the switch could be shrunk horizontally since a larger effective on-resistance could be acceptable for a specific application. This would greatly reduce semiconductor horizontal size and therefore costs.

Smart power switches will be implemented in such a way that they will mostly perform their tasks on their own [1]. The goal is to relieve load from the microcontroller and transfer it to the logic silicon portion of the smart switch. For instance, PWM signal would not have to be implemented by the microcontroller anymore. Instead, such signal could be generated internally, thus saving costs and simplifying the design from an application point of view.

Figure 1.3 and table 1.2 show the change in architecture associated to moving from 12 to 42 V. If each load were controlled by their own semiconductor device, the switching contact of the ignition lock would not be necessary anymore since it could be emulated via software (as a control signal to the semiconductor device). However, the number of branches which sink a certain amount of leakage current would increase. This, together with the increase of voltage, would bring up a limitation related to the quiescent current which could be delivered by the battery to guarantee a proper service long-term wise. Therefore, the semiconductor industry will have have to meet this requirement in order to justify the change from 12 to 42 V.

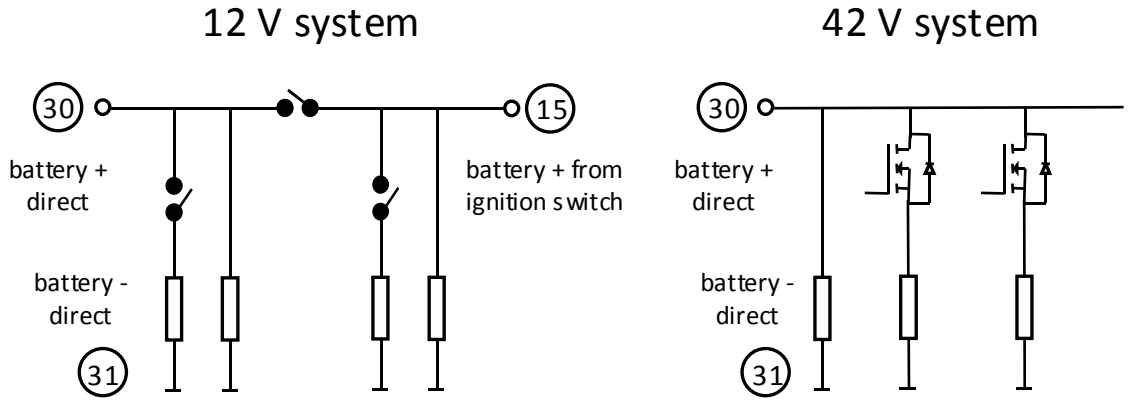

Figure 1.3: Change in architecture and application of smart switches

Battery terminals used	30, 31 and 15	30 and 31
Battery size	800 Wh	800 Wh
Battery voltage	12 V	42 V
Battery charge	66 Ah	19 Ah
Total quiescent current	18 mA	5 mA
No. modules	60	60
Quiescent current per module	300 µA	80 µA

Table 1.2: Change of requirements associtated to the new 42 V architecture

1.1.1. A practical example of smart power technology

Since the system analyzed in this thesis work uses a smart power switch, the main approach followed to implement this kind of technology will be introduced in this section. Although the technology described hereafter is not state-of-the-art, the principles and concepts mentioned will be useful to the reader. The technology in question includes the use of n-channel VDMOS (vertical double-diffusion MOS) structures among others. This strategy is mainly adopted to reduce the chip area with respect to other configurations like lateral diffusion. A simplification of the structure used for VDMOS switches can be observed in figure 1.4. For automotive applications, the backside of the device will be connected to the battery voltage supply and will act as the drain of the device. The n^- epilayer will determine the voltage withstanding capability of the switch. On top of this, the vertical configuration will allow for paralleling of several cells in a relatively small amount of silicon area, significantly reducing the effective on-resistance of the device [2]. All in all, this configuration results in very good current and voltage handling capability, which is very suitable for most automotive applications.

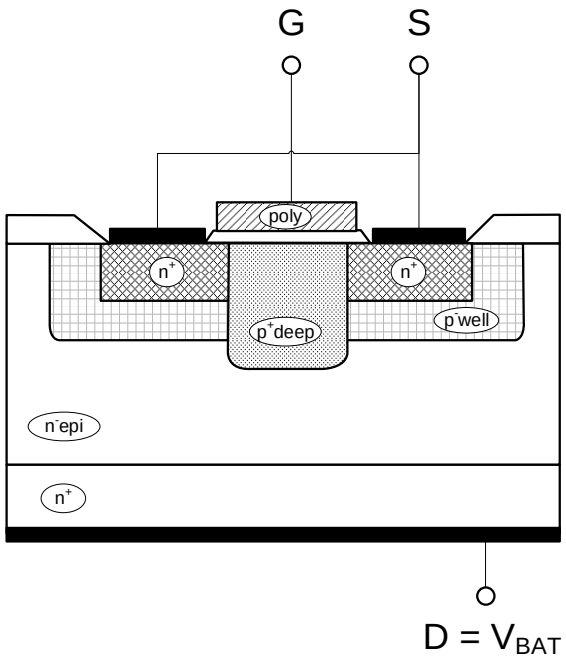

Figure 1.4: Simplified structure of a VDMOS realized in the described smart power technology

The temperature range that these devices will have to withstand may go between -40 and +125 °C. The power dissipated in the switch has to be therefore minimized to keep the device at a safe temperature operation. This can be achieved for example by making turn-on and turn-off transitions

strong and rapidly. For this reason, a charge-pump circuit is typically used. Such circuit topology capable of level-shifting can be realized making use of CMOS technology. The n-channel transistors which are not part of the power silicon will lay on the common n^- epilayer embedded at the same time in a p^- well. A supplementary n-type deposition with low doping levels will be required to form a lightly doped drain structure combined with the n^+ source and drain implants. This, together with field-plate termination, will provide them with the isolation level required to withstand large voltage values [2].

Another important demand in the automotive industry is the mass production capability. The technology presented as an example in this section makes use of a reduced mask sequence which involves well-known steps of relatively low complexity. For this reason, a p^- well will be diffused before polysilicon deposition. This layer will act as the p^- body for the power VDMOS and as the p^- substrate for the n-channel transistor. Double-diffused self-aligned gate MOS devices are not conventionally built up this way. However, the channel length of power VDMOS is not a limiting factor and the beneficial effects of using traditional double diffusion are not so critical. On top of this, a p^+ deep diffusion will be required to short the p^- body to the n^+ source diffusion of the power VDMOS. At the same time, this n^+ diffusion will be used to make up the n^+ source and drain terminals of the NMOS devices [2].

The charge-pump circuitry will require a sufficiently high-value and fast capacitor to raise the gate voltage above that of the battery at the desired switching frequency. Consequently, the technology will also include an n^+ implant that will be placed under the MOS capacitor structures. This will guarantee that the gate driving criteria are met [2].

In summary, the masking steps of the technology are the following:

1. p^- well
2. deep p^+
3. n^- deposition
4. n^+ cap
5. thin oxide
6. polysilicon
7. n^+ source-drain
8. contact
9. aluminum

Nine steps are required in total, thus complying with the cost-limiting requirements for a technology which focuses on mass production for automotive applications. figure 1.5 shows the cross section of the described smart power technology in a simplified manner. The different masking steps mentioned before can be observed at the different device structures.

Five main devices can be fabricated in the smart technology described in this section:

- Low-voltage p- and n-channel transistors
- High-voltage p- and n-channel transistors
- VDMOS switch
- Zener diode
- MOS capacitor

Both low-voltage n- and p-channel devices in the logic portion of the silicon will use an intermediate voltage supply V_{DD} lower than that of the battery V_{BAT}. Additional circuits such as discharging devices compatible with inductive loads, short-circuit detection devices, short-circuit protections, overvoltage protections, gate protections and temperature detection devices are typically implemented in a smart

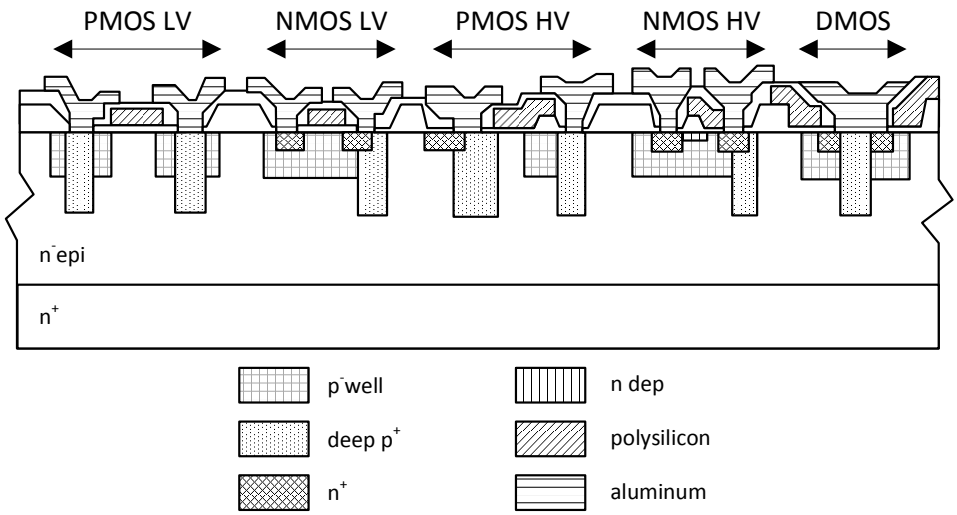

Figure 1.5: Overview of the cross-section of the described smart power technology

power switch. The logic part of the silicon will be mainly dedicated to generating signals to interact with, for instance, an external micro-processing unit [2].

The concepts introduced in this section can be put together to design a smart switching device as a solution for a specific application. As an example, a practical realization of a high-side power switch is described in [3]. The application demands a switch which is capable of selectively powering LED and bulb loads in order to minimize the manufacturing and assembling costs. The requirements for these two types of loads are significantly different, and therefore two different switching configurations would have to be realized. On top of the traditional relaying function, the device is equipped with a communication protocol to interact with other devices in a microcontroller-based application, slew rate control to meet EMI requirements, embedded protection features against short circuits, overcurrent and overtemperature, sensing of load current and open-load detection. This solution was achieved by making use of a single device as a result of using smart technology. On the other hand, using traditional relaying devices would have required at least two devices with different characteristics suitable for each application.

1.2. LEDs in automotive applications

LEDs are semiconductor devices (pn junctions) that produce light due to a phsyiscal phenomenon known as electroluminescence. It consists in the emission of light when a material is exposed to an electric field and current. From a practical point of view, when an LED is applied certain voltage level between its terminals with the required polarity (the pn junction has to be forward biased in order to emit light) a recombination process is triggered: electrons from the conduction band cancel out with holes from the valence band. As a result, photons (and heat) with an amount of energy which depends on the band gap level of the semiconductor are released. The color of the light emitted by the device depends therefore on the material used. As a consequence of the forward biasing a current will flow through the pn junction. This current will determine the number of electrons which recombine and therefore the number of photons which are released. This means that the luminosity will be mainly determined by the current flowing through the LED. Figure 1.6 and figure 1.7 show two characteristic curves that depict the overall behavior of an LED device from the manufacturer CREE (CREE XLamp XP-L2 [4]). It can be seen how the voltage drop across the device increases with the current and how the luminosity is very dependent on the forward current.

LEDs are becoming more and more popular with respect to other lighting devices in the latest years. What is more, the penetration of LEDs within the automotive industry is predicted to keep increasing even further. New technologies and devices are emerging and those which remain are becoming more

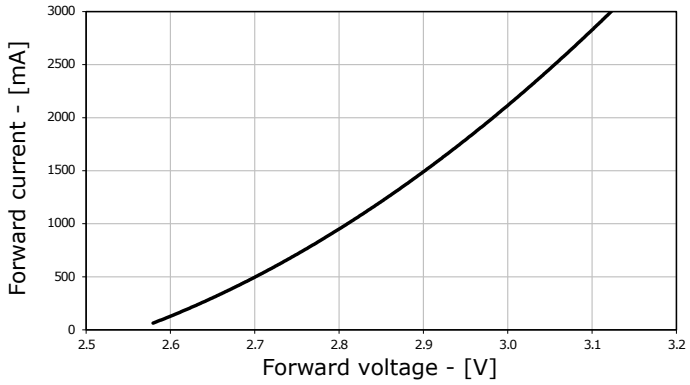

Figure 1.6: Voltage vs. current of the CREE XLamp XP-L2

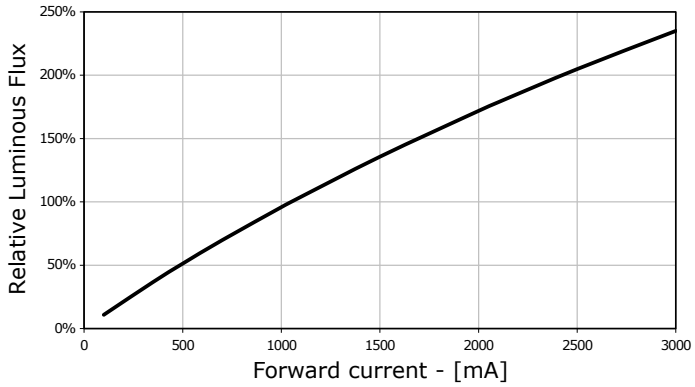

Figure 1.7: Relative luminosity vs. current of the CREE XLamp XP-L2

and more optimized and used. Overall, LED technology is constantly growing and evolving towards what will be the future standard in the lighting market [5]. The main advantages of LED lighting with respect to traditional lighting devices such as bulbs used for automotive applications are:

- High reliability. LEDs are very reliable compared to light bulbs. This is a very important aspect in a field such as automotive where safety standards are so relevant. LED lights are resistant to shock, vibrations and impacts, and therefore they make great outdoor lighting systems for rough conditions. On top of this, the lifetime of LEDs can be in the order of 100000h [6].
- High luminous efficacy. Maximizing the luminous efficacy will yield in lower power losses. Energy efficiency is playing a more and more important role in an industry which seems to be getting greener and greener. LEDs have a luminous efficacy in the order of 100 lm/W and more [7], while traditional light bulbs operate at a value of around 10 lm/W [8]. Figure 1.8 show an efficacy comparison between different light sources. It can be seen how LEDs deliver the maximum amount of light for a given electrical power. What is more, LED technology is expected to make substantial increases in efficacy in the short term [7].
- Fast switching possible. Unlike traditional light bulbs, LEDs can be used with techniques such as PWM for dimming [9].
- Short turn-on time. Compared to traditional light bulbs, LEDs present a very short warming up time and can reach full brightness operation in a very brief amount of time. According to [10] the turn-on and off times of LEDs is in the order of nanoseconds.
- Flexibility. LEDs can be put together in any shape or pattern to produce a final lighting system with full dynamic control. Lighting effects can be achieved and the emission of light can be modified in many ways.

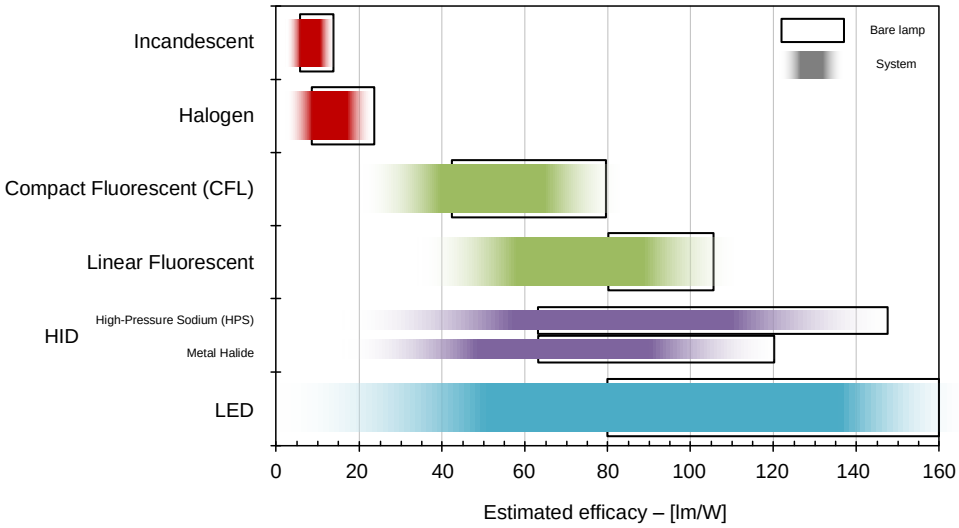

Figure 1.8: Approximate range of efficacy for various light sources. The rectangular boxes correspond to the efficacy of a bare lamp. The gradient area corresponds to the efficacy of the whole lighting system including other loss mechanisms.

On the contrary, LEDs also present some drawbacks with respect to traditional solutions:

- Cost. LEDs are considered too expensive in many applications compared to other light sources. Manufacturers however keep working on reducing production costs while increasing the light output of their devices. However, LED prices have decreased in the latest years, pulling forward the payback time of this lighting systems [5].
- Lack of standardization. Due to the constant growing and evolving of the LED market standardization is not as well defined as with, for instance, traditional light bulbs.
- Need of a driver. Driving a light bulb is generally much easier than controlling a LED. A driver circuit will be needed in order to manage all the aspects that play a role in the light emission characteristics of this kind of lighting system. On the other hand, the possibilities available will always be more than those given by traditional solutions.

According to [11] lighting solutions for automotive applications can be categorized as for the current level and the nature of the energy conversion. Figure 1.9 shows the different groups and the main differences between them. This thesis work focuses on an application which is intended to be used together with high-current LEDs using a DC/DC converter. Therefore, the system analyzed in this document would fall into the category in the upper right hand corner of the figure.

An overview of the broad range of lighting solutions for automotive applications is presented in [12] and [13]. A summary of the possibilities is given below:

- Exterior lighting. The main advantage of using LEDs for exterior lighting consists in the flexibility given by this technology. Vibrant and highly customizable solutions can be created with respect to traditional options. On top of this they offer an almost immediate response and a very long lifetime which suits very well automotive applications where safety is a key element. LEDs can be used in all kind of configurations:
  - Headlamps
  - Adaptive headlamp
  - Daytime running
  - Fog
  - Position
  - Stop / tail

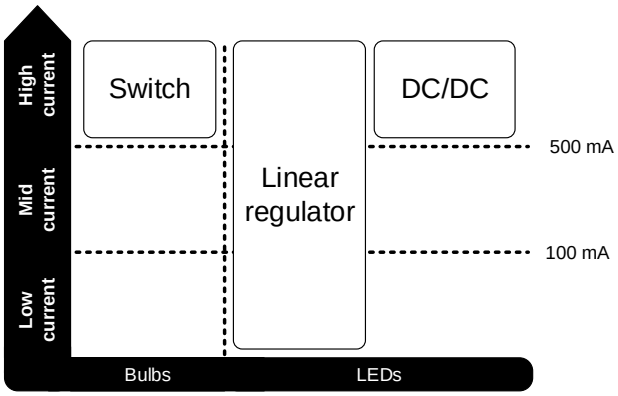

Figure 1.9: Different categories of lighting solutions and their automotive applications.

  - Turn

- Interior lighting. This kind of lighting should maintain its level even during transients on the input voltage. Also, some LEDs need to be turned on when certain maintenance operation is required, either constantly on or flashing to gain the driver's attention. The most common applications are:
  - Dome
  - Foot well
  - Tell tale
- Backlighting infotainment and cluster. This plays an important role on the interaction of the driver with the automobile system. LEDs bring up a broad range of possibilities to offer adaptive and customizable options that will improve the driving experience and comfort.
  - Hybrid cluster.
  - Digital cluster.
  - Backlighting / head units.

1.3. DC/DC converters in automotive applications

Figure 1.10 depicts an example of the power tree used in automotive applications as described in [14]. The battery (either 12 or 24 V) will be tipically connected to protection devices related to voltage, current and reverse polarity. After this, a boosting stage will be used in order to guarantee a minimum voltage level during cranking. Wide input range DC/DC converters will be connected subsequently to this voltage bus in order to power other buses or directly feed vehicle loads such as LED chains.

Automotive environments face a very wide temperature range and also produce high levels of input transients and interference. In addition, power supplies must be able to withstand load-dump transients. Currently, most of the automotive applications run from a 12 V battery. However, many regulators are rated for 28-40 VDC to handle transients that get through the previous stages and protections. Supplies that were not directly attached to the battery would not need such high voltage input specification. Many of the switched DC/DC converters used in automotive feed downstream LDO regulators to deliver cleaner power. All in all, power management in automobiles has become a complex task mostly due to the large amount of requirements that power supplies have to meet. Some of these are:

- Multiple output voltages with different current ratings. Many diverse loads are used in an automobile: microprocessors, alarms, GPS system, displays... For this reason DC/DC converters are used along with linear regulators [15].

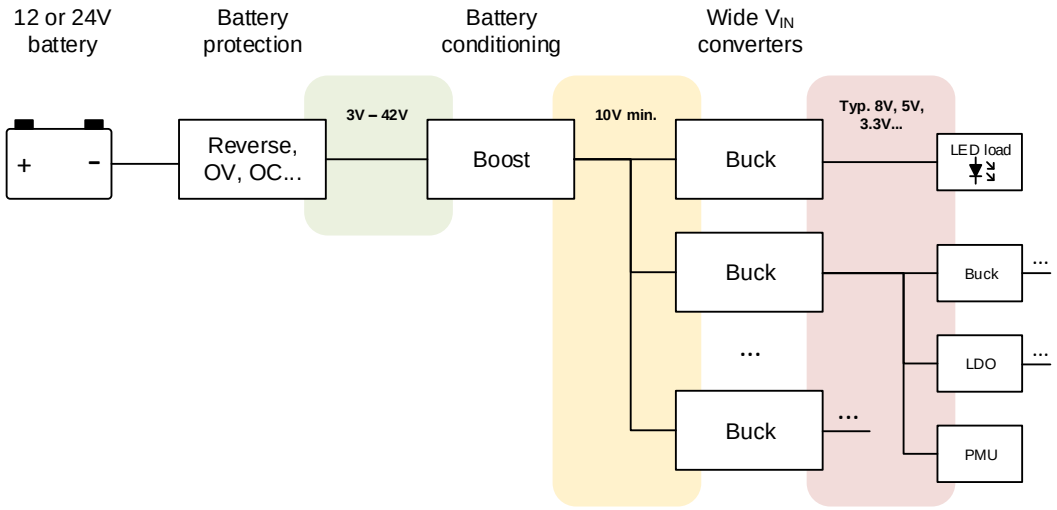

Figure 1.10: Typical automotive power tree.

- Wide input voltage range. The power management system has to be able to withstand conditions such as cold-cranking, load dumping and battery jumping [16].
- Low quiescent current. When the ignition is off the battery drain has to be minimized in order to extend the battery charge in time [15].
- Low noise. EM requirements are relevant since the power management system is implemented together with many radio reception and video display units that could be affected by noise generated in the power supply [15].
- High efficiency. The industry is looking for greener and greener solutions in order to minimize the power losses that result from the conversion of energy. Efficiency is the main advantage of DC/DC switched converters with respect to linear regulators.
- Low cost. The amount of parts used to implement a power management solution has to be minimum and the system should be as simple as possible in order to reduce costs.

According to [15] and [14] DC/DC switched regulators are used in the following automotive applications:

- Infotainment:
  - Instrument cluster and displays
  - Telematics
  - USB hub / charger
  - Audio amplifiers
- Advanced driver-assistance systems:
  - Camera modules
  - Radar systems
  - Park assistance
- Powertrain:
  - Start-stop voltage conditioning

  - Fuel pump
  - Fuel injection
  - Emission control and sensors
- Body electronics:
  - LED headlamps and lighting
  - HVAC controls
  - Door sensors and locking

It can be observed how the possibilities are numerous. This enables DC/DC converters to be used in a vast number of potential applications. Each of them will be associated to certain set of boundary conditions and requirements that have to be met by the specific solution.

1.4. Rapid Control Prototyping

Rapid Control Prototyping is a method used to develop, test and optimize control schemes in a relatively quick way. In this case, a set of hardware devices from the manufacturer dSPACE will be used to implement the control algorithm of the DC/DC converter presented in this document. The programming is realized by means of MATLAB Simulink following a block approach. A set of basic blocks (logical operations, counters, registers, math operations...) are available to the user. More complex blocks can be built from this in order to implement the necessary functionality. Additionally, the user can also enter manual code to create functions when implementing the control solution. This approach serves as an alternative to manually programming in VHDL. The user does not have to deal with lower level functions but still have to consider implementation aspects so that the functionality will be as desired.

Module	**Functionality**
DS1005	PowerPC 750GX running at 1 GHz
	Provides the basis of dSPACE's modular hardware
	Interface to the I/O boards
	Interface to the host PC
DS5203	FPGA Xilinx Virtex®-5 SX95T-2C
	6 ADC channels: 14 bits pipelined, 10 MSps
	6 DAC channels: 14 bits, 10 MSps
	16 digital I/O channels
	Connection to the processor board via PHS bus
DS5203M1	Piggyback module for the FPGA board DS5203M1
	6 ADC channels: 14 bits pipelined, 10 MSps
	6 DAC channels: 14 bits, 10 MSps
	16 digital I/O channels
	Connection to the processor board via PHS bus

Table 1.3: Description of the dSPACE's modular hardware used to implement the control of the DC/DC converter

The system to be implemented can be easily simulated together with the system of interest before downloading the application to the hardware platform. This way, further verification and debugging can be performed to guarantee that the solution behaves as intented. The dSPACE device includes both the processing unit, the FPGA and the interaction hardware. In order to obtain the desired behavior

from the DC/DC converter several signals will have to be monitored and taken into account within the control loop. On top of this, the operation of the dSPACE system can be observed in real time on a PC using a dedicated software from dSPACE.

Table 1.3 presents the different modules that make up the dSPACE system used for this thesis work. The main hardware unit is based on a PowerPC that takes care of little time-demanding calculations and interfacing with the rest of the modules. It also provides real time communication with the host PC. The FPGA module can be programmed via MATLAB Simulink and provides the system with access to ADCs, DACs and I/Os to physically interact with the converter. The user does not have to manually program any lines of code: the block-based system designed on MATLAB Simulink will be translated and coded into VHDL and downloaded to the FPGA. Lastly, an extension board with additional digital and analog interfaces is used to provide the dSPACE with more input and outputs. The voltage range of the ADCs, DACs and I/Os can be programmed via software by the user.

1.5. LED driver concept developed in the thesis

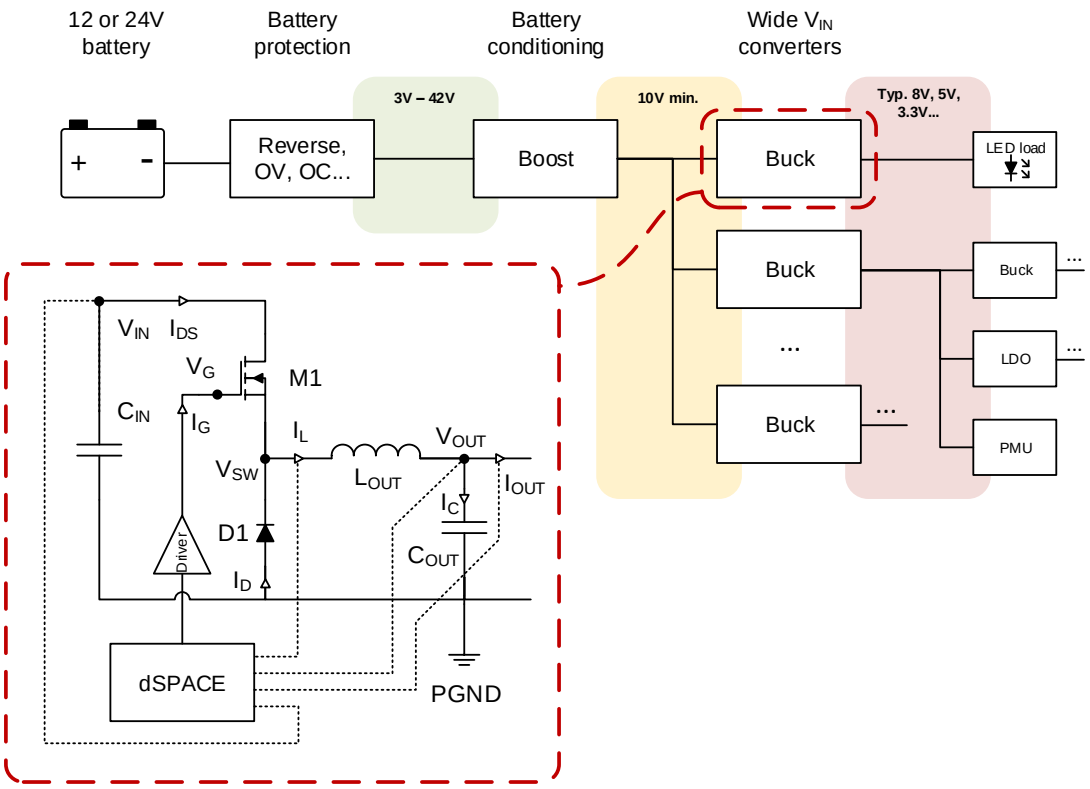

Figure 1.11: Context and structure of the LED driver developed in this thesis work.

The LED driver developed for this thesis work will be introduced in this section. Figure 1.10 was presented before as an illustration of a typical power tree implementation. The DC/DC solution analyzed in this document will be one of the components of this power management scheme. The converter will have a buck topology and its input will be typically connected to a boost converter to condition the battery voltage. A synchronous topology (which uses active devices for both high-side and low-side of the switching leg) could be used to obtain very high efficiency, especially for high current applications. However, this would introduce complexity in the design phase. A simpler topology, namely asynchronous, will be adopted since the main goal of this thesis work is to analyze the feasibility of Infineon's smart technology for DC/DC applications. Further topology improvement and optimization will be performed at later development stages. An active device will be used at the high-side of the

switching leg while a passive device will be placed at the low-side. The buck converter will be used to power LED loads. The specific applications in this field are several, and they could be based on both current or voltage source operation of the regulator. The converter presented here will be used as a flexible approach to perform system-level analysis on LED driving concepts before the integrated circuit design phase. This will allow to draw practical conclusions on the feasibility of Infineon's smart technology for LED driving applications.

Figure 1.11 depicts the concept analyzed in this thesis work and table 1.4 gives an overview of the main parameters and variables of the DC/DC converter. A buck topology will be used since it suits the application very well: for DC, the output coil is placed in series with the output load. As a result, buck converters can be easily controlled as current sources. On the other hand, voltage source operation will also be possible for LED applications which demand so. As for the high-side switch, it will require a floating driver to charge and discharge the gate when needed. Initially, an asynchronous topology will be analyzed, making use of a diode as the low-side device. This diode will free wheel the filter current when the switch is off. The input and output capacitors of the converter will be typically implemented in practice as several passive devices in order to obtain an effective frequency response as close as possible to the ideal case. Lastly, the dSPACE tool will be used to implement the control algorithm. The main parameters that could be fed back to the controller will be the input voltage, the coil current, the output voltage and the output current.

Name	**Description**
M1	High-side power switch
D1	Low-side power diode
C_{IN}	Input capacitor
L_{OUT}	Output filter inductor
C_{OUT}	Output filter capacitor
Driver	High-side floating gate driver
dSPACE	To implement the control algorithm
V_{IN}	Input voltage
V_G	Switch gate voltage
V_{SW}	Switching node voltage
V_{OUT}	Output voltage
P_{GND}	Power ground
I_{DS}	Switch drain-source current
I_G	Switch gate current
I_D	Diode current
I_L	Inductor current
I_C	Output capacitor current
I_{OUT}	Output current

Table 1.4: Parameters, variables and subsystems of the DC/DC converter

Table 1.5 shows the intial specifications of the DC/DC converter that will be developed in this thesis work. Since the input voltage will be preceded by a boost converter that will condition the battery voltage, the range of operation goes from 10 to 25 V. The output will have to feed one or several chains of LEDs. Therefore, the number of chained LEDs will roughly determine the voltage at which the converter has to operate (between 5 and 20 V). The maximum current to be delivered by the converter is limited by the maximum power dissipation that the switch can handle. The minimum output current

relates to the minimum current required to drive a led at the output. The input current limit values are derived from the maximum and minimum values of output current, output voltage and input voltage that can be handled by the converter.

Another important aspect of the LED driver is the switching frequency at which it will operate. The main factor to push the frequency as high as possible will be related to minimizing the size of the passives that form the output filter of the buck converter. This will have a huge impact on the size and price of the solution. However, pushing the frequency upwards will yield higher dynamic losses at the switch since more and more transitions will take place per unit of time. The switching frequency will also play a big role in terms of electromagnetic compatibility.

As stated before, an asynchronous topology has been adopted. Using a synchronous topology would typically yield higher efficiency due to the smaller voltage drop for a given current typical of MOSFET devices with respect to diodes. However, the higher amount of silicon that would have to be used is not really justified for these levels of current (table 1.5).

Parameter	**Min.**	**Max.**
V_{IN}	10 V_{DC}	25 V_{DC}
I_{IN}	0.2 A_{DC}	3.2 A_{DC}
V_{OUT}	5 V_{DC}	20 V_{DC}
I_{OUT}	1 A_{DC}	4 A_{DC}

Table 1.5: Input and output specifications of the DC/DC converter

The control scheme used will effectively turn the DC/DC converter into an LED driver that sets certain variable to a reference value. Different possibilities will be analyzed and discussed from a theoretical point of view and a comparison will be made in order to determine which alternative is best for the application of interest. Since this thesis work addresses the first stage of the development phase, the control scheme will be implemented using external hardware (dSPACE). In other words, the analysis presented in this document serves as a feasibility study of the possibilities that could be realized with Infineon's smart technology. Later design stages will focus on integrating the whole solution in a single silicon chip that could be sold commercially.

1.6. Motivation

The motivation for undertaking the research can be explained by having a look at the potential benefits of using Infineon's smart technology for DC/DC applications. In terms of cost and mass production, the smart technology would provide a very cost-effective solution for the automotive industry. The growing role of LEDs in lighting applications together with an affordable and robust solution that could be used to drive these devices would be a very attractive product to car manufacturers.

As for system integration, Infineon's smart technology would also be very advantageous. The whole system solution could be integrated in one package using a single technology. The amount of silicon used would be therefore minimized. Not only would cost be lower but also the overall complexity of the solution from an integration point of view. Digital circuitry and regulation loops could be implemented in smart technology along with power devices and their respective gate driving circuits. For instance, an ADC together with logic devices could be realized on chip. On the other hand, an analog approach based on implementing a compensation network using an operational amplifier could also be an option.

On the contrary, complex and state-of-the-art available technologies would be more expensive, especially when it comes to mass production. From an integration point of view, several subsystems would have to interact together since integrated solutions are not generally available. A better performance could be achieved, but mass production would be a more expensive option.

In order to provide the reader with a practical example of how the smart technology could be beneficial with respect to other available options, Infineon's LITIX^{TM} solution will be presented. The application drawing of a solution which uses Infineon's TLD5501-2QV [17] (dual-channel synchronous buck

controller with SPI interface) is shown in figure 1.12. It can be seen how one silicon chip integrates the control of the converter as well as the gate driving circuits and some other extra features (2 channels are provided). However, the power devices are not integrated on chip and therefore the solution would require of additional power silicon devices (2 more per channel). As for the passives required for the proper operation of the buck converter, coil and input and output capacitors would be present for each channel. On the other hand, the solution could be integrated on a single chip using smart technology. All in all, Infineon's new approach would provide DC/DC lighting applications with robust and solid solutions at a much lower cost, keeping system size and complexity at minimum levels.

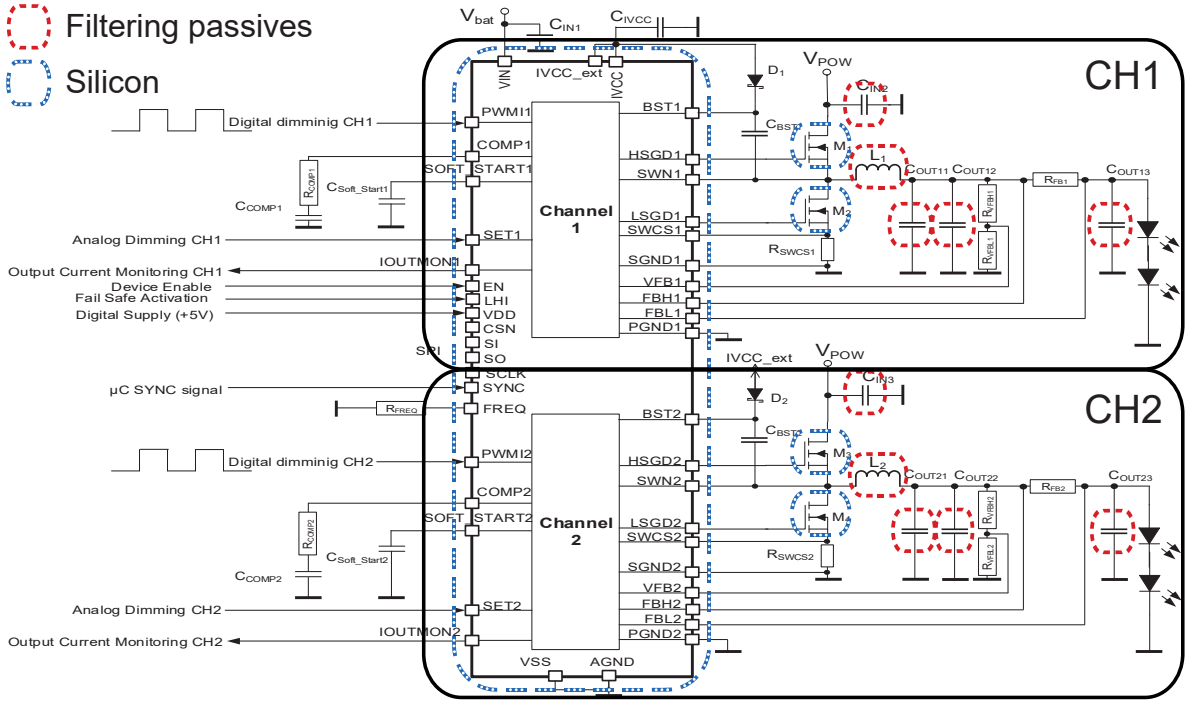

Figure 1.12: Application drawing of Infineon's TLD5501-2QV as a current regulator.

1.7. Research questions

The academic study presented in this report focuses on a set of questions that will be answered along the different chapters and sections of the document. The first research question that arises is related to the feasibility of the implementation. Infineon's smart technology is in use for several applications in the automotive industry. However it has not be determined yet whether it can be used in DC/DC converter applications that require a switching frequency in the order of hundreds of kilohertz. An answer to this question will be given firstly making use of a simulation approach. Once the obtained results prove that the application can be realized from a theoretical point of view, another question arises: how much current has to be supplied to the device in order to achieve the desired switching frequency? Or in other words, how fast can the device be switched for a given gate current level? Proceeding as before, the topic will be firstly tackled with a simulation approach. When the order of magnitude of this current is determined, a physical system capable of delivering such amount of charge to the gate will be required. What driver circuit meets the requirements needed for this application? This question will also have to be answered in order to prototype the solution for the validation of results.

Another research question focuses on the efficiency of the converter. The amount of power which is dissipated in the switch and the whole system is of vital importance. Therefore, the loss mechanisms of the switch and the converter will have to be pinpointed and studied in depth. The answer to this question will provide the reader with an estimation of the losses and the overall efficiency of the system. As a consequence of this answer another question will arise: can the losses be estimated for different input parameters so that the system could be, for instance, optimized efficiency wise?

Since one of the ultimate goals of the project consists in realizing a prototype of the system to prove its fitness for DC/DC applications, the next research question will be related to this. What is the best way to implement the system? How can the different parts of the system interact with each other and be put together? What considerations have to be taken into account to guarantee that the results obtained with the prototype are solid and valid? How can the prototype be optimized?

The control scheme that will be implemented on the converter is another relevant research objective. When having a look at the literature and state-of-the-art solutions, many options are available. Each of them presents several advantages and disadvantages. Having a specific application in mind, such advantages and disadvantages will have to be evaluated with respect to the desired operation of the DC/DC system. Different control topologies that turn the converter into an LED driver will be tested and compared in order to clarify which of the possibilities suits the application the best. Once the most fitting control scheme have been selected, a specific design be proposed. A couple of further questions related to this will be addressed. Firstly, a methodology to design the controller will have to be determined. Additionally, the response of the system to different transient phenomena will have to be evaluated.

The last set of research questions relates to the practical implementation of the chosen control scheme. The analysis performed up to this point regarding the control scheme has been mainly theoretical and based on simulation. How can such approach be implemented on the prototype using the dSPACE system? How can it be optimized? What considerations and limitations have to be taken to implement the solution in practice? Do the results obtained match with simulation?

1.8. Outline of the thesis

The first section of this thesis report introduces the topics that will be useful to the reader in future chapters. Concepts such as smart power technologies, smart switches, LEDs and DC/DC converters in automotive applications are presented. Additionally, the LED driver developed during this thesis work is introduced to the reader. To conclude with the first chapter, the research question that will be answered throughout this document are presented.

Chapter 2 focuses on answering some of these research questions: how fast the converter can be switched and how much current is needed at the gate of the MOSFET to achieve this. The feasibility study is addressed with a simulation approach. The models used to draw conclusions and results are presented in this section. Additionally, the power losses in the switch computed using simulation software are shown in the report. From this calculation, the ultimate efficiency of the converter can be estimated to get a rough idea of what values could be achieved.

A more thorough study about the power losses is given in chapter 3. The main and firstly identified loss mechanisms are pinpointed and analyzed in depth here. Loss models are presented to the reader in order to get an insight on how these estimations are derived. The ultimate goal of this approach is to obtain a loss calculator that is able to output an estimation of the system power losses for a given set of inputs. Such loss calculator is compared to the results obtained during simulation to validate its accuracy.

Chapter 4 focuses on the physical implementation of the floating high-side driver. The required gate current and the switching frequency limitations can be transferred into specifications for a driver circuit. Two systems are presented and analyzed in depth in order to prove their suitability for the application. At the end of the chapter, practical results obtained at the lab are shown to the reader to demonstrate that the practical implementation of the driver is feasible.

Once the driver implementation is known and practical measurements to prove its feasibility have been taken, the motivation to improve the overall setup of the system is proposed in chapter 5. In order to obtain a better overall behavior, the DC/DC converter is implemented on a PCB that interacts with the driver board. The steps and considerations taken to optimize the design are introduced. A set of open-loop measurements are shown to the reader in this section. Further investigations will be carried out in order to obtain a better loss model of the system which matches with the obtained results. This will lead to a further optimization of the prototype and a full understanding of all the loss mechanisms present in the prototype.

Chapter 6 elaborates on the control of the converter from a theoretical point of view. At this point several topologies will be introduced and analyzed to establish a comparison. The objective is to determine which control strategy suits the application the best. The DC and AC characteristics of the converter are analyzed by having a look at the equations that model the system. The different transfer functions will be derived in order to analyze the loop characteristics and stability. A control design will be proposed in this chapter and several simulation results will be shown to evaluate the performance of the system.

The implementation of the most suitable control algorithm on the lab prototype is presented in chapter 7. The steps taken to implement the solution are shown together with practical considerations and limitations. The behavior of the system will be analyzed and a set of measurements will be shown in this chapter to validate the previous theoretical analysis.

To conclude, chapter 8 puts together the final and overall conclusions. The suitability of Infineon's product line for this application is summarized in this section and the project outcome is presented end evaluated by means of answers to the research questions. The work carried out has still further possibilities to elaborate on which were out of the scope of this thesis. Future work possibilities will be presented here to the reader as a final remark.

2

Feasibility study based on simulation

The second chapter of this document focuses on the simulation work carried out to demonstrate whether Infineon's smart technology can be used for the desired application. Section 2.1 firstly presents the test chip used for this thesis work. Knowing the device's dimensions will allow the detailed model to give accurate results that could be compared afterwards to the prototype measurements. Once the test chip is introduced, the driver used in the simulation will be explained and analyzed to make the reader familiar with the concept in section 2.2. The whole model of the system will be shown later on in section 2.3 together with simulation results. Section 2.4 presents the main conclusions after the simulation work has been carried out. These relate to the switching frequency and driving capability of the converter as for the switch and driver limitations. Sections 2.5 and 2.6 address the problem from a quantitative point of view: the losses in the switch and the total converter limit efficiency will be presented here. Lastly, section 2.7 puts the conclusions drawn from this chapter's work together.

2.1. Introducing the test-chip

The features an characteristics of the device which is analyzed in this thesis work must be known beforehand in order to extrapolate them as input parameters in the simulation. It is crucial to know what is implemented on the device available at the lab, since it will be used to ultimately realize the prototype of the system. The test chip in question is a Double Diffused MOS structure (refer to section 1.1.1.1) or DMOS implemented in Infineon's smart technology. The device has two channels (A and B), each of them being able to operate separately. Each channel incorporates two gate contact terminals (G1A, G2A, G1B and G2B in total), a source contact terminal (OUTA and OUTB in total), a common drain terminal (VDD) and a temperature measurement terminal (which is not relevant for this study). For this specific application only one channel of the device will be used.

Regarding the power handling capability of each channel, the most important values will be related to the physical dimensions. The size of the implemented DMOS will be the main input to the model of the switch that will be used for simulation. Table 2.1 presents the most relevant quantity, namely equivalent on resistance, of the used DMOS.

Physical dimensions will be used as input for the switch model in the simulation, which will define the DMOS structure and account for all the modelled phenomena. The on-resistance at 150 °C is estimated from the total silicon area as a worst case scenario approximation.

Parameter	**Value**
$R_{DS,on}$ (@ 150 °C)	14.1 mΩ

Table 2.1: Ddefining quantities of the DMOS implemented in the available test chip

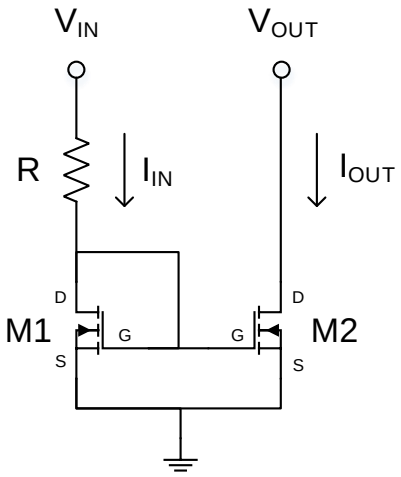

Figure 2.1: Basic configuration of a Widlar current mirror using NMOS enhancement transistors

2.2. Modelling and simulating the driver concept

The concept used at this section to model the gate driver that will charge and discharge the DMOS is based on Widlar current mirrors. This approach has been chosen due to its versatility and simplicity. It is a circuit topology that appears very often in integrated circuits since the matching between transistors that can be achieved at this level is good enough. If a current mirror approach were to be realized using discrete components, more advanced configurations that provide the implementation with feedback should be used.

A current mirror can be seen as a current-controlled current source that copies a given current through an active element. It can be split up into two different conversion steps: current to voltage, where the first active element or transistor creates a voltage reference from an input current; and voltage to current, where the second element or transistor reverts this voltage reference to a current value at the output of the mirror structure. If the matching between the two transistors is ideal, then the two currents are exactly the same (given the output voltage of the mirror equals the gate-source voltage of the input transistor).

Let us focus on a MOSFET based current mirror. Figure 2.1 shows the basic circuit configuration of a Widlar current mirror using NMOS transistors, where both M1 and M2 are enhancement mode devices. The input transistor M1 is a so-called diode-connected transistor since its gate and drain are shorted:

$$V_{DG,M1} = 0 \longrightarrow V_{GS,M1} = V_{DS,M1} \tag{2.1}$$

M1 will be in saturation if $V_{GS,M1} \geq V_{th,M1}$ and $V_{DS,M1} \geq V_{GS,M1} - V_{th,M1}$ [18]. Let us assume that the input voltage is sufficiently high for a given set of R and input current I_{IN} to guarantee $V_{GS,M1} \geq V_{th,M1}$ ($V_{GS,M1} = V_{IN} - RI_{IN}$). Then M1 will be in saturation mode. Let us also initially neglect the channel-width modulation effect. Then it can be written that (reference):

$$I_{D,M1} = K_{M1} \times (V_{GS,M1} - V_{th,M1})^2 \tag{2.2}$$

Where K is a constant that relates to the MOSFET process and both width and length of the channel [18]. It can be shown how certain gate-source voltage is obtained for a given set of transistor parameters, input voltage and resistor. By looking at the circuit configuration:

$$\frac{V_{IN} - V_{GS,M1}}{R} = K_{M1} \times (V_{GS,M1} - V_{th,M1})^2 \tag{2.3}$$

In other words, the transistor M1 acts as a current to voltage conversion element (certain gate-source voltage is generated for a given input current). By the way M1 and M2 are connected it can be seen that $V_{GS,M1} = V_{GS,M2}$. This means that:

$$I_{D,M2} = K_{M2} \times (V_{GS,M1} - V_{th,M2})^2 \tag{2.4}$$

If the following holds:

$$V_{GS,M2} \geq Vth, M2; \tag{2.5}$$

$$V_{OUT} \geq V_{GS,M2} - V_{th,M2} \tag{2.6}$$

The first condition is fulfilled given M1 is in saturation and assuming ideal matching between M1 and M2; the second condition implies that the output voltage must be larger than a certain minimum value in order to guarantee proper operation of the current mirror. Figure 2.2 depicts the concept from a graphical point of view. The channel width modulation effect is not neglected here. The slope of the VI curve of the transistor at saturation mode will create a deviation between $I_{D,M1}$ and $I_{D,M2}$ due to each transistor having a different drain-source voltage. This means that the current mirror does not behave as an ideal current source but instead has a finite output resistance equal to the output resistance of the respective output transistor. In practice such effect is not so pronounced and it will only add up a relatively small amount of error if the current mirror is dimensioned correctly.

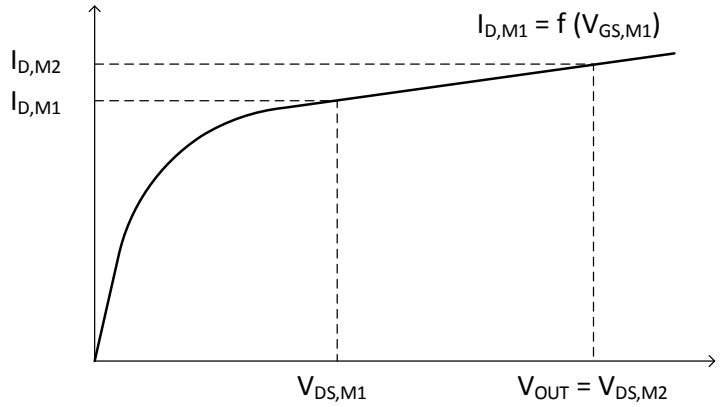

Figure 2.2: Graphical representation of current mirroring based on the VI characteristic of an NMOS transistor

It can be concluded therefore that the current through M2 is a mirrored value of the current through M1 with a certain amount of error (due to mismatching and channel width modulation) assuming that the output voltage is higher than a minimum value.

The current mirror structure can be paralleled as many time as needed in order to obtain different current ratios. Also, the width and length of the channel can be left as another degree of freedom to achieve multiplication ratios different to 1. It can be noticed how the output current has a sinking direction with respect to the load. The direction of the current can be reversed if desired by making use of PMOS transistors. Figure 2.3 shows this approach. As long as M1/M2 and M3/M4 match with each other the mirroring of the current can be considered ideal for a first approximation. The first part of the mirror built with NMOS transistors works as described earlier. The PMOS transistor M3 will convert the reference current $I_{D,M2}$ into a voltage $V_{GS,M3}$ which is the same as $V_{GS,M4}$. Assuming again the matching of these two transistors for a first approximation, M4 will convert this voltage $V_{GS,M4}$ into a current $I_{D,M4}$ which equals the input current.

The basic idea of a gate driver is an ideal current source which charges and discharges the input capacitance of the switch when desired with a certain gate current level. The current mirror concept described earlier can be used to realize such approach. An NMOS based current mirror will be used to discharge the gate of the DMOS due to the sinking direction of the output mirrored current; An NMOS / PMOS based current mirror will be used to charge the gate of the device due to the sourcing direction of the output mirrored current. Figure 2.4 depicts the circuit schematic used for simulation. The DMOS

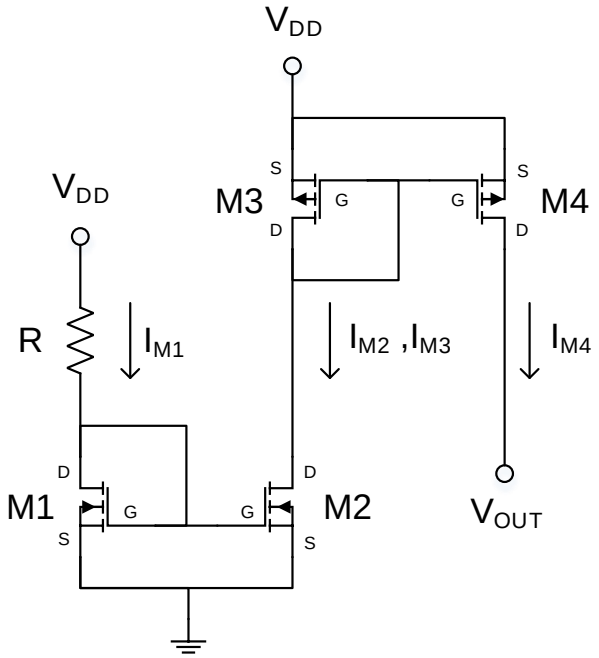

Figure 2.3: Basic configuration of a Widlar current mirror using NMOS and PMOS transistors to revert the direction of the current

is not included in the model and an ideal capacitor is used instead to emulate the capacitive behaviour of the gate. All transistors N1, N2, P1, P2, N3 and N4 are assumed to be the same size and can be implemented in Infineon's smart technology (the corresponding model will be used).

The upper current mirror will charge the capacitor at the reference charging current as long as P2 is in saturation (its source-drain voltage must have a minimum value). The pulsed voltage source is used to generate the pulsed charging current when the DMOS is to be turned on. V_{CH} will have a low and high value with a given slew rate. Its on-time will be coincident with the duty cycle of the converter times the switching period. The resistor R_{CH} will be sized based on simulation so that a current of 1 mA will go through a single transistor branch of P2. V_{DD} equals 3 V since that is the desired gate-source voltage during the on-time of the switch. The transistor P2 will actually be implemented as a number of PMOS transistors in parallel in order to obtain the desired multiplication ratio to get multiples of 1 mA. This way a variable charging current can be chosen as an input parameter for the simulation.

The lower current mirror follows the same approach. The transistor N4 will discharge the capacitor at the reference discharging current as long as it is in saturation (its drain-source voltage must have a minimum value). The pulsed voltage source V_{DCH} will be complementary to V_{CH}. Both of them will have the same high / low values as well as slew rate. R_{DCH} will be sized based on simulation to obtain a current of 1 mA through a single transistor branch of N3. The negative rail of this current mirror is 0 V since that is the desired gate-source voltage during the off-time of the switch. The transistor N4 will be a number of NMOS paralleled transistors in order to sum up the desired discharging current.

For the sake of simplicity the capacitor and both current mirrors are connected to a common ground in figure 2.4. In practice this node will not be fixed to the absolute ground since this point will be connected to the source of the DMOS transistor. This will be discussed in more depth in further sections.

Table 2.2 shows the main input parameters used to simulate the gate driver circuit that has been presented. The capacitance is initially chosen to be 1 nF to get a charging time in the same order of magnitude as that of the DMOS and to be able to size the resistors as it will be explained later. Both N and P-channel mirroring transistors are the same size for the sake of simplicity which will yield different IV curves. Therefore, in order to obtain charging and discharging currents at the output of each current mirror of 1 mA, R_{CH} and R_{DCH} will have to be sized differently.

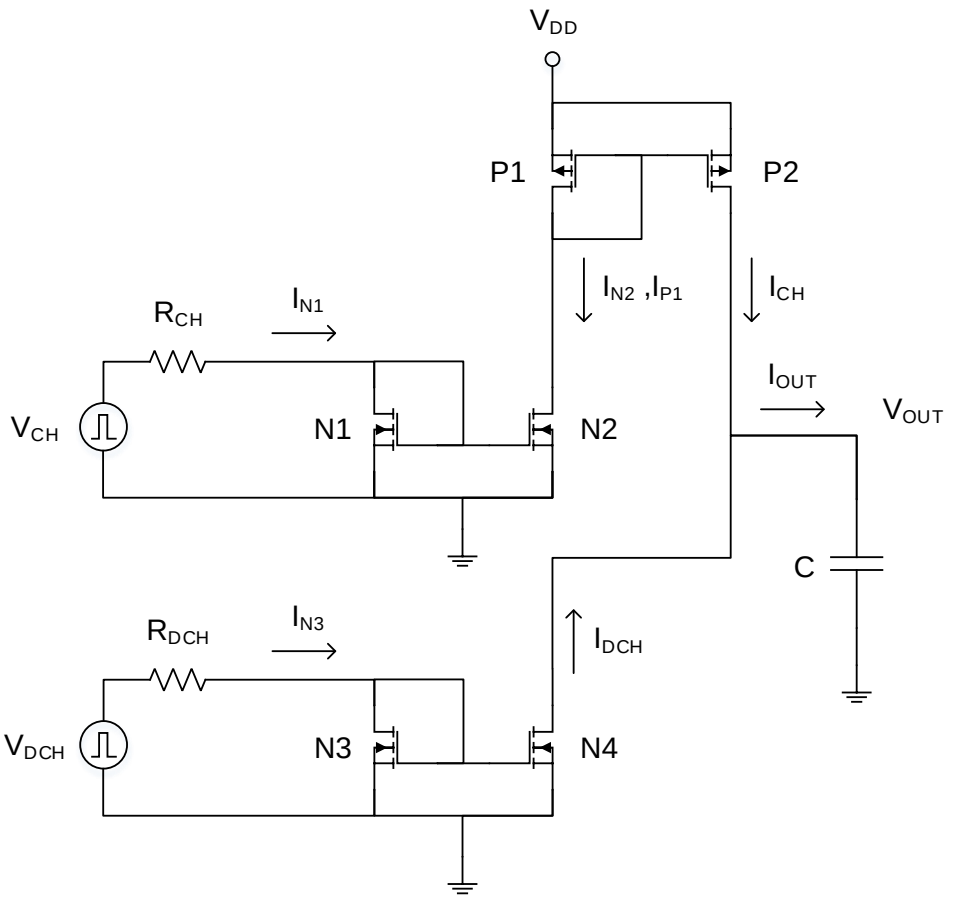

Figure 2.4: Schematic drawing of the driver concept implemented in simulation

Figure 2.5 shows how the biasing resistors has been sized in order to obtain charging and discharging currents of 1 mA at the output of the mirrors. A capacitance of 1 nF was used for this case. For the given values of R_{CH} and R_{DCH} it can be seen how the current peaks at 1 mA. From there onwards, the current decreases until reaching 0 V. This can be explained by the fact that the output transistors (P2 and N4) are in deep saturation at the beginning of the charging and discharging event respectively. As long as current is delivered to the capacitor the voltage varies. This causes the output transistors to progressively go from the saturation region to the ohmic part of the VI curve. As explained before, the current mirror does not behave as an ideal current source if channel width modulation is taken into account. Having a look at the differences between P1 and P2, it can be concluded that the main error is due to the fact that each transistor has a different drain-source voltage. As for N1 with respect to N2 the same applies. However, the difference here is much smaller since both devices are polarized at VI points very close to each other. The same applies to the currents through N3 and N4.

Once the resistors are sized to deliver a peak current of 1 mA for a single branch, the paralleling of transistors at the output can be done to realize larger currents. Figure 2.6 depicts this approach. A capacitance of 100 nF was used for this case in order to limit the voltage slopes so that the output transistors are initially deep into saturation for a minimum amount of time. The same phenomena as described before apply. The output current during charging and discharging peaks at a value of approximately 100 mA. After this a decrease of current takes place due to the output transistors leaving the saturation region. Transistors N1, N2, P1 and N3 carry the same amount of current as for the single output branch case shown earlier.

The approach followed in this section is very versatile to obtain different current levels without having to modify the circuit configuration and is valid to roughly determine how different current levels affect the driving of the DMOS. However, the practical implementation of the driver at an integrated-circuit level would be slightly different. Figure 2.7 depicts a possible way of implementing a practical gate

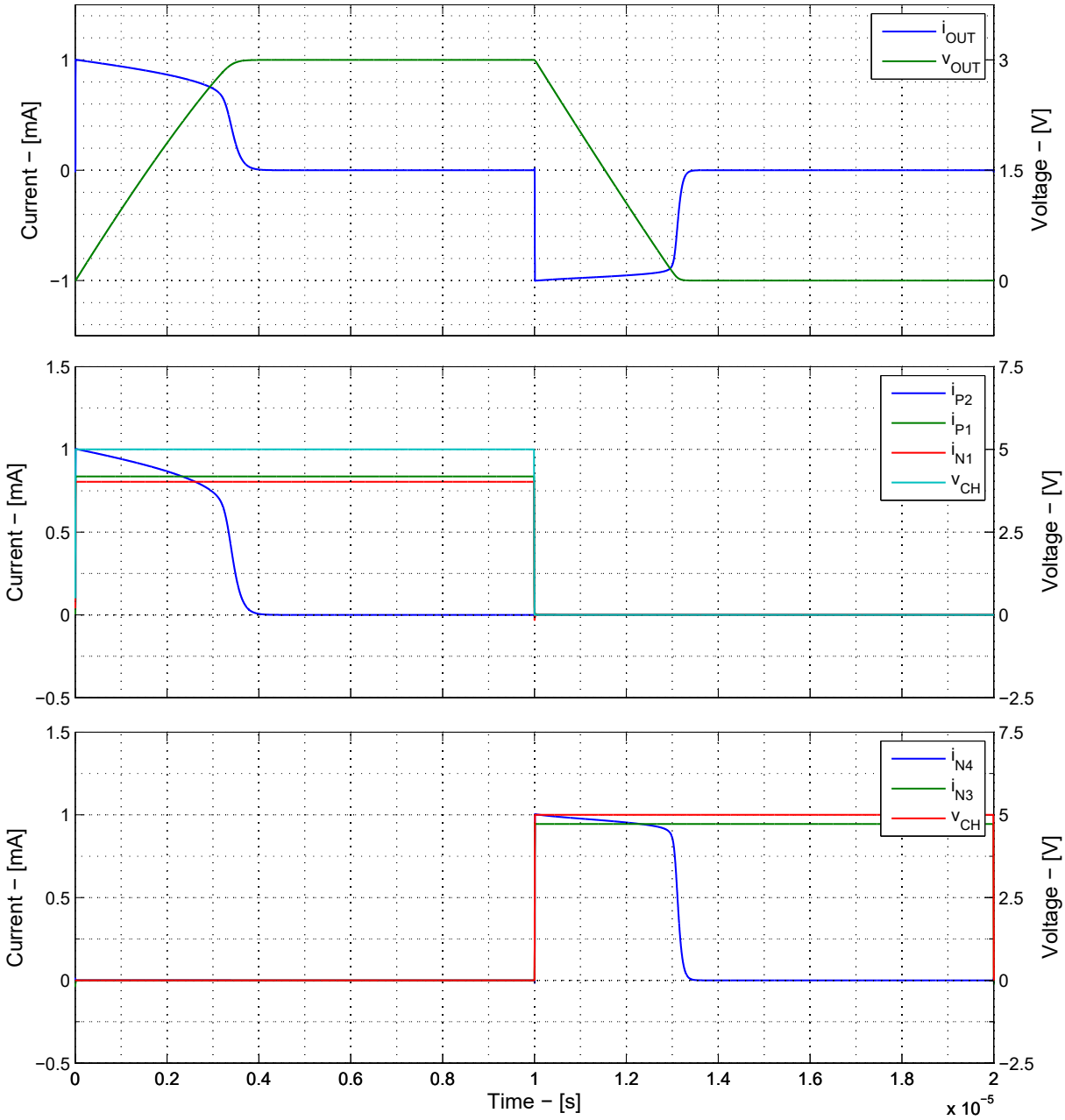

Figure 2.5: Waveforms obtained when simulating a single output branch of the gate driver concept described in this section

driver. The voltage level above battery is obtained by making use of boostrap capacitor and diode. D_{BS} charges C_{BS} from the main power supply during the off-time. When the power transistor is to be turned on, the source voltage goes above the input voltage level provided the design works as expected and the diode blocks the reverse current flow from capacitor to input voltage. This approach is very simple and cost-effective but has some limitations related to the maximum duty cycle that the converter can operate at [19]. The gate driver circuit could consist of two main subcircuits: a current source based on current mirrors, similar to the concept presented in this chapter but with fewer transistors since the silicon area would have to be taken into account; and single switches connecting the gate of the DMOS to either the positive or negative rails of the gate driver circuit. The former would provide a base charging / discharging current to the DMOS which would guarantee reaching the desired gate-source voltages during on and off states. The latter would provide an initial drive to the DMOS so that an initial peak current would bring the gate-source voltage to the threshold level much faster.

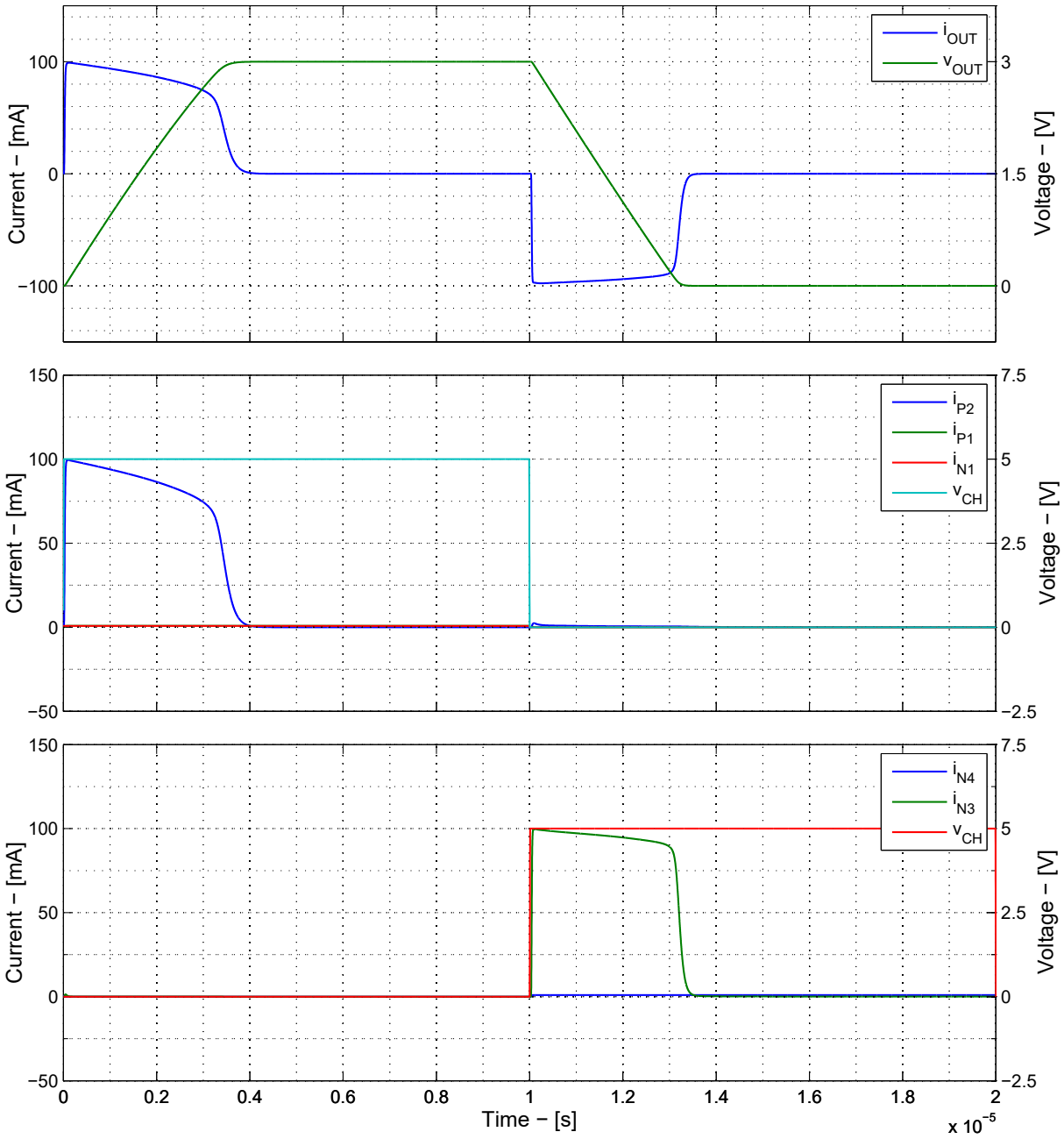

Figure 2.6: Waveforms obtained when simulating 100 parallel branches of the gate driver concept described in this section

2.3. Modelling and simulating the system

Figure 2.8 depicts the circuit that has been used for simulations. The driver will be implemented with the current-mirror concept described in the previous section. A constant input voltage is connected to the drain of the DMOS, placed at the high-side of the switching leg. A diode is used at the low side. An LC output filter connects the middle point of the switching leg to the output. The load is modelled as a resistive element. When the DMOS' gate is charged by the driver, the device will turn on. During this phase the inductor is connected to the input voltage at its positive terminal and to the output voltage at its negative terminal. The output voltage is assumed constant, given a large enough capacitor is used for the output filter. Since the buck converter steps down the input voltage, the voltage through the inductor will be positive and constant. Therefore, the current will increase linearly at a rate given by the voltage difference. When the DMOS is to be turned off, the gate driver will discharge the gate

Parameter	Value	Description
C	1, 100 nF	Capacitor to emulate the input capacitance of the power switch
SR	10 ns	Slew rate for the pulsed voltage supplies
V_{HIGH}	5 V	High-level voltage of the pulsed voltage supplies
V_{LOW}	0 V	Low-level voltage of the pulsed voltage supplies
R_{CH}	5.3 kΩ	Biasing resistor for the charging current
R_{DCH}	4.5 kΩ	Biasing resistor for the discharging current
V_{DD}	3 V	Upper rail voltage for the current mirror circuit
w_T	500 µm	Total width of the mirroring transistors
l_T	500 nm	Gate length of the mirroring transistors

Table 2.2: Simulation parameters for the gate driver circuit

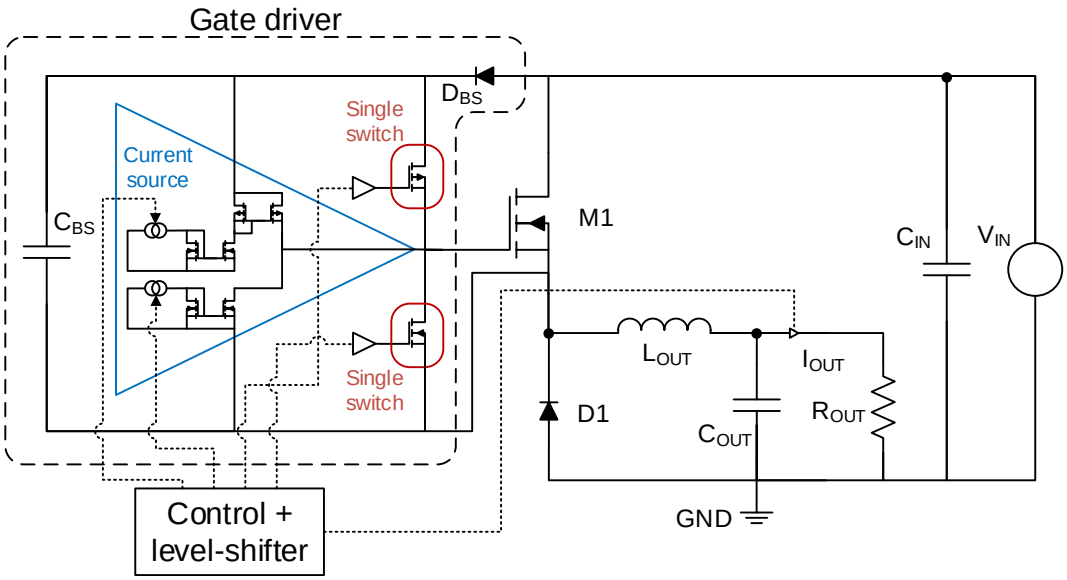

Figure 2.7: Concept diagram of a practical implementation of the gate driver on an integrated-circuit level

of the device. Once this happens, the low-side diode will freewheel the current of the coil. The positive terminal of the inductor will be connected to a slightly negative voltage (equal to the voltage drop of the diode), while the negative terminal will be connected to the output voltage. Therefore, a negative and constant inductor voltage will make the current decrease linearly.

Figure 2.9 shows some of the most relevant steady-state waveforms obtained when simulating the described circuit. The circuit parameters used for this case can be seen in table 2.3. When a positive gate current is applied to the switch, the gate-source voltage rises. An initial slope is observed at V_{GS} until certain value is reached. The rise in V_{GS} is determined by the charging of C_{GS} and C_{GD}. During this time V_{DS} can be assumed constant and therefore C_{GS} and C_{GD} toos (they are V_{DS} dependent). At this time C_{GS} is larger than C_{GD} and most of the gate current flows into the former. Once the threshold voltage is reached the so-called Miller Plateau commences and the switch carries the coil current. The slope of V_{GS} is almost zero during this phase because most of the current flows into C_{GD}. During this time V_{DS} changes rapidly and C_{GD} becomes larger and larger. When the plateau is finished C_{GD} becomes constant again. The slope of V_{GS} is lower compared to its value before reaching the threshold voltage because C_{GD} is much larger than before and comparable to the value of C_{GS} [20]. A similar behaviour can be observed during turning-off of the device. The gate current does not reach the 100 mA maximum value but it is very close. The current source can be assumed to be operating as expected.

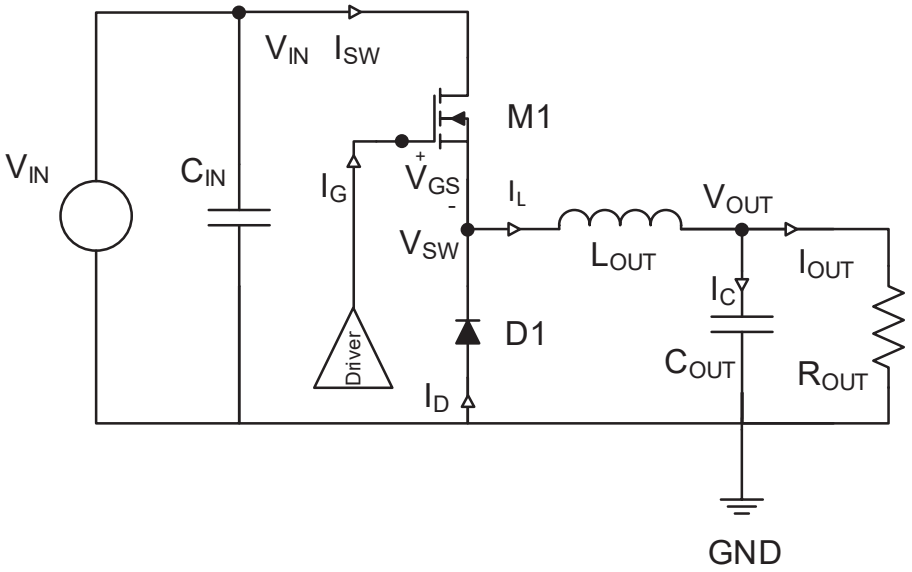

Figure 2.8: Circuit implemented in simulation to analyze the behavior of the system

It can be noticed how the switching node voltage does not present a duty cycle equal to that given by the control signal. This deviation is due to the asymmetric finite transition times of the DMOS. The switch and diode currents equal that through the inductor. The average values of the coil and output current can be observed to be equal in steady-state. Therefore, the capacitor carries the inductor ripple current, which has a triangular shape. The output voltage ripple will be proportional to the time integral of this current.

Parameter	Value	Description
f_{SW}	200 kHz	Switching frequency
D_{cont}	0.5	Control duty cycle
V_{IN}	20 V	Input voltage
$I_{G,max}$	100 mA	Gate current level
L_{OUT}	47 µH	Output filter inductor
C_{OUT}	20 µF	Output filter capacitor
R_{OUT}	6 Ω	Output resistor

Table 2.3: Parameters used to simulate the system and obtain the waveforms shown in figure 2.9

2.4. Simulation results

Once the gate driver has been introduced and explained, the main conclusions and results of the simulation will be presented in this section. The driver has been simulated for different gate current levels by setting the number of paralleled branches at the output of the current mirrors. This way the effective current delivered to the DMOS can be varied accordingly. Figure 2.10 shows how the different observed switching times have been defined. As it has been mentioned before, there will be a finite time needed to bring the gate-source voltage from its off value to the threshold level ($t_{DEL,ON}$). After this time the slope of the coil current will change from negative to positive, that is, the DMOS will start to carry the whole inductor current. The time needed to bring the gate-source voltage from off to on value is $t_{FULL,ON}$. The same applies to the switching-off times: $t_{DEL,OFF}$ is the time needed to go from V_{GS} during on state to the threshold value (and the time from which the coil current slope will become

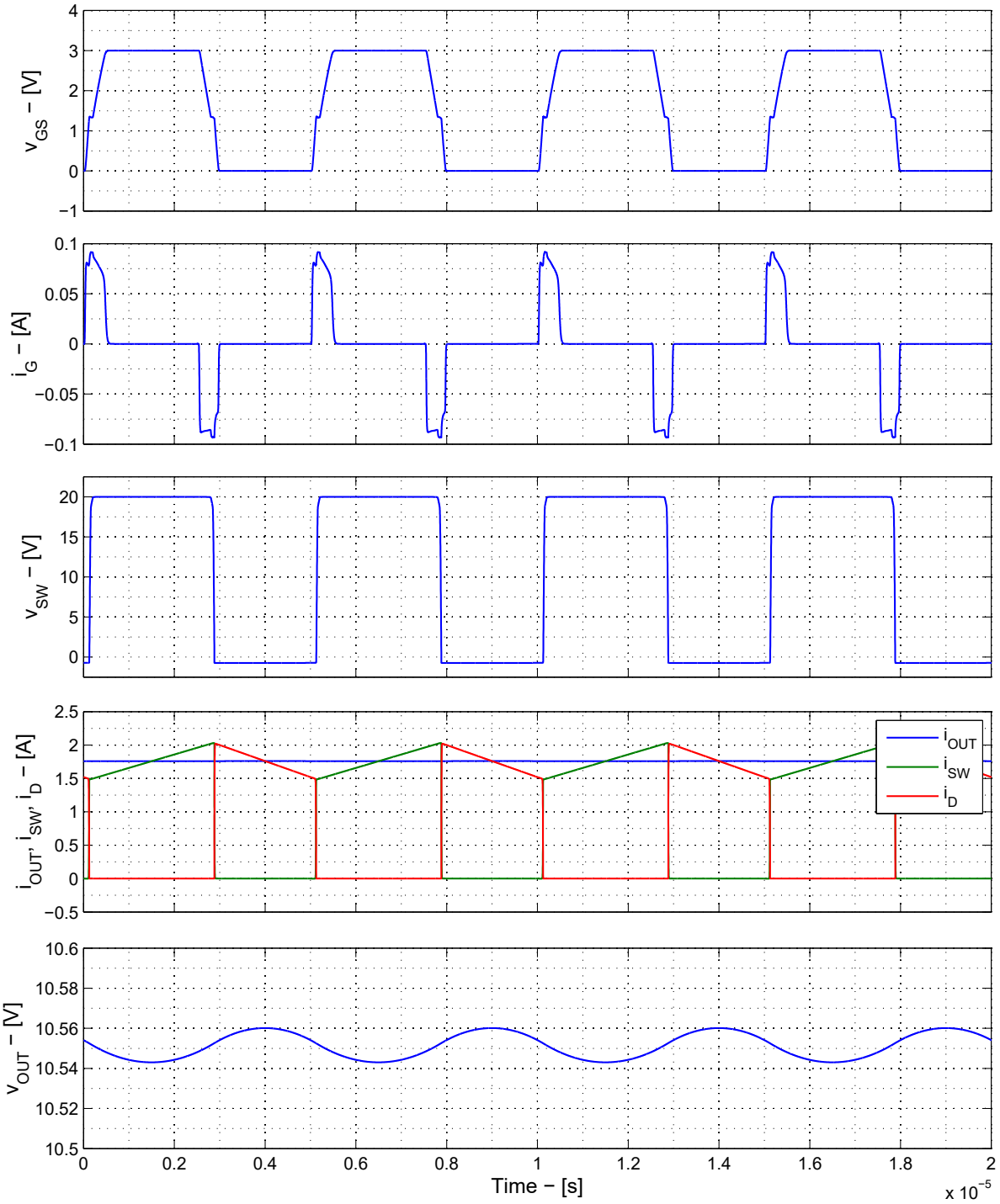

Figure 2.9: Waveforms obtained when simulating the system using the parameters shown in table 2.3

negative); $t_{FULL,OFF}$ is the time needed to fully bring the gate-source voltage to the off value. $t_{FULL,ON}$ and $t_{FULL,OFF}$ should be equal given the current source operated identically during both transistions. However, as it will be shown later on, this is not the case since the gate current during turn-on and off differ slightly from each other. It can also be noticed how the actual duty cycle, that is, the portion of the switching period during which the coil current has a positive slope, is different to the control duty cycle (the signal sent to the gate driver). This is due to the asymmetric finite transition times. For a given switching frequency f_{SW} it can be written:

$$D_{cont}^{min} = t_{FULL,ON} \times f_{SW} \tag{2.7}$$

$$D_{cont}^{max} = 1 - t_{FULL,OFF} \times f_{SW} \tag{2.8}$$

$$D_{act}^{min} = (t_{FULL,ON} - t_{DEL,ON} + t_{DEL,OFF}) \times f_{SW} \tag{2.9}$$

$$D_{act}^{max} = 1 - (t_{DEL,ON} + t_{FULL,OFF} + t_{DEL,OFF}) \times f_{SW} \tag{2.10}$$

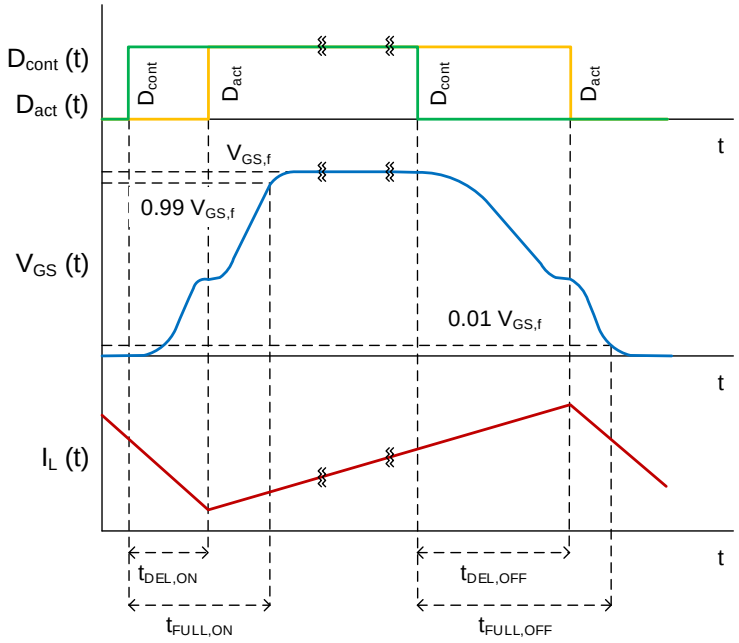

Figure 2.10: Definition of the switching times considered for the simulation of different gate current levels

The larger the current supplied to the gate of the DMOS, the faster the transition will be and therefore the switching times will be smaller. This effect can be observed in figure 2.11. The left part of the plot relates to small gate current levels. It can bee seen how the switching times decrease linearly in logarithmic scale with the current. The current source is behaving like an ideal current source and as expected the more current is supplied to the gate, the faster its voltage varies. As for the maximum switching frequency, it is defined as the frequency at which the total switching time would equal the transition times. This is not a realistic value since the duty cycle could not be changed at this time rate, but it gives an overview of how switching frequency relates to the gate current level. If the current keeps increasing, it can be seen how the logarithmic curves are not linear anymore. This means that paralleling more transistors at the output to keep increasing the current does not have the desired effect. For these points the output transistors leave saturation before the DMOS is fully on / off and therefore the current delivered is not proportional to the number of parallel branches anymore. Also, the gate current of the mirror switches will not be negligible anymore since the amount of transistors used is relatively large. In fact, it can be observed how an increase in the number of parallel branches does not bring a decrease in switching times for large values of current.

For that reason, a current level of 100 mA will be chosen as the nominal value for further investigations. This value represents a good trade-off between complexity of implementation and performance. Larger values of current could fasten the transisitions but as it has been shown they could also have a negative effect on the switching speed; smaller values would be easier to realize in practice but the performance would be improvable. The maximum switching frequency allowable for a gate current level of 100 mA is in the order of 1 MHz as shown in figure 2.11. Also, it can be noticed how $t_{DEL,ON}$ is considerable smaller than $t_{DEL,OFF}$. This will introduce a deviation between control and actual duty cycle of the converter.

Another important result obtained from simulation is the gate charge required by the DMOS to bring its voltage from 0 to 3 V and vice versa. This value is obtained by integrating the gate current during the transition times and it equals 35.9 nC for all gate current level configurations. As expected, the integration of the gate current equals this value for both charging and discharging of the gate. This is a very important value to make first-order approximations about the current required by the device to

effectively switch. Assuming an equivalent gate capacitance and a constant gate current during the transition, the switching times could be estimated as:

$$t_{trans} = \frac{C \times \Delta V}{I_G} \tag{2.11}$$

As a summary, figure 2.12 depicts how the duty cycle relates to both switching frequency and gate current level. As expected, increasing the gate current will broaden the duty cycle range for a given switching frequency. On the other hand, increasing the switching frequency for a given gate current level will shorten the duty cycle range due to the shrinking of the switching period. The relationship between duty cycle, current level and switching frequency can be also explained from a numerical point of view. Duty cycle ranges for a gate current level of 100 mA are shown in table 2.4. The same relationships as described before can be observed. The control and actual duty cycle differ from each other due to the asymmetric switching times, namely $t_{DEL,ON}$ and $t_{DEL,OFF}$. It can be seen also how this difference increases with the switching frequency.

2.5. Switch power losses

Once the limitations of the system regarding switching frequency, gate current and duty cycle have been presented and analyzed the next step is to determine the power losses in the DMOS. These are:

- Conduction losses, due to the finite resistance of the DMOS' channel. Such resistance will be primarily a function of the gate-source voltage (it is also very temperature dependent) and can be approximated as the slope of the VI curve of the device in linear or ohmic region.
- Turn-on losses, due to both current and voltage not being negligible during the transition from off to on state. The output load connected to the switching leg is highly inductive and therefore

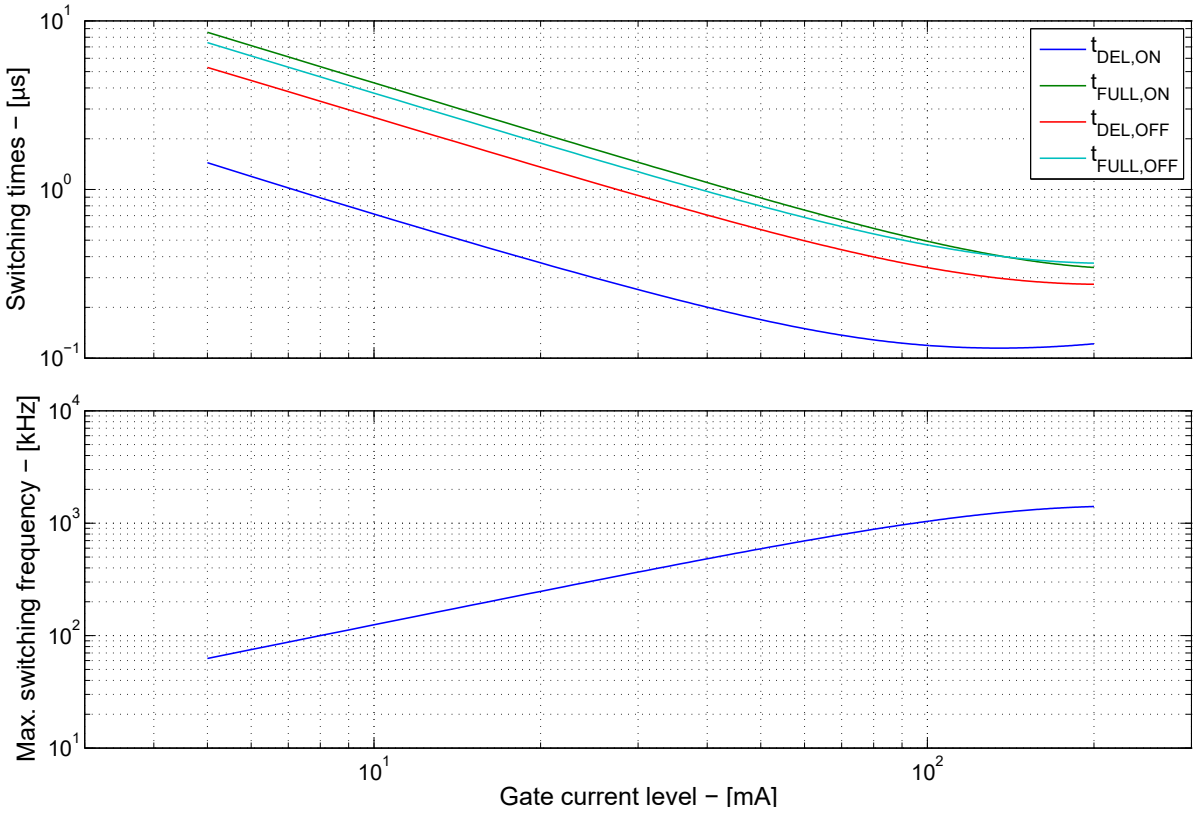

Figure 2.11: Switching times and maximum switching frequency for different values of gate current

f_{SW}	D_{cont}^{min}	D_{act}^{min}	D_{cont}^{max}	D_{act}^{max}
100 kHz	4.93 %	7.19 %	95.31 %	97.56 %
200 kHz	9.86 %	14.37 %	90.61 %	95.12 %
300 kHz	14.80 %	21.56 %	85.92 %	92.69 %
400 kHz	19.73 %	28.75 %	81.23 %	90.25 %
500 kHz	24.66 %	35.93 %	76.54 %	87.81 %
600 kHz	29.59 %	43.12 %	71.84 %	85.37 %
700 kHz	34.52 %	50.31 %	67.15 %	82.93 %
800 kHz	39.46 %	57.50 %	62.46 %	80.50 %
900 kHz	44.39 %	64.68 %	57.76 %	78.06 %
1 MHz	49.32 %	71.87 %	53.07 %	75.62 %

Table 2.4: Duty cycle ranges (control and actual) for a gate current level of 100 mA

the current through the high-side switch must increase until its final value before bringing the switching node voltage down to almost zero.

- Turn-off losses, due to both current and voltage not being negligible during the transition from on to off state. The inductive nature of the load will force the voltage across the high-side switch to build up before it lets the low-side device take over the whole current.

The switch power losses have been computed directly from the simulation waveforms in steady-state according to the following:

$$P_{SW}(t) = i_{SW}(t) \times v_{DS}(t) \tag{2.12}$$

$$P_{SW}^{avg} = \frac{1}{T_{SW}} \int_{t}^{t+T_{SW}} P_{SW}(t)\, dt = \frac{1}{T_{SW}} \int_{t}^{t+T_{SW}} i_{SW}(t) \times v_{DS}(t)\, dt \tag{2.13}$$

The whole switching period in steady state can be split into two main parts: the on-time and the off-time. The former period is the most relevant as for the DMOS losses. Within this interval, the switch will perform the turn-on action (during which the turn-on losses will take place), stay on for the amount of time commanded by the control (during which the conduction losses will take place), and perform the turn-off action (during which the turn-off losses will take place). The integration of the power dissipated in the switch will automatically account for all these loss mechanisms. Let us assume for the sake of

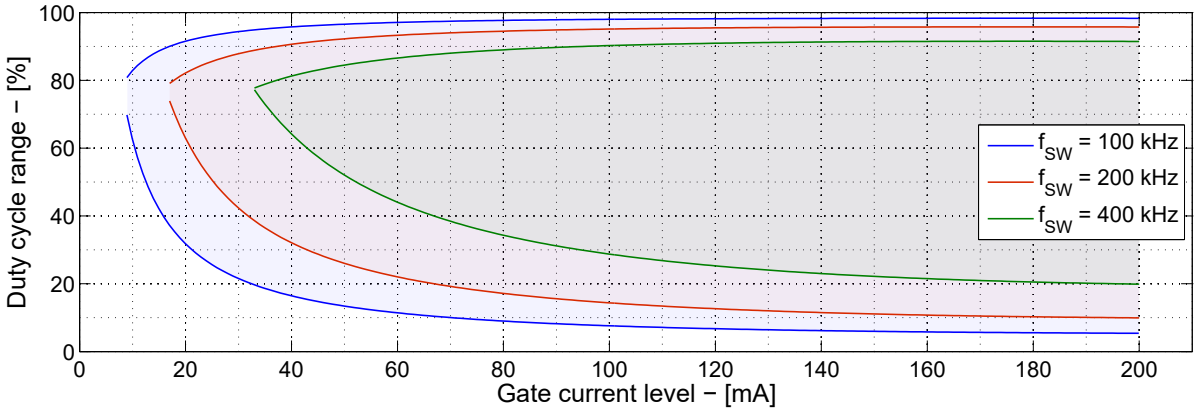

Figure 2.12: Duty cycle ranges for different values of switching frequency and gate current

simplicity that $t = 0$ happens at the start of the switching period with the command signal given by the control. Then, the different switch losses could be split as follows:

$$P_{turn-on}^{avg} = \frac{1}{t_{FULL,ON}} \int_{0}^{t_{FULL,ON}} i_{SW}(t) \times v_{DS}(t)\, dt \tag{2.14}$$

$$P_{cond}^{avg} = \frac{1}{T_{SW} - t_{FULL,ON} - t_{FULL,OFF}} \int_{t_{FULL,ON}}^{T_{SW}-t_{FULL,OFF}} i_{SW}(t) \times v_{DS}(t)\, dt \tag{2.15}$$

$$P_{turn-off}^{avg} = \frac{1}{t_{FULL,OFF}} \int_{T_{SW}-t_{FULL,OFF}}^{t_{SW}} i_{SW}(t) \times v_{DS}(t)\, dt \tag{2.16}$$

$$P_{SW}^{avg} = P_{turn-on}^{avg} + P_{cond}^{avg} + P_{turn-off}^{avg} \tag{2.17}$$

The times during which the dynamic switch losses have been defined (turn-on and turn-off losses) is somehow arbitrary and it has been chosen this way to be consistent with the previously defined switching times. The splitting up of the DMOS' losses into different terms is just presented to provide the reader with a better insight on the loss sources. However, they do not affect the total computed losses that will be shown in this section. Figure 2.13 shows the waveforms obtained in simulation to give an overview about the dynamic switching losses. The inductive character of the load can be observed during both turn-on and turn-off. As for the former, the current through the switch must build up before the voltage can decrease. This creates a peak at the power dissipated in the switch whose value is approximately equal to the voltage times the current that are being switched. Similar transitions can be observed during turn-off. It can be concluded therefore that the dynamic power losses (more specifically the dynamic switching energy) will be mostly dependent on the current and voltage that the DMOS has to operate with.

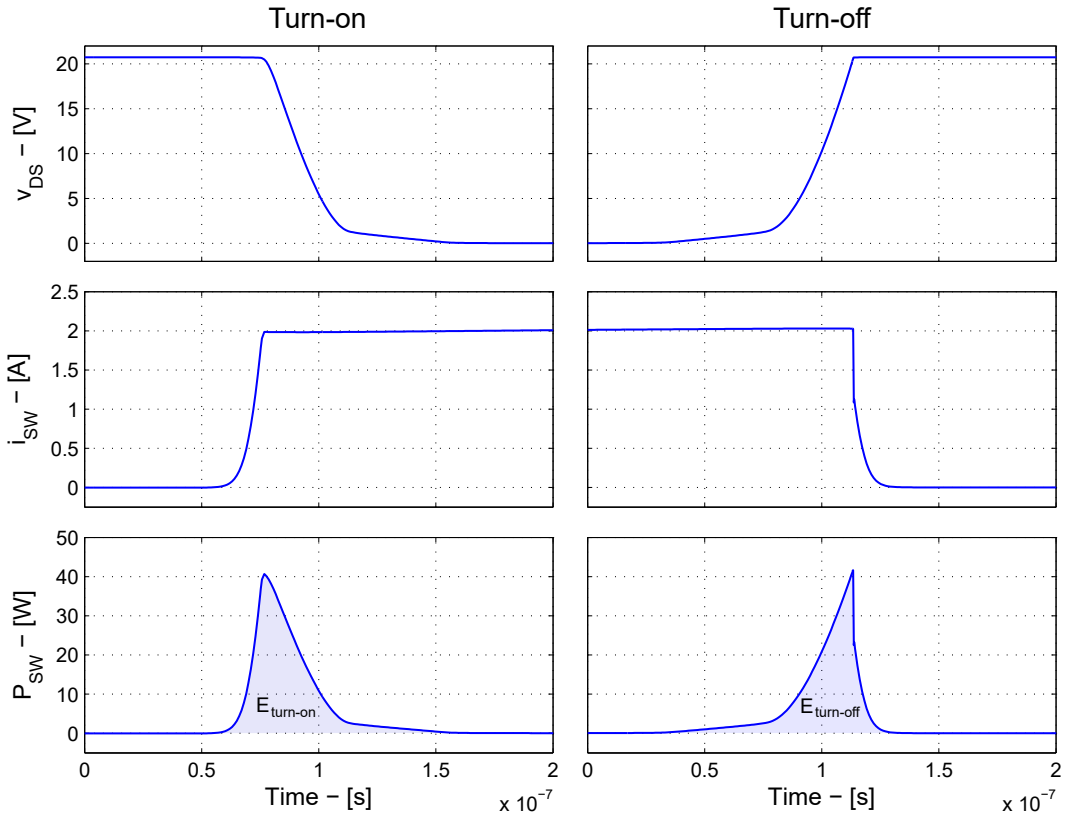

Figure 2.13: DMOS' current, voltage and power during turn-on (left) and turn-off (right) of the device

Table 2.5 presents the parameter values used to simulate the system according to figure 2.8. It must be noted that all values shown in this section are related to the steady-state operation of the converter.

The computed losses for a gate current level of 100 mA and different values of switching frequency with respect to the average output current are shown in figure 2.14. The quantities presented include the three loss mechanisms described earlier in this section. As it can be seen, the width of the curves decreases with the switching frequency. This is due to taking into account the finite switching times: the shorter the switching period, the more dominant these transition times will be. Accordingly, the operating range of the converter will be reduced. Also, as expected, the power losses increase with both current and switching frequency of the converter. The former is caused on the one hand by an increase in conduction losses. As more current is carried by the switch, conduction losses become larger. The switch acts as a resistive element that creates power dissipation proportional to the square of rms current through the device. On the other hand, increasing the current also has an influence on the dynamic losses: if the DMOS has to switch a higher current value, the energy dissipated at the transitions will be consequently larger. On top of this, the effect of the switching frequency on the switch's power losses can be explained by having a look at the energy terms:

$$E_{turn-on} = \int_0^{t_{FULL,ON}} i_{SW}(t) \times v_{DS}(t)\, dt \tag{2.18}$$

$$E_{turn-off} = \int_{T_{SW}-t_{FULL,OFF}}^{t_{SW}} i_{SW}(t) \times v_{DS}(t)\, dt \tag{2.19}$$

The energy dissipated during these transitions is somehow fixed for certain current and voltage levels given that enough time is ensured from the control stage to complete the full swinging of voltage and current. The amount of transitions per unit of time will indicate how much power is dissipated in the device:

$$P_{turn-on}^{avg} = \frac{1}{t_{FULL,ON}} \int_0^{t_{FULL,ON}} i_{SW}(t) \times v_{DS}(t)\, dt = E_{turn-on} \times f_{SW} \tag{2.20}$$

$$P_{turn-off}^{avg} = \frac{1}{t_{FULL,OFF}} \int_{T_{SW}-t_{FULL,OFF}}^{t_{SW}} i_{SW}(t) \times v_{DS}(t)\, dt = E_{turn-off} \times f_{SW} \tag{2.21}$$

That is, the dynamic power losses are proportional to the switching frequency of the converter while the energy dissipated is a function of the transition time, voltage and current of the DMOS. This can be observed in figure 2.14. Also, it is important to note that the majority of the losses come from the dynamic switching term. It can be seen how increasing the switching frequency twofold results in almost doubling the power losses. In other words, the dynamic losses are much more dominant than the conduction losses for the DMOS in question.

Parameter	Value	Description
V_{IN}	20 V	Input voltage
$I_{G,max}$	100 mA	Gate current level
L_{OUT}	47 µH	Output filter inductor
C_{OUT}	20 µF	Output filter capacitor
R_{OUT}	10 Ω	Output resistor

Table 2.5: Parameters used to simulate the system and compute the DMOS' power losses shown in figure 2.14

2.6. Converter efficiency limit given by power switch

Once the the losses in the switch are computed, their effect on the overall efficiency of the converter can be evaluated. This will give an idea or first approximation about how efficient the system can be as for the switch. In practice, the efficiency values will be lower than this estimation due to loss mechanisms present in other elements of the converter. However, this approach will give an upper limit on how efficient the solution can be. Figure 2.15 shows the values of the so-defined switch efficiency limit for

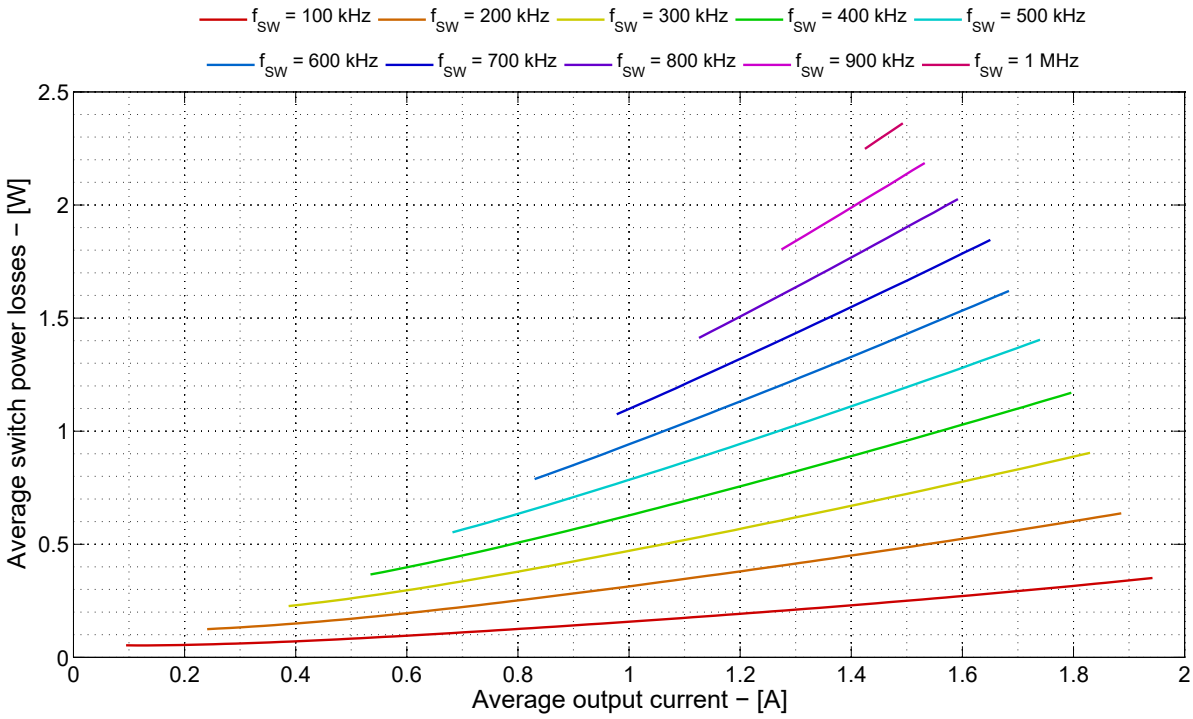

Figure 2.14: Total switch power losses for a gate current level of 100 mA and different switching frequencies with respect to average output current using the parameters given in table 2.5

a gate current level of 100 mA and different switching frequencies with respect to the average output current. Since only the DMOS' losses are taken into account so far:

$$P_{IN}^{avg} = \frac{1}{T_{SW}} \int_{t}^{t+T_{SW}} i_{IN}(t) \times v_{IN}(t)\, dt \tag{2.22}$$

$$P_{OUT}^{avg} = \frac{1}{T_{SW}} \int_{t}^{t+T_{SW}} i_{OUT}(t) \times v_{OUT}(t)\, dt \tag{2.23}$$

$$\eta[\%] = \frac{P_{OUT}^{avg}}{P_{IN}^{avg}} \times 100\% = \frac{P_{IN}^{avg} - P_{loss}^{avg}}{P_{IN}^{avg}} \times 100\% = \frac{P_{IN}^{avg} - P_{SW}^{avg}}{P_{IN}^{avg}} \times 100\% = \left(1 - \frac{P_{SW}^{avg}}{P_{IN}^{avg}}\right) \times 100\% \tag{2.24}$$

Again, the shrinking of the converter operating range due to the finite transition times becoming more and more dominant can be observed. Only values for which the total switching time is equal or smaller than the switching period are plotted. As expected, the efficiency drops with an increase in the switching frequency. This is mostly due to the dependence of the dynamic losses on the converter operating frequency. It could be concluded from here that increasing the switching frequency is not justified. However, the passives that would have to be used to satisfy certain sets of requirements such as ripple could be sized smaller. Not only would this have a huge impact on the size of the solution but also on its cost.

Having a look at the profile of the curves, it can be seen how the efficiency drops considerably for low-power points. On the contrary, the computed efficiency limit reaches values close to the maximum for high-current points. What is more, the curves still show a positive slope in this range. According to this tendency, increasing the current would yield even higher efficiency. This could be explained by the fact that the conduction losses are much smaller than the dynamic ones. The dependence on current of the former losses is quadratic while linear for the latter. In the low-power range (approximately up to 500 mA), the conduction losses are extremely small (a very small current value squared is even smaller) and the dynamic loss mechanism accounts for most of the dissipated energy; in the high-power range (approximately from 500 mA onward) the dynamic losses are still dominant with respect to conduction losses as it have been inferred from figure 2.14. If conduction losses were higher, the quadratic dependence on current would have an impact of the efficiency limit in the high-power range.

2.7. Conclusions and remarks

This section puts together all the conclusions drawn from the simulation-based feasibility study described in chapter 2. These will be relevant to the reader in order to understand the work presented further in the report. The main conclusions are:

- A gate current level of 100 mA is a good trade-off between viability of implementation and obtained performance. It has been shown how a smaller value would yield longer switching transitions times and how going above 100 mA is not really justified since it does not bring a big improvement as for switching speed. This value will be then adopted for further investigations and analysis.
- The maximum switching frequency that can be achieved is a function of the gate current level supplied to the DMOS. The main limitation comes from the fact that transitioning between on and off states (and vice versa) takes a finite amount of time. This will introduce an upper limit in the feasible switching frequency of the device.
- The duty cycle range that the converter can operate at is a function of the finite switching times and therefore depends on the gate current level. If the system is to operate for a given range, then a certain level of gate current has to be supplied to the switch.
- The finite and asymmetric switching times required to turn on and off the DMOS introduce a deviation between the duty cycle given by the control and the actual value that is applied to the output filter of the converter. The higher the switching frequency, the larger this deviation will be.
- The calculation of the power losses in the switch brings up another limitation related to the maximum allowable switching frequency that the device can operate at. As a rough first approximation, the packaging of the DMOS test-chip and the device itself can dissipate a maximum power in the order of 3 W. According to figure 2.14, a maximum switching frequency of 800 kHz would be admissible for a gate current level of 100 mA.
- As it can be observed in figure 2.14 the dynamic losses account for most of the energy dissipated in the DMOS. The conduction losses are therefore much smaller for the device analyzed in this work.

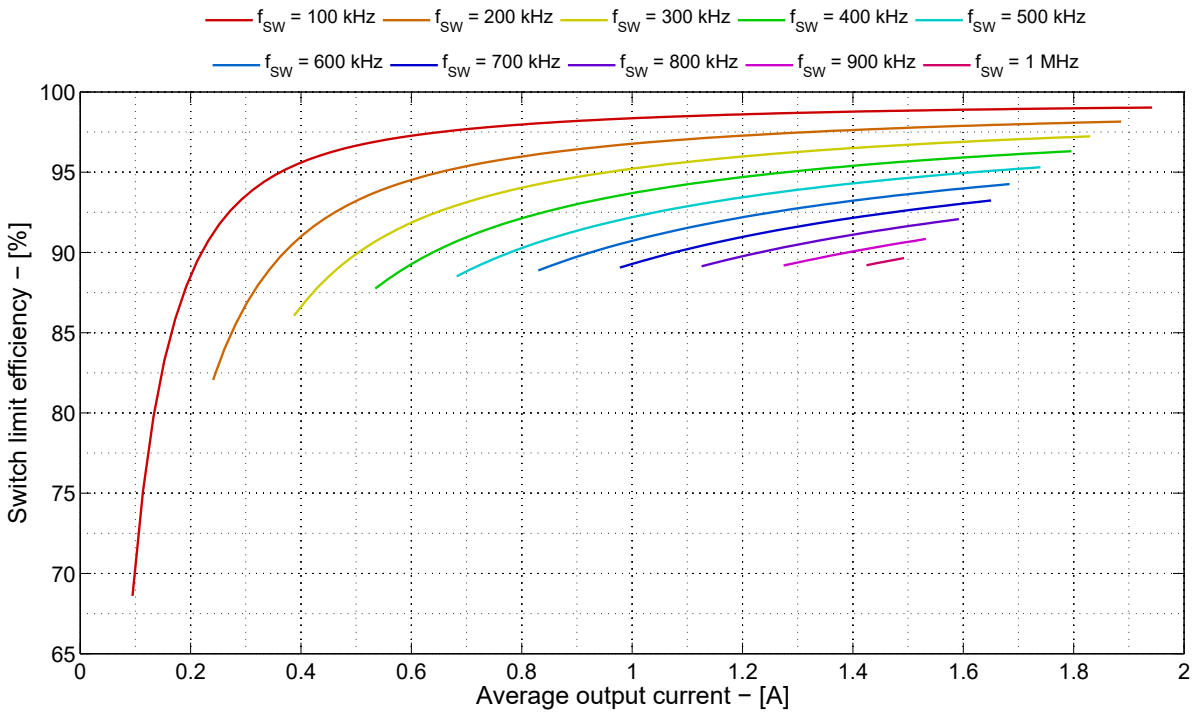

Figure 2.15: Efficiency limit given by the DMOS for a gate current level of 100 mA and different switching frequencies with respect to average output current using the parameters given in table 2.5

The simulation study carried out and presented in this chapter must be taken as a first approximation to the device's limitations. In practice, for instance, there will be parasitic elements that have not been considered in simulation. The packaging itself and the hardware implementation of the converter will introduce stray inductance and capacitance. The total amount and the effect of these on the performance of the system will depend on how robust the design is.

The switching times observed in a practical application will be larger than those observed in simulation. The change at which current and voltage can vary will be affected by parasitic inductance and capacitance respectively. It is therefore critical to optimize the design in order to obtain consistent practical values that can validate the simulation results. In practice the switching will be slower due to presence of parasitic.

The efficiency limit given in this chapter is assumed to be an upper limit to the ultimate efficiency of the converter. For example, the slower switching times obtained in practice due to parasitic elements will yield larger switching losses that will make the efficiency drop. On top of this, other lossy elements of the converter will significantly increase the total losses of the system. These aspects will be presented and analyzed in the coming chapters of this report.

Lastly, it is important to remark the effect that the weight of the different power losses in the DMOS can have on the efficiency curve. As stated before, the dynamic losses are much larger than the conduction losses for the test-chip analyzed in this thesis work. However, the shape of the switch losses could be significantly different if other device configurations were adopted. This topic is addressed in more depth in the document's section where future work is presented.

3

Loss modeling and converter dimensioning

The third chapter of this document focuses on the analysis and modeling of the converter losses. Section 3.1 is aimed to serve as an introduction to all the work carried out along the chapter. The converter waveforms in steady state will be presented and the most representative expressions will be derived here. The following sections explain the different loss mechanisms in more detail and provide the reader with a means of modeling them: section 3.2 focuses on the power switch losses; section 3.3 elaborates on the diode losses; section 3.4 explains how the coil losses are analyzed and modeled; and section 3.5 expands on the capacitor losses. Once the different loss sources have been presented from a theoretical point of view, section 3.6 discusses how the practical elements of the converter can be selected and sized based on a set of criteria. Sections 3.7 introduces the overall loss model to give an estimation of the converter efficiency based on results from previous sections. Lastly, the conclusions of this chapter are presented in section 3.8.

3.1. Steady-state operation

The first step to build a loss model of the system consists in finding the expressions that define the operation of the converter. It will be assumed that the converter is operating in steady state with a given switching frequency. Therefore the waveforms and operation repeat every switching period assuming that the system is disturbance-free. A series of assumptions will be made in order to simplify the analysis and derivation of the converter expressions:

- Only continuous conduction mode is considered. The operation of the converter can be categorized into two different modes: continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The difference lies in the nature of the coil current: for CCM, the coil current is always positive and therefore the inductor never stops conducting; on the other hand, DCM is entered when the coil current reaches zero and cannot reverse due to the blocking properties of the low-side diode (it is therefore clamped to zero until the start of the next switching period). This assumption is made for the sake of simplicity because the work presented is a first approximation to the possibilities that can be realized using Infineon's smart technology.
- The converter and its elements are assumed lossless except for the average voltage drops across the high-side switch and the low-side diode. In practice, other losses of the converter will have an effect on the steady-state waveforms. However, its effect will be neglected and the accuracy of the derived expressions will be assumed good enough.
- The input and output voltage ripple are assumed to be very small compared to their average value. Therefore they can be neglected to derive the cycle-average expressions. The ripple of these waveforms will be derived from an analytical point of view in the last part of this section.

- For the sake of simplicity, the control and actual duty cycles are considered equivalent here. That is, the switch's transitions between on and off states and vice versa are assumed instantaneous. This simplification will be good enough as long as the transition times are much smaller than the total switching period.

Figure 3.1 shows a simplified representation of some converter waveforms. The duty cycle transitions mark the start of the on and off periods. The coil voltage and current are very relevant waveforms to explain the operation of the converter. The former will have a positive value during the on-state (assuming $V_{IN}^{avg} > V_{OUT}^{avg}$) and will be begative during the off phase. Consequently, the slope of the current through the coil will be positive during the on-state and negative during the successive phase. If the converter is operating in steady-state the resulting waveform will have a triangular shape. The switch and diode currents will be a chopped portion of the mentioned current: the high-side device will conduct during the on-state and the low-side diode during the off-state. The output current will have a ripple proportional to that of the output voltage. It has been assumed however that this can be neglected. As it will be demonstrated later on, the current through the output capacitor will equal the AC component of the coil current. In reality, the output voltage will present some ripple due to this AC current. Its magnitude will be discussed further in this section.

Figure 3.2 presents the equivalent circuits used to derive the expressions for the converter waveforms. It can be written:

$$v_{L,ON}(t) = V_{IN}^{avg} - V_{SW,on}^{avg} - V_{OUT}^{avg} \tag{3.1}$$

$$v_{L,OFF}(t) = -V_{D,on}^{avg} - V_{OUT}^{avg} \tag{3.2}$$

That is, the coil voltage has a constant known value during both on and off-states. From the basic equation that defines the behavior of an inductive element:

$$v_L(t) = L\frac{di_L(t)}{dt} \longrightarrow i_L(t) = i_L(0) + \frac{1}{L}\int_0^t v_L(t)\,dt \tag{3.3}$$

Since steady-state operation is assumed ($i_L(0) = i_L(T_{SW})$)

$$\int_0^{T_{SW}} v_L(t)\,dt = 0 \tag{3.4}$$

The time integral of the inductor voltage within the switching period must equal zero:

$$\int_0^{D\,T_{SW}} v_{L,ON}(t)\,dt + \int_{D\,T_{SW}}^{T_{SW}} v_{L,OFF}(t)\,dt = 0 \tag{3.5}$$

$$\left(V_{IN}^{avg} - V_{SW,on}^{avg} - V_{OUT}^{avg}\right)D = \left(V_{D,on}^{avg} + V_{OUT}^{avg}\right)(1-D) \tag{3.6}$$

Which yields:

$$V_{OUT}^{avg} = \left(V_{IN}^{avg} - V_{SW,on}^{avg}\right)D - V_{D,on}^{avg}\,(1-D) \tag{3.7}$$

Since a resistor is connected to the output of the converter:

$$I_{OUT}^{avg} = \frac{V_{OUT}^{avg}}{R_{OUT}} \tag{3.8}$$

Let us also rework the basic equation of a capacitive element:

$$i_C(t) = C\frac{dv_C(t)}{dt} \longrightarrow v_C(t) = v_C(0) + \frac{1}{C}\int_0^t i_C(t)\,dt \tag{3.9}$$

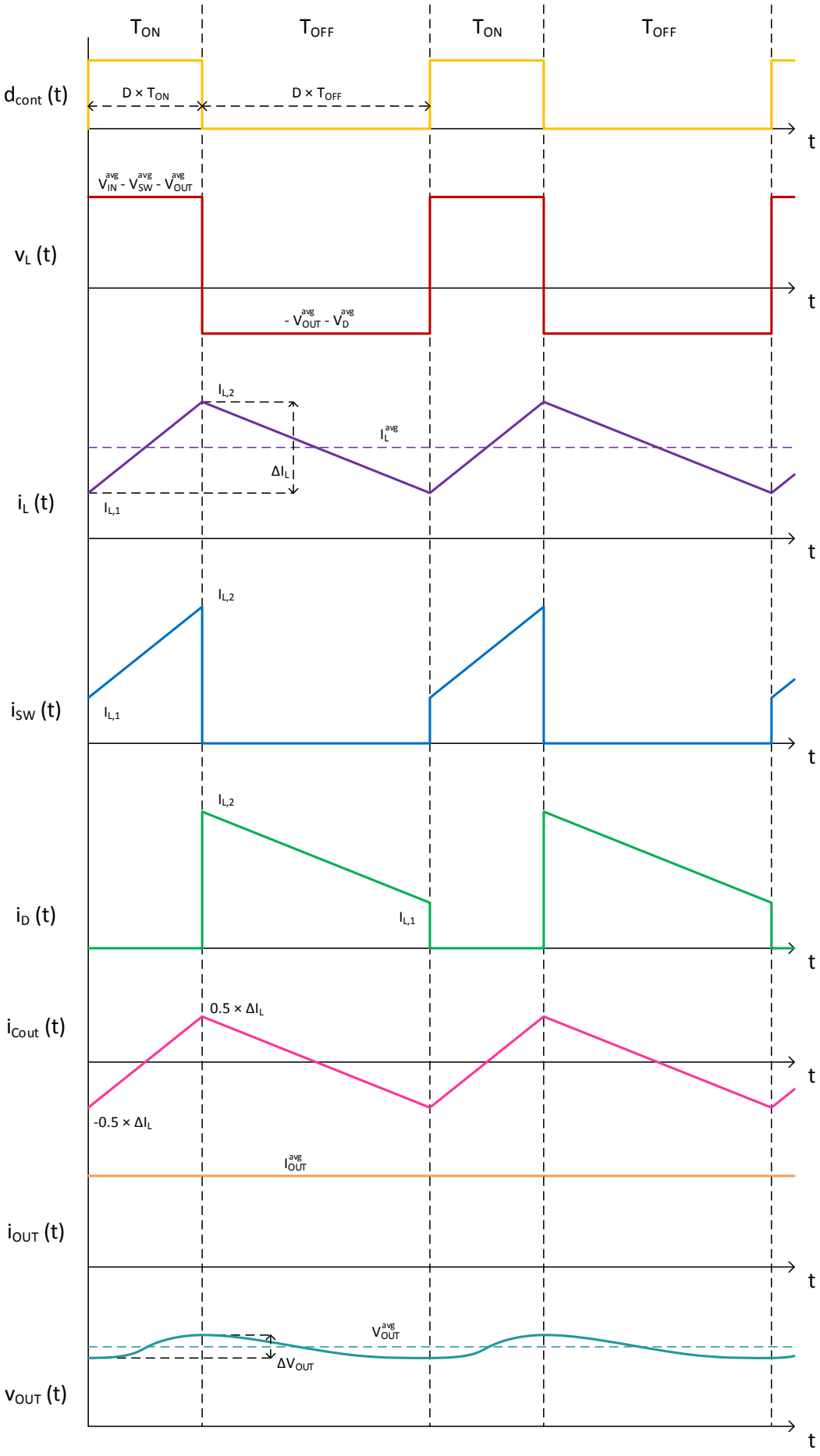

Figure 3.1: Simplified steady-state waveforms of the converter in continuous conduction model considered to elaborate the loss model

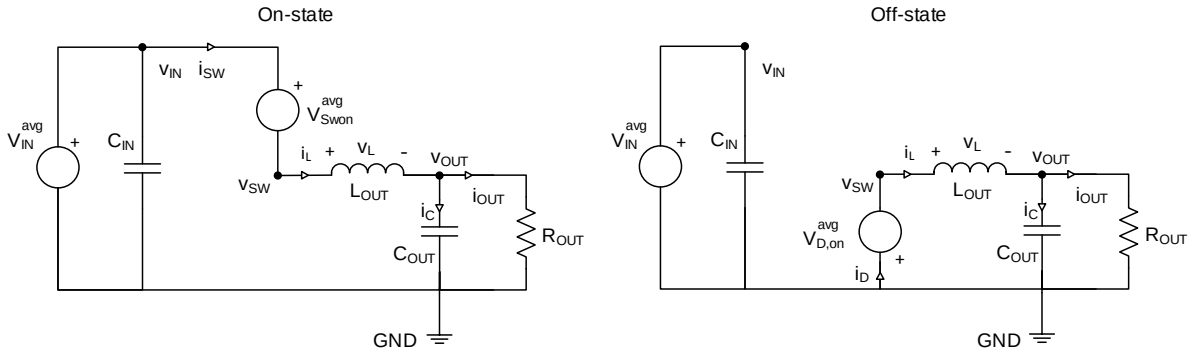

Figure 3.2: Simplified equivalent circuits during on (left) and off-state (right) used to derive the converter expressions

Again, assuming steady-state ($v_C(0) = v_C(T_{SW})$):

$$\int_0^{T_{SW}} i_C(t)\,dt = 0 \tag{3.10}$$

In other words, the average current through the output capacitor equals zero. Having a look at the output node of the converter:

$$i_L(t) = i_{C_{OUT}}(t) + i_{OUT}(t) \tag{3.11}$$

$$\int_0^{T_{SW}} i_L(t)\,dt = \int_0^{T_{SW}} i_{C_{OUT}}(t)\,dt + \int_0^{T_{SW}} i_{OUT}(t)\,dt \longrightarrow I_L^{avg} = I_{OUT}^{avg} \tag{3.12}$$

Another relevant waveform is the coil current. Since the voltage across it during on-state is constant, it can be written:

$$v_L(t) = L\frac{di_L(t)}{dt} \longrightarrow i_L(D\,T_{SW}) = i_L(0) + \frac{1}{L}\int_0^{D\,T_{SW}} v_L(t)\,dt \tag{3.13}$$

$$I_{L,1} = i_L(0); \quad I_{L,2} = i_L(D\,T_{SW}); \quad \Delta I_L = I_{L,2} - I_{L,1} \tag{3.14}$$

Then, the following can be formulated:

$$\Delta I_L = \frac{1}{L}\int_0^{D\,T_{SW}} v_L(t)\,dt = \frac{D\left(V_{IN}^{avg} - V_{SW,on}^{avg} - V_{OUT}^{avg}\right)}{L\,f_{SW}} \tag{3.15}$$

Consequently, the value of the two points of the inductor current can be expressed as:

$$I_{L,1} = I_L^{avg} - \frac{\Delta I_L}{2} \tag{3.16}$$

$$I_{L,2} = I_L^{avg} + \frac{\Delta I_L}{2} \tag{3.17}$$

Once the coil current is known, both switch and diode average currents can be derived according to the shapes depicted in Figure 3.1:

$$I_{SW}^{avg} = \frac{1}{T_{SW}}\int_0^{T_{SW}} i_{SW}(t)\,dt = \frac{I_{L,1} + I_{L,2}}{2}\,D \tag{3.18}$$

$$I_D^{avg} = \frac{1}{T_{SW}}\int_0^{T_{SW}} i_D(t)\,dt = \frac{I_{L,1} + I_{L,2}}{2}\,(1 - D) \tag{3.19}$$

As for the input capacitor, its average current equals zero. Then:

$$I_{IN}^{avg} = I_{SW}^{avg} \tag{3.20}$$

So far, all the relevant average waveforms have been presented and derived. The rms value of a generic waveform can be expressed as:

$$S^{rms} = \sqrt{\frac{1}{T_{SW}} \int_0^{T_{SW}} s^2(t)\, dt} \tag{3.21}$$

Additionally, the rms values of a waveform having a DC and an AC term can be expressed as follows:

$$S^{rms^2} = S_{DC}^{rms^2} + S_{AC}^{rms^2} \tag{3.22}$$

The rms value of a triangular bipolar waveform can be expressed by means of its amplitude:

$$T^{rms} = T_{peak} \frac{1}{\sqrt{3}} \tag{3.23}$$

The inductor current can be expressed as a DC value (which equals I_{OUT}^{avg}) plus a triangular ripple whose rms value will be:

$$I_{L,DC}^{rms} = I_{OUT}^{avg} \tag{3.24}$$

$$I_{L,AC}^{rms} = \frac{\Delta I_L}{\sqrt{12}} \tag{3.25}$$

Therefore, the total rms inductor current is:

$$I_L^{rms} = \sqrt{I_{OUT}^{avg\,2} + \frac{\Delta I_L^2}{12}} \tag{3.26}$$

According to the rms value of a trapezoidal waveform, the diode and switch currents can be derived:

$$I_{SW}^{rms} = \sqrt{\frac{D}{3}\left({I_{L,1}}^2 + {I_{L,2}}^2 + I_{L,1}\, I_{L,2}\right)} \tag{3.27}$$

$$I_D^{rms} = \sqrt{\frac{1-D}{3}\left({I_{L,1}}^2 + {I_{L,2}}^2 + I_{L,1}\, I_{L,2}\right)} \tag{3.28}$$

To sum up, table 3.1 and 3.2 present the most relevant expressions and values derived in this chapter.

	Value
Coil current ripple	$\Delta I_L = \frac{D\,(V_{IN}^{avg} - V_{SW,on}^{avg} - V_{OUT}^{avg})}{L\, f_{SW}}$
Coil current ($t = 0$)	$I_{L,1} = I_L^{avg} - \frac{\Delta I_L}{2}$
Coil current ($t = D\, T_{SW}$)	$I_{L,2} = I_L^{avg} + \frac{\Delta I_L}{2}$

Table 3.1: Main converter operation values

Once the main converter waveforms have been presented and characterized by defining their average and rms values, the magnitudes of the output and input voltage ripple will be addressed from an

	Average value	RMS value
Input voltage	$V_{IN}^{avg} = V_{IN};$	$V_{IN}^{rms} = V_{IN}^{avg};$
Output voltage	$V_{OUT}^{avg} = \left(V_{IN}^{avg} - V_{SW,on}^{avg}\right) D - V_{D,on}^{avg}\,(1-D);$	$V_{OUT}^{rms} = V_{OUT}^{avg};$
Output current	$I_{OUT}^{avg} = \frac{V_{OUT}^{avg}}{R_{OUT}};$	$I_{OUT}^{rms} = I_{OUT}^{avg};$
Coil current	$I_{L,DC}^{avg} = I_{OUT}^{avg};$ $I_{L,AC}^{avg} = 0;$ $I_{L}^{avg} = I_{OUT}^{avg};$	$I_{L,DC}^{rms} = I_{L,DC}^{avg};$ $I_{L,AC}^{rms} = \frac{\Delta I_L}{\sqrt{12}};$ $I_{L}^{rms} = \sqrt{{I_{OUT}^{avg}}^2 + \frac{\Delta I_L^2}{12}};$
Switch current	$I_{SW}^{avg} = \frac{I_{L,1}+I_{L,2}}{2} D;$	$I_{SW}^{rms} = \sqrt{\frac{D}{3}\left({I_{L,1}}^2 + {I_{L,2}}^2 + I_{L,1}\,I_{L,2}\right)};$
Diode current	$I_{D}^{avg} = \frac{I_{L,1}+I_{L,2}}{2}(1-D);$	$I_{D}^{rms} = \sqrt{\frac{1-D}{3}\left({I_{L,1}}^2 + {I_{L,2}}^2 + I_{L,1}\,I_{L,2}\right)};$
Input current	$I_{IN}^{avg} = I_{SW}^{avg};$	$I_{IN}^{rms} = I_{IN}^{avg};$
Input cap. current	$I_{C_{IN}}^{avg} = 0;$	$I_{C_{IN}}^{rms} = \sqrt{{I_{SW}^{rms}}^2 - {I_{IN}^{avg}}^2};$
Output cap. current	$I_{C_{OUT}}^{avg} = 0;$	$I_{C_{OUT}}^{rms} = I_{L,AC}^{rms};$

Table 3.2: Average and rms values of the main converter waveforms

analytical point of view. As for the former, the inductor will be assumed as an independent triangular-shaped current source whose value is given by the circuit operating point and parameters such as voltages, load, inductance and switching frequency. It will also be assumed that the DC component of the coil current goes exclusively to the output load and therefore the output capacitor will only sink the AC component of the inductor current. The procedure followed is very similar to that presented in [21]. The idealized waveforms are shown in figure Figure 3.3. The actual capacitor will be modeled as a capacitance in series with a resistance that takes the ESR into account. The equivalent circuit is depicted in figure 3.4. It yields:

$$i_L(t) = I_{L,DC} + i_{L,AC}(t) \tag{3.29}$$

$$i_{C_{OUT}}(t) = i_{L,AC}(t) \longrightarrow I_{C_{OUT}}^{rms} = I_{L,AC}^{rms} \tag{3.30}$$

$$i_{OUT}(t) = I_{L,DC} \tag{3.31}$$

Assuming that the initial voltage is zero (valid approach since we are interested in a voltage difference) the ripple current can be expressed as:

$$i_{L,AC}(t) = \begin{cases} \frac{\Delta I_L}{2}\left(-1 + 2\frac{t}{D\,T_{SW}}\right) & \text{if } 0 < t < D\,T_{SW} \\ \frac{\Delta I_L}{2}\left(1 - 2\frac{t'}{(1-D)\,T_{SW}}\right) & \text{if } 0 < t' < (1-D)\,T_{SW} \end{cases} \tag{3.32}$$

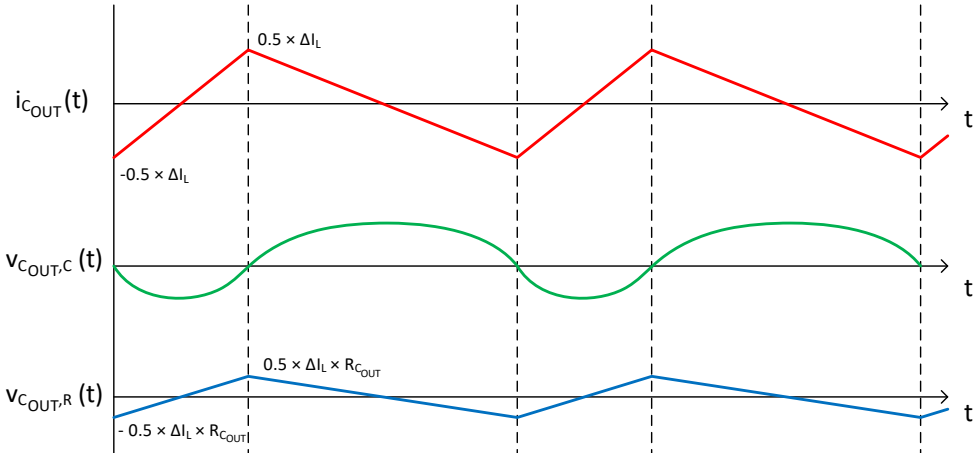

Figure 3.3: Idealized steady-state waveforms of the converter used to derive an expression for the output voltage ripple

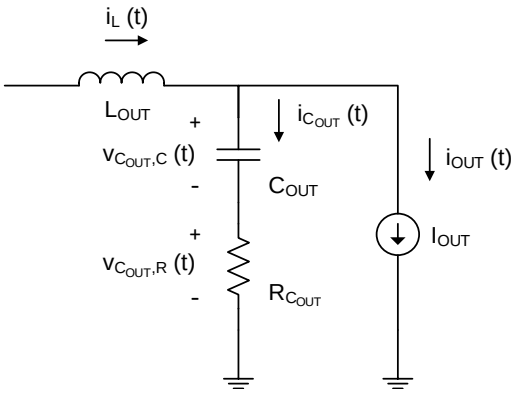

Figure 3.4: Equivalent circuit used to derive an expression for the output voltage ripple

The time origin of the second segment was changed for convenience to $t' = t - D\,T_{SW}$. Let us focus on the first period of time. According to the circuit configuration shown in figure 3.4:

$$v_{C_{OUT},1}(t) = R_{C_{OUT}}\,\frac{\Delta I_L}{2}\left(-1+2\frac{t}{D\,T_{SW}}\right)+\frac{1}{C_{OUT}}\int_0^t \frac{\Delta I_L}{2}\left(-1+2\frac{t}{D\,T_{SW}}\right)dt =$$

$$= R_{C_{OUT}}\,\frac{\Delta I_L}{2}\left(-1+2\frac{t}{D\,T_{SW}}\right)+\frac{\Delta I_L}{2\,C_{OUT}}\left(-t+\frac{t^2}{D\,T_{SW}}\right) \tag{3.33}$$

It can be seen how the output voltage ripple consists of a parabolic and a linear (triangular) expression. Due to the chosen time frame, the current through the capacitor will initially have a negative value. This first part of the voltage will present consequently a decreasing profile and the minimum can be calculated by imposing:

$$\frac{dv_{C_{OUT},1}(t_{min})}{dt} = 0 \tag{3.34}$$

Solving for t_{min} by combining both equations:

$$t_{min} = \frac{D\,T_{SW}}{2} - R_{C_{OUT}}\,C_{OUT} \tag{3.35}$$

However, this is only valid for $t > 0$. It can be written then:

$$t_{min,eff} = \begin{cases} t_{min} & \text{if } t_{min} > 0 \\ 0 & \text{if } t_{min} \leq 0 \end{cases} \tag{3.36}$$

The minimum voltage can be now computed as:

$$V_{OUT}^{min} = v_{C_{OUT},1}(t_{min,eff}) \tag{3.37}$$

Similarly, for the second time interval:

$$v_{C_{OUT},2}(t') = R_{C_{OUT}} \frac{\Delta I_L}{2}\left(1 - 2\frac{t'}{(1-D)\,T_{SW}}\right) + \frac{\Delta I_L}{2\,C_{OUT}}\left(t' - \frac{t'^2}{(1-D)\,T_{SW}}\right) \tag{3.38}$$

The maximum voltage can be obtained at:

$$t'_{max} = \frac{(1-D)\,T_{SW}}{2} - R_{C_{OUT}}\,C_{OUT} \tag{3.39}$$

Since this is only valid for $t' > 0$:

$$t'_{max,eff} = \begin{cases} t'_{max} & \text{if } t'_{max} > 0 \\ 0 & \text{if } t'_{max} \leq 0 \end{cases} \tag{3.40}$$

The maximum voltage level can be computed as:

$$V_{OUT}^{max} = v_{C_{OUT},2}(t'_{max,eff}) \tag{3.41}$$

The output voltage ripple can be finally calculated:

$$\Delta V_{OUT} = V_{OUT}^{max} - V_{OUT}^{min} \tag{3.42}$$

A similar derivation can be worked for the input voltage capacitor. The simplified waveforms used to derive this magnitude are depicted in figure figure 3.5. It is assumed that the input current only consists of a DC component whose value was calculated earlier in this section. The capacitor is again modeled as a resistive and a capacitive element in series. This is presented in figure 3.6. Assuming steady-state:

$$i_{SW}(t) = I_{SW,DC} + i_{SW,AC}(t) \tag{3.43}$$

$$i_{C_{IN}}(t) = i_{SW,AC}(t) \longrightarrow I_{C_{IN}}^{rms} = I_{SW,AC}^{rms} \tag{3.44}$$

$$i_{IN}(t) = I_{SW,DC} \tag{3.45}$$

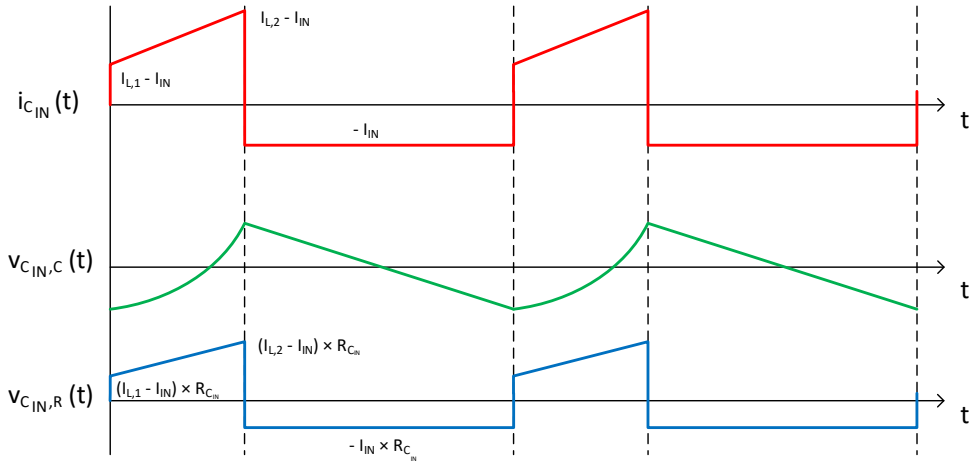

Figure 3.5: Idealized steady-state waveforms of the converter used to derive an expression for the input voltage ripple

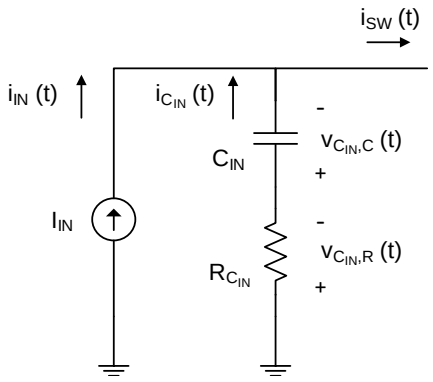

Figure 3.6: Equivalent circuit used to derive an expression for the input voltage ripple

The rms current through the input capacitor can be calculated from previously derived expressions:

$$I_{C_{IN}}^{rms} = I_{SW,AC}^{rms} = \sqrt{I_{sw}^{rms\,2} - I_{IN}^{avg\,2}} = \sqrt{I_{sw}^{rms\,2} - \left(D\,\frac{I_{L,1} + I_{L,2}}{2}\right)^2} \tag{3.46}$$

This current can be defined as a piece-wise linear function of time:

$$i_{C_{IN}}(t) = \begin{cases} I_{L,1} - I_{IN} + \frac{\Delta I_L}{D\,T_{SW}}\,t & \text{if } 0 < t < D\,T_{SW} \\ \\ -I_{IN} & \text{if } 0 < t' < (1-D)\,T_{SW} \end{cases} \tag{3.47}$$

According to the equivalent circuit, the voltage as a function of time within the first interval can be expressed as follows:

$$v_{C_{IN},1}(t) = \left(\frac{\Delta I_L\,R_{C_{IN}}}{D\,T_{SW}}\right)t^2 + \left(\frac{\Delta I_L\,R_{C_{IN}}}{D\,T_{SW}} + \frac{I_{L,1} - I_{IN}}{C_{IN}}\right)t + (I_{L,1} - I_{IN})\,R_{C_{IN}} \tag{3.48}$$

The second time derivative of this voltage is always positive. Therefore, it will have a local minimum at the time at which the first time derivative equals zero:

$$t_{min} = (I_{L,1} - I_{IN})\frac{D\,T_{SW}}{\Delta I_L} - R_{C_{IN}}\,C_{IN} \tag{3.49}$$

The value of interest during the first interval is the maximum magnitude of the voltage that will be used later on to compute the total input voltage ripple. There are three possible cases:

- The local minimum happens at $t < 0$. In this case the interval maximum will take place at $t = D\,T_{SW}$.
- The local minimum happens at $0 < t < D\,T_{SW}$. In this case the interval maximum will take place at either $t = 0$ or $t = D\,T_{SW}$.
- The local minimum happens at $t > D\,T_{SW}$. In this case the interval maximum will take place at $t = 0$.

That is, if both $v_{C_{IN},1}(0)$ and $v_{C_{IN},1}(D\,T_{SW})$ are computed and the highest value is taken into account all conditions are met:

$$V_{IN}^{max} = \begin{cases} v_{C_{IN},1}(0) & \text{if } v_{C_{IN},1}(0) > v_{C_{IN},1}(D\,T_{SW}) \\ \\ v_{C_{IN},1}(D\,T_{SW}) & \text{if } v_{C_{IN},1}(0) < v_{C_{IN},1}(D\,T_{SW}) \end{cases} \tag{3.50}$$

As for the second interval, the current through the capacitor will be negative and constant. Consequently, the capacitive element will present a discharging profile and therefore the minimum will always take place at the end of the interval (the voltage drop across the resistive element will be constant). The voltage drop across the capacitive element must be continuous (that is why the term $\frac{D\,T_{SW}}{C_{IN}}\left(I_{L,1} - I_{IN} + \frac{\Delta I_L}{2}\right)$ is introduced):

$$v_{C_{IN},2}(t') = -R_{C_{IN}}\,I_{IN} - \frac{I_{IN}}{C_{IN}}t' + \frac{D\,T_{SW}}{C_{IN}}\left(I_{L,1} - I_{IN} + \frac{\Delta I_L}{2}\right) \tag{3.51}$$

And the minimum can be computed as:

$$V_{IN}^{min} = v_{C_{IN},2}((1-D)\,T_{SW}) \tag{3.52}$$

The total input voltage ripple can be expressed as:

$$\Delta V_{IN} = V_{IN}^{max} - V_{IN}^{min} \tag{3.53}$$

3.2. Power switch losses

The aim of this section is to provide the reader with a set of equations that will serve as a mathematical model to estimate the power losses generated in the DMOS. An approach similar to that described in [22] will be adopted, including slight modifications to tailor the obtained expressions to this particular application.

3.2.1. Conduction losses

The conduction losses in the DMOS are due to the finite resistance of the channel. As a power switch, the device will be used in the linear or ohmic region where relatively a big amount of current can be carried with a small voltage drop. However, this drop is not negligible and will dissipate some heat as more and more current is conducted. The resistance of the DMOS will be, in the first place, inversely proportional to its area. The device used presents a vertical structure and therefore the current is conducted vertically from drain to source (a lateral device would conduct current in the horizontal direction and therefore the device area would have a different impact on the resistance). Increasing the area would yield a lower current density, consequently decreasing the heat dissipated to the finite resistance of the conducting path.

Another relevant aspect that will determine the value of the on-resistance will be the overdrive voltage at the gate. Increasing the voltage between gate and source would yield the formation of a more conductive channel and therefore the equivalent resistance would be lower.

The temperature will also have and impact on the effective resistance of the switch. MOSFETs show an increasing on-resistance with temperature. This helps avoid thermal runaway since local spots that tend to get hotter than others will start to conduct less current, achieving a global equalizing of the current density in the device. The effect of the temperature has been however neglected and the on-resistance will be considered identical for all operating points of the converter. Table 3.3 presents the most relevant values concerning the on-resistance of the DMOS. Since the power switch itself is not commercially available, there are no datasheets available. That is why these quantities were derived from simulation results that do take into account the specific device parameters.

Parameter	Value
$V_{GS,on}$	3 V
$R_{DS,on}$	6.5 mΩ

Table 3.3: Value of the DMOS' on-resistance for the specified conditions

The equivalent resistance of the DMOS for an operating point can be seen in the V-I curve of the device. From a mathematical point of view, it could be generically defined as:

$$R_{DS,on}(t) = \frac{dv_{DS}(t)}{di_{SW}(t)} \tag{3.54}$$

It can be assumed that this resistance will stay constant as long as it is taken care of properly. That is, if the amount of overdrive and the conducting area of the device remain constant. The former will be a task of the driving circuit (which will keep the DMOS in the same point of the ohmic region); the latter will be associated to using the device properly to guarantee that the current density is homogeneous throughout the device. Then, it can be written:

$$v_{DS}(t) = R_{DS,on}\, i_{SW}(t) \tag{3.55}$$

The power dissipated in the device can be expressed as follows:

$$p_{SW}(t) = v_{DS}(t)\, i_{SW}(t) = R_{DS,on}\, {i_{SW}}^2(t) \tag{3.56}$$

In order to obtain an average value of the total conduction losses within a switching period, the average can be applied:

$$P_{SW}^{cond} = \frac{1}{T_{SW}} \int_0^{T_{SW}} p_{SW}(t)\, dt = \frac{1}{T_{SW}} \int_0^{T_{SW}} R_{DS,on}\, {i_{SW}}^2(t)\, dt = R_{DS,on}\, {I_{SW}^{rms}}^2 \tag{3.57}$$

That is, the conduction losses of the DMOS are proportional to the square of the rms current through the switch. Figure 3.7 depicts the value of these losses for the parameter values shown in Table 3.4.

Parameter	Value	Description
f_{SW}	100, 400 kHz	Switching frequency
D	[10, 90] %	Duty cycle
$V_{SW,on}{}^{avg}$	0 V	Average switch voltage drop
$V_{D,on}{}^{avg}$	0.3 V	Average diode voltage drop
V_{IN}	15, 25 V	Input voltage
C_{IN}	20 µF	Input capacitor
$R_{C_{IN}}$	0.1 Ω	Input capacitor's ESR
L_{OUT}	47 µH	Output inductor
C_{OUT}	20 µF	Output capacitor
$R_{C_{OUT}}$	0.1 Ω	Output capacitor's ESR
R_{OUT}	10 Ω	Output resistor

Table 3.4: Parameter values used to compute the different DMOS' power losses in chapter 3

As expected, increasing the output current (by increasing the duty cycle) yields an increase in the conduction losses. In addition, it can be seen how changing the switching frequency has a minor effect on these losses. The rms value decreases as the switching frequency increases due to the fact that the current ripple is made smaller (the average value remains ideally constant). On the other hand, changing the input voltage has a significant impact on the conduction losses. It can be seen how for a common output current value the conduction losses are smaller for 25 V than for 15 V. The reason is that the duty cycle required to deliver a certain amount of current to the output is smaller and therefore the DMOS is conducting during a smaller amount of time.

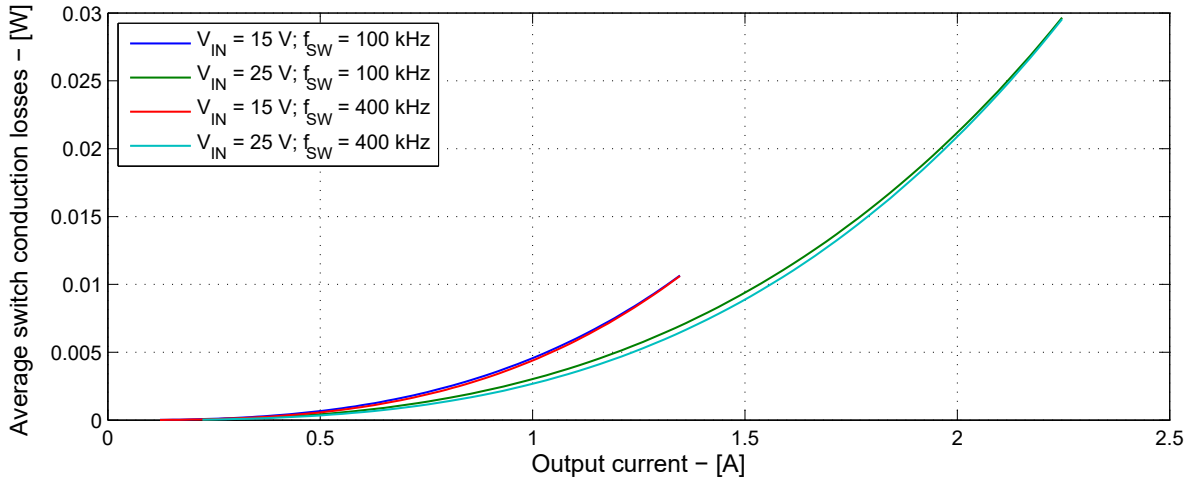

Figure 3.7: Estimated conduction losses in the DMOS according to the parameters presented in table 3.4 and table 3.3

3.2.2. Switching losses

As it has been mentioned before, the DMOS operates very similarly to an ideal switch as long as it is in the ohmic region. This way, the product between current and voltage equals almost zero (however, some conduction losses exist during the on-state as it has been discussed). Unfortunately, this is not the case during the transitioning of the device between on and off states.

Due to the nature of the buck topology, the switching leg will be driving an inductive load. This means that the rate of change of the output current is limited by the inductance seen at the source of the DMOS. In fact, this output current will be assumed constant during the switching event. Let us consider first the turn-on of the switch: a finite amount of time will be required by the high-side device to take over the current. While this happens, the diode is still conducting and therefore the switch sees the whole input voltage across its terminals. Once the diode is fully off and the switch is conducting all of the output current, its voltage has to go to (almost) zero. Again, this requires a finite amount of time to charge the parasitic capacitances at the switching node. A similar phenomenon occurs during the turn-on event: in order for the low-side device to start taking over the current, the DMOS has to let its voltage increase. Once this voltage reaches the input supply value, the switch will start letting the diode conduct. This will also require a finite amount of time. Both events are depicted in a simplified manner in Figure 3.8

Since all waveforms are assumed linear, the generated energy during these switching events can be easily calculated:

$$E_{ON,1} = \frac{1}{2} V_{SW,ON} I_{SW,ON} t_{ON,1} \tag{3.58}$$

$$E_{ON,2} = \frac{1}{2} V_{SW,ON} I_{SW,ON} t_{ON,2} \tag{3.59}$$

$$E_{OFF,1} = \frac{1}{2} V_{SW,OFF} I_{SW,OFF} t_{OFF,1} \tag{3.60}$$

$$E_{OFF,2} = \frac{1}{2} V_{SW,OFF} I_{SW,OFF} t_{OFF,2} \tag{3.61}$$

However, it is more interesting to obtain expressions of the average power dissipated due to the finite transitioning of the switch between on and off states:

$$P_{ON} = (E_{ON,1} + E_{ON,2}) f_{SW} \tag{3.62}$$

$$P_{OFF} = (E_{OFF,1} + E_{OFF,2}) f_{SW} \tag{3.63}$$

$$P_{SW}^{dyn} = P_{ON} + P_{OFF} \tag{3.64}$$

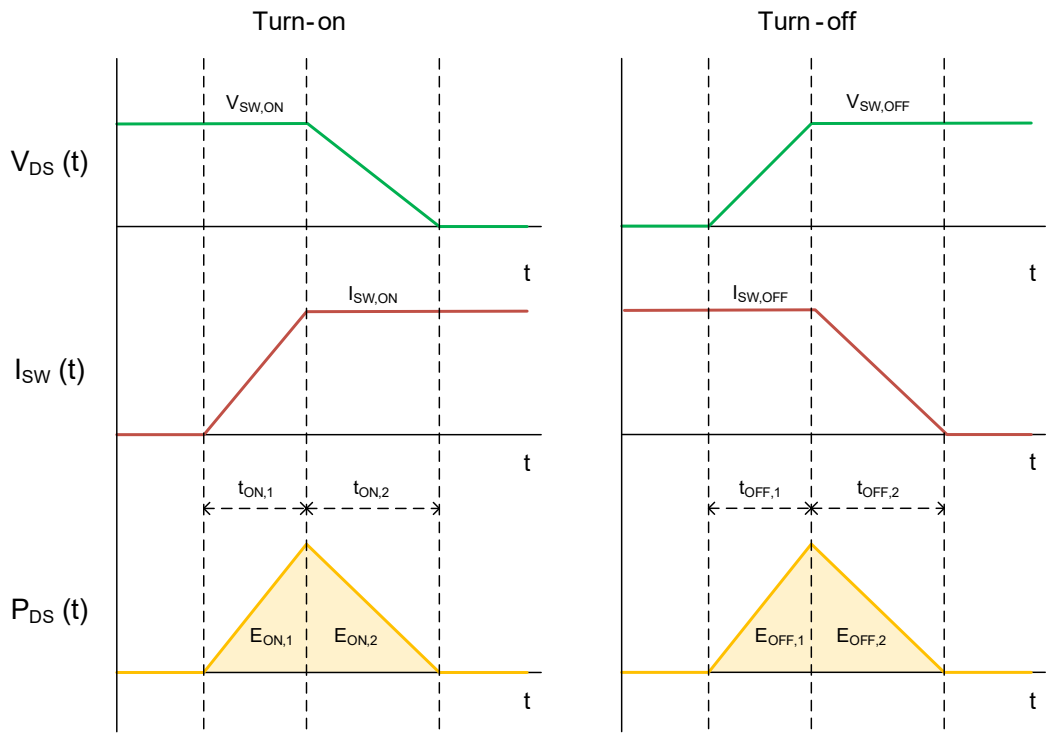

Figure 3.8: Simplified waveforms during turn-on (left) and turn-off (right) considered to model the switching losses

That is, the switching or dynamic losses are directly proportional to the switching frequency of the converter. For the sake of simplicity, the switching times can be considered constant (that is, the transitions always take the same amount of time). Increasing the switching frequency would increase the amount of transitions per unit of time as well. Consequently, the switching losses would be larger. On top of this, these losses will also depend on what values of current and voltages are switched. Let us express the dynamic losses using the values derived from steady state:

$$P_{ON} = \frac{1}{2} V_{IN}^{avg} I_{L,1}(t_{ON,1} + t_{ON,2}) f_{SW} \tag{3.65}$$

$$P_{OFF} = \frac{1}{2} V_{IN}^{avg} I_{L,2}(t_{OFF,1} + t_{OFF,2}) f_{SW} \tag{3.66}$$

Figure 3.9 presents the estimation obtained by using the parameters given in table 3.4. The values for the switching times are taken from simulation results and can be observed in table 5.2.

As expected, the switching losses increase with both the output current and the input voltage. The curves associated to 25 V are wider than those corresponding to 15 V. This is due to the fact that more output current can be delivered for the same duty cycle value. As for the switching frequency, it can be noticed how the dynamic losses are directly proportional to it. As the derived expression implies, doubling the switching frequency will yield doubling the dynamic losses.

3.2.3. Gate losses

Another source of losses in the DMOS is present at the gate of the device. As it has been discussed, certain current has to be supplied to the gate of the switch in order to turn on and off the device. The finite resistance of this path will create ohmic losses that will not be decrease the amount of power delivered to the output. This resistance is mostly present due to PCB traces and packaging of the power switch. As a rough estimation, this resistance will be assumed to be in the order of 2 Ω.

Figure 3.10 presents the approach followed to estimate the power losses generated at the gate of the DMOS. The gate current will be assumed to be a pulsed waveform for both charging and discharging

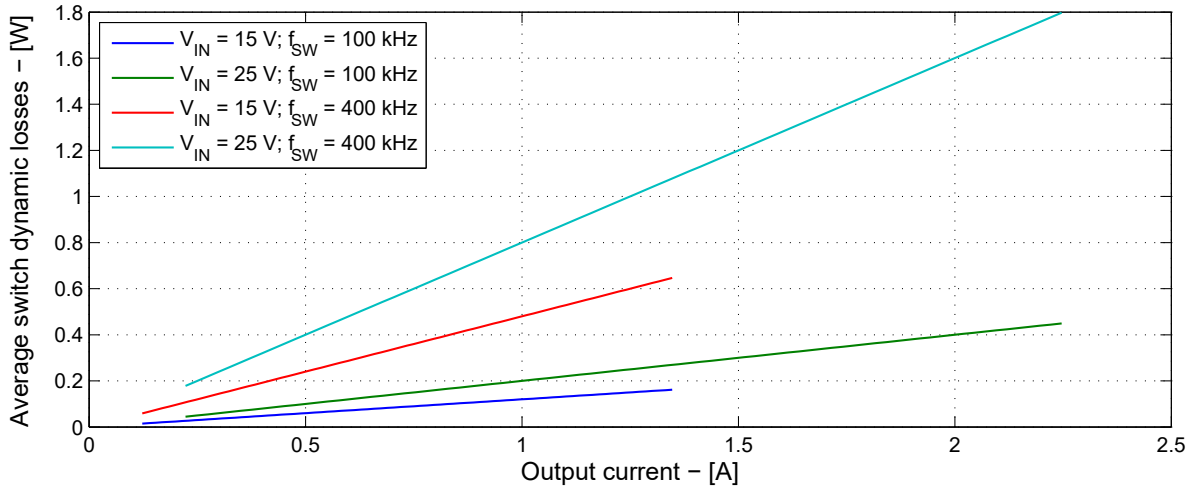

Figure 3.9: Estimated dynamic losses in the DMOS according to the parameters presented in table 3.4 and table 5.2

Time	Value
$t_{ON,1}$	20 ns
$t_{ON,2}$	60 ns
$t_{OFF,1}$	60 ns
$t_{OFF,2}$	20 ns

Table 3.5: Transition times considered to estimate the switching losses of the DMOS

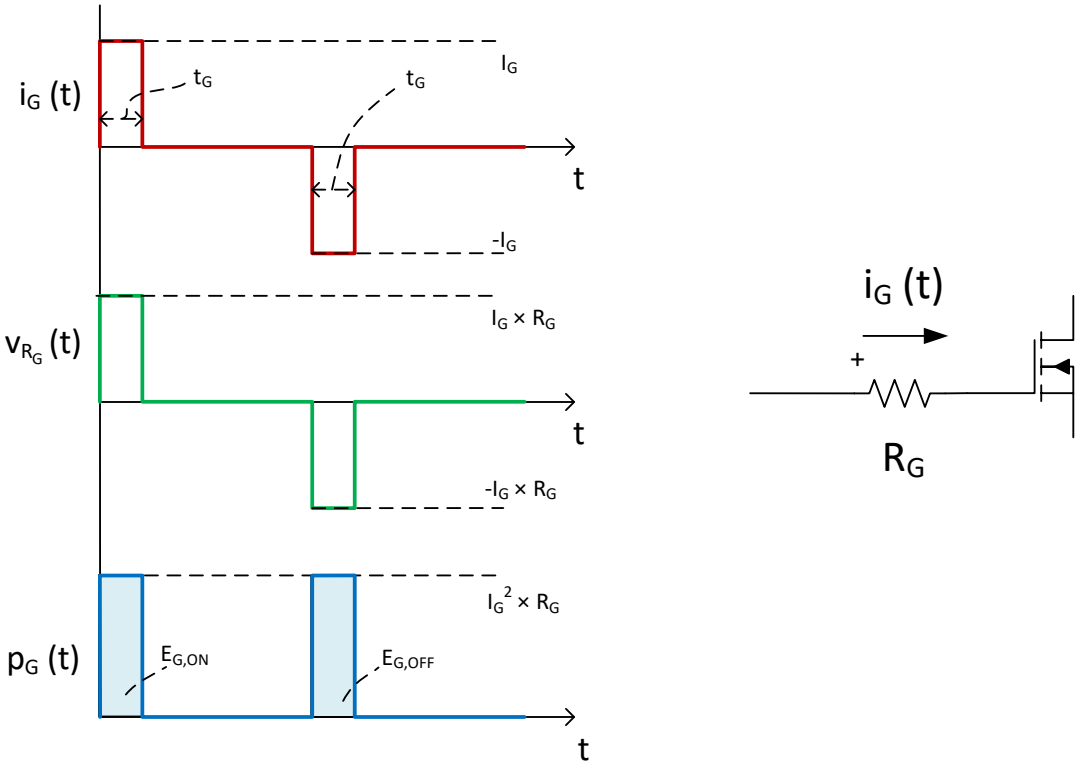

Figure 3.10: Approach used to model and estimate the gate power losses of the DMOS

that has a value of I_G during a time t_G. Such current will create a voltage drop across the equivalent gate resistance. Due to this resistive element, an amount of power will be dissipated. It can be written:

$$E_{G,ON} = t_G \, {I_G}^2 \, R_G \tag{3.67}$$

$$E_{G,OFF} = t_G \, {I_G}^2 \, R_G \tag{3.68}$$

Let us use the following to simplify both expressions:

$$Q_G = I_G \, t_G \tag{3.69}$$

$$E_{G,ON} = I_G \, Q_G \, R_G \tag{3.70}$$

$$E_{G,OFF} = I_G \, Q_G \, R_G \tag{3.71}$$

Averaging the energy for a switching interval:

$$P_G^{avg} = 2 \, I_G \, Q_G \, R_G \, f_{SW} \tag{3.72}$$

That is, the gate losses are proportional to gate current level, gate charge, gate resistance and switching frequency. Let us evaluate the expression for a given operating point in order to get a rough estimation of how large these losses are:

$$I_G = 100mA; \;\; Q_G = 35nC; \;\; R_G = 2\Omega; \;\; f_{SW} = 200kHz;$$
$$P_G^{avg} = 2 \times 100mA \times 35nC \times 2\Omega \times 200kHz = 2.8mW$$

The chosen values are justified by the analysis performed so far. It can be seen how the gate losses are relatively small (especially compared to the dynamic losses) and do not depend on the point at which the converter is operating.

3.2.4. Comparison between derived switch loss model and simulation results

The total switch losses derived from both simulation and estimation results have been presented separately so far. This section aims to serve as a comparison between the two approaches to show how accurate the modeling performed so far is. Figure 3.11 presents the overall switch losses for an input voltage of 20 V and different values of switching frequency. It can be seen how the matching is very good for almost the whole operating range. However, there is a small deviation for low-power points due to assuming constant transitioning times. This simplification is not so valid as the current to be switched becomes lower and lower. In summary, the estimation of the switch losses can be considered very accurate and valid for further analysis.

3.3. Diode losses

As presented earlier, the DMOS' losses can be categorized into conduction, dynamic and gate losses. As regards the low-side device, namely the diode, the loss sources will be similar. Since diodes are not controlled devices, the gate losses will not be present for this kind of devices. However, dynamic and conduction losses could still appear. As for the former, they will be neglected because a schottky device will be used; as for the latter, still a finite resistance will create energy dissipation in the silicon die.

For a buck converter operating in continuous conduction mode, the diode will be forced off by the active switch and its current will have to be taken over by the high-side device. When switching off from this conducting state, a charge redistribution in the low-side diode will have to take place. In case of traditional pn-junction diodes this will require certain amount of reverse current and time to move the minority carriers and adapt the charge distribution to that existing during the non-conducting state. This reverse current peak together with the voltage built across the device will dissipate an amount of power which can be very large for some cases. What is more, this reverse current will be forced through

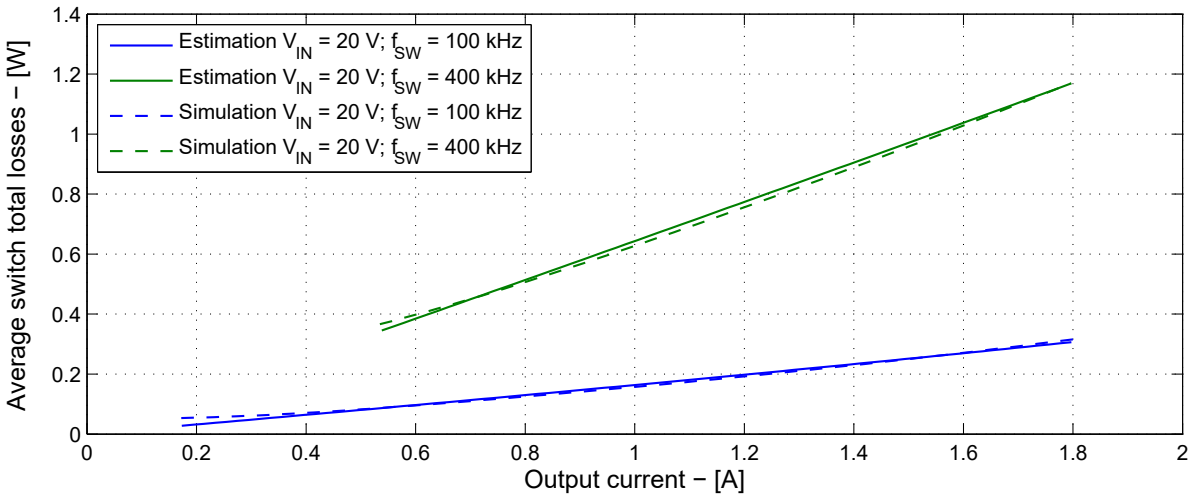

Figure 3.11: Comparison between simulation-based and estimated total losses in the DMOS according to parameters presented in table 3.4, table 3.3 and table 5.2

the high-side switch and will create additional losses [23]. On the other hand, schottky diodes have electrons as majority carriers on both sides of the junction and can be considered unipolar devices. Consequently, the recombination between holes and electrons will not take place. As a result, turn-on and turn-off can be considered immediate for most applications since no minority carriers must be injected into the device during turn-on and pulled out during turn-off [24].

As for the conduction losses, they will occur for both schottky and traditional pn-junction diodes. The following assumption will be made in order to express the V-I characteristics of the diode:

$$v_D(t) = V_D + R_D\, i_D(t) \tag{3.73}$$

That is, the V-I curve will be a straight line with certain slope added to a voltage offset. This model takes into account the finite resistance of the device and the minimum voltage drop needed to bias the diode. The power dissipation can be expressed as:

$$p_D(t) = v_D(t)\, i_D(t) = i_D(t)\,(V_D + R_D\, i_D(t)) = V_D\, i_D(t) + R_D\, {i_D}^2(t) \tag{3.74}$$

The average power in steady-state will be then:

$$P_D^{cond} = \int_0^{T_{SW}} p_D(t)\, dt = V_D \int_0^{T_{SW}} i_D(t)\, dt + R_D \int_0^{T_{SW}} {i_D}^2(t)\, dt \tag{3.75}$$

This expression can be written as:

$$P_D^{cond} = V_D\, I_D^{avg} + R_D\, I_D^{rms\,2} \tag{3.76}$$

That is, the conduction losses will be proportional to the average current (due to the voltage drop across the device) and to the square of the rms current (due to the resistance of the diode). Figure 3.12 presents the conduction losses of the low-side diode as modeled in this section. The parameters used are shown in table 3.6.

Parameter	Value
V_D	0.3 V
R_D	50 mΩ

Table 3.6: Parameters used to estimate the diode conduction losses presented in figure 3.12

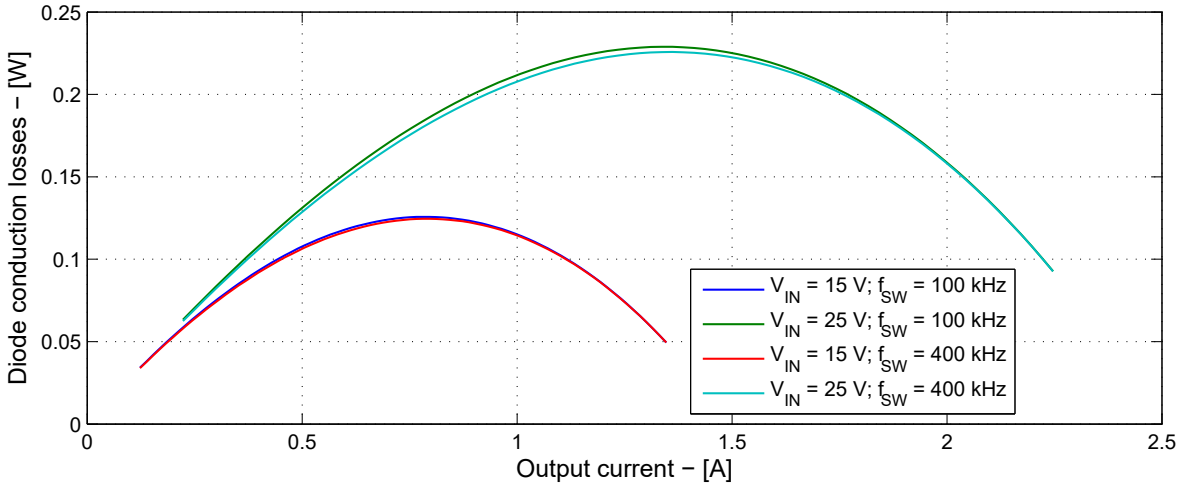

Figure 3.12: Conduction losses in the low-side schottky diode according to the parameters shown in table 3.6 and table 3.4

It can be seen how changing the switching frequency while keeping the input voltage constant has hardly any significant effect on the diode losses. Varying the switching frequency ideally only affects the ripple while the average remains constant. Let us assume that the ripple is negligible. Then, it can be written:

$$I_D^{avg} = I_O\,(1-D) \tag{3.77}$$

$$I_D^{rms} = I_O\,\sqrt{1-D} \tag{3.78}$$

$$P_D^{cond} = (1-D)\,(I_O\,V_D + {I_O}^2\,R_D) \tag{3.79}$$

This expression shows that for a given output current level, the conduction losses will decrease with an increasing duty cycle and vice versa. This would mean that increasing the input voltage for a given output current (that is, decreasing the duty cycle) will yield larger diode conduction losses.

It can be also noticed that the curve presents a maximum. Let us reformulate the previous expression:

$$D = \frac{I_O\,R_{OUT}}{V_{IN}} \tag{3.80}$$

$$P_D^{cond} = \left(1 - \frac{I_O\,R_{OUT}}{V_{IN}}\right)(I_O\,V_D + {I_O}^2\,R_D) \tag{3.81}$$

In other words, the conduction losses can be modeled as a curve with order 3. As seen in figure 3.12, the maximum happens at approximately half of the current range. It can be proven that this maximum will be located between $D = 0.5$ (if $R_{OUT} = \infty$) and $D = 2/3$ (if $R_{OUT} = 0$). The exact location will depend on the output resistance itself and other parameters such as input voltage, diode equivalent resistance and diode equivalent voltage offset.

3.4. Coil losses

The inductor is a key component in the buck converter and the operation of the system really depends on its properties. Typically, they consist of wire wound around a core of magnetic material that may include an air gap. They store energy in a magnetic field during the on time and deliver that energy back to the load during the off time. In other words, the inductor will provide the output of the converter with a smoothed excitation despite the chopping nature of the switching leg. Inductors dissipate power in the core and in the windings. Exact calculations of these losses can be complex. However, they can be estimated using data sheet parameters and simplified models.

Let us introduce some basic magnetic parameters associated with inductors. Ampere's and Faraday's law can be used to explain the operating principle of inductive elements. It will be assumed that

the magnetic field is uniform throughout the core length and that it is contained within the core material. Then, Ampere's law can be written as [25]:

$$H(t)\, l_{EQ} = n\, i_L(t) \tag{3.82}$$

Where H is the magnetic field strength (in amps per meters), l_{EQ} is the equivalent core length (in meters), n is the number of turns of the wound conductor and i_L is the current through the coil (in amps). Faraday's law, which relates the voltage across the coil to the magnetic flux contained within the core can be expressed as [25]:

$$v_L(t) = n\,\frac{d\Phi(t)}{dt} = n\,A_C\,\frac{dB(t)}{dt} = L\,\frac{di_L(t)}{dt} \tag{3.83}$$

Where v_L is the voltage across the inductor (in volts), Φ is the magnetic flux (in webers), B is the magnetic flux density (in teslas), A_C is the cross sectional area of the core (in square meters) and L is the inductance of the coil (in henries). This two equations show how both magnetic field density and strength relate to voltage and current through the coil. Applying a positive voltage across the coil during the on state will yield an increase in both magnetic field density and strength. Consequently, the current through the coil will increase. A negative voltage during the off state will have the opposite effect: decreasing magnetic field strength and density and therefore decreasing the current through the inductor.

In practice, the variation is not linear and exhibits non-idealities (due to, for instance, saturation of the core and magnetic field not being totally homogeneous). Figure 3.13 present an example of the magnetic curve created in a magnetic core. The horizontal axis corresponds to the magnetic field strength and the vertical axis to the magnetic field density. It can be clearly seen how the curve has a variable slope and presents some kind of hysteresis behavior. It can also be noticed how the magnetic fields always a positive sign. This is due to the fact that the buck converter is operating in continuous conduction mode and the direction of the current cannot be reversed.

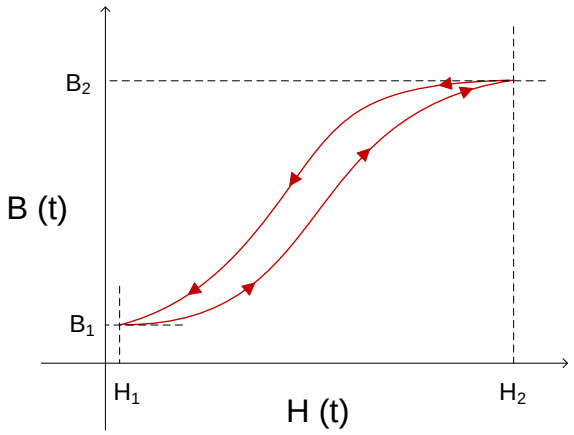

Figure 3.13: Magnetic BH curve of an inductor in a buck converter operating in continuous conduction mode

3.4.1. Core losses

The hysteresis phenomenon is the main contributor to the core losses in the inductor. This behavior of core materials implies that the energy taken back from the magnetic field is lower than that used to generate it. Figure 3.14 tries to depict this concept. The energy losses due to the changing magnetic field during a switching cycle can be expressed as:

$$E_{hyst} = \int_0^{T_{SW}} v_L(t)\, i_L(t)\, dt \tag{3.84}$$

Using Ampere's and Faraday's laws:

$$E_{hyst} = \int_0^{T_{SW}} (n\,A_C\,\frac{dB(t)}{dt})\,(H(t)\,\frac{l_{EQ}}{n})\,dt \tag{3.85}$$

$$E_{hyst} = A_C\,l_{EQ}\left(\int_{B_1}^{B_2} H(B)\,dB + \int_{B_2}^{B_1} H(B)\,dB\right) \tag{3.86}$$

Two different area integrals can be observed in figure 3.14:

$$A_1 = \int_{B_1}^{B_2} H(B)\,dB \tag{3.87}$$

$$A_2 = \int_{B_2}^{B_1} H(B)\,dB \tag{3.88}$$

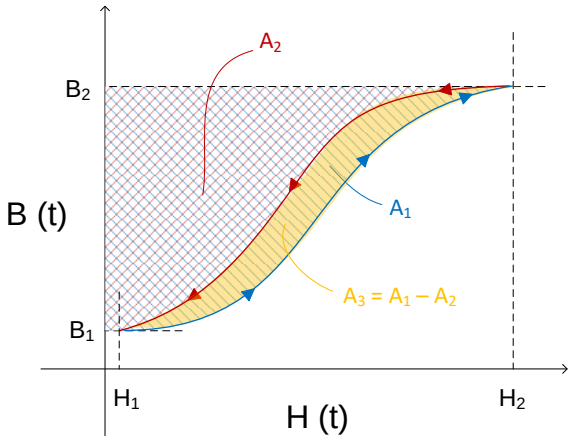

Figure 3.14: Magnetic energy flow of an inductor in a buck converter operating in continuous conduction mode to show hysteresis losses

A_1 (blue) relates to the energy delivered to the coil during the on state to store energy by means of a magnetic field. A_2 (red), on the other hand, relates to the energy given back from the magnetic field during the off phase. Due to the hysteresis of the magnetic loop, the latter will be lower than the former. The difference between these two areas, A_3, relate to the actual losses due to magnetic hysteresis.

The second type of core loss is due to eddy currents, which are induced in the core material by a time varying flux. According to Faraday's law, this will induce a voltage at the core whose effect would try to oppose the causing flux. Since the core is made up of a conducting material, a current will circulate. As expected, the finite resistance of the material will yield additional power losses. Because the core material has high resistance, losses due to eddy currents in the core are usually much less than those due to hysteresis [25].

Once both mechanisms have been presented from a theoretical point of view, a way to model them will be presented. Core-loss measurements are difficult because they require complicated setups to measure flux density and because they require, for instance, the estimation of hysteresis-loop areas. Some inductor manufacturers supply this data by means of material curves to approximate the core loss in an inductor. However, this curves are based on measurements done using sinusoidal excitation, which is not very useful when dealing with power electronic converters. On the other hand, a more theoretical-oriented approach can be followed. This is the case of the Modified Steinmetz Equation (MSE) [26]. This procedure establishes a way of calculating the lossesfor arbitrary waveforms of flux while using the available set of parameters of the classical Steinmetz equation.

The MSE is based on the empirical Steinmetz equation, which estimates power losses per unit of volume and can be expressed as:

$$P_{core} = C_m\,f^{\alpha}\,B^{\beta} \tag{3.89}$$

Where C_m, α and β are empirical parameters derived from measurements carried out using sinusoidal excitation. Therefore, this approach is not considered accurate when working with non-sinusoidal waveforms. On the other hand, the MSE is based on the following expressions:

$$P_{core} = \left(C_m {f_{EQ}}^{\alpha-1} B^{\beta}\right) f_{SW} \tag{3.90}$$

$$f_{EQ} = \frac{2}{\Delta B^2 \pi^2} \int_0^{T_{SW}} \left(\frac{dB}{dt}\right)^2 dt \tag{3.91}$$

Where f_{EQ} weighs the non-sinusoidal character of the excitation waveforms applied to the core material. C_m, α and β are again empirical constants obtained from sinusoidal excitation. The MSE presented is expressed in a generic form. As a step further, it can be applied to the converter analyzed in this thesis work:

$$\Delta B = \frac{V_{IN}\,(1-D)}{k_{COIL}\, f_{SW}} \tag{3.92}$$

Where k_{COIL} is a constant whose value depend on the number of turns and the cross sectional area of the core. As for the equivalent switching frequency, the term which includes the integral of the time derivative of the flux density can be expressed as:

$$\int_0^{T_{SW}} \left(\frac{dB}{dt}\right)^2 dt = \int_0^{D\,T_{SW}} \left(\frac{V_{IN}\,(1-D)}{k_{COIL}}\right)^2 dt + \int_{D\,T_{SW}}^{T_{SW}} \left(\frac{V_{IN}\,D}{k_{COIL}}\right)^2 dt \tag{3.93}$$

$$\int_0^{T_{SW}} \left(\frac{dB}{dt}\right)^2 dt = \frac{D\,(1-D)}{f_{SW}} \left(\frac{V_{IN}}{k_{COIL}}\right)^2 \tag{3.94}$$

The equivalent frequency will be then:

$$f_{EQ} = \frac{2}{\pi^2} \frac{1}{D\,(1-D)} f_{SW} \tag{3.95}$$

Since the excitation of the coil is always in the same direction:

$$B = \Delta B \tag{3.96}$$

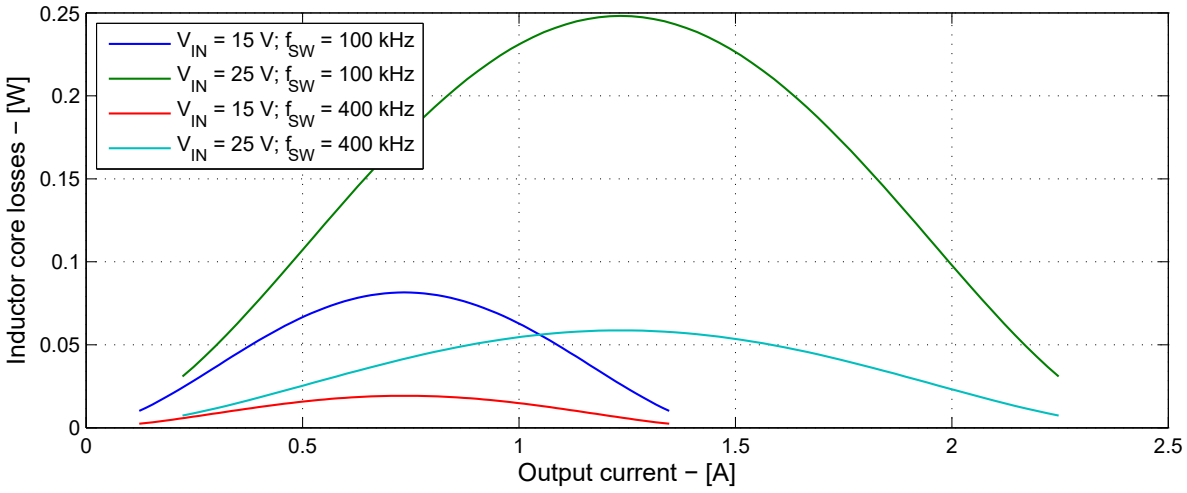

Figure 3.15: MSE-based estimation of inductor core losses according to the parameters presented in table 3.7 and table 3.4

Figure 3.15 shows the estimation of the core losses according to the inductor parameters shown in table 3.7. These were derived from a commercial coil whose manufacturer provides a calculator tool to estimate the losses. It can be noticed how the core losses significantly increase with the input voltage.

Parameter	Value
C_m	700.37×10^{-6}
α	1.173
β	2.213
k_{COIL}	1.923×10^{-3}

Table 3.7: Parameters used to estimate the inductor core losses presented in figure 3.15

A higher input voltage will mean a higher flux density peak (according to the MSE the losses will be highly dependent on this variable). On the other hand, it can be seen how increasing the switching frequency brings the core losses down. Again, the explanation can be found by having a look at the MSE: doubling the switching frequency will ideally reduce the flux density peak to half of its initial value. The equivalent switching frequency will increase with this, but since the value of beta is approximately twice the value of alpha the overall losses will be smaller.

3.4.2. Winding losses

These losses are sometimes known as copper losses too, but since other materials can be used to build the conductors, they will be referred to as winding losses. In addition to the core losses previously presented, losses also occur in the inductor windings. These can be split into DC and AC winding losses. The former are due to the DC resistance and DC rms current through the inductor. This current will generate Joule heating in the conductor which can be expressed as:

$$P_{wind,DC} = R_{wind,DC}\, {I_{L,DC}^{rms}}^2 \tag{3.97}$$

Where $R_{wind,DC}$ is the equivalent DC resistance of the coil winding which is typically given my manufacturers or estimated / measured for hand-crafted coils. On top of the DC winding losses, the AC component of the coil current will also generate power losses. These must be treated separately due to the so-called skin effect. Increasing the frequency of the AC current will increase the effective resistance of the winding at this frequency. The changing current will induce a changing flux perpendicular to the current that induces it. According to Faraday's law, this variation of flux will induce eddy currents which create themselves a varying flux opposing the initial one. The induced flux is strongest at the center of the conductor and weakest at its surface. Therefore, the current density at the center will decrease. In other words, current will get pushed to the surface of the conductor, increasing the current density at this part [25].

This problem is relatively complex and its analysis can be simplified by defining the so called skin depth:

$$D_{sk} = \sqrt{\frac{\rho}{\pi\, \mu\, f_{SW}}} \tag{3.98}$$

Where ρ is the resistivity of the conductor (typically copper) and μ is the conductor permeability ($\mu = \mu_0\, \mu_R$ where μ_R is 1 for copper). The equivalent AC resistance can be calculated by assuming that the effective area of the conductor is that of the ring whose thickness equals the skin depth. This assumption can be considered valid as long as the skin depth is much smaller than the conductor diameter. The ratio between DC and AC resistances can be expressed as follows:

$$\frac{R_{wind,AC}}{R_{wind,DC}} = \frac{\pi\, r^2}{\pi\, r^2 - \pi\, (r - D_{sk})^2} \tag{3.99}$$

Where r is the radius of the winding conductor. Eddy currents in the inductor windings can also be induced by nearby conductors. This phenomenon is usually known as proximity effect. For inductors with many overlapping turns, the increased eddy currents cause a resistance considerably higher than

that from the skin effect alone. The analysis becomes very complicated and calculations are assumed beyond the scope of this thesis work. The proximity effect will be therefore assumed negligible. The AC winding losses can be expressed as:

$$P_{wind,AC} = R_{wind,AC}\, I_{L,AC}^{rms\,2} \tag{3.100}$$

And the total winding losses will be:

$$P_{wind} = P_{wind,DC} + P_{wind,AC} \tag{3.101}$$

Parameter	Value
$R_{wind,DC}$	42.7 mΩ
r	1.3 mm
ρ	1.68 x 10^{-8} Ω m
μ	4 π x 10^{-7} H / m

Table 3.8: Parameters used to estimate the inductor winding losses presented in figure 3.16

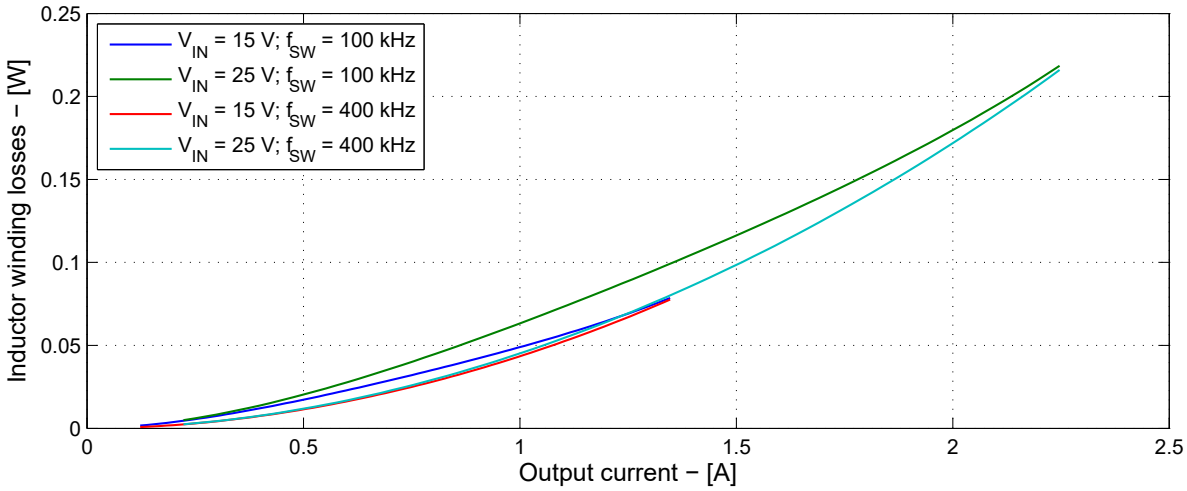

Figure 3.16: Estimation of inductor winding losses according to the parameters presented in table 3.8 and table 3.4

Figure 3.16 presents the estimation of the winding losses according to the parameters shown in table 3.7. These have been derived from data provided by a coil manufacturer. It can be observed how the 4 different cases present similar winding losses. This is due to the fact that the DC winding losses are the dominant loss source. The DC component of the coil current ideally remains constant and therefore the power dissipated in the equivalent DC resistance for a given output current is the same for all cases. The differences are due to the AC component of the coil current, which depends on the switching frequency and the input voltage of the converter. Increasing the former parameter yields lower AC winding losses due to the current ripple becoming lower; increasing the latter parameter yields larger winding losses due to the increase in current ripple. This difference becomes smaller and smaller with the switching frequency: the first two curves differ from each other much more than the other two curves.

3.5. Capacitor losses

Ideally, capacitors present no losses and simply store energy by means of electric fields that can be given back to the circuit afterwards according to its operating principle. In practice, there will be a

resistive behavior due to the physical characteristics of capacitor devices. When an alternating voltage is applied to a capacitor, current will start to flow through its dielectric material and its conductive parts (electrodes, lead wires, terminations...). The finite resistance seen by this flow of current will create a power dissipation that will yield a temperature increase in the passive device.

The overall resistance of the capacitor, usually referred to as equivalent series resistance (ESR) is a sum of two elements: the resistance of the dielectric material; and the resistance of the conductive parts. As for the former, each material presents a dissipation factor which is frequency dependent and displays a small increase with increasing frequency. This part of the ESR is high for low frequencies and decreases with increasing frequency. As for the conductive parts, it will be assumed as a constant frequency independent value. Overall, the dielectric resistance dominates at low frequencies while the resistance of the conductive parts is dominant at higher frequencies [**?**].

The value of the ESR is usually not well defined in datasheets and therefore assumptions have to be made in order to estimate it. The main factor that determines the magnitude of the ESR is the capacitor technology. Aluminum electrolytic devices typically used as bulk capacitors with high capacitance values have an ESR in the order of hundreds of mΩ or even higher. What is more, their frequency response is limited and they are not effective capacitances in the range of hundreds of kilohertz. On the other hand, ceramic capacitors have a more limited amount of capacitance per device. Their ESR, in the order of tens of mΩ, is much lower than that of aluminum capacitors. Additionally, their frequency response is much better and they act as the effective capacitance in the range of hundreds of kilohertz. These devices will therefore provide the power converter with the filtering properties required at input and output.

In practice, the input and output capacitance will be built up from several devices constructed in different technologies. This way, big bulk capacitors will be used at input and output to filter out transient responses of the system. Smaller and faster ceramic capacitors of different sizes will be used to provide the converter with the required filtering elements. The loss mechanism will be tackled by assuming a single equivalent ESR at both input and output which represents the losses of all capacitive devices. The losses can be then expressed as:

$$P_{C_{IN}} = R_{C_{IN}} I_{C_{IN}}^{rms\,2} \tag{3.102}$$

$$P_{C_{OUT}} = R_{C_{OUT}} I_{C_{OUT}}^{rms\ 2} \tag{3.103}$$

Where $R_{C_{IN}}$ and $R_{C_{OUT}}$ are the equivalent series resistances of input and output capacitors respectively. Table 3.9 presents the parameter values used to estimate the capacitor losses depicted in figure 3.17 and figure 3.18. These values have been obtained after paralleling the ESR taken from datasheet of aluminum [27] and ceramic [28] capacitors.

As regards the estimation of the input capacitor losses, it can be observed how increasing the switching frequency yields a decreasing in the power losses. This can be explained by a decrease of the current ripple, since the current through the input capacitor is equal to the AC component of the switch current. On the other hand, increasing the input voltage will make the current that can be delivered for a given duty cycle increase. Consequently, the current range will increase and the capacitor losses will be larger for most operating points. Another interesting fact about the input capacitor losses is that they increase with output current and duty cycle until a maximum point is reached, from which the rms current becomes smaller.

The output capacitor losses also exhibit this maximum point. However, it will be roughly located at the middle operating point where the coil current ripple is maximum. An increase of the switching frequency significantly decreases the power losses due to the ripple becoming smaller. As for the input voltage, increasing its value yields larger power losses due to the increase in ripple current. In addition, the current that can be delivered for a given duty cycle increases together with the capacitor losses for most of the current range.

3.6. Selecting and sizing of components

Once the modeling of the losses has been presented and described, the actual components that will be part of the buck converter have to be selected. In order to guarantee proper functioning of the

Parameter	Value
$R_{C_{IN}}$	0.2 Ω
$R_{C_{OUT}}$	0.2 Ω

Table 3.9: Parameters used to estimate the capacitor losses presented in figure 3.17 and figure 3.18

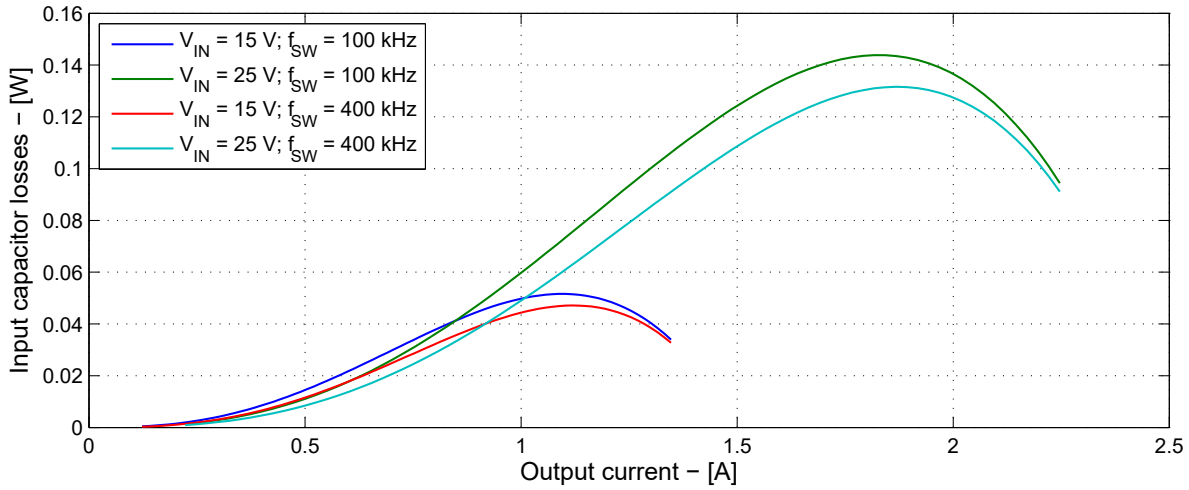

Figure 3.17: Estimation of input capacitor losses according to the parameters presented in table 3.9 and table 3.4

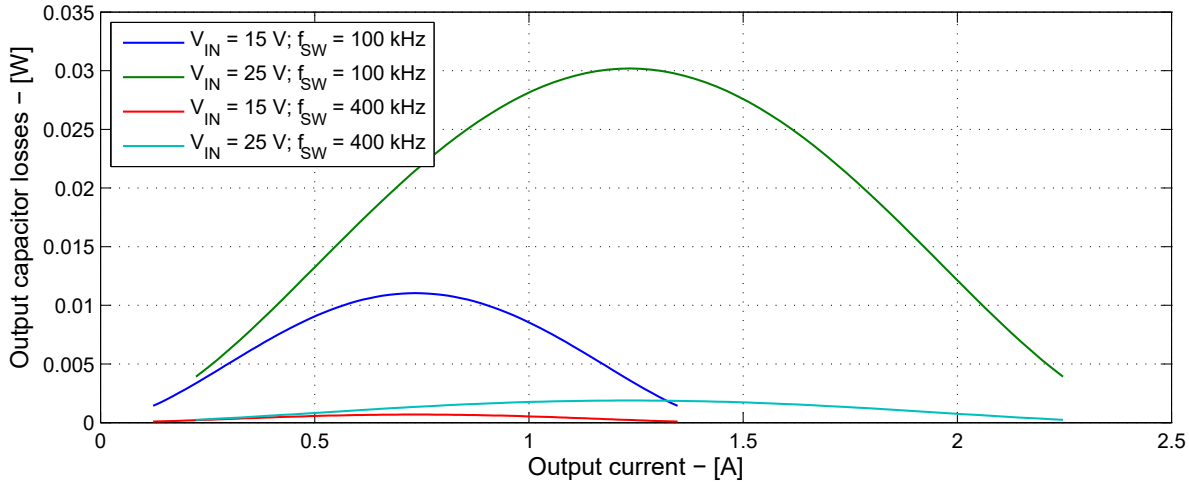

Figure 3.18: Estimation of output capacitor losses according to the parameters presented in table 3.9 and table 3.4

solution, each of them will have to meet a certain set of requirements. These will be typically related to current, voltage and temperature restrictions. The approach followed will be based on the steady state waveforms which have been derived earlier in this section. Another relevant input to the selecting process will be the information obtained from manufacturer datasheets. All in all, the sizing of the components will be an iterative process which will be satisfactory once all conditions are met.

3.6.1. Coil

The first element of the converter that will be sized is the inductor. It will determine the amount of current that the switching leg has to carry. In addition, it will also dictate the amount of ripple current that the output capacitor has to filter out. In summary, the output coil can be seen as the central element of the sizing of the converter.

Coils can be either handcrafted or directly bought to manufacturers that sell fixed valued devices. In case the former approach is adopted, the value of inductance to be realized is chosen by the designer. The core material and shape that suit the application best in terms of cost, size and performance can be selected in the design process. Additionally, the conductor can be chosen and wound as desired in order to obtain certain inductance, equivalent resistance and field distribution. For instance, the design would be an iterative process where the input parameters are the desired inductance, core material / shape and conductor. The final design must satisfy a set of requirements related to field density (to avoid saturation), temperature and inductance. This procedure is generally applied for very specific applications whose design goal is optimizing the solution.

On the other hand, the passive element can be also selected from a list of commercially available devices. This way, only certain values of inductances can be used. Each series of devices will come in a specific package and the design presents more freedom in this respect. The final solution could be modified or adapted afterwards to suit another application. This approach is therefore more versatile. The negative side is that the solution will not be so cost-effective and its price will be influenced by the manufacturer. However, more and more devices are becoming available in the market and the possibilities are numerous if the application of interest is not too specific. This approach will be adopted since the solution analyzed in this thesis work is in the development phase. This way, the design flow will be more flexible and faster.

After examining commercially available solutions to take into consideration for the design phase, Vishay's IHLP-6767GZ-11 [29] coil series has been observed to be suitable for the application of interest. Table 3.10 presents different options available and their corresponding parameters that will be given as inputs for the sizing process. The inductance has a tolerance of 20 % in both ways due to the fabrication process and the given value is measured at 100 kHz. The maximum DC resistance will be determined by the winding used for each model. Generally, the larger the inductance the more amount of copper will be required, resulting in a larger equivalent resistance. The DC heat rating current is the current that causes a temperature increase of approximately 40 ºC. The DC saturation current is defined as the DC current that yields a drop of 20 % in the inductance value. The self-resonant frequency (SRF) is the frequency above which the passive device will not behave as an inductance due to the parasitic elements coming into play. The coils from this series are manufactured to operate between -55 and +125 ºC.

Ind. ($\pm$ 20 %) [µH]	**DC res. [mΩ]**	**Heat rat. curr. [A]**	**Sat. curr. [A]**	**SRF [MHz]**
10	9.33	19	17	8.0
15	14.4	14	12	7.5
22	21.0	12	9.5	4.3
33	37.0	10.7	9.0	4.8
47	42.7	8.7	8.6	4.1
56	57.8	7.2	4.2	2.9
68	75.7	6.1	4.5	3.0
82	91.7	5.5	4.5	2.6
100	110	5.0	4.0	2.1

Table 3.10: Different coil options available in Vishay's IHLP-6767GZ-11 series

Vishay's IHLP coils are in the family of composite power inductors (CPI), whose construction differs from conventional magnetics since the assembly process is reversed [30]. CPI construction starts with a pre-wound coil of wire that is welded or soldered into a frame. Such assembly is then placed in a steel die filled with powdered metal, which will be compressed from above and below to form a dense magnetic body around the coil. This confers Vishay's inductors an almost linear and soft saturation curve [31]. Figure 3.19 shows this phenomenon: the red line represents a typical saturation curve for a ferrite core power inductor; the blue curve represents the saturation curve of an IHLP inductor

from Vishay. It can be seen how the former reaches a current value from which the inductance drops drastically. This is known as the saturation knee. Operating the inductor beyond this current level will yield hard saturation and is dangerous because of the inductive impedance dropping significantly (an uncontrolled rise in current can occur). The IHLP presents a much softer saturation curve without saturation knee. Different material and core volumes can be used in order to obtain different properties and inductors. Several IHLP-based series are commercially available from Vishay.

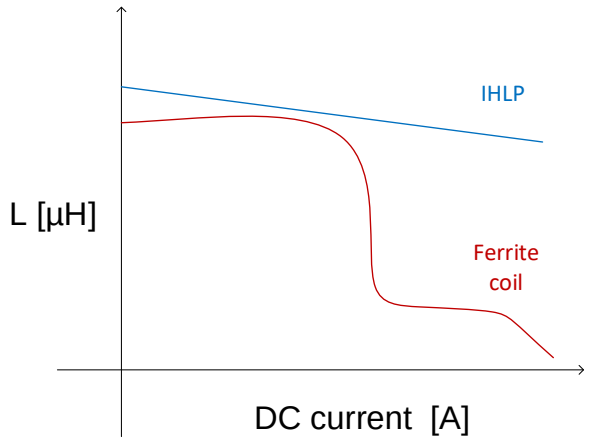

Figure 3.19: Saturation current of IHLP coils compared to traditional ferrite-based inductors

The design approach followed to size the inductor will be similar to that presented in [32], [33] and [34]. The maximum allowed current ripple will determine the amount of inductance required by the converter. Once this value is known, a specific model will be chosen from the commercially available series. Core losses will be estimated by calculating the peak flux density. The designer can then verify that the combination of core and copper losses yield a temperature rise of less than the maximum 125 °C operating temperature of the composite inductor. In addition, core losses should be limited to less than one third of the total losses to mitigate any aging effects associated with the powdered iron in the core [32]. Lastly, the peak current must be calculated in order to verify that it is lower than the saturation current provided by the datasheet.

As it has been derived before, the current ripple can be expressed:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT})\, D}{f_{SW}\, L} = \frac{V_{IN}\,(1-D)\, D}{f_{SW}\, L} \tag{3.104}$$

Let us focus on the worst case scenario value, which happens when the product $(1-D)\,D$ is maximum, that is, when $D = 0.5$:

$$\Delta I_L^{max} = \frac{V_{IN}^{max}}{4\, f_{SW}\, L^{min}} \tag{3.105}$$

To strike a compromise between output capacitor size and cost and inductor size, the worst case ripple ratio will be assumed to be 40 % [32]. This ratio is defined as the quotient between the amplitude of the AC and DC components of the coil current. The worst case value of this ratio will happen for the lowest output current that the converter can operate at:

$$\Delta I_L^{max} = 0.4\, I_{OUT}^{min} \tag{3.106}$$

Then, the minimum required inductance can be calculated:

$$L^{min} = \frac{V_{IN}^{max}}{1.6\, f_{SW}\, I_{OUT}^{min}} \tag{3.107}$$

Let us assume that the converter will operate at a frequency of 400 kHz. Substituting for the practical values:

$$L^{min} = \frac{25V}{1.6 \times 400kHz \times 1A} = 39.06\mu H \tag{3.108}$$

Since a tolerance of 20 % is given for IHLP coils, the commercial inductance required will be:

$$L = 1.2\, L^{min} = 46.88\mu H \tag{3.109}$$

This approach could also be applied to other switching frequencies as shown in table 3.11 (with 20 % tolerance taken into account). As expected, increasing the frequency at which the converter operate will allow us to use a lower inductance keeping the current ripple to its maximum. The size of the solution could be further optimized by having a look at different series. However, due to the rough specifications of the converter (this thesis work focuses on analyzing the feasibility of the concept rather than coming up with an optimized solution) a nominal inductance of 47 µH from Vishay's IHLP-6767GZ-11 series will be taken as the nominal option for further consideration.

f_{SW} [kHz]	L^{min} [µH]
100	187.5
200	93.75
300	62.5
400	46.88
500	37.5
600	31.25
700	26.79
800	23.44

Table 3.11: Minimum required inductance for different values of switching frequency

Having a look at the datasheet of the coil [29], two more aspects can be added on the performance of the chosen inductor. Figure 3.20 presents how the inductance varies with respect to the DC bias current. Increasing the current yields a lower effective value of inductance. For the maximum DC output current of 4 amps, the equivalent inductance equals 40 µH approximately. This value is far from both the saturation and the heat rating currents specified in the datasheet (shown in table 3.12). Two conclusions can be drawn from this: saturation will not take place; and the temperature rise will be much lower than 40 ºC. What is more, a DC current of 4 amps yields a temperature rise of less than 10 ºC according to figure 3.20. As for the variation of inductance with the switching frequency, it can be seen how the effective inductance stays roughly constant at its nominal value of 47 µH for frequencies below 1 MHz.

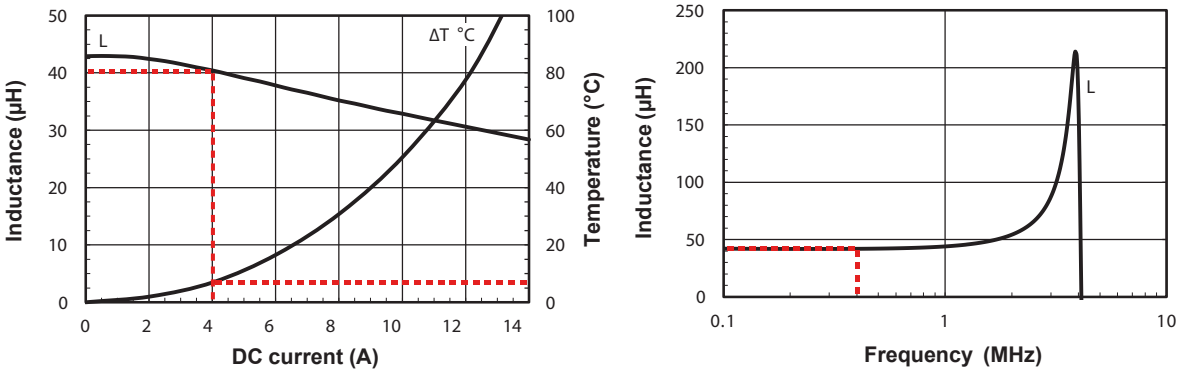

Figure 3.20: Inductance deviation with respect to DC current and switching frequency; temperature rise with respect to DC current

Once the value of inductance for the maximum DC output current is known ($L_{eff} = 40\mu H$), the maximum current $I_{L,2}$ taking the 20 % tolerance into account can be calculated (for a duty cycle equal

to 0.5):

$$I_L^{max} = I_{OUT}^{max} + 0.5\,\frac{V_{IN}^{max}}{4\,f_{SW}\,0.8\,L_{eff}} \tag{3.110}$$

Substituting:

$$I_L^{max} = 4A + 0.5\,\frac{25V}{4 \times 400kHz \times 0.8 \times 40\mu L} = 4.24A \tag{3.111}$$

The next step is to calculate the core losses of the selected coil. As described earlier, the MSE will be used for this purpose. The coefficients needed to estimate such losses can be obtained from [35] and are presented in table 3.12. Combining all previously defined expressions, the core losses can be expressed:

$$P_{core} = C_m \left(\frac{\pi^2\,D\,(1-D)}{2}\right)\left(\frac{2\,f_{SW}}{\pi^2\,D\,(1-D)}\right)^{\alpha}\left(\frac{V_{IN}\,(1-D)}{k_{COIL}\,f_{SW}}\right)^{\beta} \tag{3.112}$$

It can be seen how the largest core losses will be generated at the maximum input voltage (25 V). In addition, the winding losses can be estimated according to the expressions derived earlier in this chapter. On top of this, the equivalent DC resistance as a function of temperature can be estimated according to [32] as:

$$R_{wind,DC}(T_{amb}, \Delta T) = R_{wind,DC}(25^oC)\,\frac{234.5 + T_{amb} + \Delta T}{259.5} \tag{3.113}$$

Let us assume an ambient temperature of 50 ºC and a temperature rise of 10 ºC according to figure 3.20:

$$R_{wind,DC}(50C, 10C) = 42.7m\Omega \times \frac{234.5 + 50 + 10}{259.5} = 48.5m\Omega \tag{3.114}$$

Parameter	Value
I_{DC}^{sat}	8.6 A
I_{DC}^{heat}	8.7 A
C_m	700.37×10^{-6}
α	1.173
β	2.213
k_{COIL}	1.923×10^{-3}
$R_{wind,DC}(25C)$	42.7 mΩ
r	1.3 mm
ρ	1.68 x 10^{-8} Ω m
μ	4 π x 10^{-7} H / m
Temp. coeff	11.3 ºC / W

Table 3.12: Parameters used to analyze the inductor losses of the 47 µH coil from Vishay's IHLP-6767GZ-11 series

The coil losses are computed with the presented values for an input voltage of 25 V and shown in figure 3.21. Observing the total losses, the maximum occur for the maximum current of 4 A (approximately 0.7 W). According to the temperature coefficient of the device, this will yield a temperature rise of 7.9 ºC. This matches very well with the initial temperature estimation. The total temperature will be therefore well below the maximum value of 125 ºC, namely 57.9 ºC. The manufacturer also mentions in [32] that the core losses should be limited to one third of the total losses to mitigate any aging effects associated with the powdered iron in the core at elevated temperatures. Although this is not really the case of this application (high temperatures are not really reached) the core losses are always smaller

and only comparable to winding losses for the low-current range. For these points, the temperature rise will be almost zero and therefore the aging effects of the powdered iron will not be problematic at all.

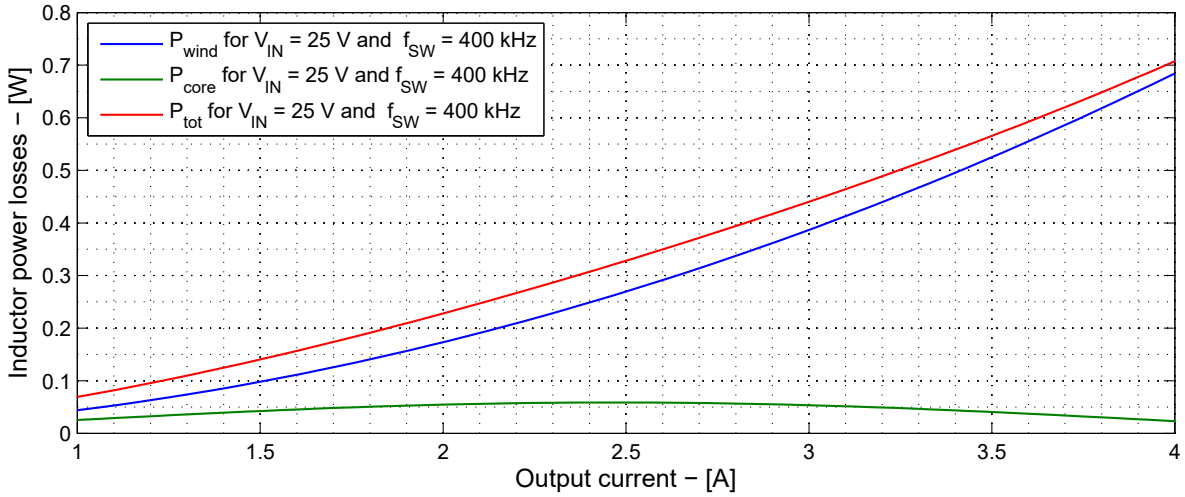

Figure 3.21: Estimated losses of the 47 µH coil from Vishay's IHLP-6767GZ-11 series according to table 3.12

3.6.2. Power switch

When selecting the switch for a buck converter, a series of parameters have to be considered to verify that a given device can be used in a specific application. These include the maximum continuous drain current, the breakdown drain-source voltage, the drain-source on-state resistance and the maximum gate-source voltage.

The maximum continuous drain current should be higher than the maximum output current of the converter. In this case, the maximum value of output current equals 4 A. What is more, the maximum current including the ripple current for the worst case scenario has been calculated earlier to be 4.24 A. This value can be easily handled by the DMOS implemented using Infineon's smart technology.

The breakdown voltage of the device has to be higher than the maximum expected peak voltage. This value will be closely related to the maximum input voltage, namely 25 V. On top of this, overshooting could take place due to the parasitic elements of the practical implementation and the voltage ripple. It will be assumed that these AC components are always lower than 20 % of the DC input voltage. That is, the maximum expected instantaneous voltage will be equal to:

$$V_{DS}^{max} = 1.2\, V_{IN}^{max} = 1.2 \times 25V = 30V \tag{3.115}$$

The DMOS used for this application can handle this amount of voltage during off-state since its breakdown voltage is larger than this value. As for the maximum gate-source voltage and the on-state resistance, these two parameters will be closely related to each other. The gate-source voltage applied to the DMOS will have to be below its maximum rating. For the converter presented in this thesis work, this voltage will equal 3 V. This value is below the maximum ratings tolerated for the DMOS implemented in Infineon's smart technology. The larger this voltage level, the smaller the resistance will be. Ideally, the equivalent resistance of the device should be minimized to keep conduction losses low. In fact, the equivalent resistance of the used DMOS equals 6.5 mΩ. It has been shown earlier that this value yields very small conduction losses for the current range of the converter.

Another important condition to verify that the DMOS can be used with the buck converter is related to the power dissipation. The package used to physically implement the switch on silicon is a PG-TSDSO-14-22. This will introduce a limitation regarding the maximum power that the switch can generate in order to properly operate the device keeping the temperature rise under control. This value has been roughly estimated to be in the order of 3 W. That is, the total losses of the power switch should be kept

below this value in order to guarantee safe temperature operation of the DMOS. Figure 3.22 depicts the total losses estimated in the switch for an input voltage of 25 V and a switching frequency of 400 kHz. It can be seen how the dynamic losses dominate over the conduction losses and how a power dissipation in the order of 3 W is generated for the maximum output current. It can be concluded therefore that the analyzed test-chip meets all requirements and can be therefore used in practice.

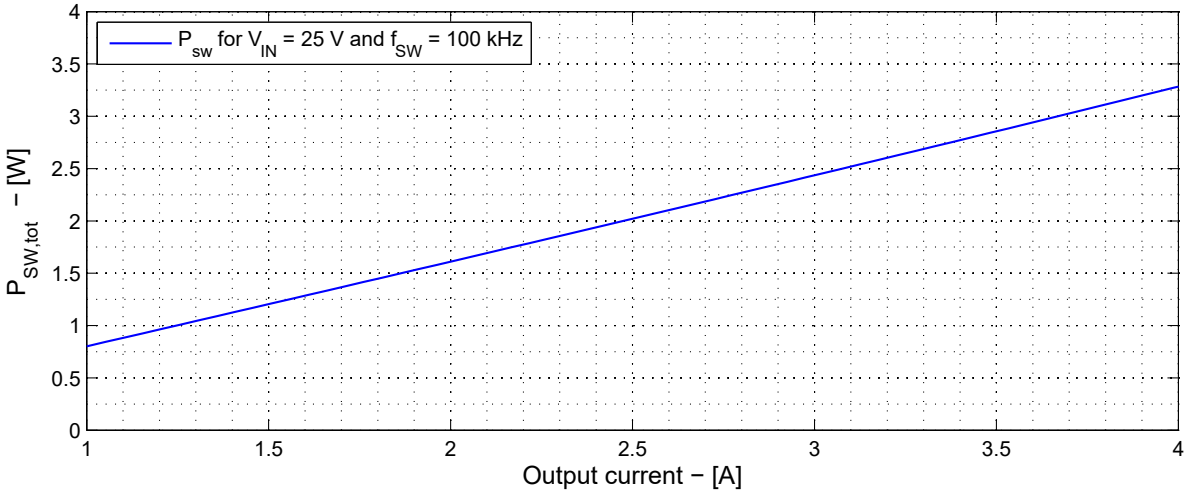

Figure 3.22: Estimated losses of the DMOS for an input voltage of 25 V and a switching frequency of 400 kHz

3.6.3. Diode

When selecting the low-side diode for the buck converters, four parameters should be considered: forward voltage drop, reverse breakdown voltage (peak and rms), average forward current and maximum power dissipation. Schottky diodes will be preferred and therefore the recommended choice. They are characterized by a low forward voltage drop, which reduces the power dissipation considerably [33]. Additionally, faster response compared to standard silicon diodes reduces diode switching losses which are actually neglected.

The schottky diode B560C from Diodes Incorporated [36] will be analyzed to determine whether it can be used for the buck converter of interest. The first values presented in the datasheet are the reverse breakdown voltage and the rms reverse voltage value, which equal 60 and 42 V respectively. As for the former, it is well above the maximum input voltage plus the allowed overshoot of 20 %, that is, 30 V. This mean that the low-side diode can withstand the DC voltage during the on-state. The later relates to the rms value of the blocking voltage. The rms value of this can be expressed as:

$$V_{D,rev}^{rms} = V_{IN}\sqrt{D} \tag{3.116}$$

The maximum would take place for the maximum duty cycle, which is still well below the maximum rating of 42 V_{rms}. The average forward current can be estimated using the following expression:

$$I_D^{avg} = I_{OUT}\,(1-D) \tag{3.117}$$

The maximum will take place for the minimum duty cycle, which in any case will be lower than the corresponding maximum rating of 5 amps. Once these requirements have been verified, the maximum power that the device can handled must be estimated in order to check whether the temperature rise that it would cause can be withstood by the diode. The expressions derived earlier in this chapter have been used to evaluate the losses of the B560C, which are depicted in figure 3.23. It can be seen how the maximum takes place at around 3 A with a value of 0.54 W. According to the datasheet, the junction temperature would be:

$$\Delta T_{J,A}^{max} = P_D^{max}\,R_{\Theta J,A} = 0.54W \times 50C/W = 26.8C \tag{3.118}$$

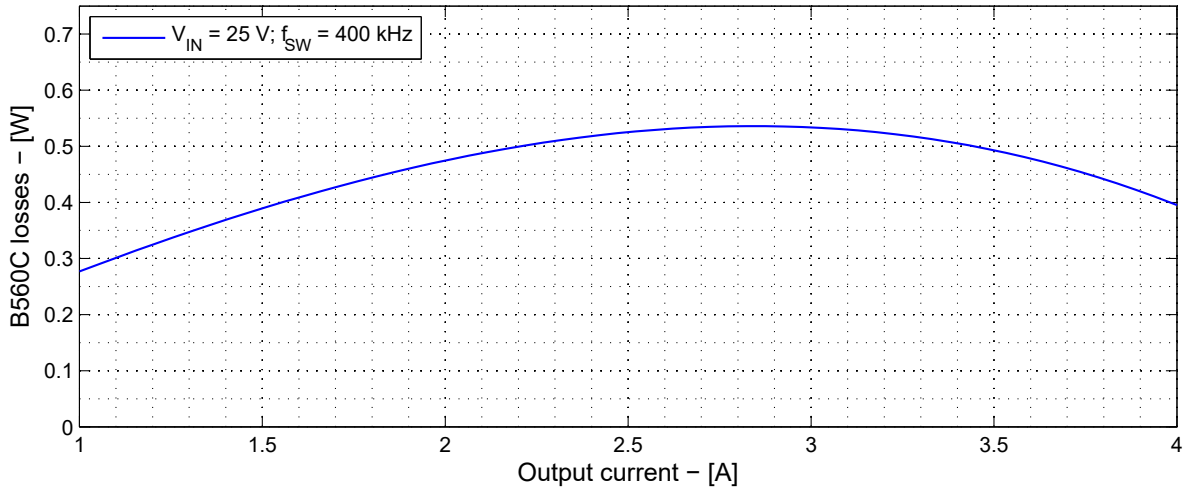

Figure 3.23: Estimated losses of the B560C diode for an input voltage of 25 V and a switching frequency of 400 kHz

That is, the diode junction will be at a maximum temperature of $T_J^{max} = T_{amb}^{max} + \Delta T_{J,A}^{max}$. This value will be below the operating temperature range specified in the datasheet, namely -55 to 150 ºC. It can be concluded then that the B560C from Diodes Incorporated is a suitable device for the application.

3.6.4. Input capacitor

Buck converters generate a pulsating ripple current with high di/dt at the input which are a source of electromagnetic interference. Without input capacitors, the ripple current will be supplied by the input power source. Parasitic resistance and inductance will cause high-voltage ripple that disrupts electronic devices, and the circulating ripple current will result in increased conducted and radiated electromagnetic interference. Input capacitors are required since they provide a path for ripple current and stabilize bus voltage during a transient events [37]. The input capacitor will have two main functions: provide the switching frequency current to the circuit to limit the ripple at the input and damp out the transient oscillations coming from the input power supply.

Multilayer ceramic capacitors (MLCC) are particularly good regarding filtering of the switching frequency ripple. They will effectively act as capacitors at the switching frequency and their equivalent series resistance is very low. Consequently, the ESR will be initially neglected to derive the minimum amount of capacitance needed at the input. Figure 3.5 shows the current through the input capacitor and the resulting voltage ripple. For these calculations it will be assumed that the coil current is constant. This way, the current through the capacitor will equal I_{OUT} - I_{IN} during the on-state and -I_{IN} during the off-state. This way, the ripple can be estimated as:

$$\Delta V_{IN} = \frac{(1-D)\,D\,I_{OUT}}{C_{IN}\,f_{SW}} \tag{3.119}$$

The worst case will take place for D = 0.5 and maximum output current:

$$C_{IN}^{min} = \frac{I_{OUT}^{max}}{4\,\Delta V_{IN}{}^{max}\,f_{SW}} \tag{3.120}$$

The desired maximum voltage ripple at the input will be 0.25 V:

$$C_{IN}^{min} = \frac{4A}{4 \times 0.25V \times 400kHz} = 10\mu F \tag{3.121}$$

In practice, capacitors present a tolerance due to manufacturing uncertainties which will be taken into account. Additionally, the effective capacitance will be affected by the DC voltage biasing and the operating temperature of the device. Let us focus on a commercial device from Murata's series GRM

[38]. The capacitor is rated 35 V with X7R dielectric and is packed in a 1210 size. Its tolerance is 10 % and the operating temperature goes from -55 ºC to 125 ºC. Having a look at the datasheet, it can be seen how the change rate for a DC bias voltage of 25 V (worst case) is 40 %. Then, the worst case scenario ripple after paralleling two of these devices would be:

$$\Delta V_{IN}{}^{max} = \frac{I_{OUT}^{max}}{4\,0.9\,0.6\,C_{IN}\,f_{SW}} = \frac{4A}{4 \times 0.9 \times 0.6 \times 20\mu F \times 400kHz} = 0.231V \tag{3.122}$$

That is, placing two capacitors in parallel meet the ripple requirements as for DC bias and tolerance. The maximum temperature rise can be estimated by determining the rms current that will go through the capacitors. Figure 3.24 shows the rms value of the input capacitor current for different parameters. It can be seen how the maximum current equals 1.62 A. According to the datasheet, this level yields a temperature rise of less than 1 ºC (assuming the current is shared equally by the two capacitors). Therefore, the capacitor can be considered to keep its rated value as for temperature derating.

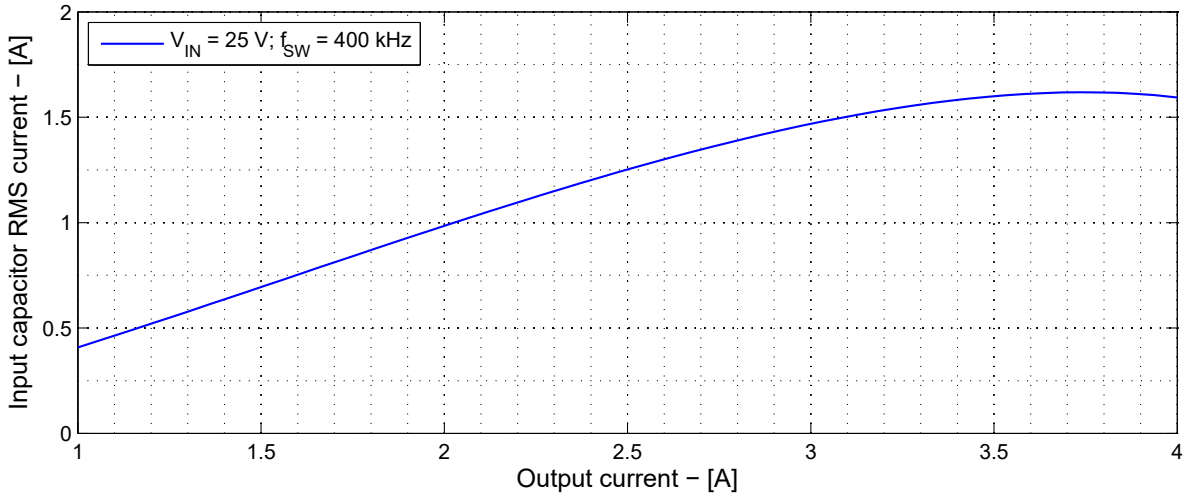

Figure 3.24: Input capacitor rms current for an input voltage of 25 V and a switching frequency of 400 kHz

The fast transition time during which the DMOS goes on and off leads to high di/dt slopes of the input current and high voltage spike at the input and switching node. The equivalent series inductance (ESL) of the ceramic capacitor plays a significant role in this respect. Thus, it is desirable to minimize the input capacitor ESL. This can be achieved by adding a small capacitor with low ESL. This parameter varies with material and structure, and as a general rule of thumb, the smaller the case, the smaller the ESL [37]. For this reason, a small 100 nF 0805 50 V X7R capacitor from KEMET [39] will be included in the design. Its effect on the efficiency can be neglected since the ESR will be extremely small, and it is added to the design to improve the transient response of the system.

While ceramic capacitors are excellent regarding filtering of ripple current at the switching freqeuncy, it will be necessary to meet further input voltage requirements related to transient response. Bulk capacitors with high capacitance are more cost-effective than ceramic capacitors. Aluminum electrolytic capacitors will be used for this purpose. There will be two key factors to select the input bulk capacitors: overshoot and undershoot requirement of transient response and allowable ripple current requirement of the bulk capacitor. The ESR of the bulk capacitor (ESR_{bulk}) and the capacitance (C_{bulk}) need to meet the transient response requirement.

Figure 3.25 depicts the idealized system response when a load step is applied to the output of the converter. The load step appears at the output and consequently the current through the coil i_L rises until it reaches the new DC operating point. The current carried by the switch i_{SW} is a chopped version of this coil current. Its average value could be approximated by the product of i_L and the duty cycle D [37]. On the other hand, the input power supply will deliver the current i_{PS} to the converter. The difference between the average switch current and the input supply current will have to be provided by the input capacitor. This will create a voltage transient which will add up on top of the DC input voltage value. There will be two main contributors to this transient: a voltage drop related to the ESR_{bulk} and a

voltage drop related to the capacitive behavior ($C_{bulk}\frac{dv_{IN}}{dt} = i_{C_{bulk}}$). The overall effect of the transient response should be lower than the undershoot or overshoot requirement.

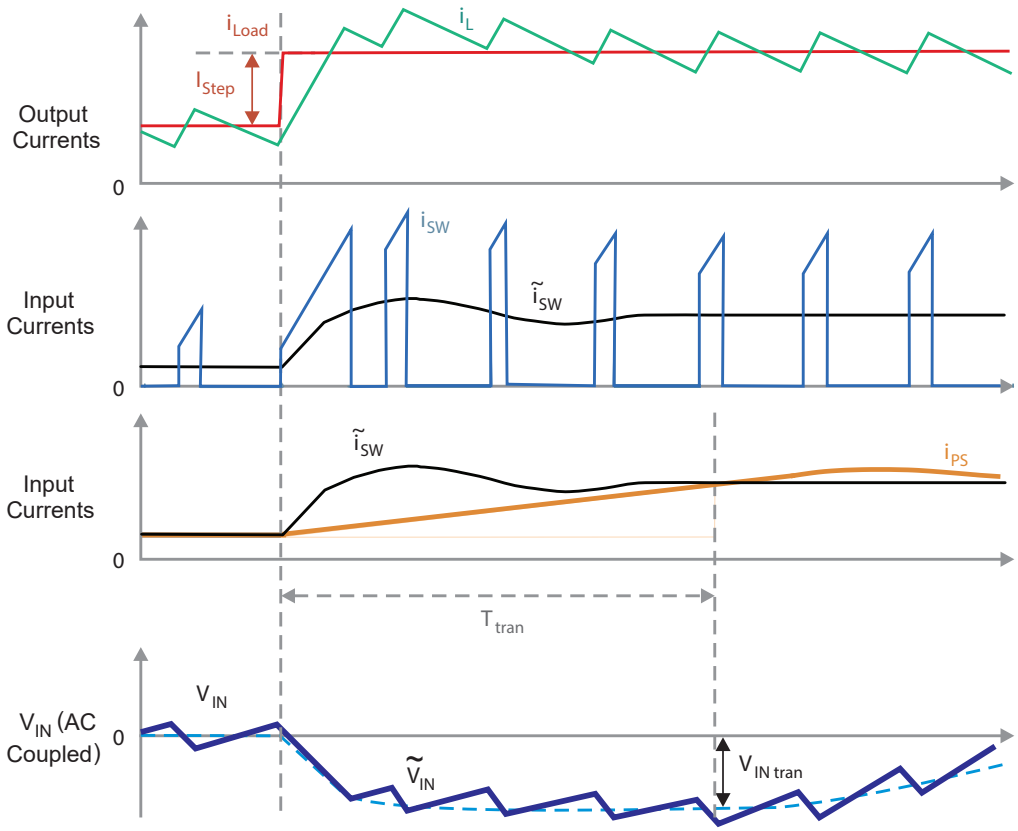

Figure 3.25: Idealized system response when a load step is applied to the output of the converter

The relationship between cycle average output and input current can be expressed as follows:

$$I_{IN} = D\, I_{OUT} \tag{3.123}$$

When it comes to a load step at the output, it will also appear at the input side:

$$\Delta I_{IN} = D\, \Delta I_{OUT} \tag{3.124}$$

The first requirement to the bulk capacitor will be related to its equivalent series resistance. The load step will create a current step which will be initially covered by the capacitor itself. This current will create a voltage drop proportional to both current and ESR which can be expressed in a simplified manner:

$$\Delta V_{IN,ESR} = ESR_{bulk}\, D^{max}\, \Delta I_{OUT} \tag{3.125}$$

This voltage drop will have to be lower than the overshoot or undershoot requirement:

$$ESR_{bulk} \leq \frac{\Delta V_{IN,tran}}{D^{max}\, \Delta I_{OUT}} \tag{3.126}$$

The second contributor is related to the capacitive behavior of the bulk capacitor. According to [37], the converter output-current rise time during a transient event, T_{tran}, can be approximated:

$$T_{tran} = \frac{1}{4\, f_{BW}} \tag{3.127}$$

Where f_{BW} is related to the control bandwidth of the converter. Let us assume that the charge demand during T_{tran} due to the current step will be supplied by both the power supply and the input capacitors. Then:

$$C_{IN}\,\frac{dv_{IN}}{dt} = i_{C_{IN}} \tag{3.128}$$

$$\Delta V_{IN} = \frac{1}{C_{IN}}\int_0^{T_{tran}} i_{C_{IN}}\,dt \tag{3.129}$$

$$\Delta V_{IN} = \frac{1}{C_{IN}}\,\frac{\Delta I_{OUT}\,D\,T_{tran}}{2} \tag{3.130}$$

The input capacitance required to meet the transient requirement can be then expressed as:

$$C_{IN} = \frac{\Delta I_{OUT}\,D\,T_{tran}}{2\,\Delta V_{IN,tran}} = \frac{\Delta I_{OUT}\,D}{8\,f_{BW}\,\Delta V_{IN,tran}} \tag{3.131}$$

The ceramic capacitors present at the input will contribute to the total capacitance. Therefore, the requirement related to the bulk capacitor can be expressed as:

$$C_{IN,bulk} = \frac{\Delta I_{OUT}\,D}{8\,f_{BW}\,\Delta V_{IN,tran}} - C_{IN,cer}\,k_{tol} \tag{3.132}$$

Parameter	Value
$\Delta V_{IN,tran}$	0.5 V
ΔI_{OUT}	2 A
D^{max}	0.8
f_{BW}	5 kHz
$C_{IN,cer}$	20 µ F
k_{tol}	0.54

Table 3.13: Parameters related to selecting the input bulk capacitor

The specific requirements for the input bulk capacitor are shown in table 3.13. The requirements can be calculated numerically:

$$ESR_{bulk} \le \frac{\Delta V_{IN,tran}}{D^{max}\,\Delta I_{OUT}} = \frac{0.5V}{0.8\times 2A} = 0.31\Omega \tag{3.133}$$

$$C_{IN,bulk} \ge \frac{\Delta I_{OUT}\,D}{8\,f_{BW}\,\Delta V_{IN,tran}} - C_{IN,cer}\,k_{tol} = \frac{2A\times 0.8}{8\times 5kHz\times 0.5V} - 20\mu F\times 0.54 = 69.2\mu F \tag{3.134}$$

A 100 µF 50 V aluminum electrolytic capacitor from Vishay's 160 CL [40] series meets the calculated requirements taking into account its 20 % tolerance. The allowable ripple current of this capacitor must be larger than that which will present at the converter. Electrolytic capacitors generally have an impedance that is much higher than that of ceramic capacitors used for ripple current filtering calculated earlier at the switching frequency (they will somehow act as a resistance whose value is equal to its ESR). It will be then assumed that the ripple voltage is not affected by the bulk capacitor. The idealized ripple current through the bulk capacitor can be approximated as a triangular waveform (it will proportional to the input voltage ripple). The bulk capacitor ripple current can be then expressed as:

$$I_{C_{IN,bulk}}^{rms} = \frac{\Delta V_{IN}^{max}}{ESR_{bulk}\,2\sqrt{12}} = \frac{0.231V}{0.12\Omega\times 2\times\sqrt{12}} = 0.28A \tag{3.135}$$

The rated rms current of the selected bulk capacitor is larger than the calculated value. Therefore, it can be used to meet all requirements related to the input voltage transients.

3.6.5. Output capacitor

The function of the output capacitor is to filter the inductor current ripple and deliver a stable output voltage. It also has to be ensured that load steps at the output can be supported by the output capacitors before the converter is able to react. Proceeding in the same manner as for the input capacitor, ceramic capacitors will be used to filter out the switching frequency ripple. As described in [41], the ESR of such capacitors can be initially assumed negligible to calculate ripple in a simpler way:

$$\Delta V_{OUT} = \frac{\Delta I_L}{8\, C_{IN}\, f_{SW}} \tag{3.136}$$

Let us assume that the output capacitor will be a combination of 10 µF devices used at the input. The worst case scenario will happen for the maximum ripple current, namely 0.4 A, and an output voltage of 20 V which yields a DC bias derating of 30 % in capacitance (on top of the 10 % tolerance). Besides, the maximum allowed voltage ripple will be 15 mV:

$$C_{IN}^{min} = \frac{\Delta I_L^{max}}{8 \times 0.9 \times 0.7\, \Delta V_{OUT}^{max}\, f_{SW}} = \frac{0.4A}{8 \times 0.9 \times 0.7 \times 0.015V \times 400kHz} = 13.2\mu F \tag{3.137}$$

That is, using two capacitors in parallel the voltage ripple requirement will be met. On top of the ripple due to the capacitive behavior, there will be some additional voltage drop due to the ESR. This can be approximated as:

$$\Delta V_{IN,ESR} = \Delta I_L\, ESR \tag{3.138}$$

The ESR of two devices in parallel will be in the order of 5 mΩ. Then:

$$\Delta V_{IN,ESR} = 0.4A \times 5m\Omega = 2mV \tag{3.139}$$

This value is small enough to make the previous selection still valid. As mention earlier, the transient requirement will also apply to the output voltage. When a load step takes place at the output, the inductor current will have to catch up to the new operating point. The load step will make the output capacitor supply the required charge to the output before the regulator adapts to the new load level. This will yield a voltage transient whose overall effect can be split up into two causes. The equivalent ESR at the output will create a voltage drop due to the peak current that the capacitor has to deliver. This will act as an upper limit to the ESR:

$$ESR_{bulk} \leq \frac{\Delta V_{OUT,tran}}{\Delta I_{OUT}} \tag{3.140}$$

Additionally, the time during which charge is supplied to the output by the capacitor will yield a voltage drop due to the capacitive behavior itself. According to [41], this voltage drop can be approximated as:

$$\Delta V_{OUT,tran} = \frac{{\Delta I_{OUT}}^2\, L}{2\, C_{OUT}\, V_{OUT}} \tag{3.141}$$

The requirement related to the capacitive drop yields:

$$C_{OUT}^{min} = \frac{{\Delta I_{OUT}}^2\, L}{2\, \Delta VOUT, tran\, V_{OUT}} = \frac{4A^2 \times 47\mu H}{2 \times 0.25V \times 5V} = 75.2\mu F \tag{3.142}$$

The ceramic capacitance present at the output will bring down this value (taking into account tolerances and DC bias):

$$C_{bulk}^{min} = 75.2\mu F - 20\mu F \times 0.9 \times 0.7 = 62.6\mu F \tag{3.143}$$

However, the tolerance of the bulk capacitor (typically 20 %) and other effects will make this value slightly higher. Therefore, an aluminum capacitor of 100 µF like the one selected for the input will be used at the output. The ESR requirement can be expressed numerically:

$$ESR_{bulk} \leq \frac{\Delta V_{OUT,tran}}{\Delta I_{OUT}} = \frac{0.25V}{2A} = 0.125\Omega \tag{3.144}$$

The ESR of the selected bulk capacitor is 0.12 Ω, so it can be concluded that it meets all requirements presented so far. Lastly, the rms current must be lower than the rated value specified in the datasheet:

$$I_{C_{OUT,bulk}}^{rms} = \frac{\Delta V_{OUT}^{max}}{ESR_{bulk}\, 2\sqrt{12}} = \frac{0.223V}{0.12\Omega \times 2 \times \sqrt{12}} = 0.26A \tag{3.145}$$

Which is below the maximum value for the passive device. On top of the selected ceramic and aluminum capacitors, an even smaller ceramic capacitor will be added to improve the higher-frequency response. This way, the impedance at the output can be kept low for a broader frequency range. No single value of capacitance could cover this frequency range due to internal parasitic inductance.

3.7. Overall efficiency of the converter

So far, the buck converter loss sources has been analyzed, modeled and estimated. In addition, a set of requirements have been presented to select commercially available options that will be part of the practical implementation of the converter. Once the different parts have been selected, the overall losses of the system and therefore the efficiency can be calculated. This will give an approximation of how energy efficient the system is. What is more, knowing the power losses of the converter will allow for its optimization efficiency wise. Other components could be selected if the solution is to be further optimized. The estimation presented hereafter will be assumed to be good enough as a first approximation to a solution which uses Infineon's smart technology. Table 3.14 shows the different parameters of the selected parts obtained from the datasheet that have been used to estimate the losses: the coil losses will be estimated as described earlier making use of the MSE; the DMOS losses will account for dynamic and conduction losses as mentioned in this chapter; the schottky diode will present losses due to the finite resistance of the silicon; and the capacitor losses will be estimated by making use of an equivalent series resistance of all capacitors used at both input and output.

Figures 3.26, 3.27, 3.28 and 3.29 present the efficiency estimation for different input voltage values with respect to the output current level using the parameters from table 3.14. The converter parts has been sized for a switching frequency of 400 kHz. However, the efficiency has also been estimated for lower values of this parameter to get an overview on how it affects the power losses. The points plotted are those who guarantee continuous conduction mode and which are realizable with a gate current level of 100 mA. The first point to notice is the output current range (equivalent to duty cycle range), which is different for each switching frequency. Increasing this parameter will yield an increase in the current range allowable due to the lowering of the current ripple (CCM will be guaranteed for lower current levels). However, the opposite effect will also take place due to a stretching of the switching period. Both effects will play a role in opposite directions and the overall current range will be determined by these two aspects together.

Parameter	Value
L	47 µH
C_m	700.37×10^{-6}
α	1.173
β	2.213
k_{COIL}	1.923×10^{-3}
$R_{wind,DC}$	42.7 mΩ
r	1.3 mm
ρ	1.68 x 10^{-8} Ω m
μ	4 π x 10^{-7} H / m
$t_{ON,1}$	20 ns
$t_{ON,2}$	60 ns
$t_{OFF,1}$	60 ns
$t_{OFF,2}$	20 ns
$V_{GS,on}$	3 V
$R_{DS,on}$	6.5 mΩ
R_D	50 mΩ
V_D	0.3 V
$C_{IN,cer}$	20 µF
$C_{IN,bulk}$	100 µF
$ESR_{C_{IN}}$	0.15 Ω
$C_{OUT,cer}$	20 µF
$C_{OUT,bulk}$	100 µF
$ESR_{C_{OUT}}$	0.15 Ω
R_{OUT}	10 Ω

Table 3.14: Parameters used to estimate the converter efficiency

The second effect that can be observed is the variation of efficiency with respect to the input voltage level for a given output current level. The main contributors to this will be dynamic switching, diode and core losses. The former have been presented earlier in this section, and it can be seen how they are directly proportional to the input voltage. As for the diode losses, the term related to the voltage offset will be directly proportional to the input voltage level. Core losses will increase with input voltage due to the peak flux density becoming larger. All in all, it is shown how increasing the input voltage level yields a lower efficiency for certain output current.

The switching frequency also affects the overall efficiency of the system. The main cause of this variation are the dynamic switching losses. As discussed earlier, the switching losses generated in the DMOS will be directly proportional to this parameter. Therefore, increasing the switching frequency will cause an increase in the switching losses since more transitions will take place per unit of time. Conduction switch, diode, winding and capacitor losses will be hardly influenced by this change. However, core losses will be affected by the switching frequency at which the converter operates. Since the β coefficient is approximately twice the α coefficient, increasing the switching frequency will bring down core losses to half of its value.

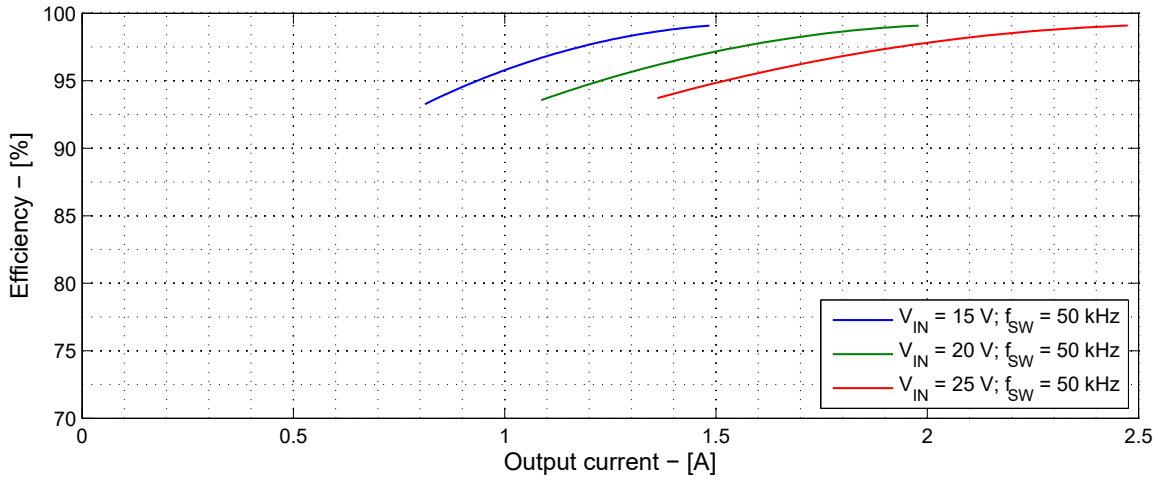

Figure 3.26: Overall estimated efficiency of the converter for a switching frequency of 50 kHz using the parameters presented in table 3.14

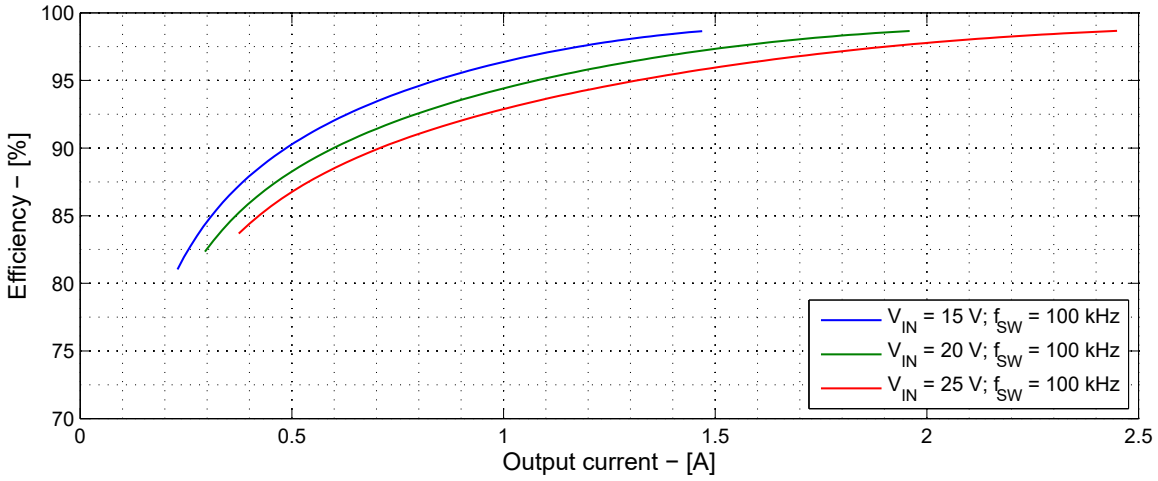

Figure 3.27: Overall estimated efficiency of the converter for a switching frequency of 100 kHz using the parameters presented in table 3.14

On top of the mentioned parameters which affect the efficiency, it can be observed how this considerably drops for small values of output current: the higher the output current, the higher the efficiency. The main reason of such tendency are the dynamic switching losses. Low current operating points are characterized by a low power handling of the converter. The ratio between switching losses and total delivered power for these points is larger than that obtained for higher current. If a smaller DMOS were used, switching losses could be made smaller and the efficiency would be significantly better for the low power region. Also, it can be inferred that the efficiency will be better and better for higher currents until conduction losses in the DMOS become comparable to dynamic losses.

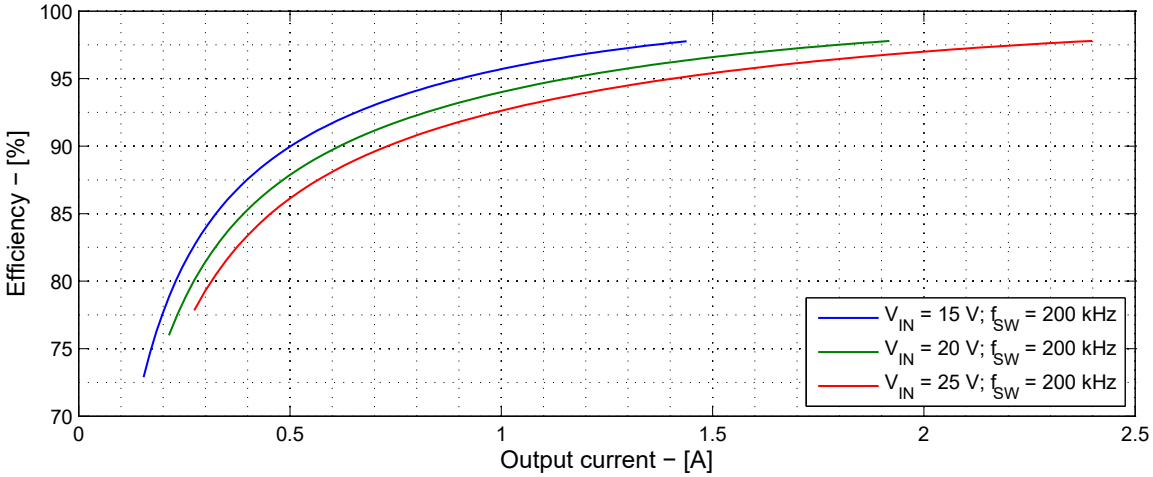

Figure 3.28: Overall estimated efficiency of the converter for a switching frequency of 200 kHz using the parameters presented in table 3.14

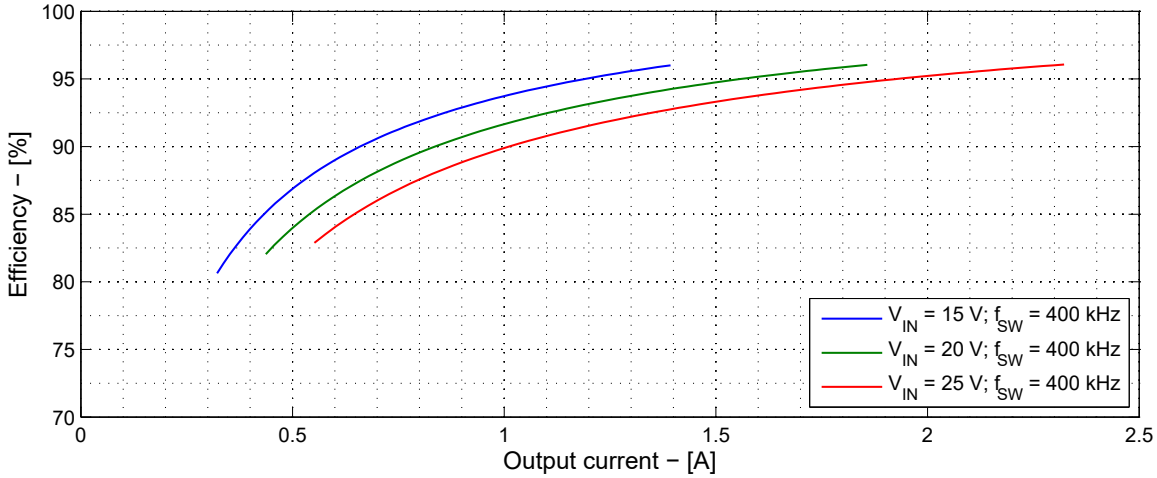

Figure 3.29: Overall estimated efficiency of the converter for a switching frequency of 400 kHz using the parameters presented in table 3.14

3.8. Conclusions and remarks

The study presented in this chapter has been based on idealized waveforms of the buck converter. In practice, the measured waveforms will not fully match this approximation. What is more, all parameters that have been been assumed a constant value will present some kind of variation with time and other unmodeled phenomena. However, the actual waveforms will be very close to those estimated from the approach presented in this chapter and the power loss estimation can be considered accurate enough with respect to what will be obtained in practice.

It has been mentioned that only condtinuous conduction mode has been considered to design and size the converter. Discontinuous conduction mode presents a series of advantages and disadvantages with respect to CCM. For instance, the switching losses will be minimized since a soft-switching operation can be inherently achieved. On the other hand, higher rms currents will be needed to transfer the same amount of power. All in all, losses will present a slightly different distribution which could be more suitable for low power operating points. This will be out of the scope of this thesis work since the approach presented here consists of a feasibility study to evaluate the suitability of Infineon's smart technology for DC/DC applications.

It must be also mentioned that the dimensioning of the LC filter is not optimum. The criteria followed take into account general aspects of the converter operation rather than a specific application where the boundary conditions would be well defined. The goal of the analysis presented in this chapter is to design a prototype of the system to further develop the DC/DC concept using Infineon's smart technology. Future work would include a more specific optimization and characterization of the components.

4

Implementing the high-side driver

The fourth chapter of this document elaborates on the practical realization of the high-side gate driver. Section 4.1 introduces the floating gate driver concept that will be analyzed in this chapter. Two different systems which could be potentially suitable for this application are available at Infineon. System A, a DAC-based current source, is explained in detail in section 4.2. The concept, main properties and limitations of this approach will be presented there. The following section (4.3) focuses on system B, an active-feedback-amplifier-based current source. Again, its working principle and main limitations will be analyzed in detail. Once the two different systems have been introduced and studied, a comparison between them is presented in section 4.4 to summarize the selection criteria and justify the final choice. Section 4.5 addresses the practical aspects of the implementation: measurements obtained with two different switches will be shown and discussed. Both theoretical and practical aspects will be reviewed in section 4.6 in the form of final conclusions. These will be used as the starting point for the next chapter of this document, which will focus on the optimization of the converter prototype as a whole.

4.1. Floating driver concept

It has been mentioned before that the DMOS will be placed at the high-side position of the switching leg of the back converter. The low-side device will be a schottky diode which, unlike the high-side switch, can only conduct when the surrounding circuits allows it. The DMOS can be turned on and off actively at any moment of time desired by the user or, in a practical case, the control circuitry. The conditions that must be guaranteed for this purpose are related to the voltage present between the gate and source terminals of the switch. If the DMOS is to be turned on, this voltage must be larger than certain threshold value. How much overdrive is applied with respect to this threshold will influence the equivalent resistance of the silicon; if the switch is to be turned off, the gate-source voltage must be brought to a value lower than the threshold. The circuit used for this purpose will be the gate driver.

The main feature of the high-side driver that will be required is that it will have to be floating with respect to the power ground of the buck converter. When the switch is on, the source terminal will be ideally equal to the input voltage. That is, the gate voltage must be above this value in order to meet the requirements to turn the DMOS on. On the other hand, when the switch is off, the source terminal will be ideally at zero volts (directly tied to power ground through the low-side diode). Therefore, the gate driver must supply a voltage at the gate of the DMOS lower than the threshold with respect to power ground. In other words, it can be said that the reference voltage of the gate driver, namely the source terminal, will present a floating chopped form due to the working principle of the buck converter. The gate driver circuitry must be able to supply the required voltage at the gate depending no matter what value is seen at the source of the switch.

The prototype of the converter that will be designed in this thesis work will make use of a gate driver that fulfills these specifications. It must be able to operate at the desired switching speed, and at the same time it must deliver the required amount of current to the DMOS so that its switching transitions will be fast enough. As a first step, such driver will have the form of a PCB with discrete components.

The goal will consists in verifying that the DMOS implemented using Infineon's smart technology can be used for DC/DC lighting applications. In addition, a concept for the gate driver can be analyzed and studied for further product development. The ultimate target is to integrate the driving concept on silicon by making use of Infineon's smart technology. This way, the whole package would include both the power switch and the required circuitry to turn it on and off. Additionally, other features related to protecting and sensing could be implemented along in the solution.

The two following sections of this chapter present two different systems available at Infineon Technologies. These were developed and used for applications with very different boundary conditions. Therefore, their suitability for DC/DC lighting applications must be first analyzed. Once both systems are characterized and their limitations are known, a comparison can be made in order to determine which suits the application of interest best.

4.2. Interaction between the gate driver and the dSPACE system

Rapid Control Prototyping was firstly presented in the introductory chapter of this document. The specific interaction between the dSPACE and the gate driver system will be discussed in more depth hereafter. As a summary, the dSPACE device used makes use of an FPGA-based system that contains digital input/output channels, ADCs and DACs. This FPGA will be used along with an extension module that provides the system with additional peripheral channels (extra digital input/output channels, ADCs and DACs). The FPGA will by mastered by a PowerPC control unit which is programmed by the user making use of a block approach on MATLAB Simulink. The software will translate the block design into C code for the microprocessor unit and into VHDL code for the FPGA.

The user will then have to program the control scheme of the converter using this approach and in the end, such control must culminate in signals that will be sent/read to/from the gate driver system via the FPGA peripherals. This communication can be in both directions: if a signal is to be read from the converter to apply certain control law, an ADC channels will be used to bring the analog signal into a digital value that can be used by the dSPACE to control the converter; if an analog signal is to be sent to the gate driver to apply certain control action to the converter, a DAC channel will be used; if a digital binary signal is required to operate the converter (dictated by either the gate driver or the dSPACE) and input/output digital channel will be used. It must be noted that certain delay will take place when the interaction takes place. Depending on the nature of this intercommunication, such delay can be neglected (if the speed at which it happens is much lower than the delay time) or must be taken into account (if the speed is comparable to the delay time).

4.3. System A: DAC-based current source

The first driver concept that will be presented in this chapter is a DAC-based current source, hereafter named system A. This approach was used in the early development phase of products that made use of previous Infineon's smart technologies. The switching frequencies that this driver aimed to achieve were in the order of 5 kHz, with a current level in the range of 1 mA. It can be seen then how the boundary conditions for which this system was designed are significantly different to those required for the application of interest analyzed in this thesis work.

Figure 4.1 shows the concept drawing of system A as a whole. The different functions are grouped in shaded areas while the discrete ICs used are shown as interconnected blocks. The drawing includes all the elements present on the PCB, but only some of them will be used in practice for the application of interest. Therefore, only the modules that are strictly necessary to operate the gate driver for the buck converter presented in this document will be discussed in detail. Temperature, current and voltage measurement units will not be used. The board is designed to drive a two-gate switch, but it can also be used for a single gate by paralleling the two available channels with twice the amount of allowed current. This system is designed to operate along with the dSPACE system as presented in the earlier section. A DIN connector will be present on the board that will connect all dSPACE terminals to the PCB.

Firstly, system A includes a supply conditioning and level shifting stage that will be connected to a 5 V input power supply. It will make use of an LDO (LP3990MF-3.3 [42]) that generates 3.3 V from

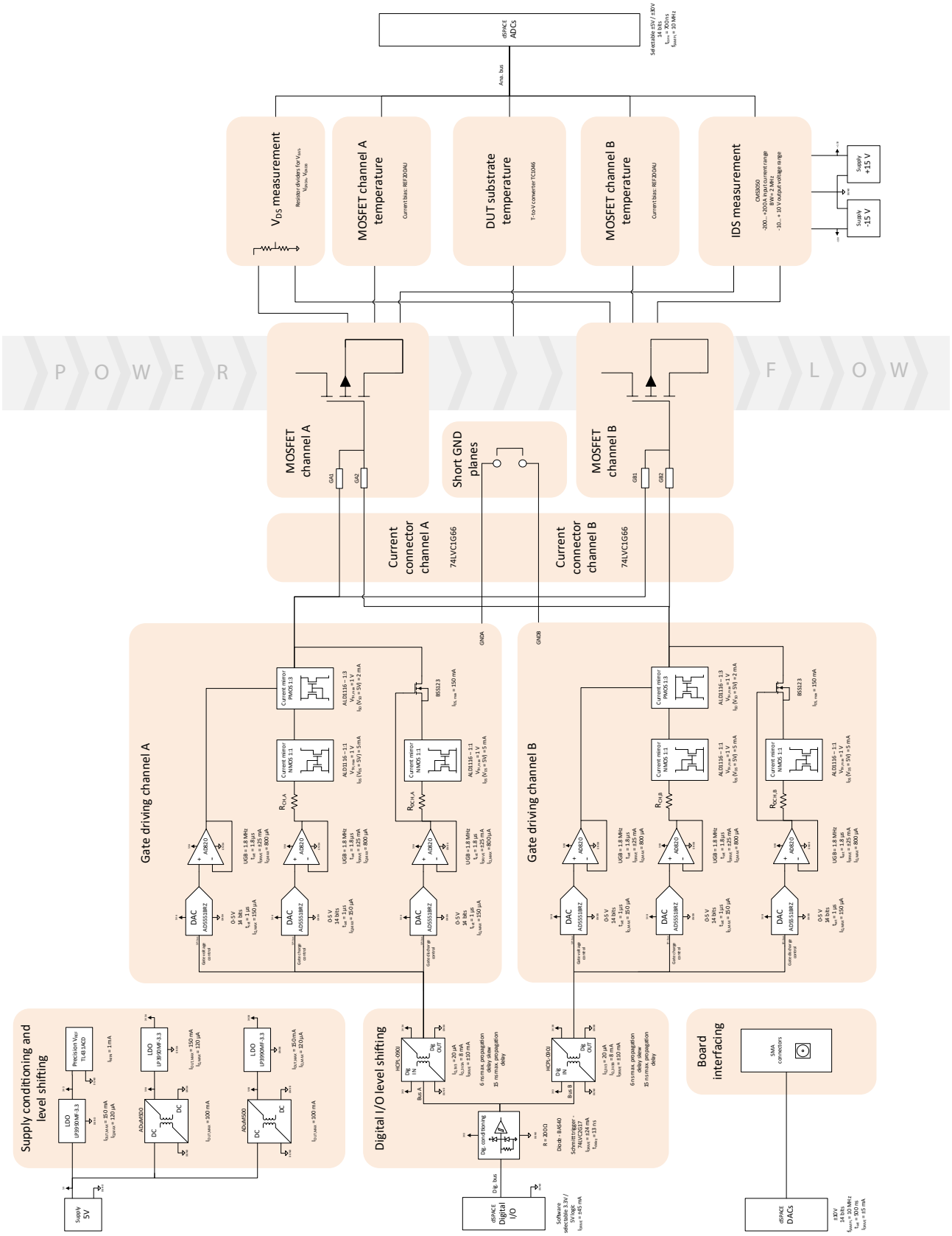

Figure 4.1: Concept drawing of system A, a DAC-based current source

the input power supply. This reference will be connected to a precision programmable reference IC (TL431ACD [43]) that will regulate the output of the LDO to a precise value dictated by a resistor divider. Two isolated DC/DC converter ICs (ADuM5000 [**?**]) will be connected to the input power supply to generate galvanically isolated 5 V domains (5VA and 5VB). These will power again two LDOs to obtain 3.3 V with respect to the isolated references (GNDA and GNDB). These 5 V and 3.3 V domains will be therefore floating with respect to the power ground to which the input power supply will be connected. The main limiting factor of this stage will be related to the maximum current that can be handled by each DC/DC converter. According to the datasheet, this maximum current equals 100 mA.

The digital input and outputs of the dSPACE will be conditioned and protected my making use of terminating resistors (200 Ω) and zener diodes (BAS40-04 [44]) that will limit over and undervoltages that might appear at these points. Schmitt trigger ICs will be added afterwards to filter and improve the digital signals (74LVC2G17 [45]). There will be 15 signals in total: four of them will be related to the charging and discharging of each channel; two of them, to the voltage charging level of each channel; two of them, to to dynamically interconnect the two floating grounds; one of them, to act as the clock signal of the SPI bus; and six of them to act as chip select signals for each DAC IC. Each of these signals will be connected to a channel of a high-speed digital isolator (HCPL-090J [46]) that will move the ground-referenced signals to the floating references GNDA and GNDB. The main limiting factor of this part of the driver will be related to the speed at which the digital isolators can work at. According to the datasheet, the maximum delay propagation times will be 15 plus 9 ns. These time can be assumed to be negligible compared to the desired switching frequency that is to be achieved (these times would be 1 % of the total switching time required for 400 kHz).

The working principle of this concept relies and DAC ICs (AD5551BRZ [47]), 14-bit precision devices that are controlled via SPI. This approach is used to provide the final implementation with versatility. This way, concepts in the early development phase can be tried out and tested under different conditions. Each DAC will be connected to a digital signal which will set the analog voltage at its output (charging, discharging and voltage level of each channel), to a chip select signal and to the SPI clock. All of them will come from the digital isolators and therefore the DACs will operate with respect to the floating references GNDA and GNDB. The output of the DACs will be buffered by an op-amp in voltage follower configuration (AD820 [48]). The limitations of this stage will be related to speed at which the ICs can effectively operate and the current they can carry. As for the former, the DACs have a settling time of 1 µs and the op-amps have a unity gain bandwidth of 1.8 MHz and a settling time of 1.8 µs. These values could be allowed but the proper operation of the driver would have to be cross checked in practice. As for the current capability, the op-amps can deliver or sink a maximum current of 25 mA. As it will be discussed later, these ICs will serve as the input current source of current mirrors. If a current level of 100 mA were to be realized, a multiplication factor or paralleling of the two channels would be required.

The output of the op-amps will be connected to NMOS current mirrors realized using discret transistors that come matched within a single package (ALD1116 [49]). Therefore, the precision of the circuit will be assumed good enough. As it has been mentioned earlier in the document, a PMOS mirror (realized using ALD1107 [50]) will be needed to reverse the direction of the current and allow for charging of the gate. Additionally, the voltage level up to which the current mirrors act as so can be set by a DAC. In summary, the op-amps together with DACs set the charging and discharging current level for each channel, and the voltage up to which the gate is charged can be defined as well with a combination of DAC and op-amp. The concept is the same for both channels. The limiting factor of this part of the circuitry will be related to the transition times of the transistors and the maximum current they can carry. Having a look at the datasheet, the maximum rating for the specific operating conditions of the transistors is 5 mA for the NMOS devices and 2 mA for the PMOS devices. Therefore it can be concluded that these driver circuit could not be used to deliver a gate current level of 100 mA unless several boards were operating in parallel.

4.4. System B: active-feedback-amplifier-based current source

The system described in this section, hereafter system B, was initially developed to drive Infineon's OptiMOS family of switches at a switching frequency up to 20 kHz. It allows for dynamic setting of the current since it was originally designed to be able to control the gate current shape and slope to optimize

the switching behavior of the power MOSFET. However, the initial design did not consider operation for higher frequencies. Therefore, an initial analysis must be carried out to determine whether the system could operate at the desired switching frequency of 400 kHz, delivering the required gate current level of 100 mA.

Figure 4.2 presents the concept drawing of system B. This will be enough to understand and justify its selection as a suitable solution for the application of interest. Like system A, the concept drawing groups the different functions of the driver in shaded areas while the discrete ICs used are shown as interconnected blocks. The initial design includes both low and high-side driver, but only the latter will be used. Although it is shown in the concept drawing, the following discussion will not present any details about it since it is not necessary for the buck converter. System B also includes an IC to guarantee safe insertion and removal of the device under test, but it will be bypassed since it is not of interest to this application. It also includes a line impedance stabilization network (LISN) to create a known impedance and to provide a radio frequency noise measurement port that will not be used for this thesis work and therefore will be omitted.What is more, voltage and current measurement units available at the board will not be used either. The device under test will be connected to the driver PCB through a DIN connector. The dSPACE will be connected to the driver board as well and it will interact with the system through digital inputs/outputs, ADCs and DACs.

5 power supply channels will be required to operate the high-side driver circuit of system B. Firstly, two channels must supply +15 and 15 V with respect to power ground. Several LDOs will be used to generate other voltage levels: an LM2940 [51] will be used to obtain+12 V from +12 V; an LM2990 [52] will be used to generate -12 V from -15 V; an LM317MSTT3 [53] will be used to generate -6 V absoluto from -12 and +12 V; another LM317MSTT3 will be used to generate +5 V from +12 V; another LM317MSTT3 will be used to generate -7 V absolute from -12 V. A power supply with an input voltage of -12 V will have to be connected to the -12 V port (generated by the LDO) to generate -24 V with respect to the absolute ground (PGND). Overall, several voltage domains will be generated from 3 input power supply channels by making use of LDO ICs. These voltage levels will be used by other ICs present on the driver board. In addition, two power supply channels will be used to generate the two floating voltage domains: the COM terminal of this source will be connected to the source terminal of the DMOS and +12 and -12 V will be used to power the ICs that operate in this voltage domains.

The high side driver will interact with the dSPACE in the first place via 2 DAC channels. These can generate a voltage between +10 and -10 V with 14-bit resolution. The sampling frequency of this peripheral is 10 MHz and the settling time is 10 ns according to the datasheet. According to these specifications, the DAC will be able to operate at the desired speed with enough accuracy. The voltage generated by the dSPACE will be conditioned at the driver PCB and connected to the first active-feedback amplifier of the PCB. The operating principle of this IC can be simplified as a differential amplifier that is able to generate an output voltage with a specified offset. The IC used will be an AD8130 [54] followed by a push-pull configuration using 2SCR293P (npn) [55] and 2SAR293P (pnp) [56]. According to the datasheets, the amplifier will have transition times which are compatible with the aimed switching speed (settling time of 20 ns, rise time of 1.7 ns, fall time of 1.4 ns). As for the npn transistor, it will present switching times that are fast enough as well: on time of 90 ns, fall time of 60 ns; the pnp transistor will have similar characteristics: on time of 60 ns and fall time of 50 ns. The current capability of these devices will be above that needed to operate the gate driver as needed: a collector current of 0.5 A can be carried for a base current of 25 mA (the active feedback amplifier which supplies the bases of the transistors can deliver up to 40 mA).

The first active-feedback amplifier will be used to translate the input voltage given by the DAC to an output current created by the voltage drop across a known resistor. The DAC can effectively apply a differential voltage at the input of the amplifier between -2 and +2 V. If this voltage equals +2 V, a current of 100 mA will be generated at the output of the amplifier. This current will be connected in series to another resistor which will create a voltage drop with respect to the -12 V domain. This way, the DAC voltage level can be transferred from the dSPACE domain to a lower voltage level. Again, an active-feedback amplifier will be used to generate a DAC-controlled current. That is, the DAC voltage imposed by the dSPACE will be transfer into a reference current by the driver PCB.

A digital input/output channel of the dSPACE will be used to determine whether the driver has to charge or discharge the gate of the switch. Such digital signal will be connected to a digital isolator to shift the voltage level from the dSPACE domain towards the domain with respect to -12 V present

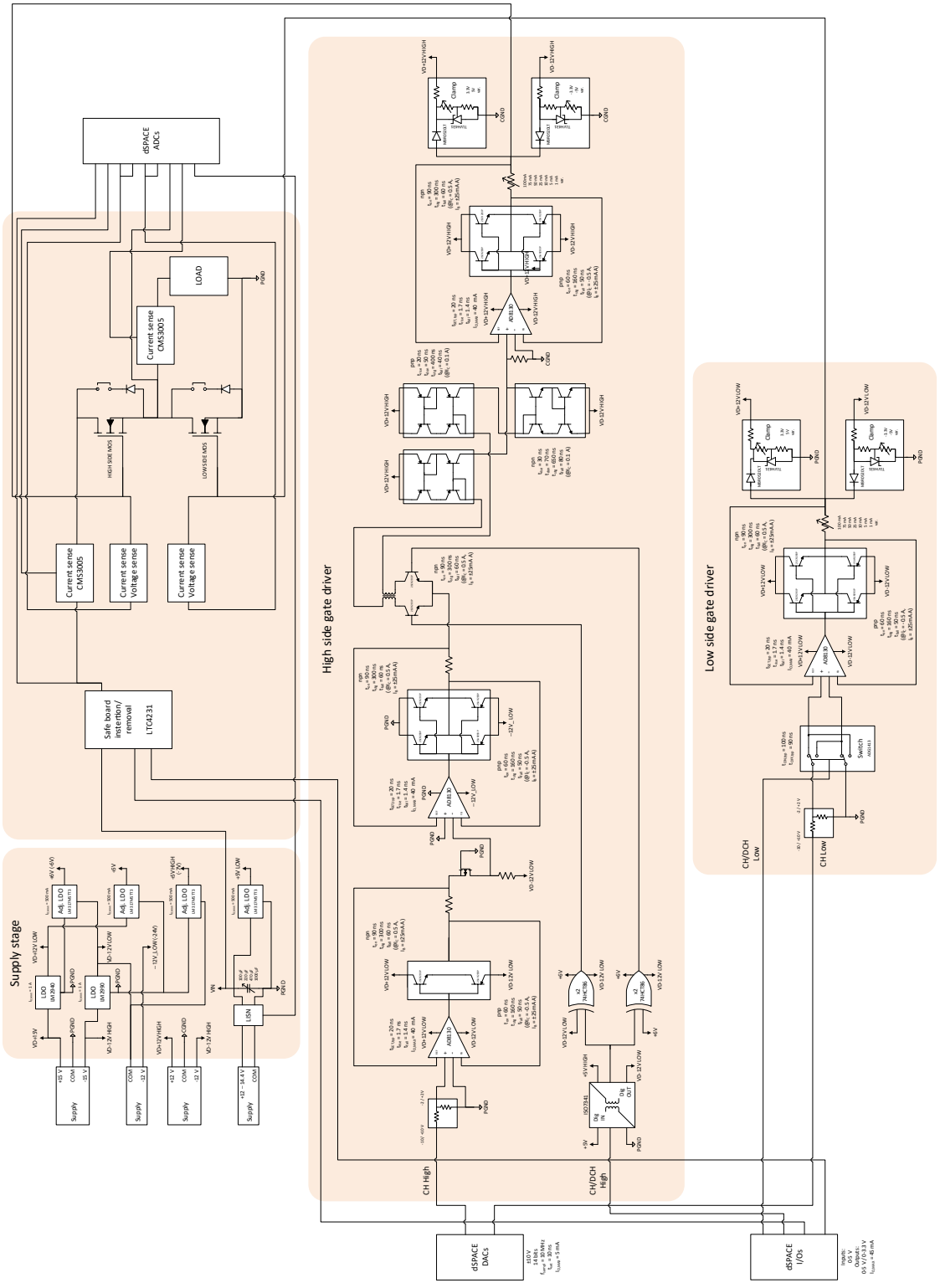

Figure 4.2: Concept drawing of system B, an active-feedback-amplifier-based current source

at the board. The output of the isolator will be connected to an XOR gate IC that will be used to drive two npn transistors (2SCR293P). These will chop the internal reference current generated by the driver into two different signals: whenever the dSPACE tells the driver to charge the gate of the switch, only the transistor associated to the charging branch will conduct; whenever the dSPACE tells the driver to discharge the gate of the switch, the opposite transistor associated to the discharging branch will conduct. This way, the dSPACE system will be able to control the duty cycle of the converter.

The reference current has been so far split into a charging and a discharging branch. These two currents will be connected to current mirrors that will duplicate the current in the floating domain that will be used by the DMOS. The charging branch will make use of a single current mirror implemented with pnp matched transistors (QST9 [57]); the discharging branch will make use of a pnp mirror (implemented with QST9) and an npn mirror (implemented with QSX8 [58]) to revert the direction of the current and allow for discharging of the gate. The overall output current will create a voltage drop with respect to the floating reference. Its shape will be ideally a bipolar square waveform with a duty cycle coincident to that of the converter given by the dSPACE. The main limitations of this stage will be related to the speed at which the mirrors are able to replicate the current and the maximum current rating. According to the datasheet of the pnp transistors, a current of 100 mA can be carried with the following transitioning times: rise time of 20 ns, delay time of 50 ns and fall time of 40 ns. As for the npn transistors, these times will be similar: rise time of 30 ns, delay time of 70 ns and fall time of 80 ns. It can be seen how these times are much smaller than those needed to switch the converter at a frequency of 400 kHz.

The following part of the circuit will be based again on an active-feedback amplifier that will drive the output voltage created by the current mirrors to a double push-pull stage. This way, the current driving capability will be guaranteed. A known resistor will be placed to determine the amount of current that correspond to the amplified voltage. This way, the current level can be easily adjusted by the equivalent resistance seen at this point. Lastly, a clamping stage will be used to limit the voltage until which the transistor is charged and discharged. The clamping circuit will consist of a voltage reference IC (TLVH431 [59]), a variable resistor and a schottky diode (MBR0520LT [60]). The variable resistor can be adjusted by the user to generate a stable voltage reference out of the TLVH431. The schottky diode will be connected between the gate of the switch and the generated voltage level in such a direction that it will conduct and clamp the gate voltage once the reference value is reached. This way, the user can determine the on and off state gate-source voltage level.

4.5. Comparison between System A and System B

	System A	**System B**
Power supply channels	1	5
dSPACE DAC channels	0	1
dSPACE digital I/O channels	7 + 1	1
Voltage level set by	Software	Hardware
Current level set by	Software	Hardware / Software
Current capability	2 mA per channel	100 mA
Switching frequency capability	20 kHz	1 MHz

Table 4.1: Simplified comparison between driver circuits of system A and B

Once both systems have been presented and their working principle and limitations have been discussed, a simplified comparison is shown in table 4.1. The first aspect that can be compared is the number of power supply channels required: system A is very simple in this regard and only needs one input power supply of 5 V; system B is more complicated and requires more external power supplies, namely 5. System A does not make use of any DAC channel of the dSPACE system. The DAC devices are embedded on the driver PCB itself and they are controlled by the dSPACE via SPI. On the other

hand, system B makes directly use of a DAC channel to indirectly set the internally generated reference current. As for the number of digital inputs/outputs, system A requires 7 signal lines per channel to control the DACs via SPI on top of the extra line needed to implement the SPI clock. System B is more simple in this respect, and it only uses one single digital input/output channel to set the charging or discharging operation of the driver.

The voltage level at which the gate of the DMOS is charged is also a degree of freedom in the driving process. System A allows dynamically setting this value via software (that is, the dSPACE) since it will be adjusted by one of the SPI-controlled DAC devices. On the contrary, system B only allows for a static configuration via hardware of the charging voltage level. This can be done by trimming the variable resistor that is present in the clamping circuit described earlier. Additionally, the current level at which the driver charges and discharges the gate of the switch can be changed. With system A, this value can be set again via software by means of the SPI-controlled DAC devices. System B allows for both static hardware and dynamic software setting of the current level. The former can be achieved by changing the resistor at the output of the driver PCB which sets the current level as a function of the voltage drop across it (which is set by the active-feedback amplifier). The latter can be done by changing the analog value generated by the dSPACE DAC channel.

The more relevant aspects which will ultimately determine the suitability of the gate driver for the application developed in this thesis work are the current and switching frequency capability. As presented earlier, system A will be limited by the maximum current that can be carried by the output current mirror, which equals 2 mA per channel. If a current level of 100 mA is to be realized, several channels would have to be paralled, which is not really a recommended option as for complexity, size and cost. According to the datasheets, system B will be capable of delivering a gate current level of 100 mA. Regarding the switching frequency capability, system A will be mainly influenced by the speed at which the onboard DACs can operate at. SPI protocol would have to be implemented to control the 3 present DACs devices per channel. The data would have to be send separately and using a single line for all of them. Consequently, the maximum switching frequency at which all the necessary information would have to be sent over to the board from the dSPACE would be limited. The maximum switching frequency that could be reached has been estimated to be 20 kHz. System B does not make use of SPI protocol, and the interaction between the driver and the dSPACE is simpler in this regard. The charging and discharging operation is controlled by a digital output of the dSPACE unit which can change toggle every FPGA clock cycle (100 ns). There will be more restrictive elements at the driver that will limit the operating switching frequency of the system, which has been estimated to be 1 MHz.

To sum up, it has been shown how system B meets all the requirements associated to driving the DMOS of the buck converter as required. The only drawback of this concept with respect to system A is that it makes use of a relatively large amount of power supplies. The concept could be further optimized in this regards, but this thesis work focuses on the early development phase of the converter. Therefore, it will be assumed that the available driver can be used successfully to draw conclusions on the suitability of Infineon's smart technology for DC/DC applications.

4.6. Measurements obtained using System B

It has been concluded that system B can be used to drive the high-side switch of the buck converter. The driver concepts will be able to provide a current level of 100 mA at a switching frequency of 400 kHz according to the theoretical analysis and the datasheets of the ICs used in the design. As it has been mentioned earlier, this system was initially designed to operate at a much slower switching frequency, namely 20 kHz. Therefore, the design did not take into account parasitic elements or unmodeled phenomena that are negligible at 20 kHz but that could play a relevant role at 400 kHz. For instance, any ringing that was seen as a spike in the frequency range of 20 kHz and lower will be seen now as a much distorting signal that clearly influences the behavior of the system.

The next step is to determine whether the driver system can be used from a practical point of view. At the time this thesis work was carried out, the system was not used at Infineon, but a setup was available at a partner institute. The obtained measurements were therefore performed at a temporary setup in order to analyze the practical suitability of the driver PCB. The results will be shown in the following subsections. It must be taken into account that the prototype setup and the interaction between the

driver PCB and the DMOS test-chip was not optimized at all. Consequently, the results obtained will present a worst case situation. The potential behavior that could be obtained with an optimized setup will be shown in the next chapter.

4.6.1. Using Infineon's BSC020N03LS

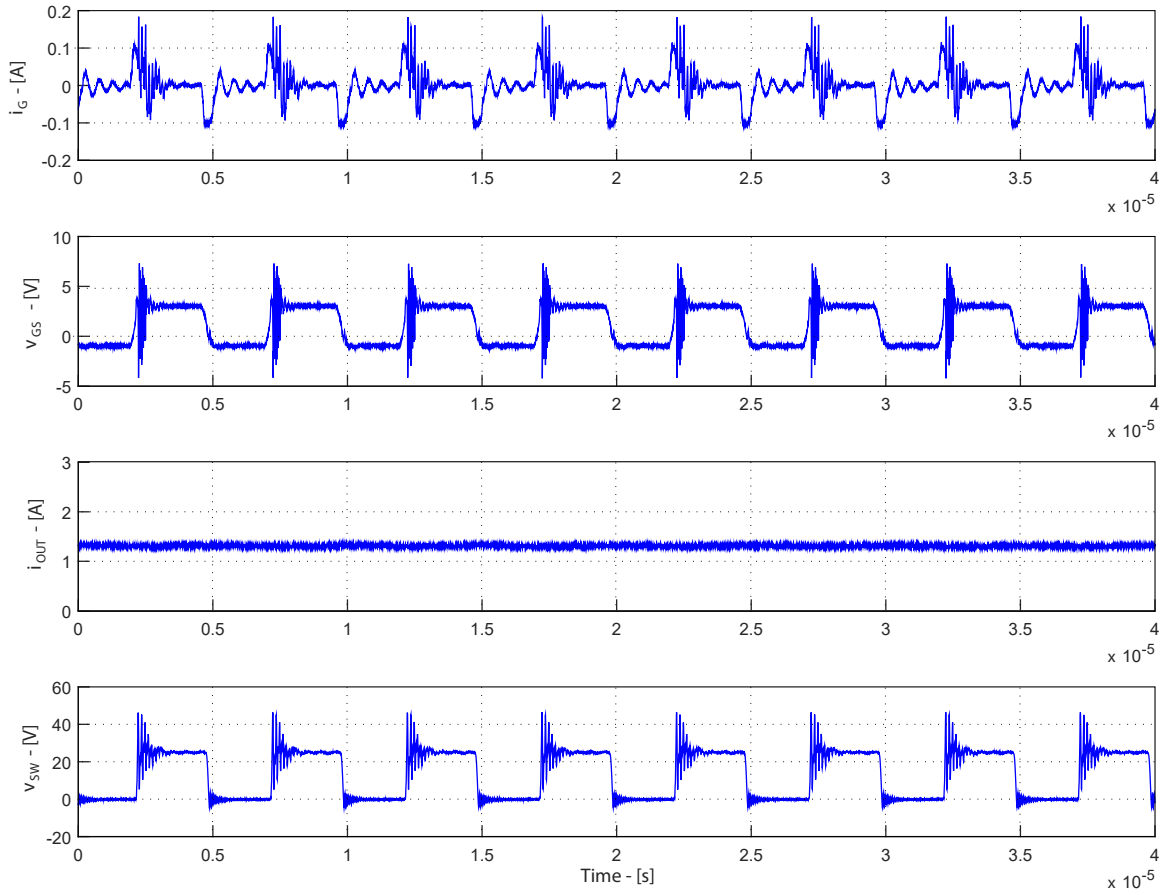

Figure 4.3: System parameters used to evaluate the performance of system B with Infineon's BSC020N03LS

System B was first tried out using a different switch from Infineon that was available at the partner institute. The parameters and the system components are presented in table 4.2. The output resistor, inductor and capacitor have been given these values due to availability. The measurements carried out and presented here are a first approximation to what could be achieved. The duty cycle for this example was set to 75 %, the switching to 200 kHz, the current level to 100 mA and the input voltage to 25 V. The setup includes the mentioned switch from Infineon at the high-side and a schottky diode at the low-side. The equivalent gate capacitance of this switch is in the order of 6 nF according to the datasheet [61].

Figure 4.3 shows the results obtained using the parameters given in table 4.2. It can be seen how the input current reaches the maximum expected value of 100 mA. Once the peak is reached, the current decreases until it reaches 0. The opposite takes place during the discharging transition. As for the gate-source voltage, the measurement shows how this voltage equals 3 V during the on-state (after the charging is complete) and slightly below zero (after the discharging is complete). The small negative value is due to the voltage drop of the diode that clamps the voltage to zero. The output voltage presents the expected value given by the output resistor and the duty cycle applied to the converter. The last waveform shown is the switching node voltage, that is the negated waveform of the low-side diode voltage drop. It can be observed how it equals the input voltage during the on-state and zero during the off-state.

Parameter	Value
R_{OUT}	10 Ω
L_{OUT}	25 µH
C_{OUT}	22 µF
D	0.75
f_{SW}	200 kHz
i_G^{max}	100 mA
V_{IN}	25 V

Table 4.2: Measurement results obtained with system B and Infineon's BSC020N03LS according to the parameters presented in table 4.2

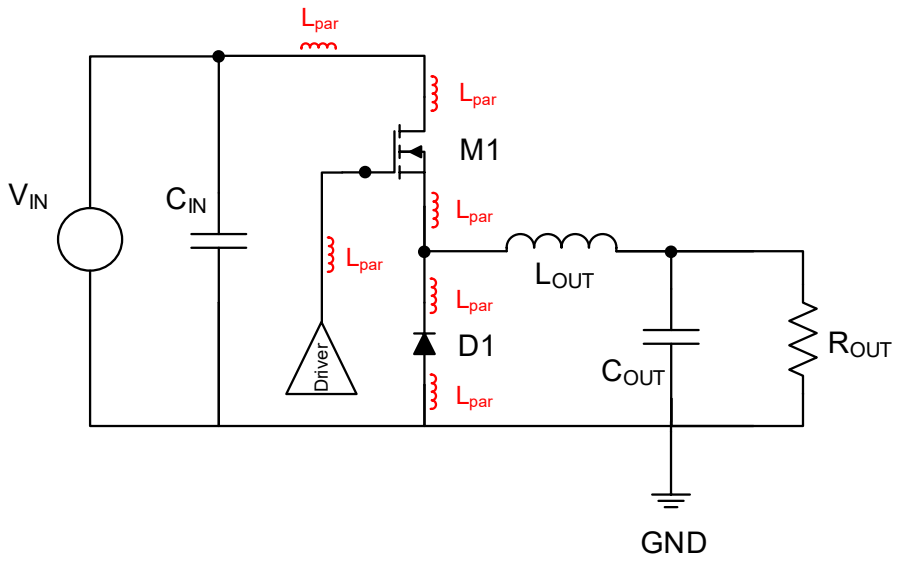

Figure 4.4: Schematic diagram of the converter setup where the parasitic inductances that contribute to the resonant response are highlighted

The waveforms however are far from the ideal case. A lot of ringing is present at the gate current, gate-source voltage and switching node voltage. It will be assumed that this behavior is due to the badly optimized setup. A lot of inductance is present at the path that joins the gate driver output and the gate of the switch. This will contribute to a resonance of current and voltage when the voltages are chopped (the parasitic capacitance will be influenced by the switch's gate capacitance, PCB and setup itself). As for the ringing that appears at the switching node voltage, the inductance present at the fast switching loop will create an unwanted resonance when the switching takes place (the parasitic capacitance will again be determined by the switch's capacitance, diode's capacitance, PCB and setup itself). Figure 4.4 depicts this concept in a schematic diagram of the converter.

4.6.2. Using Infineon's smart technology DMOS

Once the response of the system has been evaluated using a smaller switch and the results have been discussed, a similar set of measurements will be performed using the DMOS test-chip implemented in Infineon's smart technology. The driver PCB setup will be identical to that presented earlier. It is shown in more depth in table 4.3. The main difference with respect to the earlier switch is the packaging: since no extension boards compatible to the DMOS test-chip package were available, the connection of the switch to the driver PCB had to be realized in a very inefficient way, shown in figure 4.5. The

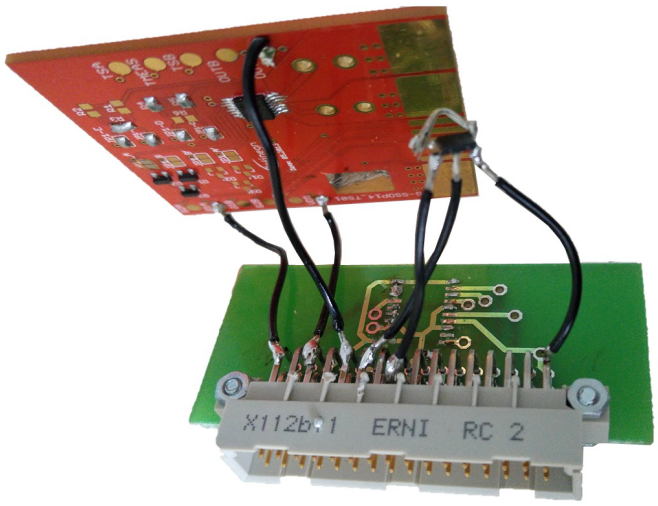

Figure 4.5: Extension board used to quickly test the interaction between system B and Infineon's smart technology DMOS

Parameter	Value
R_{OUT}	10 Ω
L_{OUT}	25 µH
C_{OUT}	22 µF
D	0.5
f_{SW}	200 kHz
i_G^{max}	100 mA
V_{IN}	25 V

Table 4.3: System parameters used to evaluate the performance of system B with Infineon's smart technology DMOS

used extension board includes DMOS devices for both high and low-side positions. However, the low-side DMOS will be shorted by the schottky diode soldered on the driver PCB. It can be seen how the rough and quick wiring and soldering used contribute to very high parasitic inductances. However, the measurements obtained with this setup will be taken as a very first approximation to what could be obtained with a more professional layout.

Figure 4.6 presents the obtained waveforms. Having a look at the gate current, it is observed how the maximum value reached is slightly below 100 mA for both charging and discharging. The switching is however satisfactory and the device can be turned on and off when the dSPACE dictates. The gate-source voltage is as expected, with a high-side value of 3 V during on-state and a low-side value slightly below 0 during the off-sate (again due to the voltage drop of the clamping diode). The drain-source voltage of the DMOS is depicted in the third subplot. It presents a squared shape with a positive value equal to the input voltage during off-state and zero value during on-state (slightly above zero due to the finite resistance of the channel). The voltage present at the switching node is complementary to its drain-source counterpart: when the DMOS is on it equals the input voltage and when it is turned off, it equals zero.

As observed from previous measurements, the waveforms are not ideal at all. A very dominant resonant response can be observed on top of the expected ideal behavior. The causes of this degraded performance are again unwanted parasitics. It can be seen however how the resonance that appears at the switching node is much slower than that observed for the previous measurement with Infineon's BSC020N03LS. The DMOS test-chip presents larger equivalent capacitances and therefore the equivalent resonant frequency will be lower. Additionaly, the inductance added by the quick and

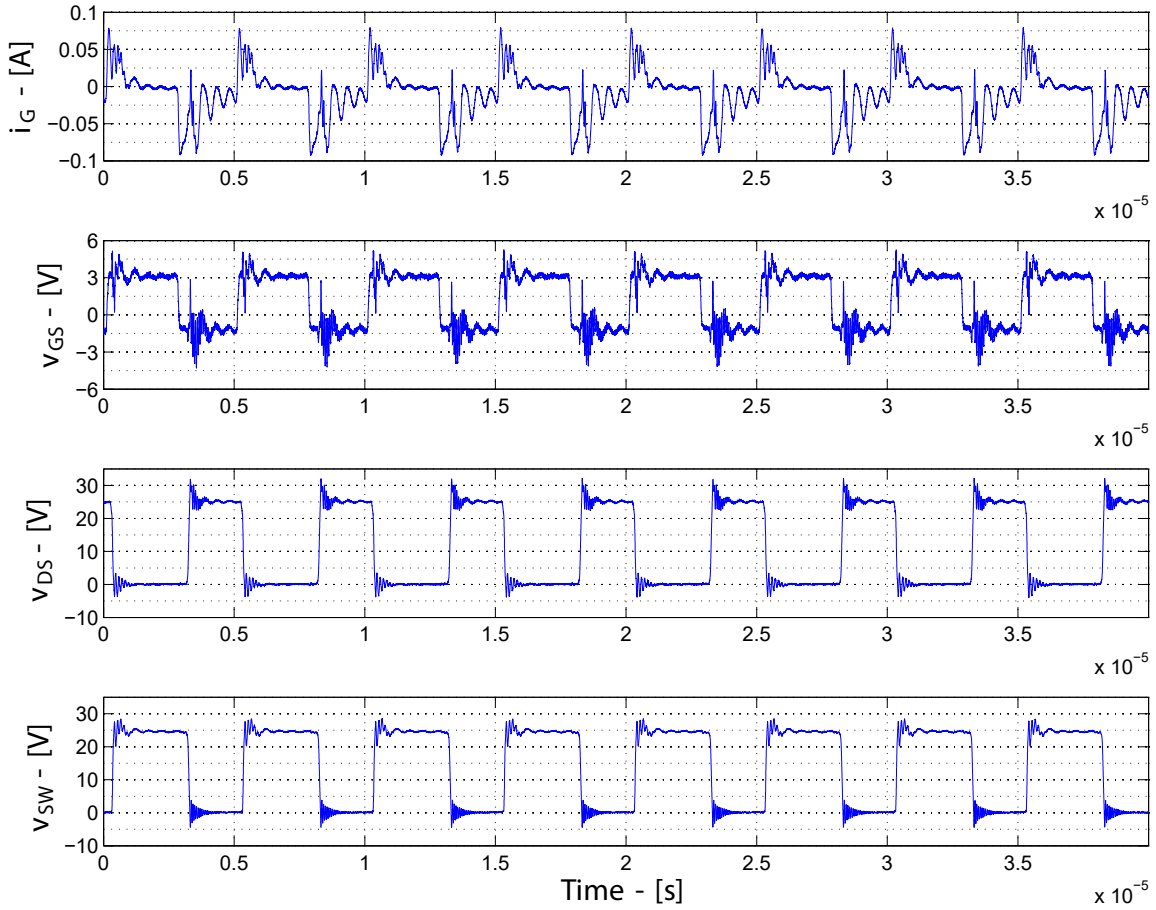

Figure 4.6: Measurement results obtained with system B and Infineon's smart technology DMOS according to the parameters presented in table 4.3

untidy setup makes the problem even worse. All in all, it can be concluded that the response obtained so far is not acceptable at all. Nonetheless, such poor performance can be totally justified by the setup and the layout of the system. The next chapter of this document will focus on improving this aspect to obtain a good system performance.

4.7. Conclusions

The first conclusion that can be drawn after analyzing the gate driver problem from a theoretical point of view is that system B can be used to drive the DMOS. According to the different datasheets of the discrete components and the working principle of the system, a gate current level of 100 mA can be delivered to the gate of the switch. What is more, this switching operation can be performed at a frequency in the order of 400 kHz. On the other hand, system B was initially designed to drive a smaller MOSFET at a lower switching frequency. Therefore the operation of the driver under the new boundary conditions must be validated from practical measurements.

The second conclusion will be related then to the behavior of the system observed from practical measurements. It has been shown how the prototype setup as it was initially designed does not provide good enough results. The origin of this poor performance is mainly related to undesired parasitic elements that play a non negligible role at frequencies in the order of 400 kHz. The original design would use the system at frequencies up to 20 kHz where these resonant behaviour was not dominant at all. Additionally, the layout used to analyze the interaction between the DMOS and system B is not optimized at all. This also contributes to making the problem with parasitic elements even worse.

The third conclusion is related to the improvement of the prototype setup. A series of assumptions

have been made in order to justify the bad performance observed from measurements. If the causes of the problem are known, several measures can be taken to improve the response of the converter. The next chapter of this document will elaborate on this aspect. Several actions to improve the setup of the system as a whole and the driver concept itself will be presented and discussed. The ultimate goal will be based on obtaining a working prototype of the system on which a control scheme can be implemented to prove the suitability of Infineon's smart switch technology for DC/DC applications.

5

Improving the prototype results

The fifth chapter of this document focuses on improving the response of the prototype system. Section 5.1 sets out the motivation for this approach while section 5.2 elaborates on the concept that will be implemented to realize such improvement. The PCB that includes the DC/DC converter will be discussed in detail in section 5.3 together with the criteria and aspects taken into account for its design. Section 5.4 elaborates on further improving the prototype setup by minimizing the inductance at the gate of the DMOS introduced by the gate driver PCB. Section 5.5 presents a comparison between measured efficiency of the system and its estimation obtained using the previously derived loss model. The mismatching between the two approaches will lead to further analysis of the loss model and its comparison to the prototype. This way, section 5.6 focuses on comparing different loss mechanisms between both the converter prototype and the loss model. Such analysis will bring up an initially unmodelled phenomenon related to a reference current generated internally by the driver circuitry that generates losses in the system. This aspect will be discussed from a theoretical point of view in section 5.7 and the practical aspects that yield improvements on the prototype setup will be presented in section 5.8. In order to support the methodology and steps followed to optimize the system, simulation results that match with the measurements observed in practice will be shown in section 5.9. With a better understanding of the prototype system, section 5.10 will focus on further improving the loss model. Finally, section 5.11 will present a comparison between the measured efficiency curves and their estimation with the improved loss model. Additionally, the most relevant waveforms of the converter in steady-state will be shown to demonstrate how the operation of the improved prototype setup can be considered robust and valid for further analysis. Section 5.12 summarizes the work presented in the chapter and puts the previously drawn conclusions together.

5.1. Motivation

The previous chapter concluded by presenting the results obtained when using system B to drive the DMOS of the buck converter. As mentioned earlier, the results are far from satisfactory. Considerable ringing can be observed at all relevant waveforms and the system behavior is not close to what could be expected at all. It was assumed that such bad performance was mainly due to the parasitic elements introduced by the inefficient setup. A much better response can be obtained if the overall layout of the system is optimized according to the needs of the application. Since the aimed switching frequency of 400 kHz is twenty times larger than that for which system B was initially designed to operate at, further aspects and limitations will have to be taken into account. The main concern will be put on the fast switching loop of the converter that includes both the diode and the DMOS. Ideally, all elements should be as close to each other as possible, which did not happen at all for the measurements shown previously.

The driver PCB, namely system B, will be used to just drive the gate of the high-side switch. This way, all possible parasitics that were not taken care of in the design for a switching frequency in the order of 20 kHz could be eliminated or at least minimized. Unlike the initial setup, where the driver PCB

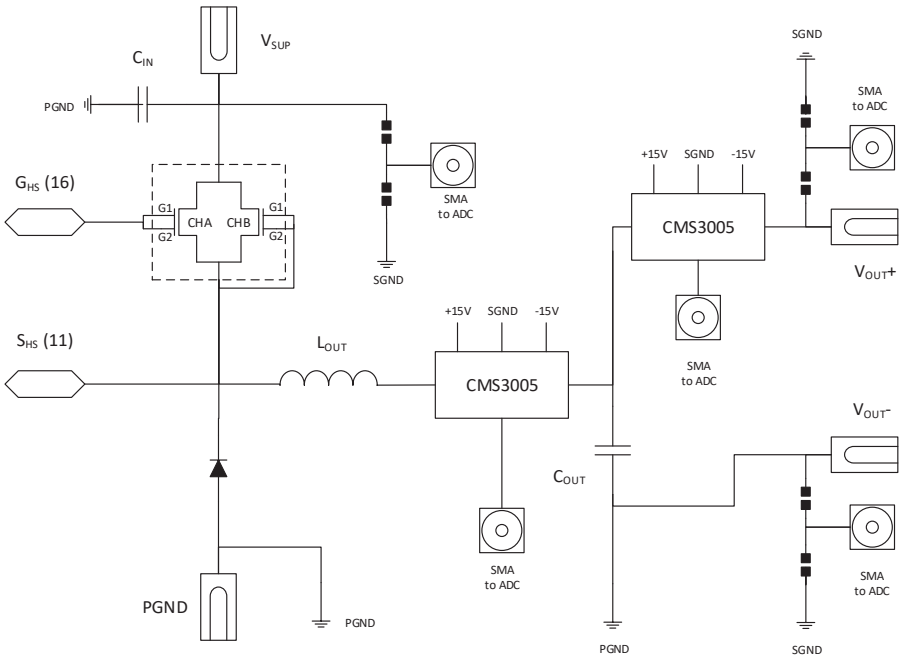

Figure 5.1: Concept drawing of the converter PCB used to optimize the system setup

was also used as the layout PCB of the converter, the idea is to include all elements (input capacitors, switch, diode, coil, output capacitors and measuring units) on a single PCB that minimizes parasitics and therefore optimizes the response of the converter. The following sections discuss and present this approach in detail in order to acquaint the reader with the final prototype design.

5.2. Concept

Figure 5.1 depicts the concept of the extension board that will interact with the driver PCB. The first aspect that can be noticed is that it includes the whole asynchronous buck topology on a single board: input capactor(s), diode, switch, coil and output capactor(s). This way, the layout of the different elements can be optimized, unlike the initial setup that was used to demonstrate the feasibility of system B. There, the different elements of the converter were connected to the driver PCB at different points of the board. This yielded extremely large parasitics, which are especially critical if contained in the switching loop. This had as ultimate results the poor performance observed in the measurements. With the new concept this will not happen, and the switching loop parasitics will be minimized as it will be explained later in this chapter.

Additionally, the two boards (system B and the board presented here) will interact through a DIN connector, although this interaction will only take place at two points: the gate and the source of the DMOS. These are required in order to deliver and sink the returning current needed to drive the transistor. Eliminating any other interaction with the driver PCB will allow for a minimization of any parasitic effects that could be caused by system B (originally designed to operated at a much lower switching frequency). The driver PCB initially included measuring elements and connectors that were used for the initial measurements. The improved setup will use its own measuring devices in order to integrate the whole solution on a single PCB and again, to optimize the performance of the system.

The new board will connect the gate of the DMOS to the gate terminal of the driver PCB in a very straightforward manner. The measurements taken earlier were obtained by connecting the DMOS to the driver PCB using a very inefficient wiring (as can be seen in figure 4.5). This will improve the parasitic inductance present on the path from the driver to the switch itself. The expected gate waveforms will be much closer to the ideal case than those obtained in the previous chapter.

Another relevant aspect of the prototype and the system as a whole is the feedback of the signals to the control. The new approach puts together all the necessary measuring devices to bring back the

signals from the analog domain to the dSPACE system. This way, the control will have the required signals available to command the converter. In this case, the signals that will be monitored are input and output voltage and coil and output current. The two former will be conditioned by means of a simple resistor network; the currents will be measured making use of CMS3005 sensing units [62]. All signals will be brought out of the PCB on to the dSPACE using SMA connectors.

Figure 5.1 also shows how the power ground (PGND) will be different to the reference plane used for the measurements (SGND). This will be implemented via the physical layout of the PCB in order to minimize any possible distortion of the measured signals by the switching action of the converter. Both ground will be joint together at a single point of the PCB where the amount of noise is relatively small.

It can be seen how the DMOS test-chip consists of two channels, A and B. Each of them is routed out of the package by two terminals, G1A and G2A for gate A, and G1B and G2B for gate B. Since the application of interest will only make use of a single channel, namely A, the other will be forced off. This can be achieved by shorting the gate to the source to make sure that its voltage never exceeds the threshold and therefore does not conduct any current. As for channel A, both gate terminals will be connected together. The connection points present at the new board are the following: DMOS gate and source terminal to driver PCB; input voltage supply (V_{SUP}); input power ground ($PGND$); positive output voltage (V_{OUT+}); negative output voltage (V_{OUT-}), which will be electrically the same point as PGND; SMA connector input voltage measurement; SMA connector coil current; SMA connector output current; SMA connector positive output voltage; and SMA connector negative output voltage. The latter will be used in case there were a voltage offset between the converter ground, PGND, and the reference ground of the dSPACE ADCs (it should be ideally the very same point).

The power domain or voltages required to operate the board are: the input supply, whose power will be handled and transferred to the output by the converter hardware;+15V, needed to power the current sensors; and -15V, also required to power the current sensing elements. Typically, 3 power supply channels will be employed to supply these domains. In case the converter is to be run open-loop and no feedback is required, the current sensors can be left off and the only supply needed will be at the input of the converter.

The main advantage of the new approach is that different passive elements, namely capacitors and coils, can be put in the system in a very clean and efficient way to further investigate how they could affect the overall performance. Also, in case a different converter topology had to be tried out, the driver PCB could still be used to charge and discharge the gate terminals of the switches. All in all, the described concept is very flexible and versatile and still takes care of minimizing the parasitic elements influenced by the layout of the system.

5.3. DC/DC converter PCB implementation

The physical implementation will be described in this section once the concept to improve the prototype setup has been discussed. PCB layout will be one of the most critical aspects to minimize the parasitic effects that could degrade the performance of the system and therefore special care must be taken when placing and routing the components of the buck converter. [63], [64] and [65] present several recommendations and layout techniques that will be taken into account for the design of the PCB. Figure 5.2 shows the PCB layout that was designed to implement the concept introduced in the previous section. The design contains four different layers that will be explained in more detail hereafter.

The top layer (top-left corner of figure 5.2) includes all the elements of the converter that handle a significant amount of power (input and output capacitors, switch, diode and coil). This is done to minimize the use of vias that would introduce extra inductance at paths that could be carrying a significant amount of current. The width of these power carrying traces have been chosen for a temperature increase of 30 ºC when carrying a DC current of 5 A. The top-middle layer (top-right corner of figure 5.2) contains the power ground of the converter. This is done to place the returning path of the high-frequency signals as close as possible to the top layer (emissions will be therefore minimized). This layer will also act as a shield to the DC/DC, significantly improving the EMI performance of the board. The bottom-middle layer (bottom-left corner of figure 5.2) is used as the sensing ground. It will be electrically separated from the power ground to provide an analog reference which is isolated from the power ground which can contain significant high-frequency currents. This way, any possible distortion

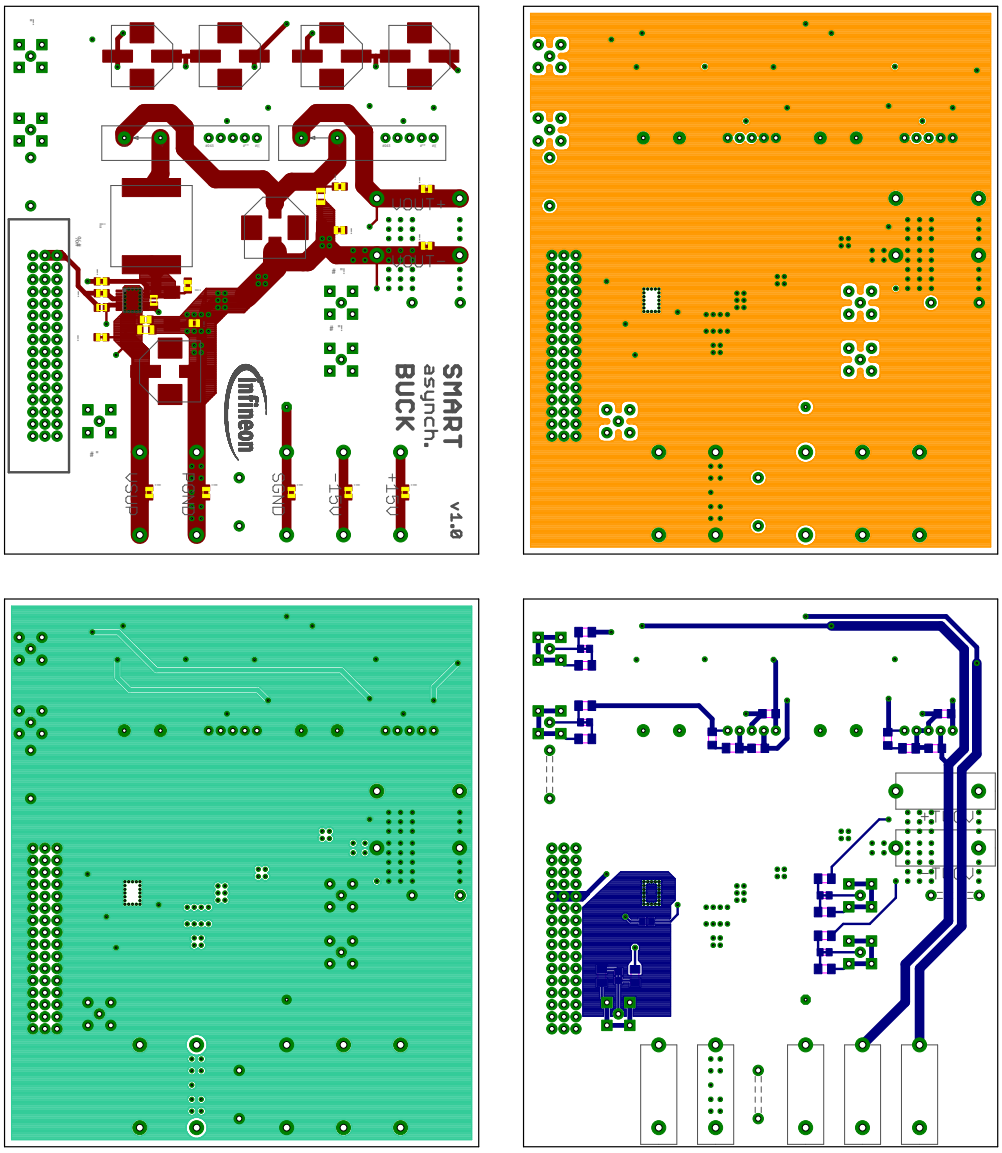

Figure 5.2: Layout of the designed DC/DC converter PCB. Top-left: top layer; top-right: top-middle layer; bottom-left: bottom-middle leyer; bottom-right: bottom layer

of the measurements can be avoided. Both power and sensing grounds must be connected together at a single point far away from the zone where the high-frequency are circulating (namely the switching node). Lastly, the bottom layer will contain the elements associated to the sensing units and will be used to route the measured signals (input and output voltage and coil and output current).

It can be observed that a ring of thermal vias is placed underneath the DMOS test-chip to thermally join the package (where the power losses are generated) to a plane placed on the bottom layer. This will significantly improve the thermal dissipation capability of the switch which will have to handle relatively large amount of power. It will be very important to keep the silicon as cool as possible in order to guarantee safe temperature operation of the converter.

As it has been mentioned earlier, minimizing the length of the high-frequency switching loop to minimize inductance introduced by PCB traces will be critical. The operation of the converter yields two main high-frequency loops: during the on-state, the switch will be conducting a significant amount of current from the input to the output of the converter through the coil; during the off-state, the current will freewheel through the diode, coil and output. Overall, the current through the coil will be continuous. Big current jumps, however, will occur at the switch and diode of the converter. The most critical loop will be

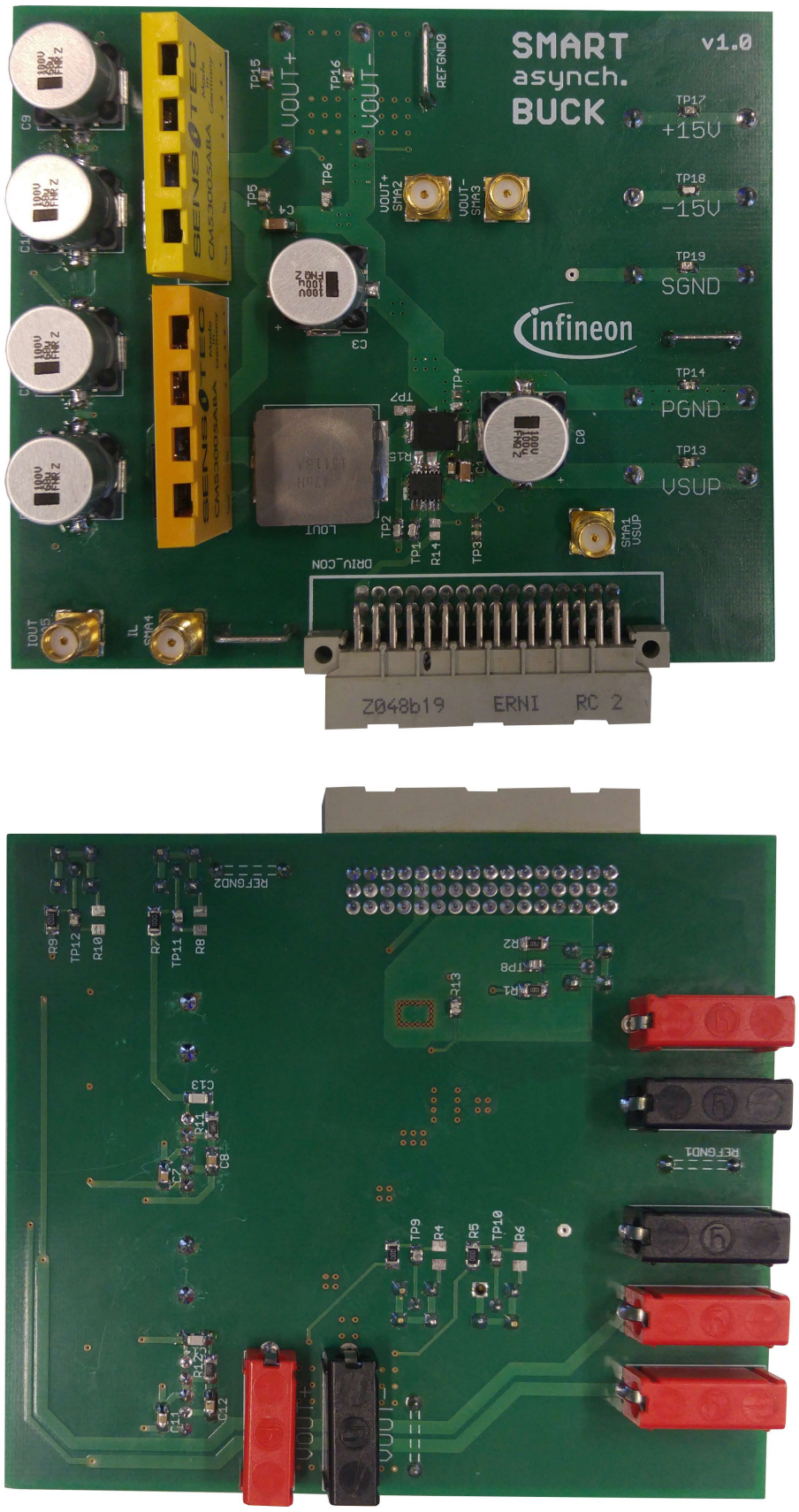

Figure 5.3: Top and bottom view of the designed DC/DC extension board

therefore that which contains the input capacitor, the DMOS and the low-side diode. Consequently, they will have to be placed as close as possible to each other. In order to avoid any inductance introduced by vias, they will also be placed on the same layer.

Input and output capacitors where selected earlier in this document according to a set of requirements. These were related to both the maximum allowed high-frequency ripple and the transient response to load steps. Due to practical limitations of different capacitor technologies, their effective capacitance will not be homogeneous along the frequency domain. In order to compensate for this, a more ideal capacitor will be implemented by means of several devices. For this reason, capacitors of different sizes and technologies will be used.

Fast voltage transitions must be taken into account when designing the layout of the converter PCB. The copper used to create traces on the PCB will present a capacitive behavior since it has to be charged before it can conduct any current. Therefore, the amount of copper used for the switching node (whose voltage rapidly changes from input voltage to zero and vice versa) must be minimum. This will minimize any parasitic capacitance added to the source of the DMOS that would slow down the transitions and would yield an increase of switching losses.

The high-frequency current component that is carried by the output coil will also introduce a design rule to the PCB of the converter. Such high-frequency current will be associated to a high-frequency magnetic field. Let us imagine there were some conductive material at the vicinity of the coil. Part of this fast changing magnetic field in the coil will leak to the outside in practice and could reach the conductive element. Consequently, eddy currents would be induced and additional losses would occur. This can actually happen on the PCB is some unnecessary amount of copper is placed around the inductor. Therefore, any ground or copper planes at the vicinity of the coil must be eliminated in order to avoid extra losses.

The converter PCB designed in this section will contain signals of very different nature. On the one hand, the converter will handle high-frequency currents required to transfer power from input to output. On the other hand, some signals of the converter will have to be measured in order to control the system. The latter must be kept as far away from the noise generating signals (high-frequency currents generated by the operation of the converter) as possible. That is why the bottom layer has been used for this purpose. Additionally, measured signal traces will be routed out to their respective SMA connectors far from the ”hot” switching node that could contaminate the measurements.

In addition to the special attention that must be taken to route the measurement traces, the two different reference planes must also be taken care of. The sensing ground will be used as a reference to the measured signals and should not be affected by any noise coming from the high-frequency currents of the converter. The power ground must act as both reference to the power circuit and as a shielding elements. The two planes have to be connected together at a point which is far from the switching node. This way, noise coupling between the two references will be minimized and the integrity of the measured signals will be kept. A good area of the PCB to do so is the output of the converter. Several vias will be used to electrically connect the two planes and this will be therefore taken as the absolute zero reference of the converter.

Current measuring units required to monitor coil and output current will be placed on the board with buffering capacitors (aluminum electrolytic and ceramic) and output filter to improve their linear response as specified in the datasheet. The output voltage generated by the current sensor can be then connected to the ADCs directly. The same can be done with the output voltage, since its range is within the allowed voltage of the peripheral. The input voltage however must be scaled down by using a resistor divider to condition it to the allowed voltage range.

Figure 5.3 shows the top and bottom views of the practical realization of the DC/DC extension board discussed in this section. The components soldered on-board are those selected in chapter 3 to meet the requirements related to the operation of the converter.

5.4. Improving the setup: minimizing inductance at the gate

The extension PCB that includes the buck converter has been designed according to a series of guidelines to minimize the parasitics at critical points. This way, the performance of the converter will not

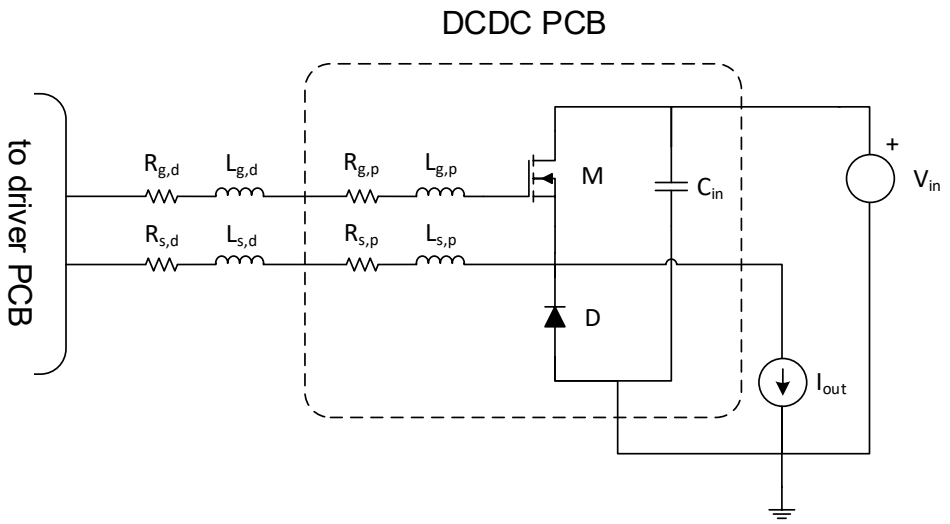

Figure 5.4: Main parasitic indutance and resistance elements that appear in the converter

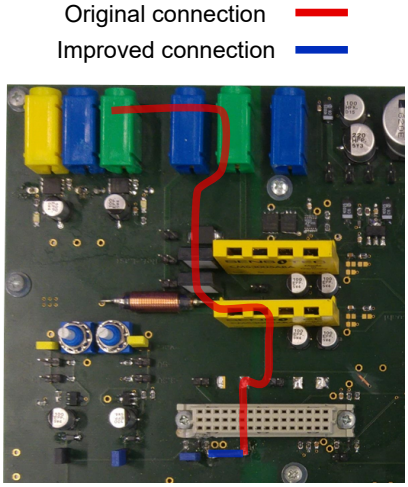

Figure 5.5: Graphical comparison between the original and the improved connection path between the DC/DC board and the driver PCB

be severely affected by unexpected phenomena such as resonance. On top of this, the driver PCB, namely system B, will be used to drive the gate of the DMOS. As mentioned earlier, this board was designed to operate at a much lower switching frequency. Consequently, the requirements related to introduced parasitics were not so demanding. For instance, a parasitic inductance which created a resonance could be ignored if the system was to operate at 20 kHz. If this frequency is increased twenty times, namely 400 kHz, this resonance will not be negligible with respect to the total switching period. In order to be able to obtain an acceptable response, the driver PCB has to be improved as well with respect to the initial design. Since system B will exclusively used to drive the DMOS, the only part of the circuit that will have to be optimized is related to the high-side driver. Figure 5.4 presents a schematic drawing of the converter where the most relevant parasitic elements are shown. These can be categorized into two different types: those introduced by the DC/DC PCB layout (with a subscript p); and those introduced by the driver PCB layout (with a subscript d). The resistive elements will be related to the finite resistance of the PCB traces that will create a voltage drop ; the inductive elements will be related to the inductance introduced by the PCB traces as well. $L_{g,p}$, $R_{g,p}$, $L_{s,p}$ and $R_{s,p}$ have already been minimized when designing the DC/DC PCB. On the other hand, $L_{g,d}$, $R_{g,d}$, $L_{s,d}$ and $R_{s,d}$ will correspond to a design aimed to operate at 20 kHz and therefore could be further optimized.

Figure 5.5 shows the top view of the driver PCB at the area where the converter extension board

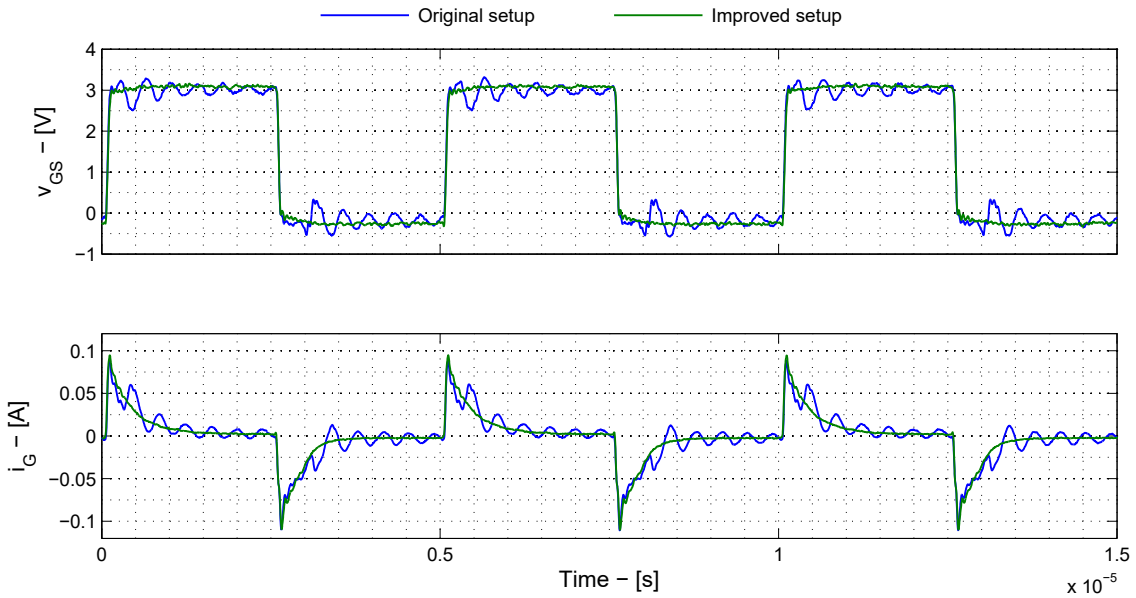

Figure 5.6: Comparison between original and improved setup (minimizing parasitic inductance at the gate of the DMOS) for a switching frequency of 200 kHz

is connected through a DIN connector. The path which initially connected the source of the DMOS (at the DC/DC PCB) to the corresponding terminal of the driver PCB is highlighted in red. It can be seen how this trace is extremely long, which will introduce large values of $L_{s,d}$ and $R_{s,d}$. The results obtained with the inefficient connection were good enough if the system was operated at a maximum switching frequency of 20 kHz. However, if the system is operated at 400 kHz, the inductance introduced by this long connection will generate an unacceptable response. On the contrary, the new path which connects the source terminals of both the DC/DC PCB and the driver board is highlighted in blue. This is much shorter and therefore will minimize the parasitic elements introduced by the physical layout.

A set of measurements was performed when the new connection path was implemented, in order to compare some of the DMOS waveforms before and after introducing the change in parasitic inductance. Gate-source voltage and gate current are plotted in figure 5.6 for both cases. It can be seen how the original setup presents an overlapping resonant response with a resonant frequency in the order of 2 MHz. It appears at both voltage and current waveforms and is mainly due to the parasitic inductance $L_{s,d}$ shown in figure 5.4. The improved setup shows a much better response close to what be expected ideally. Gate-source voltage goes between 3 V at on-state and slightly below 0 V during off-state. The transitions between on and off and vice versa are very smooth for the new setup. Similarly, the gate current shows a very smooth profile. The peak value is slightly below 100 mA but still the driver is able to charge and discharge the gate of the DMOS at the desired speed. It can be concluded then that the quality of the switch waveforms is extremely improved by the new setup and the obtained response can be considered satisfactory now.

Once the interaction between the DC/DC PCB and the driver board has been improved, the effect of the gate current level on the switching time can be analyzed.The upper half of figure 5.7 shows the gate current and the gate-source voltage for different current level configurations during turn-on. As expected, it can be seen how increasing the maximum current yields faster transitions. The more the driver is pushed to deliver a large current, the more it deviates with respect to the expected maximum value. It can be observed how the gate current roughly reaches 90 mA for the 100 mA configuration. However, for a gate current configuration of 10 mA the driver shows a much more accurate tuning of the delivered current. All in all, the overall response of the driver can be considered satisfactory.

If the gate current delivered by the switch is integrated along time the amount of gate charge required by the switch can be obtained. The simulation work carried out and discussed earlier in this document concluded that the DMOS would need a gate charge in the order of 35 nC. The results obtained by integrating the measured gate current show a very good matching with respect to simulation. For a current level of 100 mA the total charge delivered to the gate is approximately 33 nC. This level stays

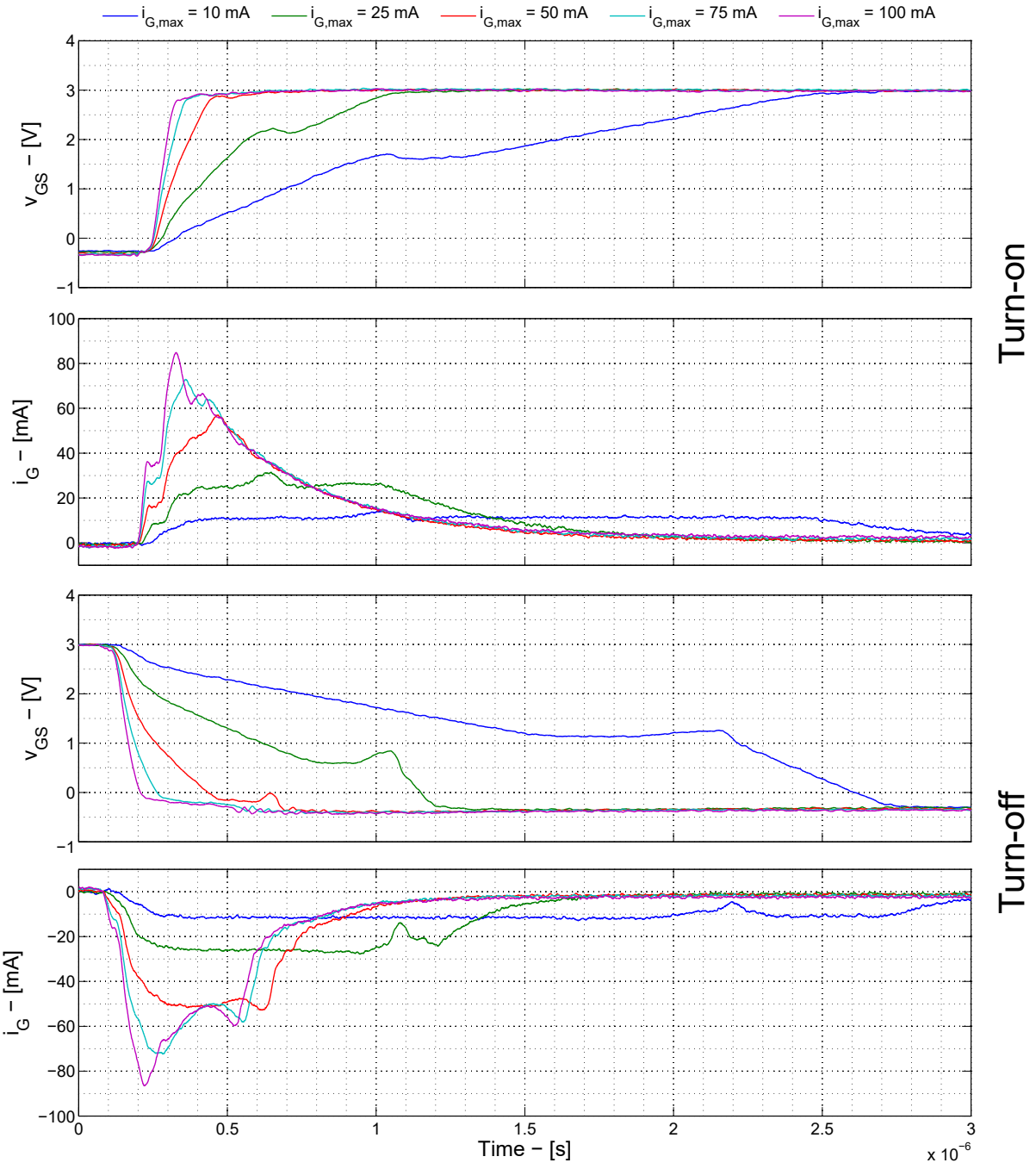

Figure 5.7: Gate-source voltage and gate current for different gate current levels during turn-on (upper half) and turn-off (bottom half)

almost constant for different driver current configurations.

The bottom half of Figure 5.7 shows the homologous waveforms during turn-off. Similar remarks can be done: the voltage goes down to a value slightly below 0 V (due to the voltage drop of the negative clamping diode) when fully turned-off. If the current level is small enough, the plateau can be even observed. As for the current, the peak values are very accurate for low current configurations and deviate from the expected value if the driver is pushed to deliver more and more current.

5.5. Mismatching between open-loop measurements and loss model

So far the driver PCB and the DC/DC extension board have been improved in order to obtain an acceptable response of the converter for the whole range of switching frequencies. The first aspect that can be studied to validate the analysis of the converter is the efficiency. Earlier chapters of this document focused on providing a loss model of the system to estimate the overall efficiency of the converter. The efficiency of the prototype can be evaluated in order to establish a comparison between the theoretical analysis and the practical results. The efficiency will be evaluated by computing the average input and output powers at the prototype setup for different operating points. The converter will be composed of the practical components selected in chapter 3. An output resistor of 6 Ω will be used as the output load. The average input power will be calculated by multiplying the input voltage and the input current and computing its average value. Similarly, the output power will be reckoned by multiplying output current and voltage and evaluating its average value.

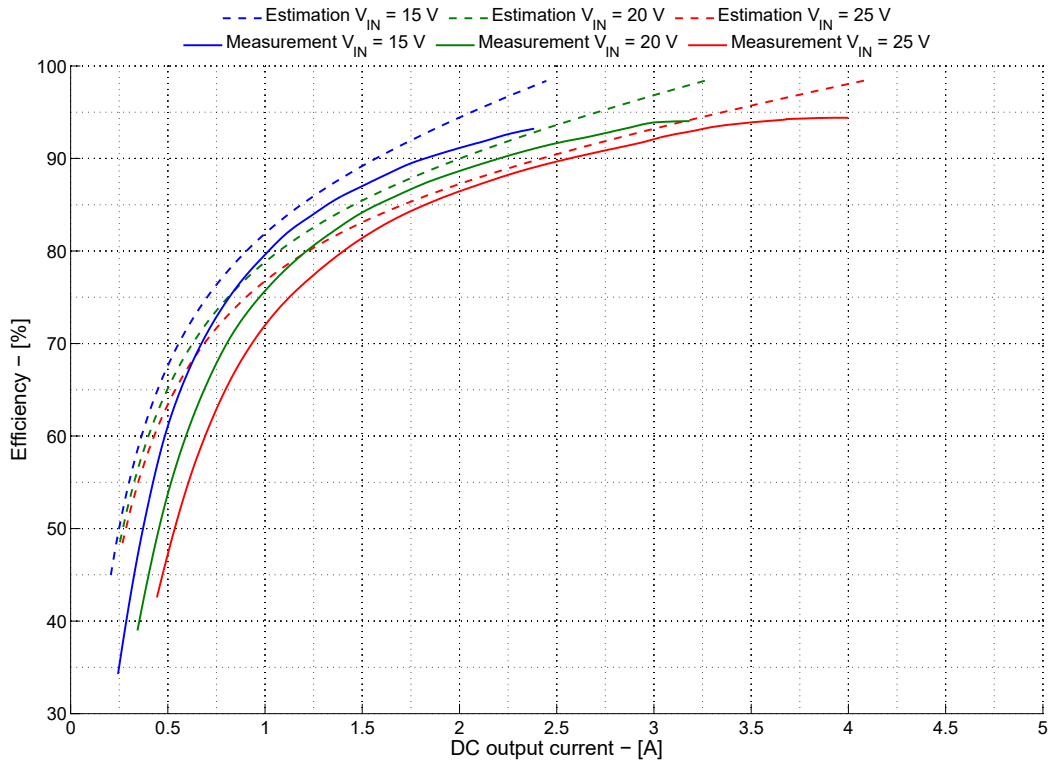

Figure 5.8: Comparison between measured and estimated efficiency for a switching frequency of 100 kHz

The measured efficiency obtained for different switching frequencies is presented in figures 5.8, 5.9 and 5.10. Let us first focus on the results obtained for a switching frequency of 100 kHz. The estimation provided by the loss model is shown in dashed lines while the measurement results are plotted using continuous lines. The comparison is made for three different voltage levels. As expected, the efficiency drops for both estimation and measurements at the low current range. On top of this, it can bee seen how increasing the input voltage for a given value of output current yields a decrease in efficiency. This is mostly caused by the DMOS dynamic losses becoming larger and larger (they are proportional to the input voltage). It can also be observed that the higher the current delivered to the output, the higher

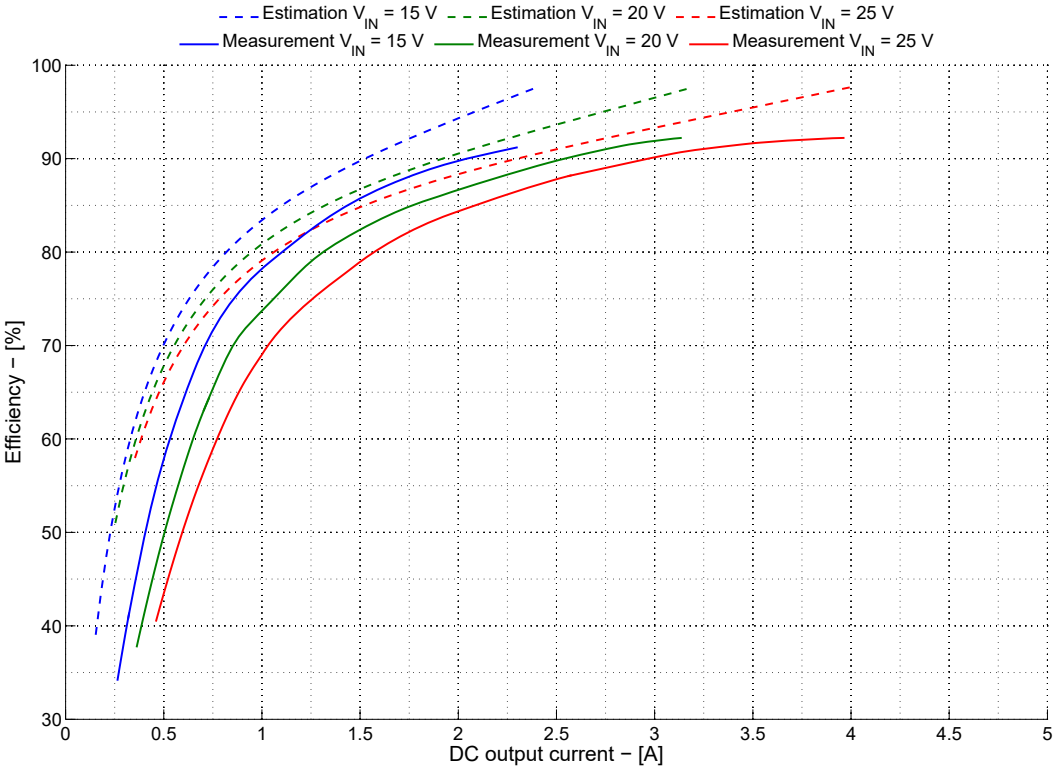

Figure 5.9: Comparison between measured and estimated efficiency for a switching frequency of 200 kHz

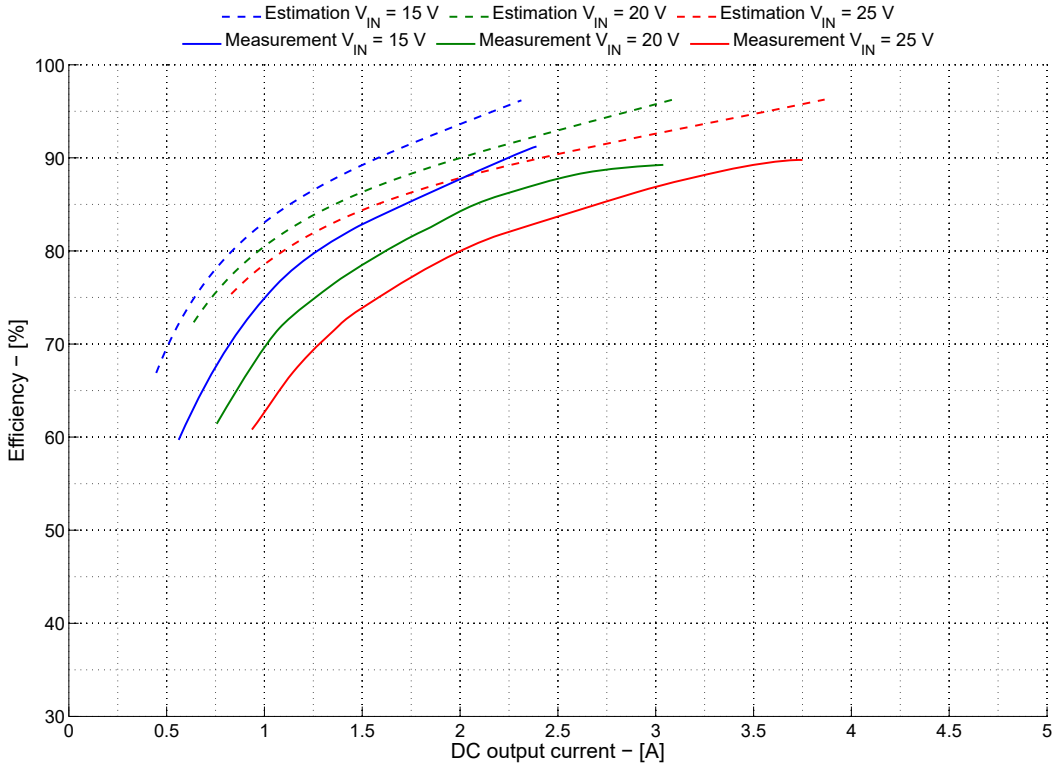

Figure 5.10: Comparison between measured and estimated efficiency for a switching frequency of 400 kHz

the efficiency of the converter will be. However, the mismatch between estimation and measurements is evident.

The matching between the estimated and the measured efficiency for higher switching frequencies (figures 5.9 and 5.10) is not any better. Again, the observed profile of the efficiency curves is similar as that mentioned for 100 kHz: the efficiency drops for low current points and it becomes higher and higher with the output current; besides, increasing the input voltage yields a decrease in efficiency for a given output current level. All in all, the mismatch is again unacceptable.

It can be concluded therefore that the loss model derived earlier in this document is not predicting well the different loss mechanisms present in the converter. It could also be that the converter is not operating as expected and that additional unknown losses are being generated in open-loop mode. In any case, further investigation has to be carried out to find the root cause of the mismatch. These will be addressed in the following section.

5.6. Improving the loss model

Figures 5.8, 5.9 and 5.10 presented a comparison between the loss model and the measured efficiency of the improved conveter prototype. It has been concluded that this initial estimation is not satisfactory and that further investigations have to be carried out in order to determine the origin of this mismatch. The approach followed will consist in isolating different loss sources of the converter. This way, the losses could be measured separately and the loss model could be corrected in case the initial approach does not provide with an accurate estimation.

5.6.1. Experimental determination of diode losses

The first element of the converter that can be easily isolated and characterized is the schottky diode. Figure 5.11 shows a schematic drawing of the setup used to measure the diode losses separately. A power amplifier was used to generate a square waveform voltage. When the input voltage is larger than the diode voltage drop, the resistor will conduct the amount of current corresponding to the voltage level; when the input voltage is zero, the resistor will not conduct any current. This setup emulates the operation of the low-side diode of the buck converter.

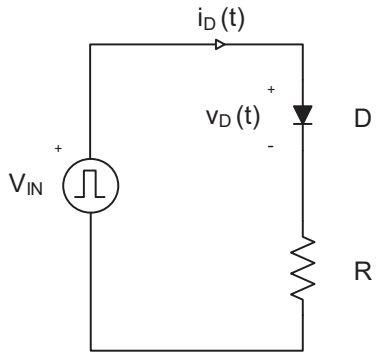

Figure 5.11: Schematic drawing of the setup used to characterize the diode losses

The losses in the schottky diode were defined earlier:

$$P_D^{avg} = V_D\, I_D^{avg} + R_D\, I_D^{rms} \tag{5.1}$$

Both the rms and the average values will be computed for different operating points. The losses in the diode will be measured experimentally by computing the instantaneous power ($p_D(t) = i_D(t)\, v_D(t)$) and averaging it for a finite amount of switching periods. The results obtained for both cases will be compared to determine how accurately the diode losses are estimated. table 5.1 presents some of the obtained values. The values are rounded but the relative error is shown to give an overview of the deviation between the two approaches. It can be seen how the measured losses are very similar to

those obtained using the loss model of the diode. The maximum observed error is approximately 7 %, which is considered good enough. Therefore, it can be concluded that the estimation of the diode losses is accurate enough and does not originate the mismatch between estimated and measured efficiency.

I_D^{avg} [A]	I_D^{rms} [A]	P_D^{meas} [W]	P_D^{est} [W]	Error [%]
0.069	0.096	0.022	0.022	2.97
0.116	0.161	0.037	0.036	2.09
0.164	0.226	0.055	0.052	5.66
0.261	0.358	0.091	0.085	6.91
0.456	0.622	0.167	0.156	6.50
0.947	1.288	0.376	0.367	2.38
1.426	1.925	0.600	0.613	-2.18
1.752	2.206	0.760	0.769	-1.17

Table 5.1: Comparison between measured and estimated diode losses

5.6.2. Experimental determination of switch losses

Once the diode losses are known, a simplified setup of the converter can be built to characterize the losses generated in the DMOS. Figure 5.12 presents the schematic drawing of this setup. The switching leg of the buck converter will be present, and since the diode losses have been confirmed to be accurately estimated, the the switch will be the only element left to characterize. A very large air coil will (1 mH) be placed at the output of the switching leg. This way, the current that goes through the output resistor can be assumed constant. Consequently, the current carried by the switch during the on-state will be constant. During the off-state, the diode will take over the current, which will be assumed constant and equal in value.

The values of the DMOS transition times were initially taken from the simulation analysis. Since the setup is available, they can be characterized in practice in order to check the accuracy of initial loss estimation. After having a look at different operation points of the converter, it has been concluded that the practical transition times are larger than those given by simulation. This was already expected since the simulation workbench did not take any parasitic capacitance into account. In practice, the physical implementation on the PCB and other aspects will add some parasitic capacitance to the switching node. This will slow down the transitioning between on and off states. Consequently, the overall dynamic losses will be slightly larger than those estimated initially.Table 5.2 summarizes the values observed for the different transition times.

With the newly corrected transition times, a comparison between the modeled dynamic losses and the actual measurement can be established in order to determine the accuracy of the loss model. The expression used to estimate the dynamic losses will be as derived earlier in this document:

$$P_{dyn}^{est} = \frac{1}{2} V_{IN} I_{OUT} f_{SW} (t_{ON,1} + t_{ON,2} + t_{OFF,1} + t_{OFF,2}) \tag{5.2}$$

Table 5.3 presents the different values of measured and estimated dynamic losses for a switching frequency of 200 kHz and an input voltage of 20 V. This same procedure was carried out for other operating conditions (different switching frequencies and input voltages). After having a look at the computed values, it can be concluded that the loss model with the corrected transition times provides accurate enough estimation of the dynamic losses in the DMOS. The maximum relative error for the operated conditions associated to table 5.3 is roughly 5 %. It can be concluded then that the model of the DMOS dynamic losses is accurate enough.

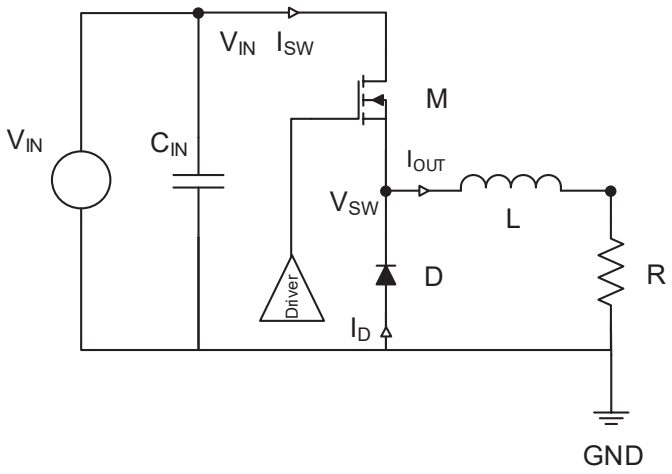

Figure 5.12: Schematic drawing of the setup used to characterize the switch losses

Time	Value
$t_{ON,1}$	55 ns
$t_{ON,2}$	60 ns
$t_{OFF,1}$	105 ns
$t_{OFF,2}$	25 ns

Table 5.2: Transition times measured at the simplified setup depicted in figure 5.12

So far, the losses in the diode and the switch have been proven to be matching with their respective estimations. However, an unexpected behavior was observed when having a detailed look at the current through DMOS and diode using the setup described in figure 5.12. The value measured using a current probe corresponded to that expected plus a constant value of 100 mA. After carefully analyzing the prototype setup and the interaction between the driver PCB (system B) and the DC/DC extension board, it can be observed how the reference current internally generated by the driver finds its return path through the switching leg back to the source terminal. This aspect will be addressed in detail in the following section.

D [%]	I_{OUT} [A]	P_{dyn}^{meas} [W]	P_{dyn}^{est} [W]	Error [%]
20	0.681	0.248	0.243	2.25
30	0.978	0.360	0.371	-2.96
40	1.265	0.472	0.495	-4.67
50	1.555	0.594	0.620	-4.27
60	1.842	0.716	0.745	-3.85
70	2.132	0.840	0.870	-3.45
85	2.582	1.040	1.060	-2.32

Table 5.3: Comparison between measured and estimated dynamic DMOS losses for an input voltage of 20 V and a switching frequency of 200 kHz according to the setup presented in figure 5.12

5.7. Driver reference current

When analyzing the switching losses in detail, it was observed that the current through the switch was not exactly equal to that delivered to the output of the converter. In addition to the output losses, the DMOS current included a term equal to 100 mA which is coming from the gate driver. Figure 5.13 depicts the concept drawing of both converter and driver boards. It can be seen how the internally generated reference current of 100 mA circulates through the power hardware to return back to the driver through the source terminal. This reference current is initially tuned to 100 mA by the driver circuitry. Depending on the state of the CH/DCH signal (that is, depending on the direction of the current that the driver has to supply to the gate), the current will circulate to the corresponding current mirrors. Consequently, this current will circulate through the floating power supplies as well so that Kirchhoff's law will apply (the algebraic sum of currents in a network of conductors meeting at a point must be zero).

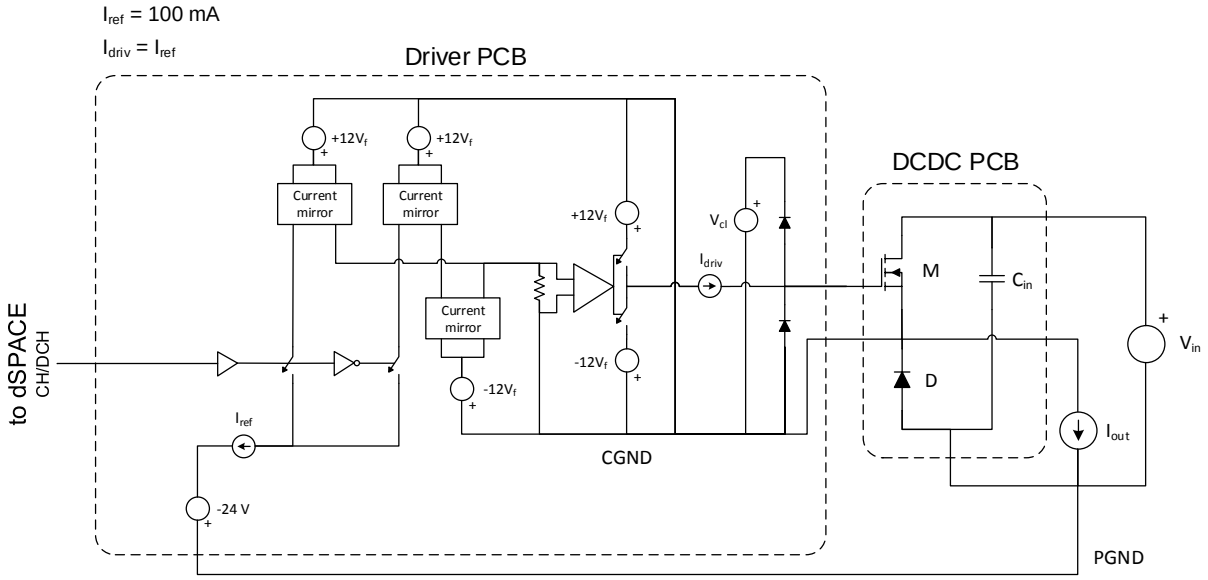

Figure 5.13: Concept drawing of the whole system to explain how the reference current circulates back to the driver through the converter

Let us firstly focus focus on the on-state, depicted in more detail in figure 5.14. Since the diode will not be conducting during this phase, it has been omitted. The reference current of 100 mA will circulate and get mirrored in the driver PCB according to the arrows that show the magnitude of the current through each piece of wire. In order to keep the balance, the reference current must circulate back to the source terminal. This can only happen if the DMOS lets it through. Consequently, the input voltage supply will have to carry such current.

The equivalent circuit is slightly different during the off-state, presented in figure 5.15. The switch is omitted during this phase since it will be forced off. Similarly to what has been described for the on phase, the reference current will circulate and get mirrored in the driver PCB as described by the arrows. Since Kirchhoff's law must apply, the reference current will circulate back to the source terminal. However, this time the diode will have to let the current through.

Not only will this reference current create additional switch (conduction and dynamic) and diode losses, but also the input power supply will have to deliver further power in order to allow the current to circulate back to the driver. This new power was not taken into account in the initial loss model and could introduce a considerable change. Additionally, the switched nature of this reference current will create additional parasitic effects that will be addressed in the following section.

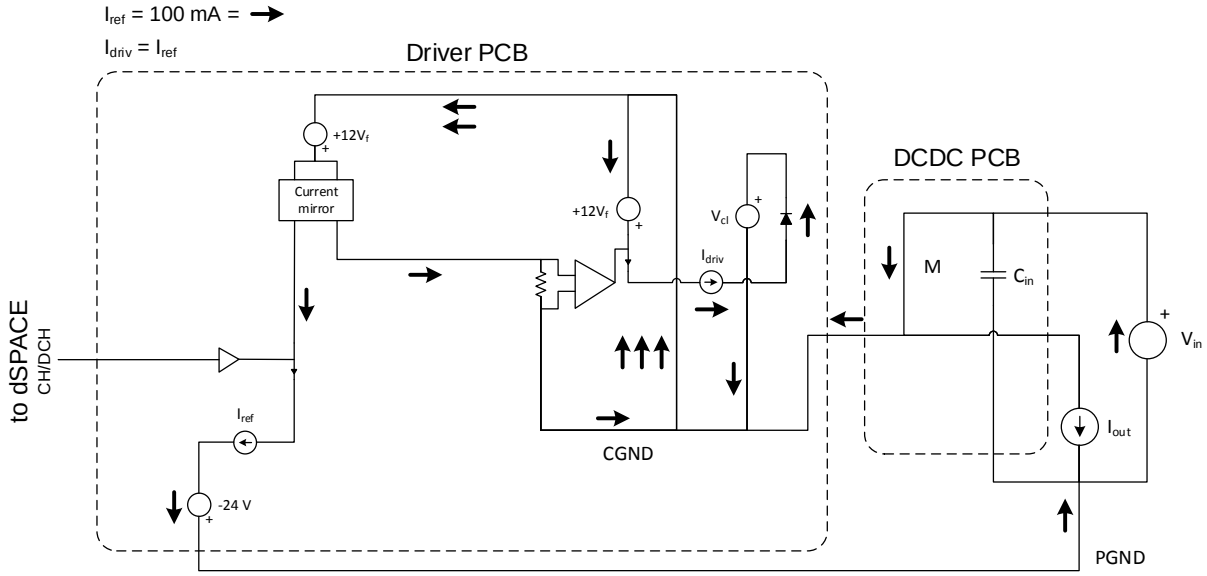

Figure 5.14: Concept drawing of the whole system to explain how the reference current circulates back to the driver through the converter during on-state

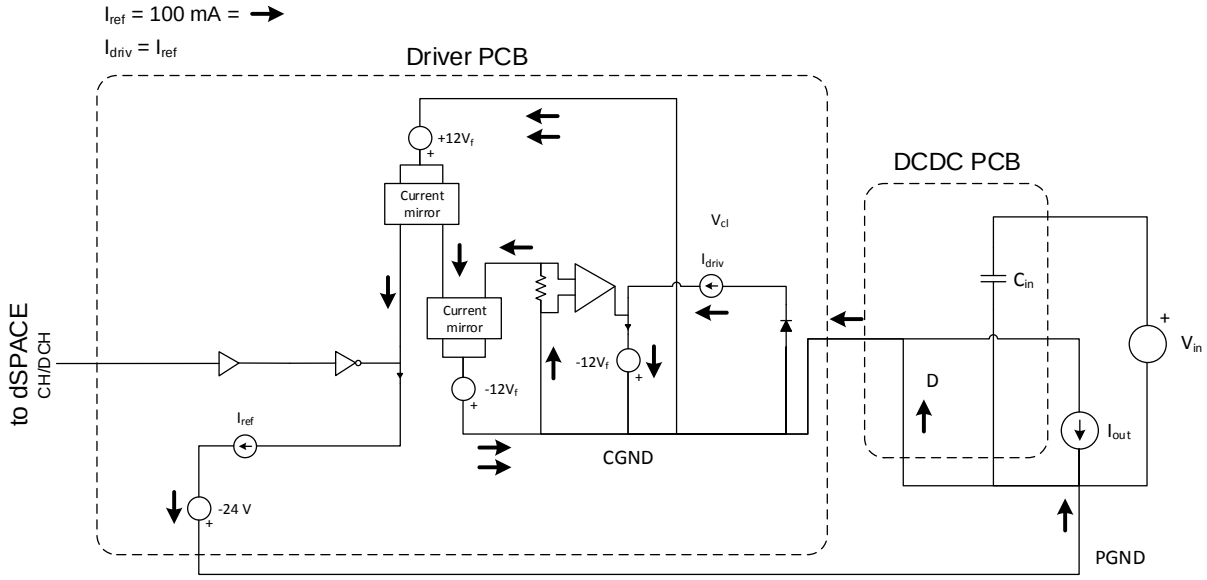

Figure 5.15: Concept drawing of the whole system to explain how the reference current circulates back to the driver through the converter during off-state

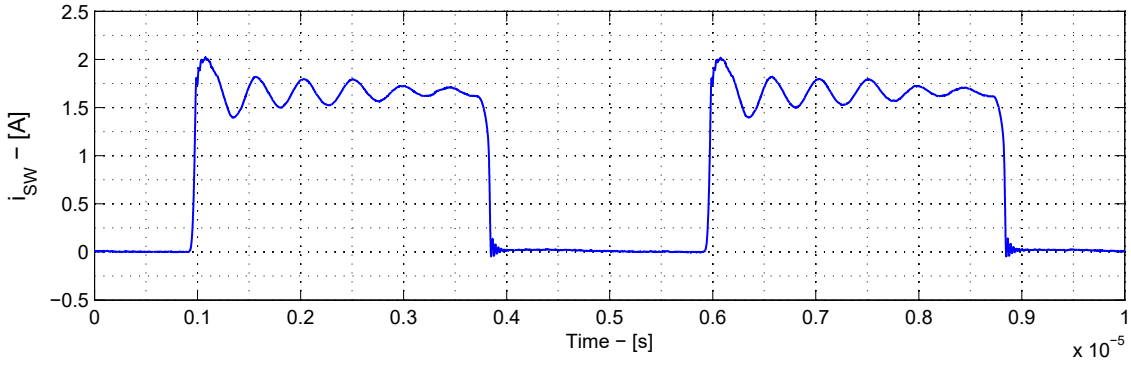

Figure 5.16: Current through the high side switch where the resonant response can be observed

5.8. Improving the prototype setup

The reference current generated internally by the driver will circulate through the hardware of the power converter as described in the earlier section. Such current will switch paths depending on the conduction state of the converter. Ideally, the current through the switch during the on-state should be equal to the output current plus the 100 mA of the reference current. Figure 5.16 shows the DMOS current for a switching frequency of 200 kHz. It can be observed how a resonant current circulates through the switch on top of the ideally expected squared current. Such behavior is not considered satisfactory: it will create additional losses and could affect the overall performance of the system. Further investigations will be carried out in the following subsection in order to eliminate it.

5.8.1. Floating supply issue

The resonance observed in figure 5.16 has its source in the parasitic capacitance added by the floating power supply. Figure 5.17 presents a concept drawing the whole system where the parasitic elements that play a role are identified. The parasitic inductance at the gate driver side have already been discussed earlier: they will be introduced by the PCB traces. The connecting wire between the DC/DC PCB and the reference ground will also contain some parasitic inductance and resistance due to the physical conductor used. In addition, the supply which is used to power the floating high-side driver will present a parasitic capacitance to its ground. Due to the AC mains, all supplies' ground will be connected together. This will create a loop through which the resonance can take place. The equivalent resonant circuit is shown at the bottom-left corner. When a transition from off to on takes place, the equivalent resonant impedance will trigger a response similar to what can be observed in figure 5.16 (the resonant path is highlighted in red). Similarly, when the switch is turned off, the diode will offer another path for the resonant current to circulate (the resonant path is highlighted in blue).

Several solutions can be adopted to solve the problem identified at this point:

- Using a 50 Hz isolation transformer. If the floating power supply is connected to the AC mains via a 50 Hz isolation transformer, the parasitic capacitance which was placed initially between source and ground can be partially eliminated. The transformer itself will present some parasitic capacitance but it will be smaller than that added by the power supply. This solution is simple and valid but the size, weight and cost of the solution are not advantages.

- Using a high-frequency isolation transformer. If the frequency at which the galvanic isolation is applied is brought up, the the size of the transformer will decrease significantly. This transformer will be now placed between the power supply and the driver PCB. That is, the floating power supply will still be connected to the AC mains. However, the galvanic isolation provided by the high-frequency transformer will eliminate the parasitic capacitance initially observed. This solution is more advantageous with respect to the 50 Hz transformer as for size and cost. Several solutions are commercially available and the difficulty of implementation would be relatively low. On the

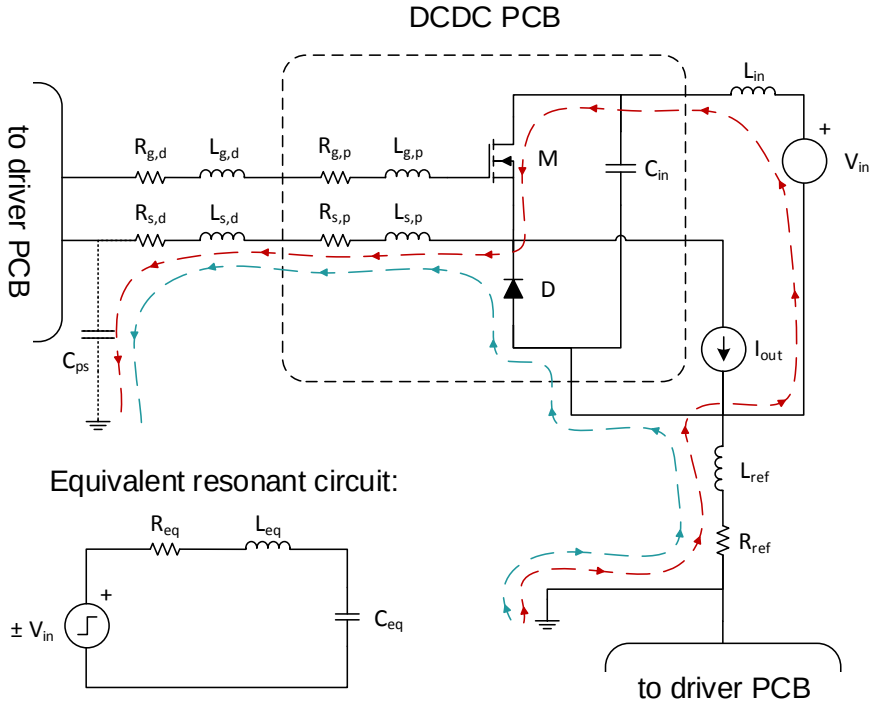

Figure 5.17: Concept drawing of the whole system to explain how the parasitic capacitance added by the floating power supply creates a resonance response

other hand, the driver PCB would have to be slightly modified. For further versions of system B, this approach would be a good choice.

- Using a battery. This will be the adopted solution due to its simplicity. If a battery is used to supply the high-side driver, no capacitance at all will appear between source and ground. The battery will float up and down with the source of the converter and any possible resonance will not happen since it will find no path to circulate.

Figure 5.18 plots the comparison between the original (driver powered by a grounded supply) and the improved approach (driver powered by battery). The reference current is measured at the wire that connects the DC/DC extension board to the absolute ground. It can be seen how the resonant response even dominates over the 100 mA expected DC value when the driver is powered by a grounded supply. If the battery is used the reference current becomes almost DC with a rough value of 100 mA. As for the switch current, it can be seen how the resonance yields an extra current circulation which will derive in additional losses. If the high-side driver is powered by a battery

To sum up, it can be concluded that using a battery to power the high-side floating driver solves the problem. The response of the converter with this approach can be considered acceptable and useful to validate further investigations. The next subsection of this chapter will focus on slightly improving the overall response of the system by proposing a new tuning of the reference current.

5.8.2. Tuning the driver reference current

As mentioned earlier, the reference current will create an additional power intake by the converter which will yield lower efficiency. The initial design of the driver board includes an internal reference current of 100 mA. For the current range at which the converter will have to operate, especially for the low power points, this amount of current will not be negligible at all. However, this internally generated current could be slightly modified or tuned to a different value. It has been discussed earlier in chapter 4 that system B makes use of active-feedback amplifiers to deliver the required amount of current to the gate of the DMOS. More specifically, the reference current is generated from a fixed voltage drop

Figure 5.18: Reference and switch currents for two different setups: high-side driver powered by grounded power supply and high-side driver powered by battery

across a resistor set by one of these operational amplifiers. Substituting the initially sized resistor will yield different values for the reference current. As expected, this will have an impact on the driver performance. A higher current will yield higher losses but at the same time would allow for a faster response up to some point; a lower current would slow down the operation of the driver but would increase the overall system efficiency.

All in all, a trade-off between performance and losses is the goal of the new tuning. After trying out several values for the driver reference current in practice, it has been concluded that a value of 20 mA still gives a good performance in terms of driving capability and brings up the efficiency considerably. That is, the reference current can be made 5 times smaller and the converter will still be able to operate in the same manner as before. The driver operation will still add some losses to the initial derived model that will have to be corrected in order to take this aspect into account. This will be discussed in more depth in future sections of this chapter.

5.9. Validating results using simulation

The root cause of the problems mentioned in earlier sections to which practical solutions have been provided can also be explained from a simulation point of view. The approach followed in practice the led to practical solutions was somehow iterative and supported by simulation. Simulation results are presented in this section in order to acquaint the reader with the whole picture. Let us first address the issue with the parasitic inductance introduced by the driver system. Figure 5.19 presents the results obtained from simulation to support the approach followed. The original setup makes reference to the initial setup of the driver which connected the source of the DMOS to the corresponding terminal at the driver PCB through the long inefficient trace (figure 5.5). It can be observed how the introduced inductance contributes to a resonant response with the parasitic capacitances seen at that node. Reducing such parasitic inductance will yield the results referred to as ”improved setup”. It can be seen how the switch waveforms are almost ideal now and the driver performance for the desired switching frequency can be considered satisfactory.

The issue related to the parasitic capacitance added by the grounded power supply can also be observed at simulation. If this introduced capacitance is added between the source terminal of the driver and the reference ground a similar response to that observed in practice is shown in simulation. Figure 5.20 plots the reference current and the switch current obtained from simulation for the two different setups. The ”original setup” waveforms are related to the case which includes the grounded

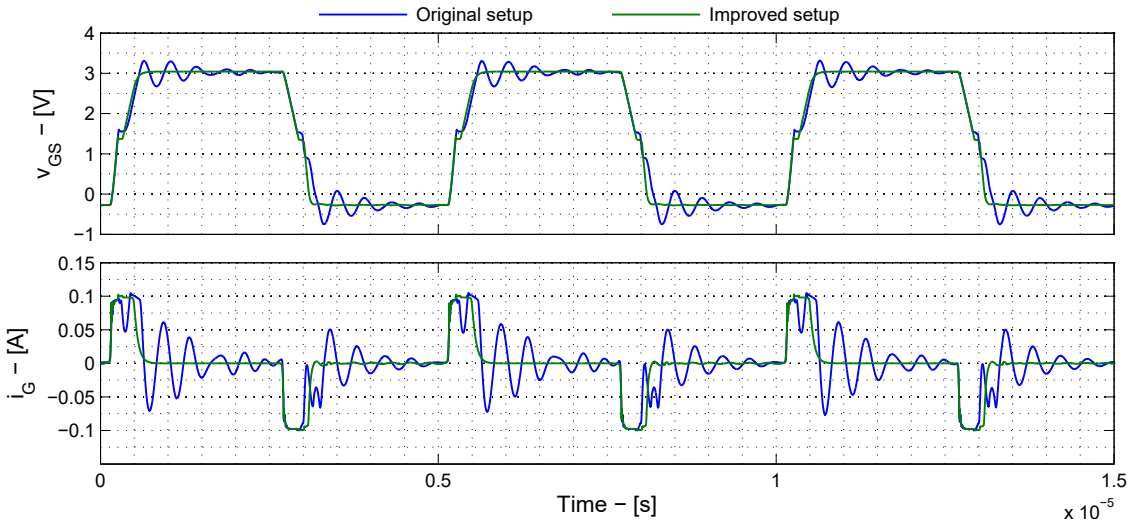

Figure 5.19: Simulation results obtained to validate the results of improving the driver setup to minimize the parasitic inductance. Gate-source voltage and gate current are plotted for the two different configurations

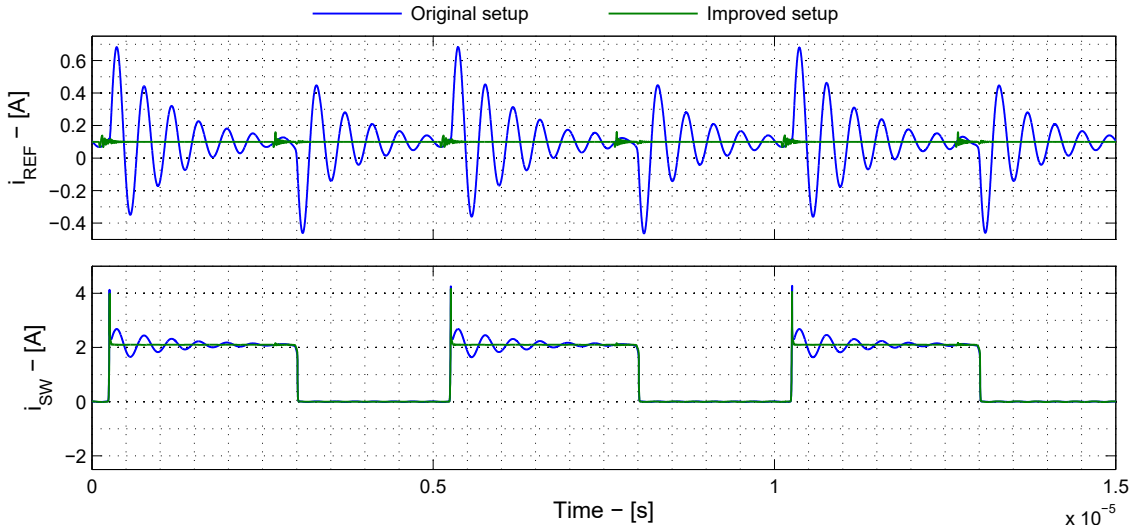

Figure 5.20: Simulation results obtained to validate the results of improving the driver setup to solve the floating supply issue. Reference current through ground and switch current are plotted for the two different configurations

floating power supply. A considerable resonant response can be observed by the introduced parasitic capacitance between source and ground. It will add a possible path for the oscillations to happen unlike what would ideally expected. This resonance will add to the reference current generated by the driver and which has to circulate back to the source terminal of the driver. During the on-state, the whole current will circulate through the DMOS, as can be seen in figure 5.20. The ideal and expected switch current should have a squared shape. If a battery is use instead to supply the high-side floating part of the driver, simulation gives the results referred to as ”improved setup”. The reference current will be now almost DC and with the expected value of 100 mA. The switch current will be much closer to the ideal waveform. It can be concluded then that simulation supports all measures taken in practice to improve the response and the quality of the waveforms of the converter.

5.10. Modeling the additional losses

The initially derived loss model has been shown to provide an inaccurate estimation of the overall system efficiency. This section focuses on improving such initial loss model by introducing two new

loss sources. The first of them will be related to the on-board measurement devices present on the designed DC/DC extension board. The second will be related to the previously discussed issue: the driver reference current that circulates through the buck converter back to the source terminal of the gate driver.

5.10.1. Measurement losses

The designed DC/DC extension board includes a series of measurement devices to be able to provide the control system, namely the dSPACE, with feedback signals. In practice, such sensing units will be implemented by means of physical elements that are not lossless. Let us first focus on the measuring element used to monitor the input voltage. The ADC channels of the dSPACE have a voltage range of $\pm$30 V. However, the input voltage could present a larger instantaneous value. For this reason, a voltage divider will be used to scale down the input voltage. Two resistors of 1 kΩ and 1.5 kΩ have been used for this reason. The measured signal can be expressed as:

$$V_{IN}^{ADC} = \frac{1.5k\Omega}{1k\Omega + 1.5k\Omega} \times V_{IN} = 0.6 \times V_{IN} \tag{5.3}$$

The voltage scaling by means of the resistor divider will yield an inherent current:

$$I_{div} = \frac{V_{IN}}{2.5k\Omega} \tag{5.4}$$

This current will dissipate heat in the resistors:

$$P_{div} = {I_{div}}^2 \times 2.5k\Omega = \frac{{V_{IN}}^2}{2.5k\Omega} \tag{5.5}$$

Table 5.4 presents the associated power losses for different values of input voltage. It can be seen how the larger the input voltage, the large the losses generated. This amount becomes especially significant for the low current range. If a voltage of 25 V is present at the converter, the power losses are even comparable to other loss sources of the converter. It can be concluded that the introduction of these losses to the model will considerably affect the estimated efficiency.

V_{IN} [V]	P_{div} [mW]
10	40
15	90
20	160
25	250

Table 5.4: Estimated losses generated in the input voltage resistor divider

In addition to the voltage divider, two current sensing units from Sensitec are present on the DC/DC extension board. According to the datasheet [62], the sensor presents a finite equivalent resistance between the two conducting terminals that are used to sense the current. According to the datasheet, the current of the primary conductor is, in the worst-case, 12 mΩ. The two current sensors will be placed accordingly to measure the coil and output current. It will be assumed that the power dissipated in the equivalent resistance can be expressed as:

$$P_{sens,I_L} = R_{EQ}\, I_L^{rms\,2} = 12m\Omega \times I_L^{rms\,2} \tag{5.6}$$

$$P_{sens,I_{OUT}} = R_{EQ}\, I_{OUT}^{rms\,2} = 12m\Omega \times I_{OUT}^{rms\,2} \tag{5.7}$$

Table 5.5 shows the power losses in each current sensor as a function of the rms current they carry. It can be seen how this power is significantly small for the low current range. However, if the sensed current becomes large enough, the power dissipated in the primary conductors of the sensor should be taken into account.

I^{rms} [A]	P_{sens} [mW]
0.1	0.12
0.5	3
1	12
2	48
4	192

Table 5.5: Estimated losses generated in the current sensor

5.10.2. Driver reference current losses

The driver reference current will affect the loss model in three different ways. First of all, the current the switch will have to carry will be slightly different to that expected from the ideal steady-state waveforms. The conduction and dynamic losses will be slightly larger than those initially estimated since the current the switch will have to carry is larger:

$$I_{SW,on} = I_{L,1} + I_{ref} = I_{L,1} + 20mA \tag{5.8}$$

$$I_{SW,off} = I_{L,2} + I_{ref} = I_{L,2} + 20mA \tag{5.9}$$

The larger the output current, the more negligible the reference current will be. The driver reference current will mostly have a significant impact on the switch losses for the low current range.

The driver reference current will also affect the diode losses in a similar way. The current that the diode has to carry during the off-state will be affected too:

$$I_{D,on} = I_{L,2} + I_{ref} = I_{L,2} + 20mA \tag{5.10}$$

$$I_{D,off} = I_{L,1} + I_{ref} = I_{L,1} + 20mA \tag{5.11}$$

Similar to the influence seen at the switch losses, the driver reference current will have an impact on the diode losses for the low current operating range.

Lastly, the reference current will yield an additional power intake by the converter from the input power supply. As described in figure 5.14, the input supply will have to let the reference current through, which will introduce an additional power term. This can be expressed as:

$$E_{ref} = V_{IN}\, I_{ref}\, D\, T_{SW} \tag{5.12}$$

$$P_{ref} = \frac{E_{ref}}{T_{SW}} = V_{IN}\, I_{ref}\, D \tag{5.13}$$

Table 5.6 presents the estimated additional power intake by the converter for a duty cycle of 50 % and an input voltage of 20 V. It can be seen how the losses are extremely large for a reference current of 100 mA (the initial tuning of the gate driver). With the new tuning of the internal reference current of 20 mA, the losses under these operating conditions equal 200 mW. This value must be taken into account but is five times smaller than that obtained for the initial driver setup.

5.11. Final open-loop measurements

The open-loop measurements performed using the initial prototype setup yielded results that were not consistent at all. Firstly, the efficiency curves did not match with the estimation provided by the loss model derived in chapter 3. Additionally, several initially unmodeled phenomena have been characterized in order to further improve the prototype setup. Originally, the driver reference current was not taken into account by the loss model. In addition, the sensing solutions incorporated on the DC/DC

I_{ref} [mA]	P_{ref} [mW]
10	100
20	200
50	500
100	1000

Table 5.6: Estimated losses generated by the reference current for a duty cycle of 50 % and an input voltage of 20 V

board and their contribution to the overall system losses was not modeled. On top of this, the reference current of the driver PCB has been further tuned to a lower value to bring up the efficiency for all operating points. All in all, the prototype has been severely improved with respect to its initial setup. Consequently, the results obtained at this stage will differ from those obtained at the beginning of this chapter.

Figure 6.1 presents a tilted view of the whole system configuration: the driver board lays horizontally on the test bench; the DC/DC extension PCB is connected to the driver board through the DIN connector and lies vertically. Figure 5.22 shows the prototype setup from an aerial perspective. Here, the different part of the system are highlighted in different colors: the green-shaded area corresponds to the part of the driver PCB which is used to interact with the external hardware, including dSPACE and other measurement units; the red-shaded area corresponds to the high-side driver contained in the driver PCB; the blue-shaded area corresponds to the DC/DC extension board. The parts of the driver PCB that are not shaded are not used by the application analyzed in this thesis work.

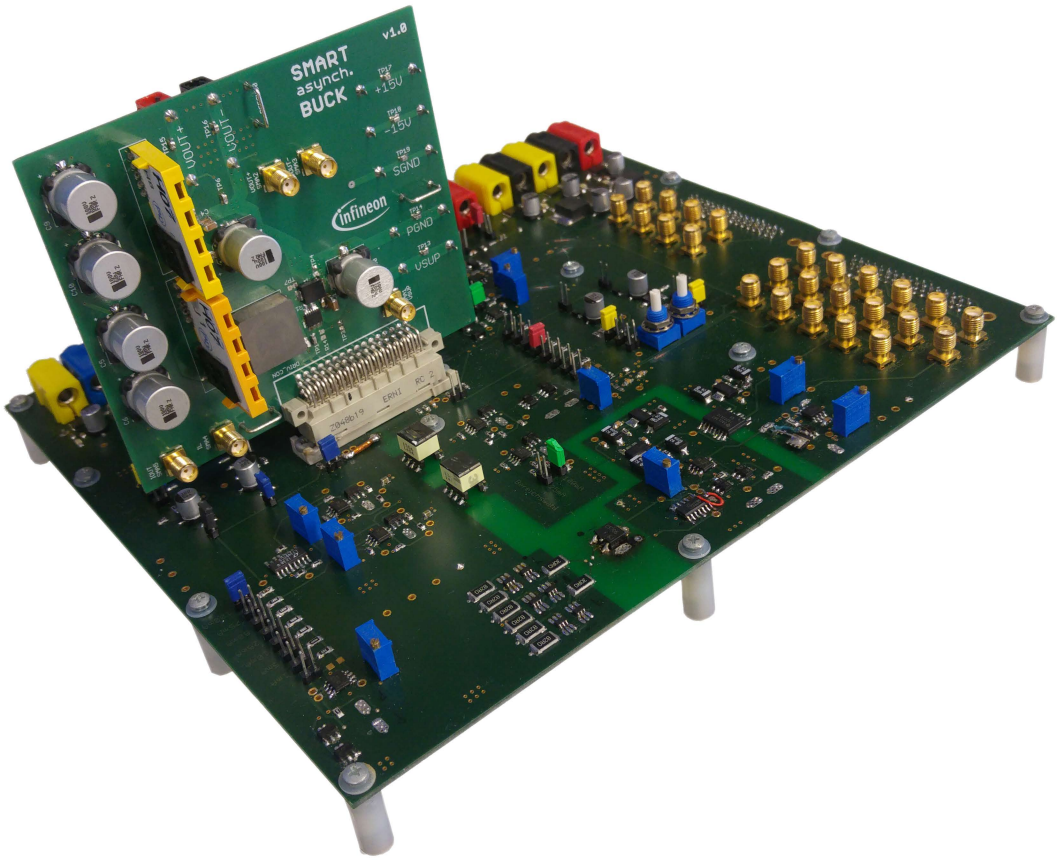

Figure 5.21: Tilted view of the whole system prototype, including the driver PCB (horizontal) and the DC/DC extension board (vertical)

Assuming that the improvement of the loss model and the prototype setup presented and justified

earlier in this chapter are overall satisfactory, the results obtained at this points should be much more solid. That is, in terms of efficiency, the measured curves should be matching with the estimation provided by the loss model. The comparison between the efficiency measurements on the final prototype setup and the the efficiency estimated by the loss model will be presented in the following subsection.

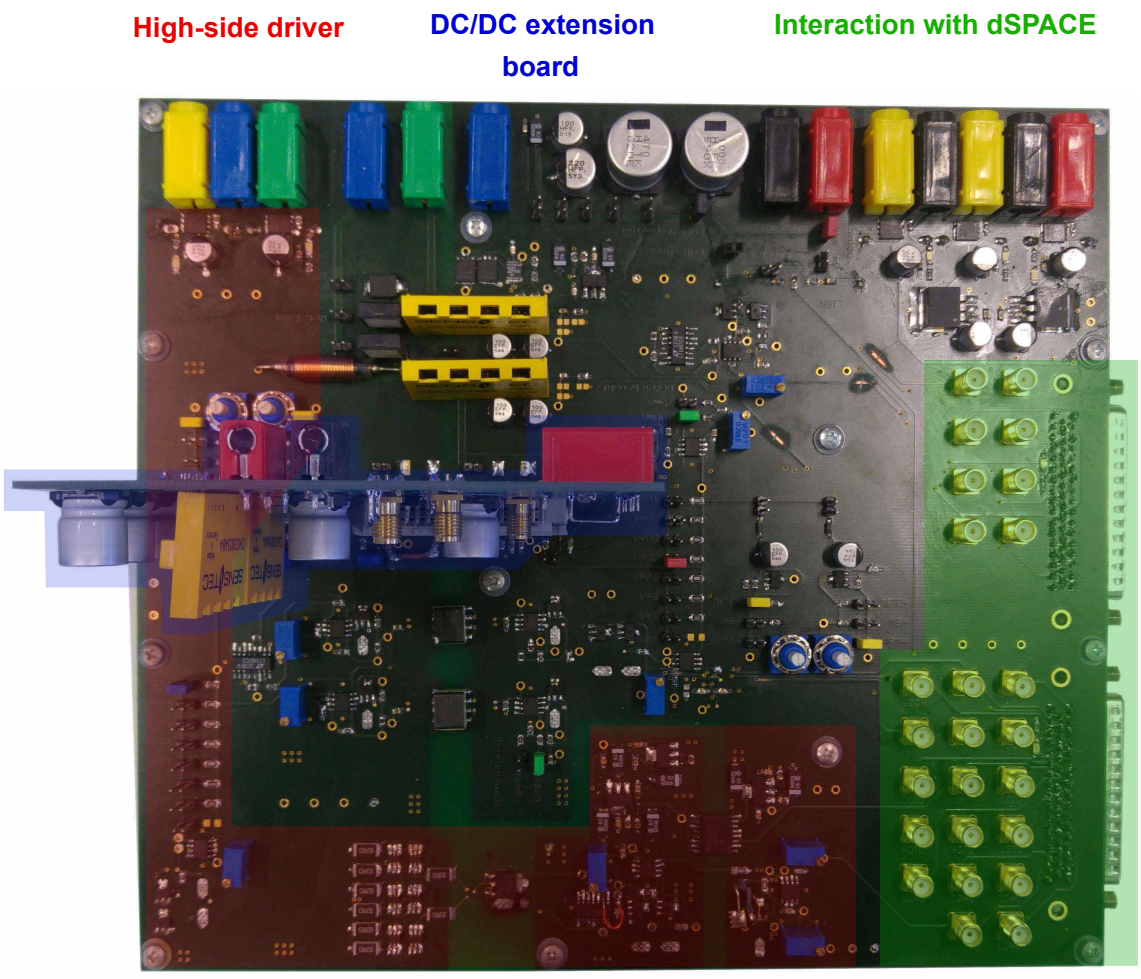

Figure 5.22: Top view of the prototype where the different parts of the system are highlighted

5.11.1. Comparing the efficiency measurements and the loss model

Figures 5.23, 5.24, 5.25 and 5.26 show the comparison between measured and estimated efficiency for a switching frequency of 50, 100, 200 and 400 kHz respectively. It can be observed how the matching is overall very good. The discrepancies initially seen for low-current points are corrected in the set of measurements presented here. This improvement can be mainly explained by the inclusion of sensing and driver reference current losses in the loss model and the correction of the actual transition times used to estimate the dynamic switch losses. As for the former, they will be constant and very dominant for the low-current operating region. The lower the current, the more dominant they will be. As for the driver reference current, they will add an initial power intake which is not negligible for any operating point. Similarly, the correction of the switching times will yield larger switch losses which will bring both estimation and measured curves closer to each other.

The previous set of measurements also showed a mismatch at the high current range. The newly obtained efficiency curves significantly reduce these discrepancies. This is mainly due to the introduction of the driver reference current in the loss model and to the correction of the transition times of the DMOS observed in practice. The former will introduce a relevant amount of power initially not taken into account by the loss model. The latter will produce a larger estimation of the switch dynamic losses.

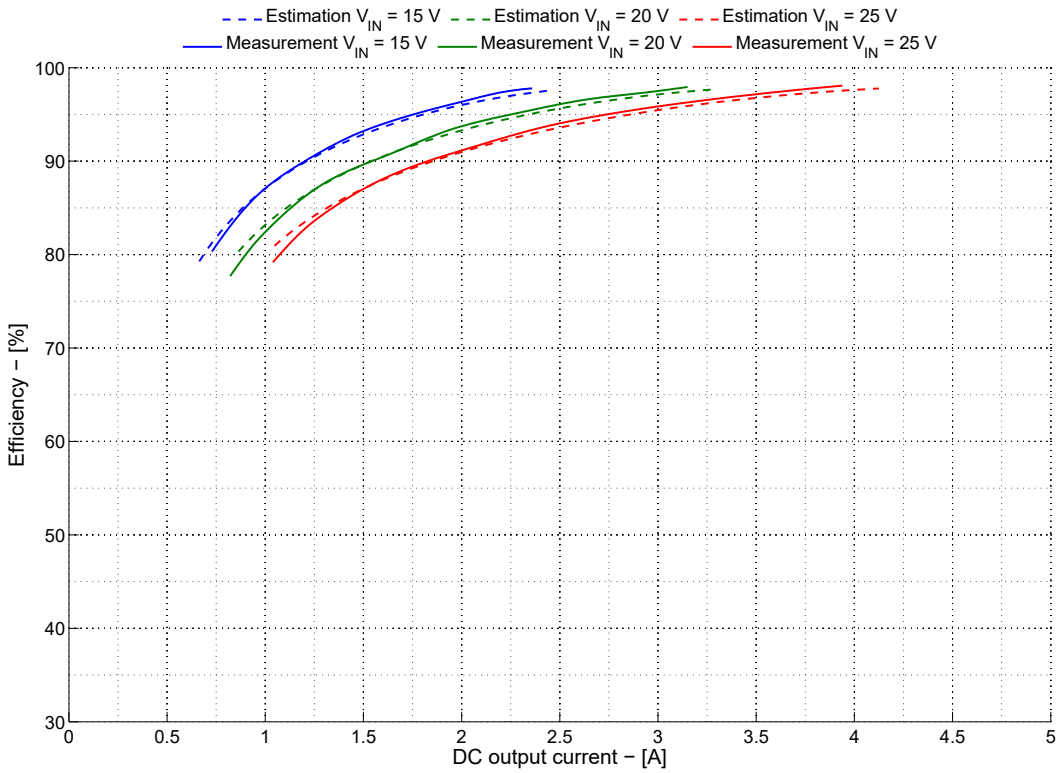

Figure 5.23: Comparison between estimated and measured efficiency with the improved prototype setup for a switching frequency of 50 kHz and different values of input voltage

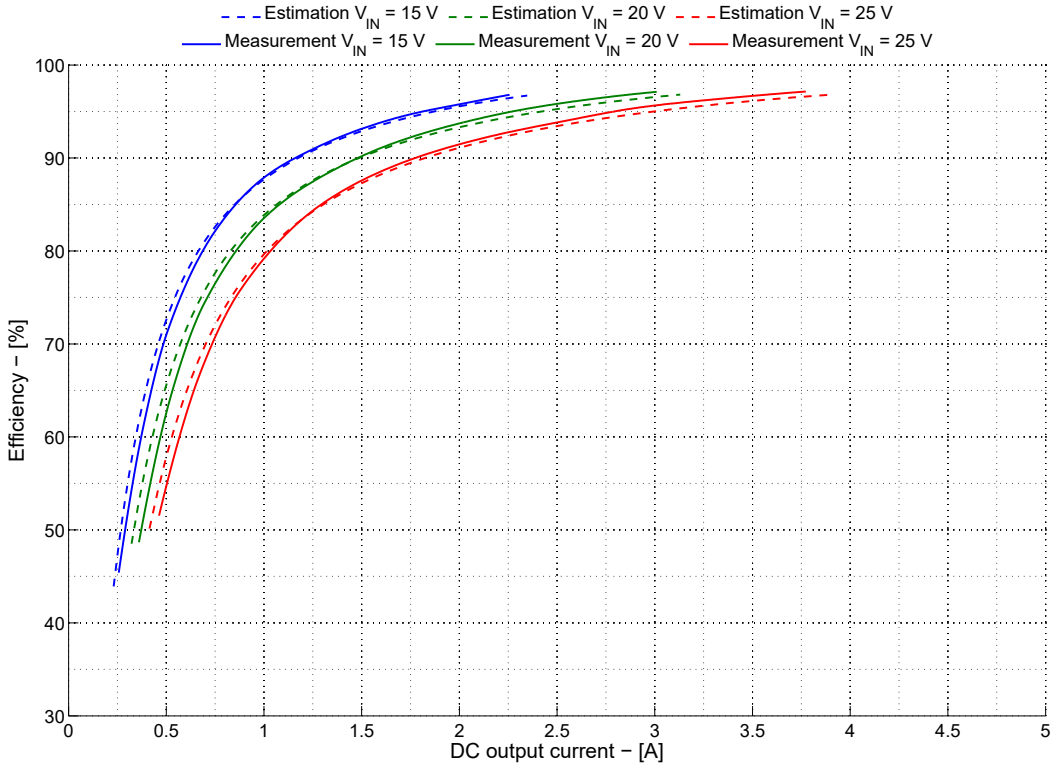

Figure 5.24: Comparison between estimated and measured efficiency with the improved prototype setup for a switching frequency of 100 kHz and different values of input voltage

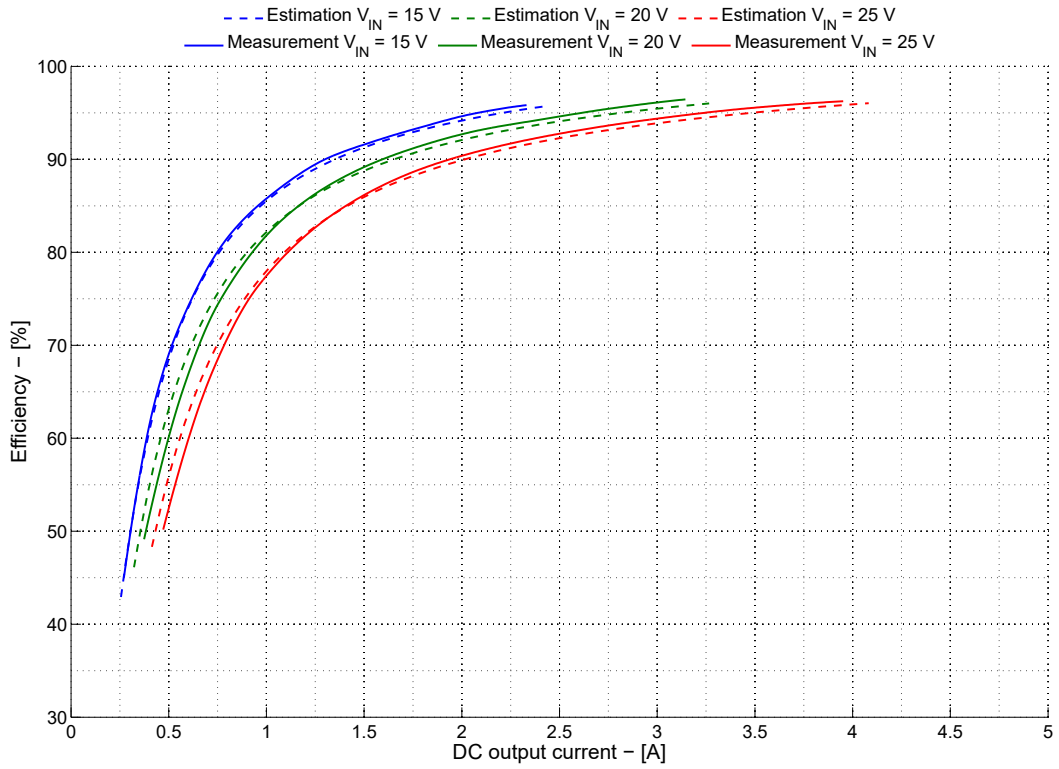

Figure 5.25: Comparison between estimated and measured efficiency with the improved prototype setup for a switching frequency of 200 kHz and different values of input voltage

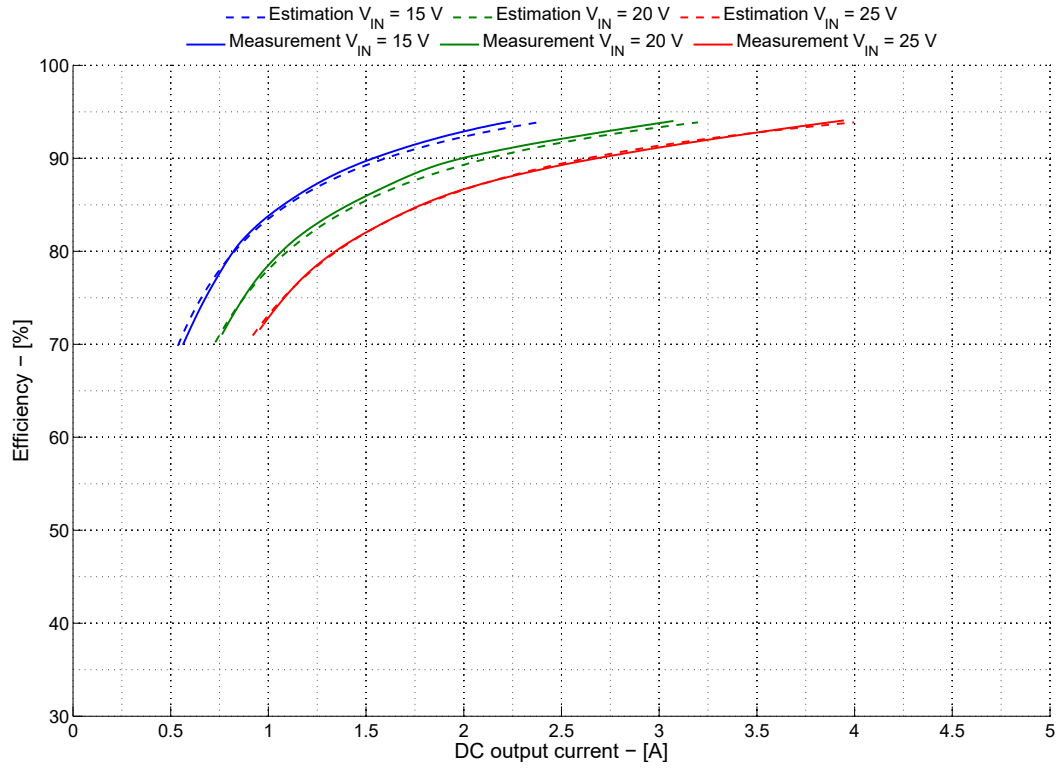

Figure 5.26: Comparison between estimated and measured efficiency with the improved prototype setup for a switching frequency of 400 kHz and different values of input voltage

Altogether, estimation and measurements will be brought closer to each other and the matching can be considered very good and solid at this point.

With regard to the shape of the efficiency curves observed, they are as expected. Low-power points are characterized by the handling of a small amount of power. This will yield a lower efficiency, due to the fact that the sum of all loss mechanism is relatively large compared to the power transfer characteristics of this operating region. Larger and larger current will increase the amount of power handled by the converter. The growing rate of the losses will be lower than the growing rate of the transferred power. Consequently, the overall computed efficiency will be larger. Additionally, it can be observed how the slope of the efficiency curves is always positive. That is, if the system is to be operated for larger and larger currents, the efficiency must be expected to keep increasing. The loss modeling can be confirmed to be very satisfactory and solid now.

Let us focus on figure 5.23, which presents the efficiency curves for a switching frequency of 50 kHz. Firstly, it can be observed how the operating range is somehow narrow compared to other switching frequencies. This is mainly due to the large ripple created by the converter for such small switching frequency. Therefore, the continuous conduction will only be granted for large current operating points. Besides and as expected, the overall efficiency decreases with an increasing input voltage level. The main cause can be found in the dynamic switching losses becoming larger and larger with the input voltage. The peak efficiency is roughly measured and estimated at 98 %.

Figure 5.24 focuses on the efficiency for a switching frequency of 100 kHz. For these conditions. it can be seen how the operating range significantly broadens at the low-power region. This is due to the ripple becoming half of that obtained for 50 kHz. This will allow for continuous conduction mode at lower power operating points. As mentioned earlier, the efficiency decreases with an increasing input voltage level due to the dynamic switch losses becoming smaller and smaller. On top of this, it can be observed how the overall values of efficiency are slightly lower than those obtained for 50 kHz. Increasing the switching frequency will have a twofold effect: some losses will increase (for instance dynamic switch losses) and some others will decrease (coil losses due to ripple current). The overall change will be a net increase of losses which will yield lower efficiency. The peak value for 100 kHz is roughly 97 %.

If the frequency is pushed higher, the coil current ripple will be reduced. Figure 5.25 presents the efficiency curves for 200 kHz. However, the broadening of the operating range due to the ripple becoming lower and lower with an increase in the switching frequency is not observed at this figure. This is due to the fact that the limitations related to the driving of the DMOS impose now a limit on the duty cycle. That is, due to the limited current capability of the gate driver, the switch cannot be commuted at any duty cycle; on the contrary, this will yield a minimum duty cycle at which the operation of the converter is feasible. The peak efficiency observed for 200 kHz is approximately 96 %.

Lastly, the efficiency curves obtained if the converter is operated at 400 kHz are plotted in figure 5.26. For these conditions, the current capability of the gate driver also yields a stretching of the operating range. The switching period is much smaller compared to previous conditions and the system is much more sensitive to the limitations of the gate driver. However, the obtained efficiency is still good enough. Once more, it can be seen how increasing the switching frequency yields a net decrease in system efficiency. The peak can be now roughly observed at 94 %.

Overall, the improved loss model yields very solid estimations for all switching frequencies and operating conditions. Additionally, the new tuning of the driver reference current cause an increase in efficiency. The newly proposed tuning reduces this reference current by five times. Therefore, the additional power intake due to this term will be made five times smaller.

5.11.2. Analyzing the converter waveforms

The efficiency of the converter has been discussed in the previous subsection from both measurements and estimation results. These curves characterize the converter as for the power transferring capability and give an overview of how dominant the losses are with respect to the total handled power. Another relevant aspect of a power converter is related to the generated waveforms. A set of equations and expressions have been derived earlier in this document assuming a quasi-ideal behavior of the converter. In practice, the obtained waveforms will differ slightly from these. However, another interesting

way to evaluate the quality of a power converter design can be based on how close to the ideal case the actual operation is. Figures 5.27, 5.28, 5.29 and 5.30 plot the most interesting waveforms of the buck converter in steady-state for different switching frequencies to evaluate the actual operation of the system.

It can be seen how the first subplot of all figures (gate-source voltage) presents the expected behavior and is very close to what could be ideally expected (a square wave). The higher the frequency is pushed, the more dominant the transitions will be with respect to the total switching period. During the on-state, the gate-source voltage is clamped to 3 V by the high-side driver output circuitry; during the off-state, it equals a small negative value due to the voltage drop of the forward biased diode of the negative clamping circuit. Any resonant response that could be observed with the original prototype setup is not present at all with the improved prototype.

The gate-source voltage is mainly determined by the gate current. It will determine the speed at which the capacitances seen at the gate are charged and therefore influences the switching of the DMOS. Let us assume the DMOS is initially off and at a certain point in time the charging of the gate is initiated. Initially the driver will peak to its current level (100 mA) or a value close to it. This will rapidly charge the gate of the switch. Since the clamping circuitry of the high-side driver is non-ideal, it will start to draw current before the gate-source voltage reaches its final value. If the switching frequency is small enough (namely 50 kHz), the gate current will be seen as a single pulse that approaches zero with the charging of the gate. If the frequency is pushed higher (namely 400 kHz) some resonance will be comparable to the overall waveform. This is mainly due to the parasitic elements of the clamping circuit that play a role when they start conducting. However, its effect will not affect the performance significantly for the scope of this work. An analogous explanation can be given for the discharging of the gate. Altogether, it can be confirmed that the driver is able to provide the required amount of current to the gate of the DMOS to allow for switching at frequencies in the order of 400 kHz.

The switching node is also a very relevant point of the converter: it summarizes the operation of the whole switching leg (DMOS plus diode) and can be assumed to be the input of the LC filter. Ideally, the switching node voltage is a square wave that clips between ground and input voltage. In practice, the switching of the leg will take a finite amount of time required to charge and discharge the equivalent capacitances. For a relatively low switching frequency (50 kHz), the ideal waveform will almost be observed in practice. The more the frequency is pushed, the more dominant the transition times will be. The switching node voltage also present a nonideality in term of duty cycle distortion. The control of the converter (the dSPACE) will send a command duty cycle by means of a digital input/output. This will influence the times at which the driver charges and discharges the gate of the DMOS, and consequently the times at which the switching node rails up or down. However, this charging and discharging process takes a finite amount of time. If the frequency is high enough, the finite transition time will affect the actual duty cycle that the output LC filter sees. As expected, the higher the switching frequency, the higher the deviation between control and actual duty cycle. This can be seen at the two boundary conditions, figures 5.27 (50 kHz) and 5.30 (400 kHz). The control duty cycle is 50 % for both plots but the actual duty cycle considerably changes for 400 kHz. On top of this, it can be seen how the finite resistance of the DMOS introduces a small voltage drop during on-state. On the contrary, the diode voltage drop makes the switching node voltage slightly negative during off-state.

Perhaps the most relevant waveform of a buck converter that will be used as a current driver is the coil current. In steady-state, the average value of the coil current will be equal to the average value of the output current. Assuming that the output voltage is constant and the switching node is a square wave, the current through the coil should be triangular. Ideally, it is also assumed that the inductance of the coil remains constant. It has been mentiones that the switching node voltage deviates from a square wave with an in increase in switching frequency. Accordingly, the coil current will deviate from the ideally expected triangular waveform. What is more (it will be discussed in the next paragraph), the output voltage will present an alternating component. Lastly, the effective inductance of the coil will be dependent on many factors (for instance temperature, DC current bias...). All in all, the measured coil current will present some nonidealities as well. However, it can be seen that for all plotted measurements the results are very close to a triangular wave whose DC value equals the average output current. As expected, the ripple will decrease with the switching frequency. Let us focus on the current seen for 50 kHz: the slope during on and off-states is almost constant (it varies slightly due to inductance change). If the switching frequency is made higher and higher, the on and off slopes become

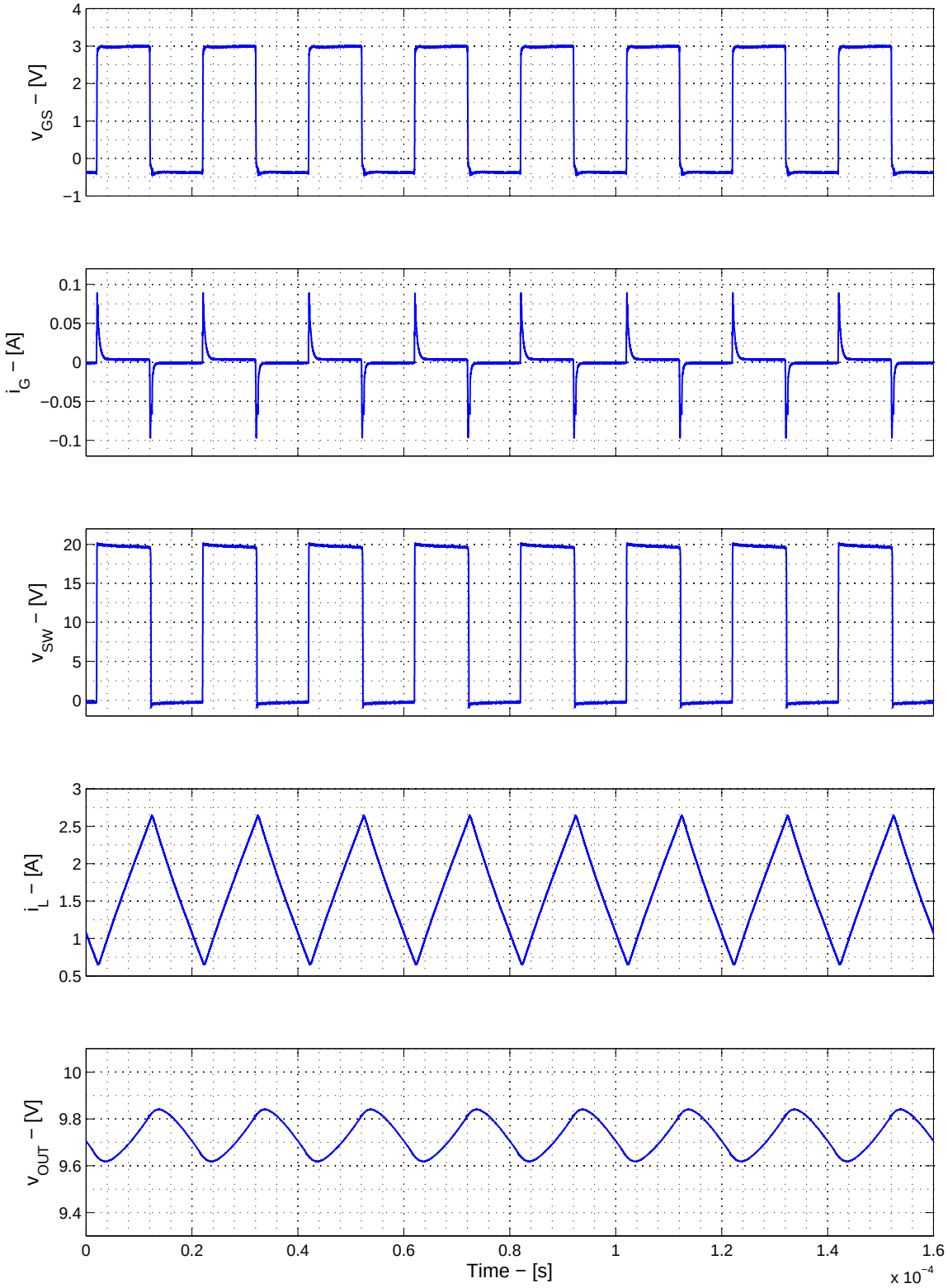

Figure 5.27: Steady-state converter waveforms (gate-source voltage, gate current, switching node voltage, coil current and output voltage) measured on the improved prototype setup for a switching frequency of 50 kHz, an input voltage of 20 V and a control duty cycle of 50 %

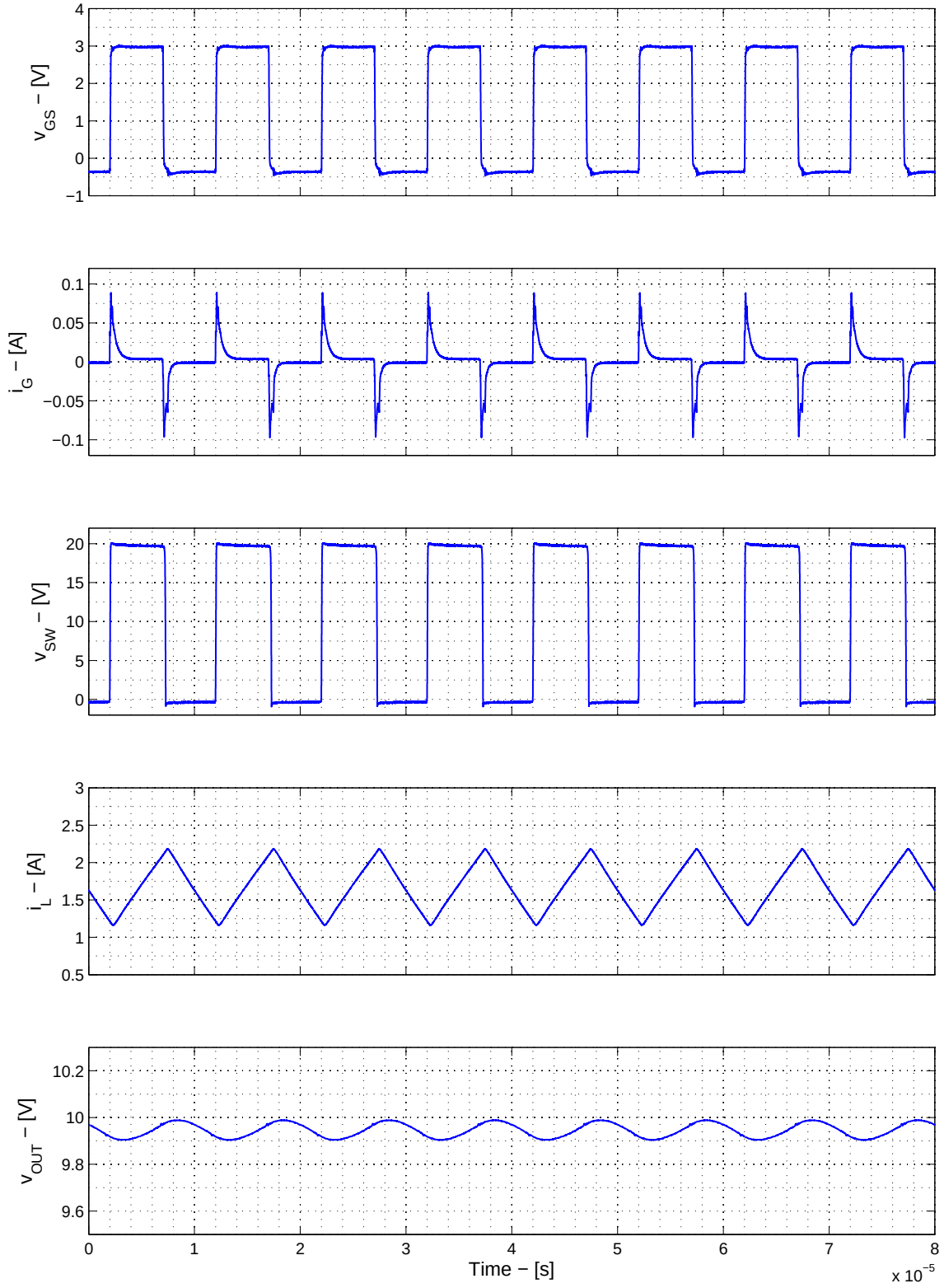

Figure 5.28: Steady-state converter waveforms (gate-source voltage, gate current, switching node voltage, coil current and output voltage) measured on the improved prototype setup for a switching frequency of 100 kHz, an input voltage of 20 V and a control duty cycle of 50 %

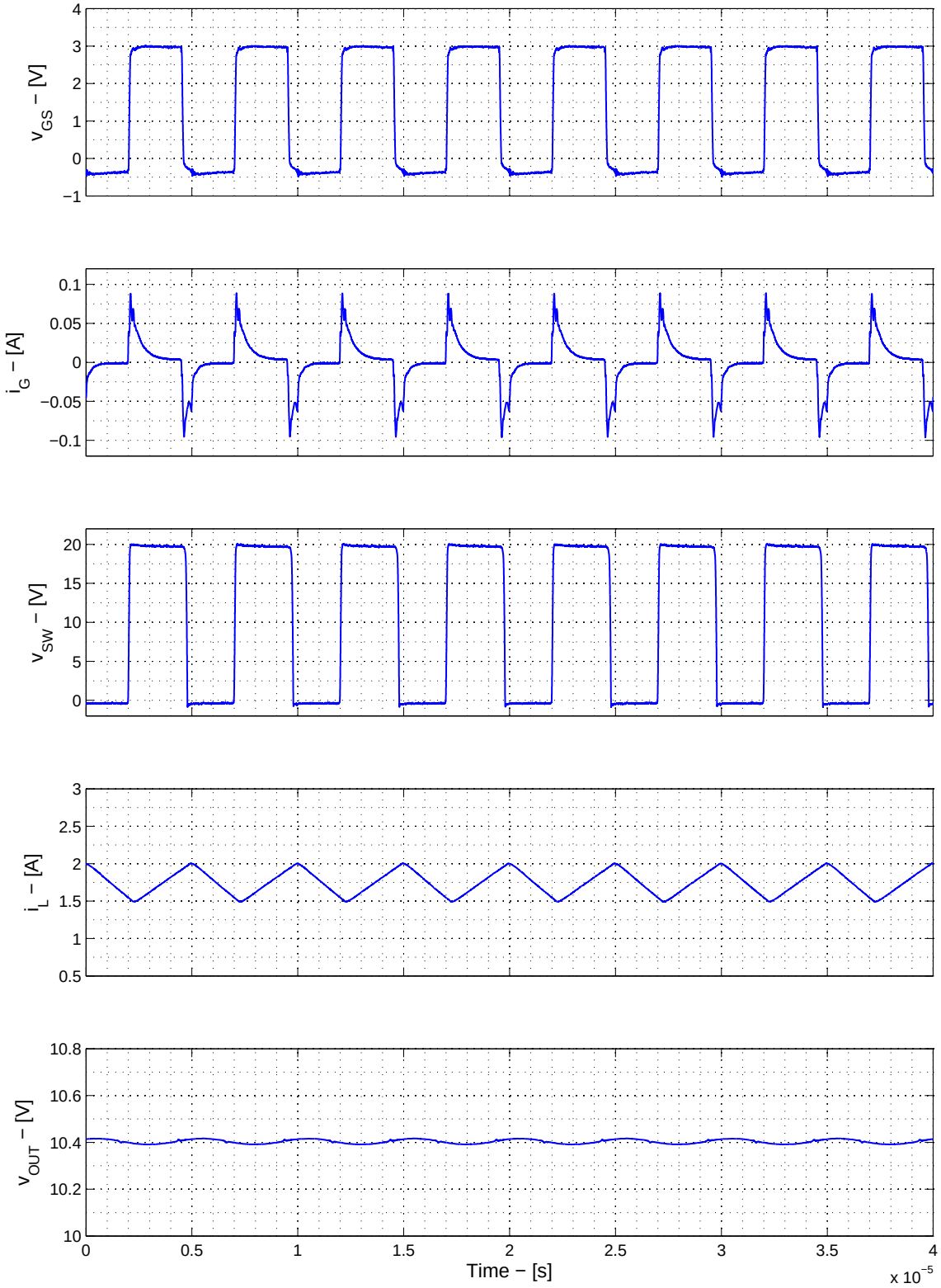

Figure 5.29: Steady-state converter waveforms (gate-source voltage, gate current, switching node voltage, coil current and output voltage) measured on the improved prototype setup for a switching frequency of 200 kHz, an input voltage of 20 V and a control duty cycle of 50 %

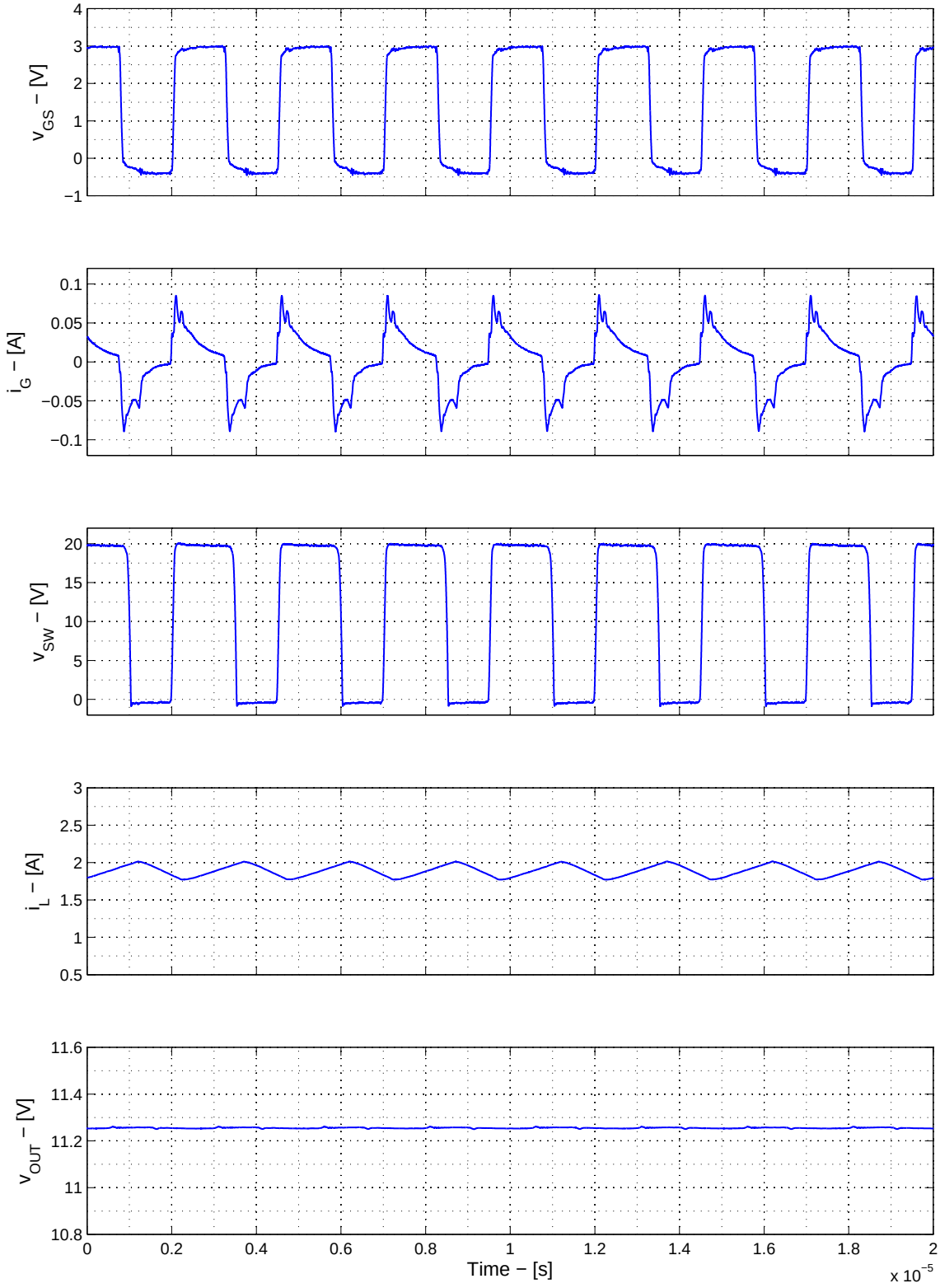

Figure 5.30: Steady-state converter waveforms (gate-source voltage, gate current, switching node voltage, coil current and output voltage) measured on the improved prototype setup for a switching frequency of 400 kHz, an input voltage of 20 V and a control duty cycle of 50 %

more and more constant since the coil is operating in a narrower current range. However, it can be seen how the finite transition times round the peaks of the coil current. The deviation between control and actual duty cycle can also be observed by looking at the slopes of the coil current. In addition, it can be concluded that no saturation takes place since the effective inductance stays almost constant.

Lastly, the output voltage is a relevant waveform of the buck converter. It will be composed of a DC component and an alternating voltage that is mainly determined by the coil current ripple and the filtering properties of the output capacitor. If this capacitor presents no equivalent series resitance, the output ripple will be given by the integration of the triangular ripple current by the capacitive behavior of the passive element. In practice, however, this is not the case. The finite resistance of the capacitor will add an AC voltage proportional to the ripple current. The larger the current ripple, the larger the voltage ripple will be then. This can be clearly observed in figure 5.27: the shape of the output voltage ripple is a combination of the triangular shaped resistive drop and a quadratic term given by the capacitive element. If the frequency is brought up, for instance 200 kHz (figure 5.29), it can be seen how the ripple becomes lower and the voltage ripple becomes mainly quadratic. As expected, the higher the switching frequency, the smaller the output voltage ripple will be. In fact, figure 5.30 shows how the voltage ripple becomes almost negligible.

5.12. Conclusions

The analysis carried out and discussed in this chapter started off by presenting the concept designed to improve the prototype of the system. The results obtained initially were not satisfactory enough and several possible root causes were identified in order to come up with a better setup. The DC/DC extension board has been designed to optimize the behavior of the system and minimize any possible parasitics that could degrade the performance of the converter. Firstly, the focus was set on minimizing the parasitic inductance seen at the gate of the switch. The improvement has been confirmed to be effective and matching with the expected results. Further steps led to conclude that the initially derived loss model was not accurate enough and that further investigations had to be performed in order to pinpoint the mismatch. The experimental determination of diode and switch losses using modified setups led to a deeper analysis on an initially unmodeled phenomenon: the driver reference current. A couple of modifications have been proposed in order to obtain an even more solid prototype (floating supply issue and new tuning of the reference current). Overall, the improvement of the prototype was characterized by a series of upgrades that gave rise to others at the same time. Simulation was also used to confirm the results observed in practice. In the end, the final setup presents a solid and satisfactory performance.

The corrected loss model takes into account practical transition times of the DMOS. Those observed in simulation corresponded to a converter without any parasitics. In practice, any capacitance added to the switching node will slow down the transitions and will have thus an impact on the overall performance. Also, the inclusion of the losses related to sensing elements present on the DC/DC extension board have been confirmed to bring both measurement and estimated efficiency curves closer. Altogether, it can be concluded that the loss model provides very accurate results for all tested operating conditions and could be used to optimize the converter in terms of selected components. What is more, it can be deduced that the modeling of the coil losses based on parameters provided by the manufacturer is accurate enough.

As for the efficiency of the converter, it can be observed how the values measured at the lab are sufficiently good: peak efficiencies of 98, 97, 96 and 94 % are obtained for 50, 100, 200 and 400 kHz respectively. The curves show a considerable efficiency drop for low current points, which can be expected by having a look on how the different mechanisms contribute to the whole losses. It has also been confirmed that increasing the switching frequency yields lower efficiency for a given output current. On the other hand, increasing the switching frequency would allow for smaller and cheaper passive elements to meet the electrical requirements of the converter. On the whole, this aspect appears as a trade-off between the size and cost of the converter and its efficiency. The focus of this thesis work is not put on this regard; it focuses on the feasibility of Infineon's smart technology for DC/DC applications. Further development stages will tackle this aspect from a more particular point of view, when the application-specific requirements are available to the designer. At this point of the study, it can be concluded that Infineon's DMOS can be switched at a frequency of 400 kHz with a gate

current level of 100 mA.

It has been mentioned earlier in the discussion that the efficiency always shows a positive slope. This could mean that the analyzed DMOS is actually overdimensioned: if a smaller amount of silicon were used, the switching of the device would be faster. As a result too, conduction losses would increase. This trade-off should have to be taken into account to dimension the DMOS to the optimum size required by the application. This aspect will be discussed in more depth in the last chapter where potential future work is presented.

As a final conclusion, the validity of the obtained results leads to confirming that the prototype can be used to further analyze and study the control of the converter. So far, the system has been run open-loop. That is, the dSPACE was set to give a fixed command to the driver board in order to run the converter at a given duty cycle no matter what the output signals were. In practice, the converter will be used in a smarter way: one or several control loops will be established making use of electrical quantities that will yield command signals from the dSPACE to the converter hardware. With this approach, the converter can be effectively used as an LED driver. This analysis will be performed and discussed in the following chapters.

6

Controlling the converter

The sixth chapter of this document addresses the control aspects of the converter previously designed and optimized. Section 6.1 sets out the requirements for the control of the converter and the elements that will be taken into account for its design. Section 6.2 gives an introduction on the methodology that will be followed to evaluate the stability response of the control system. Different schemes and topologies will be presented from a theoretical point of view in section 6.3. First of all, the traditionally implemented voltage mode control loop will be introduced. As an alternative, peak-current-mode control and average-current-mode control will be presented and compared to each other. The approach followed to obtain the converter transfer functions and the loop gain will be discussed in section 6.4. Once an AC linear model of the converter is derived, the most suitable control scheme, namely the average-current-mode control, will be analyzed and designed in detail in section 6.5. Simulation results of the DC/DC converter working in closed loop using the previously designed compensation will be shown in section 6.6 to evaluate its transient performance.

6.1. Motivation

So far, the converter prototype has been analyzed in open-loop operation. That is, the gate driver is set to switch the DMOS at certain duty cycle and switching frequency. The obtained response will be a function of several variables such as input voltage and output load. A change in any of these will cause the operating point to drift away from that initially set. In practice, converters operate in a smarter way. More specifically, they behave as regulators. In other words, the converter will be able to operate regulating certain parameter to a reference value no matter what other variables are. As it has been mentioned before, the converter developed in this thesis work is aimed to serve as a flexible hardware platform to perform system-level analysis before the actual integrated circuit is designed. Hence, the applications in which it could be used to draw practical conclusions are numerous. On the one hand, some LED loads may require a current source to drive them; on the other hand, it may also be necessary that the converter would act as a voltage source to drive LED loads. The latter will be considered as the application of interest in this chapter, although the same approach could be used to operate the buck converter as a current source.

Figure 6.1 shows the schematic drawing of the application that will be analyzed with a simplified control loop. The system will act as a voltage source that sets the output voltage to a specific value. This way, the LED modules that are paralleled at the output of the converter will present a continuous luminous response. Each of these modules will typically include an internal regulation method to balance the current drawn from each branch. If the load changes, that is, if the number of LED modules that are connected to the converter changes, the regulator must guarantee that the voltage will remain constant. Additionally, if the input voltage presents variations, the regulator must be able to reject them by keeping the output voltage unaltered.

From a requirement point of view, the regulator will have to fulfill a set of requisites. First of all, the control will have to compensate for load current variations. This will appear as an upper limit for

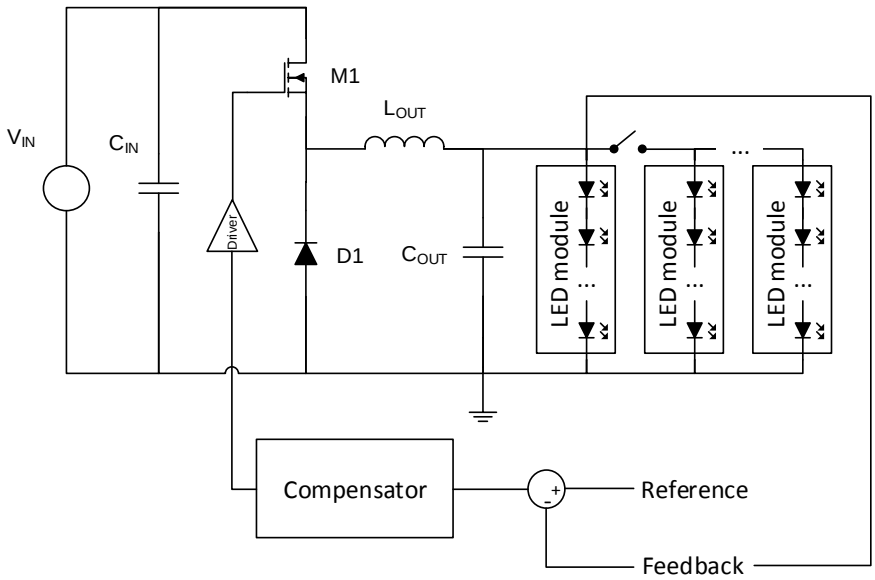

Figure 6.1: Concept drawing of the converter including schematic and simplified control loop

the output impedance that the regulator can drive. Besides, the control will also have to compensate for line voltage variations that could transfer to the output. Similarly to load current variations, this will translate into the design as a limit for the line-to-output transfer function. The transient response time will also be a very important parameter to evaluate the response of the regulator. This smart operating of the converter will be possible by introducing the so called compensator or controller. From a control theory point of view, it will modify the loop gain of the system such that all specifications could be met. As for its design, the methodology followed will be based on meeting certain requirements related to crossover frequency and phase margin. All these aspects will be discussed in further sections of this chapter.

6.2. Stability analysis

It will be shown later in this chapter that the converter in open-loop can be modeled as a transfer function, for instance, from duty cycle (control) to output voltage. This way, the converter can be seen as a control system with a set of poles and zeros located at different frequencies. Closing the loop by means of introducing a compensator will have an effect on the final system. In fact, the closed loop transfer function will be different to that observed in open loop. Closing the loop effectively moves the poles of the loop gain. This could yield instability if some of the poles fall on the right-half plane. What is more, the system can be still stable but present a very oscillatory response which is not satisfactory for a given application.

The stability of the closed-loop system can be analyzed using the phase margin test. This makes use of the so called loop gain, that is, the gain of the elements that form the loop placed in series. It will be discussed later in this chapter that the loop gain can be expressed for a given topology (including both the converter and the compensator). Then, the magnitude and phase of the resulting transfer function will determine whether the system is stable or not. Let us express the loop gain as T(s). Then, the crossover frequency can be defined as:

$$||T(2\,\pi f_{cross}\,j)|| = 1 \tag{6.1}$$

Where $s = 2\,\pi f\,j$ to evaluate the response of the transfer function for a given frequency. That is, the crossover frequency is defined as the frequency for which the magnitude of the loop gain equals unity. Then, the phase margin can be expressed as:

$$\varphi_{PM} = 180° + \angle T(2\,\pi f_{cross}\,j) \tag{6.2}$$

In other words, the phase margin is the difference with respect to 180° of the loop gain phase at the crossover frequency. The phase margin test dictates that the system can be considered stable if its phase margin is larger than zero degrees.

This can also be explained qualitatively: a phase shift of -180° (phase margin of 0°) would imply a positive feedback which could make the system unstable. On the other hand, the crossover frequency marks the unity gain range: signals with frequency components above the crossover frequency will be damped out by the control loop itself and will not make the system unstable; signals with frequency components below the crossover frequency will be amplified by the control loop. The phase shift of these points must be equal or lower than 180° in order to avoid positive feedback that would cause instability. The phase margin relates to how far the system is from becoming critically stable: if the phase margin is negative, frequency components below the crossover frequency that are amplified by the control loop will feed back with a positive sign. As expected, this will make the overall control system unstable; if the phase margin is positive, positive feedback will not take place and the system could be considered stable.

Additionally, the phase margin will be strictly related to the quality factor of an equivalent second order transfer function. In practice, most converter transfer functions can be approximated in the vicinity of the crossover frequency as such. Let us express this as:

$$T(s) = \frac{1}{1 + \frac{s}{Q\,w_{cross}} + \left(\frac{s}{w_{cross}}\right)^2} \tag{6.3}$$

The quality factor Q is related to the resonant behavior of the second order response of the system: a large quality factor will yield a large peak at the resonant frequency in the magnitude of the loop gain (a pair of complex poles which would cause a relatively large resonant response); a small quality factor will yield a softer magnitude profile (two real poles which will cause no oscillatory response at all). The larger the phase margin, the lower the quality factor of the closed loop gain and vice versa. That is, the transient response of the closed loop system (the actual control system) can be analyzed by means of the phase margin of the loop gain (the loop gain of all the element in series). In practice, a value of 0.5 (critically damped) for the quality factor corresponds to a phase margin in the order of 70 degrees. Tuning the compensator for a smaller phase margin will yield a faster response with more and more overshoot (ultimately ringing if the phase margin is zero); tuning the compensator for a larger phase margin will yield a slower response with no overshoot at all. In practice, the phase margin for a good regulator design should be between 50 and 75 degrees.

In addition to the phase margin, the crossover frequency will also have a relevant meaning on the transient response of the regulator. The closed loop transfer function can be assumed to have unity gain from DC to the crossover frequency if the compensator is designed properly. This means that the response time of the regulator will be in the order of magnitude of the inverse of the crossover frequency. Therefore, it acts as a critical parameter in the design of the control loop: the higher the crossover frequency, the faster the transient response will be.

6.3. Control loop topologies

The possibilities to close the loop and turn the converter into a regulator are several. The concept has been introduced earlier in this chapter: a compensator or controller will be placed in the loop to modify its gain. This way, the desired crossover frequency and phase margin can be obtained. However, the topology of each control scheme and the nature of the signal used to feed back the compensator will be different. Aspects such as ease of design and implementation will be taken into account to choose the most suitable alternative. On the other hand, each control topology will present specific advantages and disadvantages. This section presents the three most suitable control schemes from a theoretical point of view to acquaint the reader with the concept and to justify the final selection.

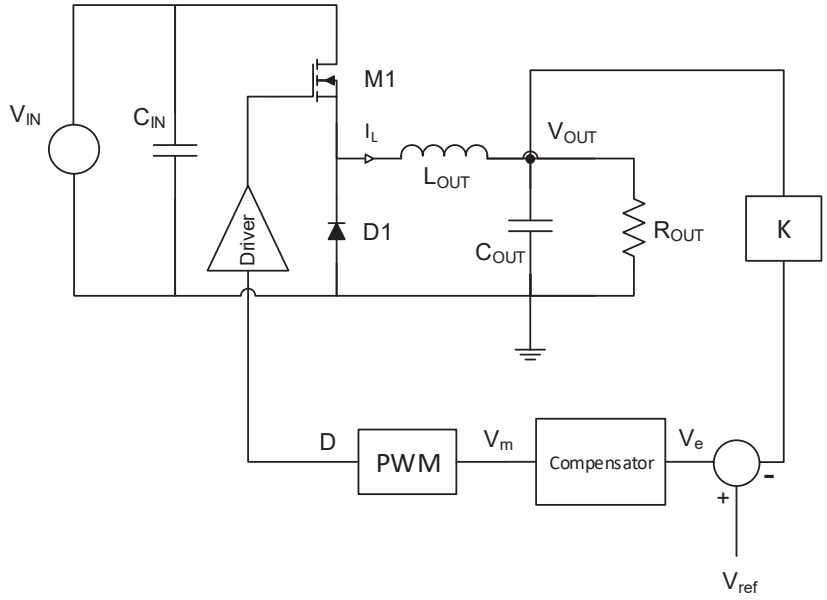

Figure 6.2: Concept drawing of the converter using a voltage mode control topology

6.3.1. Voltage mode control

The voltage mode control approach is the most known and used traditionally. Since the goal of the regulator is to keep the output voltage at a certain reference value, the voltage mode control concept uses the output voltage signal itself to feed back the compensator. Its basic structure can be observed in figure 6.2. The topology is very simple and presents a single loop. Therefore it can be easily analyzed and tuned from a theoretical point of view.

The duty cycle to output voltage transfer function will typically have the form of a second order system with a pair of complex poles introduced by the LC output filter. That means that the phase shift of the transfer function will be 180° for frequencies well above the resonant frequency, that is, a phase margin of zero. In practice, the ESR of the output capacitor will introduce a zero at high frequency which will inherently increase the phase margin of the loop gain. In any case, the compensator must include some kind of phase addition in order to be able to reach the desired amount of phase margin for a given crossover frequency. This can only be achieved by means of a PID or type-3 compensation network.

According to figure 6.2, the loop gain will consist of the converter input to output transfer function times the sensing gain, the compensator and the PWM modulator. This can be modeled ideally as a gain term that relates the control voltage with the duty cycle sent to the converter. The gate driver will not be explicitly considered for the loop gain and its effect can be initially neglected. In practice, it will introduce a delay to the control signal and some extra phase margin might be necessary to obtain the desired response.

The PID compensator can be designed to deliver certain amount of phase at the desired crossover frequency. Additionally, the integral term will introduce finite gain at DC which will make the steady state error zero. In practice, the designed compensation network can be implemented using analog or digital electronics (or a combination of both). If the subtraction between the reference and the fed back signal is to be implemented by means of an op-amp, its gain-bandwidth product will have to be typically high in order to allow the PID to work as expected (the op-amp must be able to provide the required gain at the frequencies at which the phase is added to the loop gain).

6.3.2. Peak-current mode control

Figure 6.3 shows the basic concept drawing of the peak-current mode control topology. It can be seen how two loops are now present: an inner loop that takes care of the coil current and an outer loop

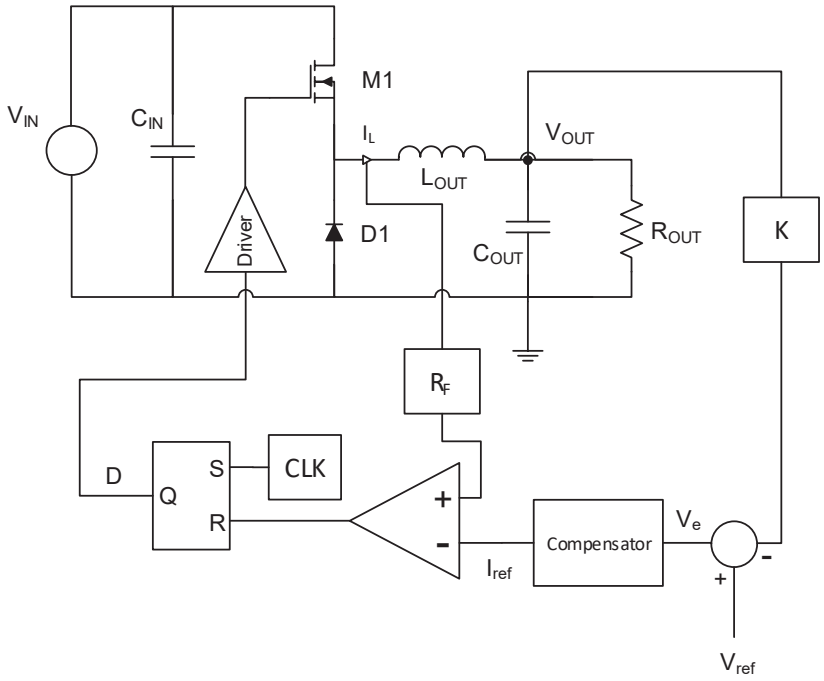

Figure 6.3: Concept drawing of the converter using a peak-current mode control topology

that sets the reference for the inner current loop. This effectively removes the coil from the control to output transfer function. That is, the coil behaves inherently as an ideal current source using this control topology. The compensation of the outer loop will be then much simpler than that required for voltage mode control described earlier.

It can be seen how the coil current is used now as the modulating ramp. A clock signal triggers the switching on of the DMOS at the start of the period. When the sensed coil current reaches the reference current i_{ref}, the transistor is turned off. Additionally, the output voltage is monitored and subtracted to a reference that goes into a compensator. The output of this compensator will set the reference current i_{ref} for the inner current loop.

The control to output transfer function will present a single pole response and therefore a simple type-2 or PI compensation network can be used since no phase addition is necessary (a minimum phase margin of 90° will be ideally obtained). The integral term of the compensator will provide the loop gain with infinite DC gain. The crossover frequency can be set by adjusting the proportional term of the compensator.

This control topology presents however a big disadvantage: subharmonics and even instability are observed if the system is to operate with duty cycles above 50 %. In order to avoid this, a compensation ramp must be introduced in the design. This increases the complexity of the solution significantly and makes this topology not so simple anymore. Additionally, the noise immunity of this approach is not good at all: any spikes or noise coupled to the coil current sensed signal could affect the internal comparison and trigger false commutations. This will become more and more problematic if the ripple of the current is smaller and smaller.

6.3.3. Average-current mode control

Figure 6.4 shows the concept diagram of average-current mode control. Again, two loops are employed to regulate the output voltage. The inner loop regulates the coil current to a reference value i_{ref}; the outer loop senses the output voltage and generates the reference current that will be used by the compensator of the inner current loop.

In this case, the inner loop will be designed around the control to coil current transfer function. It will be shown later in this chapter how a PI compensator will be enough to obtain the desired crossover

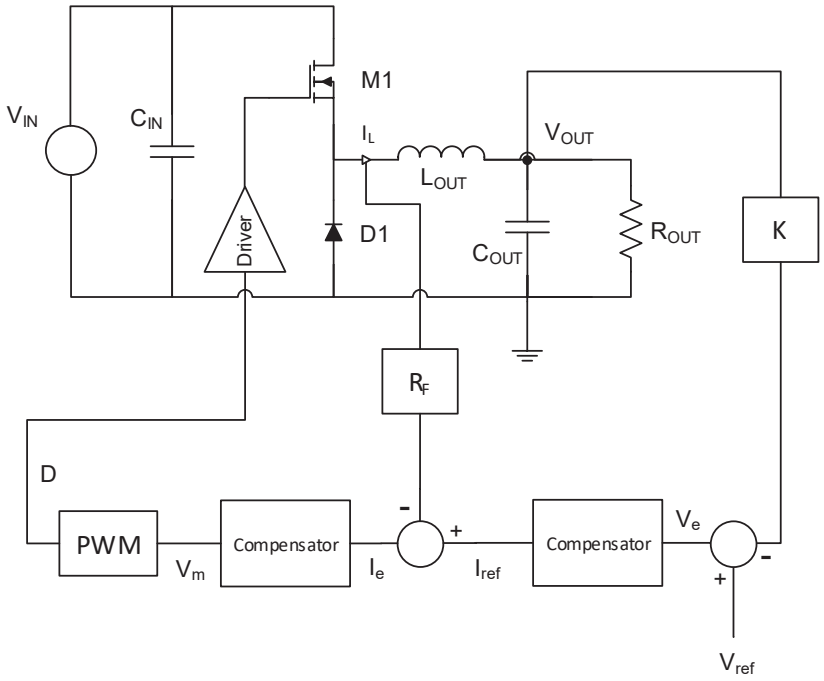

Figure 6.4: Concept drawing of the converter using an average-current mode control topology

frequency and phase margin for the response of the current. Additionally, this PI compensator will include an extra pole to filter out switching components and possible noise coupled to the sensed current. This will provide the loop with a low-pass nature and that is why this control scheme is typically known as average-current mode control.

The compensator for the outer loop will be designed around the control output voltage transfer function ($G_{vc} = v_{OUT}(s)/v_c(s)$). Again, a relatively simple PI controller can be used to close the loop with the desired crossover frequency and amount of phase margin.

6.3.4. Comparison

Once the three different control topologies have been introduced separately from a theoretical point of view, a comparison will be made in this section in order to conclude which alternative suits the application the best. Table 6.3 presents the main aspects of the three alternatives in a summarized form: cells that contain a check mark are considered advantageous; cells that contain an x mark represent a negative feature. As for loop complexity, voltage mode control appears to be the simplest topology since it only makes use of a single loop. Both peak and average-current mode controls rely on two loops to regulate the output, which can make the implementation a slightly harder.

In terms of compensator implementation, both peak and average-current mode control are implemented using relatively simple PI controllers. On the other hand, voltage mode control requires the use of a PID controller to boost the phase margin. Such implementation is not so trivial since a good operational amplifier will have to be used in order to provide the needed gain at the crossover frequency.

The noise immunity of voltage and average-current mode controls is very good. The former makes use of a large amplitude ramp to modulate the control signal and produce the duty cycle command; the latter has an inherent averaging character that filters out possible spikes or high-frequency harmonics that might have a negative impact on the operation of the regulator. On the other hand, peak-current mode control presents very deficient noise immunity. Since the coil current signal is used as the modulating ramp, a certain minimum amount of ripple must be guaranteed in order to obtain robust operation. In addition, possible spikes or noise coupled to the sensed current may affect the switching operation of the converter.

The line and load to output rejection of both peak and average-current mode control is very good.

	VMC	PCMC	ACMC
Loop complexity	✓	×	×
Compensator implementation	×	✓	✓
Noise immunity	✓	×	✓
Line and load to output rejection	×	✓	✓
Inherent current monitoring	×	✓	✓
Additional complexity	×	×	✓

Table 6.1: Summarized comparison between different control topologies

The inner loop will be much faster than the outer voltage loop and is capable of sensing any perturbations in load or line, therefore reacting to line or load perturbations. The voltage mode control presents a more deficient rejection since any of these changes will have to be firstly sensed at the output voltage and then corrected by the control loop.

Current monitoring is usually necessary in order to protect the converter from over current or short circuit conditions. Additionally, if several units are to be operated in parallel to supply a common load, sensing the current provides a means of equally distributing the power delivered by each regulator. Both peak and average-current mode controls come with inherent current sensing. On the other hand, voltage mode control exclusively senses the output voltage and would require extra effort to provide the solution with current monitoring features.

Additionally, peak-current mode control typically requires a compensation ramp in order to make the system stable at duty cycles above 0.5. This does not come for free and must be implemented in practice with extra effort and complexity. Voltage mode control can also be improved by making use of a feed-forward approach: if the modulator ramp is changed proportionally to changes in the input voltage, the rejection at the output can be improved significantly. However this requires an additional effort at the implementation phase.

All in all, average-current mode control appears as the most suitable topology for this application. In terms of simplicity and ease of implementation, building the two-loop structure does not imply too much complexity since they are simple. As for features and performance, average-current mode control appears as a better alternative compared to voltage and peak-current mode control schemes for all the reasons exposed earlier. What is more, Infineon's smart switch technology can make use of a current sensing scheme that would include the current monitoring without having to use additional sensing circuitry. All things considered, average-current mode control will be chosen as the best control topology for the application of interest and will be further analyzed in this thesis work.

6.4. Modelling the converter

The transfer function of the converter circuit must be derived in order to design a specific control topology. In practice, switches are non-linear elements that will confer the control to output transfer response of the system with a non-linear characteristic in most cases. As an exception, the buck converter ideally presents a linear characteristic since the output voltage is proportional to the control magnitude, namely the duty cycle. However, this is not the general case: other topologies such as boost or buck-boost present a non-linear control to output characteristic.

As a general rule, a linear model has to be derived so that classic control theory concepts can be applied. This is the case of the phase margin test earlier introduced in this chapter. Given the converter can be expressed as a linear transfer function with certain magnitude and phase, the stability of the control system can be analyzed together with the expected transient response. This is a relatively simple but powerful approach that will allow the designer to size and optimize the compensator or controller for a specific application of interest.

The first step to obtain a linear model that can be used to design the compensator is to average

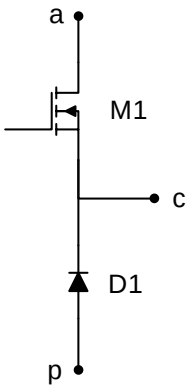

Figure 6.5: Switching leg with the corresponding naming criteria used to derive the linear model of the converter

the switching waveforms of the converter. Figure 6.5 shows the naming criteria that will be adopted. The switch terminal will be named a (active), the diode terminal p (passive) and the common terminal c (common). Let us assume an ideal operation without silicon voltage drop:

$$i_a(t) = \begin{cases} i_c(t) & \text{if } 0 < t < d(t)\,T_{sw} \\ 0 & \text{if } d_k\,T_{sw} < t < T_{sw} \end{cases} \tag{6.4}$$

$$v_{cp}(t) = \begin{cases} v_{ap}(t) & \text{if } 0 < t < d(t)\,T_{sw} \\ 0 & \text{if } d(t)\,T_{sw} < t < T_{sw} \end{cases} \tag{6.5}$$

Let us take the average during one switching cycle:

$$< i_a(t) >= d(t)\ < i_c(t) > \tag{6.6}$$

$$< i_{cp}(t) >= d(t)\ < v_{ap}(t) > \tag{6.7}$$

The initial circuit consisting of non-linear devices could be approximated by this averaged model. However, due to the product between quantities the model is still non-linear. Let us perform perturbation and linearization: an operating point will be assumed and small variations around it will be introduced. Then, the different average variables can be expressed as (the < > notation is omitted hereafter):

$$d(t) = D + \hat{d}(t) \tag{6.8}$$

$$i_a(t) = I_a + \hat{i}_a(t) \tag{6.9}$$

$$i_c(t) = I_c + \hat{i}_c(t) \tag{6.10}$$

$$v_{cp}(t) = V_{cp} + \hat{v}_{cp}(t) \tag{6.11}$$

$$v_{ap}(t) = V_{ap} + \hat{v}_{ap}(t) \tag{6.12}$$

Where the capitalized variables refer to operating point values and hatted variables refer to small-signal quantities. Let us plug these expressions into the previously derived relationships:

$$I_a + \hat{i}_a(t) = (D + \hat{d}(t))\,(I_c + \hat{i}_c(t)) \longrightarrow I_a + \hat{i}_a(t) = D\,I_c + D\,\hat{i}_c(t) + \hat{d}(t)\,I_c + \hat{d}(t)\,\hat{i}_c(t) \tag{6.13}$$

$$V_{cp} + \hat{v}_{cp}(t) = (D + \hat{d}(t))\,(V_{ap} + \hat{v}_{ap}(t)) \longrightarrow V_{cp} + \hat{v}_{cp}(t) = D\,V_{ap} + D\,\hat{v}_{ap}(t) + \hat{d}(t)\,V_{ap} + \hat{d}(t)\,\hat{v}_{ap}(t) \tag{6.14}$$

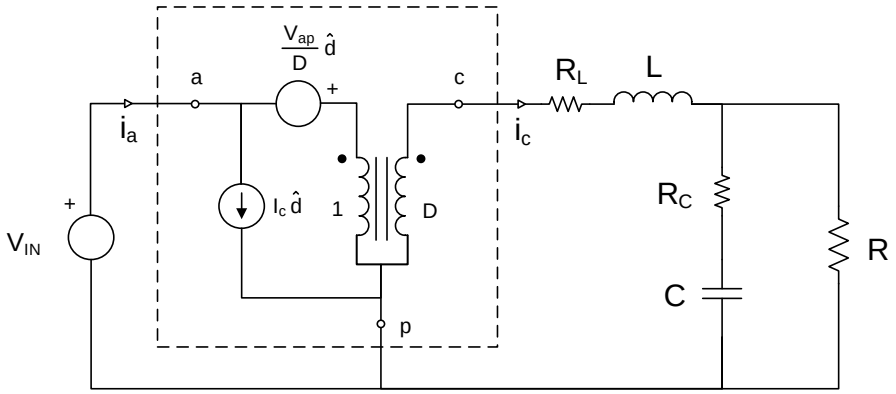

Figure 6.6: Time-invariant, linear, large-signal equivalent circuit of the converter that will be used to design the control loop

Let us neglect the product between two small-signal quantities:

$$I_a + \hat{i}_a(t) = D\, I_c + D\, \hat{i}_c(t) + \hat{d}(t)\, I_c \tag{6.15}$$

$$V_{cp} + \hat{v}_{cp}(t) = D\, V_{ap} + D\, \hat{v}_{ap}(t) + \hat{d}(t)\, V_{ap} \tag{6.16}$$

The steady-state quantities can be separated from the AC variables:

$$I_a = D\, I_c \tag{6.17}$$

$$V_{cp} = D\, V_{ap} \tag{6.18}$$

$$\hat{i}_a(t) = D\, \hat{i}_c(t) + I_c\, \hat{d}(t) \tag{6.19}$$

$$\hat{v}_{cp}(t) = D\, \hat{v}_{ap}(t) + V_{ap}\, \hat{d}(t) \tag{6.20}$$

These relationships can be expressed in the form of a large-signal linear equivalent circuit. The two steady-state relationships can be represented by an ideal transformer with a turn ratio of D. The small-signal quantities can be reflected to the primary side and expressed together in the equivalent circuit. Figure 6.6 presents the converter circuit with the equivalent large-signal linear equivalent circuit. It can be seen how the switching elements have been replaced for linear components (dependent sources and an ideal transformer). The DC response of the converter can be analyzed by making all small-signal quantities zero. The AC response of the converter, that is, the transfer functions, can be obtained by substituting the operating point values and isolating the corresponding small-signal quantities.

6.5. Designing the compensator of the average-current mode control loop

The converter stage has been modeled as a linear system for a given operating point in the previous section. From this point, control theory can be applied to design the compensator. As it has been mentioned earlier, average-current mode control consists of two loops: an inner current loop and an outer voltage loop. The design will focus firstly on closing the inner current loop. This will be done by deriving the corresponding transfer function from the small-signal linear model. Then, the gain loop can be expressed in order to design the compensator required to obtain certain crossover frequency and phase margin.

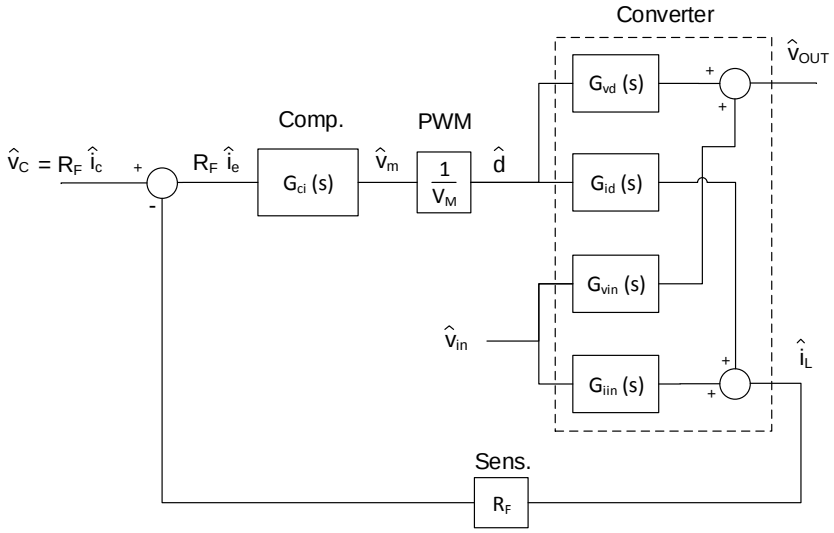

Figure 6.7: Block diagram of the inner current loop present in average-current mode control

Once the inner loop is designed, the focus will move on to the outer voltage loop. The methodology will be similar: the corresponding transfer functions will be derived from the small-signal linear model in order to determine the compensation needed to close the loop.

6.5.1. Inner current loop

Figure 6.7 shows a block diagram of the inner current loop used for average-current mode control. It can be seen how certain voltage reference will be given by the outer voltage loop ($\hat{v}_C$). The sensed current will be subtracted from this quantity and will be the input of the current compensator G_{ci} (s). This block will output a voltage signal v_m that will be sent to a PWM. The gain of this modulator can be ideally modeled as a gain term which depends on the amplitude of the saw tooth waveform. The output of the modulator will serve as input to the converter that will produce a certain set of outputs. The different transfer functions can be observed within the dashed block. It can be seen how the transfer function around which the current loop will be closed is G_{id}, that is, the control to coil current. The loop gain can be then expressed as follows:

$$T_i(s) = G_{ci}(s)\,\frac{1}{V_M}\,G_{id}(s)\,R_F \tag{6.21}$$

The compensator will be initially neglected in order to realize its gain requirements. The term R_F will be a function of the sensing method used to feed back the coil current. The next step will consists in deriving the control to coil current transfer function.

Firstly, the operating point has to be calculated according to the equivalent circuit shown in figure X. This can be done by cancelling all small signal quantities. The series resistance of coil and capacitor will be neglected for this calculation. At DC, the inductor can be considered a short and the capacitor an open circuit. Then, it can be concluded that:

$$V_{ap} = V_{IN} \tag{6.22}$$

$$I_c = I_{OUT} = I_L \tag{6.23}$$

$$D = V_{OUT}/V_{IN} \tag{6.24}$$

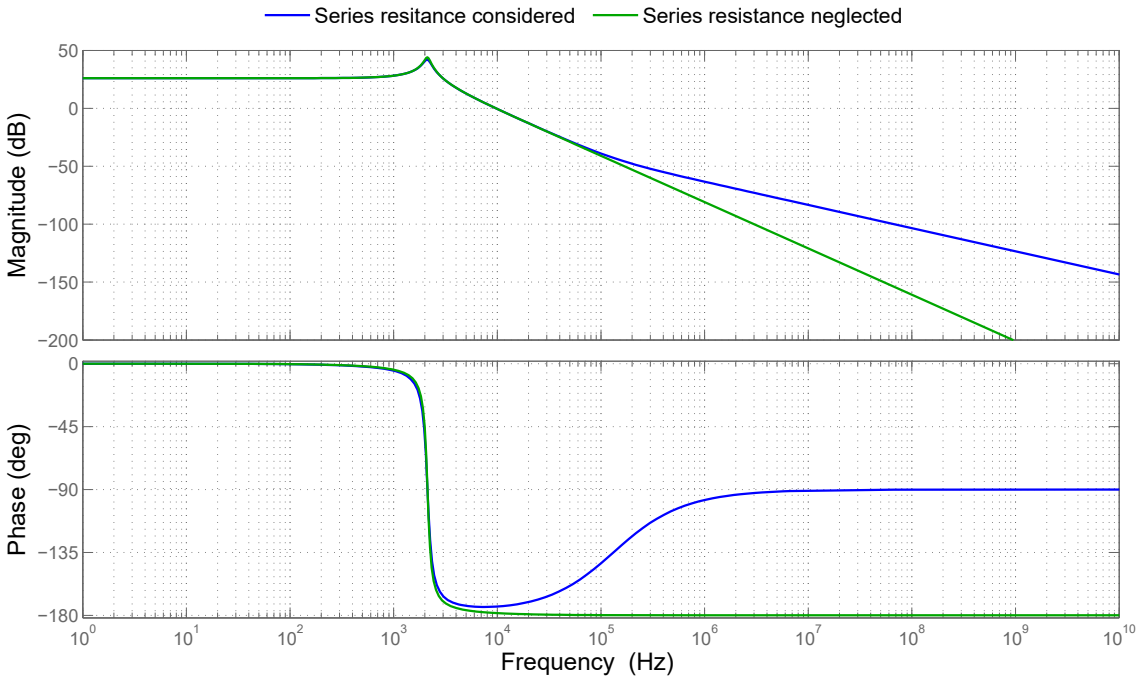

Figure 6.8: Magnitude and phase response of the control to output transfer function

The dependent sources can now be expressed as a function of the operating point. Since the transfer function of interest is control to coil current, the small signal quantity related to the input voltage will be assumed zero. The transfer function can be expressed as:

$$G_{id}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{\hat{i}_L(s)}{\hat{v}_{OUT}(s)} \frac{\hat{v}_{OUT}(s)}{\hat{d}(s)} = \frac{\hat{i}_L(s)}{\hat{v}_{OUT}(s)} G_{vd} \tag{6.25}$$

The control to output G_{vd} is a well-known transfer function very often discussed in the literature. According to [66], it can be expressed as:

$$G_{vd}(s) = \frac{V_{IN}\,(1 + R_C\,C\,s)}{1 + \frac{R_L}{R} + \left(\frac{L}{R} + R_C\,C + \frac{R_L\,C + R_L\,R_C\,C}{R}\right)s + \frac{R + R_C}{R}\,L\,C\,s^2} \tag{6.26}$$

It can be seen how the LC filter introduces a pair of poles which will cause a total phase shift of -180°. The ESR of the output capacitor creates a high-frequency zero that would help increase the phase margin. The input voltage appears as a DC gain term. In case the series resistance of coil and capacitor are neglected:

$$G_{vd}(s) \approx \frac{V_{IN}}{1 + \frac{L}{R}\,s + L\,C\,s^2} \tag{6.27}$$

Figure 6.8 plots both transfer functions (with and without taking the series resistance terms into account). It can be observed how the high-frequency zero is not present anymore and how only the DC gain and the complex pair of poles remain if the ESR of the output capacitor is neglected.

As for the other term, it can be seen how the coil current and the output voltage relate to each other by the parallel impedance of output capacitor and resistor. This can be expressed as:

$$\frac{\hat{i}_L(s)}{\hat{v}_{OUT}(s)} = \frac{1}{R \,||\left(R_C + \frac{1}{C\,s}\right)} = \frac{1 + (R + R_C)\,C\,s}{R\,(1 + R_C\,C\,s)} \tag{6.28}$$

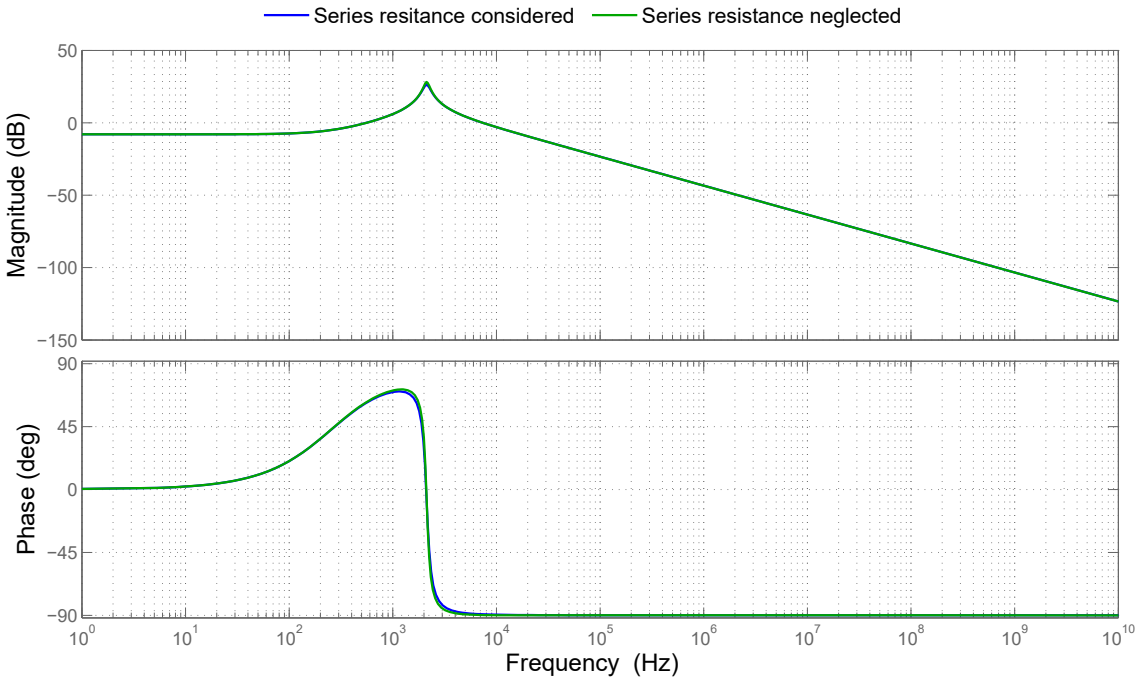

Figure 6.9: Magnitude and phase response of the uncompensated loop gain for the inner current loop

The high-frequency ESR-related term appears now as a pole that will cancel out the zero from the control to output transfer function. The DC gain, as expected, will be the inverse of the output resistance. A low-frequency zero appears now from the combination of output capacitance and resistance. The control to coil current transfer function can be then expressed as:

$$G_{id}(s) = \frac{V_{IN}\,(1 + (R + R_C)\,C\,s)}{R\left(1 + \frac{R_L}{R} + \left(\frac{L}{R} + R_C\,C + \frac{R_L\,C + R_L\,R_C\,C}{R}\right)s + \frac{R + R_C}{R}\,L\,C\,s^2\right)} \tag{6.29}$$

The low-frequency zero resulting from the output impedance will add 90° of phase, making a total phase shift of -90° at high frequency. This presents an advantage with respect to the LC output filter transfer function G_{vd}, which has a phase shift of -180° at high frequency (if the ESR is neglected). Consequently, a PI or type-2 compensator will be enough to achieve the desired crossover frequency with certain amount of phase margin. This transfer function can be simplified if the series resistance of capacitor and coil is neglected:

$$G_{id}(s) \approx \frac{V_{IN}\,(1 + R\,C\,s)}{R\left(1 + \frac{L}{R}\,s + L\,C\,s^2\right)} \tag{6.30}$$

The DC magnitude of this transfer function equals the input voltage over the output resistance. The low frequency zero added by output capacitor and resistor appears at the numerator. A pair of poles can be seen at the denominator as a result of the LC configuration of the output filter. Once the transfer function is known, the current loop gain (compensated and uncompensated) can be expressed as described earlier:

$$T_i^u(s) = \frac{1}{V_M}\,G_{id}(s)\,R_F \tag{6.31}$$

$$T_i(s) = G_{ci}(s)\,T_i^u(s) \tag{6.32}$$

Figure 6.9 shows the bode plot of two uncompensated loop gains, one including the series resistance terms and the other neglecting them. The parameter values are those presented in table 6.2.

It can be seen how the simplified expression gives almost the same result as the detailed transfer function. Therefore, the series resistance terms will be neglected for further analysis on this transfer function. As expected, the low frequency pole can be observed at approximately 260 Hz. The two poles appear as a complex pair at a resonant frequency of 2.1 kHz. The resonant behavior is evidenced by the peak of the magnitude at this frequency value. After that, the magnitude rolls off at 20 dB per decade. As for the phase, it can be seen how the low-frequency zero adds phase margin until the pair of poles start playing a role. The phase at high frequency is -90°.

Parameter	Value
L	47 µH
R_L	47 mΩ
C	120 µF
R_C	10 mΩ
V_M	5 V
V_{IN}	20 V
D	50 %
f_{SW}	400 kHz
R_F	0.5 Ω
K	1

Table 6.2: Parameter values used to design the average-current mode control

The desired crossover frequency of the inner current loop will be set to one tenth of the switching frequency, that is, 40 kHz. At this frequency range, the gain loop can be approximated as:

$$T_i(s) \approx G_{ci}(s)\,\frac{V_{IN}\,R_F}{L\,V_M\,s} \tag{6.33}$$

That is, a slope of -20 dB per decade with certain gain that is influenced by that of the compensator. The crossover frequency can be set by introducing the gain term of the compensator and forcing the expression to equal 1:

$$1 = K_{ci}\,\frac{V_{IN}\,R_F}{L\,V_M\,2\pi\,f_{cross,i}} \tag{6.34}$$

$$K_{ci} = \frac{L\,V_M\,2\pi\,f_{cross,i}}{V_{IN}\,R_F} = 5.906 \tag{6.35}$$

For this specific tuning, the required proportional gain equals 5.9. The transfer function of the resulting gain loop is shown in figure 6.10 (only the proportional part of the compensator is introduced). It can be seen how the crossover frequency is effectively set to 40 kHz by just lifting up the magnitude with the proportional term. Still, the response of the system can be improved: an inverted zero will be added to obtain infinite gain at DC, and a high-frequency pole will be added to give the inner current loop the low-pass nature typical of average-current mode control.

As a compromise between noise filtering and high gain at low frequency, the inverted zero and the filtering pole will be placed according to the expressions:

$$f_{z,i} = \frac{f_{cross,i}}{4} = 10\,kHz \tag{6.36}$$

$$f_{p,i} = 4\,f_{cross,i} = 160\,kHz \tag{6.37}$$

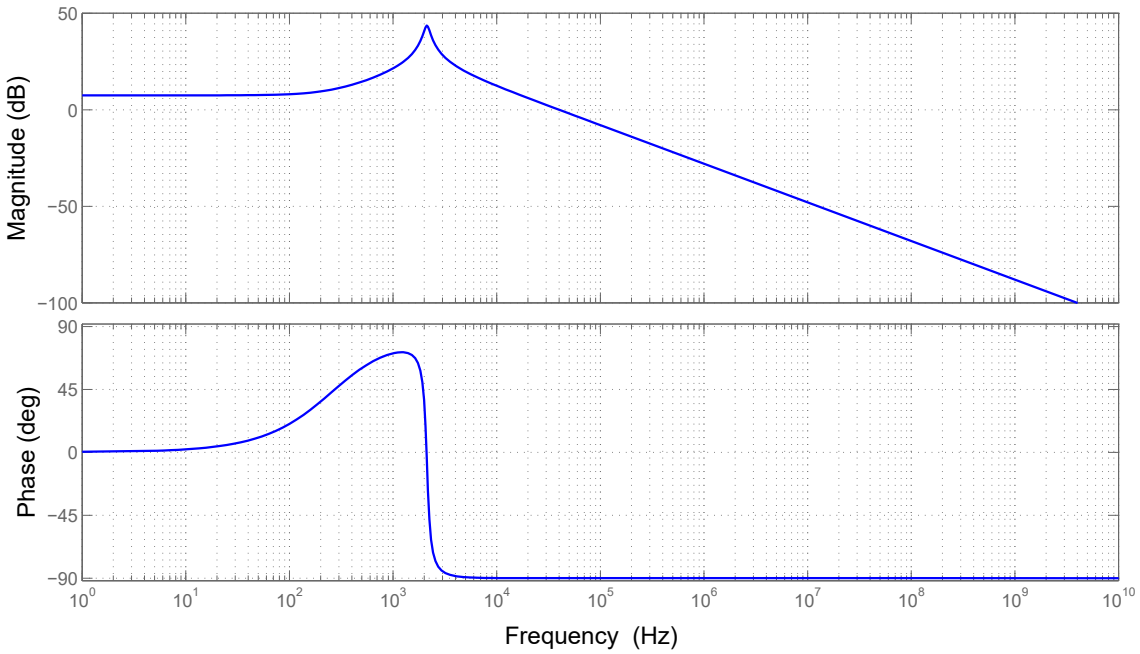

Figure 6.10: Magnitude and phase response of the loop gain for the inner current loop including the compensator proportional gain

The compensator will have the following transfer function:

$$G_{ci}(s) = K_{ci}\,\frac{1+\frac{2\,\pi\,f_{z,i}}{s}}{1+\frac{s}{2\,\pi\,f_{p,i}}} \tag{6.38}$$

Figure 6.11 plots the magnitude and phase response of the compensator. It can be seen how the magnitude at the crossover frequency equals the expected value (15.4 dB). It will introduce some phase change due to the integrator, the zero and the pole. The overall loop gain is plotted in figure 6.12. It can be seen how the gain tends to infinite at DC and how the compensator reduces the phase margin to around 60° (with respect to an initial value of 90°). This will be considered an acceptable tuning for the inner current loop.

6.5.2. Outer voltage loop

The outer voltage loop will be closed around the initially designed current loop. The output of the voltage loop compensator will serve as input for the inner current loop. For this reason, the closed-loop transfer function from v_c to i_L will be firstly derived. The loop gain of the inner current loop has been already defined as:

$$T_i(s) = G_{ci}(s)\,\frac{1}{V_M}\,G_{id}(s)\,R_F \tag{6.39}$$

Having a look at figure 6.4, the closed loop transfer function can be expressed as follows:

$$\left(v_C(s) - i_L(s)\,R_F\right)G_{ci}(s)\,\frac{1}{V_M}\,G_{id}(s) = i_L(s) \tag{6.40}$$

$$G_{ic}(s) = \frac{i_L(s)}{v_C(s)} = \frac{1}{R_F}\,\frac{T_i(s)}{1+T_i(s)} \tag{6.41}$$

Once this transfer function is derived, the outer voltage loop can be built up from the blocks shown in figure 6.4. It can be seen how the voltage loop gain can be expressed as the series connection of the

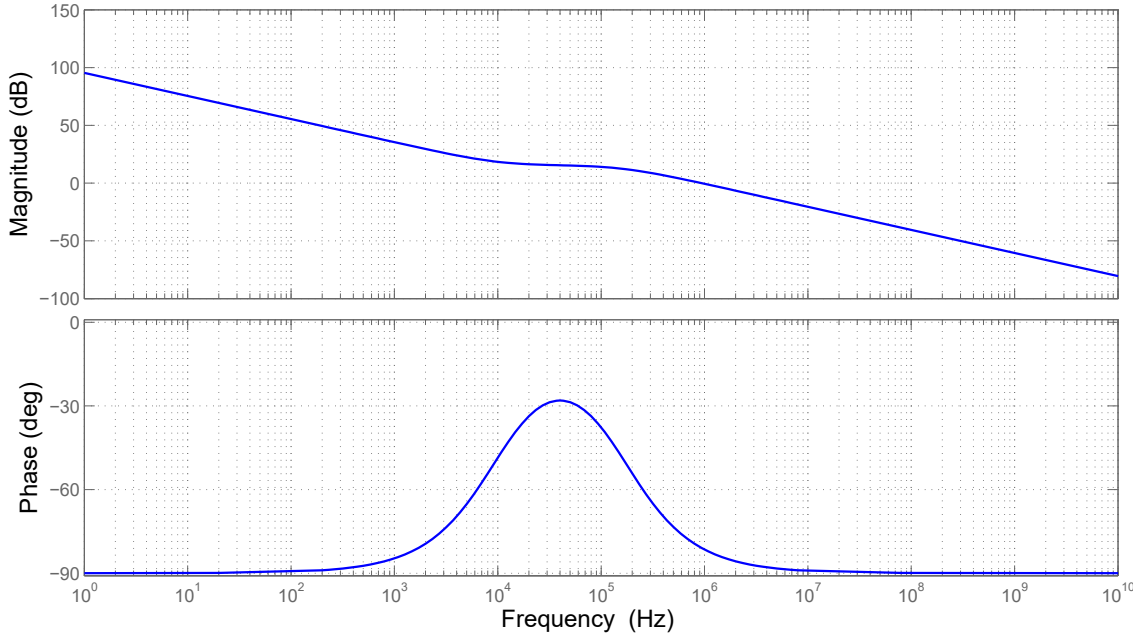

Figure 6.11: Magnitude and phase response of the current compensator transfer function

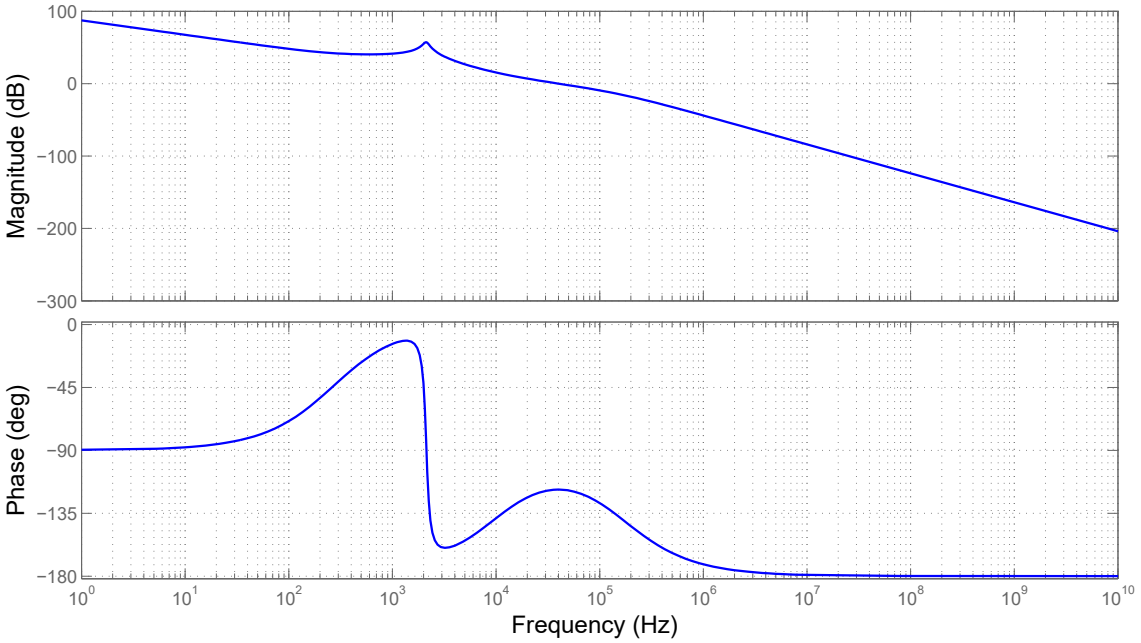

Figure 6.12: Magnitude and phase response of the compensated loop gain for the inner current loop

voltage compensator, the control to current transfer function and the parallel impedance of the output capacitor and the output resistor. The sensing term associated with the output voltage will also appear in the voltage loop gain:

$$T_v(s) = G_{cv}(s)\, G_{ic}(s)\, \frac{v_O(s)}{i_L(s)}\, K \tag{6.42}$$

The fractional term was derived previously:

$$\frac{v_O(s)}{i_L(s)} = R \| \left(R_C + \frac{1}{C\, s} \right) = R\, \frac{1 + R_C\, C\, s}{1 + (R + R_C)\, C\, s} \tag{6.43}$$

Additionally, the closed current loop transfer function G_{ic} can be approximated in the low-frequency range. Since a PI compensator was used, the current loop gain T_i presents infinite gain at DC. Then:

$$\frac{T_i(s)}{1 + T_i(s)} \approx 1 \tag{6.44}$$

Consequently, G_{ic} can be approximated in the low frequency range as:

$$G_{ic}(s) \approx \frac{1}{R_F} \tag{6.45}$$

This means that the inner current loop turns the coil into a current source whose magnitude depends on the control signal given by the voltage loop. As a consequence, the effect of the coil is also removed from the outer loop, which can be simplified as well:

$$T_v(s) = G_{cv}(s)\, \frac{1}{R_F}\, \frac{v_O(s)}{i_L(s)}\, K \tag{6.46}$$

$$T_v(s) = G_{cv}(s)\, \frac{1}{R_F}\, K\, R\, \frac{1 + R_C\, C\, s}{1 + (R + R_C)\, C\, s} \tag{6.47}$$

The uncompensated voltage loop gain is plotted in figure 6.13 for both cases. It can be seen how the simplified expression is almost identical for frequencies below 5 kHz. Since the goal crossover frequency will be in this range, the approximation will be valid to tune the voltage compensator. A PI controller will be used again to obtain infinite gain at DC. A reasonable value for the voltage loop crossover frequency will be one tenth of its current loop counterpart:

$$f_{cross,v} = \frac{f_{cross,i}}{10} = 4kHz \tag{6.48}$$

The voltage loop gain can be further simplified in this frequency range if these assumptions are made:

$$R_C \ll R \tag{6.49}$$

$$1 \gg R\, C\, s \tag{6.50}$$

Consequently, the loop gain can be expressed as:

$$T_v(s) = G_{cv}(s)\, \frac{1}{R_F}\, K\, \frac{1}{C\, s} \tag{6.51}$$

The proportional part of the voltage controller can be adjusted to obtain the desired crossover frequency:

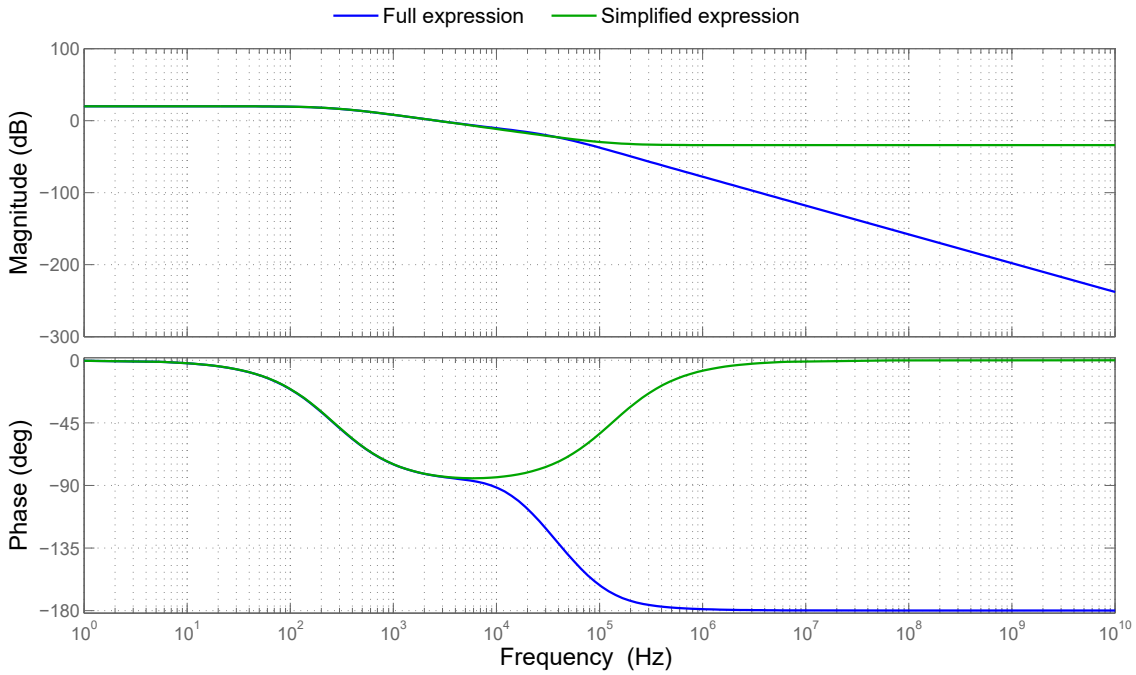

Figure 6.13: Magnitude and phase response of the uncompensated loop gain for the outer voltage loop

$$1 = K_{cv} \frac{1}{R_F} K \frac{1}{C\, 2\, \pi\, f_{cross,v}} \tag{6.52}$$

$$K_{cv} = R_F\, C\, 2\, \pi\, f_{cross,v}\, \frac{1}{K} = 1.508 \tag{6.53}$$

Figure 6.14 shows the voltage loop gain when the proportional compensator is introduced. It can be seen how both transfer functions (using G_{ic} and its simplified version) have a crossover frequency of 4 kHz as expected from the design. The compensator can be further improved if an inverted zero and a filtering pole are added:

$$f_{z,v} = \frac{f_{cross,v}}{4} = 1kHz \tag{6.54}$$

$$f_{p,v} = 4\, f_{cross,v} = 16kHz \tag{6.55}$$

The voltage compensator magnitude and phase are plotted in figure 6.15. The integrator and filtering effect can be observed at the magnitude profile. The phase margin will be slightly reduced by introducing the voltage compensator. Figure 6.16 plots the voltage loop gain when the voltage compensator is introduced. It can be seen how the crossover frequency is set to the desired value of 4 kHz with a phase margin of 66.8°. This amount will be considered sufficient to obtain a good transient response.

Table 6.3 shows a summary of the designed compensators. The phase margin values obtained for both loops are in the admissible range. The crossover frequencies are sufficiently high to obtain a good transient performance.

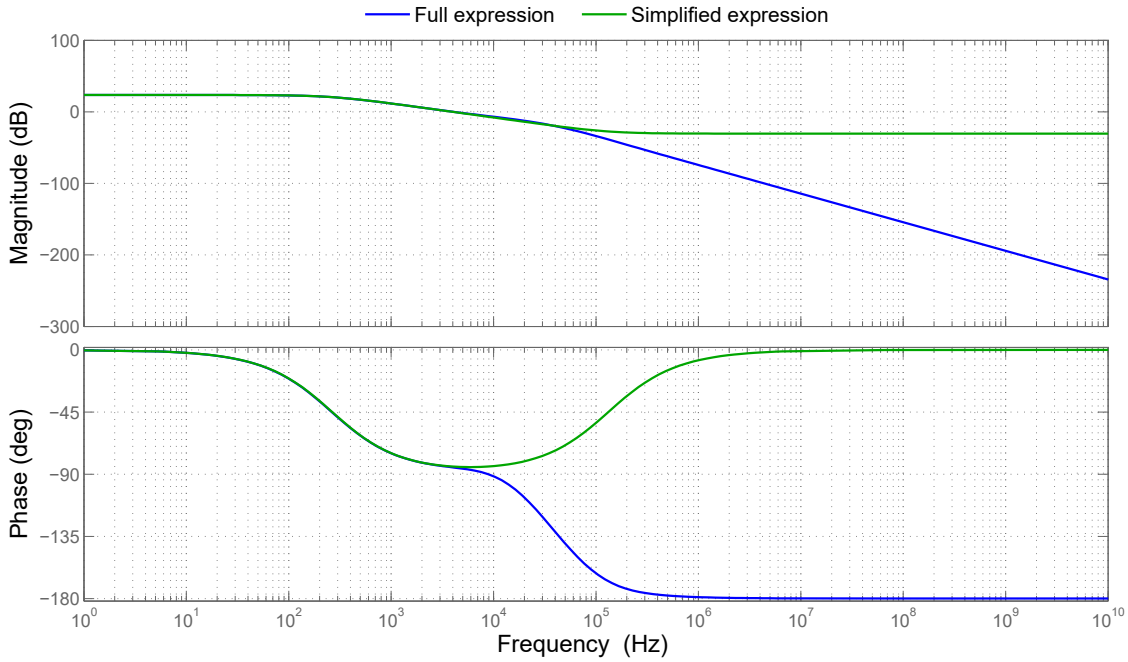

Figure 6.14: Magnitude and phase response of the voltage loop gain including the proportional term

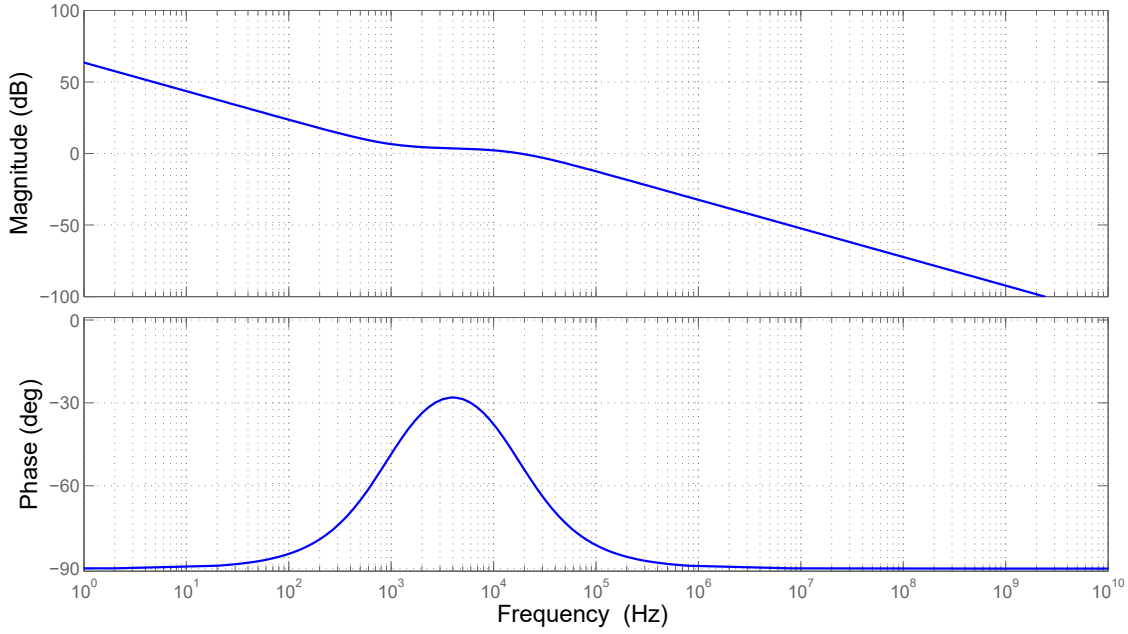

Figure 6.15: Magnitude and phase response of the voltage loop compensator

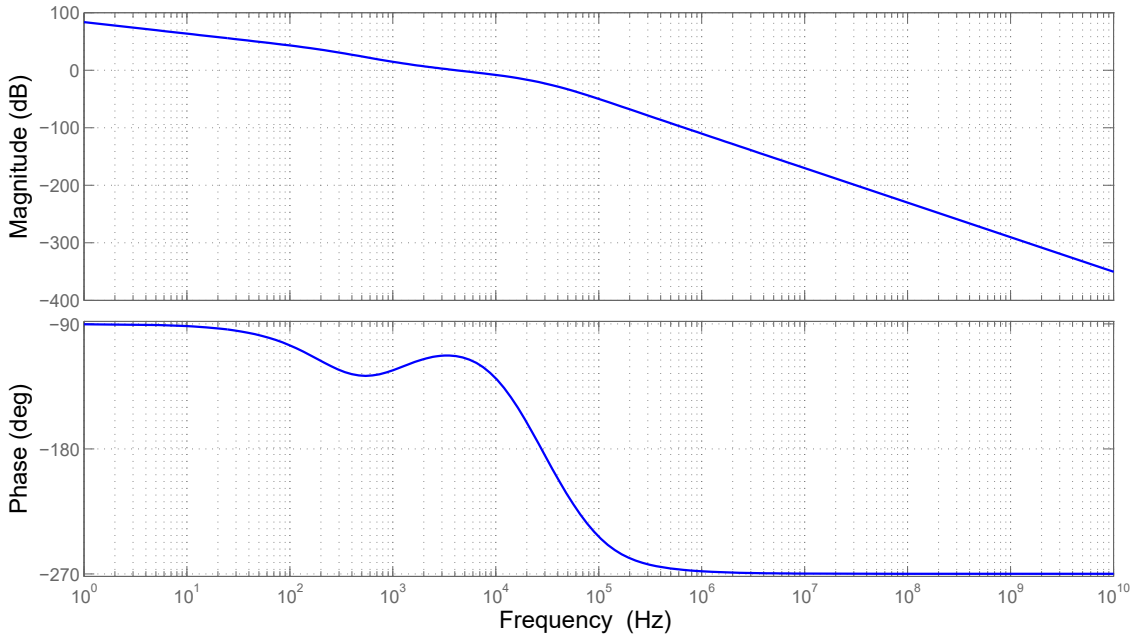

Figure 6.16: Magnitude and phase response of compensated loop gain for the outer voltage loop

	Current compensator	**Voltage compensator**
f_{cross} [kHz]	40	4
PM [deg]	61.9	66.8
K	5.906	1.508
f_z [kHz]	10	1
f_p [kHz]	160	16

Table 6.3: Compensator design parameter used for the average-current mode control scheme

6.6. Simulation results

Once both inner and outer loops have been designed, the response of the system will be analyzed by having a look at simulation results. Table 7.1 summarizes the parameters used during simulation and their nominal value. In case any of them is modified during the simulation, it will be mentioned. The output filter has been sized accordingly to the values obtained in chapter 4. The coil presents a value corresponding to the nominal and its series resistance is as specificed in the datasheet. The 20 µF capacitor corresponds to the ceramic device, with a very small ESR in series. On the other hand, the aluminum capacitor appears as a 100 µF device with a much larger ESR. It must be noted that tolerances will not be taken into account during simulation. The input voltage will be assumed to be 20 V. The output load resistor will have a value of 6.1 Ω, since that will be available at the lab for further validation of results.

Parameter	Nominal value
L_{OUT}	47 µH
R_L	50 mΩ
$C_{OUT,1}$	20 µF
$R_{C,1}$	5 mΩ
$C_{OUT,2}$	100 µF
$R_{C,2}$	200 mΩ
R_{OUT}	6.1 Ω
V_{IN}	20 V
f_{SW}	400 kHz

Table 6.4: Simulation parameters and their nominal value used to obtain the results presented in this chapter

Firstly, the response to reference voltage steps will be evaluated. That is, a step of 0.5 V with respect to the previous operating point will be applied as the reference signal to the outter voltage loop. The system will be assumed in steady state for an operating point of 10 V at the output. Figure 7.8 shows the system response when the step is applied in the positive direction. It can be seen how the new reference point will be 10.5 V. The upper half of the figure shows how the output voltage tries to follow the reference. It takes approximately 100 µs for the voltage to reach the new reference point. The amount of overshoot is around 10 %. The bottom half of the figure shows how the coil current reacts to the reference step: since the new operating point is above that set previously, the current increases to charge the output capacitors to the new desired level. Once the transient is over, the coil current presents a new steady-state value corresponding to the operating point of 10.5 V at the output.

Figure 7.9 shows the response to a negative reference step. The observed behavior is very similar to that seen previously for the positive step. The voltage takes around 100 µs again to cross the newly set reference and a small amount of undershoot is present. The coil current significantly decreases with respect to the steady-state value to force a discharge of the output capacitor. Once the transient has passed, the current settles to the new steady-state point. All in all it can be seen how both outer and inner loops adjusts their corresponding control signals to follow the reference. Also, it can be seen how the system behaves linearly, since the step response is symmetrical for steps with opposite sign.

Another important characteristic response of the system is related to changes at the input voltage. In practice, the converter will be connected to a supply which present certain amount of ripple. What is more, line steps could occur due to sever load variations or certain frequency components could be present on top of the DC. Line-to-output rejection will be evaluated by having a look at how the system behaves when voltage steps of 5 V are applied to the input voltage of the converter. According to the working principle of average-current mode control, the inner loop will firstly realize this change of voltage at the input and will consequently react to it.

Figure 6.19 plots the three main waveforms that can be analyzed to draw conclusions when a

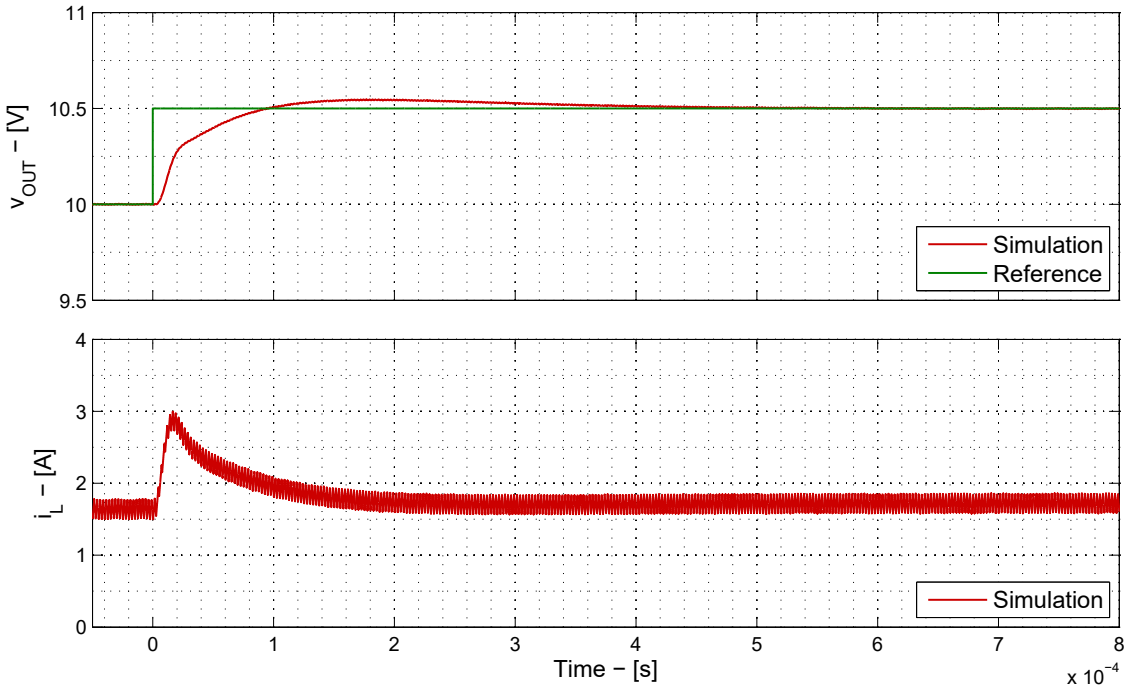

Figure 6.17: System response to a positive voltage reference step of 0.5 V. The simulations parameters are presented in table 7.1

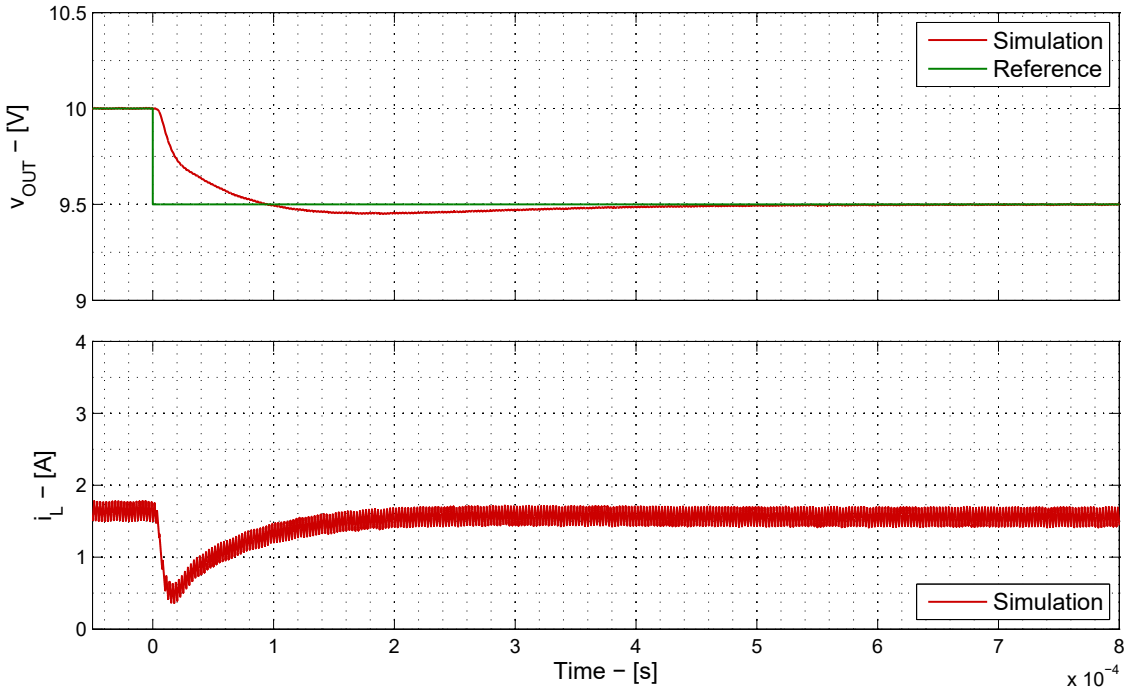

Figure 6.18: System response to a negative voltage reference step of 0.5 V. The simulations parameters are presented in table 7.1

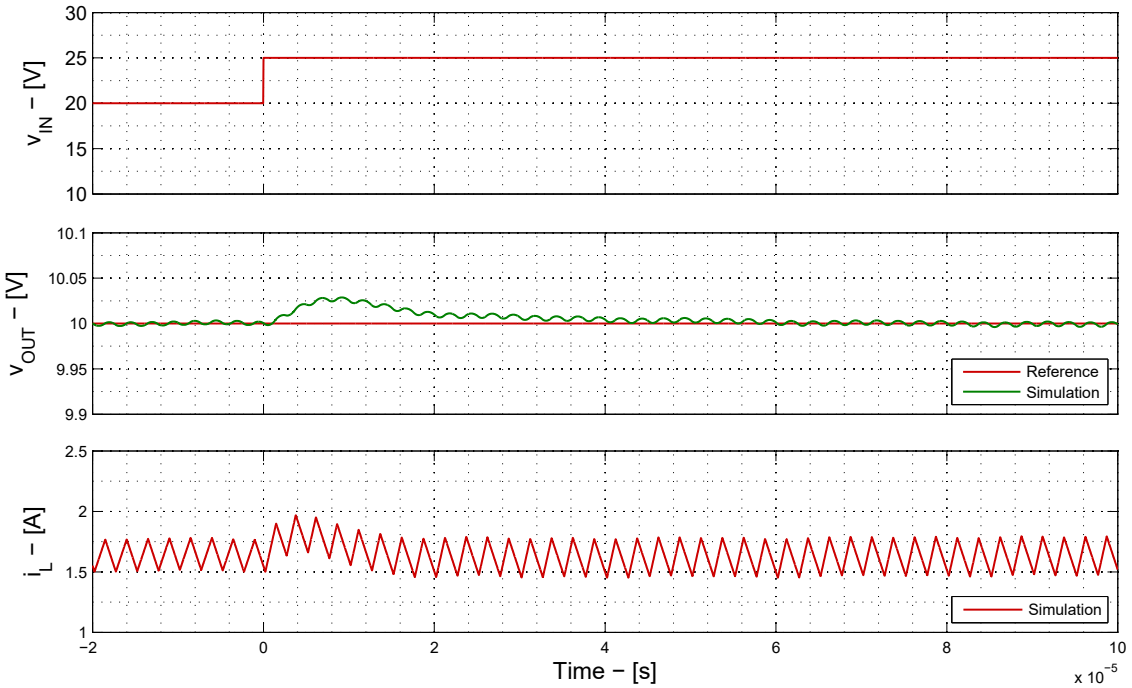

Figure 6.19: System response to a positive line step of 5 V. The simulations parameters are presented in table 7.1

positive voltage step of 5 V is applied at the input. This can be seen in the first subplot: at time t = 0 the input voltage goes from its nominal value of 20 to 25 V. As a consequence, the slope of the coil current will change in the next switching period. From an intuitive point of view, it could be seen how an increase of the input supply would yield an increase of both output voltage and current. However, the inner current loop will react to it and decrease the duty cycle command sent to the driver. The maximum overshoot seen at the output voltage with respect to its reference value of 10 V is in the order of 25 mV. After a time period of approximately 20 µs, the control is able to bring back the output voltage to its reference value. It can be seen how the current presents a slightly different shape at the newly set steady-state operating point: lower duty cycle with a larger amount of ripple.

Figure 6.20 can be analyzed in a similar fashion: a negative line step of 5 V will take place at t = 0. As a consequence, the slope of the coil current will significantly decrease. The new operating point for this input voltage condition would yield a lowering of both output voltage and coil current. However, the control is fast enough to sense the change and react to it: a larger duty cycle command will be sent to the driver to compensate for the input voltage drop. This way, the output voltage will be brought back to its reference value. The undershoot observed in this case is in the order of 50 mV with a recovery time of approximately 30 µs.

It can be concluded that the line-to-output rejection offered by the average-current mode control is extremely good. Changes at the input are quickly sensed by the inner current loop which reacts to bring back the output voltage to its reference value. The recovery time and the over/undershoot observed for both cases is very small. It can be concluded that the response of this control scheme to line steps is very good.

Lastly, the performance of the system can be evaluated by having a look at the response when a load step takes place. In practice this will be similar to connecting and disconnecting LED chains in parallel at the output of the operating converter. Ideally, the control must be able to reach to these changes and keep the output voltage at its reference value so that the load sees the same amount of voltage.

Figure 6.21 presents the simulation results when a negative load step is applied, that is, when the resistance at the output is halved from its nominal value to 3.05 Ω. Had not the control reacted to this load step, the output voltage would decrease to half of its previous value if the current was kept constant. However, the load change is seen at the inner current loop, which reacts to it by increasing the amount

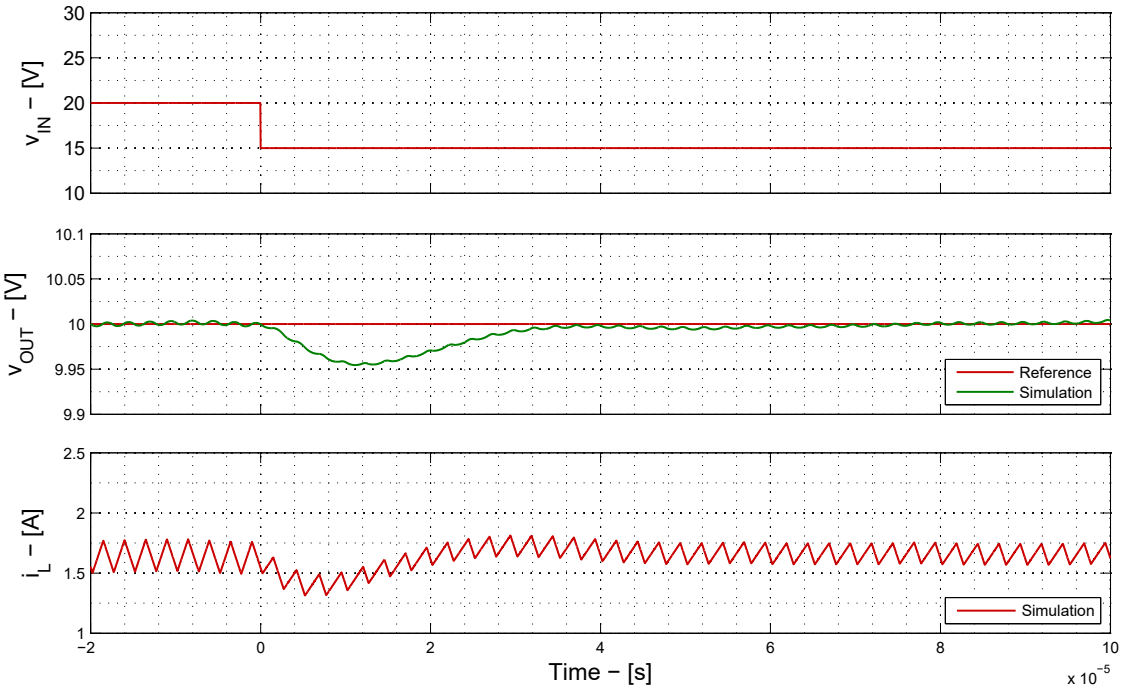

Figure 6.20: System response to a negative line step of 5 V. The simulations parameters are presented in table 7.1

of current. Consequently, the initially falling output voltage will be brought back to the reference value. Since the output resistance has been halved, the new operating point will be characterized by twice the amount of initial current through the coil. This can be seen once the transient response is over. The undershoot observed is in the order of 350 mV and the recovery time is approximately 400 µs.

Figure 6.22 shows the opposite response to that presented previously. Here, a positive load step is applied from half the nominal output resistance to the nominal value. This could be equivalent to disconnecting two identical LED chains previously operating in parallel. If the control would not react to this change and the current was kept constant, the output voltage would settle at twice its initial value. However, the load increase is reacted to by the control loop. The current forced through the coil will be made lower in order to bring back the output voltage to the reference value. The overshoot observed is in the order of 350 mV, with a recovery time of 400 µs.

In summary, the proposed control scheme also succeeds at regulating the output voltage in presence of abrupt load changes. Together with the observed response to line and reference steps, average-current mode control appears as a very efficient and well performing alternative to turn the converter into an LED driver.

6.7. Conclusions

A comparison between different control schemes has been presented in this chapter. It has been proven that the average-current mode control appears as the most advantageous and suitable control strategy for the application of interests. Aspects such as ease of design and implementation, performance and noise immunity are the main features. The control topology has been described by means of presenting the two separate loops, inner current and outer voltage, that construct the overall scheme.

A small signal model has been presented in order to obtain the necessary transfer functions. The compensator properties and features will be derived from these in order to meet certain stability and transient response requirements. It has been concluded that a simple type-2 or PI compensation is enough to close each loop with the desired amount of phase margin and crossover frequency.

A practical design of both current and voltage loops has been carried out in this chapter in the continuous frequency domain. That is, both compensators can be expressed as transfer functions in

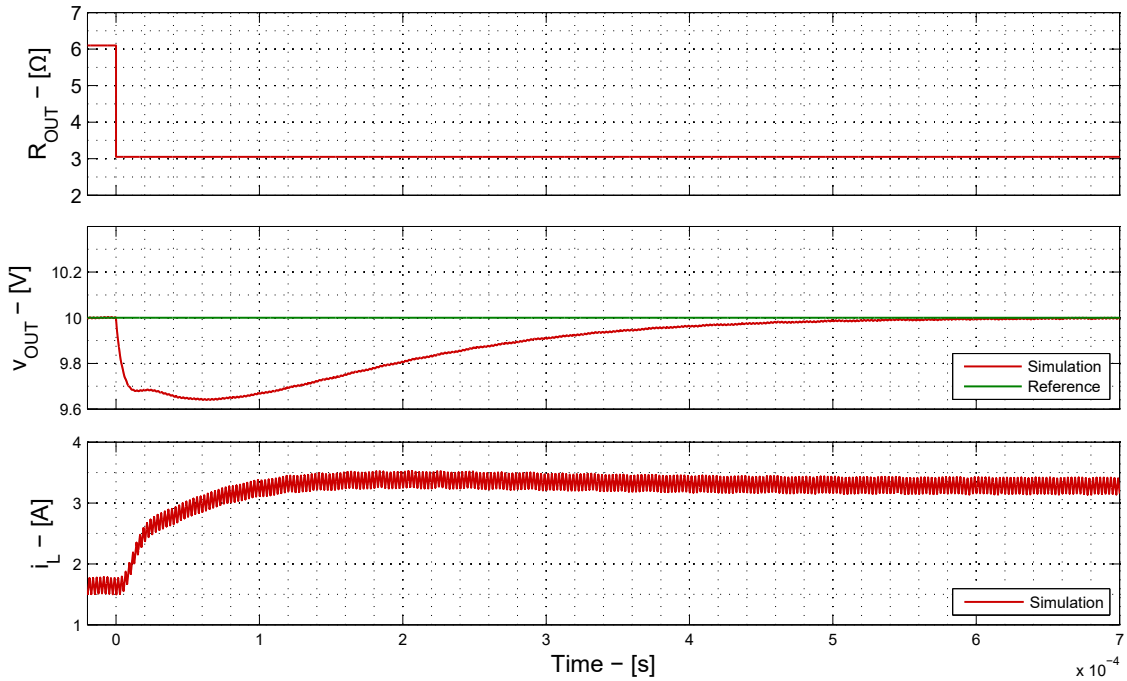

Figure 6.21: System response to a negative load step (the output resistance is halved). The simulations parameters are presented in table 7.1

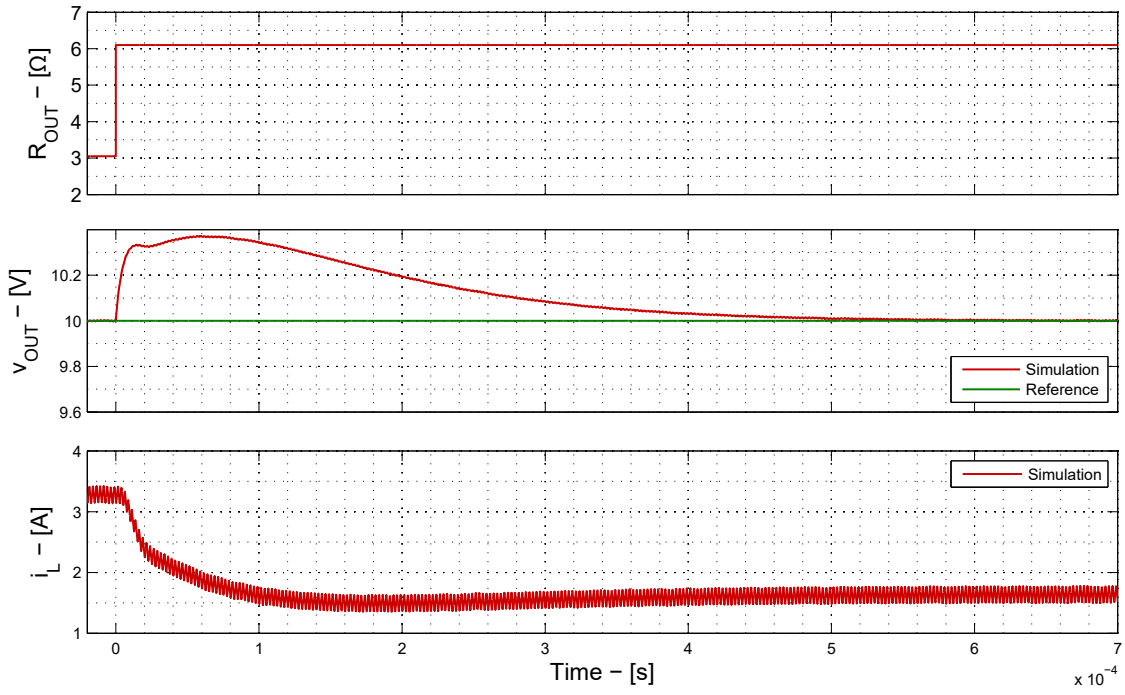

Figure 6.22: System response to a positive load step (the output resistance is doubled). The simulations parameters are presented in table 7.1

the s-domain. The proposed design is not optimized but serves as an example of how the controller can be sized and tuned. Further investigation could be carried out in order to determine an optimum design according to certain boundary conditions and improve the performance.

Simulation results have been presented to analyze the response of the system using the proposed control scheme. Firstly, reference voltage steps were applied to the input of the regulator in order to observe how the system responds to these changes. Secondly, the behavior of the system when the input voltage changes was analyzed. Lastly, the rejection of load steps is observed and analyzed from simulation results. It can be concluded that the proposed scheme presents a solid, robust and therefore satisfactory response to all these transient phenomena.

A practical implementation of the control scheme will be described in detail in the following chapter. The prototype designed earlier in this thesis work will be used to validate the response obtained with the average-current mode control approach. Since the platform used to implement the control solution is a digital system (dSPACE, which makes use of an FPGA), the compensator transfer functions will have to be discretized and expressed in the z-domain. This will bring up a series of limitations and considerations that will be analyzed in the next chapter.

7

Implementing the control scheme on the lab prototype

Chapter 7 focuses on describing the practical implementation of the proposed control scheme on the designed prototype. The first section sets out the basics to understand why and how the transfer functions that represent the compensator have to be discretized. General aspects about the implementation will also be presented here. Section 7.2 addresses the discretization from an analytical point of view. The discrete-time equation that models the controller will be derived here. Section 7.3 elaborates on how the implementation will be carried out. Practical limitations due to the fixed-point representation and the limited precision available will be discussed. In the end, the implementation of the compensators together with the whole system will be presented. Once the controller is working on the prototype, the system response will be analyzed and compared to simulation results to validate the performance obtained. Lastly, conclusions will be put together in section 7.5 as a summary of the work carried out in the chapter.

7.1. Introduction

The compensator transfer functions have been derived and expressed in the previous chapter in continuous time domain, that is, s-domain:

$$G_c(s) = K_c \frac{1 + \frac{2\pi f_z}{s}}{1 + \frac{s}{2\pi f_p}} \tag{7.1}$$

As stated before, there will be two control loops, one closed around the other. Both the inner current loop and the outer voltage loop will make use of a compensator in the form of the expression above. The gain term and the position of the poles and zeros have already been discussed and presented in chapter 6.

This transfer function in the s-domain could be implemented in practice by means of an operation amplifier with a set of passive devices (namely capacitors and resistors) which would define the position of the poles and zeros, as well as the gain of the controller. This is typically known as an analog compensation network, and could be done on silicon making use of Infineon's smart technology.

On the other hand, the control topology could also be implemented in the digital domain. Let us imagine that an ADC would be used instead of having an analog readout of the signals. Then, a digital value resulting from the ADC conversion would be available at each sampling period. If the sampling period is made short enough, this digital and discrete implementation could be considered a good approximation of the formerly presented analog approach.

For this specific application, the control solution will be implemented on the lab prototype making use of a dSPACE system. Such platform makes use of a PowerPC (PPC) and an FPGA interacting with

each other. The former will communicate to the PC (and therefore the user) and perform a series of calculations at a speed in the order of kHz. The latter will interact with the ADCs and perform a series of simpler calculations (fixed-point) but at a much higher speed (in the order of MHz). Consequently, the control scheme will be implemented on the FPGA platform making use of a discrete control scheme. The PowerPC will send the required set of parameters given by the user to the FPGA so that it could operate according to the desired conditions.

As a result, the proposed transfer functions will have to be discretized to the z-domain. This way, the expected response of the system with a continuous time domain compensator could be compared to its equivalent discrete implementation. However, several aspects and limitations will have to be taken into account.

Firstly, the sampling rate of the ADC will impose an upper limit on the maximum frequency component that can be properly represented in the digital world. For this application, the ADC will present a sampling frequency of 10 MHz. Part of the frequency response of the transfer functions will be modified due to the discretization. However, since the Nyquist frequency is well above the frequencies of interest, the response of the digital implementation will be assumed to be comparable to that obtained with the analog and continuous approach.

Secondly, the precision with which the transfer function coefficients are expressed will bring up another limitation. Since the FPGA is only capable of performing fixed-point operations, certain care will have to be taken when implementing the controller. On the other hand, due to the integer character of the compensation, the result of future computations will depend on previously obtained values. That is, the capability to keep track of previous computations with certain precision will also bring up a limit on how many decimal bits will be necessary to control the system successfully.

7.2. Discretizing the compensator transfer functions

The discretization of the compensator transfer function will be performed in order to come up with an expression in the z-domain that could be later on implemented on the digital system. The zero-order hold (ZOH) or forward Euler method provides an exact match between the continuous- and discrete-time systems in the time domain for staircase inputs. This will be a good approximation to the application of interest since the inputs to the compensators will be of this type (a new readout will come from the ADC sampling period). The following substitution can be applied in order to discretize a given continuous-time transfer function:

$$s = \frac{z-1}{T_s} \tag{7.2}$$

If this is done, the compensator transfer function in the z-domain results:

$$G_c(z) = \frac{y_c(z)}{u_c(z)} = \frac{a_1\, z - a_2}{z^2 - b_1\, z + b_2} \tag{7.3}$$

$$a_1 = K_c\, 2\,\pi\, f_p\, T_s \tag{7.4}$$

$$a_2 = K_c\, 2\,\pi\, f_p\, T_s \left(1 - 2\,\pi\, f_z\, T_s\right) \tag{7.5}$$

$$b_1 = 2 - 2\,\pi\, f_p\, T_s \tag{7.6}$$

$$b_2 = 1 - 2\,\pi\, f_z\, T_s \tag{7.7}$$

That is, the coefficients of the discrete transfer function depend on the gain term and the position of pole and zero. Their sign is taken out of the coefficient expression. This expression can be further modified to get a better insight on its implementation:

$$G_c(z) = \frac{y_c(z)}{u_c(z)} = \frac{a_1\, z - a_2}{z^2 - b_1\, z + b_2}\,\frac{z^{-2}}{z^{-2}} = \frac{a_1\, z^{-1} - a_2\, z^{-2}}{1 + b_1\, z^{-1} + b_2\, z^{-2}} \tag{7.8}$$

Let us express the same equation as a function of the input and output of the compensator:

$$y_c(z) = a_1\, z^{-1}\, u_c(z) - a_2\, z^{-2}\, u_c(z) + b_1\, z^{-1}\, y_c(z) - b_2\, z^{-2}\, y_c(z) \tag{7.9}$$

Multiplying a signal by z^{-1} is equivalent to applying a one-sampling-time delay. Then, the output can be expressed as a function of the obtained samples at $t = t_k$:

$$y_{ck} = a_1\, u_{ck-1} - a_2\, u_{ck-2} + b_1\, y_{ck-1} - b_2\, y_{ck-2} \tag{7.10}$$

That is, the output of the compensator can be calculated from the delayed input and output times the corresponding coefficient. It could be seen as well as a digital filter. The implementation would require 4 multiplications by constants, 2 substractions, 1 sum and 4 registers to store the delayed input and output readouts. Since average-current mode control makes use of two loops, this would have to be implemented twice. The coefficients will be calculated separately for the inner current and outer voltage loops. The input to the outer voltage loop will be the voltage error (output voltage reference minus output voltage readout); the input of the inner current loop will be the current error (output of the voltage loop minus coil current readout).

7.3. Implementing the control scheme on the dSPACE

Once the compensators have been expressed in their discrete form and the digital implementation is clear, certain practical limitations have to be taken into account. The transfer functions will be implemented on an FPGA environment which is only capable of performing operations with fixed-point numbers. The coefficients of the digital filter will be therefore truncated or rounded due to the limited precision of fixed point. This could yield a different frequency response due to altering of gain and pole / zero position.

7.3.1. Representing the filter coefficients with fixed-point precision

A re-scaling of the coefficients will be performed in order to maximize the fixed-point precision and obtain a good performance with the digital filter. Let us assume that the filter coefficients will be represented with a word length of n bits. Since the sign is known beforehand, an unsigned representation will be sufficient.

The first step in order to maximize the precision is to calculate the position of the first non-zero element in binary representation of the coefficient. This way, the unnecessary left-hand zeros could be shifted out of the fixed point representation and more significant bits could be represented with a word length of n. This can be easily calculated with the expression:

$$f \leq log_2 \frac{1}{c_i} \tag{7.11}$$

Where f will be an integer and c_i the coefficients of the digital filter to be implemented. It can be observed that the formula will yield a positive value if the coefficient is lower than 1 and a negative value if the coefficient is larger than 1. Once the value f is obtained for each coefficient, a shifting operation will be performed in order to actually re-scale the coefficient:

$$c_i' = c_i\, 2^n\, 2^f \tag{7.12}$$

That is, the re-scaled coefficient will be a result of shifting the comma position of the original value (n+f) rightwards. Then, a truncation to n bits will take place in order to represent the coefficient with the available precision. This approach will allow to minimize the error between the original digital filter expression and its implementation with a limited amount of bits.

Figure 7.1 shows a practical example of how the re-scaling is performed. In this case, c is equal to 0.0835789. According to the expression above, f will equal 3.The binary representation will have

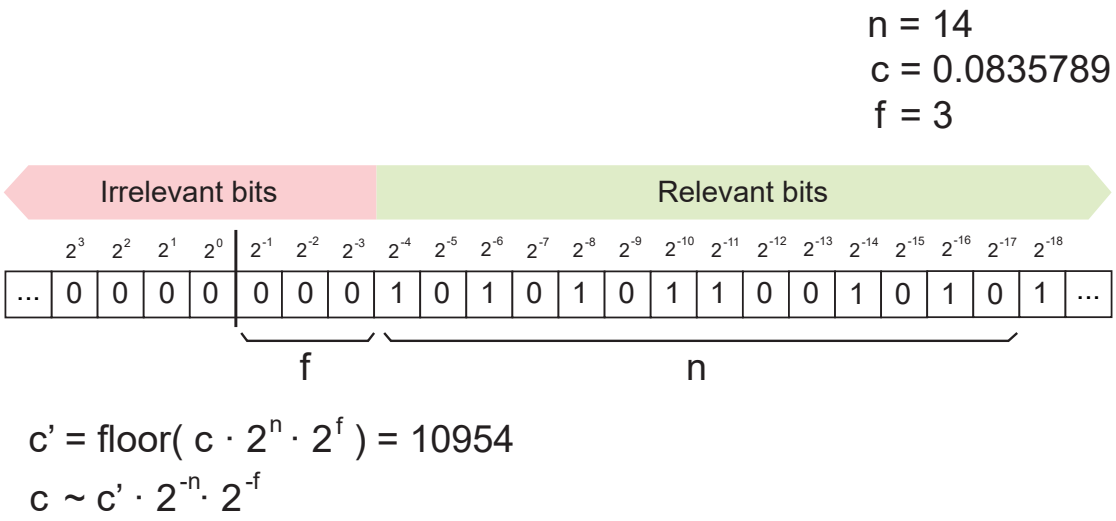

Figure 7.1: Practical example of how the filter coefficients are re-scaled. For this case n = 14

only zeros at the left of the comma position since the coefficient is lower than 1. What is more, the amount of zeros at the right of the comma position will be given by f. This way, the coefficient can be re-scaled to maximize the number of useful bits that actually contain relevant information. Once the binary representation is truncated to the word length (14 for this example), the re-scaled coefficient is obtained. This approach will be followed for each coefficient, and each of them will yield a different value.

As expected, once the coefficient is multiplied by its corresponding signal, the resulting value will be shifted back to its original position. It can be concluded that a coefficient word length of 14 bits is enough to successfully represent the compensator transfer functions of the proposed controller designed without modifying its response for the frequency range of interest.

7.3.2. Additional considerations

As mentioned, the coefficients of the digital filter will have a limited precision due to the limited amount of bits used to represent numbers in fixed-point format. Additionally, the internal operations performed by the controller will also result in decimals and non-integer results.

It has been shown that the output of the digital filter is a function of input and output together with their delayed values. Consequently, the internal precision of the calculations performed must be good enough to keep track of signal changes. That is, a minimum number of decimal bits for the fixed point representation must be guaranteed so that the controller will work as expected. Simulation results have proven that X decimal bits are enough to successfully keep track of signal changes and obtain a performance comparable to that obtained with the continuous-time transfer function.

Besides this, care must be taken to avoid overflow when performing operations with fixed-point representation. For this reason, the subtractions will always be performed before the final sum. Additionally, the width of the results must be enough so that no overflow will take place.

7.3.3. Implementing the digital filter

Figure 7.2 depicts the block diagram of the compensator implementation. It gives a good overview of how the solution will be implemented on the dSPACE. The approach followed is based on using a Simulink Toolbox (Xilinx System Generator) that includes simple blocks. These will be used to build up more complex digital circuits that eventually form the compensator. It can be seen how the error is initially calculated by performing a subtraction. The resulting signal is passed through two register blocks that will store the delayed error. The coefficients are multiplied to their corresponding signal and

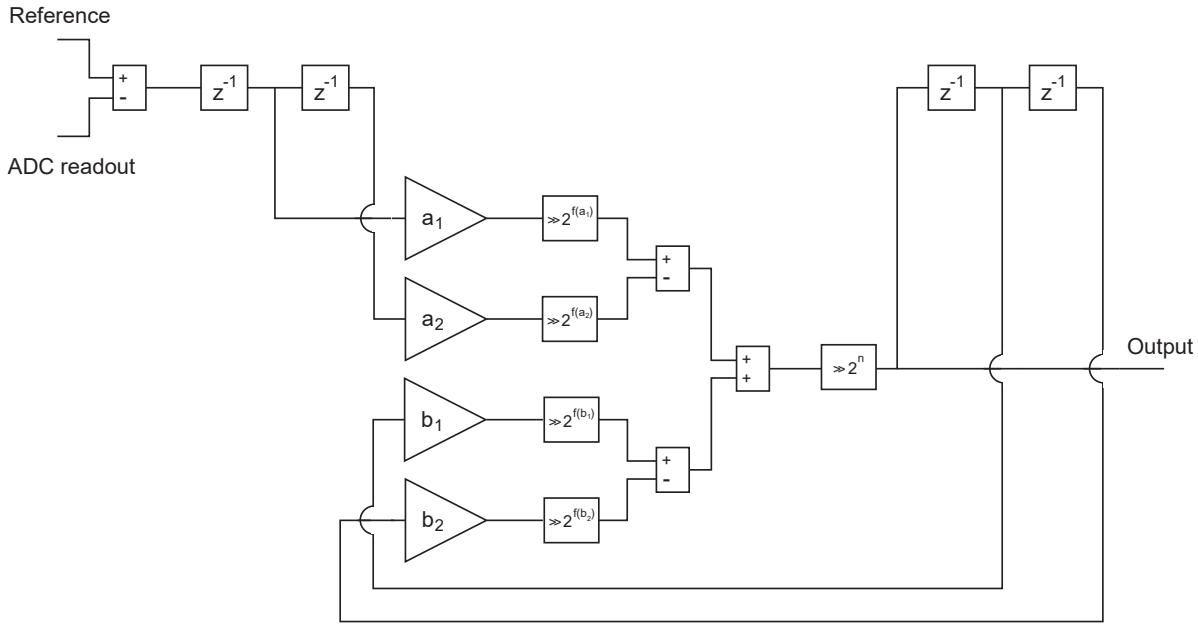

Figure 7.2: Block implementation of the discrete-time compensator

then shifted back f number of bits. An additional subtraction will be performed to ultimately sum up the terms coming from input and output side. Lastly, the result will be shifted back n bits. The output of the controller will be taken from this point. It can also be noticed how two more registers will be needed to delay the output signal.

This block will be implemented twice with their corresponding coefficient to form both the inner current and the outer voltage loops. The voltage loop will precede the current loop and the output of the former will serve as the reference input of the latter. This way the average-current mode control scheme will be built as described in chapter 6. The reference input of the voltage loop will be given by the user. The ADC readout of the voltage loop will be the output voltage signal coming from one of the dSPACE ADC channels. Similarly, the coil current will be translated to digital by an ADC channel and send to the current loop compensator block.

7.3.4. Implementing the full system

Once the key element of the control has been implemented, a series of additional blocks have to be designed so that the system will work autonomously. A series of input parameters will be set by the user such as gate current level, switching frequency, maximum coil current, maximum output voltage and operating point. This will be sent to the FPGA internally (the user does not have to design this interaction). Additionally, the FPGA will also set a group of variables that will be sent back to the user for monitoring purposes. These include the ADC measurements and the state of the system. Figure 7.3 presents a block diagram of the overall system implementation.

Firstly, a state machine will be implemented to keep track of the converter operation. Five different states will be defined: idle, start-up, running, overvoltage and overcurrent. The former will be considered as the initial default state: the switch will be forced off and therefore the output will remain zero. When the user gives the start signal, the system will enter start-up. A ramp will be sent as the voltage reference to the outer loop in order to achieve a smooth start-up to the desired operating voltage point. Once the system has reached the desired output voltage, the converter will enter running mode. At any moment, overcurrent and overvoltage faults can be detected. This will trigger a transition to the corresponding fault mode. These modes will only be exited when the triggering fault is cleared and when the user sends a resetting flag. This block will run at the FPGA frequency: 100 MHz.

The start-up ramp sent to the outer voltage loop must be generated by the FPGA as well. For this

reason, a ramp generator block has been designed. A counter will be used to increment the reference every certain amount of FPGA cycles until the desired operating point is reached. Once this happens, the ramp generator will set a flag to indicate the state machine that the ramping up process has finished successfully and that running mode can be entered. This block will also run at 100 MHz.

In order to detect overcurrent and overvoltages faults, a monitor block will be implemented on the FPGA. The ADC readout of the corresponding signals will be monitored and compared to a maximum allowed value. Since the ADC sampling frequency is 10 MHz, this blocks will run synchronously at the same speed. In case a fault is detected, a flag variable will be sent to the state machine to trigger the corresponding transition.

The outer voltage loop will take the reference from a multiplexer controlled by the state machine: if the system is in start-up mode, the ramp will be selected; if the system is in running mode, the operating point will be forwarded to the reference of the voltage loop. Additionally, the output voltage readout will be sent to the voltage compensator to calculate the error. Consequently, this block will run synchronously to the ADC at a frequency of 10 MHz.

Similarly, the current loop will take its reference input from the output of the voltage loop. The readout of the coil current ADC channel will be forwarded to this block to calculate the corresponding current error. Again, the compensator block will run synchronously to the ADC at a frequency of 10 MHz.

The output of the inner current loop will serve as an input to the PWM. The modulator will be implemented by means of a counter running at the FPGA frequency (100 MHz) which is compared to the output of the current compensator. The reset of the counter will be triggered by the switching frequency parameter. This way, the saw-tooth analog waveform typically used for PWM will be emulated. It can be noticed how the smaller the switching frequency, the higher the PWM resolution will be. The modulator will output a boolean signal that will be sent to the driver to switch the DMOS as dictated by the control.

The boolean output of the PWM will be forwarded to a digital output of the FPGA which is connected to the driver PCB. Therefore, the control loop will trigger the switching on and off of the DMOS. It must be noted that the driver will introduce certain amount of delay and distortion with respect to the ideal duty cycle given by the control. However, the phase margin of the control scheme has been designed with sufficient room so that the system will still be stable. The higher the switching frequency, the higher the impact the driver will have on the overall response of the system.

Lastly, the current level will be set by the user. It can be changed accordingly to the DMOS requirements. In the end, the corresponding digital value will be forwarded to a DAC channel. This will create an analog voltage sent to the driver PCB that will adjust the gate current level to the indicated value.

7.4. Measuring the system response

Table 7.1 summarizes the parameters and their nominal values that will be used for the comparison between the prototype and the simulation results. The prototype includes the hardware that was selected in chapter 4 of this document. Accordingly, the simulation parameters will be given so that they match with the physical implementation of the converter. It can be seen how the output capacitor will be implemented as two devices in the simulation: a 20 µF device with small ESR and a 100 µF capacitor with relatively large ESR.

The figures presented in this section will include both simulation and lab results that have been obtained to validate the consistency of the work carried out. The effect of the driver PCB was not taken into account for the simulation. In practice, the duty cycle command sent from the current loop to the driver will not be directly applied to the high-side switch. Due to the finite gate capacitance and gate current level, certain amount of time will be necessary to turn on and off the device. This will introduce delay and distortion with respect to the ideal duty cycle command given by the PWM. Also, the passive devices of the buck converter are treated as ideal and linear devices in simulation. In practice, tolerances and other non-linear effects (DC-bias, temperature, saturation...) will slightly affect the effective impedance of each componet. However, it will be initially assumed that all these non-modelled phenomena will have very little or no impact at all on the final results.

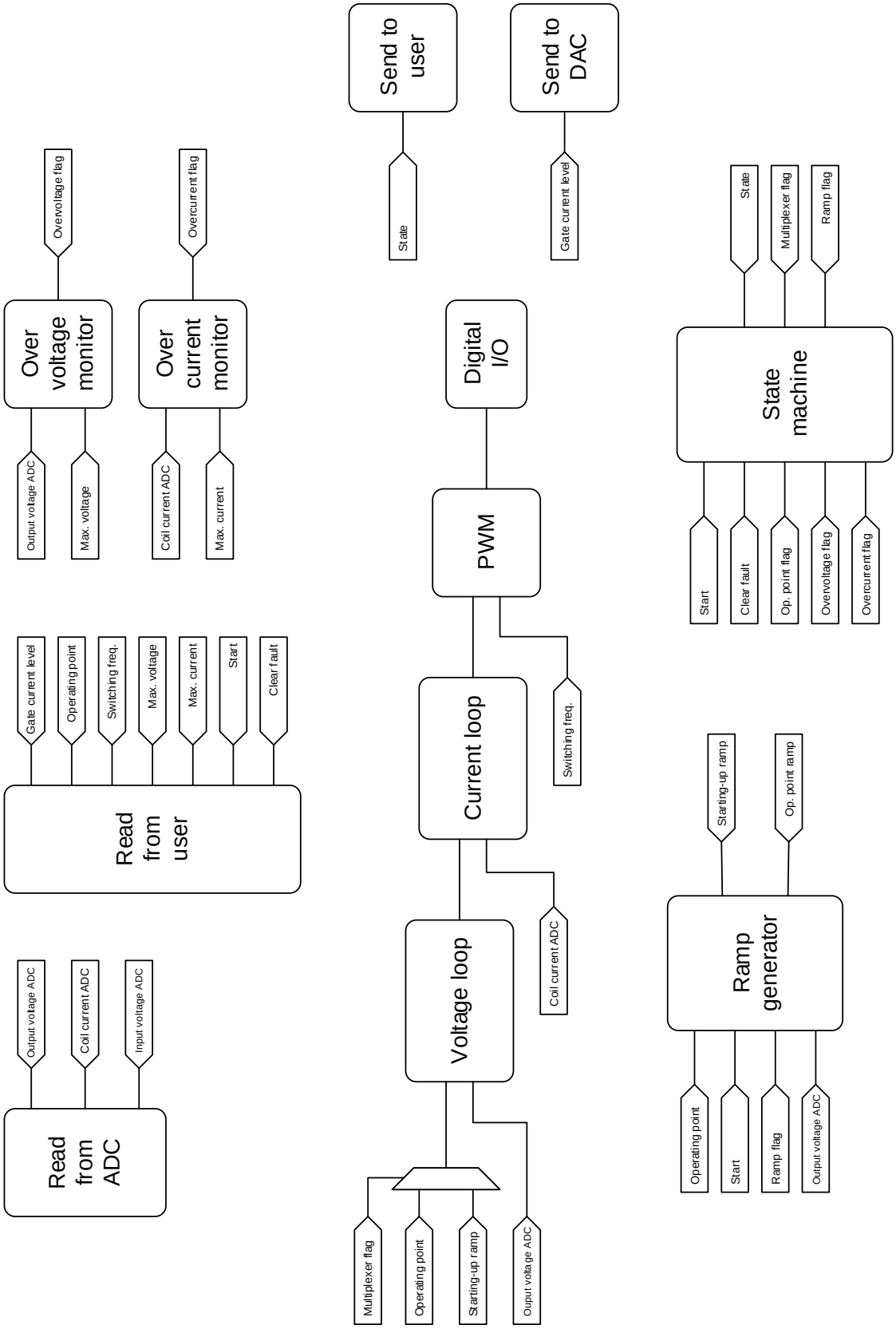

Figure 7.3: Block diagram of the system that will be implemented on the dSPACE to control the prototype

Parameter	Nominal value
L_{OUT}	47 µH
R_L	50 mΩ
$C_{OUT,1}$	20 µF
$R_{C,1}$	5 mΩ
$C_{OUT,2}$	100 µF
$R_{C,2}$	200 mΩ
R_{OUT}	6.1 Ω
V_{IN}	20 V
f_{SW}	400 kHz

Table 7.1: Simulation parameters and their nominal value used to obtain the results presented in this chapter

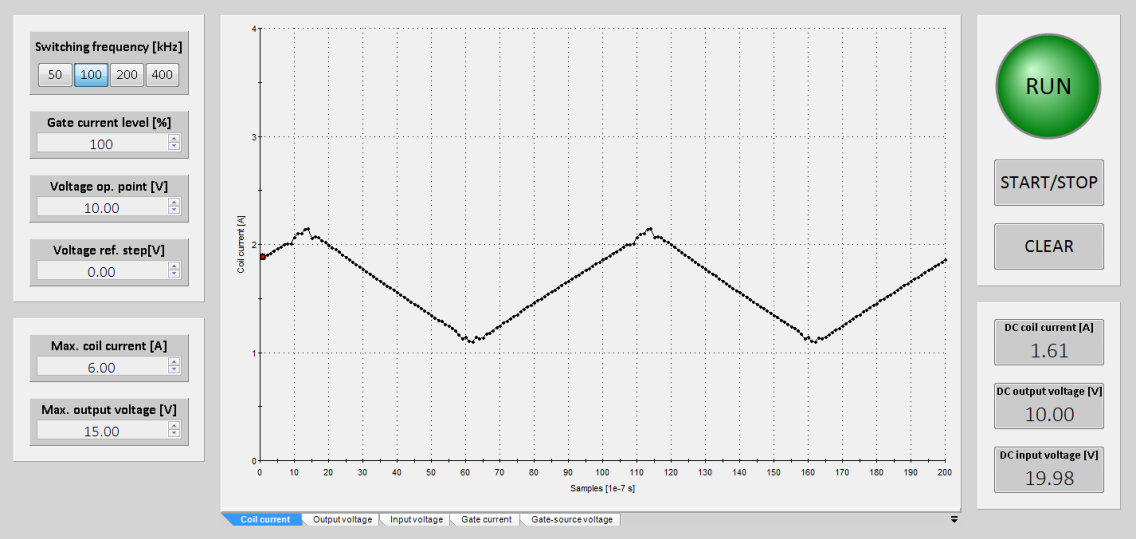

Figure 7.4: Screenshot of the GUI created to remotely control the converter from the PC

Figure 7.4 shows a screenshot of the graphical user interface that was designed to monito the system and send the input parameters to the dSPACE. The main values that can be set by the user are the switching frequency, the gate current level, the output voltage operating point, the maximum coil current allowed and the maximum output voltage allowed. A plot of some relevant system waveforms can be observed as well as the DC magnitude of coil current, output voltage and input voltage.

Firstly, the comparison will focus on the inner current loop. For this reason, the current loop will be operated separately without the outer voltage loop. With this approach, the user can set a coil current reference value. It will be interesting to observe this response since the dynamics of this loop are much faster than those of the outer voltage loop. Any possible discrepancies or mismatches could be observed here in a simpler way. On the other hand, a good matching between simulation and measured waveforms would indicate a successful modelling of the system.

Figure 7.5 plots the response of the system when a positive reference current step is applied to the reference of the current loop (from 1 to 2 A). The controller must be able to adjust the duty cycle command to the new corresponding value which would produce a DC coil current of 2 A. It can be observed how the matching between the simulation and the measured waveforms is extremely good. The biggest differences appear at the moment of the transient itself. These could be mainly caused by the driver. However, the response observed in simulation predicts the actual behavior very well. The amount of overshoot observed is in the order of 25 % and the step time is approximately 15 µs.

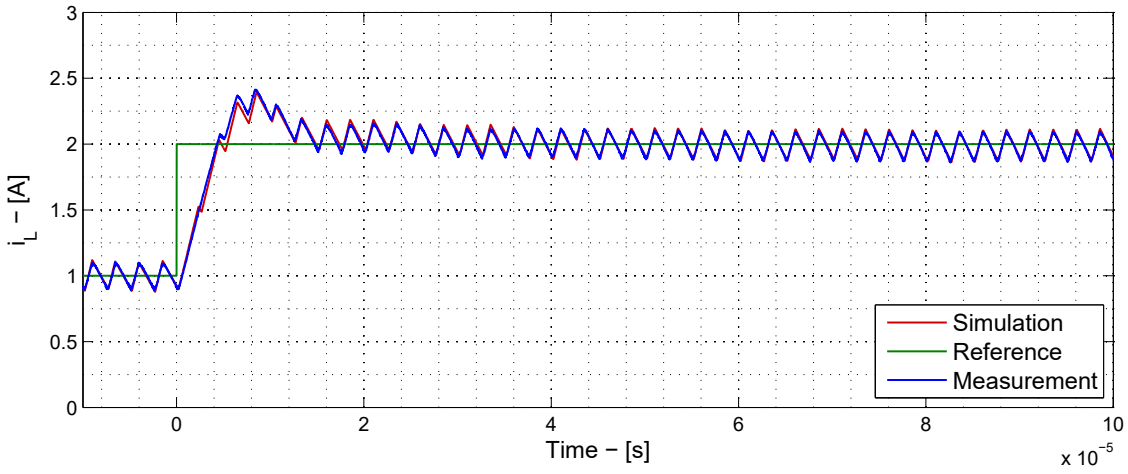

Figure 7.5: System response to a positive reference current step of 1 A. The simulations parameters are presented in table 7.1

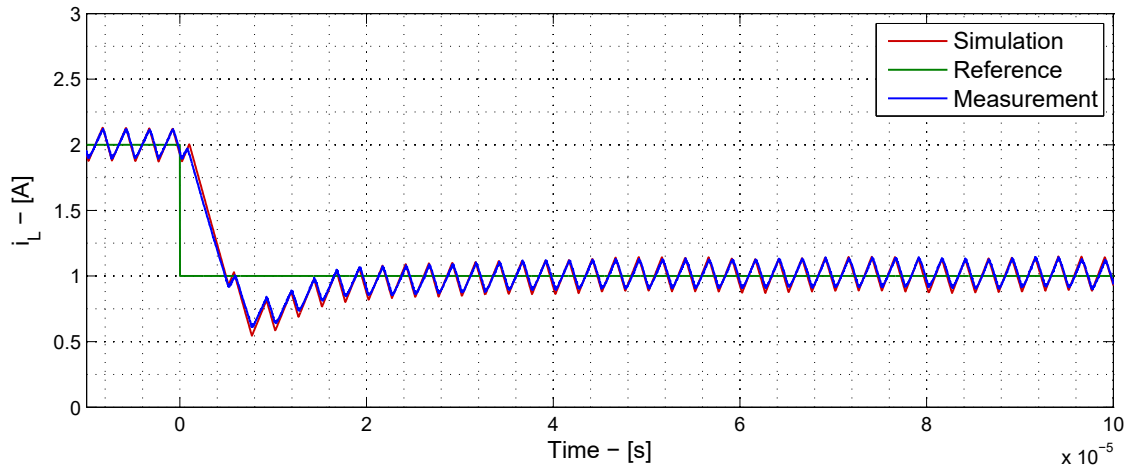

Figure 7.6: System response to a negative reference current step of 1 A. The simulations parameters are presented in table 7.1

Figure 7.6 depicts the waveforms observed when the opposite step (from 2 to 1 A) is applied to the reference of the current loop. Again, it can be seen how the controller is able to correct the duty cycle command to set the coil current to the desired value. The matching between the simulation and the prototype waveforms is very satisfactory. The differences are hard to notice and they could be mainly due to the driver PCB. The undershoot is in the order of 20 % with a step time around 15 µs.

Once the current loop has been evaluated and compared, it can be concluded that the simulation results predict very well the actual waveforms observed at the lab. As stated, the slight differences could be due to passive element's unmodelled phenomena and to the driver PCB which slightly delays and distorts the duty cycle command.

The relatively fast dynamic response of the current loop has been compared to validate the results. Similarly, the response of the system with the two loop structure (inner current and outer voltage) can be evaluated and compared. The first transient phenomenon that the converter has to react to is the starting-up. For this reason, both simulation and prototype waveforms during start-up have been plotted in figure 7.7. The ramping-up signal is sent to the converter at t = 0. From there on the voltage reference signal is increased until the final operating point is reached (10 V). It can be observed how the coil current ramps up as well to make the output voltage follow the increasing reference. Once the operating point voltage is reached, a very and almost negligible overshoot is observed at both simulation and prototype. In this case the output voltage is brought up from 0 to 10 V in approximately 1.4 ms. As for the coil current, its value guarantees that the output voltage sticks to the reference. Once the operating point is reached, the current stabilizes down at the steady-state DC value. It can

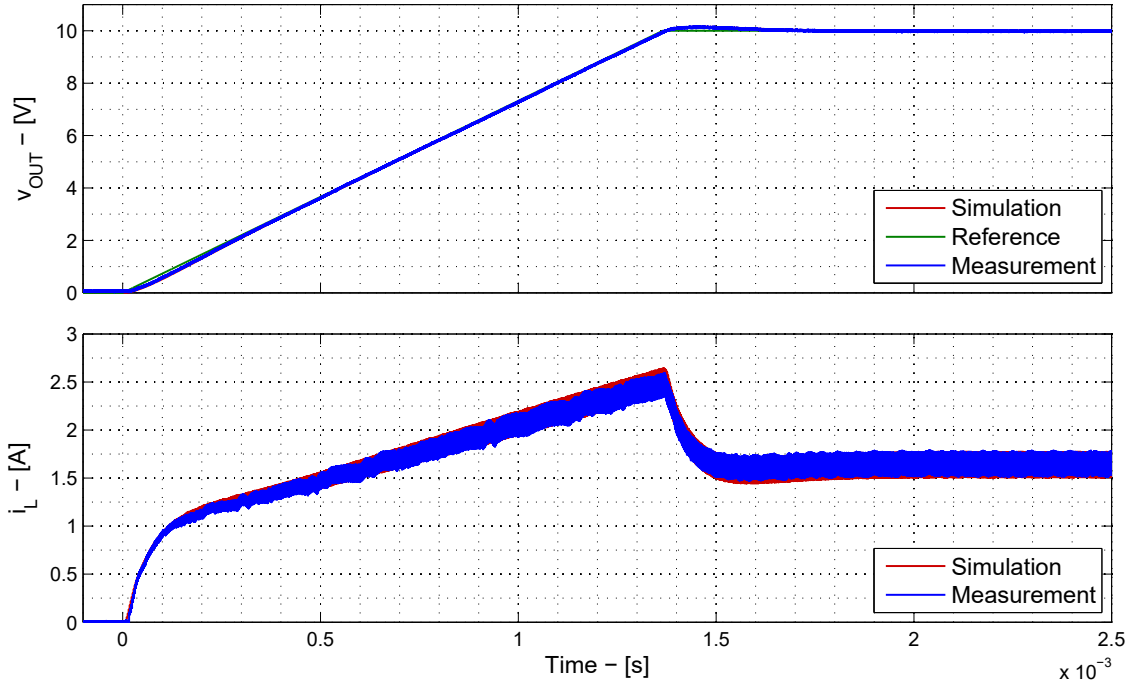

Figure 7.7: System response to a starting-up ramp to reach the operating point of 10 V. The simulations parameters are presented in table 7.1

be noticed how the matching between simulation and lab results is again very good.

The output voltage reference can still experiment changes even after the starting-up phase has made the system reach the operating point. This transient phenomena can be observed in figure 7.8, where a positive step of 0.5 V is applied at t = 0. As a result, the coil current is increased to charge up the output capacitors. A slight amount of overshoot is observed at the output voltage during this. The step time is in the order of 300 µs. Once the transient is over the coil current settles down at the new operating point DC value. Similarly, figure 7.9 shows the response of the system for a negative reference step of 0.5 V. The behavior observed here is very similar, with a slight amount of undershoot and a step time of approximately 300 µ. All in all, the matching between the simulation and measured waveforms is excellent for both cases.

7.5. Conclusions

The first conclusion drawn in this chapter is that the control topology can be implemented in the digital domain taking into account a series of considerations and limitations. The initial design was performed in continuous-time domain. However, since an FPGA-based system will be used to implement the solution in practice, the transfer functions had to be discretized. The main limitations associated to this approach can be dealt with if sufficient care is taken: re-scaling of the coefficient, good digital filter architecture to avoid overflow and guaranteeing enough precision to keep track of control input changes.

The results obtained with the prototype match extremely well with simulation results. There is hardly any noticeable difference for most cases. The small deviations could have their source on unmodeled phenomena such as passive mismatch, ADC conversion delay or the driver PCB. All things considered, the results and the matching are very satisfactory and they are proof that the prototype response is very robust and well-modeled.

After analyzing the obtained results compared to the simulation, it can also be concluded that the digital implementation is very solid and provides a response very similar to that obtained in simulation. Since the frequencies of interest are below the Nyquist frequency of the sampled system, the discrete approach gives almost identical results with respect to the analog continuous implementation.

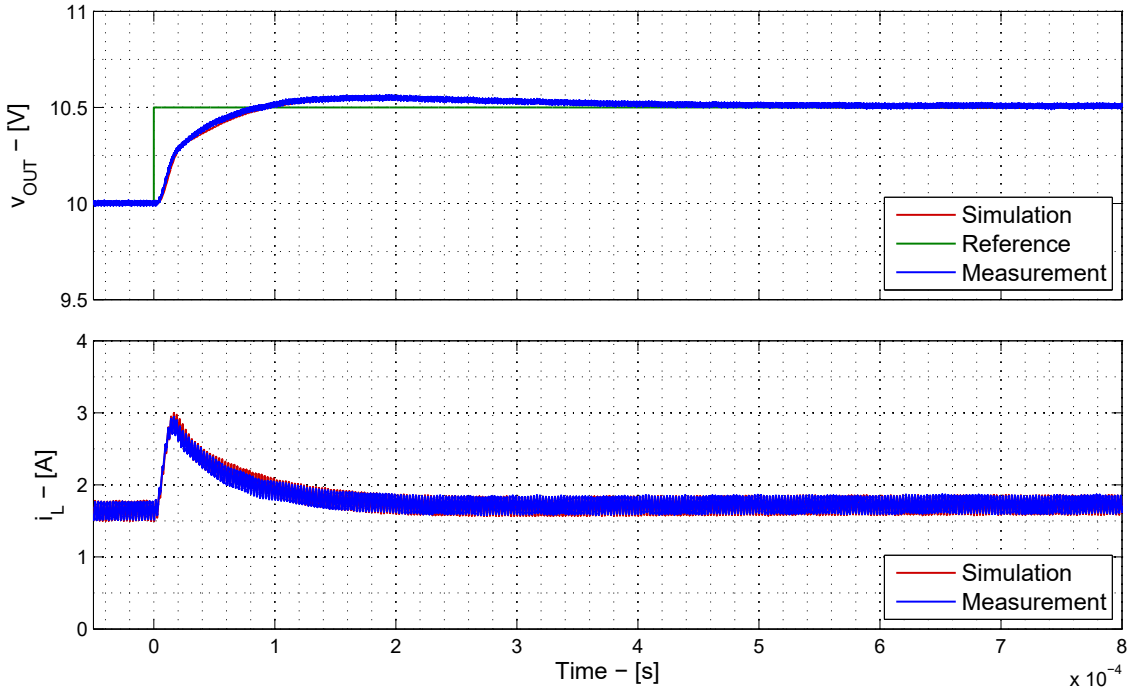

Figure 7.8: System response to a positive reference voltage step of 0.5 V. The simulations parameters are presented in table 7.1

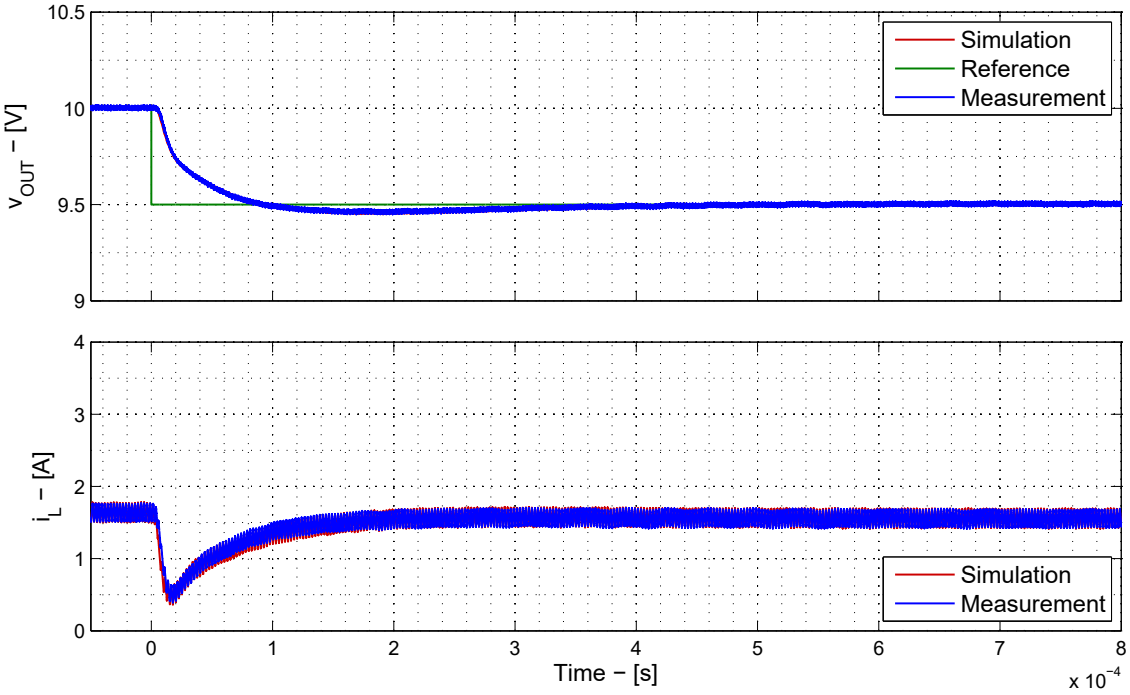

Figure 7.9: System response to a negative reference voltage step of 0.5 V. The simulations parameters are presented in table 7.1

Additionally, the driver has been observed to have a minor and almost negligible impact on the overall system response. Therefore, the assumption made during the design phase can be considered valid. All in all, it can be concluded that the converter is controlled successfully with the average-current mode control scheme. It must be therefore considered as a very robust and suitable topology when using buck converter for applications which are similar to that analyzed in this thesis work.

8

Final conclusions and future work

The last chapter of this document is intended to serve as a summary of the conclusions drawn throughout the different chapters of the report. Section 8.1 elaborates on the answers to the initially proposed research questions and their corresponding conclusions. Topics such as suitability of Infineon's smart technology for the application of interest, practical realization of the driver, selection of components, determination of efficiency, optimization of the prototype and selection and implementation of the control scheme will be discussed. Section 8.2 focuses on the future work associated to this thesis work which would allow to draw further conclusion on the presented line of investigation. Aspects related to the DMOS' size, converter topology and further setup optimization will be covered.

8.1. Final conclusions

The following sections present the drawn conclusions of the research work reported in this document. They will be presented to give an answer to the research questions which were initially formulated in the introductory chapter.

8.1.1. Suitability of Infineon's smart technology for LED driver applications

The suitability of smart technology for LED driver application was firstly tackled with a simulation approach described in detail in chapter 2. As for the gate current level, it was concluded that 100 mA is a good trade-off between viability of implementation and obtained performance: according to simulation, a smaller value would yield longer switching transitions times; going above 100 mA would not be really justified since it would not bring a big improvement as for switching speed. As a consequence, it was proven that a switching frequency in the order of hundreds of kilohertz could be achieved. More specifically, the maximum switching frequency will be a function of the gate current level supplied to the DMOS. The main limitation comes from the fact that transitioning between on and off states (and vice versa) takes a finite amount of time. This will introduce an upper limit in the realizable switching frequency.

In addition, it was observed from the results presented in chapter 2 that the duty cycle is affected by the gate current level and the switching frequency. On the one hand, the duty cycle range that the converter can operate at will be a function of the finite switching times and therefore depends on the gate current level. On the other hand, the finite and asymmetric switching times required to turn on and off the DMOS will introduce a deviation between the duty cycle given by the control and the actual value that is applied to the output filter of the converter. The higher the switching frequency, the larger this deviation will be.

The realization of the prototype led to further conclusions in this topic. First of all, it was concluded that the optimization of the setup was crucial to obtain a solid performance that would allow for validation of results. The measurements presented in chapter 5 clearly confirmed the conclusions drawn

in chapter 2 from simulation results: a switching frequency of 400 kHz can be achieved with a gate current level of 100 mA. The duty cycle deviation due to finite asymmetric switching times can also be seen when running the converter in open-loop. Another important interpretation of the measurements shown in chapter 5 is that additional parasitic capacitance will be present in the lab prototype of the system. These were not taken into account initially for simulation and and in practice they will slow down the switching transitions. All in all, the prototype results leads to confirming that Infineon's smart technology can be used for LED driving applications.

8.1.2. Realization of the floating high-side driver

The initial analysis performed with simulation software assumed a driver topology that would be implemented on chip using smart technology. That is, several transistors would be placed and connected on the silicon die to build the driver circuitry. Setting up the prototype required however a discrete realization of the gate driver as a first attempt in the early development phase to prove the suitability of smart technology for DC/DC applications. The simulation approach initially carried out could be considered still valid as long as gate current level and transition time requirements were met.

Chapter 4 presented a detailed study on two available gate driving circuits (system A and B). The first criteria to determine whether they could be used or not for the application of interest was based on specifications provided by each integrated circuit manufacturer in the corresponding datasheet. Out of this analysis, it was concluded that system B could be used to deliver a gate current level of 100 mA at a switching frequency in the order of hundreds of kilohertz.

Further investigation based on the prototype was performed to ultimately conclude that system B could be used as the driver circuit of the DMOS. The practical measurements presented and discussed in chapter 5 prove that the approach followed in chapter 4 is valid. However, optimization of the setup is crucial to guarantee an acceptable performance. The final conclusion is therefore that the prototype confirms the results observed with the simulation approach in terms of gate driver and switching frequency requirements.

8.1.3. Determination of the efficiency of the system

Chapter 2 presented an analysis of the switch losses observed in the simulation phase. The efficiency limit given in this chapter was assumed to be an upper boundary to the ultimate efficiency of the converter. An efficiency limit of approximately 96 % was observed for a switching frequency of 400 kHz. In practice, the slower switching due to parasitic elements will yield larger switching losses that will make the efficiency drop. On top of this, other lossy elements of the converter will significantly increase the total losses of the system. However, the obtained results allowed to conclude that the application is feasible in terms of power dissipation and thermal considerations.

Chapter 3 analysed the different loss mechanisms present in the converter to build a detailed loss model. First of all, a derivation of the converter waveforms in steady state was performed. After this, different loss modeling approaches were proposed to estimate the separate sources. The comparison between the loss model and the results observed in simulation allowed to conclude that the matching between the initially proposed loss model and simulation was very good.

The results given by simulation and the loss model were later on analyzed and compared to those obtained with the prototype of the system in chapter 5. The initially proposed loss model was concluded to be inaccurate and therefore a new one was derived. The improved loss model was corrected to take into account practical transition times of the DMOS (those observed in simulation corresponded to a converter without any parasitics). In practice, parasitic capacitance was added to the switching node, which slowed down the transitions and had an impact on the overall performance. Also, the inclusion of the losses related to sensing elements present on the DC/DC extension board allowed to bring both measurement and estimated efficiency curves closer. Altogether, it was concluded that the new loss model provides very accurate results. After improving both the loss model and the prototype setup it was proven that the matching obtained was very satisfactory. The validation of the obtained results served to confirm therefore that the loss model can be used to estimate losses accurately and that the prototype presents a very robust behavior. It was also concluded that a good understanding of the loss mechanisms as well as a good prototype setup are crucial to obtain good performance and matching.

8.1.4. Selection of converter passive elements

A general methodology to dimension the passive elements of the converter was presented in chapter 3. Such approach can be followed for a different set of boundary conditions and requirements. It was concluded that the passive elements of the converter can be chosen accordingly and further optimization could be carried out together with the loss model. For instance, the proposed approach could be used to size the passive elements and choose the best family of devices from a manufcaturer to maximize the efficiency of the system.

8.1.5. Optimization of the prototype setup

Chapter 5 explains how the minimization of parasitic elements is crucial to obtain good results. The prototype results initially obtained were not satisfactory enough and several possible root causes were identified in order to come up with a better setup. An additional PCB was designed to optimize the behavior of the system and minimize any possible parasitics that could degrade the performance of the converter. The focus was set on minimizing the parasitic inductance seen at the gate of the switch. Further steps led to conclude that the initially derived loss model was not accurate enough and that further investigations had to be performed in order to determine the mismatch. The experimental determination of diode and switch losses using modified setups led to a deeper analysis on an initially unmodeled phenomenon: the driver reference current. A couple of modifications to the driver board (system B) were also proposed in chapter 5 in order to obtain an even more solid prototype setup. Overall, the improvement of the prototype was characterized by a series of upgrades that gave rise to others at the same time. Simulation was also used to confirm the results observed in practice. In the end, the final setup was observed to present a solid and satisfactory performance that allowed to validate both simulation and practical results.

As for the efficiency of the converter with the optimized setup, it was concluded that the values measured at the lab were sufficiently good: peak efficiencies of 98, 97, 96 and 94 % were measured for 50, 100, 200 and 400 kHz respectively. The curves show a considerable efficiency drop for low current points, which can be expected by having a look on how the different mechanisms contribute to the whole losses. It was also confirmed that increasing the switching frequency yields lower efficiency for a given output current. On the other hand, increasing the switching frequency would allow for smaller and cheaper passive elements to meet the electrical requirements of the converter. On the whole, this aspect appears as a trade-off between the size and cost of the converter and its efficiency. It was concluded that an overdimensioing of the DMOS resulted in dynamic switching losses being much more dominant than conduction losses.

8.1.6. Selection and design of a suitable control scheme

A comparison between different control schemes was presented in chapter 6. It was concluded that the average-current mode control appears as the most advantageous and suitable control strategy for the application of interests. Aspects such as ease of design and implementation, performance and noise immunity were the main deciding factors. The control topology was described and a small signal model was presented in order to obtain the necessary transfer functions. The compensator properties and features were derived from these in order to meet certain stability and transient response requirements. It was concluded that a type-2 or PI compensation would be enough to close both loops with the desired amount of phase margin and crossover frequency.

A practical design of both current and voltage loops in the continuous frequency domain was proposed in chapter 6. This served as an example of how the controller could be sized and tuned. Simulation results were presented to analyze the response of the system using the proposed control scheme and to confirm that the analyzed control topology is suitable for the application of interest. Reference and input voltage steps as well as load steps were applied to observe the system performance. Altogether, it was concluded that the proposed scheme presents a solid, robust and therefore satisfactory response to all these transient phenomena.

8.1.7. Practical implementation of the control scheme

A practical implementation of the control scheme was described in detail in chapter 7. Since the platform used to implement the control solution is a digital system, the previously proposed compensator transfer functions had to be discretized and expressed in the z-domain. This was proven to bring a series of limitations that were analyzed in chapter 7 as well. It was concluded that if certain considerations were taken into account, the digital implementation of the solution would be satisfactory. These included aspects such as re-scaling of the coefficients, using a good digital filter architecture to avoid overflow and guaranteeing enough precision to keep track of control input changes.

The results obtained with the prototype were observed to match extremely well simulation results. It was concluded that the slight differences could be due to unmodeled phenomena such as passive mismatch, ADC conversion delay or the driver PCB. All things considered, the results and the matching were very acceptable and they stand as a proof that the prototype response is very robust and well-modeled. After analyzing the obtained results compared to the simulation, it was also concluded that the digital implementation is very satisfactory and provides a response very similar to that obtained in simulation.

8.2. Future work

Several interesting aspects related to the analyzed LED driver have been left for the future due to limitation of research boundaries and lack of time . Future work concerns deeper analysis of particular concepts, new proposals or simply curiosity. This section is aimed to serve as an introduction to aspects related to this thesis work that could be further investigated to draw additional research conclusions. Each of the subsections tries to outline directions for future lines of investigations.

8.2.1. Optimizing the size of the DMOS

Chapter 2 and 5 mentioned that the obtained efficiency curves always present a positive slope. This ever-increasing curve profile could be due to an overdimensioing of the DMOS. It would be then interesting to investigate the effect of using different DMOS sizes. If a smaller device was used, the associated capacitances would be smaller. As a consequence, the switching of the device would be faster, hence making dynamic losses smaller. As the main drawback, conduction losses would increase. From a qualitative point of view, if a smaller DMOS was used, higher efficiency curves for low current points where the dynamic losses are the main contributor could be expected. On the other hand, higher current points would experience a decrease in efficiency due to increased conduction losses. Overall, the optimum DMOS size would be a trade-off between dynamic and conduction losses which would result in the minimum total amount of losses. This optimization problem could be tackled making use of the available loss model. Then, the amount of silicon used to implement the DMOS in smart technology could be customized to minimize the overall switch losses and therefore maximize the efficiency.

8.2.2. Analyzing the synchronous buck topology

As presented in chapter 3, the diode losses can be modeled as:

$$P_D^{cond} = V_D\, I_D^{avg} + R_D\, I_D^{rms\,2} \tag{8.1}$$

The first term of the expression is related to an offset voltage coming from the inherent characteristics of diode devices. The second term is associated to the finite resistance of the silicon used to build the rectifying device. Let us assume that a synchronous topology was use instead: the low-side passive device, namely diode, would be substituted by an active switch. By default, the operating characteristics of active devices are such that the term associated to the offset voltage (V_D for the diode) is almost zero and could be neglected. Then, the low-side device conduction losses could be expressed as:

$$P_{LS}^{cond} = R_{LS}\, I_{LS}^{rms\,2} \tag{8.2}$$

That is, using a low-side MOSFET would eliminate from the expression the term assiciated to V_D. On the other hand, additional sources such as dynamic switching and gate driver losses would be introduced. Additionally, the complexity of the driving circuitry would be slightly increased since an extra gate driver would have to be used. However, the driver design of the low-side device would be much simpler than that required for the high-side switch. Also, additional complexity would be introduced in the control scheme due to, for instance, introduction of dead-time to avoid short circuiting at the input supply. Altogether, the synchronous topology appears as another degree of freedom to consider when designing the LED driver. As a first qualitative approach, it could be expected that a synchronous topology would be very beneficial for applications that require a relatively large amount of current. This way, large diode conduction losses would be replaced by smaller low-side active device's dynamic switching losses. This optimization problem could be tackled as well making use of the loss model to estimate the efficiency for different operating points.

8.2.3. Measuring the system response with an LED load

The analysis carried out throughout this thesis work assumes the output load to be a resistor. That is, the impedance connected at the output of the converter that dictates the relationship between voltage and current is a resistance. In practice, the designed converter will be used to drive LED loads. The characteristics of these device are significantly different to those of a resistor. LEDs can be model in a first approximation as a resistance in series with a voltage source. The former will account for the effect of current in the voltage drop across the device to match the effective curve; the latter will account for the initial offset voltage required to forward bias the pn junction and light up the device. This equivalent resistance is known in the literature as dynamic resistance and will correspond to the slope of the V-I curve. The magnitude of both the offset voltage and the dynamic resistance varies significantly with respect to the type of LED used.

Using such equivalent circuit to emulate the impedance of the LED at the output would model more accurately the response of the system in real applications. The small-signal model would include the value of the dynamic resistance and therefore the compensator could be optimized for a specific LED load. Additionally, the response of the system to transient events would be different to that observed with fully resistive load. It would be interesting to evaluate the system response in both simulation and prototype to draw additional conclusions on how the system performs.

8.2.4. Implementing the solution on silicon using Infineon's smart technology

The ultimate goal of using Infineon's smart technology for LED driver applications would consist in realizing the solution on silicon. Power and control could be implemented on chip: the former would include the driver circuitry for the high-side switch and the DMOS itself; the latter could make use of either a digital or an analog implementation (or a combination of both). The voltage level above battery could be obtained in practice by making use of bootstrap capacitor and diode. Such capacitor would be charged through the diode from the main power supply during the off-time. When the power transistor is to be turned on, the source voltage would go above the input voltage level provided the design works as expected and the diode would block the reverse current flow from capacitor to input voltage. The gate driver circuit could consist of two main subcircuits: a current source based on current mirrors (similar to the concept presented in this thesis work in chapter 2 but with fewer transistors since the silicon area would have to be taken into account); and single switches connecting the gate of the DMOS to either the positive or negative rails of the gate driver circuit. The former would provide a base charging / discharging current to the DMOS which would guarantee reaching the desired gate-source voltages during on and off states. The latter would provide an initial drive to the DMOS so that an initial peak current would bring the gate-source voltage to the threshold level much faster.

If an analog control loop were to be realized, an operation amplifier could be built in smart technology. The desired compensation network could be placed around the op-amp making use of passive devices sized accordingly to obtain certain frequency response. On the other hand, if a digital control loop were to be realized, ADC devices would have to be implemented in smart technology. The compensator could be then implemented by means of a digital filter, similar to the approach presented in this report. In summary, the complexity of this research line is evidenced by the several amount

of considerations that would have to be taken into account. The prototype implementation approach presented in this report serves as the first step in the product development phase.

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