A NMOS Linear Voltage Regulator for Automotive Applications

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Abstract

The electronization of automobiles is considered to be a revolution in automotive technology development progress. One trend for automotive electronics design is pursuing higher level integration. System level integrated circuits are needed to simplify the automotive electronics design and increase the reliability of automobiles.

In this thesis, a prototype of linear voltage regulator is designed for system level integration. Instead of conventional PMOS linear regulator topology, a NMOS power transistor is chosen as the pass device on considerations of smaller silicon area and better dynamic performance. The characteristic differences of PMOS and NMOS linear regulators are analyzed. Based on the frequency behavior analysis of these two types of regulators, a frequency compensation scheme for the NMOS linear regulator is purposed in this thesis. This purposed scheme is able to accommodate the wide frequency variation of the NMOS linear regulator output pole. The effectiveness of frequency compensation is examined by both mathematical modeling and transistor level simulation. The over-current protection of the NMOS linear regulator is also designed, which is realized by applying another current regulation loop to the voltage regulator. This NMOS linear regulator is able to maintain a constant output current around 250mA in over-current protection scenario.

Compared to the existing PMOS linear regulator counterpart, the off-chip ceramic capacitor of this NMOS linear regulator can be reduced to 220nF (10x smaller) without sacrificing the $\pm 2\%$ output voltage accuracy within -40°C$\sim$175°C. The regulator quiescent current at no current load scenario is 12μA. Owing to the introduction of adaptive biasing scheme, the maximum quiescent current is 1.31mA. This adaptive biasing only degrades the current efficiency by maximum 4%.

At the end of the thesis, possible maximum load current and external capacitor scaling abilities of this NMOS linear regulator are discussed.

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Chapter 1

Introduction

Ever since the first modern automotive vehicle was built in Mannheim, Germany by Karl Benz in 1885 [1], it has changed the human society in a great deal. The invention of automotive vehicles shortened the distance between individuals and brought more convenience to human beings. The automobile is always considered as one of the greatest inventions of the 20th century. With the increasing development of electronic technology since 1950s, electronic devices embedded in automobile has shown significant advantages in aspects of controllability, comfortability and safety. Electronic components currently comprise 20-30% of total costs for all automotive categories, this figure is expected to reach 40% or so by 2015 [2]. In this thesis we will discuss power management in automotive vehicle and focus on NMOS linear voltage regulator design.

1.1 Power Management in Automotive Vehicles

Beside the huge mechanical system, a modern automobile vehicle can also be recognized as a complex electrical system. Power management is an indispensable part of the electrical system, which provides separate supply voltage and current driving capabilities. Take the Audi A8 for an example, the electric front screen heating is with an approximate power consumption of 1000 Watts[1], the car audio system is powered by 12V and consumes 80 Watts on average[2]. With more and more electrical modules installed on cars, both the increasing power consumption and load versatility complicate the power management system.

Figure 1.1 shows a simplified power management system in a car. This system handles the battery charging through a generator (stator and rectifier). The generator voltage control is used to regulate the generator output voltage to 12V. The battery is supplying power to separate electronic control units (ECUs) and other electric modules.

ECU is an embedded system that controls one or more electrical systems or subsystems. Modern automotive vehicles can feature up to 70 ECUs, such as airbag

[1]Source: Bosch and ADL research

[2]Source: Wikipidia and ADL research

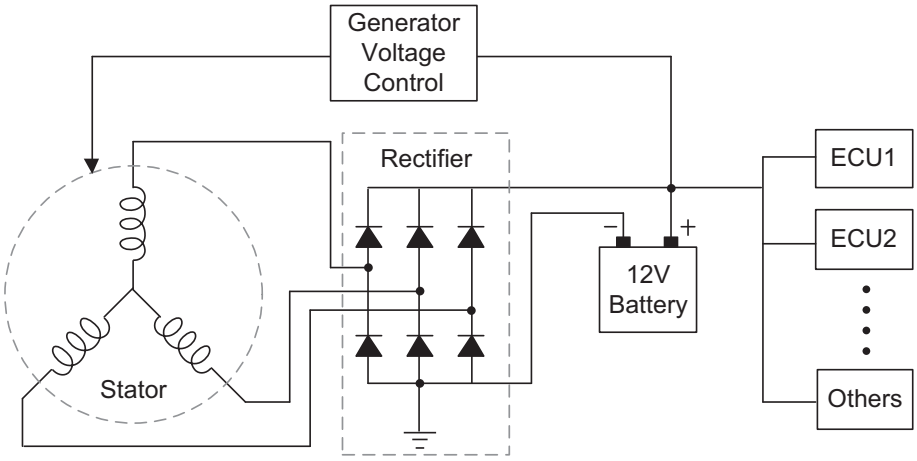

Figure 1.1: A symplified automotive power management system.

control unit, body control module[3], engine control unit, brake control module and so on.

An example of an automotive ECU is shown in Figure 1.2. It consists of power management, data transmitting and receiving, micro-controlling, sensing and actuation modules. The ECU is powered by a typical value 12V lead-acid battery. Normally, many electronic devices inside the ECU need lower voltage than this battery supply. Therefore, a power management module with DC voltage conversion is essential. To communicate with other modules, transmitters and receivers are included in the "In Vehicle Networking" part. Micro-controller is the central processing unit of the ECU. Sensors and actuators are modules which can acquire and transfer data between electronic domain and other domains.

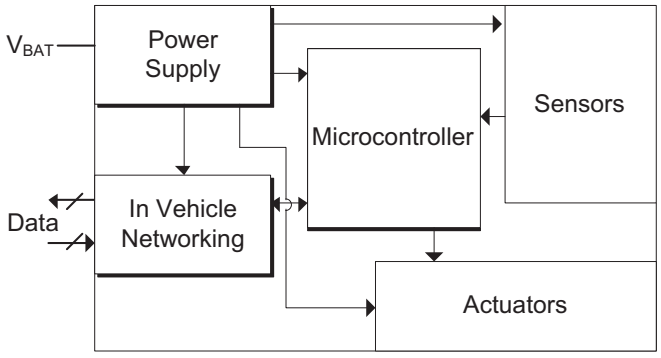

Figure 1.2: A typical ECU diagram.

[3]Which controls door locks, electric windows, etc.

1.2 Linear Regulator and Switch Mode Power Supply

A linear voltage regulator is a DC voltage converter which realizes its function by linearly regulating the input DC voltage to a lower output DC voltage, as shown in Figure 1.3(a). Since the output voltage is linearly regulated, it has advantages in aspects of dynamic response, output noise and power supply rejection, etc. The major disadvantage of linear regulator is the power conversion efficiency. When the load current is high, the power loss can be dramatic. This makes linear regulator not a suitable candidate for some systems where large output currents are required.

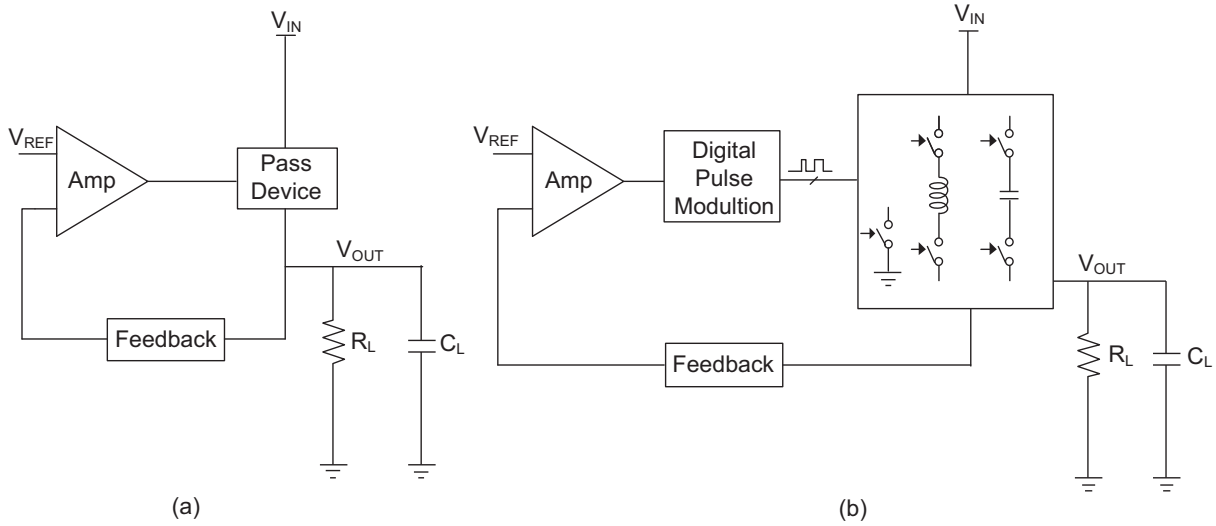

Figure 1.3: DC voltage converter topology (a) linear regulator and (b) switching regulator.

Switch mode power supply (SMPS) is a type of switching regulator which realizes power conversion with a control mechanism in the discrete time domain, as shown in Figure 1.3(b). Generally, at least one energy store component (either an inductor or a capacitor) is required in a SMPS. The fundamental principle of SMPS and linear regulator is similar. For a switching regulator, there is also a feedback loop that regulates the output voltage to its desired value. If the output voltage is not as expected, the discrete time control will decide to charge or discharge the energy store component by modulating the pulse width or frequency. The advantage of switching regulator is its efficiency can easily reach up to 80%∼90% or even higher [3]. The drawbacks are in aspects of dynamic response, output ripple and cost. The dynamic response of switching regulator can be affected by its limited bandwidth. The output ripple is caused by switching activities. The higher cost of switching regulator comes from design complexity and off-chip components. For an inductor based switching regulator, the off-chip component may include an inductor and a capacitor, while the linear regulators may only have one external capacitor, which is cheaper. The comparison of linear and switching regulator is shown in Table 1.1.

Table 1.1: Comparison of Linear and Switching Regulators

	Linear regulator	Switching regulator
Output range	$V_{OUT}<V_{IN}$	$V_{OUT}<V_{IN}$ or $V_{OUT}>V_{IN}$
Dynamic response	Fast	Slow
Efficiency	Low	High
Noise	Low	High
Cost	Low	High

1.3 Pass Device in Liner Regulators

The pass device in a linear regulator is generally a transistor with a large size. This transistor must be able to handle the maximum load current without causing over temperature and reliability issues. To realize a low drop-out voltage at high current load, the conducting resistance of the pass transistor in linear region should be extremely low. Therefore, a very large transistor size is needed.

The pass transistor can either be a BJT or a MOSFET. Classical linear regulators such as LM78xx are using BJT based pass transistors. In state-of-the-art designs, MOSFETs are widely used because on-chip system integration (e.g. a mixed-signal system) can benefit from CMOS technology.

The pass device can be a n-type or p-type transistor. Generally, for the same size, the n-type transistor has a higher current conduction ability than the p-type one[4]. However, in order to easily achieve a low drop-out voltage regulation (as will be discussed in Section 1.4), p-type transistors are preferred in many regulator designs although they are with a lower current conduction ability.

1.4 Motivations

PMOS as the pass device is the most popular choice, owing to its gate voltage always lower than the supply rail. For NMOS as the pass device, the gate voltage is higher than supply if operating in low drop-out region. Therefore, an additional circuit such as a charge pump should be added which brings more design complexity. However, NMOS as the pass device has its advantages. First, it consumes smaller silicon area for the same maximum output current specification. Second, for a NMOS linear regulator, the transistor source node is directly connected to the regulator output node, which is actually a source follower with "local feedback" characteristic. This might provide a better dynamic performance in large signal domain.

The aim of this thesis is to investigate if NMOS linear regulator is able to achieve a comparable performance with its PMOS equivalent one (the equivalent PMOS linear regulator design is already available). Moreover, since the NMOS output stage may have a better dynamic performance, there might be a chance to reduce the load capacitance (2.2μF in the available PMOS linear regulator design).

[4]The hole movement involves in breaking and forming covalent bonding, while electrons are much freer to move, therefore electrons has a higher mobility

The drawback of NMOS linear regulator is also prominent. In low drop-out region, voltage boost techniques may introduce switched capacitor circuits. It will reduce the NMOS linear regulator area efficiency, generate ripples at the output and increase the power consumption.

The performance characteristics of the available PMOS linear regulator is summarized in Table 1.2. The NMOS linear regulator should be designed within these specifications while trying to minimize the silicon area and external output capacitance.

Table 1.2: Performance Characteristics of the PMOS Linear Regulator

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Regulator Input Voltage	5.5	-	40	V
V_{OUT}	Output Voltage	4.9	5.0	5.1	V
ΔV_{out_load}	Dynamic Load Regulation	-2	-	+2	%
$t_{stabilized}$	output voltage within 0.5% after load step	-	-	1	ms
ΔV_{out_line}	Dynamic Line Regulation	-2	-	+2	%
I_q	Quiescent Current(w/o band-gap)	-	10	-	μA
C_L	External Output Capacitor	-	2.2	-	μF

1.5 Organization of This Thesis

This thesis consists of six chapters. In Chapter 2, the PMOS and NMOS linear regulators are compared. The aim is to briefly introduce the linear regulator specifications with analysis of PMOS and NMOS as pass device respectively. This will build the foundation of the regulator design in this thesis.

In Chapter 3, the design of NMOS linear regulator is presented. First, small signal behavior of the main voltage feedback loop is accurately analyzed and modeled. Then, a compensation scheme which is able to add a zero without being troubled by its associated pole is proposed. After that, an adaptive biasing scheme is implemented to further increase the bandwidth of the main regulation loop. Finally, the over-current protection circuit design is discussed.

In Chapter 4, the performance evaluations based on detailed simulations of the designed NMOS linear regulator are presented.

Chapter 5 introduces scaling features of the designed NMOS regulator. In the first part, the external capacitor range of this linear regulator is discussed. The second part focuses on design recommendations for this linear regulator to adapt for different maximum load current specifications.

Finally, Chapter 6 presents conclusions of this thesis and gives suggestions for future works.

Chapter 2

Comparison of NMOS and PMOS Linear Regulators

In this Chapter, specifications of linear regulator will be discussed based on the comparison of PMOS and NMOS as the pass device. In the end, the AC characteristic of these two linear regulator topologies will be analyzed.

2.1 Basic Topology

Figure 2.1 shows the basic linear regulator topologies with PMOS and NMOS as the pass device respectively. The analysis of linear regulator specifications is based on this figure.

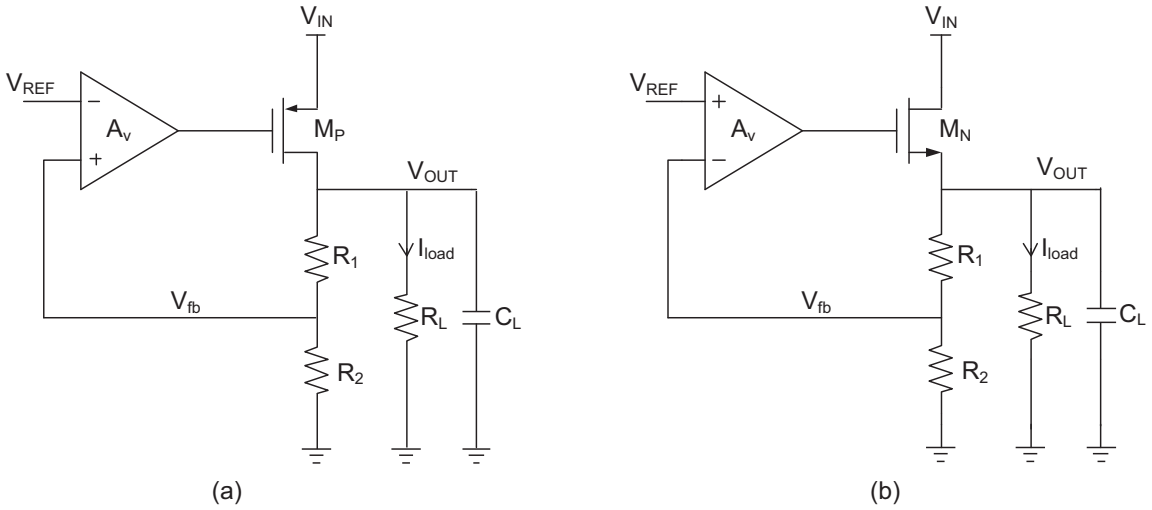

Figure 2.1: Basic linear regulator topology with (a) PMOS as pass device (b) NMOS as pass device.

2.2 Static State Specifications

2.2.1 Drop-out Voltage

The drop-out voltage is defined as the minimum voltage difference between V_{IN} and V_{OUT} (Figure 2.1) to maintain an intended voltage regulation [4]. A linear regulator which can operate in low drop-out voltage regulation is commonly named as low drop-out regulator (LDO). There is no universal agreement on how much drop-out voltage makes one voltage regulator a "LDO". Literature [5] defines a regulator with a drop-out voltage below 600mV in battery-operated environments is a LDO. In state-of-the-art design, the drop-out voltages are normally in the range of 200∼500mV.

2.2.2 Quiescent Current

The quiescent current[1] (I_q) is defined as the current consumed by the linear regulator control circuits. The power efficiency η of a linear regulator can be expressed in Equation 2.1, where I_{load} is current flowing into the load, $V_{drop-out}$ is the drop-out voltage.

$$\eta = \frac{E_{deliverd}}{E_{supplied}} = \frac{V_{OUT}I_{load}}{V_{IN}(I_{load}+I_q)} = (1 - \frac{V_{drop-out}}{V_{IN}})\frac{I_{load}}{I_{load}+I_q} \tag{2.1}$$

Both reducing $V_{drop-out}$ and I_q will increase the efficiency. The linear regulator efficiency is changing over I_{load} variation. As I_{load} is much larger than I_q, the $I_{load}/(I_{load}+I_q)$ term[2] approximately equals to 1, the dominate factor affecting power efficiency is $V_{drop-out}$.

2.2.3 Line Regulation

Line regulation represents the ability of a regulator to withstand static variations from its supply. It is defined as a gain between regulated output and input supply $\Delta V_{OUT}/\Delta V_{IN}$. The static supply voltage variation might be caused by the battery voltage reduction during one discharge cycle. Figure 2.2 shows an estimated lead-acid battery discharge curve and its regulated output.

Ideally, the regulated voltage should be fixed until the regulation losing its effectiveness. However, due to the finite loop gain, the output voltage actually varies with supply voltage. It should be noted that even line regulation is a DC specification, it would be easier to analyze it in small signal domain. The analysis starts from the PMOS regulator shown in Figure 2.1(a), suppose the transconductance of M_P is g_{mp}, its output resistance is $r_{o,p}$, A_v is the open-loop gain of the amplifier. Now assume a small variation happens at the V_{IN} node by ΔV_{IN}, the V_{OUT} node should have a correspondent voltage variation by ΔV_{OUT}. The equation can be set up as:

[1] Also named as ground current I_{gnd}

[2] Which is the current efficiency

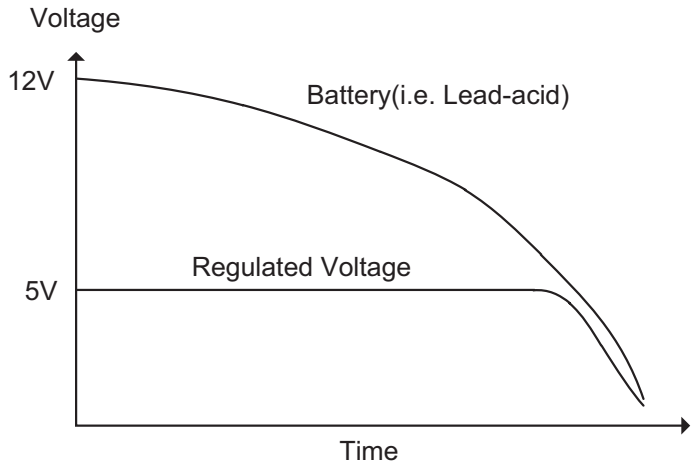

Figure 2.2: Lead-acid discharge curves under a constant load current.

$$(\Delta V_{IN} - \Delta V_{OUT}\frac{R_2}{R_1+R_2}A_v)g_{mp}[(R_1+R_2)||R_L||r_{o,p}] = \Delta V_{OUT} \tag{2.2}$$

Normally, the term $g_{mp}[(R_1+R_2)||R_L||r_{o,p}]$ can be much greater than 1 in most cases, Equation 2.2 can be simplified as:

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} = \frac{g_{mp}[(R_1+R_2)||R_L||r_{o,p}]}{1+g_{mp}[(R_1+R_2)||R_L||r_{o,p}]A_v\frac{R_2}{R_1+R_2}} \approx \frac{1}{A_v\frac{R_2}{R_1+R_2}} \tag{2.3}$$

From Equation 2.3, it shows that increasing A_v will improve the line regulation.

The line regulation analysis of NMOS regulator is based on Figure 2.1(b). Again, the transconductance of M_N is g_{mn}, the output resistance is $r_{o,n}$, A_v is the open loop gain of the amplifier. The Equation of ΔV_{IN} variation on ΔV_{OUT} is:

$$[(-\Delta V_{OUT}\frac{R_2}{R_1+R_2}A_v - \Delta V_{OUT})g_{mn} + \frac{\Delta V_{IN}-\Delta V_{OUT}}{r_{o,n}}][(R_1+R_2)||R_L] = \Delta V_{OUT} \tag{2.4}$$

The line regulation of the NMOS regulator can be expressed as:

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} = \frac{1}{(1+\frac{R_2}{R_1+R_2}A_v)g_{mn}r_{o,n} + \frac{r_{o,n}}{(R_1+R_2)||R_L} + 1} \tag{2.5}$$

It is interesting to notice that the term $\frac{r_{o,n}}{(R_1+R_2)||R_L}$ is a number which is much smaller than $(1+\frac{R_2}{R_1+R_2}A_v)g_{mn}r_{o,n}$. It can be proved as follows:

$$\frac{r_{o,n}}{(R_1+R_2)||R_L} = \frac{\frac{1}{\lambda I_{load}}}{\frac{V_{OUT}}{I_{load}}} = \frac{1}{\lambda V_{OUT}} \tag{2.6}$$

For common analog process (e.g. 0.5μm gate length), the channel length modulation factor λ is around 0.1 [6]. Therefore, according to Equation 2.6, the term $\frac{r_{o,n}}{(R_1+R_2)||R_L}$ is much smaller than $(1+\frac{R_2}{R_1+R_2}A_v)g_{mn}r_{o,n}$, for the latter one is almost a multiplication of A_v and intrinsic NMOS transistor gain $g_{mn}r_{o,n}$.

Then, Equation 2.5 can be simplified as:

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} \approx \frac{1}{\frac{R_2}{R_1+R_2}A_v g_{mn} r_{o,n}} \tag{2.7}$$

From Equation 2.7, the line regulation for NMOS regulator is related to A_v and the NMOS transistor intrinsic gain $g_{mn}r_{o,n}$. Compared with PMOS regulator line regulation result (Equation 2.3), the NMOS regulator has an improved line regulation by $g_{mn}r_{o,n}$. This result makes sense because the NMOS pass device is acting as a "cascode" transistor between V_{IN} and V_{OUT}. If a variation adds on the drain node of a regulated NMOS transistor, its equivalent variation on the source node should be attenuated by the transistor intrinsic gain and the amplifier open-loop gain A_v.

2.2.4 Load Regulation

The load regulation is defined as the static output voltage variation (ΔV_{OUT}) in response to static load current changes (ΔI_{OUT}). The PMOS load regulation analysis is based on Figure 2.1(a). Again, the small signal analysis is used, A_v is the amplifier open-loop gain, g_{mp} is the transconductance of PMOS, I_{load} is the current load flow through R_L (assume R_1 and R_2 are much larger than R_L). The relation between the output voltage variation and load current is:

$$-\Delta V_{OUT}\frac{R_2}{R_1+R_2}A_v g_{mp} = \Delta I_{load} \tag{2.8}$$

Therefore, the $\Delta V_{OUT}/\Delta I_{load}$ is:

$$\frac{\Delta V_{OUT}}{\Delta I_{load}} = -\frac{1}{\frac{R_2}{R_1+R_2}A_v g_{mp}} \tag{2.9}$$

From Equation 2.9, the load regulation ability is determined by A_v and g_{mp}.

The NMOS regulator load regulation analysis is based on Figure 2.1(b). Again, A_v is the amplifier open-loop gain, g_{mn} is the NMOS transconductance, I_{load} is the current load flow through R_L. The transfer function of load current variation on output voltage is:

$$(-\Delta V_{OUT}\frac{R_2}{R_1+R_2}A_v - \Delta V_{OUT})g_{mn} = \Delta I_{load} \tag{2.10}$$

The expression of $\Delta V_{OUT}/\Delta I_{load}$ is:

$$\frac{\Delta V_{OUT}}{\Delta I_{load}} = -\frac{1}{(\frac{R_2}{R_1+R_2}A_v + 1)g_{mn}} \approx -\frac{1}{\frac{R_2}{R_1+R_2}A_v g_{mn}} \tag{2.11}$$

It is found that for the NMOS regulator, the load regulation is also dependent on A_v and g_{mn}.

2.2.5 Temperature Drift

The temperature variation also affects the linear regulator output voltage accuracy. Linear regulator temperature coefficient (TC) is defined as the percentage of output voltage variation in response to temperature change [5], which has a unit of %/℃. It can be expressed as:

$$TC = \frac{1}{V_{OUT}}\frac{\Delta V_{OUT}}{\Delta T} = \frac{(\Delta V_{REF} + \Delta V_{OS})(\frac{V_{OUT}}{V_{REF}})}{V_{OUT}\Delta T} = \frac{\Delta V_{REF} + \Delta V_{OS}}{V_{REF}\Delta T} \tag{2.12}$$

ΔT represents the temperature changes, ΔV_{REF} and ΔV_{OS} are reference voltage and input equivalent offset variation according to temperate change. From Equation 2.12, the temperature impaction on output voltage is directly dependent on the temperate coefficient of reference voltage ($\Delta V_{REF}/\Delta T$) and the temperate coefficient of input equivalent offset voltage ($\Delta V_{OS}/\Delta T$).

2.3 Dynamic State Specifications

The abilities of linear regulator in response to supply voltage and load current transient variation are two major dynamic state specifications. The output voltage spike and recovery time affect the regulator output accuracy, which degenerates the quality of output voltage. Good transient response with small output voltage variation including overshoots and undershoots is critical to prevent an accidental turn off or resetting of the load device [7]. The output voltage spike is in large signal domain, where slewing and non-linear behavior happen. Therefore, it is difficult to accurately define the spike voltage and recovery time.

In this section, the transient behavior is divided into a few time periods. It is possible to qualitatively analyze the transient behavior at each time period. A comparison of linear regulators with infinite and finite bandwidth is analyzed based on Figure 2.3.

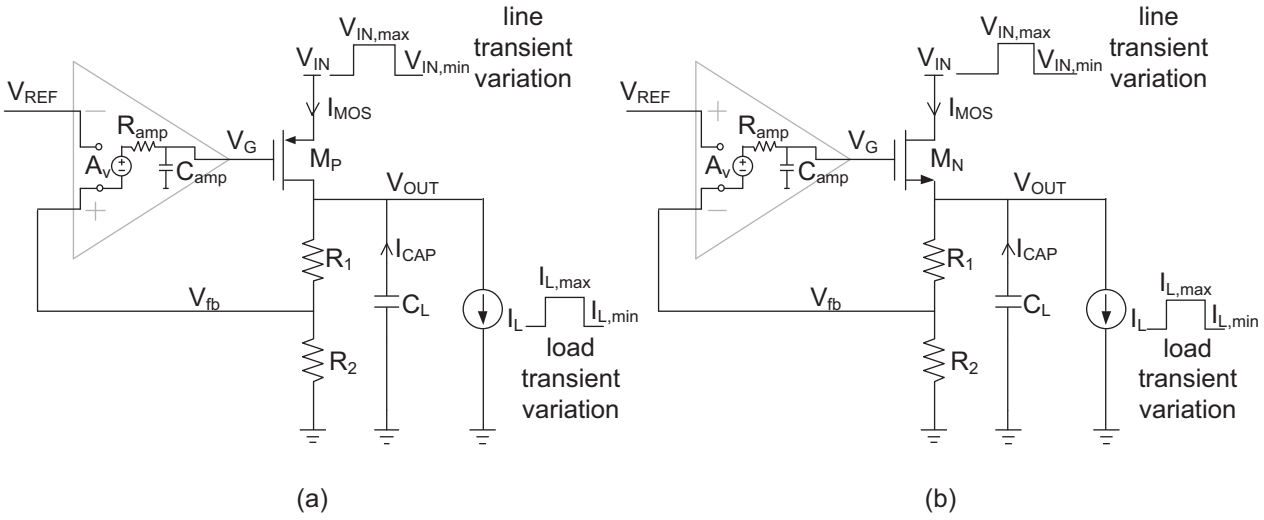

Figure 2.3: Transient response of (a) PMOS regulator (b) NMOS regulator.

2.3.1 Line Transient Response

Line transient response is the output voltage transient variation (V_{OUT} in Figure 2.3) in response to the supply voltage (V_{IN}) suddenly changes. In automotive environment, the supply voltage variation can be caused by car cranking[3], electromagnetic inferences, noise, etc.

In this subsection, the line transient response of PMOS and NMOS regulator will be discussed separately. A possible line transient response of PMOS regulator is shown in Figure 2.4, where (a) is a feedback loop with infinite bandwidth, (b) is with finite bandwidth. In (a), as the supply voltage V_{IN} suddenly jumps up and down, the gate voltage V_G immediately follows the V_{IN}, which makes V_{OUT}, I_{MOS}, I_{CAP} unchanged.

In (b), limited bandwidth will make V_{OUT} vary with V_{IN}. The transient behavior can be divided into the following $t_1 - t_9$ time periods:

At t_1, the V_{IN} and V_G are kept at their nominal value. It should be noted that at this time I_{MOS} is at medium current load, which makes the regulator able to adjust output current up and down[4].

At t_2, V_{IN} suddenly goes up. Due to the limited bandwidth, V_G begins to slew, V_{SG} is larger than t_1. The increased I_{MOS} current flows into the load capacitor C_L, which leads to an increased V_{OUT}.

At t_3, the slew period ends. Both I_{MOS} and I_{CAP} excursions (compare to their nominal value at t_1) are reducing. The regulation loop begins to take control of V_{OUT}.

At t_4, the regulation loop controls V_{OUT} back to its nominal value. The curve is sort of RC discharging, the time constant is related to the loop bandwidth.

At t_5, V_G reaches its maximum. The V_{SG} is the same with t_1.

[3]Cranking is referred to as the voltage drop of the car battery during engine starting

[4]If I_{MOS} is in its minimum, V_{OUT} can be at a voltage higher than nominal for a while since the regulator has only source ability and no sink capability to its load

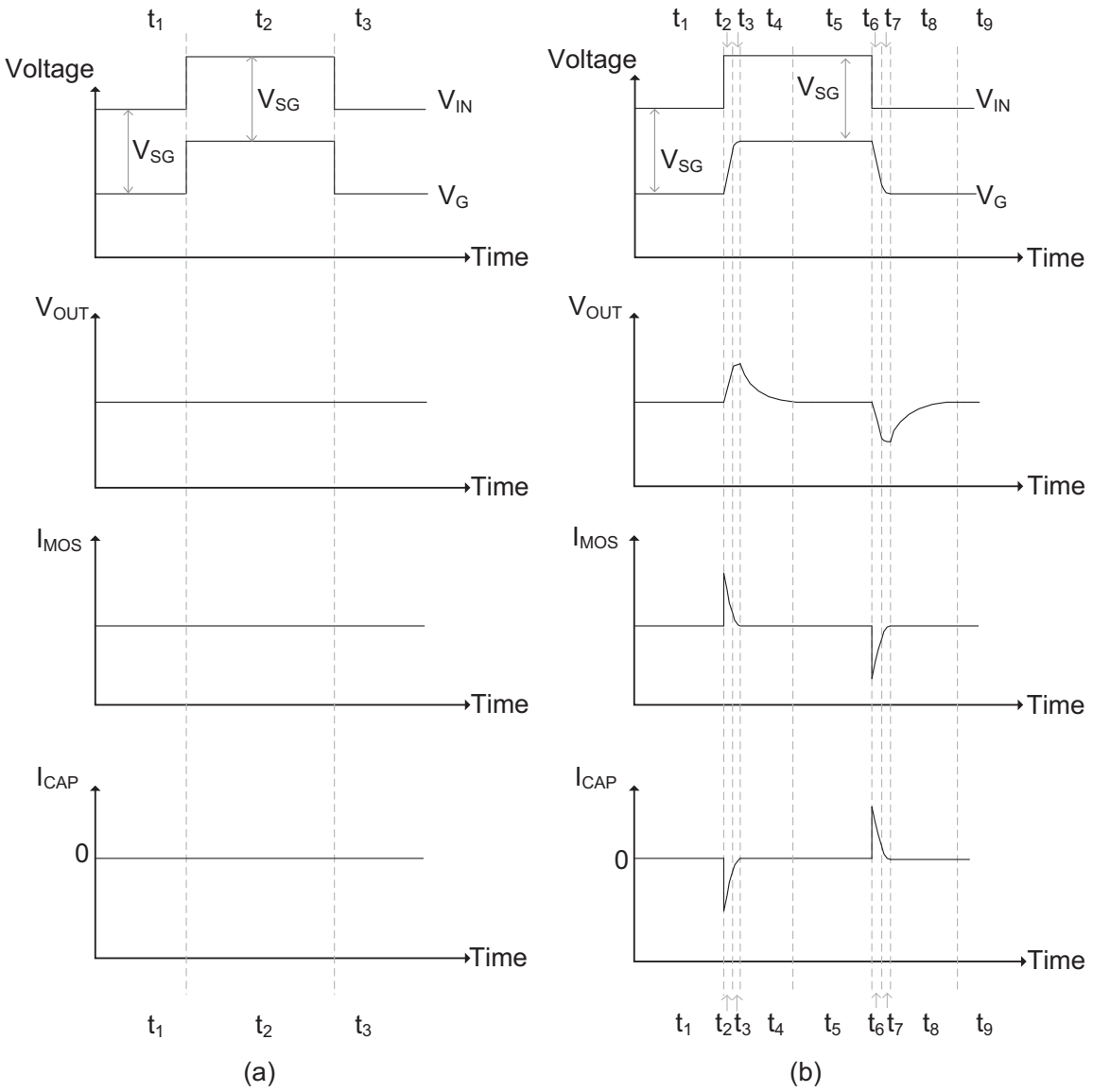

Figure 2.4: One possible PMOS linear regulator line transient response (a) with infinite bandwidth (b) with finite bandwidth.

At t_6, V_{IN} suddenly rolls down. Again, V_G starts to slew. I_{MOS} suddenly reduces, I_{CAP} is providing current to compensate the current difference (I_{MOS}+I_{CAP}=I_L, assume I_L is constant during line transient).

At t_7, the slew period ends, V_{OUT} is gradually controlled by the feedback loop. Both I_{MOS} and I_{CAP} excursions (compare to their nominal value at t_1) are reducing. At the end of t_7, V_{OUT} reaches its minimum value.

At t_8, the feedback loop fully takes over the control of V_{OUT}. V_{OUT} is back to its nominal value like a RC curve. The time constant of the RC curve is related to the loop bandwidth.

At t_9, the line transient is over, the status is the same with t_1.

The line transient response of NMOS linear regulator is shown in Figure 2.5, where (a) is with infinite bandwidth, (b) is with finite bandwidth. For the infinite bandwidth case, no matter how the supply voltage V_{IN} varies, the V_{OUT} is kept at its nominal value. The finite bandwidth transient behavior is divided into $t_1 - t_9$ time periods. Each period will be discussed as follows:

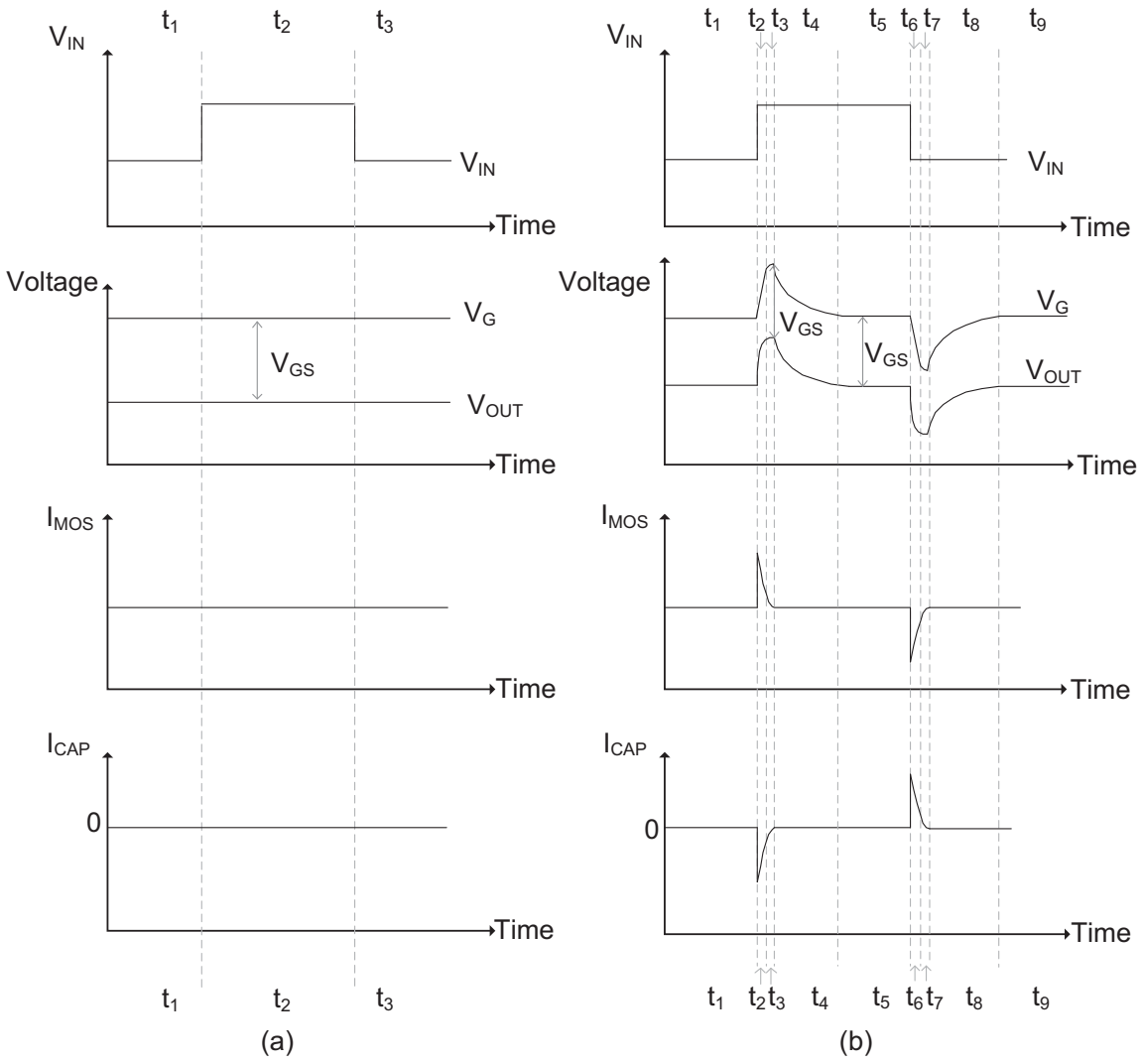

Figure 2.5: One possible NMOS linear regulator line transient response (a) with infinite bandwidth (b) with finite bandwidth.

At t_1, V_{IN} and V_{OUT} are at their nominal value. Again, I_{MOS} is assumed to be providing medium current load.

At t_2, V_{IN} suddenly goes up. Due to channel length modulation, I_{MOS} starts to provide additional current. This current is directly charged into C_L (assume I_L is constant), which makes V_{OUT} suddenly increase. V_G starts to slew to follow the fast V_{OUT} variation.

At t_3, V_G is controlled by the feedback loop. I_{MOS} and I_{CAP} excursions (compare to their nominal value at t_1) reduce. At the end of t_3, the V_{GS} is adjusted to its nominal value (the same with t_1), and V_{OUT} is at its maximum value.

At t_4, the regulation loop fully takes over and regulates V_{OUT} back to its nominal value.

At t_5, all the voltages are at their nominal value.

At t_6, V_{IN} suddenly rolls down. Again, I_{MOS} is reducing owing to channel length modulation, V_{OUT} immediately decreases. The current difference between I_L and I_{MOS} is compensated by I_{CAP}. The fast V_{OUT} rolling down causes V_G starting to slew.

At t_7, V_{GS} is near its nominal value. I_{MOS} and I_{CAP} excursions (compare to their nominal value at t_1) is decreasing. By the end of t_7, the V_{OUT} is at its minimum.

At t_8, the feedback loop fully takes over and regulates V_{OUT} back to its nominal value.

At t_9, the line transient is over, the status is the same with t_1.

2.3.2 Load Transient Response

Load transient response is defined as the linear regulator's ability to regulate the output voltage during fast load transients [8]. In practical cases, the circuit loaded by a linear regulator can be dynamic (e.g. a micro-controller operating at several tens of MHz), the load current variation is fast and unpredictable. The output voltage changes in response to maximum load current variation at given period of time should be defined for a linear regulator. In this subsection, the load transient behavior will be analyzed in detail.

One possible load transient waveform of a PMOS linear regulator is shown in Figure 2.6, where (a) is with infinite bandwidth. During load transient variation, I_L is provided by the power transistor current I_{MOS}. The output voltage V_{OUT} is unchanged. (b) is with finite bandwidth, its transient behavior is divided into a few time periods, the analysis is as follows:

At t_1, I_L and V_{SG} are at their nominal value.

At t_2, I_L rises up immediately. Due to the loop delay, the major current for I_L variation is provided by I_{CAP}. Charge flowing out of C_L causes V_{OUT} decease. Since I_L rising edge can be very fast (e.g. 60mA/μS), the fast variation which beyond the loop bandwidth makes V_G slewing.

At t_3, I_{MOS} becomes the dominate source providing the load current I_L. The feedback loop gradually controls V_{OUT} (slew period ends). For I_{CAP} is reducing, the speed of V_{OUT} rolling down is reduced in comparison with time period t_2.

At the beginning of t_4, I_{MOS}=I_L, $I_{CAP} = 0$. V_{OUT} reaches its minimum value. Then the loop begins to regulate V_{OUT} back to its nominal value. The discharge curve can be roughly modeled as a RC curve.

At t_5, V_{OUT} is back to its nominal value, V_{SG} is at its maximum which provides the maximum load current $I_{L,max}$.

At the beginning of t_6, I_L goes down from $I_{L,max}$ to $I_{L,min}$. Again, this current variation is mainly provided by I_{CAP}. The fast V_{OUT} variation causes slewing on V_G.

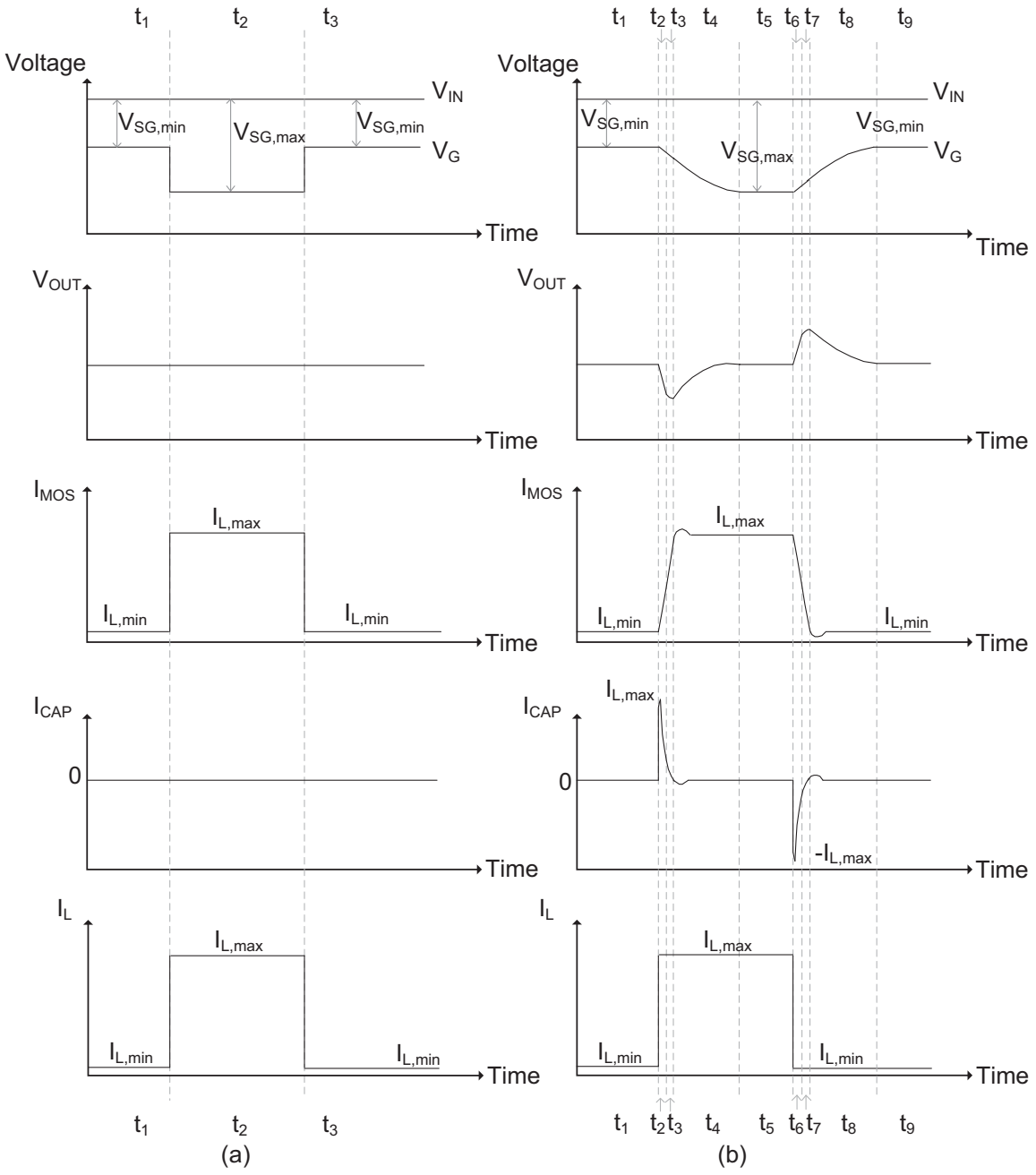

Figure 2.6: One possible PMOS linear regulator load transient response (a) with infinite bandwidth (b) with finite bandwidth.

At t_7, I_{CAP} excursions is decreasing. The feedback loop takes the control of V_{OUT}. Finally, I_{CAP}=0, and V_{OUT} reaches its maximum.

At t_8, the loop fully takes over the control and V_G is increasing as a RC curve.

At t_9, the load transient is over, the status is the same with t_1.

One possible NMOS linear regulator load transient response is shown in Figure 2.7, where (a) is with infinite bandwidth. As the load current suddenly varies from $I_{L,min}$ to $I_{L,max}$, the gate voltage V_G is fast enough to directly rise up to the expected $V_{GS,max}$. In the whole process, the output voltage V_{OUT} is unchanged. (b) is with finite bandwidth, the waveform is analyzed based on the divided a few time periods.

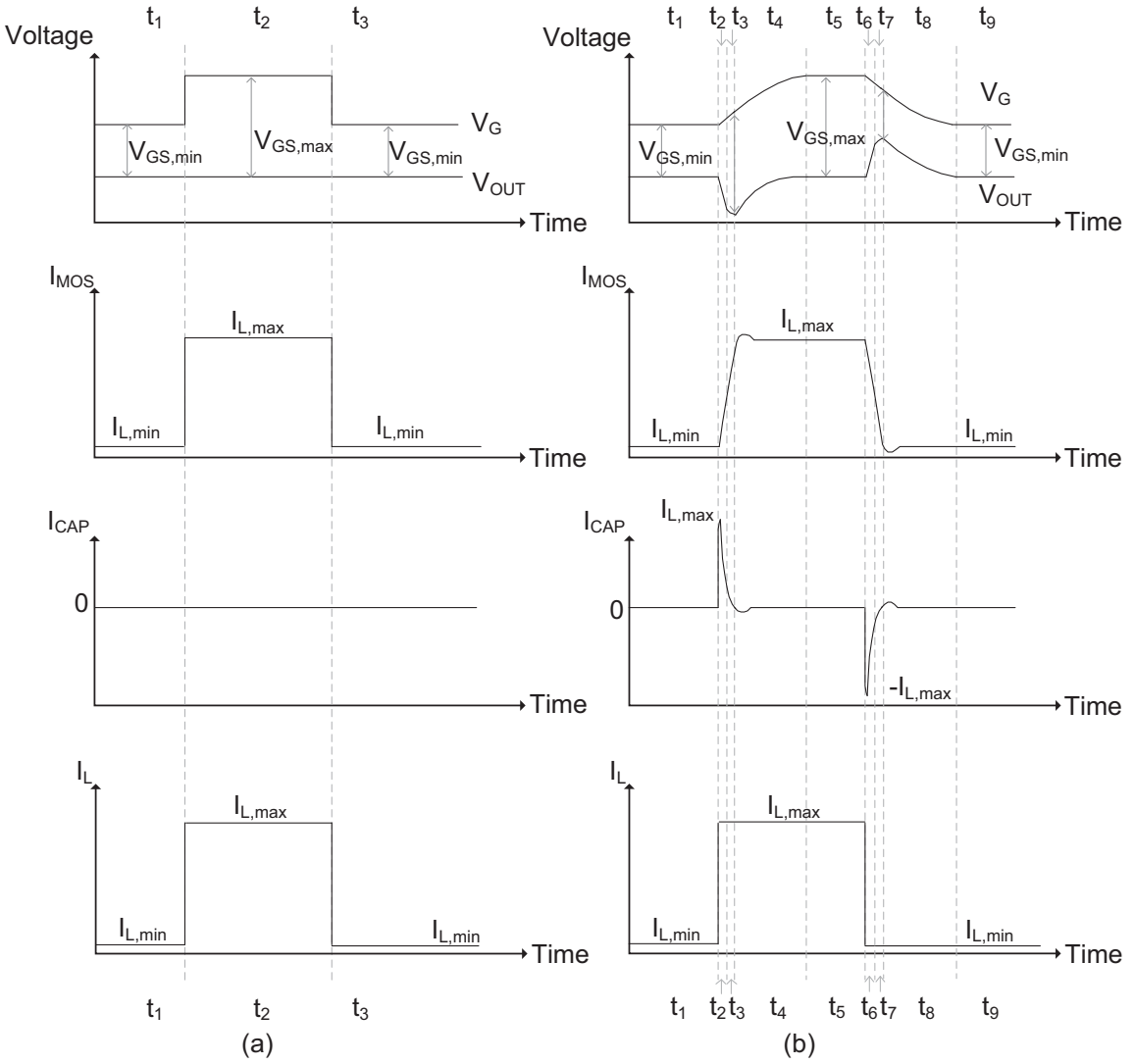

Figure 2.7: One possible NMOS linear regulator load transient response (a) with infinite bandwidth (b) with finite bandwidth.

At t_1, I_L and V_{OUT} are at their nominal value.

At the beginning of t_2, I_L suddenly increases to $I_{L,max}$. The majority of current I_L is provided by I_{CAP}. Charges flowing out of C_L will make V_{OUT} roll down at very fast speed. The decreasing V_{OUT} will feedback to the input of the amplifier. If the V_{OUT} variation speed is beyond bandwidth, it will cause V_G slewing.

At t_3, V_{GS} is becoming larger and I_{MOS} is the dominate source providing $I_{L,max}$. For I_{CAP} excursion is reduced, the V_{OUT} rolling down speed is slower than t_2 period. At the end of period t_3, the I_{MOS} equals to $I_{L,max}$, V_{GS} reaches $V_{GS,max}$, I_{CAP}=0. V_{OUT} is at its minimum value.

At t_4, the feedback loop takes over the control of V_{OUT}. The V_{OUT} rising curve can be treated as RC charging.

At t_5, V_{OUT} is at the nominal value, I_{MOS} and V_{GS} are at their maximum.

At t_6, the load current is rolling down from $I_{L,max}$ to $I_{L,min}$. At the very beginning of t_6, due to bandwidth limitation V_{GS} is still around $V_{GS,max}$. The current difference between I_{MOS} and I_L will be provided by I_{CAP}, which is a current flowing into the capacitor. V_{OUT} is rising up at a very fast speed, which makes V_G slewing down.

At t_7, I_{MOS} is reducing, the loop gradually takes over the control of V_{OUT}. The amount of I_{CAP} is decreasing as the difference between I_{MOS} and I_L are becoming smaller and smaller. V_{OUT} is increasing at a slower speed in comparison with t_6 period.

At the beginning of t_8, I_{MOS}=I_L, I_{CAP}=0, V_{OUT} is at its peak value. The regulation loop fully takes over the control of V_{OUT}. V_{OUT} goes back to its nominal value by a RC discharging curve.

At t_9, the load transient is over, the status is the same with t_1.

2.4 High Frequency Specifications

2.4.1 Power Supply Rejection Ratio

The power supply rejection of a linear regulator can be defined as the ability to maintain a constant voltage V_{OUT} in the presence of noisy V_{IN} [9]. Figure 2.8(a) shows a linear regulator attenuating the supply noise appearing at the regulated output.

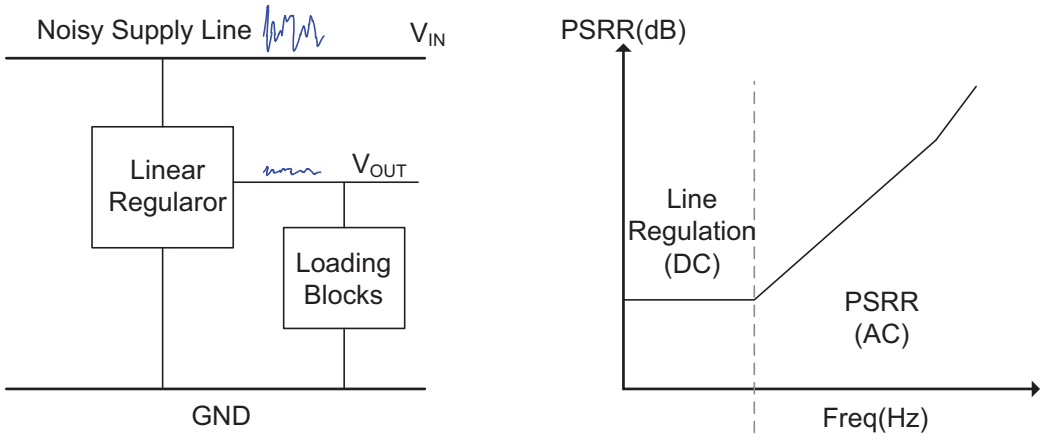

Figure 2.8: (a) Power supply rejection on linear regulator (b) typical bode plot of PSRR.

In comparison with the line regulation ability as discussed in Section 2.2, power

supply rejection ratio (PSRR) is in AC domain. Therefore, the small signal analysis should be used. The PSRR is defined as:

$$PSRR = |20log_{10}(\frac{V_{OUT}}{V_{IN}})| \tag{2.13}$$

A typical bode plot of PSRR is shown in Figure 2.8(b). In low frequency range, the supply variation can be treated as a DC component, which is actually the line regulation discussed in Section 2.2.3. As frequency increases, more noise or ripple from the supply line will show up at the output of the regulator. This is mainly caused by both the feedback loop gain rolling down and capacitors inside the linear regulator which provides AC signal paths conducting between supply and output.

For PMOS linear regulators, the noise on the power supply line directly shows at the source of the PMOS power transistor. High PSRR performance can be achieved by making the gate node have the same variation with source node. Therefore, the V_{SG} is unchanged. For NMOS linear regulator design, the signal conducting path from the power supply to the power transistor gate should be minimized. In this way, the V_{GS} of NMOS power transistor is not affected by the noisy power supply.

2.4.2 Output Noise

The output noise is an important specification when the linear regulator is loading a noise sensitive Analog/RF block, for example a high quality audio circuit or a RF transceiver. The noise coming from the linear regulator will degrade the loading circuit performance. The noise of a linear regulator consists of three main parts: band-gap reference noise, feedback elements noise, linear regulator circuit noise.

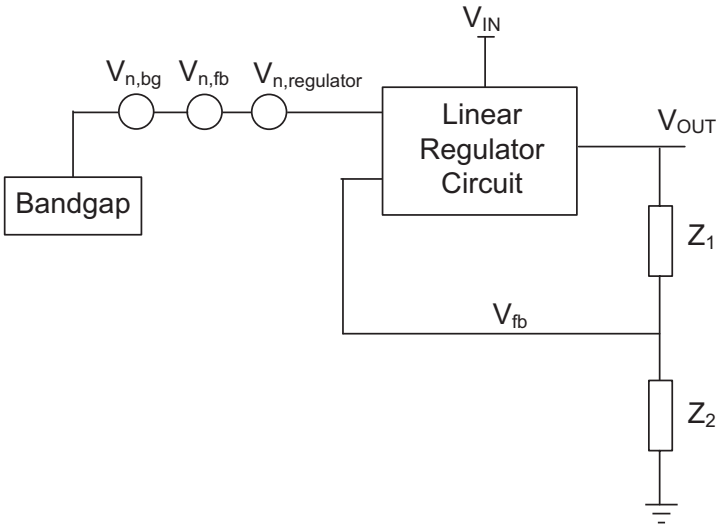

Figure 2.9: Equivalent input noise of linear regulator.

The equivalent input noise source is shown in Figure 2.9, where $V_{n,bg}$ is the equivalent output noise from band-gap, $V_{n,fb}$ is the equivalent noise source from feedback

elements, $V_{n,LDO}$ is the equivalent input noise from the linear regulator. The $V_{n,bg}$ and $V_{n,LDO}$ depend on the circuit implementation of band-gap and linear regulator respectively. If the feedback elements are all resistors, this voltage to voltage feedback topology in Figure 2.9 has an equivalent thermal noise source contributed by R_1 and R_2 in parallel [10], which is $V_{n,fb}^2$=4KT($R_1 \| R_2$).

2.4.3 Electromagnetic Interference

The electromagnetic interference (EMI) of a linear regulator can be defined as the electromagnetic emissions from the regulator to the main power distribution system [11]. An EMI disturbance example in an automotive environment is illustrated in Figure 2.10.

Generally, if the pass transistor operates in the saturation region, the PMOS linear regulator has a better EMI performance, for the reason that the voltage variance at the regulator output node showing at the power supply line is attenuated by the output impedance of the PMOS transistor. While for NMOS pass device, at high load current, the impedance seen from the output node to the supply line may be smaller than the PMOS output impedance, which may lead to worse EMI performance. It should be noted that if the pass transistor operates in the linear region, the EMI performance of NMOS and PMOS regulators should be identical, because the pass transistor is simply equivalent to a resistor.

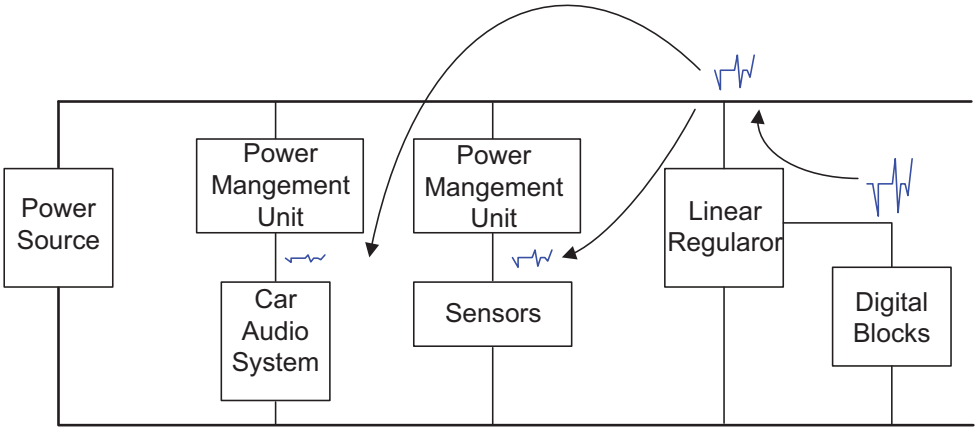

Figure 2.10: EMI example in automotive environment.

2.5 Frequency Behavior

A linear regulator is a negative feedback system. Therefore, its frequency behavior determines the loop response time, which is strongly linked to dynamic specifications such as line and load response of the regulator. A critical issue for a feedback system is stability. Frequency behavior difference between PMOS and NMOS regulators affects the frequency compensation choice. Simple second-order linear regulator

topologies are shown in Figure 2.11. It must be noted that Figure 2.11 only represents conventional linear regulators with relatively large C_L[5]. The aim of this section is to illustrate internal pole P_1 and output pole P_2 movement at low/full current load scenario.

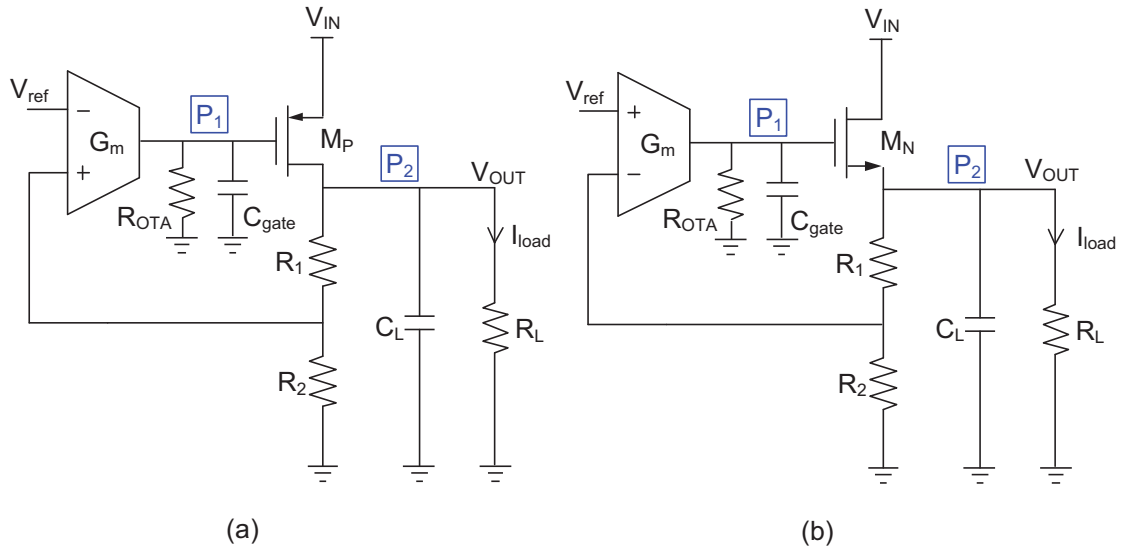

Figure 2.11: A simple topology of (a) PMOS regulator (b) NMOS regulator.

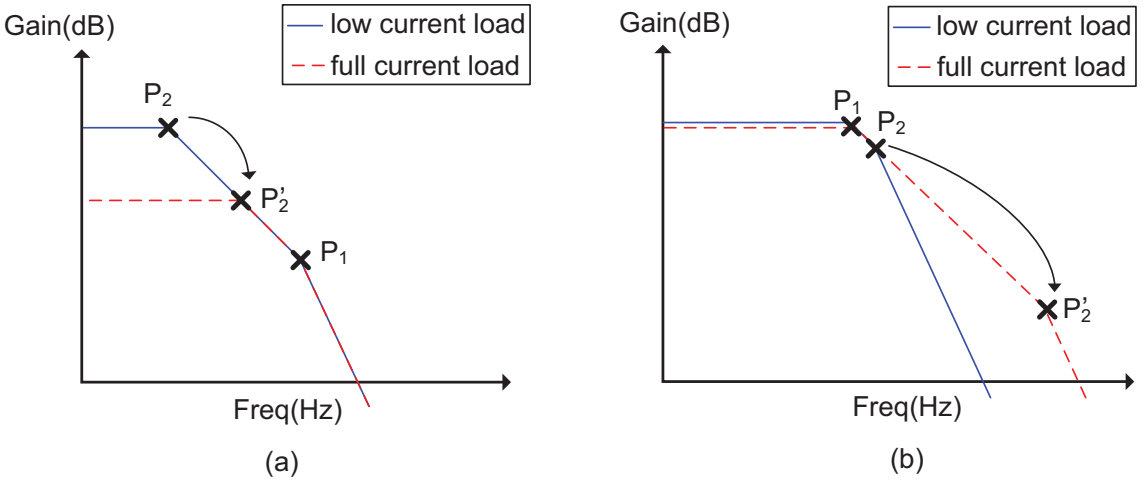

Figure 2.12: Bode plot of (a) PMOS regulator (b) NMOS regulator.

For PMOS linear regulator shown in Figure 2.11(a), the second-order system consists of two poles P_1 and P_2. A possible open-loop bode plot at low load current

[5]For some linear regulators, the output capacitive load is very small, therefore their frequency behavior can not be represented by Figure 2.12.

scenario is shown by the solid line in Figure 2.12(a). Roughly speaking, P_1 is generated by M_P gate capacitance C_{gate} and the G_m stage output resistance R_{OTA}, which locates at:

$$f_{P1} = -\frac{1}{2\pi R_{OTA} C_{gate}} \tag{2.14}$$

P_2 is generated by the output capacitor C_L and regulator load resistance R_L, which locates at:

$$f_{P2} = -\frac{1}{2\pi R_L C_L} = -\frac{I_{load}}{2\pi V_{out} C_L} \tag{2.15}$$

It is clear that as the load current I_{load} increases, P_2 linearly goes to the higher frequency. The open-loop gain (neglecting the feedback factor) of the PMOS linear regulator is mainly the multiplication of gain of G_m stage and gain of power transistor, which is:

$$A_v = G_m R_{OTA} g_{mp} r_o \tag{2.16}$$

g_{mp} is the transconductance of PMOS power transistor, β is the current factor which equals to $\mu_p C_{ox} W/L$. Substituting with $g_{mp} = \sqrt{2\beta I_{load}}$ and $r_o \approx 1/(\lambda I_{load})$, Equation 2.16 can be rewritten as:

$$A_v = \frac{G_m R_{OTA} \sqrt{2\beta}}{\lambda} \frac{1}{\sqrt{I_{load}}} \tag{2.17}$$

Suppose G_m and R_{OTA} are unchanged during load current variation, β and λ are determined by process and transistor size, the open-loop gain is inversely proportional to square root of loading current I_{load}. As I_{load} goes up, the open-loop gain reduces.

A possible second-order NMOS linear regulator topology is shown in Figure 2.11(b). Again, if C_L is in a large value, the possible open-loop bode plot at low load current scenario is shown by the solid line in Figure 2.12(b). P_1 is at the output of OTA which locates at:

$$f_{P1} = -\frac{1}{2\pi R_{OTA} C_{gate}} \tag{2.18}$$

P_2 is at the output of linear regulator, the output resistance of this node is roughly $1/g_{mn}$(assume $(1/g_{mn}) \ll R_L \| (R_1+R_2)$), where g_{mn} is the transconductance of NMOS power transistor. The frequency of P_2 can be expressed as:

$$f_{P2} = -\frac{g_{mn}}{2\pi C_L} = -\frac{\sqrt{2\beta I_{load}}}{2\pi C_L} \tag{2.19}$$

From Equation 2.19, P_2 is proportional to the square root of load current. As the load current increases, P_2 goes to the higher frequency.

The open-loop gain of NMOS linear regulator is composed by the gain from OTA and the gain of NMOS power transistor. Assume $R_L \ll R_1+R_2$, it can be written as:

$$A_v = G_m R_{OTA} \frac{g_{mn} R_L}{1 + g_{mn} R_L} \tag{2.20}$$

If $g_{mn}R_L \gg 1$, then $A_v \approx G_m R_{OTA}$. The $g_{mn}R_L$ relation can be expressed as:

$$g_{mn} R_L = \sqrt{2\beta I_{load}} \frac{V_{out}}{I_{load}} = \frac{\sqrt{2\beta} V_{out}}{\sqrt{I_{load}}} \tag{2.21}$$

Normally, if I_{load} in hundreds of mA current range, $g_{mn}R_L$ could be a term alway larger than 1. For example, V_{out}=5V, $I_{load,max}$=120mA, β ≈1.7, the minimum $g_{mn}R_L \approx 27$, which makes the gain of the NMOS source follower roughly equals to 1. It should be mentioned that from Equation 2.21, as I_{load} increases, $g_{mn}R_L$ reduces, which makes overall open-loop gain A_v also reduce. However, since $g_{mn}R_L$ is normally the dominate term at both numerator and denominator in Equation 2.20, the gain reduction due to output current increase is negligible.

It is obvious that both the PMOS and NMOS linear regulator in Figure 2.12 are unstable feedback systems. Therefore, compensation techniques should be applied. The movement of P_2 according to different load current adds difficulty for compensation, for the reason that the compensation scheme should be effective among P_2 movement range. Based on Equation 2.15 and Equation 2.19, Figure 2.13 is plotted to show the frequency range that P_2 moves over the loading current from 10μA to 120mA for PMOS and NMOS regulators respectively. Assume β=1.7, λ=0.2, C_L=220nF, it can be seen that for PMOS regulator, P_2 starts at 1Hz and ends around 10kHz. While for NMOS regulator, P_2 starts at 5KHz and ends at 500kHz approximately.

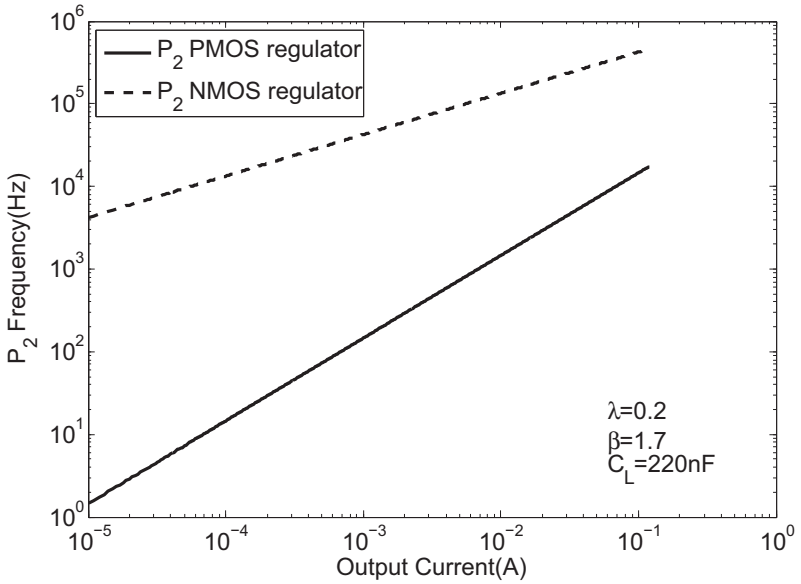

Figure 2.13: P_2 movement over load current.

It can be concluded that the P_2 movement range for NMOS linear regulator is much wider than the PMOS one. For PMOS linear regulators, the P_2 movement can be controlled within the bandwidth (e.g. keep the bandwidth greater than 10kHz),

therefore the number of poles and zeros within bandwidth can be unchanged during load current variation, which may provide better chance for compensation. While for NMOS linear regulators, wide P_2 movement may go out of the bandwidth, which adds more complexity for compensation.

Chapter 3

Design of NMOS Linear Voltage Regulator

3.1 Pass Device Characteristic and Sizing

Before really entering into the design phase of the NMOS linear regulator, both pass transistor characteristic and its sizing should be known. As stated in Section 1.4, the maximum supply voltage is 40V, therefore a power transistor with a high breakdown voltage should be used. A double diffused n-type MOSFET in advanced BCD technology [12] is shown in Figure 3.1, the source of the transistor is implanted in a p-well. The n-well is acting as the drift region. p-well and n-well are forming a PN diode which is the body diode. The transistor is based on silicon on insulator (SOI) technology. The buried oxide is used to isolate the substrate.

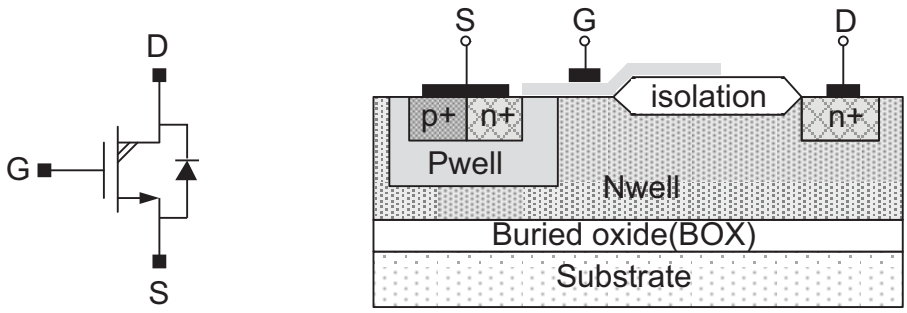

Figure 3.1: Power MOS symbol and the cross section view.

The minimum width to length ratio of the power transistor needs to be determined. The pass transistor should work in saturation region and linear region. In saturation region, the drain current I_D and V_{GS} relation is quadratic, while in linear region this relation is linear. For the same V_{GS} range, the current conduction ability bottleneck is in linear region. Therefore, the power transistor minimum width to length ratio can be found by measuring the linear region drain-source resistance R_{DS}. In this design, the expected R_{DS} is 0.5V/120mA$\approx$4.17Ω.

Practically, the minimum width to length ratio should be enlarged to compensate non-idealities such as bond wire resistance, transistor mismatch, etc. Moreover, the heat density should also be taken into account before finally deciding the area of the transistor. Finally, a NMOS power transistor with an area three times smaller than the PMOS power transistor (used in the available PMOS linear regulator) is chosen in this design.

3.2 NMOS Linear Regulator Topology

From top level point of view, if starting from a PMOS linear regulator topology to design its NMOS equivalent, an analog level shifter block should be added to level up the gate voltage as shown in Figure 3.2. It should be mentioned that the op-amp is built in low voltage domain (V_{DDL}) in the previous PMOS design on considerations of better transistor matching[1] and smaller silicon area. The charge pump is added to boost the level shifter supply voltage when the battery (V_{BAT}) is low (regulator in low drop-out). When the battery is high, the charge pump is disabled and the battery is supplying the analog level shifter.

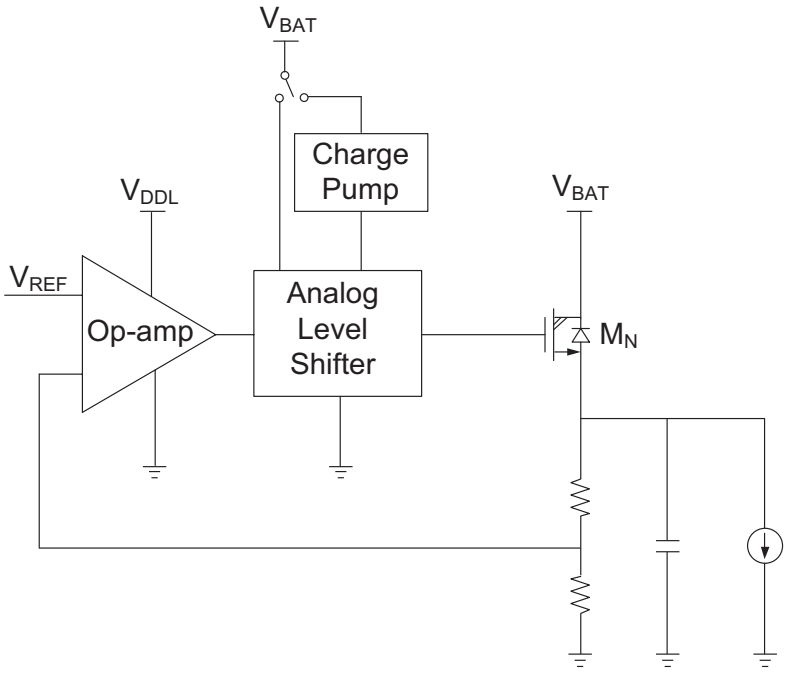

Figure 3.2: NMOS linear regulator topology.

There are three blocks in this NMOS linear regulator top view (op-amp, analog level shifter, charge pump), it is easy to find ways to combine some blocks together. For example, the charge pump and analog level shifter can be combined which directly boost the op-amp output voltage up to control the gate of M_N. Giustolisi et al. are using charge merging technique to boost the gate voltage [13][14]. Camacho et al. are

[1]High voltage transistors are normally with poor matching characteristics

applying a switched floating capacitor to generate the gate voltage [15]. The charge pump and analog level shifter combining together has advantages in aspect of lower static current consumption and less complexity of the circuit. The biggest disadvantage is the noise that the switching floating capacitor circuit generates. According to the application environment for this design, the NMOS regulator is in low drop-out regulation (LDO mode) only during engining starting. In most of operation time, the linear regulator is working in high drop-out regulation (HDO mode), the switch circuit still adds noise in high drop-out region, which is a drawback for automotive applications.

The other method to simplify Figure 3.2 is to combine the charge pump and the amplifier together (neglecting the analog level shifter stage) [16]. The advantage of this combination is that the charge pump is effective only during the low battery case. The switching noise exists in low battery supply, which only lasts for a short period of time. In normal case, the amplifier is directly connected to battery. As the battery voltage can be maximum 40V, a high voltage amplifier should be designed.

3.3 High Voltage Error Amplifier

Both operational transconductance amplifier (OTA) and operational amplifier (op-amp) can be used as a gain stage in linear regulator design. The gain stage is also named as "error amplifier (EA)", because it amplifies the voltage difference between the reference and the feedback voltage. As discussed in Section 2.2 and Section 2.3, the error amplifier characteristics are directly related to the static and dynamic performance of a linear regulator. Therefore, the design of error amplifier is key of the whole linear regulator design.

Since OTA has a high output resistance, its output resistance and power transistor gate capacitance can be combined together to form a dominate low frequency pole, which is referred to as internal compensated regulator[2]. This is a good solution for some capacitor-free linear regulator structures [17][18]. For these structures, the low output capacitance leads to a high frequency output pole (outside the desired bandwidth), the system can be designed as a single pole system.

For external compensated linear regulators (the output pole is the dominate one), an op-amp (cascading of an OTA and a buffer) is common to drive the gate of the power transistor. Since the output pole is the dominate one, any internal poles will add difficulties for compensation. Therefore, a buffer is added between the OTA and the gate of power transistor. This configuration makes the power transistor gate node with low impedance (for the low output resistance of the buffer). The OTA and the buffer interface is also with low impedance (for the low parasitic capacitance between OTA and buffer). In this way, one low frequency pole at the power transistor gate (OTA as gain stage) is traded by two relative high frequency poles (op-amp as gain stage).

[2]The dominated pole is inside the control circuit

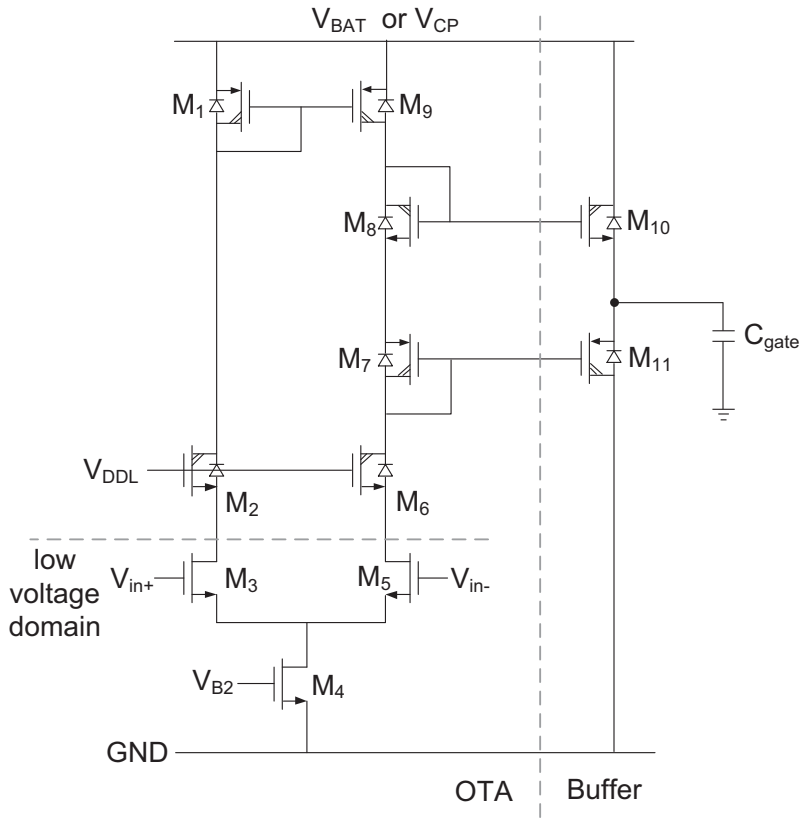

Figure 3.3: High voltage operational amplifier with cascode low voltage input pair.

In this design, the op-amp is preferred to drive the gate node of the power transistor. This preference is mainly based on the frequency compensation choice which will be discussed in Section 3.4.3. The high voltage operational amplifier is shown in Figure 3.3. The input pair transistors (M_3 and M_5) are low voltage transistors for better matching. The gain stage is composed by transistors M_1-M_9, two diode connected transistors M_7 and M_8 are mirroring the current flow through their branch to M_{10} and M_{11}.

M_{10} and M_{11} is named as a feed-forward Class AB biasing output stage [19]. The drawback of this topology is the output voltage swing is limited by the gate-source voltage of the output transistors [20]. However, in this design, considering the supply is provided either by the charge pump or the battery (always higher than 10V), the output voltage swing of the op-amp can be designed within 5.5V$\sim$8.3V, which means the requirement of op-amp output voltage swing is not critical.

One consideration of using a Class AB output stage is during line and load transient variation, the capacitative nodes may slew. The overall slew rate is limited by large capacitive nodes. By applying this Class AB output stage, the slew rate at the gate node can be increased.

3.4 Frequency Compensation

For now, the size of the power transistor, regulator topology and op-amp structure are decided, the next step is to tie these modules into a feedback loop. As discussed in Section 2.5, the NMOS linear regulator is difficult to compensate because the output pole movement over load current is dramatic. In this section, firstly the load capacitor size of this linear regulator is chosen, then the feedback loop is modeled in small signal domain. Finally, the proposed frequency compensation will be presented.

3.4.1 Output Capacitor Sizing

In this design, the external output capacitor is required as this linear regulator is targeted for providing supply voltage to devices on printed circuit board (PCB). From previous PMOS linear regulator design, a typical value 2.2μF external ceramic capacitor is defined. Since the NMOS regulator has possible advantages in transient response, there might be chance to reduce this output external capacitance in order to reduce the linear regulator cost. An output ceramic capacitor of 220nF is targeted in this design.

However, it should be noted that the value of output capacitor is related to high frequency performance such as PSRR, noise, etc. Lowering the output capacitance value may degrade these performance. Another challenge of reducing the output capacitance is the smaller output capacitance, the wider frequency range the output pole moves as expressed in Equation 2.19, which may add difficulties for frequency compensation.

3.4.2 Small Signal Modeling

Before doing frequency compensation, the small signal behavior of the feedback loop should be modeled. Based on the high voltage op-amp structure and linear regulator topology, the small signal equivalent of the feedback loop can be expressed in Figure 3.4.

It should be noted that the Class AB output stage is modeled as a single source follower. In numerical calculation, the $g_{m,BUF}$ is the transconductance of p-type and n-type source followers (M_{10} and M_{11} in Figure 3.3) adding together. The gate-source capacitance of M_{10} and M_{11} are neglected.

The transconductance of the power transistor ($g_{m,MN}$) is varying over different load current, which changes the small signal behavior of the loop. It is necessary to model the transconductance of the power transistor M_N first. Transconductance modeling of NMOS power transistor is based on two different operating regions.

In sub-threshold region (I_L is low), the n-channel of M_N is not formed. The gate voltage is controlling the p-type substrate to form a NPN bipolar transistor. Therefore, the transconductance of the NMOS transistor can be roughly modeled as a bipolar junction transistor (BJT). The transconductance of BJT is expressed

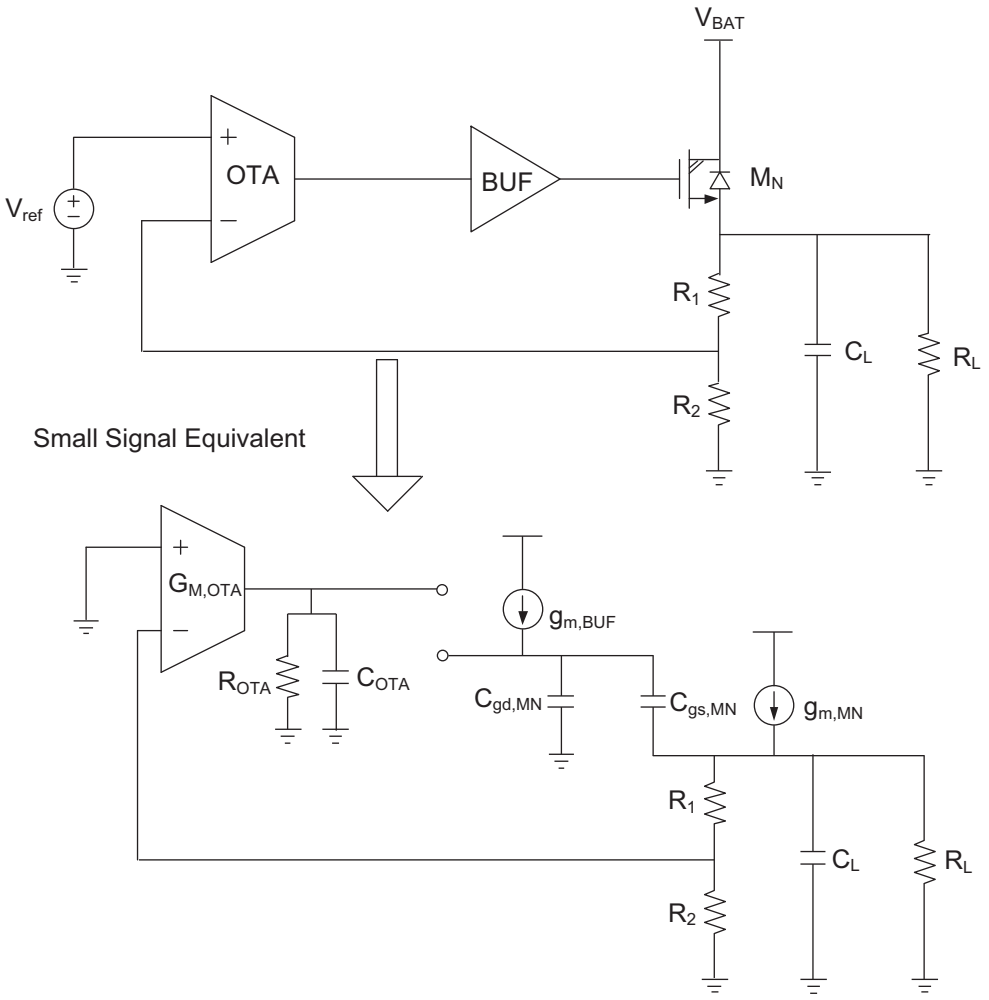

Figure 3.4: Small signal equivalent of NMOS linear regulator.

in Equation 3.1, where V_t is the thermal voltage, I_q is the quiescent current, n is a constant.

$$g_{m,substhreshold} \approx \frac{I_L + I_q}{nV_t} \tag{3.1}$$

In saturation region, the transconductance of NMOS power transistor can be modeled as Equation 3.2, where μ_n is electron mobility, C_{ox} is the gate oxide capacitance, W and L are the width and length of the power transistor, V_{GS} is the gate to source voltage, V_{TH} is the threshold voltage.

$$g_{m,saturation} \approx \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH}) = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_L} \tag{3.2}$$

For now, the transconductance of each transistor operation region is modeled. In this design, the current factor $\beta = \mu_n C_{ox} \frac{W}{L} \approx 1.7$. The transconductance is plotted in Figure 3.5. The solid line is the simulation result from Spectre, the dashed line is from the calculation results based on Equation 3.1 and Equation 3.2. (Matlab code is shown in Appendix C.1)

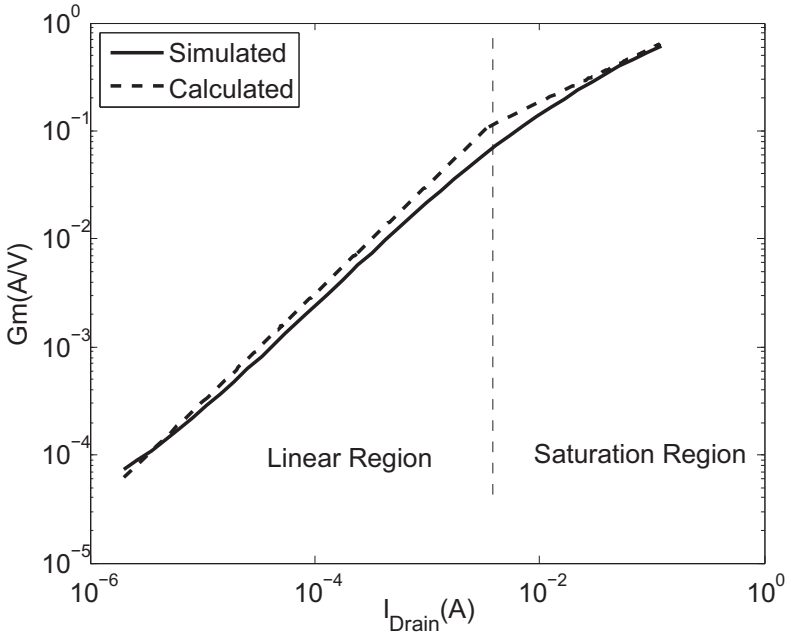

Figure 3.5: Transconductance of NMOS power transistor.

The symbolic transfer function of Figure 3.4 need to be calculated. First of all, the AC feedback loop is broke at the negative input of the op-amp while keeping the DC bias point right as shown in Figure 3.6[3].

The transfer function is calculated as the signal transferring from V_{in} to V_{out}. At each node(V_1-V_3) the current follows Kirchhoff law. Then, there are equations as follows:

$$\begin{cases} -V_{in} G_{M,OTA} \dfrac{R_{OTA}}{1 + sR_{OTA}C_{OTA}} = V_1 \\ (V_1 - V_2) g_{m,BUF} = sC_{gd,MN} V_2 + sC_{gs,MN}(V_2 - V_3) \\ (V_2 - V_3)(g_{m,BUF} + sC_{gs,MN}) \dfrac{R_L}{1 + sR_L C_L} = V_3 \\ V_{out} = \dfrac{R_2}{R_1 + R_2} V_3 \end{cases} \tag{3.3}$$

There are 4 equations and 4 unknown symbolics (suppose input signal V_{in} is already known) in Equation 3.3. The relation between V_{in} and V_{out} can be calculated

[3]In this design, the feedback loop is broke by Spectre stb analysis with the method presented in [21]

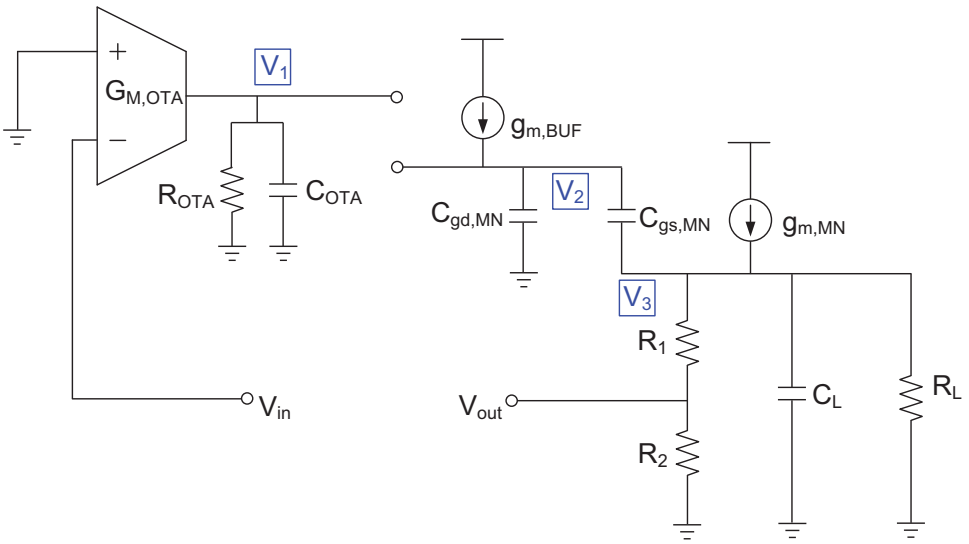

Figure 3.6: Transfer function calculation.

in Matlab (see Appendix C.2), the solution can be simplified based on the practical component parameters (Table 3.1):

Table 3.1: Components Parameters of the NMOS Linear Regulator

Symbol	Parameter	Symbol	Parameter
R_1	6.26MΩ	C_L	220nF
R_2	2MΩ	C_{OTA}	0.3pF
$g_{m,BUF}$	90μS	$g_{M,MN}$	60mS
$G_{M,OTA}$	59μS	$C_{gs,MN}$	14pF
R_{OTA}	1.31GΩ	$C_{gd,MN}$	8pF

The transfer function can be written as:

$$\frac{V_{out}}{V_{in}} \approx \frac{g_{m,MN}g_{m,BUF}G_{M,OTA}R_2R_LR_{OTA} + sg_{m,BUF}C_{gs,MN}G_{M,OTA}R_2R_LR_{OTA}}{\begin{array}{l}s^3C_LC_{OTA}(C_{gd,MN}+C_{gs,MN})(R_1+R_2)R_LR_{OTA} \\ +s^2g_{m,BUF}C_LC_{OTA}(R_1+R_2)R_LR_{OTA} \\ +sg_{m,MN}g_{m,BUF}C_{OTA}(R_1+R_2)R_LR_{OTA} \\ +g_{m,BUF}(R_1+R_2)(1+g_{m,MN}R_L)\end{array}} \tag{3.4}$$

Equation 3.4 can be further simplified as (suppose the poles are widely separated, the detailed simplification steps are discussed in Appendix A):

$$\frac{V_{out}}{V_{in}} \approx A_v \frac{1+s\dfrac{C_{gs,MN}}{g_{m,MN}}}{(1+sR_{OTA}C_{OTA})(1+s\dfrac{C_{gs,MN}+C_{gd,MN}}{g_{m,BUF}})(1+s\dfrac{C_L}{g_{m,MN}})} \tag{3.5}$$

where A_v is the DC gain of the loop, $A_v = -G_{M,OTA}R_{OTA}\frac{R_2}{R_1+R_2}\frac{g_{m,MN}R_L}{1+g_{m,MN}R_L}$.

From Equation 3.5, there are three poles and one zero in the transfer function. The zero Z_1 is formed by the power transistor $g_{m,MN}$ and $C_{gs,MN}$, which is a feed-forward zero locates at the left half plane (LHP), the frequency of it is:

$$Z_1 = -\frac{g_{m,MN}}{2\pi C_{gs,MN}} \tag{3.6}$$

Pole P_1 is generated by the interface of the OTA and the buffer, the frequency is:

$$P_1 = -\frac{1}{2\pi R_{OTA}C_{OTA}} \tag{3.7}$$

Pole P_2 is formed by the buffer output resistance and the power transistor gate capacitance, it is at relative high frequency for the buffer output resistance is $1/g_{m,BUF}$, the frequency is:

$$P_2 = -\frac{g_{m,BUF}}{2\pi(C_{gs,MN}+C_{gd,MN})} \tag{3.8}$$

Pole P_3 is generated by the output capacitance C_L and the $g_{m,MN}$. The resistance seen from the regulator output node is roughly $1/g_{m,MN}$, the frequency of P_3 is:

$$P_3 = -\frac{g_{m,MN}}{2\pi C_L} \tag{3.9}$$

3.4.3 Proposed Compensation Scheme

As discussed in Section 3.4.2, the transfer function of the feedback loop has three poles (P_1-P_3) and one zero (Z_1). P_1 and P_2 are fixed at certain frequencies, Z_1 and P_3 are variant to load current due to $g_{m,MN}$ is in their expressions. Since Z_1 is a high frequency LHP zero, it increases both gain and phase at a certain frequency range and possibly makes the feedback loop more stable. The only "trouble maker" to the stability of the loop is the output pole P_3, because it can vary a lot over the whole output current range (Figure 2.13).

The compensation scheme should accommodate the P_3 movement. In other words, the compensation should be functional over all current load. The wide movement range of P_3 adds difficulties for compensation. To deal with this movement, roughly speaking, two methods might be effective:

(1) Making P_3 always out of the expected bandwidth.
(2) Accommodate P_3 movement by adding a zero.

Method (1) can be realized by increasing the standby load current (e.g. in mA range) to move P_3 to higher frequency, but this is unacceptable for the low quiescent current requirement in this design. It can also be realized by some pole-splitting methods [7][22], which push the output pole out of the bandwidth. However, two reasons make this solution not suitable for this design. One is the gain of NMOS

power transistor in source follower configuration is near 1 which makes pole spitting very difficult. The other is the large 220nF load capacitor resulting the output pole at relatively low frequency. To push this pole to the higher frequency may require a very large spitting capacitor and high current consumption.

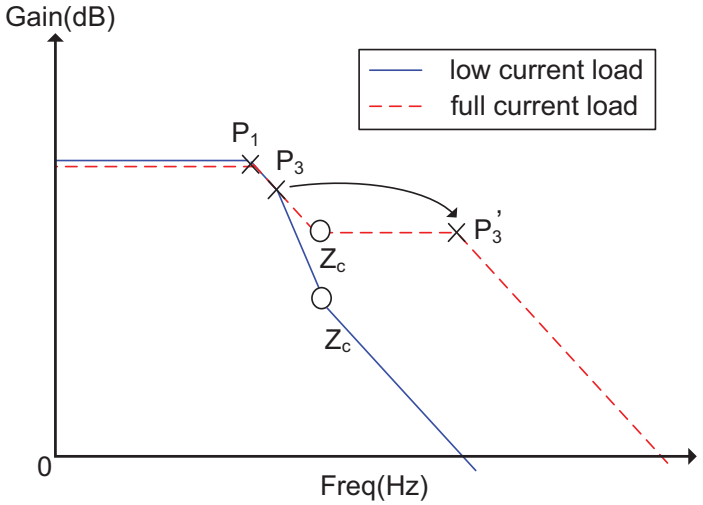

Figure 3.7: Compensation scheme of Method (2).

Method (2) can be conceptually shown in Figure 3.7, where Z_c is the zero added in the loop. It can be seen that as the load current increases, the output pole P_3 moves to the higher frequency. However, due to the existence of Z_c, the loop is stable because the phase shift of P_1 is compensated by Z_c. It is interesting to notice that as P_3 goes to higher frequency, the bandwidth also get extended. This may add advantages on transient performance as the bandwidth of the linear regulator is playing a role in line/load response.

It seems that Method (2) is a good candidate for the frequency compensation. To compensate this loop, the zero Z_c should meet two requirements: One is it must near the minimum frequency of P_3 to ensure the low current load stability; the other requirement is the associated pole generated by adding zero Z_c should be outside the maximum close-loop bandwidth. The drawback of Method (2) is the generation of low frequency Z_c needs large passive components (big resistor and big capacitor), which requires large silicon area. Also, adding Z_c through passive components will bring an associate pole with it. A few zero generation topologies are shown in Figure 3.8. If the Z_c is at low frequency, the associated pole is also at relatively low frequency.

To make Z_c located at low frequency without consuming too much silicon area, the resistive divider R_1 and R_2 in Figure 3.4 is preferred to be reused in frequency compensation as shown in Figure 3.8(c), because the low quiescent current requires large R_1 and R_2 (e.g. in MΩ range). To make the associate pole locate at higher frequency, literature [23] presents an active zero compensation scheme, which is able to generate a zero by using the resistive divider. Two drawbacks in this solution are unacceptable for this design, which are: (1) the interface between the active zero generation circuit and the resistive divider are adding DC inaccuracy at the output;

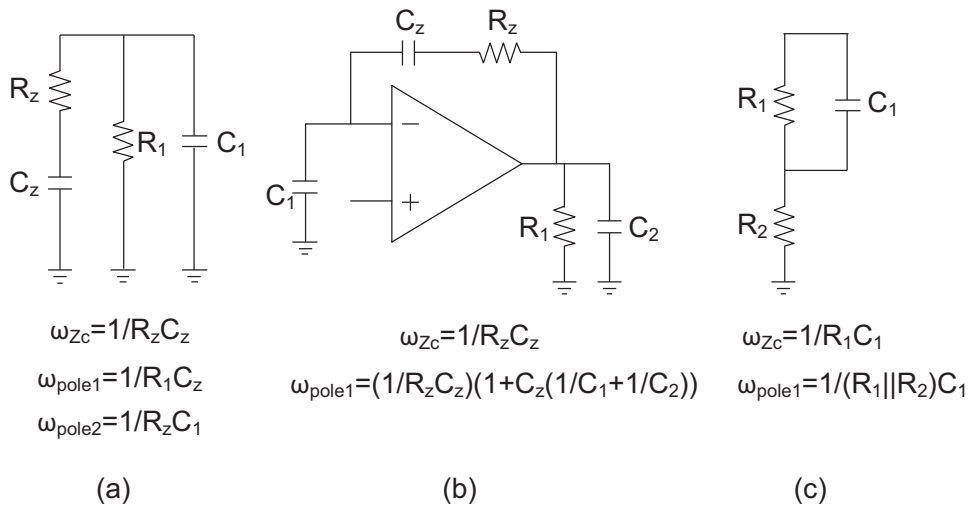

Figure 3.8: Adding a zero and its associated pole.

(2) the active zero generation circuit may not be functional when the output voltage varies vigorously.

By analyzing the structure shown in Figure 3.8(c), it can be calculated that the frequency of the associated pole is $(R_1 + R_2)/R_2$ times higher than the zero. The optimum solution for this design is making the associated pole absolutely disappear. A possible solution can be to make the associated pole merge with other poles. To be specific, by making the dominate pole at the output of the resistive divider, the time constant of the associated pole can be added into the very large time constant generated by the dominate pole. This idea is illustrated in Figure 3.9.

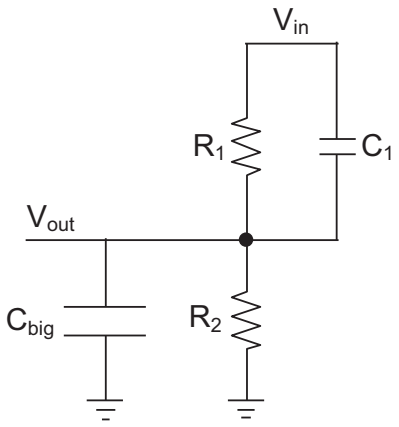

Figure 3.9: Adding a zero while merging the associated pole with dominate pole.

The transfer function from V_{in} to V_{out} in Figure 3.9 can be written as:

$$\frac{V_{out}}{V_{in}} = \frac{\dfrac{R_2}{1+sR_2C_{big}}}{\dfrac{R_1}{1+sR_1C_1}+\dfrac{R_2}{1+sR_2C_{big}}} = \frac{R_2(1+sR_1C_1)}{(R_1+R_2)+sR_1R_2(C_{big}+C_1)} \tag{3.10}$$

The pole is at $-1/2\pi(R_1||R_2)(C_{big}+C_1)$ and the zero is at $-1/2\pi R_1C_1$. If $C_{big} \gg C_1$, the effect of the associated pole on the dominate pole is negligible.

For now, the method of adding a zero without being troubled by its associated pole is found. The next step is to generate a large capacitance to form the C_{big}. It turns out that pole splitting technique is a perfect candidate for generating an equivalent large capacitance. In this design, the C_{big} can be generated by connecting the high voltage op amp into an integrator configuration by C_2 as shown in Figure 3.10. The equivalent capacitance at the input of amplifier is around A_vC_2, where A_v is the open-loop gain of the op-amp. If the signal transfers from the input node of resistive divider V_{in} to the gate node of power transistor V_{gate}, the nodal equations can be written as:

$$\begin{cases} \dfrac{V_{in}-V_1}{R_1} + s(V_{in}-V_1)C_1 = \dfrac{V_1}{R_2} + s(V_1-V_{gate})C_2 \\ -G_{M,OTA}V_1 = \dfrac{V_2}{R_{OTA}} + sC_{OTA}V_2 \\ g_{m,BUF}V_2 = g_{m,BUF}V_{gate} + sC_{gate}V_{gate} + s(V_{gate}-V_1)C_2 \end{cases} \tag{3.11}$$

Suppose the poles and zeros are separated, transfer function is calculated by Matlab (Appendix C.3) as[4]:

$$\frac{V_{gate}}{V_{in}} \approx \frac{\begin{array}{l} s^3C_1C_2C_{OTA}R_1R_2R_{OTA} + s^2C_2C_{OTA}R_2R_{OTA} \\ -sg_{m,BUF}C_1G_{M,OTA}R_1R_2R_{OTA} - g_{m,BUF}G_{M,OTA}R_2R_{OTA} \end{array}}{\begin{array}{l} s^3C_1C_{OTA}C_{gate}R_1R_2R_{OTA} + s^2g_{m,BUF}C_1C_{OTA}R_1R_2R_{OTA} \\ +sg_{m,BUF}C_2G_{M,OTA}R_1R_2 + (R_1+R_2)g_{m,BUF} \end{array}} \tag{3.12}$$

The transfer function can be further simplified as:

$$\frac{V_{gate}}{V_{in}} \approx A_v \frac{(1+sR_1C_1)(1-s\dfrac{C_2C_{OTA}}{g_{m,BUF}R_1C_1G_{M,OTA}} - s^2\dfrac{C_2C_{OTA}}{g_{m,BUF}G_{M,OTA}})}{[1+sG_{M,OTA}R_{OTA}C_2(R_1||R_2)](1+s\dfrac{C_{OTA}C_1}{G_{M,OTA}C_2})(1+s\dfrac{C_{gate}}{g_{m,BUF}})} \tag{3.13}$$

where $A_v = -G_{M,OTA}R_{OTA}\dfrac{R_2}{R_1+R_2}$

[4] The simplification is based on C_1=10pF, C_2=1.2pF and other numerical values shown in Table 3.1

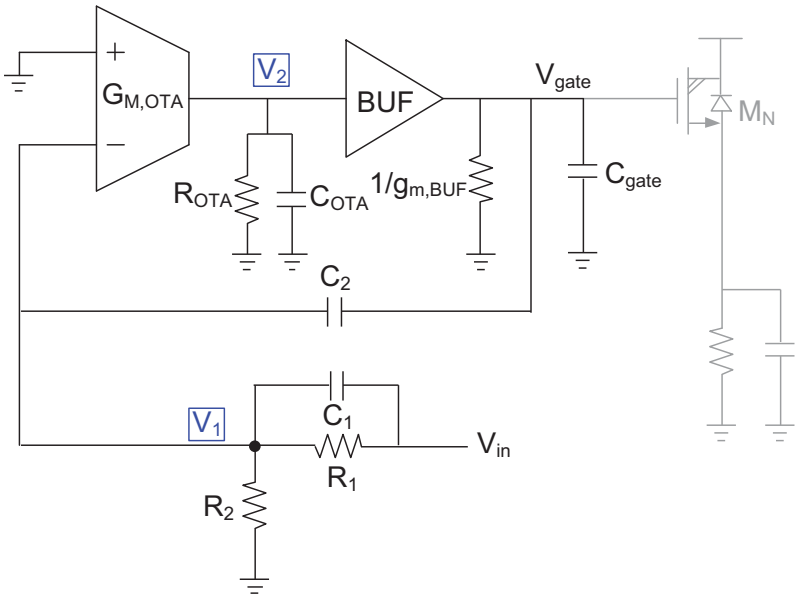

Figure 3.10: Integrator configuration with C_2.

First starting from the numerator, there are three zeros, the first zero Z_1 is the expected zero to compensate the system, which locates at:

$$Z_1 = -\frac{1}{2\pi R_1 C_1} \tag{3.14}$$

Another two zeros are generated by the feed-forward capacitor C_2. It should be noted that this zero pair is a LHP zero and a RHP zero in combination. The content in the numerator second parentheses of Equation 3.13 can be simplified as (based on $R_1C_1 \gg C_2C_{OTA}$):

$$1 - s^2 \frac{C_2 C_{OTA}}{G_{M,OTA} g_{m,BUF}} \tag{3.15}$$

It results two zeros at:

$$Z_{2,3} \approx \pm \frac{1}{2\pi} \sqrt{\frac{G_{M,OTA} g_{m,BUF}}{C_2 C_{OTA}}} \tag{3.16}$$

We now calculate the pole frequencies, P_1 is the pole formed by the splitting equivalent capacitor C_2 and resistive divider, which is at:

$$P_1 = -\frac{1}{2\pi G_{M,OTA} R_{OTA} C_2 (R_1 || R_2)} \tag{3.17}$$

P_2 is formed by the OTA transconductance and capacitance, C_1 and C_2 is forming a capacitive feedback around the OTA. The pole frequency is:

$$P_2 = -\frac{1}{2\pi} \frac{C_2}{C_1} \frac{G_{M,OTA}}{C_{OTA}} \tag{3.18}$$

P_3 is formed by the buffer output resistance and gate capacitance at the power transistor, which locates at:

$$P_3 = -\frac{g_{m,BUF}}{2\pi C_{gate}} \tag{3.19}$$

In Equation 3.13, the simplification is based on the assumption that P_2 and P_3 are separated. P_2 and P_3 can also form a pair of complex poles. To further model this transfer function, the transfer function of Equation 3.13 can be written as:

$$\frac{V_{out}}{V_{in}} \approx A_v \frac{(1+sR_1C_1)(1-s\frac{C_2C_{OTA}}{R_1C_1G_{M,OTA}gm,BUF}-s^2\frac{C_2C_{OTA}}{G_{M,OTA}g_{m,BUF}})}{[1+sG_{M,OTA}R_{OTA}C_2(R_1||R_2)](1+s\frac{C_{OTA}C_1}{G_{M,OTA}C_2}+s^2\frac{C_1C_{OTA}C_{gate}}{g_{m,BUF}G_{M,OTA}C_2})} \tag{3.20}$$

The complex poles can be formed if:

$$(\frac{C_{OTA}C_1}{G_{M,OTA}C_2})^2 < 4\frac{C_1C_{OTA}C_{gate}}{g_{m,BUF}G_{M,OTA}C_2} \tag{3.21}$$

which is:

$$\frac{g_{m,BUF}}{C_{gate}} < 4\frac{C_2}{C_1}\frac{G_{M,OTA}}{C_{OTA}} \tag{3.22}$$

The pair of complex poles will have a resonate frequency at:

$$P_{2,3} = -\frac{1}{2\pi}\sqrt{\frac{g_{m,BUF}G_{M,OTA}C_2}{C_1C_{OTA}C_{gate}}} \tag{3.23}$$

For now, the signal transfer behavior from the input of the resistive divider to the gate of power transistor has been analyzed. It would be necessary to know the total feedback loop transfer function. The signal transfer from the gate of the power transistor M_N to the output of the linear regulator will meet one zero (Equation 3.6) and one pole (Equation 3.9). Assume $C_{gate}\approx C_{gs,MN}+C_{gd,MN}$ and neglect the resistive divider loading effect due to break the AC loop (for C_L is large), the simplified transfer function of the whole loop can be written as:

$$\frac{V_{out}}{V_{in}} \approx \frac{A_v(1+sR_1C_1)(1-s^2\frac{C_2C_{OTA}}{g_{m,BUF}G_{M,OTA}})(1+s\frac{C_{gs,MN}}{g_{m,MN}})}{[1+sG_{M,OTA}R_{OTA}C_2(R_1||R_2)](1+s\frac{C_{OTA}C_1}{G_{M,OTA}C_2}+s^2\frac{C_1C_{OTA}C_{gate}}{g_{m,BUF}G_{M,OTA}C_2})(1+s\frac{C_L}{g_{m,MN}})} \tag{3.24}$$

where $A_v = -G_{M,OTA}R_{OTA}\frac{R_2}{R_1+R_2}$

The pole zero locations are summarized in Table 3.2.

Table 3.2: Poles and Zeros Location of the Whole Loop

Poles	Zeros
$P_1 = -\frac{1}{2\pi G_{M,OTA} R_{OTA} C_2 (R_1 \| \| R_2)}$	$Z_1 = -\frac{1}{2\pi R_1 C_1}$
$P_{2,3} \approx -\frac{1}{2\pi}\sqrt{\frac{g_{m,BUF} G_{M,OTA} C_2}{C_1 C_{OTA} C_{gate}}}$	$Z_{2,3} \approx \pm\frac{1}{2\pi}\sqrt{\frac{g_{m,BUF} G_{M,OTA}}{C_2 C_{OTA}}}$
$P_4 = -\frac{g_{m,MN}}{2\pi C_L}$	$Z_4 = -\frac{g_{m,BUF}}{2\pi C_{gs,MN}}$

It should be noted that $P_{2,3}$ are assumed to be a pair of complex poles (Inequation 3.22 is easily tenable in this design), the $P_{2,3}$ frequency in the table is the resonant frequency(where gain and phase reduce on bode plot).

More accurate overall transfer function is calculated by solving nodal equations which is shown in Appendix B.

The accuracy of the small signal modeling should be verified. Figure 3.11 shows the low load current bode plot of the overall transfer function, where the solid line is the Spectre transistor level simulation result. The dashed-dot line is based on the simplified transfer function shown in Equation 3.24. The dashed line is based on the calculated overall transfer function Equation B.2 in Appendix B.

It can be seen that the simplified transfer function is accurate enough to describe transistor level circuit AC behavior. The poles and zeros marked on the figure are corresponding to Table 3.2.

Since the bode plot at low load current is already known, it would be interesting to notice the stability. The bode plot can be simplified as shown in Figure 3.12.

Suppose the gain roll down from P_1 to P_4 is by 20dB/dec, from P_4 to 0dB is by 40dB/dec. Then, the following equation holds:

$$A_{v,dB} - 20log_{10}\frac{f_{P4}}{f_{P1}} - 40log_{10}\frac{f_{BW}}{f_{P4}} = 0 \tag{3.25}$$

which is:

$$A_{v,dB} = 20log_{10}\frac{f_{P4} f_{BW}^2}{f_{P1} f_{P4}^2} \tag{3.26}$$

Suppose the decimal value of $A_{v,dB}$ is $A_{v,decimal}$, Equation 3.26 can be rewritten as:

$$A_{v,dB} = 20log_{10} A_{v,decimal} = 20log_{10}\frac{f_{P4} f_{BW}^2}{f_{P1} f_{P4}^2} \tag{3.27}$$

which can be simplified as:

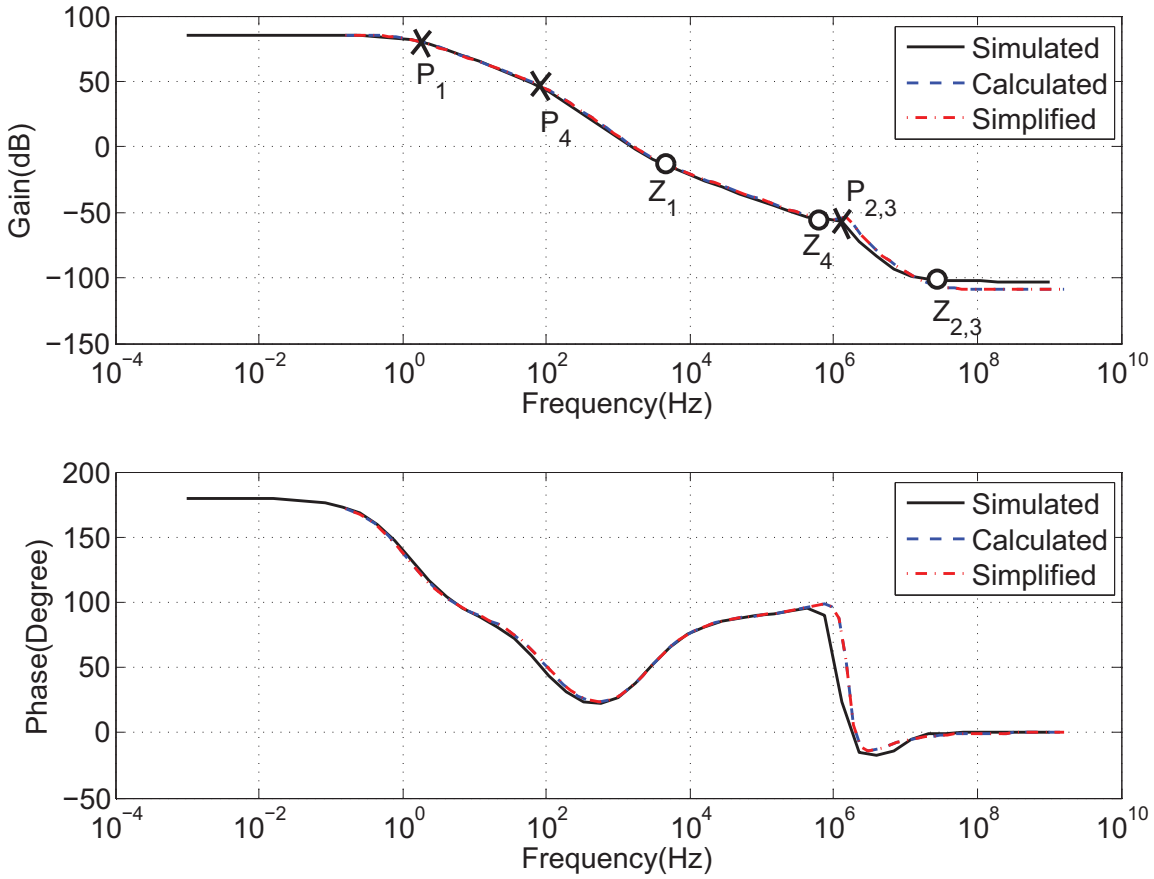

Figure 3.11: Bode plot at I_L=0μA.

$$A_{v,decimal} = \frac{f_{BW}^2}{f_{P1} f_{P4}} \tag{3.28}$$

The bandwidth is:

$$f_{BW} = \sqrt{A_{v,decimal} f_{P1} f_{P4}} \tag{3.29}$$

Since the bandwidth, poles and zeros frequency are already known, the phase margin (PM) of this bode plot can be written as:

$$PM = 90 - arctan\frac{f_{BW}}{f_{P4}} + arctan\frac{f_{BW}}{f_{Z1}} \tag{3.30}$$

which is:

$$PM = 90 - arctan\sqrt{\frac{A_{v,decimal} f_{P1}}{f_{P4}}} + arctan\sqrt{\frac{A_{v,decimal} f_{P1} f_{P4}}{f_{Z1}^2}} \tag{3.31}$$

According to Table 3.2, it can be rewritten as:

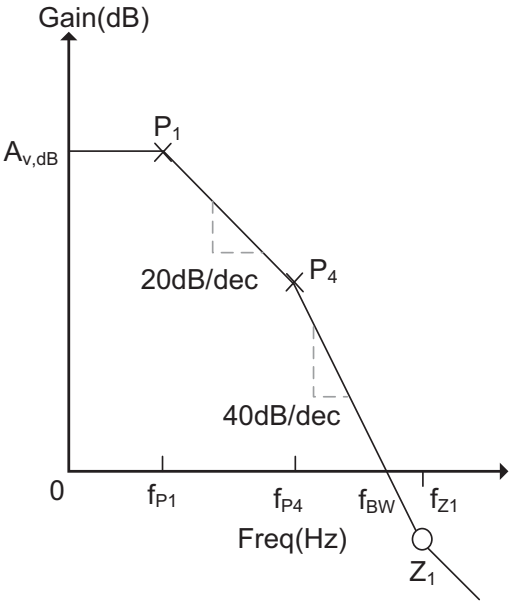

Figure 3.12: Simplified bode plot analysis at I_L=0μA.

$$PM = 90 - arctan\sqrt{\frac{C_L}{g_{m,MN}R_1C_2}} + arctan\sqrt{\frac{g_{m,MN}R_1C_1^2}{C_LC_2}} \tag{3.32}$$

Assume $A_{v,decimal}f_{P1}$ is 100kHz, sweep f_{P4} and f_{Z1}, the phase margin can be plotted in Figure 3.13.

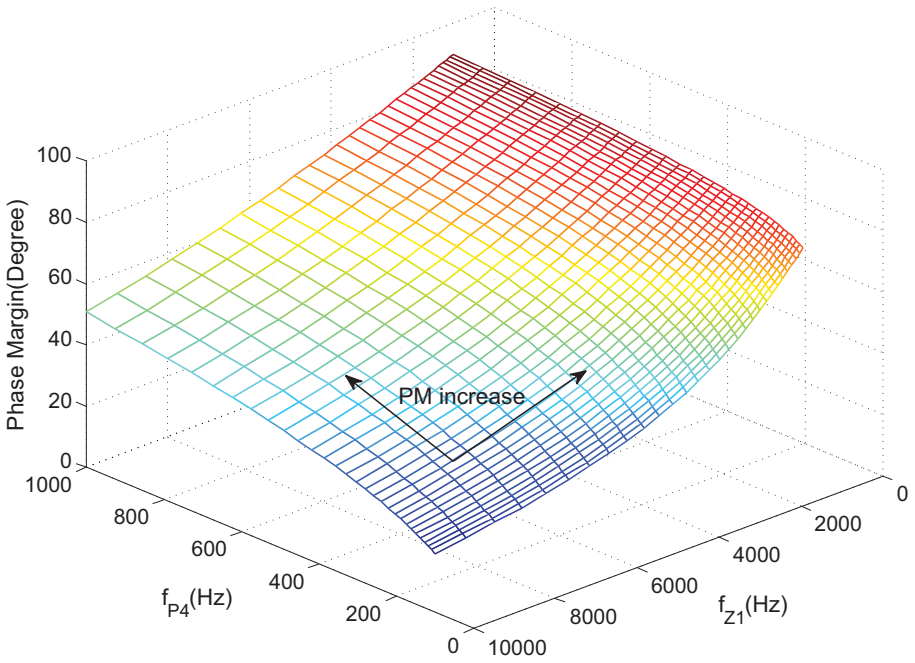

Figure 3.13: Phase margin analysis at I_L=0μA.

It can be seen that either moving f_{P4} to higher frequency or moving f_{Z1} to lower frequency will improve the phase margin. However, these two approaches are costly for the design. To be specific, moving f_{P4} to the higher frequency means more quiescent current ($g_{m,MN} \propto \sqrt{(I_q + I_L)}$). While moving f_{Z1} to lower frequency means increasing R_1C_1, which means more silicon area.

Next, the feedback loop stability at high current load is investigated. Again, the transfer function is based on Equation B.2 and Equation 3.24. $g_{m,MN}$ is based on Figure 3.5. The bode plot at full current load (I_L=120mA) is shown in Figure 3.14. The solid line is the transistor level simulation result in Spectre, the dashed line is the based on the overall transfer function and the dashed-dot line is based on the simplified transfer function.

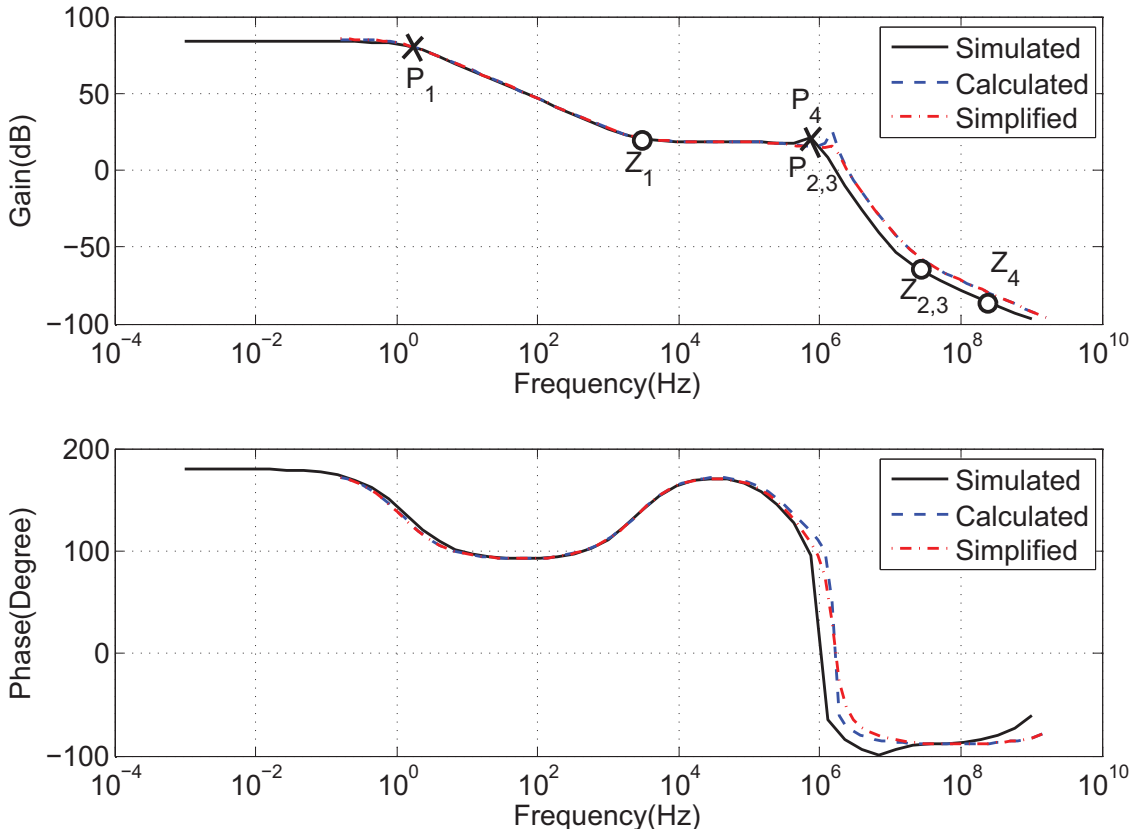

Figure 3.14: Bode plot at full load current I_L=120mA.

It can be concluded that the calculated transfer function describes the transistor level AC behavior accurately. P_4 has already moved to the higher frequency, which resulted in a bandwidth extension. However, as shown in Figure 3.14, the feedback system at full current load is instable, because the bandwidth is larger than the $P_{2,3}$ frequency, resulting in four poles one zero inside bandwidth. Since the bandwidth should be lower than the $P_{2,3}$ frequency, it is important to know the bandwidth expression. The simplified bode plot is show in Figure 3.15

Since the frequency axis(x-axis) is in logarithmic scale. The following holds:

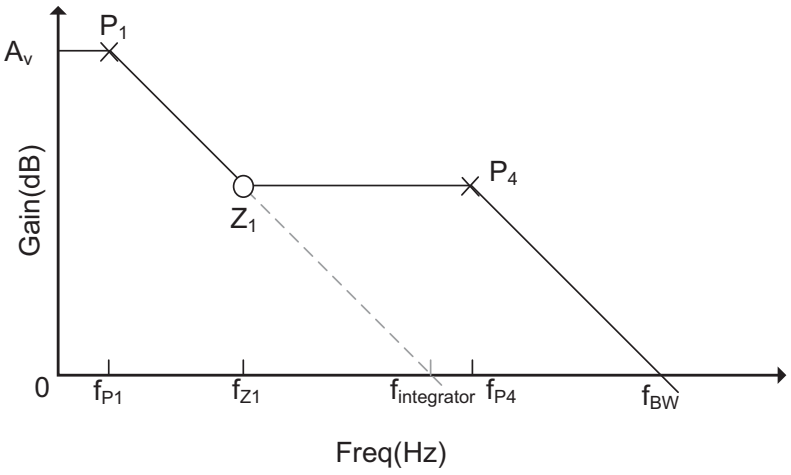

Figure 3.15: Stability analysis at high load current.

$$\frac{f_{BW}}{f_{integrator}} = \frac{f_{P4}}{f_{Z1}} \tag{3.33}$$

Using the pole-zero expressions in Table 3.2, the bandwidth can be written is:

$$f_{BW} = \frac{g_{m,MN} C_1}{2\pi C_L C_2} \tag{3.34}$$

From Equation 3.34, it can be seen that either reducing C_1 or increasing C_L and C_2 can limit the bandwidth. However, according to Equation 3.32, the value of C_1 is chosen to increase the phase margin at low current load. Typical value of C_L is determined. The only value can be tuned is C_2. As C_2 increases, the f_{BW} is limited. $P_{2,3}$ also go to the higher frequency which allows us to stabilize the system.

By increasing C_2 the system can be compensated by sort of "narrow-banding" technique, but it sacrifices the transient performance by making the feedback loop bandwidth slower. If this bandwidth extension characteristic of the proposed compensation scheme can be taken advantage of, methods of pushing $P_{2,3}$ to higher frequencies without limiting the bandwidth should be considered.

3.5 Adaptive Biasing

In this section, an adaptive biasing method is introduced which can stabilize the system without sacrificing the bandwidth. Form Table 3.2, $P_{2,3}$ can be moved to higher frequency by increasing $g_{m,BUF}$ and $G_{M,OTA}$. According to the op-amp topology (Figure 3.3), it can be known that the tail current flow through M_4 determines both the bias current of the OTA and the buffer. As the tail current increase, both the $g_{m,BUF}$ and $G_{M,OTA}$ will increase. If the tail current of M_4 is proportional to the load current I_L, then $P_{2,3}$ will move to higher frequency as I_L increases. In this way, the stability of the loop can be ensured without sacrificing the bandwidth. The concept of adaptive biasing is illustrated in Figure 3.16.

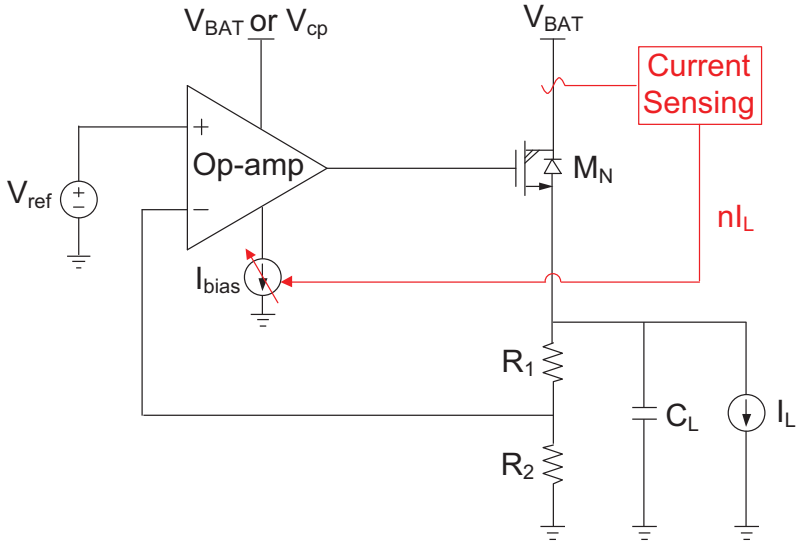

Figure 3.16: Illustration of adaptive biasing idea.

3.5.1 Current Sensing for Adaptive Biasing

The current sensing of NMOS transistor can be achieved by keeping the node voltages of M_N and M_{N1} exactly the same as shown in Figure 3.17. The source node voltage of M_N and M_{N1} are regulated to the same voltage level, the current sensing can work precisely.

The only error of this current sensing scheme is due to the mismatch of M_N, M_{N1} and the finite gain of the OTA. It can be found that when the output current increases, the regulation loop gain reduces, the sensing error increases. Since the output current sensing is not required to be very accurate, this error can be tolerated.

It should be noted that in low drop-out regulation, M_N and M_{N1} are effectively resistors. The sensing current is still with the same ratio to the current flow through the pass transistor because the R_{DS} resistance is inversely ratioed. Therefore, the current sensing scheme in Figure 3.17 works accurately in saturation and linear region.

3.5.2 Frequency Compensation for Current Sensing Loop

Since the regulation loop is used for generating a NMOS current mirror, the stability of this regulation loop should be taken care of. Moreover, the bandwidth of this loop is the "bottleneck" of the overall bandwidth of the regulator, because the stability of the main feedback loop is relies on this adaptive biasing. If the adaptive biasing is slower than the main loop, it might cause stability problems.

R_3 and C_3 are added at V_{OUT1} node for frequency compensation of the current sensing loop. This compensation is functional when M_{N1} is conducting little current. At this scenario, V_{OUT1} node is actually a high impedance node, and the OTA output also provides a high impedance node. These two low frequency poles inside the loop cause stability issues.

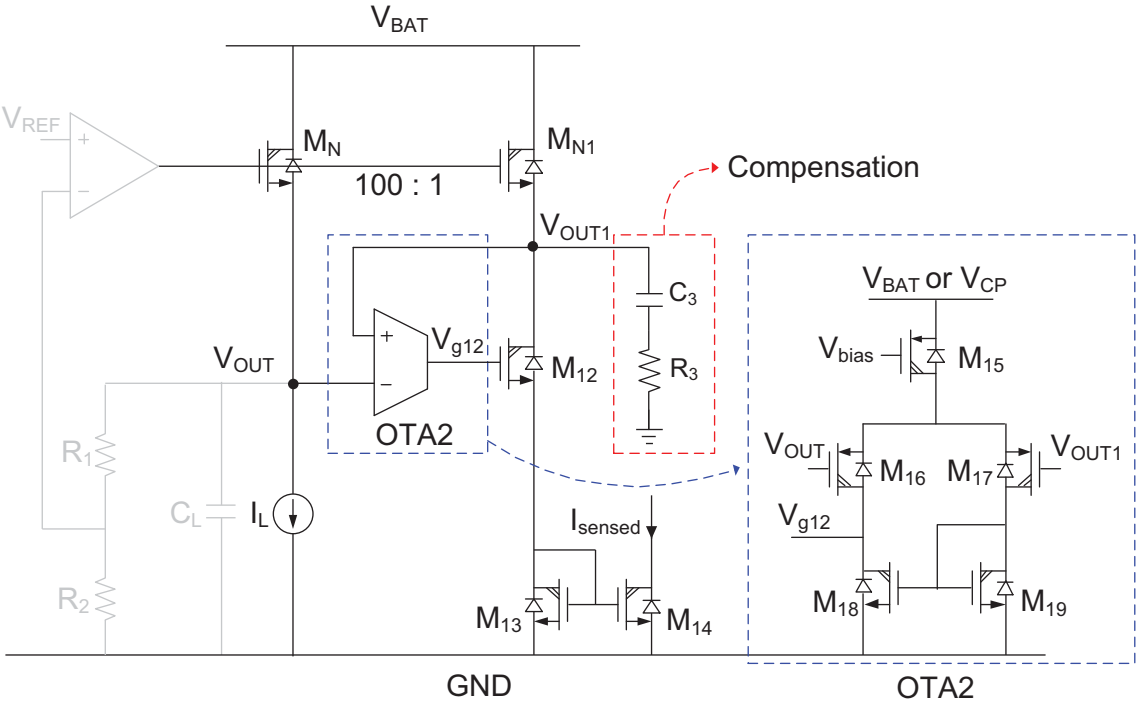

Figure 3.17: Current sensing scheme with regulated source node voltage.

Normally, to deal with two low frequency poles, "pole splitting" is a good candidate. However, there are two causes that make it not suitable for this design. The first is the bandwidth of this regulation loop should not be limited by frequency compensation. The second is at high load current, the gain reduction of M_{12}(due to current flow through M_{N1}) will make the spitting not very effective.

Based on these considerations, a compensation scheme which does not limit the bandwidth and only effective at low current load is desired. The current sensing loop is broke at the V_{OUT1} node. The equivalent small signal model is shown in Figure 3.18, the transfer function can be written as:

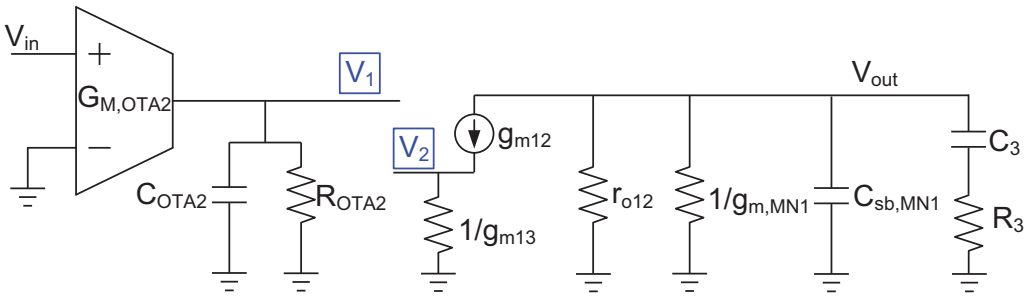

Figure 3.18: Small signal equivalent of current sensing loop.

$$\begin{cases} V_{in}G_{M,OTA2} = \dfrac{V_1}{R_{OTA2}} + sV_1C_{OTA2} \\ g_{m12}(V_1 - V_2) = g_{m13}V_2 \\ g_{m12}(V_1 - V_2) = \dfrac{V_{out}}{r_{o12}} + g_{m,MN1}V_{out} + sC_{sb,MN1}V_{out} + \dfrac{V_{out}}{R_3 + \dfrac{1}{sC_3}} \end{cases} \tag{3.35}$$

The complete transfer function is written as:

$$\frac{V_{out}}{V_{in}} = \frac{g_{m12}}{g_{m12} + g_{m13}} \frac{G_{M,OTA2}R_{OTA2}r_{o12}(1 + sC_3R_3)}{(1 + sR_{OTA2}C_{OTA2})[1 + g_{m,MN1}r_{o12} + s(C_3r_{o12} + r_{o12}C_{sb,MN1} + C_3R_3 + g_{m,MN1}r_{o12}C_3R_3) + s^2C_3R_3r_{o12}C_{sb,MN1}]} \tag{3.36}$$

Suppose $g_{m,MN1}r_{o12} \gg 1$, $C_3 \gg C_{sb,MN1}$, Equation 3.36 can be simplified as:

$$\frac{V_{out}}{V_{in}} \approx \frac{g_{m12}}{g_{m12} + g_{m13}} \frac{G_{M,OTA2}R_{OTA2}r_{o12}(1 + sC_3R_3)}{(1 + sR_{OTA2}C_{OTA2})[g_{m,MN1}r_{o12} + s(1 + g_{m,MN1}R_3)r_{o12}C_3 + s^2C_3R_3r_{o12}C_{sb,MN1}]} \tag{3.37}$$

It can be seen that in Equation 3.37, there is one pole at $P_5 = -1/(2\pi R_{OTA2}C_{OTA2})$ and one zero at $Z_5 = -1/(2\pi R_3C_3)$. For another two poles in the transfer function, their frequencies are related to the $g_{m,MN1}$. At low current load, the term in the denominator of Equation 3.37 $s(1+g_{m,MN1}R_3)r_{o12}C_3 \approx sr_{o12}C_3$ (for $g_{m,MN1}$ is quite small e.g. 1μS), which leads the two poles $P_6 = -g_{m,MN1}/(2\pi C_3)$ and $P_7 = -1/(2\pi R_3C_{sb,MN1})$ respectively. The simulated bode plot is shown in Figure 3.19.

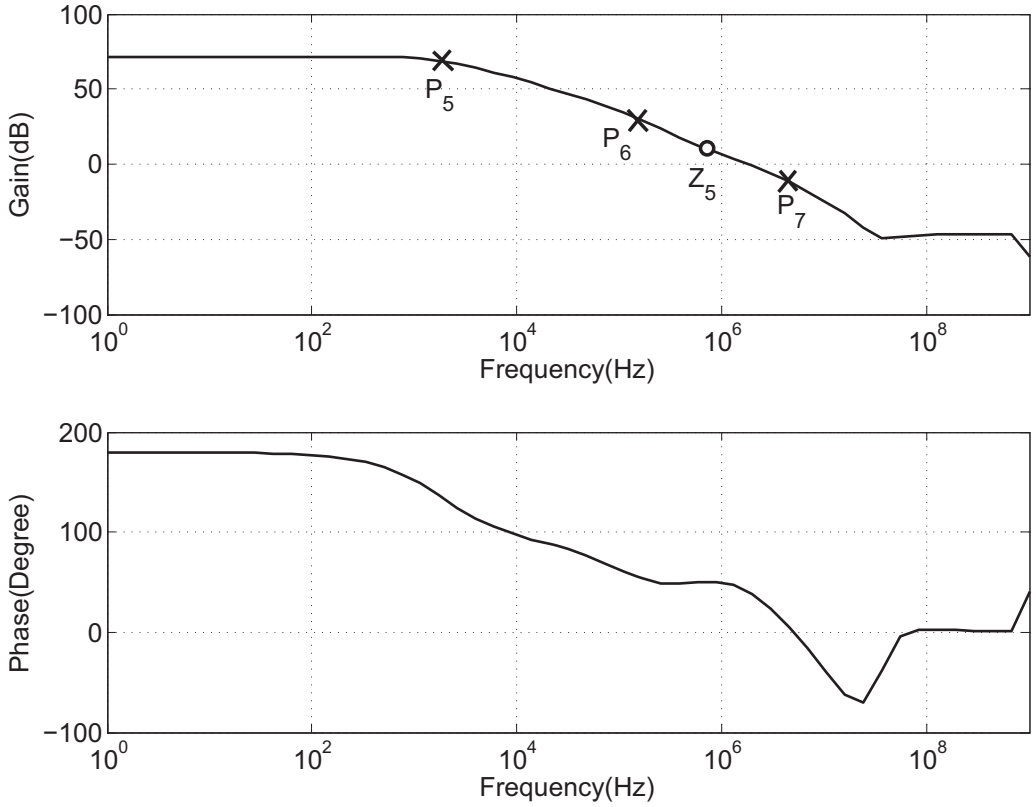

Figure 3.19: Current sensing loop bode plot at $I_L = 0\mu A$.

At high load current, the term in the denominator $s(1 + g_{m,MN1}R_3)r_{o12}C_3 \approx sr_{o12}C_3g_{m,MN1}R_3$ (for $g_{m,MN1}$ is much larger due to current increases, $g_{m,MN1}R_3 \gg 1$), the P_6 and P_7 frequencies are changed to $-1/(2\pi R_3C_3)$ and $-g_{m,MN1}/(2\pi C_{sb,MN1})$ respectively. The Z_5 and P_6 are canceling each other, the P_7 is at relatively high frequency for $C_{sb,MN1}$ is quite small. The simulated bode plot of current sensing at high current load is shown in Figure 3.20.

Figure 3.21 shows the phase margin and bandwidth over all current load for this current sensing regulation loop, it can be seen that the bandwidth of this loop is alway higher than 1MHz. The minimum bandwidth happens at the current is at 250mA[5], which is around 3.5MHz. The bottleneck of the main voltage regulation loop bandwidth should be lower than this value.

[5]It should be noted that the typical maximum current load for this regulator is 120mA, however, stability should be guaranteed to near 250mA before the current limitation operates.

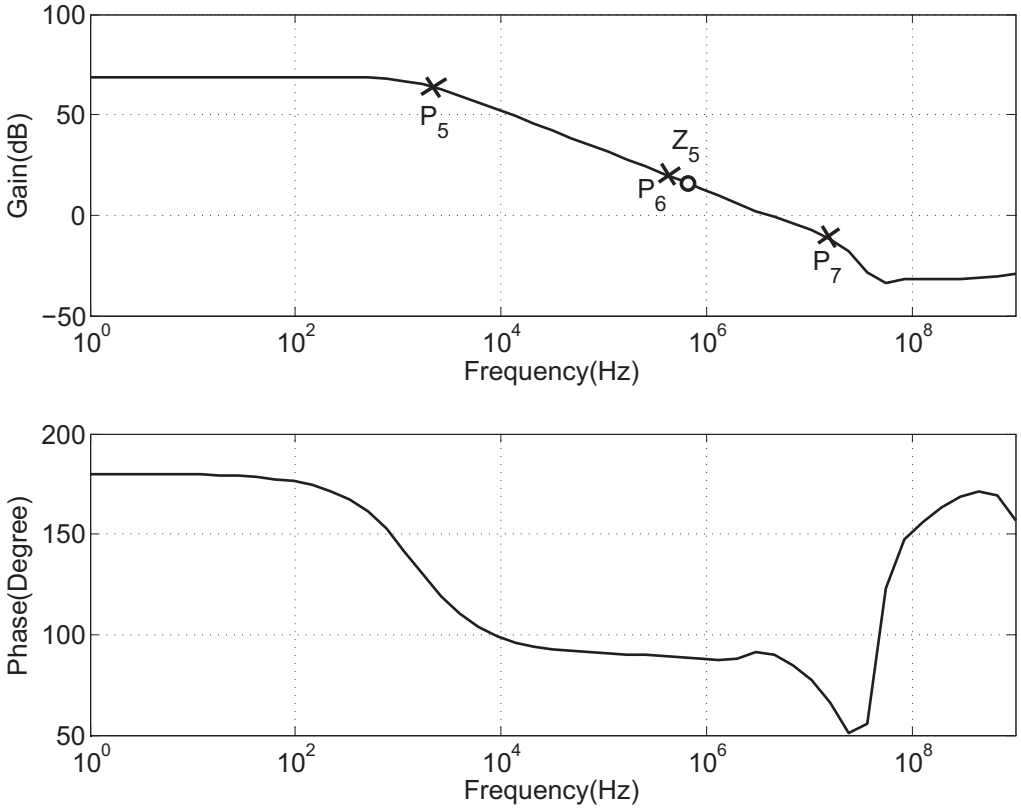

Figure 3.20: Current sensing loop bode plot at I_L=120mA.

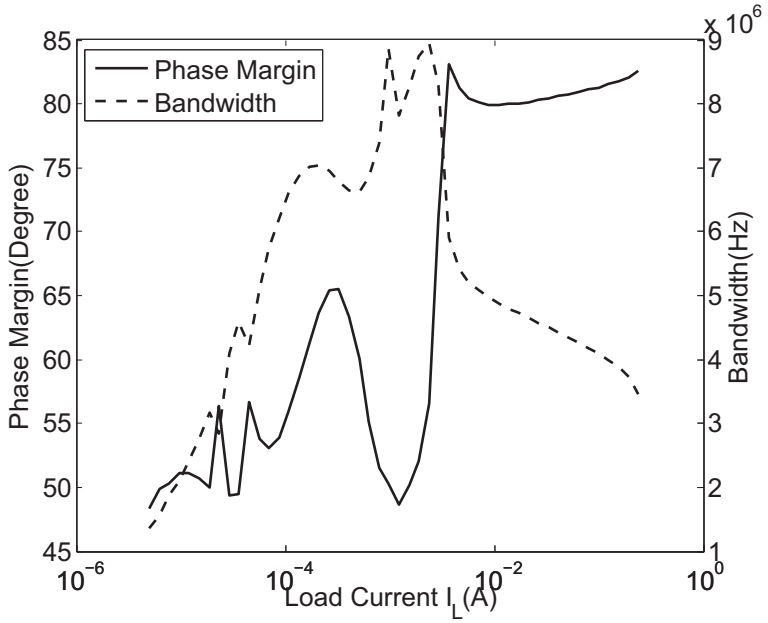

Figure 3.21: Phase margin and bandwidth versus load current for current sensing loop.

3.5.3 Adaptive Biasing Current Ratio Consideration

For the adaptive biasing, the ratio between output current I_L and high voltage op-amp bias current should be defined. It is clear from $P_{2,3}$ frequency in Table 3.2 that the more bias current, the higher frequency of $P_{2,3}$. However, this bias current degrades the overall current efficiency. Especially, in this design, the bias current can be provided by a charge pump during low battery mode. Higher current ability for charge pump requires more silicon area.

At high current load, the bias current should be at its maximum. Theoretically, if $P_{2,3}$ are always kept at 3∼4 times higher than the bandwidth frequency. The system can be kept stable with a good damping behavior. However, the bandwidth of the linear regulator is not increasing linearly with I_L. The bandwidth increases faster near low current load region. Therefore, an adaptive biasing circuit (composed by M_{13}, M_{14} and R_{limit}) with peak current limitation and fast bias increasing rate near low current load is used, which is shown in Figure 3.22.

The voltage drop on R_{limit} is forcing M_{14} going into the linear region at high current load. The maximum adaptive bias current can be limited to $(V_{in+} - V_{TH,3})/R_{limit}$. The adaptive bias current $I_{dyn,bias}$ versus I_L is shown in Figure 3.23.

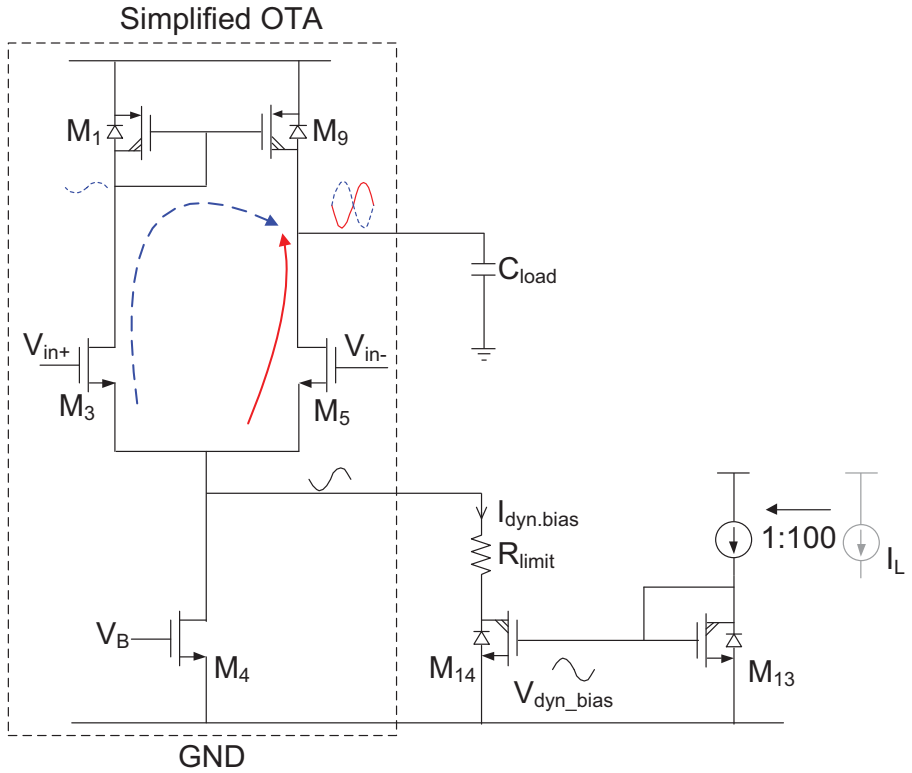

Figure 3.22: Adaptive biasing on the main voltage feedback loop stability analysis.

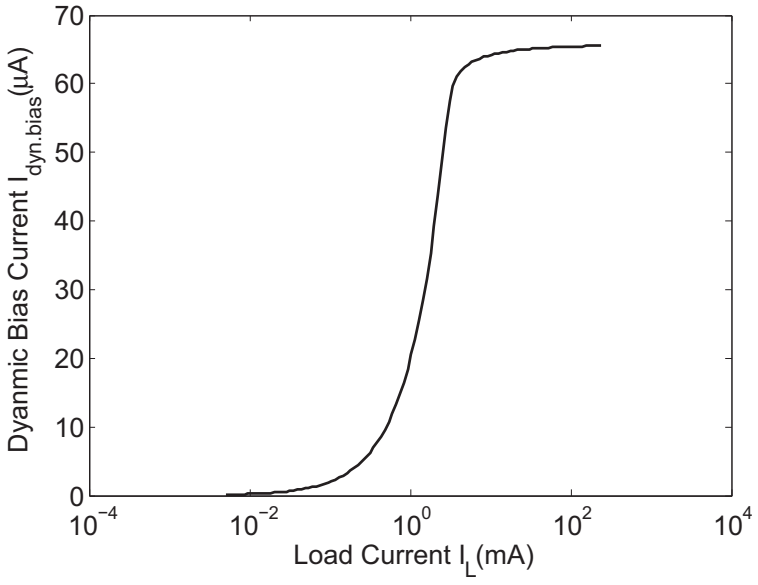

Figure 3.23: Adaptive biasing current versus load current I_L.

3.5.4 Adaptive Biasing Effect on Main Voltage Regulation Loop

The interesting question for adaptive biasing scheme would be "Does it affect the linear regulator main voltage regulation loop stability?". To find this answer, the effect of adaptive biasing on the op-amp output will be analyzed, which is shown in Figure 3.22.

It can be seen that there are two paths (dashed and solid line) for the adaptive biasing signal (the sine-wave). If transistors are perfectly matched and there are no parasitic poles in the signal transfer paths, the op-amp output should not be affected by the adaptive biasing signal variation (as shown that the solid and dashed waveform are canceling each other at C_{load} node). However, in practical circuits there must be some asymmetries. To further verify the stability of adaptive biasing loop, the AC loop is broken at M_{14} gate node, a test AC signal V_{t_in} is injected, the feedback signal V_{t_out} is received at the M_{13} gate node. The open-loop gain (V_{t_out}/V_{t_in}) plot of the adaptive feedback loop is shown in Figure 3.24.

The maximum gain of the adaptive biasing loop is less than -20dB. Therefore, the adaptive biasing loop through the whole regulator can not be treated as a "feedback" system, because even for a signal injects into the feedback system, there is not strong enough a signal back. Therefore, stability of this adaptive biasing loop is ensured.

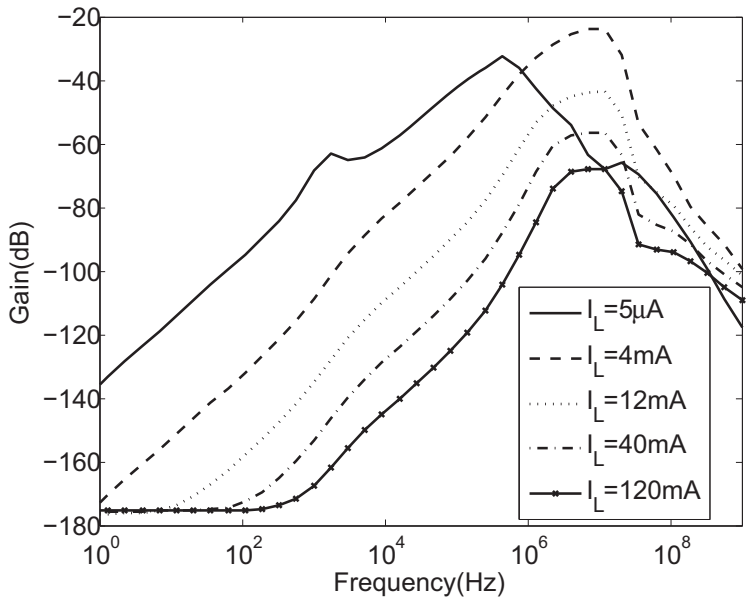

Figure 3.24: Adaptive biasing loop gain plot.

3.5.5 Linear Regulator High Current Load Stability with Adaptive Biasing

At high current load (I_L=120mA), the linear regulator main voltage feedback loop bode plot with adaptive biasing is shown in Figure 3.25. From this plot, it can be seen that with the implementation of adaptive biasing, $P_{2,3}$ is moved to the higher frequency (compare to Figure 3.14), which ensures the system stability at high current load.

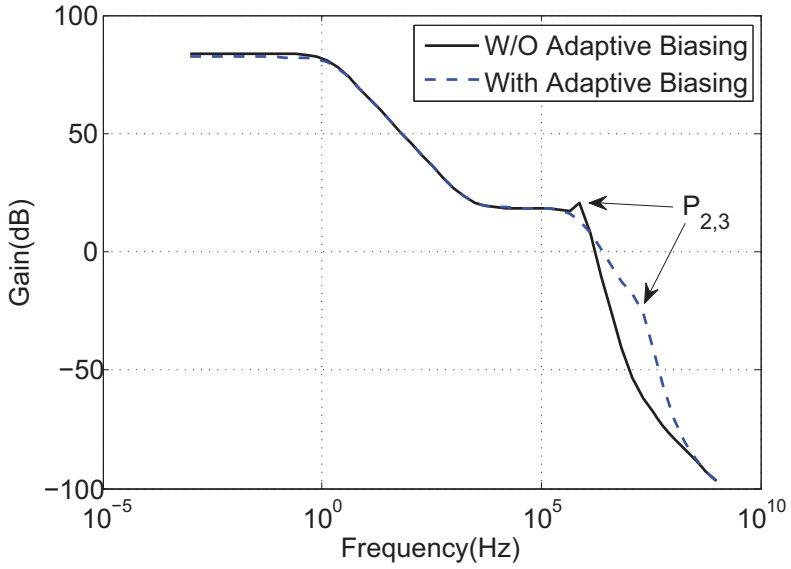

Figure 3.25: Linear regulator high current load bode plot with adaptive biasing

3.6 Over-current Protection

The linear regulator should have the over-current protection (OCP) ability to protect itself from overload current damage, because current above limitation may cause the power transistor heating up which reduces its lifetime and may result in device failure. In real applications, the over-current scenario could be caused by the over power demand from the loading circuit. In this case, the linear regulator should better be kept at some constant output current to drive the loading circuit, this feature prevents the loaded circuit from resetting if the over power demand only lasts a short period of time.

The output current I_L and the load resistance R_L relation is shown in Figure 3.26. If there is no over-current protection mechanism in the linear regulator, the load current can be very high when R_L is low (as the dashed line shows).

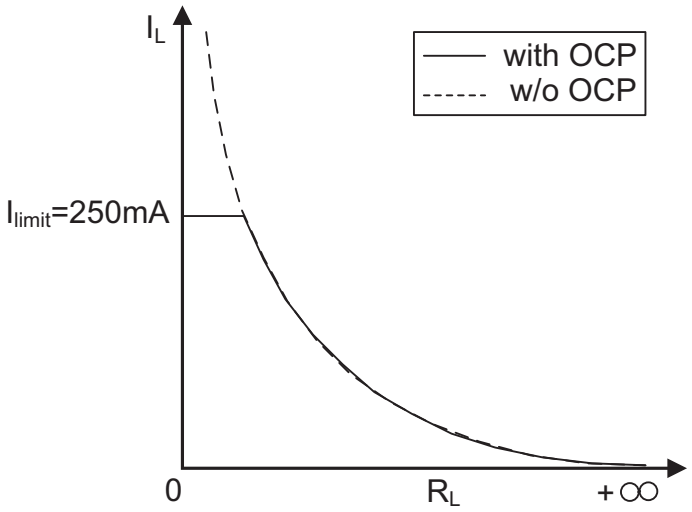

Figure 3.26: Current limitation scheme.

When the linear regulator is in OCP mode, the output voltage will linearly reduce with the load resistance. Therefore, the main voltage regulation of the loop should be disabled, or else this loop will try its best to regulate the output voltage to 5V. To disable the main regulation loop, one method has been implemented to force the input transistor into cut-off region as shown in Figure 3.27. Again, the current sensing should be added to know the exact output current value[6]. The over-current protection is able to control M_{OCP}. If the output current is below I_{limit}, current I_2 is near 0, which adds no effect on the overall loop. If the output current is higher than I_{limit}, then the over-current control circuit will increase the gate voltage of M_{OCP}, making the current of M_9 flows through M_{OCP}. Then, as the I_1 barley equals to zero, M_5 can be treated as operating in cut-off region, the main voltage regulation loop is disabled.

[6]It should be noted that the current sensing for OCP is not based on Figure 3.17, because in that figure M_{12} and M_{13} both need voltage headroom to be functional. Since V_{OUT} might be a low voltage during the current limitation, this current sensing circuit in Figure 3.17 can not work accurately

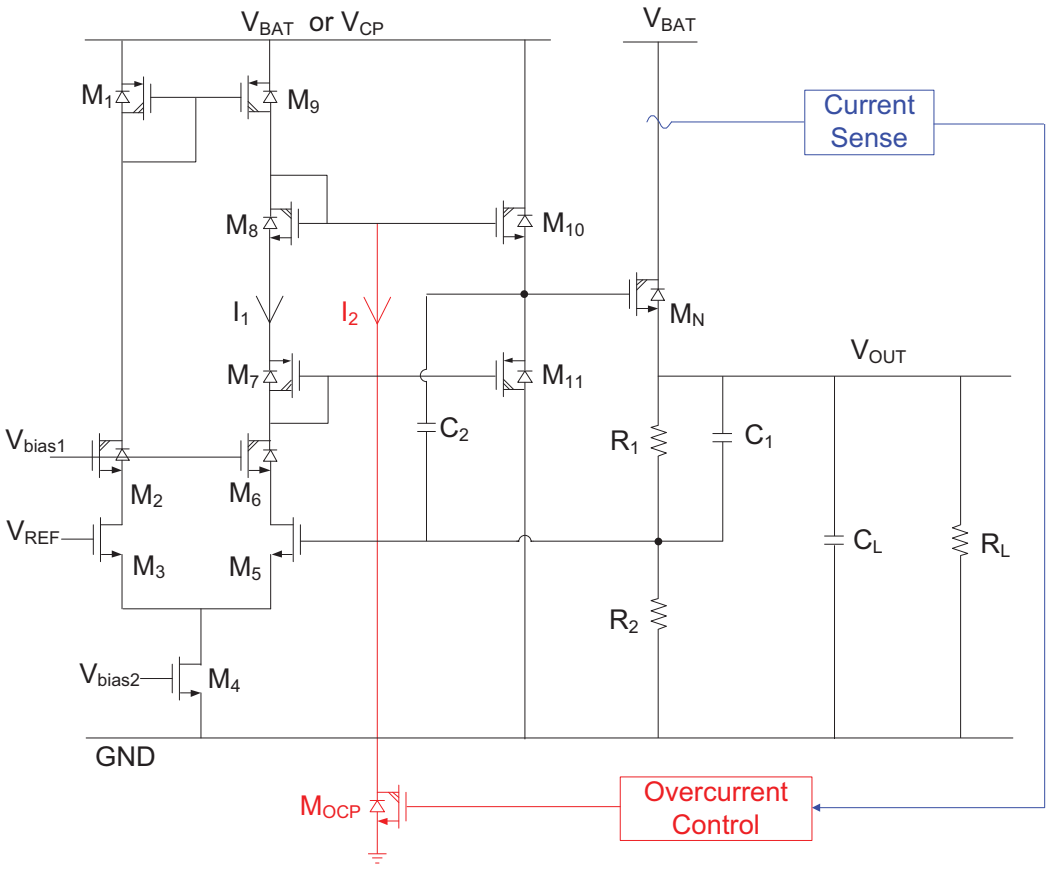

Figure 3.27: Over-current limitation.

The detailed transistor level implementation is shown in Figure 3.28. M_{15} and M_{16} form a PMOS current mirror which mirrors out the current $I_{D,N2}$ flowing through M_{N2}. M_{15} is a large transistor to ensure a small $V_{SG,15}$. M_{15}, M_{16}, M_{18} and M_{19} compose a current comparator which compares the difference between I_{D16} and I_{D18}. M_{17} is acting as a voltage clamp to make sure M_{18} and M_{19} can be low voltage transistors (providing advantage in mismatch).

Since there is DC gain in both current comparator and M_{21}, when the over-current protection circuit operates, it actually forms another regulation loop which forces input current ($I_{D,N2}$) equaling to some ratio of input current ($I_{Ref,limit}$). In this way, the output current can be regulated to a fixed I_{limit}, it is actually a current regulator being formed in over-current protection.

This current regulator has two stages of amplification, which provides a high gain to ensure the output current accuracy. The stability of this current regulation loop should be taken care of. In this design, R_5, C_4, M_{20} have been added for frequency compensation. Since M_{21} is acting as a common source amplifier, pole spitting technique is considered to be a good way to compensate this system. The additional capacitance C_4 at the gate of M_8 should be a small value, or it will introduce asymmetry for the main feedback loop.

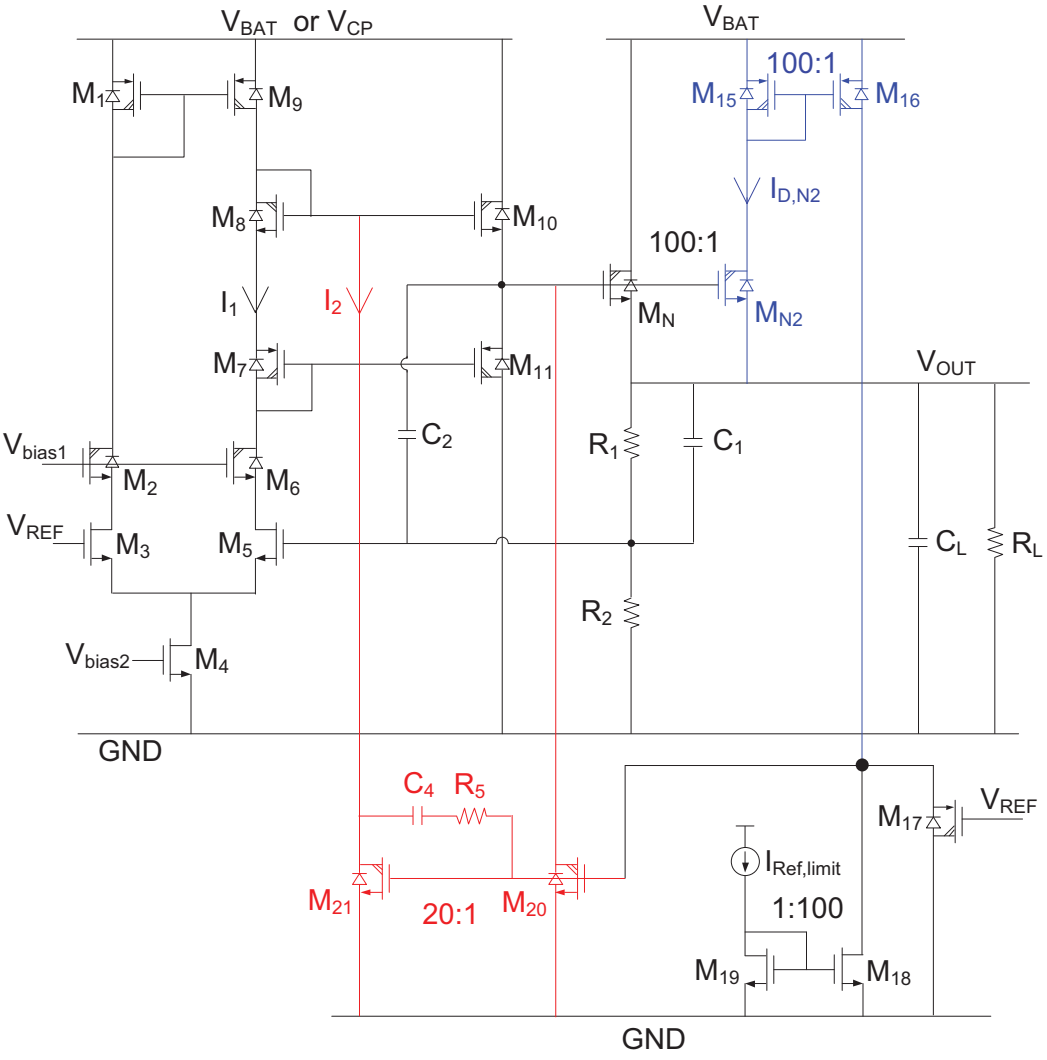

Figure 3.28: Over-current limitation schematic.

The simplified loop for stability analysis is shown in Figure 3.29. Roughly speaking, 3 poles and 2 zeros are inside the loop. It should be noted that the gate capacitance of M_N is neglected in this simplified loop for the reason that M_{20} can provide enough current bias for source follower M_{10}, then the pole at the gate of M_{N2} can be at high frequency.

Since C_4 is acting as a pole splitting capacitor, the frequency of P_8 is:

$$P_8 = -\frac{1}{2\pi(r_{o16}||r_{o18})g_{m21}(r_{o21}||r_{o9})C_4} \tag{3.38}$$

Due to the introduced capacitive feedback by C_4, P_9 is spitted into relative higher frequency. Suppose the capacitive to ground at node P_8 is roughly $C_{node8} \approx C_{gs20} + C_{gs21} + C_{db18} + C_{db16}$. Then P_9 frequency is at:

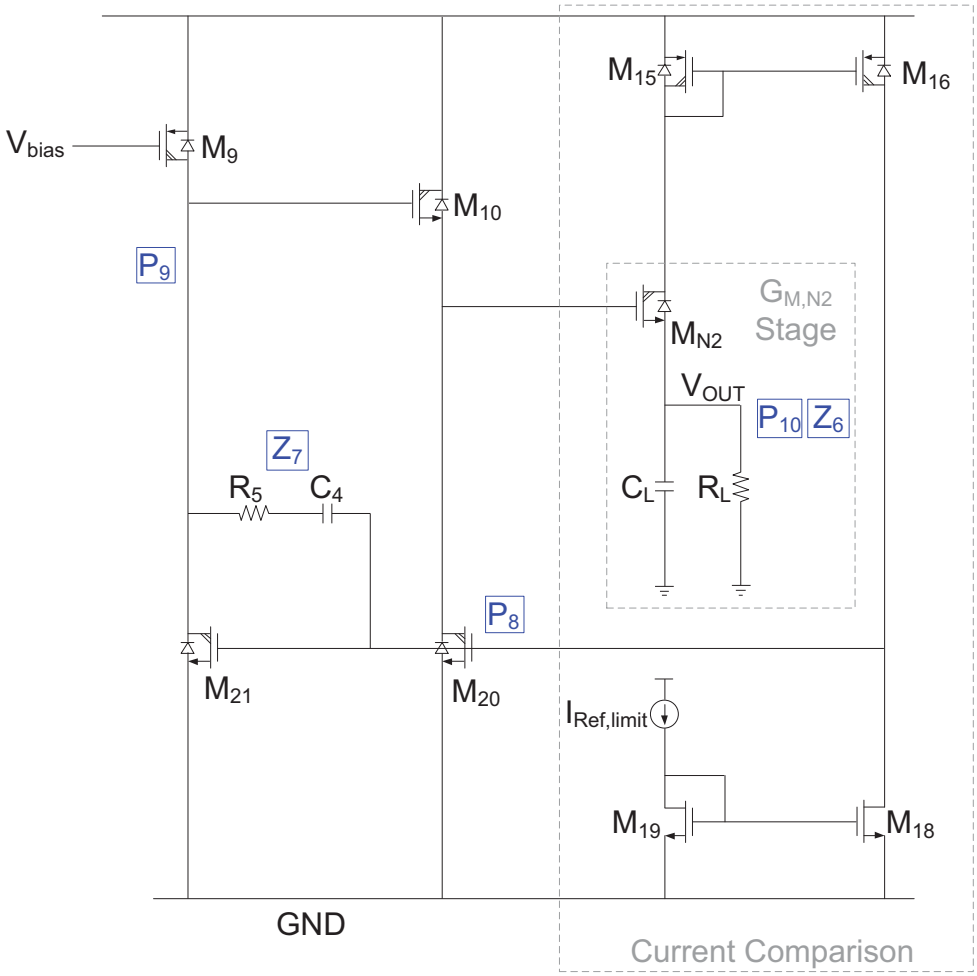

Figure 3.29: Current limitation simplified loop for stability analysis.

$$P_9 = -\frac{g_{m21}}{2\pi C_{node9}} \frac{C_4}{(C_{node8} + C_4)} \tag{3.39}$$

where $C_4/(C_{node8}+C_4)$ is the feedback factor for the capacitive feedback loop that C_4 introduced.

It is interesting to notice that M_{N2} is actually a source degenerated transconductance stage, which transfers the voltage signal into current to the current comparator input. The degeneration impedance is composed by R_L and C_L. In this way, the transconductance can be written as:

$$G_{M,N2} = \frac{g_{m,MN2}}{1 + g_{m,MN2}\dfrac{R_L}{1 + sR_LC_L}} = \frac{g_{m,MN2}(1 + sR_LC_L)}{1 + g_{m,MN2}R_L + sR_LC_L} \tag{3.40}$$

As the $G_{M,N2}$ is the proportional to the transfer function, then it results a zero Z_6 at:

$$Z_6 = -\frac{1}{2\pi R_L C_L} \tag{3.41}$$

And a pole P_{10} at:

$$P_{10} = -\frac{1 + g_{m,MN2} R_L}{2\pi R_L C_L} \tag{3.42}$$

This zero-pole pair locates at range of several kHz (e.g. R_L=10Ω, C_L=220nF will result Z_6=73kHz), it will extend the bandwidth (if the bandwidth> Z_6), which will cause instability. This problem is quite difficult to handle, because R_L is a variable which can not be decided, C_L is a fixed value. As the OCP operates, the fixed output current results $g_{m,MN2}$ is also a constant. It is true that reducing the $g_{m,MN2}$ will make the zero and pole close to each other, however, due to accurate matching requirements, the M_{N2} should be at most 100 times smaller than the main power transistor M_N, $g_{m,MN2}$ can not be reduced arbitrarily.

The resistor R_5 and capacitor C_4 generate a LHP zero to save some phase shift near the the bandwidth, which frequency is roughly at:

$$Z_7 = -\frac{1}{2\pi R_5 C_4} \tag{3.43}$$

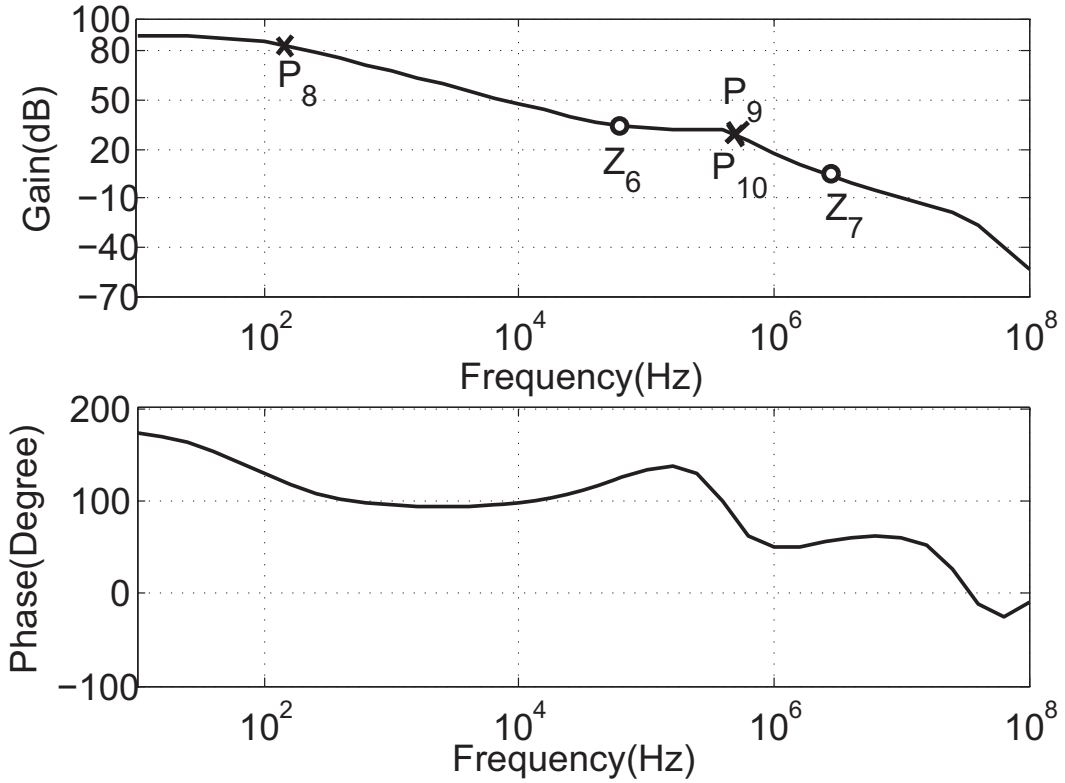

Figure 3.30: Current limitation loop bode plot (R_L=10Ω).

The bode plot of the over-current protection loop is plotted in Figure 3.30. To enable the over-current protection loop, a R_L=10Ω resistor is loaded.

The over-current loop stability over different load resistor R_L is shown in Figure 3.31. It can be found that over the resistive load, the over-current control system is stable.

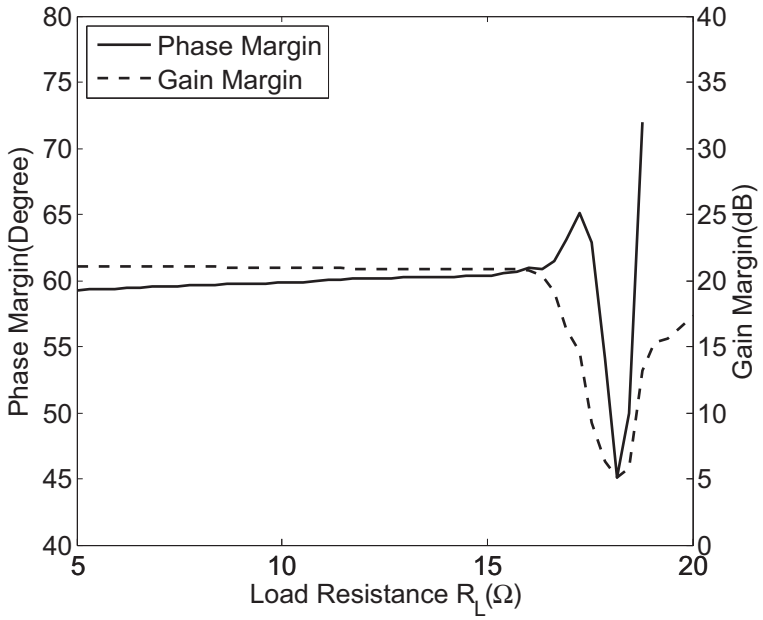

Figure 3.31: Current limitation stability over R_L.

The main voltage regulation loop bode plot in OCP mode is shown in Figure 3.32. It can be seen that as the over-current protection is enabled, the main loop gain is kept at below 0dB, which shows the main voltage regulation loop is effectively disabled.

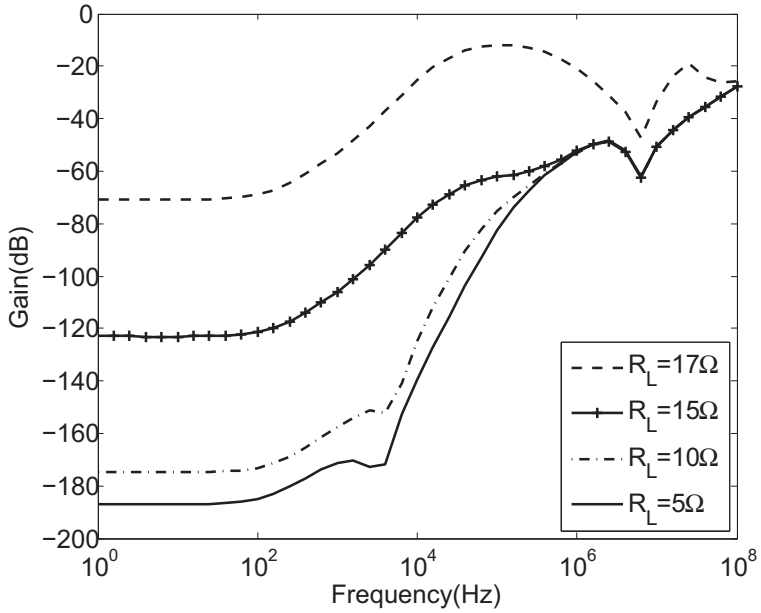

Figure 3.32: Main voltage regulation loop gain plot over R_L.

Chapter 4

Performance Evaluations

In this chapter, the performance of NMOS linear regulator will be presented and summarized. All the simulations are based on the test-benches shown in Appendix D.

4.1 Static Performance

4.1.1 Drop-out Region

From Figure 4.1, it shows that the regulator is functional around 5.2V, which makes low drop-out regulation available. It should be noted that in the low drop-out range (e.g. the battery voltage V_{BAT}<10V), the charge pump (V_{CP}) is assumed to be turned on to provide supply voltage for the op-amp.

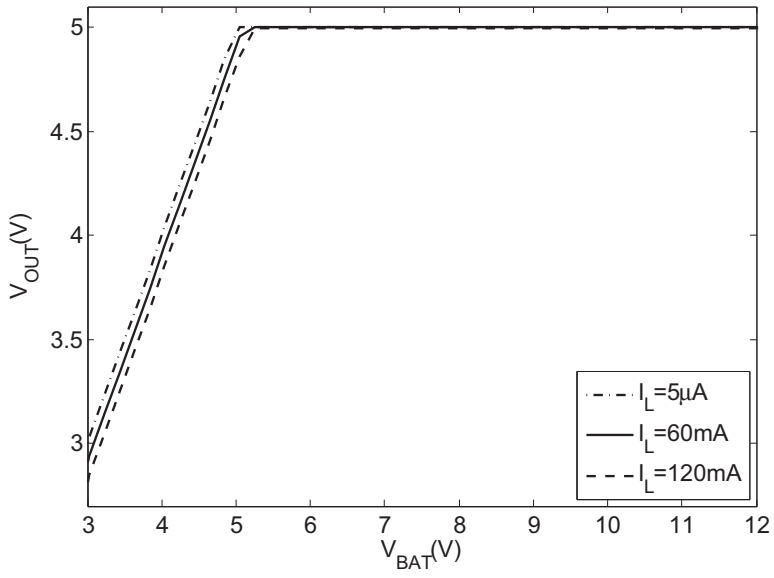

Figure 4.1: V_{OUT} versus V_{BAT} (V_{CP}=10V, typical process corner, temp=27°C).

4.1.2 Quiescent Current and Current Efficiency

The quiescent current I_q over load current I_L is plotted in Figure 4.2. When there is no load current, the quiescent current is 12μA. At full current load scenario, due to adaptive biasing I_q becomes 1.31mA. It should be noted that the band-gap circuit quiescent current is excluded in this figure.

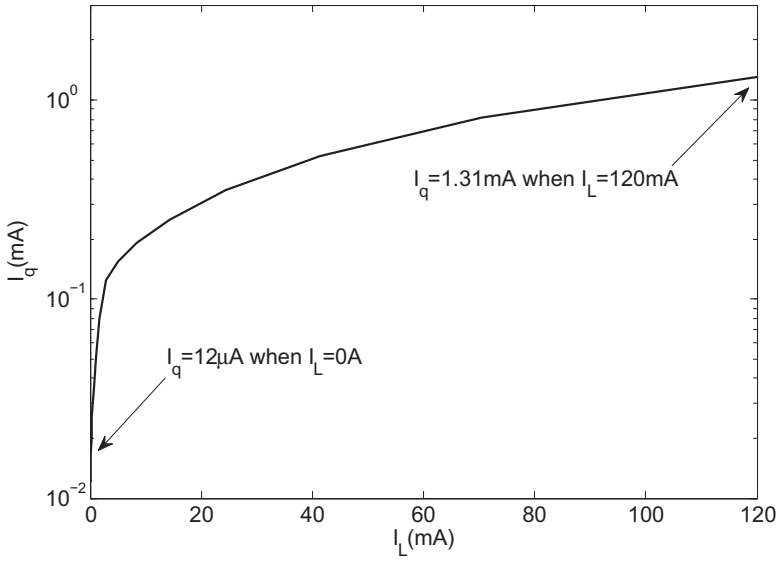

Figure 4.2: I_q versus I_L (V_{BAT}=12V, typical process corner, temp=27°C).

Since adaptive biasing scheme is used in this design, it is important to know how much the overall current efficiency (as defined in Equation 4.1) it degrades.

$$\eta_{current} = \frac{I_{load}}{I_{load} + I_q} \times 100\% \tag{4.1}$$

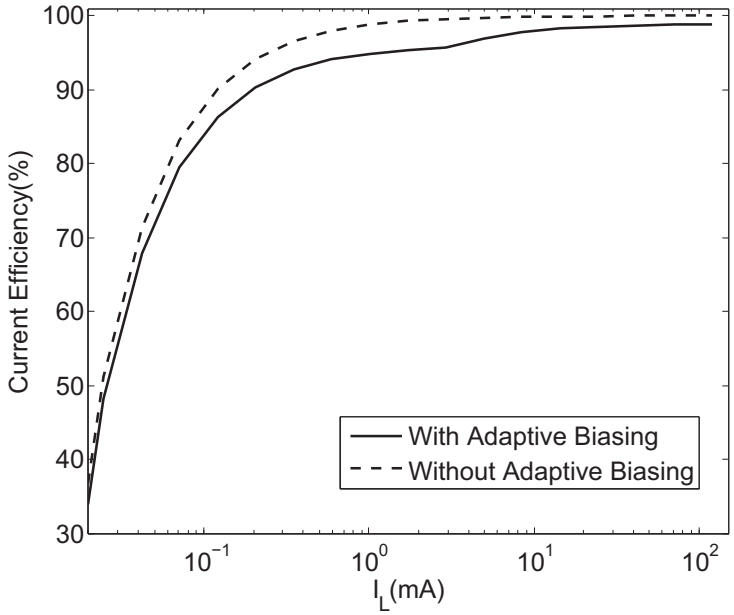

Figure 4.3: Current efficiency (V_{BAT}=12V, typical process corner, temp=27°C).

Figure 4.3 shows the current efficiency of this NMOS linear regulator. The dashed line is the current efficiency without adaptive biasing (I_q is always 12μA). It can be found that the adaptive biasing scheme degrades the current efficiency. However, the degradation is not very prominent at low current (below 0.1mA). For I_L≈3mA, the maximum degradation happens due to the biasing current for the op-amp reaches its maximum (as shown in Figure 3.23), it only reduces this efficiency by 4%. At high current load, the majority of I_q is contributed by the 100:1 current mirror in the current sensing circuit, the degradation of the efficiency is around 1%.

4.1.3 Static Output Voltage Accuracy

The static output voltage accuracy of the linear regulator is presented in this subsection. Figure 4.4 shows the line regulation performance. The line regulation ability is enhanced by the intrinsic gain of NMOS power transistor as expressed in Equation 2.7, which makes the output voltage quite accurate in response to different battery voltages.

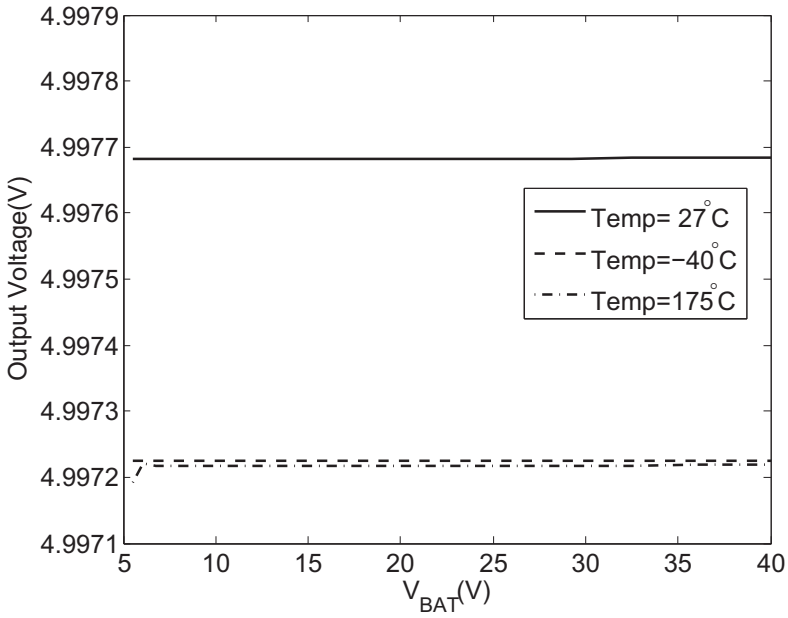

Figure 4.4: Static line regulation (I_L=120mA, typical process corner).

Figure 4.5 shows the load regulation performance. The output voltage becomes more inaccurate as the load current increases. There are two reasons for this inaccuracy, one is as the current goes up, voltage drop on the modeled 25mΩ bond-wire parasitic resistor will increase (e.g. 25mΩ×120mA=3mV). The other is the DC gain of the loop decreases as I_L increases (Equation 2.11). However, the gain reduction is not prominent as shown in Figure 3.25. From Figure 4.5, the maximum inaccuracy is around 3mV, this is mostly contributed by the bond-wire resistance voltage drop.

In practical cases, the mismatch between transistors and passive components also contribute to the output voltage inaccuracy. Figure 4.6 shows the monte-carlo sim-

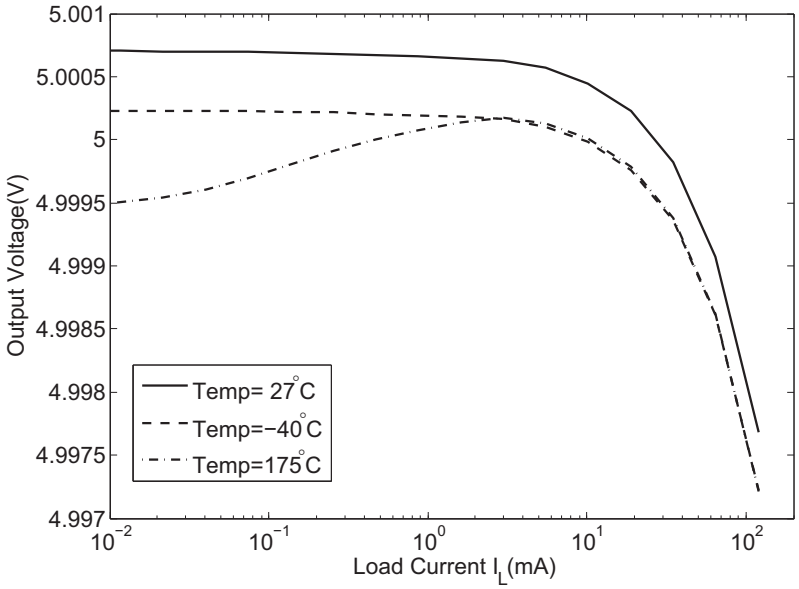

Figure 4.5: Static load regulation(V_{BAT}=12V, typical process corner).

ulation results of the output voltage over all process corners and temperature range. One standard deviation (σ) of output voltage is 11.4mV, for $\pm 3\sigma$ range, the output voltage will spread $\pm$34.2mV. This inaccuracy can be solved by trimming of the feedback resistors during the chip fabrication.

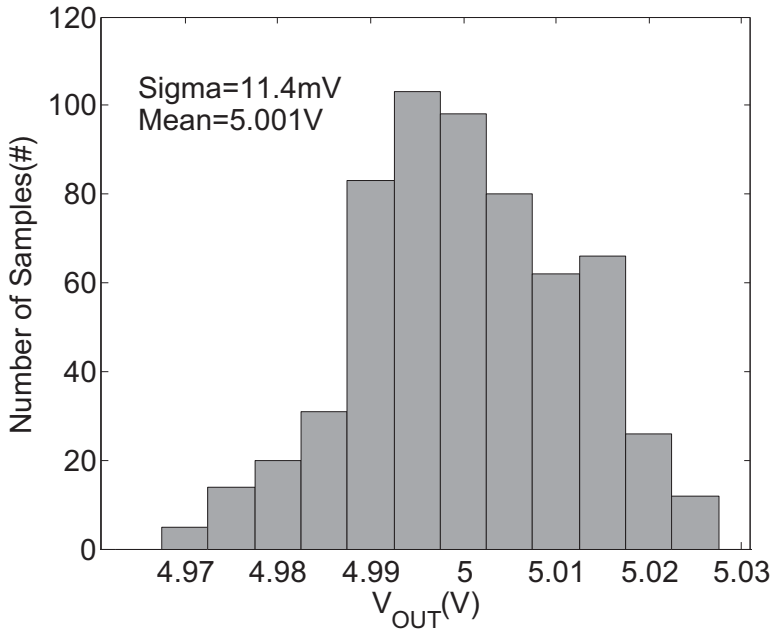

Figure 4.6: Ouput voltage spread (V_{BAT}=12V,I_L=0,-40°C$\sim$175°C).

4.2 AC Performance

The main voltage regulation open-loop bode plot over different load current is shown in Figure 4.7. As the load current increasing, the output pole is moving to higher frequency. Owing to the added zero and adaptive biasing scheme, the system stability can be ensured.

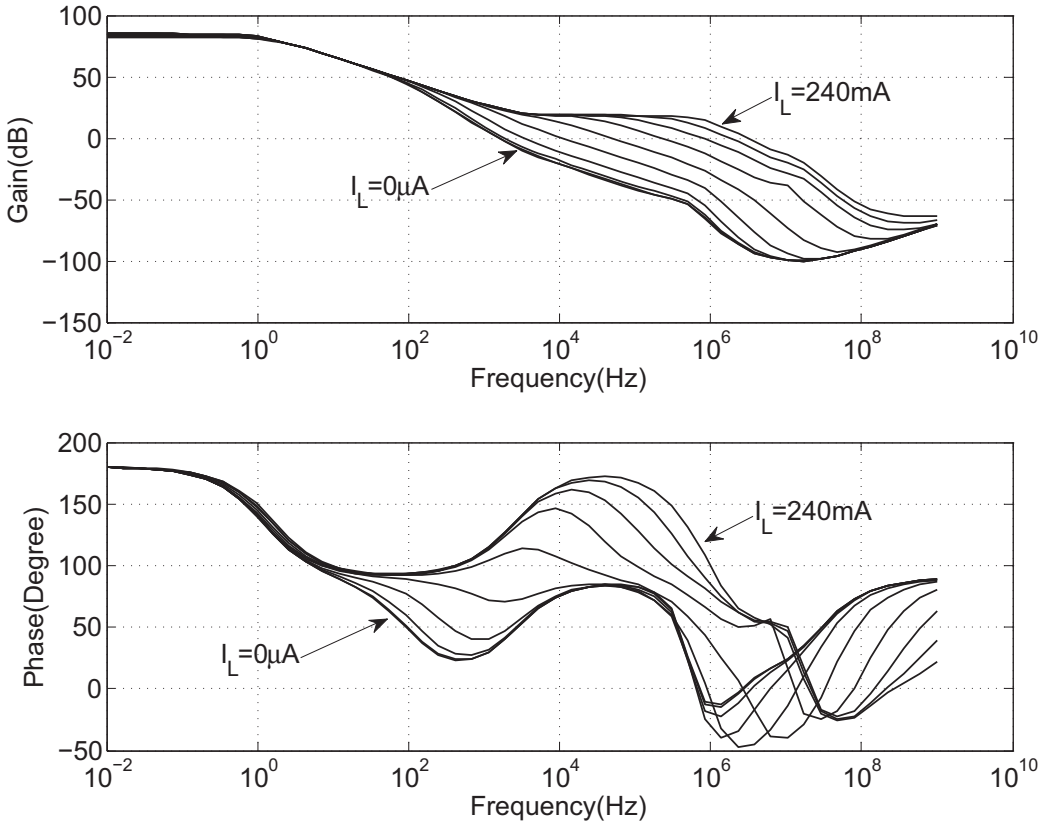

Figure 4.7: Bode plot over different I_L.

The phase and gain margin is shown in Figure 4.8. It shows that at zero load current the phase margin is around 35°. However, as the load current increases to around 10μA, the phase margin is above 45°. It should be noted that although the system shows under-damped behavior (for the phase margin is low) in low load current range, the regulator output voltage variation due to load response in this range is not critical. The reason for that is small current variation can be immediately compensated by the charge stored on the large external capacitor.

The bandwidth of the overall loop is shown in Figure 4.9. The bandwidth is increased with the load current I_L, which meets the expectation in Section 3.4.3. This increased bandwidth will reduce the loop response time, which improves the transient performance of linear regulator.

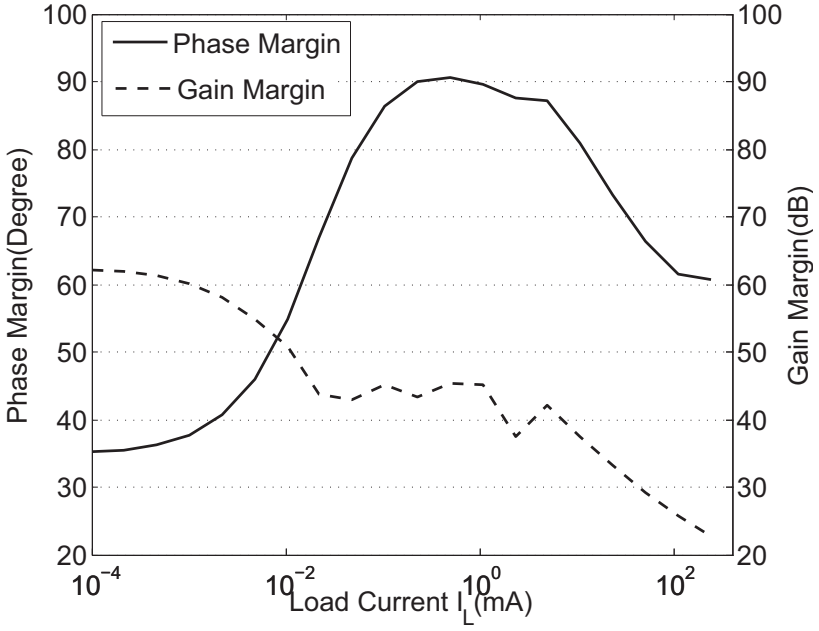

Figure 4.8: Phase and gain margin versus I_L

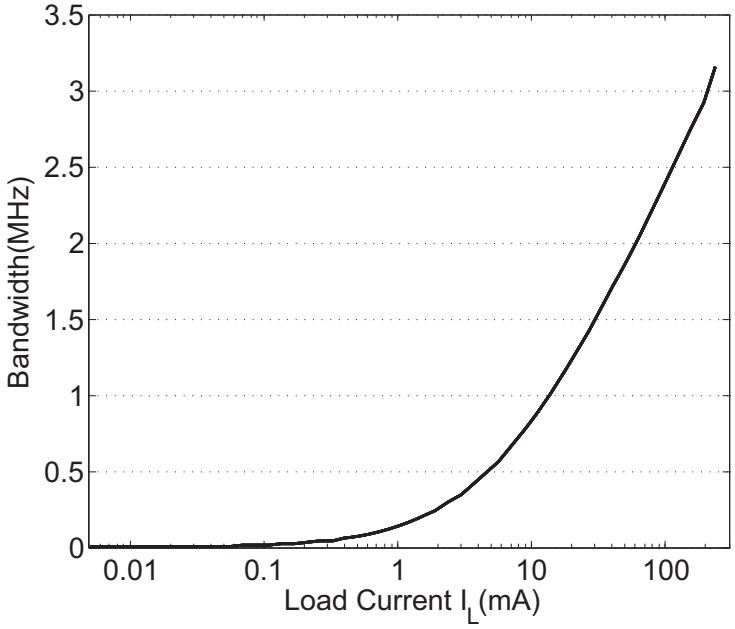

Figure 4.9: Bandwidth versus I_L.

4.3 Dynamic Performance

4.3.1 Line Transient Response

The low battery line transient response is shown in Figure 4.10. In this test-case, the supply voltage of op-amp is 10V (the charge pump is ON). The dashed line shows the $\pm 3\sigma$ range of the V_{OUT} during the line transient variation. This $\pm 3\sigma$ range in this

section means over the full temperature range (-40°C∼175°C), with process corners and mismatch included, 99.97% samples will have the output variation within the dashed range.

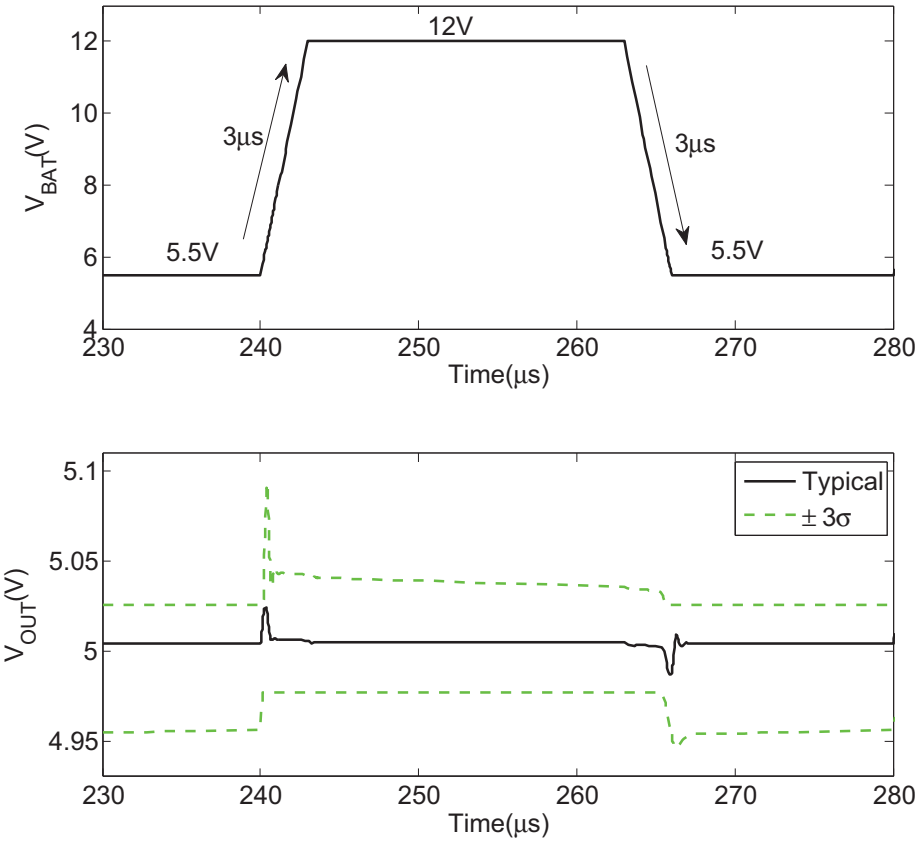

Figure 4.10: Low battery line transient response (I_L=120mA, -40°C∼175°C).

The high voltage line transient response is shown in Figure 4.11. It can be seen that as the NMOS power transistor goes into saturation region, the V_{BAT} transient variation on V_{OUT} is greatly reduced.

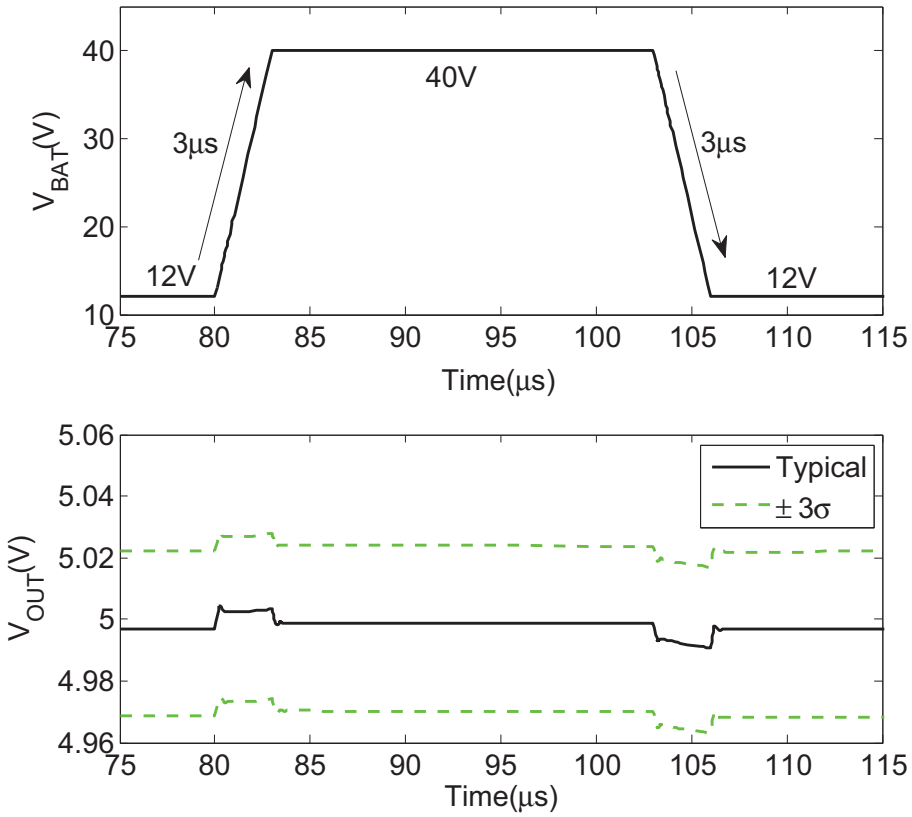

Figure 4.11: High battery line transient response(I_L=120mA, -40°C∼175°C).

4.3.2 Load Transient Response

The load transient response for V_{BAT}=12V is shown in Figure 4.12. It can be found that for a typical process corner (temp=27°C, no mismatch and process corners), the V_{OUT} variation is around ±50mV. For ±3σ range, the output voltage can vary around ±100mV.

From Figure 4.8, in low load current region, the system shows under-damped characteristic. It is necessary to check if this region gives any critical under-damp behavior to the feedback system. The V_{OUT} variation in response to I_L varies from 0 to 100μA in 100ns is shown in Figure 4.13. It can be seen that there is a little under-damped behavior showing up, however, the amplitude of output voltage variation is not prominent due to low I_L.

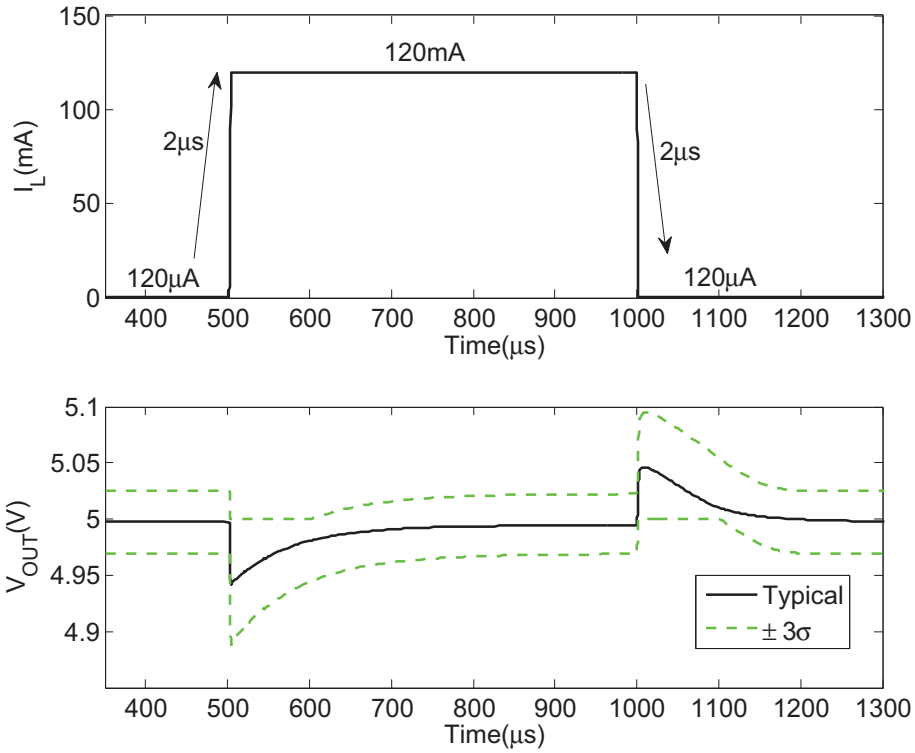

Figure 4.12: Load transient response (V_{BAT}=12V,-40°C∼175°C).

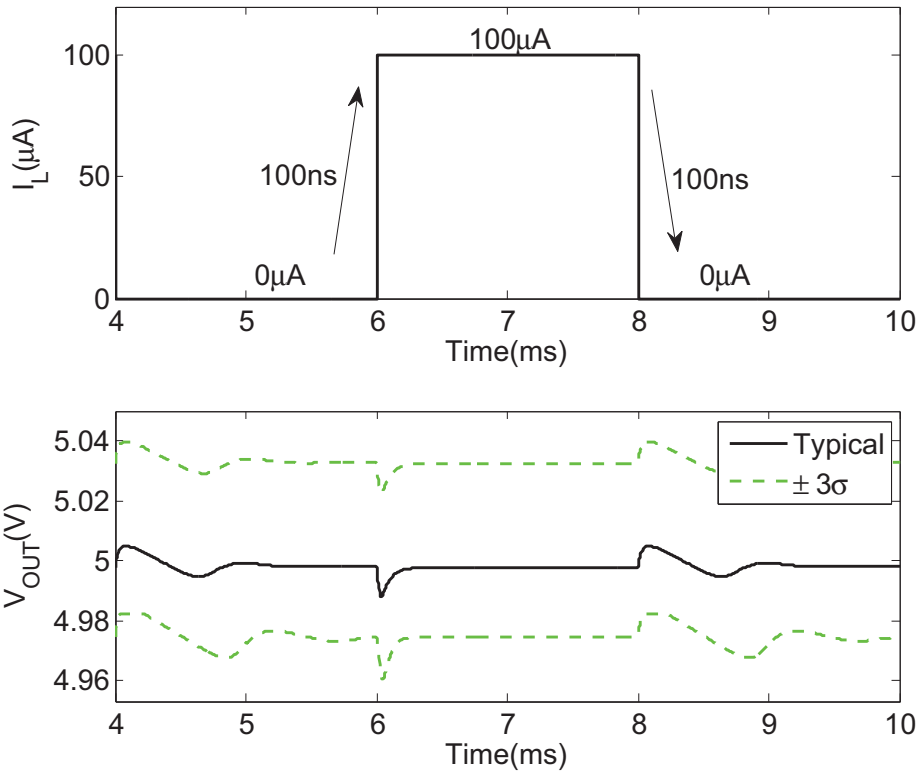

Figure 4.13: Low current load transient response (V_{BAT}=12V,-40°C∼175°C).

To make the test-bench match practical load current behavior better, a staircase load current is applied to this regulator. The output voltage variation is shown in Figure 4.14.

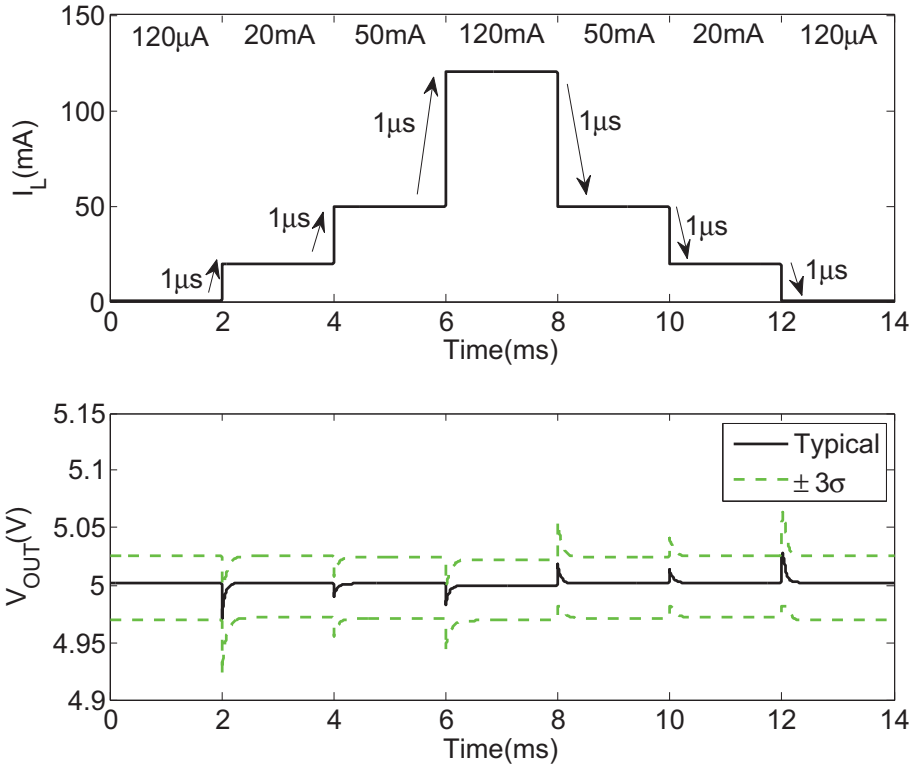

Figure 4.14: Staircase load transient response (V_{BAT}=12V,-40°C∼175°C).

It should be noted that in some transient test-cases, the required minimum I_L is from zero to some high current load. To deal with this case, a current sink path should be designed. This is discussed in Appendix E.

4.4 High Frequency Performance

4.4.1 Power Supply Rejection

The power supply rejection is shown in Figure 4.15. The PSRR is around 63dB at 100kHz. The worst case for PSRR is around 37dB.

4.4.2 Output Noise

The output noise of this linear regulator is shown in Figure 4.16. The integrated noise from 1Hz to 1MHz is 66.4μV_{RMS}. The low frequency noise is mainly contributed by the resistive divider thermal noise and $1/f$ noise of the input pair transistors. As frequency goes higher, the output capacitor also plays a role to attenuate the total noise.

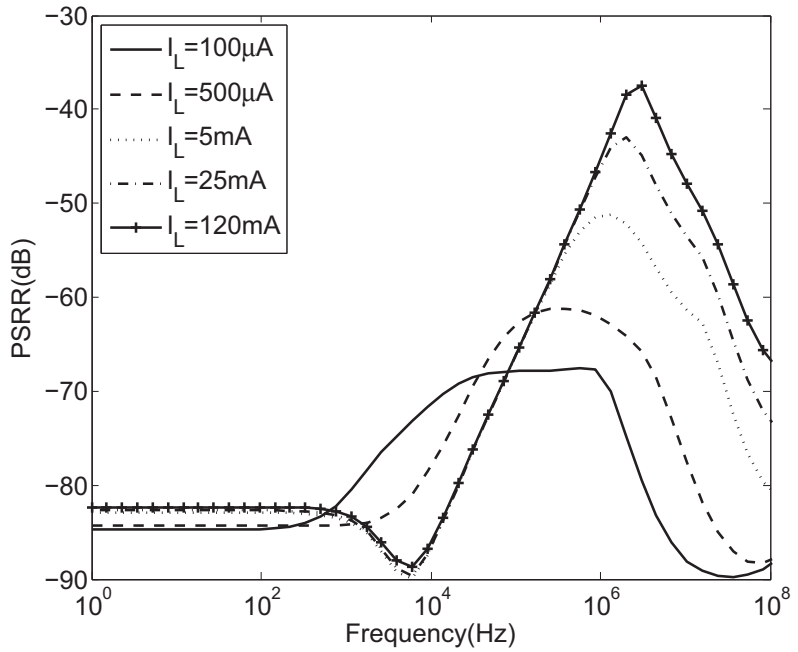

Figure 4.15: PSRR over I_L (V_{BAT}=12V,typical process corner, 27°C).

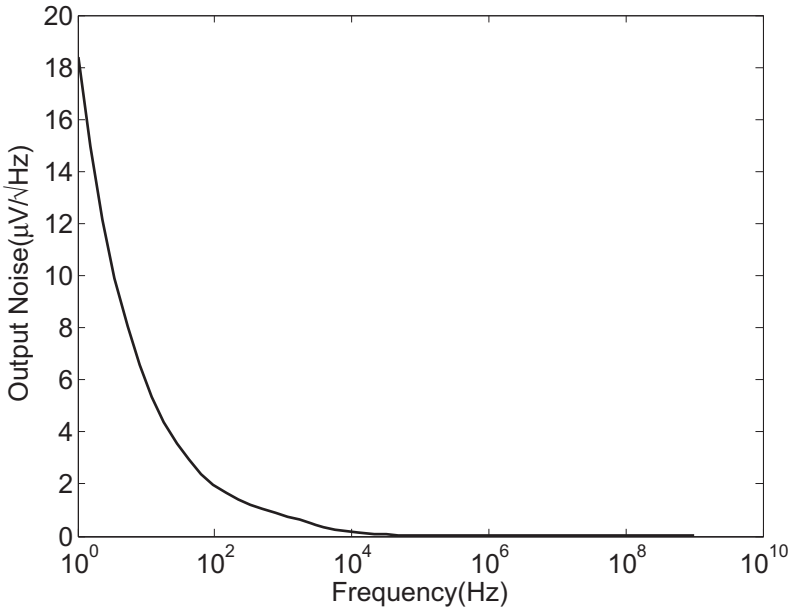

Figure 4.16: Output noise (I_L=20mA,typical process corner, 27°C).

4.5 Over-current Protection Performance

The static load current I_L versus load resistor R_L plot is shown in Figure 4.17. This plot meets the expectation shown in Figure 3.26. It can be seen that the limitation current level can vary with temperature.

The test-bench of the over-current limitation is shown in Appendix D. The output

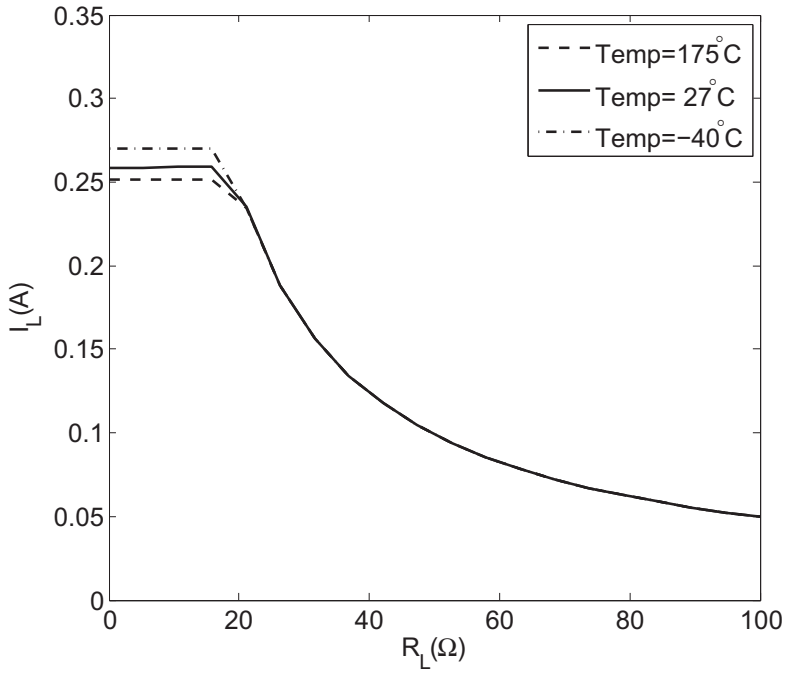

Figure 4.17: I_L versus R_L (V_{BAT}=12V, typical process corner).

resistance is periodically varies from 50Ω to 10Ω with 2μs transition time (Figure D.2). If the over-current protection is not functional, this will lead to the output current variation from 100mA to near 500mA. Figure 4.18 shows the effectiveness of the over-current protection. The load current is kept around 250mA when 10Ω is loaded. Due to the bandwidth limitation, the current can beyond the limitation at the very beginning of the output resistance reduction (e.g. from 50Ω to 10Ω). The protection circuit will regulate the output current to 250mA within 10μs.

It can be found that the regulating current has some spread (from 221mA to 320mA), this is mainly caused by the current mirror error of M_{18} and M_{19} in Figure 3.28. In order to save the quiescent current, $I_{Ref,limit}$ should be low (250nA in this design). Therefore a large current mirror ratio should be used. The low current drives this two transistors in weak inversion region where the (V_{GS}-V_{TH})-I_D has an exponential relation, this makes the current mirror more inaccurate due to V_{TH} mismatch.

4.6 Overall Performance Summary

Table 4.1 shows the overall performance summary of this NMOS linear regulator.

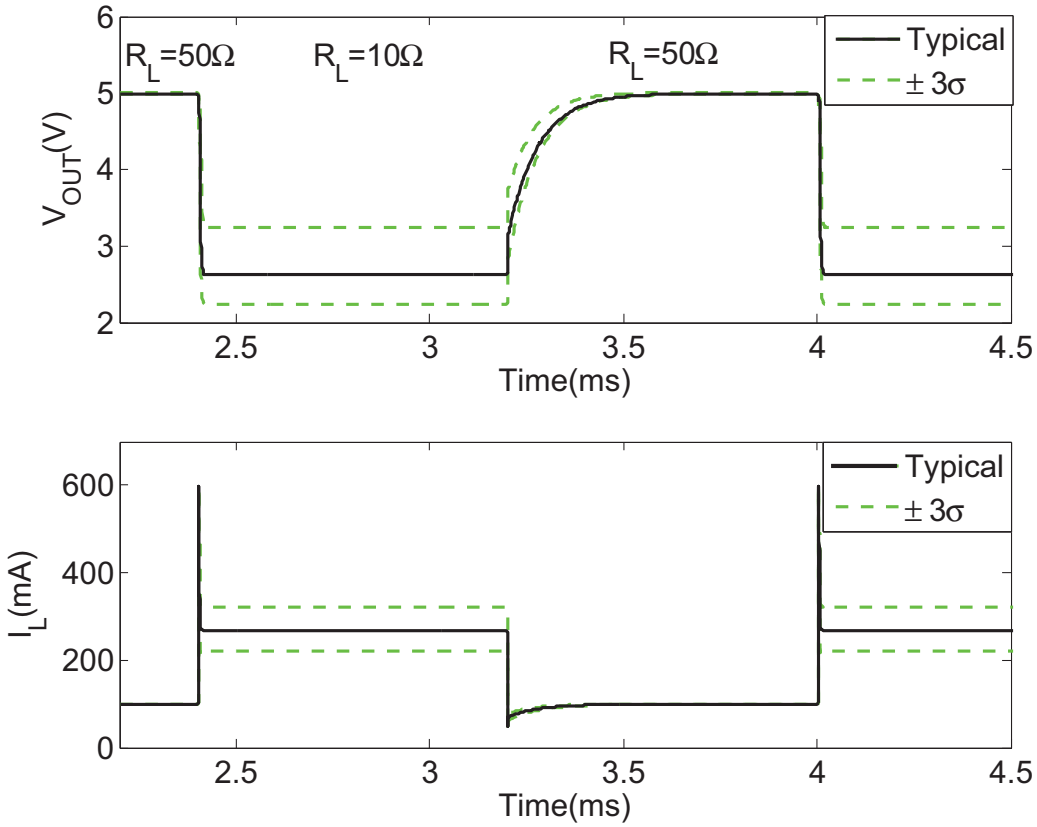

Figure 4.18: Over-current protection transient behavior (V_{BAT}=12V,-40°C∼175°C).

Table 4.1: Overall NMOS Linear Regulator Performance Summary

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Regulator Input Voltage	5.5	–	40	V
V_{OUT}	Output Voltage	4.9	5.0	5.1	V
ΔV_{out_load}	Dynamic Load Regulation	-2	-	+2	%
$t_{stabilized}$	Output Voltage Within 0.5% After Load Step	-	-	1	ms
ΔV_{out_line}	Dynamic Supply Regulation	-2	-	+2	%
I_q	Quiescent Current(I_L=0, w/o band-gap)	–	12	–	μA
PSRR	Power Suplly Rejection@100kHz	–	63	–	dB
V_{noise}	Output Noise	–	66.4	–	μV_{RMS}
C_L	External Capacitance	–	220	–	nF

Chapter 5

Scaling Features

As the NMOS linear regulator is already designed, the scaling abilities on external capacitance and maximum load current should be investigated. In this chapter, the possible scaling features on this NMOS linear regulator will be discussed.

5.1 External Capacitor Scaling

In this design, the typical value of the external load capacitor C_L is 220nF. More C_L values are also acceptable. From Figure 3.13, the low load current stability might be degraded by the large output capacitor (moving f_{P4} lower), however, this degradation can be tolerable. As we discussed, even the low phase margin at low current load makes the system under-damped, it can be easily compensated by the charge stored at the output capacitor, which may not result big output voltage variation.

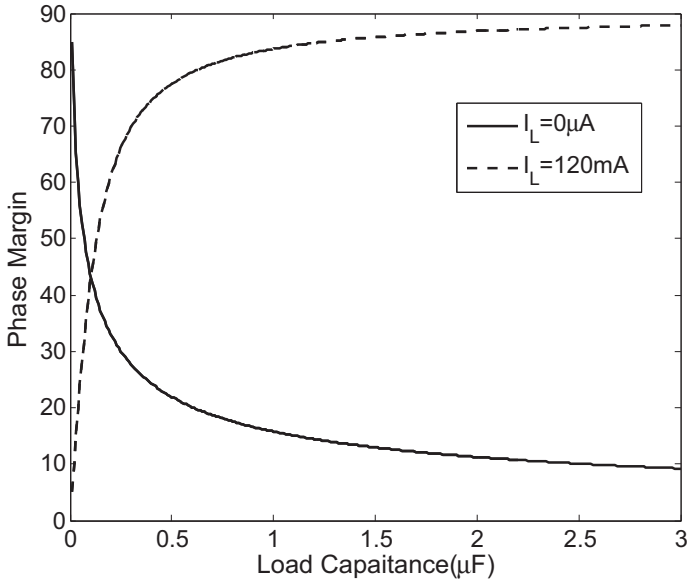

Figure 5.1: Phase margin among output capacitor sizing range.

The calculated phase margin over different C_L is plotted in Figure 5.1. Clearly, there is a trade-off between high current load and low current load stability. To be

specific, when C_L is low (e.g. less than 60nF), at high current load, the phase margin is only around 30°. This under-damped behavior at high load current will result large output voltage variation. When C_L is high (e.g. greater than 1μF), at low load current, the phase margin is around 15°.

In this design, the $P_{2,3}$ is around 10MHz at maximum current load. If the linear regulator maximum bandwidth is near this frequency at high load current, the system is instable. Figure 5.2 shows the expected bandwidth over C_L. At C_L≈20nF, the expected bandwidth is at 10MHz, the whole system is quite under-damped which is risky to define the linear regulator with this C_L value. Therefore, the C_L with at least 20nF is required for stability.

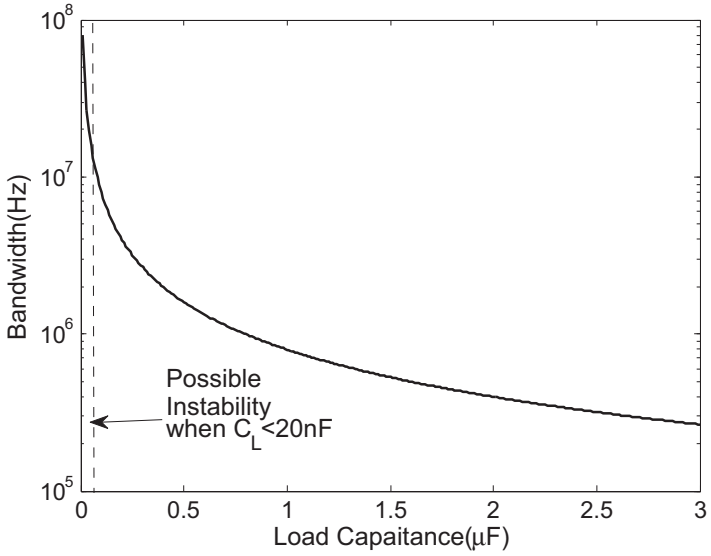

Figure 5.2: Bandwidth at high current load over C_L.

To further investigate the impact of different C_L value on the transient behavior, several C_L values are chosen for the load transient simulation. The V_{OUT} variation for I_L goes from low to high is shown in Figure 5.3. It can be seen that the different C_L resulting different damping behavior of V_{OUT}. Lower C_L makes the phase margin lower, the system becomes more under-damped as shown in C_L=100nF curve. For large C_L, the system is over damped, the reaction time becomes much longer as shown in the C_L=2.2μF curve.

The load transient behavior for I_L varying from high to low over different C_L is shown in Figure 5.4. Higher C_L value will make the V_{OUT} overshoot smaller, but due to the larger capacitance, the V_{OUT} needs more time to decrease to nominal output voltage (5V).

It should be noted that normally a larger C_L will result in a better transient response for a lower linear voltage regulator. However, in this design the C_L is inversely proportional to the bandwidth, if C_L is increased, the reduced loop speed will also degrade the transient performance. From Figure 5.3 and Figure 5.4, increasing C_L from 100nF to 2.2μF only improved V_{OUT} variation by ±7mV approximately.

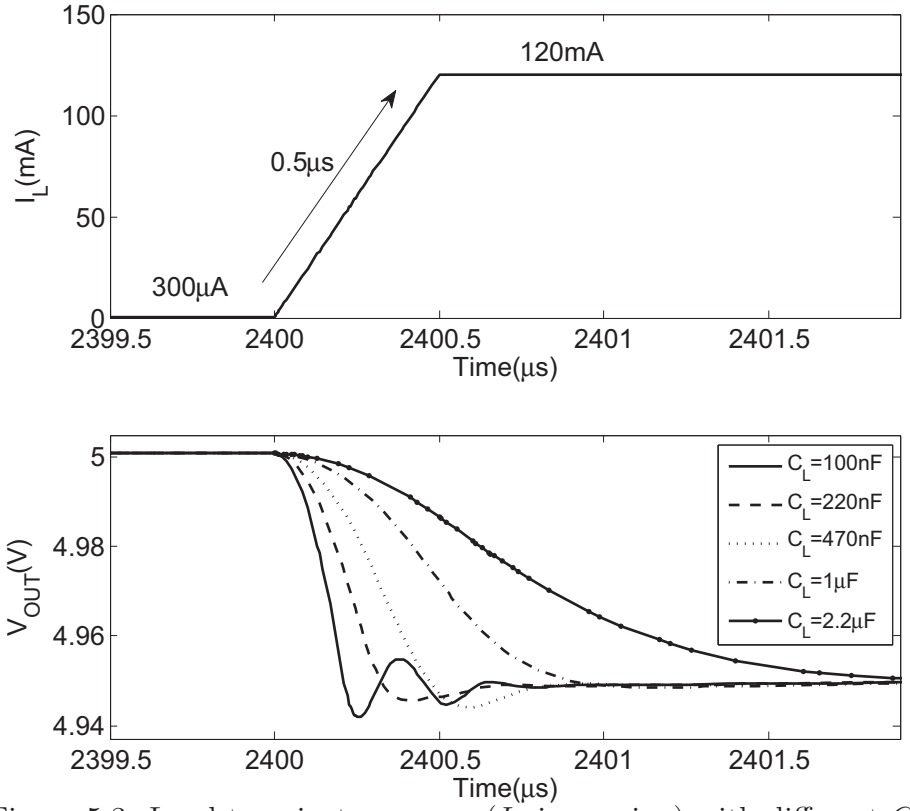

Figure 5.3: Load transient response (I_L increasing) with different C_L.

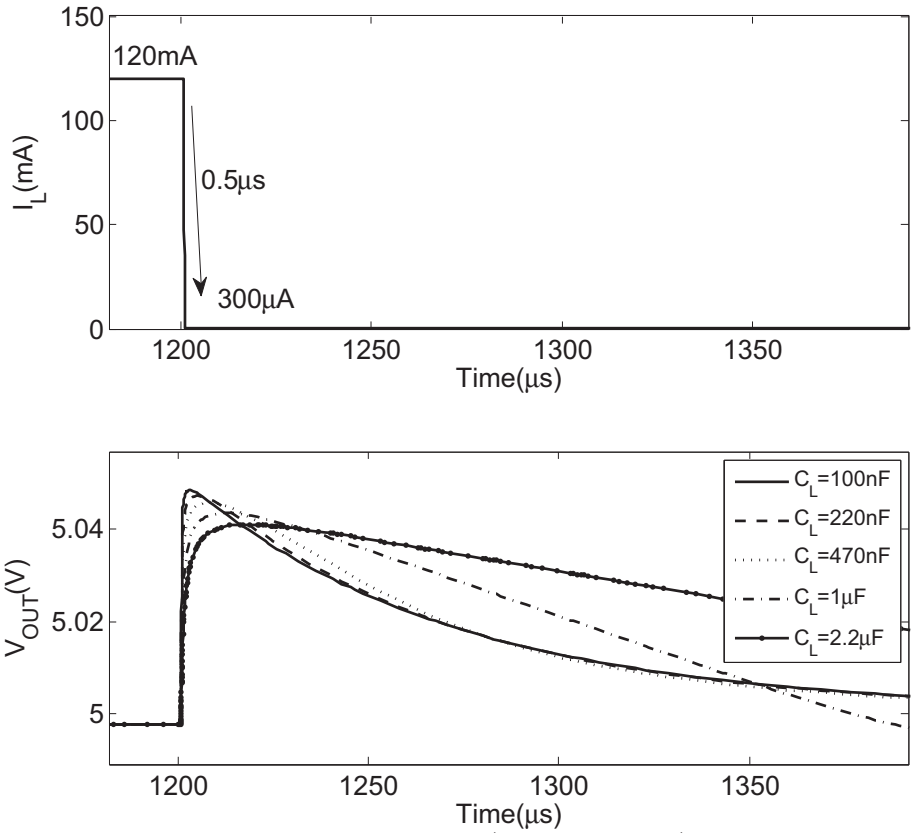

Figure 5.4: Load transient response (I_L decreasing) with different C_L.

5.2 Load Current Scaling

In this design, the typical maximum output current is 120mA. The load current can also be scalable. To scale the current, the first consideration is power transistor sizing. From Section 3.1, the minimum of the transistor size is determined by the linear region R_{DS} resistance of the power transistor. As the maximum load current increasing/decreasing n times, the R_{DS} should be reduced/increased by n times, which leads to the size of power transistor increase/decrease by n times.

The second thing to check is the effect on main loop stability when scaling maximum I_L. First, the high current load bandwidth is proportional to the transconductance of power transistor $g_{m,MN}$. Since the size of the power transistor has changed by n times, the $g_{m,MN}$ is changed by n times, as expressed in Equation 5.1.

$$g_{m,MN} = \sqrt{2\mu_n C_{ox}\frac{nW}{L}nI_L} = n\sqrt{2\mu_n C_{ox}\frac{W}{L}I_L} \tag{5.1}$$

To roughly keep the same bandwidth to ensure the stability at high current load, based on Equation 3.34, C_L can be tuned to accommodate the $g_{m,MN}$ scaling. This means C_L should also be n times in response to nI_L.

For power transistor changes by n times, the C_{gate} also changes by n times. If $n > 1$, $P_{2,3}$ (Table 3.2) will move to a lower frequency. This means even the maximum bandwidth is kept at the same, there is still a potential instability risk. $P_{2,3}$ can be kept at the same frequency during scaling by changing $g_{m,BUF}$ by n times. This can be done by providing a n^2 times adaptive biasing current.

For the low current load stability, it is a pity that $g_{m,MN}$ at low current load does not scale with transistor size as analyzed in Equation 3.1. To keep the same phase margin at low current load (Equation 3.32), the quiescent current flow through power transistor at low current load should be changed by n times to accommodate the modified n times C_L.[1]

To make the factor n into practical values, possible I_L scaling factors are summarized in Table 5.1. It should be noted that these values are only leading to a functional (stable) linear regulator, there is still much room for optimization. Different trade-offs can be made for specific applications.

Table 5.1: Load Current Scaling

Scaling Factor	I_L	C_L	Max $I_{dyn.bias}$	I_q@I_L=0A
n=0.42	50mA	100nF	11μA	9.5μA
n=1	120mA	220nF	65μA	12μA
n=2.1	250mA	470nF	286μA	17.5μA
n=4.2	500mA	1μF	1.2mA	26μA
n=8.4	1A	2.2μF	4.6mA	47μA

The linear regulator in this design is scaled up to maximum 1A current load based on Tablet 5.1. The load transient behavior is shown in Figure 5.5. It can be seen

[1] In this design, the quiescent current flow through power transistor is 5μA when I_L=0.

that the linear regulator is stable and shows no under-damp behavior. The bond-wire resistance will contribute a lot on voltage drop at high current load (around 1A×25mΩ=25mV).

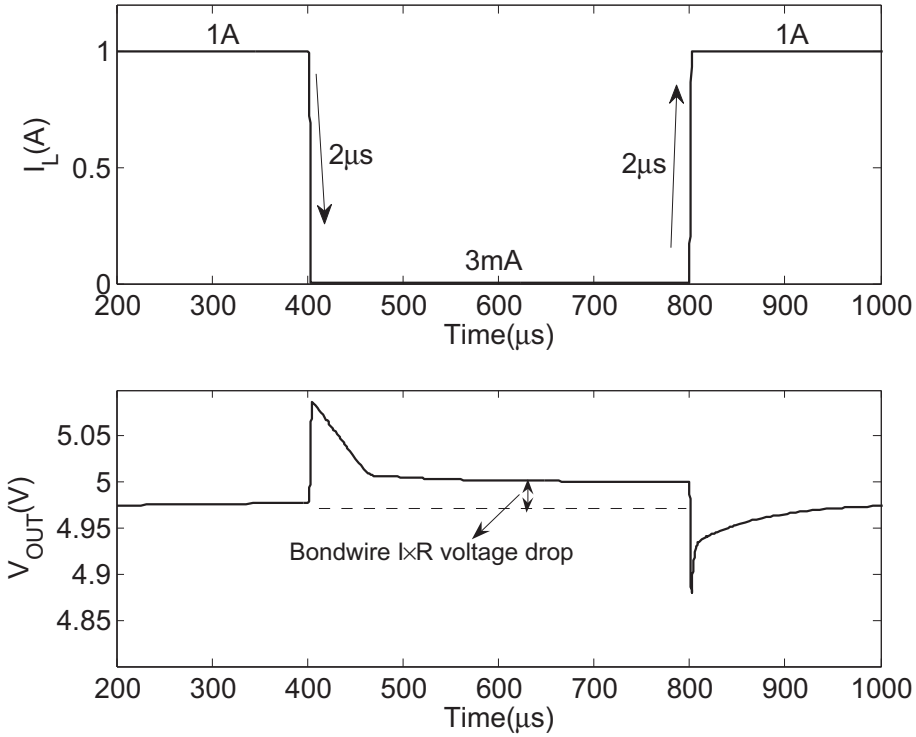

Figure 5.5: A 1A linear regulator load transient response.

Chapter 6

Conclusions and Future Work

In this thesis, a NMOS linear regulator is presented. The small signal behavior of the regulation loop has been accurately modeled. Based on the small signal model, a frequency compensation scheme which can generate a zero without being troubled by its associated pole is proposed. The effectiveness of the compensation is verified by both calculation and simulation.

This NMOS linear regulator is able to keep $\pm 2\%$ output voltage accuracy within -40°C$\sim$175°C. With the implementation of adaptive biasing, the quiescent current of this linear regulator can vary from 12μA to 1.31mA, the current efficiency is only degraded within 4%. Owing to the proposed frequency compensation scheme, this regulator can achieve a maximum 3MHz bandwidth. Compared to the PMOS linear regulator counterpart, the power transistor area can be decreased by 3 times, the output external capacitor can be reduced from 2.2μF to 220nF without sacrificing the performance.

Due to the time limit, measurement results of this NMOS linear regulator test-chip is not included in this thesis. Beside the silicon verification of this work, from design point of view, the future work can be done in four aspects: (1) designing an area-efficient charge pump which has an output current ability around 200μA; (2) designing a low battery sensing circuit which can enable/disable the charge pump; (3) adding short circuit protections, over-voltage protections (e.g. V_{GS} protection) and ESD protections; (4) trimming can be implemented on the feedback resistors R_1 and R_2 to minimize the output voltage spread.

Appendix A

Method for Simplifying the Transfer Function

The expected simplified equation in the numerator or denominator of a transfer function for pole zero calculation is as Equation A.1, where a, b, c are symbolic or numerical terms, where s is Laplace variable.

$$(1+as)(1+bs)(1+cs)=0 \tag{A.1}$$

Assume a, b, c are real, another expression of Equation A.1 is:

$$\underbrace{abc}_{p}s^3+\underbrace{(ab+bc+ac)}_{q}s^2+\underbrace{(a+b+c)}_{t}s+1=0 \tag{A.2}$$

Equation A.2 is the form that Matlab transfer function solution are given (with the calculated symbolic value p, q, t). If the p, q, t are are already known, it is possible to solve solutions of a, b, c.

Assume $a \ll b \ll c$, we have:

$$t=a+b+c\approx c \tag{A.3}$$

Since c is the largest term, which will result the lowest frequency pole or zero (the dominate one).

Also, p and q have a relation:

$$\frac{q}{p}=\frac{ab+bc+ac}{abc}=\frac{1}{a}+\frac{1}{b}+\frac{1}{c}\approx\frac{1}{a} \tag{A.4}$$

which is:

$$a\approx\frac{p}{q} \tag{A.5}$$

a is smallest term, which is actually the highest frequency pole or zero (the least dominate one).

The intermediate term b can be found as:

$$p = abc \tag{A.6}$$

Substituting a and c solutions into Equation A.7, then:

$$b = \frac{p}{ac} = \frac{q}{t} \tag{A.7}$$

Therefore, if the p, q, t of a third order system are given, it is easy to roughly calculate its separated solutions of a, b, c. It should be noted that this calculation is only on the assumption that a, b, c are real and widely separated. In cases that a, b, c are near each other and/or complex numbers, this simplification method will be inaccurate.

Appendix B

The Overall Transfer Function Calculation

It is true that the total transfer function can be calculated by solving nodal equations. The small signal behavior of the whole loop is shown in Figure B.1. The nodal equations can be written as:

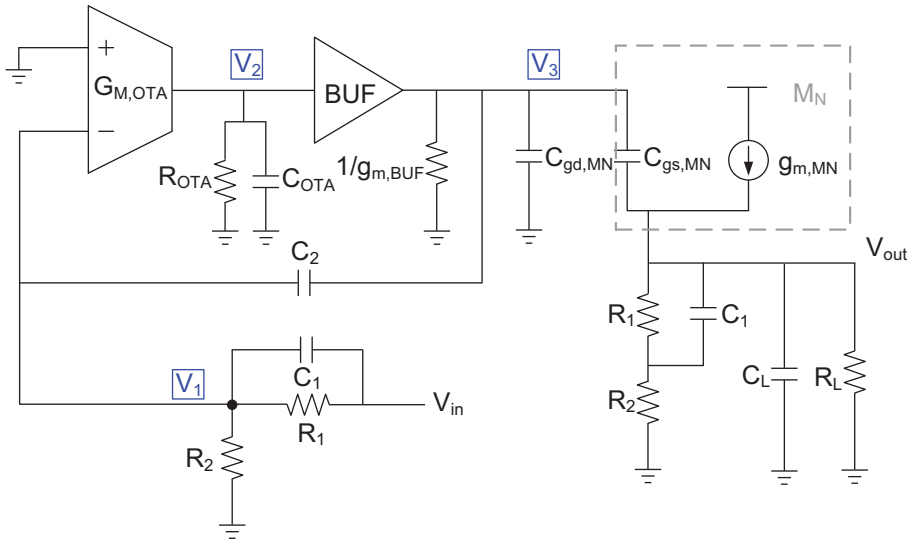

Figure B.1: Signal signal model for the whole loop.

$$
\begin{cases}
sC_1(V_{in}-V_1)+\dfrac{V_{in}-V_1}{R_1}=\dfrac{V_1}{R_2}+sC_2(V_1-V_3) \\
-G_{M,OTA}V_1=\dfrac{V_2}{R_{OTA}}+sC_{OTA}V_2 \\
g_{m,BUF}V_2=g_{m,BUF}V_3+sC_2(V_3-V_1)+sC_{gd,MN}V_3+sC_{gs,MN}(V_3-V_{out}) \\
(g_{m,MN}+sC_{gs,MN})(V_3-V_{out})=sC_LV_{out}+\dfrac{V_{out}}{R_L}
\end{cases}
\tag{B.1}
$$

The transfer function can be calculated by Matlab(see code in Appendix C.4) as[1]:

$$\frac{V_{out}}{V_{in}} \approx \frac{\begin{array}{l} s^4 C_1 C_2 C_{OTA} C_{gs,MN} R_1 R_2 R_L R_{OTA} + s^3 C_1 C_2 C_{OTA} R_1 R_2 R_L R_{OTA} g_{m,MN} \\ -s^2 C_1 C_{gs,MN} G_{M,OTA} R_1 R_2 R_L R_{OTA} g_{m,BUF} \\ -sC_1 G_{M,OTA} R_1 R_2 R_L R_{OTA} g_{m,MN} g_{m,BUF} - G_{M,OTA} R_2 R_L R_{OTA} g_{m,MN} g_{m,BUF} \end{array}}{\begin{array}{l} s^4 C_1 C_L C_{OTA} (C_{gd,MN} + C_{gs,MN}) R_1 R_2 R_L R_{OTA} + s^3 C_1 C_L C_{OTA} R_1 R_2 R_L R_{OTA} g_{m,BUF} \\ +s^2 C_2 C_L G_{M,OTA} R_1 R_2 R_L R_{OTA} g_{m,BUF} + sC_2 G_{M,OTA} R_1 R_2 R_L R_{OTA} g_{m,MN} g_{m,BUF} \\ +g_{m,BUF}(R_1 + R_2)(1 + g_{m,MN} R_L) \end{array}} \tag{B.2}$$

[1]Simplification is based on small numerical terms shown in Appendix C.5

Appendix C

Matlab Codes

C.1 G_m Calculation

```
clc;
clear;
%%%%%%%%%%%%%%Import data from Cadence simulation results%%%%%%%%%%
plotData = importdata('U:\Simulated_Data_CSV_format\gm_MN_plot.csv');

loglog(plotData.data(:,1),plotData.data(:,2),'k','LineWidth',2)
xlabel('I_{load}(A)','FontSize',15);
ylabel('Gm(A/V)','FontSize',15);

set(gca,'FontSize',15);%change X,Y Tick font size

hold on;

%%%%%%%%%%%%%%%%Calculated Model%%%%%%%%%%%%%%%%%%%%%%%%%%

%%Weak Inversion Region(2uA-3.5mA)
I_out=2e-6:1e-6:3.5e-3

    g_MN=I_out/0.0325

loglog(I_out,g_MN,'--k','LineWidth',2)
hold on

%%Saturation Region(3.51mA-120mA)
I_out=3.51e-3:1e-3:120e-3

    g_MN=sqrt(3.4*I_out);

loglog(I_out,g_MN,'--k','LineWidth',2)

hleg = legend('Simulated','Calculated','Location','NorthWest');%legend curve%
```

C.2 Uncompensated Transfer Function Calculation

```
clc;
clear;

%For fast calucation speed%
%V_1=x, V_2=y, V_3=z%

syms    s x y z G_MOTA R_OTA C_OTA s g_mbuf C_gdMN...
        C_gsMN g_mMN R_L C_L R_1 R_2 V_out V_in

S = solve('-V_in*G_MOTA*(R_OTA/(1+s*R_OTA*C_OTA))=x',V_in,...
          '(x-y)*g_mbuf=s*C_gdMN*y+s*C_gsMN*(y-z)',y,...
          '(y-z)*(g_mMN+s*C_gsMN)=z/(R_L/(1+s*R_L*C_L))',z,...
          'V_out=(R_2/(R_1+R_2))*z',V_out);

TF=(S.V_out/S.V_in)

collect(TF,s)
```

C.3 Transfer Function to the gate of M_N

```
clc;
clear;

%For fast calucation speed%
%V_1=x, V_2=y%

syms    s x y G_MOTA R_OTA C_OTA s g_mbuf C_gate...
        R_1 R_2 C_1 C_2 V_gate V_in

S = solve('(V_in-x)/R_1+s*(V_in-x)*C_1=x/R_2+s*(x-V_gate)*C_2',V_in,...
          '-G_MOTA*x=y/R_OTA+s*C_OTA*y',y,...
          'g_mbuf*y=g_mbuf*V_gate+s*C_gate*V_gate+s*(V_gate-x)*C_2',V_gate);

TF=(S.V_gate/S.V_in)

collect(TF,s)
```

C.4 Compensated Transfer Function Calculation

```
clc;
clear;

%For fast calucation speed%
%V_1=x, V_2=y, V_3=z%

syms    s x y z G_MOTA R_OTA C_OTA s g_mbuf C_gdMN...
        C_gsMN g_mMN R_L C_L R_1 R_2 C_1 C_2 V_out V_in

S = solve('s*C_1*(V_in-x)+(V_in-x)/R_1=x/R_2+s*C_2*(x-z)',V_in,...
          '-G_MOTA*x=y/R_OTA+s*C_OTA*y',y,...
```

```
12              'y*g_mbuf=g_mbuf*z+s*C_2*(z-x)+s*C_gdMN*z+s*C_gsMN*(z-V_out)',z,...
13              '(g_mMN+s*C_gsMN)*(z-V_out)=s*C_L*V_out+V_out/R_L',V_out);
14
15 TF=(S.V_out/S.V_in)
16
17 collect(TF,s)
```

C.5 Comparison of Bode Plot

```
1  clc;
2  clear;
3
4  %Values in transfer function aproximation%%
5  R_1=6.26e6;
6  R_2=2e6;
7  g_mbuf=90e-6;
8  G_MOTA=59e-6;
9  R_OTA=1.31e9;
10 C_OTA=0.3e-12;
11 C_L=220e-9;
12 C_1=10e-12;
13 C_2=1.2e-12;
14 C_gsMN=14e-12;
15 C_gdMN=8e-12;
16 R_L=1e6;%Change the load current by R_L
17 I_out=5/R_L
18 %%%%
19
20 %Switch the Output Power transistor between Weak Inversion BJT
21 %and Staurated MOS operation%
22
23 if I_out<=3.5e-3 %Operating in BJT mode
24     g_mMN=I_out/0.0325
25 else              %Operating in MOSFET mode
26     g_mMN=sqrt(3.4*I_out)
27 end
28
29 %End of Values in tranfer function aproximation%
30
31
32 %Simulation results%
33 subplot(2,1,1)
34 %import simulated data%
35 plotData=importdata(...
36     'U:\Simulated_Data_CSV_format\bode_plot_low_current_with_modified_ckt_0726.csv');
37
38 semilogx(plotData.data(:,1),20*log10(abs(plotData.data(:,2)+1j*plotData.data(:,3)))...
39     ,'k','LineWidth',1.5)
40 xlabel('Frequency(Hz)','FontSize',15);
41 ylabel('Gain(dB)','FontSize',15);
42 set(gca,'FontSize',15);%change X,Y Tick font size
43 hold on;
44 grid on;
```

```
45
46 %Caculation result%
47
48 w = logspace(0,10,100);
49
50 tf=(((C_1*C_2*C_OTA*C_gsMN*R_1*R_2*R_L*R_OTA*(1j*w).^4)...
51      +(C_1*C_2*C_OTA*R_1*R_2*R_L*R_OTA*g_mMN)*(1j*w).^3)...
52      +((-C_1*C_gsMN*G_MOTA*R_1*R_2*R_L*R_OTA*g_mbuf)*(1j*w).^2)...
53      +(-C_1*G_MOTA*R_1*R_2*R_L*R_OTA*g_mMN*g_mbuf*(1j*w).^1)...
54      +(-G_MOTA*R_2*R_L*R_OTA*g_mMN*g_mbuf))...
55      ./((((C_1*C_L*C_OTA*C_gdMN*R_1*R_2*R_L*R_OTA...
56      +C_1*C_L*C_OTA*C_gsMN*R_1*R_2*R_L*R_OTA)*(1j*w).^4)...
57      +((C_1*C_L*C_OTA*R_1*R_2*R_L*R_OTA*g_mbuf)*(1j*w).^3)...
58      +(C_2*C_L*G_MOTA*R_1*R_2*R_L*R_OTA*g_mbuf*(1j*w).^2)...
59      +(C_2*G_MOTA*R_1*R_2*R_L*R_OTA*g_mMN*g_mbuf*(1j*w).^1)...
60      +(R_1*g_mbuf+R_2*g_mbuf+R_1*R_L*g_mMN*g_mbuf+R_2*R_L*g_mMN*g_mbuf)));
61
62
63 f=w/(2*pi);
64 semilogx(f, 20*log10(abs(tf)),'--','LineWidth',1.5);
65 hold on;
66
67
68 %Aproximation result%
69 Av=-G_MOTA*R_OTA*(R_2/(R_1+R_2));
70
71 tf2=Av*((1+1j*w*R_1*C_1)...
72      .*(1-(1j*w).^2*(C_2*C_OTA/(G_MOTA*g_mbuf)))...
73      .*(1+1j*w*C_gsMN/g_mMN))...
74      ./((1+1j*w*G_MOTA*R_OTA*C_2*(R_1*R_2)/(R_1+R_2))...
75      .*(1+(1j*w)*((C_OTA*C_1)/(G_MOTA*C_2))+(1j*w).^2*(C_1*C_OTA*(C_gsMN+C_gdMN)...
76      /(g_mbuf*G_MOTA*C_2)))...
77      .*(1+1j*w*C_L/g_mMN));
78
79
80 semilogx(f, 20*log10(abs(tf2)),'r-.','LineWidth',1.5);
81 hold on;
82
83 hleg = legend('Simulated','Calculated','Simplified',...
84                'Location','NorthEast');
85
86 hold off;
87
88 %Phase Plot%
89 subplot(2,1,2)
90
91 H=180/pi*angle(plotData.data(:,2)+1j*plotData.data(:,3));
92 %1j for complex index for fast speed
93
94 semilogx(plotData.data(:,1),H,'k','LineWidth',1.5)
95
96 hold on;
97
98 xlabel('Frequency(Hz)','FontSize',15);
```

```
99  ylabel('Phase(Degree)','FontSize',15);
100 set(gca,'FontSize',15);%change X,Y Tick font size
101
102 %Caculation result%
103
104 f=w/(2*pi);
105 semilogx(f, 180/pi*(angle(tf)),'--','LineWidth',1.5);
106 hold on;
107
108 %Approximation result%
109
110 semilogx(f, 180/pi*(angle(tf2)),'r-.','LineWidth',1.5);
111 hold off;
112
113 hleg = legend('Simulated','Calculated','Simplified',...
114               'Location','NorthEast');
115 grid on;
```

Appendix D

Test-benches

The test-bench used for NMOS linear regulator performance evaluation is shown in Figure D.1.

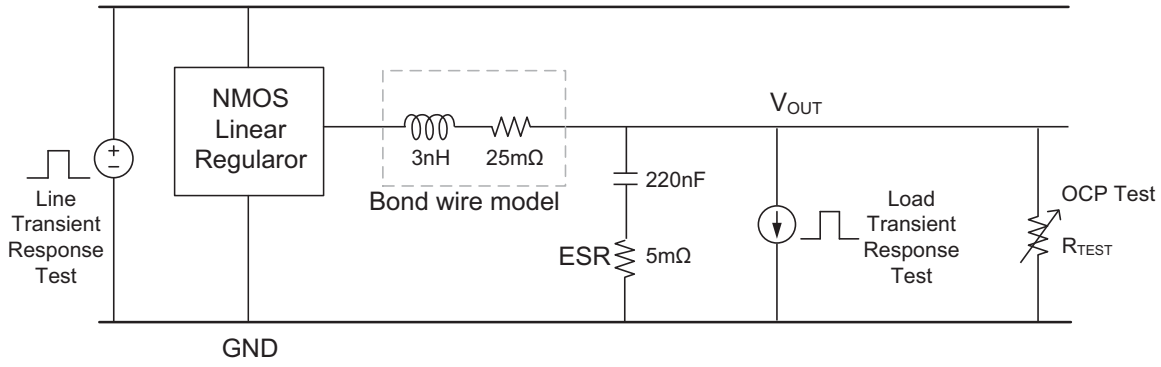

Figure D.1: Test-benches.

The R_{TEST} resistance variation in time scale for OCP test is shown in Figure D.2.

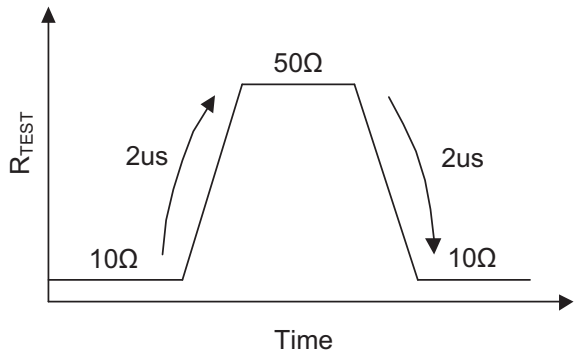

Figure D.2: R_{TEST} waveform.

Appendix E

Current Sink Path

For this linear regulator, the test case of load transient variation from 0μA to 120mA is not included in Chapter 4, because the power transistor is only able to source current to the load. The linear regulator can also be treated as a Class A output voltage buffer. If the load current suddenly reduces to 0A, the power transistor current and load current difference will charge the output capacitor, making the output voltage higher than the nominal value.

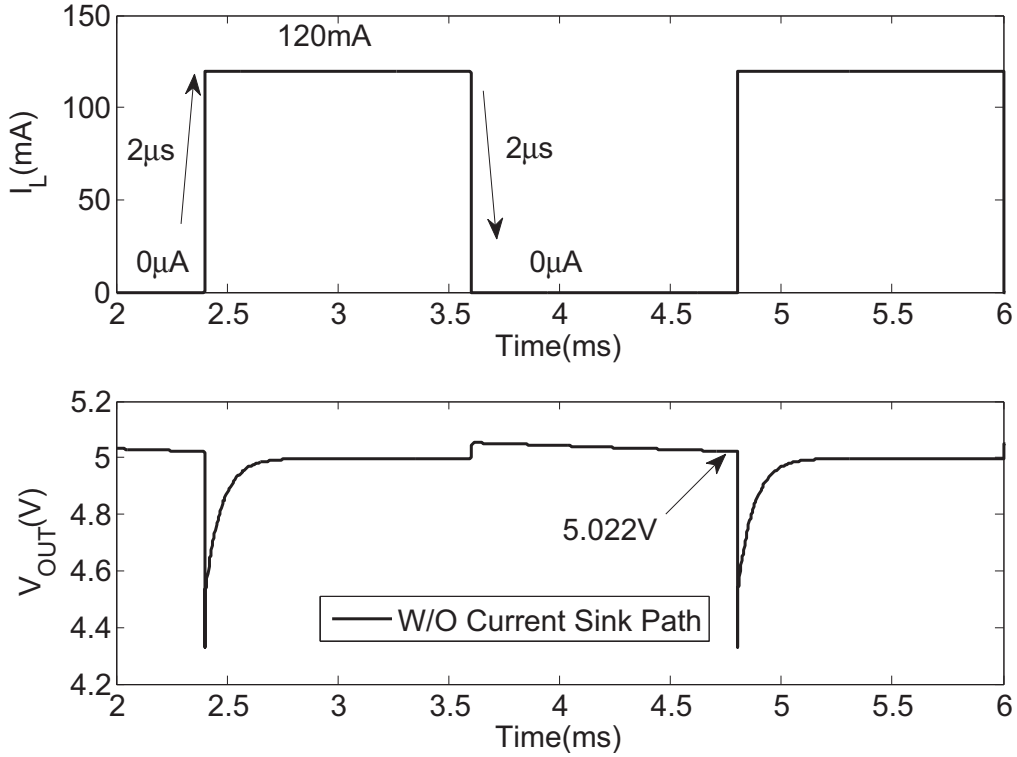

Figure E.1: Without current sink path.

The power transistor does not have the ability to sink current, the output voltage reduces only by the discharging path composed by R_1+R_2 and C_L. Since R_1, R_2, C_L

are all in relative large values. The discharging time constant can be quite long (e.g. $\tau \approx$1.32s in this design).

In this case, if the output voltage "stucks" at a level higher than its nominal, the feedback loop will force the gate voltage V_G to reduce (in some cases V_G may even below 5V). Then, when the load current suddenly increases, the gate voltage will experience a larger excursion from low to high than its normal case. For the larger excursion on V_G, the output voltage will have larger spikes which is shown in Figure E.1. It can be seen that the output voltage is stuck at 5.022V before the I_L increases. This results a large V_{OUT} variation by 700mV.

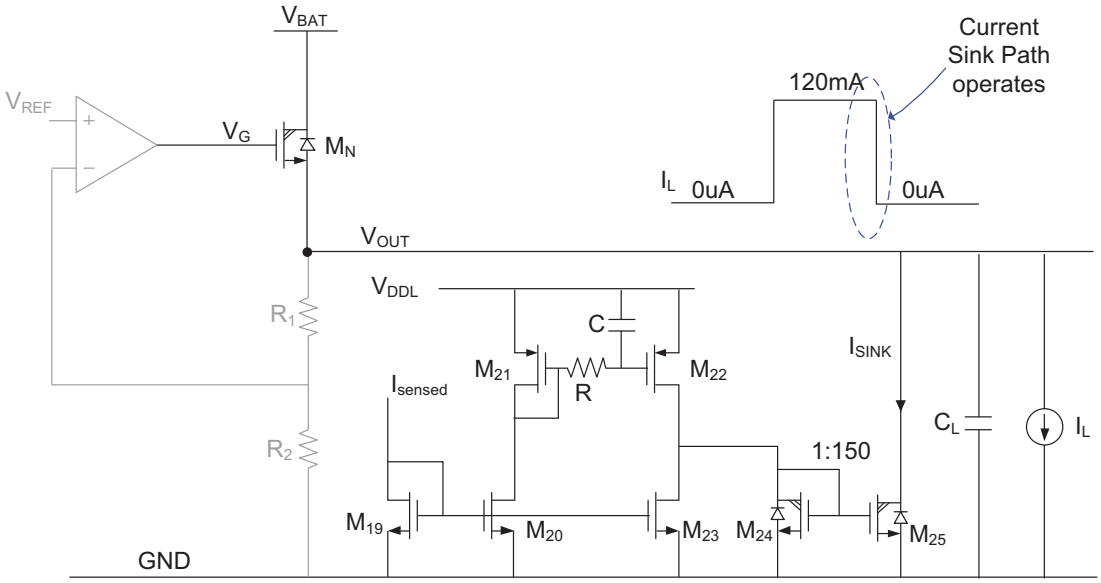

Figure E.2: Current sink path circuit.

To solve this problem, a current sink path should be added. The current sink circuit is active only when the load current varies from high to low. In other cases, the current sink path should not draw any quiescent current from the linear regulator. Figure E.2 shows one possible current sink path solution. Again, the output current is sensed by the circuit described in Section 3.5.1. In normal case, the current from M_{22} and M_{23} are roughly equal, little mismatch current flows into M_{24}. If M_{22} and M_{23} are chosen to be long channel devices, the channel length modulation effect can be further reduced, the static mismatch current will be negligible.

When I_L changes from 0 to its maximum, the M_{23} will sink all current from M_{22}, pulling the gate of M_{25} down to ground, $I_{SINK} \approx 0$. When I_L changes from maximum to 0, M_{20} and M_{23} will shut off. Due to the RC delay, M_{22} still provides high current. The current difference between M_{22} and M_{23} will sink into M_{24} which mirrors current to M_{25} forming a large amount of current I_{SINK}.

The effectiveness of this current sink path is simulated and the results are shown in Figure E.3. It can be seen that during I_L from high to low, the peak I_{SINK} is around 80mA. This I_{SINK} current peak removes additional charge on C_L. The output voltage can be back to its nominal value after 800μs, the V_{OUT} variation can be reduced to

70mV, which is nearly 10 times smaller than the case without current sink path.

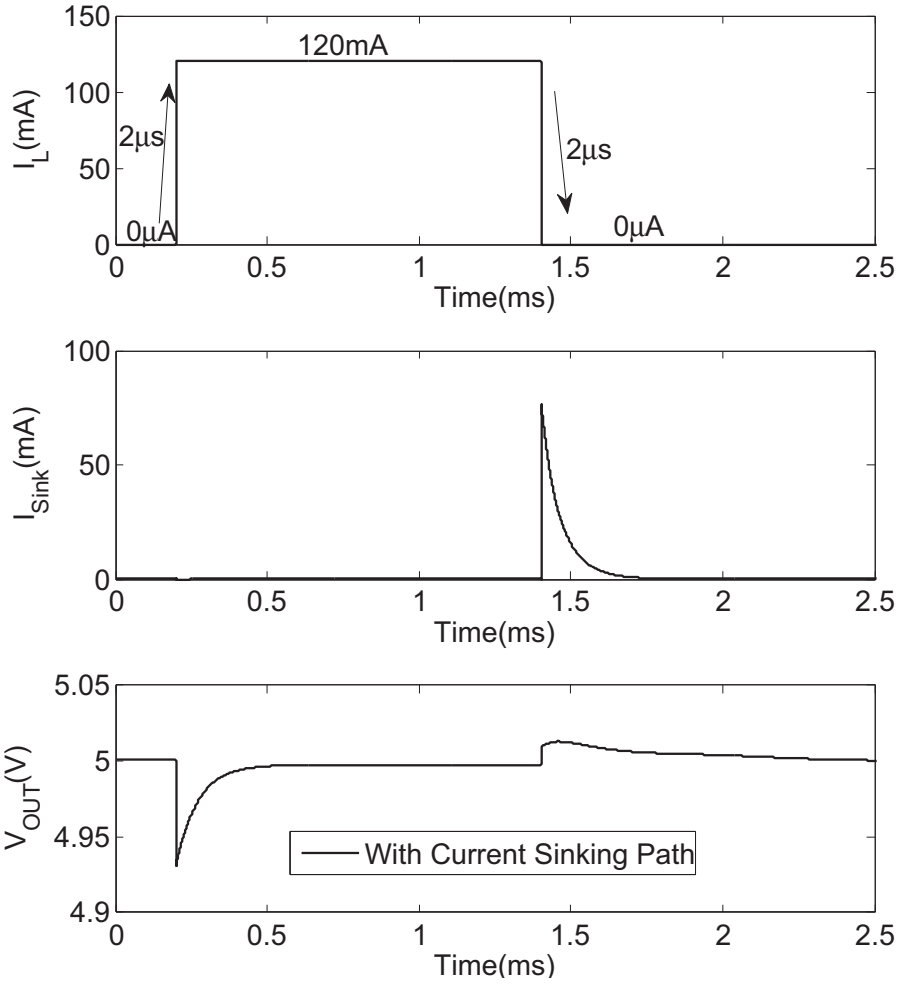

Figure E.3: With current sink path.

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