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A 9-bit 33MHz Hybrid SAR Single-slope ADC

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Abstract

In this work a 9-bit, 33MHz hybrid SAR single-slope ADC for element-level digitization in 2D ultrasound transducer arrays is presented. This hybrid architecture consists of a 5-bit SAR ADC followed by a 4-bit single-slope ADC. In the comparator design, the dynamic comparator and the continuous-time comparator for the SAR and single-slope conversion, respectively, are combined together with a shared preamplifier. The simulated ENOB is 8.96 bit, the power consumption is 800uW, the estimated area is 0.015mm^2 and the achieved FoM is 48.7fJ/conv-step.

Contents

Abstract

1. Introduction

The main subject of this thesis is a 9-bit, 33MS/s, element-level hybrid successive approximation register (SAR) and single-slope ADC for application in a 3D ultrasound imaging systems. The proposed design introduces the combination method of these two types of ADCs to achieve a two-stage design, which is a attempt to address the area and power consumption limitation of the element-level ADC design in 3D ultrasound imaging systems.

In this introductory chapter, the application of this ADC is discussed. This is followed by a short discussion of the challenges and the previous research. Then, the motivation and objectives of this work are briefly described. Finally, the organization of the thesis is given.

1.1 ADC Application and Challenges

The element-level ADC presented in this thesis is invented to be applied in a 3D Trans-Esophageal Echocardiography (TEE) imaging system, which can create high-quality real-time images of the heart and its blood vessels using ultrasound wave. In the TEE system, a gastroscopic tube is involved and an ultrasound transducer is mounted at its tip. By inserting this tube into the patient's esophagus, images can be made directly from the backside of the heart. As a result, the TEE pictures are more detailed, compared with Transthoracic Echocardiography (TTE), the most common type of echocardiogram. As an element-level ADC, the beamforming for steering and focussing can be achieved by full digital delay elements. Compared with analog delay, the delay resolution can be remarkably increased, which can improve the imaging quality.

In order to achieve a full digital 3D TEE imaging system, several challenges should be considered.

To achieve 3D images without any mechanical repositioning involved, a 2D transducer array that consists of more than a thousand transducers is required, with which beamsteering and focusing in both azimuthal and elevation planes can be performed. In other words, there would be thousands of channels between the probe and the ultrasound machine, if these elements are connected to an external imaging system with separate cables [1]. More than 1000 cables are a prohibitive number of connections that are hard to fit in the endoscope. Therefore, the cable count should be reduced.

On the other hand, for a full digital 3D ultrasound imaging system, the beam formation circuit should be implemented in the digital domain, which means an element-level ADC is required in front of the beam former. However, the TEE application makes the design of the ADC really difficult. Since the TEE probe is inserted into the esophagus of a patient, the esophageal cavity limits the size of the transducer, as well as front-end circuit which is mounted at the tip of the probe as well, to around 1cm. This leads to an element size of 100 to 200µm. In this small space, LNAs, element-level ADCs, and the digital beam formers should be implemented, which means the design should be really compact. Furthermore, to avoid

overheat of the human tissue, a constraint of maximum power consumption is put on the front-end electronics. The power consumption of a commercially available TEE imaging probe in transmit mode is about 1W to 2W [2]. For the receive electronics the power constraint should also be set at the same magnitude, around 1W. Since there would be thousands of elements within the transducer handle, for the front-end circuit, the power consumption should be around 1mW including the power consumption of a LNA, an element-level ADC, and a beam former which is shared by many elements.

In the end, these challenges make it really hard to achieve a 3D ultrasound imaging system with 2D transducer array, let alone the full digital beam-forming solution [3].

1.2   Previous Research

In [4], in order to achieve "real time" 3D ultrasound imaging and eliminating the motion artefacts, 2D sparse array is utilized. In order to achieve high acoustic pressures and get rid of the "clutter" within the image of cardiac chambers, a fully sampled 2D array is required. However, it is unfeasible to achieve this fully sampled array with the traditional beamforming technology, due to the large number of interconnection cables, high power consumption. In order to address this problem and achieve a 2D transducer array with high imaging quality, a hybrid beam-forming electronics composed of both analog and digital beam-forming sections is utilized [5] [6].

The beam formation is split in two stages, as shown in Figure 1. The first stage is located within the transducer handle with the analog beam forming which could be achieved by low power analog delay and summation. Since the transducers inside the sub-group are selected to be close to each other in space, only fine delays are needed. The second stage is located in the ultrasound machine with a traditional 128 channel digital beam-former, which provides the digital delay [1]. In the end, this sub-array beam formation approach reduces the number of channels and connections to an manageable number, which makes the 2D transducer array possible. However, this is still not a full digital beam formation solution.
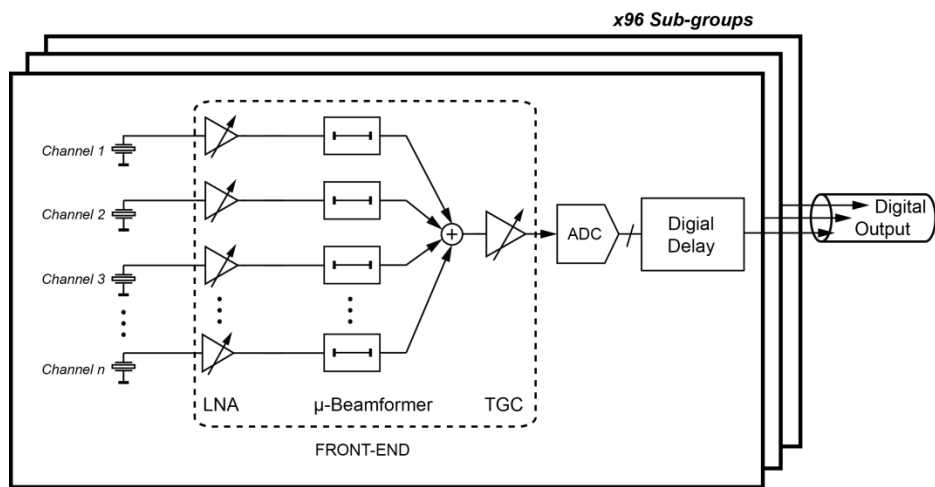

Figure 1 Block diagram of the TEE Imaging System with Hybrid Beamformer [2] [7]

1.3   Motivation and Objectives

The μ-beamforming scheme shown in Figure 1 precludes parallel beamforming of the whole volume for high-frame-rate imaging and suffers from finite delay resolution, which limits the beamforming approaches that can be implemented. Ideally, one would like to have access to all elements level RF signal so as to be able to implement beamforming fully in the digital domain.

To obtain the required delay accuracy and a complete reconfigurability of the beam-forming process, the beam former could be implemented by FPGA [8] and DSP processor [9]. This requires that the RF signal received by the individual transducer elements are digitized.

Therefore, an important step in achieving a full digital beam formation solution for the 2D transducer array that to design an element-level ADC with compact circuit and low power consumption. Figure 2 shows the block diagram of the full digital receive beam formation 3D TEE imaging system. The ADC is set directly behind the LNAs. Together with the digital beam-former and summation, a digital output of the probe is achieved. Consequently, a full digital beam formation solution for a 2D transducer array could be achieved as well.
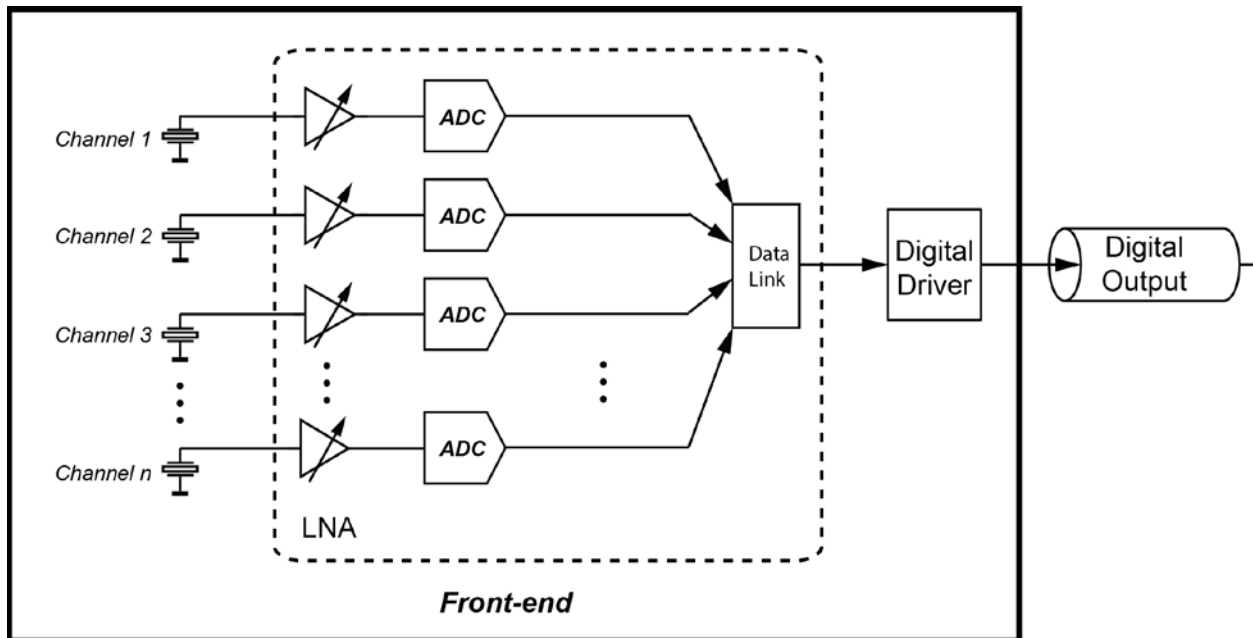
Figure 2 Block diagram of the proposed TEE imaging system

1.4 Organization of the Thesis

The thesis is organized as follows. In chapter 2, the ADC requirements are discussed including the introduction of the specifications, as well as the ADC architecture comparison and selection. In chapter 3, the architecture level design is described including a short review of the sampling and switching scheme of a SAR ADC, an introduction about the shared architecture of the single-slope ADC, the combination of these two ADCs and finally the power optimization of the entire hybrid ADC. Chapter 4 illustrates the transistor level design of the building blocks. The thesis ends with simulation results and discussion in chapter 5.

2. ADC Architecture Choice

As mentioned in the previous chapter, the challenge to design a low power consumption ADC with a compact circuit is the fundamental difficulty to implement a full digital beam formation for the 3D TEE imaging system. In this chapter, these difficulties will be translated into design targets for the ADC. Based on that, the architecture choice will also be made.

2.1 ADC Requirements

In this ADC design, the area and power budget is limited by the application. The power consumption should be less than 1mW. The centre frequency of the selected transducer is 5MHz, so the pitch size of the transducer should be half of the wavelength of the ultrasound signal which is 150µm. As a result, the chip area of the ADC is also limited by the transducer size to be less than 0.01mm^2. Besides these, the other specifications are also determined. The bandwidth of interest in the receive mode is from 3.75MHz to 6.25MHz. According to the Nyquist Criterion, the sampling frequency of the ADC should be higher than twice this centre frequency. In order to make this ADC design suitable for even higher frequency transducer application, the sampling frequency of the ADC is set to 33MS/s. Furthermore, since the dynamic range of the output signal of the LNA in Figure 2 is around 45dB, the effective number of bits (ENOB) as a quality measure of the ADC for both linearity and resolution should be larger than 8 bit. To make the design conservative, the resolution of the ADC is selected at 9bit.

Based on these specifications, the figure of merit (FoM) of this ADC can be calculated with the following equation:

$$FOM = \frac{P}{2^{ENOB} \cdot f_S} \tag{1}$$

where P is the power consumption of the ADC, and f_s is the sampling frequency. The FoM of the required ADC is around 60fJ/conversion-step. The FoM versus sampling frequency of state-of-the art ADCs is shown in Figure 3. Comparing our design target with the state of the art, candidate ADC architecture can be found.
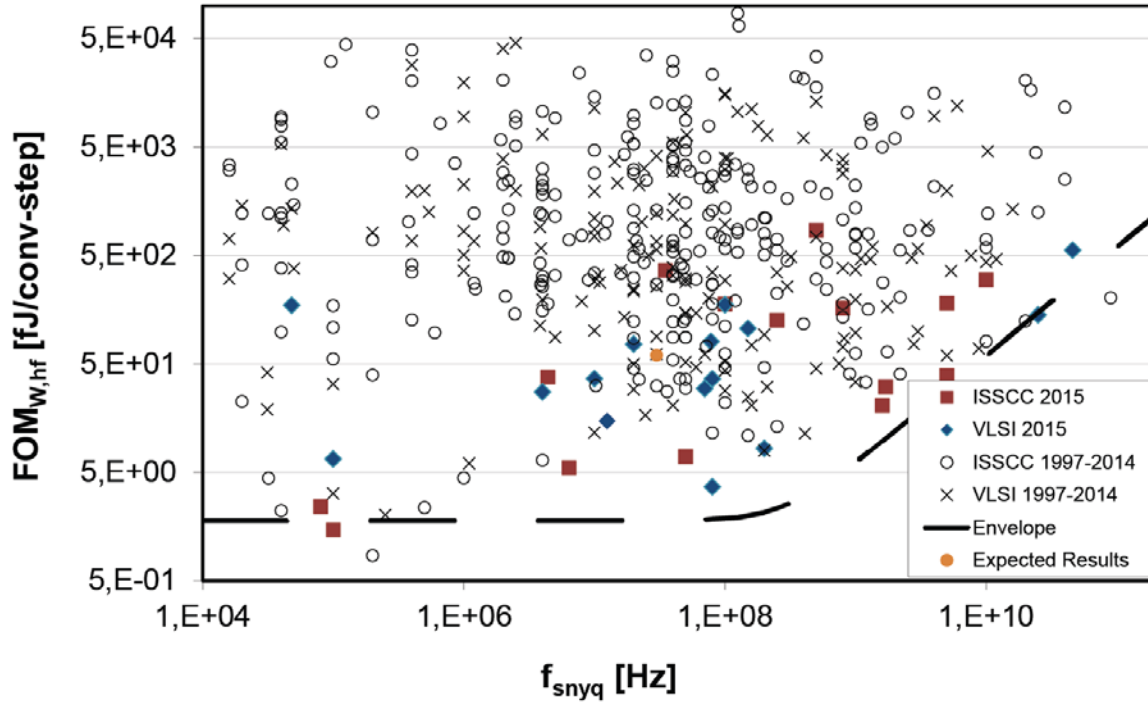
Figure 3 State-of-the art ADCs [10]

2.2 Candidate architectures

It is convenient to find out the candidate architectures by checking the FoM in the ADC performance survey [10]. For our middle speed (tens of MHz), middle resolution (eight to ten bits) application, commonly-applied ADC architectures are the two-step pipeline SAR ADC [11], the time-interleaved pipeline SAR ADC [12], and the SAR ADC [13], due to the reason that the SAR ADC is widely known as the most power efficient architecture.

However, the rank of FoM is not a sufficient method to find out the candidate architecture, due to the reason that the FoM definition is mainly based on the power consumption and conversion speed trade-off, which means the trade-off between power consumption and chip area is not taken into account. For example, the chip area of time-interleaved SAR ADC is at least twice as much as that of the corresponding SAR ADC due to the time-interleaved building blocks of the circuit. Unfortunately, even though these designs are implemented with better technology 28nm, 40nm, 90nm, none of the above ADCs meet the die-size requirement of our application.

Since the trade-off between the area and power consumption is not considered in the ADC performance, there is no direct way to evaluate the most area efficiency ADC architecture. However, it is obvious that

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architecture with a simple circuit topology may have an advantage in die-size. As a result, the single-slope ADC, which is widely utilized as a column-parallel ADC in image senors is considered. In the image sensor application, different types of ADCs have been employed as well, such as the SAR ADCs [14] [15], cyclic ADCs [16], and single-slope ADCs [17] [18] which is obviously the most widely used. The reason is because that single-slope ADCs can be implemented with a highly shareable circuit, which mainly consists of a ramp-signal generator, a comparator and a counter. As a result, the chip area of the single-slope ADC is much smaller than that of cyclic ADCs and SAR ADCs. Moreover, as a column-parallel ADC, the ramp-signal generator can be shared by each pixel in the column, which ensures the uniformity of the conversion.

However, the conversion speed of single-slope ADCs is relatively low. For a N-bit A/D conversion, the conversion time of both SAR and cyclic ADCs is N clock cycles, while 2^N clock cycles are required for a single-slope ADC. The conversion speed problem limits the performance and application of the single-slope ADC.

In order to solve this problem, various approaches have been reported, such as the multiple-ramp single-slope (MRSS) ADC [19] [20] [21], and the dual-slope ADC [22]. Normally, this kind of approach can only achieve a several times higher conversion speed compared with the conversional single-slope ADC [19], because they are not focussing on the fundamental problem of the single-slope ADC, which is the counter. No matter how fast the input frequency is, the counter has to count 2^N times to complete the full conversion, which fundamentally limits the conversion speed for both single-slope and multiple ramp ADCs.

In order to eliminate the counter in the single-slope ADC, in a recently published design, the counter-based single-slope ADC is replaced by a single-slope ADC with time-to-digital (TDC) convertor [23]. Since the conversion time of a TDC is not limited by the external clock period, but the time resolution of the TDC, which could be less than 4.5ps in the recently published design [24], the conversion speed of a TDC based single-slope ADC can also be remarkably increased. As a result, the conversion speed problem of the single-slope ADC is solved by the TDC-based architecture.

However, a critical issue of this high time resolution TDC is that the chip area and the power consumption increases as the resolution increases with the working time duration get longer. To address this problem, a two-stage structure is proposed [25] [26]. In the first stage, a coarse TDC performs a quantization operation with lower time resolution. In the second stage, a fine TDC is utilized to quantize the residue value of the first quantization. While the power consumption could be reduced due to the reason that the most power hungry part of the ADC has a shorter working time.

2.3   Proposed Architecture

In order to obtain a further power reduction on the single-slope ADC, an alternative approach is introduced in this thesis: a hybrid SAR and single-slope ADC. Rather than a single-slope ADC with coarse-fine TDC structure, a coarse-fine ADC structure is proposed. In contrast with the earlier published combination of the single-slope and SAR ADC [27], which a 3-bit single-slope ADC in the coarse stage and a 8-bit SAR ADC in the fine stage, the proposed architecture is like the zoom-ADC [28]. The first

stage is a low resolution SAR ADC which performs the coarse conversion, and the residue input voltage is quantized by the fine stage, a single-slope ADC. Since the SAR ADC can be very power efficient (less than 10fJ/con-step) [29], it is expected that the power consumption of the entire ADC should be lower than a pure single-slope ADC, while the chip area will be larger. As a result, a trade-off between power and area consumption should be considered. In order to reduce the design complexity of the single-slope ADC, a delay-line based TDC is selected as the quantizer.

2.4　Summary

In this chapter, the architecture choice has been made by comparing different candidate architectures, as a hybrid SAR and single-slope ADC. The design targets are shown in Table 1.

Table 1 Design Targets of Prototype Hybrid SAR SS ADC

Specification	Design Target
Technology	TSMC 0.18um CMOS
Supply voltage	1.8V
ENOB	8~9 bit
Resolution	> 8bit
Conversion time	30ns
Power consumption	<1mW
FoM	<60fJ/conversion-step

3. Architecture Level Design

As described in the previous section, SAR ADCs have relatively high conversion speed and the lowest power consumption, but at the cost of large C-DAC area. Single-slope ADCs, on the other hand, have a really compact circuit due to their simple and highly shareable structure, but are trapped in the trade-off between conversion speed and power consumption. In this chapter, it will be shown that the two structures can be combined to meet the requirements of our application, while keeping middle speed, middle resolution, and relatively low power consumption and small area.

This chapter is organized as follows. Section 3.1 describes the architecture of the SAR ADC including the calculation of the thermal noise and mismatch of the C-DAC, the sampling method, and the switch scheme. Section 3.2 introduces the architecture of the single-slope ADC, detailing how to solve the slow conversion speed problem and how to design the shared ramp-generator. Section 3.3 describes two ways to combine SAR and single-slope ADC. The chapter ends up with the division of resolution and conversion time of the two conversion phases in Section 3.4.

3.1 SAR ADC Architecture

Figure 1 shows a simplified system-level diagram of a SAR ADC with binary weighted C-DAC. In this section, the SAR architecture is introduced as follows, the thermal noise and mismatch of the C-DAC, sampling and switching scheme.
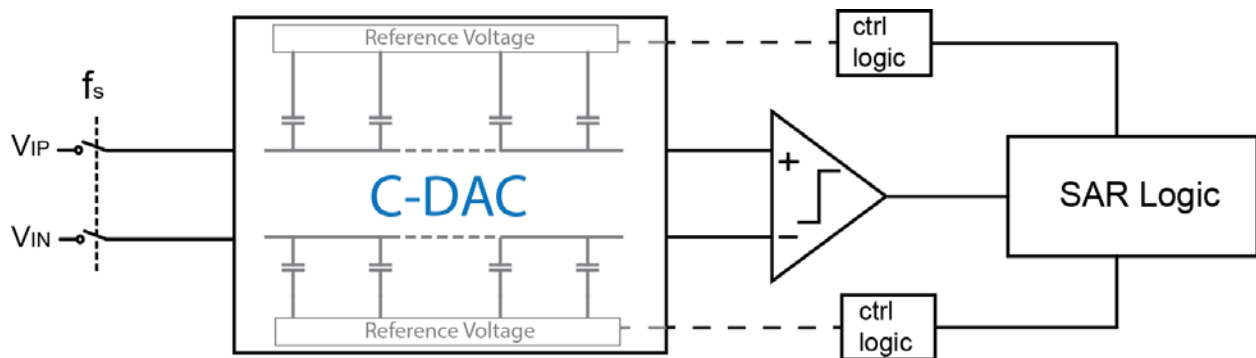

Figure 4 SAR ADC

3.1.1   Thermal noise and mismatch calculation of the C-DAC of the SAR ADC

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The C-DAC is one of the most important building blocks of a SAR ADC. The minimum value of the total capacitance and the unit capacitance are determined by the thermal (kT/C) noise and the capacitor mismatch.

The thermal noise limits the minimum size of the total capacitance of the C-DAC. The thermal noise power is given by,

$$v_{n,Samp}^2 = 2\frac{kT}{C_{DAC}}$$

(2)

where k is Boltzmann constant, T is temperature, C_{DAC} is the total capacitance of one branch of the differential C-DAC.

To obtain a quantization noise dominated design, the quantization noise should be larger than the thermal noise. The quantization noise power is given by,

$$v_q^2 = \frac{V_{LSB}^2}{12}$$

(3)

in which V_{LSB} is the LSB voltage of the ADC. The constraint of the capacitance can be deduced from (2), (3), with a 9-bit resolution, and a reference voltage of 200mV:

$$C_{DAC} > \frac{24kT}{V_{LSB}^2} \approx 652fF$$

(4)

Since this would correspond to an extremely small LSB capacitance of around 50fF, the capacitor matching accuracy limits the minimum capacitor value. The mismatch can be described by,

$$\frac{\sigma_{\Delta C}}{C} < \frac{1}{2^N}$$

(5)

where N is the resolution. To achieve a 9-bit accuracy, the capacitor mismatch should be smaller than 0.19%. In the Monte-Carlo simulation, a pair of $7*7\mu m^2$ MIM capacitors with the capacitance around 73.5fF are selected. Sigma of this mismatch is 0.18%, which is smaller than the required value. With this unit capacitor, a total C-DAC capacitance of 1176fF is obtained, which meets the thermal-noise requirement given by (5) with margin.

3.1.2   Sampling Scheme of the SAR ADC

SAR ADCs employing a C-DAC can be implemented using either top-plate sampling or bottom-plate sampling [30]. In recent published SAR ADC designs, bottom plate sampling scheme is more commonly used [31], [32]. Figure 5 shows a 5-bit bottom-plate sampling SAR ADC. During the sampling phase, the

top plate of the capacitor is connected to V_{cm} through the switches S_3, and the bottom plates of the capacitors connected to V_{ip} through S_1, so the input voltage V_{ip} - V_{cm} is sampled on the capacitors.
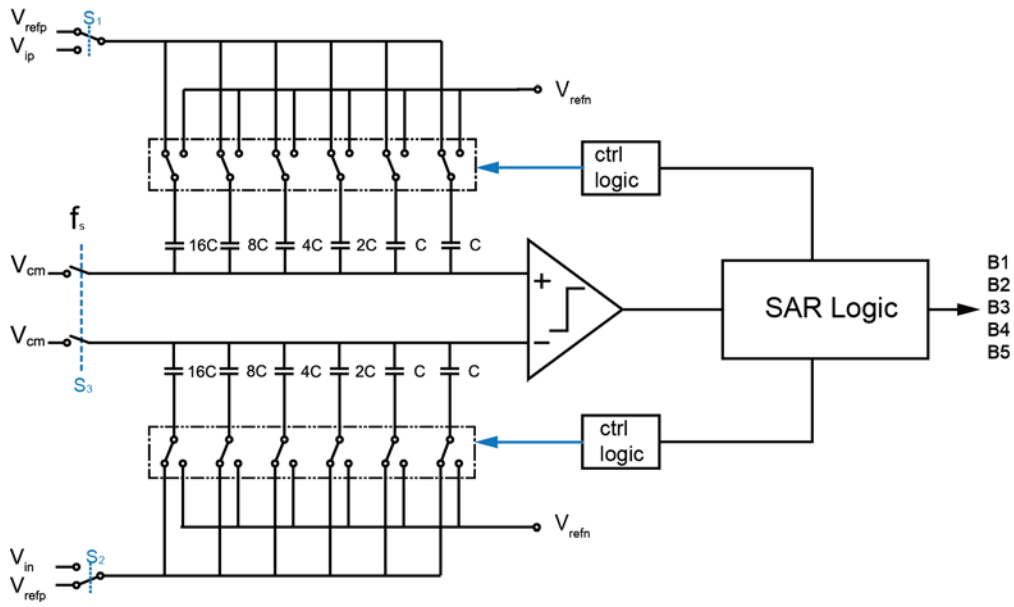

Figure 5 A Bottom Plate Sampling SAR ADC

Compared with bottom-plate sampling, top-plate sampling scheme could provide a more compact design while having the same resolution. Figure 6 shows a 5-bit SAR ADC diagram with top-plate sampling method. The C-DAC area of the bottom-plate sampling SAR ADC is twice as much as that of the top-plate sampling SAR ADC. Since the input voltage is sampled on the top-plate of the capacitors, the first comparison takes place directly after the sampling phase, which simplifies the MSB conversion. As a result, the MSB capacitor of bottom-plate sampling scheme is not required any more, which saves half of the C-DAC area. In the end, top-plate sampling is selected as our sampling scheme. This does not mean the top-plate sampling is perfect, because in the sampling phase the parasitic capacitance of the comparator will be sampled to the input voltage, which means the parasitic capacitance is included in the capacitance of the C-DAC. Since the parasitic capacitance is quite small compared with the C-DAC, this impact can be tolerated.
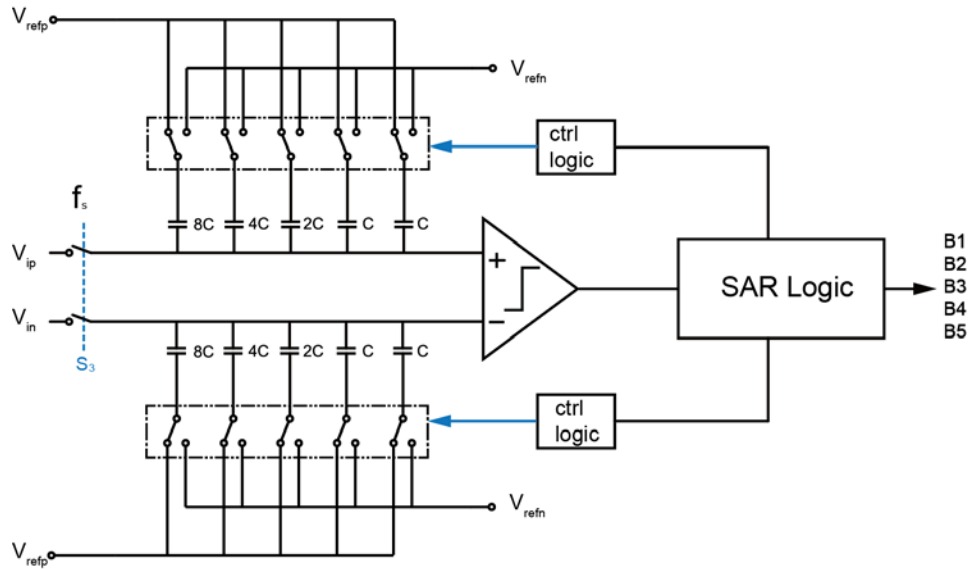
Figure 6 A 5-bit top-plate sampling SAR ADC

3.1.3 Switching Scheme of the SAR ADC

In a conventional SAR ADC, the trial-and-error searching procedure is always applied which is shown in Figure 4, but this simple and intuitive switching scheme is not the most energy efficient one. Since power consumption is the other most concerned factor in our design, a monotonic downwards switching procedure is selected.
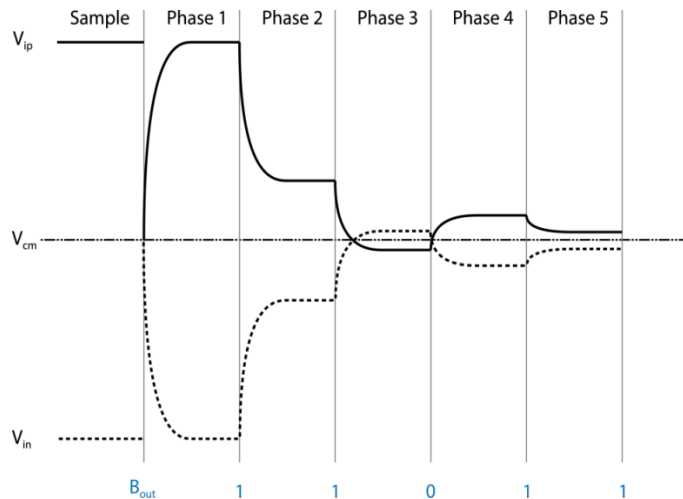

Figure 7 Waveform of conversional switching procedure

This switching procedure can be explained with the top-plate sampling scheme in Figure 6. During the sampling phase, the input signal is sampled on the top plates via bootstrapped switches, in order to increase the sampling speed. In the meanwhile, all the bottom plates are set to V_{refp}. Next, the first

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comparison takes place directly after the sampling switches turn off. If V_{ip} is larger than V_{in}, the bottom plate of the MSB capacitor, on positive side, switches to V_{refn}, with MSB B1 equal to '1', and the negative side remains unchanged. Otherwise, the bottom plate of the MSB capacitor, on negative side, switches to V_{refn}, with MSB is '0', and the positive remains unchanged. The ADC repeats the procedure until the LSB is determined. As a result, in each conversion cycle, only one capacitor is switched, which reduces both the charge redistribution in the C-DAC, and the switch control circuit. Thus, the monotonic switching scheme leads to a smaller charge dissipation. The waveform of the monotonic downwards switching scheme is shown in Figure 8.
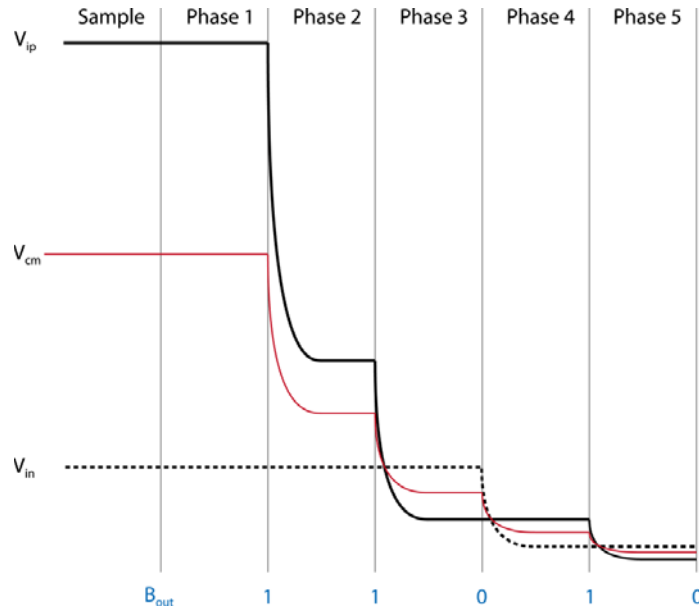

Figure 8 Waveform of monotonic switching scheme

To compare the energy dissipation of these two switching schemes, the average switching energy of each method is calculated [33]. If the digital output codes are equivalent, the average switching energy of a conversional SAR ADC can be described as equation (6)

$$E_{avg,bp} = \sum_{i=1}^{n} 2^{n+1-2i}(2^i - 1)CV_{ref}^2 \tag{6}$$

where n is the resolution, and V_{ref} is the reference voltage.

For the monotonic switching procedure, the average switching energy is :

$$E_{avg,tp} = \sum_{i=1}^{n-1} (2^{n-2-i})CV_{ref}^2 \tag{7}$$

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For a 9-bit SAR ADC, the conversional switching method consumes $680.7CV^2_{ref}$, and the monotonic switching procedure consumes $127.5CV^2_{ref}$ [33].

The applied sampling and switching scheme saves the C-DAC area and energy dissipation of the charge redistribution during the conversion, but the schemes have disadvantages as well.

For the top plate sampling scheme, the parasitic capacitance of the input transistors of the comparator is directly connected to the C-DAC. As a result, in the sampling phase, the input voltage is also sampled on the parasitic capacitance which makes the parasitic capacitance part of the C-DAC, and influences the conversion results. Since this parasitic capacitance is quite small compared with the capacitance of C-DAC, the influence can be considered as gain error and easily calibrated.

For the monotonic switching scheme, the common-mode voltage, as shown in Figure 8, shifts down together with the input voltage. Since the reference voltage is 200mV, the common-mode voltage shifts at most 175mV, which will have to be taken into account in the design of the comparator.

3.2   Single-slope ADC Architecture

As discussed in the previous chapter, the motivation of selecting single-slope ADC as the fine convertor of this hybrid ADC is due to its simple and shareable structure. The building blocks of a single-slope ADC consists of a voltage-to-time conversion (VTC) part including a comparator, a ramp-signal generator and a time-to-digital conversion part which is a TDC. Since this is not a time-interleaved design, the comparator cannot be shared. In the end, the shared ramp-signal generator, and shared delay-line of the TDC are introduced in this section.

3.2.1   Shared Ramp-signal Generator

In recently published ADCs, different methods are implemented to achieve a ramp-signal generator [34] [35]. The most commonly used method is to discharge the sampling capacitor linearly with a current source, as shown in Figure 9. The constant current draining on the sampling capacitor C1 results in a linearly discharged input voltage V_{in1} which is shown in Figure 10.
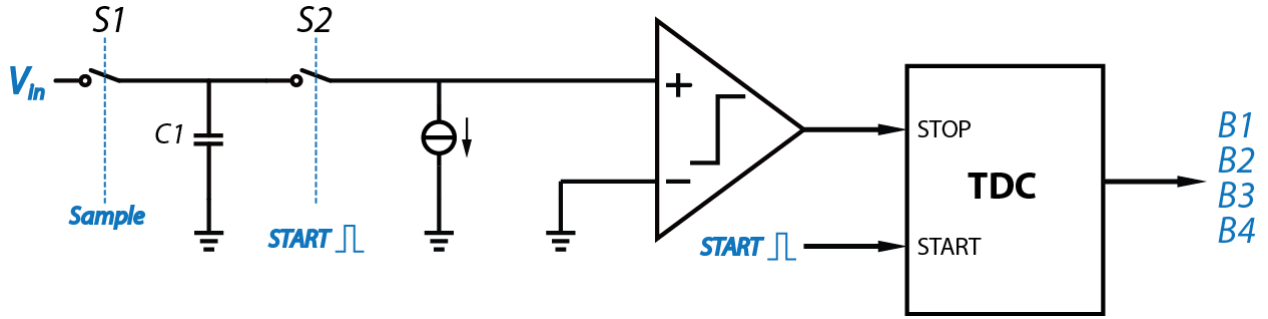
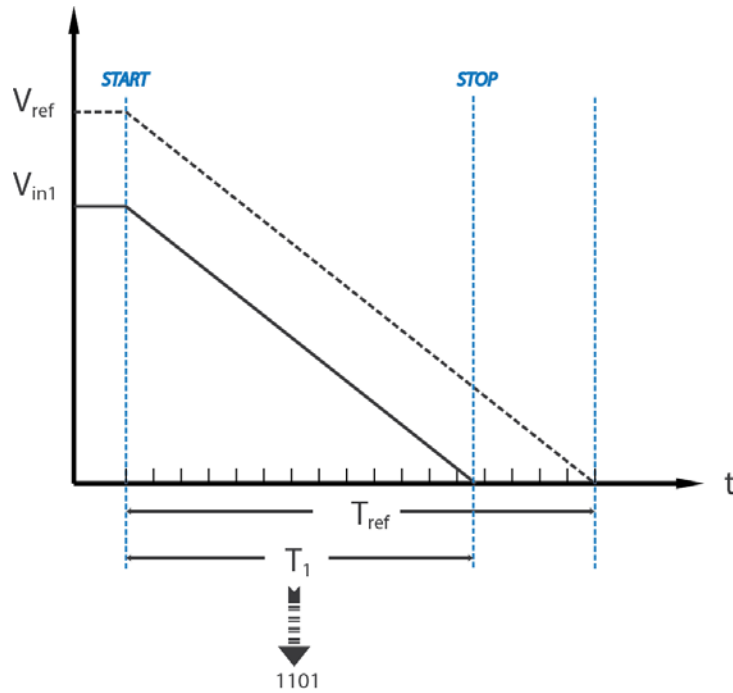**Figure 9 Single-Slope ADC Current Discharge Model**

Figure 10 A 4 bit SS ADC Waveform with Current Source as Ramp Generator

The voltage of the positive input node of the comparator in Figure 9 is given by equation (8),

$$V_+ = V_{in} - \int_0^{T_1} \frac{I}{C_1} \, d\tau \tag{8}$$

Where V_{in} is the sampled input voltage, and T_1 is the resulting time duration between the start signal turning the current source on and the stop signal due to the output of the comparator going high. In the end, the linear relation between the input voltage V_{in} and the resulting time duration T_1 can be deduced as,

$$V_{in} = \frac{T_1 \cdot I}{C_1} \tag{9}$$

Thus, the VTC function is achieved.

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After quantizing the time to a digital output code by a TDC, V_{in} can be expressed as,

$$V_{in} = B_{out} \cdot V_{ref} \tag{10}$$

where B_{out} is the result of the analog-to-digital conversion.

However, this introduced method is unsuitable to make a shareable ramp-signal generator due to the reason that current cannot be accurately shared to parallel connected following circuits, while voltage can. As a result, instead of discharging the sampling capacitor with a current source, a ramp voltage source is applied in our application. Figure 11 shows a simplified diagram of a single-slope ADC with the ramp voltage source as the ramp-signal generator.
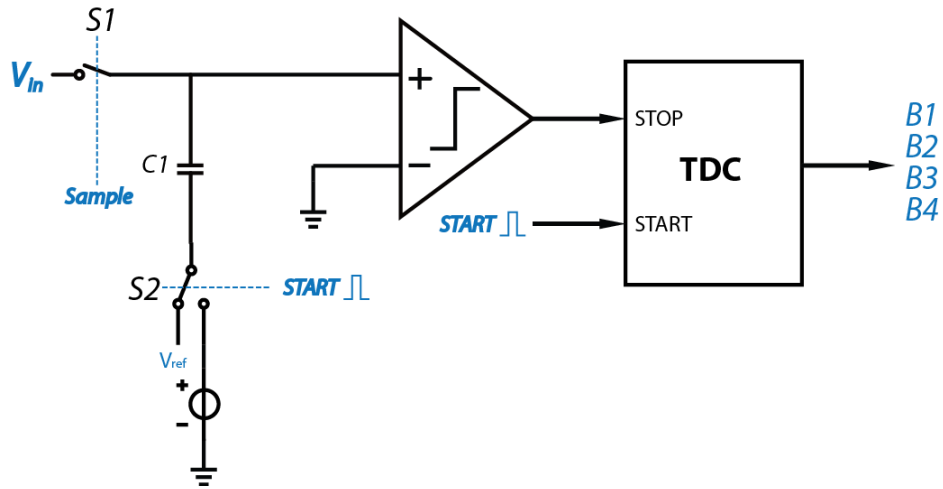

Figure 11 Single-Slope ADC with Voltage Ramp

During the sampling phase, S1 turns on, and S2 connects to V_{ref}. Next, S1 turns off, and S2 switches to the ramp voltage source. In the meantime, the ramp voltage source starts ramping. As a result, the voltage at the positive input node of the comparator is not discharged but shifted together with the ramp voltage signal. The waveform is shown in Figure 12.
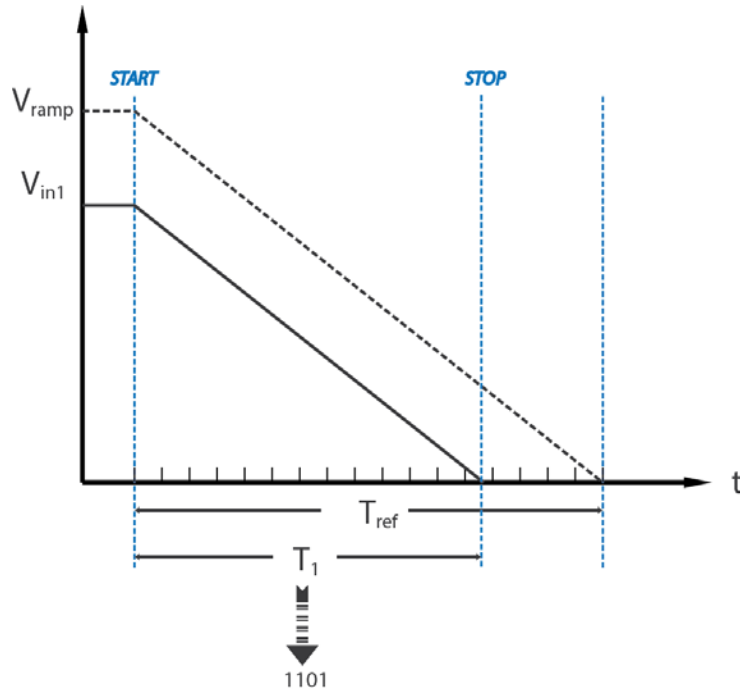
Figure 12 Waveform of a 4bit SS ADC with Ramp Voltage Source as Ramp Generator

As a result, the linear relation between the input voltage and the resulting time duration is achieved by this linearly shifted voltage, which is the VTC function. By quantizing the time duration into a digital code, the input voltage can be again expressed as equation (10).

In the end, the ramp voltage source as the ramp-signal generator achieves the same function with the current source method. In addition to that, the ramp voltage source can be easily shared.

By improving the circuit in Figure 11 into a differential version in Figure 13, our application can be well served. Figure 14 shows the waveform of the differential version of the circuit, which requires two opposite direction voltage ramps. The structure of the ramp voltage source is a current source charged capacitor which is followed by a source-follower to drive the following sharing circuits. The implementation details will be discussed in the following chapter.
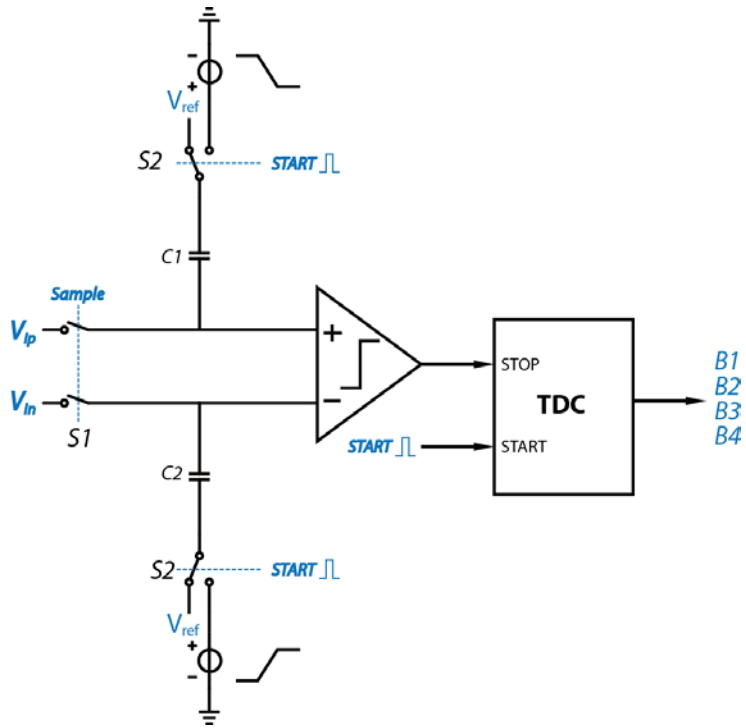
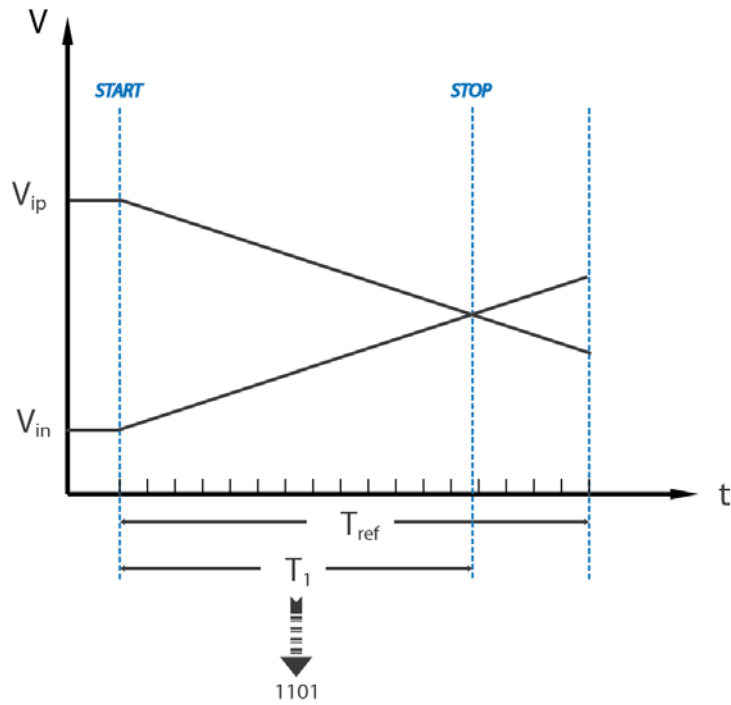**Figure 13 Differential Single-slope ADC with Voltage Ramp**

Figure 14 Waveform of a 4bit Differential SS ADC

3.2.2 Global Delay-line

The second part that could be shared is the delay-line of the TDC. Figure 15 shows the delay-line based TDC structure including a delay-line, a D flip-flop (DFF) chain and a thermal-to-binary encoder. The input pulse runs through the delay-line, until the stop signal latches all the results in the DFF chain. If in multiple TDCs the start signal comes at the same time, this input pulse will run through every single element of the delay-lines in ideally the same time duration. In other words, the delay-lines of the TDCs are doing the same job, which makes it possible to share them.
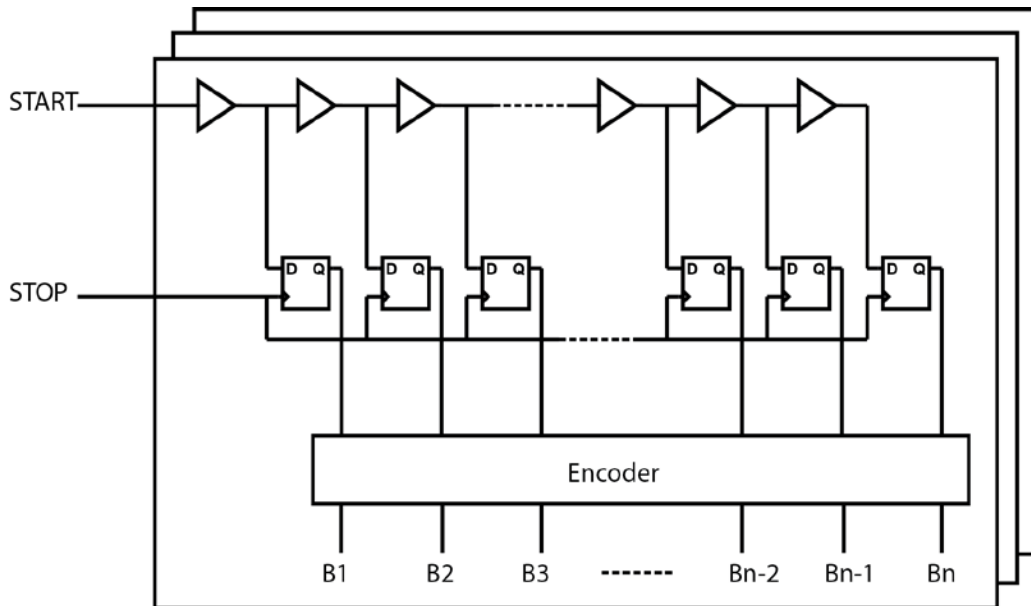

Figure 15 Delay-line TDC

Figure 16 shows the structure of the TDC with global delay-line. This shared structure saves not only area but also power consumption of the delay-line. In addition to that, all the TDCs share a uniform delay now.
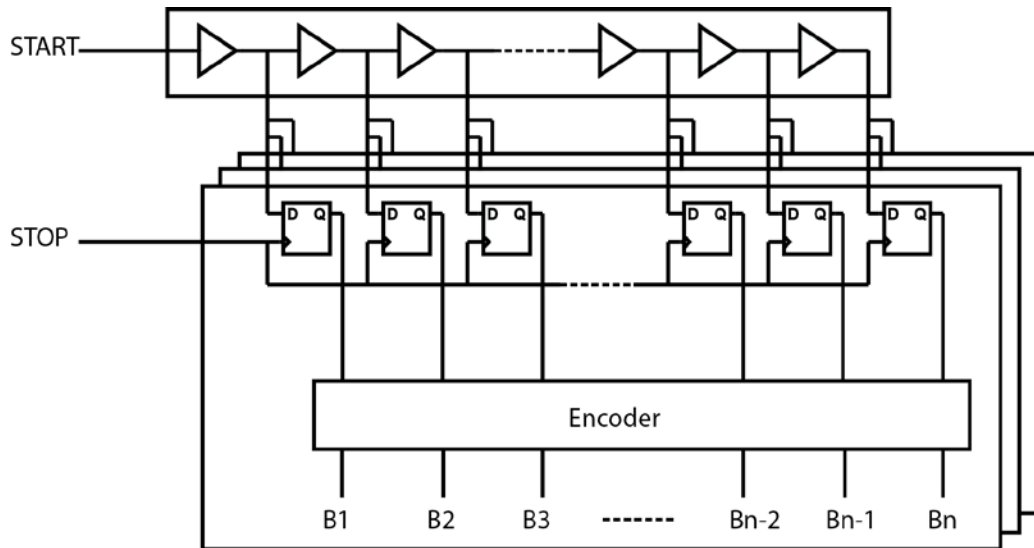
Figure 16 Global Delay-line TDC

Summary

In the end, in the shareable single-slope ADC structure, a ramp-signal generator based on ramp voltage source and a global delay-line are implemented.

3.3   Time and Resolution Division of the Hybrid SAR & Single-slope ADC

The hybrid ADC is obtained by combining the SAR ADC and the single-slope ADC together. As a result, the power consumption and area of the design would rank between the SAR and single-slope ADC. In order to achieve this design in the limited area with the minimum power consumption, both the resolution and working time of these two ADCs should be optimized. This is discussed in the following sections.

3.3.1   Resolution Division of the Hybrid ADC

While the most power efficient implementation would consist of a SAR ADC without single-slope structure, this is not feasible within the available chip area.

As discussed in section 3.1.1, the selected unit capacitance of the C-DAC in the SAR ADC is 73.5fF, with an area of around $7*7\mu m^2$. For a 6-bit resolution, the C-DAC area would be around $56*56\mu m^2$ excluding connections. This value is roughly a third of the area budget, which is considered too much. For a 5-bit C-DAC, the area would be roughly half of this size, which is considered to be acceptable. Since our principle is to utilize the SAR structure as much as possible, 5-bit is selected as the resolution of the SAR ADC. As a result, the resolution of the single-slope ADC is also determined as 4-bit.

3.3.2   Timing for SAR and Single-slope ADC

The power consumption of SAR and single-slope ADC is different and highly related to their working time. In order to optimize the power consumption of the entire ADC, the working time of these two structures should be determined.

The power consumption of the hybrid SAR single-slope ADC is divided into two parts:

1. Power consumption of the single-slope ADC, including the power consumed by a continuous-time comparator, and a TDC.
2. Power consumption of the SAR ADC, consisting of the power consumed by the dynamic comparator, and the SAR control logic.

To calculate the optimum point, a function that describes the relation between the power consumption and the working time should be defined. The method is organized as follows. Step 1, define the relation between the working time of the single-slope phase (T_{SS}) and its power consumption (P_{ss}). Step 2, find the relation between the power consumption(P_{SAR}) and working time of the SAR (T_{SAR}) conversion phase. Step 3, combine these two relations by the total conversion time relation $T_{conv} = T_{SS} + T_{SAR}$.

Step 1: Relation between power consumption and conversion time of single-slope conversion phase

The power consumption of the single-slope ADC is given by

$$P_{ss} = f(T_d, T_{d\_comp}) \tag{11}$$

$$P_{ss} = P_{TDC} + P_{comp} \tag{12}$$

$$T_{ss} = T_{TDC} + T_{d\_comp} = 2^N T_d + T_{d\_comp} \tag{13}$$

where T_d is the unit delay of the TDC of the single-slope ADC, $T_{d\text{-}comp}$ is the delay time of the continuous-time comparator, and P_{SS}, P_{TDC}, P_{comp} represent the power consumption of the single-slope step, the TDC, and the continuous-time comparator respectively.

In the analysis, it is difficult to directly calculate the relation between delay-time and power consumption of both the TDC and comparator. As a result, the relation is defined by doing a transistor-level circuit simulation. By recording the delay-time under different power consumption, the relation can be found.

For the comparator analysis, a self-biased inverter-based comparator structure is selected, which is shown in Figure 17. Due to its higher current efficiency, with the same comparing delay the inverter-based structure will consume less power, which makes the analysis more conservative. Since this is a self-biased structure, there are two ways to adjust the power consumption and then to influence the delay-time of the comparator. One is by resizing the input transistors, and the other is by sweeping the supply voltage. The latter one is obviously easier, and is also what we choose to do.
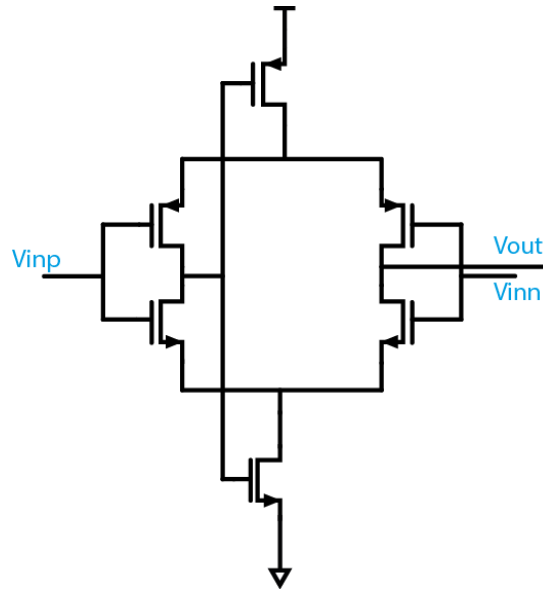
Figure 17 Continuous Time Comparator

Keeping the input signal the same, by sweeping the supply voltage of the comparator, the delay would be different. Then, record the value of power (the average supply current of the comparator times the corresponding supply voltage) and the corresponding delay-time as coordinate. The relation can be fitted in MATLAB as is shown in Figure 18.

In Figure 18, the red line is a 5th order polynomial fitted line. The delay-time of comparator changes from 17.8ns to 1.8ns. For smaller delay-time, the power consumption gets extremely large.
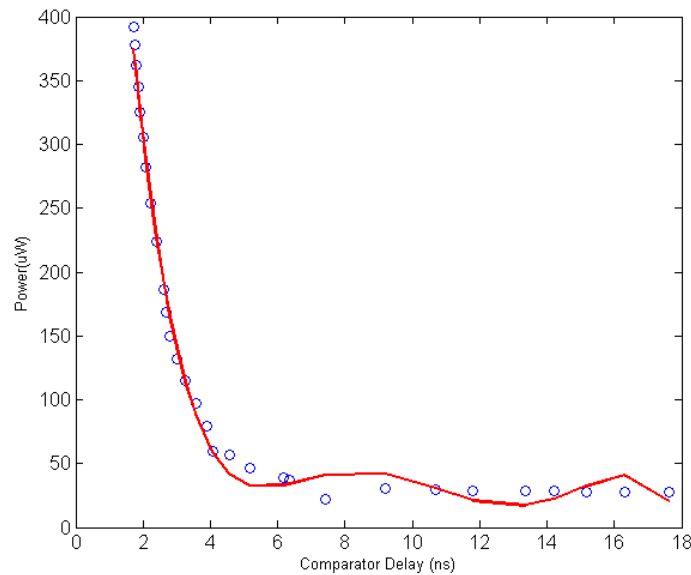

Figure 18 Comparator Power VS. Comparator Delay

In the analysis of the TDC, a 4-bit buffer-based delay-line is applied which is shown in Figure 19. By sweeping the supply voltage, the delay-time is changed. Then, record the value of power (the average supply current of one unit delay-element times the corresponding supply voltage) and the corresponding delay-time as coordinate. The delay-time of a single delay element is found by dividing the overall 4-bit delay-time from V_{in} to V_{out} by 16. The result is shown in Figure 20.

Figure 19 4 bit Delay Line

With the delay-time varying from 1.33ns to 2.12ns, the power consumption of a single delay element decreases to 16.5uW.
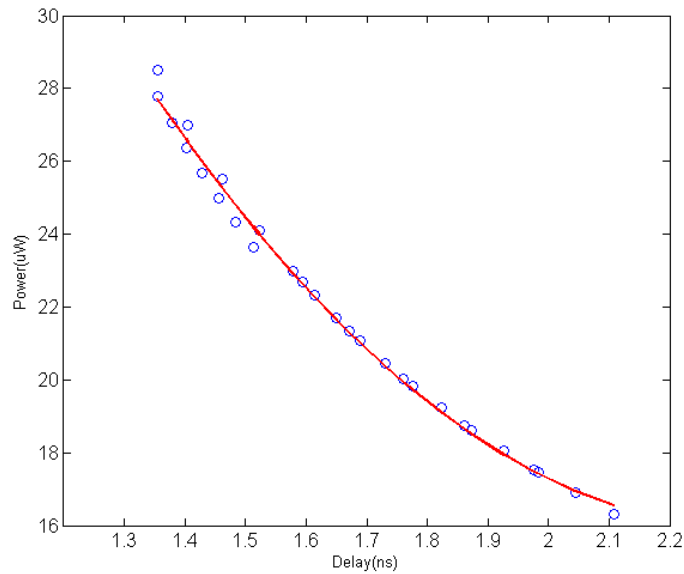

Figure 20 Delay Element Power VS. Delay

Since the relation is for a single delay-element, it can be translated to the power consumption of the complete delay-line by multiplying by 2^N (N is the resolution of the TDC). So far, the two parts of the power consumption of the single-slope phase (P_{comp}, P_{TDC}) have been discussed. There are three variables in the power functions: resolution, working time, and unit delay. In order to plot this three-variable relation, the controlled-variable method is applied.

The controlled variable in Figure 21 is the working time of the single-slope ADC, which is selected as 15ns. Then T_{d_comp} in equation (11) can be replaced by $(15 - T_d)$. As a result, the power consumption

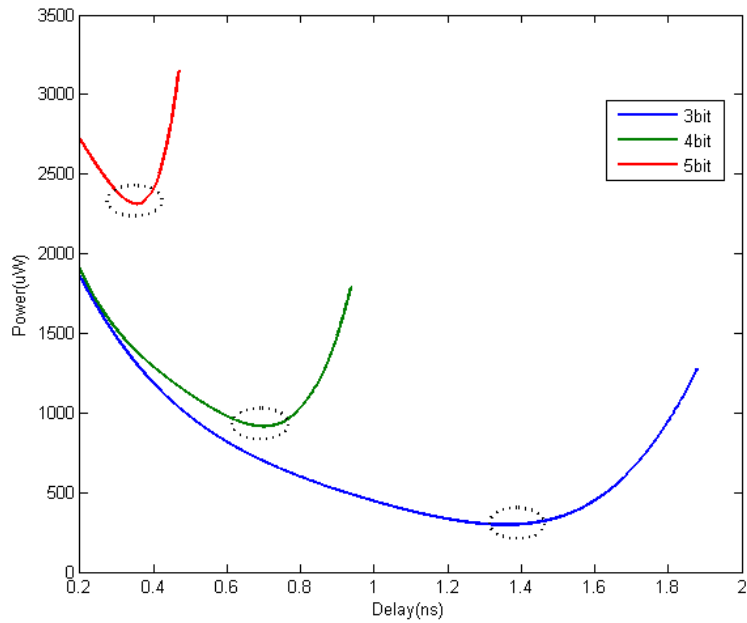functions of 3 to 5 bit single-slope ADC with 15ns working time are found, which are plotted in Figure 21.

Figure 21 Single-slope Power VS. Unit Delay (fixed working time)

Since the conversion time of the single-slope ADC is fixed at 15ns, the entire delay-time cannot be larger than this value. In other words, the unit delay should be less than this value divided by the member of delay elements.

Between the starting point and the optimum point, the power consumption is dominated by the TDC. The power consumption decreases with the increasing of the unit delay-time. The comparator power consumption is dominant in the right part between the optimum point to the ending point. The power consumption of the comparator increases because the delay time left for comparator is squeezed to zero.

The other controlled-variable in Figure 22 is the resolution which is set as 4-bit. In Figure 22, when the unit delay is selected like the orange arrow shown, the power consumed by the TDC is selected as well. As the conversion time is increased from 16ns to 20ns, more time remains for the comparator, which relaxes the power consumption.
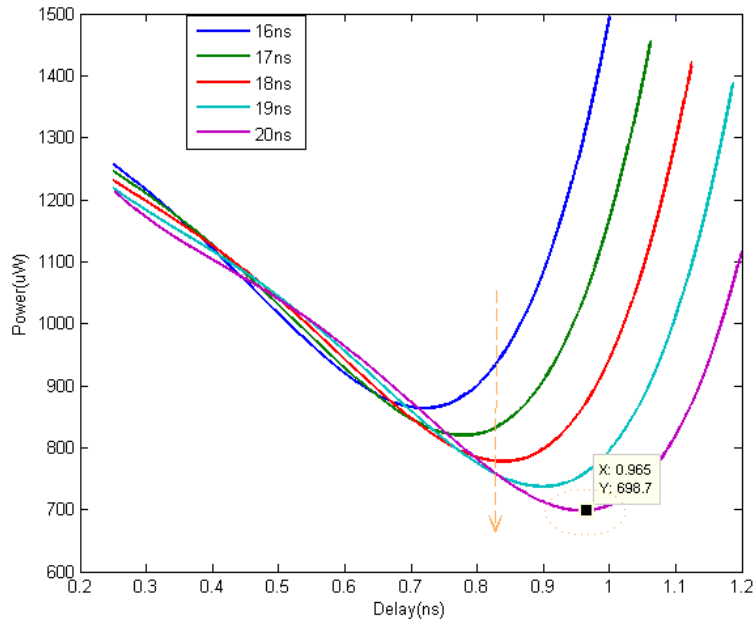
Figure 22 Single-slope Power VS. Unit Delay (fixed resolution)

Step 2: Relation between power consumption and working time of the SAR conversion phase

In the analysis of the SAR conversion, the relation between P_{SAR} and T_{SAR} can be deduced from figure of merit (FOM).

$$FOM = \frac{P_{SAR}}{2^{ENOB} \cdot f_S} \qquad (14)$$

where f_S is the sampling frequency. In our application, the resolution of the SAR ADC is 5-bit. In this calculation, it is treated as the 5 MSB bits of a 9-bit SAR ADC, which means ENOB is 9. In equation (10), in order to make the estimation conservative, the FOM is selected as 100fJ/step.

From the 5-bit SAR working time T_{SAR}, T_S and f_S can be expressed as equation(11) ,equation(12) .

$$T_S = \frac{9}{5} \cdot T_{SAR} \qquad (15)$$

$$f_S = \frac{1}{T_S} = \frac{1}{9/5 \cdot T_{SAR}} \qquad (16)$$

Deduced from equation(10) , P_{SAR} is given by:

$$P_{SAR} = \frac{FOM \cdot 2^{ENOB}}{9/5 \cdot T_{SAR}} \tag{17}$$

However, if the energy consumed by SAR ADC is considered, it is a constant value which is only relative to the resolution. In other words, SAR ADC consumes roughly constant value per conversion step. The reason is that the power consumed by the dynamic comparator and SAR control-logic circuits is instantaneous power. In the end, there is no relation between the energy dissipation (E_{SAR}) and the conversion time (T_{SAR}). Thus, since the SAR ADC consumes constant energy versus time, the longer conversion time of the single-slope ADC, the less energy consumption of the entire ADC. This is proved by the following step 3.

Step3: Combination of P_{SAR} and P_{SS}

Since there is no relation between the energy dissipation (W_{SAR}) and the conversion time (T_{SAR}), it is reasonable to combine the three parts power consumption (P_{comp}, P_{TDC}, P_{SAR}) in equation (14),

$$\begin{cases} P_{comp} = f_1(T_{ss} - 2^N \cdot T_d) \\ P_{TDC} = f_2(T_d) \\ P_{SAR} = f_3(30 - T_{ss}) \end{cases} \tag{18}$$

in energy domain.

As a result, the entire energy consumption of the ADC is given by equation (15)

$$E = E_{SAR} + E_{SS} = P_{SAR} \cdot T_{SAR} + P_{SS} \cdot T_{SS} \tag{19}$$

Sweeping T_{SS} from 15ns to 24ns, the relation between the entire energy dissipation of the entire hybrid ADC and the unit delay of the TDC is shown in Figure 26.
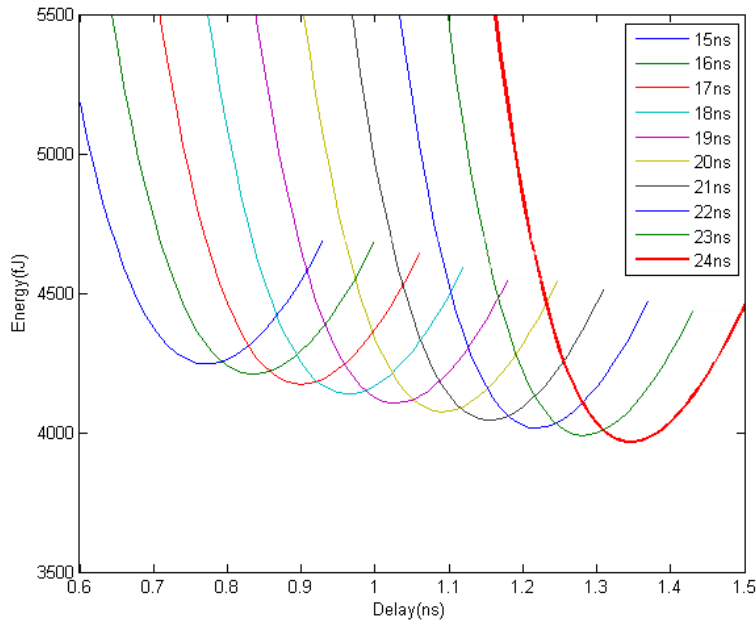
Figure 23 Energy of the ADC

Conclusion

Figure 23 shows that the entire energy consumption decreases with the increasing of the working time of the single-slope ADC (T_{SS}). Since the energy consumed by the 5-bit SAR ADC is constant, the longer time that the single-slope conversion takes in the 30ns, the lower energy would be consumed by the single-slope ADC and also the entire hybrid ADC. The most energy efficient point happens when SAR conversion takes no time, and all of the 30ns is utilized for the single-slope conversion.

In the end, the conclusion is that, in the entire analog-to-digital conversion, the SAR ADC should take the possible minimum working time with 5-bit resolution, and the single-slope ADC should take the rest conversion time with 4-bit resolution.

3.4   Combination of these two ADCs

As described in the previous section, the applied SAR ADC has top-plate sampling scheme and monotonic switching procedure. The single-slope ADC has a globally shared delay-line and ramp-generator. In this section, the combination these two ADCs is introduced.

The combined architecture of this 5-bit SAR and a 4-bit single-slope ADC is shown in Figure 24. Since in a SAR ADC the last capacitor of C-DAC is always connected to the switched reference, it is possible to utilize this capacitor as the share point between the SAR conversion and the single-slope conversion. In

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the SAR conversion, the bottom plate of this dummy capacitor is connected to V_{ref}. Then, the start signal comes, which switches this bottom plate to the ramp voltage.
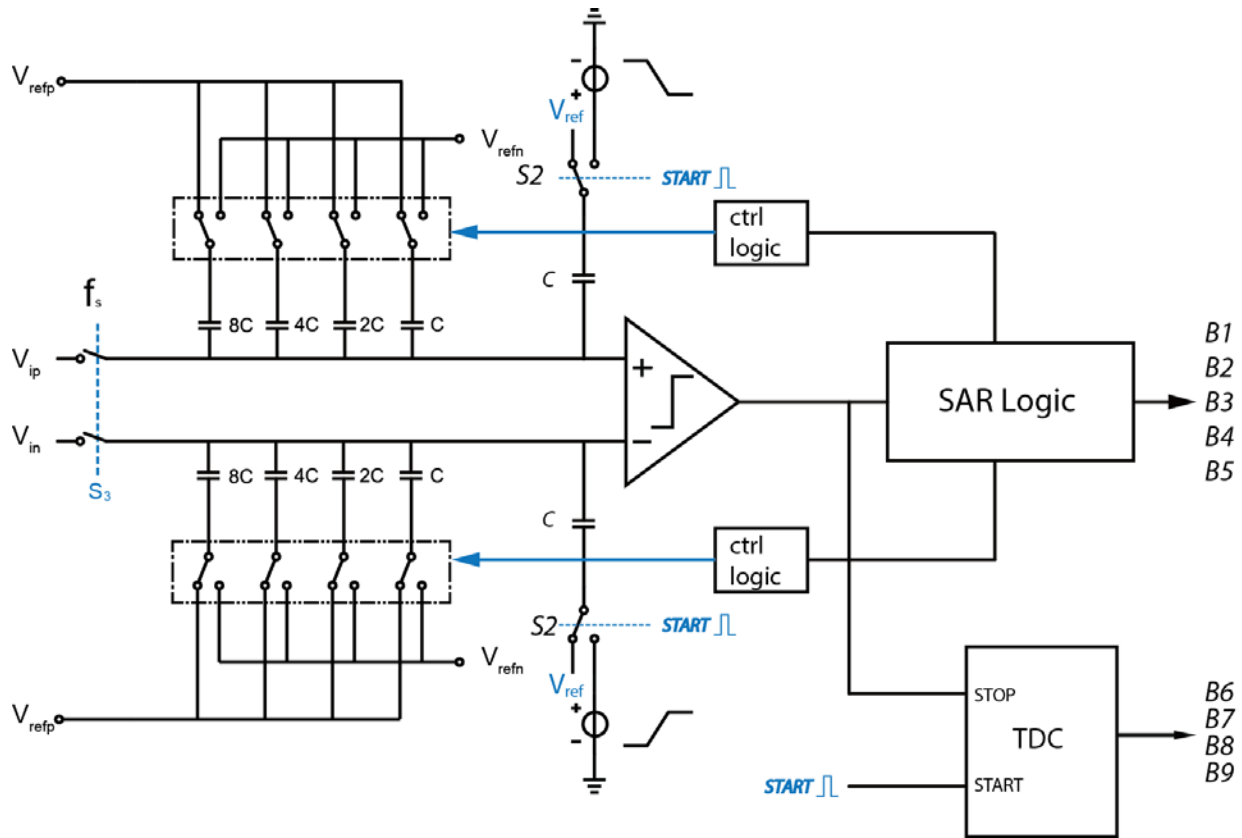

Figure 24 Hybrid SAR SS ADC Architecture Level Circuit (1)

Before the timing diagram is shown, two points in Figure 24 should be discussed first, one is the comparator, the other is the ramp-signal generator.

3.4.1 Comparator of the hybrid SAR SS ADC

In a SAR ADC, in order to save the power consumption, a dynamic comparator is applied because there is no static current in the structure. In a single-slope ADC, the dynamic comparator is unsuitable, because the dynamic comparator could introduce extra quantization error into the conversion. As a result, a continuous-time comparator is utilized.

In our application, if these two comparators are directly connected to the C-DAC, a pair of parasitic capacitors would be inevitably connected to the C-DAC. In addition to that, the input node of these two comparators would suffer different offset. In the worst case, if the difference between these two offset voltages is larger than the residue voltage on the C-DAC after the SAR conversion, there would be no valuable result from the single-slope conversion. In the end, a new comparator structure is required to combine these two comparators together. This combination is achieved by a shared pre-amplifier with one dynamic and one continuous-time second stage. Although the pre-amplifier increases the power

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consumption of the comparator, the offset problem can be addressed. This comparator has a shared differential input node, a differential output node of the dynamic comparator and a single-ended output node of the continuous-time comparator, which is shown in Figure 25. The implementation detail is discussed in the next chapter.
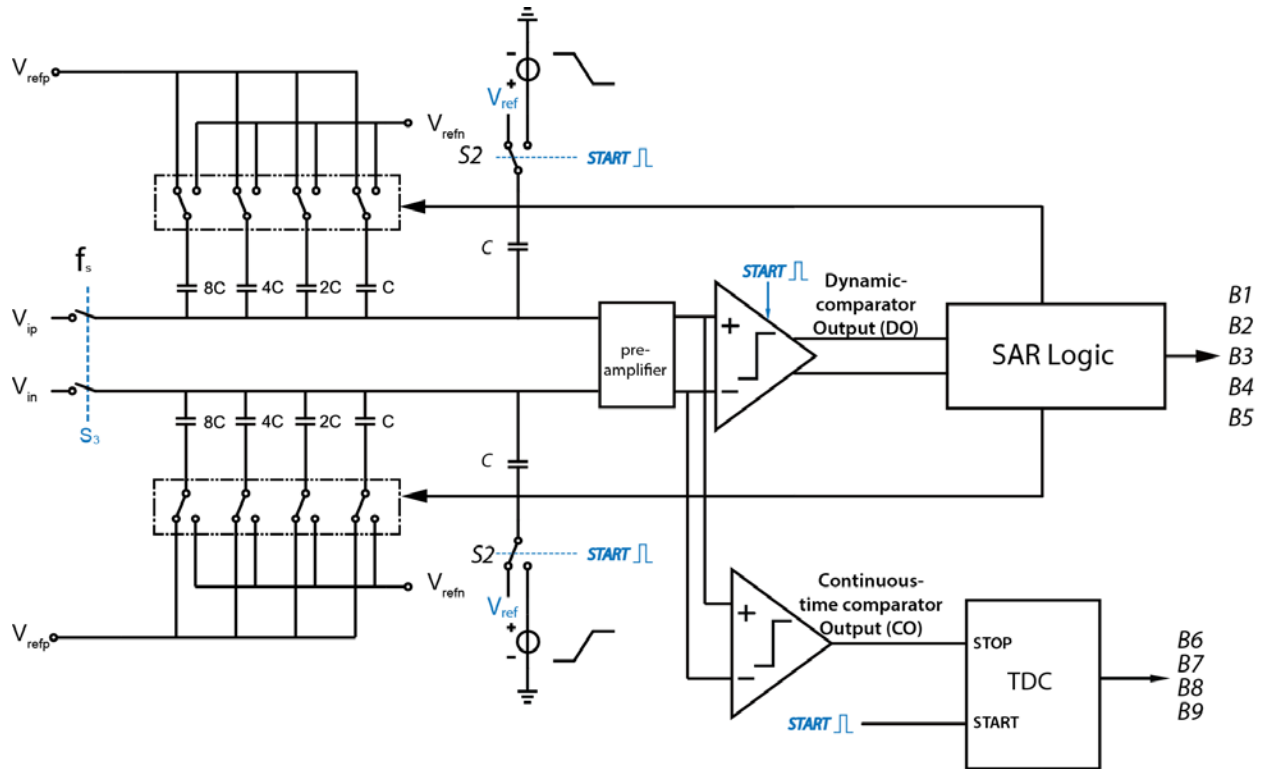

Figure 25 Hybrid SAR SS ADC Architecture Level Circuit (2)

3.4.2   Connection of the ramp-signal

The other point should be discussed is the ramp-signal. The ramp-signal in Figure 25 is simplified as only ramping down at the positive node, and ramping up at the negative node. However, in reality, the LSB of a SAR conversion (B5) can be one or zero, which means the positive input node could be both high and low. In order to make sure these two input nodes cross each other in the single-slope conversion, the ramping-down signal should be connected to the higher voltage node, and the ramping-up signal to the lower voltage node. Figure 26 shows one example. In Figure 26 (a), when the LSB is 0, V_{ip} should ramp up and V_{in} should ramp down; while in Figure 26 (b), V_{ip} should ramp down and V_{in} should ramp up.
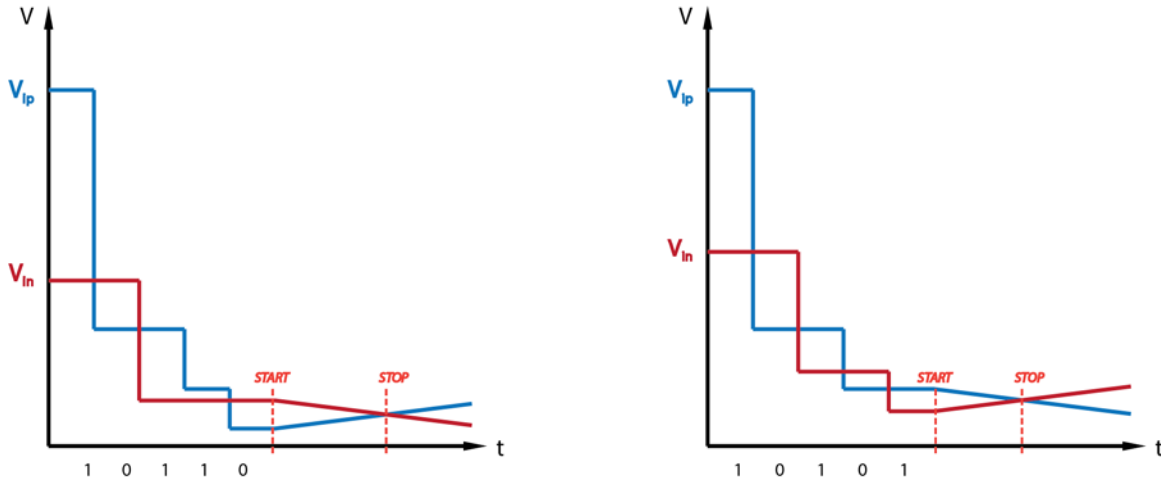
In this ramping procedure, the differential input signal can be described by the following equation:

$$V_{ip} - V_{in} = B_{out,SAR} \cdot V_{ref,SAR} + (-1)^{(1-B_5)} B_{out,SS} \cdot V_{ref,SS} \tag{20}$$

In order to implement this bi-directional ramping procedure, a chopper switch controlled by the LSB B5 is applied. In Figure 27, if B5 is 1, which means CP1 node is higher than CP2, CP1 is connected to VR1 to ramp down, and CP2 is connected to VR2 to ramp up. If B5 is 0, which means CP1 node is lower than CP2, Cp1 and CP2 nodes will swop the connections to VR2 and VR1 respectively.
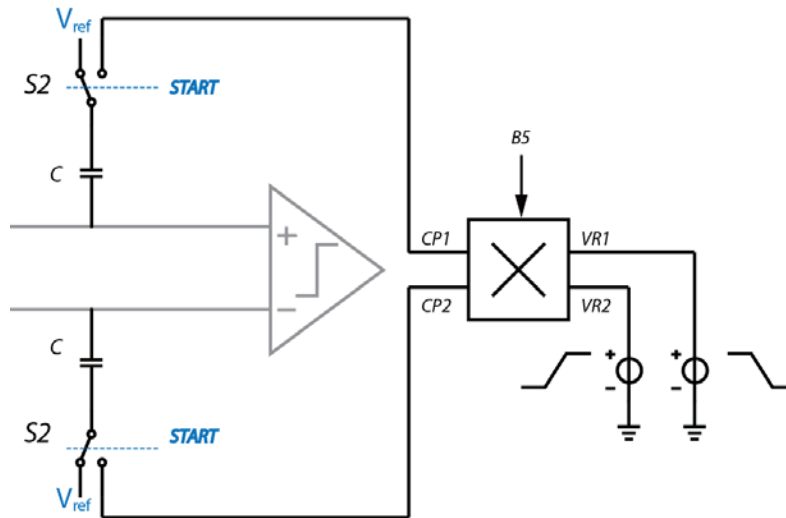
Figure 27 Ramp Selection by Chopper Switch

In our application, the ramp-signal generator is shared by different ADCs. Different results of B5 may cause crosstalk among these ADCs at the output node of the ramp-signal generator. In order to keep the output node of the ramp-signal generator clean, a better solution is found. One example is shown in Figure 28 to explain the operation. After the fifth comparison, B5 is zero, which controls the V_{ip} flips

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back 1 LSB of the SAR conversion. Compared with Figure 28 (a), the single-slope ADC conversion changes from directly quantizing the residue voltage of the SAR conversion to quantizing the subtraction of the residue voltage from one LSB of the SAR conversion. As a result, it is possible for each of the input nodes to connect to a fixed ramping direction.
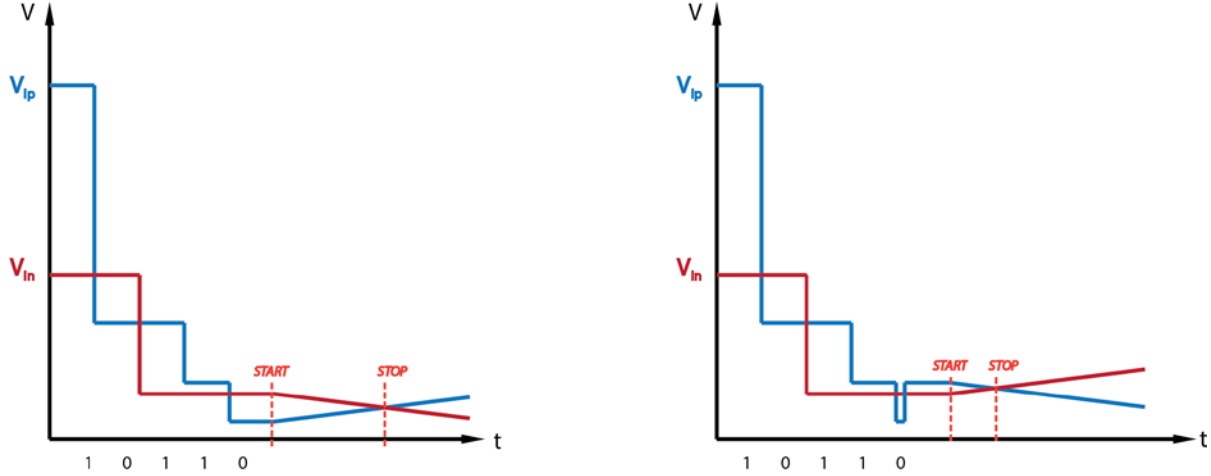

Figure 28 Final Bit Flip Over (a) and (b)

This relation is expressed in equation (21),

$$V_{ip} - V_{in} = B_{out,SAR} \cdot V_{ref,SAR} + \{(1 - B_5) \cdot (LSB_{SAR}) + (-1)^{(1-B_5)} B_{out,SS} \cdot V_{ref,SS}\} \qquad (21)$$

when B5 is 1, it is the same with equation (20). While if B5 is 0, the second part in equation (21) is (LSB – $B_{out,SS} V_{ref,SS}$), which is the subtraction of the single-slope conversion result from the LSB of SAR conversion.

3.4.3 Ramp-signal Over-ranging

In a SAR conversion, there are at most two times that the differential input voltage gets close to 0V. The noise and offset at the input node of the comparator may result in comparison errors, but for a pure SAR ADC, this kind of error will only lead to 1 LSB mistake of the outcome. For example, to a 5-bit SAR ADC, the error between the digital output code "11000" and "10111" is 1 LSB, and error between "11110" and "11111" is also 1 LSB. However, in our application, 1 LSB error in the coarse SAR ADC means 1 MSB error of the fine single-slope ADC, which is an unacceptable mistake. As a result, to address this problem, an over-range voltage is applied to the start point of the ramp-signal.

As shown in Figure 29, a small increment is introduced to the ramp-signal before it ramps down. While this small increment results in losing of some resolution, the value is quite small and acceptable. The implementation details of the over-range procedure will be introduced in the next chapter.
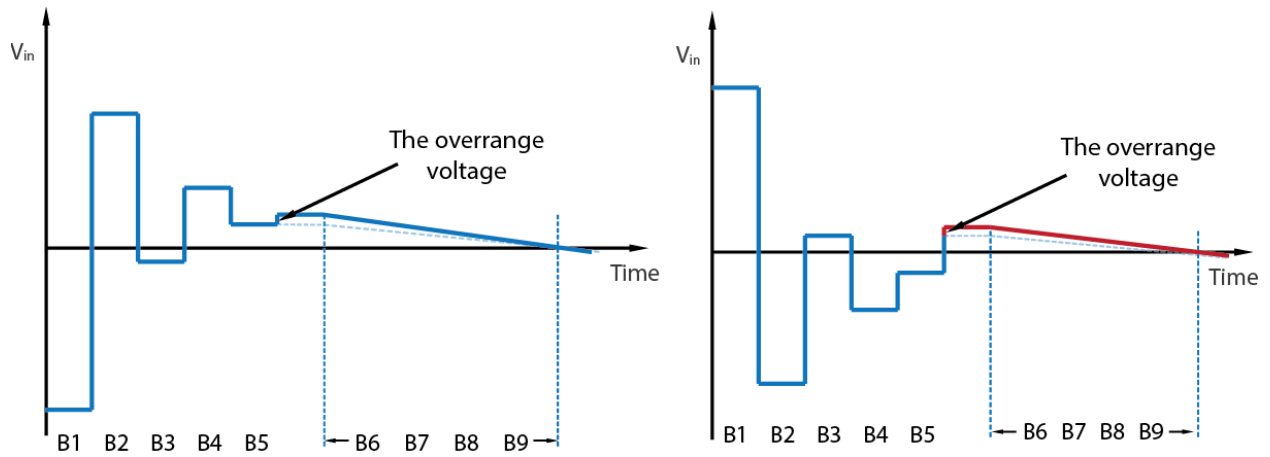
Figure 29 Over-range Procedure

3.4.4 Timing diagram of the hybrid SAR SS ADC

In the end, Figure 26 shows the timing diagram corresponding to the example mentioned in Figure 28 (b). In the timing diagram, the first three signals, reset, sampling phase, and trigger of the asynchronous of the SAR ADC, are generated by one 33MHz external clock signal with several custom designed delay elements. The signal start of the single-slope conversion is an external clock signal. The TDC working time duration is between the start and stop signal, which is the time duration when the comparator starts working and then provides the output.
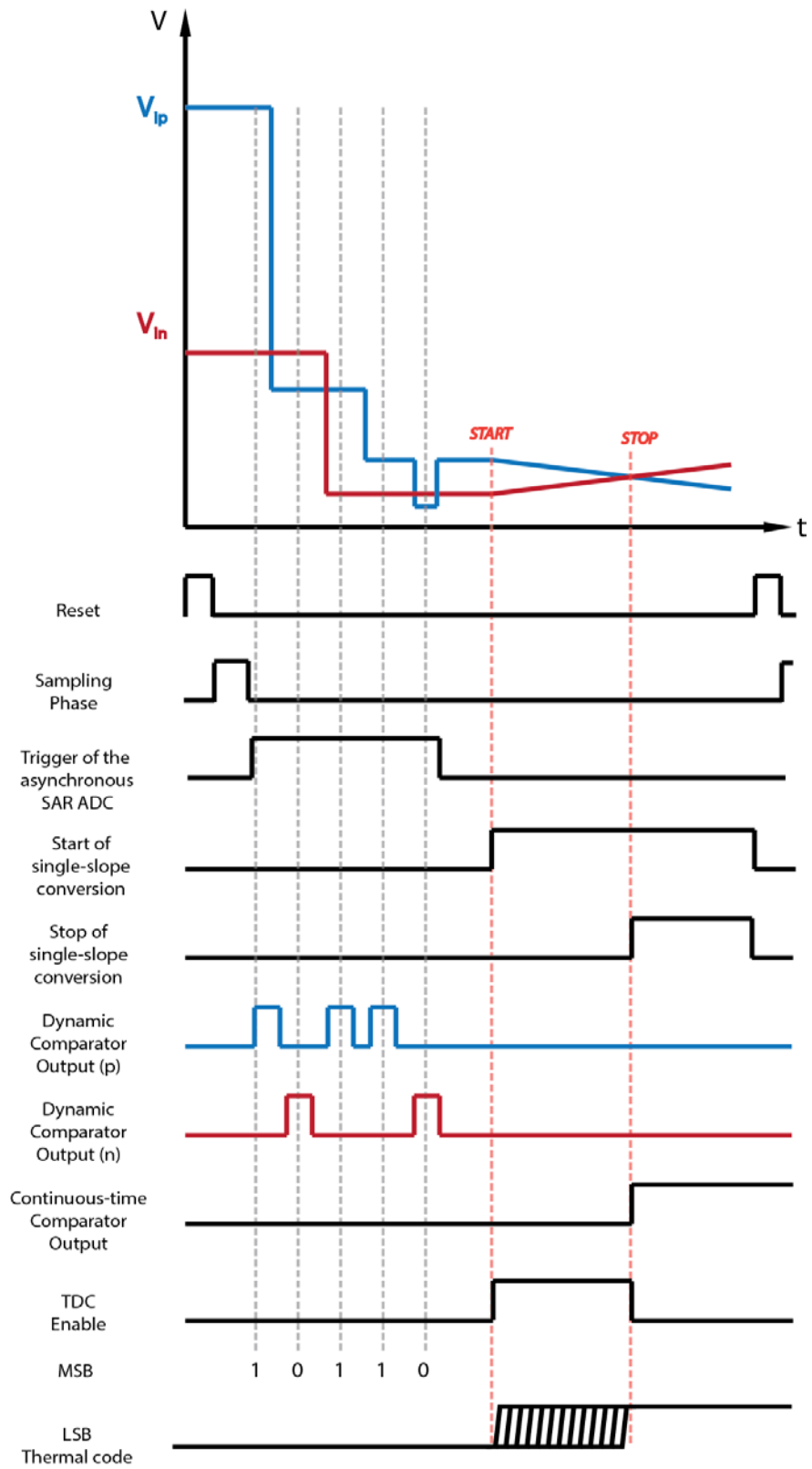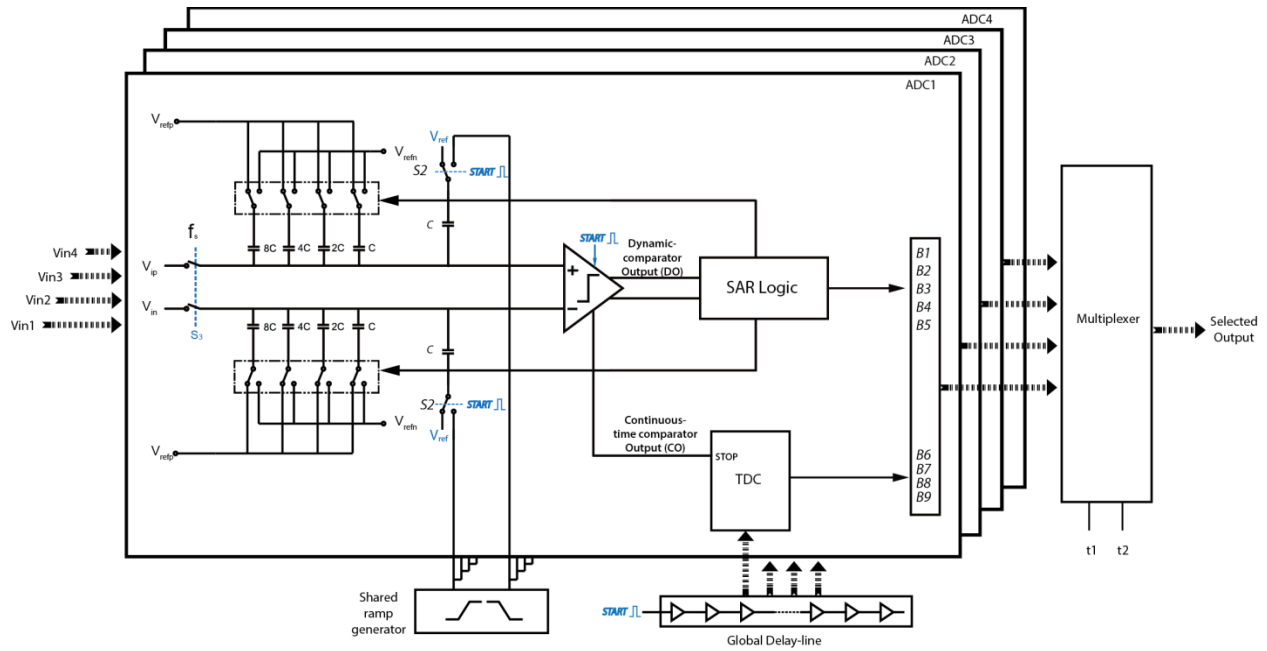
Figure 30 Timing Diagram of the Proposed ADC

Figure 31 2*2 ADC Array

Figure 31 shows a 2*2 ADC array with the shared ramp-signal generator and the global delay-line. The output signal of these 4 ADCs are selected by a multiplexer.

4. Circuit Design

After talking about the architecture of this ADC, the circuit design of each building block will be introduced in this chapter. This chapter is organized as follows. Section 4.1 describes the circuit design of the comparator including the shared preamplifier (section 4.1.1), the continuous-time comparator (section 4.1.2) and the dynamic comparator (section 4.1.3), and different noise analysis methods for the dynamic comparator and the continuous-time comparator. Section 4.2 then introduces the TDC design, including the global delay-line (section 4.2.1) and the two dimensional encoder (section 4.2.2). Compared with a traditional Wallace-tree encoder, the chip area of the proposed encoder is quite small. Section 4.3 describes the circuit design of the ramp-signal generator, including the current source design, source follower design, and the voltage over-range design. This chapter ends with timing-control circuit design in section 4.4.

4.1   Comparator Structure

As already mentioned in the previous chapter, a dynamic comparators and a static comparator are commonly applied for SAR and single-slope convertor, respectively. However, in our application, the two different types of comparators will introduce additional input offset and extra parasitic capacitance to the input nodes. In order to solve these problems, a shared preamplifier structure is selected in our design. The circuit design of the comparator will be discussed with three sections: preamplifier, continuous-time comparator, and dynamic comparator.

4.1.1   Preamplifier Design

Figure 32 shows the resistively loaded preamplifier. As the first stage of both the dynamic and continuous-time comparator, the speed of this stage is more important compared with the gain. In order to increase the speed of this stage, the value of the load two resistors is reduced, while, in the meantime, the gain of this preamplifier $g_m \cdot R$, is correspondingly reduced. In the end, the current consumption of preamplifier is 120μA. The gain of the preamplifier is 18dB, and the 3dB bandwidth is 38MHz.

Since this preamplifier is connected to a latch as the dynamic comparator and another gain stage as continuous-time comparator, the trade-off between gain and speed is not a big problem.
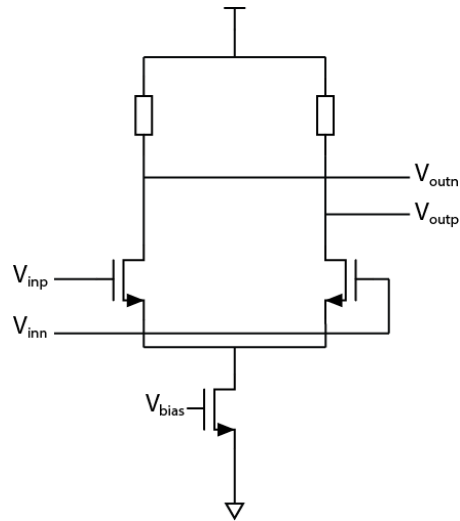
Figure 32 Preamplifier of the Comparator

However, in the simulation, the kickback noise of this structure influences the conversion voltage at the input nodes of the comparator. As shown in Figure 33, the voltage changes at the output nodes will transmit back to the input nodes through the capacitors C_{gd} of the input transistors, with the ratio C_{gd}/C-DAC.
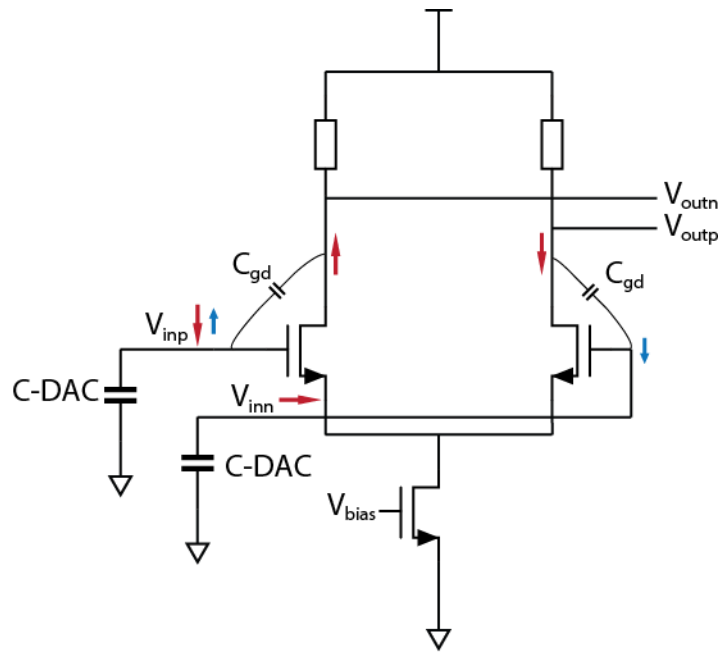
Figure 33 Kickback Noise at the Input node of the Preamplifier

Figure 34 shows the simulated voltage changes at the input nodes of the comparator, which are sampled at 1.2V, and 1V respectively at the beginning. As already mentioned above, the monotonic switching scheme is applied here, which means there should be only one input node of the comparator changing at one time. An example is shown in Figure 34, the red curve is the voltage of the positive input node of the

C-DAC V_{inp}, and the blue curve is the negative input node of the C-DAC V_{inn}. Since the V_{inp} is higher than V_{inn}, the V_{inn} should be stable.
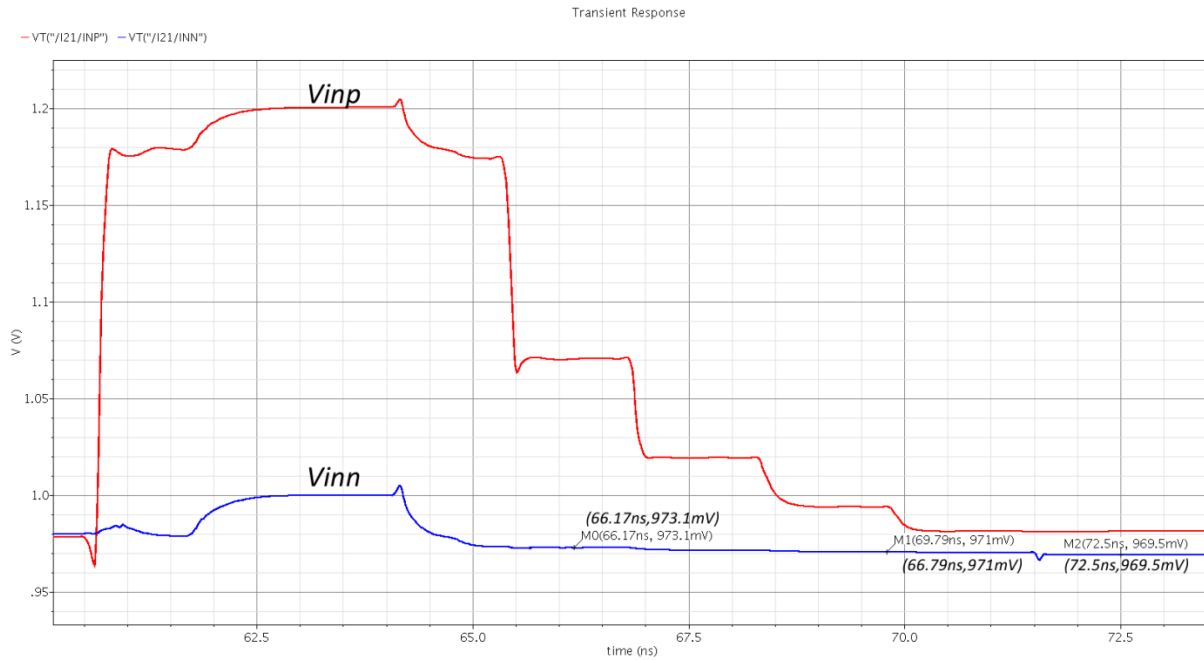
Figure 34 Input Voltages of the Comparator during SAR Conversion

However, from the marks being labelled in Figure 34, the negative input node V_{inn} is slightly going down. This error is due to the kickback noise we mentioned above, that the voltage reducing at the positive input node V_{inp} makes the negative input node voltage reduced.

What is worse, this is not a common-mode voltage change. Figure 36 shows impact of the kickback noise on the differential voltage of the input nodes. From the annotated voltage level, we can find out that the error of the voltage change in each conversion is larger than one LSB (around 0.8mV). As a result, the residue voltage of the SAR conversion, which is also the input voltage of the single-slope convertor is not correct. In the end, the input voltage can never be recovered, which means this ADC is not working properly.
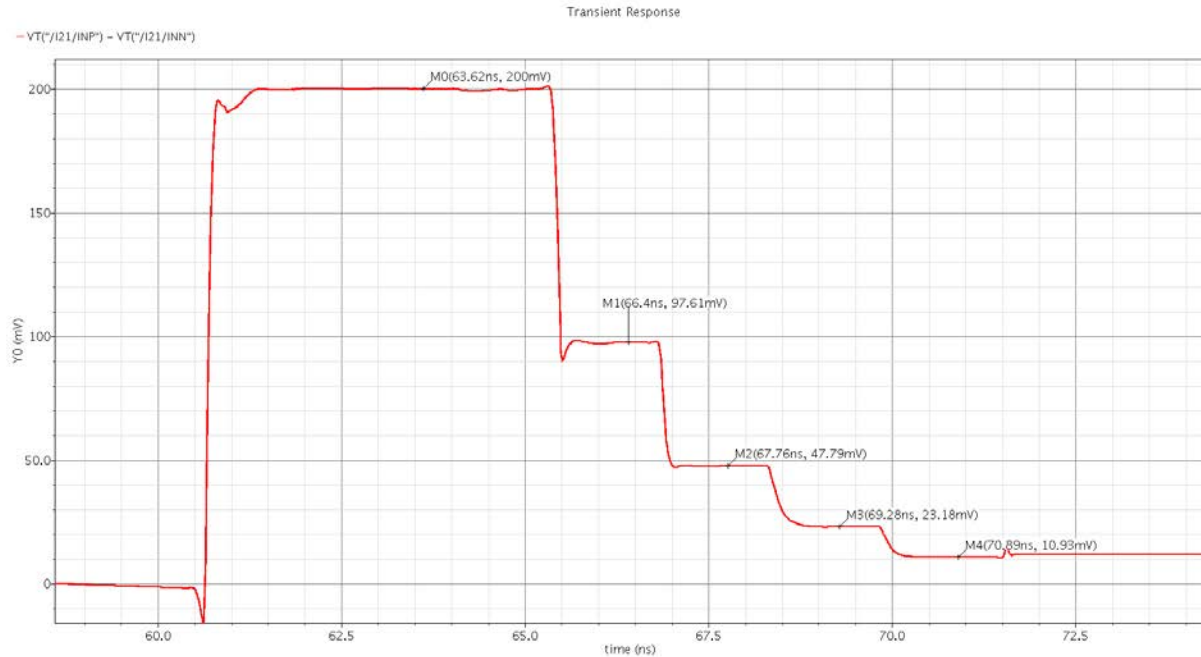
Figure 35 Differential Input Voltage of the Comparator

In order to weaken the connection between the output node and the input node, a cascode transistor is applied, as shown in Figure 37. As a result, the impact of the output nodes can be neglected.
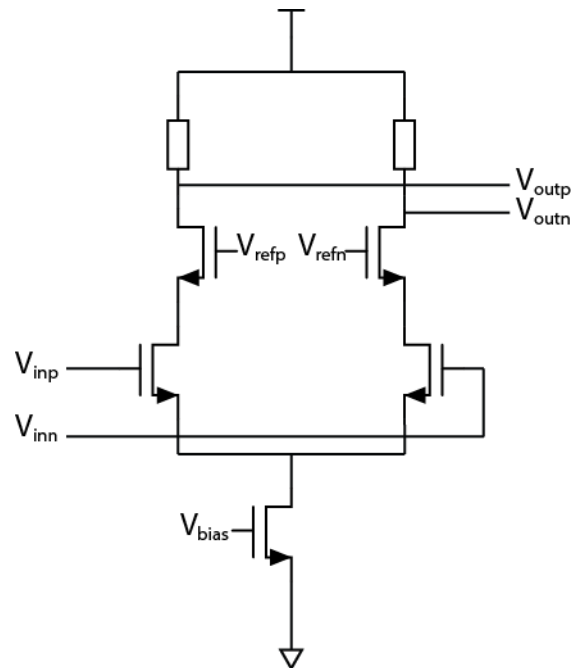
Figure 36 Cascoded Resistive Load Preamplifier

Figure 38 shows the differential voltage of the input nodes of the comparator. With the help of the cascode transistor, the error of voltage change in each conversion step is less than one LSB. Consequently, we can conclude that the kickback noise problem is solved.
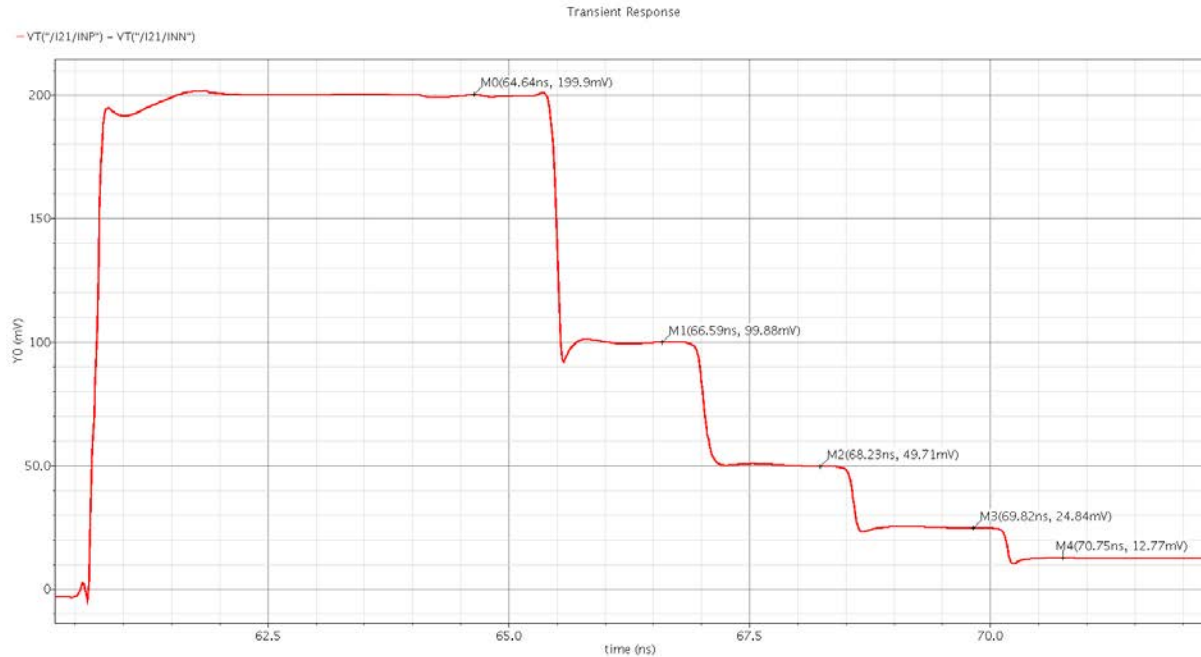
Figure 37 Differential Input Voltage of the Comparator

4.1.2 Continuous-time Comparator

The structure of the continuous-time comparator is shown in Figure 39. The first stage of this structure is the shared preamplifier, and the following two stages are used to provide enough gain to generate a rail-to-rail output signal. The DC gain of this three-stage structure is 71dB.

Figure 38 Continuous-time Comparator

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As already mentioned in section 3.4.2, the voltage of the positive input node of the comparator is always higher than the negative one. As a result, during the single-slope conversion, the positive output node of the comparator always outputs an increasing signal. The output signal of the comparator stands for the crossing moment of 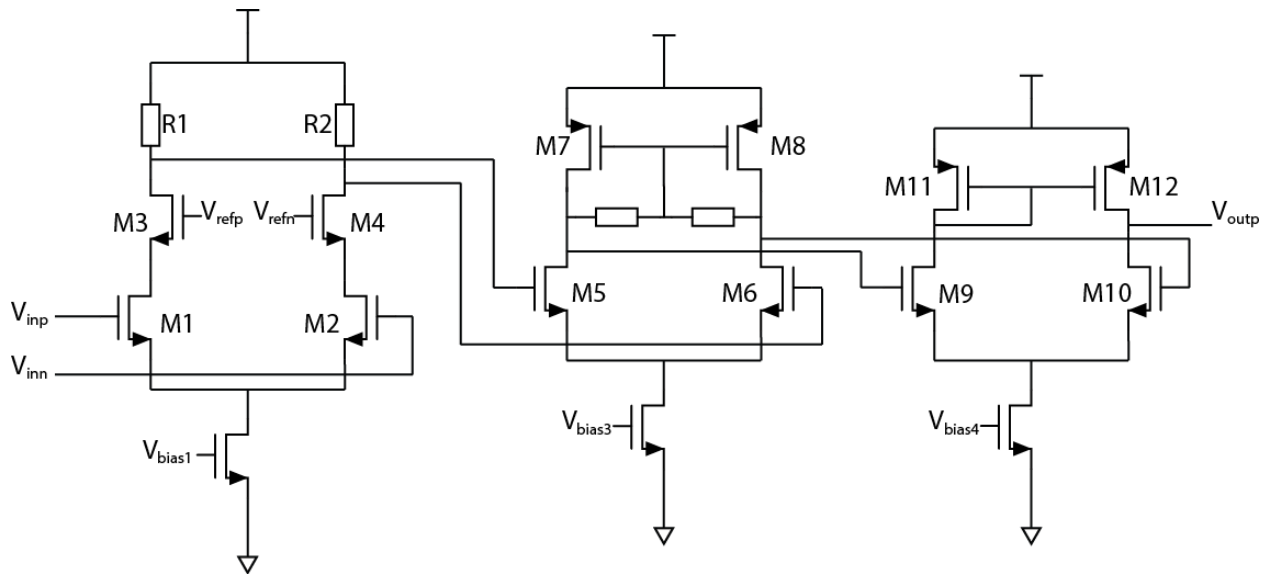the input signals, which is supposed to be used as the stop signal to latch the results of the delay-line. The delay-time of the comparator is shown in Figure 40, which is around 2.2ns. Compared with the 15ns single-slope conversion time, this delay time is acceptable.
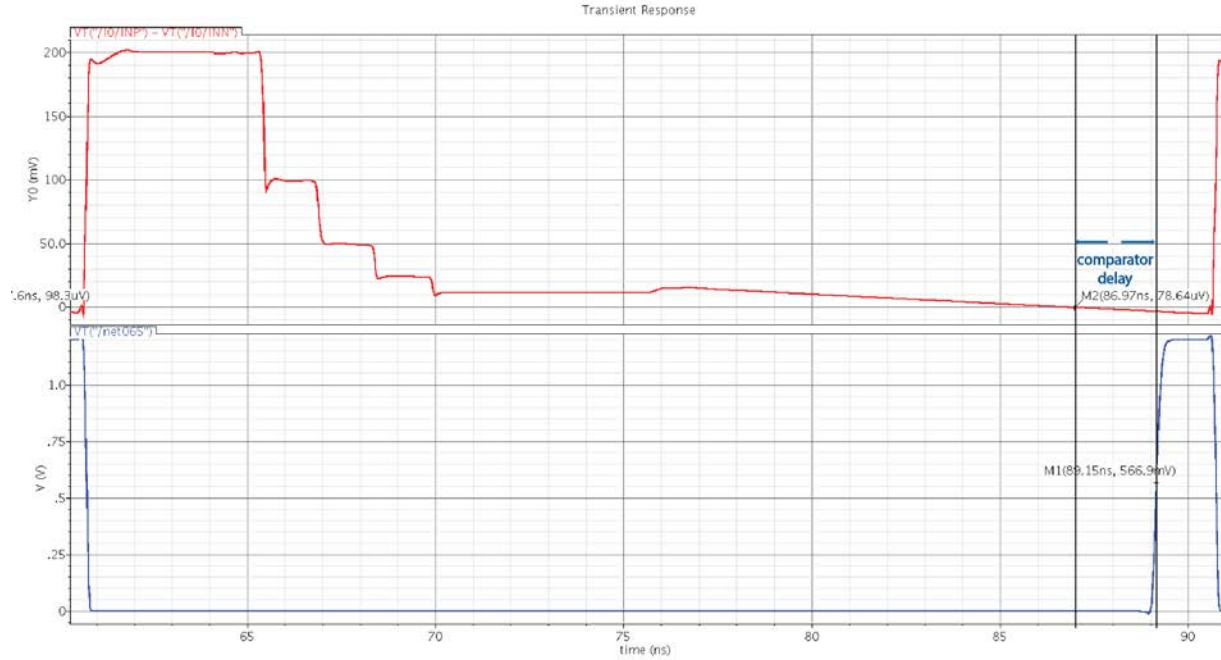

Figure 39 Continuous-time Comparator Delay-time

The noise analysis of comparator-based circuits is different from the traditional steady-state noise analysis method. The traditional noise analysis method is based on the assumption that the amplifier is in steady-state and even small signal, while comparators do not necessarily reach steady state and add noise throughout the operation. In other words, the comparator noise depends on the transient response, so the variance and the time-averaged root-mean-square (RMS) value of the noise is not static with time.

In order to estimate the noise value, a noise analysis model should be made. In [36], since the preamplifier of a comparator dominates both the noise performance and the delay-time, a noise analysis model consisting of a preamplifier is made. The input referred noise power can be given by:

$$\overline{v_{in,ZCD}^2}(t_R) = 4kTR_n \cdot \frac{1}{4\tau}\coth(\frac{t_R}{2\tau}) \tag{22}$$

where R_n is input-referred thermal noise resistance in usual transconductance amplifiers, τ is the time constant at the output node of the transconductance amplifier, t_R is the delay-time of the preamplifier.

From the transient simulation results of the preamplifier, the g_m is around 1mS, R_L is 10KΩ t_R is around 0.2ns, and τ is around 0.01ns.Combining equation (22) and the simulation results, an input referred RMS noise voltage around 300uV is found, which is smaller than ½ LSB of the ADC.

4.1.3 Dynamic Comparator

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Figure 41 shows the structure of the applied dynamic comparator, which is the preamplifier shown in Figure 37 with a dynamic latch as the second stage. The transistors M5 and M6 are the input transistors of the second stage, which transfers the voltage difference of the output nodes of the preamplifier into the current difference. This current difference will break the balance of the positive feedback connected latch, when the falling CLK signal comes and generates the output signals. After the CLK signal returns back to high stage, the total equivalent capacitance of the output nodes will be discharged, and the output voltage will reset to zero.
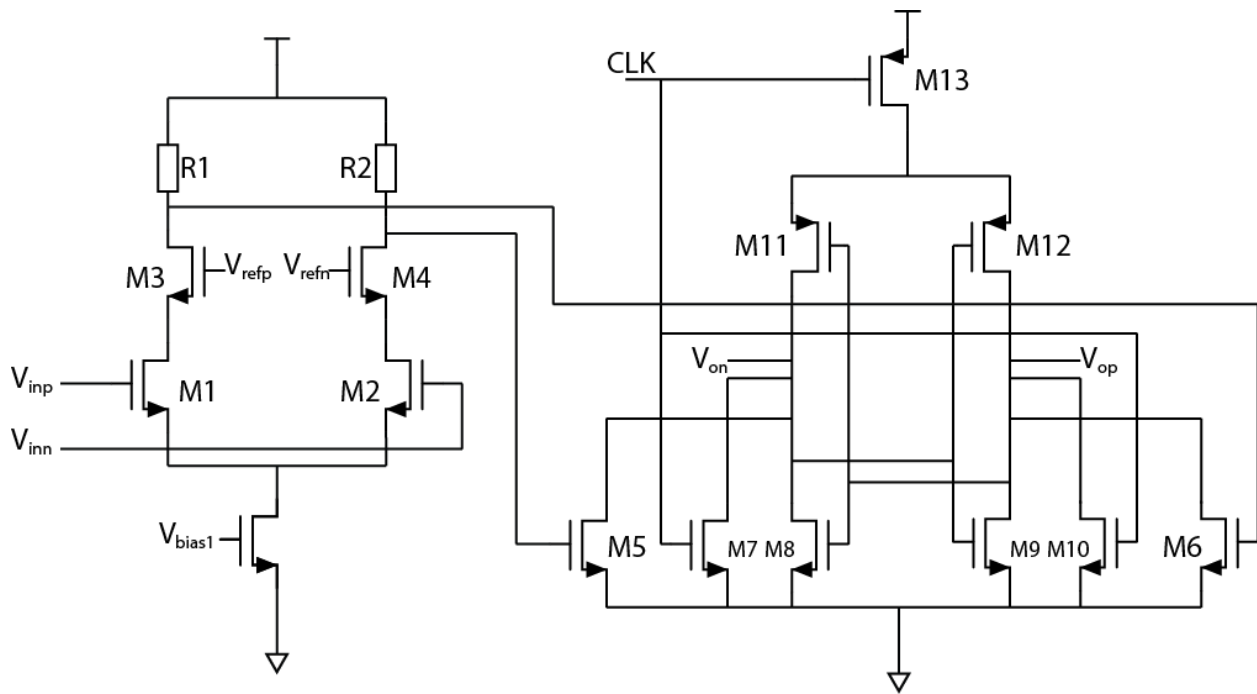
Figure 40 Dynamic Comparator

The noise analysis of dynamic comparator is different from that of continuous-time comparators. In our application, noise of the dynamic comparator is simulated with transient noise analysis. The input voltage is swept from several microvolts to several millivolts. For each input voltage, a number of comparison events occur. Since the input voltage is quite small, only part of the comparison results is correct. In order to count the number of correct comparisons, a test bench has been designed, as shown in Figure 42.
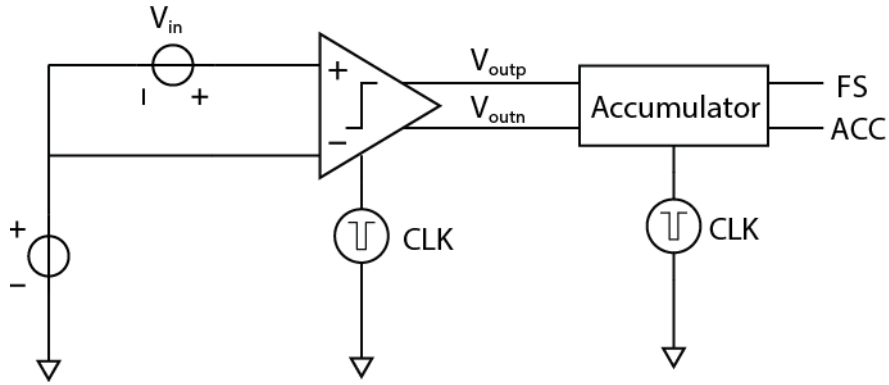
Figure 41 Test Bench of the Dynamic Comparator Noise Analysis

The accumulator is implemented with Verilog-A. FS and ACC nodes are utilized counting the correct comparison number and the total comparison number, respectively. As a result, the correct comparison ratio can be defined as ACC/FS. In the first approximation, since the noise source is mainly thermal noise, the distribution of the correct decisions must resemble a normal distribution.

For example, if the input voltage V_{in} is 0V, the correct comparison ratio should be 50%. With the increasing of the positive input voltage, the ratio also increases. When the correct comparison ratio is 67.7%, the input referred RMS noise voltage of the dynamic comparator should equal to V_{in}. In the end, the RMS noise voltage can be simulated.

As shown in Figure 43, the ratio of ACC/FS is illustrated as the yellow curve at bottom, which approaches 67.7% after 500 comparisons. As a result, the input referred RMS noise voltage of the comparator is the input voltage at the time, which is 90uV.

Figure 42 Transient Noise Simulation Result

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In our design, in order to minimized the noise of the dynamic comparator, the following guidelines are considered [37]:

- Increasing the ratio W/L of the transistors M5 and M6 in Figure 41.
- Decreasing the overdrive voltage of the input transistors of the dynamic latch which are M5 and M6 as well.
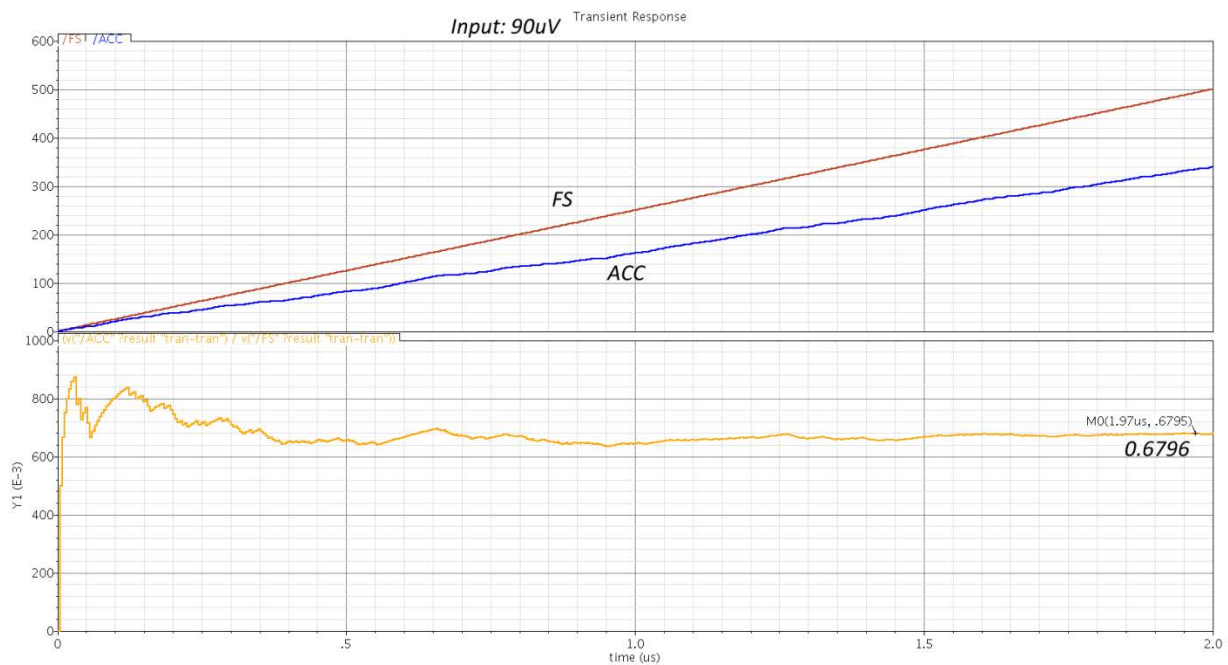- Optimize the common mode voltage of M5 and M6 for a minimum noise value.

4.2 TDC design

In the TDC design, a delay-line based TDC, which consists of a delay-line, a latch-line, and a thermometer-to-binary encoder, is applied.

4.2.1 Global Shared Delay-line

For the application of the global delay-line shown in Figure 16, there is one issue in the circuit design should be considered, that the controlling of the delay time of the delay-line. In 0.18µm TSMC CMOS technology, the minimum delay time of the buffer (a collection of two invertors) at 1.8V as the supply voltage is around 100ps, which is quite small compared with our design target. The required delay time can be adjusted, by tuning the supply voltage of the delay-line. The working time of single-slope phase is around 15ns. By decreasing the supply voltage to 690mV, the delay time gets close to 13ns, which is suitable for our application. As a result, the delay-line is powered by a separate supply voltage. Considering the digital supply voltage is 1.2V, it can be difficult for the output nodes of the delay-line to drive the following stage, which is latching stage to store the results of the delay elements. In order to drive the following latch-line, a voltage level-shifter from 690mV to 1.2V is applied to each of the delay elements.

4.2.2 Encoder Design

The output code of the TDC is a thermometer code, which should be mapped into a straight binary code. The most commonly used encoding scheme is the Wallace-tree encoder [38]. Although it is mentioned in [38], [39] that the Wallace tree is the simplest and the most area efficient way to implement this encoding scheme, the complexity of this approach is still a disadvantage of this method. Due to this complexity problem, the chip area of this encoder increases exponentially with the number of input. The required number of full-adder cells can be calculated by,

$$X_N = \sum_{i=1}^{N}(i-1) \cdot 2^{(N-1)} \tag{23}$$

where N is the resolution, which is 4.1 in our application. As a result, 16 full-adder cells are needed.

To implement a full-adder, 9 NAND logic gates are required, which is almost twice as much as a D flip-flop. In the end, the encoder will dominate the chip area of the TDC. In order to reduce the chip area consumption, a new type of encoder is proposed here.

The encoding algorithm is processed by counting the number of ones in the thermometer codes with full-adders. In the classical Wallace tree encoder, the input signals are treated as one dimensional. For example, in our application, the 16 inputs are counted from 1 to 16. While in this proposed encoding method, the input signals are counted as a 2D matrix, from "11" to "44", which is also 16 inputs. In other words, the input signals are counted in both horizontal and vertical directions.

The out bit in each row Y_{out} in Figure 44 indicates whether the row is full. Each full row accounts for 4 ones in the input, so the end-of-row bits can be used to derive the MSBs of the binary code. The LSBs can be obtained by looking at the number of ones in the first non-full row. v

An example is shown in Figure 44, there are 10 ones in the input signals, which means there are two full rows and the MSBs of the binary output signal is supposed to be "10". For the first non-full row, there are two ones, so the LSBs of the binary output signal are supposed to be "10" as well. As a result, the 4-bit binary output signal is "1010". For our application, the input is counted from "0001" to the maximum value "1111" which is 15, but there are 16 elements should be counted in our delay-line. In the end, one extra output bit is introduced, in the encoder, leading to a "4.1-bit" code, to output the "10000", when there are 16 ones, which is the green numbers in Figure 44.

IN	X1	X2	X3	X4	Y_{out}	MSB
1X	1	1	1	1	1	
2X	1	1	1	1	1	10
3X	1	1	0	0	0	
4X	0	0	0	0	0	4.1bit
X_{out}	1	1	0	0	4.1bit outcome 01010	
LSB		10		4.1bit		

Figure 43 An Example of the Proposed Encoder.

In order to achieve this encoding algorithm, only two full-adders and some other logic gates are required, which are quite compact compared with the classical Wallace tree encoder consisting of 144 NAND gates (9*16). Figure 45 shows the circuit level implementation of the proposed encoder, the number of applied NOR and OR gates is 42, which is much smaller compared with the classical Wallace tree encoder.
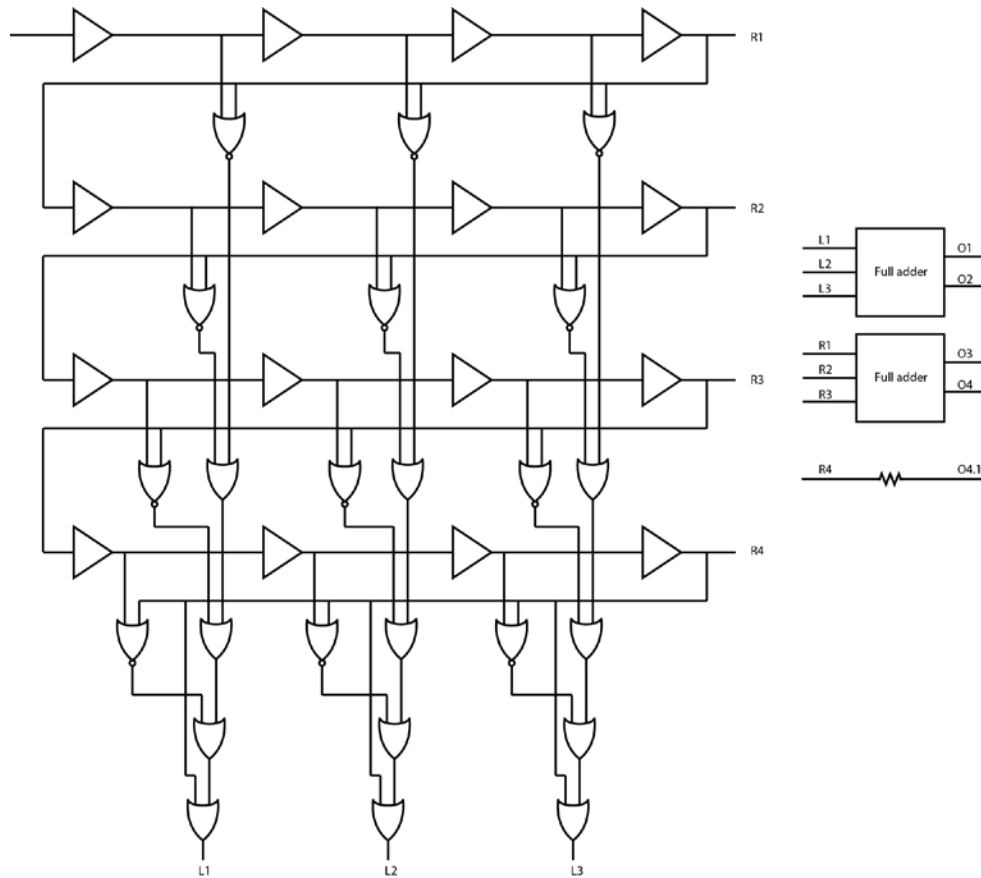
Figure 44 Circuit Level Implementation

4.3 Voltage Ramp Generator

As already mentioned in the previous chapter, the ramp-signal generator is implemented by a current source charged capacitor followed by a source follower. Since the linearity of the single-slope conversion is directly influenced by the linearity of the ramp-signal, the circuit design of the ramp-signal generator is quite important as well.

The nonlinearity of the ramp-signal generator is mainly contributed by two parts: one is the current source, the other is the source follower.

4.3.1 Current Source Design

In the system level design, the current source applied to charge the capacitor is regarded as an ideal current source with infinite output impedance, while in the circuit level design this output impedance is not large enough and changes slightly with the voltage at the output of the current source. In order to improve the impedance of the current source, the cascoded current mirror structure is utilized, which is shown in Figure 46.

With the help of the cascoded transistors, the simulated current change during the charging procedure is much less than 13nA, which is the current value that can lead to an LSB voltage error at the voltage ramp-signal generator, guaranteeing sufficient linearity of the current source.
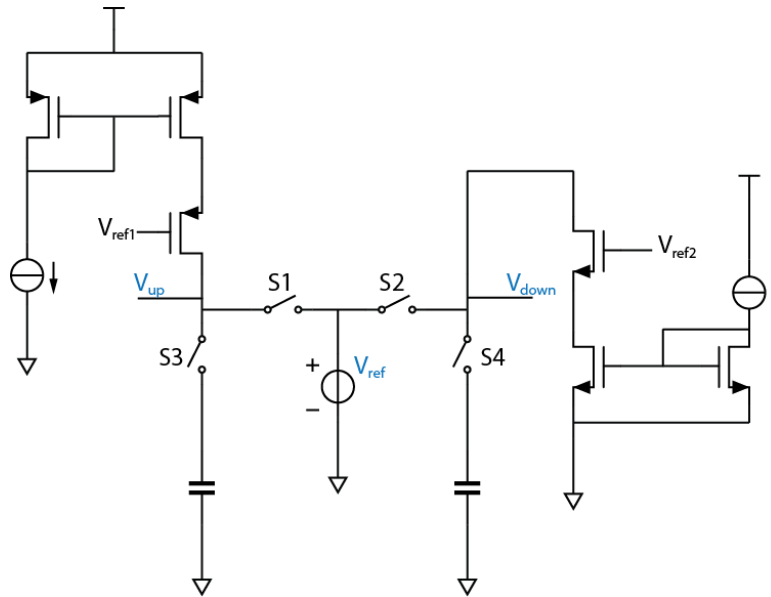
Figure 45 Cascoded Current Mirror

4.3.2   Ramp-signal Over-ranging Design

As already introduced in section 3.4.3, the purpose of the ramp-signal over-ranging is to compensate for the comparing errors that are caused by the offset of the comparator. As shown in Figure 29, the differential input voltage is shifted up by a certain value. As shown in Figure 47, this voltage shift depends both on the resistance of R1, R2, and the current level.

Figure 46 Implement of the Voltage Over-range

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In the SAR conversion phase, switches S3, S4 and A2, B2 are on, so the voltage value at the nodes V_{up} and V_{down} are equal to V_{ref}. Then, in the single-slope conversion phase, switches A1 and B1 are on, and A2, B2 and S3, S4 are off. Thus, there will be a voltage drop of the value $R1 \cdot I_{push}$ for V_{up} and a voltage rise of the value $R2 \cdot I_{pull}$ for V_{down}. These voltage changes of V_{down} and V_{up} are shown in Figure 48.
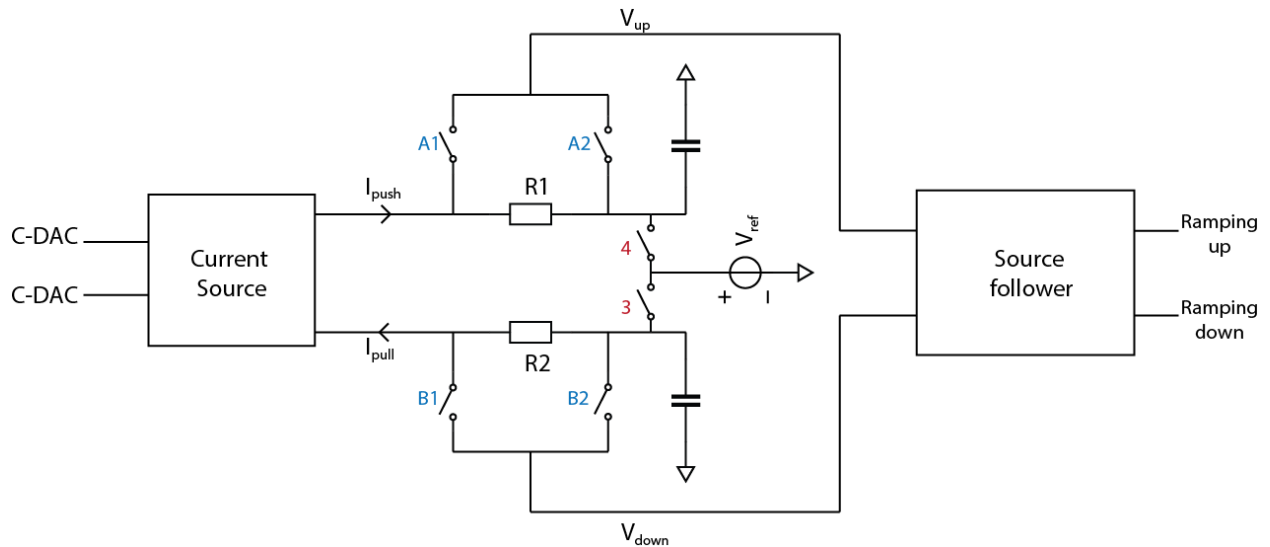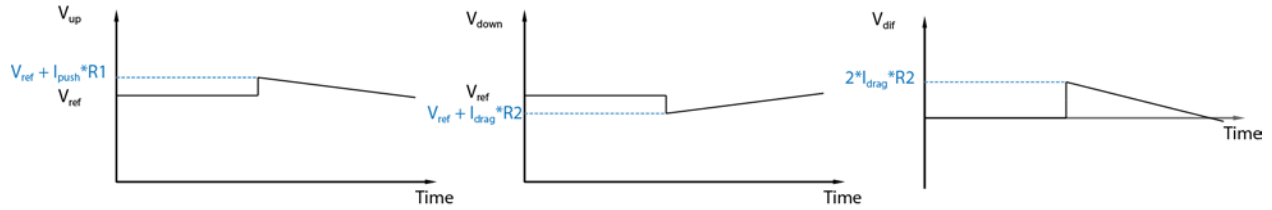

Figure 47 Voltage Changes of Over-range

The voltage change of the differential voltage, $2 \cdot I \cdot R$, can compensate for the offset voltage of the comparator and guarantee the input signals can cross each other. To avoid that the switches A1, A2 and B1, B2 are on at the same time, non-overlapping clock signal are generated on chip.

The timing diagram of this voltage ramp generator is shown in Figure 49. When switches A2, B2, S3, S4 are on, the output voltages V_{up} and V_{down} are connected to a low-impedance node with the voltage of V_{ref}. Next, A1, B2 switch on. The current sources start to charge and discharge the two capacitors respectively. In consequence, the output voltages V_{up}, and V_{down} start to ramp up and ramp down.

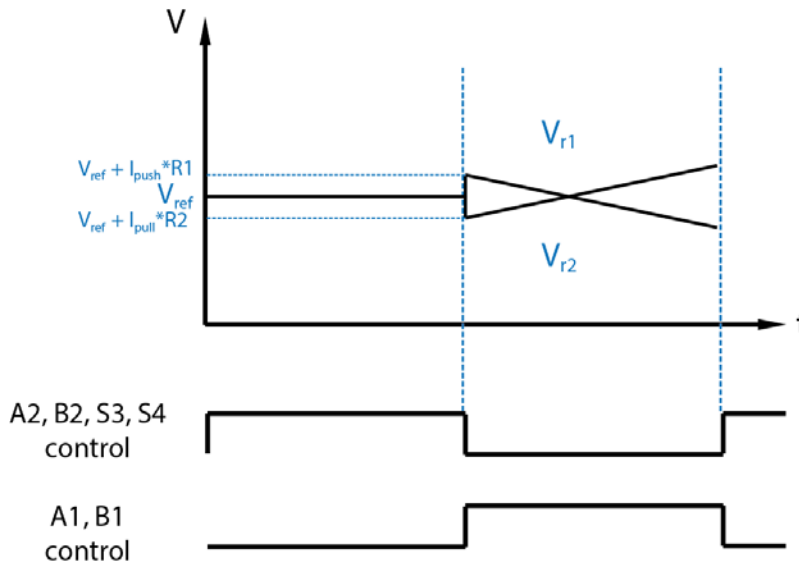**Figure 48 Timing Diagram of the Voltage Ramp**

4.3.3   Source Follower Design

In order to drive the 4 ADCs that share the ramp generator, a source-follower is required. A conventional "voltage follower" is shown in Figure 50(a). The output voltage V_{out} follows the input voltage V_{in}, except one V_{gs}. A drawback of this circuit that the current running through the transistor depends on the output

current. As a result, the V_{gs} is not constant, and the trans-conductance of the transistor is not constant either, which affects the linearity of the source-follower.
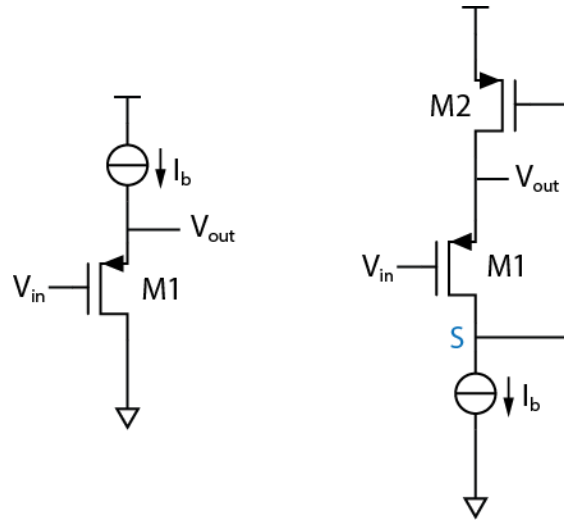

Figure 49 Source follower (a), (b)

The other source-follower shown in Figure 50(b) is called a Flipped voltage follower (FVF) [40], in which the current running through M1 is constant. Thus, V_{gs} of M1 is constant without considering the short-channel effect, and the trans-conductance is also constant, which improves the linearity of the source-follower. The feedback loop also decreases the output impedance which improves the drivability and saves the power consumption.

In this flipped voltage follower design, there is a severe problem, that the voltage at the sensing node (i.e. node S in Figure 50) increases faster compared with the rising input voltage [41]. The unequal voltage change may push the transistor M1 to the edge of saturation faster, which means the input swing of this source-follower is limited.

In our application, the input voltage of the source-follower is two opposite-direction ramp-voltages with the voltage range of 130mV each. In order to reduce the input voltage range required for one single source follower, the PMOS and NMOS FVF are both utilized. The PMOS FVF shown in Figure 51 (a) is applied for the ramping-down input signal, and the NMOS FVF shown in Figure 51 (b) is utilized for the ramping-up signal.
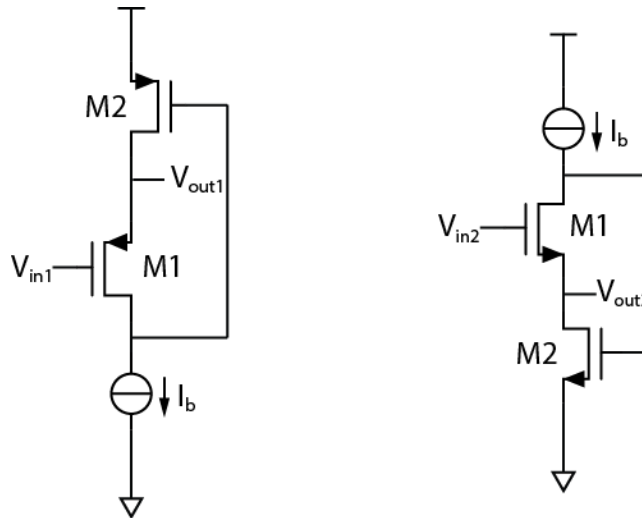
Figure 50Applied FVF (a) PMOS FVF (b) NMOS FVF

The source follower output is shown in Figure 52. During the sampling phase and SAR conversion phase, V_{out1} and V_{out2} are connected to the bottom plates of the C-DAC as the low impedance nodes, so the big voltage gap has no impact on the circuit. Then, in the single-slope conversion phase, each of these outputs starts to ramp up and down, respectively.
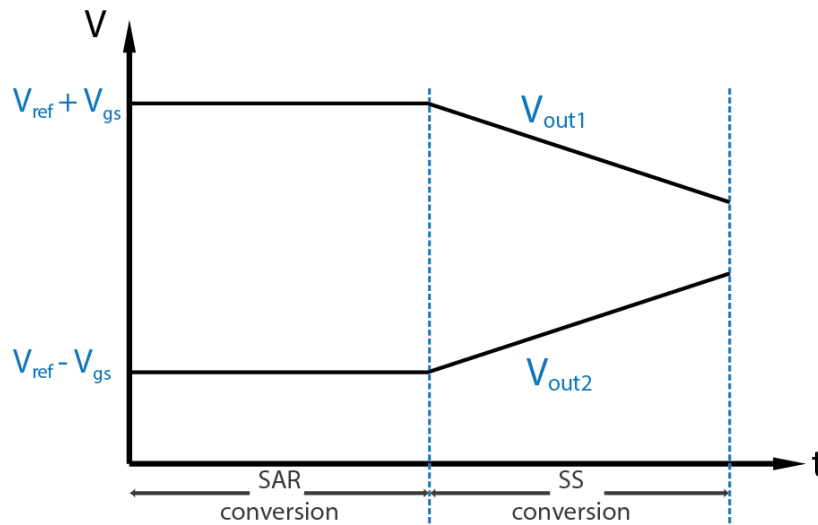
Figure 51 Source Follower Output

4.4   Timing Control

As shown in the timing diagram Figure 30, there are three main control signals: "reset", "sampling", and "trigger". The pulse widths of these three signals are 1.5ns, 2.5ns, and 4ns, respectively. As shown in Figure 53, the three control signals are all rising edge triggered, and the falling edge of each signal is utilized to generate the increasing edge of the next signal.
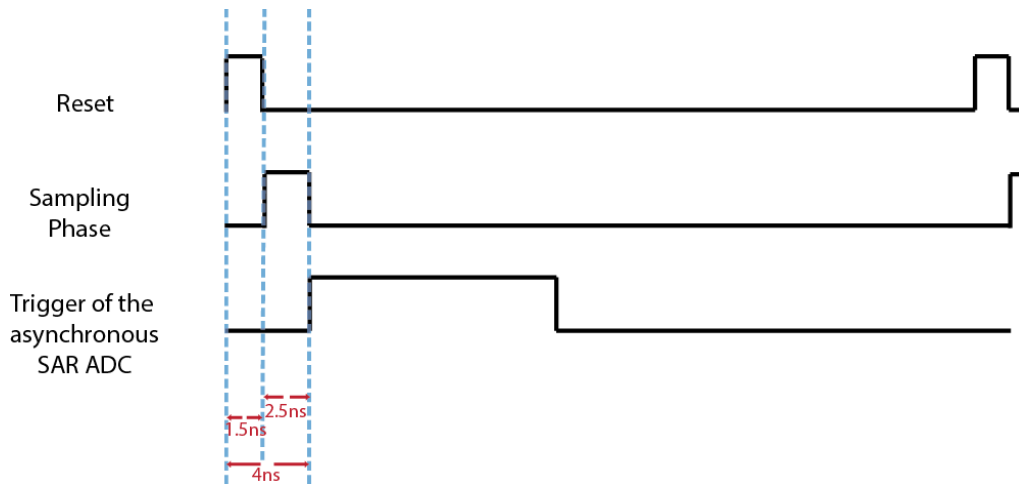
Figure 52 Timing Diagram of the Three Control Signals

In order to achieve these 1.5ns, 2.5ns, and 4ns pulse widths, the most straight-forward way is to delay an input pulse by a chain of delay-elements (a collection of invertors). However, the minimum delay in 0.18 TSMC CMOS technology is 100ps, which means tens of delay-elements are required. Although no static power consumption is required for digital buffers, the switching energy is also non-negligible. In order to solve this problem, a tunable delay based on a logic controlled current-starved delay element is used [42]. The proposed delay cell is shown in Figure 54. The power consumption of this delay cell is smaller than the power consumption of 10 invertor based delay line with 1.2V as the supply voltage.
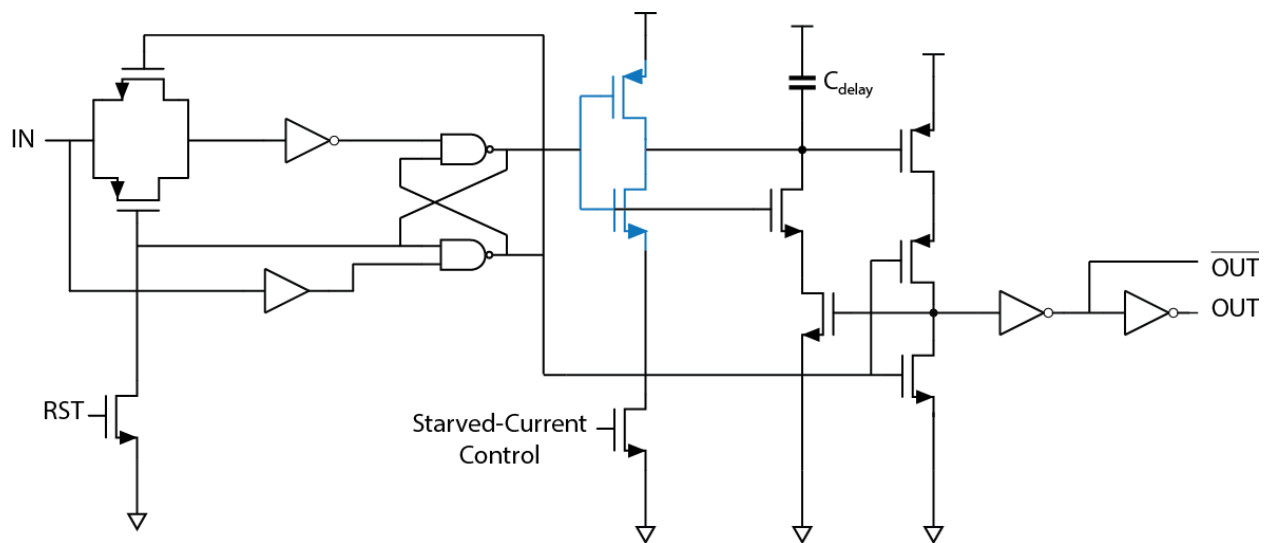
Figure 53 Proposed Delay Cell [43]

The delay time is adjusted by tuning the current running through the core invertor, which are the two transistors in blue. In our application, by controlling the starved-current, and the delay capacitor, the three different delay time are obtained.

5. System Level Simulation Results

The performance of the ADC is shown in this chapter, with the simulation results of the transistor level circuit. This chapter is organized as follows, section 5.1 introduces the calibration methods used in the ADC design, including the gain error calibration in the SAR conversion, and the reference voltage and offset calibration applied in the single-slope conversion. Section 5.2 describes the linearity of the ADC with integral non-linearity (INL). Section 5.3 describes the SNDR of the ADC with fast fourier transform (FFT) result and the ENOB is also calculated. This chapter ends up with section 5.4 illustrating the power consumption of the entire ADC.

5.1   Calibration of the Output Codes

Since the proposed ADC has a two-stage structure, calibration is required to combine the results of these two stages together. In the simulation, this calibration is obtained by an ideal DAC implemented with Verilog-A. With this ideal DAC, the digital codes can be converted back to analog signals. Comparing the output of the DAC with the sampled voltage of the ADC, we can make sure whether the calibration is successful. The applied calibration includes two parts, the first one is for the reference voltage of the SAR conversion, the second one is for the full-range of the ramp-signal in the single-slope conversion.

As already mentioned in section 3.4.2, if the LSB output of the SAR conversion is 0, which means the differential residue voltage is negative, the negative input node of the C-DAC will flip back one LSB voltage of the SAR conversion to make the differential voltage positive. In order to obtain this function, one more unit capacitor is applied in the C-DAC. Moreover, the input transistors of the comparator will also introduce parasitic capacitance. As a result, there is a gain error in each SAR conversion step, compared with the ideal case. Taking the voltage change in the SAR MSB conversion as an example, V_{step} is given by:

$$V_{step} = \frac{V_{ref} \cdot 8C_0}{C_{total} + C_0 + C_p} \tag{24}$$

where C_{total} equals $16C_0$, and C_0 represents the unit capacitor of the C-DAC, and C_p represents the parasitic capacitance of the comparator. Ideally, the voltage change of each step is $1/2V_{ref}$, $1/4V_{ref}$, to $1/16V_{ref}$. Now the voltage changes become $8/17V_{ref}$, $4/17V_{ref}$, to $1/17V_{ref}$, where there is ratio of $17/16$ in each step voltage change. This ratio is the gain error that should be calibrated. To compensate for this gain error, the reference voltage is changed. In the simulation, the reference voltage can be calculated by,

$$\frac{V_{step,real}}{V_{step,ideal}} = \frac{V_{ref,ideal}}{V_{ref,real}} \tag{25}$$

where $V_{step,real}$, $V_{step,ideal}$ represent the corresponding voltage changes in real and ideal situation, and $V_{ref,real}$, $V_{ref,ideal}$ are the reference voltages in real and ideal situation. Taking the simulation results as an example, with the ideal reference voltage 200mV, the MSB step voltage change $V_{step,real}$ is 91.53mV, which should be 100mV in ideal case. As a result, the calibrated reference voltage should be 218.5mV.

The second part of the calibration is about the reference voltage of the single-slope conversion. Ideally, the full-range of the reference voltage of the single-slope conversion should equal the LSB voltage of SAR conversion. In our application, due to the over-range voltage, and the delay of the continuous-time comparator, the actual full-range voltage is larger than the LSB of the SAR conversion.
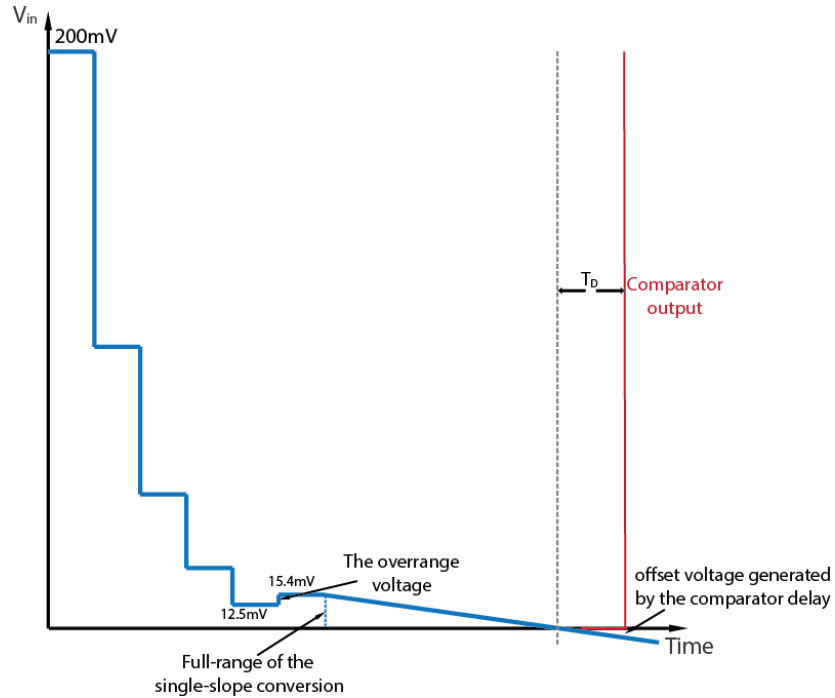

Figure 54 Calibration of the single-slope part

The full-range voltage of the single-slope conversion equals the residue voltage on the C-DAC of the maximum input voltage plus the over-range voltage, which is 15.4mV. The over-range voltage can be found by the voltage change at the differential input nodes, when the over-range is finished. The offset voltage generated by the continuous-time comparator equals the differential voltage at the input nodes when the comparator output signal comes. The Total offset voltage is 4.6mV.

5.2   Linearity

The INL is simulated with a voltage ramp signal, which covers the full-scale of the input range from -200mV, to 200mV. This ramp voltage source is applied as the input voltage of the ADC. In order to make sure the input step is less than the LSB voltage of the ADC, more than 700 conversion cycles have been simulated. As shown in Figure 55, the red line in the first subplot is the output voltage of the ideal DAC, the yellow line in the second subplot is the input ramp-signal. Subtracting the input voltage from the output voltage of the ideal DAC, and then dividing the result by the LSB voltage of the ADC, the equivalent INL can be defined, which is shown in the third subplot.
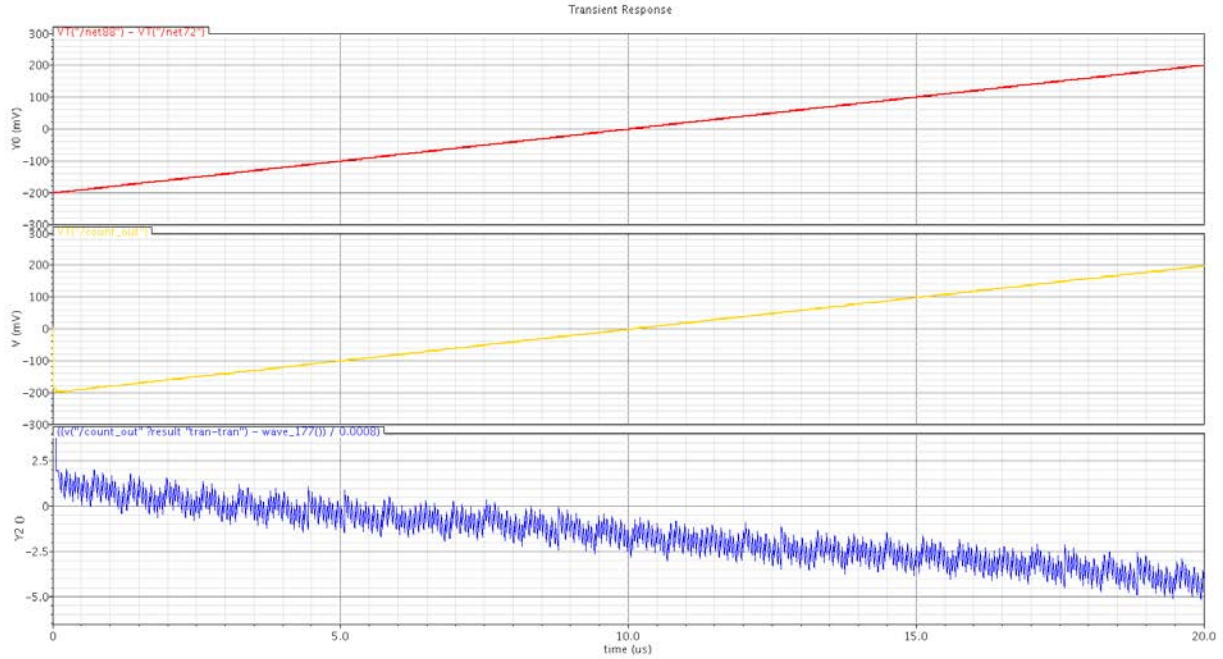
Figure 55 INL of the ADC

There is a fixed gain error in the INL results. After the gain error calibration, the INL result is shown in Figure 57, from -1.275LSB to 1.344LSB.
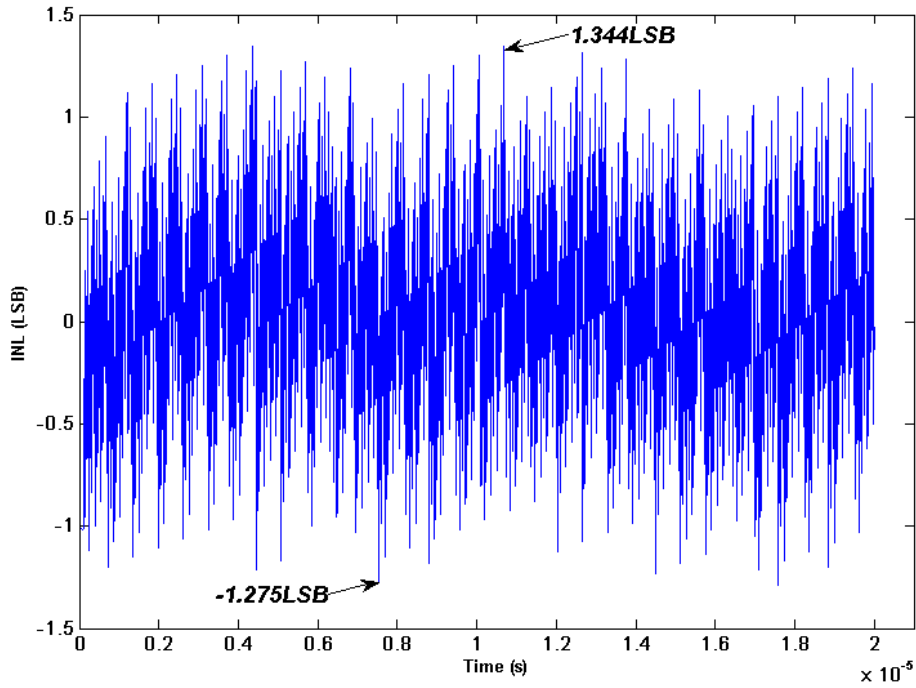
Figure 56 INL after calibration

5.3 SNDR

This ADC output spectrum shown in Figure 56 is simulated with 5MHz, sine signal, with the amplitude of 200mV, which is the maximum amplitude of the input signal. After calculating the FFT, the SNDR is calculated by the fundamental tone at 5MHz with the attenuation of -13.41dB, compared with second highest tone at 8.33MHz, with the attenuation of -69.14dB, which is 55.71dB. The effective number of bits (ENOB) is calculated by,

$$ENOB = \frac{SNDR - 1.76}{6.02} \qquad (26)$$

which is 8.96bits.
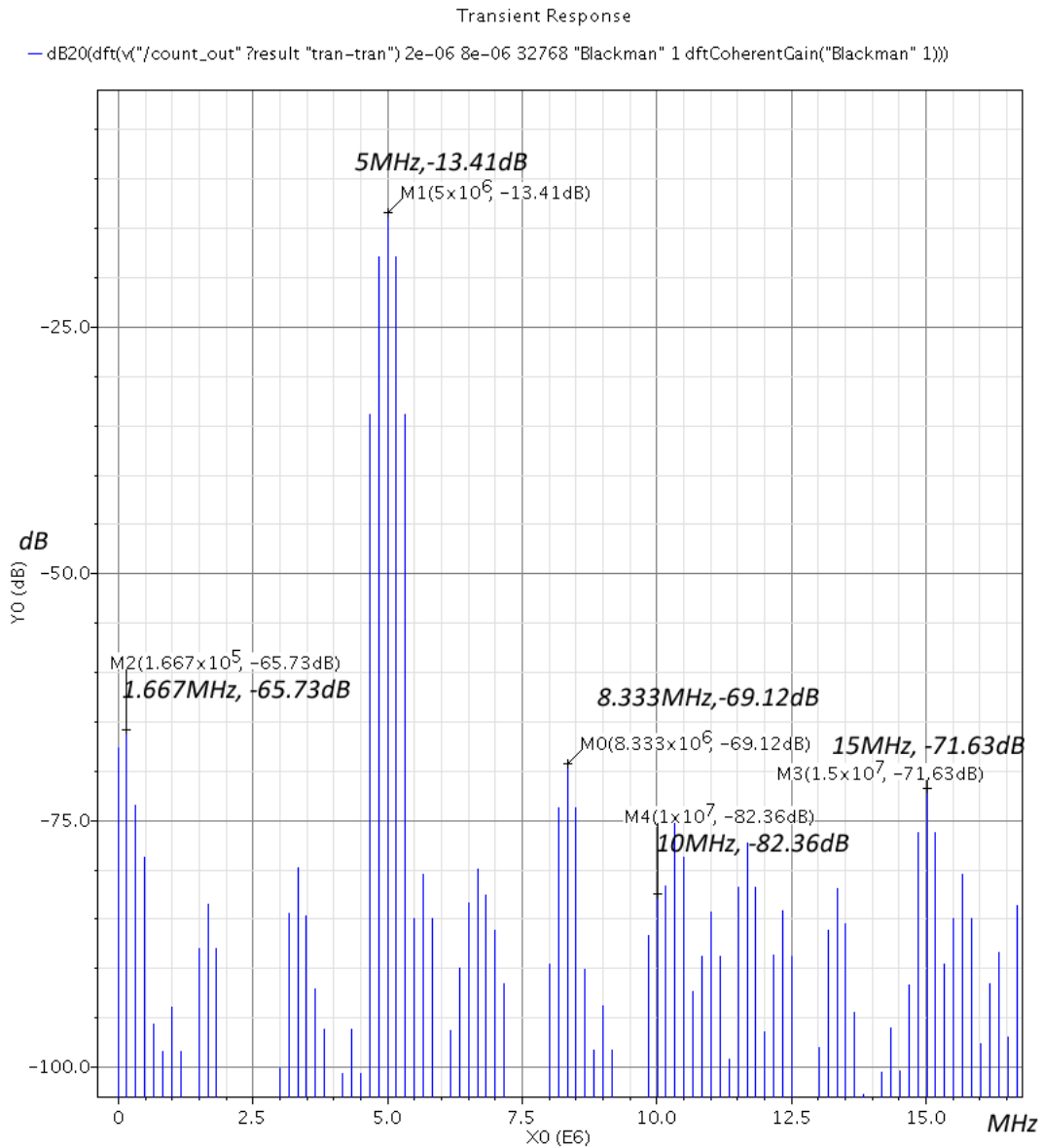
Figure 57 Simulated ADC output spectrum

5.4　Power consumption

The power consumption of this ADC is mainly contributed by the comparator, and the digital SAR logic. The total current consumed by the comparator is divided into three parts: preamplifier, second and third stage of the continuous-time comparator, dynamic latch of the dynamic comparator. The current consumed by the preamplifier is 180µA, and for the second and third stage of the continuous-time comparator, the current is 120µA. With the supply voltage of 1.8V, they contribute 540µW power consumption. The average current of the dynamic latch of the dynamic comparator is 121µA. The average current of the digital logic is 201µA. With the digital supply of 1.2V, the digital power consumption is 240µW. The power consumed by the C-DAC is 32.4µW. As a result, the total power consumption of the ADC is around 800µW, which is less than the design target mentioned in Introduction. The figure of merit (FOM) can be calculated by,

$$FOM = \frac{Power}{2^{ENOB} \cdot f_S}$$

(27)

where f_S is the sampling frequency, which is 33.33MHz.

Specification	Design Target	Simulation Results
Technology	TSMC 0.18um CMOS	TSMC 0.18um CMOS
Supply voltage	1.8V	1.8V (analog), 1.2V(digital)
ENOB	8~9 bit	8.96bit
Resolution	> 8bit	9bit
Conversion time	30ns	30ns
Power consumption	<1mW	800uW
FoM	<60fJ/conversion-step	48.7fJ/conversion-step

6. Conclusion

6.1   Thesis contribution

In the presented work, a 9-bit 33MHz hybrid SAR single-slope ADC has been successfully designed. The proposed ADC architecture has been simulated with transistor level circuits, and the simulation results prove that the conversion speed and resolution targets are met.

The dynamic and continuous-time comparator with shared preamplifier works properly. For designing the comparator this most important building block in the circuit, several issues have been realized and already improved. In the design of the comparator, the speed of the preamplifier is very important. Since an asynchronous SAR ADC has been implemented, the clock period of each conversion cycle is determined by the SAR logic delay and the dynamic comparator delay. If the differential input voltage is quite small, the output nodes of the preamplifier may not change completely when the next clock signal arrives, which can generate a big error in the results. This problem has been solved by increasing the current of the preamplifier. For the continuous-time comparator, the input voltage is the residue voltage of the SAR conversion on the C-DAC, which can be any small value. If the input voltage of the continuous-time comparator is quite small, in the single-slope conversion, this voltage can only last for a very short time and then cross zero. As a result, it is really hard for the continuous-time comparator to sense the voltage and give the output signal. This very small-value and short-time input signal can lead to a mistake in the comparator decision, which results in error in the output codes of the ADC. This is a GBW problem for the comparator, which has been solved by increasing the current as well.

The estimated dimension of the chip is around 100µm*150µm, and the area of the chip should be around 0.015mm^2 which is larger than our design target.

6.2   Future work

In the future work, layout and measurement are the main two parts.

In the layout of the C-DAC, the unit capacitor is always connected in the common-centroid way, which can minimize the stress and temperature gradients across the capacitors. The resistance and the routing parasitic capacitance will also be proportional to the capacitors value. For the layout of the comparator, in order to minimize the mismatch of the input transistors, the input transistors are always connected as "DABBABAABD", where "D" stands for dummy, and "A", "B" stands for the multiple of the two input transistors.

For the measurement, the reference voltage of the SAR conversion is provided by an external voltage source. The current of an ramp-signal generator is also provided by the external current source. In order to change the delay-time of the delay-line in the TDC, the supply voltage of the delay-elements is also provided by external voltage source. As a result, all these variants make the measurement a little bit complicated. In the future design, it is better to have an auto-tuning on the delay-time of the delay-line,

for example, a delay lock loop (DLL) can be implemented. Although some other problems can be generated by the DLL design, it is better to control one of the variants to make the measurement easier.

For the further improvement of the performance of the ADC, the power consumption can be reduced by shutting down the second and third stages of the continuous-time comparator, during the SAR phase. In our design, the second stage requires quite a long time to find the biasing points when it turns on at the beginning of the single-slope phase, which is the main reason that this ideal is abandoned.

In our design, the estimated chip area is larger than our expected value, which can be reduced by applying lower resolution in the SAR conversion. Due to the trade-off between area and power consumption mentioned in section 3.3, lower resolution in SAR conversion may slightly increase the power consumption.

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