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Crystallographic Silicon-Etching for Ultra-High Aspect-Ratio FinFET

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The fabrication process for the FinFET with ultra-high fin-height to fin-width aspect-ratio is presented. The processing is based on the crystallographic etching of (110) bulk silicon-wafers by TMAH to expose the vertical (111) planes. The nitride-spacers are used as the hard-mask for the fin-etching and the fins are isolated by the planarization and etch-back of the thick isolation oxide. The demonstration devices exhibit nearly ideal *S* of 62-64 mV/dec and *DIBL* of 10 mV/V or lower, for the gate-length of 410 nm and the height of the active part of the fin of 400 nm. The output current is limited by the large series resistances for both pFETs and nFETs, and additionally by the gate-depletion in nFETs, but large currents per fin, above 30 μA for pFET are achieved due to tall fin-structure.

Introduction

The challenge of moving towards the ultimate CMOS scaling-limit depends on the ability to contain short-channel effects (SCE). Fully-depleted devices, particularly with double gate, have significantly stronger coupling between the gate and channel potential, compared to bulk CMOS devices, which gives them superior performance for ultra-short gates. The double- or triple-gate FinFET is considered the best candidate to succeed planar bulk devices for the 22 nm node and beyond, due to the potential for integration in current CMOS technology. Good suppression of the SCEs in FinFETs results in a steep subthreshold slope and flatter output curves in saturation, which reduce drain leakage and increase output resistance, respectively. This makes them particularly attractive for low-power and high-gain applications. Various FinFET-based circuits have been demonstrated and characterized, such as digital logic, SRAM, DRAM and Flash memory (1,2,3,4). Moreover, FinFETs are also considered for analog applications and have shown potential in the frequency range below 10 GHz, with further improvement possible by the reduction of parasitics (4).

The vertical position of the active surface of the FinFET allows wider channels than the equivalent bulk CMOS of the same silicon area. The area efficiency is maximized by the increase in fin height, providing that the width of the etched fins can be kept uniform over the complete fin-height, since channel potential and consequently device performance, are strongly dependent on the fin width. The etched fin needs to be narrow for good control of the channel potential by the gate, and at the same time high quality of the etched surfaces is needed to reduce surface scattering. Furthermore, the value of parasitic gate resistance and capacitances depends on the geometry of the structure, namely, number of fins, fin-height and fin spacing, and when the total device width is divided over several fins, the FinFET with the channel width distributed over the smaller

number of taller fins will have lower parasitics and better frequency-performance than the one with a larger number of shorter fins (5).

In this work, we present the fabrication of the 1 μm tall and approximately 20 nm wide fins by crystallographic silicon-etching on (110) bulk silicon wafers. After isolation of the fins, the demonstrated MOS devices are processed on the fin sidewalls. The properties of the tall-fin structure are discussed, followed by an overview of the results of the electrical measurements on the processed devices.

Device Processing

The SOI substrates are often used in FinFET processes since they offer simple device isolation. However, to allow the freedom of choice for the fin-height, bulk silicon wafers were used in this work, and additional processing steps are included for the isolation of the fins from the substrate. Furthermore, the use of bulk silicon wafers also reduces process cost. The targeted aspect-ratio of silicon etching, of 1 μm:20 nm is beyond typical RIE processes, but the crystallographic etching in tetra-methyl-ammonium-hydroxide (TMAH) offers such anisotropy between different crystal planes and has already been investigated for the FinFET processing (6,7,8). Silicon etching in TMAH is very slow for (111) crystal planes compared to other directions and this property is used to etch the silicon fins by exposing vertical (111) planes on silicon wafers with (110) surface orientation. The etching is also very selective to silicon dioxide and nitride, and they can be used as hard-masks for the fin pattern.

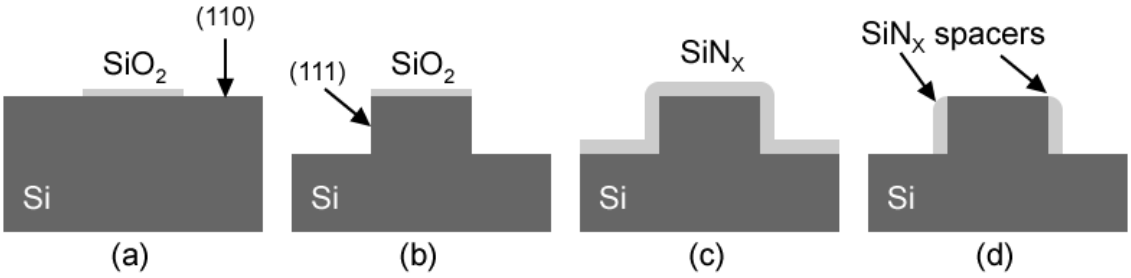

Figure 1. Formation of nitride-spacer hard-mask. Oxide is used as the hard-mask on (110) bulk silicon wafer (a). Silicon hill with two, nearly vertical sidewalls is formed by 150 nm deep silicon etching in TMAH (b). Oxide is removed and 50 nm of silicon nitride is deposited by LPCVD (c). Nitride is etched by RIE to form nitride spacers (d).

The FinFET process flow starts with ion implantations and annealing, which form the well regions with roughly uniform doping of $2 \cdot 10^{17}$ cm^{-3} and $3 \cdot 10^{16}$ cm^{-3} for p-well and n-well, respectively. The fin-etching by TMAH is done using a nitride-spacer hard-mask, as shown in Figure 1. A thin oxide-layer defined by optical lithography, is used to mask the etching of 150 nm tall hills on silicon surface by TMAH. Two sidewalls are aligned to the (111) planes and are almost perfectly vertical and these sides are used for the spacer formation. The oxide mask is removed and 50 nm thick layer of silicon nitride is deposited by LPCVD and etched by RIE, forming the spacers around the silicon-hill region. In addition to the spacers, the deposited oxide layer is locally preserved to serve as a hard-mask to pattern large pad areas for the source and drain contacts. The fin-etching in 25 % TMAH solution heated to 85°C is done next, resulting in approximately 1.1 μm tall silicon fins, shown in Figure 2.

The electrical isolation of the fins from the substrate is achieved by the deposition of a thick oxide layer, planarization and etch-back, shown in Figure 3 (9). A thin oxide layer is thermally grown as an interfacial oxide and 1.9 μm thick LPCVD oxide is deposited, densified to reduce porosity of the layer, and planarized by CMP. The oxide etch-back in a buffered-HF (1:7) solution exposes the top part of the fin, which is used for the active part of the FinFET.

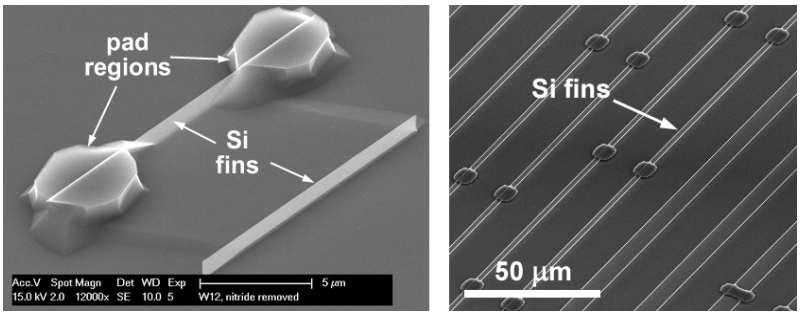

Figure 2. Silicon fins etched in 25 % TMAH at 85°C. Silicon-nitride spacers fabricated from the 50 nm thick nitride-layer, are used as the hard-mask for narrow fins and LPCVD silicon-dioxide as the hard-mask for large pads (left). Fins with a height of over 1 μm and width in the sub-30 nm range are mechanically stable even for long segments (right).

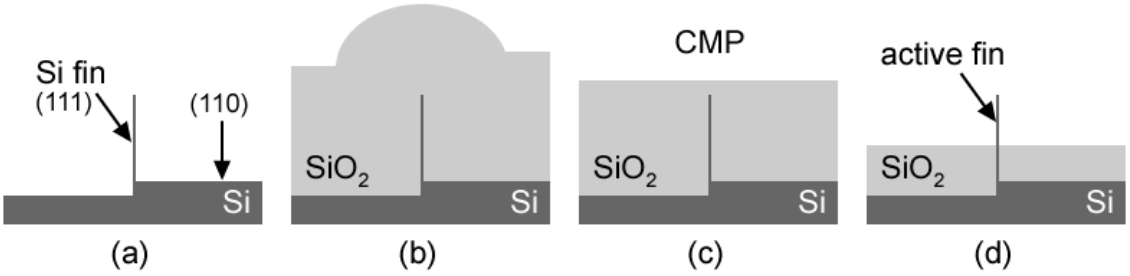

Figure 3. Electrical isolation of tall silicon fins on bulk wafers (a). Thick layer of LPCVD oxide is deposited (b). Oxide surface is planarized by CMP (c) and etched-back in a buffered-HF solution (d).

Thermal oxidation at 800°C in an oxygen environment is performed for the formation of gate oxide and 300 nm thick polysilicon is deposited by LPCVD as the gate material. Furnace diffusion is used to dope the gate polysilicon with phosphorous, followed by the gate patterning by TMAH, shown in Figure 4. The hard-mask for the gate patterning is formed from the 30 nm thick deposited layer of silicon nitride. The nitride hard-mask is removed and the source and drain regions are implanted at 60° tilt angles in addition to implantations for the pad regions. Next, the isolation oxide is deposited, contact holes are opened and implanted dopants activated by furnace annealing at 950°C for 20 min. The fabrication process ends with the formation of the metal lines.

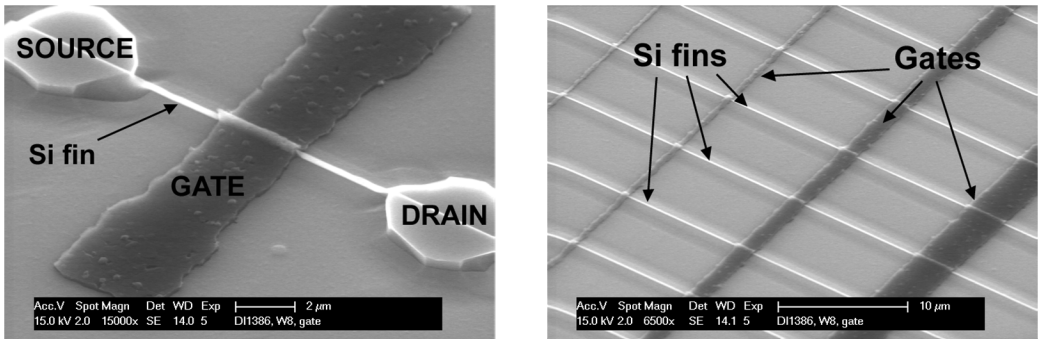

Figure 4. SEM image of the oxide-isolated silicon fins, with n^+-polysilicon gates etched by TMAH (left). The long gates over the long fins demonstrate good process controllability (right).

Structure Properties

The SEM analysis of the fin cross-sections reveals the ultra-high aspect-ratio of the final fins, with the fin height exceeding 1 μm, as shown in Figure 5. The width of the fin, including the gate oxide, is in the sub-30 nm range, but due to the resolution limit of the SEM, it is difficult to determine the width more accurately than this. The loss of width from the initial nitride-spacer thickness of 50 nm is caused by the finite TMAH anisotropy and by the part of the silicon fin being consumed during liner and gate oxidations. The crystallographic silicon-etching leaves nearly atomically smooth fin sidewalls, which should reduce surface scattering in the FinFET. The (111) crystal orientation of active surfaces is not preferred in standard CMOS, because of lower electron mobility compared to (100) surfaces (10). However, the hole transport benefits from (111) orientation and the overall circuit-performance can be improved since it is limited by the pFETs. Additionally, the quality of the ultra-thin gate oxides on the (111) surface was shown to be as good or better compared to oxides on the (100) surface in sub-5 nm range (11). The height of the active device is determined by the etch-back of the isolation oxide and, with additional lithography steps for device selection, the etch-back can be used to adjust the channel width to different values over the same wafer.

The fabricated FinFETs are demonstration devices and a simple processing is employed for the formation of the gate, as well as for the source and drain regions. Large MOS capacitors on (100) silicon wafers are processed in parallel with the FinFETs and the gate-oxide capacitance C_{OX} is extracted from C-V measurements. The estimated thickness of the gate-oxide from the gate capacitance value is 4.6 nm, which translates into approximately 7 nm for the (111) surface (12), assuming that the gate depletion is insignificant. The final gate-lengths are calculated from the measured loss of lateral gate-dimensions during polysilicon etching.

Narrow fin regions which connect the source and drain pads with the channel region cause large series resistances. Silicon etching by TMAH exposes vertical fins, but also other (111) crystal planes, and the non-vertical planes, sloped from the pads towards the channel, limit the minimum spacing between the gate-edge and the pad regions, as shown in Figure 6. A reduction of series resistance can be achieved by the selective growth of silicon-germanium or pure silicon on fin sidewalls with the gate separated by spacers, and in this case, large pads are no longer needed for device contacting. Due to the

underetching of silicon sidewalls not-aligned to vertical (111) planes in TMAH, devices require larger dimensions. However, this can be prevented by the high-dose boron implantation which drastically reduces the TMAH etch-rate (13).

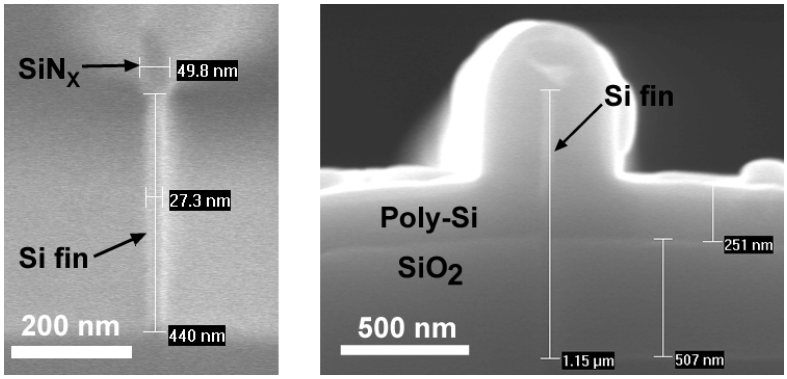

Figure 5. SEM image of the silicon fin after oxide CMP and etch-back (left). SEM image of the FinFET cross-section (right). Height of the active part of the fin in the figure is approximately 630 nm, resulting in an exceptionally high aspect-ratio.

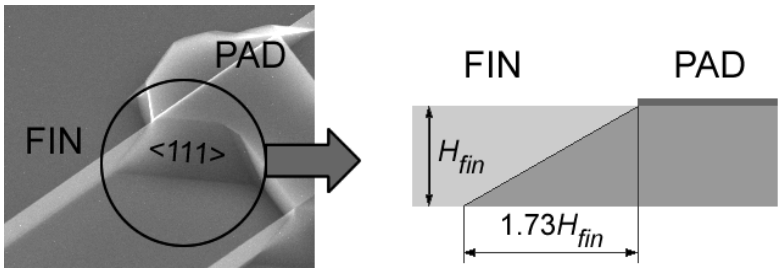

Figure 6. Crystallographic etching exposes additional (111) planes bounded by the pad hard-mask. The intersection of the vertical and angled (111) planes extends into the fin by $\sqrt{3}H_{fin}$, limiting the minimum distance between the gate and the source/drain pads.

Electrical Characterization

The measured transfer characteristics of the p-channel and n-channel FinFETs, fabricated on tall fin-structures, are shown in Figure 7. The threshold voltages (V_{th}) of the pFET and nFET devices are -1.05 V and -0.15 V, respectively, and are mainly influenced by the gate workfunction and body potential, whereas the depletion charge has little impact due to lightly doped and narrow channel. The V_{th} level is an issue common to fully-depleted devices, and can be solved by increasing the body doping and using p^+-polysilicon gate for pFETs, to reach the proper CMOS levels, with the penalty of lower carrier mobility in the channel (14). A better solution for the adjustment of V_{th} is the replacement of the thermal-oxide/polysilicon gate-stack with high-*k*/metal structure, with the possibility of the gate-workfunction engineering to reach the targeted V_{th}.

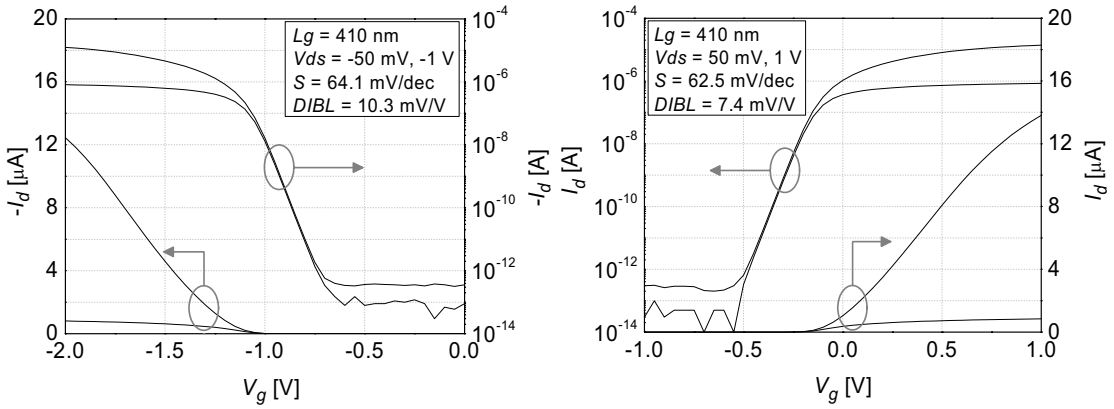

Figure 7. Transfer characteristics of p-channel (left) and n-channel (right) FinFETs with 410 nm long gates and a 400 nm tall active part of the fin. Excellent subthreshold performance is achieved with nearly ideal *S* and low *DIBL*.

As can be seen in Figure 7, the fabricated devices have excellent subthreshold performance, with a nearly ideal inverse subthreshold slope (*S*) of 62-64 mV/dec and drain-induced barrier-lowering (*DIBL*) in the 10 mV/V range. Because of the narrow fins, the gate has a strong control over the channel potential and the gate length can be scaled further, without significant degradation of the subthreshold characteristics from the SCEs. The output characteristics in Figure 8 show good current saturation, which can also be attributed to the suppression of the SCEs. Unexpectedly low drain-currents are measured for the n-channel devices, which exhibit lower output-currents than the pFETs. The part of the cause of this anomaly is traced to the gate-polysilicon depletion in nFETs, shown in Figure 9. Contrary to the nFET, the n^+-polysilicon gates of the pFET are accumulated near the gate-oxide interface when devices are biased in strong inversion, and the capacitance from the accumulation charge is large enough to not degrade the effective gate capacitance. Furthermore, the higher channel doping of nFETs is also responsible for the lower nFET current. The maximum measured transconductances for devices with L_g = 410 nm and $H_{active\ fin}$ = 400 nm are 30.7 μA/V and 15.6 μA/V, for the pFET and nFET, respectively.

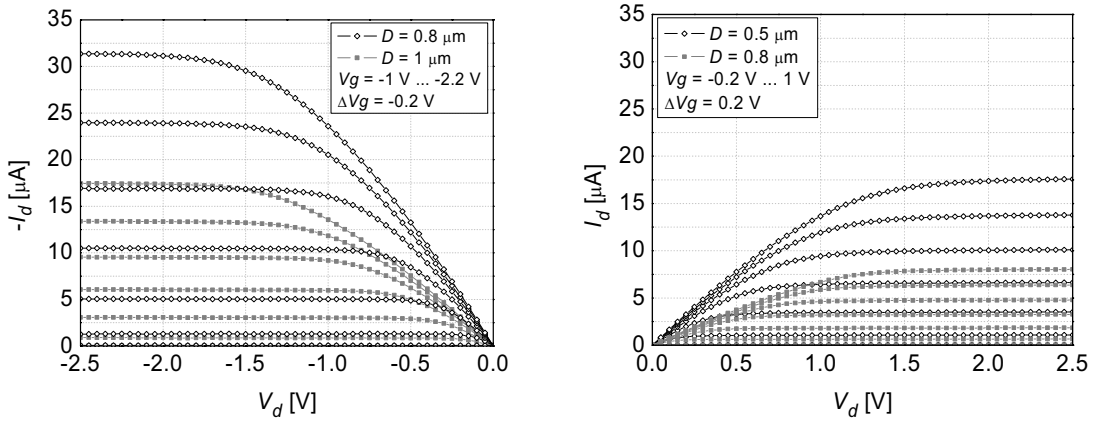

Figure 8. Output characteristics of p-channel (left) and n-channel (right) FinFETs. The drain current of the pFETs is significantly larger than that of the nFETs. The distance between the gate and the source/drain pad *D* significantly impacts the current through series resistances.

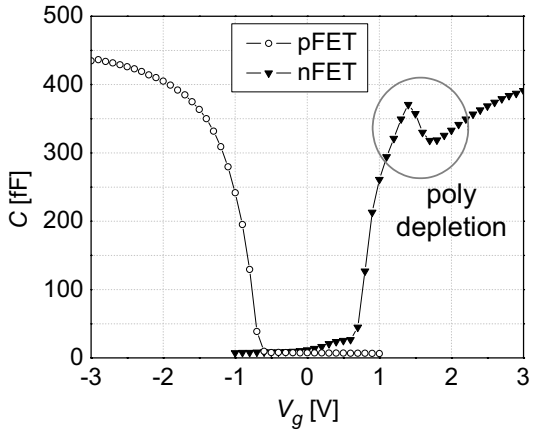

Figure 9. Capacitance-voltage measurements on large p-channel and n-channel transistors reveal depletion of the n^+-polysilicon in nFETs responsible for the lower output-current. Threshold voltages are different from the FinFETs because of the thicker body of the measured transistors.

The source and drain series resistance has significant impact on the performance of the measured devices, as evident from Figure 8. By reducing the distance between the gate and the source/drain, the output current increases, but the minimum distance is limited by the intersection of the vertical plane of the fin and the non-vertical (111) planes, as explained in Figure 6. Additionally, the source and drain pads are not self-aligned to the gate and the overlay accuracy of the lithography system needs to be accounted for in the layout, which increases the gate-source and gate-drain distance further. However, even with large series resistances, the wide transistor-channel allowed by the tall fin-structure, results in very-high currents per single fin, above 30 μA per fin for 410 nm long p-channel devices. Moreover, there is a large potential for further improvement by the scaling of the gate-length and the reduction of series resistances.

Conclusions

The fin-heights achieved by the crystallographic etching of silicon by TMAH are approximately 1.1 μm and are among the tallest reported, whereas the fin-width is kept in the sub-30 nm range, resulting in extremely high aspect-ratio. The operation of the p-channel and n-channel FinFETs fabricated on the tall fin-structure demonstrates the validity of the tall-fin concept. Due to narrow fins, i.e. thin silicon channel, devices show excellent subthreshold-performance, whereas the large fin-height gives high output currents for pFETs. The n-channel devices suffer from gate-depletion effects which reduce their output current, but this can be easily rectified by a more advanced gate-stack. Further improvements can be expected with the application of a more advanced lithography, as well as rapid thermal processing. The reduction of series resistances would particularly enhance the output current and transconductance, which are already comparable to the best results achieved per single fin, because of the large channel-width.

The presented FinFET concept is suitable for increasing the current density per used silicon area, since more transistor channels can be packed in a single fin. It also offers advantages in reduction of gate parasitics in devices that use several fins. Moreover, the increasing attention directed towards the use of (110) silicon wafers for bulk CMOS for

maximizing the hole mobility, places the described process as a very promising option for combined bulk CMOS and FinFET ICs.

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