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A High-PDE, Backside-Illuminated SPAD in 65/40-nm 3D IC CMOS Pixel With Cascoded Passive Quenching and Active Recharge

Scott Lindner, Sara Pellegrini, Yann Henrion, Bruce Rae, Martin Wolf, and Edoardo Charbon

***Abstract*— We present a complete pixel based on a single-photon avalanche diode (SPAD) fabricated in a backside-illuminated (BSI) 3D IC technology. The chip stack comprises an image sensing tier produced in a 65-nm image sensor technology and a data processing tier in 40-nm CMOS. Using a simple, CMOS-compatible technique, the pixel is capable of passive quenching and active recharge at voltages well above those imposed by a single transistor whilst ensuring that the reliability limits across the gate-source (V_{GS}), gate-drain (V_{GD}) and drain–source (V_{DS}) are not exceeded for any device. For a given technology, the circuit extends the maximum excess bias that SPADs can be operated at when using transistors as quenching elements, thus improving the SPAD sensitivity, timing performance, and photon detection probability uniformity. Implemented with 2.5-V thick oxide transistors and operated at 4.4-V excess bias, the design achieves a timing jitter of 95-ps full-width at half maximum, maximum photon detection efficiency (PDE) of 21.9% at 660 nm and 0.08% afterpulsing probability with a dead time of 8 ns. This is both the lowest afterpulsing probability at 8-ns dead time and the highest peak PDE for a BSI SPAD in a 3D IC technology to date.**

***Index Terms*— Single-photon avalanche diode, single-photon imaging, 3D image sensor.**

I. Introduction

A RECENT paradigm shift in single-photon avalanche diode (SPAD) based imagers is the development of imaging ICs in 3D technologies, with the first demonstration of a 3D IC SPAD achieved in [1]. In addition to the increase in fill-factor (FF) obtained by placing the CMOS circuitry beneath the SPAD, the technologies for the photodetector tier and CMOS processing can be chosen independently [2], thus allowing the combination of image sensor processes with high density CMOS. The disadvantage is that the maximum operating voltage of a transistor, and thus the excess bias when using a single transistor to quench and recharge, in highly scaled technologies is very limited. In technologies at 65 nm and below it is typical for thick oxide devices to be tolerant to just 2.75 V. For certain high performance SPADs [3], [4], the timing jitter and PDP can be improved greatly when biased above this voltage with only a small increase in dark count rate (DCR). Furthermore, operating at high excess bias improves the (PDP) uniformity across an array [3]. Thus, there is a pressing need for quenching and recharge circuits with a maximum excess bias voltage greater than 2.75 V.

In this letter we present a cascoded passive quenching and active recharge (PQAR) pixel which can operate at excess biases above the tolerance of a single low-voltage thick oxide transistor without the use of an area intensive poly-silicon resistor [4] or a high voltage process option [5]. The quenching and recharge circuit is coupled to a BSI SPAD in a 3D IC implementation.

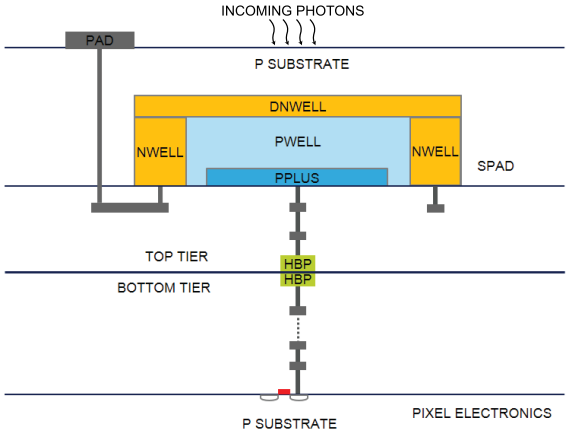

Fig. 1. p-well/deep n-well SPAD [6] in 65/40 nm 3D IC CMOS technology.

II. SPAD Structure and 3D IC Technology

The SPAD multiplication region is formed between the p-well and deep n-well implants, as implemented in [6],

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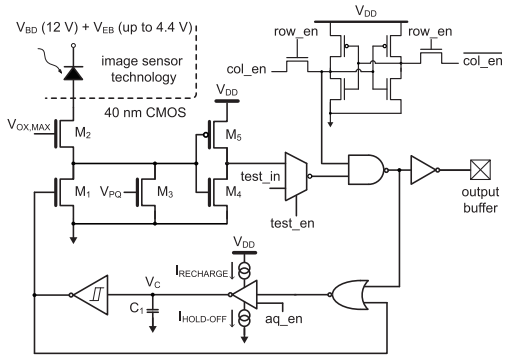


Fig. 2. Cascoded PQAR SPAD pixel.

see Fig. 1. The data processing tier and image sensing tiers are implemented in 40 nm CMOS and a standard 65 nm BSI image sensor process technology, respectively. Connections are made between the two tiers with hybrid bonding pads (HBP) using a wafer level hybrid bonding process, as detailed in [7]. Use of 40 nm CMOS for the data processing tier raises the prospect of increasingly complex electronics and smaller pixel pitches. Better SPAD performance could be expected from less scaled, e.g. 180 nm CMOS, or custom technologies [8], however, the 65 nm BSI imaging technology was chosen as the resulting 3D IC technology can support a wider range of high volume applications, some of which have different requirements, e.g. much smaller pixel pitches or different photodetectors. Custom technologies are not necessarily incompatible with 3D IC technologies, and in the future we may see custom SPADs combined with advanced CMOS.

III. Circuit Operation

The cascoded PQAR pixel circuit is shown in Fig. 2. The transistors M_1-M_5 are thick oxide devices with a nominal supply voltage of 2.5 V. As in [9] and [10] the voltage range of the interface is extended with transistor M_2, in series with M_1. The gate of M_2 is connected to a DC bias voltage, $V_{OX,MAX}$. This is set to the maximum voltage the gate oxide can handle reliably, 2.75 V, to ensure maximum range. M_3 provides a passive quenching option for testing purposes.

The active recharge is implemented through the combination of a NOR gate, an inverter charging a MOSCAP $C_1 = 5.7$ fF and a schmitt trigger. This circuit is similar to [11], except for the charging ($I_{RECHARGE}$) and discharging ($I_{HOLD-OFF}$) currents of the inverter that are supplied via two independently controllable wide-swing cascode current mirrors, whose input current is derived from an off-chip reference. $I_{HOLD-OFF}$ is tuneable over a range of 42 nA to 1 μA, for a dead time range of 8-100 ns.

Simulations showing key device and circuit voltages are shown in Fig. 3. When a photon is detected, the fast rising voltage at the drain of M_1, which is off, forces M_2 into the cut-off region. The anode of the SPAD charges quickly to the SPAD excess bias voltage, V_{EB}. This voltage, which can be up to 4.4 V, is distributed between the two devices ensuring that the gate-source (V_{GS}), gate-drain (V_{GD}) and drain-source (V_{DS}) voltages of both transistors are limited to less than 2.75 V. This ensures the gate oxide integrity of the

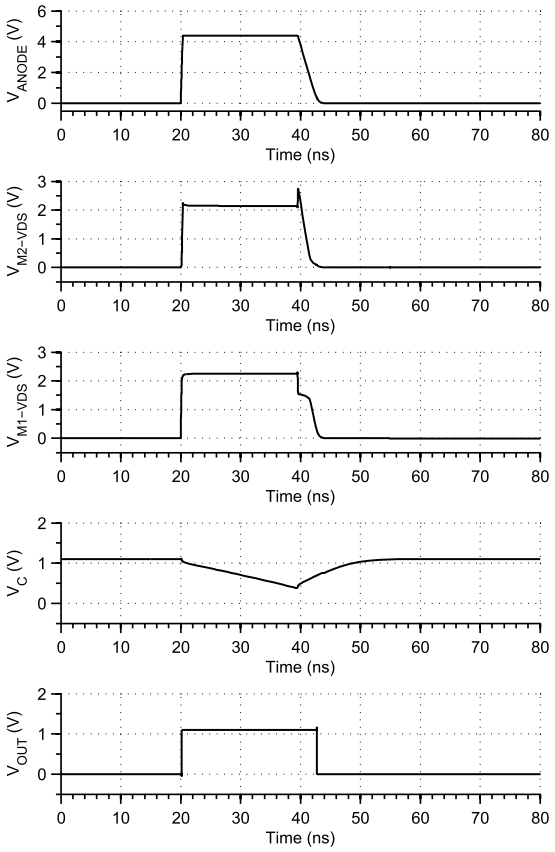


Fig. 3. Avalanche quenching and recharge simulation showing critical circuit voltages.

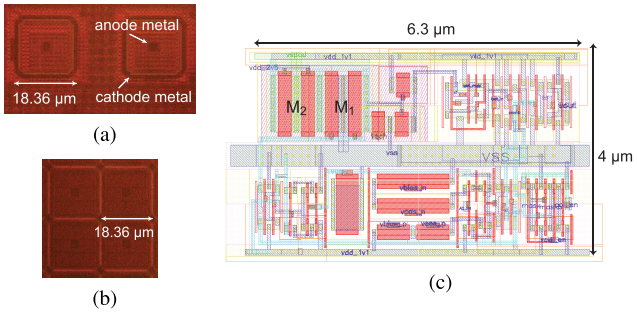
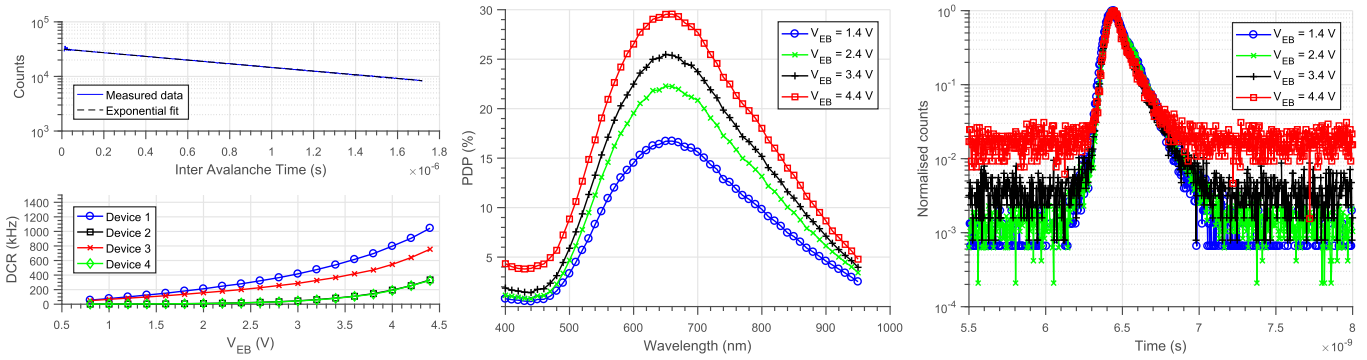


Fig. 4. (a) Pixel test structures micrograph showing two 18.36 μm pitch pixels separated by 11 μm gap, (b) Array format, fill-factor is 74.37% (c) Pixel circuit layout.

inverter formed from M_4 and M_5 which is used to detect the fast rising edge at the drain of M_1. The high impedance of M_1, M_2 and M_3 holds the anode voltage at V_{EB}, quenching the avalanche.

Upon the detection of a photon, C_1 is discharged with the current $I_{HOLD-OFF}$. Once the threshold of the schmitt trigger is crossed, $V_{GS,M1}$ rises to $V_{DD} = 1.1$ V. $V_{DS,M1}$ begins to drop, increasing $V_{DS,M2}$ until $V_{GS,M2}$ exceeds its threshold voltage, turning the device on. This results in a peak in $V_{DS,M2}$ which defines the maximum achievable excess bias voltage if we are to assume a strict limit on V_{DS} of 2.75 V. The anode of the SPAD is then discharged to ground through M_1 and M_2 until $I_{RECHARGE}$ charges C_1 to the upper threshold of the schmitt trigger. At this point, $V_{GS,M1}$ falls to zero, the SPAD is fully recharged and ready to detect another photon.



(a) (b) (c)

Fig. 5. SPAD characterisation results, (a) Afterpulsing (top), V_{EB} = 4.4 V, dead time = 8 ns and DCR (bottom), (b) PDP versus wavelength (c) Timing jitter measurement performed at 700 nm.

IV. Results and Discussion

The circuit was fabricated in the backside illuminated 3D IC technology discussed in Section II. The photodetection and data processing tiers are produced in 65 nm image sensor and 40 nm CMOS processes, respectively. A micrograph of the BSI SPAD pixel and a neighboring test pixel separated by a gap of 11 μm is shown in Fig. 4a. The darkened rings around the SPAD and the square in the middle are the metal connections to the anode and cathode. The pixel circuit occupies an area of 4 μm $\times$ 6.3 μm and is coupled to a "Fermat" [12] shaped SPAD with 250.7 μm^2 active area. This can be laid out in array format, see Fig. 4b, with a 18.36 μm pixel pitch, achieving a fill-factor of 74.37%. The layout of the pixel circuitry is shown in Fig. 4c.

The **dark count rate** is measured on 4 separate devices at 25 °C using V_{EB} up to 4.4 V, shown in Fig. 5a. Although high, these results are expected to improve with process refinement. Furthermore, for certain applications, e.g. light detection and ranging, DCR is less of a concern due to the dominant contribution of background illumination, even when using narrow near-infrared filters.

The **afterpulsing** results, showing the inter-avalanche times, are pictured in Fig. 5a. The SPAD dead time is set to 8 ns with V_{EB} = 4.4 V. The afterpulsing probability is calculated by determining the deviation from the exponential fit, and shown to be 0.08%. This is the lowest reported afterpulsing with 8 ns dead time for a BSI SPAD to date, thus demonstrating the suitability of the pixel and technology to photon counting rates as high as 125 Mcps.

Photon detection probability measurements over the wavelength range from 400-950 nm are shown in Fig. 5b. The results demonstrate an approximate 27% improvement in peak PDP by increasing V_{EB} from 2.75 V to 4.4 V. At 450 nm the estimated improvement is 316%. The peak PDP of 29.5% at 660 nm results in a peak PDE (PDP $\times$ FF) of 21.9%. This is the highest reported for a BSI SPAD in a 3D IC sensor.

Timing jitter measurements were performed by illuminating the sensor with a supercontinuum laser source and acousto-optic tuneable filter at a wavelength of 700 nm. The time interval between the SPAD pulses and the seed pulse of the laser was measured with a Lecroy Waverunner 204MXi-A oscilloscope. Care was taken to ensure that less than 1 photon was detected per 100 laser pulses to avoid pile-up. The timing jitter at a range of excess biases is pictured in Fig. 5c. The full-width at half maximum (FWHM) of the timing responses in ps are 122 (1.4 V), 114 (2.4 V), 104 (3.4 V) and 95 (4.4 V). This includes the jitter of the laser (FWHM = 20 ps) and the output buffer (FWHM = 55 ps). Subtracting these additional jitter sources results in FWHM timing responses in ps of 107 (1.4 V), 98 (2.4 V), 86 (3.4 V) and 75 (4.4 V).

In comparison to existing 3D IC BSI SPAD pixels [1], [13], which use only passive quenching and recharge and a thick oxide inverter to shift the voltage level, this design uses significantly more devices for the interface to the SPAD. The cascoded quenching scheme allows it to operate at higher V_{EB} using transistors that exhibit lower voltage tolerance, as explained in Section III. The active recharge capability enables higher count rates than can be achieved with passive recharge. Despite its higher complexity and extra features, e.g. electrical masking with a NAND and 6T-SRAM, this pixel design would still leave 59% of the pixel area free for circuitry such as counters when using the 7.83 μm pixel pitch from [13].

V. Conclusion

We presented the design and characterisation of a pixel based on a BSI SPAD with cascoded passive quenching and active recharge fabricated in a 65/40 nm 3D IC CMOS technology. To the best of our knowledge, this is the first all-transistor SPAD pixel capable of operating at excess biases above the voltage rating of a single transistor without exceeding the voltage reliability limits of any device.

The active recharge capability allows the pixel to operate at up to 125 Mcps at 4.4 V excess bias with 0.08% afterpulsing probability. Furthermore, the 4.4 V excess bias enables a peak PDE of 21.9% at 660 nm. This is, to the best of our knowledge, the lowest afterpulsing with 8 ns dead time and the highest peak PDE for a BSI SPAD in a 3D IC image sensor to date.

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