

Bachelor of Science Thesis

Development of Battery System and Output for the DeciZebro

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ABSTRACT

In this thesis it is described how a Battery System and an Output System are designed. This design is part of a Power System for the DeciZebro swarm robot. Two other parts are designed, the Input System [1] and the Control System. [2] A battery pack was designed, together with a Battery Management System. Next the Output System was designed. Finally the whole system, including input and control, were integrated on a Printed Circuit Board (PCB). No tests have yet been done, due to financing issues. All designs are based on literature research that has been described at the start of each chapter.

PREFACE

This Thesis was written as a part of the "Bachelor Afstudeer Project" for the Bachelor Electrical Engineering at the TUDelft. During this project we have been supported by our supervisor, Chris Verhoeven, and our daily supervisor, Daniël Booms. Furthermore we would like to thank Mattijs Otten for thinking with us and coming to solutions together. The rest of the Zebro team has also supported us in this project. A special thanks should be given to Erik Smit for helping us design the PCB, something we had never done before. We would also like to thanks Lisanne Kesselaar for her help during the soldering of the [PCB](#).

The software we used for the design of this system was KiCad, used together with GitHub for version control. KiCad comes with an integrated [PCB](#) design tool.

We hope you enjoy reading this thesis,

Wilfred Lopes & Frank van Veelen
July 25, 2018

GLOSSARY

- ADC** Analog to Digital Converter [vii](#), [12](#), [13](#)
- BMS** Battery Management System [vii](#), [xi](#), [5–7](#), [12](#), [27](#), [29–31](#), [33](#), [35](#), [36](#), [39](#), [41](#)
- CM** Common Mode [vii](#), [25](#), [26](#)
- DAC** Digital to Analog Converter [vii](#)
- DM** Differential Mode [vii](#), [25](#), [26](#), [31](#)
- EMC** Electro-Magnetic Compatibility [vii](#), [25](#)
- EMI** Electro-Magnetic Interference [vii](#), [xi](#), [1](#), [25–27](#), [30](#), [41](#)
- ESD** Electro-Static Discharge [vii](#), [4](#), [7](#), [13](#), [27](#), [39](#)
- ESR** Equivalent Series Resistance [vii](#), [20–22](#)
- EVs** Electric Vehicles [vii](#), [9](#)
- IC** Integrated Circuit [vii](#), [19](#), [21–23](#), [30](#), [39](#)
- LDO** Low-Dropout linear voltage regulator [vii](#), [xi](#), [7](#), [8](#), [15](#), [17–19](#), [23](#), [24](#), [27](#), [39](#)
- Lipo** Lithium Polymer [vii](#), [9](#)
- MCU** Micro-Controller Unit [vii](#), [7](#), [8](#), [15](#), [27](#), [28](#), [30](#), [36](#), [39](#), [41](#)
- MPTT** Maximum Power Point Tracking [vii](#), [8](#)
- PCB** Printed Circuit Board [iii](#), [v](#), [vii](#), [xi](#), [5](#), [7](#), [12](#), [13](#), [19](#), [26](#), [27](#), [29–31](#), [33](#), [35–37](#), [39](#), [41](#)
- PMS** Power Management System [vii](#), [xi](#), [7](#), [12](#), [29](#), [30](#), [39](#), [41](#)
- PV** Photo-Voltaic [vii](#), [5–8](#), [30](#)
- PWM** Pulse Width Modulation [vii](#), [17](#), [18](#), [22](#)
- SMD** Surface-Mounted Device [vii](#), [41](#)
- SoC** State of Charge [vii](#), [4](#), [7](#), [10–13](#), [36](#), [37](#)
- SoH** State of Health [vii](#), [11](#), [12](#)
- TVS** Transient-Voltage-Suppresion [vii](#), [7](#), [13](#), [39](#)

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1

INTRODUCTION

This Bachelor's Thesis is done for the Zebro team of the TUDelft. The Zebro team is developing the DeciZebro, for which the goal is to have a fully autonomous robot that can function as a platform on which swarm robotics can be researched. This means the DeciZebro needs a power supply that is self-sustaining. The robot should be able to function indefinitely without human interaction.

This is why a power supply was designed that implements wireless charging via the Qi standard, as well as power collection via a solar panel. While the solar panel provides very little power, it does increase the self-sustainability of the DeciZebro. In case a fault occurs and the DeciZebro is out of power away from the charging station, the DeciZebro can "sleep" until enough power is generated. For testing purposes a faster charging method via a laptop adapter is also implemented. The DeciZebro also needs a means of storing power. This is done via a battery pack inside the body of the DeciZebro. Lastly the power should be provided at the output at the correct voltages.

Everything should be designed for semi-mass production, since the goal is to have 150 DeciZebro's working together. This means a PCB should be designed.

This project was done by a group of six Bachelor's students. The project was split in three parts, of which this thesis is one part. This part focuses on the design of the energy storage as well as providing the correct output voltages to the rest of the DeciZebro.

In this thesis the requirements are first described. Secondly, an overview of the design of the whole system is given. Thirdly, the design of the battery system is explained in detail. Fourth the output and its' EMI filter are designed. After this the system integration is described. Next the PCB design stage and a cost analysis is described. Lastly, the system is tested according to a test plan.

2

PROGRAM OF REQUIREMENTS

To get a clear overview of the project a program of requirements is formed. This chapter describes the design requirements and restrictions. These requirements are those of the entire system, while the requirements for the system described in this thesis are in bold. The requirements of each subsystem are then worked out further. The requirements are derived from the assignment submitted by the Zebro team. The original document can be found in Appendix A.

2.1. OVERALL POWER SYSTEM REQUIREMENTS

- **The entire system shall fit within the specified dimensions of the robot, according to Appendix B**
- The system shall support 230VAC charging via laptop charging interface
- The system shall support inductive charging via the Qi charging standard, featuring receiving coil(s) that are embedded at the bottom of Zebro
- The system shall support charging batteries via a PV module at the top of Zebro
- The system shall support directly supplying Zebro modules via the PV cell as well as via the battery
- **The system shall utilise a damage protection system to avoid damage to any part of the DeciZebro**
- **The power supply shall be able to deliver 16V - 1A continuously, with a peak of 5A, fused without voltage regulation**
- **The power supply shall be able to deliver 5V - 1A and 3.3V - 1A, both fused with voltage regulation**
- **There shall be an over-current protection module**
- The communication with the main robot shall go according to the DeciBus protocol developed by the Zebro team, based on the I²C protocol
- Information about the power management system shall be divided in "Want to know" and "Need to know" signals
- Information about the power management system shall be stored in virtual registers that are to be accessed by the main DeciZebro computer
- Safety shall be guaranteed, even if one component fails
- **The total system price shall be below €100 for a series of 150**

2.2. BATTERY MANAGEMENT SYSTEM SPECIFICATIONS

1. Electrical

- (a) The battery shall be able to be charged with the maximum power of the laptop adapter
- (b) The battery shall be protected against overcharge
- (c) The battery shall be protected against over-discharge
- (d) The battery shall be protected against short-circuits
- (e) The battery management system shall be able to provide an accurate [State of Charge \(SoC\)](#) estimation (within 5% of actual [SoC](#))
- (f) The connectors shall be protected against [Electro-Static Discharge \(ESD\)](#)

2. Thermal

- (a) The battery shall be protected against high temperatures
- (b) The battery pack shall not overheat itself during a charge cycle
- (c) The battery pack shall not overheat itself during a discharge cycle

3. Mechanical

- (a) The battery shall be protected against mild shocks

2.3. OUTPUT SPECIFICATIONS

1. The system shall be able to deliver power to the four output busses

- (a) 2x16V unregulated with a peak of 5A
- (b) 5V regulated with a peak of 1A
- (c) 3.3V regulated with a peak of 1A

2. The system shall be able to convert this power from the main power bus which has a minimum voltage of 12V and a maximum of 16.8V

3. Each voltage bus shall have a current limiter/short-circuit protection

4. Each voltage bus shall have a fuse

5. The output converters shall be able to be enabled/disabled for control

6. Each output converter shall have a high-temperature shut-off option

3

SYSTEM DESIGN

This chapter discusses the overall design of the power system that is going to be used in the DeciZebro. The workload of this project is divided amongst six members, which form a total of three subgroups. Thus, the project is divided into three modules: peripherals, power electronics and control. The peripherals group handled all the different inputs together with the correct conversion for connection to the power bus. This includes a [Photo-Voltaic \(PV\)](#) cell, Qi charging and a laptop interface. The power electronics group handled the complete battery management system and the output power conversion together with the [PCB](#) design. The control group handled all monitoring and safety features in the system. This included adding temperature sensors, current sensors as well as a way of communicating with the main controller. The requirements for the whole system were discussed in Chapter 2.

The choice was made to have the [BMS](#) on a different [PCB](#). This was decided in order to have more space on the main [PCB](#) and make the complete power management system more modular. This also enables the possibility of using a different battery chemistry when needed.

3.1. OVERVIEW

The total system overview, including the connectivity between each sub-module will be discussed. A schematic overview of the top-level of the main [PCB](#) is given in figure 3.1. The peripherals group implemented the Qi

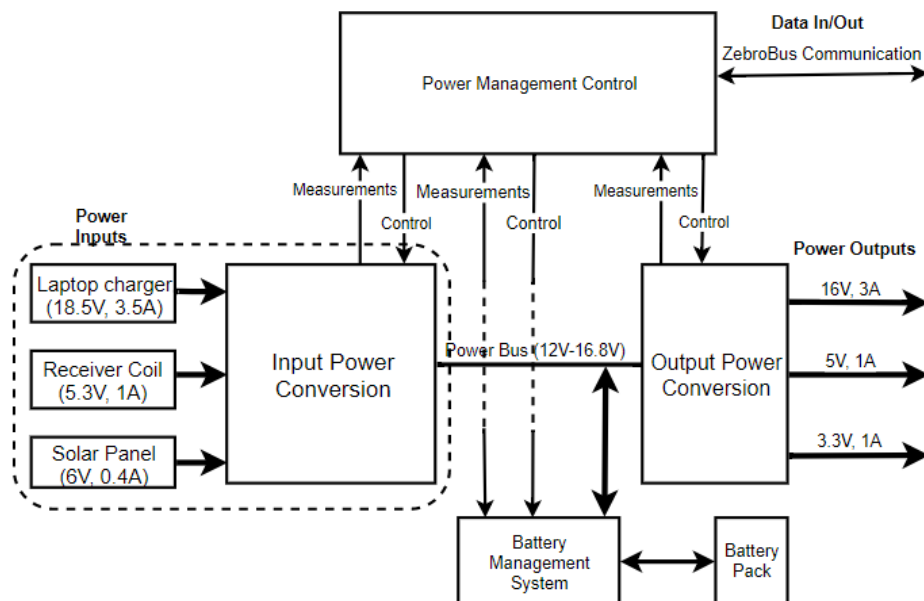


Figure 3.1: Top level overview of the main [PCB](#)

and input block, the control group the control block and the power electronics group the **BMS** and the output conversion. The top level of the **BMS** is given in the figure below.



Figure 3.2: Top level overview of the **BMS**

3.1.1. TOPOLOGY

The battery is chosen as the voltage reference for the power bus. The input sources will function as current sources providing power to the output. The reason being that the **PV** cell, the laptop interface and the Qi can be approximated as current sources. Also, it is not recommended to have different voltage sources in parallel with each other. It is easier to just 'inject' current into the power bus since parallel current sources add, while parallel voltage sources do not.

3.1.2. CONNECTORS

All connectors on the power management system are found below:

- Input
 - Molex-KK-6410 for Qi charging 2 pins (J1)
 - Phoenix Terminal block PT 3.5mm for laptop input (J3)
 - Molex-KK-6410 for **PV** cells (J13)
- Control
 - 2x3 Header pins as a debug interface (J4)
 - 1x3 Header pins for the **BMS** data input (J5)
 - SEK-18 series 6 contacts header as ZebroBus interface (J7)
- Output
 - Molex-KK-2045 4 pin connectors for the four outputs (J9-J12)
 - Molex-KK-2045 4 pin connector for the on/off button (J8)
 - JST-VH-B2P 2 pins connector as **BMS** power input (j6)
- BMS
 - JST-VH-B2P 2 pins connector as **BMS** power output (J3)
 - JST-VH-B2P 2 pins connector as battery input (J2)
 - JST-XH 5 pins connector as battery balance connector (J1)
 - 1x3 Header pins for the **BMS** data output (J4)

3.1.3. ESD PROTECTION

Connectors might get statically charged. When trying to connect connectors, this charge might get discharged onto the **PMS** resulting in a very high voltage spike. To prevent this, a **Transient-Voltage-Suppresion (TVS)** diode will be used. This diode should be connected parallel to each input, as well as at the **BMS** connectors. The diode has a very high impedance for low frequencies, thus it can be approximated as an open circuit. However, for very high frequencies, the diode conducts for very small amounts of time (in the order of nanoseconds). This allows the **ESD**-induced high current to have a low-impedance path, thus protecting the circuit.

3.2. SUBSYSTEMS

This section discusses the different subsystems and what their function is.

3.2.1. INPUT CONVERSION

As mentioned before, the **PMS** requires support for the following input sources:

- Laptop interface
- **PV** cell
- Qi wireless charging

The input subsystem handles all the conversion that needs to take place in order to safely use the power put in by these sources. The choice was made to separate the Qi and laptop interface, so only one of them can be used at the same time. This was mainly done to preserve space on the **PCB** and reduce the total cost of components by only using one converter for both inputs. It is also more practical, since in "autonomous mode" the DeciZebro doesn't have access to a laptop charger, while in "testing mode" it is more convenient to only use a laptop charger. Of course, the same does not hold for the **PV** cell. The **PV** cell is equipped in order to provide a continuous power flow when directly under sun. The purpose of the **PV** cell is to make the batteries last a bit longer, and to be able to charge when the DeciZebro has run out of charge. In "autonomous mode" the DeciZebro can use both the Qi and the **PV** cell to charge. In "testing mode" the DeciZebro can charge by laptop or again, with the **PV** cell. Thus the **PV** cell is always enabled.

The input subsystem also has fuses for each input. One for Qi and the laptop charger (since they follow the same path) and one for the solar. To protect the input against reverse polarity, P-MOS transistors are used to function as efficient diodes. Also, each input is monitored with a shunt current sensor, which can determine the current flow and voltage at that point. In case of a fault, each input can be disabled to prevent further damage. The detailed design of this subsystem is further discussed in their respective thesis [1].

3.2.2. POWER BUS

As mentioned before, the voltage of the power bus is simply the voltage of the batteries. This was done in order to not have an additional converter in the power line, thus improving efficiency without sacrificing extra space. The input sources are current sources that provide the power to the main power bus. In the case that the batteries need to be charged, the power bus provides the power to the **BMS**. The power bus also includes shunt current and power monitoring and a PMOS transistor as a diode to prevent power flowing from the output to the input or **BMS**. Since the **Micro-Controller Unit (MCU)** and sensors of the **PMS** always needs to have power, a low-dropout regulator is added directly to the power bus to convert the bus voltage to 3.3 volt. Since the power draw of the **MCU** and sensors are very low (< 1W) a **LDO** is used in order to preserve space on the **PCB** and save additional component cost.

3.2.3. BATTERY MANAGEMENT SYSTEM

The **BMS** manages the charging and discharging of the battery. It includes safety features which detect over-voltage, under-voltage, over-current, short-circuits and critical temperatures. When using multiple cells, the **BMS** also supports balance charging which always ensures that every cell has the same voltage. The **BMS** also includes a data interface which allows the **MCU** to request data about the battery status (e.g. **SoC**, current temperature, current, voltage, capacity of each cell etc). The **BMS** also has a fuse in the powerbus to protect against over-currents and short-circuits. The complete design of the **BMS** will be discussed in Chapter 4

3.2.4. OUTPUT CONVERSION

The output subsystem needs to support:

- 16V unregulated bus with 5A peak for the right motors
- 16V unregulated bus with 5A peak for the left motors
- 5V regulated bus with 1A peak
- 3.3V regulated bus with 1A peak

The output subsystem converts the bus voltage to the required bus voltages at the output. It does this by using multiple converters. The 16V unregulated busses use only a single buck-boost converter. The 5V and 3.3V busses use a different buck-converter to convert the voltage to a lower voltage, which then power the [LDOs](#) for a regulated voltage. To ensure that no over-currents will occur, a fuse is added to each output, together with a shunt current sensor. Like the input, the output also includes the functionality of disabling each individual output. This allows the [MCU](#) to properly handle a power fault when it occurs. Even when the [MCU](#) for some reason, does not catch the fault in time, the output is protected by fuses. The complete design of the output conversion will be discussed in Chapter 5

3.2.5. CONTROL

The control subsystem makes sure that each part of the power management system is protected against faults. This is done by adding the necessary sensors at the most important points in the power management system. Since the input uses a [PV](#) cell, the control subsystem implements an [Maximum Power Point Tracking \(MPTT\)](#) control in order to ensure maximum power from the [PV](#) cell. The control subsystem also acts as a data interface for the main controller in the DeciZebro. For visibility, LEDs are added. The list of LEDs that will be found on the power management system can be found below.

- Two LEDs for debugging
- Three LEDs to determine which input is connected
- Three LEDs to determine which output is connected
- Five LEDs to determine battery health/state of charge

The complete control subsystem design will be further discussed in their respective thesis [2].

4

BATTERY SYSTEM

Because the DeciZebro is a mobile system, some sort of power storage should be implemented. The energy storage system chosen is a battery pack. This battery pack consists of cells and a Battery Management System (BMS). First, the chemistry of these cells is chosen. Next, the BMS is designed.

4.1. THEORETICAL BACKGROUND

4.1.1. BATTERY CHEMISTRY'S

With growing interest in [Electric Vehicles \(EVs\)](#) and renewable energy, interest in electrical energy storage is also growing. The chemistry of a battery has a lot of influence on the performance of a battery. Because the DeciZebro should be semi-mass produced in the near future, the chemistry chosen should be widely available. The chemistry chosen should also be rechargeable (also called secondary cells). This is why only the most available rechargeable chemistry's were considered. These are¹:

- NiCd: A positive electrode consisting of NiOOH and a negative electrode of Cd. [3], table 1.1. Was widely used before NiMH took over. Now NiMH performs better in almost every aspect and is more environmentally friendly.
- NiMH: A positive electrode consisting of NiOOH and a negative electrode of H₂. [3], table 1.1.
- Li-ion: Lithium ions are "trapped" inside metal oxide or graphite, depending on the SoC. These ions are transported when charging/discharging. The transportation is done by a liquid electrolyte (See figure 4.1)
- LiPo: The working is very similar to that of Li-ion batteries, however the electrolyte is solid instead of liquid.

To determine the best suited battery chemistry for the system different parameters should be compared. This is done in table 4.1. All these parameters are for a full charge/discharge cycle of the battery, since it is desired to return to the charging station as little as possible.

Notes: Operating temperature in this context means the worst case operation, since all different types of operations should be possible while in the Zebro. [Lithium Polymer \(Lipo\)](#) batteries are not explicitly discussed in the table since they are very similar to Li-ion batteries.

Other than these parameters all battery chemistry's require special considerations when implementing them in a system like the DeciZebro. NiCd and NiMH cells have a valve built-in in a lot of cases. This valve is used to depressurise the cell after overcharging. The gases discarded by the cells have to be able to escape the case of the DeciZebro.

The main difference between Li-ion and [Lipo](#) cells is the packaging they come in. [Lipo](#) cells come in "pouches". These are soft and sensitive to mechanical pressure applied. Li-ion cells come in various shapes and sizes but always in a hard case, which makes them more resistant to mechanical pressure.

From table 4.1 and the other considerations it can be concluded that Li-ion batteries are superior in almost every regard.

¹<http://www.baj.or.jp/e/statistics/06.html>

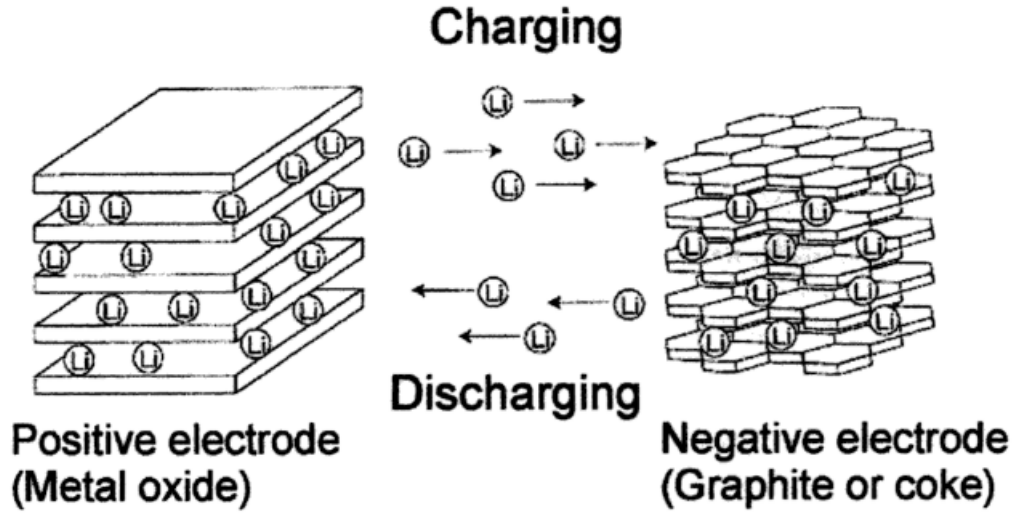


Figure 4.1: The working of a lithium ion battery [3]

Table 4.1: A comparison of the battery chemistry's

Parameter	NiCd	NiMH	Li-ion
Voltage [V]	1.2	1.2	3.7
Specific energy [Wh/kg]	55 [5]	90 [5]	100-170 [5]
Operating temperature [°C]	10-45 [6]	10-60 [7]	0-45[8]
Charge/discharge efficiency (low current) [%]	96 [9]	95 [9]	99 [9]
Charge efficiency (high current) [%]	70 [9]	80 [9]	90 [9]
Approx. price [Wh/€] (Mouser)	0.5	0.6	0.7
Self-discharge rate [%/month]	20-30 [6]	45[10]	2-3 [11]
Lifetime [cycles]	<1000 [6]	<1000[12]	800->2000 [13]

The Li-ion batteries have the highest cell voltage, which means less batteries have to be used in series to get to a higher voltage. This higher voltage means the current will become smaller for the same power usage. This results in less losses.

The specific energy is the highest, the efficiency is the highest, the price is the lowest and the self-discharge is the lowest. The lifetime is the highest as well. The maximum operating temperature of NiMH batteries is however greater than that of Li-ion batteries. Short research regarding the charging patterns required for the different battery chemistry's has also been done. The charging of Li-ion batteries can be done relatively easily.

Considering all the mentioned benefits of Li-ion batteries this will be the used chemistry.

The chosen batteries should be implemented safely. More about this can be read in section 4.2. It is also important to charge the batteries in such a way that the capacity of the battery can be used, while maintaining lifetime of the cells. The theory behind charging methods is first discussed in subsection 4.1.2.

4.1.2. CHARGING METHODS

The charging method has a large influence on the life time (amount of cycles) of a Li-ion battery. [14] Suggested in this paper is, charging should be done with a low current for a low SoC (<0.1), because the internal resistance of the cell is high for a low SoC. Also suggested is the current should be low for a high SoC, since otherwise the potential of the graphite could drop below 0V versus Li^+/Li . This results in metallic plating of the graphite, which results in unwanted reactions. This reduces the capacity of the cell.

The charging profiles discussed are: CC-CV, CP-CV and MCC-CV. Constant Current-Constant Voltage starts by providing a constant current until a cell voltage of 4.2V is reached. After this a constant voltage of 4.2V is provided.

Constant Power-Constant Voltage instead keeps the power stable in the first stage. This means a high current is provided first, which then reduces as the voltage of the cell increases. After a cell voltage of 4.2V is

reached a constant voltage is provided.

Multiple Constant Currents-Constant Voltage uses multiple stages of different constant currents. The profile starts by providing a relatively low current to the cell, until a certain threshold is reached after which the current is increased until 4.2V cell voltage is reached. After this the current is reduced to keep the voltage at a stable 4.2V.

For low average charging currents ($<0.5C$) it is suggested to use CC-CV charging since the effect of the high initial impedance is small enough, and it does not result in metallic plating. For larger charging currents it is suggested to use CP-CV, since the ending current should be small enough to not result in metallic plating of the graphite.

More complex charging profiles, like sinusoidal charging or pulsed charging, are also being researched. These however do not seem to be more promising than CC-CV charging[15] and research is not mature. All charging profiles can also apply a pre-charging current, to overcome the problem of the high impedance at the start of a charging cycle.

4.1.3. CELL BALANCING

Because no two cells are exactly equal, during charging of two series cells the voltage over cell 1 could be greater than 4.2V, while the voltage over cell 2 is not yet 4.2V. Cell balancing can be implemented to prevent this problem. Charge is removed from the offending cell (cell 1) to increase the effective capacity of the pack. The result is all cells are charged to 4.2V.

There are multiple methods to balance the cells. Passive cell balancing uses resistors to convert the excessive energy of the offending cell to thermal energy. [16] This is not energy efficient since all balancing power is lost.

Another option is active cell balancing. This uses capacitive or inductive energy storage to reduce the voltage difference between the cells, after which it is provided to a cell with a lower cell voltage.[16]

4.1.4. STATE OF CHARGE ESTIMATION

Multiple methods for estimating the remaining charge in a Li-ion pack are used. These are all shortly discussed. Some of these are online measurements, others are offline measurements. Online means no interruption of the battery operations is necessary for the measurement. [17] Offline measurements are not considered, since stopping the DeciZebro to estimate the SoC is not viable.

VOLTAGE READOUT

This is a very non-invasive way of measuring the SoC. The voltage of the cells is monitored, which is then related to the SoC-voltage curve which results in a SoC estimation. The problem with this method is the fact that a stable voltage over the whole SoC range is desired and the current draw has influence on the voltage of a cell. This means the SoC would be estimated higher while charging and lower while discharging. By also measuring the current entering the pack, this difference could be compensated to a certain extent. This method is also sensitive to noise in the measurements. [17]

COULOMB COUNTING

Also called the current integration method, this SoC estimation uses a current sensor which measures current entering and leaving the battery pack. This current read-out is then integrated to estimate the charge available in the pack. Pure coulomb counting suffers from having no reference point or feedback, which means in the long term it will be very inaccurate. This is solved by using a reference point (mostly the full charge point) to re-calibrate the estimation. More complex algorithms also use the history of the battery performance (expressed in State of Health (SoH)) to re-calibrate the maximum charge.

OTHER METHODS

More complex algorithms to estimate the SoC are also being developed. Neural Networks can be used [18] possibly with fuzzy logic [17], (Robust) (Extended) Kalman Filters can be used (REKF)[19] and electrical models can be used [17]. Combinations of these methods are also used. Direct methods are not available for Li-ion packs, while they are for lead-acid batteries.[17]

4.2. DESIGN

4.2.1. BATTERY PACK

The battery chemistry chosen is Li-ion. There are different cathode/anode chemistry combinations available. These all result in slightly different characteristics. For this design the most important one is capacity, since protection will be added for the pack. The battery chosen is the Panasonic NCR18650B 3350mAh.²

It was chosen to use a standard size battery, because these are easily replaceable which is important for the DeciZebro. The 18650 battery is one of the most used Li-ion batteries. Eight of these batteries could be fitted in the size allocated (see Appendix B). These are connected in a 4s2p (4 series, 2 parallel) pack to get a nominal voltage of 14.8V. The nominal capacity available is 6.7Ah or 99.2Wh.

The pack is provided with two connectors. One is a 5-pin low power connector used for the cell balancing. The connector of choice is a JST-XH 5 pins connector. The other connector is a JST-VH-B2P, used for the power transfer to the battery. These are both connected to the PCB on which the BMS is placed.

4.2.2. BATTERY MANAGEMENT SYSTEM - SCHEMATIC

The BMS should implement a range of protection features (Over-current (charge/discharge), Over-voltage and Temperature). It should also be capable of charging the battery cells, balancing the battery cells and discharging the battery cells. The BMS should provide the control of the Power Management System with information about the battery (SoC, SoH, Voltage, Current draw). It should also be able to provide the PMS with an error code when a protection feature is activated.

The BMS should support up to 4 Li-ion cells in series with a capacity of 6.7Ah each.

Because of time constraints an integrated solution was desired. Because of experience in the DeciZebro team with the bq-series of Texas Instruments and availability of the evaluation boards of this series these were considered.

The bq78350-r1 in combination with the bq76920 is a solution that implements all these features and more. It provides a SoC estimation using a Coulomb Counter that is compensated for the SoH. [20] It also provides a SoH estimation. The current draw can be read by the control of the PMS, as well as activation of the protection features. These protection features include:[21]

- Over-current in Discharge
- Short Circuit in Discharge
- Over-voltage
- Under-voltage

It is also capable of cell balancing. All features are programmable according to the cell chemistry and pack layout. This programming will be discussed in section 4.2.3

It provides communication over the SMBus protocol, which is based on the I²C interface.[22] More about this communication can be read in the thesis of the control subgroup. [2]

The implementation of this integrated solution can be found in appendix C. This schematic will now be further discussed.

CELL BALANCING

R14-R18 in combination with C10-C14 and the bq76920 are used to balance the cells. If unbalance is detected in the cells the bq76920 connects the two pins connected to the cell with the higher voltage, which creates a path for the current with a 2 kΩ impedance for DC. This drains the cell with a maximum current of $\frac{4.2V}{2k\Omega} \approx 50\text{mA}$ to balance the cell with other cells. The capacitors are used to block the switching noise generated in the bq76920 from reaching the cell. The values used for the resistors as well as the capacitors are recommended by the manufacturer.

CURRENT SENSING

The current sensing is done using a shunt resistor. This is resistor PE2512FKE7W0R01Z1. The voltage over this resistor is then measured by an Analog to Digital Converter (ADC) inside the bq76920. The recommended input range of this ADC is $\pm 200\text{mV}$. [21] Since the current through the resistor is fused at 10A, this would mean the optimal resistance to maximise accuracy is 20 mΩ, however during a short circuit situation the current will

²<https://www.nkon.nl/rechargeable/18650-size/panasonic-ncr18650b-made-in-japan.html>

be above this 10A for a short time period. The [ADC](#) could then be damaged. This is why a resistance of 10 mΩ is used.

CHARGE/DISCHARGE SELECTION

The bq76920 can drive two MOSFETs that determine whether power can enter or leave the battery. These are managed so that only one of these can be on at the same time. The MOSFETs driven are Q2 and Q4. Additional circuitry has been added to provide load detection. When the PACK- pin is high while CHG is off because a load is present, the CHG pin is pulled high through R25, R26. This can then be read-out by the microcontroller. A diode (D_CHG1) is added to make the CHG pin able to drive the MOSFET. Q3 is added to protect the CHG pin from voltages below Vss, when PACK- is being pulled below Vss.

THERMISTOR READ-OUT

The bq76920 supports a read-out of 1 thermistor. This is done using the measurement of the voltage on pin VC1 and a voltage divider. The thermistor recommended is a 10 kΩ resistance, in combination with R24, which is also 10 kΩ. This means at room temperature (25 °C) the voltage measured on pin TS1 is $\frac{1}{2} * VC1$. The voltage is then converted to a digital temperature value using an [ADC](#).

LED DISPLAY

The 5 LEDs on the [PCB](#) (D8-D12) are used to indicate the [SoC](#) of the battery pack. The bq78350-r1 has internal LED drivers to power these LEDs. The DISP port is used to enable or disable the display. The DISP pin is pulled high by the 221 kΩ resistor (R29). This means for our system the LEDs are always turned on.

VOLTAGE MEASUREMENT

The voltage measurement of the pack is done using the voltage division between R27 and R28. This gives a maximum voltage of 0.1 V on the BAT pin. This voltage is used in the [SoC](#) estimation algorithm.

OTHERS

Decoupling capacitors are added as recommended by the datasheet. [21] TVS diodes are placed near both power connectors, as these are directly connected to MOSFETs, which are sensitive to [ESD](#). This is prevented by placing the [TVS](#) diodes. For the balance connector this was not needed, as this connector is connected to passive components that are better at handling [ESD](#).

4.2.3. BATTERY MANAGEMENT SYSTEM - PROGRAMMING OF THE BQ78350-R1

The programming of the bq78350-r1 was done using the EV2300 in combination with bqStudio. The software supports the Li-ion batteries chosen. This means a lot of settings are automatically correct. Calibration should however be done manually, as well as setting the correct battery topology (4s2p). All protection settings should also be set.

The minimum voltage of the individual cells is set to 3.0V, while the datasheet recommends 2.5V cut-off. This is done because the battery monitoring electronics should stay on. This means some capacity is lost, however most capacity can still be used. The absolute voltage cut-off is set at 2.6V to be safe.

The maximum current draw is set at 6.7A, since this is the maximum current that should be needed for the output. While the battery can supply more as long as 2 are in parallel, when one battery dies or is disconnected for some reason, the other battery can supply a maximum of 6.7A. This means the system can still function with half of the batteries disconnected.

The thermistor TS1 should be set to cell temperature, the FET temperature should be monitored separately. Precharge should be enabled, since this makes the charging more efficient. Both FETs should be turned off in all current-based faults.

Removal recovery should be enabled. This senses a digital transition of the PRES pin after which the system recovers. This happens when the pack is disconnected and connected again.

For this prototype all faults should be reset manually, to make the device more safe. This makes sure the electronics do not recover themselves causing them to repeatedly get the same fault, which might cause the DeciZebro to overheat. After testing using these settings this could be less strict and only require manual reset for some of the faults. This means all faults should be set in the Permanent Fail setting.

The display should be configured to use the LEDs to display the [SoC](#).

5

OUTPUT CONVERSION

The output conversion design will be discussed in this chapter. First the topology of the output will be given. Followed by a section which discusses the choice and design of each component that is used in the output.

5.1. TOPOLOGY

The topology of the output subsystem can be found in the figure below.

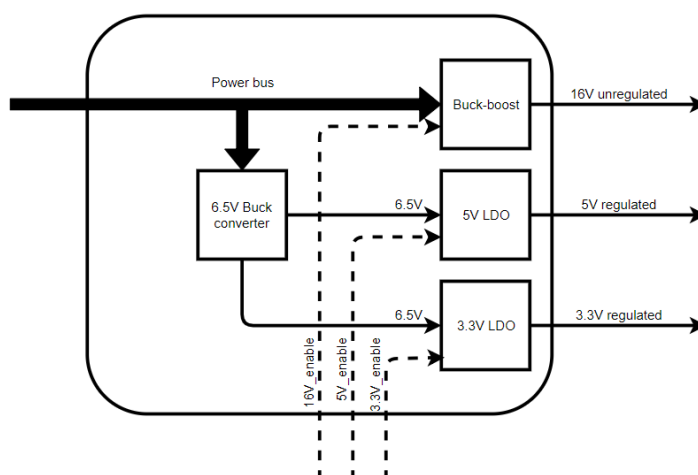


Figure 5.1: Topology of the output subsystem

Chapter 4, mentions that the battery voltage lies between 12 volt (when empty) or 16.8 volt (when fully charged). This means that the power bus also lies between 12 and 16.8 volt. For the 16V busses, this means that when the power bus voltage is 16.8V, it needs to be stepped-down to 16V and when the power bus voltage is 12V, it needs to be stepped-up to 16V. The appropriate converter that can handle this requirement is the buck-boost converter. Since the unregulated 16V busses can pull 5A, this means that the 16V bus can pull a total of 80 watt from the batteries. For this reason, the chosen buck-boost converter requires a high efficiency.

In order to use an LDO, a buck-converter is used to convert the power bus voltage (12V-16.8V) to a voltage of 6.5V. By bringing the voltage from the power bus to a voltage of 6.5V with a buck-converter, proves to be more efficient than using only an LDO. With a voltage of 6.5 volt at the input of each LDO, it is converted into a regulated 5V and 3.3V respectively.

In case of a fault detected by the safety & control subsystem, the converters need to be individually enabled or disabled. The lines that stem from the converters are the control lines. These lines are connected to the MCU which determines when to enable/disable the converter.

5.2. BUCK-BOOST CONVERTER TRADE-OFF

As mentioned before, a buck-boost converter can both step-up and step-down the voltage. To choose a suitable buck-boost converter, first the requirements need to be known. These are as follows:

1. Minimum input voltage of 12 volts or lower
2. Maximum input voltage of 16.8 volts or higher
3. Maximum output current of 5 ampere
4. High efficiency ($> 90\%$)
5. Needs to be available and in stock
6. The whole circuit of the buck-boost needs to be as small as possible due to space constraints on the main PCB
7. As cheap as possible
8. Enable pin

There exists many different buck-boost converter topologies, however the four main topologies are: buck-boost, Ćuk converter, SEPIC converter and the four-switch buck-boost. A general overview will be given between the four topologies, and the chosen topology will be further discussed in depth.

BUCK-BOOST

A generic buck-boost converter is a voltage to voltage converter. The input is a voltage source, this voltage source gets converted to a current source through the use of an inductor. At the output, the current source gets converted to a voltage source through the use of a capacitor at the output. Since this capacitor and inductor are part of the topology, and thus needed for operation, an additional transformer is not needed. [23] Since the power bus and the output busses are both voltage sources, this is ideal. This way, the system is more efficient since it doesn't need to transform current to voltage. This converter also utilizes little components, however unfortunately also a diode. Using a diode in most power systems is a massive power drain. Thus often resulting in the conversion having low efficiency. Additionally, the buck-boost is an inverting topology, this can complicate things even further. [24]

ĆUK CONVERTER

From the observations made earlier ([23]), it can be concluded that the Ćuk converter is a current to voltage converter. This is not ideal for the system since it introduces unnecessary losses. It also inverts the output, while needing two inductors and two capacitors. The inductors need to be rated for a relatively high current, while also having a low resistance. This often results the inductor to be fairly large and thus not very ideal for a PCB with a lot of components and a space constraint.

SEPIC CONVERTER

The SEPIC converter is also a current to voltage converter. For the same reason as explained above, this is not ideal. The converter also uses two inductors and two capacitors like the Ćuk converter, however it doesn't invert the output. The SEPIC convert can be hard to control, compared to other topologies.

FOUR-SWITCH BUCK-BOOST

This topology is the result of cascading a boost-converter and a buck-converter. When $V_{in} > V_{out}$ the converter operates in buck-mode. When $V_{in} < V_{out}$ the converter operates in boost-mode. It also uses only one inductor and one capacitor compared to the Ćuk- and SEPIC converters. The original buck and boost converters contain a diode in their circuit. However this topology replaces those diodes with MOSFETs. This results in the topology to use four MOSFETs. Since MOSFETs have low power losses compared to diodes, they improve the overall system efficiency.

All in all, the Ćuk- and SEPIC converters both require larger components and are both not as efficient as the other topologies. An advantage that the Ćuk- and SEPIC converters have, is that the switching MOSFETs in both topologies are placed at the output, instead of the input. This means that the input is not affected by the switching of these MOSFETs. It turns out that the inductors needed in a Ćuk converter, require more

space then the four MOSFETs and the inductor (used in the buck-boost) combined. Eventually this slightly reduces the footprint and also slightly reduces the cost. The same holds for the SEPIC converter. Thus the four-switch buck-boost is the preferable topology. Reaching both higher efficiency while having a slightly smaller footprint, it is the ideal choice. However, in this case, the MOSFETs are located at the input. This leads to the input current forming a ripple. This ripple can be rather problematic and will be further discussed in Chapter 6.

5.3. THEORETICAL BACKGROUND

This section will discuss the theoretical background of the four-switch buck-boost converter, buck converters and the LDOs.

5.3.1. FOUR-SWITCH BUCK-BOOST THEORY

As mentioned before, the four-switch buck-boost is a cascaded combination of a buck-converter and a boost converter. First the buck mode will be discussed. This is followed by a discussion of the boost mode. The schematic of a four-switch buck-boost can be found in the figure below.

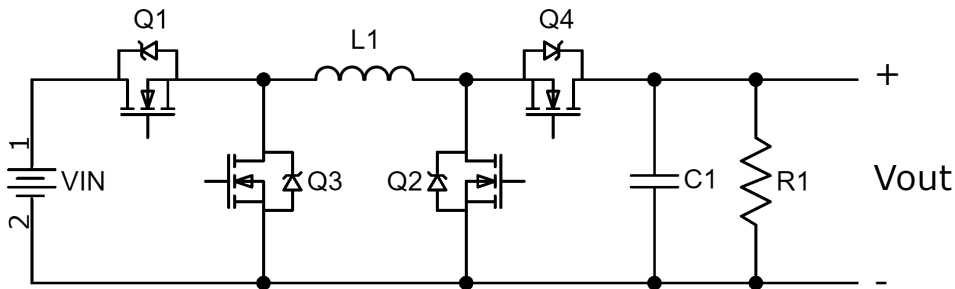


Figure 5.2: Schematic of a four-switch buck-boost

BUCK MODE

When $V_{in} > V_{out}$, the converter requires operation in buck mode. This is done by switching Q4 on and Q2 off. The schematic that remains is known as the buck converter. The schematic is found below.

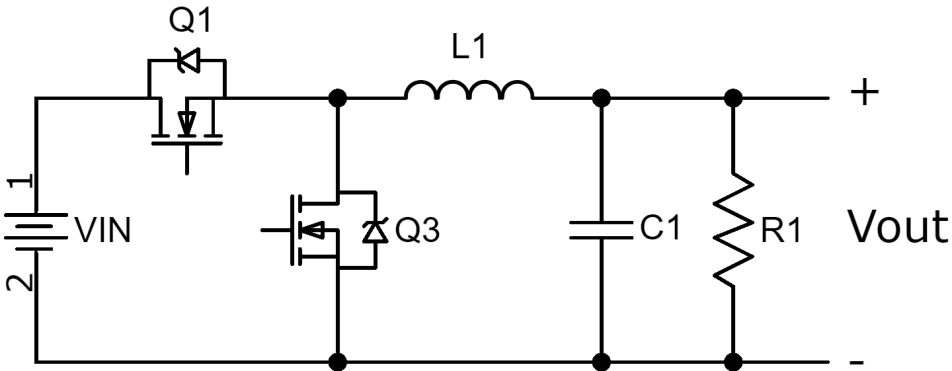


Figure 5.3: Four-switch buck-boost when in buck mode

The **Pulse Width Modulation (PWM)** is generated on switch Q1, which leaves switch Q3 to function as a diode. The buck converter functions exactly as a normal buck converter would. When Q1 is open, the current through the inductor (L1) slowly rises. To oppose the current change through the inductor, a voltage is generated that opposes the source voltage, thus reducing the output voltage. However, when left on long enough, the current eventually stops changing, which results in the voltage generated by the inductor to also decrease. This causes the output voltage to rise again, since less voltage opposes the source voltage. In order to prevent this, Q1 needs to be closed in time. If done correctly (when the current is still increasing) the voltage generated across the inductor will remain. The energy is stored in the form of a magnetic field. When Q1 is closed, the inductor acts as a current source and the current decreases. Eventually, the magnetic field

generated by the inductor depletes which results in an output voltage of zero. Like before, to prevent this, Q1 needs to be opened at the right time. If this cycle is done correctly, the output voltage gets reduced exactly to what is required by having the correct duty-cycle.

BOOST MODE

When $V_{in} < V_{out}$, the converter needs to operate in the boost mode. This is done by switching Q1 on and Q3 off. The schematic that remains is known as the boost converter. The schematic is found below.

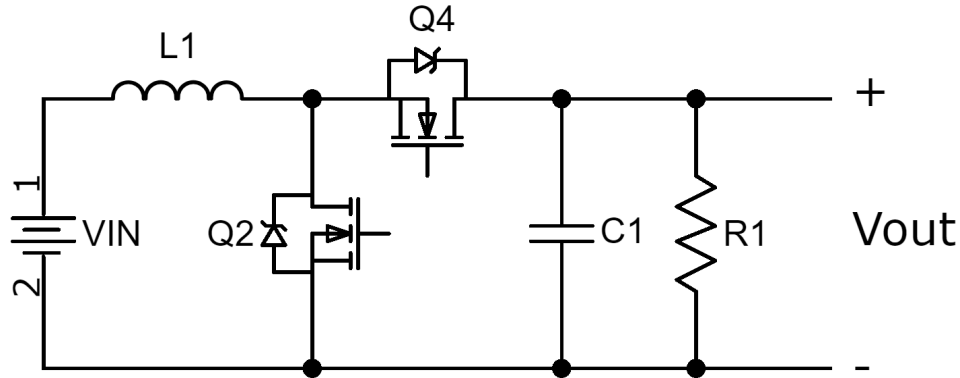


Figure 5.4: Four-switch buck-boost when in boost mode

The PWM is generated on switch Q2, which leaves switch Q4 to function as a diode. The boost converter functions exactly as a normal boost converter would. When Q2 is open, the current through the inductor (L1) slowly rises. This generates a voltage that opposes the voltage source and thus lowers the output voltage. To prevent this, Q2 should close. This allows the magnetic field generated by the inductor to convert into current flowing to C1 and R1 in order to oppose the current change. Since the impedance is higher than the open-state, current eventually decreases. This generates a voltage across the inductor, however this time the voltage supports the voltage source, thus increasing the output voltage. If the cycle is done correctly, the output voltage gets boosted exactly to what is required by having the correct duty-cycle.

TRANSITION MODE

When V_{in} roughly equals V_{out} , the converter operates in the transition mode. In this mode Q3 and Q2 are open, while Q1 and Q4 are closed. This basically functions as a straight line letting the input voltage directly equal the output voltage.

5.3.2. BUCK

Since the buck converter which is going to be used for the LDOs is just a simple buck converter, the explanation of how it works is already discussed in section 5.3.1.

5.3.3. LOW-DROPOUT REGULATOR

A low-dropout regulator functions almost exactly as a linear voltage regulator. These regulators have the advantage that they are absent of a high switching noise and have a low component count. However, unlike the switching converters (e.g. buck, buck-boost etc) they need to dissipate power and are thus less efficient. The schematic is shown below.

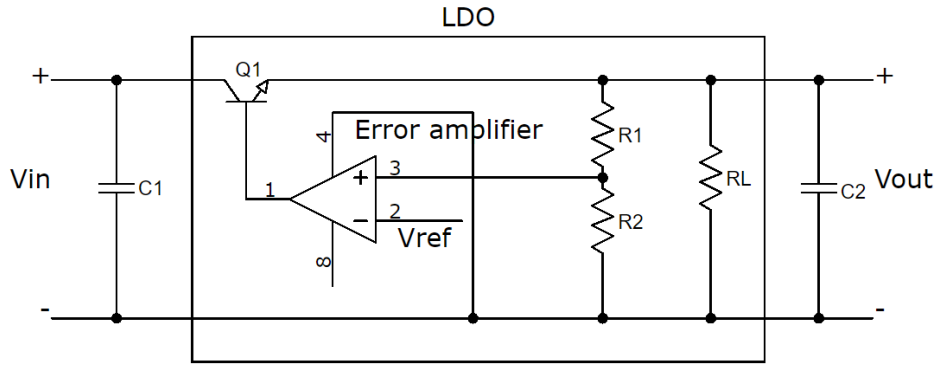


Figure 5.5: LDO schematic

Where V_o is the output voltage, V_i the input voltage, I_o the output current and I_q the current drained when the LDOs is has no load at the output. The LDO functions by comparing the output voltage with the reference voltage. The difference between a low-dropout regulator and a linear voltage regulator, is that the minimum input voltage needed for regulation can be much lower compared to the linear voltage regulator. This effectively means less power is 'thrown away' by the LDO. The efficiency of the LDO is given by the formula given below. [[25]]

$$\eta = \frac{I_o V_o}{(I_o + I_q) \cdot V_i} \cdot 100 \quad (5.1)$$

As can be concluded from the equation, the bigger the difference between the input and output voltage ($V_i + V_{dropout} \geq V_o$), the lower the efficiency.

The LDO makes sure the output voltage stays at exactly the correct voltage. This makes the output regulated. When the output voltage is higher than the reference voltage, the error amplifier amplifies the difference between the inputs to turn open Q1. This results in the voltage decreasing at the output. When the output voltage is lower than the reference voltage, the error amplifier forces Q1 to close. This results in the voltage to increase. Thus the output voltage oscillates. however this oscillation often has a very low ripple.

5.4. DESIGN

This section will discuss the design of the buck-boost converter, buck converter and the LDO. The circuits will be given and discussed.

5.4.1. BUCK-BOOST

The chosen Integrated Circuit (IC) is the LM5176 four-switch synchronous buck-boost controller by TI. This IC fulfils the requirements 1 through 5 and 7 and 8 stated in section 5.2. Since the 16V unregulated bus needs to supply 80W peak, efficiency is more important than PCB space required. For this reason 6 is not fulfilled. The most important specs are given in the list below, the rest of the specs can be found in the datasheet. [26]

1. Wide V_{IN} : 4.2V to 55V
2. Flexible V_{OUT} : 0.8V to 55V
3. High efficiency buck-boost transition
4. V_{OUT} short protection
5. Adjustable switching frequency
6. Optional input or output average current limiting

"High efficiency buck-boost transition" basically means that the LM5176 employs extra control when switching converter modes. This assures a low ripple voltage at the output. The LM5176 also contains integrated current limiting for protection against over-currents or short-circuits. The current at which this happens can

be chosen freely, the same holds for the switching frequency. The parameters that need to be set are: the output voltage, inductor selection, maximum output voltage ripple, maximum current ripple, current limit and the switching frequency. The calculations are given for each parameter and at the end of this section the schematic is given and discussed.

OUTPUT VOLTAGE

To configure the correct output voltage, the correct resistors for voltage division at the FB pin of the LM5176 need to be changed to the correct value. This value can be calculated by the equation below.

$$R_{FB2} = \frac{V_{OUT} - 0.8V}{0.8V} \cdot R_{FB1} \quad (5.2)$$

Where R_{FB1} is chosen to be 20 k Ω in this case. For an output voltage of 16V, the feedback resistor is calculated to be 383 k Ω .

SWITCHING FREQUENCY

Choosing the switching frequency is a trade-off. A higher switching frequency results in: smaller capacitor and inductors, lower efficiency and a lower achievable output voltage. While a lower switching frequency results in: bigger capacitor and inductors, higher efficiency and a higher achievable output voltage. The switching frequency can be calculated according to the equation below.

$$R_T = \frac{\left(\frac{1}{F_{SW}}\right) - 190ns}{116pF} \quad (5.3)$$

The switching frequency can be between 100 kHz and 600 kHz. Since space is an important constraint of the system design, the frequency can't be too low. However, in order to preserve efficiency, a very high frequency is also not a good choice. For this reason, a frequency of around 350 kHz was chosen. However, a resistor of 23 k Ω wasn't available due to time of purchase. For this reason, a resistance of 23.2 k Ω was chosen. Resulting in a switching frequency of 347 kHz.

INDUCTOR SELECTION

When choosing the optimal inductor value, a trade-off should be made between the maximum ripple current at the output and the size of the inductor. Since the power management system on the PCB has a space constraint, the size of this inductor is slightly more important than the maximum ripple current. According to the datasheet, in the buck mode, the inductor selection is based on limiting the peak to peak current ripple ΔI_L to 40% of the maximum inductor current at the maximum voltage. This can be calculated according to the equation below.

$$L_{BUCK} = \frac{(V_{IN(MAX)} - V_{OUT}) \cdot V_{OUT}}{0.4 \cdot I_{OUT(MAX)} \cdot F_{SW} \cdot V_{IN(MAX)}} \quad (5.4)$$

For $V_{IN(MAX)}$, 16.8V is chosen, $I_{OUT(MAX)}$ 6.7A and V_{OUT} 16V. This results in a L_{BUCK} of 0.82 μ H.

According to the datasheet, in the boost mode, the inductor selection is based on limiting the peak to peak current ripple ΔI_L to 30% of the maximum inductor current at the maximum voltage. This can be calculated according to the equation below.

$$L_{BOOST} = \frac{V_{IN(MIN)}^2 \cdot (V_{OUT} - V_{IN(MIN)})}{0.3 \cdot I_{OUT(MAX)} \cdot F_{SW} \cdot V_{OUT}^2} \quad (5.5)$$

For $V_{IN(MIN)}$, 12V is chosen, $I_{OUT(MAX)}$ 6.7A and V_{OUT} 16V. This results in a L_{BOOST} of 2.7 μ H. In this case, the inductor in the boost mode requires a larger inductor value. However, this too is a trade-off between maximum ripple current (as can be seen in the equations themselves) and the inductor size. A higher inductor value results in a lower maximum ripple current but a larger inductor. As mentioned before, since space requirements are slightly more important to the power management system PCB, a lower inductor current is chosen. A standard inductor value of 2.20 μ H is readily available and thus will be used. This will result in slightly higher ripple current in the boost mode and a lower ripple current in the buck mode. This higher ripple current is not harmful when capacitors with a low equivalent series resistance ([Equivalent Series Resistance \(ESR\)](#)) are used. Since capacitors can't dissipate a lot of heat, a high ripple current can potentially

generate a lot of heat if the [ESR](#) of the capacitor is high. For this reason, ceramic capacitors should be used at the output, to ensure a low [ESR](#) and thus prevent capacitors from overheating and damaging the system.

The maximum current through the inductor can be calculated from the following equation.

$$I_{L(PEAK)} = \frac{V_{OUT} \cdot I_{OUT(MAX)}}{0.9 \cdot V_{IN(MIN)}} + \frac{V_{IN(MIN)} \cdot (V_{OUT} - V_{IN(MIN)})}{2 \cdot L1 \cdot F_{SW} \cdot V_{OUT}} \quad (5.6)$$

Assuming an efficiency of at least 90%, the $I_{L(PEAK)}$ is calculated to be 12A. Thus the inductor should be rated for this current.

MAXIMUM OUTPUT VOLTAGE RIPPLE

Since there was no requirement given for the maximum output voltage ripple, it was assumed to have it as low as possible while not sacrificing too much space. To reduce the output voltage ripple, a low [ESR](#) is required. A capacitor has an [ESR](#), the maximum ripple current generates a maximum ripple voltage. This maximum ripple current occurs at the minimum input voltage. The maximum output voltage ripple due to the maximum ripple current through the capacitor can be calculated by the equation given below.

$$\Delta V_{RIPPLE(ESR)} = \frac{I_{OUT(MAX)} \cdot \sqrt{\frac{V_{OUT}}{V_{IN(MIN)}} - 1} \cdot V_{OUT}}{V_{IN(MIN)}} \cdot ESR \quad (5.7)$$

Assuming an [ESR](#) of 0.15 mΩ, the ripple voltage caused by [ESR](#) is equal to 0.8 mV. This is almost negligible.

In order to smooth the output voltage and have a low voltage ripple, a relatively high capacitor value is required. Looking at the example in the datasheet, a voltage ripple of around 25 mV is used. In order to calculate the output capacitor required to achieve this voltage ripple, the equation below is used.

$$\Delta V_{RIPPLE(COUT)} = \frac{I_{OUT} \cdot \left(1 - \frac{V_{IN(MIN)}}{V_{OUT}}\right)}{C_{OUT} \cdot F_{SW}} \quad (5.8)$$

Assuming a maximum voltage ripple of 23 mV, a capacitor value of 216 μF is required. The datasheet recommends a combination of ceramic and bulk capacitors for low [ESR](#).

CURRENT LIMITING

For protection against short-circuits and over-currents, a current limiter is available on the LM5176. It basically functions by choosing a resistor which has a very low resistance. This makes it so that, even with high currents, the voltage drop across the resistor is very small (in the order of milli-volt). This allows the [IC](#) to sense this voltage drop and by using a comparator, determine whether there is a short-circuit or an over-current. However, the LM5176 doesn't contain an external pin which the safety & control group can read. This is important because the group needs to know whether there is a short-circuit or an over-current for telemetry. To avoid complications, the safety & control group should employ their own safety on the 16V voltage bus. Thus this function is disabled.

SCHEMATIC OF THE LM5176

The schematic of the LM5176 is given in the figure below.

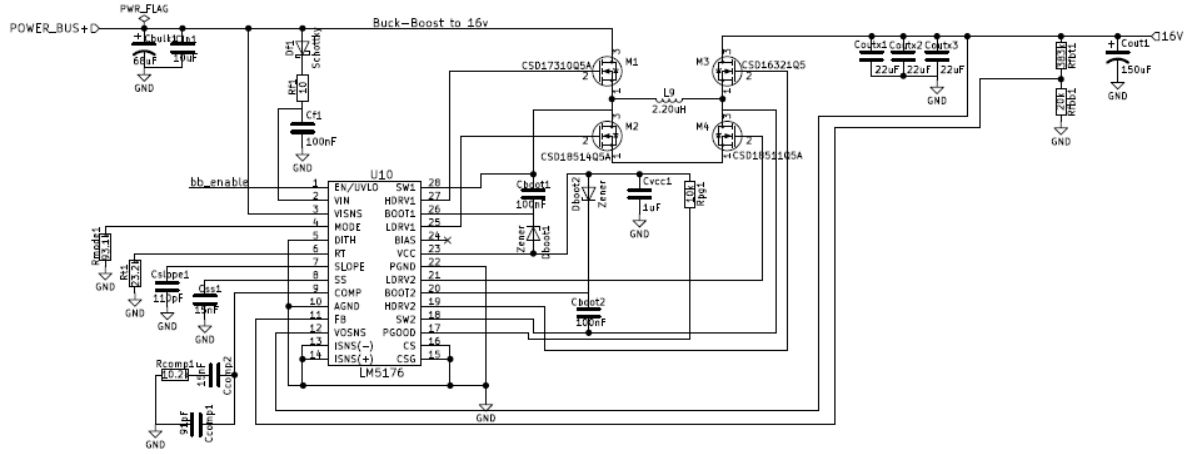


Figure 5.6: LM5176 schematic

Looking at the output capacitors, a total of 216 μF can be seen. The 22 μF capacitors have an [ESR](#) of 2.05 m Ω , while the 150 μF capacitor has only 0.020 m Ω . Having these capacitors in parallel, reduces the [ESR](#) to the value used in the calculation of the $V_{\text{RIPPLE(ESR)}}$. As explained before, to set the output voltage, a resistor divider circuit is used. This can be seen in front of the three parallel capacitors at the output. Furthermore, connected to the RT pin is the 23.2 k Ω resistor. This resistor sets the frequency to 347 kHz. Also, in between the four MOSFETs, the inductor value of 2.20 μH can be found.

The four MOSFETs chosen are four different N-channel MOSFETs. This is done in order to achieve a high efficiency. As explained in section [5.3.1](#), two MOSFETs are [PWM](#) and the other two act as diodes. M1 and M3 are high-side switching MOSFETs, while M2 and M4 are low-side switching MOSFETs. Since the power bus voltage is between 12V and 16.8V, the LM5176 operates in boost mode most of the time. For this reason, to preserve cost, the MOSFETs M3 and M4 (which correspond to the MOSFETs Q4 and Q2 respectively in figure [5.4](#)) are required to have a low $R_{\text{DS(on)}}$, thus making the switching more efficient as less power is lost in the MOSFETs.

The high-side MOSFETs are required to have a rather low V_{GS} , that make it ideal for switching and also save some space. The reason being, that high-side MOSFETs are not referenced to ground. Therefore, on the source side of the MOSFET, the supply voltage is present. In order to enable the MOSFET, the gate voltage needs to be higher than the source. For this reason, the bootstrap capacitors are used in the circuits (Cboot1 and Cboot2). They are connected between the SW1/SW2 pin and the BOOT1/BOOT2 pin of the LM5176. This is necessary as the HDRV1/HDRV2 requires an extra boost in voltage in order to raise the gate voltage higher. If the V_{GS} voltage is lower, a smaller capacitor can be used and can be switched faster. For both the high-side MOSFETs, a 100 nF bootstrap capacitor is used. Low-side MOSFETs can have higher V_{GS} , since they are referenced to ground, thus making them easier to switch. The safety & control group handle the current limiting. For this reason the ISNS(-)/ISNS(+) together with the CS/CSG pins, are shorted. This disables the LM5176 from current limiting without the knowledge of the MCU. All other component and values can be found in the datasheet of LM5176.

5.4.2. BUCK

The chosen [IC](#) is the TPS565201 synchronous step-down voltage regulator. The specifications of this buck-converter are simple. It has a 4.5V to 17V input, output voltage from 0.76V to 7V, 5A max current and a set 500 kHz switching frequency. This buck-converter doesn't need an enable pin since it isn't directly connected to the output. Also, because the power draw is very low compared to the unregulated 16V bus, efficiency should still be high, but not in the 90-th percentile. Which parameters will be changed and the calculation will be discussed below.

OUTPUT VOLTAGE, INDUCTOR VALUE AND INPUT CAPACITORS

Like with the LM5176, the output voltage is set by a feedback network consisting of a simple voltage division circuit. The output voltage can be set according to the equation found in the datasheet [\[27\]](#), given by:

$$V_{\text{OUT}} = 0.760 \cdot \left(1 + \frac{R1}{R2}\right) \quad (5.9)$$

The datasheet recommends choosing a large-enough resistor value to improve efficiency at light loads, but not too high to reduce noise. In table 2 of the datasheet, a table with recommended component values is given. From this table it can be determined that R1 should be 75 k Ω , R2 10 k Ω , L1 3.3 μ H, C8 and C9 can be chosen between 20 to 60 μ F. Since space is important, the standard value 22 μ F capacitor is used for both C8 and C9. The peak ripple current can be calculated by the following equation.

$$I_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \cdot \frac{V_{IN(MAX)} - V_{OUT}}{L_O \cdot f_{sw}} \quad (5.10)$$

and

$$I_{PEAK} = I_O + \frac{I_{P-P}}{2} \quad (5.11)$$

The datasheet recommends to use $f_{sw} = 550$ kHz for this calculation. Using V_{OUT} to be 6.5V and $V_{IN(MAX)}$ to be 16.8V, the peak current can be calculated with equations 5.10 and 5.11. This results in a peak current of 3A.

INPUT CAPACITOR & BOOTSTRAP CAPACITOR

The datasheet recommends a decoupling capacitor and a bulk capacitor at the input. A ceramic capacitor over 10 μ F and an additional 0.1 μ F for high frequency filtering. The capacitor voltage rating is to be greater than the maximum input voltage. For the bootstrap capacitor, a 0.1 μ F ceramic capacitor is recommended to be connected between VBST and the SW pin.

TPS565201 SCHEMATIC

The schematic of the TPS565201 buck-converter is given in the figure below.

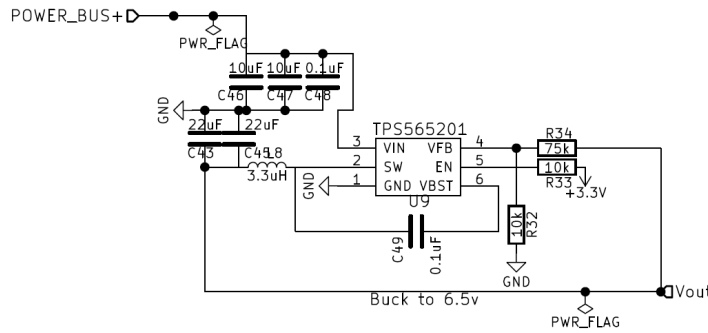


Figure 5.7: TPS565201 schematic

The voltage division required for setting the output voltage is connected to the VFB pin. Since the TPS565201 does have an enable pin, it is always enabled by using a 10 k Ω pull-up resistor. Between the VBST and SW pins, a 0.1 μ F ceramic capacitor is used for proper operation. For the input capacitor, two 10 μ F ceramic capacitors plus an additional 0.1 μ F capacitor is used. The output capacitors (previously named C8 and C9) are connected to the SW pin, together with the 3.3 μ H inductor.

5.4.3. LOW-DROPOUT REGULATOR

The chosen ICs for the 3.3V and 5V regulated output busses are the LP38692-3V3 and LP38692-5V linear regulators respectively. These LDOs are internally set to regulate 3.3V or 5V and thus have very little required external components. They are rated for a 1A load current, exactly what is required to be the maximum rated current of each bus. Included options are, thermal overload protection, foldback current limiting and an enable pin. For voltage regulation to occur, the input voltage needs to be a minimum of 5.5V (5V + 450 mV drop-out voltage). Thus, the 5V LDO will regulate the output voltage of the buck-converter of 6.5V to 5V. And the 3.3V LDO will regulate 6.5V input to 3.3V output. This does mean that the 3.3V bus is less efficient compared to the 5V bus. However, these losses are negligible compared to the 16V bus.

INPUT AND OUTPUT CAPACITORS

Since most of the circuitry is integrated in the IC, the only external components that need to be manually added are the input and output capacitors. The datasheet of the LP38692 [28], recommends a 1 μ F ceramic capacitor both at the input and the output.

LP38690/92 SCHEMATIC

The schematic of the LP38690/92 LDO is given in the figure below.

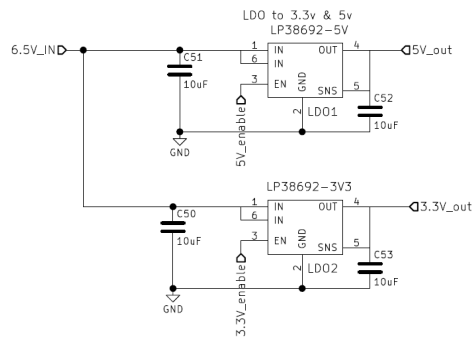


Figure 5.8: LP38690/92 schematic

The output of the TPS565201 buck-converter is directly connected to the input of these LDOs. The input and output capacitors are both chosen to be 10 μ F for added stability, without increasing the required size. Since the LDOs don't have an integrated current limiter, the safety & control group will need to add their own monitoring and safety at the output of these regulated busses. Control functionality is supported by use of enable pins to disable/enable the LDOs individually.

6

EMI FILTER

Because two converters with a switching input were placed in parallel and switching components generate noise pulses every switching cycle, these converters could influence each other and start resonating. For this reason EMI filters were added at the input of both DC/DC converters. This section discusses the theoretical background and design of the EMI filters.

6.1. THEORETICAL BACKGROUND

6.1.1. DEFINITION OF EMI

Electromagnetic interference (EMI): the degradation in performance of a device, equipment, or system caused by electromagnetic disturbance.[29] This disturbance is mainly created by switching and by electrical motors.

EMI can be classified in Differential Mode (DM) noise and Common Mode (CM) noise. DM noise is a current that is flowing in opposite directions, while CM noise is flowing in the same direction.

6.1.2. REASONS FOR USAGE

EMI filters suppress noise at high frequencies (normally above 150kHz). This can be done using either passive or active filters. Active solutions often require more expensive filters because they add their own noise.[30]

EMI filters are used in all consumer products that produce (too much) noise at a frequency above 150kHz. Products brought onto the market after January 1, 1996 have to be compliant with the European Electro-Magnetic Compatibility (EMC) standards.[29] The 150kHz cut-off is normally chosen because regulations start at this frequency.

Since the DeciZebro is not a consumer product, this regulation is not applicable. There are however other reasons to use EMI filters. When placing input-switching converters in parallel, like in the design of the PMS of the DeciZebro, the switching noise of converter 1 can start interfering with the switching of converter 2. This can eventually result in resonance and non-optimal working of the converters. Reducing the switching noise at the input of both converters can prevent this. [31]

6.1.3. IMPLEMENTATIONS

A schematic of a much used EMI filter is given in figure 6.1. The CM components are used to filter the CM noise, while the DM components are used to filter DM noise.

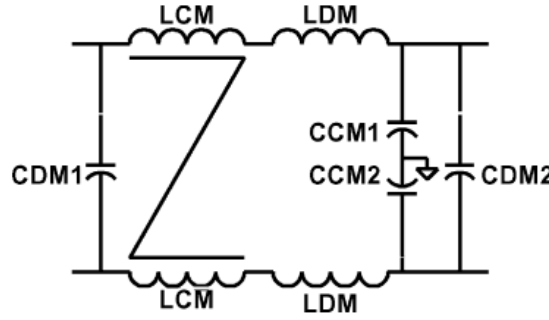


Figure 6.1: A common design of an EMI filter.[4]

More advanced implementations are also used, these are better performing but also more expensive. Power efficiency often is worse as well, since active components are used. Since performance requirements were not very strict not a lot of further research has been done.

6.2. DESIGN

Since the converters switch at a frequency of 347 kHz and 500 kHz, the noise produced will be at multiples of this frequency. There are however also different EMI noise sources in the DeciZebro, such as the 6 DC motors used for the legs. This is why a lower cut-off frequency was chosen. The lower the cut-off frequency the larger the components get. This is why a frequency lower than 150 kHz was chosen, in case the power supply would ever be used in a consumer product (the DeciZebro might one day be sold as an education kit).

It was chosen to use a symmetric filter, that only filters DM noise, since this is the noise that is generated by switching. CM noise is picked up on the power lines, but these are kept as short as possible on the PCB to prevent a large CM noise. The final result can be seen in section 6.2.1

6.2.1. FINAL RESULT

In figure 6.2 the topology used and the values of the components can be seen. The topology acts as a low-pass filter in both directions for DM noise. A mistake had been made in the calculations of f_{-3dB} . While

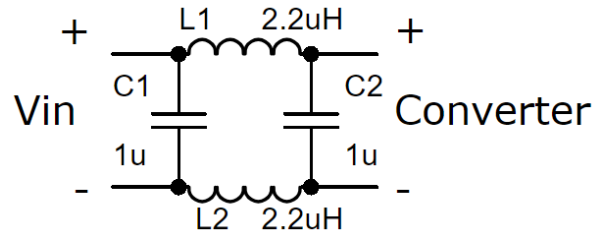


Figure 6.2: The design of the EMI filter

the intention was to use standard values to get the cut-off frequency below 150 kHz, a factor 2 mistake had been made which resulted in $f_{-3dB} = 76\text{kHz}$. This means the components used are not the smallest possible, however this proved to be no problem while designing the PCB. In a new version of the PCB this could be changed. This should be done according to equation 6.1.

$$f_{-3dB} = \frac{1}{2\pi} \frac{1}{\sqrt{2LC}} \quad (6.1)$$

In which L and C are the values for both L1, L2 and C1, C2 respectively. The inductors should support their respective converters maximum output current, while the capacitors should support the maximum power bus voltage.

7

SYSTEM INTEGRATION

After every subsystem had been designed individually they could be integrated with ease because the requirements of all subsystems had been defined clearly. After the integration of the subsystems fuses were added where needed in order to protect the system and the DeciZebro from faults.

7.1. BMS

The Battery System was integrated using the connectors specified in chapter 4. The output subsystem was integrated in the PCB design with the input and control subsystems. This process is explained in section 8.2.

7.2. POWER BUS

The final output schematic can be seen in Appendix E. Looking at the figure, it can be seen that a shunt current sensor monitors the bus current and voltage. In case of a power fault, the MCU is notified, and the necessary actions can be taken. To prevent power flowing from the output to the BMS or the input, MOSFET is used that acts like a diode for efficiency. At the input of the BMS connector, a TVS diode is implemented to protect the system against ESD. The LDO that is connected directly on the power bus is necessary for sensors and the MCU. As long as there is a power flow on the power bus, the MCU and the necessary sensors are always enabled. This is important for communication to the main controller of the DeciZebro and for safety during charging. An EMI filter is implemented at the input of this LDO, to protect the LDO against the ripple current generated by the switching of the Ćuk converter at the input. Also to protect the power bus against noise that gets picked up by the ground of the LDO.

7.3. OUTPUT

The final output schematic can be found in appendix D.

The first thing to notice, is the implementation of the EMI filters on the input of each converter. This is done because each switching converter has its own switching frequency. This prevents the switching from the buck-boost to affect the input of the buck-converter.

Another thing to note, is that each power line has a + and a -. Since the DeciZebro is a walking robot with no real connection to ground, all power lines must have a current return path. All the ground connections in the schematic, are known as the signal ground. This ground is implemented on a PCB by using a ground plane. The ground plane is basically an entire plane filled with a lot of copper. This plane provides a very low impedance path and thus approximates a "real" ground. More on the design of a copper plate, will be discussed in chapter 8. Each return path from the voltage busses, are connected to an EMI filter to reduce noise.

As discussed in chapter 5, each converter has an enable pin necessary for the safety & control group. In case of any power faults, the converters can be disabled until the power fault is cleared, and then re-enabled. Since the buck-converter isn't directly connected any output bus, it doesn't require an enable pin that is controllable and thus is externally pulled high. While the LM5176 does include integrated current limiting for short-circuit/over-current protection, it was chosen to disable this feature. The reason being, that the MCU

can't determine whether there is a power fault when the buck-boost itself limits the current. This could result in the motors suddenly stopping or getting less power without the [MCU](#) ever detecting this. In order to still protect the 16V unregulated bus against current faults, an external current sensor is implemented by the safety & control group. This allows the [MCU](#) to always know what current is being drawn from the bus and whether or not to disable the LM5176. For extra safety, in case the [MCU](#) doesn't function properly, a 5A fuse is implemented. The same holds for the 5V and 3.3V regulated busses using a 1A fuse. They all have an external safety circuit for power monitoring and safety. The 16V bus is split into two connectors. This allows the use of one side per connector. Also, to see whether a bus is properly working, LEDs are implemented at the output in order to clearly see the status of that bus.

8

PRINTED CIRCUIT BOARD DESIGN

8.1. DESIGN RULES

When designing a PCB one should confirm to some rules to have them produced. These rules differ from manufacturer to manufacturer, and are dependent on thickness of the copper. The lower the clearance between tracks the higher the price will become. The same holds true for smaller drill sizes. This means one should not make these too small. This is why a clearance of minimum 0.2mm and a drill size of minimum 0.3mm are used for the BMS. However, since the PMS PCB is a lot more dense, the minimum clearance used is 0.125mm and a minimum drill size of 0.25mm. Using eurocircuits¹ as a reference point, these settings shouldn't increase the price. The trace width is dependent on the current through the trace and the temperature rise allowed. This can be calculated using equation 8.1 (IPC 2221).

$$I = K * \Delta T^{0.44} * (W * H)^{0.725} \quad (8.1)$$

Where I = the maximum current allowed in amperes, ΔT is the maximum temperature rise in celsius, K = 0.024 (internal traces) or 0.048 (external traces), W = width in mils, H = thickness in mils.

Using a maximum temperature rise of 85 degrees, on a 18 μm external copper layer, the minimum track widths are given in table 8.1 at different currents. The same is given in table 8.2 for an internal copper layer of 35 μm .

Table 8.1: Minimum track width at different current on a 18 μm copper foil (external layer)

Current (A)	Trace width (mm)
1A	0.16
2A	0.42
3A	0.73
4A	1.27
5A	1.47
7A	2.33

Table 8.2: Minimum track width at different currents on a 35 μm copper foil (internal layer)

Current (A)	Track width (mm)
1A	0.22
2A	0.56
3A	0.97
4A	1.44
5A	1.96
7A	3.12

The clearance of 0.2mm is enough for voltages up to 30V (IPC 2221). This is sufficient for the PCBs designed.

8.2. MAIN PCB DESIGN

For the main PCB, an area of 133x41mm was reserved. This meant that a lot of components needed to fit in a relatively small space. For this reason, the whole system has been designed with space optimization in mind. The PCB is split into a data part and a power part. This is done to protect the data against noise generated by the power lines. This was done as much as possible, the final result can be seen in figure 8.1.

¹<https://www.eurocircuits.com/>

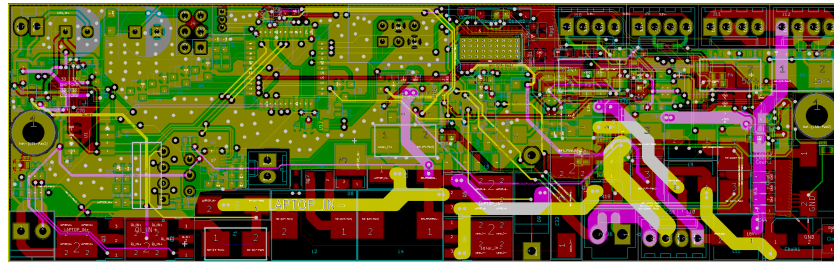
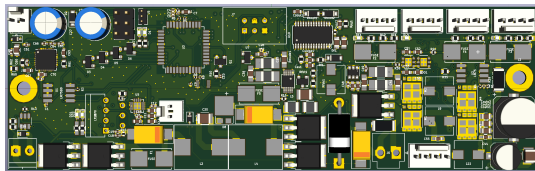


Figure 8.1: The layout of the PMS PCB

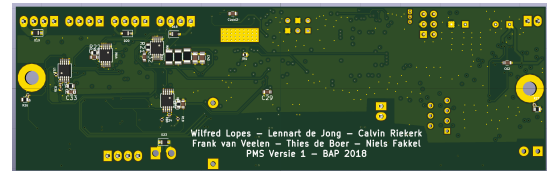
Using ground planes rather than ground traces reduces ground-loops and thus increases performance. These ground-loops can pick up EMI and induce a current in these loops. This could result in unwanted effects. The ground plane is placed on both the top and bottom layer, and stitched together with vias to support current flow. Generally, in order to further reduce EMI, power lines and their return path are recommended to overlap on adjacent layers. This cancels out any generated magnetic field the power line may have caused. However, in this case, the power lines flow through a lot of other components like inductors, capacitors and shunt resistors. This makes it difficult. Since each power line needs to be capable of conducting a peak of 5A, two vias are used when switching layers. Each via can approximately conduct 2.5A DC, so placing two will allow a current of 5A to flow without heating up the vias too much.

Special attention was placed on the placements of capacitors that act as filters and shunt resistors. In order to increase the performance and decrease the loop length, the capacitors are placed in close proximity of the IC that requires them. The same holds for shunt resistors. Since the IC measures an analog signal, placing the shunt resistor far away could induce a lot of noise. Thus, making the measurement inaccurate. For this reason, they are placed very close to the IC. All connectors are placed in logical places. The output connectors are all placed at the edge of the PCB which faces the inputs inside the DeciZebro. The on/off switch connector is placed at the same side as the switch itself. The same holds for the laptop connector. Since the PV cell connectors come from above the PMS, this connector can be practically anywhere on the PCB, thus it is placed close to components which accept solar input. The same holds true for the coil connector, however this comes from below the PCB.

A render of the final PCB design can be seen in the figures below.



(a) The front side of the PMS PCB



(b) The back side of the PMS PCB

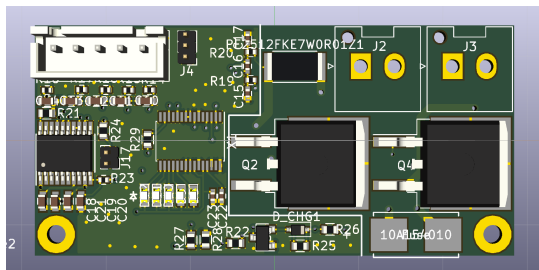
Figure 8.2: A render of the PMS PCB

The final design uses a total of four layers to decrease the cost per PCB even further. From these renders, it can clearly be seen that the larger components, which are used for the power lines, are mostly grouped together at the bottom right side of the PCB. The top left side is occupied by data lines and the MCU. To save some space on the front side of the PCB, components are also placed on the back side. The components placed on this side, should all be very thin. This avoids making the PCB very bulky which could cause the PCB to not fit in the allocated space inside of the Zebro. The last thing to notice are the two mounting holes used to mount the PMS PCB to the Zebro itself. These holes are 3.5mm in diameter and coupled to an LC-filter to remove transients picked up from the Zebro itself.

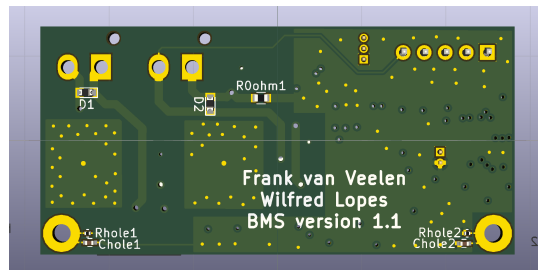
8.3. BMS PCB DESIGN

It was chosen to have the BMS on a separate PCB, both to save space on the main PCB and to make the design more modular, something that is important to the Zebro team. The PCB will be placed on the same level as the batteries, below the main PCB. The size available for the BMS PCB is then 56.3mm*27mm. A 3D view of the final PCB is given in figure 8.3. An overview of the layout is given in figure 8.4.

As can be seen it was chosen to keep the power part separated from the data part on the PCB. This was done to minimise the effect of the MOSFET switching noise on the data. The power +/- lines were placed on top of each other as much as possible. This was also done to reduce the effects of noise, since the DM noise will cancel out for a big part. For the sensing resistor a differential pair was used, with via stitching as shielding on both sides to prevent noise. The mounting holes are connected to the ground plane with a filter on the back side of the PCB. The TVS diodes are also placed on the back side. A ground plane was used on the front and back copper layer to shield the data signals. These ground planes are stitched together with vias. The MOSFETs have a thermal relief plane on the back copper and the front copper, stitched together with vias.



(a) The front side of the BMS PCB



(b) The back side of the BMS PCB

Figure 8.3: A render of the [BMS PCB](#)

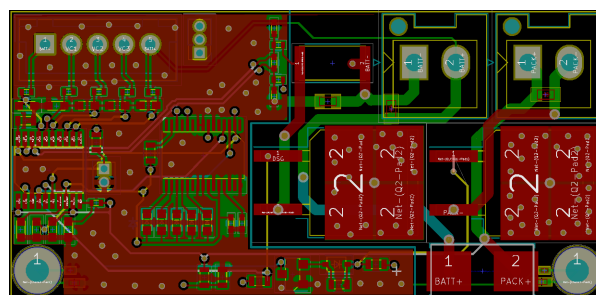


Figure 8.4: The layout of the **BMS PCB**

9

COST ANALYSIS

In this chapter the total cost of the system will be discussed, first for a single prototype, after which the cost of the system for semi-mass production (a series of 150) will be discussed.

9.1. PROTOTYPE

In table 9.1 the price of the system is specified per part. The total price for a single prototype is €283.3. As can be seen a large part of this is the PCB price. The components are about half of the total amount.

9.2. SEMI-MASS PRODUCTION

In table 9.2 the price of the system is specified per part. The total price of a series of 150 is estimated to be €17435.18. This comes down to €116.23 per robot. The components price is an estimate based on average discount for a series of 150. The PCB priced is based on an invoice from PBCway.¹ The batteries, coil and solar panel prices are actual prices for a series of 150.

Table 9.1: The price of the system-parts for a single prototype

Part	Amount	Cost [€]
Batteries	8	38.40
Main PCB	1	31
BMS PCB	1	42
Components main PCB	1	134.47
Components BMS PCB	1	24.84
Coil	1	9.59
Solar Panel	1	3

Table 9.2: The price of the system-parts for a series of 150

Part	Amount	Cost [€]
Batteries	1200	3,720
Main PCB	150	230.60
BMS PCB	150	241.83
Components main PCB	150	10,085.25
Components BMS PCB	150	1,863
Coil	150	919.5
Solar Panel	150	375

¹<https://www.pcbway.com/>

10

SYSTEM TEST

10.1. TESTPLAN

10.1.1. OUTPUT CONVERSION

The tests performed for the output conversion are aimed to test the safety features, efficiency and if the conversion is performed correctly at different loads. The requirements are found in section 2.3.

The equipment required for these test are listed below.

- The main PCB
- A thermometer (preferably an infrared heat camera)
- A DC power supply capable of providing 16.8V-8A
- A multi-meter
- A 3.3 Ω power resistor
- A 4 Ω power resistor
- A 5 Ω power resistor
- A 6 Ω power resistor
- A 7 Ω power resistor
- An oscilloscope

LOAD TEST

To determine if the voltage conversion is performed correctly, different loads are attached to the output in order to see if the output voltage remains stable. First, a DC power supply is attached at the input of the BMS connector to act as the power bus. A 4 Ω power resistor is attached at the unregulated 16V power supply. The multi-meter is used to determine the current through the power resistor. An oscilloscope is used to determine the output voltage waveform. If the current through the power resistor doesn't exceed 5 ampere and the voltage waveform remains stable (around 16V), the 16V bus has passed the test. This test is performed with different loads of 5, 6 and 7 Ω

The test for the 5V and 3.3V busses are comparable. However, as load, 5 and 3.3 Ω power resistors are used respectively. If the current through the power resistor doesn't exceed 1 ampere, and the voltage waveform remains 5V and 3.3V respectively, the power busses passed the test.

EFFICIENCY

To determine the efficiency of the power busses, the power output across the resistor is calculated together with the input power. This is calculated by the equation: $P_{out} = I^2 R$ at the output and $P_{in} = V \cdot I$ at the input. This input power is determined from the DC power supply. To calculate the efficiency, equation $\eta = \frac{P_{out}}{P_{in}}$ can be used.

SAFETY & CONTROL

The output converters can be enabled or disabled by control signals. Since to decide whether or not the converter must be enabled or disabled is decided by the [MCU](#) and the safety and control itself is implemented by the control group, this test is not in the scope of our thesis.

10.1.2. BMS

The tests conducted for this subsystem should at least make sure whether the requirements (section [2.2](#)) are met. Since lithium batteries can be dangerous when not handled correctly and this test is done to confirm the correct handling, some safety measures should be taken. A bucket of sand should be present to throw the batteries in, in case the batteries start heating up. For the same reason someone should be present during all tests.

For all requirements a test is conducted, while some are combined into one test to save time. These tests will be described in this section. Some equipment is necessary to conduct these tests:

- The [BMS PCB](#)
- The battery pack including cables with connectors
- A thermometer (preferably an infrared heat camera)
- A DC power supply capable of providing 20V-5A
- A bucket of sand
- A multi-meter
- A laptop with the bqStudio software
- A TI EV2300 module with cables
- A 6 Ω power resistor
- A 2 Ω power resistor

SHOCK TEST

For this prototype the battery pack could not be assembled in a way that would be used to semi-mass produce a battery pack. This is why it is chosen to not test the shock resistance of the prototype pack, as the result is not relevant for the final product. Requirement [3a](#) will not be tested for this prototype.

DISCHARGING TEST

Since the batteries are partly filled by the manufacturer the first test will be a discharge test. During this test the temperature will be monitored to confirm requirement [2c](#). The temperature shall be noted every 30 seconds. The discharging will be done by connecting the pack (PACK+/-) to a power resistor so that a current of maximum 3A is pulled from the pack. This means a resistor of 6 Ω should be used. The power resistor should be able to handle 3A continuous. The discharging is continued until the fuel gauge detects an undervoltage. This will confirm requirement [1c](#). For safety reasons the voltage of the cells should be monitored and the load disconnected if the undervoltage protection does not work.

After this test the [SoC](#) estimation should be 0%. This will be confirmed using the TI EV2300 module connected to the SMBus.

CHARGING TEST

After the pack has been fully drained a charging test shall be conducted. This shall be done using a DC power supply connected to the pack (PACK+/-). The DC power supply should be able to supply up to 5A at 20V. The voltage should be higher than the maximum voltage of the pack to make sure the overcharge protection works. The current provided to the pack shall be monitored to determine whether the charging profile is followed. The temperature of the pack will again be monitored and noted every 30 seconds. The voltage of the cells should also be monitored to make sure none overcharge. These results can also be used to see whether the cell balancing works.

When the cells reach 4.2V the charging current should drop while the voltage remains 16.8V, until there is no charging current. It should be monitored whether this works correctly. If this works correctly requirement 1a and 1b are met.

After this test the SoC estimation should be 100%. This will be confirmed using the TI EV2300 module connected to the SMBus.

OVERCURRENT/SHORT CIRCUIT TEST

With these charged cells the over-current and short circuit protection can be tested. First the pack (PACK+/-) is connected to a power resistor so that the current provided by the pack is 8A. The fuse¹ will not blow, while the electronic over-current protection should activate. The resistor value should be 2 Ω. The current through the resistor should be measured to determine if the protection has activated.

STATE OF CHARGE ESTIMATION TEST

The SoC estimation has at this point already been tested for 0% and 100%. Testing for other values is difficult since the actual SoC is not known. For this a battery tester could be used. These are however expensive and were not available. The SoC estimation accuracy can be further tested if an accurate reading of the SoC can be obtained.

10.2. RESULTS

Sadly, due to time constraints and some internal financing issues, the PCBs could not be ordered in time for this thesis. For this reason no tests could be performed. This will be done before the defense and results will be delivered before then.

¹See appendix C

11

CONCLUSION

Since no tests could be done in time for this thesis the conclusion will be based on theoretical specifications. The conclusion based on the tests will be added when the tests are done. To see which specifications (relevant to this thesis) were fulfilled, a look is needed at the requirements given in section 2.1. A brief summary is given below.

- **"The entire system has to fit within the specified dimensions of the robot, according to Appendix A"**
For this reason, throughout the design of the PMS and BMS, space has always been factored in the choices taken. This was mainly done with choosing smaller inductor or capacitor values and by choosing ICs which have small footprints. Also, at the output, it was chosen to use only one buck-converter, rather than two, to save space. Even if using two buck-converters would result in a higher output efficiency, this was deemed not great enough to sacrifice the available space on the PCB. One of the reasons to implement the BMS on a separate PCB, was to save additional space on the main PMS PCB. Looking back at chapter 8, it can be seen that both the BMS and PMS fit on a 56.3x27mm and 133x41mm space respectively.
- **"Utilise a damage protection system to avoid damage to any part of Zebro"**
In this case, the IC's used for the BMS needed to adhere to the specifications discussed in section 2.2. The battery system theoretically meets all requirements, except for requirement 3a. The overheating of the battery packing during charging/discharging should not happen as not a lot of heat is generated because of the high efficiency charging profile. The electrical requirements are all met by using the bq76920/bq78350-r1 combination. The heat protection is done using a thermistor supported by this combination. If for some reason the ICs don't function as expected, the BMS also contains a fuse rated for 10A. For the PMS, the chosen ICs all automatically disable when the temperature gets too high. Also, each output converter has an enable pin that the safety & and control group can freely manipulate. If for some reason the MCU can't resolve the power fault, each output has a fuse rated for the maximum current allowed on that bus. Also, to avoid ESD at the connectors of the PMS, TVS diodes were added in parallel to these connectors. Thus all specifications discussed in section 2.3 are fulfilled.
- **"The power supply should be able to deliver 16V - 1A continuously, with a peak of 5A, fused without voltage regulation"**
This was implemented by using a high efficiency four-switch buck-boost LM5176 set at 16V. This IC is rated for 5A, and to ensure that it doesn't go over the maximum allowable current, a fuse is added for protection.
- **"The power supply should be able to deliver 5V - 1A and 3.3V - 1A, both fused with voltage regulation"**
This was implemented by using a buck-converter to reduce the power bus voltage, to a more workable 6.5V. The output of the buck-converter is then connected to the input of a 5V LDO and a 3.3V LDO, which regulates the voltage to 5V and 3.3V respectively. The buck-converter is rated for 2A+, and the LDOs are rated for 1A each. To further ensure that current lies below the maximum allowable peak, fuses are added for protection.

- **"There should be an over-current protection module"** This was mainly implemented by the safety & control group. The output converters can be turned off when an over-current occurs. Fuses were also added.
- **"The total system price should be below €100 for a series of 150"** This was not reached. The total system price is €116.23 for a series of 150. This means there should be costs saved. This will be further discussed in section [12](#)

12

DISCUSSION & RECOMMENDATIONS

Some things during this project could have gone better, as always. These will be discussed in this chapter.

The most obvious improvement point is time management and communication. The PCB design was done just in time to be able to test it for this thesis. However due to communication with the finance department of the TUDelft through the secretary the PCBs could not be delivered in time. This meant no testing could be done, so that no results are available. There are multiple solutions to prevent this. One could order the PCBs more directly, so that communication is easier. One could also make sure the PCBs designs are done even earlier. This was however hard, since the time available for the project was short.

To save space, smaller inductors and capacitors could be used at the EMI. Unfortunately, due to a calculation mistake, this was discovered when the PCB was already ordered. This shouldn't matter for the performance, but it would make the PCB layout a bit more simple. However, saving space by using smaller components isn't always necessary and always a good solution. For both the PMS and the BMS PCB, 0201 Surface-Mounted Device (SMD) components were used. They are great for saving space, however they are not so great for mass production. These miniature components require special state-of-the-art pick-and-place machines in order to accurately place them on the solder pad. Even if such a machine was available, the accuracy is still limited to the quality of the component, delivery quality and how they are supplied to the feeder. [32] For this reason it is recommended to use bigger components like a 0402 package or bigger.

During the design of the PMS PCB, in an attempt to keep the price per PCB as low as possible, only 4 layers were used. This made routing very tedious. While using 6 layers would be slightly more expensive, it provides more layers to separate the 3.3V plane and the data lines, thus reducing noise in the data lines. This would also allow the ground planes to be slightly more filled, resulting in better isolation for the data lines. Also, more care needs to be taken when determining the trace width of signals. The current PMS PCB uses a trace width which is too thin for the rated current in an internal layer. This trace is situated at the LM5176 on the LDRV1/LDRV2/HDRV1/HDRV2 pins. These pins are used to provide current to the gates of the MOSFETs. However, after the PCB manufacturing, it was noticed that these pins can supply a maximum of 1.8A. Thus requiring a trace width of 0.55mm according to table 8.2. Another minor problem, is that at the bottom of the MOSFETs on the LM5176, the voltage is floating as seen in figure 5.6. The effect of this remains unknown, since during the time of writing this thesis, the no testing has been performed for reasons already explained.

The power supply for the MCU is connected to the power bus. However, in a worst case scenario, the MCU might decide to disable the discharge of the BMS system. This will result in the entire PMS not receiving any power. Thus the MCU can't re-enable the discharge of the BMS system, which results in the system remaining in an off-state. This can be solved by powering the MCU and necessary sensors directly from the battery. Doing so, will ensure that the MCU will always be enabled when the battery has enough charge. For added safety a fuse is recommended to be placed in this direct voltage line in case of a short-circuit.

A big improvement that could be made on this system is the mechanical strength of the battery pack. One could either 3D print a battery holder or use a spot welder and nickel strips to connect the batteries.

If more standardized Li-ion battery sizes are available one could use these to gain capacity. The 18650 size, while widely available, does not fit in the case very well, which results in a loss of space. The 25500 size fits better, however at the time of this project it was not available from trustworthy manufacturers. When this is done one should also reconsider the amount of cells in series, as 5 cells in series would be more optimal in combination with the laptop adapter.

Another option to solve these issues is to order a custom made battery pack. These are rather expensive, but could become cheap when ordering for semi-mass production. A cost-benefit analysis should be made after requesting an invoice.

The costs of the total system should be lowered approximately €16. This could be fixed by using 4 batteries instead of 8. This is however not desirable since capacity is lost. It could also be chosen to remove the buck-converter to 6.5V at the output. This would mean the transfer efficiency to the 5V and 3.3V bus is lowered, however the total system would be cheaper.

A

ASSIGNMENT

Development of an on-board power system for the DeciZebro

Bachelor Final Project

1. Introduction

The Zebro team develops six legged autonomous robots that are specifically aimed at demonstrating swarm behavior. Swarm robotics aims to replicate the way animals cooperate into robotics. This requires robots to be autonomous and make decisions without interference from a central computer, a leader robot or a human. This decentralized behavior can lead to swarming behavior using simple rules. The Zebro team hopes to demonstrate this behavior using 8 robots during the second semester of the academic year 2017/2018.

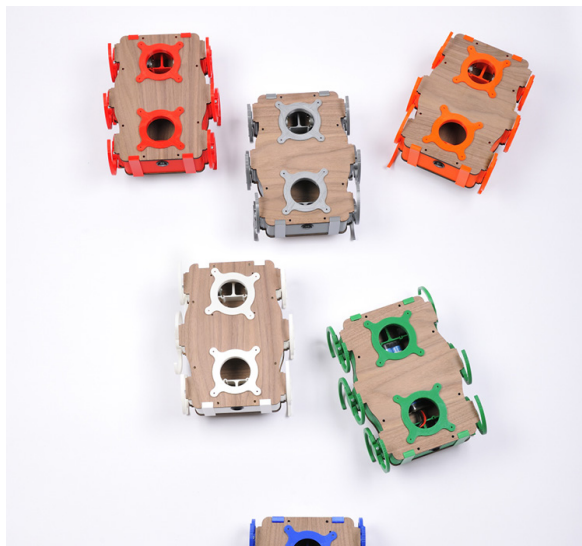
The next step is to upscale. In simulations it is already possible to operate an autonomous swarm of 100 robots. However, feeding the swarm is still a challenge. The swarm consumes electricity, and is dependent on it for its survival. Current DeciZebro's weigh around 1.7 kilograms and draw 1A of power continuously when walking. Given the current battery capacity, this limits the robot to about 2,5 hours of operation.

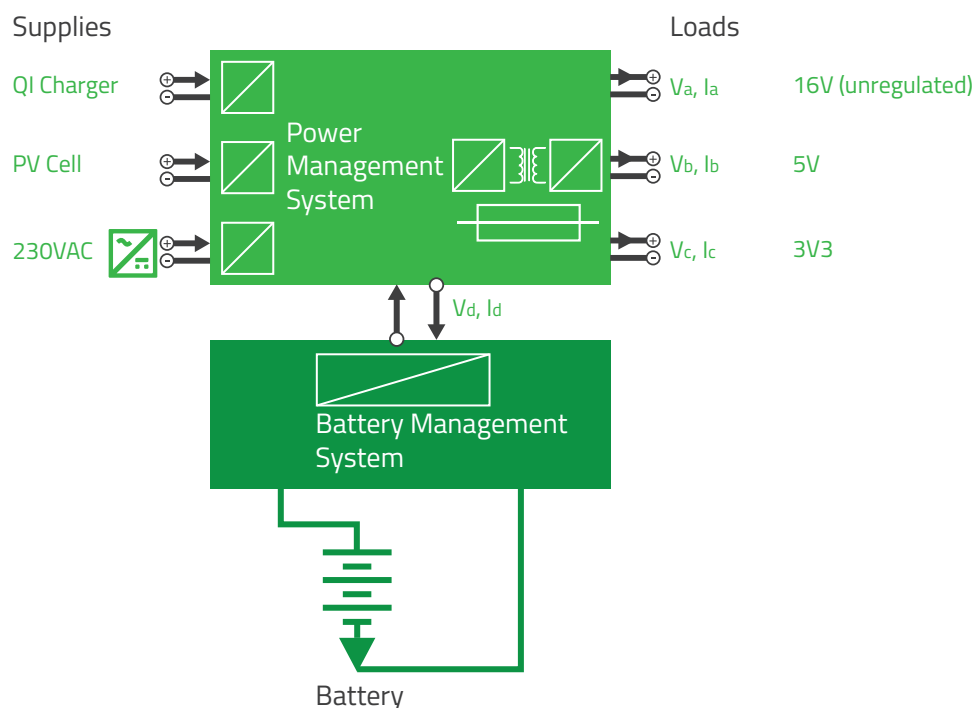
2. Assignment outline

The DeciZebro is equipped with two module slots at the top of the robot. We hope to be able to use one of these slots to facilitate a solar charging module. The goal of this module would be to provide a continuous additional power supply that complements the power supply from the battery. This secondary power supply should be able to either charge the battery or directly supply part of the robots power consumption.

Apart from being charged by solar power, the batteries must also be chargeable by a Zebro charging station. For autonomous charging, the Zebro will hover directly above an inductive charger. A power receiving coil should be incorporated in the Zebro's bottom plate. Furthermore, the battery management PCB, governing the power inflow from charging and outflow to modules should be developed.

In short, the Zebro team is looking for an integrated power system solution for the DeciZebro. This includes the design of an on board, solar based, power generation module, on-board inductive charging capability and the necessary power and battery management system PCB. The main challenge lies in the design of this PCB in such a way that it can facilitate the three different methods of charging, as well as handling different load scenarios. (see figure on the next page)





3. Criteria

The main and most complex component within this BAP assignment is the design of the power management system, which will be discussed first. Added to the development of this system, a battery management system needs to be developed. Furthermore, the system must be demonstrated as a whole, including the different charging options and loads listed in the figure above.

Power Management

1. Battery charging

- 230VAC charging via a cable hook-up (Laptop charger interface)
- Via the QI inductive charging standard
- Via a photovoltaic cell to be mounted on the top of Zebro

2. Loads

- 16V line, unregulated, 1A continuous with 3A peak load, fused
- 5V, 1A, fused
- 3.3V, 1A, fused
- Ability to supply these loads with either battery, PV cell or both, depending on the power demand from the modules

3. Safety

- The Charger Module should implement an Autonomous Module Damage Protection System (AMDPS), be capable of determining short circuits and overvoltage, preventing the module from destroying itself.

Battery Management

- a. The battery module should be able to determine the combined state of charge of the batteries
- b. A choice of battery should be made. These should be NiMH or NiCD batteries, and be chosen in such a way as to provide the longest runtime for Zebro. For this, the available space in DeciZebro should be taken into account.
- c. The battery temperature should be measured. If a predetermined threshold value T_{max} is reached Zebro should shut down. A warning signal should be given at T_{high}

Further Criteria

- a. The PCB to be developed should fit within the allocated space in DeciZebro
- b. The total cost of the system, including batteries and PV cell, should be kept below €100,- including possible pick and place manufacturing at our electronics manufacturing partner EPR.
- c. The system elements (different types of supplies and loads) should be independently verified and a complete system demonstration should be given.

The system will be tested by equipping at least two Zebro's with an identical charging module and determining whether the module correctly charges either the batteries or delivers directly to the modules. Furthermore, charging via wire and wireless charging should be verified.

4. Requirements

Power Management

- | | |
|------|---|
| PM-1 | Support 230VAC charging via a laptop charging interface |
| PM-2 | Support inductive charging via the Qi charging standard, featuring receiving coils that are embedded at the bottom of Zebro |
| PM-3 | Support charging the batteries via a PV module at the top of Zebro |
| PM-4 | Support directly supplying Zebro modules via the PV cell as well as via the battery |
| PM-5 | Supply 16V at 1A continuous with 3A peak currents, fused |
| PM-6 | Supply 5V, fused |
| PM-7 | Supply 3.3V, fused |
| PM-8 | Utilize a damage protection system as described under 3.3 (Safety) to avoid damage to any part of Zebro |

Interface requirements

- | | |
|------|---|
| IF-1 | Feature a laptop charging interface |
| IF-2 | Feature a size specification and interface for Qi receiving coils |
| IF-3 | Feature a size specification and interface for placing the PV cells on the roof |
| IF-4 | Adhere to the provided module slot and size specification for the PCB |
| IF-5 | Adhere to the provided slot for the battery pack |

Thesis requirements

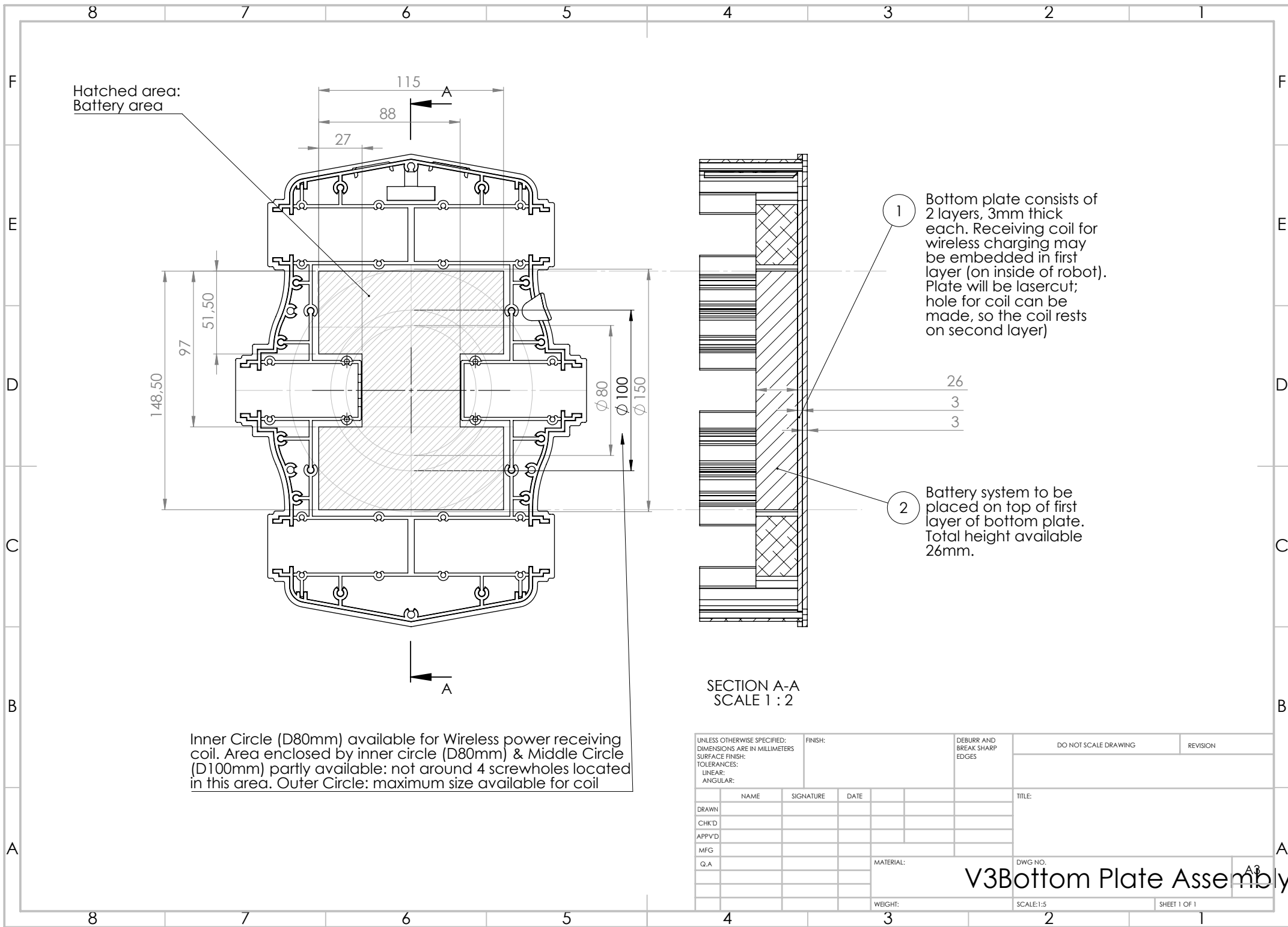
- | | |
|------|---|
| TR-1 | Develop the necessary architecture (software and hardware) to develop the Power and battery management system. A suggested split in architecture is between Controls, Power Electronics and Peripherals |
|------|---|

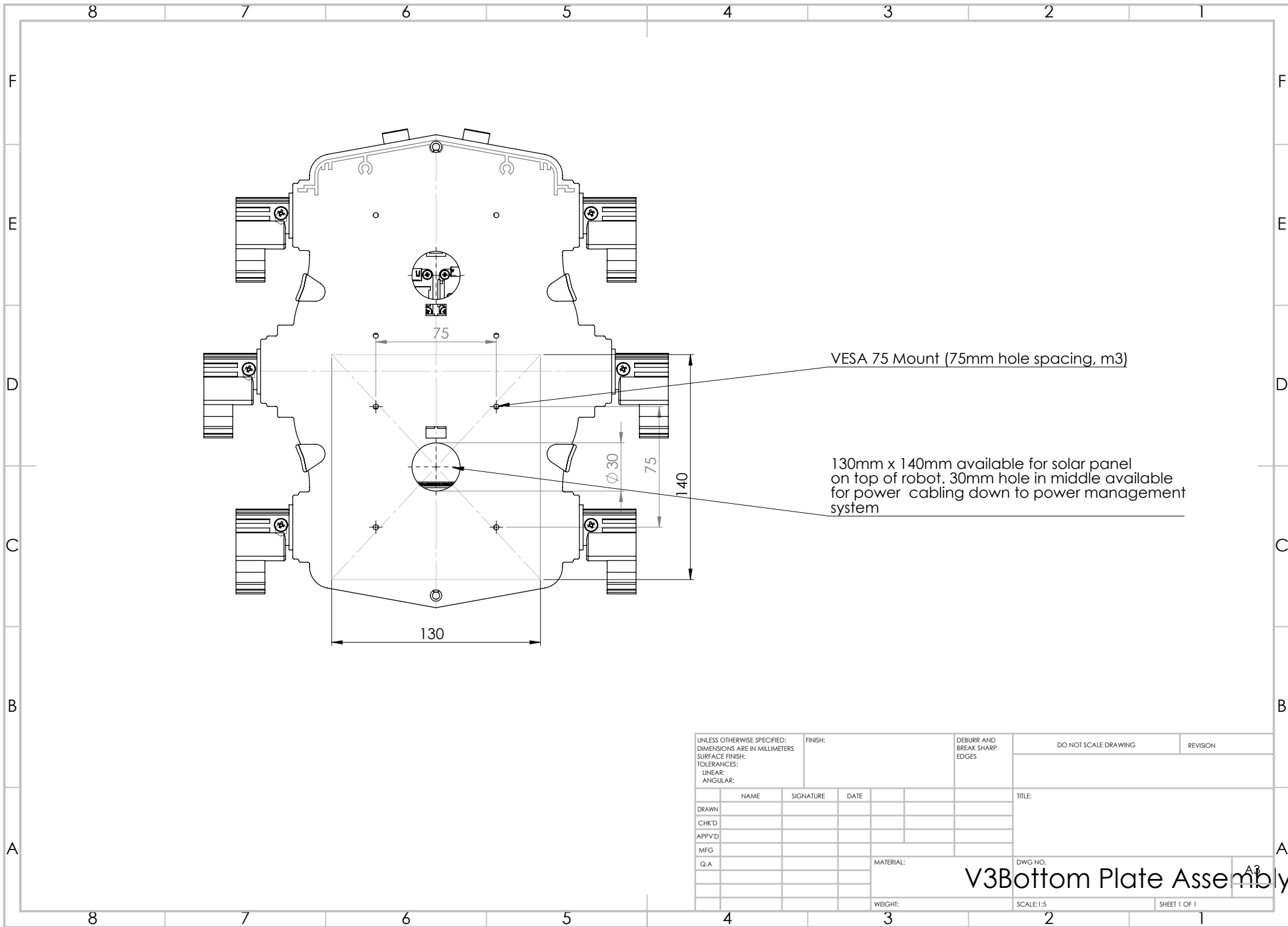
- TR-2 Develop a test bench to confirm power generated by the solar charging module is correctly handled by the battery management system, being either stored in the battery or consumed directly.
- TR-3 Demonstrate battery charging capability via 230VAC or inductive charging
- TR-4 Provide an advisory document for the design of a mass production power system to be implemented within large swarms of Zebro's in the future, based on experience obtained during this project. For use by team developing the next generation of Zebro's

B

SCHEMATICS DECIZEBRO

These are the schematics provided by the Zebro team.





VESA 75 Mount (75mm hole spacing, m3)

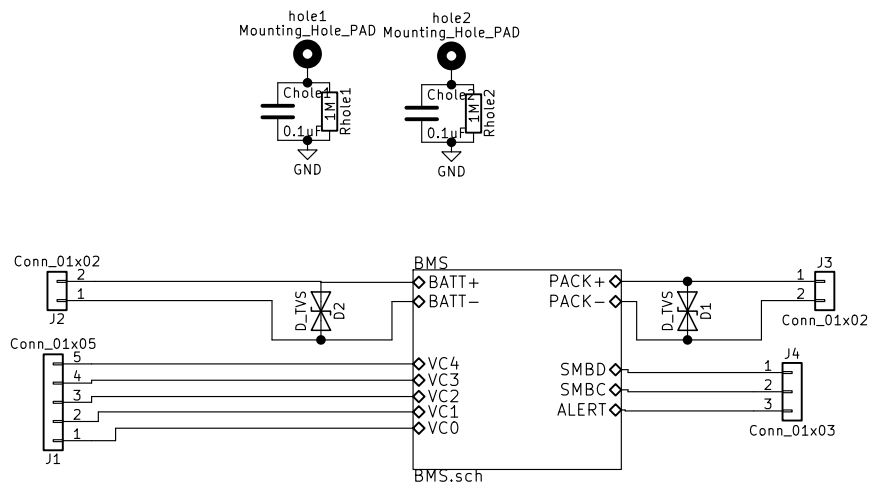
130mm x 140mm available for solar panel on top of robot. 30mm hole in middle available for power cabling down to power management system

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS SURFACE FINISH: TOLERANCES: LINEAR: ANGULAR:					FINISH:		DEBURR AND BREAK SHARP EDGES		DO NOT SCALE DRAWING			REVISION		
NAME		SIGNATURE		DATE						TITLE:				
DRAWN														
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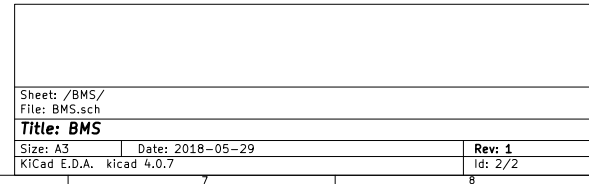
V3Bottom Plate Assembly

C

SCHEMATIC BMS

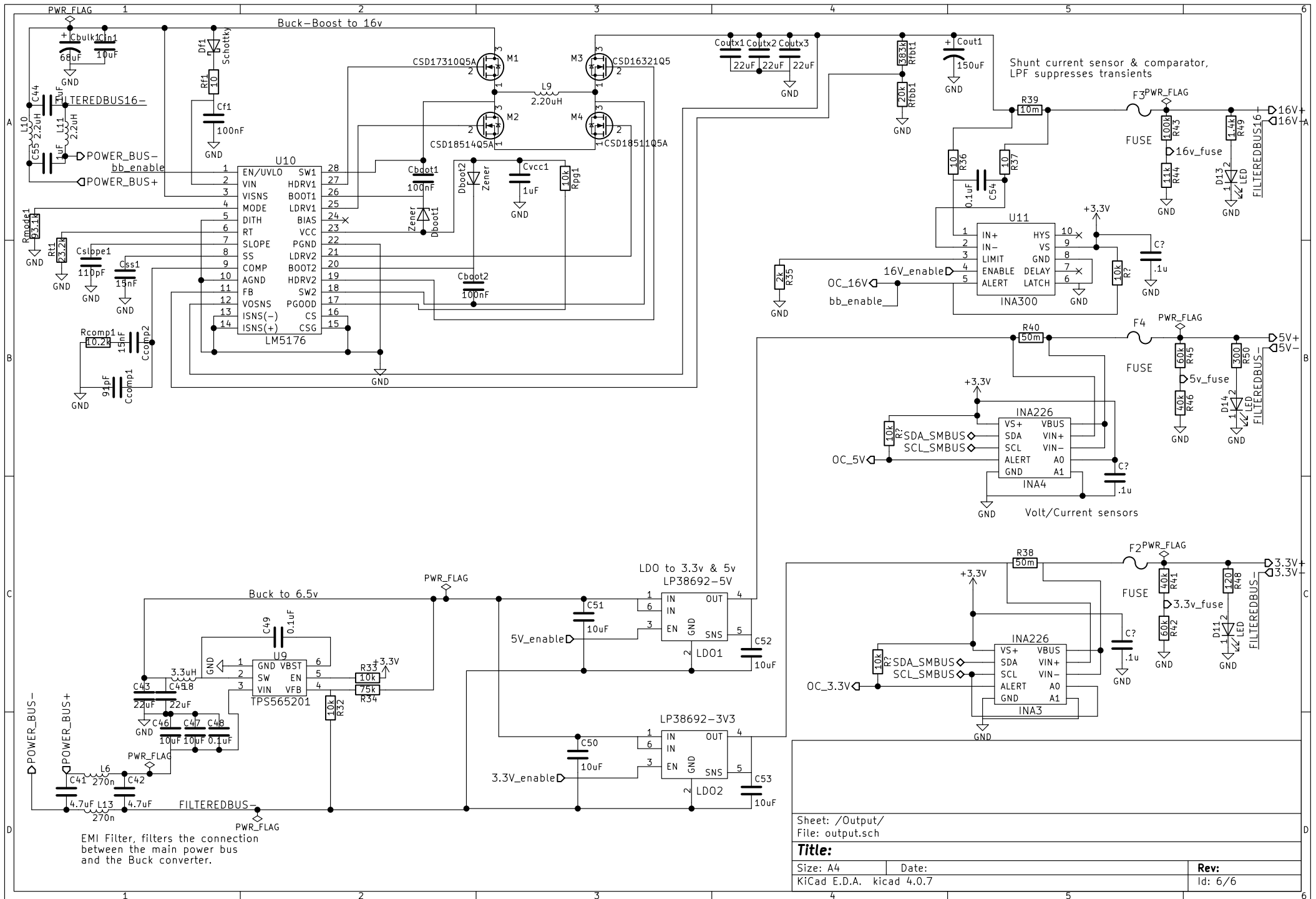


Includes overcurrent protection, overdischarge protection, underdischarge protection, SMBus communication, Balance charging, Temperature shut-down, SoC estimation, Battery health estimate, Voltage per cell, Current drawn etc. Reverse polarity will be solved by implementing a hardware based solution (fool-proof connectors).



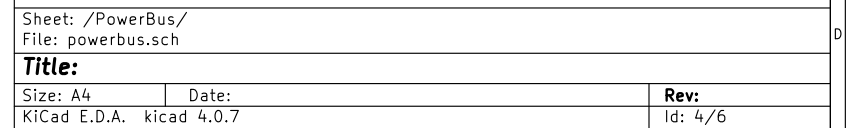
D

SCHEMATIC OUTPUT CONVERSION



E

SCHEMATIC POWERBUS



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