System in package (SiP) technology

Fundamentals, design and applications

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System in package (SiP) technology: fundamentals, design and applications

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Abstract

Purpose – The purpose of this paper is to demonstrate a novel 3D system-in-package (SiP) approach. This new packaging approach is based on stacked silicon submount technology. As demonstrators, a smart lighting module and a sensor systems were successfully developed by using the fabrication and assembly process described in this paper.

Design/methodology/approach – The stacked module consists of multiple layers of silicon submounts which can be designed and fabricated in parallel. The 3D stacking design offers higher silicon efficiency and miniaturized package form factor. This platform consists of silicon submount design and fabrication, module packaging, system assembling and testing and analyzing.

Findings – In this paper, a smart light emitting diode system and sensor system will be described based on stacked silicon submount and 3D SiP technology. The integrated smart lighting module meets the optical requirements of general lighting applications. The developed SiP design is also implemented into the miniaturization of particular matter sensors and gas sensor detection system.

Originality/value – SiP has great potential of integrating multiple components into a single compact package, which has potential implementation in intelligent applications.

Keywords Gas sensor system, LED module, PM sensor, System-in-package (SiP)

Paper type Research paper

1. Introduction

With the increasing demand for miniaturization of portable electronics, higher function integration level and lower cost are major challenges in the semiconductor industry. System-in-package (SiP) technology is one of the fastest emerging technologies offering highly flexible and low-cost integration and packaging solutions (Anna, 2008). An SiP may optionally contain passive devices, Micro-Electron-Mechanical system (MEMS), optical components and other packages and devices (Chen *et al.*, 2008). SiP possesses many advantages as an enabling technology of More than Moore (MtM). It provides smaller form factor compare with discrete individually packaged devices. More importantly, it reduces time-to-market through concurrent development of module and system, more design flexibility and easy redesign. Besides, SiP has the generic compatibility with heterogeneous integration of various die technology including Si, GaAs, SiGe, silicon on insulator and MEMS, providing great benefit for MtM system integration (Roozeboom *et al.*, 2005). 3D integration provides opportunity for miniaturization, high bandwidth, low power and high performance (Lau, 2011; Thomas *et al.*, 2011). Substrate play a significant role in the design of 3D SiP. Polymer laminates are widely used in consumer electronics because of the low cost. But the implementation of polymer-based substrates into 3D integration and SiP has been obstructed by the material drawbacks such as mismatched coefficient of thermal expansion, insufficient thermal dissipation and difficult manufacturing of high-density interconnection. From this perspective, silicon makes a well-suited candidate for packaging substrates. Moreover, silicon-based packaging process is inherently compatible with integrated circuits (IC)/MEMS processes, helping open new opportunities for 3D heterogeneous integration. The silicon-based 3D integration, represented by

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silicon interposer technology, has been intensively researched recently (Limansyah *et al.*, 2009; Zoschke *et al.*, 2011). Most of the technologies have been developed for 3D IC integration, accommodating high-density through-silicon vias (TSVs). The attempt of implementing TSV technology into semiconductor industry is been carried out for many years. However, because of many critical issues of this technology, its introduction into high volume manufacture has been hindered (Gambino *et al.*, 2015). As more functionalities are integrated into one single package, the miniaturization of packaging becomes challenging. Wafer level packaging (WLP) has become a promising solution for highly integrated packaging (Lau *et al.*, 2010). Fan-in WLP can shrink package size and height, simplify the supply chain and provide a lower overall cost (Fan, 2010). Fan-out WLP allows higher ball count by extending the packaging size beyond the area of the chip. One of the well-known examples of a fan-out WLP is embedded wafer level ball grid array (eWLB) technology, which can reduce manufacturing costs, uses a combination of front- and back-end manufacturing techniques with parallel processing. eWLB technology also offers procurement flexibility, lower cost of ownership, better total system and solution costs and faster time to mass production, which is suitable for IC and low power devices integration based on the thermal management (Yonggang *et al.*, 2010). Unlike IC integration, most MEMS systems and sensor applications do not require high density of interconnections, meaning more dedicated and cost-effective solution needs to be developed.

In this paper, a novel 3D SiP design platform has been developed using the stacked silicon submount (3S) technology. The design platform aims to provide a flexible and cost-effective solution of 3D heterogeneous integration for applications such as MEMS applications and smart sensor systems. The function of silicon has been expanded from interposer to packaging submount to make possible high integration density. Low-density TSVs were adopted to assure the cost-effectiveness and the suitability for applications such as MEMS and sensors. Moreover, the presented approach aims to realize miniaturized and fully functional SiP instead of modules or devices. By using the 3S technology, highly compact modules with system function are aimed to be achieved at reasonable cost. A smart lighting system (Dong *et al.*, 2013, 2015) and particulate matter (PM) sensor system (Dong *et al.*, 2017, 2016) were chosen as development demo in this paper.

One of the research approach used in this paper is the combination of development of common design rules and the demonstration of specific applications. The design rules deal with shared elements or aspects in the development of individual applications and provide a technology platform for related applications. More considerations need to be taken into account when it comes to certain application based on the common platform. Multi-physical design will be intensely addressed in this paper, as it is the most challenging part in such system design, whereas the most valuable novelty of this research to the whole community.

2. Fundamental design and fabrication processes

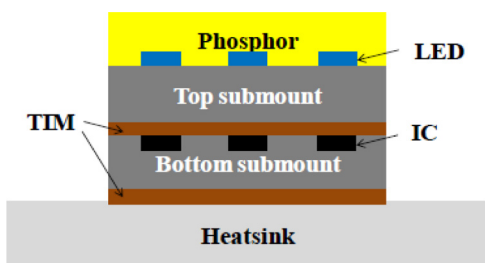
The presented SiP concept was developed for applications such as MEMS devices and sensor systems. The design will be presented in detail using a selected demonstrator, but inherently, it is applicable to a wider range of applications. Figure 1 shows the structure of the proposed module with 3Ss, which is used in smart lighting application. The top submount carries all the light emitting diodes (LEDs) which are encapsulated with a layer of phosphor. The driver circuit components are embedded on the bottom submount. The two submounts are glued with thermal interface material (TIM), and the whole stack is adhered to a heat sink by the same TIM.

The 3S process mainly consists of two parts, namely, the fabrication of submount and module assembly. The fabrication process can be basically fulfilled by standard silicon microfabrication process. Among all, some processes are intensively used for applications like solid-state lighting (SSL) where multiple heterogeneous chips are integrated based on silicon submount. The next section will explain some representative processes in SiP technology.

2.1 Metallization in cavity

As packaging substrates, silicon submounts act as carriers of all the circuitry components, including bare die ICs, discreet passive devices and even small outline packages. To make the best of real estate of the submount surface and increase the packaging density, sometimes part of the components are placed into indented cavities beneath the submount surface. One way to make cavities out of silicon is to use wet etch process. Silicon wafer with an orientation of <100> can be anisotropically etched by KOH solution, forming cavities with angled sidewalls. One of the challenge of the implementation of wet-etched cavity is the metallization patterning inside the cavities. Most of the cavities that are used to embed chips have a depth of over 100 μm, which makes it difficult to pattern materials using normal photolithography. To overcome such difficulty, photoresist must be coated on the wafer by spray coating rather than spin coating. Due to the topology of the etched surface, normal spin coating results in insufficient coverage of photoresist inside the cavities. For deep cavities, multi-step spray coating might be needed to achieve sufficient thickness of photoresist. Normal photolithography can be used for patterning the photoresist with prolonged exposure time. One thing that needs to be taken into account is that the minimum trace width or spacing should be at least comparable with the cavity depth, if not bigger. Otherwise, lithography techniques may not be adequate to achieve patterning with good quality. In other technologies, 3D printing can be used to fulfill the metallization inside the cavities, and with the development of metallization-on-polymer technology, polymer-based packaging substrate can be formed by molding (Kim *et al.*, 2006), which will reduce the cost of fabrication again.

Figure 1 Schematic of designed SiP module using 3S technology



2.2 Through-silicon via process

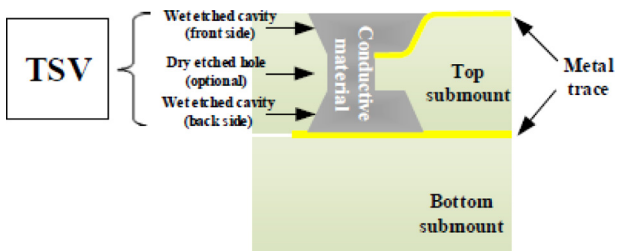
The vertical electrical interconnection from the top to the bottom submount was achieved by TSVs filled by conductive silver glue, while the two layers were bonded using thermal grease. The interconnections between the two layers also play as input/outputs (I/Os) to external circuitry. The proposed vertical interconnections are realized by a two-step process: etching based via forming and the filling of conductive material, as shown in Figure 2. To minimize the cost of process, the silicon etching part can be mostly or fully realized by wet etching process which presents high controllability, uniformity and low cost. Dry etching process may also be supplemented only if necessary. The filling of conductive material in the vias avoids thermal plating process in standard TSV process, which gives most of the issues on cost reduction as well as reliability.

2.3 Embedded passive device

Passive devices, including resistors, capacitors and diodes, consist more than 50 per cent of the real estate on polymer-based laminates (PCB) for most application circuits. Most of the passive devices used in consumer electronics are surface mount type, enabling the integration of them into a compact SiP. The state-of-the-art of embedded passive technology includes embedded device into packaging substrates or PCBs, either in rigid or flexible ones. Compared with discrete passives, embedded or integrated passive devices show increased electrical performance and reliability, reduced size and cost.

In our proposed approach, the integration of passive devices is realized through assembly-based process. After the silicon submount is prepared, the cavity for hosting the passive devices is finished with metal electrodes. Conductive material needs to be dispensed on the electrodes. At least two kinds of materials can be selected, solder paste and conductive adhesives. For solderable electrodes, such as copper, nickel or gold, solder paste is the best interconnection material. Reflow process can be used to melt the solder and then cool down to form solid solder joints. However, aluminum, which is widely used for traces and electrodes, requires special solder paste to realize the soldering process simply because aluminum is easily oxidized. Also, to form reliable intermetallic compound between aluminum and solder metal, higher soldering temperature is required, which for some applications, is unfavorable. Conductive adhesives can be an alternative of solder. Silver-based conductive glue has been widely used to form electrical interconnections between IC bare dies and electrodes. These glues contain polymeric solvents which require a curing process at certain temperature. Figure 3 shows schematics of typical passive devices embedded into silicon submount.

Figure 2 Cross-sectional schematic of modified TSV: etching-based via forming and filling of conductive material



3. Applications and discussion

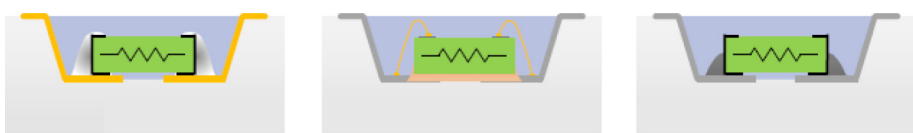
Focusing on the applications such as smart lighting module and sensor systems, a dedicated 3D wafer level SiP design is developed and presented in this section. The design, fabrication and packaging of the SiP according to the application are presented.

3.1 Smart lighting module

Designed for smart luminaires, the presented module consists of a LED light source, integrated drivers and a control circuitry. The light source contains two independent chains, each of which emits warm white (3,000 K) and cold white (6,500 K) light. The brightness of each chain can be adjusted with an infrared-based remote controller synchronously or independently, so that the whole module can provide light with variable color temperatures and different brightness. The controlling can be carried out by an infrared controller or any other devices with an infrared module, such as smart phones and personal digital assistants. As the integrated module possesses small form factor, its application includes, but is not limited to, bulbs, downlights and ceiling lights, at different locations including apartments, offices and workshops.

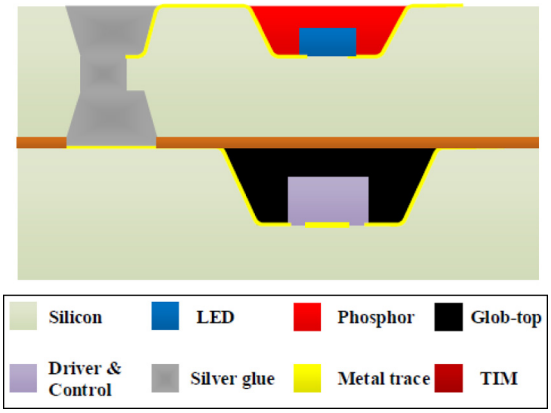
To improve the light extraction and minimize the size of the module, a 3D SiP was designed using the 3S technology. In brief, the module is a double-layered structure using silicon as submounts for each layer. The dimension of the module is 17 × 17 mm, and the thickness is less than 2 mm. Figure 4 illustrates the cross-sectional schematic of the designed module. The top submount carried all the LED dies to form the light source with phosphors. The driver and control circuitry was embedded into the bottom submount. The vertical electrical interconnection from the top to the bottom submount was achieved by TSVs filled by conductive silver glue, while the two layers were bonded using thermal grease. The interconnections between

Figure 3 Cross-sectional schematic of embedded passive device structure



Notes: (a) Solderable pads with SMT device; (b) non-solderable pads with wire-bondable device; (c) non-solderable pads with SMT device

Figure 4 Cross-sectional diagram of the 3D SiP module



the two layers also play as I/Os to external circuitry. To enhance the light extraction, the top submount was coated with a thin layer of aluminum. Among all the metals, only silver shows higher reflectivity than aluminum. Furthermore, design with cavities has also been studied. Aluminum-coated cavities help extract more light from the LEDs according to our test.

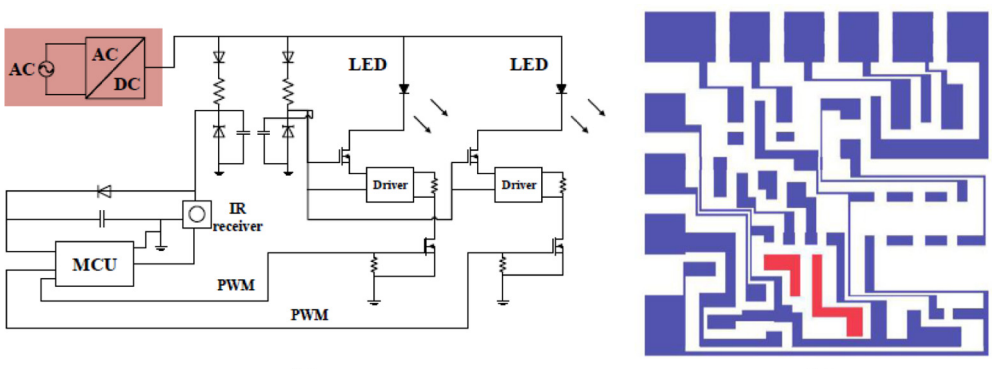
Figure 5 shows a typical circuit of infrared remote control luminaires. Two LED chains are designed with different color temperatures. Linear drivers are used to limit the currents passing each LED chain. The pulse width modulation (PWM) method is used to control the brightness of the LEDs. A micro-control unit (MCU) receives commands from an infrared receiver and sends the PWM signal to the switches on the driver paths. This circuit was adopted as a case study in this paper because of specific reasons.

To ease the unnecessary complexity of the module design, the power supply part [shadow highlighted in Figure 5(a)] in the circuit was not integrated in the module because of the bulkiness of the components. The 3S technology aims to develop a novel SiP approach; therefore, it only bares dies were used in the design except for the surface mount-type passive devices (SMDs). The benefit of this SiP approach comes from the compact form factor and cost reduction.

For smart control circuitry, high-frequency signal usually exists, to which special attention needs to be paid. The PWM control signal in the selected lighting application has a frequency of 1 kHz. This frequency was set by the preprogramed MCU provided by the supplier. Also, because the linear driver was used to control the LEDs, as long as the frequency of PWM signal is above 200 Hz, which can causes flickering, it meets the requirement of the LED application. In the layout design, high-frequency signal traces were kept wide and short and apart from each other by a safe gap, as indicated in Figure 5(b).

The top submounts were fabricated on 800-μm-thick, 4-inch double-side polished p-type, <100> orientation, silicon wafers. The process began by depositing 400 nm of silicon nitride (Si_3N_4) on both sides of the wafer by low-pressure chemical vapor deposition (LPCVD) at 850°C. This layer was then patterned and etched to form a hard mask for wet Si etching [Figure 6(a)]. Cavities were etched in the bulk Si using 33 per cent KOH solution at 85°C to the depth of 250 μm [Figure 6(b)]. Afterwards, a SiO_2 masking layer of 4 μm was coated by plasma-enhanced chemical vapor deposition (PECVD) [Figure 6(c)]. Deep reactive ion etching (DRIE, Adixen AMS100 system) process was carried out for the formation of TSVs, followed by removing the oxide-masking layer [Figure 6(d-e)]. Afterwards, the wafer surface was again covered with a SiO_2 layer, using wet thermal oxidation. The thickness of this layer was 3 μm to prevent dielectric breakdown at high voltages [Figure 6(f)]. Al was then sputtered by physical vapor deposition (PVD) for the interconnections between the ICs and reflective layer on the front side of the submounts with a layer thickness of 2 μm [Figure 6(g)]. Because the submounts contained many etched cavities, spray-coated positive photoresist, with the nominal thickness of 9 μm on the top surface, had to be used for metal patterning. The thickness of the resist layer at the top and bottom edges of the cavities was investigated using scanning electron microscope imaging (Figure 7). Top edge measured thickness was approximately 2.2 μm, which was sufficient for wet or plasma etching of Al. Resist buildup at the bottom corner was approximately 16 μm, which was patterned by using prolonged exposure and development times. It should be pointed out that some of the bare dies assembled on the bottom submount have bigger thickness, so they will extrude from the cavities and form uneven surface of the bottom submount. The backside cavities on the top submount were used to cover those higher dies when

Figure 5 (a) Schematic of the smart LED module adopted from a commercialized lamp [The power supply (highlighted) is kept out of the 3D SiP] and (b) trace layout of the driver and control circuitry (red highlighted part: PWM control signal with frequency of 1 kHz)



(a) (b)

Figure 6 Fabrication process flowchart of top-amount fabrication process

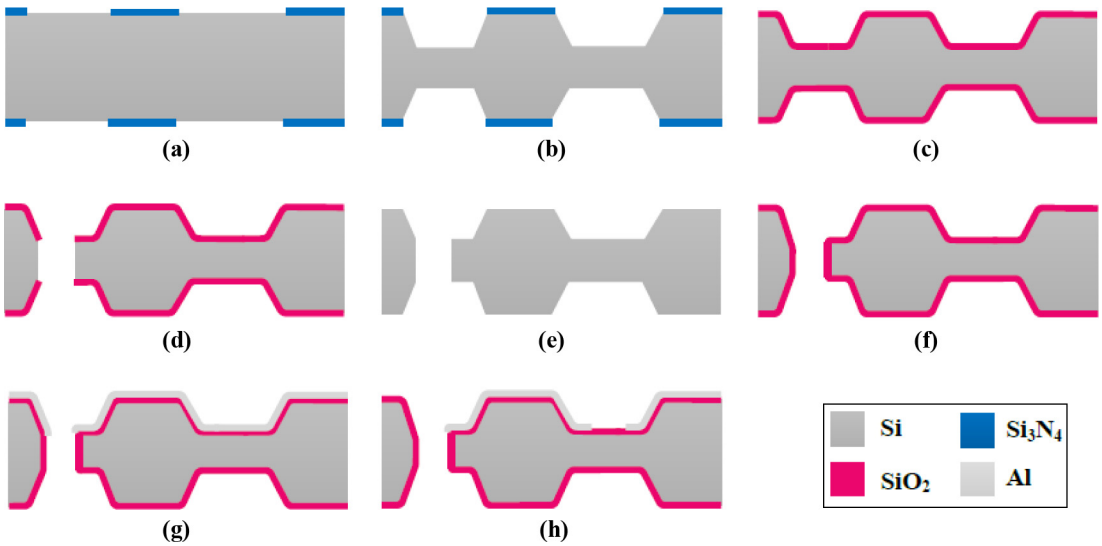
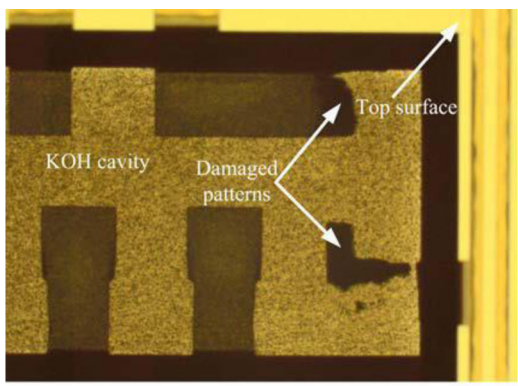
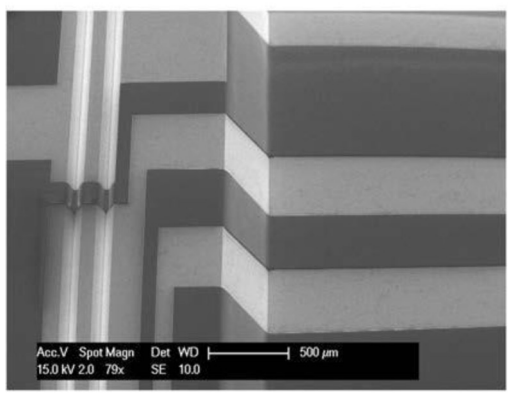


Figure 7 (a) Damaged photoresist patterns because of reflection from sidewalls; (b) scanning electron microscope image of patterned photoresist, using anti-reflective coating



(a)



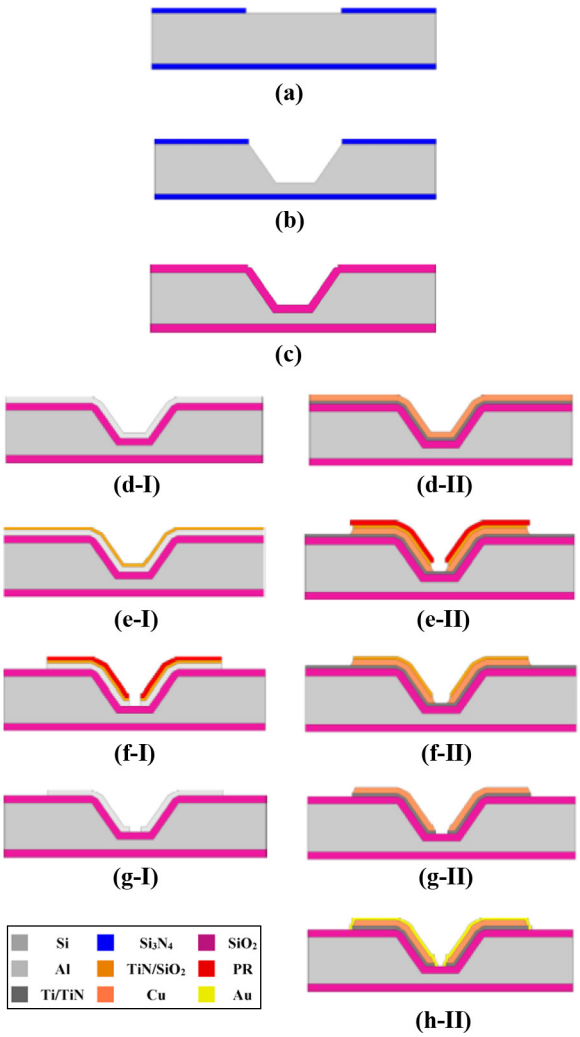
(b)

the submount bonding was conducted, so that the total thickness of the submount stack was kept as low as possible.

The bottom submounts were fabricated with similar process. The wafers used were single-side polished, <100>, with the thickness of 525 μm. The KOH cavities were etched only on the front side at a depth of 400 μm using the same recipe [Figure 8(a and b)]. A SiO_2 isolation layer of 3-μm thickness was thermally grown after the nitride masking layer was removed [Figure 8(c)]. Two different metals were used by PVD sputtering process, namely, Al and Cu with the same layer thickness of 2 μm. The processing steps for both metals will be discussed separately; Al was deposited directly on thermal SiO_2. It was observed that some of the structures were ruined because of light reflection from the metalized sidewalls of cavities during exposure. This phenomenon was not observed in the fabrication of top submounts because the cavities were not so deep as the ones of the bottom submounts. An anti-reflective coating consisting of 50 nm TiN, and 15 nm of PECVD SiO_2 was deposited to solve the resist damage issue because TiN is well-known to absorb light emitted, while the thin oxide layer was used to improve photoresist adhesion to the substrate. TiN/Al stack was patterned using an inductive coupled plasma-reactive ion etching (ICP-RIE) etcher [Figure 8(f-I)]. The Al-based submounts were finalized by removing the anti-reflective layer (ARL) from the interconnect surface by another short buffered hydrofluoric acid (BHF) dip followed by short RIE etch step for etching of SiO_2 and TiN [Figure 8(g-I)]. The Ti/TiN (10/40 nm) barrier/adhesion layer was sputtered prior to Cu PVD [Figure 8(d-II)]. The aforementioned anti-reflective coating (TiN/SiO_2) was also used for patterning Cu. TiN ARL was etched in ammonia, hydrogen peroxide and deionization (DI) water solution (1:4:4). Bulk Cu layer was etched using sodium persulfate and DI water with a very small amount of sulfuric acid [Figure 8(e-II)]. The photoresist was then removed with N-methyl-2-pyrrolidone at 70°C [Figure 8(f-II)]. Then, BHF and TiN etching solutions were used again to remove the thin SiO_2 and the TiN on top of Cu and the Ti/TiN layers under the Cu [Figure 8(f-II)]. To prevent oxidation of Cu, the interconnections were finalized with electroless Au plating of 100 nm [Figure 8(g-II)].

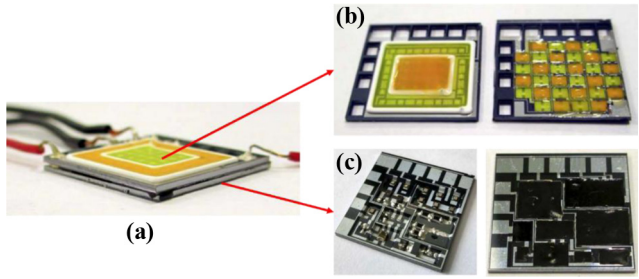
The top submount only carries LED dies. The assembly of LEDs was done by standard die bonding and wire bonding

Figure 8 Fabrication process flowchart of bottom-amount fabrication process; I: metallization process with Al; II: metallization process with Cu



process. Both the die bond and wire bond process was achieved at the wafer level. Then, the wafer was diced into dies. To get white light, yellow and red phosphor were used to convert the blue light. In the module, yellow phosphor was used to get cold white light (6,500 K), while yellow and red mixed phosphor was used for warm white light (3,000 K). The phosphor powder was dispersed into silicone before being dispensed. For the submount with cavities, the phosphor was dispensed on top of LEDs directly. For the planar design, two rings of dam were dispensed to form reservoirs prior to phosphor dispensing, as indicated in Figure 9(b). The driver and control circuit components were assembled on the bottom submounts, including both the SMD passives and bare die ICs. For the submount with Al trace (pads), all the interconnections were formed by silver glue. The silver glue was first dispensed on the pads, and then, the components were picked and placed on top, followed by the glue-curing process. For the submount with Cu trace (pads), first the SMDs were attached to the pads using pre-dispensed solder paste. Then, the submount was heated to 200°C for 10 s to melt the solder paste. Then, the bare die ICs

Figure 9 (a) Side view of stacked silicon module; (b) top submounts with cured phosphor; (c) assembled bottom submount before and after encapsulation



were attached to the submount using the same process as used for the Al submount. For both type of submount assembly, wire bonding was carried out on all bare dies, followed by glob-top encapsulation to protect the bond wires, as shown in Figure 9(c).

The stacking of submounts consists of two parts, namely, mechanical bonding and electrical connection. The two submounts were bonded using two-component thermal grease with the thermal conductivity of 30 W/mK. The thermal grease was dispensed on top of bottom submount first. Then, the top submount was aligned with and pressed onto the bottom one. To connect the module to external circuit, wires were also connected out from silver glue-filled TSVs [Figure 9(a)]. The stacking process was conducted at the chip level. To evaluate the design and process, multiple tests were conducted on the testing vehicles, including function validation, thermal test and optical test.

The stacked module was adhered on a metal plate by thermal pad for thermal test, as shown in Figure 10. The input voltage was 50 VDC, and the power consumption was 6 W. The temperature was measured at room temperature of 25°C by a thermal infrared imager. The highest temperature of 80.8°C appeared on the LED locations. For most of the indoor lighting applications, this temperature is fully acceptable. Considering that the luminaires usually provide more efficient heatsinks than the measurement setup, the temperature of the LEDs is expected to be lower. Thermal issue is one of the biggest challenges for SiP technique. Our testing results show that the proposed 3D SiP approach is suitable for medium-power application in terms of thermal management. For high-power applications, the presented module is also expected to show satisfying performance taking advantage of the higher thermal conductivity of the silicon submount than other substrate materials, such as polymer-based laminations. One potential thermal improvement would be achieved by implementing more advanced submount bonding technology. The thermal grease bonding approach can be replaced by eutectic bonding or fusion bonding, either of which helps reduce the thermal resistivity of the module.

The light output measurement was carried out on single top submount (light source) and stacked module in the integrating sphere. For the single top submount, 48 VDC was applied, and the current and the light output were measured. For the stacked module, 53 VDC was chosen. The measurement results are listed in Table I. The low and high color temperatures were designed to be 3,000 and 6,500 K,

Figure 10 Temperature distribution of the SiP module inside working bulbs without the cap: individual cavity design ([a] and [b]); modified planar design ([c] and [d])

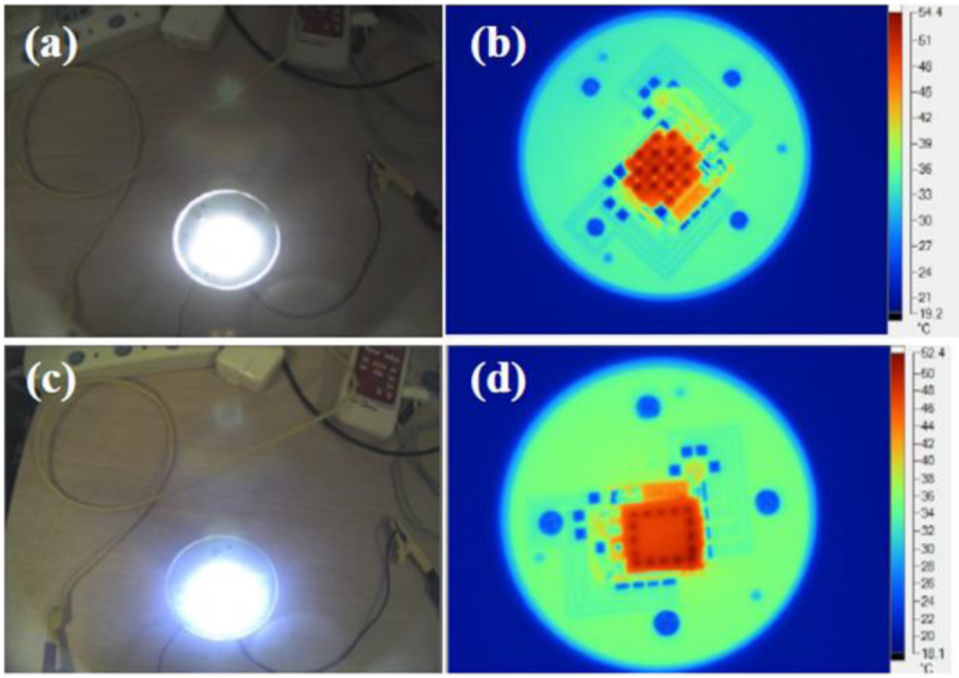


Table I Optical test results of unstacked submounts and stacked module

Sample	Planar TS			Cavity TS			Stacked module with cavity TS
	Low CT	High CT	Mixed	Low CT	High CT	Mixed	Mixed
Input voltage (V)	48	48	48	48	48	48	53
Input current (mA)	65	71	140	71	63	140	138
Light output (lm)	147	249	393	191	211	399	329
CT(K)	2526	6590	4683	2863	7021	4309	3803

Notes: TS = Top submount; CT = color temperature

respectively. From the measurement results, deviation can be seen because of the phosphor dispensing process. The stacked module showed less light output than single top submount because the effective voltage on LED chains was lower than the input voltage (53 VDC) because of the distributed voltage on the driver and control circuit. Moreover, the current passing through the LEDs was also slightly smaller than the input current because of the current bypassing the control circuit (about 5 mA). For commercialized luminaires, better optics need to be integrated with the module, which can further enhance the light performance. The light performance of LED highly relies on the temperature. Unexpectedly, high temperature will fasten output degradation. The presented silicon submount approach should provide satisfying reliability by easing the thermal management. More detailed results were discussed in the previous work (Dong *et al.*, 2013, 2015).

3.2 P.M. sensor system

With the increasing public awareness of the impact of PM on human health, real-time monitoring of PM exposure level has attracted more interest than ever before. While a great deal of effort has been put into the miniaturization of PM sensors, a wider range of applications is still hindered by big form factor and high cost. A novel design of PM sensor based on silicon microfabrication is presented. Silicon microfabrication and assembly process enable relatively small form factor and low cost. The operation principle of the sensor is light scattering, an indirect way of measuring PM concentration. Silicon-based microfluidic channel serves as air flow path including the sensing chamber where the light scattered by aerosol particles is detected. The chips are integrated in the form of bare dies, reducing the size of the whole system compared with PCB assembly of packaged devices.

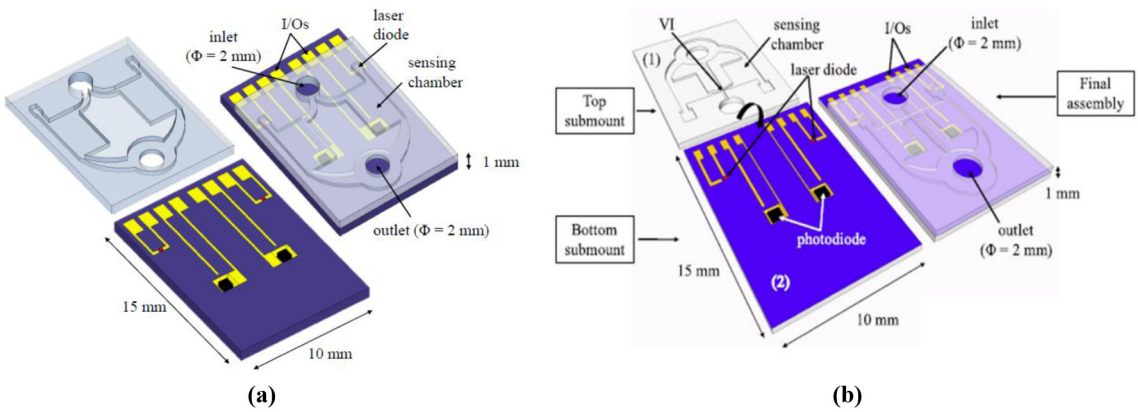
The sensor consists of a sensing unit and unit and control circuitry. The sensing unit is formed by two 3Ss, with the size of 15 × 10 × 1 mm. The bottom silicon submount hosts the chip elements and the interconnections. A red light laser diode with a wavelength of 650 nm is used as a light source in this work. A photodiode (T1670P, Vishay Inc.), used as light receiver, is placed into a cavity. On each submount, two pairs of light source and receiver are assembled for design redundancy and

easing the sensor testing. Laser diodes with different wavelengths can be mounted on each side of the sensor to accommodate wider range of particle size and composition. On the edge of the bottom submount, metal pads are placed for connecting all the chips with external control circuitry. The top submount contains air flow channels with inlet and outlet. When the two submounts are stacked, a sealed sensing chamber is formed with light source and receiver in between, as illustrated in Figure 11.

The top submounts only contain microfluidic channels and inlet and outlet through holes. The wafers used are double-side polished, <100>, with the thickness of 500 μm. A SiO_2 masking layer of 300 nm is first thermally grown. The oxide layer on the front side of the wafer is patterned using dry etching [Figure 12(a)]. DRIE process is carried out for the formation of micro-fluid channels [Figure 12(b)]. Then, the wafer is flipped and the oxide layer on the backside is patterned [Figure 12(c)]. DRIE process is again conducted to form the through holes [Figure 12(d)], followed by removing the oxide masking layer [Figure 12(e)]. An ARL is coated on the front side of the wafer [Figure 12(f)].

The bottom submounts are fabricated on 500-μm-thick 4-inch p-type, <100> orientation, silicon wafers. The process starts by depositing 200 nm of Si_3N_4 on top side of the wafer by LPCVD at 850°C. This layer is patterned and forms a hard mask for wet Si etching. Afterwards, the resist is removed by oxygen plasma etching [Figure 13(a)]. Cavities are etched in the bulk Si using 40 per cent KOH solution at 80°C to the depth of 300 μm [Figure 13(b)]. The nitride masking layer is then removed by plasma etching. Afterwards, a SiO_2 isolation layer of 3 μm is coated by PECVD. Al is then sputtered by PVD for the interconnections between the ICs on the submount with layer thickness of 1 μm [Figure 13(c)]. Because the submounts contains deep etched cavities, spray-coated positive photoresist, with the nominal thickness of 9 μm on the top surface, has to be used for metal patterning. The Al layer is dry etched using plasma etcher, and the submounts are finalized by removing the photoresist with O_2 plasma [Figure 13(d)]. An ARL on top of the silicon submount surface is then deposited. To do this, the oxide isolation layer is dry etched after the Al etching to expose the silicon wafer surface [Figure 13(e)]. Then, a lift-off process step is conducted to form the ARL. Negative

Figure 11 Bottom submount accommodates chips and electrical connections, while top submount forms air channel and sensing chamber by stacking onto the bottom half



Notes: (a) 3D Schematic structure of PM sensor; (b) 3D Schematic structure of the p.m.2.5 sensor with virtual impactor (VI)

Figure 12 Fabrication process flow of top silicon submounts

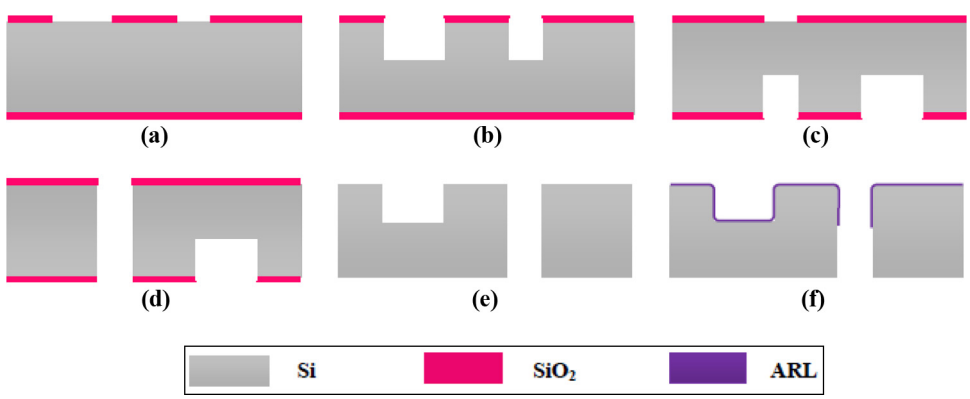
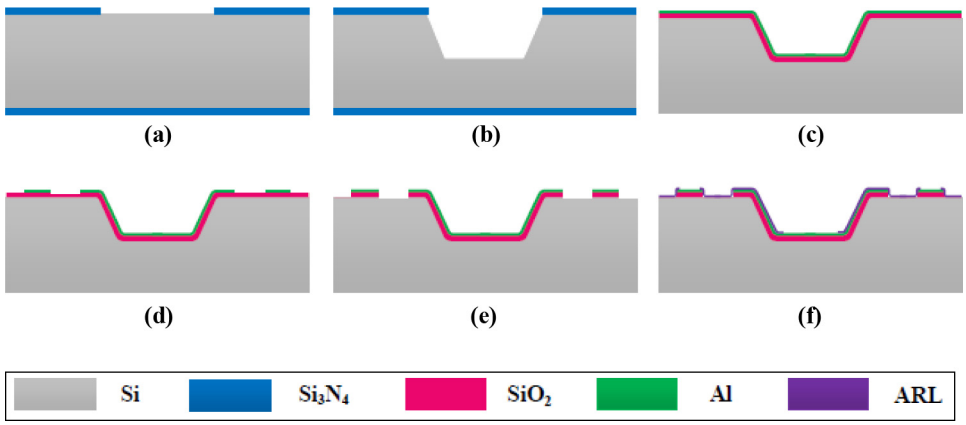


Figure 13 Fabrication process flow of bottom silicon submounts



photoresist is coated on the wafer and patterned to expose most of the wafer surface except for the electrodes for IC interconnections. Then, a layer stack of $TiO_2/SiO_2/TiO_2/SiO_2$ is deposited by evaporation. The thickness of each layer in the layer stack is determined according to the light source parameters. The photoresist lift-off is done by boiling the wafer in acetone [Figure 13(f)]. The submount silicon wafer is singulated into chips. The assembly process consists of bare die IC connection, submount stacking and external connection. The bare die laser diode and photodiode are placed on the bottom submount and connected with electrode by conductive silver adhesive. Wire bonding is used to connect upper electrodes of bare dies to the submount pads. Then, the top submount is aligned and mounted on the bottom submount by adhesive bonding. To further prepare for the later sensor testing, the assembly is mounted on a piece of PCB, through which the I/Os of the sensor would be connected to the control circuit board. A fraction of plastic pipe is glued over the air outlet to connect with a micro pump, which pulls the air from inlet to outlet by negative pressure leading to an air flow rate of 20 mL/min. Figure 14 shows an assembled sensor ready for testing.

The sensors are tested in a 25 m^3 environmental chamber. A calibrated portable aerosol spectrometer (OPC 1.109, GRIMM Inc.) is used as reference for real-time particle concentration monitoring. The GRIMM monitor has been widely used and proved as a trustable particle concentration monitor with a deviation factor of maximum 3 per cent. During the testing, the aerosol generator works periodically with each working cycle consisting a 15-min on-time and 45-min off-time. The sensors are sampled at a frequency of 16 Hz. The GRIMM monitor, however, is preset to give a reading every 6 s. Therefore, we average the sensor measurements to fit this lower sampling interval. Figure 15(a) shows the sample data from two tested sensors and the reference aerosol monitor. The x-axis represents the elapsed time from the beginning of the test and plotted on the y-axis is the raw data of the tested sensors (10-bit ADC-values, upper curves) and the PM concentration measured by the GRIMM monitor (in $\mu g/m^3$, lower curve). During the aerosol generator on-period, the particle concentration in the testing chamber rises and peaks around 55 $\mu g/m^3$ according to the GRIMM monitor readings. After the generator is switched off, the concentration slowly drops to under 10 $\mu g/m^3$. Our sensors clearly catch the concentration change, but the lower detection limit is observed. Both linear and polynomial regression analysis with different polynomial orders are conducted between the readings of our sensor and the

Figure 14 Sensor assembly connected with micro pump for testing

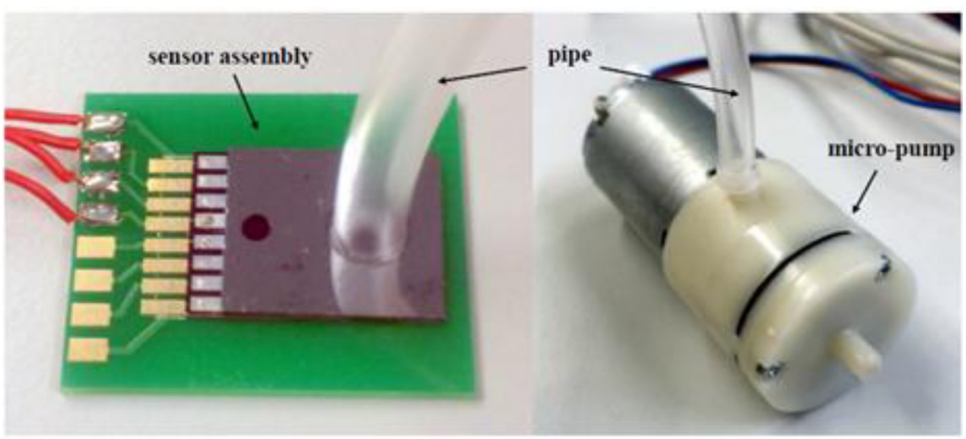
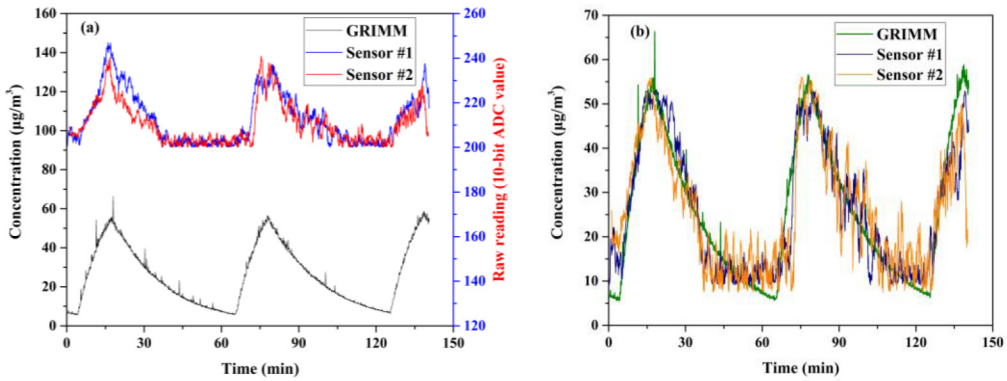


Figure 15 Representative readings from the tested sensors and the reference monitor



(a) **(b)**

Notes: (a) Raw data; (b) calibrated data

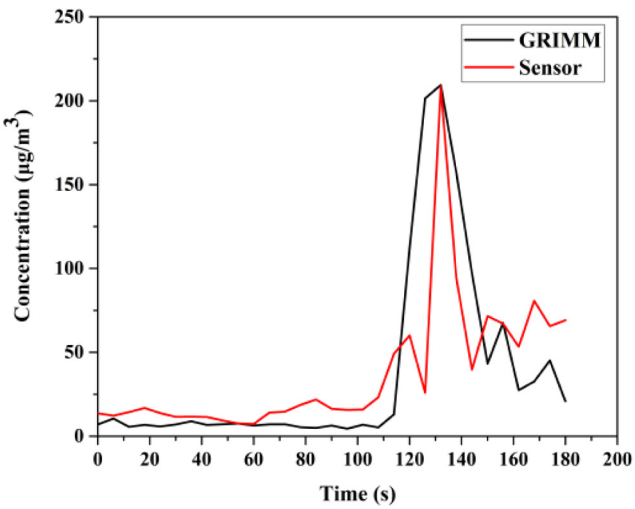
GRIMM reference. To evaluate the quality of curve fitting, the standard deviation and mean absolute error (MAE) $\text{MAE} = \frac{1}{n}\sum_{i=1}^{n}|f_i - y_i|$ are computed, and the results are summarized in Table II in which the polynomial order of 1 stands for linear regression. Also listed in Table II are the values of R^2 of the regression analysis. According to the regression result, the best fitting is achieved by the third-degree and second-degree polynomial regression for Sensor 1 and Sensor 2, respectively. The achieved measurement accuracy reaches 4.38 and 5.80 μg/m^3, respectively.

Another test carried out on the sensors is an indoor dust test. Both the GRIMM monitor and our sensor are placed in the office, while the floor is swept by a broom. The same calibration procedure is applied to raw data from the tested sensor, and the calibrated readings are shown in Figure 16 with the reference readings from the GRIMM monitor. As the broom sweeps across the room, the PM concentration can reach as high as 200 μg/m^3. Due to the uneven spatial distribution of the PM in the room, the measurement of our sensor is not completely overlapped with the one from the GRIMM monitor. But the measurement results still show that our sensor possesses good capability of fast and reliable detection of indoor airborne particles. More detailed about designs and results of PM sensor and p.m. 2.5 sensor were discussed in the previous work (Dong *et al.*, 2017, 2016).

Table II Results of regression analysis

Polynomial order	1	2	3	4
SD (μg/m³)				
Sensor 1	6.35	5.91	*5.81*	15.35
Sensor 2	8.11	*7.72*	21.05	39.50
MAE (μg/m³)				
Sensor 1	4.74	*4.43*	4.38	14.29
Sensor 2	6.27	*5.80*	19.48	38.44
R^2				
Sensor 1	0.836	0.858	0.863	0.867
Sensor 2	0.730	0.765	0.770	0/776

Figure 16 Indoor dust testing result



Notes: The tested sensor (red curve) shows fast and accurate response to indoor aerosol particle concentration change

3.3 Gas sensor system

Gas sensors are used in many applications including detection of toxic and combustible gases; monitoring emissions from vehicles and other combustion processes; breath analysis for medical diagnosis; and quality control in the chemicals, food and cosmetics industries. There are various types of gas sensors, such as optical, electrochemical, catalytic, surface acoustic wave, capacitive and semiconductor gas sensors for different gases (Lin *et al.*, 2015). In this gas sensor system, suitable size MEMS gases sensors can be composited to sensor array (Fleischer and Lehmann, 2012). Temperature and humidity are very important parameters for measuring gas concentration. While temperature compensation can be found in most gas measuring systems, the humidity of the medium is neglected in many cases. For rough concentration measurement, this limitation can be accepted, but for highly accurate measurements, humidity acts like an interfering gas.

Additionally, driver and control circuit, micro-processer chips, wireless communication chips, output conditioning circuit were used in gas sensor system.

Figure 17 illustrates the cross-sectional schematic of the designed system. The top submount carried all the temperature and humidity dies. The driver and control circuitry was embedded into the bottom submount. The vertical electrical interconnection from the top to the bottom submount was achieved by TSVs filled by conductive silver glue, while the two layers were bonded using thermal grease. The interconnections between the two layers also play as I/Os to external circuitry. Furthermore, the bare sensor die was wire bonded to the bottom submount and covered by top submount with holes for gases flowing to the surface of the sensors, decreasing the cost of gas sensors package and form factor compared to PCB board system (Patel *et al.*, 2012). The presented intelligent system aims to realize miniaturized and fully functional SiP instead of modules or devices which can be used as a note of sensors network or internet of things (IoT).

3.4 Discussion

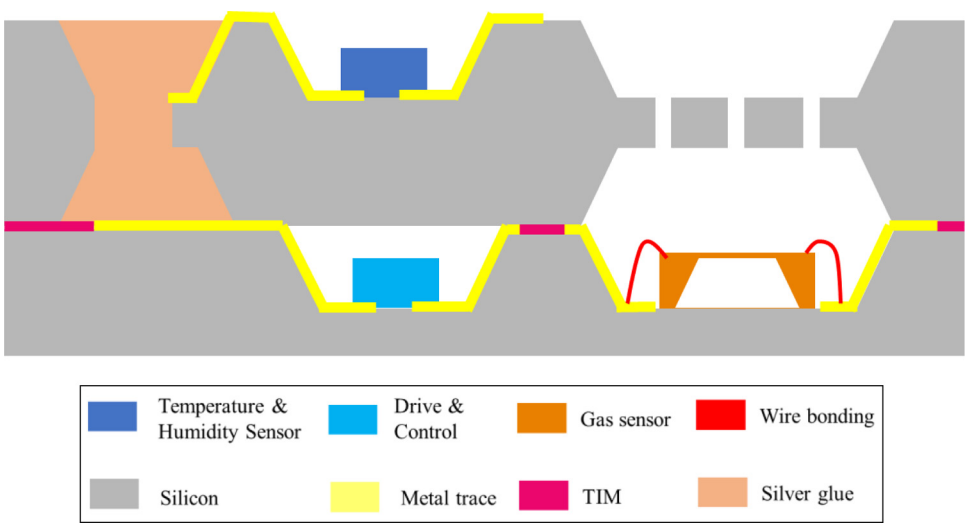
This paper presents a novel SiP design as a solution for system integration of intelligent applications. With era of intelligence approaching, highly integrated smart modules and systems are in high demand while currently always fit the needs of emerging applications. The research conducted and presented aims to provide a designated solution to bridge the technology gap and promote wider range of the intelligent applications.

Development of intelligent systems always embraces multi-physical design because such systems deliver functionalities of various domains and require interactions with surroundings in different ways. For instance, optical design is involved in lighting applications together with thermal, electrical and mechanical design. MEMS sensors need proper structural design together with electric circuitry design. When SiP design is used, the aforementioned design aspects become more challenging because the compact form factor poses additional limitations on the freedom of design.

For SSL module, a silicon substrate with higher thermal conductivity compared to most of the packaging substrate materials, such as ceramic, PCB, metal-core printed circuit board, can greatly ease the thermal issue because of fast spread of heat through silicon both vertically and laterally was used for thermal management of the LEDs. Remote phosphor is an effective approach to reduce the thermal damage of phosphor from the LEDs. The thermal management further extends to the interaction among different components within a system, mainly the heat sources and the heat sensitive components. For integrated smart lighting system, electrical components including active ICs and sensors are inevitably affected by the heat from the LEDs. For general lighting application, optical design is the core of development of a system that guarantees sensitivity and accuracy. The design with aluminum-coated cavities help extract more light from the LEDs. To achieve high performance of PM and p.m. 2.5 sensor, the optimal of both structural parameter and materials property were designed in this demonstration. In the design, the top submount contained microfluidic air channels with inlet or outlet is fabricated by silicon substrate, which can be replaced by microfluidic materials with an ARL, such as ceremic, SU-8 and PDMS. Moreover, it is very possible and cost-effective to make such sensors based on cheaper material forming methods, such as injection or 3D printing. Development needs are done closely with substrate supplier and packaging house.

The requirement for packaging substrates including precise dimension and controlled surface roughness. The substrate should provide the main housing of the sensor, as well as metal traces for electrical interconnections. The supplier should process capability of precise polymer forming (molding) and metallization on polymer. The packaging process is not so challenging, it only involves die attach and die bond. Besides, some customized assembly process may be needed, such as parts gluing and dicing. The modified TSV process in intelligent gas sensor system can be the gas flow holes for gas sensors chip. The materials of submount substrate also can use other semiconductors materials with through-hole technology, such as PCB, glass, ceramic and polymer. For many intelligent

Figure 17 Cross-section diagram of gas sensor system



applications, supporting circuitry enables interaction between the hardware and the surroundings. Therefore, the electrical design should always be taken into account for the system design. In the applications presented, the customized circuitry is integrated with the process of silicon microfabrication and optimized by packaging process. The attempt made in this paper about 3D SiP design platform using the 3S technology is expected to provide better understanding toward the SiP technology and its protentional implementation in intelligent applications. For large volume production, cost is always a driver for technology evolvement. To build the intelligent world, a massive net of intelligent devices are needed. Enabled by novel material and process development, more cost economical solutions are created to meet the fast-growing need of smart devices. Within semiconductor industry, aforementioned technologies such as WLP and SiP have been serving the goal of reducing cost. Besides, emerging low cost technologies are also seeking opportunities to play their role. For instance, 3D printing technology, also known as additive manufacturing, has already shown its great potential in many applications (Lipson and Kurman, 2013). There is no reason that this technology should not benefit the microelectronics industry.

4. Conclusion

This paper presents an SiP design using silicon as packaging substrate (submount). The fabrication of the silicon substrates is mainly realized by MEMS process, and some customized processes are modified to better suit the need of selected applications. The microfabrication of silicon guarantees accurate dimensions for micro-structure design, which is beneficial for optics-related applications. Besides, the MEMS process is a batch process, thus intrinsically leading to high uniformity and reproducibility. The 3D structure out of silicon is mainly realized by etching. The silicon etching includes isotropic and anisotropic etching, and both are implemented in the presented SiP design. By combining the two types of etching, modified TSV process is developed and implemented into SSL module development. On the other hand, the micro-machined cavity in silicon submount presents challenge for the fabrication of the SiP module, especially the fabrication of the silicon submounts. When the cavity is used for embedding components, metallization inside the cavity is often needed. To achieve good quality of metal patterning, photoresist needs to be spray coated, and prolonged exposure and development time are used.

A full miniaturization design of a smart LED module is demonstrated enabled by proposed 3D SiP approach. The optimization of the module design covers thermal, optical, electrical and structural aspects of the system design. Developed silicon microfabrication process is successfully implemented into the fabrication of silicon submounts of the smart LED module. 3D interconnection and embedded component are fulfilled by means of WLP process. The module prototype is fully characterized and delivers all designed functionality and good thermal and optical performance, proving the proposed 3D SiP design's promising approach for miniaturization of smart lighting modules.

The developed SiP design is also implemented into the miniaturization of PM sensors. Light scattering is selected as the operation principle of the PM sensor because of its capability of continuous monitoring, easy maintenance and low power consumption. Light scattering and microfluidics analysis are conducted to optimize the design parameters, including the sensor dimension, the optical property of the sensor material, the control circuitry and so on. A complete design of the PM sensor is presented with well-tested performance. The silicon-based SiP design is very suitable for integrated smart sensor applications.

An intelligent wireless gases detection system integrated with temperature and humidity sensors, based on SIP technology, was designed to realize minimization for growth market of distributed wireless sensor system, which will constitute the hardware infrastructure of the IoT.

SiP has great potential of integrating multiple components into a single compact package, which meets the need of "MtM" trend: function enrichment of highly integrated systems. The attempt made in this paper is expected to provide better understanding toward the SiP technology and its potential implementation in intelligent applications.

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