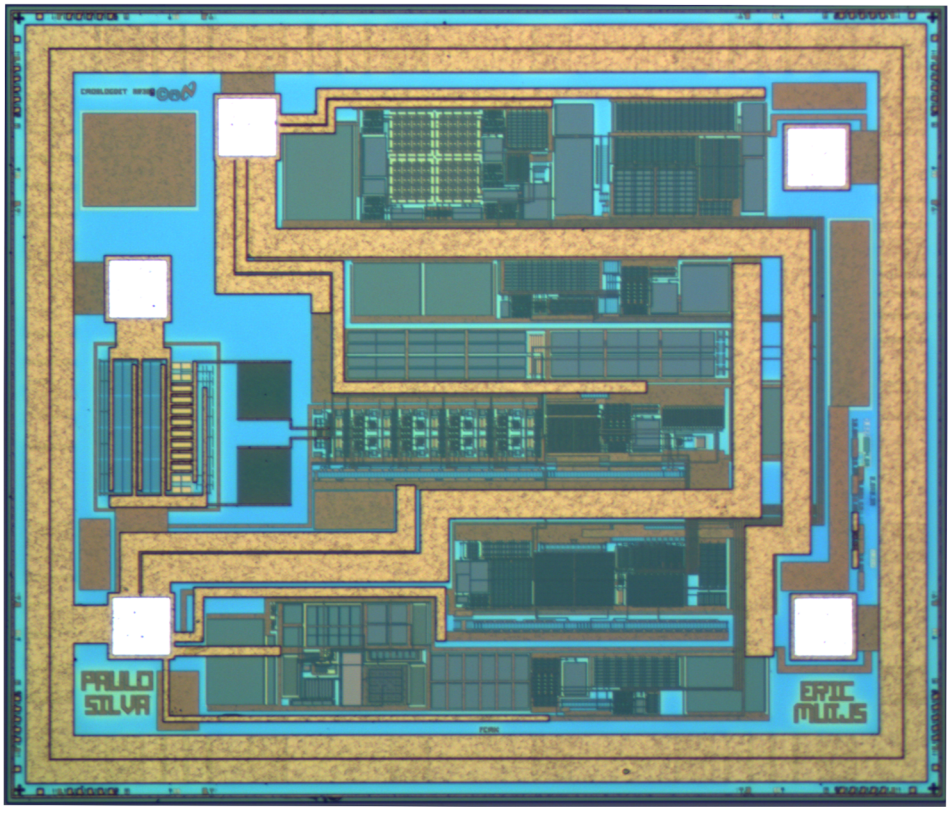
A CMOS Temperature Compensated Log-Amp Detector

Eric Muijs

Master of Science Thesis



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Microelectronics

A CMOS Temperature Compensated Log-Amp Detector

Master of Science Thesis

For the degree of Master of Science in Microelectronics at Delft University of Technology

Eric Muijs

May 22, 2013

Faculty of Electrical Engineering, Mathematics and Computer Science · Delft University of Technology

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A CMOS Temperature Compensated Log-Amp Detector

by

Eric Muijs

in partial fulfillment of the requirements for the degree of

Master of Science Microelectronics

Dated: May 22, 2013

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Abstract

To accurately set the output power of a power amplifier in handsets, a power control loop is often used. A coupler before the antenna senses a fraction of the output Radio Frequency (RF) signal and feeds it to the input of a logarithmic amplifier (log-amp) detector. The output of this device is proportional to the logarithm of the average peak value of the RF input signal. Knowledge about the modulation type employed, allows accurate calculation and control of the transmitted power.

Most log-amp detectors are made in bipolar processes for RF performance. However, due to the recent advancement in RF performance of analog CMOS technologies, designing a log-amp detector in CMOS becomes more attractive in terms of cost and integration in handsets. The designed prototype Integrated Circuit (IC) demonstrates that a temperature compensated log-amp RF power detector can be designed using standard 0.18 μm CMOS technology.

A total of 24 samples have been measured. All samples handle an input power ranging from -50 to +10 dBm for RF input signals ranging from 100 MHz to 1.8 GHz. A typical dynamic range of 38 dB for a $\pm$1 dB log-conformance error was achieved. Up to 900 MHz the temperature drift is never larger than $\pm$1.1 dB for all 24 measured samples over a temperature range from -40 to +85°C. The current consumption is 6.3 mA from an 1.8 V power supply and the chip area spans 0.76 mm^2. Apart from the limited bandwidth of the IC, dynamic range and temperature performance proved to be similar to products from the major companies on the analog market.

Newer CMOS nodes were tested to get an understanding of the scalability of this design. Simulations show that using 65 nm CMOS technology the bandwidth can be increased significantly (up to $3X$) while attaining the same power consumption.

A new temperature scheme was introduced, which uses a Proportional To Mobility (PTM) biasing scheme to stabilize the output of the log-amp detector over temperature. Simulations show that using the PTM scheme the temperature drift is within $\pm$0.8 dB for RF input frequencies up to 900 MHz .

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Preface

As part of my master Microelectronics I did an one-year internship at Texas Instruments. Dr.ir A. van Staveren suggested me to design a log-amp RF power detector in 0.18 μm CMOS technology. The measurement data of this Integrated Circuit (IC) would provide a data point on the bandwidth and temperature performance of this technology node. Extrapolating the bandwidth performance for newer technology nodes would provide a basis on the feasibility of a commercial CMOS log-amp detector.

Acknowledgements

The work described in this thesis would not have been possible without the support and dedication of many people. First I want to thank Dr.ir. P.G. Raymundoa Silva, my daily supervisor, for his assistance and dedication during the complete design cycle of the chip. I also want to greatly thank Dr.ir. W.A. Serdijn, for his enthusiasm and help during the project. Furthermore I want to thank Dr.ir. A. van Staveren for giving me the opportunity to work at Texas Instruments Delft with a highly dedicated team of analog IC designers, which all supported me during this project.

Delft, University of Technology
May 22, 2013

Eric Muijs

Chapter 1

Introduction

The output of a logarithmic amplifier (log-amp) detector is proportional to the logarithm of the average peak value of the RF input signal.

Application Log-amp detectors are mainly used in the telecommunication business. In both mobile phones and base stations it is important to control the output power of the Power Amplifier (PA) to [6]:

- Keep the output power of a PA within the specifications of the desired broadcast standard
- Prevent interference from handset to handset
- Minimize power consumption in handset
- Prevent inter-modulation in base station receivers
- Measure the power of an input signal in a spectrum analyzer

The log-amp detector in this thesis is designed as part of a power control loop. The output power of a PA inside a handset can not be set accurately enough within an output power range of $\pm 2\,\mathrm{dB}$, as required by the modulation standards [6]. Therefore, a negative feedback control loop is used as shown in Figure 1-1. The coupler senses a portion of the output Radio Frequency (RF) signal going to the antenna, which will be subsequently measured by the log-amp detector. The digital control block senses the output of the log-amp detector to regulate the PA output power to the desired value.

Design Goal Most log-amp detectors are made in bipolar processes for RF performance. However, due to the recent advancement in RF performance of analog CMOS technologies, designing a log-amp detector in CMOS becomes more attractive in terms of cost and integration in handsets.

The specifications for a log-amp power detector for mobile handset use can be extracted from cellular wireless standards such as GSM/CDMA/EDGE/WCDMA. Typically a Dynamic Range (DR) of ≥30 dB is needed, at carrier frequencies ranging from 700 MHz up to 2.1 GHz. However, due to the relatively old CMOS node of 180 nm the Bandwidth (BW) will be limited. Therefore, the BW specification is set to 900 MHz, a carrier frequency which is used in the GSM and LTE broadcast standards.

RF power detectors for handsets have an industry temperature range of -40 to 85°C, for which the typical temperature drift should be ≤1 dB. This is to prevent the need for characterization over temperature. Although log-amp detectors in bipolar technology present good temperature stability [7, 8]. CMOS log-amp detectors for RF power detection so far published fail to demonstrate consistent performance over a wide temperature range [9, 10]. Hence, the design of this CMOS log-amp detector will be focused on temperature performance.

As the chip is designed for mobile phone use, power consumption should be limited to about 20 mW. To match the coupler, a characteristic input impedance of 50 Ω will be used as this is the standard for most RF transmissions. A summary of the specifications is given in Table 1-1.

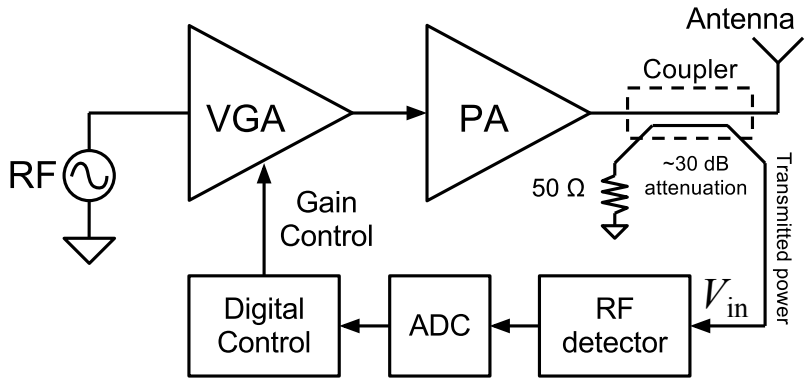


Figure 1-1: Block diagram of a power control loop in a handset

Dynamic Range	Bandwidth	Max Temperature Error	Power Consumption
≥30 dB	≥900 MHz	±1 dB	≤20 mW

Table 1-1: Specifications for the CMOS log-amp detector

Chapter 2

Architecture

This chapter gives an introduction to the field of log-amp detectors. To be able to understand how this type of system operates, it is most intuitive to describe the logarithmic amplifier first. After this introduction the base-band log-amp will be introduced, for which the transfer is formulated and different aspects of the architecture will be described. This will be followed by the log-amp detector, which is the core architecture used in the final circuit design. To be able to compare performance among log-amp detectors two figure of merits are discussed, which will be used to evaluate temperature drift and derive temperature compensation.

2-1 The Logarithmic Amplifier

System A logarithmic amplifier is a non-linear system, for which the transfer is a logarithmic function. Signals with a large dynamic range can be converted into an output signal with a smaller dynamic range.

To achieve an ideal logarithmic transfer it is possible to use an operational amplifier, together with an exponential feedback element as shown in Figure 2-1. If the gain of the operational amplifier (opamp) is infinite, the overall transfer will be equal to the inverse transfer of the feedback path. An exponential element in the feedback, a diode for example, will thus result in a logarithmic transfer.

In this figure the input V_{in} and output V_{out} units are voltages. Resistor R is used to convert the input voltage in a current. This current $I_D = V_{\text{in}}/R$ will pass through the diode, which has an exponential behavior from voltage to current:

$$I_D = I_S(e^{V_{\text{out}}/nV_T}), \tag{2-1}$$

where I_S is the reverse bias saturation current, V_{out} is the voltage across the diode, V_T is the thermal voltage and n is the ideality factor of the diode.

The inverse of (2-1) is the desired logarithmic transfer function: $V_{\text{out}} = nV_T \ln(V_{\text{in}}/(RI_S))$.

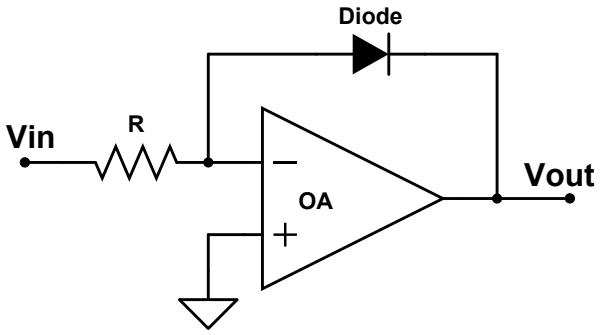


Figure 2-1: Schematic of a logarithmic amplifier implemented with feedback

2-1-1 Baseband Log Amp

A logarithmic transfer can also be achieved by a piece-wise linear approximation method. To understand how this approximation can achieve a logarithmic function, a baseband log amp will be explained [8]. This system comprises of two components:

- Gain cells: cells that exhibit a gain of A up to a certain input voltage E_{kA} (knee voltage), at which the cell clips to $A \cdot E_{\mathrm{kA}}$ (2-2). See Figure 2-2.
- Summation cells: cells that add the output of the gain cells, see Figure 2-3.

Mathematically the gain-cell transfer can also be described as:

$$V_{\text{out-A}}(V_{\text{in-A}})\ [V] = \begin{cases} A \cdot V_{\text{in-A}}, & \text{if } |V_{\text{in-A}}| < E_{\mathrm{kA}}\,, \\ A \cdot E_{\mathrm{kA}}, & \text{if } |V_{\text{in-A}}| \geq E_{\mathrm{kA}}\,, \end{cases} \tag{2-2}$$

in which A is the gain of the gain cell. Knee voltage E_{kA} is given by:

$$E_{\mathrm{kA}} = \frac{\max(V_{\text{out-A}})}{A}\,, \tag{2-3}$$

where $\max(V_{\text{out-A}})$ is equal to $A \cdot E_{\mathrm{kA}}$.

The gain cells and summation cells are connected as shown in Figure 2-3.

First lets assume that input signal V_{in} is really small, such that only the last gain cell achieves its maximum output ($V_{\mathrm{in1}} = \frac{E_{\mathrm{kA}}}{A^2}$). According to Figure 2-3, the output voltage will be:

$$V_{\mathrm{out1}} = \frac{E_{\mathrm{kA}}}{A^2} + \frac{E_{\mathrm{kA}}}{A} + E_{\mathrm{kA}} + AE_{\mathrm{kA}}\,. \tag{2-4}$$

At the next transition ($V_{\mathrm{in2}} = \frac{E_{\mathrm{kA}}}{A}$) the last two gain cells are saturated, yielding an output of:

$$V_{\mathrm{out2}} = \frac{E_{\mathrm{kA}}}{A} + E_{\mathrm{kA}} + 2E_{\mathrm{kA}}A\,. \tag{2-5}$$

At the last transition ($V_{\mathrm{in3}} = E_{\mathrm{kA}}$) all gain cells are saturated. Hence, the output is equal to:

$$V_{\mathrm{out3}} = E_{\mathrm{kA}} + 3E_{\mathrm{kA}}A\,. \tag{2-6}$$

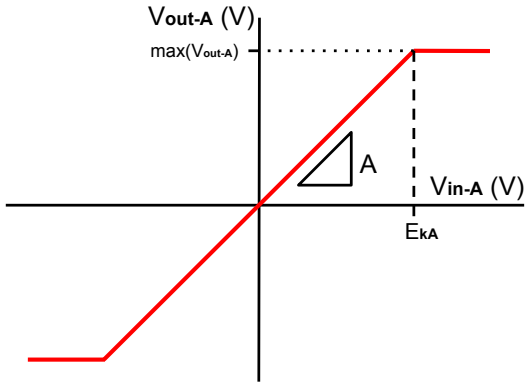


Figure 2-2: Transfer of ideal gain cell

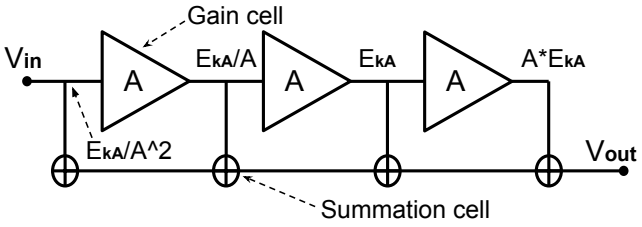
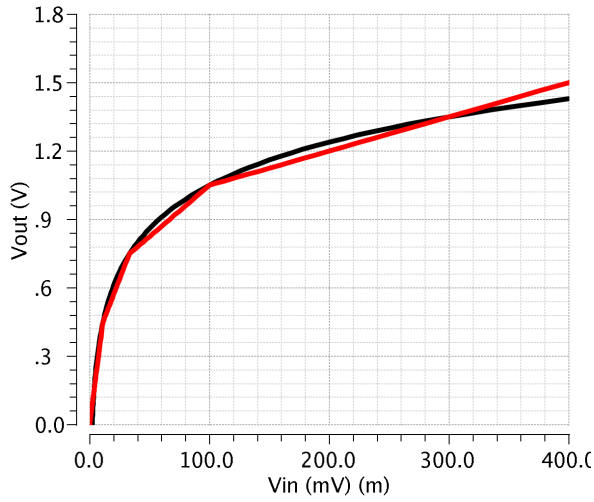


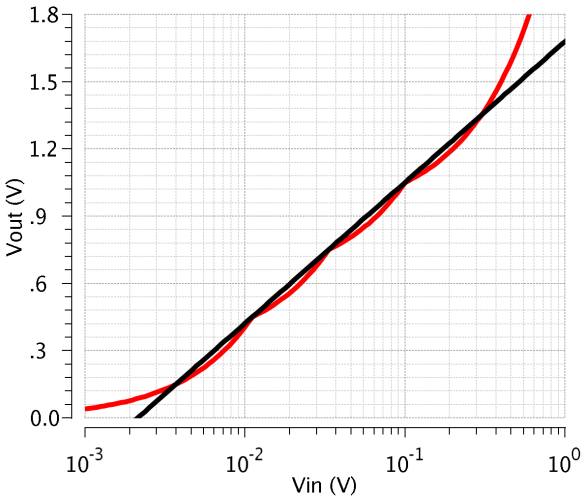
Figure 2-3: Block diagram of baseband log amp

So at each gain cell saturation, the output will increase by a linear factor, while the input actually is multiplied with the gain of the gain cell (A). This shows how this system implements a logarithmic function using piece-wise approximation.

A comparison between an ideal logarithmic response versus the baseband log-amp output is shown in Figure 2-4a.



(a) Axis (linear, linear)



(b) Axis (logarithmic, linear)

Figure 2-4: Transfer of 3-stage baseband log amp [black = ideal log transfer, red = log-amp output]

Output Model The equation for an ideal logarithmic response equals:

$$V_{\text{out}} = K_S \cdot 20 \log \left(\frac{V_{\text{in}}}{V_I} \right), \tag{2-7}$$

in which K_S [V/dB] and V_I [V] are two fitting parameters, which control the shape of the logarithmic transfer.

Calculating K_S can be done by subtracting two outputs:

$$\begin{aligned} \Delta V_{\text{out12}} &= \Delta V_{\text{out2}} - \Delta V_{\text{out1}} \\ &= E_{\text{kA}} \cdot A - \frac{E_{\text{kA}}}{A^2} \\ &\sim E_{\text{kA}} \cdot A \,. \end{aligned} \tag{2-8}$$

Substituting this result in the ideal log equation of (2-7) yields:

$$\begin{aligned} \Delta V_{\text{out12}} &= K_S \cdot 20 \log\left(\frac{A V_{\text{in2}}}{V_I}\right) - K_S \cdot 20 \log\left(\frac{V_{\text{in1}}}{V_I}\right), \\ E_{\text{kA}} \cdot A &= K_S \cdot 20 \log(A)\,, \\ K_S &= \frac{E_{\text{kA}} A}{20 \log(A)}\,. \end{aligned} \tag{2-9}$$

The term E_{kA}/A^2 in (2-8) is relatively small and is neglected in this calculation. In the next paragraph a correction technique is able to cancel this term.

Using the first clipping point: $(V_{\text{in1}}, V_{\text{out1}})$, K_S (2-9) and the ideal log (2-7), parameter V_I can be calculated (see Appendix A-1):

$$V_I = \frac{E_{\text{kA}}}{A^{N+1/(A-1)}}\,, \tag{2-10}$$

in which N is the number of stages of the log amp.

Plotting the log-amp transfer in a graph with a logarithmic x-axis yields an output which can be approximated by a linear line approximation, as shown in Figure 2-4b. Rewriting the voltages V_{in} and V_I in dBV:

$$X_{\text{in}}\,[\text{dBV}] = 20 \log(V_{\text{in}})\,, \tag{2-11}$$

$$X_I\,[\text{dBV}] = 20 \log(V_I)\,, \tag{2-12}$$

substituting (2-11) and (2-12) in the ideal log equation of (2-7):

$$\begin{aligned} V_{\text{out}} &= K_S \cdot 20 \log\left(\frac{V_{\text{in}}}{V_I}\right) \\ &= K_S \cdot (X_{\text{in}} - X_I)\,, \end{aligned} \tag{2-13}$$

yields an expression of a linear line. The slope K_S and intercept point X_I are defined as:

$$K_{\text{S}}\,[\text{V/dB}] = \frac{E_{\text{kA}} A}{20 \log(A)}\,, \tag{2-14}$$

$$X_{\text{I}}\,[\text{dBV}] = 20 \log\left(\frac{E_{\text{kA}}}{A^{N+1/(A-1)}}\right). \tag{2-15}$$

In Figure 2-4b the black line represents the ideal logarithmic response, while the red line is the log-amp output. At very low input levels the system has a linear transfer, deviating from the black line. When the rightmost gain cell clips at input voltage V_{in1}, the log amp has a logarithmic response, following the black line up to input voltage V_{in3}. When the input increases above this voltage, the first summation cell will again yield a linear response, deviating from the ideal black line.

Top-end correction In the previous paragraph, the term E_{kA}/A^2 was neglected in (2-8). The output for a log amp for which this term is not neglected is shown in Figure 2-5, indicated by the blue line. To approximate the ideal logarithmic output transfer, the output voltage

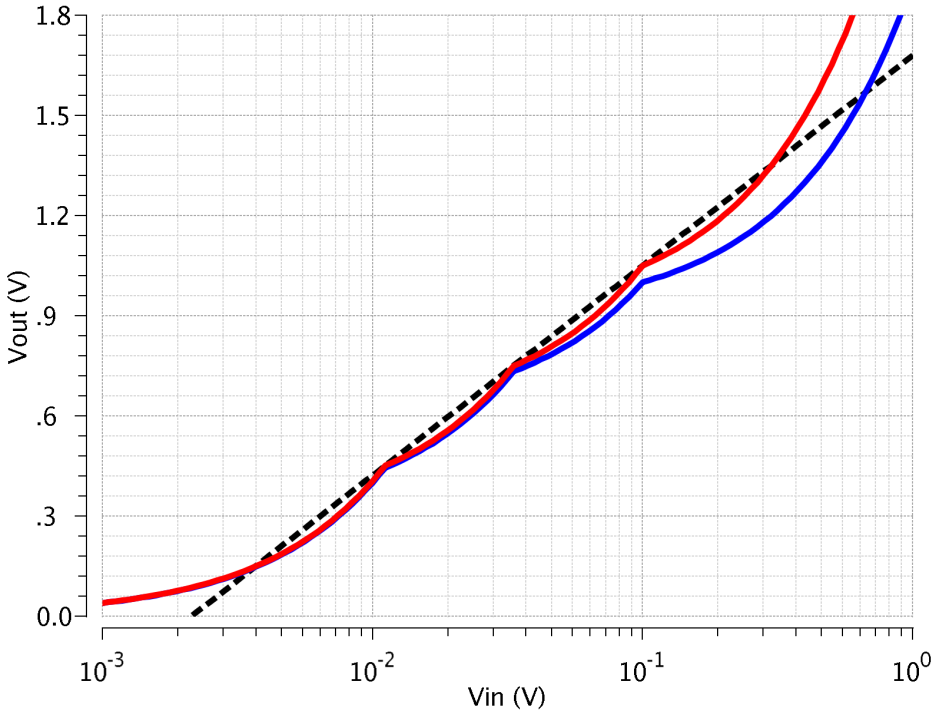


Figure 2-5: Output baseband log amp for $N = 3$ [black = ideal log, red = with, blue = without top end correction]

always increases by a linear amount, $A \cdot E_{\mathrm{kA}}$, as the input is multiplied by a factor A. This means that the slope should be constant for as long as not all stages are clipped. However, from (2-4) and (2-5) the increase in output voltage is:

$$\Delta V_{\mathrm{out12}} = \Delta V_{\mathrm{out2}} - \Delta V_{\mathrm{out1}} = E_{\mathrm{kA}} \cdot A - \frac{E_{\mathrm{kA}}}{A^2}\,. \tag{2-16}$$

Comparing $\Delta V_{\mathrm{out12}}$ to the increase in output between (2-5) and (2-6), it becomes clear that they are not the same:

$$\Delta V_{\mathrm{out23}} = \Delta V_{\mathrm{out3}} - \Delta V_{\mathrm{out2}} = E_{\mathrm{kA}} \cdot A - \frac{E_{\mathrm{kA}}}{A}\,. \tag{2-17}$$

For small inputs, the $\frac{E_{\mathrm{kA}}}{AX}$ part is quite small and could be neglected. However, when the input of the log amp grows, this part becomes bigger: X reduces by one for each transition, resulting in a reduction of the slope.

Another way to explain the need for top-end correction is that all other stages, except the first gain cell (high input), have preceding stages for which the output voltage increases as the input increases towards the knee voltage. However, the first gain cell (high input), does not have these preceding stages.

To achieve the same slope across all transitions, a top-end correction factor is applied to the first summation cell. This means that the addition from this summation cell is "weighted"

with a factor D_0 equal to [8]:

$$D_0 = \frac{A}{A-1}\,. \tag{2-18}$$

Now the output for the first transition is given by ($V_{\text{in1}} = E_{\text{kA}}/A^2$):

$$\begin{aligned} V_{\text{out1}} &= \frac{A}{A-1}\cdot\frac{E_{\text{kA}}}{A^2} + \frac{E_{\text{kA}}}{A} + E_{\text{kA}} + E_{\text{kA}}\cdot A\,, \\ (A-1)\cdot V_{\text{out1}} &= E_{\text{kA}}\left(\frac{1}{A} + 1 - \frac{1}{A} + A - 1 + A^2 - A\right), \\ V_{\text{out1}} &= E_{\text{kA}}\cdot\frac{A^2}{A-1}\,. \end{aligned} \tag{2-19}$$

For the second transition ($V_{\text{in2}} = E_{\text{kA}}/A$) the output is equal to:

$$\begin{aligned} V_{\text{out2}} &= \frac{A}{A-1}\cdot\frac{E_{\text{kA}}}{A} + E_{\text{kA}} + 2E_{\text{kA}}\cdot A \\ &= E_{\text{kA}}\cdot\frac{2A^2 - A}{A-1}\,. \end{aligned} \tag{2-20}$$

For the third transition ($V_{\text{in3}} = E_{\text{kA}}$) the output is equal to:

$$\begin{aligned} V_{\text{out3}} &= \frac{A}{A-1}\cdot E_{\text{kA}} + 3E_{\text{kA}}\cdot A \\ &= E_{\text{kA}}\cdot\frac{3A^2 - 2A}{A-1}\,. \end{aligned} \tag{2-21}$$

Now ΔV_{out} for all transitions is given by:

$$\Delta V_{\text{out}} = AE_{\text{kA}}\,, \tag{2-22}$$

which yields a constant V_{out} increase for all transitions, thus a constant slope. The output curve with and without top-end correction is shown in Figure 2-5.

Output model with Top-End correction Due to the top-end correction, the slope is equal as without top-end correction but does not decrease when the input increases:

$$K_S = \frac{AE_{\text{kA}}}{20\log(A)}\,. \tag{2-23}$$

The intercept point follows again from (2-7), the slope (2-23) and a (V_{in1},V_{out1}) point:

$$V_I = \frac{E_{\text{kA}}}{A^{N-1+D_0}}\,. \tag{2-24}$$

Instead of using dBV, the V_{in} and V_I can be expressed in power [dBm]:

$$P_{\text{in}}\,[\text{dBm}] = 10\log\left(\frac{V_{\text{in}}^2}{Z_{\text{in}}\cdot 1\,\text{mW}}\right), \tag{2-25}$$

$$P_I\,[\text{dBm}] = 10\log\left(\frac{V_I^2}{Z_{\text{in}}\cdot 1\,\text{mW}}\right). \tag{2-26}$$

Now the input-output relation can be expressed as:

$$\begin{aligned} V_{\text{out}} &= K_S\cdot 10\log\left(\frac{V_{\text{in}}^2}{V_I^2}\right) \\ &= K_S\cdot(P_{\text{in}} - P_I)\,. \end{aligned} \tag{2-27}$$

2-1-2 G_m-Cell Log Amp

The next step is to modify the log-amp system to closer resemble a physical implementation. Although voltage summation cells can be made in practice it is much easier to add currents. This can be done by converting the output voltages of the gain cells into currents and adding these. An output resistor will convert the total current into an output voltage.

In (2-28) the output of a new G_m cell is given. This cell is basically a gain cell with a current output.

$$I_{\text{out-G}}(V_{\text{in-G}})\,[A] = \begin{cases} \dfrac{I_{\text{bias-G}}}{E_{\text{kG}}} \cdot V_{\text{in-G}}, & \text{if } |V_{\text{in-G}}| < E_{\text{kG}}\,, \\ I_{\text{bias-G}} & \text{if } |V_{\text{in-G}}| > E_{\text{kG}}\,, \end{cases} \tag{2-28}$$

where E_{kG} is the knee voltage and $I_{\text{bias-G}}$ the bias current of the G_m cell.

A block diagram of the G_m-cell log amp is shown in Figure 2-6. It is assumed that this log amp is driven with only positive input voltages.

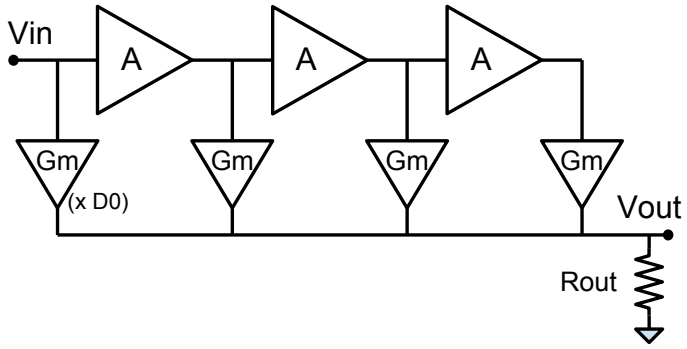


Figure 2-6: Block diagram of G_m-cell log amp

Output Model with G_m cells The output of this system does not deviate much from the original system. The only difference is that the output is now multiplied by the output resistance R_{out} and $I_{\text{bias-G}}$. The maximum output current for each G_m cell is given by:

$$\max(V_{\text{out}}) = I_{\text{bias-G}}(N - 1 + D_0)R_{\text{out}}\,, \tag{2-29}$$

where N denotes the number of stages and D_0 is the top-end correction, which is now applied by increasing the bias current of the G_m cell.

The slope and intercept-point equations can be rewritten as (see Appendix A-2):

$$K_S = \frac{I_{\text{bias-G}}R_{\text{out}}}{20\log(A)}\,, \tag{2-30}$$

$$V_I = \frac{E_{\text{kG}}}{A^{N+D_0}}\,. \tag{2-31}$$

One important thing to note is that the E_{kG} in Equation 2-31 is the knee voltage of the G_m cells. The output node of the last gain cell in Figure 2-6 determines the first logarithmic

point on the output curve. If the gain cell clips before the knee voltage of the rightmost G_m cell, E_{kG}, than $\max(V_{out\text{-}A})$ determines the first logarithmic point and thus the effective knee voltage $E_{k\text{-}eff}$:

$$E_{k\text{-}eff} = \begin{cases} \max(V_{out\text{-}A}), & \text{if } \max(V_{out\text{-}A}) < E_{kG}\,, \\ E_{kG}, & \text{if } \max(V_{out\text{-}A}) \geq E_{kG}\,. \end{cases} \tag{2-32}$$

In the rest of this chapter it is assumed that the gain cell swing is always larger than the knee voltage of the succeeding cells, such that their knee voltage (in this case E_{kG}) determines the intercept point.

From now on in this thesis the input will always be displayed in power, such that the transfer of a log amp can be expressed as:

$$V_{out} = K_S \cdot (P_{in} - P_I)\,, \tag{2-33}$$

in which:

$$K_S = \frac{I_{bias\text{-}G} R_{out}}{20\log(A)}\,. \tag{2-34}$$

2-2 Measures of Performance

To be able to distinguish log-amp performance, two types of performance metrics are discussed in this section.

2-2-1 Log-Conformance Error (LCE)

The LCE is probably the most used metric to compare log amps. This measure is based on the ideal input-output equation given by:

$$V_{out} = K_S \cdot (P_{in} - P_I)\,.$$

Using this equation, the error in dB for a point on the output curve $(P_{in1}\,[\text{dBm}], V_{out1}\,[V])$ would be:

$$\text{LCE(dB)} = \frac{V_{out1} - (K_S \cdot (P_{in1} - P_I))}{K_S}\,. \tag{2-35}$$

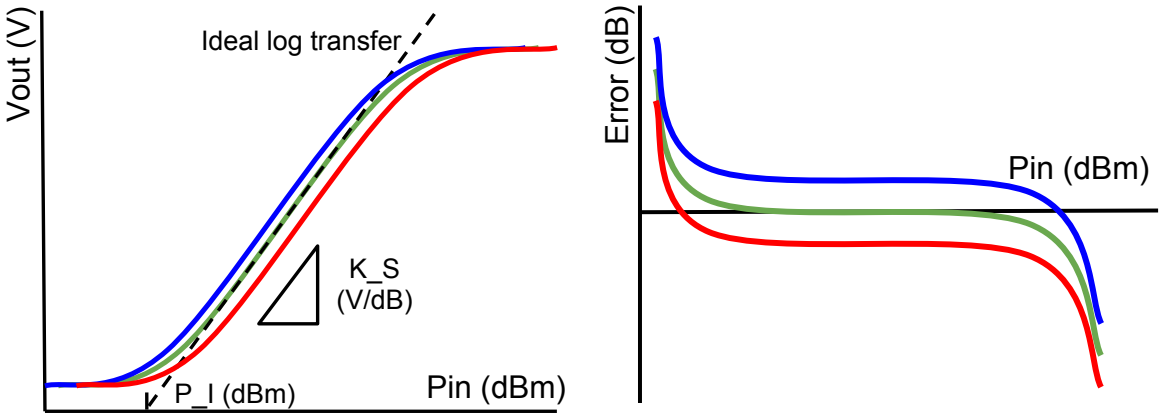
An LCE plot is thus calculated by subtracting all points of the log-amp output (Figure 2-7a) from the ideal logarithmic function with a slope K_S and intercept point P_I. These parameters are adjusted to yield an LCE fitted to the zero axis, as shown in Figure 2-7b.

In Figure 2-7a the three curves replicate three temperature output curves, with an intercept-point shift over temperature. The dotted line in Figure 2-7a represents an LCE of zero. Intercept-point shifts are visible in the LCE plot as a fixed error over input power.

2-2-2 Error Variation Over Temperature (EVOT)

The EVOT plot is a measure for the temperature drift of a log amp. The room temperature output curve is used as a reference. The error in dB for low and high temperature from this reference is the EVOT curve. Mathematically this is equal to:

$$\text{EVOT}_{cold/hot}\text{(dB)} = \frac{V_{out}(T_{cold}/T_{hot}) - V_{out}(T_{ref})}{K_S(T_{ref})}\,, \tag{2-36}$$



(a) Output curve over temperature **(b)** Log-conformance error

Figure 2-7: Output of a temperature dependent log amp [blue = cold, green = room, red = hot temperature]

where typically $T_{\text{cold}} = -40°\text{C}$, $T_{\text{hot}} = 85°\text{C}$ and $T_{\text{ref}} = 25°\text{C}$.

Basically the EVOT plot is an LCE plot for which the reference is not an ideal line, but the log-amp output at reference temperature T_{ref}. The EVOT for room temperature in thus always equal to the zero axis. The EVOTs for the output curves of Figure 2-7a are given in Figure 2-8.

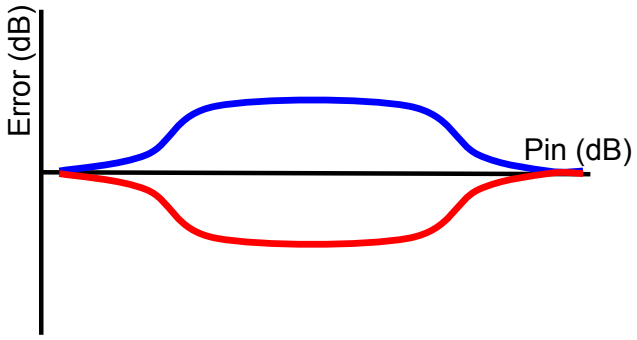


Figure 2-8: Error variation over temperature of the temperature dependent log amp [blue = cold, red = hot temperature]

2-3 Log-Amp Detector

Log-amp detectors really show why a log amp can be very useful. In a log-amp detector the G_m cells are replaced with detector cells, which perform a demodulating function. The detector cells detect the envelope of the RF input signal, such that their DC output is a measure of the average peak value of the input signal. This characteristic combined with the logarithmic response of the log amp, yields an output which is the log of the average detected envelop of the input signal. Because the output is a measure of the average peak value of the input signal, it is waveform dependent. Thus if the modulation type is known, the input power can be calculated based on the log-amp detector output.

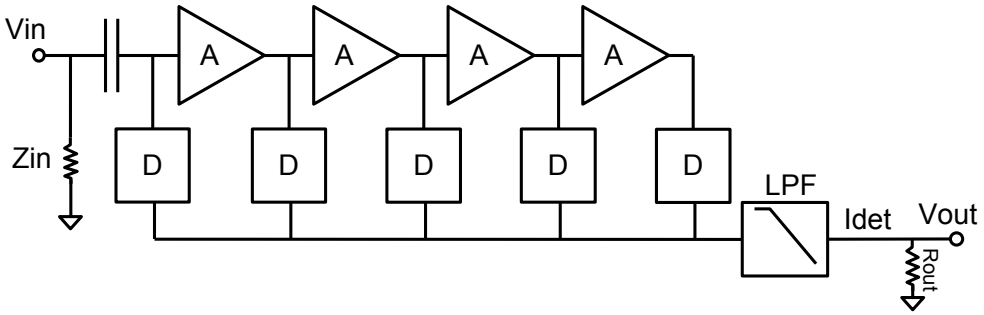


Figure 2-9: Block diagram of log-amp detector

2-3-1 Detector Cells

A large number of detector cells can be used from a theoretical point of view. In this chapter however, four types of detector cells are described. Each performs a different non-linear (demodulating) operation:

- Detector cell X^4
- Detector cell X^2
- Detector cell $|X|$
- Detector cell $\sqrt{|X|}$

Detector transfer The general output of a detector cell is given in Equation 2-37 and shown in Figure 2-10.

$$I_{\text{out-D}}(V_{\text{in-D}})\ [A] = \begin{cases} I_{\text{bias-D}}\left(\dfrac{|V_{\text{in-D}}|}{E_{\text{kD}}}\right)^p, & \text{if } |V_{\text{in-D}}| < E_{\text{kD}}\,, \\ I_{\text{bias-D}}, & \text{if } |V_{\text{in-D}}| \geq E_{\text{kD}}\,, \end{cases} \tag{2-37}$$

in which p is the power of the detector cell transfer function, $I_{\text{bias-D}}$ the bias current and E_{kD} the knee voltage of the detector cell.

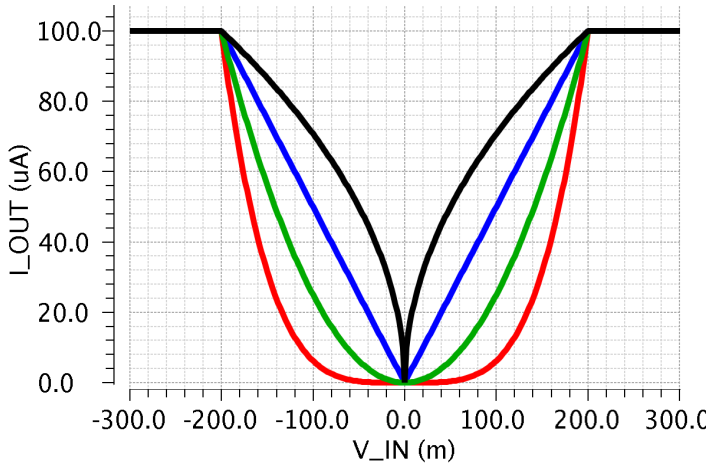


Figure 2-10: Output of detector cells with $E_{\text{kD}} = 0.2\,\text{V}$ [blue: p=0.5, black: p=1, red: p=2, green: p=4]

Demodulation of detector cell The detector cell demodulates the input signal by performing a non-linear operation. If $V_{\text{in-D}} = V_{\text{P}} \sin(x)$ and $p = 2$:

$$I_{\text{out-D}} = \frac{I_{\text{bias-D}}}{E_{\text{kD}}^2} V_{\text{in-D}}^2 \tag{2-38}$$

$$= \frac{I_{\text{bias-D}} V_{\text{P}}^2}{2E_{\text{kD}}^2} \left[1 - \cos(2x)\right], \tag{2-39}$$

which consist of a DC component: $I_{\text{bias-D}} V_{\text{P}}^2 / 2E_{\text{kD}}^2$ and a second harmonic. After the low-pass filter the detector-cell output is thus a measure of the peak, V_{P}, of the input signal.

If amplitude V_P of a sinusoidal input signal increases above the knee voltage, part of the period the detector-cell output clips to $I_{\text{bias-D}}$. As a result the average output current of the detector cell increases. After the low-pass filter this translates to a higher DC output current.

Table 2-1 shows the normalized DC output for other types of detector cells with the same input signal. Clearly all detector cells perform a demodulation of the input signal.

Detector-cell type	DC output normalized
$p = 0.5$	$\frac{9\sqrt{2P}V_{\text{P}}^2}{16\pi^{3/2}\sqrt{E_{\text{kD}}}}$
$p = 1$	$\frac{2V_{\text{P}}}{\pi E_{\text{kD}}}$
$p = 2$	$\frac{V_{\text{P}}^2}{2E_{\text{kD}}^2}$
$p = 4$	$\frac{3V_{\text{P}}^4}{8E_{\text{kD}}^4}$

Table 2-1: Normalized $I_{\text{bias-D}}$ for all detector-cell types, $V_{\text{in-D}} = V_{\text{P}} \sin(x)$

Output model for a log-amp detector Similar as in the previous section, top-end correction is needed. However each detector-cell type will need a different top-end correction factor D_0 (see Appendix A-4 for a proof):

$$D_0 = \frac{A^p}{A^p - 1}\,. \tag{2-40}$$

The lower the power, p in Equation 2-40, the more top-end correction is needed for a constant slope. The intercept point V_I is identical to the intercept point calculated in Section 2-1-2. Depending on the type of detector cell, the top-end correction will affect the intercept point according to:

$$V_I = \frac{E_{\text{kD}}}{A^{N+D_0}}\,.$$

The slope K_S remains equal to the log amp with G_m cells, because at every detector-cell transition the output voltage increases with $I_{\text{bias-D}}R_{\text{out}}$, which is equal to the output increase of the G_m cell:

$$K_S = \frac{I_{\text{bias-D}}R_{\text{out}}}{20\log(A)}\,.$$

Wobbles in the output curve Figure 2-11a shows output curves for four log-amp detectors, each with a different detector-cell type. All have appropriate top-end correction, according to (2-40). To correct the intercept-point shift due to the different top-end corrections, the knee voltage was modified.

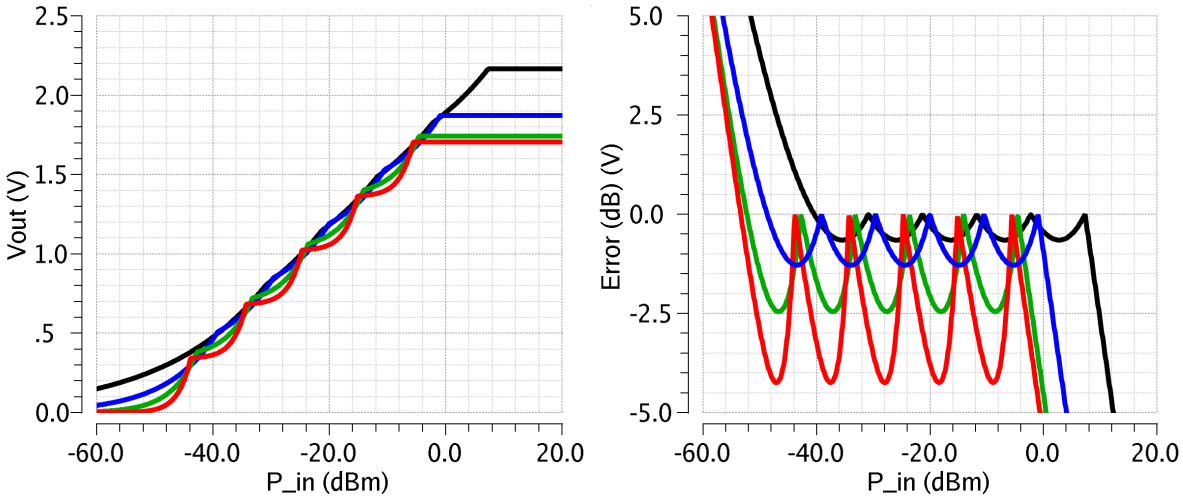
Due to the higher top-end correction of the low power detector cells ($p \leq 1$), their maximum output is higher. The LCE plot is shown in Figure 2-11b.

Although all output curves approximate the ideal logarithm, they show different responses. Wobbles, the log-conformance error in the flat region of the LCE plot, are smaller for lower power ($p \leq 1$) detector cells. This phenomena can be explained by the transfer of the detector cell, shown in Figure 2-10. For a low power detector cell, $p = 0.5$ for example, the current output increase is high for small inputs ($V_{\text{in-D}} << E_{\text{kD}}$) and a small current increase for high inputs ($V_{\text{in-D}} < E_{\text{kD}}$). This type of transfer more approximates a logarithmic function yielding an LCE with smaller wobbles.

2-3-2 Bottom-End Correction

Apart from the top-end correction, bottom-end correction is needed for sinusoidal input signals. Assume a detector cell with a knee voltage $E_{\text{kD}} = 200$ mV and $p = 2$. Figure 2-12a shows the output for multiple sinusoidal signals at different levels of input amplitude: $V_{\text{P}} = 200$ mV, 300 mV and 600 mV. The detector cell output voltages in Figure 2-12 are the current outputs of the detector cell terminated with a resistor, R_{out}.

If $A = 3$, the succeeding detector is clipping at $V_{\text{P}} = 600$ mV, while the average output of the detector cell (after the low-pass filter) only increased from 140 mV to 170 mV. See Figure 2-12b. The average output of the detector cell will never reach $I_{\text{bias-D}}$ for sinusoidal signals with finite amplitude. This result is different compared to DC input signals, for which each detector cell reaches its maximum output directly if its input amplitude reached the knee voltage. Only a square wave input signal does not suffer from this effect due to the infinite rise time of an ideal square-wave.



(a) Output curve **(b)** Log-conformance error

Figure 2-11: Output of log-amp detector with four types of detector cells [p: blue = 0.5, green = 1, red = 2, purple = 4]

As Figure 2-12b shows, a succeeding stage will still be rising in average output value. Because the last detector cell (rightmost) does not have any succeeding stages, the output of that stage should be enhanced, "weighted", to make sure that the slope is the same across all transitions, just like in Figure 2-5 with top-end correction. Figure 2-13a shows the output and LCE of a log-amp detector with and without bottom-end correction.

The bottom-end correction factor only has an influence on the intercept point V_I. Only the local slope for low-amplitude input signals is increased, the overall slope is unaffected. The intercept point will change to (see Appendix A-5):

$$V_I = \frac{E_{\mathrm{kD}}}{A^{N-1+D_0+B_0}}\,, \tag{2-41}$$

where B_0 is the bottom-end correction factor.

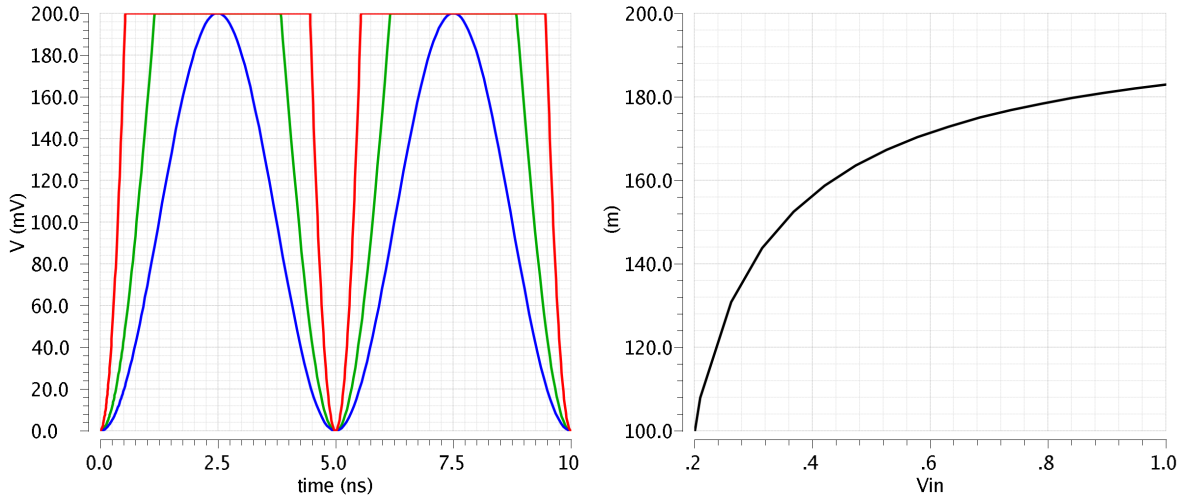
Approximation of bottom-end correction factor As with the top-end correction, bottom-end correction is needed to adjust the curve such that the slope is constant. The value of the bottom-end correction factor B_0 is dependent on the waveform as well as the type of detector cell. First the $|X|$ detector will be discussed, for a sinusoidal input signal with two amplitudes as shown in Figure 2-14. By approximating the slope at $x = 0$ it is relatively easy to calculate the clipping point, which is approximately at $x = A^{-1}$. The yellow and green areas in Figure 2-14 are given by:

$$\mathrm{Area}[\mathrm{total}] = \pi\,, \tag{2-42}$$

$$\mathrm{Area}[\sin(x)] = 2\,, \tag{2-43}$$

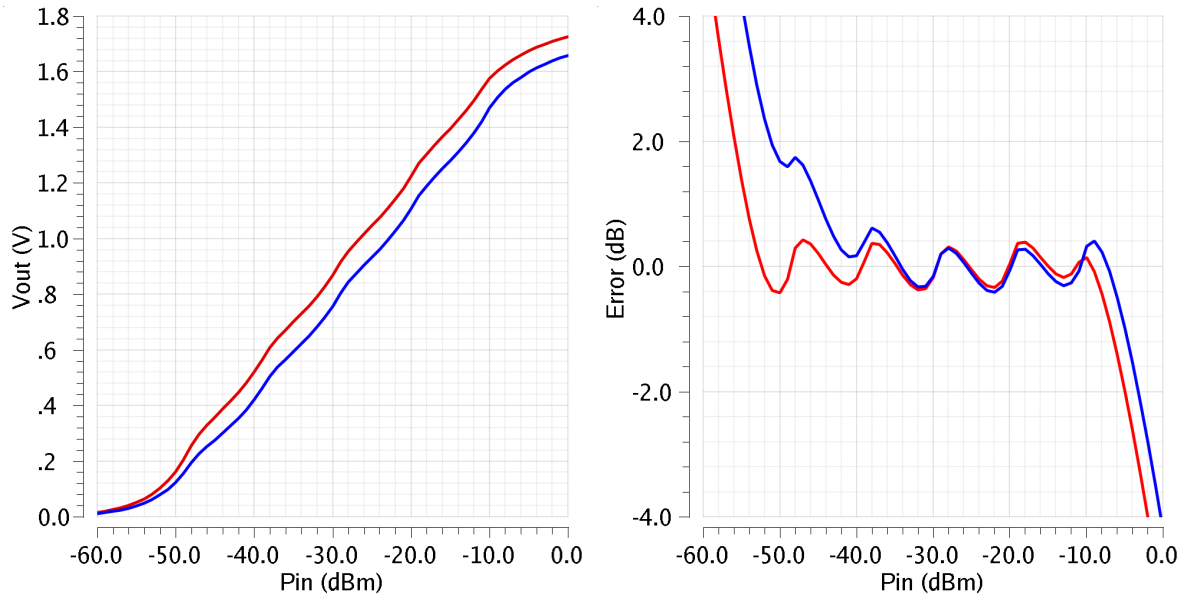
$$\mathrm{Area}[A\sin(x)] = \pi - \frac{1}{A}\,. \tag{2-44}$$

The bottom-end correction factor is the extra bias current for the last detector cell which is needed to yield the same increase in output current as the output increase of a detector cell in



(a) Output **(b)** Average of the output (after the low-pass filter)

Figure 2-12: Output of X^2 detector cell with $E_{\text{kD}} = 200$ mV for sinusoidal input signals with different amplitudes [Input amplitude: blue $= 200$ mV, green $= 300$ mV, red $= 600$ mV]



(a) Output **(b)** Log-conformance error

Figure 2-13: Output of log-amp detector with X^2 detector cells [blue $=$ without, red $=$ with bottom-end correction]

the middle of the log-amp detector. If one succeeding detector cell is considered, this factor is equal to the ratio between the green and yellow area in Figure 2-14:

$$(B_0)_{|X|,\sin} = \frac{\pi - \frac{1}{A}}{2} \tag{2-45}$$

$$= \frac{\pi}{2} - \frac{1}{2A}\,. \tag{2-46}$$

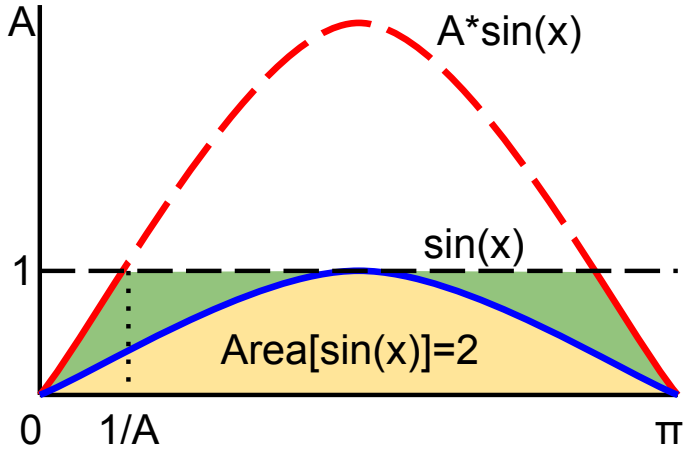


Figure 2-14: Method for calculating the bottom-end correction.

Using the same methodology the bottom-end correction can be estimated for other detector-cell types, see Table 2-2.

Detector-type	B_0
$p = 0.5$	1.28
$p = 1$	1.40
$p = 2$	1.51
$p = 4$	1.64

Table 2-2: Bottom-end correction factor B_0 for several detector-cell types (sinusoidal input signals)

2-3-3 Waveform Dependence

For different waveforms with equal Root Mean Square (RMS) values, the log-amp detector will give an intercept-point shift. This shift is independent on detector-cell type. Assuming the system approximates the ideal log equation given by [8]:

$$V_{\text{out}} = K_S \log\left(\frac{|V_{\text{in}}|}{V_I}\right), \tag{2-47}$$

which after low-pass filtering can be rewritten as:

$$\text{AVG}(V_{\text{out}}) = f \int_0^{1/f} K_S \log\left(\frac{|V_{\text{in}}|}{V_I}\right) dt. \tag{2-48}$$

The first waveform of interest is the square-wave, with infinitely small rise and fall times:

$$V_{\text{in-sw}}(t) = V_{\text{sw}} \cdot \text{sgn}\left[\sin\left(\frac{2\pi t}{T}\right)\right], \tag{2-49}$$

in which V_{sw} is the peak value, T the period and sgn the sign function[1]. Calculating the output of the log-amp detector output for a half period:

$$\begin{aligned} \text{AVG}(V_{\text{out-bw}}) &= 2T \int_0^{1/(2T)} K_S \log\left(\frac{V_{\text{sw}}}{V_I}\right) dt && \text{(2-50)} \\ &= 2TK_S \log\left(\frac{V_{\text{sw}}}{V_I}\right) \Big[t\Big]_0^{1/(2T)} && \text{(2-51)} \\ &= K_S \log\left(\frac{V_{\text{sw}}}{V_I}\right), && \text{(2-52)} \end{aligned}$$

which is equal to the output for a DC input of magnitude V_{DC}, because their average are equal. For a sinusoidal input signal of $V_{\text{in-sin}} = V_{\text{sin}} \sin(x)$ and noting that the average of a sinusoid is equal for a half-period ($0 \leq x \leq \pi$)[8]:

$$\begin{aligned} \text{AVG}(V_{\text{out-sin}}) &= \frac{1}{\pi} \int_0^{\pi} K_S \log\left(\frac{V_{\text{sin}} \sin(x)}{V_I}\right) dx && \text{(2-53)} \\ &= \frac{K_S}{\pi \ln(10)} \int_0^{\pi} \Big\{ \ln(\sin(x)) + \ln\left(\frac{V_{\text{sin}}}{V_I}\right) \Big\} dx && \text{(2-54)} \\ &= \frac{K_S}{\pi \ln(10)} \Big[-\pi \ln(2) + \pi \ln\left(\frac{V_{\text{sin}}}{V_I}\right) \Big] && \text{(2-55)} \\ &= K_S \log\left(\frac{V_{\text{sin}}}{2V_I}\right) = K_S \log\left(\frac{V_{\text{DC}}}{V_I}\right), && \text{(2-56)} \end{aligned}$$

which shows that a DC input signal with only half the amplitude of the sinusoidal input signal produces the same output. In Table 2-3 different waveforms with equal RMS powers are given, with the resulting log-amp detector output [8].

Waveform	Amplitude for RMS of V_{DC}	Log-amp output normalized	Error in dB
DC	V_{DC}	$\log(V_{\text{DC}})$	0
Square-wave	V_{DC}	$\log(V_{\text{DC}})$	0
Sinusoid	$V_{\text{DC}}\sqrt{2}$	$\log(V_{\text{DC}}/\sqrt{2})$	-3
Triangle-wave	$V_{\text{DC}}\sqrt{3}$	$\log(V_{\text{DC}}\sqrt{3}/e)$	-3.9

Table 2-3: Output of log-amp detector for different input waveforms

2-3-4 Modulation Dependence

In this section the output of a log-amp detector for two modulation schemes is presented: Amplitude-Shift Keying (ASK) and Phase-Shift Keying (PSK). Both modulation schemes transmit at the same frequency and with the same bitsteam, as shown in Figure 2-15. First it is important to make sure that both modulations have the same RMS power level. The PSK is the simplest, because with the 180° phase shift the RMS does not differ from a regular sinusoidal signal. If a DC signal has an RMS of V_{DC}, $V_{\text{PSK}} = \sqrt{2}V_{\text{DC}}$.

[1] sgn(+)=1, sgn(-)=-1.

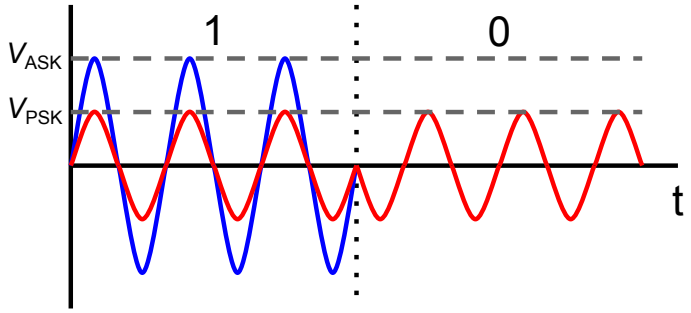


Figure 2-15: Representation of ASK and PSK modulation with equal RMS and bitstream

For the ASK the RMS calculation is similar to a normal sinusoid, except that under the root of (2-57) the value is only half as large:

$$\mathrm{RMS}_{\mathrm{ASK}} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} V_{\mathrm{ASK}}^2 \sin^2(x)dx} = \frac{V_{\mathrm{ASK}}}{2} = V_{\mathrm{DC}}, \tag{2-57}$$

thus $V_{\mathrm{ASK}} = 2V_{\mathrm{DC}}$.

Using the calculated V_{ASK} and V_{PSK} the effective output of the log-amp detector can now be calculated for both modulation schemes:

$$\begin{aligned}
\mathrm{AVG}(V_{\text{out-ASK}}) &= \frac{1}{2\pi}\int_0^{\pi} K_S \log\left(\frac{V_{\mathrm{ASK}}}{V_I}\right)dx \\
&= \frac{K_S}{2}\log\left(\frac{V_{\mathrm{ASK}}}{2V_I}\right) \\
&= K_S \log\left(\sqrt{\frac{V_{\mathrm{DC}}}{V_I}}\right), \qquad (2\text{-}58) \\
\mathrm{AVG}(V_{\text{out-PSK}}) &= K_S \log\left(\frac{V_{\mathrm{PSK}}}{2V_I}\right) \\
&= K_S \log\left(\frac{V_{\mathrm{DC}}}{\sqrt{2}V_I}\right). \qquad (2\text{-}59)
\end{aligned}$$

From (2-58) and (2-59) follows that the log-amp detector is modulation dependent given two signals with equal RMS, frequency and bitstream but with different modulation schemes.

2-4 Circuit Modeling

To obtain a model for the temperature behavior of the log-amp detector, the strong inversion CMOS equation is used:

$$I_D = \mu_n C_{\text{ox}} \frac{W}{L} (V_{\text{GS}} - V_{\text{th}})^2 \,, \tag{2-60}$$

where I_D is the drain current, μ_n is the charge-carrier effective mobility, C_{ox} the gate oxide capacitance, W and L the width and length of the gate respectively, V_{GS} the gate-source voltage and V_{TH} the threshold voltage.

Temperature dependent parameters in (2-60) are: the mobility μ_n, which decreases with temperature and V_{TH} which decreases with temperature as well. The mobility over temperature is given by [11]:

$$\mu_n(T) = \mu_{n0} \cdot \left(\frac{T}{T_{\text{ref}}} \right)^{-N_\mu}, \tag{2-61}$$

where T_{ref} the reference temperature (typically 300 K), μ_{n0} is the mobility at T_{ref} and $1.5 < N_\mu < 2$ [11] is the temperature coefficient of the mobility.

The V_{TH} over temperature can be approximated[2] to the first order by:

$$V_{\text{TH}}(T) = V_{\text{TH0}} \cdot [1 + TC_{\text{TH}}(T - T_{\text{ref}})], \tag{2-62}$$

where $-4 \times 10^{-3} \leq TC_{\text{TH}} \leq -0.5 \times 10^{-3}$[11] is the temperature coefficient of the threshold voltage and V_{TH0} the threshold voltage at T_{ref}.

2-4-1 Gain Cell

A circuit which can fulfill the function of a gain cell is the differential pair with load resistors shown in Figure 2-16. Cascading these differential pairs will form a log amp. The gain of a differential pair is given by [12]:

$$\begin{aligned} A(T) &= g_m(T) \cdot R_c(T) && (2\text{-}63) \\ &= \sqrt{\mu_n(T) C_{\text{ox}} \frac{W}{L} I_{\text{bias-A}}(T)} \cdot R_c(T), && (2\text{-}64) \end{aligned}$$

where $R_c(T)$ represent the load resistors and $I_{\text{bias-A}}$ is the bias current. The resistors $R_c(T)$ have a first-order temperature behaviour of:

$$R_c(T) = R_{c0} \cdot (1 + (T - T_{\text{ref}}) TC_{Rc}) \,, \tag{2-65}$$

where TC_{Rc} is the first-order temperature coefficient.

The threshold voltage V_{TH} does not appear in the equation of the small-signal gain (2-64), also when the body effect is included, due to equal V_{BS}. This means that only the temperature behavior of the mobility is important for the small-signal gain.

[2] Taylor approximation

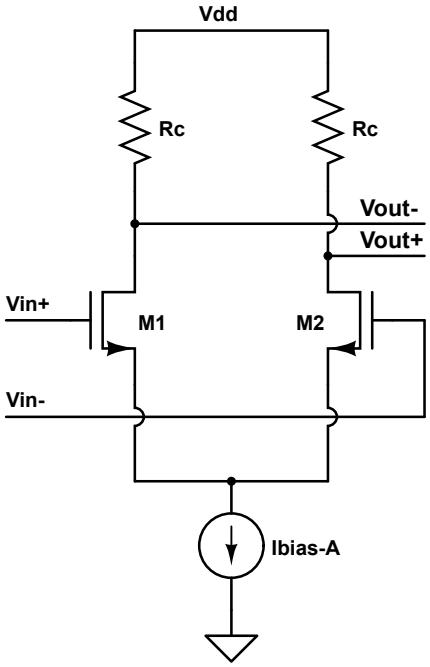


Figure 2-16: Circuit of CMOS differential pair

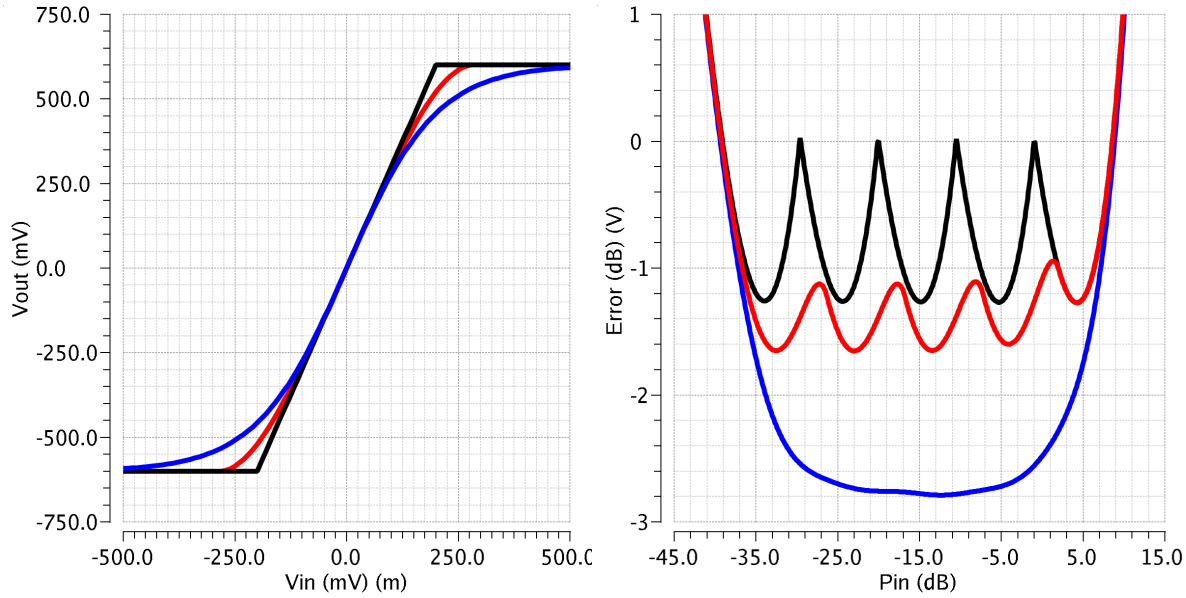
Knee voltage gain cell The knee voltage of the gain cell can be calculated in terms of the circuit parameters as:

$$\begin{aligned} \max(V_{\text{out-A}}) &= I_{\text{bias-A}} \cdot R_c\,, && \text{(2-66)} \\ E_{\text{kA}}(T) &= \frac{\max(V_{\text{out}})}{A} \\ &= \frac{I_{\text{bias-A}} \cdot R_c(T)}{\sqrt{\mu_n(T) C_{\text{ox}} \frac{W}{L} I_{\text{bias-A}}} \cdot R_c(T)} \\ &= \sqrt{\frac{I_{\text{bias-A}}}{\mu_n(T) C_{\text{ox}} \frac{W}{L}}}\,, && \text{(2-67)} \end{aligned}$$

which assumes a gain cell with an ideal transfer, with a constant gain up to the knee voltage. With real transistors however the small-signal gain reduces when the input deviates from zero, yielding a more smooth transfer characteristic. A new definition for the knee voltage is required.

Knee voltage definition The output of a gain cell made with transistors would have an output similar to the red or blue curve in Figure 2-17a. If the knee-voltage definition of (2-67) is applied, a weak-inversion model (hyperbolic tangent) would have an infinite knee voltage, which would translate to an infinite intercept point according to (2-41).

The LCE of a log amp with summation cells using three types of gain cells is shown in Figure 2-17b. In this figure it becomes clear that there is an intercept-point shift due to the smoother transfer of the gain cell. To get an approximation on the intercept-point shift, the smooth gain cell transfer is modeled as shown in Figure 2-18. The slope and intercept-point equations



(a) Output gain cell **(b)** LCE error plot

Figure 2-17: Log-amp output for different gain cells [black = ideal model, red = strong-inversion model, blue = weak-inversion model]

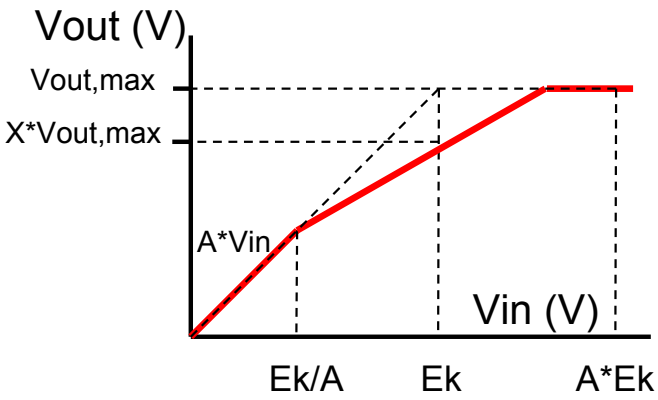


Figure 2-18: One-sided transfer of gain cell [$X \leq 1$]

for a log-amp detector with a smooth gain-cell transfer are defined by (see Appendix A-6 for a proof):

$$K_S = \frac{AE_{\mathrm{kA}}}{20\log(A)}, \tag{2-68}$$

$$V_I = \frac{E_{\mathrm{kA}}}{A^{(X-1)+N+1/(A-1)}}, \tag{2-69}$$

where X is the parameter which defines the smoothness of the gain-cell transfer. For values of $X < 1$ the intercept point will increase.

Another way to express the shift in the intercept point would be to define an effective knee

voltage, given by:

$$E_{\text{kA,eff}} = \frac{E_{\text{kA}}}{A^{X-1}}\,. \tag{2-70}$$

For $X = 1$ the knee voltage is unchanged, while for $X < 1$ the effective knee voltage will increase.

Another phenomena visible in Figure 2-17b is the "wobbles" in the LCE plot. For the weak-inversion model the LCE is nearly flat compared to the log amp with ideal gain cells. This is an advantage because in the "flat" region of the LCE curve, the errors from the ideal logarithm are much smaller.

For detector cells with a smooth transfer the intercept-point shift will also behave like (2-70), with E_{kA} replaced by E_{kD}) if $\max V_{\text{out-A}} > E_{\text{kD}}$. Smooth cells decrease the wobbles because they more replicate a logarithmic behaviour, a similar behaviour as explained in the beginning of this section, where different detector-cell types were discussed.

2-4-2 Detector Cell

The circuit of a detector cell is given in Figure 2-19. It is an NMOS version of the bipolar detector cell from [13]. Using the strong-inversion CMOS model of (2-60), the detector-cell

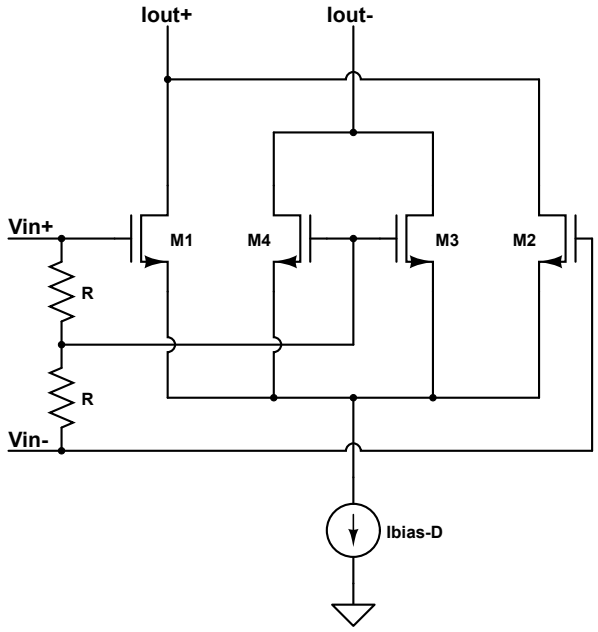


Figure 2-19: Circuit of a detector cell

transfer can be calculated as (see Appendix B-3):

$$I_{\text{out-D}}\ [A] = \begin{cases} \dfrac{\beta}{4} V_{\text{in-D}}^2, & \text{if } E_{\text{kD}} < V_{\text{in-D}}\,, \\ I_{\text{bias-D}}, & \text{if } E_{\text{kD}} \geq V_{\text{in-D}}\,. \end{cases} \tag{2-71}$$

Hence, the circuit of Figure 2-19 implements the X^2 detector cell.

Knee voltage detector cell The knee voltage can be calculated by equating row one and two of (2-71) with $V_{\text{in-D}} = E_{\text{kD}}$:

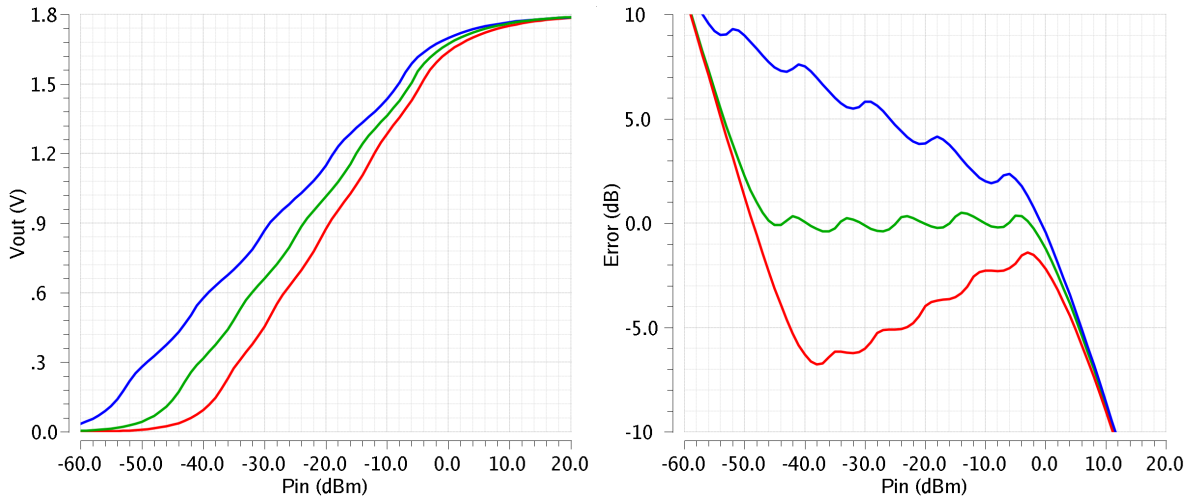
$$E_{\text{kD}} = \sqrt{\frac{4I_{\text{bias-D}}}{\beta(T)}}, \tag{2-72}$$

in which $\beta(T) = \mu_n(T)C_{\text{ox}}\frac{W}{L}$.

The detector-cell knee voltage is equivalent to the knee voltage of the gain cell, Equation 2-3.

2-4-3 Temperature Behavior of Log-Amp Detector

Assume a log-amp detector with: $N = 4$, $B_0 = 1.5$, $D_0 = 1$, $N_\mu = 1.7$, $TC_{Rc} = 0$ and with constant bias currents $I_{\text{bias-A}}$ and $I_{\text{bias-D}}$. The output of the log-amp detector over temperature is shown in Figure 2-20a.



(a) Output voltage versus input power

(b) Log-conformance error

Figure 2-20: Output of log-amp detector over temperature ($p = 2$). [blue = -40°C, green = 25°C and red = 85°C]

The gain over temperature can be modeled by (assume $A_0 = 3$, $235\,\text{K} \leq T \leq 385\,\text{K}$ and $T_{\text{ref}} = 300\,\text{K}$):

$$A(T) = A_0\left(\frac{T}{T_{\text{ref}}}\right)^{-0.85}, \tag{2-73}$$

$$\frac{\Delta A}{A} = \left(\frac{T}{T_{\text{ref}}}\right)^{-0.85} - 1\,. \tag{2-74}$$

Similarly, the knee voltage over temperature is modeled by:

$$E_{\text{kD}}(T) = E_{\text{kD0}}\left(\frac{T}{T_{\text{ref}}}\right)^{0.85}. \tag{2-75}$$

Calculating the intercept-point shift due to shift in knee voltage:

$$\Delta P_I(T) = 20\log\left(\frac{E_{\text{kD}}(T)}{A^{5.5}(T)}\right) - 20\log\left(\frac{E_{\text{kD0}}}{A_0^{5.5}}\right) \tag{2-76}$$

$$= 20\log\left(\frac{E_{\text{kD}}(T)\cdot A_0^{5.5}}{E_{\text{kD0}}\cdot A^{5.5}(T)}\right) \tag{2-77}$$

$$= 20\log\left[\left(\frac{T}{T_{\text{ref}}}\right)^{5.53}\right] = +8.8, -11.7 \text{ dB}, \tag{2-78}$$

which is close to the intercept-point shift from the simulation shown in Figure 2-20a.

Also the slope will be temperature dependent. By first calculating the derivative the slope temperature dependence can by calculated as:

$$K_S = \frac{I_{\text{bias-D}}R_{\text{out}}}{20\log(A)}, \tag{2-79}$$

$$\frac{\delta K_S}{\delta A} = -\frac{I_{\text{bias-D}}R_{\text{out}}\log(10)}{20A\ln^2(A)}, \tag{2-80}$$

$$\frac{\Delta K_S}{K_S}(T) = \frac{\Delta A}{A}(T)\cdot\frac{-1}{\ln(A)} = -21\,\%, +17\,\% \tag{2-81}$$

Hence, the slope over temperature will vary about ±20% with a constant bias current. Because the slope is the actual conversion parameter of the log-amp detector, this parameter should be as constant as possible.

The magnitude of log-conformance error in Figure 2-20b would require that every device needs calibration over temperature, significantly increasing the cost per chip. To achieve an acceptable log-conformance error within ±1 dB from -40 to +85°C, a temperature-compensation scheme is essential.

2-5 Proportional To Inverse Mobility (PTIM) Temperature Compensation

Constant-g_m biasing is a well known technique to make the trans-conductance of a CMOS transistor constant over temperature. The trans-conductance is given by [12]:

$$g_m(T) = \sqrt{2\beta(T)I_D}, \text{ in which} \tag{2-82}$$

$$\beta(T) = \mu_{n0}\left(\frac{T}{T_{\text{ref}}}\right)^{-N_\mu} C_{\text{ox}}\frac{W}{L} = \beta_0\left(\frac{T}{T_{\text{ref}}}\right)^{-N_\mu}, \tag{2-83}$$

where typically $1.5 < N_\mu < 2$.

Because $\beta(T)$ has the same temperature dependence as the mobility given by Equation 2-61, I_{bias} can be made:

$$I_{\text{bias}}(T)_{\text{constant-gm}} = I_{\text{bias0}}\left(\frac{T}{T_{\text{ref}}}\right)^{N_\mu}, \tag{2-84}$$

such that g_m follows as:

$$\begin{aligned} g_m(T) &= \sqrt{\beta_0 \left(\frac{T}{T_{\text{ref}}}\right)^{-N_\mu} I_{\text{bias0}} \left(\frac{T}{T_{\text{ref}}}\right)^{N_\mu}} \\ &= \sqrt{\beta_0 I_{\text{bias0}}}, \end{aligned} \tag{2-85}$$

which is temperature independent. This type of biasing is called proportional to inverse mobility (PTIM) because the bias current is inversely proportional to the mobility temperature dependence.

2-5-1 Gain Cell

Gain temperature compensation As shown in the previous section the gain of a differential pair with load resistors is:

$$A(T) = \sqrt{\beta(T) I_{\text{bias-A}}(T)} R_c(T),$$

in which $\beta(T) = \beta_0 (\frac{T}{T_{\text{ref}}})^{-N_\mu}$ as before. Let's assume the PTIM bias current to be:

$$I_{\text{bias-A}}(T)_{\text{PTIM}} = \frac{X_{0\text{A}}}{R_c^2(T)\beta(T)}, \tag{2-86}$$

in which $X_{0\text{A}}$ is a unit-less quantity. The gain can now be rewritten as:

$$\begin{aligned} A(T) &= \sqrt{\beta(T) \frac{X_{0\text{A}}}{R_c^2(T)\beta(T)}} R_c(T)\,, \\ &= \sqrt{X_{0\text{A}}}, \end{aligned} \tag{2-87}$$

which is constant over temperature. The PTIM bias current of Equation 2-86 has both the inverse temperature dependence of the mobility, as well as the inverse squared temperature dependence of the resistor to achieve temperature independence.

Knee voltage shift With the PTIM current of (2-86) the knee voltage from (2-3) can be rewritten as:

$$\begin{aligned} E_{\text{kA}} &= \sqrt{\frac{I_{\text{bias-A}}(T)}{\beta(T)}} \\ &= \sqrt{\frac{X_{0\text{A}}}{R_c^2(T)\beta(T)\beta(T)}} \\ &= \frac{\sqrt{X_{0\text{A}}}}{R_c(T)\beta(T)}\,, \end{aligned} \tag{2-88}$$

yielding a knee voltage which is dependent on temperature. This temperature dependence will be removed in Section 2-5.

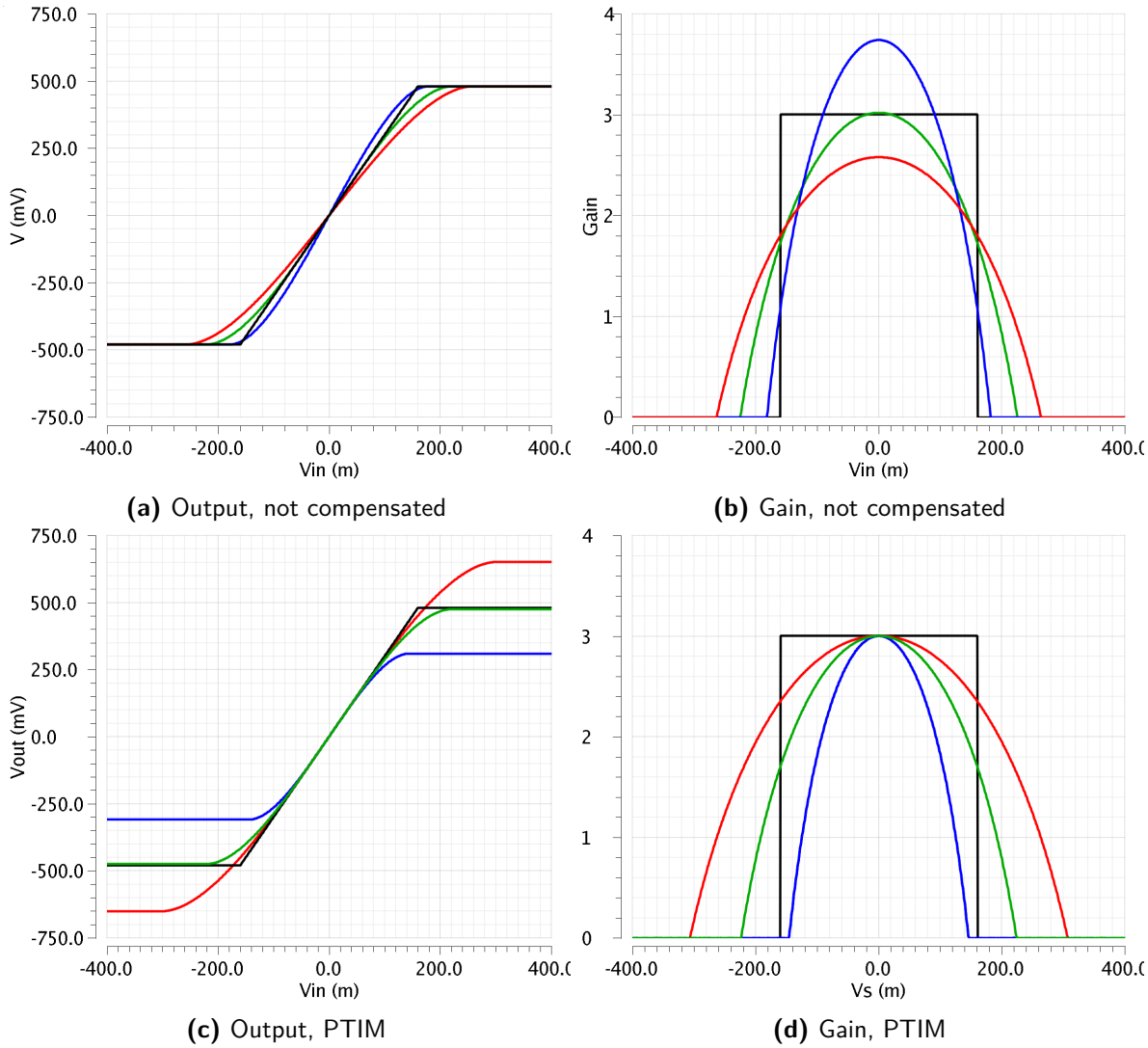
Maximum output The voltage swing of the differential pair is given by $\max(V_{\text{out-A}}) = I_{\text{bias-A}} R_c$:

$$\max(V_{\text{out-A}})(T) = \frac{X_{0\text{A}}}{R_c(T)\beta(T)}\,, \tag{2-89}$$

which is now also dependent on temperature.

Transfer and gain over temperature The following figures will show the gain cell transfer at three different temperatures with:

- Constant bias current $I_{\text{bias-A}}$ (Figures 2-21a and 2-21b)
- PTIM bias current $I_{\text{bias-A}}$ (Figure 2-21c and 2-21d)



(a) Output, not compensated

(b) Gain, not compensated

(c) Output, PTIM

(d) Gain, PTIM

Figure 2-21: Output and gain of gain cell over temperature [blue = -40°C, green = 25°C, red = 85°C, black = ideal transfer]

2-5-2 Detector Cell

From the last section it became clear that for the detector cells two properties are important: knee voltage E_{kD} and $I_{\text{bias-D}}$.

Knee voltage Assuming the same PTIM bias current as used for the gain cell (Equation 2-86), the knee voltage will be:

$$I_{\text{bias-D}}(T)_{\text{PTIM}} = \frac{X_{0\text{D}}}{R_c^2(T)\beta(T)}, \tag{2-90}$$

$$\begin{aligned} E_{\text{kD}}(T) &= 2\sqrt{\frac{I_{\text{bias-D}}(T)}{\beta(T)}}, \\ &= \frac{\sqrt{X_{0\text{D}}}}{R_c(T)\beta(T)}, \end{aligned} \tag{2-91}$$

which is equivalent to the knee voltage temperature shift of the gain cell. This means that both knee voltages will shift equal over temperature given the same bias current, keeping the relation $\max(V_{\text{out-A}}) > E_{\text{kD}}$ valid.

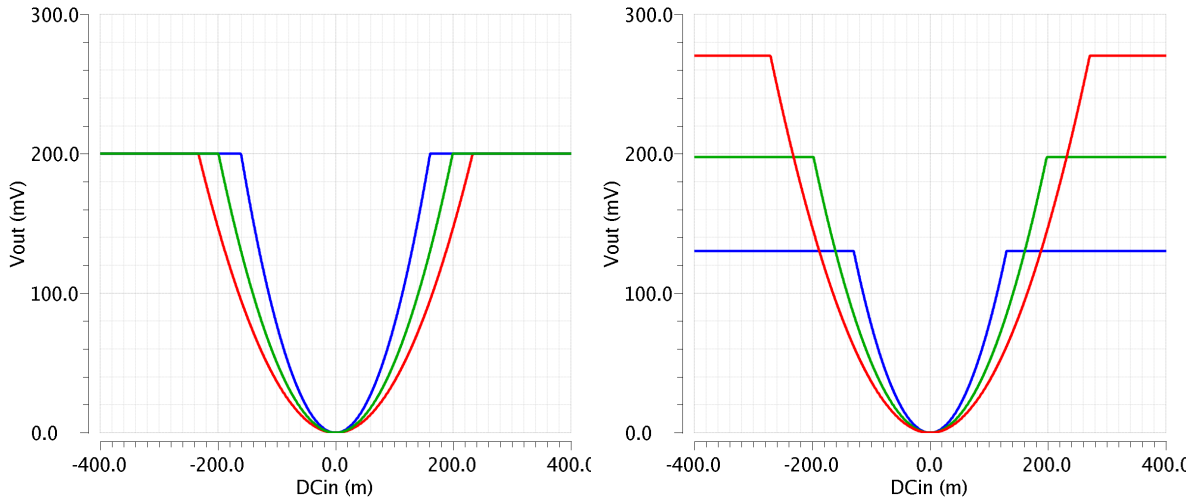
Maximum output current The bias current is the maximum output current of the detector cell, given by:

$$\max(I_{\text{out-D}})(T) = \frac{I_{\text{bias-D}}}{(R_c(T)/R_c)^2} \cdot \left(\frac{T}{T_{\text{ref}}}\right)^{N_\mu}. \tag{2-92}$$

The following figures will show the detector-cell transfer at three different temperatures with:

- No compensation (Figure 2-22a)
- PTIM bias current (Figure 2-22b)

From Figure 2-22a and Figure 2-22b it seems that the PTIM bias current does not help to make the detector-cell transfer more temperature independent. However, its purpose will be made clear in the next section.



(a) Output, no compensation **(b)** Output, PTIM

Figure 2-22: Output of detector cell over temperature [blue = -40°C, green = 25°C, red = 85°C]

2-5-3 PTIM Architecture

Intercept-point shifter To cope with the knee-voltage shift of E_{kA} and E_{kD} as seen in Figures 2-21c and 2-22b, an input scaler, with transfer $S(T)$, is put in front of the log-amp detector. The intercept point over temperature is given by:

$$V_I(T) = \frac{E_{\mathrm{kD}}(T)}{A^{N-1+B_0+D_0} \cdot S(T)}, \text{ where} \tag{2-93}$$

$$S(T) = \frac{S_0}{\beta(T) R_c(T)}, \tag{2-94}$$

where $1.5 \leq N_\mu \leq 2$. Substituting (2-91) into (2-93) yields:

$$V_I(T) = \frac{\sqrt{X_{0\mathrm{D}}}}{S_0 \cdot A^{N-1+B_0+D_0}}, \tag{2-95}$$

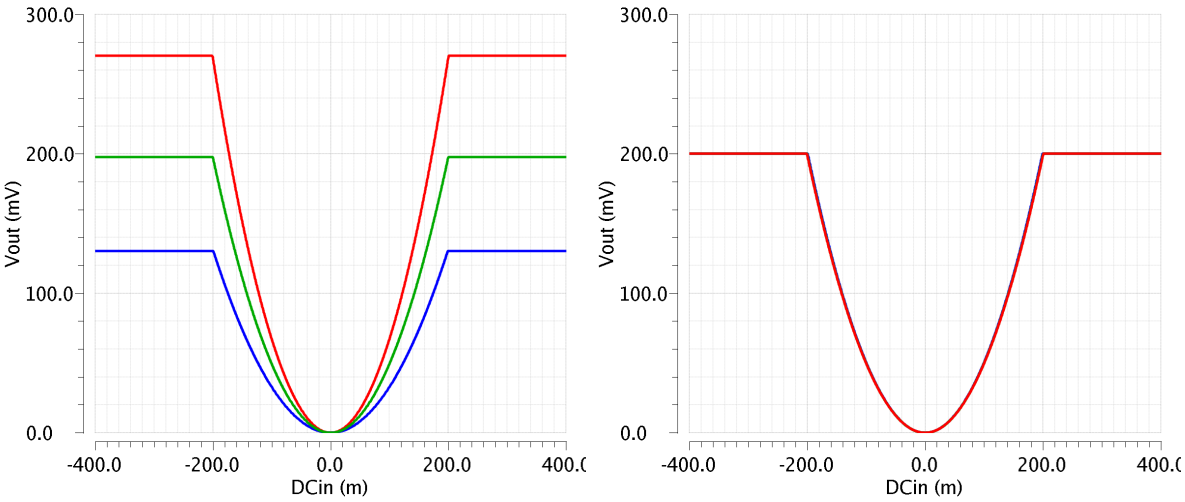
which is temperature independent. So because the knee voltages shift with PTIM, it is possible to change the whole gain of the log amp to become proportional to PTIM as well. The temperature components will drop out, yielding an intercept point which is temperature independent. See Figure 2-23a.

Current scaler As the detectors will have a current output, their maximum output current is equal to their bias current, $I_{\text{bias-D}}$. The output current of all detector cells is given by $I_{\mathrm{det}}(T)$, which also has a PTIM temperature dependence. Using a PTM (proportional to mobility) scaler block after the log-amp core can remove the current dependence:

$$I_{\text{out-const}} = I_{\text{det-ptim}}(T) \frac{I_{\mathrm{const}}}{I_{\mathrm{ptim}}(T)}, \tag{2-96}$$

where I_{const} is a current generated from a band-gap voltage over a resistor of type R_c. The output voltage of the log-amp detector will be $I_{\text{out-const}}$ over a R_c resistor, yielding a temperature independent output voltage. The output of a detector cell with the above described input and output compensation is depicted in Figure 2-23b. From this figure it is clear that the detector-cell output is temperature independent if both scalers are applied.

Block diagram Adding both scalers to the log-amp detector yields the block diagram of the PTIM temperature scheme as shown in Figure 2-24.



(a) Transfer with input scaler **(b)** Transfer with input and output scaler

Figure 2-23: Transfer of detector cell over temperature with PTIM bias current [blue = -40°C, green = 25°C, red = 85°C]

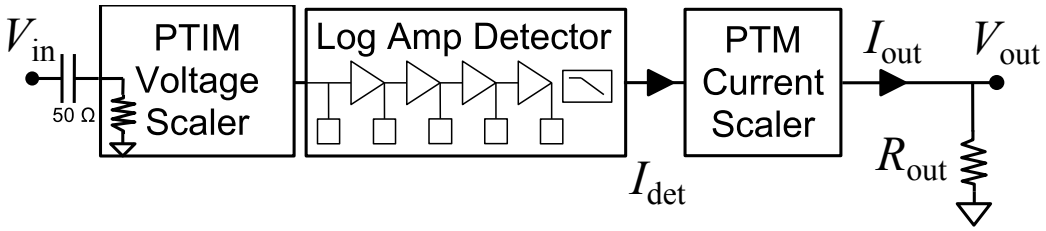


Figure 2-24: Block diagram of complete temperature compensation scheme

Chapter 3

Circuit Design

This chapter contains the most important design decisions, circuit block simulations and schematics of the final CMOS log-amp detector design. The first section will describe the overall block diagram, followed by sections and subsections containing the information for each sub-block. The final section calculates the expected slope, intercept and pedestal level of the log-amp detector.

3-1 Block Diagram

The total block diagram of the CMOS log-amp detector using the Proportional To Inverse Mobility (PTIM) bias scheme, described in Section 2-5, is given in Figure 3-1. The core functionality is located inside the log-amp core block. A look inside this block is given in Figure 3-2 and discussed in Section 3-2.

Finally, the DC current output of the log-amp core (I_{det}) is processed by the back-end, the inner block diagram of which is given in Figure 3-3 and will be further discussed in Section 3-4.

List of all major blocks:

- Log-Amp Core (Section 3-2)
  - RF Input Block (Section 3-2-1)
  - RF Front-End (Section 3-2-4)
  - Gain Cell, A (Section 3-2-2)
  - Detector Cell, D (Section 3-2-3)
- Bias Blocks (Section 3-3)
  - Bias Block A (Section 3-3-1)
  - Bias Block D (Section 3-3-2)
- Back-End (Section 3-4)
  - Differential Current to Single-Ended Current Conversion (Section 3-4-1)
  - Current Scaler (Section 3-4-2)
  - Bandgap (Section 3-4-3)
  - Current to Voltage Buffer (Section 3-4-4)

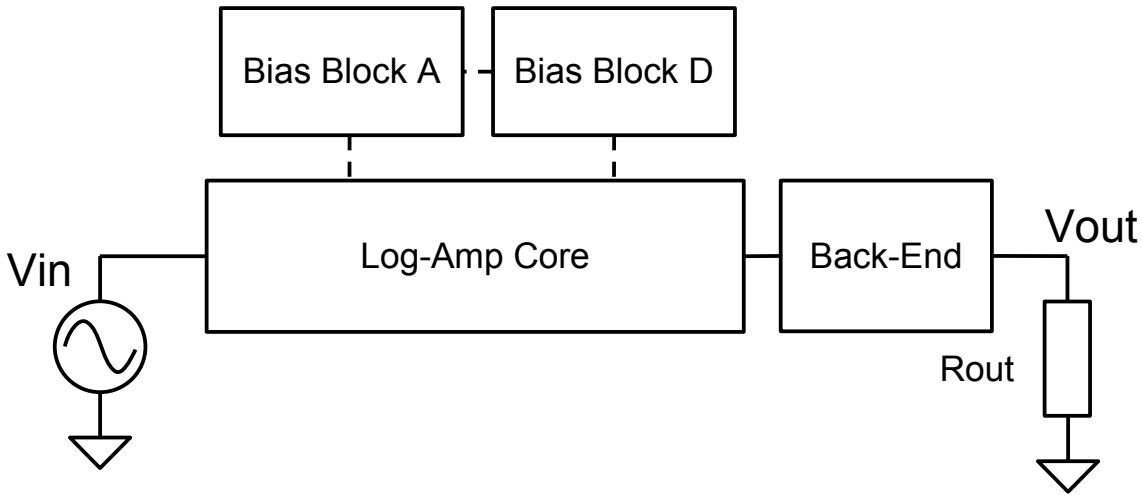


Figure 3-1: Complete block diagram of log-amp detector

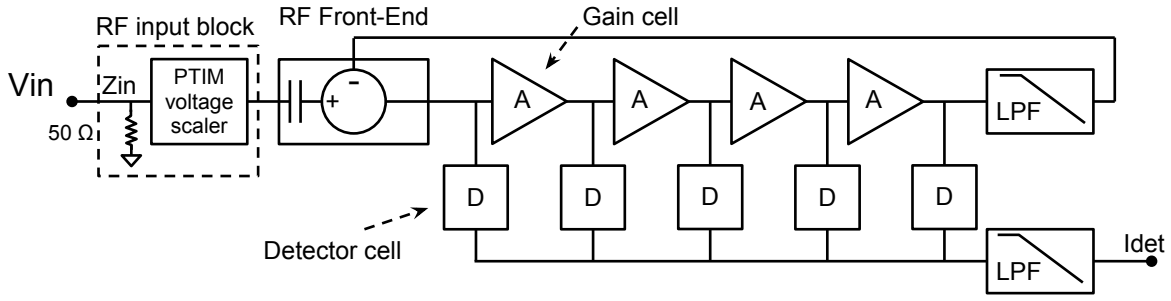


Figure 3-2: Block diagram of log-amp core from Figure 3-1

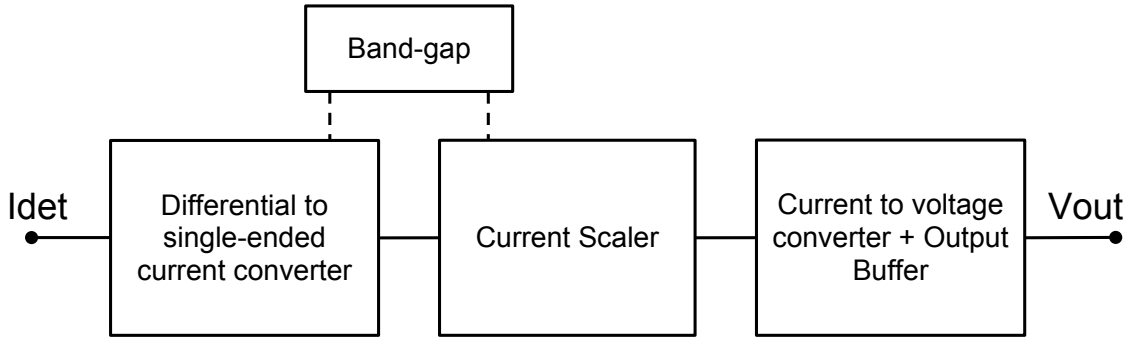


Figure 3-3: Block diagram of back-end from Figure 3-1

3-2 Log-Amp Core

3-2-1 RF Input Block

Function The function of the RF input block is to stabilize the intercept shift over temperature by approximating the PTIM temperature behavior as explained in Section 2-5. It also provides the 50 Ω input impedance which is needed to match the characteristic impedance of the coupler, see Chapter 1.

Implementation A simple circuit which fulfills these functions is depicted in Figure 3-4. From Chapter 2, the transfer of the resistor divider should be proportional to a PTIM temperature dependence:

$$S(T) = \frac{S_0}{\beta(T)R_c(T)}, \tag{3-1}$$

which is equal to the voltage temperature dependence over an $R_c(T)$ resistor biased with $I_{\text{bias-D}}$. The first-order Temperature Coefficient (TC) of (3-1) will be approximated using the available resistors in the process.

Inside the given technology, a resistor with the highest positive TC was not high enough to match the first-order TC of (3-1). By combining a positive and a negative TC resistor, the effective positive TC was increased. In the circuit of Figure 3-4 these resistors are displayed as resistor R_p with TC_p and resistor R_n with TC_n.

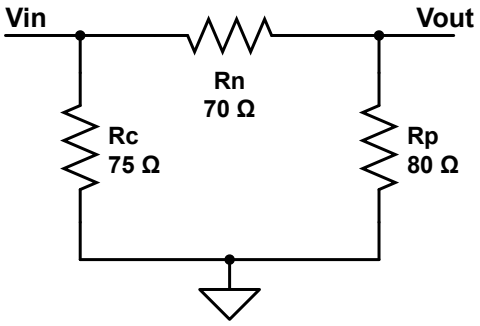


Figure 3-4: Schematic of RF input block from Figure 3-1

The transfer of the RF input block over temperature is calculated using:

$$R_p(T) = R_{p0} \cdot (1 + (T - T_{\text{ref}})TC_p)\,, \tag{3-2}$$

$$R_n(T) = R_{n0} \cdot (1 + (T - T_{\text{ref}})TC_n)\,, \tag{3-3}$$

substituting these in the transfer equation of:

$$V_{\text{out}} = V_{\text{in}} \cdot \frac{R_p}{R_p + R_n}\,, \tag{3-4}$$

yields a transfer over temperature given by:

$$V_{\text{out}}(T) = RF_{\text{in}} \cdot \frac{R_p(1 + (T - T_{\text{ref}})TC_p)}{R_p + R_n + (T - T_{\text{ref}})(R_pTC_p + R_nTC_n)}\,. \tag{3-5}$$

The first-order TC at $T = T_{\text{ref}}$ of this transfer is (see Appendix B-1):

$$TC_{\text{eff}}(T = T_{\text{ref}}) = \frac{R_p R_n (TC_p - TC_n)}{(R_p + R_n)^2}. \tag{3-6}$$

From (3-6), the combined temperature behavior of both resistors results in a higher positive TC. With the resistor values R_{p0} and R_{n0} of Figure 3-4 the effective TC can be decreased to match the temperature behavior of PTIM.

In the final design $R_p = 80\,\Omega$ and $R_n = 70\,\Omega$ such that the input impedance is kept at $50\,\Omega$. The R_c resistor is the best resistor in the given technology with: best matching, lowest temperature coefficients (TC1 and TC2) and lowest parasitic capacitance.

Maximum RF input current The PTIM voltage scaler is the first block which deals with the RF input signal. The measurement equipment is able to drive up to +20 dBm of input power, which is equivalent to a current of $I_{\text{RMS}} = 45$ mA. This means that the resistors in the layout should be wide enough to be able to withstand the large current flow. The total active area of the RF input block is thus relatively large with 136 μm x 180 μm.

Matching Table 3-1 shows two types of resistors errors: Absolute error due to random variation in area and changes in the sheet resistance due to process variations. Process

Resistor	$\left(\frac{\Delta R}{R}\right)_{3\sigma}$	Slow	Typical	Fast
R_n	$\pm 0.25\,\%$	$77\,\Omega$	$70\,\Omega$	$63\,\Omega$
R_p	$\pm 0.06\,\%$	$85\,\Omega$	$80\,\Omega$	$75\,\Omega$
R_c	$\pm 0.01\,\%$	$78\,\Omega$	$75\,\Omega$	$72\,\Omega$
Z_{in}		$47\,\Omega$	$50\,\Omega$	$53\,\Omega$

Table 3-1: Resistor value variation in RF input block

variations across corners however, are relatively high because three different types of resistors are used in the design. These three resistors are each made with a different mask, thus any combination of process corners is possible.

The worst case input impedance variation due to process variation is: $47\,\Omega \leq Z_{\text{in}} \leq 53\,\Omega$. This variation will produce an intercept shift from batch to batch of about $\pm\,0.27$ dB across the extreme corners (see Appendix B-1).

Temperature behavior For the given process the sheet resistance changes over corners, not the actual temperature coefficients. The effective TC_{eff} of the scaler changes however due to the absolute resistance of the resistors in the resistor divider.

The first-order TCs of $V_{\text{out}}(T)$ and $R_c(T)I_{\text{bias-D}}(T)$ are compared in Table 3-2.

Figure 3-5 compares $V_{\text{out}}(T)$ and $R_c(T)I_{\text{bias-D}}$ over temperature normalized to 25°C. By matching only the first-order TC the second-order TC would be responsible for a large overall temperature error. By scaling the absolute resistor values R_{p0} and R_{n0} for the complete temperature range[1], the overall temperature error was reduced significantly.

[1] Temperature ranging from -40 to 85°C.

Corner	TC1 bias detector	TC1 input scaler
slow	2.77×10^{-3}	3.08×10^{-3}
typical	2.80×10^{-3}	3.04×10^{-3}
fast	2.85×10^{-3}	2.99×10^{-3}

Table 3-2: First-order temperature coefficients of bias block D versus the input scaler at 25°C and across process corners

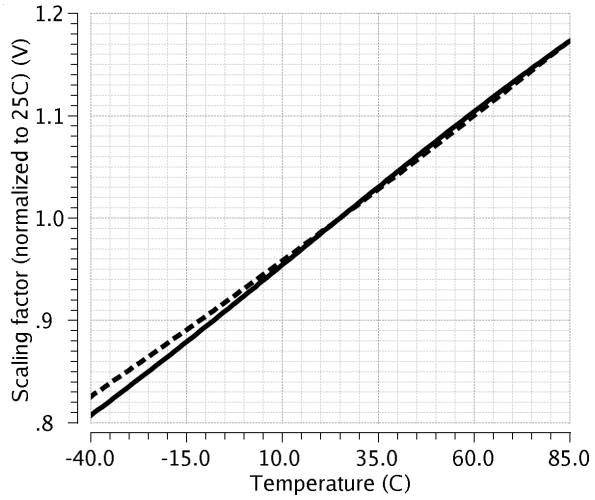


Figure 3-5: Transfer of RF input block and bias block D over temperature, normalized to 25°C [solid = RF input scaler, dotted = bias block D]

Noise The output noise can be calculated by terminating the input with 50 Ω impedance and looking at the output impedance:

$$Z_{\text{out}} = ((50||75) + 70)||80 = 44\,\Omega,$$

$$\overline{V_{\text{n,out}}^2} = 4kTR = 178kT\,\frac{\text{V}^2}{\text{Hz}}, \tag{3-7}$$

the effect of this noise source will be further investigated in Section 3-5-3.

Bandwidth Because the RF input scaler is located before the active RF circuitry, its bandwidth should not dominate the overall bandwidth. Although the sizes of the resistors are relatively large, the low impedances to ground inside the circuit result in a high bandwidth. The extracted (C-only) BW is plotted in Figure 3-6. The BW is large enough such that at 10 GHz the intercept point will shift only 0.5 dB. According to Section 3-2-2 the -3 dB bandwidth of the gain cell is around 2 GHz BW. Thus the RF input scaler will not be dominant in terms of Bandwidth (BW).

3-2-2 Gain Cell

Function The function of the gain cell is to provide a constant gain over temperature, with maximum bandwidth, as described in Chapter 2.

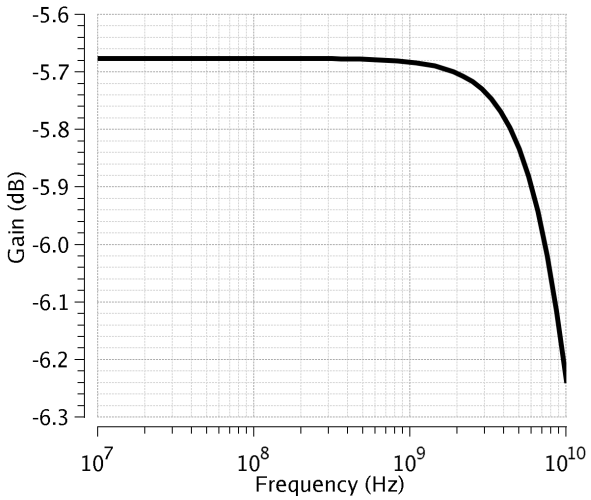


Figure 3-6: Bandwidth response of RF input block up to 10 GHz

Implementation As suggested in Chapter 2 the gain cells comprise a differential pair, as shown in Figure 3-7. To be able to cascade the gain cells[2], a voltage follower was needed. This part of the gain cell levels down the common-mode voltage of the output to properly bias the input of the next gain cell at a common-mode which does not limit the output swing of the gain cell.

An open-loop system was chosen because this topology is preferable for achieving a small gain with a maximum bandwidth. Differential input circuit are used in the complete RF core to reject common-mode interference coming from the rest of the chip.

A normal voltage follower with bulk to ground connection proved to be problematic due to the body effect. The substantial increase in V_{th} would limit the drain-source voltage of the current source in the next gain cell, squeezing it out of saturation. In the given CMOS 0.18 μm process isolated NMOS devices were available, which do not suffer from the body effect[3] and therefore leave more voltage headroom for the next gain cell.

On top of the input devices, cascodes are used mainly to increase the output impedance which slightly increased the gain due to the finite output impedance. For the same gain and current this resulted in slightly larger bandwidth, at the cost of maximum output voltage swing.

Given the specifications as mentioned in Chapter 1, the total dynamic range for the log-amp detector should be $\geq$30 dB. The total gain of the cascaded gain cells is the gain at which the input should increase from the first detector-cell knee voltage, to the last. If four gain stages would be used with each around 10 dB of gain, a theoretical maximum of 40 dB dynamic range should be possible.

The maximum output swing of the gain cell should be large enough to be able to steer most of the output current of the detector cell and to adhere to $\max(V_{\text{out-A}}) > E_{\text{kD}}$. With an maximum voltage output swing of 380 mV, 88% of the detector cells output current can be reached. A higher voltage swing would increase the current consumption for the same

[2]As discussed in Chapter 2 the gain cells will be cascaded to form a log-amp.
[3]In a isolated NMOS the bulk always is connected directly to its source, eliminating the body effect.

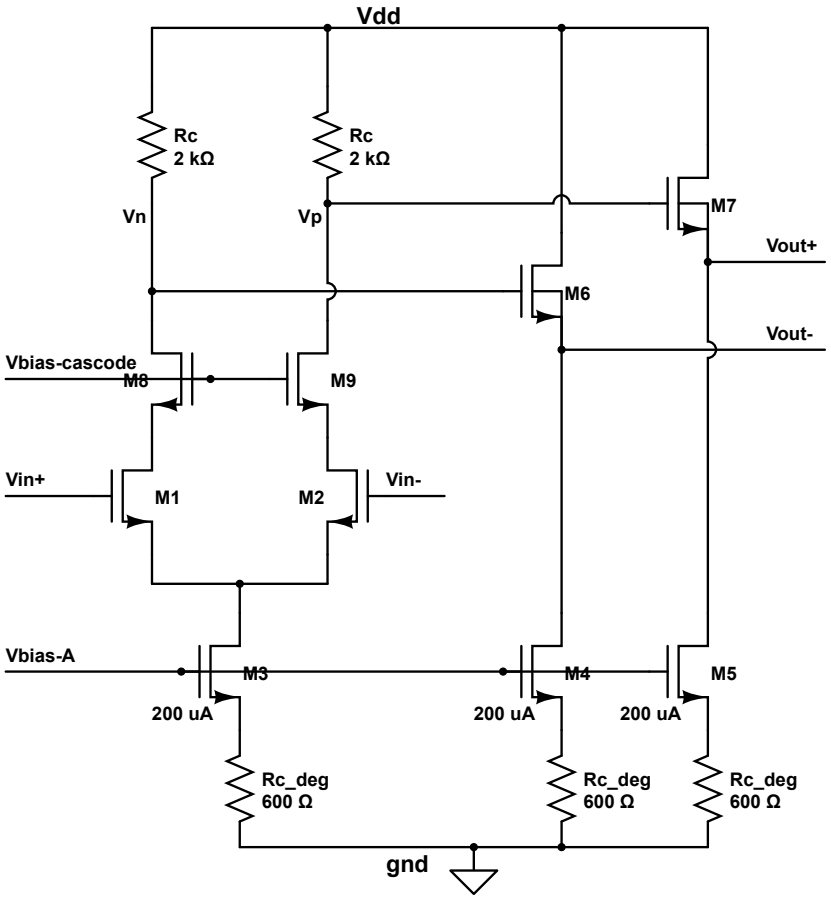


Figure 3-7: Schematic of the gain cell

bandwidth and bias conditions. The common-mode input/output voltage is 1 V, leaving enough voltage headroom for the current sources M3, M4 and M5 with source degeneration.

Bandwidth To achieve the highest bandwidth given the technology, the gate length is set to 0.18 μm for the input transistors (M1 and M2) and the voltage followers (M6, M7). To estimate the effective bandwidth it is first important to identify the nodes that will limit the performance. In Figure 3-7 the nodes R_p and R_n have a relatively high impedance to ground and high capacitive loading from the isolated NMOS. Also the output nodes $V_{\text{out}+}$ and $V_{\text{out}-}$ have a high capacitive loading due to the isolated NMOS devices and the input capacitance of both gain cell plus detector cell. To model the bandwidth capacitors C_1 and C_2 represent the total load capacitance at these nodes. For an explanation on the origin of C_1 and C_2 see Appendix B-2. The total transfer is given by[4] (see appendix for calculation):

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{g_{\text{m1}} R_c}{(1 + sC_1R_c)(1 + sC_2/g_{\text{m6}})}, \tag{3-8}$$

in which the trans-conductance of the isolated NMOS, g_{m6} equals $3.8{\times}10^{-3}$ [A/V], C_1 is the capacitance at the nodes V_p/V_n, and C_2 is the capacitance at the output. Transistors M8 and

[4]The transfer assumes infinite output impedance's of the devices.

M9 limit the Miller effect of $C_{\mathrm{GD1,2}}$ because the gain of M1/M2 from gate to drain is only -1 due to the cascoding. With a gain of 10 dB the cascodes reduce the Miller effect of $C_{\mathrm{GD1,2}}$ by a factor two. This effect is however relatively small: $C_{\mathrm{GD1,2}}$ only equals 8.5 fF and is thus relatively small compared to C_2.

$$\begin{aligned} C_1 &= 45\,\mathrm{fF} \\ C_2 &= 252\,\mathrm{fF} \end{aligned}$$

The capacitances at these two nodes, together with the impedances to ground yield two poles:

$$\begin{aligned} f_{\mathrm{p1}} &= \frac{1}{2\pi R_c C_1} \\ &= 1.77 \times 10^9\ \mathrm{Hz}\,, \end{aligned} \tag{3-9}$$

$$\begin{aligned} f_{\mathrm{p2}} &= \frac{g_{\mathrm{m6}}}{2\pi C_1} \\ &= 2.4 \times 10^9\ \mathrm{Hz}\,. \end{aligned} \tag{3-10}$$

From (3-9) and (3-10) both poles have around the same bandwidth. In the circuit of the gain cell each current source pulls 200 μA. This current distribution inside the gain-cell circuit is close to the optimal distribution because the bandwidth is always limited by the most dominant node.

Using a small-signal AC simulation, the extracted parasitic capacitance bandwidth of the gain cell loaded at the input and output with a gain and detector cell is given in Figure 3-8. In this figure the extracted BW in the simulation is a bit faster than the schematic BW thanks to optimization[5] of the layouts of the isolated-NMOS devices M6/ M7 of Figure 3-7.

Comparing the simulation result of Figure 3-8 with the poles f_{p1} and f_{p2} shows that the calculation accurately predicts the simulation result.

Gain over temperature The PTIM bias current discussed in Section 2-5 is generated in the circuit of Section 3-3-1, which keeps the gain constant over temperature:

$$I_{\text{bias-A}}(T)_{\mathrm{PTIM}} = \frac{X_{0\mathrm{A}}}{\beta(T) R_c^2(T)}. \tag{3-11}$$

In Figure 3-9 the small-signal gain is simulated at 100 MHz over temperature for three process corners, which show that the gain error over temperature is restricted to $\leq$0.1 dB.

The slope and intercept-point equations, shown in Chapter 2, indicate that a gain variation will most dominantly effect the intercept point:

$$V_I = \frac{E_{\mathrm{kD}}}{A^5}, \tag{3-12}$$

$$\left|\frac{\Delta V_I}{V_I}\right| = 5\left|\frac{\Delta A}{A}\right|, \tag{3-13}$$

$$\Delta P_I = 0.5\ \mathrm{dB}, \tag{3-14}$$

thus the intercept error for each process corner over the temperature range is $\leq$0.5 dB.

[5] Substantial reduction in deep n-well area.

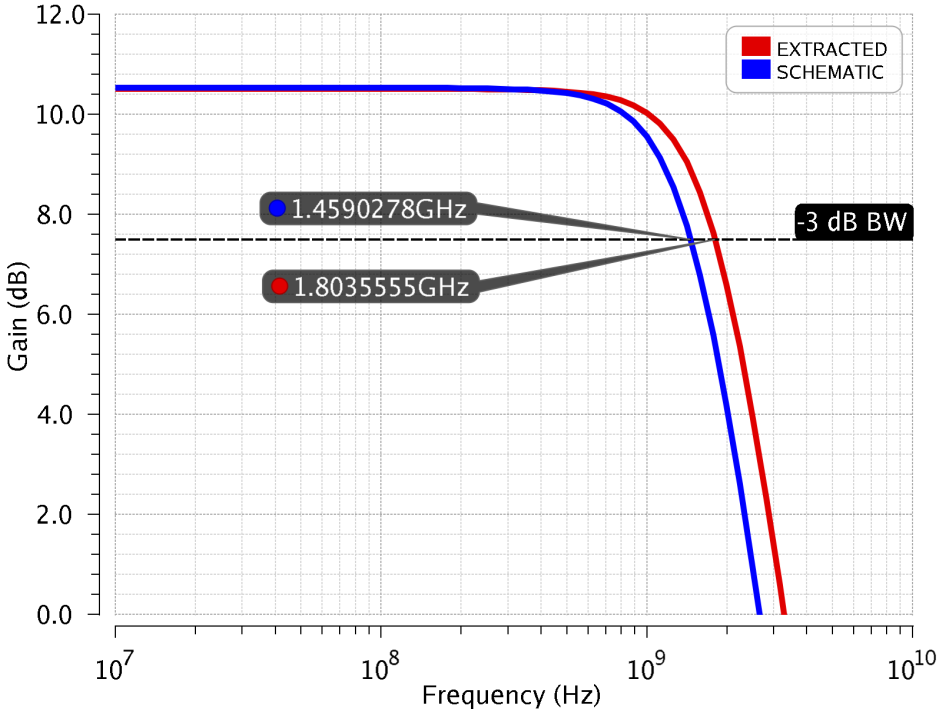


Figure 3-8: Bandwidth of the gain cell at the typical corner

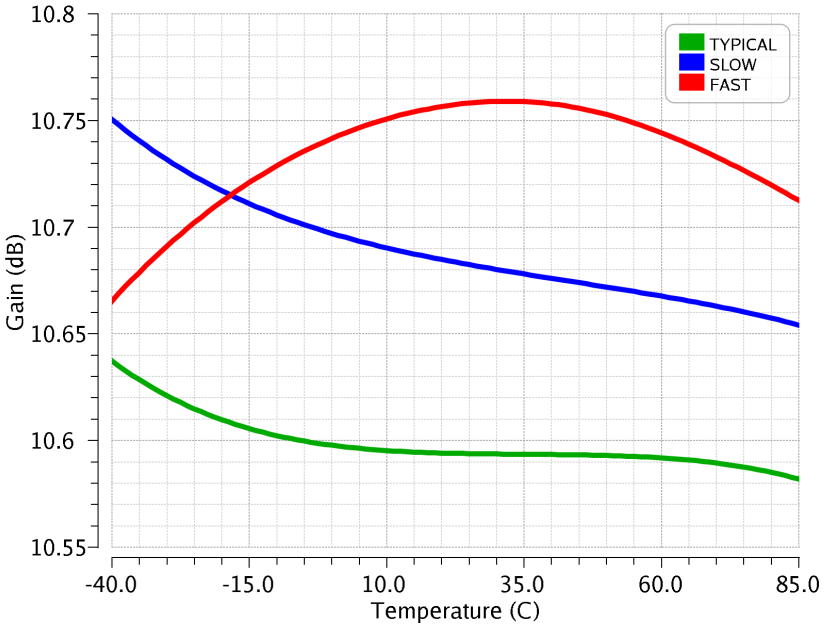


Figure 3-9: Gain of gain cell over temperature [corner: slow = blue, typical = green, fast = red]

Input offset Because the input transistors are made relatively small to achieve high BW, they will have a significant mismatch. This can be problematic in an open-loop system with a high gain (40 dB in this design), because an input offset of a couple of millivolts in the

first gain cell can clip the last couple of stages. If this occurs, part of the channel will not be usable, limiting the dynamic range significantly. To prevent this phenomena an input-offset cancellation loop is used as described in Section 3-2-4.

Equation 3-15 describes the offset as a function of the gate area WL of the transistor and the Pelgrom constant A_{Vth}, a process dependent offset parameter [14]. The input transistors of the differential pair are biased close to zero overdrive voltage, to efficiently use the limited voltage headroom of the 1.8 V supply. Therefore, the threshold-voltage variation is assumed to be dominant in output current offset.

$$(\Delta V_{\mathrm{TH}})_{\sigma} = \frac{A_{\mathrm{Vth}}}{\sqrt{WL}} \tag{3-15}$$

Using this formula the $(\Delta V_{\mathrm{input,OS}})_{3\sigma} = 7$ mV, which was confirmed with a DC match simulation[6], which yielded a $(\Delta V_{\mathrm{input,OS}})_{3\sigma} = 8$ mV for the input devices. Caution is advised with using the Pelgrom constant in this condition, because the layout is done with bandwidth in mind. The transistor pairs that are considered are relatively far apart and no matching geometries are used for both the gain cells and detector cells. The layout of these cells was arranged to minimize parasitic capacitance, not to minimize offset. Therefore, it is preferable to have some margin on the amount of steering capability of the offset cancellation loop, which will be discussed in Section 3-2-4.

Gain cell to gain cell mismatch The matching of the current sources from gain cell to gain cell is of importance as well. Different tail currents $I_{\text{bias-A}}$ will result in a different gain A for each gain cell:

$$A = \sqrt{\beta_0 I_{\text{bias-A}}} \cdot R_c \,,$$

taking the first-order derivative over the bias current for: $(\Delta I_{\text{bias-A}})_{3\sigma} = 5.3\,\mu A$[7], $I_{\text{bias-A}} = 200\,\mu$A, $\beta_0 = 0.0125\,A^{-1}\Omega^{-2}$ and $R_c = 2\,\mathrm{k}\Omega$ yields:

$$(\Delta A)_{3\sigma} = \Delta I_{\text{bias-A}} \cdot \frac{R_c\sqrt{\beta_0}}{2\sqrt{I_{\text{bias-A}}}} = \pm 0.04 = \pm 1.3\% \,. \tag{3-16}$$

Comparing this to Figure 3-10 where multiple Verilog-A simulations show the effect of gain errors between gain cells: ±5%, ±10%, ±20%. This plot gives an understanding in how much gain error between gain cells is allowed for a certain log-conformance error. Gain errors less than 5% translate to log-conformance errors $<<$ 0.5 dB, which can be neglected.

Noise The dominant noise sources of the gain cell are the input transistors as well as the voltage followers. All noise at the input of the channel will be amplified by the channel over the complete bandwidth and converted to DC by the detector cells, rendering thermal noise as the dominant noise source. Base-band signals out of the rightmost gain cell experience feedback to the input of the channel via the offset-cancellation loop. Therefore, the effect of 1/f noise is reduced by the loop gain.

The thermal noise of a MOS device is given by [12]:

$$\overline{I_n^2} = 4kT\gamma g_{\mathrm{do}}, \tag{3-17}$$

[6] Simulation that calculates the input referred offset using statistical device models.
[7] Based on a DC match simulation, see appendix B-2.

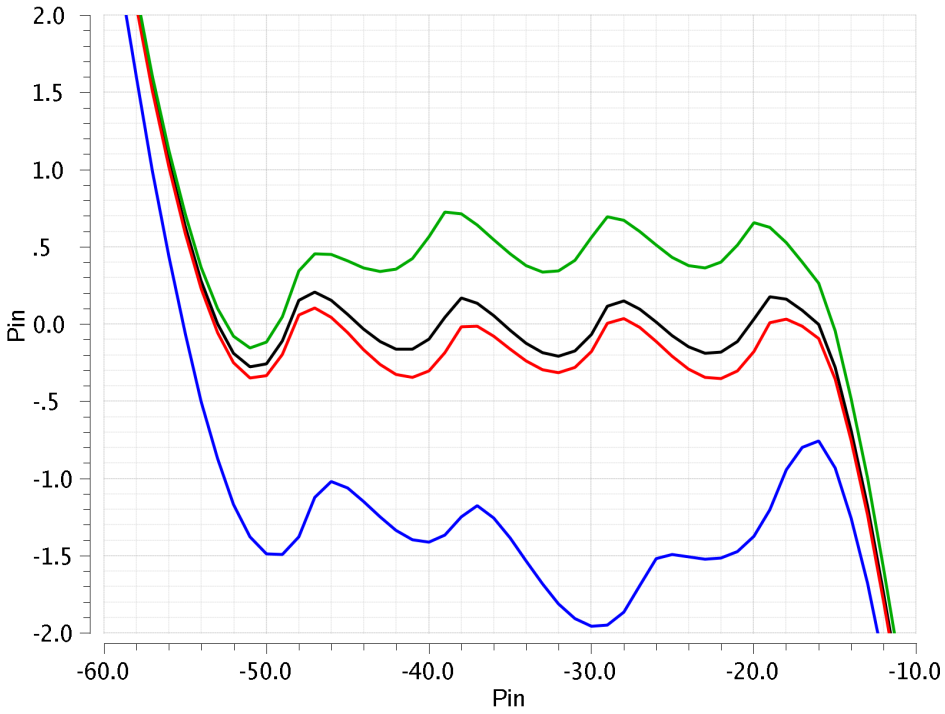


Figure 3-10: Output of log-amp detector with mismatched gain cells [black = 0%, red = 5%, green = 10%, blue = 20%

in which g_{do} is the inverse of the output impedance in the triode region. For convenience g_{do} is assumed to be equal to g_m as used in [12], this assumption is most accurate for long-channel devices. The parameter $\gamma = 1.8$ for a typical 0.18 μm CMOS process [15]. Using this parameter the input referred noise of one gain cell can be calculated as (see Appendix B-2):

$$\overline{V^2_{\mathrm{n,in,total}}} = 8kT\left(\frac{\gamma}{g_{\mathrm{m12}}} + \frac{1}{g^2_{\mathrm{m12}}R_c} + \frac{\gamma}{g_{\mathrm{m67}}g^2_{\mathrm{m12}}R^2_c}\right), \tag{3-18}$$

where g_{m12} is the trans-conductance of the M1/M2, g_{m67} the trans-conductance of M6/M7 and $\gamma = 1.8$.

To achieve a rough estimate for the noise it is assumed that: $\gamma = 1.8$, $A = g_{\mathrm{m12}}R_c = 10.53$ dB and $g_{\mathrm{m67}} = 2g_{\mathrm{m12}}$. Thus $g_{m12} \sim 3.4/(2\ \mathrm{k}\Omega) = 1.7 \times 10^{-3}\ A/V$. This results in:

$$\overline{V^2_{\mathrm{n,in,A}}} = (8.5 \times 10^3 + 1.4 \times 10^3 + 3.7 \times 10^2)kT, \tag{3-19}$$

$$= 10.3 \times 10^3 kT\ \frac{V^2}{\mathrm{Hz}}. \tag{3-20}$$

Later in this chapter the input referred noise of the log-amp detector is calculated. This input noise source will appear on the output as a fixed noise pedestal level, which is an output voltage even if the input of the log-amp detector is zero.

3-2-3 Detector Cell

Function The detector cell is part of the log-amp detector, which rectifies the input RF signal. The low-pass filter after the detector cell takes the average of all detector-cell outputs, which will be a representation of the peak value of the input wave.

Implementation A detector cell with differential input is given in Figure 3-11. This detector cell consists of two differential pairs in parallel: one connected to the input as in the gain cell, while the other is connected to the common-mode of the input signal. As shown in Chapter 2, the output of the detector is given by:

$$I_{\text{out-D}} = \begin{cases} \frac{\beta}{4} V_{\text{in-D}}^2, & \text{if } V_{\text{in-D}} < E_{\text{kD}} \\ I_{\text{bias-D}}, & \text{if } V_{\text{in-D}} \geq E_{\text{kD}} \end{cases} \tag{3-21}$$

in which $\beta = \mu_n C_{\text{ox}} \frac{W}{L}$. The detector-cell transfer of (3-21) is a non-linear operation, which modulates the input signal as described in Section 2-3. The detector cell is biased with a

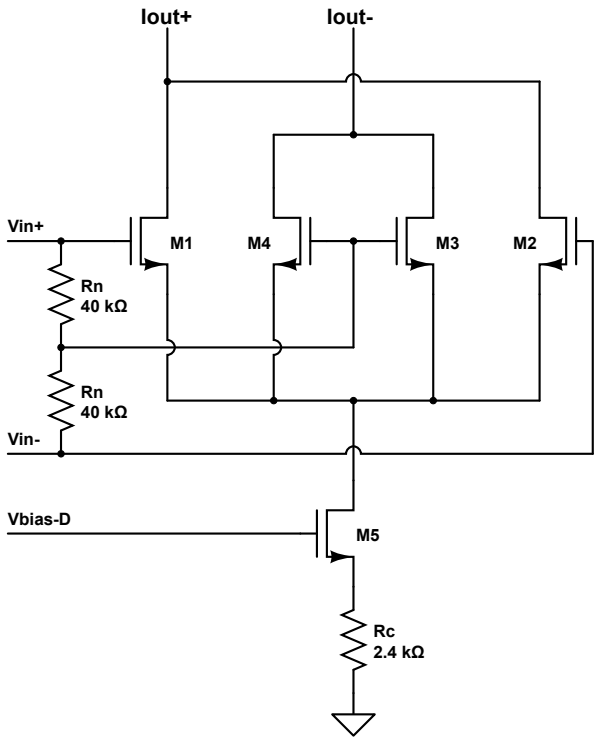


Figure 3-11: Schematic of the detector cell

PTIM bias current generated by the circuit of Section 3-3-2. In the final design the detector cell has a knee voltage E_{kD} of about 0.3 V, which adheres to $\max(V_{\text{out-A}}) > E_{\text{kD}}$.

The top-end and bottom-end correction factors were determined by comparing LCE plots for the required RF frequencies and changing the factors for maximum dynamic range. These simulations resulted in: $B_0 = 1.03$ and $D_0 = 0.37$.

These values differ from the calculated values in Chapter 2: the top-end correction is actually lower than 1 and the bottom-end correction is also smaller than calculated in Section 2-3-2.

Two things can be said about the top-end correction factor. The maximum output current of a detector cell connected to a gain cell is limited by the output swing of the gain cell (88% of $I_{\text{bias-D}}$). The first detector cell is directly connected to the input and hence does not have this limited $\max(V_{\text{out-A}})$. This can be corrected by reducing the current, consequently lowering the top-end correction factor D_0.

Secondly it became clear that for sinusoidal input signals bottom-end correction is needed (see Chapter 2). This effect is most apparent in the first detector cell because of the three succeeding stages. Therefore, the top-end correction factor can be reduced.

The last gain cell has much smaller loading capacitance at its output (only a detector cell). Hence, for high input frequencies its output swing will be higher compared to other gain cells with more loading due to slewing. This reduces the bottom-end correction factor.

Bandwidth For the gain cell the bandwidth should be as high as possible to allow the log-amp detector to work for high-frequency RF input signals. After the demodulation performed by the detector cell only the DC part of the signal carries the information. High bandwidth after demodulation is thus not of key importance. At nodes $I_{\text{out+}}$ and $I_{\text{out-}}$ the demodulation is carried out. Hence, before the signal reaches these nodes AC bandwidth is important. This suggests that the input devices of the detector cell need to be small to reduce the load capacitance at the output of the gain cells.

In Figure 3-12 the RF→DC demodulation bandwidth of the detector is simulated. A high-

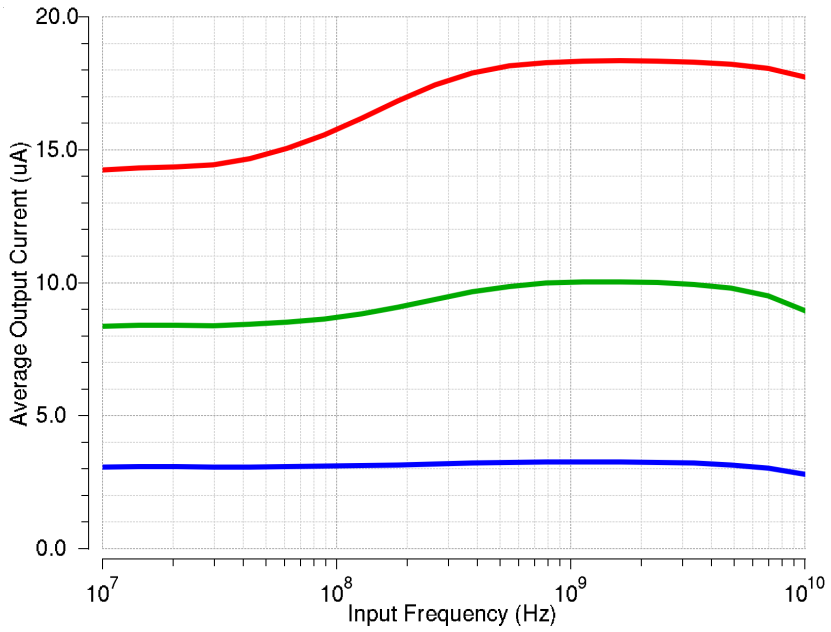


Figure 3-12: DC output current of detector cell for a sinusoidal input signal with several amplitudes [blue = 0.1 V, green = 0.2 V and red = 0.4 V input amplitude]

pass response at around 100 MHz is visible in the figure. This is due to the capacitance located

at the source node of the input devices. The non-linear operation of the detector cell will rectify the AC current into a DC output current, effectively increasing the current output of the detector. Finally at around 6 GHz the DC output current will drop because C_{GS} forms a low-pass filter which squeezes the effective gate-source voltage, decreasing the output current.

Mismatch The slope K_S is directly affected by the output current of each detector cell:

$$K_S = \frac{\max(I_{\text{out-D}})R_{\text{out}}}{20\log(A)}\,. \tag{3-22}$$

Hence, the maximum output current for each detector cell determines the local slope. This current deviates for each detector cell mainly because of the input offset of input transistors M1/M2/M3/M4, which are responsible for a fixed output current. This offset reduces the effective steerable current and therefore reduces the local slope. The offset of one input transistor of the detector cell is given by:

$$\begin{aligned}(\Delta V_{\mathrm{TH}})_{3\sigma} &= \frac{3A_{Vth}}{\sqrt{2WL}} \\ &= 4.9\text{ mV}\,.\end{aligned} \tag{3-23}$$

The output offset current follows from the trans-conductance $g_{m14} = 125 \times 10^{-6}$ A/V:

$$\begin{aligned}(\Delta I_{\text{out-D}})_{3\sigma} &= \sqrt{4}\cdot g_{m14}\cdot(\Delta V_{\mathrm{TH}})_{3\sigma} \\ &= \pm 1.2\,\mu\text{A}\,.\end{aligned} \tag{3-24}$$

Another part of the output offset comes from current source M5, whose DC current is different for each detector cell. Using large transistors for the current source and applying source degeneration the output offset current is given by[8]:

$$(I_{\text{bias-D}})_{3\sigma} = 20\ \mu\text{A} \pm 122\ \text{nA}, \tag{3-25}$$

which is negligible compared to the mismatch of the small input devices from (3-24).

The output offset calculation can now be rewritten to a local-slope offset for $\max(I_{\text{out-D}}) = I_{\text{bias-D}}$ and $I_{\text{bias-D}} = 20\ \mu$A:

$$\begin{aligned}\frac{\delta K_S}{\delta I_{\text{bias-D}}} &= \frac{R_{\text{out}}}{20\log(A)}, \\ \left(\frac{\Delta K_S}{K_S}\right)_{3\sigma} &= \frac{\Delta I_{\text{bias-D}}}{I_{\text{bias-D}}} \\ &= \pm 1.2\%.\end{aligned} \tag{3-26}$$

The total output current offset can be calculated using the offset of one detector cell as:

$$(\Delta I_{\text{det}})_{3\sigma} = \sqrt{5}\cdot(\Delta I_{\text{out-D}})_{3\sigma} = \sqrt{5}\cdot\pm 1.2\ \mu\text{A} = \pm 2.7\ \mu\text{A}, \tag{3-27}$$

which will later be used in Section 3-5-3 to calculate the output pedestal voltage[9] spread.

[8] Based on DC match simulation, see appendix B-2 for calculation.
[9] Output of log-amp detector at zero input.

Noise Compared to the noise from the gain cells, the noise from the detector cells will not be dominant in terms of increased pedestal level. This is because the noise of the first gain cell will be amplified and then demodulated by the detectors, resulting in an output pedestal level. The detector cells do contribute to this pedestal level because input referred noise from the detector will be demodulated to DC. However their contribution is limited because no amplification is present.

The 1/f noise from the detector cells directly influences the complete output curve. However this output voltage is negligible versus the output signal ranging from 0.4 to 1.8 V.

3-2-4 RF Front-End

Function The RF front-end block has three functions: coupling of the RF input signal to the log-amp detector, providing a proper common-mode for the first gain cell and detector cell and control the input of the first gain cell to cancel the offset of the whole the channel.

Implementation The RF front-end circuit is given in Figure 3-13. Capacitor C1 couples the RF signal into the channel directly to node $V_{\text{out}+}$. Node $\text{RF}_{\text{in-}}$ is connected to ground and is put there for symmetry. The common-mode generation part of the circuit is a replica of the gain cell, rendering the output common-mode equal to the output common-mode of a gain cell.

Input referred offset of the channel Given a gain of $A \sim 3$ for the gain cells, the complete offset for the whole channel can be calculated using the offset calculated in Section 3-2-2 as:

$$\begin{aligned}(V_{\text{OS,in,channel}})_{3\sigma} &= \sqrt{\sum_{N=1}^{4} \frac{(V_{\text{OS,in,A}})_{3\sigma}^2}{A^{2(N-1)}}} \\ &= \sqrt{(8\text{ mV})^2 + \frac{(8\text{ mV})^2}{3^2} + \frac{(8\text{ mV})^2}{3^4} + \frac{(8\text{ mV})^2}{3^6}} \\ &= 8.5\text{ mV}, \end{aligned} \tag{3-28}$$

where $V_{\text{OS,in,A}}$ is the input-referred offset of a gain cell. The outcome of this equation proves that first gain cell is the dominant source of offset for the channel.

Offset cancellation loop The feedback loop is shown in Figure 3-14. The output of the channel is low-pass filtered, to measure its DC output. This output signal is fed back into the circuit of Figure 3-13 at OS_+ and OS_-, which controls the DC input of the channel to cancel the total output offset. The maximum input offset steering capability of this loop is $50\,\mu\text{A} \cdot 2\,\text{k}\Omega = 100\,\text{mV}$, which is much larger than the 6σ input offset of the channel, 17 mV according to (3-28).

Frequency Response The offset control loop can be seen as three blocks in a negative feedback configuration as seen in Figure 3-14.

First lets devise the general frequency response, which is given by the black boxes A, B and C in a negative feedback configuration as:

$$\begin{aligned} V_{\text{out}} &= V_{\text{in}}\big[A(s)B(s)) - V_{\text{out}}(C(s)B(s)\big] \\ &= V_{\text{in}}\frac{A(s)B(s)}{1 + B(s)C(s)}, \end{aligned} \tag{3-29}$$

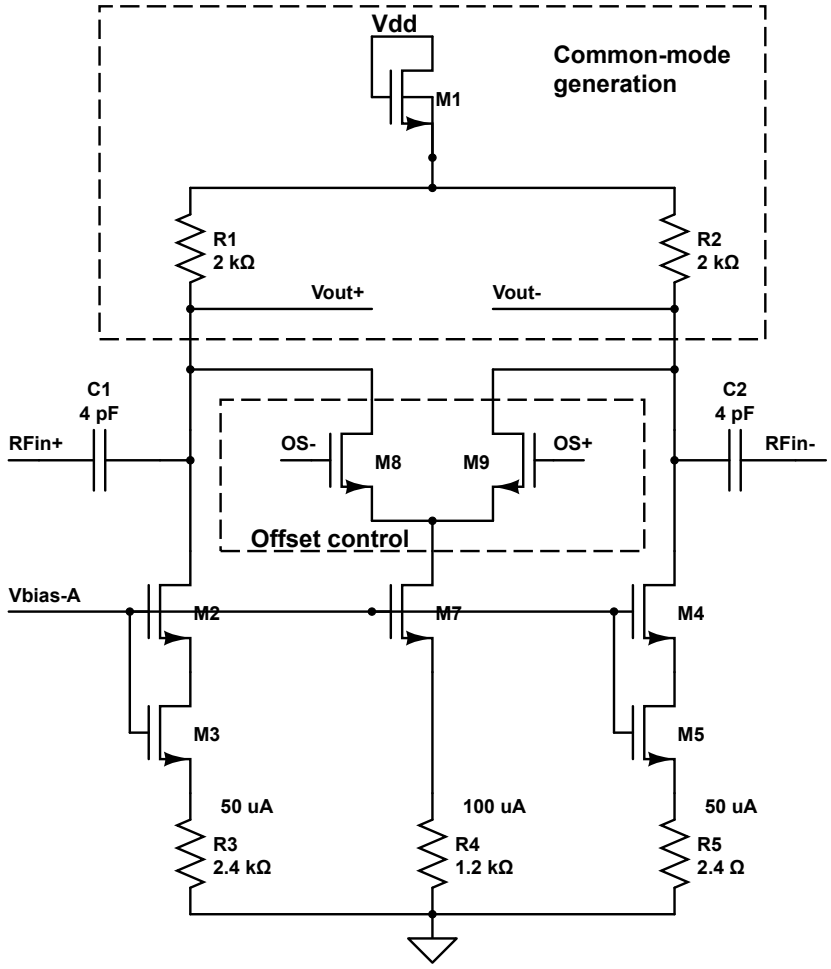


Figure 3-13: Schematic of RF front-end block

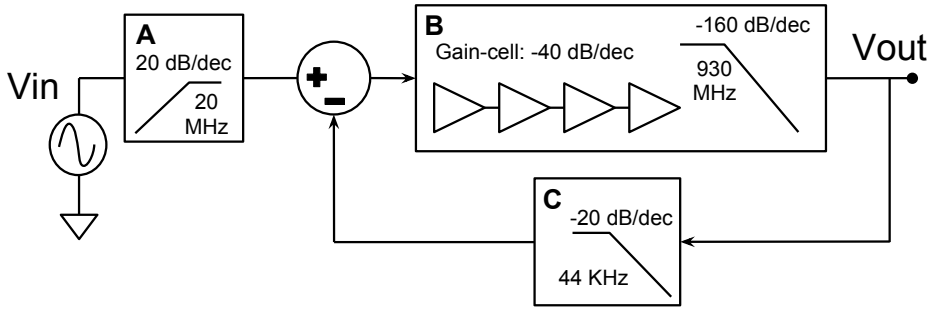


Figure 3-14: Block diagram of offset cancellation loop

substituting $A(s)$, $B(s)$ and $C(s)$ in this equation:

$$\begin{aligned} A(s) &= \frac{s\tau_{\mathrm{A}}}{1+s\tau_{\mathrm{A}}}, \\ B(s) &= \frac{1}{(1+s\tau_{\mathrm{B}})^{8}}, \\ C(s) &= \frac{1}{1+s\tau_{\mathrm{C}}}, \end{aligned}$$

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{s\tau_{\text{A}}(1+s\tau_{\text{C}})}{(1+s\tau_{\text{A}})((1+s\tau_{\text{B}})^8(1+s\tau_{\text{C}})+1)}. \tag{3-30}$$

This proves that the actual transfer is a band-pass response, with two zeroes and multiple poles. This is confirmed by the AC simulation shown in Figure 3-15. The design of this band-pass response should be such that at the minimum RF input frequency, the transfer is flat. For this design the minimum input frequency is 20 MHz. The total -3 dB input frequency bandwidth ranges from 20 up to 930 MHz.

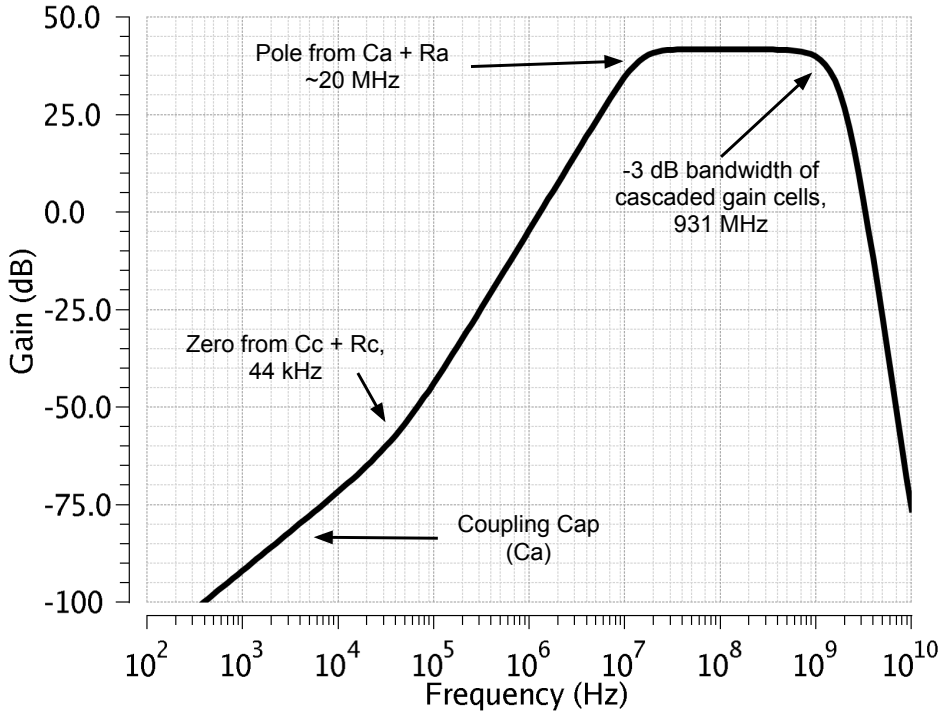


Figure 3-15: Band-pass response of offset cancellation loop

Input-Referred Noise of the Channel The total input referred noise power of the channel caused by the gain cells can be calculated by using (3-18) and referring every noise source to the input of the channel ($A = 3$):

$$\begin{aligned}
\overline{V^2_{\text{n,in,channel}}} &= \sum_{N=1}^{4} \frac{\overline{V^2_{\text{n,in,A}}}}{A^{2(n-1)}}, \\
&= \overline{V^2_{\text{n,in-A}}}\left(1+\frac{1}{A^2}+\frac{1}{A^4}+\frac{1}{A^6}\right), \\
&= \overline{V^2_{\text{n,in-A}}} \cdot 1.125, \\
&= 1.2\times 10^4 kT\ \frac{V^2}{\text{Hz}},
\end{aligned} \tag{3-31}$$

where $V^2_{\text{n,in,A}}$ is the input referred noise of the gain cell. The result of this calculation will be used in Section 3-5-3 to calculate the output pedestal level caused by the noise from the channel.

3-3 Biasing

3-3-1 Bias Block A

Function Bias block A provides the bias current to make the gain of the gain cells constant over temperature.

Implementation The circuit of bias block A is given in Figure 3-16. Its architecture is based on the constant-g_m biasing from [1]. In the schematic of Figure 3-16 the currents through transistors M1 and M2 are made equal by amplifier OA1. For this situation the current through resistor $R_{\text{c,ptim}}$, $I_{\text{bias-A}}$, can be zero or defined by:

$$\begin{aligned} V_{\text{GS1}} &= V_{\text{GS2}} + I_{\text{bias-A}} R_{\text{c,ptim}} \,, \\ \sqrt{\frac{2I_{\text{bias-A}}}{\beta}} + V_{\text{TH}} &= \sqrt{\frac{2I_{\text{bias-A}}}{n \cdot \beta}} + V_{\text{TH}} + I_{\text{bias-A}} R_{\text{c,ptim}} \,, \\ I_{\text{bias-A}} R_{\text{c,ptim}} &= \sqrt{\frac{2I_{\text{bias-A}}}{\beta}} - \sqrt{\frac{2I_{\text{bias-A}}}{n \cdot \beta}} \,, \\ I_{\text{bias-A}} &= \frac{1}{R_{\text{c,ptim}}^2} \frac{2L_1}{\mu_n C_{\text{ox}} W_1} \frac{(\sqrt{n}-1)^2}{n} \,, \end{aligned} \tag{3-32}$$

where $\beta = \mu_n C_{\text{ox}} L_1 / W_1$, L_1 the gate length of M1, W_2 the gate width of M2 and n the ratio between the area of transistors M1 and M2 in Figure 3-16.

Current $I_{\text{bias-A}}$ is exactly proportional to inverse mobility (PTIM) that was needed to bias the gain cell, as discussed in Section 2-5.

Mobility Effect In the circuit of Figure 3-16 current $I_{\text{bias-A}}$ should be such that the gain of the gain cell is as constant over temperature as possible. To achieve this, the mobility behavior of the bias current should be matched to the mobility behavior of transistors M1 and M2.

To increase the accuracy of the bias current two phenomena should be accounted for in the PTIM bias generator: mobility degradation and velocity saturation, which are both short channel effects. The effective mobility is given by:

$$\mu_{n\text{-eff}} = \frac{\mu_n v_{\max} L}{v_{\max} L (1 + \theta V_{\text{OV}}) + \mu_n V_{\text{DS}}}, \tag{3-33}$$

where $v_{\max}$ is the maximum velocity of the carriers in the channel, θ is a technology dependent fitting parameter and $V_{\text{OV}} = V_{\text{GS}} - V_{\text{TH}}$ is the overdrive voltage.

The effective mobility is thus dependent on the biasing conditions of the Metal-oxide-semiconductor field-effect transistor (MOSFET). The overdrive voltage of the input transistors of the gain cell is equal to the overdrive voltage of M1/M2 in Figure 3-16 if they have the same current density and the same unit device. Simulation results in Figure 3-17a show the gain error over temperature for different L sizes inside the bias block A (same W/L ratio). When M1/M2 use the same device size as the input transistors of the gain cell, the gain error over temperature reduces to $<0.5\,\text{dB}$.

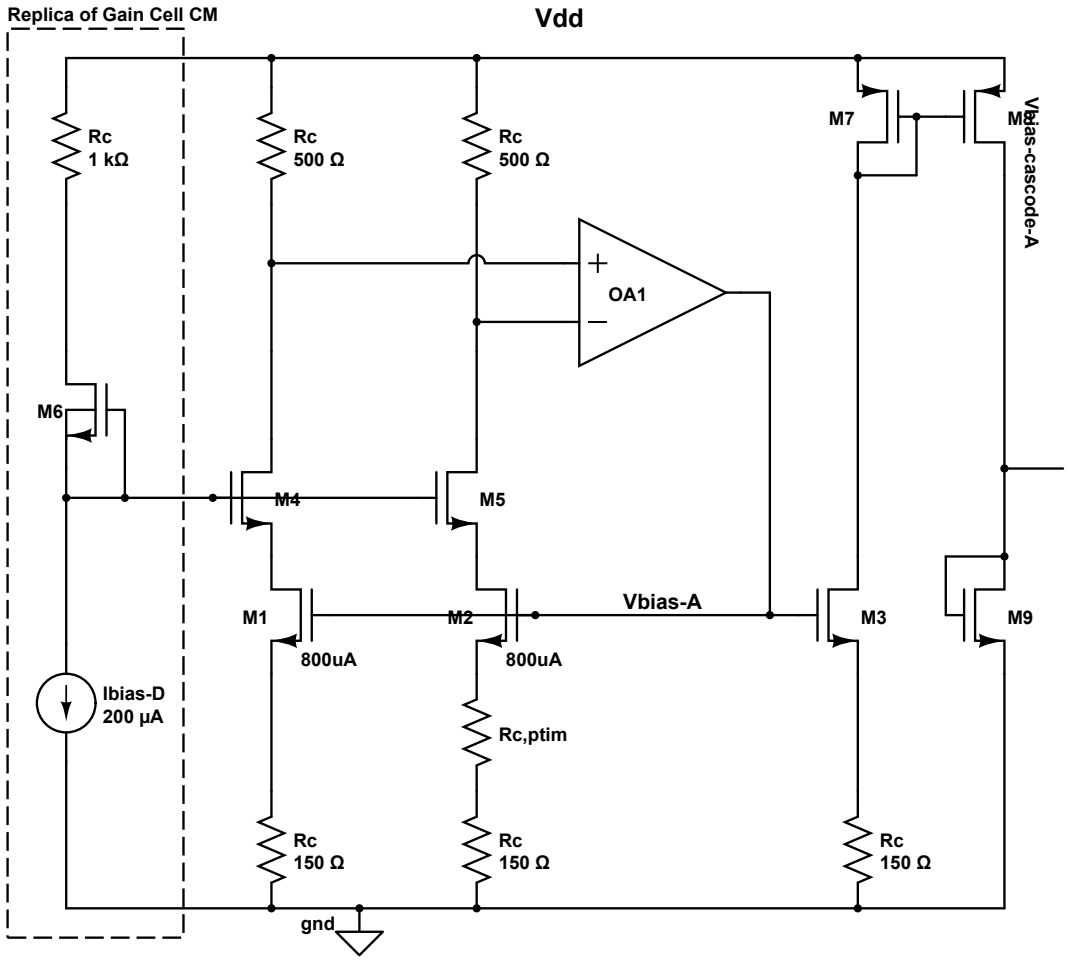


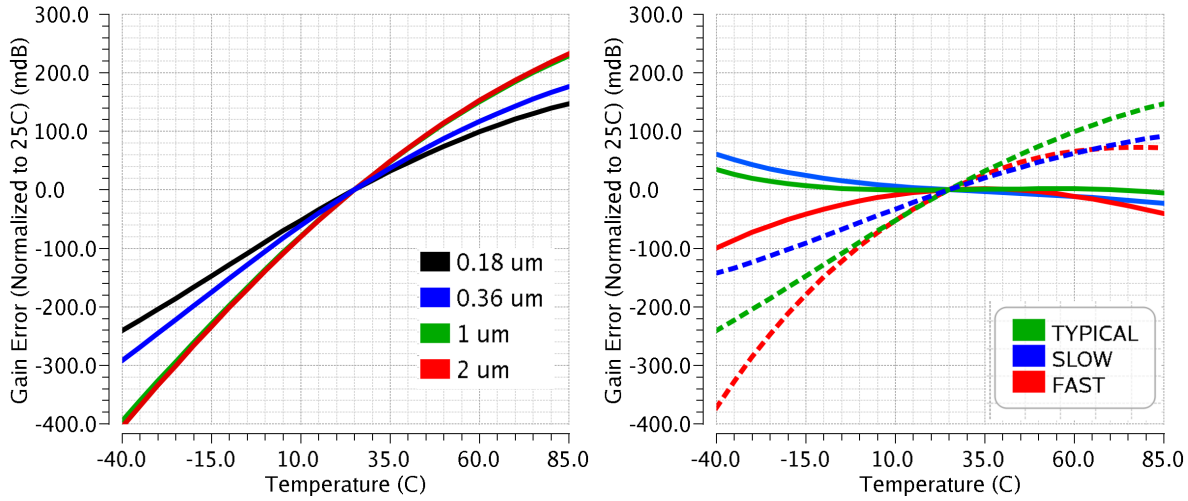
Figure 3-16: Schematic of bias block A, based on [1]

In order to bias the input transistors of the gain cell and M1/M2 with similar V_{DS} voltages, cascode devices M4/M5 are employed in the bias generator. This further reduces the gain error over temperature to <0.1 dB for the extreme corners, as shown in Figure 3-17b.

Offset of Bias Current The transistors M1/M2 were copied from the the input transistors of the gain cell for temperature performance. Their large current density per unit transistor is however not beneficial to achieve a low offset. To reduce the offset significantly the current consumption of this block will therefore be relatively large.

Calculating the bias current spread of bias block A can be predicted by looking at the Pelgrom constant for both M1 and M2. M1 is four times smaller than M2, thus M1 will be dominant in offset. Also part of the offset is from the input transistors of OA1. Their offset results in a mismatch between the current through M1 and M2.

A simplified calculation is done using the Pelgrom constant in Appendix B-5. This calculation matched with a DC-match simulation in which the bias current spread is $(I_{\text{bias-A}})_{3\sigma} = 780 \pm 33\,\mu\text{A} = 780\,\mu\text{A} \pm 4.3\%$. The gain dependence on this current can be calculated through



(a) Different L-sizes in bias block A, constant W/L, $L = 0.18\,\mu$m in gain cells

(b) With (solid) and without (dotted) cascodes in bias block A, $L = 0.18\,\mu$m in gain cells and bias block A

Figure 3-17: Normalized gain of gain cell over temperature

(3-16):

$$\begin{aligned} \Delta A &= \Delta I_{\text{bias-A}} \cdot \frac{R_c\sqrt{\beta}}{2\sqrt{I_{\text{bias-A}}}} \\ \Delta A &= \frac{A\Delta I_{\text{bias-A}}}{2I_{\text{bias-A}}}, \\ \frac{\Delta A}{A} &= \pm 2.2\%\,. \end{aligned} \tag{3-34}$$

This gain offset affects mostly the intercept, from chip to chip:

$$\begin{aligned} P_I &= 20\log\left(\frac{E_{\text{kD}}}{A^5}\right) \\ &= \frac{20}{\ln(10)}\ln\left(\frac{E_{\text{kD}}}{A^5}\right), \\ \frac{\delta P_I}{\delta A} &= \frac{20}{\ln(10)}\frac{A^5}{E_{\text{kD}}}\frac{-5E_{\text{kD}}}{A^6}, \\ \Delta P_I &= \frac{-100}{\ln(10)}\frac{\Delta A}{A} \\ &= \mp 0.96\ \text{dB}\,. \end{aligned}$$

Start-up The cascodes used in the bias block A give rise to start-up problems if the amplifier is biased from the current generated inside bias block A. This gives the bias circuit an extra operating point in which transistors M4 and M5 can put M1 and M2 in triode, such that M4 and M5 dictate the current flow of the circuit. To remove this operating point from the circuit the amplifier was biased externally by bias block D of Section 3-3-2.

3-3-2 Bias Block D

Function This circuit provides an accurate current reference for the back-end and the detector cells. It is also used for biasing bias block A and starting every circuit in the chip, except for the band-gap, which was equipped with its own start-up circuitry.

Implementation In the previous section the transistors of bias block A use the same unit device as the gain-cell input transistors. Although this helped keeping the gain constant over temperature, the minimum L transistors do not provide a very accurate current reference. Also the current density per unit device is high ($100\,\mu$A) such that distributing small currents is less accurate.

As described in Section 2-5 only current $I_{\text{bias-D}}$ and the knee voltage have a direct relation with the output curve. Keeping g_m constant over temperature is thus not important. Therefore it is not necessary to have the same unit devices in this bias circuit as in the input devices of the detector cell. Only the current sources of the detector cells match with M1 and M2 in Figure 3-18, to copy current $I_{\text{bias-D}}$ easily with bias line $V_{\text{bias-A}}$, the output node of OA1.

The accuracy in this circuit lies in the matching between the current source that biases the detector cell and the current that will be divided in the current scaler, to be discussed in Section 3-4-2. As long as the current over temperature approximately equals the current over temperature from bias block A, knee voltages E_{kA} and E_{kD} shift together over temperature, which was explained in Section 2-5. Thus the assumption that one is dominant, will be valid over temperature.

As discussed in Section 3-2-1, the temperature dependence of the input PTIM voltage scaler matches over temperature with bias block D to achieve a stable intercept.

The unit devices of this bias block use large L ($2\,\mu$m) and two times the total transistor area compared to the bias circuit of Section 3-3-1, to reduce the offset of the output current, which will be responsible for slope variation from chip to chip. Large transistors as current source for the detector cell reduce the mismatch between bias currents $I_{\text{bias-D}}$, reducing local slope variations.

Offset of the bias current As discussed previously in Chapter 2 bias current $I_{\text{bias-D}}$ from the detector cells directly affect the slope. Calculating the output current spread of this bias generator can be predicted by looking at the Pelgrom constant for both M1 and M2. Transistor M1 is four times smaller than M2, thus contributing more to the spread. Also the offset of the input transistors of OA1 affect the output current because they are responsible for mismatch between the current of M1 and M2 (see Appendix B-6). Using a DC simulation the current from bias block D is $(80\,\mu\text{A} \pm 1.25\%)_{3\sigma}$. The effect on the output slope is:

$$K_S = \frac{I_{\text{bias-D}} R_{\text{out}}}{20\log(A)}, \tag{3-35}$$

$$\frac{\Delta K_S}{\Delta I_{\text{bias-D}}} = \frac{K_S}{I_{\text{bias-D}}}, \tag{3-36}$$

$$\frac{\Delta K_S}{K_S} = \frac{\Delta I_{\text{bias-D}}}{I_{\text{bias-D}}}, \tag{3-37}$$

$$= \pm 1.25\%\,. \tag{3-38}$$

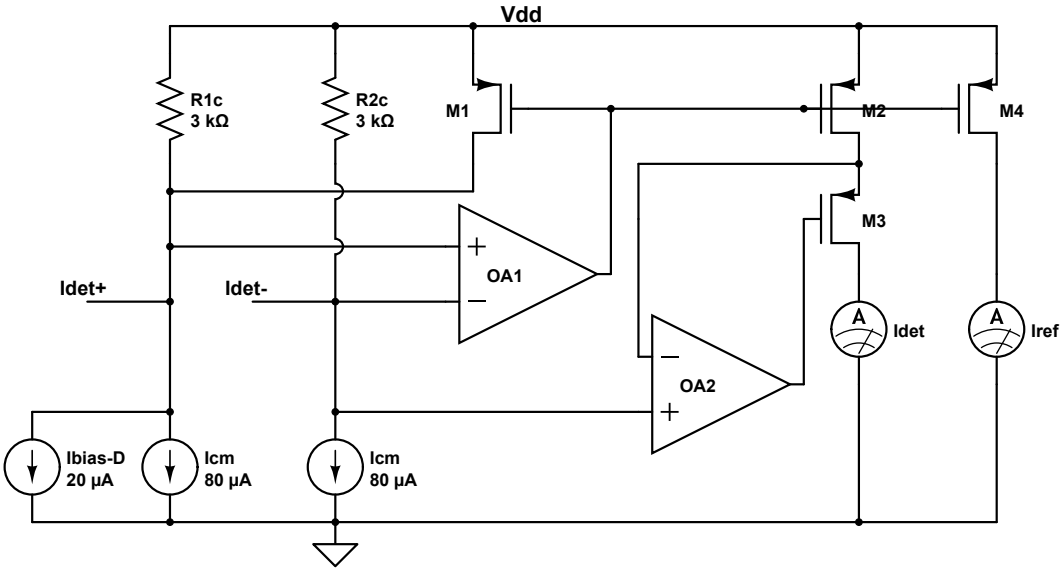


Figure 3-18: Schematic of bias block D

Start-up The start-up of bias block D was checked over all PVT conditions:

- Process corners: slow, typical and fast
- Supply voltage: 1.6 - 2.0 V
- Temperature range: -50 - 125°C

3-4 Back-End

3-4-1 Differential Current to Single-Ended Current Conversion

Function The differential current coming out of the low-pass filter in the RF core block, represents the output of the log-amp detector. To further process this current it is made sing-ended in this block. The advantage of a single-ended current is a more simple current scaler, as will be discussed in Section 3-4-2.

Implementation The low-pass filtered differential output current of the detectors I_{det}, is the input of this block. As the power increases of the RF signal, $I_{\text{det}} = I_{\text{det+}} - I_{\text{det-}}$ increases. The circuit of the detector, described in Section 3-2-3, is designed in such a way that $I_{\text{det+}} \geq I_{\text{det-}}$. The amplifier OA1 in Figure 3-19 will make sure that the voltage across resistors $R1_{\text{c}}$ and $R2_{\text{c}}$ is equal. When $I_{\text{det+}} > I_{\text{det-}}$ the difference, $I_{\text{det+}} - I_{\text{det-}}$, flows though transistor M1, keeping the voltages across the resistors equal.

Without current I_{cm}, the voltage at $I_{\text{det+}}$ and $I_{\text{det-}}$ in Figure 3-19 is controlled to $V_{\text{dd}} - I_{\text{det-n}} R_c$. For high-power RF inputs, the current $I_{\text{det-}}$ becomes small compared to $I_{\text{det-p}}$, leaving little voltage headroom for transistor M1. Therefore, a common-mode current, I_{cm}, is used to make sure that M1 is biased with a minimum V_{DS} of 240 mV. To keep M1 on even if $I_{\text{det+}} = I_{\text{det-}}$, an extra current $I_{\text{bias-D}}$ is added. After the PTM current scaler this current will translate to a temperature independent pedestal voltage at the output, V_{pedestal}.

To accurately copy current I_{det} from M1 to M2, amplifier OA2 will make the drain voltage of M2 equal to that of M1. Source degeneration could increase the matching between M1 and M2 but was not applicable due to the low voltage headroom available for M1: $V_{\text{DS}} \sim 240$ mV. The single-ended output current I_{det} is fed into a trans-linear loop, which will be explained in the next section. Output current I_{ref} is used for voltage references inside the trans-linear loop.

The circuits of OA1 and OA2 of Figure 3-19 are given in Figure 3-20a.

Frequency compensation The current through transistor M1 is constantly changing depending on the output current from the detectors. The trans-conductance (g_{m1}) of M1 changes with the RF input power. For low-power RF input powers the gain of M1: $g_{\text{m1}} R_c < 1$ and for large input power g_{m1} increases such that $g_{\text{m1}} R_c > 1$. To compensate for the extra variable gain generated though transistor M1 the Miller cap (C_c) inside amplifier OA1 was increased to compensate for the extra gain of the third stage. This is only possible because the gain of the third stage is kept low (<5) by using a small resistor R_c and low W/L ratio for M1. A higher gain for the third stage would require a more complicated frequency compensation network. The bode plot with and without frequency compensation is shown in Figure 3-21.

The frequency compensation in Figure 3-21 increases the load capacitance at node X in Figure 3-20a. Due to the Miller effect C_c will be multiplied by the gain of the second stage (∼120x). The dominant pole with $C_c = 25 \times 10^{-12}$, $A_2 = 120$ and the impedance at node X, $r_{\text{o,X}} = 0.9 \times 10^6$, will be:

$$f_{\text{p1}} = \frac{1}{2\pi(1 + A_2) C_c r_{\text{o,X}}} \sim 50 \text{ Hz}. \tag{3-39}$$

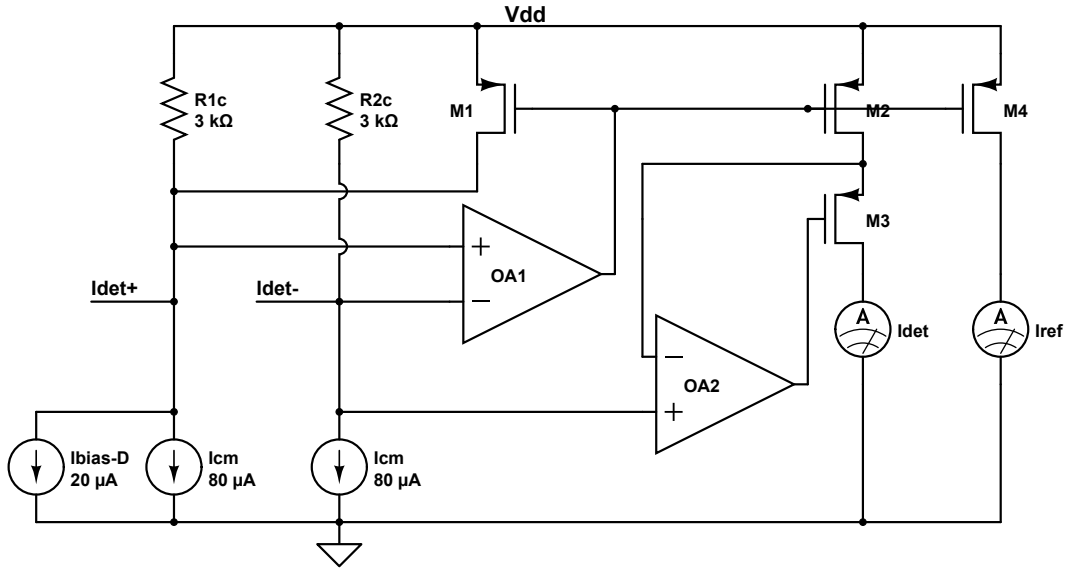
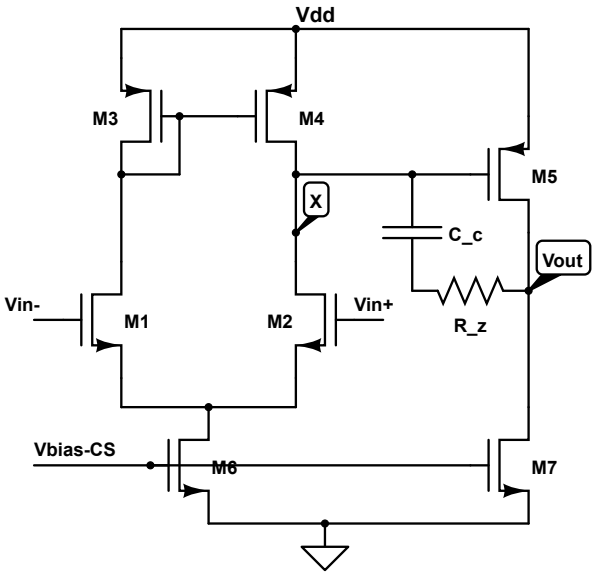


Figure 3-19: Schematic of differential current to single-ended current conversion block



(a) Schematic

	OA1	OA2
C_c	25 pF	1.2 pF
R_z	13 kΩ	6 kΩ

(b) Miller compensation parameters

Figure 3-20: Amplifiers OA1 and OA2 from Figure 3-19.

The second pole (f_{p2}) is around 500 kHz and is coming from the output node of OA1: V_{out}. This pole is cancelled by the zero coming from the frequency compensation network ($C_c = 25$ pF, $R_z = 13$ kΩ, $g_{\mathrm{m5}} = 220 \times 10^{-6} A/V$):

$$f_{\mathrm{z,1}} = \frac{1}{2\pi C_c (R_z - g_{\mathrm{m5}}^{-1})} \sim 750 \text{ kHz}^{10}. \tag{3-40}$$

This pole-zero cancellation with R_z significantly increases the phase margin. The second zero

[10] Given in [12] on page 365.

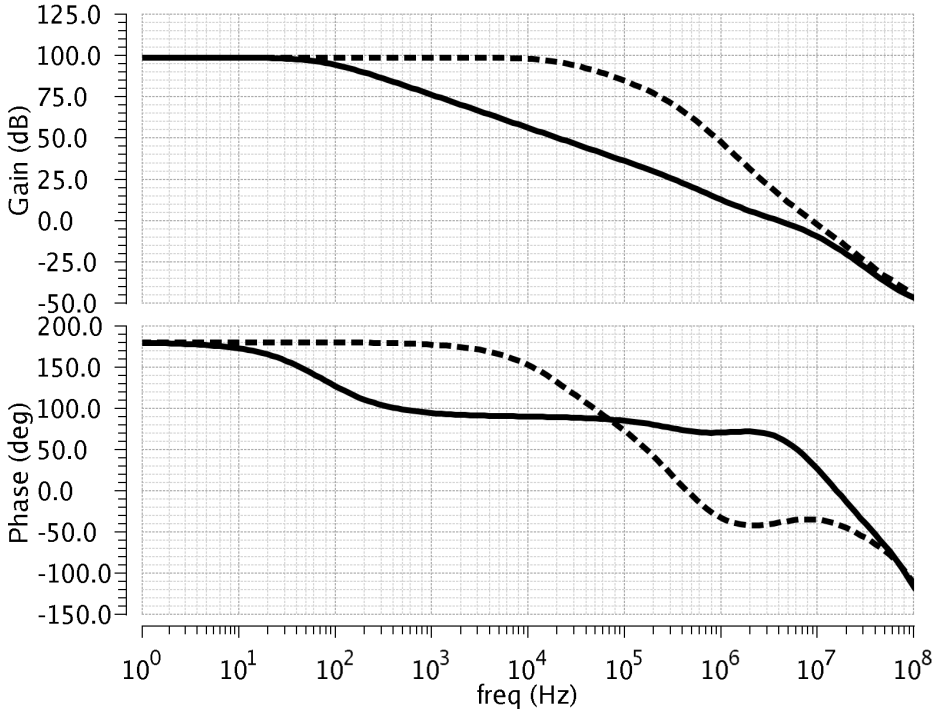


Figure 3-21: Bode plot at room temperature for maximum input power [solid = after-, dotted = before- compensation]

($f_{z,2}$) of around 2 MHz is coming from the low-pass filter of the RF core block. This zero limits the gain margin.

Figure 3-22 shows the phase and gain margin versus RF input power. As the input power increases the phase and gain margin drop substantially. The minimum Phase Margin (PM) and Gain Margin (GM) over process corners (slow, typical, fast), supply voltage (±10%) and temperature (-40°C - 85°C) are given by:

$$\begin{aligned} PM &> 61^\circ \\ GM &> 15 \text{ dB} \end{aligned}$$

Offset The output current offset from this circuit is dominated by the input offset of OA1, in Figure 3-19. The large size of the current mirror consisting of M1 and M2, their offset contribution on the output current is not dominant. The input offset of OA1 is dominated by M1, M2 and M3, M4 in Figure 3-20a:

$$\begin{aligned} (\Delta V_{\text{TH}})_{3\sigma,M12} &= \frac{3A_{V_{\text{TH}}}}{\sqrt{WL}}, \\ &= 0.6 \text{ mV}, \qquad (3\text{-}41) \\ (\Delta V_{\text{TH}})_{3\sigma,M34} &= 1.9 \text{ mV}. \qquad (3\text{-}42) \end{aligned}$$

The input offset follows from:

$$(\Delta V_{\text{in,OA1}})_{3\sigma} = \sqrt{\left((\Delta V_{\text{TH}})_{3\sigma,M12}\right)^2 + \left((\Delta V_{\text{TH}})_{3\sigma,M34} \cdot \frac{g_{\text{m34}}}{g_{\text{m12}}}\right)^2} = 1.76 \text{ mV} \qquad (3\text{-}43)$$

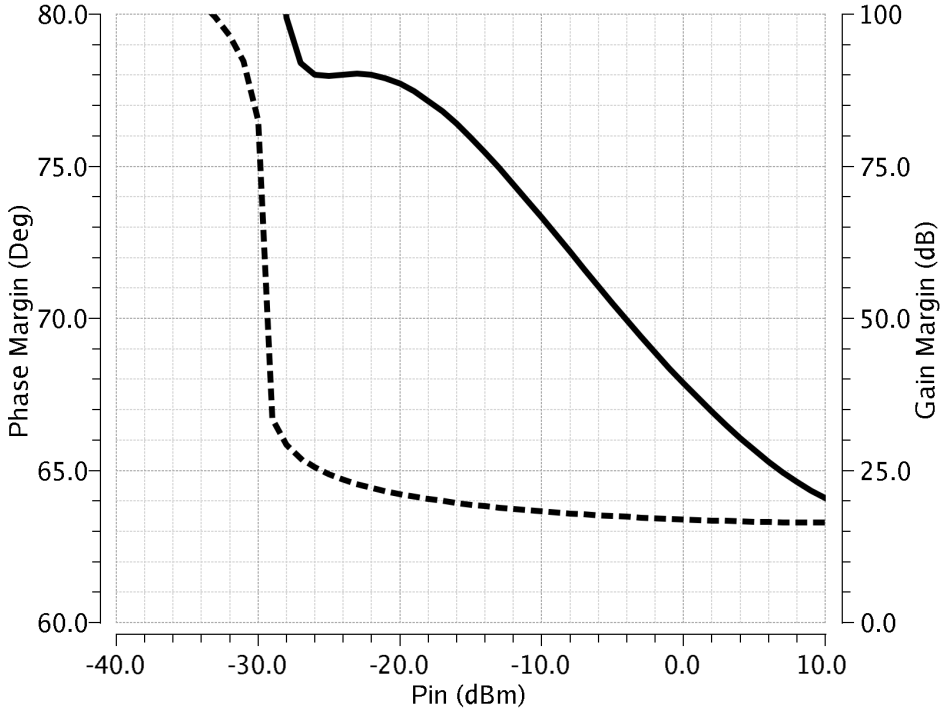


Figure 3-22: Phase and gain margin over input power. [solid = PM, dotted = GM]

Any offset at the input of the amplifier OA1 will be converted into an output current by the $R1_c$ and $R2_c$ resistors in Figure 3-19:

$$(I_{\text{out}})_{3\sigma} = 20\,\mu \pm \frac{(\Delta V_{\text{in,OA1}})_{3\sigma}}{R_c}\ \text{A} = 20 \pm 0.59\ \mu\text{A}. \tag{3-44}$$

This result was verified with a DC match simulation where $(\Delta I_{\text{out}})_{3\sigma} = 0.67\ \mu$A. The DC match differs due to the mismatch of the currents I_{CM} in Figure 3-19, which was not included in the calculation.

In the above offset calculation the spread of the current $I_{\text{bias-D}}$ and detector cells was not included because the total offset of the pedestal voltage will be calculated in Section 3-5-3.

3-4-2 Current Scaler

Function As described in Section 2-5, a PTM current scaler block is needed succeeding the detector cells for the PTIM temperature compensation scheme. A trans-linear (TL) circuit does this current operation.

Implementation The CMOS fabrication process allows for a maximum supply of 1.8 V for the low-voltage devices. Because this supply voltage is nearly equal to two stacked V_{be}s of $\sim$700 mV, little voltage headroom would be left for the current sources and other bias circuitry. Therefore, for this trans-linear loop, the up and down topology is the most convenient [16]. Figure 3-23 shows the current scaler, with an ideal transfer of:

$$I_{\text{out}} = I_{\text{det}} \frac{I_{\text{const}}}{I_{\text{ptim}}}, \tag{3-45}$$

which is the current operation needed to make the PTM scaler, as discussed in Section 2-5.

To make room for transistor M5, the whole trans-linear loop is lifted up by 0.2 V, as shown in Figure 3-23 by the voltage source V_{ref1}.

For optimal performance the available bipolar devices were used for the translinear-loop. For a complete CMOS implementation these can however be replaced with MOSFETs biased in weak-inversion.

Due to low-beta ($\beta < 30$) bipolar devices available in the CMOS process, base currents cause relatively large errors in the transfer function. Using amplifiers which can feed these base currents, the ideal function can be approximated much more closely. Biasing the bipolar devices with approximately equal V_{ce} minimizes the error due to the Early effect. The collector current of transistors Q1 and Q4 is equal to I_{det} and I_{out} respectively, the value of which can be up to 160 μA[11]. Therefore OA1 and OA3 must be able to supply the base currents which can be 6 μA in worst case conditions. The circuit diagram of amplifiers OA1-OA4 is given in Figure 3-24a, which consist of a basically a differential pair with a current mirror on top. OA5 differs because its low common-mode input voltage of $\sim$0.2 V requires a PMOS input pair, as shown in Figure 3-24b.

Frequency Compensation The single-stage amplifiers of Figure 3-23 form, together with bipolar transistors Q1-Q4, two-stage feedback loops. The gain of these loops is not very important because the base and collector voltages do not need to be exactly equal: for $V_{\text{bc}} < 50$ mV the second-order effects will be small.

The most favorable frequency compensation technique, a phantom zero [17], which is an implemented zero which is visible in the loop but not in the transfer, will not be effective; OA1 together with Q1 form a loop with current output. The feedback comes from the high impedance node, the collector of Q1. To make the feedback stronger a really large resistor or inductor is needed, which is not practical for all the loops in Figure 3-25.

The next preferred stabilization technique is pole splitting, which is used for all five loops. The trans-conductance of bipolar transistors Q1 and Q4 varies because the input current

[11] 85°C, fast process corner and maximum output detector cells.

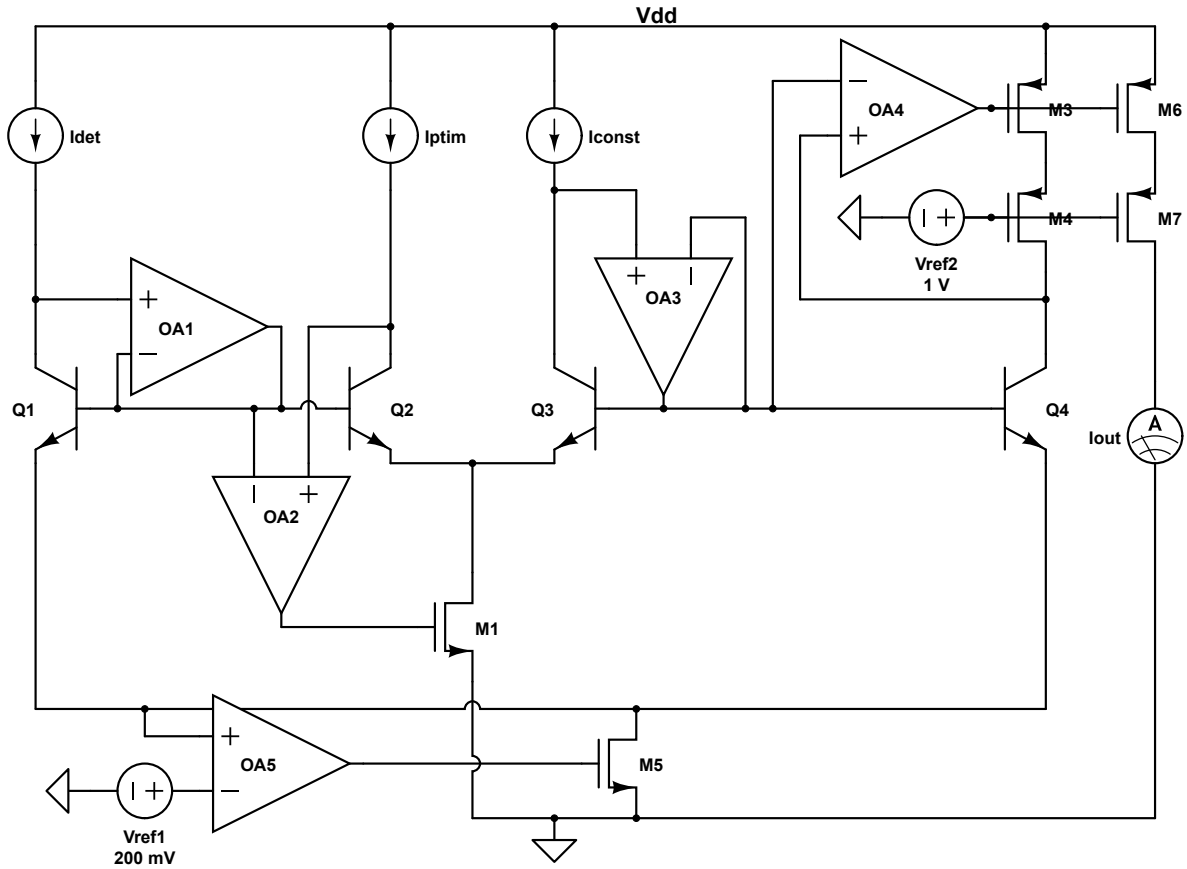


Figure 3-23: Complete schematic of the current scaler

varies from 20 to 120 μA at room temperature. This changes the total gain of the loops and could potentially affect stability. However, due to the Miller effect, a higher g_m will increase the Miller capacitance and therefore the stability is nearly independent of the input current I_{det}, in contrast with the loop in Section 3-4-1. The five feedback loops of Figure 3-23 are described in Table 3-3.

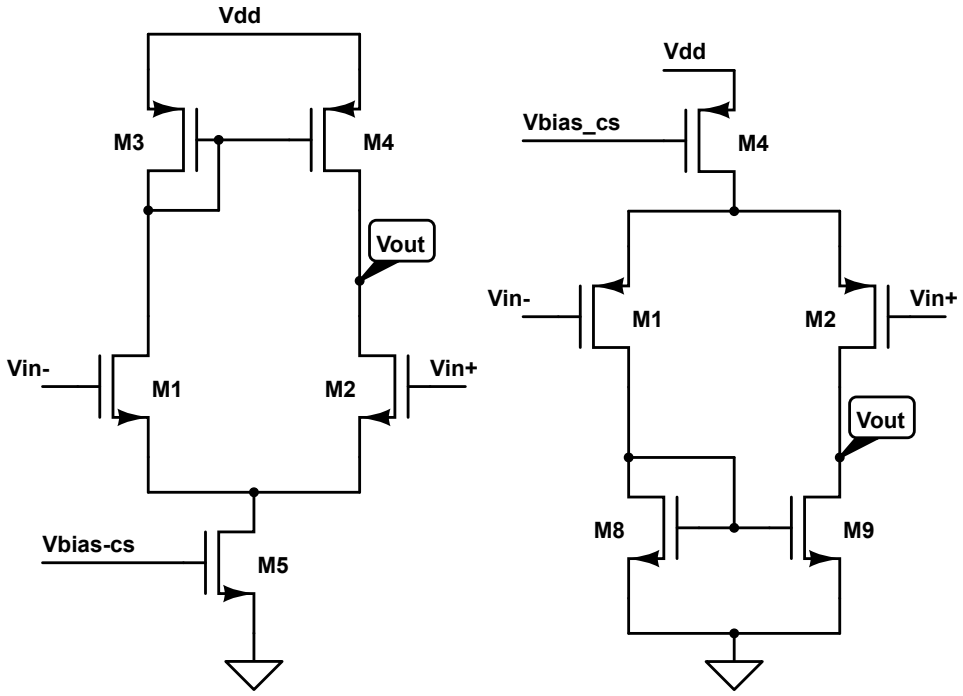
All of these loops use the same frequency compensation technique[12]: addition of a Miller cap (C_c) to slow-down the dominant pole and use the nulling resistor (R_z) to approximately cancel the first non-dominant pole in the loop.

The minimum phase margin and gain margin for all loops over corners (slow, typical, fast), supply voltage ($\pm 10\%$) and temperature (-40°C - 85°C) are given by:

$$\begin{aligned} PM &> 68^\circ \\ GM &> 16\,\text{dB} \end{aligned}$$

Offset The output current offset of Figure 3-23 is dependent on: ΔI_{det}, ΔI_{ptim}, ΔI_{const}, the matching of Q1-Q4 and the matching of M3 and M6.

[12]This compensation technique a combination of pole-splitting (the Miller capacitance) and pole-zero cancellation (the nulling resistor combined with the transistor).



(a) Schematic of OA1-OA4 **(b)** Schematic of OA5

Figure 3-24: Amplifiers OA1-OA5 from Figure 3-23

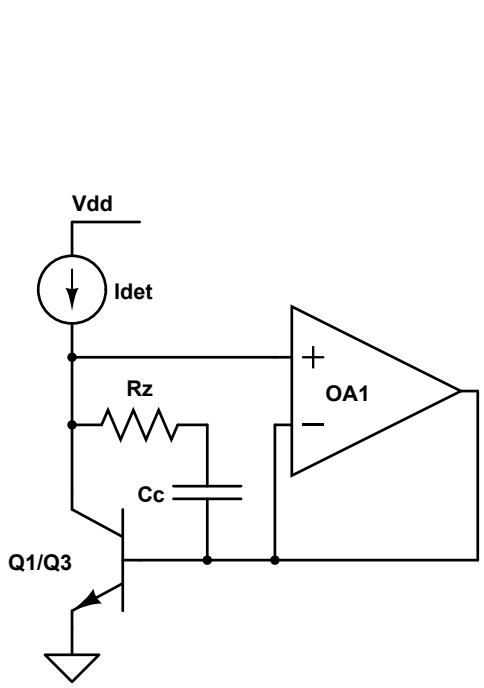
Loop	Devices	Figure	Description
1	OA1, Q1	3-25a	Bias Q1 at $V_{\mathrm{bc}} \sim 0$
2	OA2, M1, Q2	3-25b	Bias Q2 at $V_{\mathrm{bc}} \sim 0$ by controlling the emitter.
3	OA3, Q3	3-25a	Bias Q3 at $V_{\mathrm{bc}} \sim 0$
4	OA4, M3, Q4	3-25c	Bias Q4 at $V_{\mathrm{bc}} \sim 0$
5	OA5, M5	3-25d	Bias Q2 with I_{ptim} and $V_{\mathrm{bc}} \sim 0$

Table 3-3: Loops of Figure 3-23

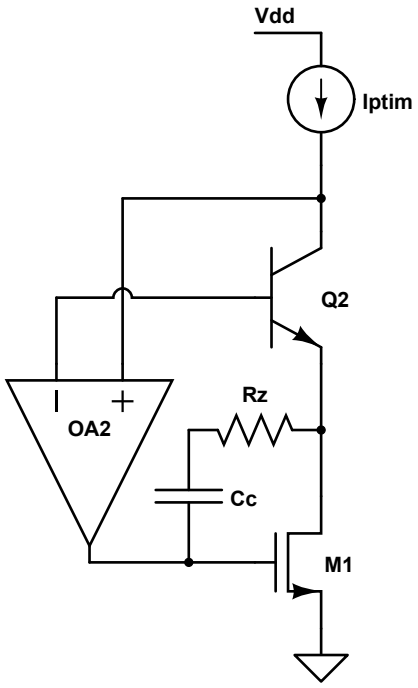
By their sizing the bipolar devices were made negligible in terms of offset. Looking at the trans-linear block only, without the spread of the input currents, M3 and M6 dominate the offset performance:

$$(\Delta I_{\mathrm{out}})_{3\sigma} = g_{\mathrm{m36}}(\Delta V_{\mathrm{TH}})_{3\sigma,M36} = 0.49\,\mu\mathrm{A}, \tag{3-46}$$

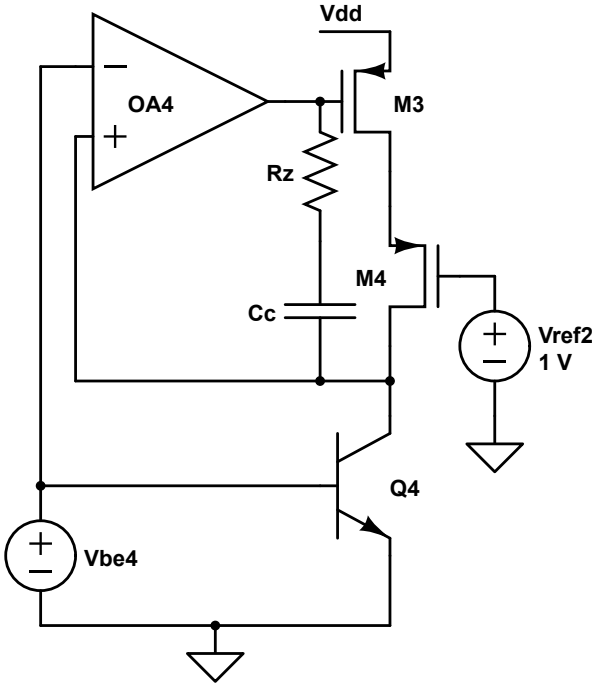
which was confirmed by a DC match simulation, rendering $(\Delta I_{\mathrm{out}})_{3\sigma} = 0.52\,\mu$A. The effect of this output current spread on the intercept point will be calculated in Section 3-5-2.



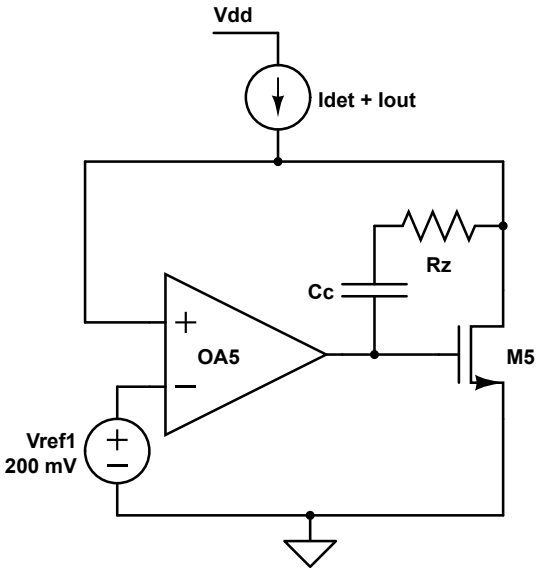
(a) Loop 1 and 3



(b) Loop 2



(c) Loop 4



(d) Loop 5

Figure 3-25: Equivalent circuits of the loops from Figure 3-23

3-4-3 Bandgap Reference

Function For the trans-linear loop in the previous section, a constant over temperature current I_{const} and two V_{ref}'s are needed. This block provides these currents.

Implementation The band-gap voltage block will be treated like a black box in this thesis, because it was copied from the IP[13] library. It is modeled in Figure 3-26 as a DC voltage source.

To create a temperature independent current for the trans-linear loop, the $R1_c$ resistor is used to convert the band-gap voltage into a current. The constant current is copied using transistor M1, M2, M4 and M5. Transistor M2 is biased with a drain voltage which is made equal to M1 with OA2, to accurately copy the current. This is important because current I_{const} will be used in the trans-linear loop to scale the output current, which will define the complete transfer[14] of the log-amp detector.

Currents I_{ref1} and I_{ref2} are used inside the trans-linear loop to for two reference voltages and is used as I_{cm} in the circuit of Figure 3-19.

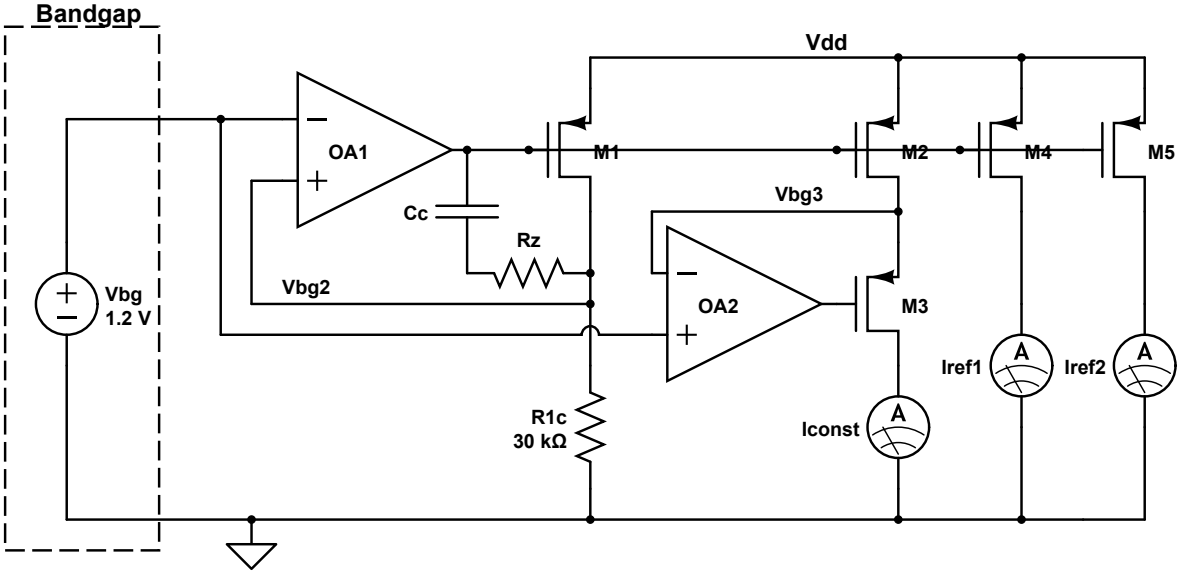


Figure 3-26: Schematic of the bandgap reference

Frequency compensation Similar as in the previous sections, the frequency compensation consist of pole splitting using the Miller effect and pole-zero cancellation with R_z. OA1 is a differential pair with a PMOS mirror on top, equal to the circuit of Figure 3-24a. Together with transistor M1 of Figure 3-26, the loop consist of two stages. The output of OA1 will be the dominant pole, which can be compensated using Miller compensation. With the addition of C_c in Figure 3-27, the bandwidth of the dominant pole is reduced from about 10 to 1 KHz. The added zero from the nulling resistor compensates for the pole of around 10 MHz.

[13] Intellectual property.
[14] Changes in this current directly control the slope of the transfer curve.

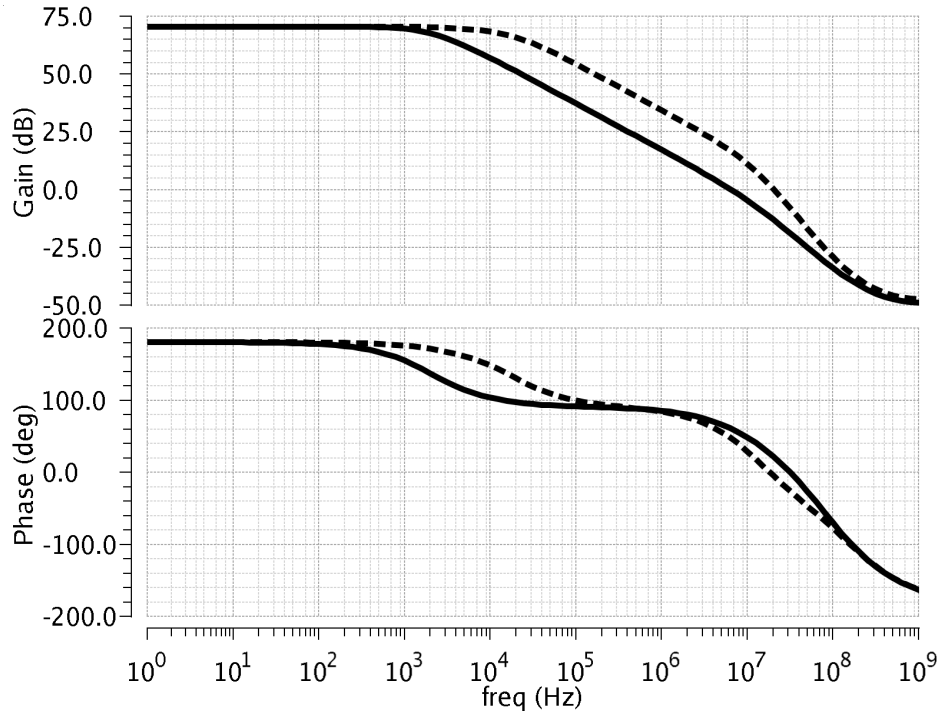


Figure 3-27: Loopgain and phase of OA1 with M1. [solid = with-, dotted = without- compensation]

Amplifier OA2 is a two-stage amplifier equal to the circuit of Figure 3-20a. Because OA2 is only used for biasing the drain of M2, the gain could be kept low. Stabilization was obtained using Miller compensation.

Offset The voltage from the band-gap block will be copied by OA1 as V_{bg2}. Assuming infinite gain and an ideal band-gap reference voltage, the error on V_{bg2} will be caused by the input transistors of OA1:

$$(\Delta V_{\mathrm{bg2}})_{3\sigma} = 1.5\,\mathrm{mV}. \tag{3-47}$$

Another important source of output current offset is the mismatch between and M1 to M2. M1 is two times the size of M2, such that the final output current is equal to 20 μA. Using the Pelgrom constant to calculate the offset between M1 and M2:

$$(\Delta V_{\mathrm{th}})_{3\sigma,M1,M2} = \sqrt{\left(\frac{3A_{V_{\mathrm{th}}}}{\sqrt{2WL}}\right)^2 + \left(\frac{3A_{V_{\mathrm{th}}}}{\sqrt{2WL}}\right)^2} = 0.9\,\mathrm{mV}, \tag{3-48}$$

combining this result with the trans-conductance of M2: 255 $\times 10^{-6}$ A/V, results in an output current spread of:

$$(\Delta I_{\mathrm{const}})_{3\sigma} = \sqrt{\left(\frac{(\Delta V_{\mathrm{bg2}})_{3\sigma}}{R_c}\right)^2 + (g_{\mathrm{m3}}(\Delta V_{\mathrm{TH}})_{3\sigma,M1,M3})^2} = 0.23\ \mu\mathrm{A}$$

Comparing this value to the DC match result of $(\Delta I_{\mathrm{const}})_{3\sigma} = 0.28\ \mu$A, proves that the calculation is quite accurate. The rest of the spread originates from the band-gap circuit.

3-4-4 Current to Voltage Buffer

Function This block does some extra low-pass filtering and the final current to voltage conversion. The output op-amp should be able to handle a variety of output loads.

Implementation The circuit of the current to voltage buffer is given in Figure 3-28, in which the amplifier is shown in Figure 3-29.

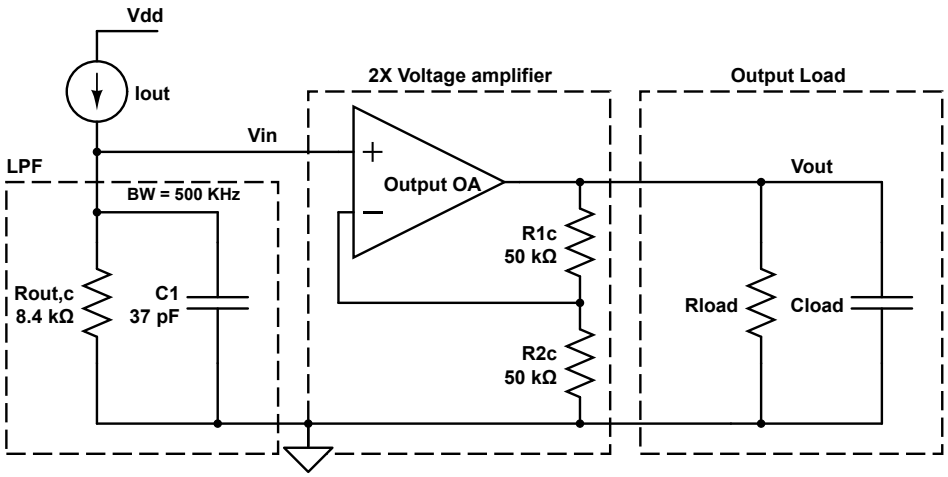


Figure 3-28: Schematic of current to voltage buffer with load

I-V Conversion The output current of the log-amp detector I_{out} is converted to a output voltage with resistor $R_{\text{out,c}}$. Voltage V_{in} ranges from 0.17 up to 1 V at maximum input power. The final low-pass filter determines the speed of the response to a power step at the input. Excluding the output load capacitance from the measurement equipment, the ideal response time would be $(500\,\text{KHz})^{-1} = 2\,\mu\text{s}$.

Output Op-Amp The circuit of the Output OA is given in Figure 3-29. The final output stage of the op-amp is a simple class-A stage with a 320 μA current output. A PMOS input pair was chosen for two reasons: the common-mode level of V_{in} does not exceed 1 V and PMOS have better matching compared to the NMOS transistors. Frequency compensation is again done through pole splitting, because the unknown output load will not qualify for the phantom zero stabilization technique. Given a resistive load of 50 kΩ and a high input V_{in} of 0.8 V, the PM and GM for multiple capacitive loads are shown in Figure 3-30.

Offset The first offset component is originating from the input devices of the opamp. This input offset directly affects the output voltage, thus changes the intercept of the curve. Another offset component is the matching between the resistors of the feedback network, which affect the output slope. The effect of this mismatch is not dominant due to the size of the resistors in the layout. The mismatch between input transistors M1 and M2 in Figure 3-29

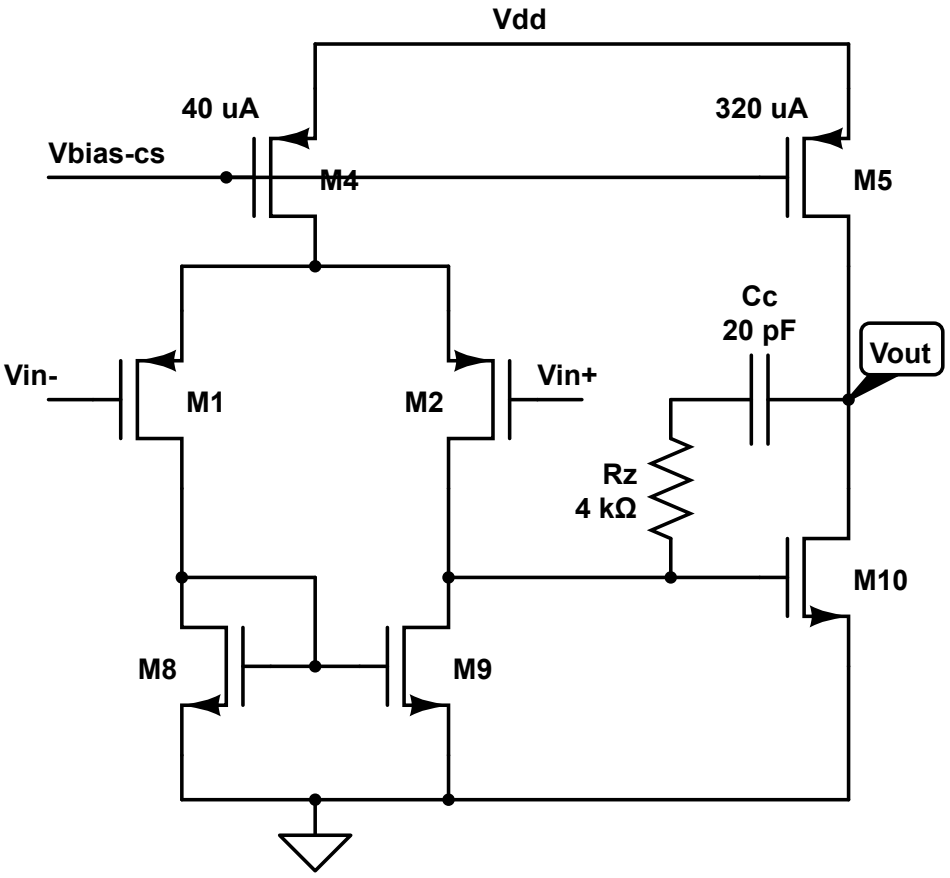


Figure 3-29: Schematic of output OA from Figure 3-28

is given by:

$$(\Delta V_{\mathrm{TH,M12}})_{3\sigma} = \frac{3A_{V_{\mathrm{TH}}}}{\sqrt{WL}} = 0.53 \text{ mV}. \tag{3-49}$$

Also M8 and M9 in the opamp play an important role for the input offset:

$$(\Delta V_{\mathrm{TH,M89}})_{3\sigma} = \frac{3A_{V_{\mathrm{TH}}}}{\sqrt{WL}} = 0.40 \text{ mV}, \tag{3-50}$$

calculating this to the input of the opamp and adding the contribution of M1 and M2:

$$(\Delta V_{\mathrm{in}})_{3\sigma} = \sqrt{\left(\frac{g_{\mathrm{m89}}}{g_{\mathrm{m12}}}(\Delta V_{\mathrm{TH,M89}})_{3\sigma}\right)^2 + (\Delta V_{\mathrm{TH,M12}})^2_{3\sigma}} = 0.88 \text{ mV} \tag{3-51}$$

The output offset is two times the input offset of the opamp[15]: $(\Delta V_{\mathrm{out}})_{3\sigma} = 1.76\,\mathrm{mV}$. This matched with a DC match simulation: $(\Delta V_{\mathrm{out}})_{3\sigma} = 1.72\,\mathrm{mV}$. This output offset affects the intercept point as described in Section 3-5-2.

[15] Assuming that the resistors are not dominant in terms of output offset.

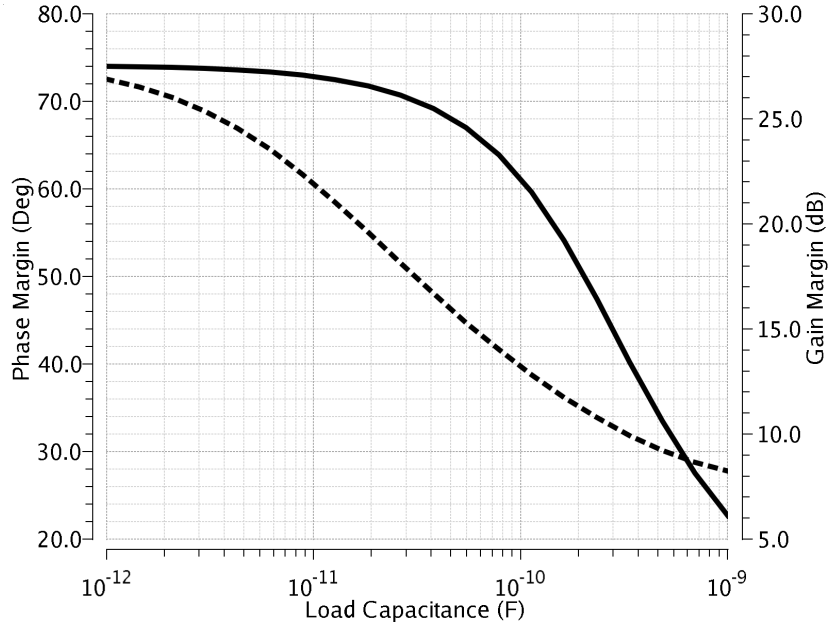


Figure 3-30: Phase and gain margin over output load capacitance at $R_l = 50\ k\Omega$ and $V_{\text{in}} = 0.8$ V. [solid = PM, dotted = GM]

3-5 Output Characteristics

3-5-1 Slope

The slope can be calculated from $I_{\text{bias-D}} = 20\,\mu\text{A}$, $R_{\text{out}} = 8.4\ k\Omega$, $A = 10.5\ \text{dB} = 3.4$, the current-gain of 1 of the current scaler and the 2X multiplication by the output buffer:

$$K_S = \frac{2I_{\text{bias-D}}R_{\text{out}}}{20\log(A)} \tag{3-52}$$

$$= 32\,\text{mV/dB}. \tag{3-53}$$

Table 3-4 adds the main contributors for the slope offset.

Input transistors detector cell	±2.7%
Bias block D	±1.3%
Band-gap output current	±0.6%
Current Source of Detector Cells	±0.3%
Total	±3.1%

Table 3-4: Slope offset contributors (3σ)

$$(K_S)_{3\sigma} = 32 \pm 1\ \text{mV/dB} \tag{3-54}$$

3-5-2 Intercept Point

The intercept point of the log-amp detector can be calculated from $A = 3.4$, $E_{\text{kD}} = 0.3\,\text{V}$, $N = 4$, $X = 0.9$, $B_0 = 1.03$ and $D_0 = 0.37$:

$$(V_I)_{\text{RF-FE}} = \frac{E_{\text{kD}}}{A^{(X-1)+N+D_0+B_0-1}}, \tag{3-55}$$

$$= 1.6 \times 10^{-3}\,\text{V}, \tag{3-56}$$

which is the input voltage at the RF Front-End. To calculate this voltage back to the input this voltage is multiplied by the inverse transfer of the RF input block (0.53^{-1}):

$$V_I = 0.53^{-1}(V_I)_{\text{RF-FE}} = 3 \times 10^{-3}\,\text{V}, \tag{3-57}$$

with the $50\,\Omega$ input impedance this translates to a DC input power of:

$$P_I = 10\log(V_I^2/50) = -67\,\text{dBW} = -37.4\,\text{dBm} \tag{3-58}$$

The fixed pedestal output voltage of 336 mV shifts the intercept point down with $366/32 = 11.44\,\text{dB}$. Yielding a DC intercept of -49 dBm, which is equivalent to a sinusoidal input power of -46 dBm.

Table 3-5 shows the main contributors to the slope offset.

$$(P_I)_{3\sigma} = -46 \pm 1.8\,\text{dBm} \tag{3-59}$$

Detector Cells	±1.4 dB
Bias Block A	±1 dB
Differential to single-ended current conversion	±0.3 dB
Current Scaler	±0.25 dB
Current to Voltage Buffer	±0.1 dB
Total	±1.8 dB

Table 3-5: Intercept offset contributors (3σ)

3-5-3 Pedestal level

The pedestal level on the output curve, which is the output voltage for zero input power, is coming from:

- Fixed current I_{ptim} added in the circuit of Figure 3-19
- Detected noise of the RF-core

The absolute pedestal level, excluding noise sources is simply: $V_{\text{pedestal}} = 2R_{\text{out}}I_{\text{ptim}} = 336$ mV. To estimate the DC offset of the pedestal level, the detector cells are assumed to be dominant in offset. As calculated in Section 3-2-3, the output current spread of the detector cells is given by:

$$(\Delta I_{\text{out,5det}})_{3\sigma} \pm 2.7\,\mu\text{A}\,. \tag{3-60}$$

The trans-linear loop has a current gain of 1, thus the current is multiplied by the resistor $R_{\text{out}} = 8.4$ kΩ and multiplied by two by the output buffer:

$$(\Delta V_{\text{pedestal}})_{3\sigma} = (\Delta I_{\text{out,5det}})_{3\sigma} \cdot (2R_{\text{out}}) = 45 \text{ mV}, \tag{3-61}$$

which matches with a DC match simulation which yields: $(\Delta V_{\text{pedestal}})_{3\sigma} = 51$ mV.

To estimate the input noise power which is modulated by the log-amp detector, it is assumed that the channel has a finite bandwidth with an eight order pole at a frequency ω_p. Because the total BW as seen from Figure 3-15 is only 930 MHz, the effective noise BW is $B_n \sim 940$ MHz (see Appendix B-4 for derivation). For T = 300 K the calculated effective input-referred noise power is (see Appendix B-4):

$$P_{\text{in,n,eff}} = -49.5 \text{ dBm} \tag{3-62}$$

which is the power of a sinusoidal input signal which is responsible for a fixed output noise voltage. Comparing this value to the intercept point of -37.4 dBm (without the fixed pedestal) shows that noise will not be dominating the output pedestal level. This was confirmed by a transient noise simulation with a 10 GHz input noise bandwidth, rendering a noise output pedestal level of 8 mV. This result is indeed negligible versus the fixed DC pedestal level of about 0.34 V.

If the noise would be dominant, it would limit the lower part of the dynamic range, such that adding extra stages will not achieve a lower intercept point. Adding stages will only increase

the noise due to the higher gain of the channel and only extend the dynamic range to higher power levels.

The following chapter will discuss the measurement setup and show the most important measurement results.

Chapter 4

Measurements

This chapter will show the measurement setup, the results and finish with a discussion and comparison versus other log-amp detectors.

4-1 Measurement Setup

The measurement setup is given in Figure 4-1. The chip is put on a test Printed Circuit Board (PCB), which is connected to a power supply, vector signal generator and a digital multimeter. Using LabView software, the Vector Signal generator can be controlled with a General Purpose Interface Bus (GPIB) to sweep the input power, modulation and frequency. The output voltage is then measured using a digital multimeter which also connects with the GPIB interface. The measurement data is written into a ".txt" file which is read by a MATLAB script for generating the plots in this chapter. A detailed figure of the measurement setup can be seen in Figure 4-1.

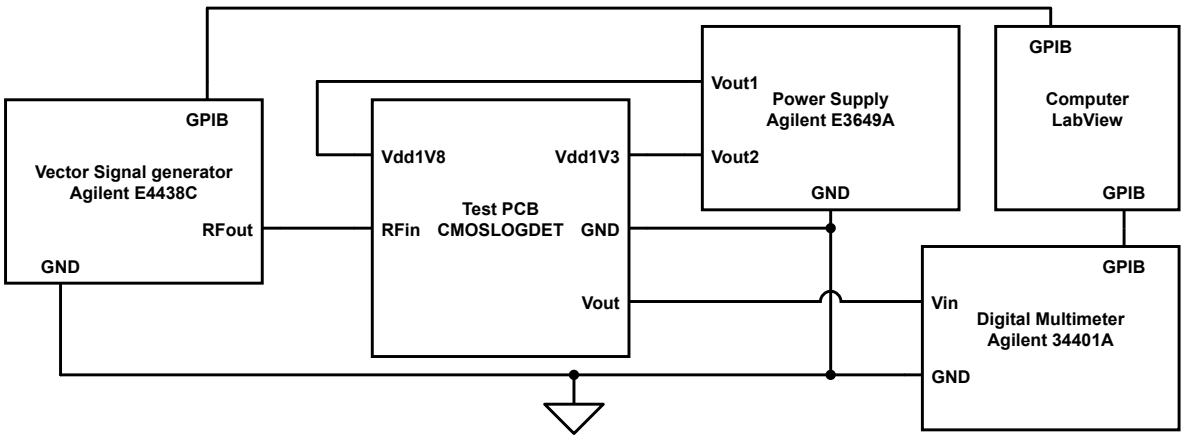


Figure 4-1: Block diagram of measurement setup

Two types of measurements were carried out:

1. A batch of 24 samples was measured for sinusoidal inputs at 100, 700, 900, 1500, 1800 and 2100 MHz over the full input power range (-50 to +10 dBm). The detection curves were obtained at -40, +25 and 85°C for a fixed 1.8 V supply voltage.
2. A batch of 3 samples was measured for sinusoidal inputs with an input power of -20, -10, 0, +10 dBm for an input frequency range from 10 MHz to 10 GHz.

Recap of most important definitions:

LCE The log-conformance error is the error in dB from an ideal logarithmic response.

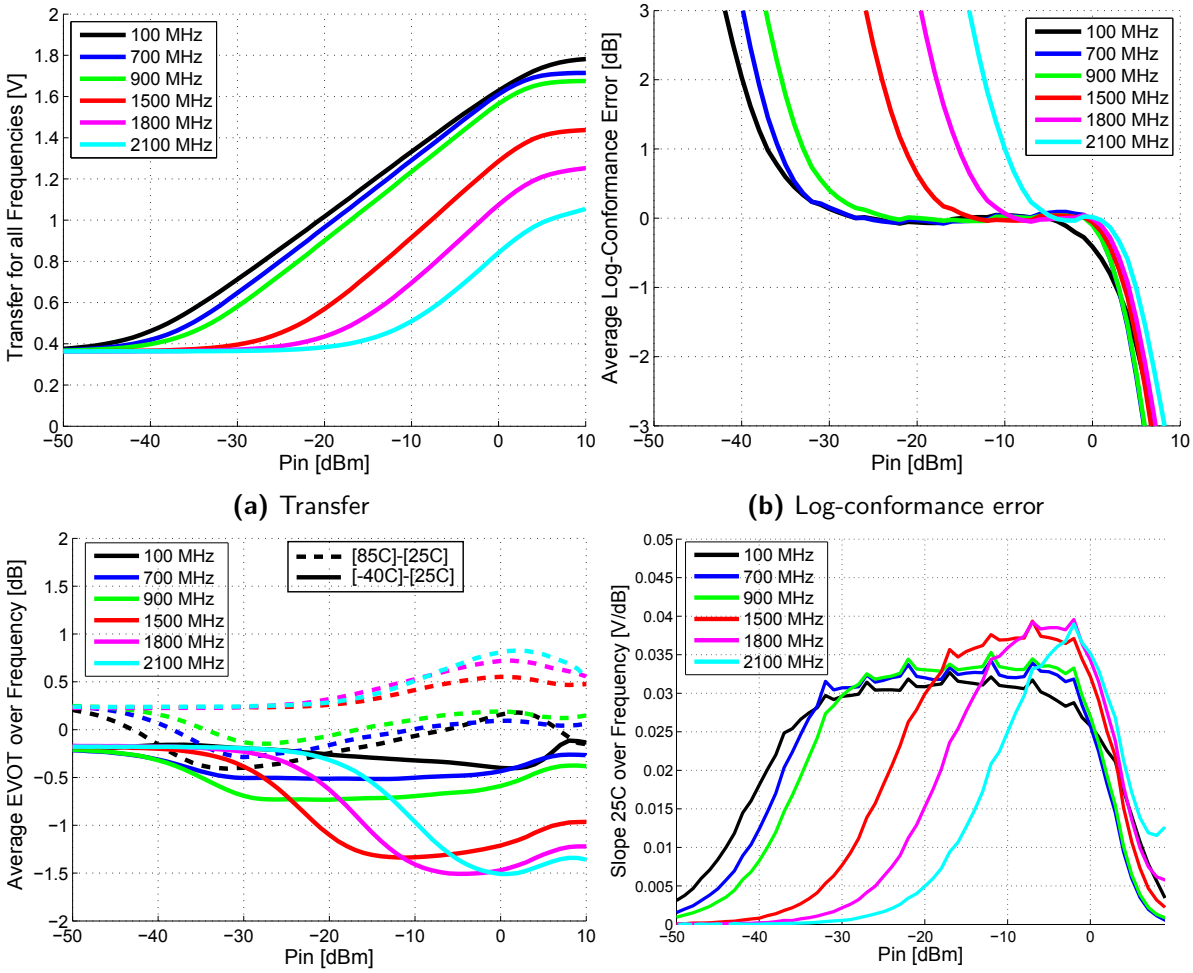
EVOT This metric shows the error in dB between the log-amp detection transfer at a certain temperature in relation to the transfer obtained at the 25°C reference temperature.

Typical The average performance of all samples for every input power.

Max Temperature Drift The error range which fits the outer boundaries of the EVOT plot for all samples.

4-2 Measurement Results

1. Figure 4-2 shows the typical (average among the 24 samples) detection (a), LCE (b), EVOT (c) and slope (d) curves for all measured input frequencies.
2. Figure 4-3 shows the frequency response for all four input powers at room temperature.
3. Figure 4-4 shows the transfer of all boards over temperature for every measured input frequency.
4. Figure 4-5 shows the typical LCE plots at -40, +25 and +85°C.
5. Figure 4-6 shows the temperature drift of all samples for the extremes of the temperature range (-40°C and 85°C) in relation to 25°C.
6. Figure 4-7 shows the distribution of the intercept point and the slope over temperature.
7. Figure 4-8 shows the distribution of the pedestal level over temperature.
8. Table 4-1 is a summary of the most performance data
9. Table 4-2 sum up non-RF specifications



(a) Transfer

(b) Log-conformance error

(c) Error variation over temperature

(d) Slope at 25°C over Frequency

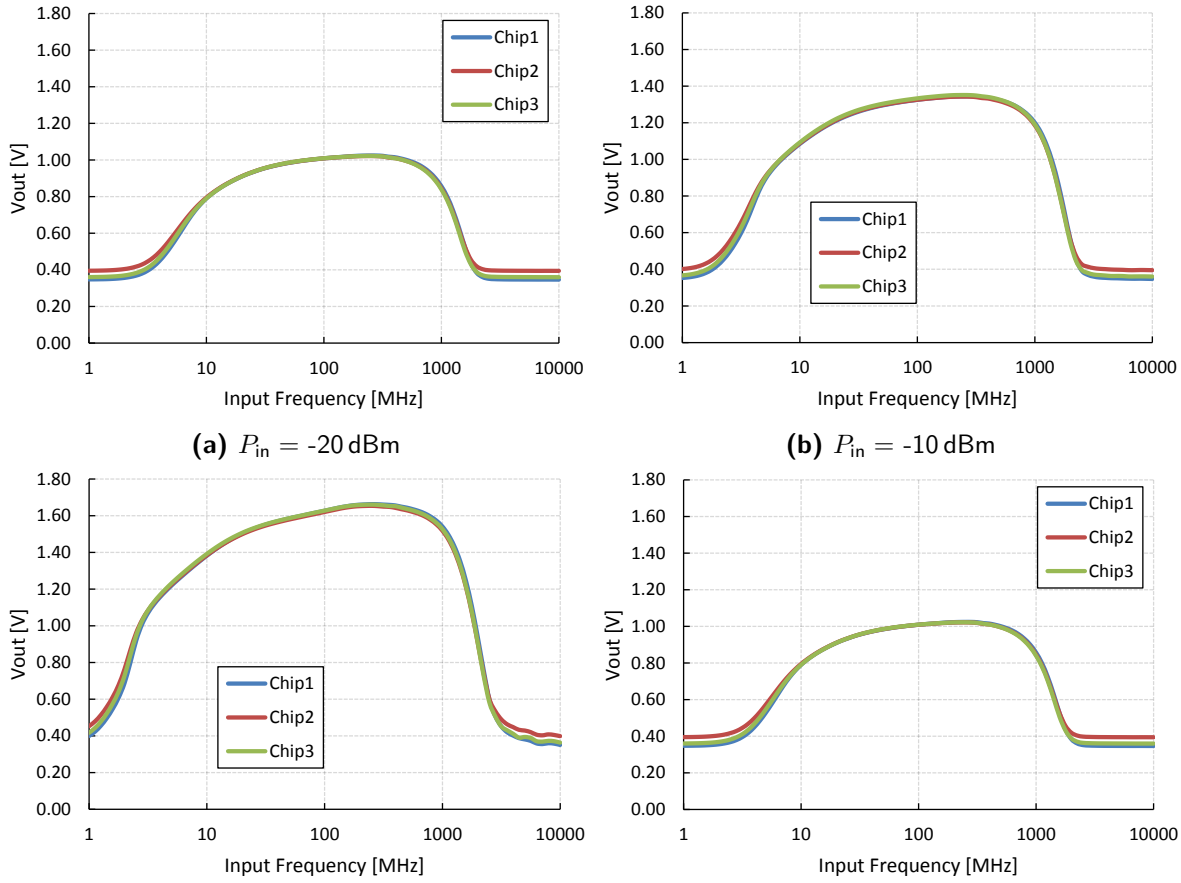
Figure 4-2: Typical performance over frequency

Frequency	0.1 GHz	0.7 GHz	0.9 GHz	1.5 GHz	1.8 GHz	2.1 GHz
DR LCE $\leq \pm 1$ dB 25C	40 dB	39 dB	36 dB	25 dB	19 dB	15 dB
DR LCE $\leq \pm 1$ dB -40/85C	38 dB	38 dB	34 dB	-	-	-
DR LCE $\leq \pm 3$ dB -40/85C	49 dB	45 dB	42 dB	30 dB	24 dB	19 dB
Max Temperature Drift (dB)	± 1.1	± 1.0	± 1.1	+1.1,-1.7	+1.4,-1.9	+1.6,-2.0

Table 4-1: Performance summary: Typical LCE and Max Temperature Drift.

Specification	Quantity
Supply Voltage	1.8 V
Power Consumption	6.3 mA
Chip Area	0.76 mm^2
Response time	6 μs

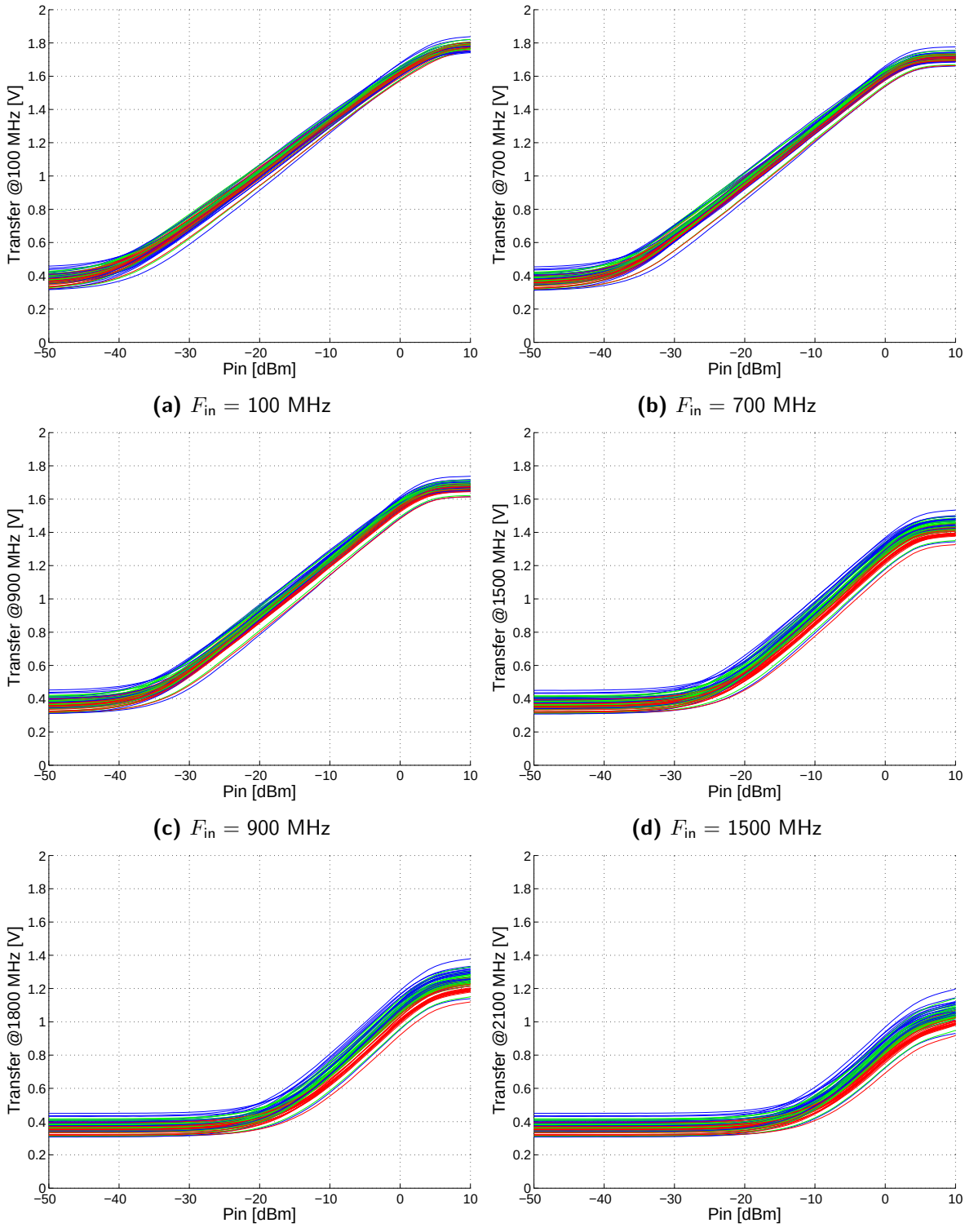
Table 4-2: Baseband Specifications



(a) P_{in} = -20 dBm **(b)** P_{in} = -10 dBm

(c) P_{in} = 0 dBm **(d)** P_{in} = 10 dBm

Figure 4-3: Output voltage over frequency at several input powers, three samples

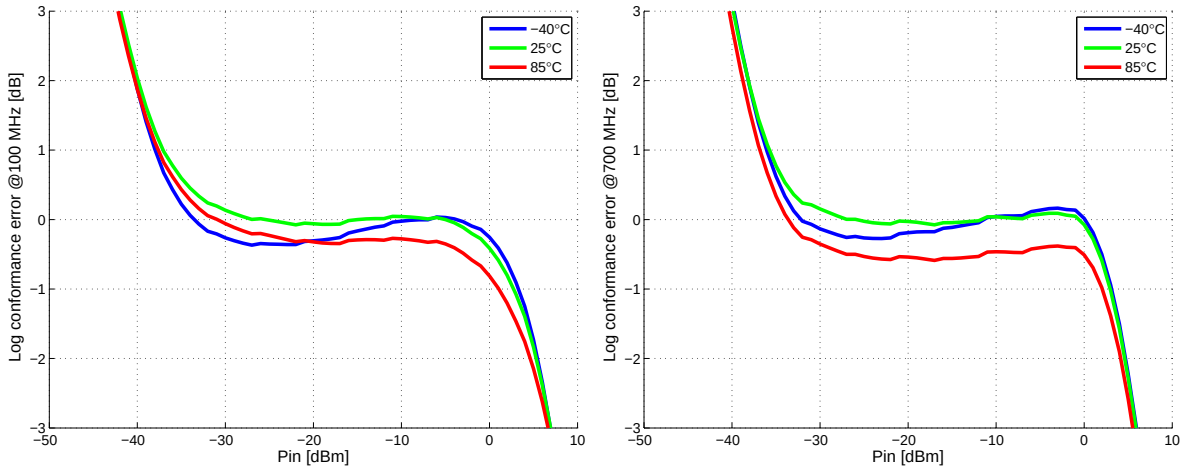


(a) $F_{\text{in}} = 100$ MHz **(b)** $F_{\text{in}} = 700$ MHz

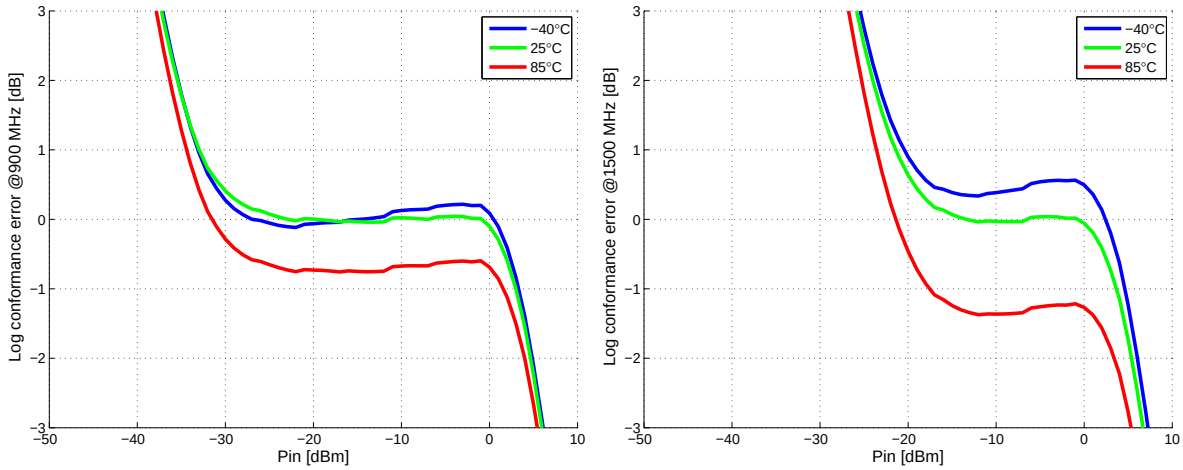
(c) $F_{\text{in}} = 900$ MHz **(d)** $F_{\text{in}} = 1500$ MHz

(e) $F_{\text{in}} = 1800$ MHz **(f)** $F_{\text{in}} = 2100$ MHz

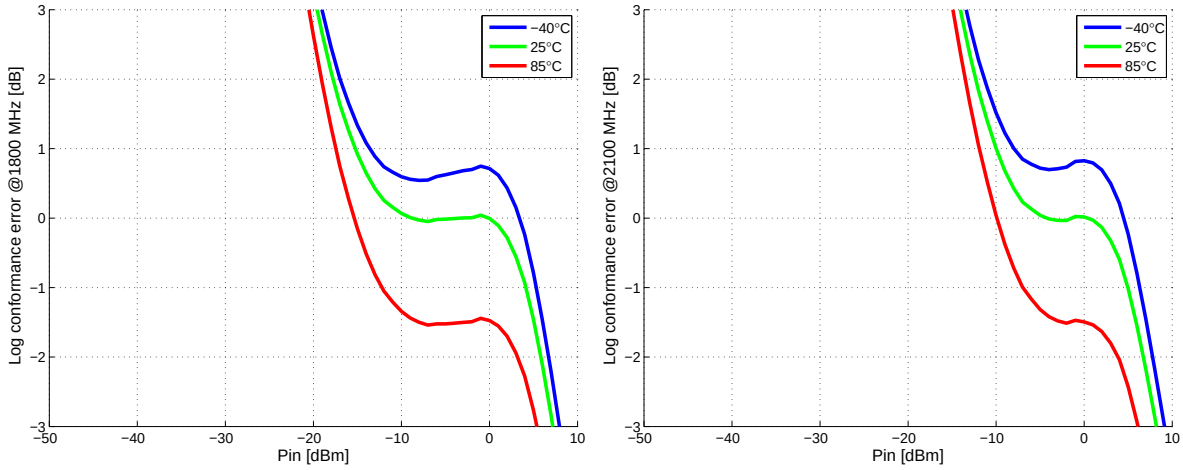
Figure 4-4: Transfer over temperature for all samples at several input frequencies [blue = -40°C, green = 25°C, red = 85°C]



(a) $F_{\text{in}} = 100$ MHz **(b)** $F_{\text{in}} = 700$ MHz

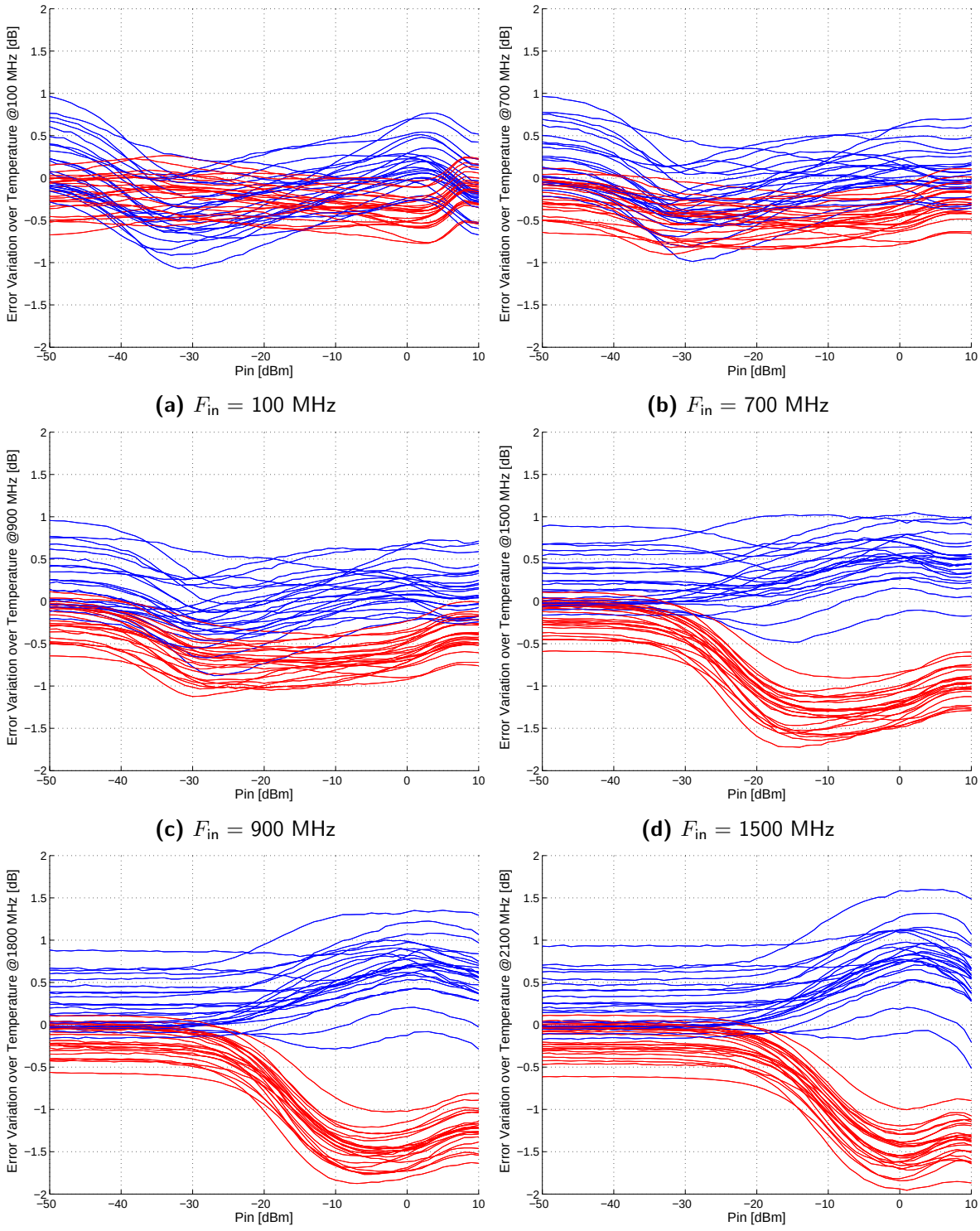


(c) $F_{\text{in}} = 900$ MHz **(d)** $F_{\text{in}} = 1500$ MHz



(e) $F_{\text{in}} = 1800$ MHz **(f)** $F_{\text{in}} = 2100$ MHz

Figure 4-5: Typical LCE performance for several frequencies

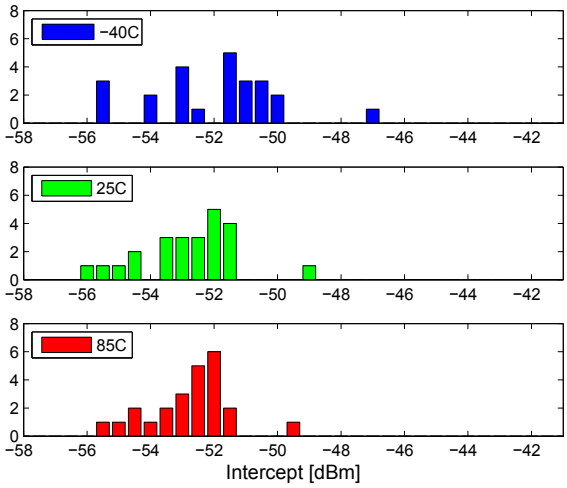


(a) $F_{\text{in}} = 100$ MHz **(b)** $F_{\text{in}} = 700$ MHz

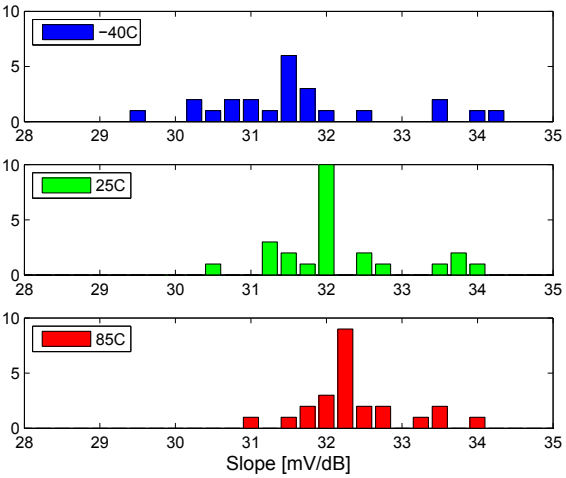
(c) $F_{\text{in}} = 900$ MHz **(d)** $F_{\text{in}} = 1500$ MHz

(e) $F_{\text{in}} = 1800$ MHz **(f)** $F_{\text{in}} = 2100$ MHz

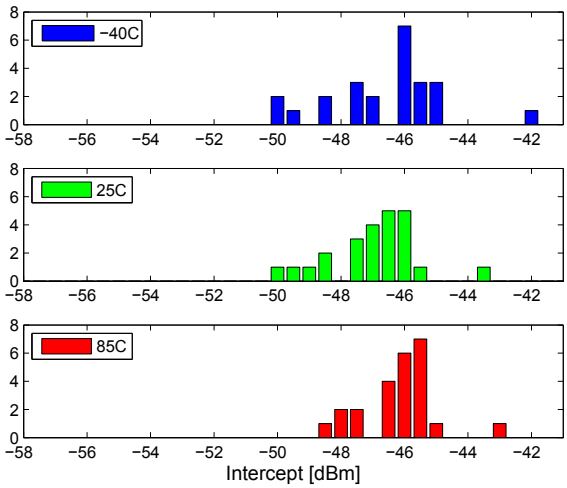
Figure 4-6: Error variation over temperature for all samples [blue = (-40°C) - (25°C), red = (85°C) - (25°C)]



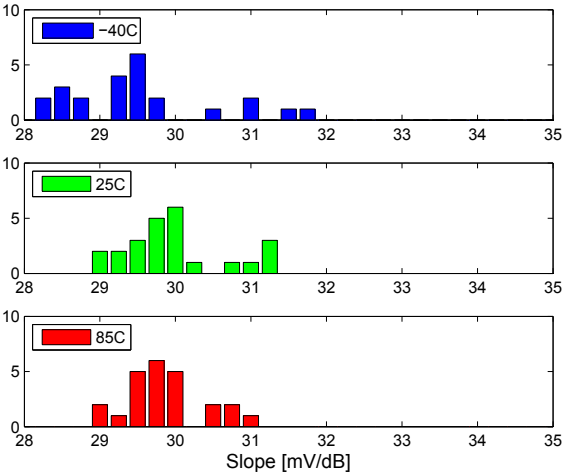
(a) Spread intercept point for $F_{\text{in}} = 100\,\text{MHz}$



(b) Spread slope for $F_{\text{in}} = 100\,\text{MHz}$



(c) Spread intercept point for $F_{\text{in}} = 900\,\text{MHz}$



(d) Spread slope for $F_{\text{in}} = 900\,\text{MHz}$

Figure 4-7: Histogram of intercept point and slope over temperature

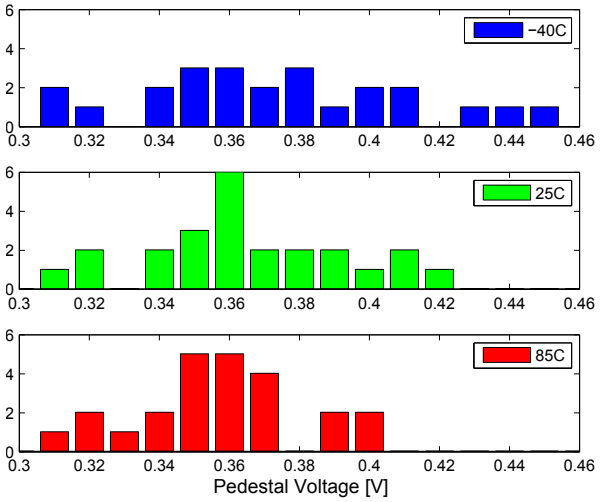


Figure 4-8: Spread output pedestal over temperature

4-3 Discussion

Bandwidth The -3 dB bandwidth of the four cascaded gain cells is around 930 MHz. This BW limitation is temperature dependent. For lower temperatures the BW is higher, which results in a temperature dependent intercept point. This degrades both the EVOT and LCE for input frequencies above 900 MHz.

Dynamic Range The DR for ± 1 dB LCE is 39 dB at 25°C for frequencies between 100 and 700 MHz. For input frequencies above the -3 dB BW of the cascaded gain cells, 930 MHz, the ± 1 dB-LCE dynamic range is reduced significantly.

Error Variation over Temperature Up to 900 MHz the temperature drift is never larger than ± 1.1 dB for all 24 measured boards. This result was achieved without employing any method of temperature calibration. For input frequencies above the -3 dB BW of 930 MHz, the temperature errors become larger because the bandwidth is temperature dependent.

For low temperatures the gain cells have a larger bandwidth, while for high temperatures this bandwidth is smaller. Hence, the gain of the gain cell becomes more temperature dependent. This affects both the intercept point and the slope.

Intercept Point The spread on the intercept point is more than expected in the calculation of Section 3-5-2, which showed that $(P_I)_{3\sigma} = -46 \pm 1.8$ dBm. This could be explained by the layout of the detector cell, which was optimized for low parasitic capacitance. The Pelgrom constant however assumes a layout optimized for offset, underestimating the input offset of the detector cells.

Slope As the slope is the conversion parameter of the log-amp detector, it is expected to be constant over samples and temperature. From the calculation of Section 3-5-1 the output slope is given by $(K_S)_{3\sigma} = 32 \pm 1$ mV/dB. The histogram of Figure 4-7 confirms that the calculation approximates the spread of the slope.

Pedestal Level The calculated output pedestal level was given by $(V_{\text{pedestal}})_{3\sigma} = 336 \pm 45$ mV. This is rather low compared to the output pedestal spread of Figure 4-8, but can be again explained by the detector-cell layout.

4-4 Performance Comparison

Log-amp detectors in bipolar technology present good temperature stability for RF applications [7, 8]. CMOS log-amps for RF power-detection so far published fail to demonstrate consistent performance over a wide temperature range [9, 10].

The CMOS log-amp detector presented in this thesis does compete in temperature stability with published bipolar log-amp detectors [7, 8] as well as commercial products of the major analog companies [2, 3, 4, 5]. These companies are Analog Devices (AD8314)[2], Texas Instruments (LMV221)[3], Linear Technology (LT5534)[4] and Maxim (MAX4001)[5].

From the results in Table 4-3, the designed CMOS log-amp detector can match products in terms of temperature performance, dynamic range, power consumption and power range. However, the CMOS log-amp detector lacks the large bandwidth of the commercial products.

Specification	This Design	AD8314	LMV221	LT5534	MAX4001
DR ±1 LCE 50-100 MHz 25°C	40 dB	46 dB	40 dB	52 dB	45 dB
DR ±1 LCE 900 MHz 25°C	36 dB	48 dB	44 dB	52 dB	45 dB
DR ±1 LCE 1800 MHz 25°C	19 dB	45 dB	43 dB	52 dB	45 dB
DR ±1 LCE 50-100 MHz -40/85°C	38 dB	43 dB	32 dB	38 dB	42 dB
DR ±1 LCE 900 MHz -40/85°C	34 dB	43 dB	34 dB	47 dB	43 dB
DR ±1 LCE 1800 MHz -40/85°C	-	38 dB	34 dB	34 dB	43 dB
F_{in} Min [MHz]	20	100	50	50	100
F_{in} Max [MHz]	900	2700	3500	3000	2500
Response Time	6 μs	70 ns	2 μs	40 ns	70 ns
Power Range (−) [dBm]	-40	-47	-45	-58	-45
Power Range (+) [dBm]	+5	-5	+2	+2	0
Power Consumption [mW]	11	12	20	19	17

Table 4-3: Performance of this design versus four commercial products [2, 3, 4, 5]

A smaller CMOS technology node would allow the extension of the bandwidth for the same current consumption, which will be investigated in the next chapter.

Chapter 5

Scaling

5-1 Process Technology

The log-amp detector was designed and produced in CMOS 0.18 μm, which is a relatively mature technology. To achieve more bandwidth (BW) for the same current consumption, two newer CMOS technology nodes were investigated: 130 nm and 65 nm.

To compare the bandwidth of different technology nodes easily, only the circuit of the gain cell is scaled. This simplification is relatively accurate because the gain cell limits the BW response in the 0.18 μm CMOS design.

In smaller CMOS processes the supply voltage decreases, leaving less room for the cascoding used in Section 3-2-2. To be able to compare the technologies fairly, the gain-cell circuit of Figure 5-1 is used. For a gain cell driven with an ideal differential input, the common-source node of the input devices is an AC-ground. Hence, an ideal current source can be used to simplify biasing.

The isolated NMOSTs used in the gain cell were modeled as normal NMOSTs for which the bulk was connected directly to the source. This was done to eliminate the body effect to reduce the voltage drop of the voltage followers, as explained in Section 3-2-2.

The voltage followers M3 and M4 in the final design were twice the size of M1 and M2, so this ratio was kept constant with scaling. To approximate detector-cell loading, the gain cells were loaded with gain cells as shown in Figure 5-2. Because in the 0.18 μm design the input capacitance of the gain cell is higher than the input capacitance of the detector cell, the capacitive load is overestimated.

5-2 Scaling Techniques

This section discusses four scaling techniques which are used to scale the circuit of the gain cell. The length of the input devices in the gain cell are always fixed to the minimum gate length of the technology, to achieve maximum Bandwidth (BW).

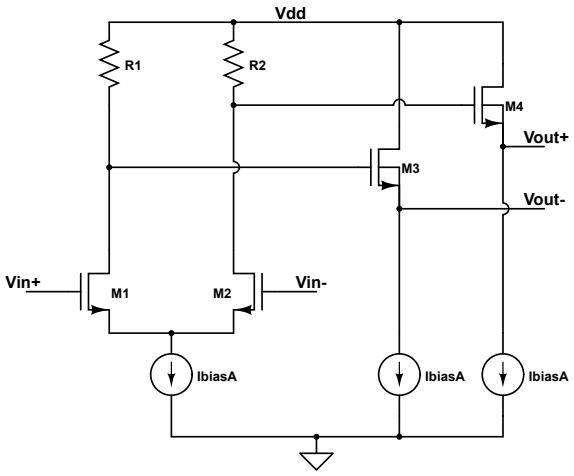


Figure 5-1: Schematic of gain cell used for scaling

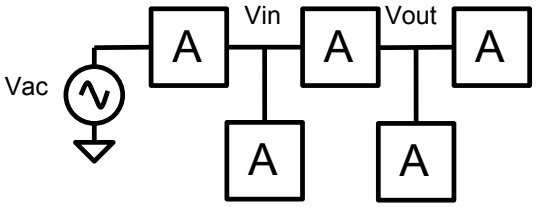


Figure 5-2: Block diagram of bandwidth simulation

Constant-g_m scaling This type of scaling changes W/L ratio of M1 and M2 inside the gain cell, to keep their trans-conductance equal to the 0.18 μm design.

Constant-W/L scaling This type of scaling keeps the W/L ratio constant.

Constant-overdrive scaling This type of scaling keeps the overdrive voltage of input devices M1 and M2 equal over technology.

Constant-Pelgrom scaling This type of scaling keeps the input-referred offset constant. Smaller nodes have a thinner oxide, which reduces the Pelgrom constant according to $A_{\mathrm{Vth}} \sim t_{\mathrm{ox}}$[1]. The width is adjusted to meet the offset value.

5-3 Methodology

To fairly compare the technologies, it is important that the scaled gain cells have enough voltage headroom for a real current source. Therefore, the minimum drain voltage of the current source is assumed to be 50 mV. In both 130 nm and 65 nm source degeneration on the current source would be much harder, if not impossible, due to the lower supply voltage.

Plan

1. The gain cell is sized according to the scaling method
2. The resistors R1 and R2 are adjusted to meet $A = 10\,\mathrm{dB}$
3. Multiple gain cells are connected according to Figure 5-2
4. The bandwidth and gain is measured between V_{in} and V_{out} of Figure 5-2

Because a gain of 10 dB was not always possible, the figure of merit for comparing the bandwidth is the Gain-Bandwidth (GBW).

[1]Parameter t_{ox} is the oxide thickness.

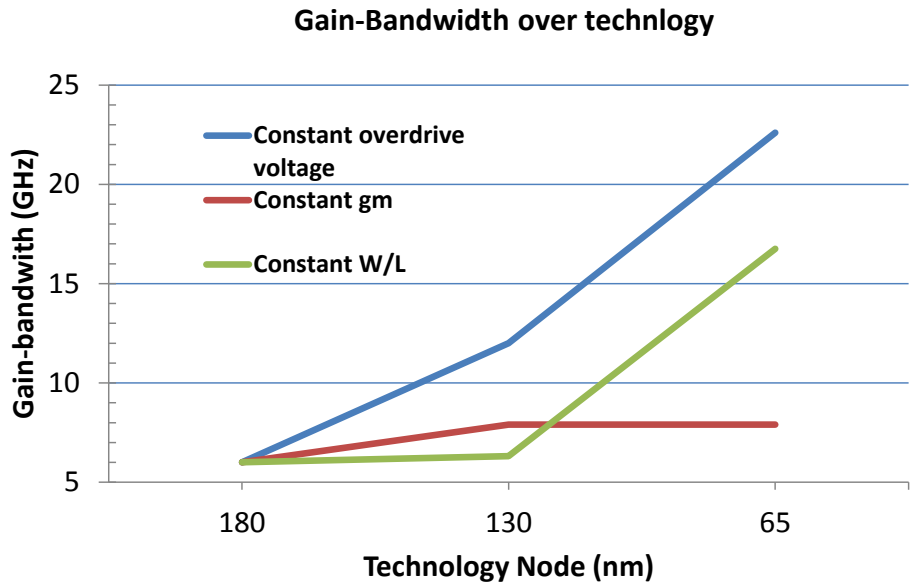


Figure 5-3: Gain-bandwidth for $L = 180\,\text{nm}$, $130\,\text{nm}$ and $65\,\text{nm}$, $I_{\text{bias-A}} = 200\,\mu\text{A}$.

Bandwidth for the same power consumption Figure 5-3 shows the GBW for a fixed power consumption.

Constant-g_m scaling does not benefit from the transition from 130 nm to 65 nm. This is because the gate width needed to be increased substantially to achieve the same trans-conductance as in the 180 nm design. This significantly increased the parasitic capacitance of the transistors, canceling the effect of the smaller gate length. Additionally, resistors $R1$ and $R2$ needed to be increased to cancel the effect of the reduce in output impedance.

Constant-W/L scaling improved the GBW from 180 nm to 130 nm, but did not improve when moving to the 65 nm technology. For the same current and W/L ratio the trans-conductance significantly dropped, as well as the output impedance for the 65 nm technology. Hence, to keep the gain constant the resistors needed to be increased significantly, lowering the bandwidth.

The constant-overdrive scaling seems to benefit most in terms of GBW. This is because the gate width of the input transistors was reduced more than with constant-W/L scaling, to achieve overdrive voltages around zero (the overdrive voltage in the 0.18 μm design). Therefore, the parasitic capacitances reduced more rapidly than was expected by keeping the same W/L ratio. Due to this rapid reduction in area the GBW increased substantially for both 130 nm and 65 nm technology.

Because the oxide thickness did not scale directly proportional to the gate length, Pelgrom constant A_{Vth} only decreased slightly. Hence, constant-Pelgrom scaling did not improve the GBW, as the area of the transistors of the gain cell needed to be nearly equal over technology to keep the input offset equal.

Current savings For a smaller CMOS process the current consumption of the gain cell can be reduced, while keeping the same GBW.

As the drain current is lowered with constant-g_m scaling, the trans-conductance reduces. Hence, the width of the transistor is increased to keep the same trans-conductance. Both effects reduce the current density and will push the input transistors more to weak-inversion.

For constant-W/L as well as constant-Pelgrom scaling the current density is reduced only by lowering the drain current. Hence, also with this type of scaling the biasing conditions of the transistor change towards weak-inversion.

Only for constant-overdrive scaling the current density is kept more or less constant. When the drain current is lowered the width of the input transistors is reduced to keep the overdrive voltage constant. Because the operating region of the transistors does not change, the PTIM temperature scheme used in the 0.18 μm design is still valid. Therefore, constant-overdrive scaling was picked as the scaling method to investigate the reduction in current consumption for newer technology nodes.

Figure 5-4 shows that with constant-overdrive scaling the newer technology nodes really help to significantly reduce the current consumption for a certain GBW.

Table 5-1 shows the estimated performance of the log-amp detector in 130 nm and 65 nm technology. The power consumption reduces proportional to the supply voltage.

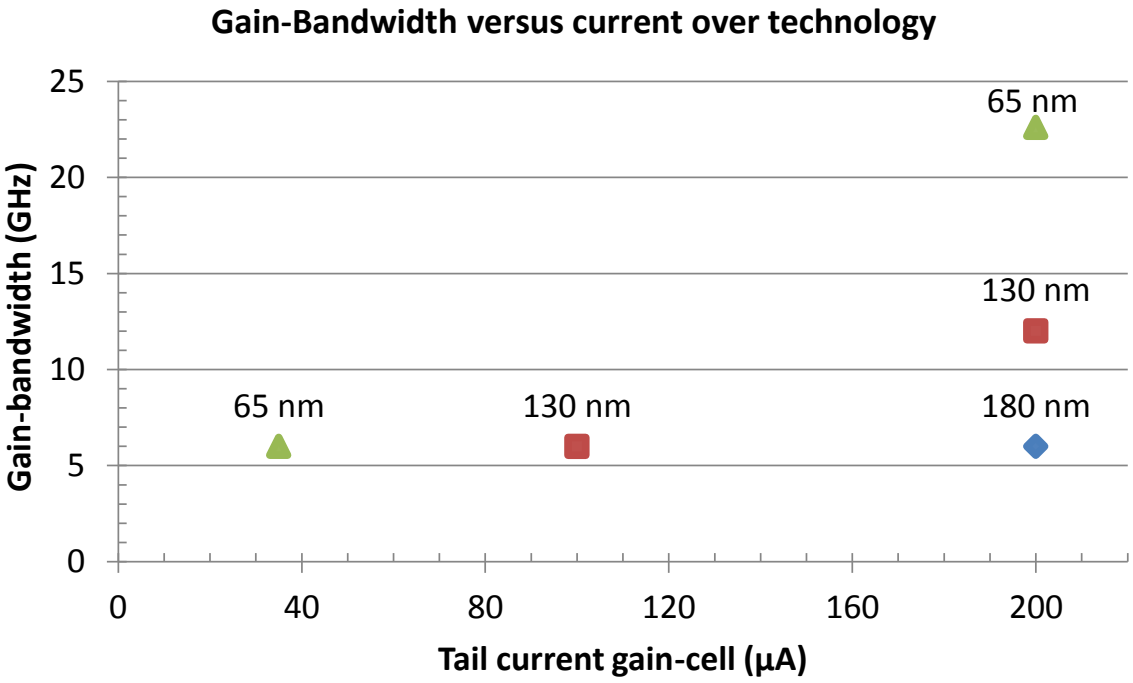


Figure 5-4: Gain-bandwidth versus current consumption, constant-overdrive scaling

5-4 Effects of scaling

Sub-threshold Biasing As supply voltages scale down more rapidly than the threshold voltages of the devices, it becomes more attractive to bias in weak-inversion to make the most use of the available voltage headroom.

Specification	0.18 μm design	130 nm design	65 nm design
DR $\pm$1 LCE 50-100 MHz 25°C	40 dB	40 dB	40 dB
F_{in} Min	20 MHz	20 MHz	20 MHz
F_{in} Max	0.9 GHz	1.8 GHz	3.4 GHz
Supply Voltage	1.8 V	1.6 V	1.2 V
Power Consumption	11 mW	9.8 mW	7.3 mW

Table 5-1: Performance estimation for newer CMOS processes (130 nm and 65 nm)

In sub-threshold the current through a CMOS transistor is defined as (see Appendix C):

$$I_D = I_0 e^{\left(\frac{V_{\text{GS}}}{nV_T}\right)}, \tag{5-1}$$

where I_0 is the drain current at $V_{\text{GS}} = V_{\text{TH}}$, n is the slope factor given by $1 + C_{\text{D}}/C_{\text{ox}}$ and V_T is the thermal voltage.

This gain of a differential pain for sub-threshold biasing (see Appendix C)

$$A = g_m \cdot R = \frac{I_D}{nV_T} \cdot R, \tag{5-2}$$

where $V_T = kT/q$.

Thus a PTAT temperature scheme should be applied, yielding the same scheme as in bipolar log-amp detectors. To step to smaller CMOS nodes, this is how the design should be implemented.

Matching Although matching becomes better as the oxide thickness decreases, according to $A_{\text{Vth}} \sim t_{\text{ox}}$ [12], the reduction in t_{ox} does not make up for the reduction in area with constant-overdrive scaling. Therefore, matching becomes worse for smaller nodes with constant-overdrive scaling. However, matching in the channel was not considered to be important because the offset-cancellation loop nullifies the output offset of the channel.

Constant-Pelgrom scaling could be used to keep the input-offset constant. The increase in GBW for this type of scaling is however heavily dependent on the scaling of Pelgrom constant A_{Vth}. Which did not render a satisfying GBW increase for the given process technologies

The following chapter will investigate a new type of temperature-compensation scheme.

Chapter 6

Proportional to mobility temperature compensation

In Chapter 2 the PTIM temperature compensation was introduced. Its temperature performance was shown in Chapter 4. A new temperature-compensation scheme will be derived in this chapter called proportional to mobility (PTM) temperature compensation.

6-1 Architecture

In the new proportional to mobility (PTM) temperature scheme it is assumed that the gain cell is biased exactly as with the PTIM temperature scheme, as discussed in Chapter 2. Only the biasing of the detector cell will be modified, as will be explained in the following paragraph.

Principle The intercept point of the log-amp detector was given by:

$$V_I = \frac{E_{\text{kD}}}{S(T)A^{N+D_0+B_0-1}}\,, \tag{6-1}$$

in which B_0 the bottem-end correction factor, D_0 the top-end correction factor, N the number of stages, $S(T)$ the transfer of the RF input scaler and for which $E_{\text{kD}} < \max(V_{\text{out-A}})$.

Using the PTIM scheme to bias the gain cell the denominator of (6-1) is already constant over temperature. If transfer $S(T) = 1$ and if knee voltage E_{kD} is temperature independent, then the intercept point would remain constant over temperature as well. Equation 6-3 shows the knee voltage of the detector cell. If bias current $I_{\text{bias-D}}$ would be PTM instead of PTIM:

$$I_{\text{bias-D,PTM}}(T) = I_{0D}\left(\frac{T}{T_{\text{ref}}}\right)^{-N_\mu}, \tag{6-2}$$

where $1.5 \leq N_\mu \leq 2$ and I_{0D} is the bias current at T_{ref}.

Substituting bias current $I_{\text{bias-D,PTM}}$ in the equation of the knee voltage of the detector cell results to:

$$E_{\text{kD}}(T) = 2\sqrt{\frac{I_{\text{bias-D}}(T)}{\beta(T)}} \tag{6-3}$$

$$= 2\sqrt{\frac{I_{0\text{D}}}{\beta_0}}, \tag{6-4}$$

where $\beta(T) = \beta_0(T/T_{\text{ref}})^{N_\mu}$.

Hence, with the PTM bias current the knee voltage of the detector cell is temperature dependent rendering the intercept point temperature independent. This eliminates the resistor divider inside the RF input block of Section 3-2-1, which was needed in the PTIM compensation scheme. As the resistor divider can be eliminated, only a 50 Ω input resistor is needed to match the output impedance of the coupler. This is an advantage because the resistors in the resistor divider of the RF input block should match the temperature behavior of the transistors, which are both dependent on technology.

The disadvantage of the PTM scheme is that knee voltage E_{kD} will not follow the output swing of the gain cell, $\max(V_{\text{out-A}})$, which still is PTIM, as shown in Figure 6-1. The maximum voltage swing of the gain cell, $\max(V_{\text{out-A}})$, should now be larger such that in the worst case, at -40°C, it will still saturate the detector cell to adhere to $E_{\text{kD}} < \max(V_{\text{out-A}})$. If this condition is violated the effective knee voltage will change over temperature, according to (2-32); for low temperatures the effective knee voltage would be equal to $\max(V_{\text{out-A}})$, while for high temperatures E_{kD} is dominant. Hence, the intercept point increases for high temperature and vice versa.

The maximum output current of the detector cell is now PTM temperature dependent (Figure 6-2a), thus a PTIM current scaler is needed at the output of the detector cells, opposite to the PTM current scaler needed for the PTIM scheme.

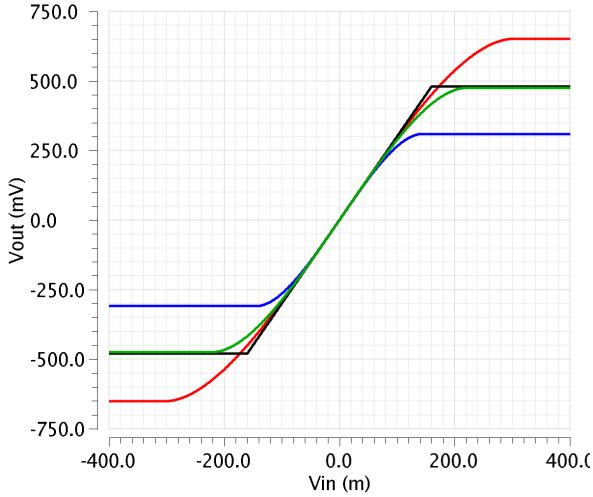
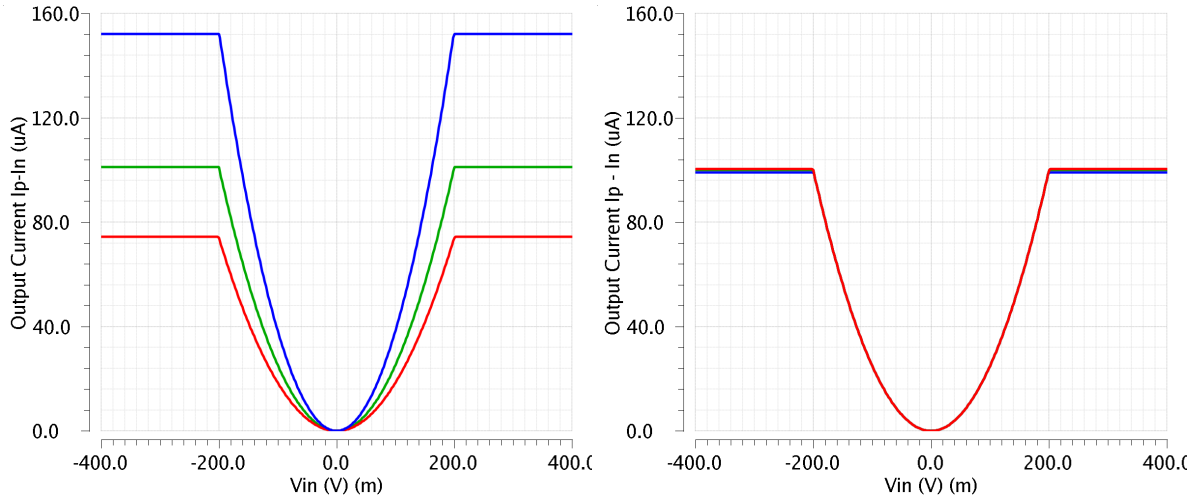


Figure 6-1: Transfer of gain cell with PTIM bias current [blue = -40°C, green = 25°C, red = 85°C, black = ideal transfer]



(a) Output detector cell with a PTM $I_{\text{bias-D}}$ bias current

(b) Output detector cell with a PTM $I_{\text{bias-D}}$ bias current and PTIM output current scaler

Figure 6-2: Output of detector cell with the PTM temperature scheme [blue = -40°C, green = 25°C, red = 100°C]

Parameter	PTIM	PTM
$I_{\text{bias-A}}(T) =$	$I_{0A}(\frac{T}{T_{\text{ref}}})^{N_\mu}$	$I_{0A}(\frac{T}{T_{\text{ref}}})^{N_\mu}$
$I_{\text{bias-D}}(T) =$	$I_{0D}(\frac{T}{T_{\text{ref}}})^{N_\mu}$	$I_{0D}(\frac{T}{T_{\text{ref}}})^{-N_\mu}$
$A(T) =$	$\sqrt{\beta_0 I_{0\text{A}}} R_c$	$\sqrt{\beta_0 I_{0\text{A}}} R_c$
$E_{\text{kD}}(T) =$	$\sqrt{\frac{I_{0D}}{\beta_0}}(\frac{T}{T_{\text{ref}}})^{N_\mu}$	$\sqrt{\frac{I_{0D}}{\beta_0}}$
$S(T)$	$\sim S_0(\frac{T}{T_{\text{ref}}})^{N_\mu}$	1

Table 6-1: Summury of important parameters: PTIM and PTM, strong-inversion model

Figure 6-2a shows the detector cell transfer after PTM biasing. The knee voltage is constant over temperature. After a PTIM output current scaler the output of the detector cell is shown in Figure 6-2b. As expected, the transfer in this figure is temperature independent without the use of an input scaler in RF input block.

Table 6-1 sums up the difference of PTIM versus PTM for the most important input parameters.

Generating the PTM bias current Although the model from (6-3) is valid for strong inversion operation, it is important to realize that the transistors of the detector cell do not operate in this region continuously. As the input deviates from the stable zero condition, the current density of the transistors inside the detector cell changes significantly. This means that the transistors will operate in both strong, moderate and weak inversion.

This effect has an influence on the effective transfer curve of the detector cell, as the transition to maximum output current will be not as steep as predicted with the strong-inversion model. For a detector cell in which all transistors operate continuously in weak inversion the output

is given by (Appendix D):

$$I_{\text{out-D}} = I_{\text{bias-D}} \cdot \left(\frac{e^{\frac{V_{\text{in+}}}{nV_T}} + e^{\frac{V_{\text{in-}}}{nV_T}} - 2e^{\frac{V_{cm}}{nV_T}}}{e^{\frac{V_{\text{in+}}}{nV_T}} + e^{\frac{V_{\text{in-}}}{nV_T}} + 2e^{\frac{V_{cm}}{nV_T}}} \right), \tag{6-5}$$

where n is the slope factor given by $1 + C_D/C_{\text{ox}}$, V_{cm} is equal to $\frac{V_{\text{in+}}+V_{\text{in-}}}{2}$ and V_T is the thermal voltage.

Equation (6-5) yields a detector-cell output which is directly proportional to the bias current and with a fixed knee voltage V_T. While for the strong-inversion model the output current of the detector cell is given by:

$$I_{\text{out-D}}\ [A] = \begin{cases} \frac{\beta}{4} V_{\text{in-D}}^2, & \text{if } E_{\text{kD}} < V_{\text{in-D}}\,, \\ I_{\text{bias-D}}, & \text{if } E_{\text{kD}} \geq V_{\text{in-D}}\,. \end{cases} \tag{6-6}$$

Hence, when the input of the detector cell is below the knee voltage the output current is independent of the bias current for strong inversion.

In reality, as the input increases, some input transistors will be biased more towards strong inversion, while others move into weak inversion. To generate bias current $I_{\text{bias-D}}$ for the detector cell, an open-loop bias generator would be very difficult. This is because all temperature effects in the input transistors of the detector cell should be accounted for to generate this special PTM current. A feedback bias configuration would be able to generate a bias current to fix the output current of the detector cell.

The closed-loop system in Figure 6-3 controls bias current $I_{\text{bias-D}}$ such that output voltage $V_{\text{out-D}}$ is equal to reference voltage V_{ref2}, for a certain input voltage V_{ref1}. This input reference voltage at the input of the detector cell biases the detector cell to about half its knee voltage, E_{kD}. The loop ensures that for every temperature bias current $I_{\text{bias-D}}$ is controlled to keep $V_{\text{out-D}}$ constant.

The transfer of a detector cell biased with PTM bias current $I_{\text{bias-D}}$ and terminated with the back-end and output resistor is shown in Figure 6-4. From this figure is becomes apperent that the bias loop is able to control two points, one point at $V_{\text{in-D}} = \frac{E_{\text{kD}}}{2}$ and the maximum output current, $I_{\text{bias-D}}$. Naturally, the detector-cell output is zero at zero input voltage, which sums up to a three-point fixed transfer over temperature.

The architecture for the PTM scheme is equal to the PTIM scheme, except for the RF input block and the PTIM current scaler, as shown Figure 6-5.

Stability A positive and a negative feedback loop exist in Figure 6-3. To ensure stable behavior, the negative feedback loop is made stronger than the positive one. This has been established by increasing the size (2X) of the current source in Figure 6-3.

6-2 Circuit Design

6-2-1 Gain Cell

The gain cell was modified to increase the output swing, to ensure $E_{\text{kD}} < \max(V_{\text{out-A}})$. To allow a bigger output swing the cascodes were removed as well as the source degeneration, to

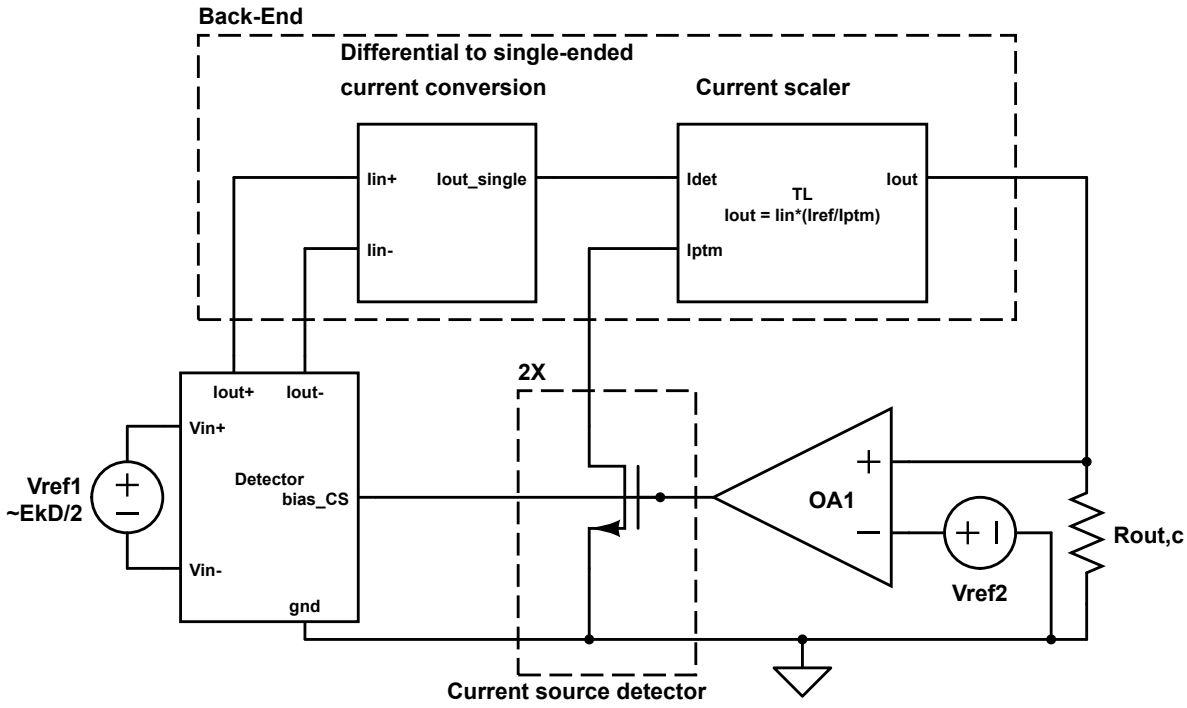


Figure 6-3: Bias-generator loop of PTM temperature scheme

maximize the available voltage headroom. This is at the cost of temperature compensation for gain, bandwidth and matching. The current consumption was increased by 50% for achieving a larger maximum output swing and to increase bandwidth.

6-2-2 Detector Cell

The PTM scheme is based on the strong inversion behavior of the detector cell. The PTIM design used a relatively large W/L ratio which resulted in a relatively low current density. Due to this the transistors operate close to weak inversion, which according to (6-5) has a fixed knee voltage V_T. This effects causes the knee voltage to be relatively insensitive to changes in the bias current. Using the bias loop of Figure 6-3 results in a bias current with a huge temperature sensitivity: from -40 to 85°C the bias current changed by a factor of $40X$.

By reducing the W/L ratio but keeping the area of the input devices approximately equal, the current density was increased significantly (∼30x). This reduces the bias current range over temperature generated by the PTM generator because the transistors were biased more to strong inversion, significantly increasing the knee voltage sensitivity to bias current $I_{\text{bias-D}}$. Finally, the ratio from -40 to 85°C was reduced to a factor $3X$, which is much more practical.

6-3 Simulation Results versus PTIM

In this section the EVOT of the PTIM and PTM temperature schemes are compared for 100 MHz and 900 MHz.

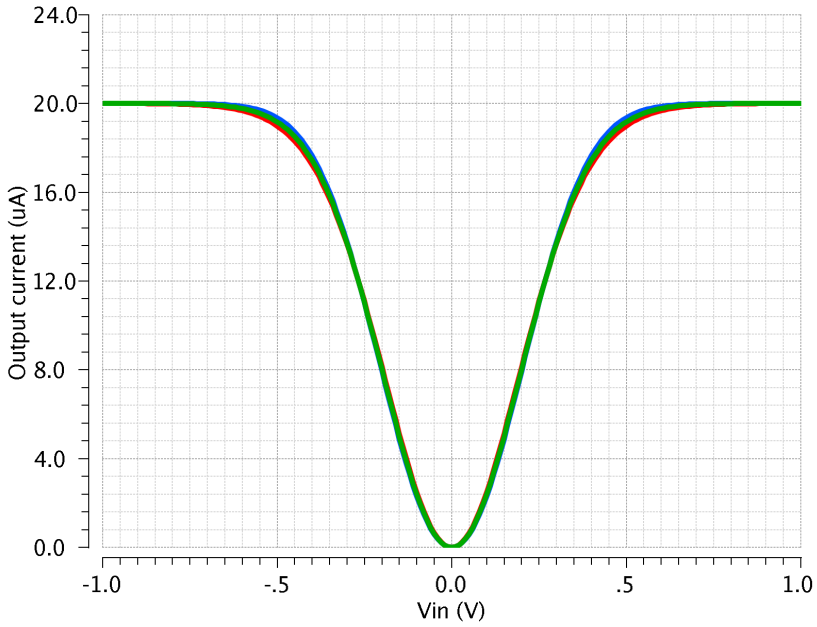


Figure 6-4: Simulated DC output detector cell after the back-end [blue = -40°C, green = 25°C and red = 85°C]

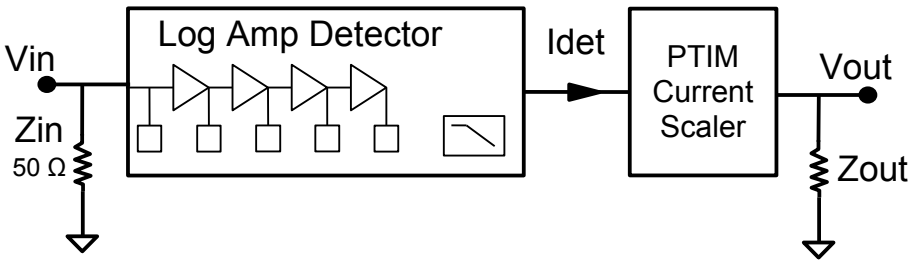


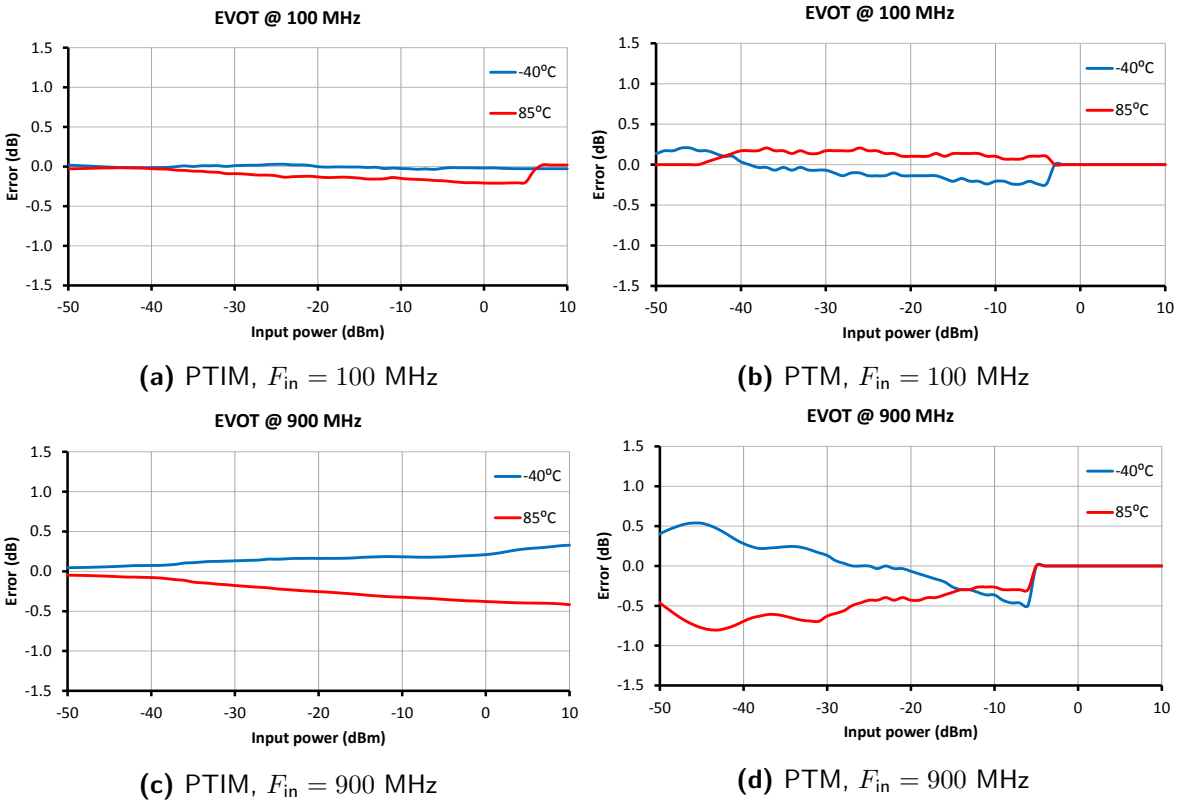
Figure 6-5: Architecture of PTM temperature-compensation scheme

6-4 Discussion

For low input frequencies, the temperature performance is comparable to the PTIM temperature scheme. Due to the modifications in the circuit of the gain cell to increase the maximum output swing, its bandwidth reduced. Hence, the temperature drift increased significantly for 900 MHz.

The cause of low-frequency degradation in temperature performance is the removal of the cascodes, to increase the output voltage swing of the gain cell. As indicated in Section 3-3-1, the addition of the cascodes reduced the temperature error from 0.5 dB to 0.1 dB over temperature.

Clearly, in terms of performance the PTIM scheme is better. Mostly because the PTIM scheme does not need gain cells with a high output swing, which results in a higher BW and better temperature performance. Still the PTM scheme achieves reasonable temperature performance with an EVOT within ±0.8 dB up to 900 MHz.



(a) PTIM, $F_{\text{in}} = 100$ MHz

(b) PTM, $F_{\text{in}} = 100$ MHz

(c) PTIM, $F_{\text{in}} = 900$ MHz

(d) PTM, $F_{\text{in}} = 900$ MHz

Figure 6-6: Error variation over temperature for PTIM and PTM

Advantages of PTM

- No need for technology-dependent resistor divider in RF input scaler
- Lower intercept point because no attenuator is present at the input: $S(T) = 1$

Disadvantages compared to PTIM

- Requires large output swing of gain cells, reducing BW
- More area due to second back-end for PTM current generation

Chapter 7

Conclusion

A complete implementation of an RF power detector in 0.18 μm CMOS technology based on the log-amp detector architecture was demonstrated. Using proportional to inverse mobility temperature compensation, the temperature drift is reduced significantly.

The measured prototype IC has an input power range from -50 to +10 dBm for RF signals ranging from 100 MHz to 1.8 GHz. This design attains a typical dynamic range of 39 dB for a $\pm$1 dB log-conformance error (LCE). Up to 900 MHz the temperature drift is never larger than $\pm$1.1 dB for all 24 measured samples over a temperature range from -40 to +85°C. The current consumption is 6.3 mA from an 1.8 V power supply and the chip area spans 0.76 mm^2.

The CMOS log-amp detector presented in this thesis does compete in temperature stability with published bipolar log-amp detectors as well as commercial products.

Newer CMOS nodes were tested to give an understanding of the scalability of this design. Simulations show that using 65 nm CMOS technology the bandwidth can be increased significantly (up to 3X), with a 33% reduction in power consumption.

A new temperature scheme was introduced, which uses proportional to mobility biasing to stabilize the output of the log-amp detector over temperature. This removes the need for the RF input block in the design. Simulations show that the temperature drift is bounded to $\leq$ 0.8 dB.

My Contributions

- Circuit design and layout of log-amp detector with temperature compensation
- Measurements of the log-amp detector
- New temperature compensation scheme, PTM
- Investigation on the bandwidth and current consumption of smaller CMOS nodes
- Analytical expression for:

  - the intercept-point shift for smooth gain-cell and detector-cell transfers
  - an approximation of the bottom-end correction factor
  - the top-end correction factor for different types of detector cells

Further Research

- Further improve the 0.18 μm design in terms of bandwidth, to be able to compete with commercial products of today
- Implement design in smaller CMOS process, to further increase the bandwidth performance
- Designing a prototype IC of a log-amp detector with the PTM temperature scheme

Appendix A

Architecture

A-1 Output Model Log-Amp

By taking one point of the curve V_{out1}:

$$(X_1, Y_1) = \left(\frac{E_{\text{kA}}}{A^{N-1}}, E_{\text{kA}}(A + 1 + \frac{1}{A} + ... + \frac{1}{A^{N-1}}) \right), \tag{A-1}$$

in which N is number of stages.
Output equation and the slope K_S:

$$V_{\text{out}} = K_S \log\left(\frac{V_{\text{in}}}{V_I}\right), \tag{A-2}$$

$$K_S = \frac{AE_{\text{kA}}}{\log(A)}. \tag{A-3}$$

It follows that:

$$E_{\text{kA}}\left(A + 1 + \frac{1}{A} + ... + \frac{1}{A^{N-1}}\right) = \frac{AE_{\text{kA}}}{\log(A)} \cdot \log\left(\frac{\frac{E_{\text{kA}}}{A^{N-1}}}{V_I}\right), \tag{A-4}$$

$$\left(1 + \frac{1}{A} + \frac{1}{A^2} + ... + \frac{1}{A^N}\right)\log(A) = \log\left(\frac{\frac{E_{\text{kA}}}{A^{N-1}}}{V_I}\right), \tag{A-5}$$

$$(A-1)\left(1 + \frac{1}{A} + \frac{1}{A^2} + ... + \frac{1}{A^N}\right)\log(A) = (A-1)\log\left(\frac{\frac{E_{\text{kA}}}{A^{N-1}}}{V_I}\right), \tag{A-6}$$

$$\frac{A - (1/A^N)}{A-1}\log(A) = \log\left(\frac{\frac{E_{\text{kA}}}{A^{N-1}}}{V_I}\right), \tag{A-7}$$

$$\log(A^{\frac{A-(1/A^N)}{A-1}}) = \log\left(\frac{\frac{E_{\text{kA}}}{A^{N-1}}}{V_I}\right), \tag{A-8}$$

$$\tag{A-9}$$

for large values of N, the $1/A^N$ part is tiny, thus V_I can be approximated by:

$$V_I \sim \frac{E_{\text{kA}}}{A^{N+\frac{1}{A-1}}}. \tag{A-10}$$

A-2 Output Model with Top-End Correction

By taking one point of the curve V_{out1}:

$$(X_1, Y_1) = \left(\frac{E_{\text{kA}}}{A^{N-1}}, AE_{\text{kA}}D_0\right), \tag{A-11}$$

in which N is number of stages and $D_0 = A/(A-1)$, the top-end correction factor.
Using the same methodology as A-1:

$$V_{\text{out}} = K_S 20 \log\left(\frac{V_{\text{in}}}{V_I}\right), \tag{A-12}$$

$$K_S = \frac{AE_{\text{kA}}}{20\log(A)}. \tag{A-13}$$

It follows that:

$$AE_{\text{kA}}D_0 = \frac{AE_{\text{kA}}}{\log(A)} \cdot \log\left(\frac{\frac{E_{\text{kA}}}{A^{N-1}}}{V_I}\right), \tag{A-14}$$

$$D_0 \log(A) = \log\left(\frac{\frac{E_{\text{kA}}}{A^{N-1}}}{V_I}\right), \tag{A-15}$$

$$\log(A^{D_0}) = \log\left(\frac{\frac{E_{\text{kA}}}{A^{N-1}}}{V_I}\right), \tag{A-16}$$

$$V_I = \frac{E_{\text{kA}}}{A^{N-1+D_0}}, \tag{A-17}$$

such that for $D_0 = A/(A-1)$:

$$V_I = \frac{E_{\text{kA}}}{A^{N+1/(A-1)}}. \tag{A-18}$$

A-3 Output Model for G_m Log-Amp

Every G_m cell contributes to the output voltage with one $I_{\text{bias-G}}R_{\text{out}}$, similar to AE_{kA} for a gain cell, which results in a slope for a voltage input as:

$$K_S = \frac{I_{\text{bias-G}}R_{\text{out}}}{\log(A)}. \tag{A-19}$$

Using the same methodology as before in Section A-1:

$$(X_1, Y_1) = \left(\frac{E_{\text{kD}}}{A^N}, I_{\text{bias-G}}R_{\text{out}}(1 + \frac{1}{A} + \frac{1}{A^2} + ... + \frac{D_0}{A^N})\right), \tag{A-20}$$

$$I_{\text{bias-G}}R_{\text{out}}(1+\frac{1}{A}+\frac{1}{A^2}+...+\frac{D_0}{A^N}) = \frac{I_{\text{bias-G}}R_{\text{out}}}{\log(A)}\log\left(\frac{\frac{E_{\text{kD}}}{A^N}}{V_I}\right), \quad \text{(A-21)}$$

$$(A-1)\Big(1+\frac{1}{A}+\frac{1}{A^2}+...+\frac{1}{A^{N-1}(A-1)}\Big) = (A-1)\frac{1}{\log(A)}\log\left(\frac{\frac{E_{\text{kD}}}{A^N}}{V_I}\right), \quad \text{(A-22)}$$

$$D_0\log(A) = \log\left(\frac{\frac{E_{\text{kD}}}{A^N}}{V_I}\right), \quad \text{(A-23)}$$

$$\log(A^{D_0}) = \log\left(\frac{\frac{E_{\text{kD}}}{A^N}}{V_I}\right). \quad \text{(A-24)}$$

The intercept point follows as:

$$V_I = \frac{E_{\text{kD}}}{A^{N+D_0}}. \quad \text{(A-25)}$$

A-4 Output Model Log-Amp Detector

If the top-end correction $D_0 = A^p/(A^p-1)$ is valid, $\Delta V_{\text{out12}} = \Delta V_{\text{out23}}$. Thus the output of a log-amp detector with $V_{\text{in1}} = E_{\text{kD}}/A^N$:

$$V_{\text{out1}} = I_{\text{bias-D}}R_{\text{out}}\left(1+\Big(\frac{1}{A}\Big)^p+\Big(\frac{1}{A^2}\Big)^p+...+\Big(\frac{1}{A^{N-1}}\Big)^p+D_0\Big(\frac{1}{A^N}\Big)^p\right), \quad \text{(A-26)}$$

$$V_{\text{out1}}(A^p-1) = I_{\text{bias-D}}R_{\text{out}}(A^p-1)\left(1+\frac{1}{A^p}+\frac{1}{A^{2p}}+...+\frac{1}{A^{Np-p}}+\frac{A^p}{A^p-1}\frac{1}{A^{Np}}\right), \quad \text{(A-27)}$$

$$= I_{\text{bias-D}}R_{\text{out}}A^p, \quad \text{(A-28)}$$

$$V_{\text{out1}} = I_{\text{bias-D}}R_{\text{out}}\frac{A^p}{A^p-1}. \quad \text{(A-29)}$$

Assuming an output of a log-amp detector with $V_{\text{in2}} = E_{\text{kD}}/A^{N-1}$:

$$V_{\text{out2}}(A^p-1) = I_{\text{bias-D}}R_{\text{out}}(A^p-1)\left(1+1+\frac{1}{A^p}+...+\frac{1}{A^{Np-p}}+\frac{A^p}{A^p-1}\frac{1}{A^{Np}}\right), \quad \text{(A-30)}$$

$$V_{\text{out2}} = I_{\text{bias-D}}R_{\text{out}}\frac{2A^p-1}{A^p-1}. \quad \text{(A-31)}$$

Assuming an output of a log-amp detector with $V_{\text{in3}} = E_{\text{kD}}/A^{N-2}$:

$$V_{\text{out3}}(A^p-1) = I_{\text{bias-D}}R_{\text{out}}(A^p-1)\left(3+\frac{1}{A^p}+...+\frac{1}{A^{Np-p}}+\frac{A^p}{A^p-1}\frac{1}{A^{Np}}\right), \quad \text{(A-32)}$$

$$V_{\text{out3}} = I_{\text{bias-D}}R_{\text{out}}\frac{3A^p-2}{A^p-1}, \quad \text{(A-33)}$$

Substracting:

$$\Delta V_{\text{out12}} = I_{\text{bias-D}}R_{\text{out}}\frac{2A^p-1-A^p}{A^p-1}, \quad \text{(A-34)}$$

$$= I_{\text{bias-D}}R_{\text{out}}, \quad \text{(A-35)}$$

$$\Delta V_{\text{out23}} = I_{\text{bias-D}}R_{\text{out}}\frac{3A^p-2-(2A^p-1)}{A^p-1}, \quad \text{(A-36)}$$

$$= I_{\text{bias-D}}R_{\text{out}}. \quad \text{(A-37)}$$

A-5 Output Model for Bottem-End Correction

$$K_S = \frac{I_{\text{bias-D}} R_{\text{out}}}{\log(A)} \tag{A-38}$$

Using the same methodology as before in A-1:

$$(X_1, Y_1) = \left(\frac{E_{\text{kD}}}{A^N}, I_{\text{bias-D}} R_{\text{out}} (B_0 + \frac{1}{A} + \frac{1}{A^2} + ... + \frac{D_0}{A^N}) \right), \tag{A-39}$$

$$I_{\text{bias-D}} R_{\text{out}} (B_0 + \frac{1}{A} + \frac{1}{A^2} + ... + \frac{1}{A^{N-1}} + \frac{D_0}{A^N}) = \frac{I_{\text{bias-D}} R_{\text{out}}}{\log(A)} \log\left(\frac{\frac{E_{\text{kD}}}{A^N}}{V_I} \right), \tag{A-40}$$

$$(A-1)\Big(B_0 + \frac{1}{A} + \frac{1}{A^2} + ... + \frac{1}{A^{N-1}} + \frac{1}{A^{N-1}(A-1)}\Big) = (A-1)\frac{1}{\log(A)} \log\left(\frac{\frac{E_{\text{kD}}}{A^N}}{V_I} \right), \tag{A-41}$$

$$(D_0 + B_0 - 1)\log(A) = \log\left(\frac{\frac{E_{\text{kD}}}{A^N}}{V_I} \right), \tag{A-42}$$

$$\log(A^{D_0+B_0-1}) = \log\left(\frac{\frac{E_{\text{kD}}}{A^N}}{V_I} \right). \tag{A-43}$$

The intercept is now equal to:

$$V_I = \frac{E_{\text{kD}}}{A^{N-1+D_0+B_0}}. \tag{A-44}$$

A-6 Output Model for Smooth Transfer of Gain Cell

3-stage logamp with $V_{\text{in1}} = E_{\text{kA}}/A^2$, $V_{\text{in2}} = E_{\text{kA}}/A$, $V_{\text{in3}} = E_{\text{kA}}$ with $D_0 = A/(A-1)$

$$V_{out1} = \frac{D_0 E_{\text{kA}}}{A^2} + \frac{E_{\text{kA}}}{A} + E_{\text{kA}} + AXE_{\text{kA}} \tag{A-45}$$

$$= AXE_{\text{kA}} + D_0 E_{\text{kA}} \tag{A-46}$$

$$V_{out2} = \frac{D_0 E_{\text{kA}}}{A} + E_{\text{kA}} + AXE_{\text{kA}} + 2AE_{\text{kA}} \tag{A-47}$$

$$V_{out3} = D_0 E_{\text{kA}} + AXE_{\text{kA}} + 3AE_{\text{kA}} \tag{A-48}$$

Slope follows as:

$$K_S = \frac{\Delta V_{\text{out12}}}{\log(A)} = \frac{AE_{\text{kA}}}{\log(A)} \tag{A-49}$$

Intercept follows from:

$$V_{\text{out1}} = K_S \frac{\log(V_{\text{in1}})}{\log(V_I)} \tag{A-50}$$

$$X + \frac{D_0}{A} = \frac{AE_{\text{kA}}}{\log(A)} \log\left(\frac{V_{\text{in1}}}{V_I} \right) \tag{A-51}$$

$$V_I = \frac{E_{\text{kA}}}{A^{X+D_0/A+N-1}} \tag{A-52}$$

Appendix B

Design

B-1 RF Front-End

Effective temperature coefficient The transfer of a resistor divider:

$$V_{\text{out}} = V_{\text{in}} \cdot \frac{R_p(1+(T-T_{\text{ref}})TC_1)}{R_p(1+(T-T_{\text{ref}})TC_1)+R_n(1+(T-T_{\text{ref}})TC_2)}. \tag{B-1}$$

Because the derivative of a fraction is $\left(\frac{f}{g}\right)' = \frac{f'g-g'f}{g^2}$, the derivative of V_{out} is equal to:

$$\frac{dV_{\text{out}}}{dT}(T) = \frac{R_pTC_1(R_n(1+(T-T_{\text{ref}})TC_2)) - R_nTC_2(R_p(1+(T-T_{\text{ref}})TC_1))}{(R_p(1+(T-T_{\text{ref}})TC_1)+R_n(1+(T-T_{\text{ref}})TC_2))^2}, \tag{B-2}$$

for $T = T_{\text{ref}}$:

$$\frac{dV_{\text{out}}}{dT}(T=T_{\text{ref}}) = \frac{R_pR_n(TC_1-TC_2)}{(R_p+R_n)^2} \tag{B-3}$$

Input Impedance The input impedance is given by:

$$Z_{\text{in}} = \frac{R_c(R_n+R_p)}{R_c+R_n+R_p} \tag{B-4}$$

Thus

$$\begin{aligned} Z_{\text{in,slow}} &= \frac{78(77+85)}{78+77+85}\ \Omega && \text{(B-5)}\\ &= 53\ \Omega && \text{(B-6)}\\ Z_{\text{in,fast}} &= \frac{72(63+75)}{72+63+75}\ \Omega && \text{(B-7)}\\ &= 47\ \Omega && \text{(B-8)}\\ & && \text{(B-9)} \end{aligned}$$

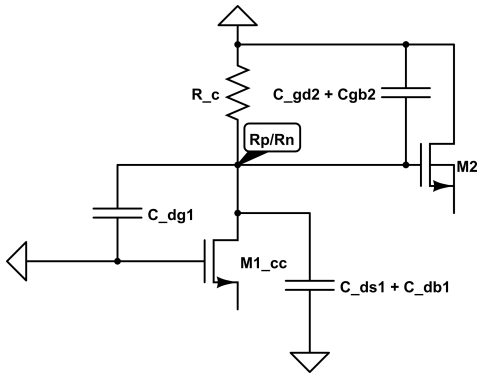
Given an RF source with a $50\,\Omega$ input impedance:

$$P_{\text{in,eff}} = P_{\text{source}} \cdot \frac{Z_{\text{in}}^2}{(50 + Z_{\text{in}})^2}. \tag{B-10}$$

The error in power into the Z_{in} impedance is:

$$\begin{aligned} P_{in} &= 10\log\left(\frac{V_{\text{in}}^2}{Z_{\text{in}}}\right), && \text{(B-11)}\\ \frac{\delta P_{\text{in}}}{\delta Z_{\text{in}}} &= \frac{-10}{\ln(10)}\frac{Z_{\text{in}}}{V_{\text{in}}^2}\frac{V_{\text{in}}^2}{Z_{\text{in}}^2}, && \text{(B-12)}\\ \Delta P_{in} &= \frac{-10}{\ln(10)}\frac{\Delta Z_{\text{in}}}{Z_{\text{in}}}, && \text{(B-13)}\\ &= \frac{-10}{\ln(10)}(\pm 6\%), && \text{(B-14)}\\ &= \pm 0.26 \text{ dB} && \text{(B-15)} \end{aligned}$$

B-2 Gain Cell



BW Using a DC simulation and writing down all parasitic capacitance's:

$$\begin{aligned} C_{\text{DG1}} &= 10 \text{ fF}\\ C_{\text{DB1}} &= 12 \text{ fF}\\ C_{\text{GB2}} &= 6 \text{ fF}\\ 2C_{\text{GD2}} &= 17 \text{ fF}\\ C_{\text{tot}} &= 45 \text{ fF} \end{aligned}$$

The isolated nmos M1 has a bulk which is connected to the main signal. Thus the big p-well bulk sits inside the isolated n-well which is biased at the supply voltage, V_{dd}. A large

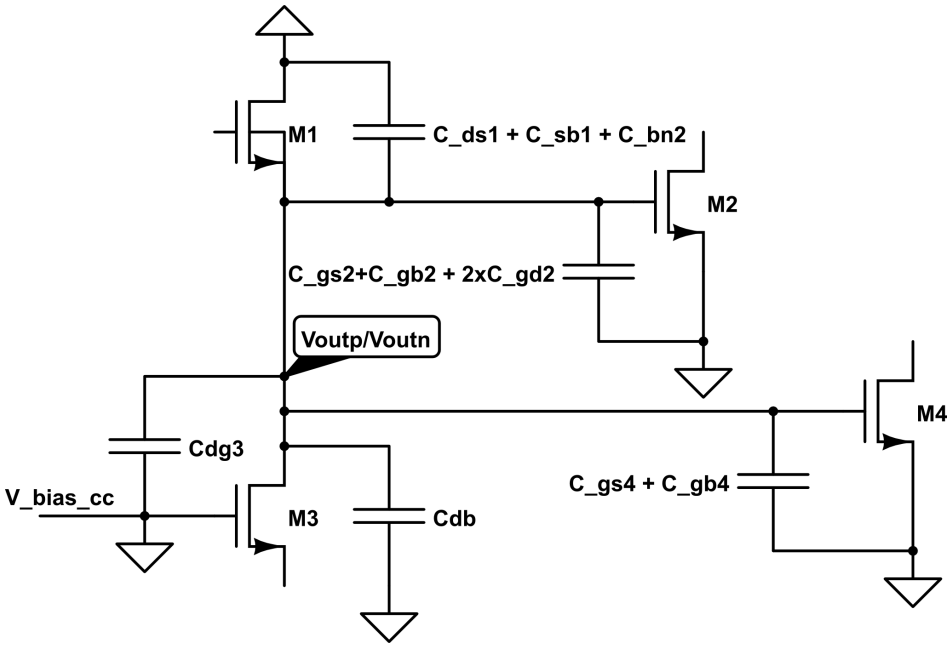


Figure B-1: In which M1/M3 is the voltage follower of the gain cell, M2 the next gain cell and M4 a detector cell.

capacitor between the bulk and this deep-nwell layers exist: C_{BN1}.

$$\begin{aligned} C_{\mathrm{DS1}} &= 9 \text{ fF} \\ C_{\mathrm{DB1}} &= 22 \text{ fF} \\ C_{\mathrm{BN1}} &= 120 \text{ fF} \\ C_{\mathrm{GS2}} &= 19 \text{ fF} \\ C_{\mathrm{GB2}} &= 3 \text{ fF} \\ 2C_{\mathrm{GD2}} &= 17 \text{ fF} \\ C_{\mathrm{DG3}} &= 23 \text{ fF} \\ C_{\mathrm{DB3}} &= 23 \text{ fF} \\ C_{\mathrm{GS4}} &= 12 \text{ fF} \\ C_{\mathrm{GB4}} &= 4 \text{ fF} \\ C_{\mathrm{tot}} &= 252 \text{ fF} \end{aligned}$$

Delta gain The delta gain is calculated by the mismatch between the current sources of the gain cells. Using degeneration resistor $R_s = 600\ \Omega$, $g_m = 3 \times 10^{-3}$ A/V (about two times the g_m of the input pair), with an $(\Delta V_{TH})_{3\sigma} = 4.8$ mV using the small signal gain of a source degenerated NMOS device:

$$I_{\text{bias-A}} = \frac{V_{\text{in}} g_m}{1 + g_m R_S} \tag{B-16}$$

Then:

$$\Delta I_{\text{bias-A}} = \frac{4.8 \times 10^{-3} \cdot 3 \times 10^{-3}}{1 + 3 \times 10^{-3} \cdot 600}, \tag{B-17}$$

$$= 5.1\ \mu\text{A}, \tag{B-18}$$

which matches closely to the DC match simulation. Because the gain is given by:

$$A = \sqrt{\beta I_{\text{bias-A}}} \cdot R_c$$

Differentiating yields:

$$\Delta A = -\Delta I_{\text{bias-A}} \cdot \frac{R_c\sqrt{\beta}}{2\sqrt{I_{\text{bias-A}}}} \tag{B-19}$$

Noise The input and output referred noise of a differential pair is given by [12]:

$$\overline{V_{\text{n,in}}^2} = 8kT\left(\frac{\gamma}{g_{m1}} + \frac{1}{g_{m1}^2 R_c}\right), \tag{B-20}$$

$$\overline{V_{\text{n,out}}^2} = 8kT(\gamma g_{m1} R_c^2 + R_c), \tag{B-21}$$

where g_{m1} is the trans-conductance of input devices of the differential pair. Because in the design the voltage followers have twice the width and twice the current, the trans-conductance g_{m2} of the voltage follower is double that of the differential pair. The input referred noise of a voltage follower with an ideal current source, is equal to the input thermal noise of a MOS [12]:

$$\overline{V_{\text{n,in}}^2} = 4kT\frac{\gamma}{g_{m2}} \tag{B-22}$$

Because two of these uncorrelated noise sources are added to the output of the differential pair with a gain of $g_{m1}R_c$:

$$\overline{V_{\text{n,out,diffpair}}^2} = 8kT(\gamma g_{m1} R_c^2 + R_c + \frac{\gamma}{g_{m2}}), \tag{B-23}$$

$$\overline{V_{\text{n,in,total}}^2} = 8kT\left(\frac{\gamma}{g_{m1}} + \frac{1}{g_{m1}^2 R_c} + \frac{\gamma}{g_{m2} g_{m1}^2 R_c^2}\right), \tag{B-24}$$

B-3 Detector Cell

Output in strong inversion Output detector cell in strong inversion region (in which V_s is the common-source node of the input devices)):

$$I_{\text{bias-D}} = \frac{\beta}{2}((V_p - V_s)^2 + (V_n - V_s)^2 + 2(V_{cm} - V_s)^2) \tag{B-25}$$

Solving for V_s with the ABC-formula:

$$V_s = V_{cm} \pm \frac{\sqrt{8I_{\text{bias-D}}\beta - 2V_n^2\beta^2 - 2V_p^2\beta^2 + 4V_nV_p\beta^2}}{4\beta} \tag{B-26}$$

Putting V_s in the output equation:

$$\begin{aligned} I_{\text{out}} &= I_{\text{out+}} - I_{\text{out-}} && \text{(B-27)} \\ &= I_{\text{bias-D}} - 2I_{\text{out-}} && \text{(B-28)} \\ &= I_{\text{bias-D}} - 2(\beta(V_{cm} - V_s)^2) && \text{(B-29)} \\ &= \frac{\beta}{4}V_{\text{in}}^2 && \text{(B-30)} \end{aligned}$$

Mismatch current source The current source mismatch can be calculated using: $g_m = 364\ \mu\text{A/V}$, $R_S = 7.2\ \text{k}\Omega$ and the calculated input offset $((V_{OS})_{3\sigma} = 1.47\ \text{mV}$.

$$\begin{aligned} (I_{\text{OS,out}})_{3\sigma} &= \frac{V_{\text{in,OS}} g_m}{1 + g_m R_S} && \text{(B-31)} \\ &= 148\ \text{nA} && \text{(B-32)} \end{aligned}$$

B-4 Channel and OSCL

Effective Noise bandwidth The noise bandwidth can be calculated using the equivalent bandwidth of the channel, which was simulated at 933 MHz. Going through a similar calculation as before and noting that every gain cell introduces two poles at the pole frequency (8 poles), the following integral should be solved:

$$\begin{aligned} \int_0^\infty \frac{dx}{x^{16} + 1} &= \frac{\pi}{16} \csc\left(\frac{\pi}{16}\right) && \text{(B-33)} \\ &= 1.006 && \text{(B-34)} \end{aligned}$$

Noise bandwidth:

$$B_n = 94 \times 10^7\ \text{Hz} \tag{B-35}$$

Input referred noise of channel The noise power at over bandwidth B_n will be modulated back to DC by the detector cells. Comparing this power to the input power of a sinusoidal input signal it is possible to estimate the pedestal output voltage using the ideal log function. The input referred noise power of the channel is given by (3-31). To calculate this back to the input of the device, it is important to look at the FE circuit of Figure 3-13.

First a simplified schematic of the circuit is given in Figure B-2.

In this figure $\overline{I_{n1}^2}$ and $\overline{I_{n2}^2}$ are the sum of all the current source noise and $\overline{I_{R1}^2}$ and $\overline{I_{R2}^2}$ are the resistor noise sources. The noise from the isolated NMOS (the $1/g_m$ resistor) is not put at the output because the circuit is symmetrical and output is $V_{\text{out+}} - V_{\text{out-}}$.
The transfer function of this circuit is given by:

$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) = \frac{sCR}{1 + sCR} \tag{B-36}$$

To calculate the output noise of this block, the input is shorted: $V_{\text{in}} = 0$. Assuming that $1/g_m << R_c$ basically all noise sources are connected to either $V_{\text{out+}}$ and $V_{\text{out-}}$. All these noise

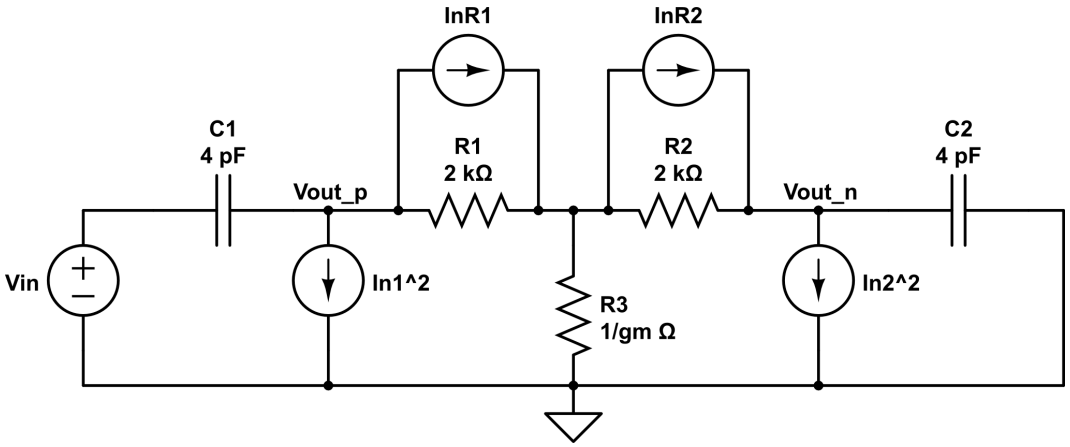


Figure B-2: Small signal equivalent of circuit 3-13 including noise sources.

sources are than filtered through the RC low pass filter. Because the overall noise bandwidth $B_n >> 1/(2\pi RC)$ the output noise power of all components inside the FE circuit are actually fixed by the internal circuit bandwidth.
In the considered noise BW the transfer function of (B-36) is approximately equal to 1, which means that $P_{\mathrm{n,out}} \sim P_{\mathrm{n,in}}$. Using the input referred noise power of all gain cells it becomes relatively easy to refer all powers to the input of the FE circuit.
The transfer seen from a current source at $V_{\mathrm{out,p}}$ and $V_{\mathrm{out,n}}$ can be written as:

$$\left|\frac{V_{\mathrm{out}}}{I_{in}}\right| = \left|\frac{R}{sRC+1}\right| \tag{B-37}$$

Which is basically a low pass filter. For a first order system the noise bandwidth $B_n = f_p\pi/2$ as seen from:

$$S_{\mathrm{out}}(f) = S_{\mathrm{in}}(f)\left|\frac{V_{\mathrm{out}}}{I_{in}}\right|^2 \tag{B-38}$$

$$P_{\mathrm{n,out}} = \overline{I^2_{\mathrm{n,in}}}R^2\int_0^\infty \frac{1}{\frac{f^2}{f_p^2}+1}df \tag{B-39}$$

In which $f_p = 1/(2\pi RC)$. Because:

$$\begin{aligned}\int \frac{du}{u^2+1} &= \tanh u \\ u &= \frac{f}{f_p} \\ du &= \frac{1}{f_p}df\end{aligned}$$

$$\begin{aligned} P_{\text{n,out}} &= \overline{I^2_{\text{n,in}}} R_c^2 f_p \int_0^\infty \frac{1/f_p}{\frac{f^2}{f_p^2}+1} df \\ &= \overline{I^2_{\text{n,in}}} R_c^2 f_p \left[\tanh(f/f_p)\right]_0^\infty \\ &= \overline{I^2_{\text{n,in}}} R_c^2 \frac{\pi}{2} f_p \end{aligned} \tag{B-40}$$

The current sources of the circuit all have a trans-conductance of $\sim 1 \times 10^{-3}$ V/A which results in a total current noise component of:

$$\overline{I^2_{\text{n,CS}}} = 6 \cdot 4kT\gamma g_m \tag{B-41}$$

$$= 4.3 \times 10^{-2} kT \tag{B-42}$$

$$P_{\text{n,out,CS}} = (4.3 \times 10^{-2} R_c^2 \frac{\pi}{2} f_p) kT \tag{B-43}$$

$$= 1.7 \times 10^5 (\frac{\pi}{2} f_p) kT \tag{B-44}$$

The resistors also produce noise:

$$\overline{I^2_{\text{n,Rc}}} = 2 \cdot \frac{4kT}{R_c}$$

$$\begin{aligned} P_{\text{n,out,R}} &= 2 \cdot \frac{4kT}{R_c} R_c^2 \frac{\pi}{2} f_p \\ &= 8kT R_c \frac{\pi}{2} f_p \end{aligned}$$

Total output noise power from FE block with $f_p = 1/(2\pi R_c C)$:

$$P_{\text{n,out,tot}} = \frac{2kT}{C} + 1.6 \times 10^5 \left(\frac{1}{4R_c C}\right) kT\ V^2 \tag{B-45}$$

$$= 5.8 \times 10^{12} kT\ V^2 \tag{B-46}$$

Adding the power from the cascaded gain cells:

$$P_{\text{n,out,tot}} = (5.8 \times 10^{12} + 1.2 \times 10^4 \cdot B_n) kT\ V^2 \tag{B-47}$$

The input referred power is than equal to the output referred power in the noise bandwidth.

To refer the input-referred noise power of the RF-FE block to the input of the log-amp detector, the power transfer of the RF input block should be used. The transfer of this block is simply $\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{80}{150} = 0.53$. As the output-referred impedance of the RF input block is $44\,\Omega$, its thermal noise can be added to the channel and noise of the FE:

$$P_{\text{n,in,tot}} = \frac{1}{0.53^2}(178 \cdot B_n + 5.8 \times 10^{12} + 1.2 \times 10^4 \cdot B_n) kT\ V^2 \tag{B-48}$$

If $B_n = 940$ MHz, k = 1.38×10^{-23} J/K, T = 300 K the total input-referred noise power is:

$$P_{n,in,tot} = 2.5 \times 10^{-7}\ V^2\,. \tag{B-49}$$

As the impedance at the input of the RF block is equal to $25\,\Omega$, this noise can be converted into Watts as:

$$P_{n,in,tot} = \frac{2.5 \times 10^{-7}\,V^2}{25\,\Omega} \tag{B-50}$$

$$= 1.0 \times 10^{-8}\,W \tag{B-51}$$

$$= -50\ \text{dBm}\,, \tag{B-52}$$

which would be the input-referred power which would yield a output voltage for an RMS detector. The log-amp detector however is dependent on the modulation, which will introduce a small factor in the conversion from power to output voltage. The difference between a sinusoidal input vs a noise input is 0.5 dB according to [8]. The equivalent sinusoidal signal noise power is thus:

$$P_{\text{n,in,tot}} = -49.5\,\text{dBm} \tag{B-53}$$

By taking a the slope and intercept from Subsections 3-5-1 and 3-5-2, as given in Chapter 3, the output noise pedestal level can be calculated.

B-5 Bias Block A

Spread Both M1 and M2 contribute directly on the output current via the output current equation. Because the circuit works by having $V_{gs1} = V_{gs2} + V_R$, any offset directly changes the current through the trans-conductance:

$$\begin{aligned} (A_{Vth,M1})_{3\sigma} &= 1.73 \text{ mV} \\ (A_{Vth,M2})_{3\sigma} &= 0.87 \text{ mV} \\ g_{m1} &= 14 \times 10^{-3} \text{ A/V} \\ g_{m2} &= 17 \times 10^{-3} \text{ A/V} \end{aligned}$$

$$\begin{aligned} (\Delta I_{\text{bias-A}})_{3\sigma} &= \sqrt{(24 \times 10^{-6})^2 + (15 \times 10^{-6})^2} \\ &= \pm 28 \ \mu\text{A} \end{aligned}$$

B-6 Bias Block D

Spread As done in the last section:

$$\begin{aligned} (A_{\text{Vth,M1}})_{3\sigma} &= 0.52 \text{ mV} \\ (A_{\text{Vth,M2}})_{3\sigma} &= 0.26 \text{ mV} \\ g_{m1} &= 1.5 \times 10^{-3} \text{ A/V} \\ g_{m2} &= 1.8 \times 10^{-3} \text{ A/V} \end{aligned}$$

$$\begin{aligned} (\Delta I_{\text{bias-D}})_{3\sigma} &= \sqrt{(.78 \times 10^{-6})^2 + (.47 \times 10^{-6})^2} \\ &= \pm 0.91 \ \mu\text{A} \end{aligned}$$

Appendix C

Scaling

$$A = g_m R_c \tag{C-1}$$

$$I_d = I_0 e^{\left(\frac{V_{gs}}{\zeta V_T}\right)} \tag{C-2}$$

$$g_m = \frac{dI_d}{V_{\mathrm{GS}}} = \frac{V_{\mathrm{GS}}}{\zeta V_T} I_0 e^{\left(\frac{V_{\mathrm{GS}}}{\zeta V_T}\right)} \tag{C-3}$$

$$= \frac{I_d}{\zeta V_T} \tag{C-4}$$

$$A = g_m R_c \tag{C-5}$$

$$= \frac{I_d}{\zeta V_T} R_c \tag{C-6}$$

Appendix D

PTM

Output of detector cell in Weak inversion Solving for $I_{\text{bias-D}} = I_{\text{out+}} + I_{\text{out-}}$:

$$I_{\text{bias-D}} = I_0(e^{\frac{V_{\text{in+}}-V_s}{nV_t}} + e^{\frac{V_{\text{in-}}-V_s}{nV_t}} + 2e^{\frac{V_{cm}-V_s}{nV_t}}), \tag{D-1}$$

$$\frac{I_{\text{bias-D}}}{I_0} = e^{-\frac{V_s}{nVt}}(e^{\frac{V_{\text{in+}}}{nV_t}} + e^{\frac{V_{\text{in-}}}{nV_t}} + 2e^{\frac{V_{cm}}{nV_t}}), \tag{D-2}$$

$$\ln\left(\frac{I_{\text{bias-D}}}{I_0}\right) = -\frac{V_s}{nV_t} + \ln(e^{\frac{V_{\text{in+}}}{nV_t}} + e^{\frac{V_{\text{in-}}}{nV_t}} + e^{\frac{V_{cm}}{nV_t}}), \tag{D-3}$$

$$\frac{V_s}{nV_t} = -\ln\left(\frac{I_{\text{bias-D}}}{I_0}\right) + \ln(e^{\frac{V_{\text{in+}}}{nV_t}} + e^{\frac{V_{\text{in-}}}{nV_t}} + 2e^{\frac{V_{cm}}{nV_t}}). \tag{D-4}$$

Because:

$$e^{\frac{-V_s}{nV_t}} = \frac{I_{\text{bias-D}}}{I_0}\left(e^{\frac{V_{\text{in+}}}{nV_t}} + e^{\frac{V_{\text{in-}}}{nV_t}} + 2e^{\frac{V_{cm}}{nV_t}}\right)^{-1}. \tag{D-5}$$

Now solving for $I_{out} = I_{\text{out+}} - I_{\text{out-}}$, putting in (D-5):

$$I_{\text{out}} = I_0 \cdot (e^{\frac{V_{\text{in+}}-V_s}{nV_t}} + e^{\frac{V_{\text{in-}}-V_s}{nV_t}} - 2e^{\frac{V_{cm}-V_s}{nV_t}}), \tag{D-6}$$

$$= I_0 \cdot e^{\frac{-V_s}{nV_t}}(e^{\frac{V_{\text{in+}}}{nV_t}} + e^{\frac{V_{\text{in-}}}{nV_t}} - 2e^{\frac{V_{cm}}{nV_t}}), \tag{D-7}$$

$$= I_{\text{bias-D}} \cdot \left(\frac{e^{\frac{V_{\text{in+}}}{nV_t}} + e^{\frac{V_{\text{in-}}}{nV_t}} - 2e^{\frac{V_{cm}}{nV_t}}}{e^{\frac{V_{\text{in+}}}{nV_t}} + e^{\frac{V_{\text{in-}}}{nV_t}} + 2e^{\frac{V_{cm}}{nV_t}}}\right). \tag{D-8}$$

Appendix E

Paper for ESSCIRC Conference

A 39 dB DR CMOS Log-Amp RF Power Detector with ±1.1 dB Temperature Drift from -40 to 85°C

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***Abstract*—This paper presents a temperature compensated logarithmic amplifier (log-amp) RF power detector implemented in CMOS 0.18 μm technology. The input power can range from -50 to +10 dBm for RF signals ranging from 100 MHz to 1.8 GHz. This design attains a typical DR of 39 dB for a ±1 dB log-conformance error (LCE). Up to 900 MHz the temperature drift is never larger than ±1.1 dB for all 24 measured samples over a temperature range from -40 to +85°C. The current consumption is 6.3 mA from a 1.8 V power supply and the chip area is 0.76 mm^2.**

I. Introduction

To accurately set the output power of a PA in handsets, a power control loop is often used. A coupler senses a fraction of the output RF signal and feeds it to an RF power detector (Fig. 1). It's output is a measure of the average peak value of the input RF signal. Knowledge about the modulation type employed allows for the accurate calculation of the transmitted power. Log-amp detectors in Bipolar technology present good temperature stability for RF applications [1], [2]. CMOS log-amps for RF power-detection so far published fail to demonstrate consistent performance over a wide temperature range [3], [4]. This prototype IC demonstrates that a temperature compensated log-amp RF power detector can be designed using standard CMOS technology while attaining a temperature drift bounded to ±1.1 dB and low power consumption.

II. System architecture

The architecture of a log-amp detector is based on a cascade of N gain cells (A), N+1 detector cells (D), an output low-pass filter (LPF1) to reject high-frequency components at the output and finally an offset cancellation loop around the cascade of gain cells and another low-pass filter (LPF2). In this design $N = 4$, as shown in Fig. 2. The transfer characteristic of A and D are respectively:

$$V_{\text{out-A}}\,[\text{V}] = \begin{cases} A \cdot V_{\text{in-A}}, & \text{if } |V_{\text{in-A}}| < E_{\text{kA}}, \\ A \cdot E_{\text{kA}}, & \text{if } |V_{\text{in-A}}| \geq E_{\text{kA}}, \end{cases} \quad (1)$$

$$I_{\text{out-D}}\,[\text{A}] = \begin{cases} \frac{\beta}{4} \cdot V_{\text{in-D}}^2, & \text{if } |V_{\text{in-D}}| < E_{\text{kD}}, \\ I_{\text{biasD}}, & \text{if } |V_{\text{in-D}}| \geq E_{\text{kD}}, \end{cases} \quad (2)$$

in which A is the voltage gain of the gain cell, E_{k} is the input referred clipping voltage (knee voltage) and in CMOS technology $\beta = \mu C_{\text{ox}} W/L$. In this design $AE_{\text{kA}} > E_{\text{kD}}$ is chosen. For an input signal with amplitude E_{kD}/A^4, only the last detector cell reaches its maximum output current, I_{biasD}.

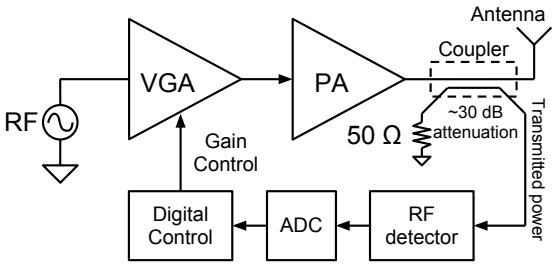


Fig. 1: Transmitted-power control loop

Increasing the input signal to E_{kD}/A^3 will clip the output of the last two detector cells to I_{biasD}. Consequently, for every multiplication of the input signal magnitude by A, a linear increase of the output current equal to I_{biasD} is expected. A piece-wise linear approximation of a logarithmic function is obtained. This logarithmic transfer can be represented by a linear relation between V_{out} and the input power P_{in} expressed in dBm:

$$V_{\text{out}}\,[\text{V}] = K_{\text{slope}}(P_{\text{in}} - P_0)\,, \quad (3)$$

where K_{slope} and P_0 are given by:

$$K_{\text{slope}}\,[\text{V/dB}] = \frac{I_{\text{biasD}} R_{\text{out}}}{20\log(A)}\,, \quad (4)$$

$$P_0\,[\text{dBm}] = 20\log\left(\frac{E_{\text{kD}}}{\sqrt{50\,\Omega}\cdot A^{N+1}}\right) + 30\,. \quad (5)$$

A. Temperature compensation

To implement a log-amp detector for which the transfer characteristic is temperature independent, both the slope (K_{slope}) and the intercept power (P_0) should be kept constant over temperature. This is achieved by temperature stabilization of both the gain cells and the detector cells and by temperature scaling of the input/output signals of the log-amp detector core (Fig. 2). Fig. 3 shows the architecture of the complete temperature compensated log-amp detector.

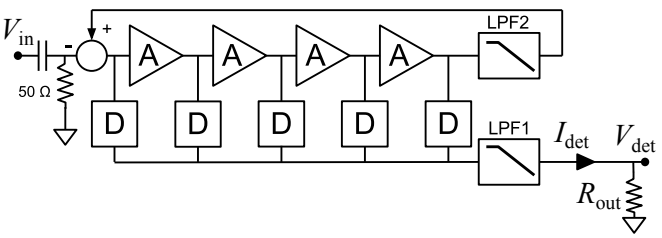


Fig. 2: Log-Amp Detector Core

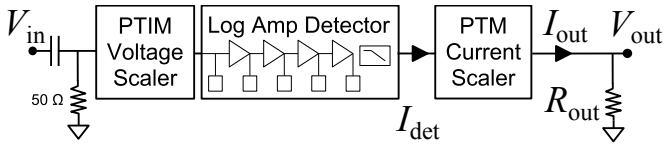


Fig. 3: Log-Amp Detector with temperature compensation

1) Gain Cell: The gain (A) variation over temperature affects the transfer's slope (4) and intercept (5). To keep both parameters constant over temperature, the gain cell (Fig. 4) should be designed to attain a voltage gain $g_m \cdot R$ that is constant over temperature:

$$A(T) = g_m(T) \cdot R(T) \quad (6)$$

$$= \sqrt{\mu(T) C_{ox} \frac{W}{L} I_{biasA}(T)} \cdot R(T)\,, \quad (7)$$

where $\mu(T) = \mu_0 (T/T_{ref})^{N_\mu}$ models the temperature dependence of the mobility with $1.5 < N_\mu < 2$ [5] and $R(T)$ represents the temperature behavior of all resistors in this design (except the resistors in the front-end scaler). If current $I_{biasA}(T)$ is designed to have a temperature dependence proportional to the inverse mobility (PTIM) and $R(T)^{-2}$, the gain A becomes to a first order constant over temperature.

2) Input PTIM Voltage Scaler: After temperature compensation, the maximum output swing of every gain cell presents a PTIM temperature dependence. Consequently the gain and detector cells, except the front-end cells, experience a maximum input voltage with PTIM temperature behavior. Therefore a PTIM voltage scaler in front of the log-amp detector core is required.

3) Detector Cell: Detector bias current I_{biasD} and knee voltage E_{kD} appear in the expressions for slope (4) and intercept (5) respectively. Rewriting (2) yields $E_{kD} = \sqrt{4 I_{biasD}/\beta}$. Because the maximum output voltage of the gain cells exhibit a PTIM behavior, E_{kD} should follow the same temperature behavior. This can be achieved using a PTIM bias current $I_{biasD} = K_0 C_{ox} L/(W R^2(T) \mu(T))$. The knee voltage becomes:

$$E_{kD}(T) = \sqrt{\frac{4 I_{biasD}(T)}{C_{ox} \frac{W}{L} \mu(T)}} = \frac{2\sqrt{K_0}}{\beta(T) R(T)}\,. \quad (8)$$

The temperature dependence of E_{kD} on both $\beta(T)$ and $R(T)$ needs to be compensated for in (5). This can be achieved through the front-end PTIM voltage scaler. The transfer of the input voltage scaler is given by:

$$S(T) = \frac{S_0}{\beta(T) R(T)}\,. \quad (9)$$

Substitution of (9) into (5) results in:

$$P_0(T) = 20 \log \left(\frac{E_{kD}(T)}{\sqrt{50\,\Omega} \cdot S(T) \cdot A^5} \right) + 30 \quad (10)$$

$$= 20 \log \left(\frac{2\sqrt{K_0}}{\sqrt{50\,\Omega} \cdot S_0 \cdot A^5} \right) + 30\,, \quad (11)$$

which yields a temperature independent intercept power P_0.

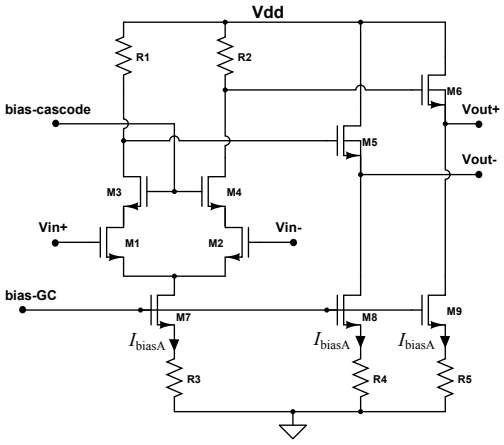


Fig. 4: Circuit of Gain-cell (A)

4) PTM Current scaler: The output current I_{det} of the log-amp detector core presents the same PTIM dependence as I_{biasD}. In order to obtain a log-amp detector with a constant transfer over temperature, a proportional to mobility (PTM) current scaler is required between the log-amp detector core and the final I-V conversion (Fig. 3):

$$I_{out\text{-}CONST} = I_{det\text{-}PTIM} \cdot (I_{CONST}/I_{PTIM})\,. \quad (12)$$

III. Circuit Design

A. Input PTIM Voltage Scaler

A resistor π-network, with a $50\,\Omega$ input impedance and 5.7 dB attenuation, implements the passive front-end voltage scaler by employing positive- and negative-temperature coefficient resistors. The first-order temperature behavior of the desired relation (9) can be approximated by controlling the resistor values R_{PTC} and R_{NTC}:

$$S(T) = \frac{R_{PTC} R_{NTC}}{(R_{PTC} + R_{NTC})^2} \cdot (TC_P - TC_N)\,. \quad (13)$$

B. Gain Cell

The circuit of the gain cell, shown in Fig. 4, is a differential pair with cascodes, the latter to improve the bandwidth by decreasing the Miller multiplication of C_{GD} of M1/M2 seen at the input of the gain cell. The voltage followers provide a lower common-mode output voltage needed to bias the next gain cell. To limit the V_{GS} voltage drop, the voltage followers were implemented with isolated NMOS devices ($V_{BS} = 0$).

C. Detector Cell

The circuit of the detector cell is depicted in Fig. 5. It is an NMOS version of the detector circuit from [6]. Differently from it's bipolar counterpart, where $E_{kD} = 4V_T$, E_{kD} is a function of transistor size and bias current in a MOS implementation. For a sinusoidal input signal $V_{in} = V_P \sin(\omega_p t)$, were $V_P \leq E_{kD}$, the detector output current can be expressed by:

$$I_{out} = \frac{\beta}{4} V_P \sin^2(x) = \frac{\beta V_P}{8} \Big(1 - \cos(2\omega_p t)\Big)\,[\mathrm{A}]\,, \quad (14)$$

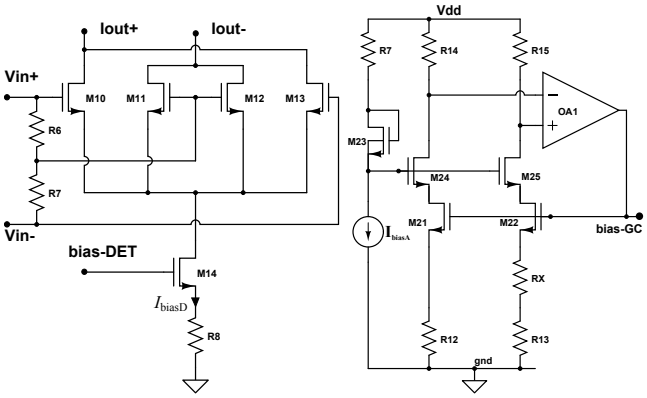


Fig. 5: Circuit of detector-cell (D)

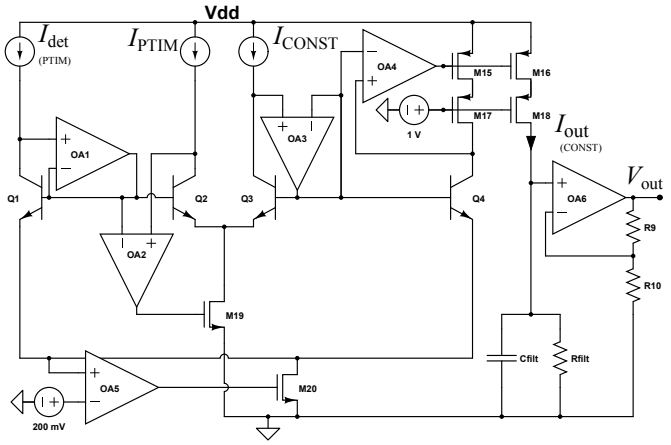


Fig. 6: Circuit of PTIM current generator.

Fig. 8: Circuit of PTM current scaler and I-V converter.

which contains a DC and a double frequency component ($2\omega_p$). After low-pass filtering only the DC component remains. The current output of the detector ($\beta V_P/8$) is thus a measure of the peak amplitude of the input signal.

D. PTIM Bias Generator

From (5) it follows that the intercept is inversely proportional to A^5. Small variations of the gain will yield relatively large intercept shifts over temperature, which requires an accurate constant-g_m bias circuit.

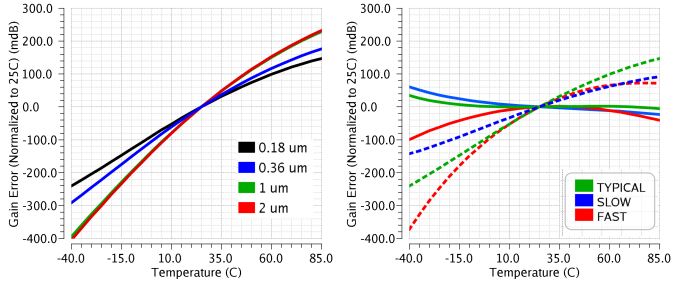
The chosen architecture for constant-g_m biasing is shown in Fig. 6. The current through transistors M21 and M22 is given by [7]:

$$I_{\text{PTIM}}(T) = \frac{1}{R^2(T)} \frac{2L_{\text{M21}}}{\mu(T) C_{ox} W_{\text{M21}}} \frac{(\sqrt{n}-1)^2}{n}, \qquad (15)$$

where n is the ratio between the areas of M21 and M22. To increase the accuracy of the bias current two phenomena should be accounted for in the PTIM bias generator: mobility degradation and velocity saturation, which are both short channel effects. The effective mobility is given by [5]:

$$\mu_{0\text{-eff}} = \frac{\mu_0 v_{\max} L}{v_{\max} L(1+\theta V_{\text{OV}}) + \mu_0 V_{\text{DS}}}, \qquad (16)$$

where $v_{\max}$ is the maximum velocity of the carriers in the channel, θ is a technology dependent fitting parameter and $V_{\text{OV}} = V_{\text{GS}} - V_{\text{TH}}$ is the overdrive voltage. The effective mobility is thus dependent on the MOSFET's biasing conditions. The overdrive voltage of the gain cell transistors M1/M2 is equal to the overdrive voltage of M21/M22 in the bias generator if they have the same current density and the same unit device. Simulation results in Fig. 7a show the gain error over temperature for different L sizes inside the bias generator (same W/L ratio). When M21/M22 use the same unit device as M1/M2, the gain error over temperature reduces to <0.5 dB. In order to bias M1/M2 and M21/M22 with similar V_{DS} voltages, cascode devices M24/M25 are employed in the bias generator. This further reduces the gain error over temperature to <0.1 dB for the extreme corners, as shown in Fig. 7b.



(a) Different L-sizes in bias generator, constant W/L, $L = 0.18\,\mu$m in gain cells.

(b) With- (solid) and without- (dotted) cascodes in bias generator, $L = 0.18\,\mu$m in gain cells and bias generator.

Fig. 7: Normalized gain error over temperature.

E. PTM Current Scaler and I-V Conversion

The translinear-loop shown in Fig. 8 implements the current relation from (12). As a result, the PTIM dependence is removed from the log-amp detector current output. For convenience the available bipolar devices were used for the translinear-loop. For a complete CMOS implementation these can be replaced with MOSFET's biased in weak-inversion. Resistor R_{filt} and a non-inverting amplifier performs the final I-to-V conversion.

IV. Measurements

A. Performance Metrics

1) Log-Conformance Error (LCE): This metric shows the error versus an ideal logarithmic curve:

$$\text{LCE}_{\text{error}}(\text{dB}) = \frac{(V_{\text{out},1} - (K_S \cdot (P_{\text{in},1} - P_0))}{K_S}. \qquad (17)$$

2) Temperature Drift: This metric shows the difference between the log-amp detection transfer at a certain temperature in relation to the transfer obtained at a reference temperature (generally 25°C). It is expressed in dB in this paper.

B. Measurement results

A batch of 24 samples was measured for sinusoidal inputs at 100, 700, 900, 1500, 1800 and 2100 MHz over the full input power range (-50 to +10 dBm). The detection curves were obtained at -40, +25 and 85°C for a fixed 1.8 V supply

voltage. The prototype IC has an active area of 0.76 mm^2 and draws 6.3 mA from the supply.

Fig. 9 shows the typical (average among the 24 samples) detection (a) and LCE (b) curves for all measured input frequencies. Up to 900 MHz the intercept shift is negligible. This is accordance with the simulated -3 dB BW of the four cascaded gain cells at 930 MHz.

Fig. 10 shows the typical LCE plots at -40, +25 and +85°C. The DR for ±1 dB LCE is 39 dB at 25°C for frequencies between 100 and 700 MHz.

Fig. 11 shows the temperature drift for the extremes of the temperature range (-40°C and 85°C) in relation to 25°C. Up to 900 MHz the temperature drift is never larger than ±1.1 dB for all 24 measured boards. This result was achieved without employing any method of temperature calibration. For input frequencies above the -3 dB BW of 930 MHz, the temperature errors become larger.

Table I shows the measured DR and temperature drift for several frequencies and metrics. Fig. 12 shows a microphotograph of the prototyped IC.

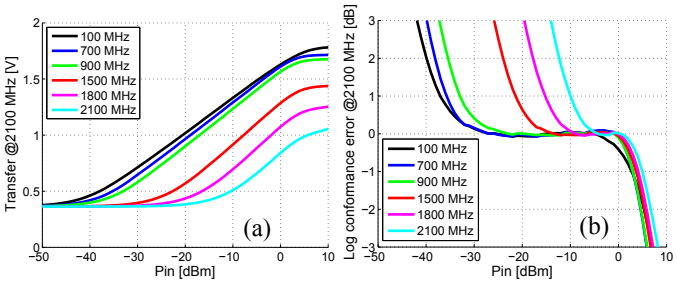


Fig. 9: Typical Detection Curves (a) and LCE (b) over frequency.

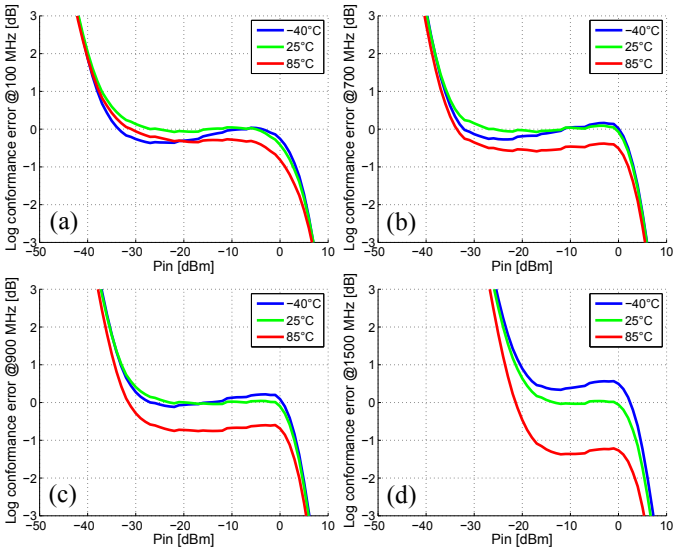


Fig. 10: Typical LCE for 100 (a), 700 (b), 900 (c) and 1500 MHz (d).

V. Conclusions

A complete implementation of a RF power detector in 0.18 μm CMOS technology based on the log-amp structure was demonstrated. Thanks to the temperature compensated architecture, the temperature drift is bounded to ±1.1 dB from -40°C to 85°C for frequencies up to 900 MHz. The use of nanometer-scale CMOS technologies would extend the bandwidth of this architecture, enabling the coverage of higher frequency bands.

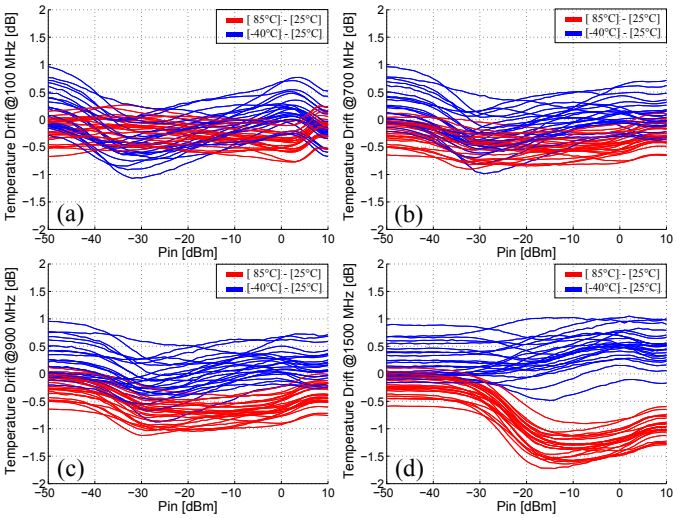


Fig. 11: Temperature Drift for 24 Samples at 100 (a), 700 (b), 900 (c) and 1500 MHz (d).

TABLE I: Performance summary - Typical DR [dB] at 25°C LCE and Max Temperature Drift [dB] for 24 samples.

Frequency	0.1 GHz	0.7 GHz	0.9 GHz	1.5 GHz	1.8 GHz
DR for ±1 dB LCE	40 dB	39 dB	36 dB	25 dB	19 dB
DR for ±3 dB LCE	49 dB	46 dB	43 dB	32 dB	27 dB
Max Temp. Drift	±1.1 dB	±1.0 dB	±1.1 dB	+1.1,-1.7 dB	+1.4,-1.9 dB

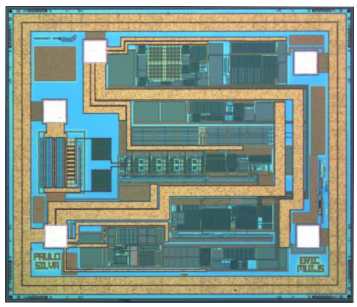


Fig. 12: Chip microphotograph

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Glossary

List of Acronyms

PTIM	Proportional To Inverse Mobility
PTM	Proportional To Mobility
BW	Bandwidth
GBW	Gain-Bandwidth
MOSFET	Metal-oxide-semiconductor field-effect transistor
DR	Dynamic Range
log-amp	logarithmic amplifier
PA	Power Amplifier
LCE	Log-Conformance Error
EVOT	Error Variation Over Temperature
TC	Temperature Coefficient
RF	Radio Frequency
IC	Integrated Circuit
PCB	Printed Circuit Board
GPIB	General Purpose Interface Bus
opamp	operational amplifier
PM	Phase Margin
GM	Gain Margin
ASK	Amplitude-Shift Keying

PSK Phase-Shift Keying

RMS Root Mean Square