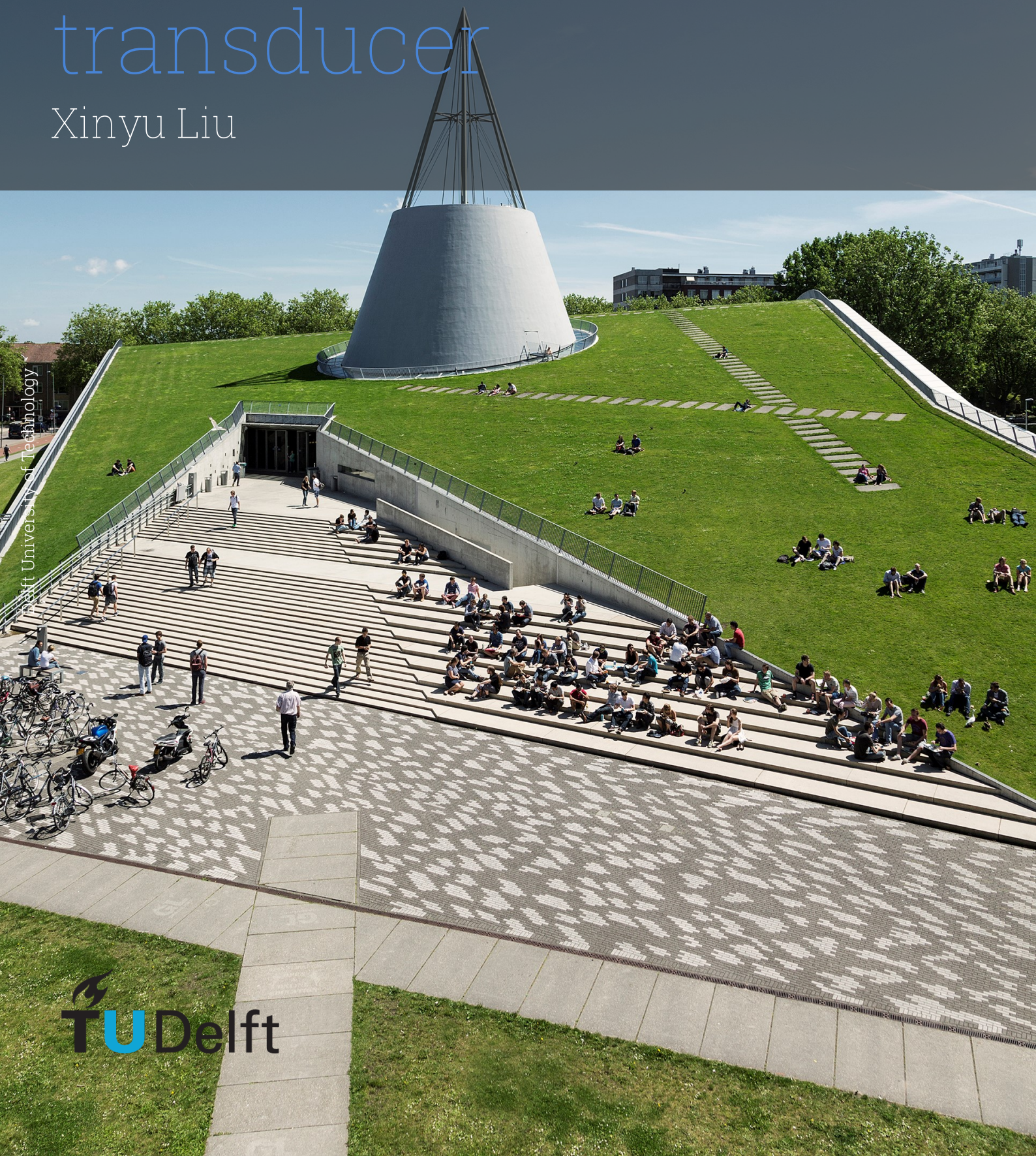
Cold start for Energy Harvesters with Piezo transducer

Xinyu Liu



TU Delft

Cold start for Energy Harvesters with Piezo transducer

by

Xinyu Liu

to obtain the degree of Master of Science
at the Delft University of Technology,
to be defended publicly on Monday September 25, 2023 at 15:00.

Student number:	5403227	
Project duration:	July 18, 2022 – September 25, 2023	
Thesis committee:	Prof. dr. ir. W. A. Serdijn,	TU Delft, supervisor
	Dr. ir. M. A. P. Pertijs,	TU Delft
	Ir. Luc. van. Wietmarschen,	Nexperia

This thesis is confidential and cannot be made public until September 25, 2024.

TU Delft

Abstract

This thesis project proposes a cold-start circuit for vibration energy harvesting from human motion. The literature research on kinetic energy harvesters shows that the piezoelectric energy harvester is the most fitting energy source because of its good adaptation to the CMOS technology, high energy density and mature commercial development.

Two major challenges in piezoelectric energy harvesting are reducing the charge wasted on continuously charging and discharging the parasitic capacitor of the piezoelectric transducer and reducing the conduction loss of the rectifier. For a self-powered system, the start-up of the system when the storage element is completely depleted, known as 'cold-start', introduces another challenge.

A rectifier is a must for piezoelectric energy harvesting because the current and voltage outputs of a piezoelectric transducer have zero mean values. In addition, there are no DC sources for the active circuit, so the circuit has to work passively during the cold start.

The core of the designed cold-start circuit is a two-stage rectifier, which has a cross-coupled rectifier and an active diode, to ensure both the cold-start capability and low rectifier voltage drop when working actively. When working passively, the storage element will be charged by the body diode of the active diode. The flipping technique is introduced to reduce the charge wasted on the parasitic capacitor. The flipping technique makes full use of the output and advantages of the active diode. The flipping technique has a very robust structure, and the power consumption and area are heavily reduced.

The implementation of the cold-start circuit is made using the Cadence Virtuoso. It is tested for the cold-start capability and potential for normal harvesting across five process corners and three temperatures. The verification results prove that the proposed cold-start circuit can complete the cold-start task for an input power level of sub-micro-watt from 1Hz to 10Hz. When working for normal harvesting, the output power is competitive to the state-of-the-art that uses the same number of flipping capacitors while the current consumption is reduced to 100nA, and the area is reduced a lot.

Preface

Firstly, I would like to express my gratitude to Nexperia Energy Harvesting for providing me with the opportunity to finish my master's thesis and for supporting all the tools and environments along the project. It has been my great pleasure to work with so many wonderful colleagues and witness the growth of the company.

I want to thank my supervisor, Professor Wouter Serdijn, who not only taught me valuable knowledge but also inspired me a lot during the project. Professor Wouter Serdijn always suggests analysing problems from the fundamental level, which turns out to be the most efficient and effective way of solving problems.

I also want to thank my daily supervisor, Luc van Wietmarschen, for his guidance and patience during the project. Luc has helped me with his experience on cold-start and energy harvesting, guided me through the entire project, helped me make reasonable design choices, reviewed my work and taught me skills in operating the IC design tools. I can't imagine how I can complete this project without his help.

I would like to thank the entire IC team for attending some of the important meetings in the project, helping me make my presentation and presentation skills better, and pointing out aspects that I had not considered. Also, a special thanks to Nourane for teaching me layout skills when I knew nothing about layout.

Finally, I want to thank my family and friends for supporting me during the project. The thesis project could be boring at times, but thankfully, my friends and family always keep encouraging me.

Contents

Abstract ii

Preface iv

1 Introduction 2
- 1.1 Energy Harvesting . . . 2
- 1.2 Cold Start . . . 2
- 1.3 Wearable Application . . . 3
- 1.4 Maximum Power Point Tracking . . . 3
- 1.5 Objectives . . . 3
- 1.6 Structure . . . 3

2 Ambient Energy Source 6
- 2.1 Introduction . . . 6
- 2.2 Thermal Energy . . . 6
  - 2.2.1 Seebeck Effect & Pyroelectric Effect . . . 6
  - 2.2.2 Thermal Energy Harvester . . . 6
- 2.3 Electromagnetic Energy . . . 6
  - 2.3.1 Electromagnetic Spectrum . . . 7
  - 2.3.2 Ambient Light Energy Harvesting . . . 8
  - 2.3.3 Photovoltaic Cell Harvester . . . 8
  - 2.3.4 RF Energy Harvesting . . . 9
  - 2.3.5 RF Energy Harvester . . . 9
- 2.4 Chemical Energy . . . 10
  - 2.4.1 Biofuel Cell & Hydrovoltaic Effect Generator . . . 10
  - 2.4.2 Chemical Energy Harvester . . . 10
- 2.5 Kinetic Energy . . . 10
  - 2.5.1 Kinetic Energy Harvesting Techniques . . . 11
  - 2.5.2 Resonant System & Non-Resonant System . . . 11
  - 2.5.3 Existing Kinetic Energy Harvester . . . 11
  - 2.5.4 Kinetic Energy Harvesting From Human Motion . . . 11
  - 2.5.5 Piezoelectric Versus Triboelectric . . . 12
- 2.6 Discussion and Conclusion on Energy Harvesting in wearable devices . . . 14

3 Piezoelectric Energy Harvesting 18
- 3.1 Introduction . . . 18
- 3.2 Equivalent Circuit of Piezotransducer . . . 18
- 3.3 Conjugate Matching Circuit . . . 18
- 3.4 Rectifying Circuit . . . 19
  - 3.4.1 Standard Rectifying Circuit . . . 19
  - 3.4.2 Maximum Power Point Tracking . . . 20
- 3.5 Figure of Merit . . . 21
- 3.6 Piezoelectric Energy Harvesting Techniques . . . 21
  - 3.6.1 Switch-Only Rectifier . . . 21
  - 3.6.2 Synchronous Switching Harvesting on Inductor (SSHI) . . . 21
  - 3.6.3 Synchronous Switching Harvesting on Capacitor (SSHC) . . . 22
  - 3.6.4 Inductive and Capacitive Flipping Techniques Comparison . . . 23
  - 3.6.5 Other Types of Synchronous Switching Harvesting Circuit . . . 24
  - 3.6.6 (Phase Shift) Synchronous Electric Charge Extraction ((PS-)SECE) . . . 24
  - 3.6.7 Double, Enhanced, Adaptive Synchronized Switch Harvesting . . . 26
- 3.7 Cold Start Capability . . . 26

3.8 Conclusion on Piezoelectric Energy Harvesting Techniques . . . 26

4 Cold Start of Piezoelectric Energy Harvester 28
4.1 Introduction . . . 28
4.2 Cold Start of Piezoelectric Energy Harvester . . . 28
4.2.1 Discussion on Topology . . . 30
4.2.2 Conclusions on Topology . . . 30
4.3 Rectification . . . 31
4.3.1 Diode-Connected Full-Bridge Rectifier . . . 31
4.3.2 Diode-connected Transistor and Cross-coupled Transistor Rectifier . . . 31
4.3.3 Fully Cross-coupled Rectifier . . . 32
4.3.4 Active Rectifier . . . 32
4.3.5 Discussion on Rectifier . . . 33
4.4 Two-Stage Rectification. . . . 34
4.5 SSHC Technique . . . 34
4.5.1 Zero Crossing Detection . . . 35
4.5.2 Direction Detection . . . 35
4.5.3 Pulse Generation . . . 35
4.5.4 Pulse Sequencing . . . 36
4.5.5 Conclusion on SSHC circuit . . . 36
4.6 Supporting Blocks . . . 36
4.6.1 Current Source . . . 36
4.6.2 Bootstrap circuit . . . 37
4.6.3 voltage-level detector . . . 38
4.6.4 Summary on Supporting Blocks . . . 38
4.7 Top Level Design . . . 39

5 Verification Scenario 42
5.1 Introduction . . . 42
5.2 Application . . . 42
5.3 Start-Up Requirements . . . 42
5.4 Circuit Modelling . . . 43
5.5 Input Power . . . 43
5.5.1 Input Power Definition . . . 43
5.5.2 Input Parameters of Piezotransducer . . . 43
5.5.3 Limitation of the System . . . 44
5.6 Subsystem Verification . . . 44
5.7 Verification Overview . . . 45

6 Cold-Start SSHC design 46
6.1 Introduction . . . 46
6.2 Cross-Coupled Rectifier . . . 46
6.3 Current source . . . 47
6.4 Delay Cell . . . 47
6.5 Active Diode . . . 48
6.5.1 Switch Type . . . 48
6.5.2 Active Diode Comparator . . . 49
6.5.3 On-Resistance Trade Off . . . 52
6.5.4 Active Diode Stability . . . 53
6.6 SSHC Technology . . . 55
6.6.1 Zero-cross Detection . . . 55
6.6.2 Direction Detection . . . 55
6.6.3 Pulse Generation and Sequencing . . . 55
6.6.4 Switches in SSHC . . . 56
6.6.5 Phases Selection . . . 56
6.7 Bootstrap Circuit . . . 57
6.8 Pulse Chain . . . 59
6.8.1 Schmitt Trigger Inverter . . . 59

6.9 Voltage-Level Detector . . . 59
6.10 Conclusions . . . 60

7 Result **62**
7.1 Introduction . . . 62
7.2 Sub-block Test . . . 62
7.2.1 Current Source . . . 62
7.2.2 Active-Diode Comparator . . . 64
7.2.3 Zero-Crossing Detection . . . 66
7.2.4 Direction Detection . . . 67
7.2.5 Pulse Generation and Sequencing . . . 67
7.3 Cold-Start Test . . . 68
7.3.1 Typical Case . . . 68
7.3.2 Transition during Start-up . . . 70
7.3.3 Behaviour of Sub-Blocks during the Start-Up . . . 70
7.3.4 Other Input Scenarios . . . 71
7.3.5 Voltage-Level-Detector Test . . . 73
7.3.6 Start-up Voltage of Each Block . . . 73
7.3.7 Minimum input power and frequency of the System . . . 74
7.4 Normal Operation Verification . . . 74
7.4.1 Output Power . . . 74
7.4.2 Power-Consumption Breakdown . . . 75
7.5 Layout and Extraction Result . . . 75
7.6 Overview of the Test Results . . . 75

8 Discussion **78**
8.1 Design Result . . . 78
8.2 Verification Result . . . 78
8.3 Comparison to Other Designs . . . 79
8.4 Discussion . . . 80

9 Conclusions **82**
9.1 Overview . . . 82
9.2 Contributions . . . 83
9.3 Future Work . . . 83

A Boundary of the start-up **86**
A.1 Minimum input power for different frequencies at TT27 . . . 86
A.2 Minimum input power for 1Hz excitation frequency at FF85 . . . 87
A.3 Minimum input frequency for 1uW input power at TT27 . . . 87

B Layout **88**

Bibliography **89**

1 Introduction

The Internet of Things (IoT) is now ushering in a hyper-connected world of seamless information exchange. It has been implemented in a wide range of applications such as healthcare, wearable devices, automation, industrial processes and environmental monitoring[13].

One of the greatest bottlenecks of IoT devices is the massive logistical and economic problem caused by the batteries. While modern ultra-low power integrated circuits consume so little power that these devices can run for years without replacing the batteries, this does not seem to be enough in terms of the overall lifetime of these devices. Installing, maintaining and replacing these batteries is by no means an elegant solution.

As more and more devices are connected to people's lives, battery solutions are neither practical nor feasible anymore. Therefore, the need for devices that can run without a battery has become increasingly important, and battery-less systems are believed to be the future of the IoT.

1.1. Energy Harvesting

One of the very promising solutions for the problem addressed above is energy harvesting. Energy harvesting refers to the process of capturing energy from the ambient environment and converting energy into electricity, which can either be used immediately or stored in a battery or a super-capacitor. Energy harvesting makes use of ambient energy, which will normally be dissipated or wasted in the form of heat, vibration and light.

There are vast quantities of energy in the environment at any given moment, in whatever form: light, sound, radio waves, vibration, heat, etc. The amount of available energy can be extremely small and sometimes unpredictable, so power management is introduced to ensure enough energy can be captured from the energy source and transferred into the correct form to enable the reliable operation of IoT devices.

Many different energy harvesting techniques for various energy sources have been introduced in recent years. However, all energy harvesting systems have three main components: 1) a transducer, 2) a power-management circuit and 3) a load.

- Transducer: The transducer is the part that converts ambient energy into electricity.
- Power-management circuit: The power-management circuit serves two purposes. Firstly, the interface circuit can track the output of the transducer and extract the maximum possible energy. Secondly, the interface circuit can condition the energy into a suitable form for the desired application.
- Load: The load includes the storage elements and other devices that consume energy.

1.2. Cold Start

While as promising as the battery-less may sound, one key issue that may occur with such a system is that when the storage of the system is empty, there is no power source for the active circuit to start the harvesting, so the harvester is in a dead state. This situation typically happens when the harvester

is fabricated and never powered up or when the harvester has not been used for a long time and the storage is completely depleted. The system should be able to start from such an energy-depleted state, a process known as 'Cold Start'.

1.3. Wearable Application

In recent years, portable and wearable devices such as smartwatches, smart glasses and smart training shoes are growing rapidly and bringing convenience to people's lives. As previously mentioned, the power supply is one of the issues for wearable devices.

A self-powered system provides great potential for wearable devices by using various ambient energy from the human body. Energy harvesting is the basics of a self-powered system. Potential ambient energy sources around the human body are extensive, such as mechanical energy, thermal energy, solar energy and chemical energy. Specifically, mechanical energy can be harvested from daily walking, running, or finger bending. The biochemical environment of the human body can act as an energy source for biofuel cells. Thermal energy exists when there is a temperature difference between the human body and the environment. And solar energy can be harvested when humans are exposed to the sun or other sources of light. Based on the characteristics of these energies, substantial attention has been paid to energy harvesting systems suitable for efficiently collecting various forms of energy.

1.4. Maximum Power Point Tracking

Maximum power point tracking (MPPT) is essential in energy harvesting. The MPPT is an impedance-matching technique for the energy harvester. The MPPT tracks the source characteristics and controls the power-management circuit so that the impedance seen by the energy sources is always optimal. Essentially, the load impedance is decoupled from the source impedance.

1.5. Objectives

The objective of the thesis project is defined as:

Design a cold-start circuit for the kinetic energy harvester that aims to harvest vibration energy from human movements

The limitation of the project is mainly set by the application of the harvester and requirements from Nexperia Energy Harvesting. The design questions and objectives based on these limitations are given as follows:

- What is the proper energy harvester for vibration energy harvesting on human motion?
- How much energy can be expected from human motion, and what is the frequency of human motion?
- What are the targets for the cold-start circuit?
- What is the minimum input level of the cold-start circuit?
- What techniques can be used for vibration energy harvesting? and which techniques can be used for cold-start applications?
- Design a cold-start circuit for the vibration energy harvester.
- The designed cold-start circuit should minimise the area consumption.
- The cold-start circuit should not affect the normal operation of the main harvester after the cold-start.

1.6. Structure

The structure of the report is constructed as follows:

Chapter 2 investigates the Ambient energy sources that can be harvested around humans. The principle of kinetic energy harvesting will be studied in detail, and the most suitable energy source will be decided.

Chapter 3 will introduce the existing techniques for vibration energy harvesting. The pros and cons of different techniques will be summarized, and the most suitable technique for the project application will be decided.

Chapter 4 will discuss the structure of the cold-start circuit. The top-level design will be concluded.

Chapter 5 will introduce the verification method of the cold-start circuit.

Chapter 6 will discuss the transistor-level design of the cold-start circuit in detail.

Chapter 7 will show the verification result based on the methods proposed in Chapter 5. Single circuit block will first be verified. System verification comes next.

Chapter 8 discusses the design process and verification results. The performance of the proposed circuit is compared to other designs. Some general remarks on the circuit are given as well.

Chapter 9 concludes the entire thesis project, highlights the contributions and gives recommendations for further optimization.

2

Ambient Energy Source

2.1. Introduction

Ambient energies that can be harvested around the human body are introduced in this chapter. The working principles of four major energy sources, thermal energy, kinetic energy, electromagnetic energy and chemical energy, are introduced. The suitability of each energy source for wearable applications will be discussed, and conclusions will be made in the end.

2.2. Thermal Energy

In this section, two mechanisms of thermal energy harvesting are introduced. Some previous research on thermal energy harvesting is summarized.

2.2.1. Seebeck Effect & Pyroelectric Effect

Temperature differences exist between the human body and the environment at almost every moment of the day. Two mechanisms, the Seebeck effect and the Pyroelectric effect are employed for two popular thermal energy harvesting generators: thermoelectric generators (TEG) and pyroelectric generators (PEG). The pyroelectric generators produce charge fluctuation from time-dependent temperature fluctuations. The thermoelectric generators produce a voltage when there is a temperature difference across the conductors.

A thermoelectric generator (TEG) is a direct-current power generation device made by a group of semiconductor thermocouples [58]. Each thermocouple consists of an n-type semiconductor and a p-type semiconductor. The connecting end of the two semiconductors is in contact with the hot end, and the non-junction end is in contact with the cold end. Due to the temperature difference, holes will accumulate at the cold end of the p-type semiconductor, and electrons will accumulate at the cold end of the n-type semiconductor, which will generate a potential difference. The structure and working principle of TEG are shown in Figure 2.1.

A pyroelectric generator (PEG) is another type of thermal energy harvester based on the pyroelectric effect. For a crystal with a spontaneous polarization property, when the crystal is heated or cooled, the intensity of spontaneous polarization changes due to the change in temperature, which leads to the generation of surface polarization charges in a certain direction of the crystal [58]. The structure and working principle of PEG are shown in Figure 2.2.

2.2.2. Thermal Energy Harvester

Applications of TEG and PEG have been studied extensively. Table 2.1 presents a group of thermal energy harvesters. In the table, the performance is measured by the power per square centimetre. The temperature variations of the experiments are also noted.

2.3. Electromagnetic Energy

In this section, electromagnetic energy harvesting is introduced. Based on the frequency band, electromagnetic energy harvesting includes ambient light energy harvesting and RF energy harvesting.

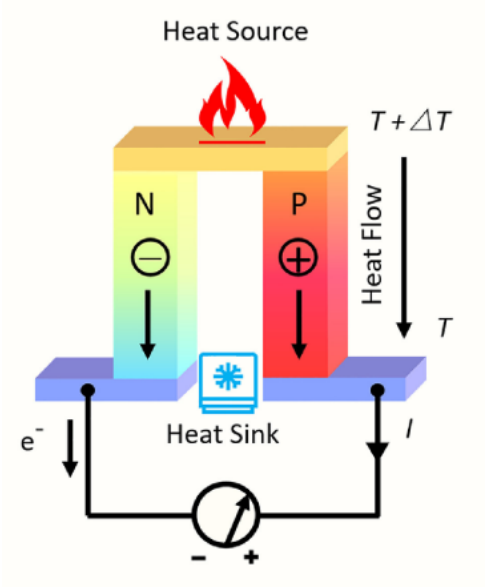


Figure 2.1: Working principle of the TEG [58]

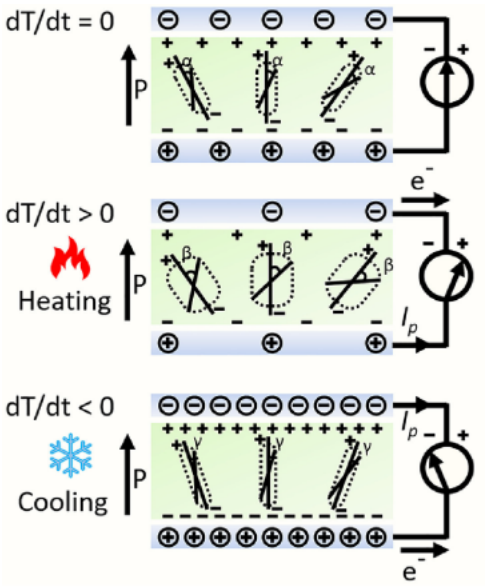


Figure 2.2: Working principle of the PEG [58]

Table 2.1: Available TEG and PEG from the literature study

Source	Harvester Type	Power Density	Temperature Variation	Size (cm^2)
[23]	TEG	3.8mW/cm^2	50K	0.03
[22]	TEG	14.9uW/cm^2	15K	0.015
[38]	TEG	83nW/cm^2	10K	150
[12]	TEG	11.14mW/cm^2	50K	10.2
[55]	PEG	4.64pW/cm^2	9K (rapidly)	0.15
[54]	PEG	0.7uW/cm^2	13K/s	12.25
[20]	PEG	6.47uW/cm^2	3.5K/s	0.25

Each energy source is introduced respectively. Some existing electromagnetic energy harvesters are presented for ambient light energy harvesting and RF energy harvesting, respectively.

2.3.1. Electromagnetic Spectrum

The electromagnetic spectrum, seen in Figure 2.3, contains all frequencies of electromagnetic radiation that propagate energy in the form of electromagnetic waves. Based on the frequency, the electromagnetic spectrum can be divided into the radio spectrum and the optical spectrum. Energy harvesting from the optical spectrum is referred to as ambient light energy harvesting, for example, solar energy harvesting and indoor light harvesting. From the radio spectrum, there is RF energy harvesting.

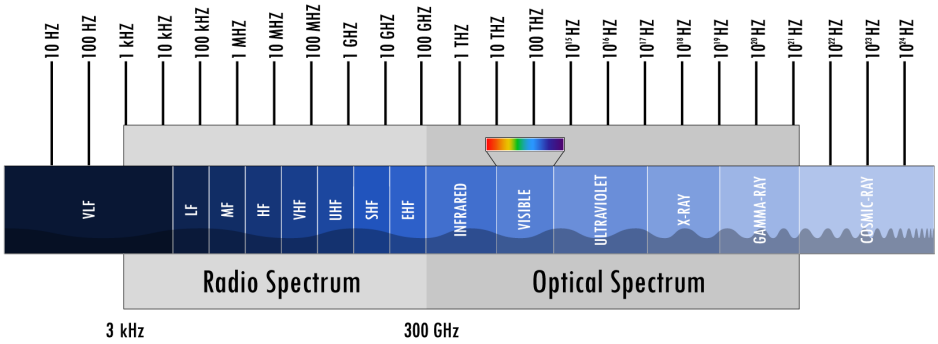


Figure 2.3: Electromagnetic spectrum [31]

2.3.2. Ambient Light Energy Harvesting

The harvesting of ambient light energy has been studied for decades. Solar energy radiation is the light and heat from the sun. It is the most common energy source used in energy harvesting systems. Indoor lighting is another type of popular source for harvesting.

The most common harvester is the photovoltaic cell (PV cell). The most important part of a PV cell is a specially treated semiconductor layer. The semiconductor layer consists of an n-type and a p-type semiconductor layer, and the conversion from light to electricity is based on the photovoltaic effect.

The photovoltaic effect is the process that generates voltage or current in a PV cell when it is exposed to sunlight. The semiconductor layer in the PV cell essentially forms a PN junction where electrons move to the positive p-side and holes move to the negative n-side. When the PV cell is exposed to light with a suitable wavelength, the protons of the light will transfer energy from the photon to an electron-hole pair in the semiconducting material, causing an electron current. The electrons will, therefore, create an electric current in the cell. The working principle of the PV cell is demonstrated in Figure 2.4

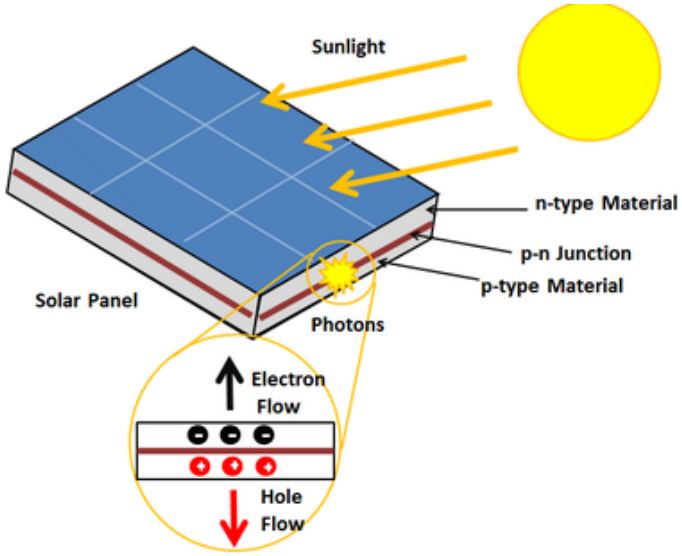


Figure 2.4: Working principle of the PV cell [11]

2.3.3. Photovoltaic Cell Harvester

A list of commercial PV cells intended for wearable applications is listed in Table 2.2. Their open-circuit voltage, short-circuit current, output power, and area are compared under 'AM1.5' conditions: a solar power of 1000W/m^2 (direct sunlight illumination) and at the temperature of 25°C.

Table 2.2: Commercial photovoltaic cell

Source	Type	Voltage(oc) (V)	Current(sc) (mA)	Power (mW)	Size (mm)
[29]	Rigid	0.63	50	22.3	22×7×1.8
[14]	Flexible	4.5	10.7	25.5	12.7×64×0.2
[5]	Rigid	3.64	4.7	13.5	24×9.5×5.1

2.3.4. RF Energy Harvesting

The fast-growing fields of wireless communication and radio sensing have covered a wide frequency band, especially in the urban area. This provides great potential for harvesting ambient RF energy. The ambient RF energy harvesting system includes a receiving antenna, an impedance-matching circuit, a rectifying circuit and a power management circuit. A high-efficiency antenna captures ambient RF energy and converts it into electrical energy. An impedance-matching circuit is used to maximize the energy transfer from the antenna to the load. A rectifying circuit converts the voltage to DC for further storage or usage. Normally, a power-management circuit is used to ensure maximum output power. A complete RF energy harvesting system can be seen in Figure 2.5.

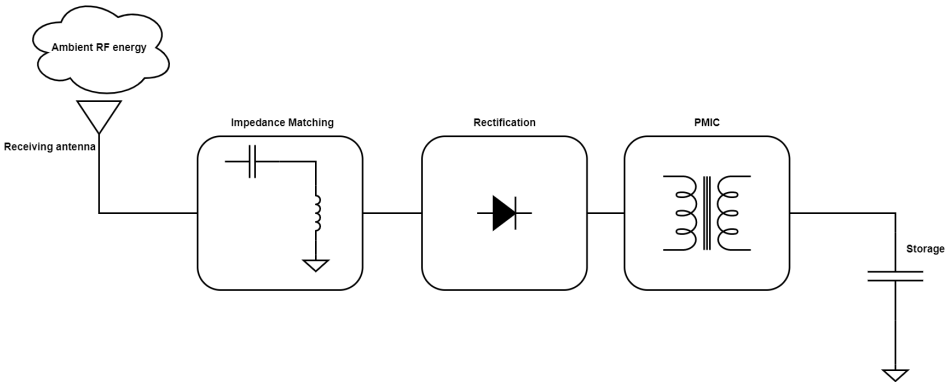


Figure 2.5: Working principle of the RF energy harvesting system

2.3.5. RF Energy Harvester

There has been a lot of research on circuit implementations for RF energy harvesting. Table 2.3 concludes with examples of different circuit topologies. The minimum input power to achieve 1V output voltage and the input power to achieve maximum efficiency are noted. Power is given in dBm, where -20dBm equals 10 µW.

Table 2.3: RF energy from different sources

Source	Minimum input power	Peak efficiency	Frequency
[35]	-23dBm	11% at -15dBm	915MHz
[46]	-3.2dBm	83% at -1dBm	2.45GHz
[32]	-10dBm	10% at -10dBm	915MHz
[44]	-26.3dBm	31.5% at -15dBm	868MHz
[45]	-27dBm	40% at -17dBm	868MHz

For ambient RF energy harvesting in the Netherlands. The frequency band now covers: 900MHz & 1800MHz for 2G, 900MHz & 2100MHz for 3G, 800MHz, 900MHz, 1800MHz, 2100MHz and 2600MHz for 4G and 700MHz, 3.5GHz and 26GHz for 5G. WiFi covers 2.4GHz, 3.6GHz, 4.9GHz, 5GHz, and 5.9GHz.

2.4. Chemical Energy

In this section, two types of chemical energy harvesting techniques from the human body are introduced. Some previous research on chemical energy harvesting is summarized.

2.4.1. Biofuel Cell & Hydrovoltaic Effect Generator

The collection and conversion of chemical energy in the human body are usually accompanied by chemical reactions as well as the transfer of electrons in chemical substances [58]. Mainly, two types of chemical energy harvesting are popular for human chemical energy harvesting: biofuel cells (BFC) and hydrovoltaic effect generators (HEG).

A biofuel cell (BFC) is a harvester that utilizes the redox reaction in living organisms to generate electricity. Based on the crystal type, it can be classified into enzymatic fuel cells (EFCs) and microbial fuel cells (MFCs). MFC is currently not an interesting research direction because the output power is related to the diffusion rate of the carrier in the biofilm, which is typically very low. The working principle of a glucose biofuel cell is shown in Figure 2.6. It can be seen that the basis of a biofuel cell is the process of electron transfer from the anode to the cathode through redox reactions of substances. When the fuel substrate is sufficient and the activity of the enzyme is ensured, the biofuel cell can produce continuous current.

Hydrovoltaic effect generator (HEG) is the other harvester that utilizes the interaction between nanomaterials and water molecules that convert the water energy into electricity. Recent research focuses on the electricity generation effects induced by water evaporation and humidity since these two processes completely rely on the natural water evaporation and the humidity in the environment. The working principle of a HEG using a porous carbon nanomaterial is depicted in Figure 2.7. In the evaporation process, the flow of water molecules in the gap of nanomaterials induces the generation of voltage and current, which is similar to the traditional streaming potential. For humidity-induced power generation, the electricity generated depends on reversible changes between hydration and dehydration [58]. When there is a concentration gradient, free hydrated ions will move from a higher concentration to a lower concentration, creating electricity.

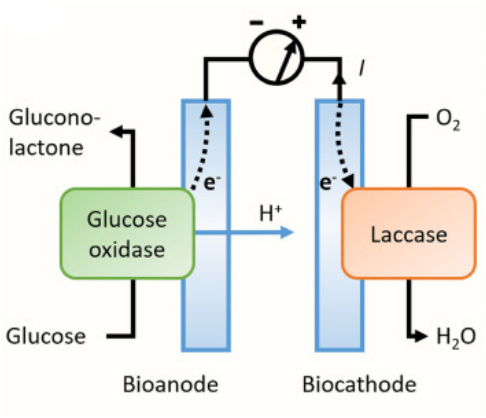


Figure 2.6: Working principle of the BFC [58]

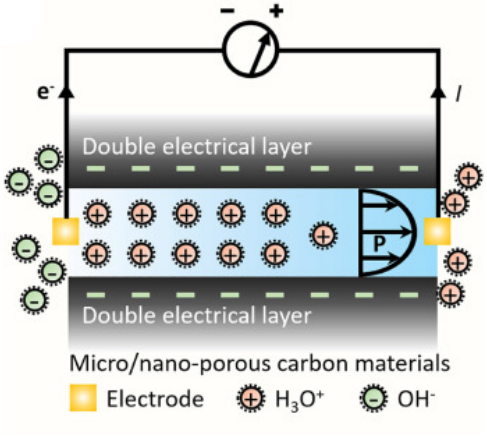


Figure 2.7: Working principle of the HEG [58]

2.4.2. Chemical Energy Harvester

A list of chemical energy harvesters is shown in Table 2.4. The output characteristics are defined as the open-circuit voltage and short-circuit current.

2.5. Kinetic Energy

This section presents the principles of the four main kinetic energy harvesting techniques first. Secondly, two categories that classify systems and existing harvesters are presented respectively. Third, facts of kinetic energy harvesting from the human body are investigated. Finally, a comparison of the two prominent harvesters is presented.

Table 2.4: Available BFC and HEG from the literature study

Source	Harvester Type	Power Density	V(oc)/I(sc))	Size (cm^2)
[1]	BFC	1.2mW/cm^2	0.5V/1mA	-
[34]	BFC	6.5mW/cm^2	0.31V/12uA	-
[53]	HEG	21.2nW/cm^2	1V/150nA	1×2.5
[26]	HEG	0.246mW/cm^2	0.5V/1.5uA	6.1×10^{-4}
[41]	HEG	0.21uW/cm^2	0.34V/10.5uA	15cm fiber
[56]	BFC	3.5mW/cm^2	0.6V/-	1

2.5.1. Kinetic Energy Harvesting Techniques

Scavenging energy from human motion can be traced back one hundred years ago. Four harvesting mechanisms have been studied extensively: piezoelectric, triboelectric, electrostatic and magnetostatic. The principles of four types of harvesters are introduced and visualized in Figures 2.8-2.11

- Piezoelectric: The energy conversion of a piezoelectric nanogenerator (PENG) is based on the piezoelectric effect. When an external force is applied to the piezoelectric material, the relative displacement of positive and negative ions in the unit cell causes the positive and negative charge centres to no longer coincide [58], forming a displacement current.
- Triboelectric: The energy conversion of triboelectric nanogenerators (TENG) depends on the coupling of triboelectricity and electrostatic induction. Horizontal motion, vertical motion and torsional stress will induce a triboelectric charge on the material surface, which will generate a current to the external circuit.
- Electrostatic: The electrostatic vibration energy harvester (e-VEH) consists of two pre-charged capacitor plates. The relative movement of two plates will cause a capacitance change, which will generate a current to the external circuit.
- Magnetostatic: The magnetostatic generator or electromagnetic generator (EMG) is based on Faraday's law, whereby a potential difference is induced when an electric conductor moves through a magnetic field [28].

2.5.2. Resonant System & Non-Resonant System

For vibration energy harvesting, a typical structure used is a cantilever structure (Figure 2.8). For such a system, a resonant frequency exists at which the harvester will output the maximum power. Typically, the resonant frequency of a commercial piezotransducer, for example, a MIDE V22B, is around hundreds of hertz without a tip mass. The resonant frequency can be tuned to the desired excitation frequency by utilizing a tip mass. Such a system is a resonant system.

Non-resonant systems do not have a particular resonant frequency and thus can convert energy over a wide frequency range. Energy in a non-resonant system is generated by the mutual friction or collision of internal structures during vibration. The advantage of these systems is that the output power remains or increases with the increase of vibration frequency. A non-resonant system is normally a custom-made device. No commercial device is available for such a system.

2.5.3. Existing Kinetic Energy Harvester

Some previous designs of the resonant systems and non-resonant systems are concluded in Tables 2.5 and 2.6, respectively. The mechanism of these systems is noted. The heights of PENG, TENG and e-VEH are a few millimetres, which is generally much smaller than that of EMG. The magnetostatic generators are cylindrical, and the heights are noted.

Resonant System

Non-Resonant System

2.5.4. Kinetic Energy Harvesting From Human Motion

[50] measures the frequency of walking and running. The frequency of the human body, in most cases, is below 10Hz. [28] investigated the kinetic energy harvesting from the upper limb. From the daily action, handshaking, finger bending, walking, hand clapping etc., the frequency is under 5Hz. The

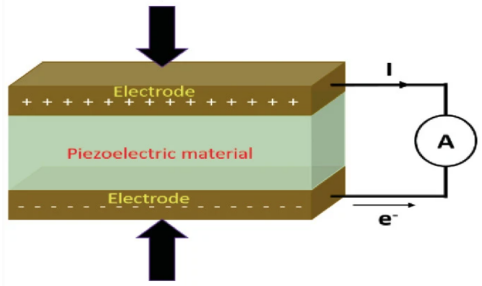


Figure 2.8: Principle of the piezoelectric generator [2]

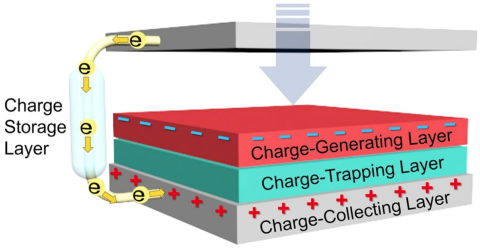


Figure 2.9: Principle of the triboelectric generator [21]

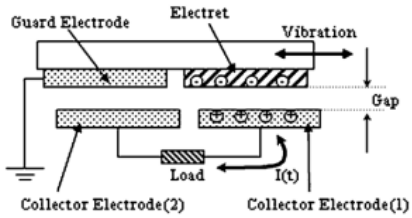


Figure 2.10: Principle of the electrostatic generator [30]

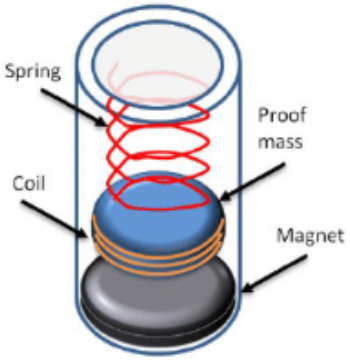


Figure 2.11: Principle of the magnetostatic generator [25]

Table 2.5: Resonant kinetic energy harvesters

Source	Type	Frequency (Hz)	Maximum Power	Size (mm^2)	Load (Ω)
[16]	PENG	80	3uW	23×23	333k
[48]	PENG	212	0.28mW	37×12	23k
[43]	PENG	68	0.023uW	7×5.5	40k
[42]	PENG	2	50uW	31.8×12.7	700k
[42]	PENG	2	18uW	36×16	700k
[6]	PENG	214	0.62uW	1.6×1.6	3M
[47]	PENG	2	27.64mW	71×25.4	7.5k

amplitude depends on which part of the body. In general, hundreds of nW to a maximum of tens of mW can be harvested from human motion.

More Discussion on Kinetic Energy Harvester

Several factors need to be considered when harvesting vibration energy from humans. First, the size of the harvester should be small enough to be compatible with humans. Second, the frequency range of the human body is usually below 10Hz, and the device has to be able to operate in this frequency range. The output power of a magnetostatic generator is related to the number of coils and the magnetic mass. Conventional magnetostatic generators are usually large and heavy to obtain higher power and operate at high frequencies. Therefore, magnetostatic generators will not be considered further. The mechanisms of the electrostatic generator and triboelectric generator both depend on electrostatic induction. However, the electrostatic generator requires the capacitor plates to be pre-charged, which might be a drawback for fabrication. A comprehensive comparison between the piezoelectric generator and the triboelectric generator conducted in [47] will be presented in the coming section.

2.5.5. Piezoelectric Versus Triboelectric

On the basis of the triboelectric harvester, four working modes have been developed: contact-separation mode (CS), lateral-sliding mode (LS), single-electrode mode (SE), and freestanding triboelectric-layers

Table 2.6: Non-resonant kinetic energy harvesters

Source	Type	Frequency (Hz)	Maximum Power	Size (mm)	Load (Ω)
[37]	TENG	5	171.13uW	26×50.5	8M
[37]	EMG	5	102.12mW	26×26×50.5	220
[24]	e-VEH	1	8uW	10×10	10M
[18]	EMG	4.6	110uW	13×13×50	17
[52]	PENG	5	128.51uW	25.1×16.8	11k
[39]	PENG	1	35uW	12×11	2M
[36]	EMG	0.25	319uW	12×12×40	40.3
[40]	e-VEH	20	10uW	5.5×5.5	-
[47]	TENG	2	1.52mW	5×5	21M

mode (FS). Figure 2.12-2.15 explains these four modes [51]. From the perspective of the output power, FT>CS>LS>SE. The piezoelectric harvester has two working modes, d_{33} mode and d_{31} mode. The former indicates that the direction of vibration is perpendicular to the piezotransducer as Figure 2.8, and the latter indicates that the direction of vibration is aligned with the transducer. The output power of the d_{33} mode is much larger than the one of the d_{31} mode since the d_{33} coefficient is several orders of magnitude larger than the d_{31} coefficient

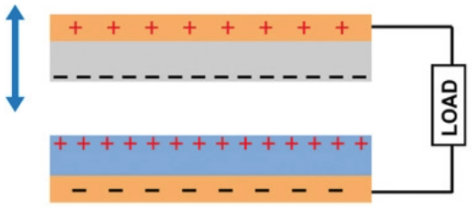


Figure 2.12: Contact-separation Mode [51]

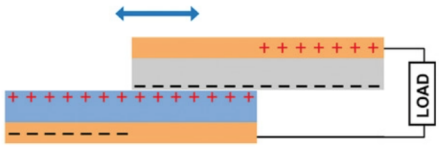


Figure 2.13: Lateral Sliding Mode [51]

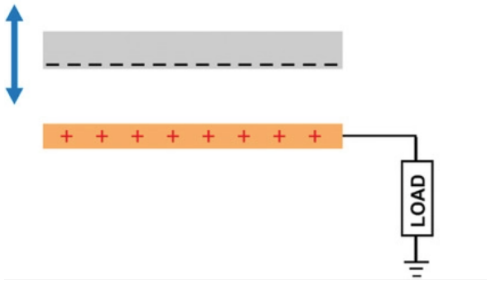


Figure 2.14: Single-electrode Mode [51]

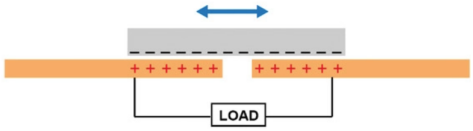


Figure 2.15: Freestanding Triboelectric-layers Mode [51]

For a fair comparison, the single-electrode (SE) TENG has a similar structure with PENG working in d_{33} mode [47]. The transferred charge Q and open-circuit voltage V_{oc} of a d_{33} mode PENG and a single-electrode TENG are given in Equation 2.1 and 2.2 and Equation 2.3 and 2.4 respectively [19].

$$Q = A\sigma_{33}d_{33} \tag{2.1}$$

$$V_{oc} = T\sigma_{33}d_{33} \tag{2.2}$$

In which d_{33} is the piezoelectric coefficient, A is the area of the piezo material, T is the thickness of the device, and σ_{33} is the stress along the direction of the applied force.

$$Q = \frac{1}{2}A\sigma_q \tag{2.3}$$

$$V_{oc} = \frac{1}{2}\frac{T}{\epsilon}\sigma_q \tag{2.4}$$

In which A is the area of the conducted surface, T is the thickness of the device, σ_q is the surface charge density caused by contact electrification and ϵ is the permittivity of the dielectric material.

Prototypes of a piezoelectric harvester and a triboelectric harvester are manufactured in [47]. The volume of PENG is 6.05cm^3 in which 4.7cm^3 is contributed by the tip mass, and the volume of TENG is 3.05cm^3. Two devices are tested under the same test bench and frequency. The working mode of TENG is SE and d_{33} for PENG. The power density and power density/cost are compared under different frequencies, seen in Figures 2.16 and 2.17.

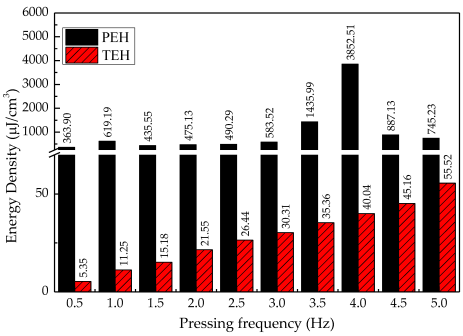


Figure 2.16: Energy density of PENG & TENG under different frequencies [47]

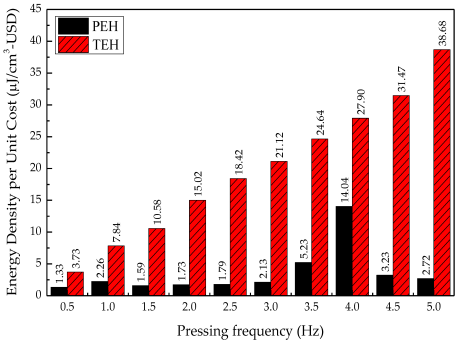


Figure 2.17: Energy density per unit cost of PENG & TENG under different frequencies [47]

Some insights can be drawn from [47]:

- The size of these two harvesters is similar. The materials for fabrication are commonly used materials, the test bench is the same, the working structure of the two devices is similar, and the test frequency is the frequency of human movement. Therefore, for wearable applications, the conclusion drawn on output power and the economy is fair.
- The energy density of the PENG is much higher than that of TENG. However, The energy density of TENG increases linearly with the frequency. Within the interesting frequency of human motion, the PENG still achieves a higher energy density.
- TENG is a lot cheaper than PENG in this experiment. However, for mass production, this might not be the case. There are already commercial piezotransducers available but TENGs are still custom-made for specific research currently and will be complicated to fabricate.
- The variation of energy density reflects the difference between the resonant system and the non-resonant system. The resonant frequency of the piezo cantilever in [47] is tuned to be 12Hz. The peek at 4Hz might result from the harmonics of the excitation frequency. For TENG, output power increases with the excitation frequency.

In addition, several major challenges of triboelectric energy harvesting are pointed out by [33]. First, the output characteristic of TENG is usually in the form of a pulse while it is a sinusoidal wave in PENG (Figures 2.18 and 2.19). TENG can only provide power at the instance the motion reaches its peak. It will be difficult for TENG to output a constant large current, and sporadic energy spikes are a challenge for the PMIC design due to the sudden large amplitude of voltage and current. Second, [47] shows that at the maximum power point, the open-circuit voltage of TENG is 125V, and the short-circuit current is only 10uA. while it is 15V and 2mA for PENG. So the internal impedance of TENGs is much bigger than that of PENGs. The huge impedance mismatch between TENGs and storage devices can make it hard for the storage elements to reach the desired power level. Third, TENG is very sensitive to the environment, such as humidity fluctuation, which will change the conductivity between two plates significantly.

2.6. Discussion and Conclusion on Energy Harvesting in wearable devices

For wearable applications, the pyroelectric generator has been discarded as an energy source due to the low frequency and small amplitude of temperature fluctuations around humans and the near

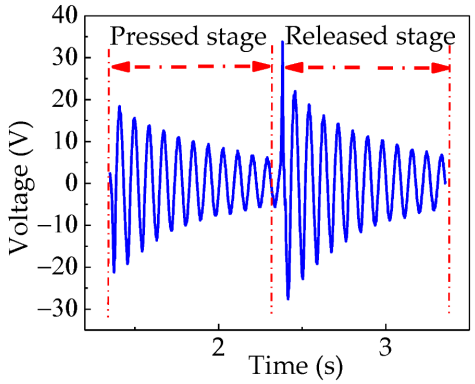


Figure 2.18: Output characteristic of the PENG under one excitation cycle [47]

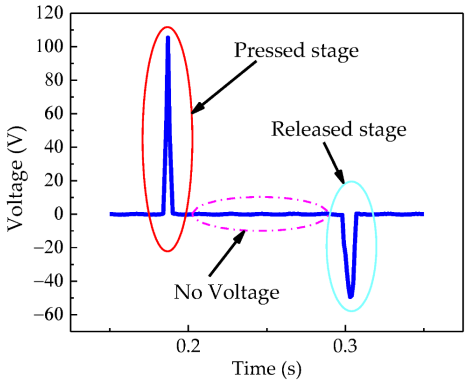


Figure 2.19: Output characteristic of the TENG under one excitation cycle [47]

absence of significant changes in body temperature over time. The same reason goes for the hydrovoltaic effect generator; it is not likely to observe significant or lasting humidity variation around humans. Therefore, only minor energy can be harvested from the human body for these two harvesters.

The thermoelectric generator is not suitable for wearable applications either. First, the TEG requires temperature differences across the devices. Typically, one end of the device should be in direct contact with the human body, and the other end exposed to the environment. So the application scenarios are limited. Second, the basis of TEG is that it will draw the heat from the heat source to the heat sink. As a result, the body will get colder, and both ends will reach the same temperature eventually. This may make some users feel uncomfortable, and also, the TEG has to be made large enough to slow down the speed of temperature reaching equilibrium so that a long-lasting harvesting period is ensured. Third, only a small temperature difference between the body and the environment can be expected in reality, and thus, the output power will be small.

For biofuel cells, although it is not constrained by the environment, there are critical drawbacks for these harvesters. First, the sustainability of the fuel has not yet been addressed. In the case of glucose biofuel cells, for example, glucose can either come from the human body or an external storage tank. Neither of these solutions is an elegant solution. For the former solution, [34] pointed out that the maximum experimental time is 20 minutes in one day before harming the human body. The latter solution makes no difference from traditional battery replacement. Second, to ensure the harvester harvests harmlessly from the human body, a series of standards (ISO 10993) for evaluating the biocompatibility of medical devices to manage biological risk is introduced. Thus, the design of the harvester for long-term usage would be a challenge since the materials required for biofuel might not be allowed due to ISO 10993.

RF energy harvesting will first require a high-efficiency receiving antenna, which will occupy a considerable amount of space, and the shape of the antenna will limit the freedom of design. In addition, electromagnetic fields can be attenuated by anything in and around humans: clothes, skin, concrete, etc. Therefore, RF energy harvesting is not suitable for energy harvesting around the human body.

Kinetic energy harvesting is not limited by the environment. Most non-resonant systems are designed at the frequency of human motion (below 10 Hz). Resonant systems are capable of harvesting energy at low frequencies as well. Magnetostatic will not be further considered because the size of such devices is not suitable for wearable applications. Electrostatic, triboelectric and piezoelectric seem fine for energy harvesting around the human body. However, electrostatic generators have the issue of precharging, which can be a challenge during fabrication. The triboelectric generator has very high internal impedance. The CMOS technology cannot handle the high output voltage from the triboelectric generator for maximum power point conversion. Also, both generators require custom-made MEMS. As for the piezoelectric generator, it is a cheap and simple structure device that can output lots of power and the matching requirement for such a device is eased. And there are commercial piezoelectric energy harvesters (MIDE V22 series) available already.

Ambient light energy harvesting, especially solar energy harvesting, does not have any drawbacks except the requirement for the presence of light. It can provide enough power for wearable applications as well. In fact, there are already wearable devices powered by solar energy, such as smartwatches

and smart bands.

In conclusion, ambient light energy harvesting and piezoelectric energy harvesting are both promising for energy harvesting around the human body. For the interest in this study, piezoelectric energy harvesting will be the direction for further study.

3

Piezoelectric Energy Harvesting

3.1. Introduction

Piezoelectric energy harvesting will be studied further in this chapter. First, the equivalent circuit and the ideal matching circuit of the piezotransducer are introduced. Second, existing harvesting techniques are introduced and compared. Finally, a conclusion is given.

3.2. Equivalent Circuit of Piezotransducer

Based on how energy is generated from the piezo material, the piezotransducer can be modelled as a current source I_p and the parasitic capacitor C_p. Besides the parasitic capacitor and current source, there is a parasitic resistor R_p for a more accurate circuit model. The equivalent circuit of the piezotransducer can be seen in Figure 3.1.

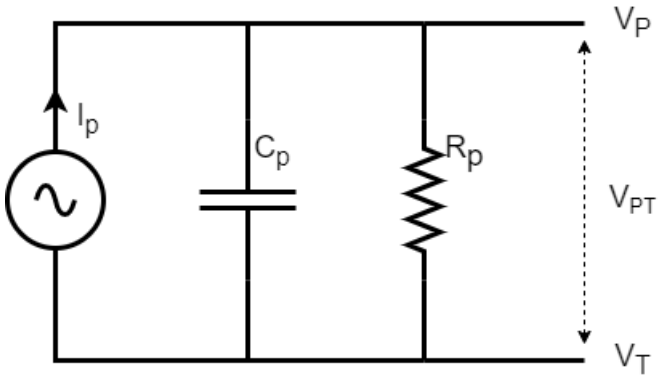


Figure 3.1: Equivalent circuit of a piezotransducer

3.3. Conjugate Matching Circuit

To maximally extract the energy from the piezotransducer, the conjugate matching circuit in Figure 3.2 is introduced. The source and load admittance can be expressed as $Y_s = j\omega C_p + \frac{1}{R_p}$, $Y_L = jZ_L + \frac{1}{R_L}$ respectively. For maximum output power, the imaginary part must cancel each other out. So a load resistor equals R_p, and an inductor equals $\frac{1}{\omega^2 C}$ is required. For a commercial piezotransducer, MIDE V22B, which has a parasitic capacitor of 9nF and the resonant frequency is tuned to 200Hz. This will require a 70.37H inductor. This value of the inductor is impractical for the integrated circuit.

Ideally, if such a conjugate matching circuit exists, the maximum power that can be extracted from the piezotransducer is only a function of parasitic resistor: $P_{out,max} = \frac{I^2 R_p}{8}$. And yet, it is not practical to have such a large inductor, and the load, in reality, cannot be purely resistive. The dominant source

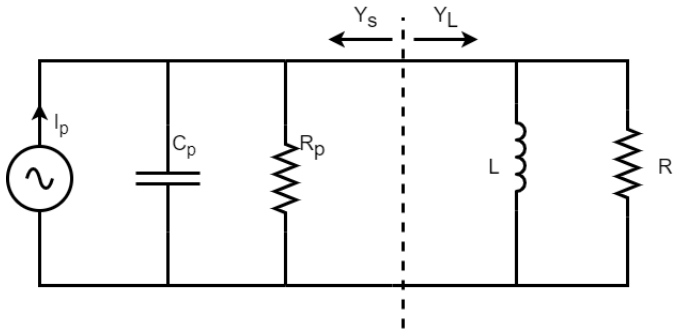


Figure 3.2: Conjugate matching circuit for the piezotransducer

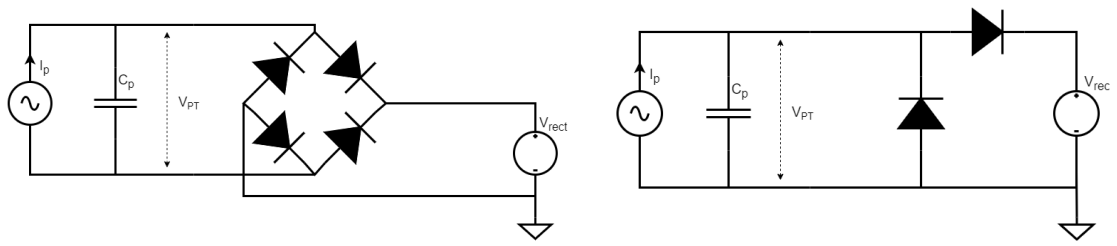
impedance is still the parasitic capacitor C_p. In fact, R_p only plays the role of a leakage resistor and the impact on the circuit is much smaller than that of the parasitic capacitor. Ignoring the R_p can still provide an accurate enough model.

3.4. Rectifying Circuit

Since the output of the piezotransducer is a random AC signal, a rectifying circuit is required to rectify the piezoelectric output to DC before further powering other devices.

3.4.1. Standard Rectifying Circuit

Two standard rectifying circuits for piezoelectric energy harvesting, Figures 3.3a and 3.3b, the full bridge rectifier (FBR) and voltage doubler (VD) are introduced. The diode voltage drop is marked as V_D.



(a) Full bridge rectifier **(b)** Voltage doubler

Figure 3.3: Schematic of the full bridge rectifier and voltage doubler

Output waveforms of two rectifiers are depicted in Figures 3.4a and 3.4b. To output the desired voltage level V_{rect}, the piezo current has to keep charging and discharging the parasitic capacitor in every cycle. The black areas represent wasted energy during this process.

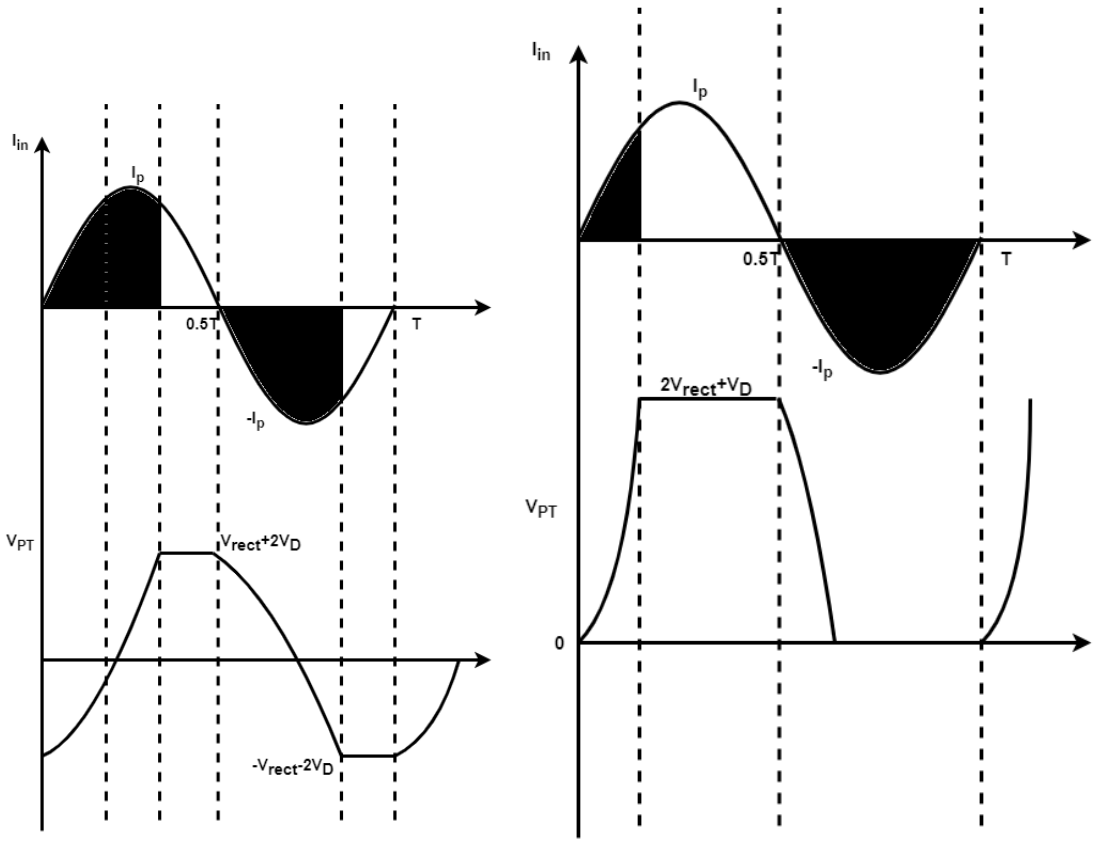
Several quantities are defined. Input current I_{in} is defined as $I_{in} = I_p \sin \omega_p t = I_p \sin 2\pi f_p t$, in which I_p is the peak current from the piezotransducer and f_p is the excitation frequency. The open-circuit voltage V_{oc} is $V_{oc} = \frac{I_p}{\omega C_p}$. The total charge produced by the piezotransducer in one cycle can be calculated below.

$$Q_p = 2\int_0^{T/2} I_p \sin \omega_p t \, dt = \frac{4I_p}{\omega_p} = 4C_p V_{oc} \tag{3.1}$$

Losses of FBR during the rectification can also be calculated, which is the charge wasted to charge and discharge the parasitic capacitor from $V_{rect} + 2V_D$ to $-(V_{rect} + 2V_D)$. This process happens two times in every cycle. The total charge delivered to the output is then derived.

$$Q_{loss,FBR} = 2C_p(V_{rect} + 2V_D - (-(V_{rect} + 2V_D))) = 4C_p(V_{rect} + 2V_D) \tag{3.2}$$

$$Q_{out,FBR} = 4C_p V_{oc} - 4C_p(V_{rect} + 2V_D) = 4C_p(V_{oc} - V_{rect} - 2V_D) \tag{3.3}$$



(a) Output of full bridge rectifier **(b)** Output of voltage doubler

Figure 3.4: Output waveforms of the full bridge rectifier and voltage doubler

The output power and maximum output power can be calculated below.

$$P_{out,FBR} = V_{rect}Q_{out,FBR}/T = 4f_pC_pV_{rect}(V_{oc} - V_{rect} - 2V_D) \tag{3.4}$$

$$P_{FBR,max} = C_pf_p(V_{oc} - 2V_D)^2, (V_{rect} = \frac{V_{oc} - 2V_D}{2}) \tag{3.5}$$

For the voltage doubler, since there is no path in the negative cycle for the current to flow through the output, the entire negative half cycle is wasted. Thus, the loss charge and output charge can be calculated.

$$Q_{loss,VD} = 2C_pV_{oc} + C_p(V_{rect} + V_D) \tag{3.6}$$

$$Q_{out,VD} = 2C_pV_{oc} - C_p(V_{rect} + V_D) = C_p(2V_{oc} - V_{rect} - V_D) \tag{3.7}$$

Maximum output power for voltage doubler can be calculated.

$$P_{VD,max} = C_pf_p(V_{oc} - V_D)^2, (V_{rect} = V_{oc} - \frac{V_D}{2}) \tag{3.8}$$

Both circuits will output the same power when the diode is ideal. Otherwise, the output power of the voltage doubler is slightly higher due to one rather than two diode drops. One critical drawback of the voltage doubler is that it does not convert any current in the negative cycle.

3.4.2. Maximum Power Point Tracking

It has shown that the maximum output power for both FBR and VD is not the situation when V_{rect} is the open circuit voltage. So a particular impedance has to be presented at the output of the rectifying

circuit. The previously introduced MPPT technique will decouple the load from the interface circuit and make sure the maximum power point is reached.

3.5. Figure of Merit

A very commonly used calculation for the Figure-of-Merit of the piezoelectric energy harvesting circuit is defined as the ratio between the output power of the proposed circuit and the power of the ideal full bridge rectifier ($V_D = 0$) as shown in Equation 3.9.

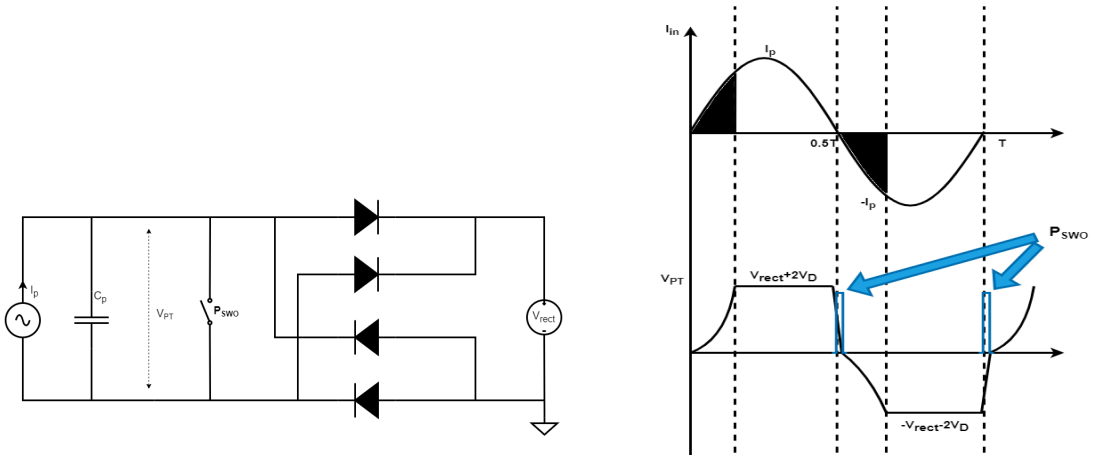
$$F.O.M = \frac{P_{out}}{P_{FBR,max}} = \frac{P_{out}}{C_p f_p V_{oc}^2} \tag{3.9}$$

3.6. Piezoelectric Energy Harvesting Techniques

To solve the problem of constantly charging and discharging the parasitic capacitor, several techniques have been proposed to help rebuild the voltage in C_p. The following sections will introduce these techniques. For simplification, the following sections will neglect diode voltage drop V_D.

3.6.1. Switch-Only Rectifier

The switch-only rectifier was first introduced. In the switch-only rectifier, the switch P_{SWO} will short C_p to the ground to discharge the voltage of C_p to zero when the piezo current changes direction; therefore, the piezo current only needs to do half the work. The schematic and output of the switch-only rectifier are shown in Figures 3.5a and 3.5b. The wasted charge is reduced compared to the FBR.



(a) Schematic of the switch-only rectifier

(b) Output of the switch-only rectifier

Figure 3.5: Schematic and output of the switch-only rectifier

The charge loss in one cycle and output power are calculated below. The output power when the diode is ideal is two times larger than the FBR output power. The maximum power point voltage is the open-circuit voltage.

$$Q_{loss,swo} = 2C_p V_{rect} \tag{3.10}$$

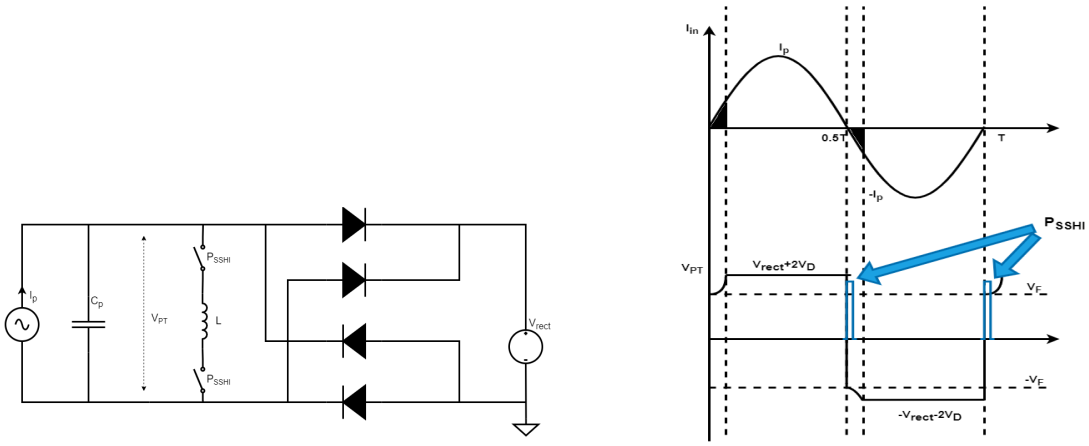
$$Q_{out,swo} = 4C_p V_{oc} - 2C_p V_{rect} = 2C_p(2V_{oc} - V_{rect}) \tag{3.11}$$

$$P_{out,swo} = 2f_p V_{rect} C_p (2V_{oc} - V_{rect}) \tag{3.12}$$

$$P_{swo,max} = 2C_p f_p V_{oc}^2, (V_{rect} = V_{oc}) \tag{3.13}$$

3.6.2. Synchronous Switching Harvesting on Inductor (SSHI)

To further reduce the charge loss, SSHI is introduced. In the SSHI circuit, an inductor is utilized to help further flip the voltage since an inductor can passively change the polarity of the voltage. Two switches will be closed at the zero-crossing point and opened when the current through the inductor drops to zero. The schematic and output of SSHI are shown in Figures 3.6a and 3.6b.



(a) Schematic of the SSHI **(b)** Output of the SSHI

Figure 3.6: Schematic and output the of SSHI

V_F is the voltage level of C_p after flipping. The flipping efficiency reflects how much voltage is rebuilt after flipping. For SSHI, it is defined by equation 3.14 [10]. R in the equation includes the parasitic and series resistor of the inductor, the ON resistor of the switch, etc. A large inductor is required for a high flipping efficiency.

$$\eta_{SSHI} = \frac{V_F}{V_{rect}} = e^{-\frac{\pi}{\sqrt{\frac{4L}{R^2 C_p}-1}}} \tag{3.14}$$

The transferred charge and output power are calculated below.

$$Q_{loss,sshi} = 2C_p(V_{rect} - V_F) = 2C_p V_{rect}(1 - \eta_{SSHI}) \tag{3.15}$$

$$Q_{out,sshi} = 4C_p V_{oc} - 2C_p V_{rect}(1 - \eta_{SSHI}) = 2C_p(2V_{oc} - (1 - \eta_{SSHI})V_{rect}) \tag{3.16}$$

$$P_{out,sshi} = 2f_p V_{rect} C_p(2V_{oc} - (1 - \eta_{SSHI})V_{rect}) \tag{3.17}$$

$$P_{sshi,max} = \frac{2C_p f_p V_{oc}^2}{1 - \eta_{SSHI}}, (V_{rect} = \frac{V_{oc}}{1 - \eta_{SSHI}}) \tag{3.18}$$

3.6.3. Synchronous Switching Harvesting on Capacitor (SSHC)

The SSHC, Figure 3.7, is introduced after SSHI. The SSHC technique utilizes N stages of flying capacitors to replace the inductor in SSHI. The output of the SSHC circuit is generally the same as the one of SSHI, despite there being lots of steps within the flipping.

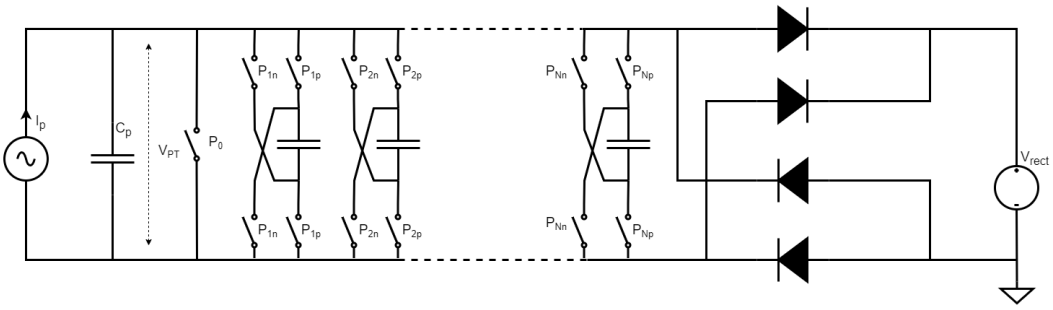


Figure 3.7: Schematic of the SSHC

The detailed flipping process is visualized in Figure 3.8. Take the flipping from positive to negative as an example. The SSHC circuit operates as follows. First, at the zero crossing point of piezo current,

the positive switches $P_{1p} - P_{Np}$ are connected and disconnected in sequence. The charge in the C_p is redistributed in every flying capacitor. Second, P_0 is closed to discharge the remaining charge in C_p to the ground. Third, the negative switches $P_{Nn} - P_{1n}$ are connected and disconnected in sequence to flip the voltage in C_p.

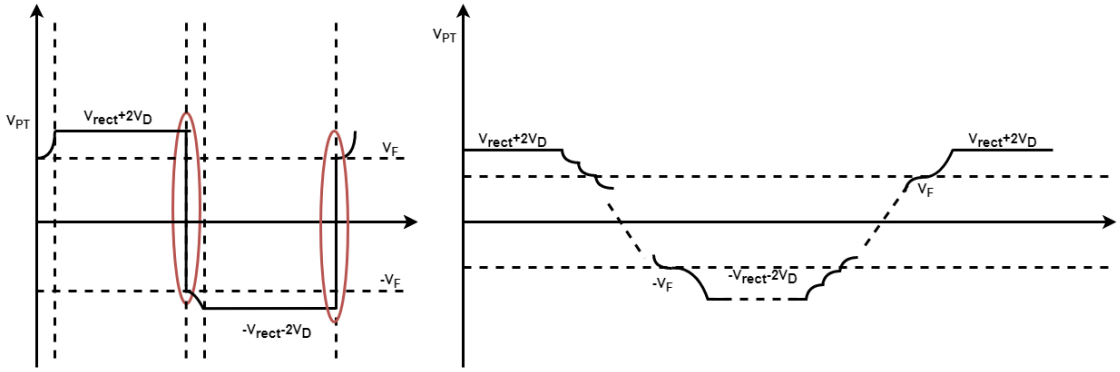


Figure 3.8: Detail of the flipping process of the SSHC

Split-phase SSHC

To further improve the flipping efficiency, more improvements can be made to increase the charge stored on each flying capacitor. Split-phase SSHC (SP-SSHC) is proposed by [3]. The working principle is using multiple connections of flying capacitors to achieve the highest voltage in each capacitor. Thus, higher flipping efficiency can be reached.

Flying Capacitor Size Selection

The flipping efficiency of SSHC is affected by the ratio between a single fly capacitor and the parasitic capacitor. [57] introduced the optimization of flipping efficiency by increasing the flying capacitor. Table 3.1 summarizes the flipping efficiency of SSHC and SP-SSHC from simulation, in which n is the number of stages and N is the total number of phases of SP-SSHC which can be calculated by $N_{max} = 1 + 2 \times \sum_{i=1}^{n} C_n^{n+1-i}$, N must be odd and $N \geq 3$.

Table 3.1: Flipping efficiency of the SSHC

Rectifier Type	Flipping efficiency
SSHC ($C_f = C_p$)	$\frac{n}{n+2}$
SSHC ($C_f = 100C_p$)	$\frac{n}{n+1}$
SP-SSHC ($C_{f,total}/C_p = x$)	$[\frac{(1+x)^2}{x} \prod_{i=1}^{\frac{N-3}{2}} \frac{(1+\frac{x}{(i+1)^2})^2}{(1+\frac{x}{i(i+1)})^2} - \frac{4x}{(N-1)^2}]^{-1}$ [3]

3.6.4. Inductive and Capacitive Flipping Techniques Comparison

In Sections 3.6.2 and 3.6.3, it was shown that SSHI and SSHC circuits have a similar working principle. Studying which of them is more suitable for wearable applications is necessary. For different flipping efficiency, the required inductor of SSHI for parasitic capacitors from 0.1nF to 100nF, the required number of stages for SSHC based on the ratio between the flying capacitor and the parasitic capacitor, and the required number of stages for SP-SSHC assuming $C_{f,total}/C_p = 400$ are calculated

Based on Figure 3.9, whenever the parasitic capacitor exceeds 10nF, an mH range inductor is required for flipping efficiency exceeding 80%, which is not going to be integratable. Figure 3.10 compares the size of the components for the SSHI circuit with a 100pF parasitic capacitor and a range of parasitic capacitors for the (SP)SSHC circuit by statistics on distributors. It is found that for the capacitors from the same manufacturers, 1nF and 10uF have the same area.

These data show that SSHC circuits have a wider range of adaptation for parasitic capacitance and that SP-SSHC takes the least area while achieving the highest flipping efficiency.

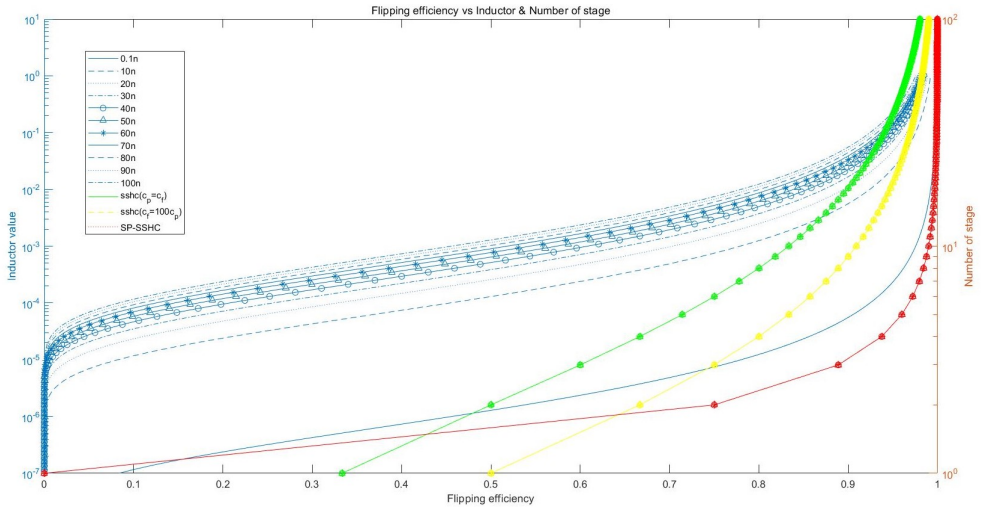


Figure 3.9: Inductor value and number of stages for the same flipping efficiency

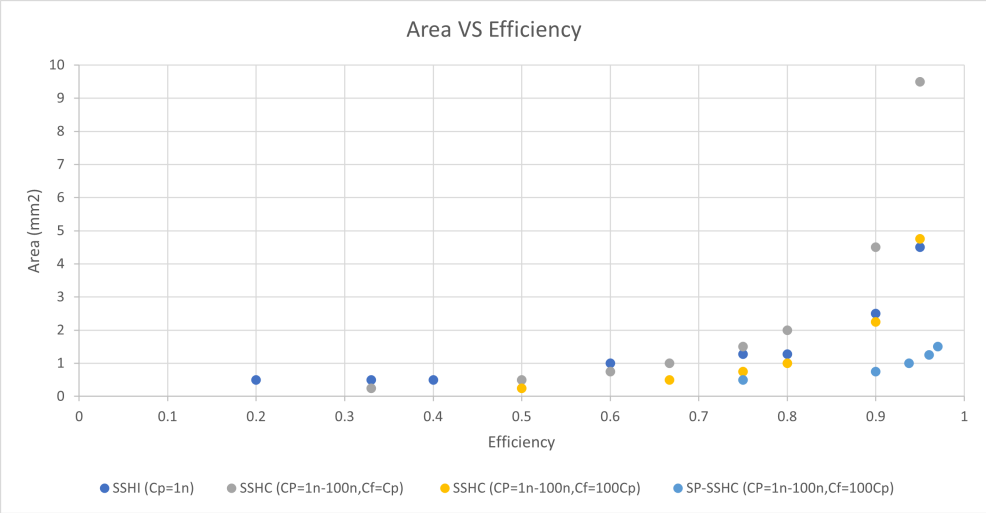


Figure 3.10: Area comparison between the SSHI, SSHI and SP-SSHC

3.6.5. Other Types of Synchronous Switching Harvesting Circuit

Other types of synchronous switching harvesting techniques are introduced in the following sections.

Synchronized Switch Harvesting on Inductor Magnetic Rectifier (MR-SSHI)

Synchronized Switch Harvesting on Inductor Magnetic Rectifier (MR-SSHI) increases the power extraction from the piezotransducer using the transformer. The schematic is shown in Figure 3.11. Switches of two inductors close at the zero crossing point from positive to negative and reverse, respectively. The transformer will amplify the voltage seen by the full bridge rectifier, so effectively, the voltage drop of FBR is reduced.

Hybrid Synchronized Switch Harvesting on Inductor(Hybrid-SSHI)

The Hybrid-SSHI combines the SSHI and MR-SSHI circuits (Figure 3.12). Hybrid-SSHI does not improve the conversion efficiency but allows a widening of the load bandwidth [7]. The switch operation is similar to the one of MR-SSHI. The extra diode compared to MR-SSHI is used to The Hybrid-SSHI will switch between MR-SSHI and SSHI based on the voltage level of the piezotransducer.

3.6.6. (Phase Shift) Synchronous Electric Charge Extraction ((PS-)SECE)

The Synchronous Electric Charge Extraction (SECE) technique (Figure 3.13) is less sensitive to changes in the load. The switch P_{SECE} only closes at the zero-crossing point of the piezotransducer current.

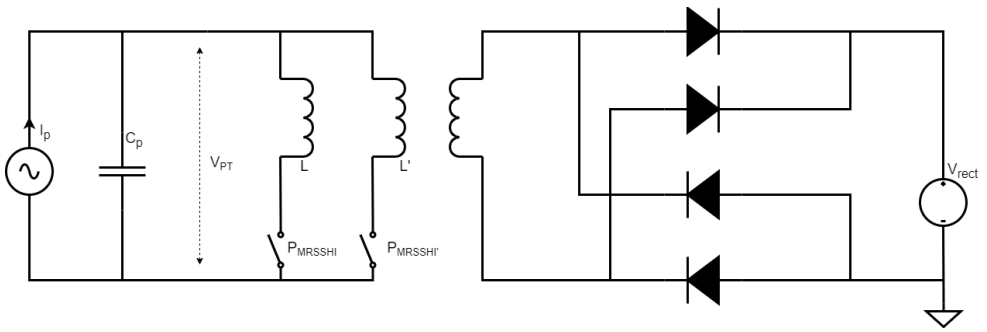


Figure 3.11: Schematic of the MRSSHI

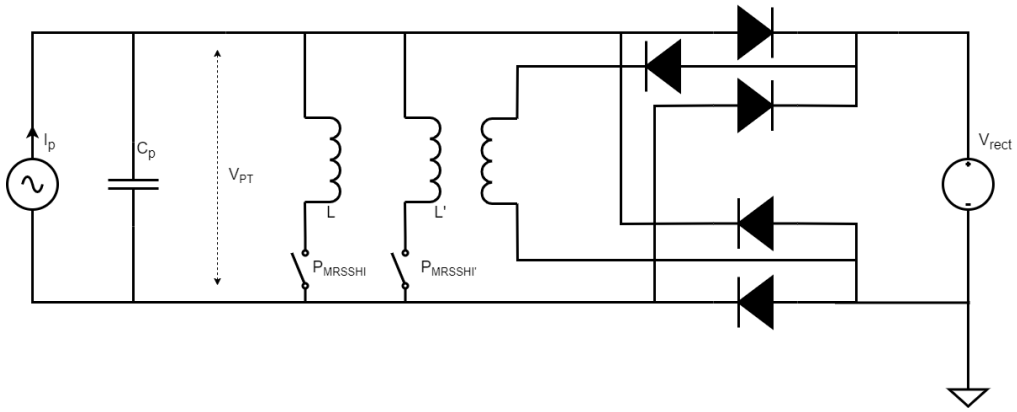


Figure 3.12: Schematic of the HSSHI

Since the switch isolates the load from the interface circuit most of the time, the impedance seen by the piezoelectric element is almost constant. One of the downsides of the SECE is that it is hard to achieve a trade-off regulation between power extraction and the electromechanical damping effect caused by the direct connection of the inductive element in the interface circuit with the piezotransducer.

To overcome the previous issue, PS-SECE is introduced. The idea is to introduce a phase shift in the switching signal so that the electromechanical damping effect can be controlled by the phase shift. The schematic is the same as SECE (Figure 3.13).

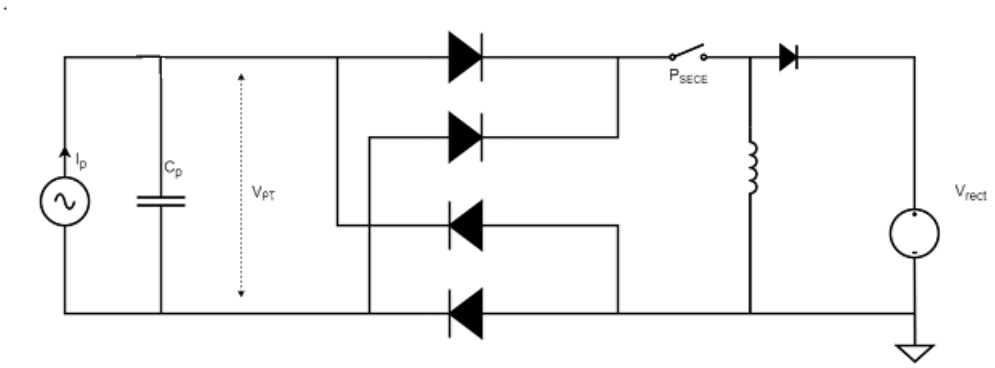


Figure 3.13: Schematic of the SECE and PS-SECE

3.6.7. Double, Enhanced, Adaptive Synchronized Switch Harvesting

Double Synchronized Switch Harvesting (DSSH) is a combination of SSHI and SECE techniques (Figure 3.14). The switch S1 will first charge the inductor L_1 and intermediate capacitor C_{int} at the zero crossing point. Then S1 will open and S2 will charge the inductor L_2. L_2 will transfer the energy to the load eventually. One advantage of the DSSH is the trade-off between damping effects and harvested energy can be controlled by finely tuning the value of the ratio between the parasitic capacitor and intermediate capacitor [7].

Enhanced Synchronized Switch Harvesting (ESSH) is introduced to ease the mismatch between C_{int}/C_p. The difference between ESSH and DSSH is that the intermediate capacitor C_{int} always stores a small amount of energy instead of completely being discharged like DSSH [7]. S2 will control the energy in C_{int} damping between a preset range. The control signal of S1 is the same as DSSH.

Adaptive Synchronized Switch Harvesting (ASSH) is an optimization of the ESSH technique particularly designed for multi-mode vibrations [7]. S1 closes multiple times in one period instead of two times in ESSH. For one-frequency excitation, it has the same control law as the one of the ESSH.

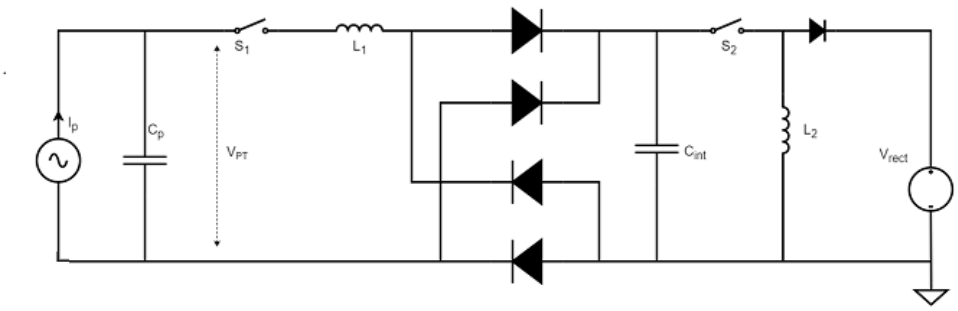


Figure 3.14: Schematic of the DSSH, ESSH and ASSH

3.7. Cold Start Capability

One important aspect of energy harvesting is the cold start. Since FBR and VD can be completely passive, they will not have any issues with the cold start. The rest of the techniques require active circuits to do the harvesting, so the cold start for them could be a problem. A typical cold-start solution for these circuits is that they will start with a passive FBR to reach a certain voltage level. Until then, the active circuit will start up to increase the power extraction. Another aspect of cold start from a piezo element is that it will not encounter the problem that can occur with a DC input, which is that the system needs to start from a low voltage level. The open circuit voltage of a piezoelectric element is usually high.

3.8. Conclusion on Piezoelectric Energy Harvesting Techniques

Several criteria to be considered for discussing which technique is the most suitable for this project are:

- Cold-start capability: The technique needs to be capable of cold-starting from an energy depletion state. Otherwise, it does not match the requirement of battery-less.
- Power extraction: The technique needs to extract as much power as possible from the piezo-transducer.
- Load dependency: The technique can output maximum power with load changing.
- Area: The technique is scaleable to the integrated circuit.

Among these criteria, the load dependency is not that important compared to the others because, typically, an MPPT and a power converter are required after the rectifying circuit, and the input impedance and output impedance are decoupled. The following Table 3.2 compares the techniques above.

Table 3.2: Comparison of harvesting techniques

Rectifier Type	Power extraction	Area	Cold-start	Load dependency
FBR,VD	Lowest	Smallest	Passive	Dependent
SSHI	Highest	Medium	2-stage start-up	Dependent
SSHC	Highest	Small	2-stage start-up	Dependent
MR-SSHI,H-SSHI	Medium	largest	2-stage start-up	Dependent
SECE, PS-SECE	Medium	Large	2-stage start-up	Independent
DSSH, ESSH, ASSH	High	Large	2-stage start-up	Independent

The fundamental limitation of the piezotransducer is the process of keeping charging and discharging the parasitic capacitor. To extract maximum power from the piezotransducer, the influence of the parasitic capacitor has to be eliminated.

FBR and VD will not be further considered because they are not capable of extracting enough power from the piezotransducer.

The use of a transformer will consume too much area, and plus, the MR-SSHI and H-SSHI circuits did not show a power extraction better than the SSHI circuit [15]. They will not be considered either.

SECE and PS-SECE techniques focus on load dependency. They can be regarded as buck converters with a very low-duty cycle connected after the full bridge rectifier. The fundamental limitation of the piezotransducer is not addressed. These techniques consume a large amount of area due to the presence of inductors. So they will not be used.

DSSH, ESSH and ASSH implement SSHI on the SECE technique, so they extract more power than SECE while not sensitive to the load. They are not the best choice either, as using two inductors is even more undesirable than one.

So far, SSHI and SSHC can provide the highest output power among all techniques since these techniques solve the fundamental limitation of the piezotransducer. SSHI consumes lots of area because of the use of inductors. The SSHC, especially SP-SSHC, can provide the highest output power while minimising the area. The load dependency can be solved by the MPPT as well.

The conclusion is that the cold start-up of an SP-SSHC would be an interesting direction for further design.

4

Cold Start of Piezoelectric Energy Harvester

4.1. Introduction

This chapter will discuss how the structure of a cold-start circuit for a piezoelectric energy harvester (PEH) is constructed. Sub-blocks in the cold-start system will be discussed. Finally, the top-level design and the estimated start-up procedure will be concluded.

4.2. Cold Start of Piezoelectric Energy Harvester

Both the current and voltage output of a PEH have zero mean values, which means no net charge is conveyed to the output. So, a rectifier is necessary for PEH.

The block diagram of a typical self-powered piezoelectric energy-harvesting circuit, adapted from [7], and voltages after each phase are shown in Figure 4.1. The sub-blocks include a rectifier to rectify the current and the voltage, harvesting techniques integrated with the rectifier to extract charge or to isolate the load, such as SSHC, SECE, etc., an MPPT block that controls the input impedance of a DC-DC converter to guarantee impedance matching if the load is not isolated, a storage element and a voltage regulator to provide a stable supply voltage if necessary. In general, the aim of piezoelectric energy harvesting mainly focuses on the following two aspects, and multiple techniques discussed in Chapter 3 are proposed to meet these two requirements.

- Extract as much energy as possible from the PEH since a considerable amount of energy is wasted to charge and discharge the parasitic capacitor.
- Adjust the load impedance such that the load impedance can match or be isolated from the source impedance.

However, the target is not quite the same in the case of a cold-start for PEH. The primary target of the cold-start circuit is to charge the storage capacitor to a certain voltage level such that there is a high enough supply voltage for the main harvester to operate properly. To reach this specific voltage, techniques to extract the required amount of energy are necessary. However, whether or not impedance matching is satisfied is less important. Reasons for abandoning the MPPT in the cold start are:

- The MPPT circuit requires a high enough supply voltage, which first needs to be generated from another circuit: a cold-start circuit.
- The current main harvester already includes an MPPT circuit. Building one MPPT circuit specifically for the cold-start circuit will overlap with the function of the main harvester and waste unnecessary power consumption and circuit area.
- The function of the MPPT is to change the load impedance, thus, the output voltage. For cold-start applications, the function might cause the failure of cold-start if the output voltage set by the MPPT is smaller than the desired voltage. The same thing will happen for a circuit without the

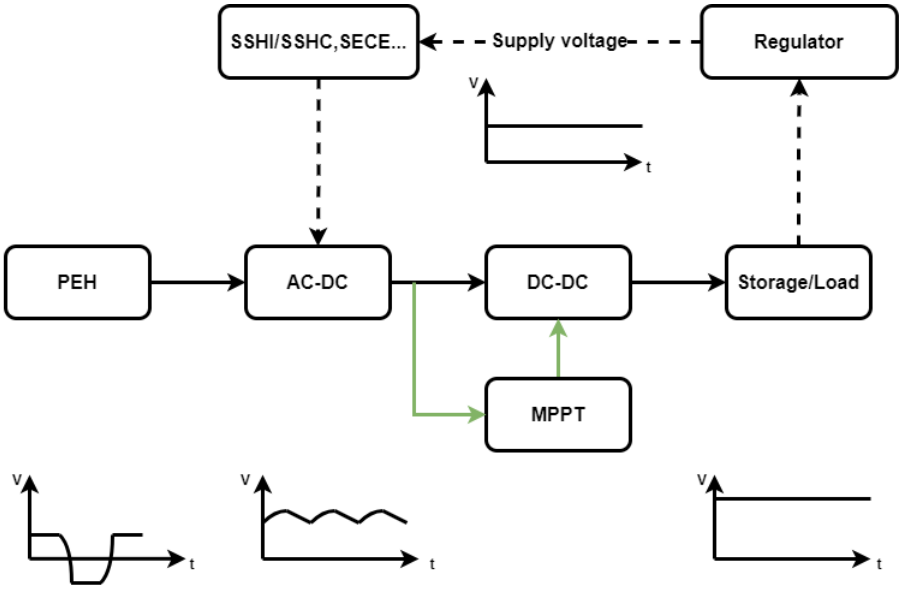
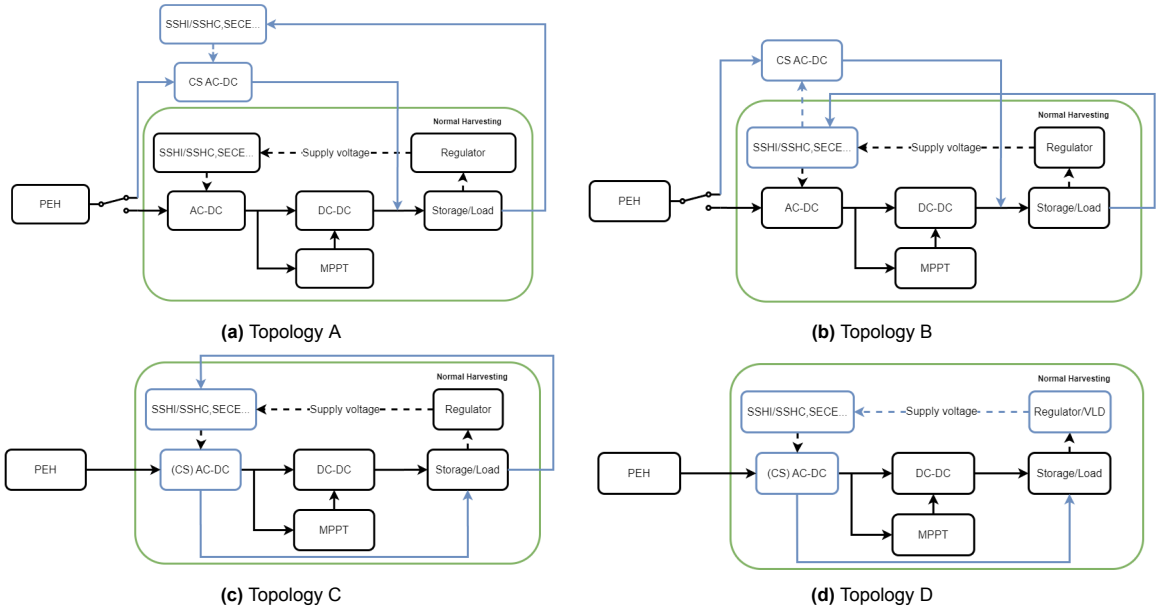


Figure 4.1: Block diagram of a PEH in normal harvesting

MPPT if the load impedance is too small to reach the desired voltage. In the end, there is always a chance that the cold-start circuit cannot reach the desired voltage with or without the presence of MPPT.

Several possible topologies in Figure 4.2 are proposed for the cold-start application. The main arguments in these topology options are the following three points:



(a) Topology A

(b) Topology B

(c) Topology C

(d) Topology D

Figure 4.2: Possible topologies

- The cold-start circuit can share parts of the same circuit with the main harvester. This integration will make the cold-start circuit more area-efficient. However, this will require a more careful and complex controller to ensure the components in the cold-start circuit will not overlap with the main harvester during normal operation.
- A voltage regulator is used in [8],[10] to provide a supply voltage for other blocks. Whether a voltage regulator is required in a cold-start circuit is worth discussing. A voltage regulator will

ensure the circuit works with a cleaner supply voltage at the cost of area and system complexity. Abandoning a voltage regulator requires the circuit to be adaptive to a wide range of supply voltages and ripples; the circuit also may not work efficiently while the voltage changes. However, it is good for the area and simplifies the design.

- A voltage-level detector can lock the output of active circuits to a well-defined state as long as the voltage level is insufficient. However, this will increase an additional block in the cold-start circuit and the lowest voltage to turn on the active circuit is limited by the threshold voltage of the voltage-level detector. Discarding the voltage-level detector will introduce potential risks that the outputs of the active circuits are left floating or uncontrolled when the supply voltage is low. This might stop the cold-start process if any node is shorted to the ground during this unclear state. The benefit is that the active circuit is naturally integrated into the cold-start circuit without a 'cold-start' process in the cold-start circuit.

4.2.1. Discussion on Topology

Four topologies are proposed for the cold-start application. The common part among these topologies is the MPPT, and the DC-DC converter blocks are bypassed during cold start.

Topologies A, B, and C all bypass the voltage regulator and voltage-level detector, so the cold-start circuit should be designed to work across a wide range of supply voltages. It is also possible to put a voltage regulator or voltage-level detector for the Topologies A, B and C.

Topology A uses a completely separate cold-start circuit. It includes the flying capacitors in the SSHC technique. A controller will switch the cold-start circuit to the main harvester after the cold-start completes. The advantage of topology A is the controller is the simplest. Only one voltage-level detector is required to disconnect the cold-start circuit. The disadvantage is it consumes more area.

Topology B uses a separate AC-DC converter. The components in the SSHC technique are shared with the main harvester. For example, it is discussed in Chapter 3 that the flying capacitor should be much bigger than the parasitic capacitor for optimal flipping efficiency. This is also required for the main harvester designed in [49], so the cold-start circuit can at least share the same flying capacitors with the main harvester. The controller is the same as the one of topology A. The components not designed for normal operation in the cold-start circuit need to be disconnected after the cold-start.

Topology C makes the main harvester also cold-start capable. This topology will require the cold-start circuit to have the same performance as the original main harvester when in normal operation. In addition, the controller for this topology needs to be carefully designed as it may encounter issues when the circuit switches to normal harvesting, where the MPPT and DC-DC converter will join the operation flow and the power supply of all blocks will be switched to the output of the voltage regulator in some cases.

Topology D implements the voltage regulator or the voltage-level detector during the cold start to solve the potential risk of Topology C. The regulator and the voltage-level detector provide a stable supply voltage and a well-defined initial state. After the cold-start, the system will only enable the MPPT and DC-DC converter. The controller design will be similar to the one in Topology C.

4.2.2. Conclusions on Topology

Among these topologies, Topology A seems to make the system too redundant. It can be easily modified to topology B by using the same group of flying capacitors. Other possible blocks to be shared are yet to be studied.

Since the current AC-DC converter and SSHC technique in [49] is controlled by an external clock signal, working during a cold start is impossible. Topology C will require a complete redesign of the main harvester while the performance of the redesigned system is hard to be competitive with the original design, although this topology does not increase extra area.

Topology D will have the same drawbacks as Topology C. And in addition, the minimum startup voltage is limited by the voltage regulator or the voltage-level detector because both two circuits require a minimum supply voltage to function properly. Voltage regulators and voltage-level detectors also add to this topology's power consumption and design complexity.

So far, Topology B does not have significant drawbacks. The rectifier and part of the SSHC technique will be specifically designed for the cold start so that the circuit can work across a wide range of supply voltages. This structure offers a good balance between cold-start capability and area savings. The controller in topology B is relatively simple, and the performance of the main harvester is not

affected after the cold start. The voltage-level detector and voltage regulator will not be used, as the intention is to make the SSHC technique naturally built into the cold-start circuit.

4.3. Rectification

A rectifier is mandatory to rectify the current from AC to DC. Several CMOS rectifiers will be discussed in this section. In the following schematics of different rectifiers, the green parts represent the path in the positive cycle, and the blue parts are the path in the negative cycle.

To evaluate the performance of a rectifier, the most important feature is the voltage drop of the rectifier; the lower the voltage drop, the higher the rectification efficiency. Another feature of a rectifier is the frequency response. However, the target operating frequency of the rectifier in this design is at low frequencies, where the rectifier's parasitic capacitors will not cause problems, so the frequency response of the rectifier is of no interest.

4.3.1. Diode-Connected Full-Bridge Rectifier

The simplest solution in CMOS technology is using the diode-connected transistors, as shown in Figure 4.3. As suggested by its name, the diode-connected rectifier comprises four diode-connected transistors. The voltage drop of a diode-connected full-bridge rectifier is the voltage across the two NMOS diodes, which is approximately two threshold voltages, depending on the current flowing through the diodes and the operation regions of the transistors.

Some advantages stand out for this type of rectifier. Firstly, it is completely passive, making it a suitable choice for cold-start applications. Secondly, the structure of such a rectifier is simple, improving its robustness and making it a reliable component in various environments. Additionally, the area of such a rectifier is efficient since the voltage drop of a diode-connected transistor is almost independent of the size of the transistor.

The disadvantage of such a rectifier is caused by the voltage drop of two diodes. Firstly, the open-circuit voltage from the PEH has to be at least higher than the voltage drops of two diodes to turn on the rectifier, thereby limiting the minimum input power level. Secondly, as indicated by Equation 3.4, the voltage drop of the rectifier reduces the output power from the PEH. The loss can be split into loss due to output voltage and loss due to voltage drop across the rectifier. The system requirement sets the output voltage, whose loss is inevitable and unchangeable. In contrast, the loss due to the rectifier voltage drop is unwanted and is more dominant than the loss caused by the output voltage when the output voltage is still low.

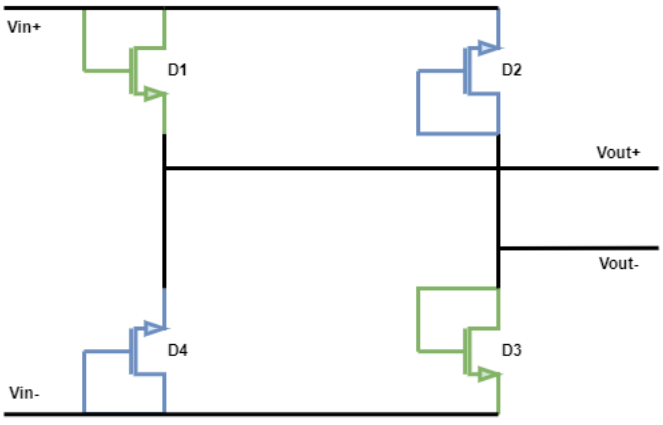
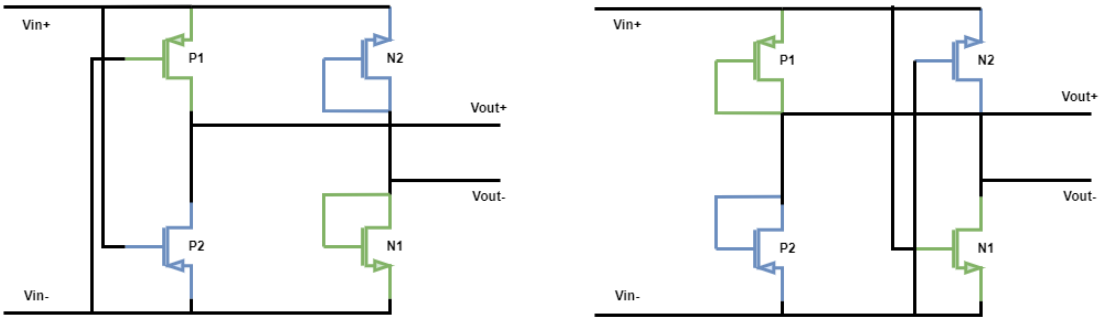


Figure 4.3: Diode-connected full-bridge Rectifier

4.3.2. Diode-connected Transistor and Cross-coupled Transistor Rectifier

In this topology, four diode-connected transistors are replaced by two diode-connected transistors and two cross-coupled transistors. The cross-coupled transistors in this rectifier act as switches during their conduction cycles.

The advantages of this type of rectifier include, firstly, the rectifier is still passive, which is a suitable option for the cold-start application. Secondly, the voltage drop is reduced to one diode voltage drop



(a) NMOS diode-connected and PMOS cross-coupled rectifier **(b)** PMOS diode-connected and NMOS cross-coupled rectifier

Figure 4.4: Diode-connected and cross-coupled rectifier

and the voltage drop of a switch. Compared to the diode-connected rectifier, the voltage to turn on the rectifier is halved, and the cross-coupled transistors will switch automatically as the diode-connected transistor conducts.

The disadvantage is still mainly the voltage drop. Although it is half the loss of a diode-connected rectifier, the loss of a threshold voltage is still not preferred. Another disadvantage is the area of the cross-coupled rectifier. Since part of the voltage drop is contributed by the on-resistance, these transistors will require more area to reduce the voltage drop.

4.3.3. Fully Cross-coupled Rectifier

Further improving the rectifier, Figure 4.5 shows the structure of a fully cross-coupled rectifier. A fully cross-coupled rectifier is a self-controlled and passive rectifier. The main advantage is that the voltage drop of this type of rectifier is only caused by the on-resistance of one NMOS and one PMOS switch.

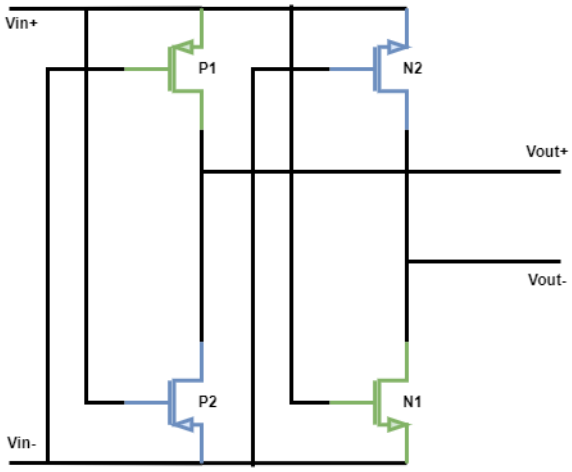


Figure 4.5: Fully cross-coupled rectifier

4.3.4. Active Rectifier

The active rectifier in Figure 4.6 uses active diodes as controlled switches to rectify the current. The active diode is implemented by a comparator and a switch. The working principle of an active diode is that the comparator will detect the direction of the current. When the current direction is positive, the comparator will close the switch and vice versa.

Several variants are proposed based on the use of active diodes, such as rectifiers using diode-connected transistors with active diodes, rectifiers using cross-coupled transistors with active diodes, and rectifiers using four active diodes. The active rectifier using four active diodes has the highest rectifying efficiency among these variants but is the most complex to design and consumes the most power.

The advantage of the active rectifier is that it provides the highest rectifying efficiency. The disadvantages are mainly caused by the area and power consumption of the comparator. Since comparators require a stable power supply, the cold-start capability is also questionable for the active rectifiers.

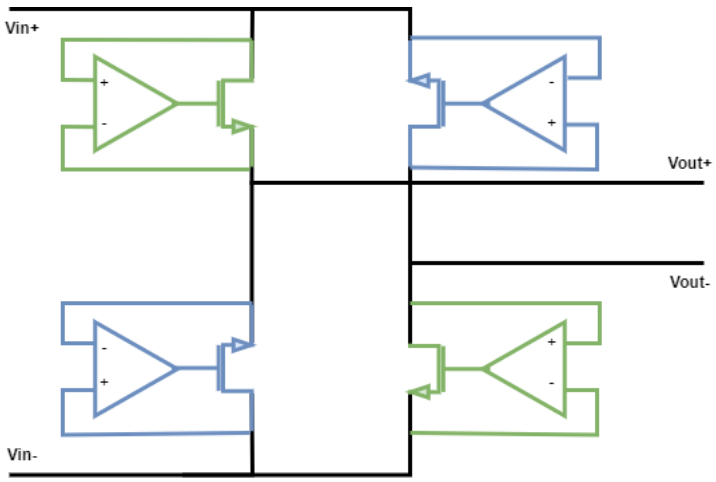


Figure 4.6: Schematic of active rectifier with four active diodes

4.3.5. Discussion on Rectifier

For cold-start applications, one of the most important features of the rectifier is whether the rectifier can work without a supply voltage. In addition, a low voltage drop is another preferred feature for piezoelectric energy harvesting, but it is less important for cold-start purposes.

The active rectifiers do not meet the requirements of working without a supply voltage. Although there is an option that the storage capacitor can firstly be charged using the body diode of the switch before the active diode turns on, this essentially turns the rectifier into a diode-connected rectifier. The barrier of two body-diode threshold voltages will limit the lowest input power, as in the case of a diode-connected rectifier.

The diode-connected full-bridge rectifier and cross-coupled rectifier are all passive rectifiers, making them a good option for the cold-start application. The voltage drops of these rectifiers are caused by diode voltage drops and the cross-coupled transistors' on-resistance. For a fully cross-coupled rectifier, the voltage drops are only caused by two cross-coupled transistor pairs. Theoretically, this will be the same as the voltage drop of the active rectifier.

As promising as the fully cross-coupled rectifier may sound, there is still one critical issue with the fully cross-coupled rectifier: its reverse current.

Figure 4.7 is the piezo-current, the voltage across the parasitic capacitor from a zero-voltage-drop rectifier and the output of the comparators in an active rectifier; Vin+ and Vin- are the top and bottom plate voltages of the parasitic capacitor, respectively. The gate of all switches in an active rectifier is controlled by a well-defined signal from the comparator, and it is either supply voltage or the ground, and thus the switch is either opened or closed.

In the case of a fully cross-coupled rectifier, assume the voltage across the parasitic capacitor is still the same as the active rectifier as Figure 4.7, then the gate and source voltage of every transistor is controlled by the voltage of the top plate and bottom plate of the parasitic capacitor. When the PEH delivers power, the gate voltage is the same as the one of the active rectifier. However, when the current starts discharging the parasitic capacitor, the voltage on the parasitic capacitor starts falling. For the active rectifier, the switch is completely opened by the comparator. For the cross-coupled rectifier, however, the switch is gradually being opened, and the switch is still conducting in this period which causes the charge in the storage capacitor to flow back into the plate of the parasitic capacitor that is being discharged. This reverse current will greatly decrease the amount of charge delivered to the storage capacitor.

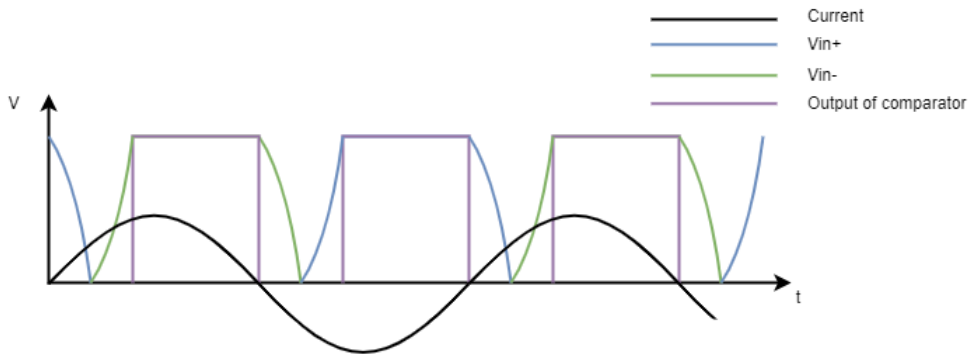


Figure 4.7: Voltage information from a zero-voltage-drop rectifier

4.4. Two-Stage Rectification.

There is a solution to this issue. Paper [27] introduces the two-stage rectification solution by adding one more active diode after a fully cross-coupled rectifier to stop the reverse current, as shown in Figure 4.8. The active diode is partly cold-start capable because the body diode in the switch can be used for conducting when the storage capacitor is completely empty. This topology ensures both the cold-start capability and high rectifying efficiency, although the power consumption and design complexity slightly increase.

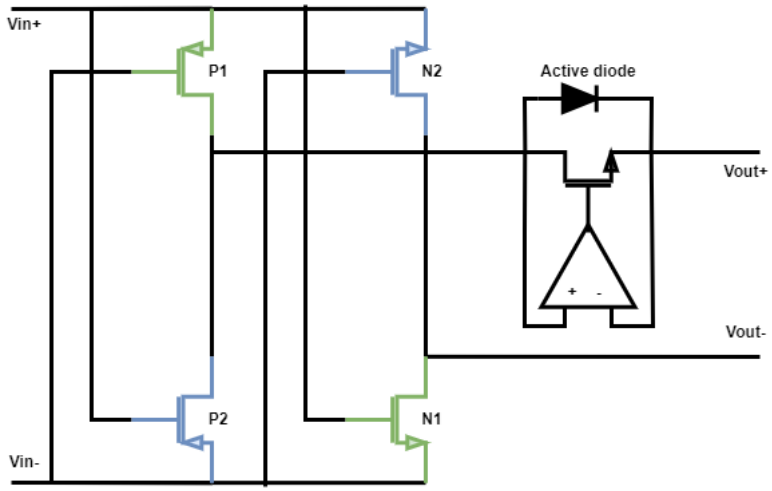


Figure 4.8: Two-stage rectifier

The working principle is the same with the cross-coupled rectifier. The green transistor rectifies the positive current, and the blue transistors rectify the negative current. The active diode will conduct whichever path the cross-coupled rectifier is conducting and open the switch when the current starts discharging the parasitic capacitor until the voltage on the parasitic capacitor is high enough to deliver power again.

4.5. SSHC Technique

To further extract charge from the PEHs, the previously introduced SSHC technique in Section 3.6.3 will be implemented because of its area efficiency and compatibility with CMOS technology.

The SSHC technique requires two pieces of information from the PEHs: the moment the current crosses zero and the direction of the current. The former information enables the flipping process, and the latter controls the direction of the flipping.

4.5.1. Zero Crossing Detection

When the current crosses zero, the parasitic capacitor will be discharged. The SSHC will start flipping the voltage on the parasitic capacitor. The characteristic of an active diode can be used to generate the zero-crossing signal. Figure 4.9 shows the relation between the current and the output of the active diode, in which Vcp and Vout are the positive and negative inputs of the comparator.

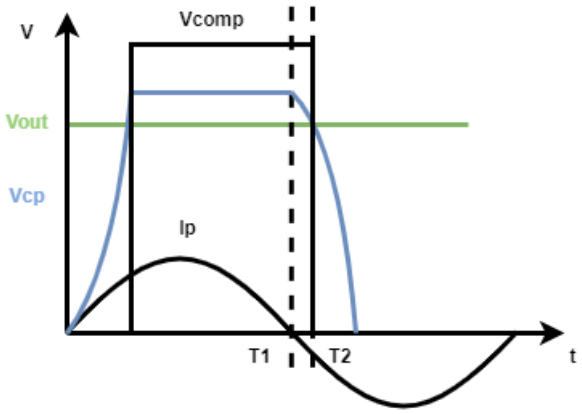


Figure 4.9: Voltage of comparator output, output voltage and piezo current

Ideally, the flipping process should happen at T1. In the actual operation, the comparator will open the switch when the voltage of the parasitic capacitor is discharged to the same voltage as the output voltage at T2. The period between T1 and T2 depends on the voltage drop of the rectifier. For an active diode, T1 and T2 can be approximately equal as the voltage drop of an active diode is very small. Therefore, the falling edge of the comparator output can be used to generate a zero-crossing signal.

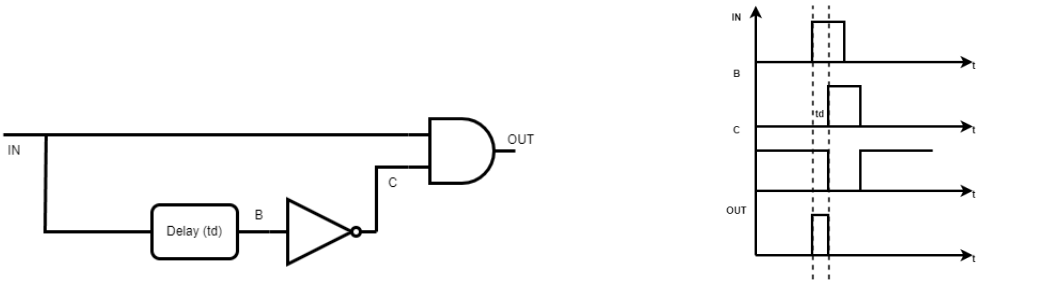
4.5.2. Direction Detection

The other piece of information required is the direction of the current. The flipping process starts after the falling edge of the active diode. By reading the waveform in Figure 4.7, the idea is that the direction information can be achieved by comparing the top and bottom plate voltages of the parasitic capacitor at the zero-crossing points. Also, the voltage difference between the top and bottom plates at this point is the largest in the entire operation cycle. One approach is to use a discrete-time comparator and clock the comparator with the output from the zero-crossing detector; this combination should generate a correct signal for direction. The advantages of using this detection mechanism are, firstly, the discrete-time comparator operates only for a short time, and the discrete-time comparator can be designed to consume no static power, only dynamic power. So, the power consumption of this comparator is very small. Secondly, the requirements of the discrete-time comparator are less stringent due to the large voltage difference between the plates of the parasitic capacitor. Fewer efforts are required to design this comparator.

4.5.3. Pulse Generation

There are no external clock signals and digital circuits to generate digitized pulses for the SSHC circuit in the cold-start scenario; the pulses have to be generated in an analogue way. Also, since the pulse generation is only used for cold-start purposes, the pulse width can be more flexible, and this block should be optimized to be simple and area-efficient.

A conventional pulse generation circuit can be used to generate a series of pulses for the SSHC circuit. Figure 4.10 shows the structure of a pulse generation circuit and its timing diagram. In general, a pulse generation circuit is a combination of logic gates. The pulse width is determined by the delay cell.



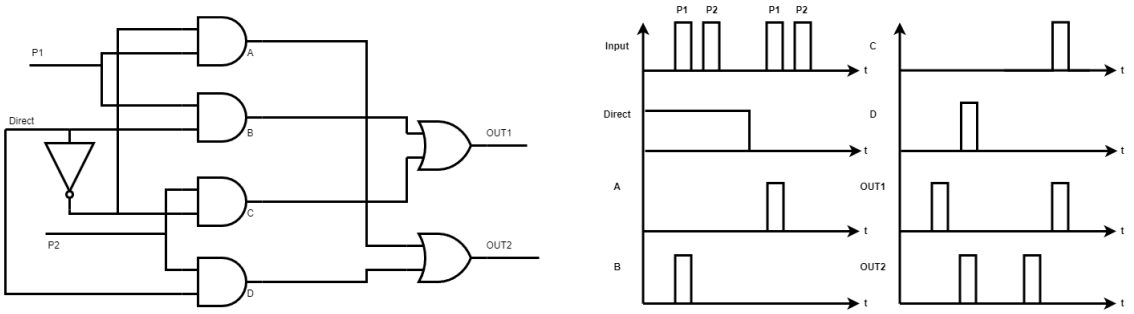
(a) Structure of the pulse generation block

(b) Timing diagram of the pulse generation block

Figure 4.10: Pulse generation block

4.5.4. Pulse Sequencing

Depending on whether the direction of the current at the zero-crossing point is positive or negative, the pulses must be put in the correct order so that the flipping process is correct. A pulse sequencing block proposed in [10] can be used to sequence two input pulses. The structure of the one pulse sequencing block and the timing diagram can be seen in Figure 4.11.



(a) Structure of the pulse sequencing block

(b) Timing diagram of the pulse sequencing block

Figure 4.11: Pulse sequencing block

4.5.5. Conclusion on SSHC circuit

The SSHC technique will be implemented to extract more charge from the energy source. The zero-crossing detection will be implemented by a falling edge trigger triggered by the output of the comparator in the active diode. The output of the zero crossing detection will be in the form of a pulse and be used as the clock signal to clock the direction detection. Direction detection will be implemented with a discrete-time comparator, clocked by the output of the zero-crossing detection. The pulse generation and sequencing blocks consist of a combination of logic gates and are only used for cold-start purposes.

4.6. Supporting Blocks

The key blocks and working principle of a cold-start SSHC rectifier for piezoelectric energy harvesting with high rectifying efficiency are finished. Some supporting blocks are still needed to support the correct operation of the circuit and will be discussed in the next sections.

4.6.1. Current Source

The active diode will require a continuous-time comparator to operate correctly. Conventionally, an operational amplifier in an open-loop configuration can work as a continuous-time comparator. For such a comparator, a biasing current is required. Therefore, a current source needs to be designed for the continuous-time comparator. The requirements are not strict since it is only used to produce a biasing current for cold-start purposes.

The current of a current source is normally determined by the ratio between a well-defined voltage and a resistor. The voltage can be the threshold voltage of a transistor, thermal voltage, or any de-

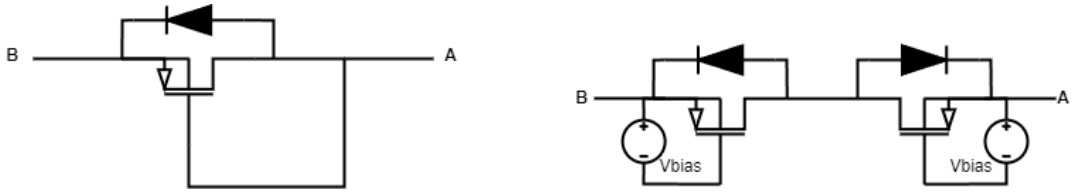
termined voltage in the circuit. A resistor can then be used with this voltage to determine the current. However, due to the resistor density limitation in CMOS technology, a large resistor will consume too much area and should be avoided for the cold-start circuit. Alternative methods to replace the resistor are required.

There are several solutions to replace the resistor in a current source. The following paragraphs will study two solutions to replace the resistors: a pseudo-resistor and a self-cascode MOSFET.

Pseudo resistor

One solution is the use of a pseudo-resistor, which is proposed to mimic large-value resistors in standard CMOS-integrated technology [17]. The simplest way to implement a pseudo resistor is to use a diode-connected transistor that works in the deep-subthreshold region, as shown in Figure 4.12a. The advantage of a single transistor pseudo resistor is its compatibility. The disadvantages include: first, Its I-V characteristic is inherently asymmetric because of the body diode. Second, it only supports a linear behaviour over a very small range of V_{AB} where the transistor works in the deep-threshold region. Last, it is very sensitive to process variations, and there is no way of optimizing the process behaviour as it is set by technological parameters.

Several symmetric pseudo-resistor topologies are proposed in [17] to improve the above-mentioned drawbacks. The basis of symmetric pseudo resistors is utilizing two single pseudo resistors and connecting them in series or parallel. The current is set by the least conducting cell when connected in series or by the most conducting cell when connected in parallel [17]. In addition, the resistance of a single transistor pseudo resistor can be tuned by either biasing the voltage between the gate and the drain or biasing the voltage between the gate and the source. Figure 4.12b presents one symmetric series pseudo-resistor that biases the gate-source voltage. With the improved pseudo resistor, the linearity and process variation are improved.



(a) Schematic of a single transistor pseudo resistor

(b) Schematic of a series symmetric pseudo resistor

Figure 4.12: Example of pseudo resistors

Self-Cascode MOSFET

The schematic of a self-cascode MOSFET (SCM) is shown in Figure 4.13. The principle of an SCM circuit is to bias the transistor M2 in the triode region so that there is a linear relation between I_{ref} and $V_{DS,s}$ of M2. The equivalent resistance of an SCM is determined by the aspect ratio between the top and bottom transistors, the biasing current of the SCM, and the inversion level of the SCM.

Discussion on Resistor Implementation

The pseudo resistor will require a biasing voltage for a stable resistance, and still, it only provides linear behaviour over a narrow voltage range. In addition, the sensitivity of process variations is very large for a pseudo resistor. By contrast, self-cascade MOSFET ensures better linearity and is relatively independent of the supply voltage and process variations. Therefore, the resistor in the PTAT current source will be implemented with a self-cascode MOSFET.

4.6.2. Bootstrap circuit

With the two-stage rectifier working as desired, the system still cannot operate in the way it is designed. The problem happens with the active diode. The maximum output voltage the comparator can provide is the supply voltage. For the switch in the active diode, the source voltage is basically also the supply voltage. In this situation, the gate-source voltage is either zero or a negative supply voltage, so the switch can never be closed.

A bootstrap circuit is introduced for this situation to provide enough gate overdrive voltage. The structure of a typical bootstrap circuit is shown in Figure 4.14 below.

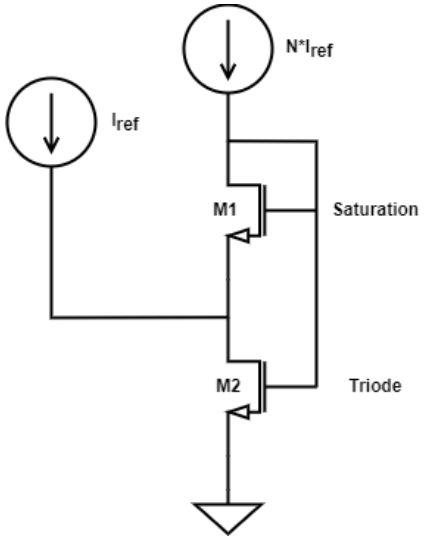


Figure 4.13: Schematic of self-cascode MOSFET

In phase one, switches S2 and S3 charge the top plate of the bootstrap capacitor to the supply voltage, and S5 connects the gate of the switch to the ground to open the switch. In phase two, S1 connects the bottom plate of the bootstrap capacitor to the source of the switch, thus lifting the top plate to the source voltage plus the supply voltage. S4 then connects the top plate to the gate of the switch. A gate overdrive voltage of supply voltage is produced to close the switch.

4.6.3. voltage-level detector

The voltage-level detector can measure the input voltage and follow the input voltage when the input voltage is higher than the threshold voltage. The voltage-level detector in this design will be used to disconnect the cold-start circuit when the voltage level in the storage capacitor is higher than the designed level. It will be implemented by an ideal block in this design because the required subsequent circuits are already available in the main harvester. So, it is unnecessary to design a new voltage-level detector, and it will not be part of the project.

The behaviour of a voltage-level detector can be seen in Figure 4.15. The voltage-level detector will be implemented with hysteresis to leave some time for the main harvester to start up. Otherwise, the cold-start will be kept turning on and off, and there will be no time for the main harvester to start up.

Figure 4.15: Input and output waveform of a voltage-level detector

4.6.4. Summary on Supporting Blocks

To ensure the correct operation and complete the cold-start stage, three supporting blocks, a current source, a bootstrap circuit, and a voltage-level detector are still needed. An alternate solution of the resistor in the current source is preferred, and the bootstrap circuit is essential for the correct operation of the active diode. The voltage-level detector will provide the cold-start circuit with a good finish and

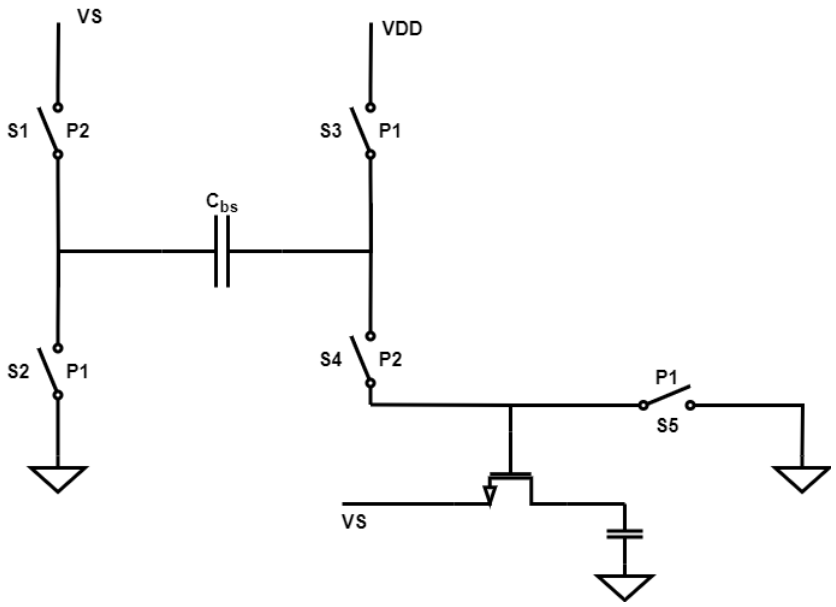


Figure 4.14: Bootstrap schematic

will be implemented with ideal blocks.

4.7. Top Level Design

With all the blocks discussed, Figure 4.16 shows the complete top-level design of the proposed cold-start circuit. In this figure, the red path represents the route of the input power, the blue path represents the route of output power, and the green path is the signal path. Such a circuit is both cold-start capable and offers low rectifier voltage drop when working as an active rectifier.

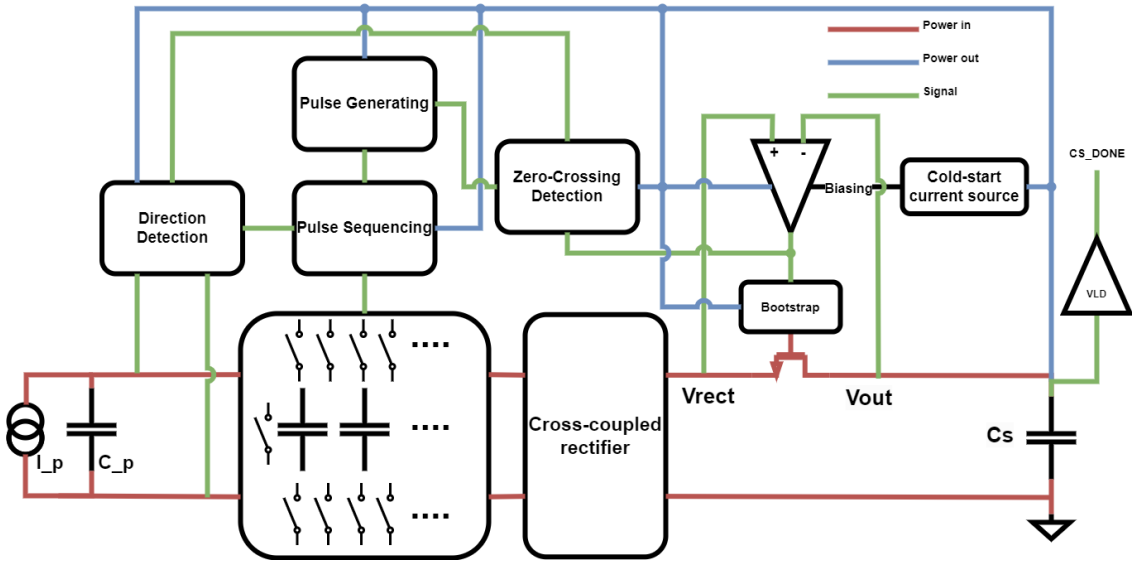


Figure 4.16: Top level diagram

The start-up sequence of the proposed design will work in the following order. As the intended start-up sequence, the cold circuit will go through three phases during the start-up. The expected output voltage and output of the voltage-level detector are shown in Figure 4.17.

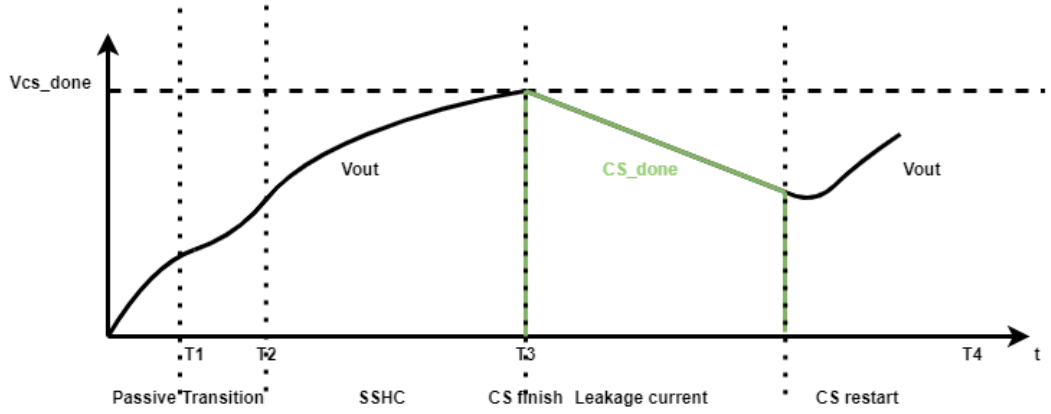


Figure 4.17: Expected result

- When the storage capacitor is completely depleted, the storage capacitor will be charged by the cross-coupled rectifier and the body diode of the active diode.
- The active diode will start working from T1 when the bootstrap circuit can provide a gate-source voltage higher than the threshold voltage. The voltage drop of the active diode will gradually decrease from T1 to T2 because the gate overdrive voltage produced by the bootstrap circuit increases with the supply voltage, making the on-resistance of the active diode decrease with the increase in the gate-source voltage.
- As the output voltage keeps increasing after T2, the effect of the bootstrap circuit and SSHC technique will appear. The voltage drop of the active diode will keep decreasing, and the flipping efficiency of the SSHC will gradually increase. More charge is extracted from the energy source as the SSHC keeps working.
- The voltage-level detector will disconnect the cold-start circuit after reaching the desired output voltage at T3. The voltage-level detector will completely shut down the cold-start circuit. The voltage on the storage capacitor will start descending due to the leakage current if nothing is connected further. The cold-start circuit will be turned on again when the output voltage is lower than the low threshold voltage of the voltage-level detector.

The structure of the continuous-time comparator, the discrete-time comparator, and the current source will be discussed in Chapter 6. The design consideration and design details of the blocks discussed in this chapter will also be discussed in Chapter 6.

5

Verification Scenario

5.1. Introduction

With the design of the cold-start circuit finished, the correct operation of the circuit needs to be verified through a series of tests. This chapter will discuss the verification of the designed system. The chapter begins by setting up the application background and design environment. Then, the start-up requirements and the definition of input power are determined. Next, the verification for the subsystems will be discussed, and conclusions will be drawn.

5.2. Application

The energy harvester aims to harvest vibration energy around human motion according to the project description given by Nexperia Energy Harvesting. Extensive literature research in Chapter 2 suggests that human movement vibrations typically occur at low frequencies, normally between 1Hz to 10Hz.

The schematic of the cold-start system is designed using Cadence Virtuoso. The process is the 180nm technology. Five process corners, SS, FS, TT, SF, and FF, will be verified. The first letter represents the speed of the NMOS transistor, and the second letter represents the speed of the PMOS transistor, with S standing for slow, F for fast, and T for typical. The circuit will be verified through different temperatures, from -40°C to 85°C. The impact of the mismatch and process variations will be checked by Monte Carlo simulations as well.

The process provides three types of NMOS transistors with different threshold voltages: nominal-VT devices, medium-VT devices and native-VT devices. The threshold voltages of these devices are approximately 870mV, 470mV and -110mV. For PMOS, only nominal-VT devices and medium-VT devices are available. Threshold voltages are 750mV and 440mV, respectively.

5.3. Start-Up Requirements

As per the requirements set forth by Nexperia Energy Harvesting, the primary function of the cold-start circuit is to charge the storage capacitor to a specific voltage level so that enough energy is accumulated on the storage capacitor to turn on the main harvester. Two requirements on start-up voltage level and current output capability will be the priority in the cold-start system. These are as follows:

1. The current main harvester will work properly from roughly 2.3V. A safety margin of 200mV is used to ensure a successful start-up. Consequently, the final voltage on the storage capacitor after the cold start should be at least 2.5V.
2. The cold-start circuit should support a leakage current of 500nA at a voltage of 2.5V. This includes the leakage current of the storage capacitor and the leakage current of the main harvester, which is not operating during cold-start.

Although area consumption is not the most important criterion in this project, it should be minimized because the cold-start circuit only plays a small part in the entire energy harvester. There is also no hard requirement on the flipping efficiency of the cold-start circuit, but a higher flipping efficiency will help the circuit reduce the start-up time, which is also beneficial to the actual application.

5.4. Circuit Modelling

The impact of the process variations and the temperature on the cold-start circuit depends on the IC technology. However, the energy source does not depend on the IC technology. The temperature or process variations of the source components can be reflected as changes in the parasitic capacitor and open-circuit voltage. So, different values of parasitic capacitors and open circuit voltage of the piezo elements will be verified.

A sinusoidal current source and a capacitor from the analogue library implement the piezoelectric energy harvester. The current source represents the charge produced per cycle, and the frequency is the excitation frequency. The frequency range is from 1Hz to 10Hz, in which most of the simulation will be done under 10Hz to minimise the simulation time, but the 1Hz frequency input will also be checked. To ensure compatibility with a wide range of piezoelectric energy harvesters, the value of the parasitic capacitor is chosen to range from 100pF to 100nF.

To simulate the desired 500nA leakage current at 2.5V, the load comprises an ideal storage capacitor and a 5MΩ ideal load resistor.

5.5. Input Power

As discussed in Chapter 3.5, the performance of a piezoelectric energy harvester is typically evaluated by comparing its performance to the output power of an ideal full-bridge rectifier operating at its maximum power point. However, it is important to note that these comparisons are based on the assumption that there is an MPPT circuit capable of adjusting the load impedance. In the case of cold-start, where the load impedance cannot be altered to accommodate variations in the piezoelectric transducer and impedance matching cannot be achieved, the conventional definition of input power may not be applicable to cold-start applications.

Due to the special situation during the cold start, an alternative definition is required. This definition should be consistent with the conventional definition while accommodating the cold-start constraints. By defining circuit parameters specific to the cold-start application, a more suitable and comprehensive performance evaluation can be done.

The following sections will explain how the input power is defined in the cold-start scenario and show the limitation of the input-power definition based on the maximum power point.

5.5.1. Input Power Definition

In Chapter 3, the parameters of a piezotransducer can be calculated by applying the output voltage and power from an ideal full-bridge rectifier. The output power of a full bridge rectifier for a given output voltage is given in Equation 5.1; the parameters in the equation are explained in Equation 3.4. The maximum power point is reached when $V_{rect} = 0.5V_{oc} - V_D$.

$$P_{out,FBR} = V_{rect}Q_{out,FBR}/T = 4f_pC_pV_{rect}(V_{oc} - V_{rect} - 2V_D) \tag{5.1}$$

The traditional definition assumes a matched load and the output voltage is a fraction of the open-circuit voltage, which is not true in the cold-start case. In this project, the input power is defined as the output power from an ideal full bridge rectifier loaded by a constant 5MΩ load resistor such that the output voltage is now detached from the impedance matching and only relates to the output power. The short-circuit current and open-circuit voltage can then be calculated using Equation 5.1 and substituting the V_{rect} from Equation 5.2, where R_L is the 5MΩ load resistor.

$$V_{rect} = \sqrt{P_{out} \cdot R_L} \tag{5.2}$$

5.5.2. Input Parameters of Piezotransducer

Using the definition from the previous section, the following tables (Table 5.1 and 5.2) are the calculated peak current of the sinusoidal current through the conventional and proposed definition. Notably, considering the case when the parasitic capacitance is 100pF, and the output power is 1uW, the conventional definition gives a sinusoidal current with a peak value of only 200nA, while the proposed definition produces a 720nA peak current. If both cases are looking for the 1uW output power, the conventional definition requires about 15V output voltage, which is far beyond the duty of the cold-start circuit, while the proposed definition requires only 2.24V.

Table 5.1: Short-circuit current of different parasitic capacitors and input power following from the conventional definition

	1uW	10uW	100uW	1mW	10mW
100p	200nA	630nA	2uA	6.3uA	20uA
1n	630nA	2uA	6.3uA	20uA	63uA
10n	2uA	6.3uA	20uA	63uA	200uA
100n	6.3uA	20uA	63uA	200uA	630uA

Table 5.2: Short-circuit current of different parasitic capacitors and input power in proposed definition

	1uW	10uW	100uW	1mW	10mW
100p	720nA	2.27uA	7.14uA	22.66uA	71.65uA
1n	840nA	2.67uA	8.43uA	26.66uA	84.3uA
10n	2.1uA	6.7uA	21.1uA	66.6uA	210.7uA
100n	14.75uA	46.64uA	147.52uA	466.4uA	1.472mA

For reference and to help future comparisons, Table 5.3 has been prepared. This table includes the corresponding MPP power calculated from the proposed input power definition. The MPP power will be higher than the proposed power, meaning that the cold-start circuit is not extracting the maximum power from the energy source. More power is wasted on the source impedance due to impedance mismatching. It is acceptable for the cold-start scenario because efficiency is less important than the output voltage during the cold-start.

Table 5.3: MPP power using the proposed definition

	1uW	10uW	100uW	1mW	10mW
100p	13uW	130uW	1.3mW	13mW	130mW
1n	1.8uW	18uW	180uW	1.8mWA	18mW
10n	1.13uW	11.3uW	112.5uW	1.1mW	11.3mW
100n	5.5uW	55.1uW	551.2uW	5.5mW	55mW

5.5.3. Limitation of the System

By calculating the charge delivered per cycle, the maximum constant current that the piezotransducer can supply can also be calculated. Equation 5.3 calculates the maximum DC current the source can provide, in which I_p is the peak current of the input current source.

$$I_{max} = Q_p \cdot f_p = \frac{2I_p}{\pi} \tag{5.3}$$

Using Equation 5.3, it becomes apparent that starting from 1uW with a parasitic capacitor of 100pF is unfeasible. In this case, the maximum DC current is 458nA, and there is no way to increase it to 500nA. For the case of 1uW input power and 1nF parasitic capacitor, the maximum current is 508nA, which is also hardly possible to provide 500nA DC current, considering the current consumption of the active circuits and losses due to the non-ideal flipping.

5.6. Subsystem Verification

The cold-start process comprises multiple stages that can be tested one after another during the start-up. From the start-up procedure, the subsystem test can be broken down into four stages.

The first subsystem test will check the period when the circuit works passively as a full-bridge rectifier. During this phase, the feasibility of utilizing the body diode in the active diode to initially charge the storage capacitor is assessed. This period also includes the transition from passive rectification to active rectification, in which whether the system can successfully be transformed into an active circuit is verified.

Subsequently, the circuit will function as an active full-bridge rectifier. The function of the bootstrap circuit in the active diode and the continuous-time comparator are evaluated. The direction-detection

and the zero-crossing detection blocks are also verified, as they are controlled by the falling edge of the comparator in the active diode. After this phase, everything that happens before the flipping technique is activated has been validated.

The pulse generation and sequence will initiate after the direction detection and zero-crossing detection. However, due to the presence of 1uF flying capacitors in the flipping technique, it will require multiple cycles to charge the capacitors before the function of the flying capacitors becomes observable. Therefore, the circuit will work as a switch-only rectifier initially and gradually turn into an SSHC rectifier as the voltage in the flying capacitors increases. The effectiveness of the flipping technique will be examined in this phase.

The cold-start will finish after the voltage in the storage capacitor reaches 2.5V. The voltage-level detector will shut down the cold-start circuit, and the cold-start is over.

In the entire start-up process, several critical signals play a pivotal role in monitoring and evaluating the system's performance. These signals include:

- Voltage on the storage capacitor. This signal reflects the energy accumulated in the system. Also, this is the only signal that will matter for the start-up.
- Voltage on the parasitic capacitor. Monitoring this signal helps assess the harvesting efficiency of the system.
- Voltages across the active diode. Measuring these voltages evaluates the efficiency of the active diode as well as the functionality of the flipping technique.
- Outputs of the direction detection and zero-crossing detection. These signals indicate whether the system is detecting the information correctly, ensuring correct flipping and synchronization.
- Pulses of flipping technique. Monitoring these pulses will make sure the flipping technique is working properly.

Measuring and analyzing these critical signals from the top level is enough to observe the working status of the entire system during the start-up. Additionally, these signals will provide insights into how to optimize the performance and efficiency further.

5.7. Verification Overview

The cold-start system will be verified using the input power outlined in Sections 5.5.1 and 5.5.2. Starting from 1uW input power with parasitic capacitors of 100pF and 1nF is impossible. The primary objective of the start-up is to charge a storage capacitor connected in parallel with a 5MΩ load resistor to a minimum voltage of 2.5V across all process corners from -40°C to 85°C.

During the testing, while the efficiency of the system will be measured, it is not the primary focus. Additionally, the lowest boundary of the start-up will be recorded across temperatures and process corners.

6

Cold-Start SSHC design

6.1. Introduction

With the top-level design decided in Chapter 4, Figure 4.16, the schematic design of the cold-start circuit will be discussed in this chapter. Each subsystem will be analyzed and discussed in terms of the start-up sequence. Cross-coupled rectifiers and current sources will be discussed first as the basis for the cold-start circuit. The active diode and circuits for the SSHC circuit will be discussed next. A summary of the schematic design will be given at the end.

The general requirement for all the subsystems is that the subsystems should be capable of working across a wide supply voltage range, and the start-up voltage of each subsystem should be as low as possible.

Unless otherwise stated, the transistors used in this design are 5V medium-VT devices.

6.2. Cross-Coupled Rectifier

A cross-coupled rectifier is a passive and self-switching rectifier. The performance of the cross-coupled rectifier is limited by the on-resistance and the reverse current. The reverse current is inevitable for such a structure, and it will be solved by the two-stage approach. Therefore, the only requirement for this rectifier is to have a low on-resistance.

The on-resistance of a transistor, assuming it to operate in strong-inversion triode region, can be calculated by Equation 6.1 below, in which W, L are the width and length of the device, μ_n is the electron mobility, C_{ox} is the oxide capacitance, V_{GS} is the gate-source voltage and V_{th} is the threshold voltage.

$$R_{on} = \frac{L}{\mu_n C_{ox} W (V_{GS} - V_{th})} \tag{6.1}$$

During the operation of the cross-coupled rectifier, the gate-source voltage is given, so the parameters available for optimization are the size of the transistors and the threshold voltage. Although there are native-VT devices with an even smaller threshold voltage, the threshold voltage is too small for native-VT devices that two paths will always conduct simultaneously, which means the cross-coupled rectifier is not rectifying anything. The size of the transistor and the ratio between PMOS and NMOS are swept for the best performance. Since the final voltage drop will be the product of the current and the on-resistance, and the current in this application is relatively small, mostly in the uA range, increasing the W/L ratio by a lot will only benefit the performance by several mV. The eventual sizes of the transistors used in the cross-coupled rectifier are given in Table 6.1. The corresponding on-resistance of the PMOSs and NMOSs at 2.5V gate-source voltage is 170Ω and 150Ω, respectively.

Table 6.1: Size of NMOS and PMOS transistors used in the cross-coupled rectifier

Transistor type	Size
NMOS	20/0.8
PMOS	80/0.8

6.3. Current source

A Proportional To Absolute Temperature (PTAT) current source is required as the cold-start current source. Figure 6.1 presents the schematic of the PTAT current source implemented with an SCM and its start-up circuit. The reference current from the current source will mainly be used to bias the comparator in the active diode. A nano-ampere reference current is designed to decrease the power consumption of the current source. The biasing current of the comparator can be adjusted by the multiplier in the tail current source if more current is required. In addition, the structure of a PTAT current source can support a wide range of supply voltages. The sensitivity to the supply voltage variations can be reduced by applying cascode transistors. However, the sensitivity to the supply voltage is already acceptable with one transistor, and to minimize the operating voltage, the cascode current sources are not used. The PTAT current is biased at 4.3nA. The estimated current consumption of the designed current source is 25.8nA.

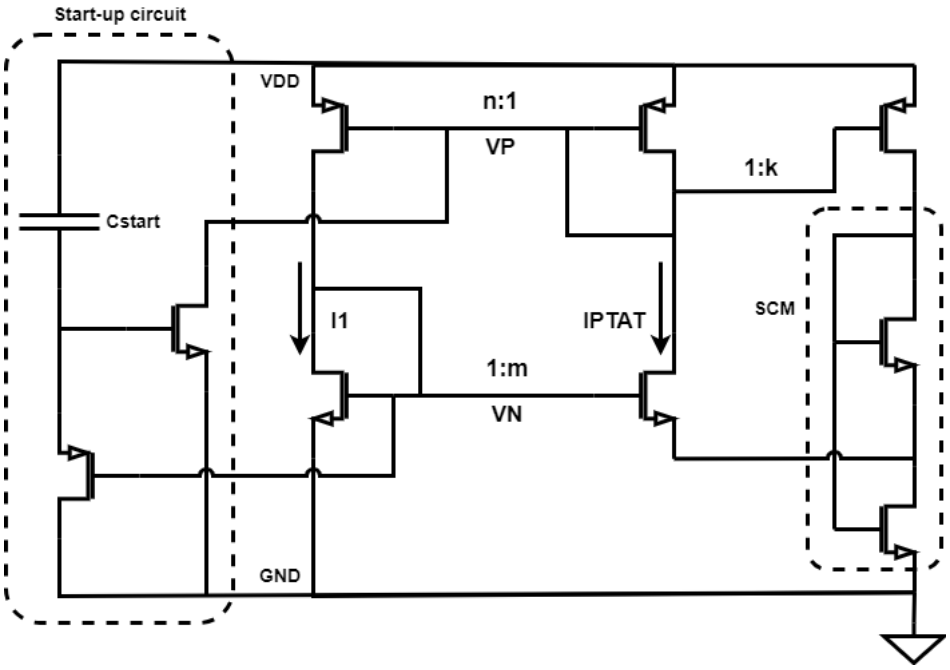


Figure 6.1: PTAT current source

6.4. Delay Cell

Delay cells are required at multiple places in this design, such as the dead-time, zero-crossing detection and pulse generation circuits in the SSHC. Conventionally, a delay cell can be realized by inserting a capacitor between two inverters, as shown in Figure 6.2a. The capacitor will increase the time required for the first stage to charge the output capacitor to either the supply voltage or the ground, thus creating latency.

The power consumption of an inverter can be split into dynamic power, static power, and short-circuit current. Static power is caused by the leakage of the diodes and the sub-threshold current. The static power is affected by the threshold voltage of the technology and the supply voltage of the application. Also, the static power is usually insignificant, and there is little way of improving it, so it will not be studied further. The other two types of power consumption are more considerable and will be studied next.

- Dynamic power is caused by charging and discharging the load capacitor and internal capacitances of an inverter. It can be calculated by Equation 6.2, in which C_L is the load capacitor, V_{DD} is the supply voltage, and f is the frequency under which the inverter operates. For this application, the dynamic power can be improved by decreasing the load capacitor or the supply

voltage.

$$P_{dynamic} = C_L V_{DD}^2 f \tag{6.2}$$

- Short-circuit current is caused by the simultaneous conduction of the PMOS and NMOS, creating a short circuit between the supply rail and the ground rail. The short-circuit current can be improved by a fast input ramp so that the period that the PMOS and NMOS are both on is decreased or by increasing the load capacitor so that the output changes slower and the period of short-circuit decreases. In addition, the short-circuit current is related to the threshold voltages of the NMOS and the PMOS transistors. With a lower threshold voltage, the short-circuit current increases.

The conventional way of increasing the load capacitor will increase the dynamic power a lot, especially if a large latency is required. In this design, the supply voltage is unchangeable, and the load capacitor is also a hard requirement for a certain latency. Also, the output of the first stage will be slowed down by the capacitor, and the short-circuit current of the second stage will be increased. Since medium-VT devices are used for a lower start-up voltage, the short-circuit current increases further. Due to the capacitor density limitation in the CMOS technology, putting capacitors will also consume additional chip area.

Another method to implement the delay cell is to use the current-starved inverter shown in Figure 6.2b. Unlike the previous way that increases the load capacitor to make the charging slower, the current-starved approach decreases the current of charging the load capacitor. Both ways will slow down the output. However, the dynamic power of a current-starved inverter is decreased a lot because there is no additional capacitor added to the output. In addition, even if the output of the first stage is slowed down, the current source in the second inverters will limit the short-circuit current. Therefore, both the short-circuit current and the dynamic power of a current-starved cell are improved a lot compared to the conventional delay cell using a capacitor. Another advantage of the current-starved delay cell is that it saves a lot of area compared to the capacitor approach.

The main disadvantage of the current-starved approach is that it will require a higher supply voltage than that of the delay cell that uses a capacitor because the two current sources do require a bit more voltage headroom for biasing. Some variants can be used to decrease the required headroom. For example, removing the I_{b1} and I_{b4} in Figure 6.2b will make the circuit only generate a latency at the rising edge of the input and less headroom is required.

The main consideration of a delay cell in this design is the power consumption, in which the power consumption of the current-starved approach is particularly prominent. Although it needs more headroom, it only just does the start-up later during a cold start, which does not affect the overall functionality or performance. Using a little headroom and time to trade for a huge decrease in power consumption and area is very worthwhile. Therefore, all delay cells in the cold-start circuit will be implemented by the current-starved approach.

Of course, the current-starved delay cell will require two bias voltages (Vp and Vn) for the transistors that implement the current sources. These voltages are already present in the current source in the overall circuit, so no extra effort is required for this approach either.

6.5. Active Diode

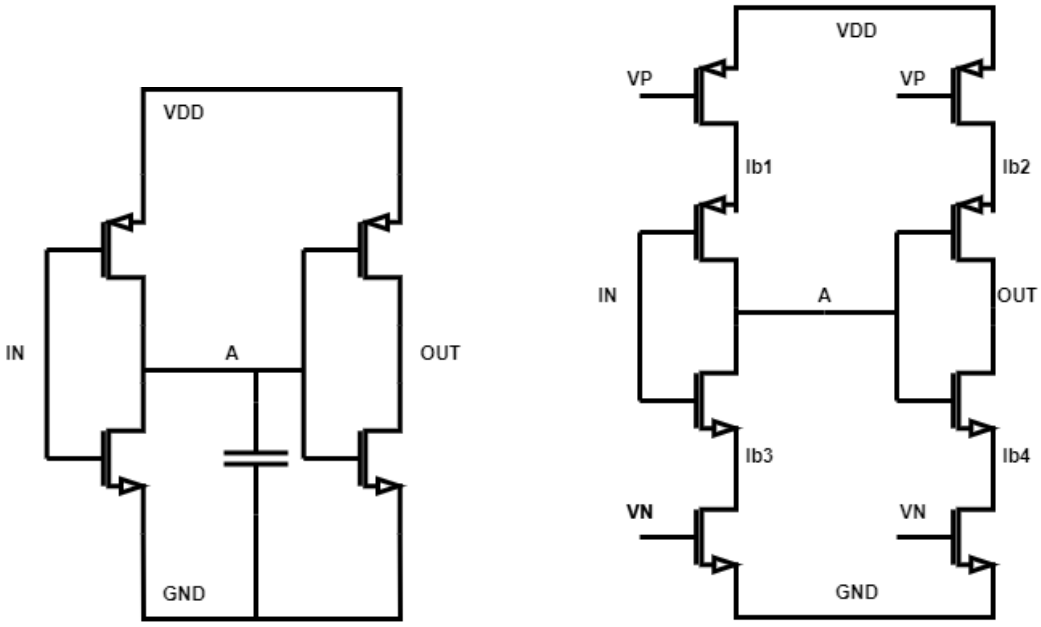
The active diode is the most important component in the cold-start circuit, as it controls all the operations of the following blocks. The active diode comprises a continuous-time comparator, a switch and the bootstrap circuit. This section discusses the design of the active diode.

6.5.1. Switch Type

The switch needs to remain closed during the passive operation. During passive operation, the output voltage of the comparator can either be the output voltage or the ground.

If a PMOS switch is used, the source-gate voltage is already higher than zero, so there is a risk that the PMOS switch is always conducting in the beginning. The start-up will not succeed in this case.

An NMOS switch has to be used to keep the switch open in the beginning. The bulk of the NMOS switch will be connected to the higher potential to ensure that the storage capacitor can still be charged by the body diode when the comparator does not have enough supply voltage.



(a) Schematic of a delay cell using capacitor

(b) Schematic of a current-starved delay cell

Figure 6.2: Delay cells

6.5.2. Active Diode Comparator

The connections of the active diode comparator are shown in Figure 6.3. The bootstrap circuit is omitted. Several requirements are summarized for the comparator.

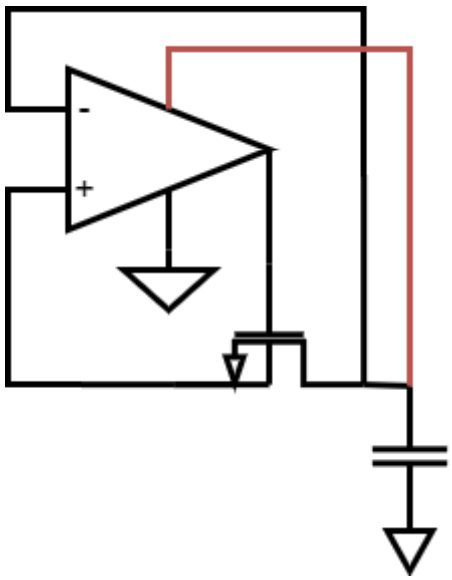


Figure 6.3: Structure of the active diode

Latency of the Comparator

Ideally, in an SSHC rectifier, the flipping process occurs immediately after the current discharges the parasitic capacitor. In this design, the flipping happens at the falling edge of the comparator. The falling edge should happen as soon as the parasitic capacitor starts being discharged if the switch voltage drop is small enough. However, the instant that the comparator opens or closes the switch will be affected by the noise, mismatch, and pull-up and pull-down speed of the comparator. This section will study the impact of latency on the rising edge and the falling edge.

The latency on the rising edge will decrease the charge delivered to the storage capacitor. The amount of charge wasted usually will not be too much as long as the latency is not too big, so a latency on the rising edge is not critical.

The latency on the falling edge is very critical. The latency is caused by the time the comparator senses the input difference and starts pulling down the output. This latency will cause the voltage on the parasitic capacitor to be discharged first before the flipping, so the efficiency of the flipping technique decreases.

The impact of latency on the falling edge will be studied. Assuming there is a latency of t_d from the comparator, some charge is wasted to discharge the parasitic capacitor during this t_d. The wasted charge can be calculated in Equation 6.3, in which V_{oc} is the open circuit of the piezotransducer, C_p is the parasitic capacitor, and f is the excitation frequency.

$$Q_{loss,t_d} = \int_0^{t_d} I_p \sin 2\pi f t \, dt \; = V_{oc} C_p (1 - \cos 2\pi f t_d) \tag{6.3}$$

The remaining voltage on the parasitic capacitor can be calculated from Equation 6.3:

$$V_{remain} = V_{rect} - V_{oc}(1 - \cos 2\pi f t_d) \tag{6.4}$$

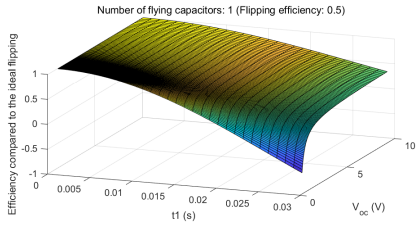
The efficiency of the flipping technique is decreased because the voltage on the parasitic capacitor is smaller. Compared to the original flipping from V_{rect}, the new flipping efficiency becomes:

$$\eta_{F,actual} = \eta_{F,ideal} \frac{V_{rect} - V_{oc}(1 - \cos 2\pi f t_d)}{V_{rect}} \tag{6.5}$$

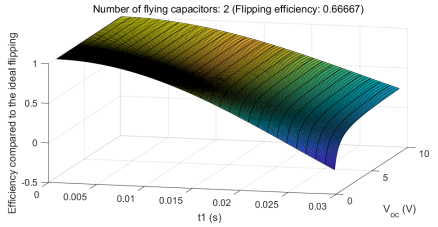
The efficiency of the SSHC technique is defined as the ratio between the flipping efficiency affected by the latency of the comparator and the ideal flipping efficiency.

$$\eta = \frac{4V_{oc} - 2V_{rect}(1 - \eta_{F,actual}) - V_{oc}(1 - \cos 2\pi f t_d)}{4V_{oc} - 2V_{rect}(1 - \eta_{F,ideal})} \tag{6.6}$$

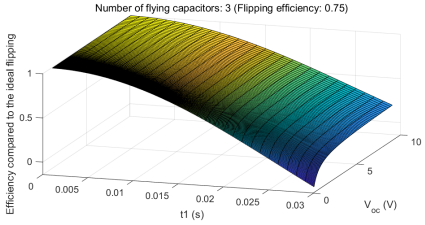
This efficiency will be affected by the latency and the open-circuit voltage. Figure 6.4 calculates the efficiency for different numbers of flying capacitors for a 10Hz excitation frequency.



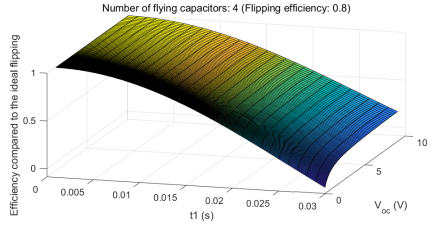
(a) Efficiency compared to an ideal flipping for one flying capacitor



(b) Efficiency compared to an ideal flipping for two flying capacitors



(c) Efficiency compared to an ideal flipping for three flying capacitors



(d) Efficiency compared to an ideal flipping for four flying capacitors

Figure 6.4: Efficiency of the flipping technique compared to an ideal flipping for different numbers of flying capacitors and open circuit voltage across the latency

The efficiency gets lower for a lower open-circuit voltage or a higher flipping efficiency. A maximum tolerable latency of 5ms is decided to keep the efficiency of the actual flipping at more than 95% of the ideal flipping.

Input Common-Mode Voltage

The comparator is powered directly from the voltage on the storage capacitor. The negative input of the comparator is the same voltage, and the positive input is the negative input voltage plus the voltage drop of the switch. Therefore, the input common-mode voltage of the comparator is the voltage on the storage capacitor, so the input pair has to be an NMOS input pair. Although a conventional OTA-based comparator or a latch comparator is possible to operate with a high common-mode input voltage, the output swing will be severely limited. A common-source PMOS second stage can be used to enlarge the output swing; however, the output swing from the first stage is barely enough to keep the PMOS in operation as the output gets higher.

A folded-cascode first stage is used because the folded-cascade structure can support an input-common voltage higher than the supply voltage while the output swing is unaffected by the input common-mode voltage. A current-starved inverter output stage is used for a rail-to-rail output swing and limits the short-circuit current.

Noise and Mismatch

Although noise and mismatch are two different parameters for a comparator, the impact of noise and mismatch will cause the rising and falling edge to appear earlier or later. Therefore, these two parameters can be categorized under the effect of latency. In the worst case, when the positive input just exceeds or drops below the negative input, the noise will have the risk of triggering the comparator multiple times if the comparator is too sensitive. However, this phenomenon will disappear when the voltage difference at the input increases.

Biasing Circuit

The layout of the biasing circuit of the active diode comparator will be drawn inside the comparator circuit for better matching. The biasing circuit of the comparator will also provide the biasing voltage for all the current-starved inverters.

Conclusion on Comparator

The comparator will be implemented with a folded-cascade first stage and current-starved inverter second stage because of a high input common-mode voltage and the desired rail-to-rail output as shown in Figure 6.5. The estimated current consumption of the comparator, including the biasing circuit, is 25.2nA.

It is not necessary for the comparator to have an operating voltage lower than the operating voltage of the current source. And the operating voltage of the current source is enough for the comparator to keep all the cascode transistors working. The tail-current source is implemented with a cascode current source to mirror the current from the current source accurately. Although the accuracy of the tail-current source is not too important in this design, there is enough voltage headroom to place the cascode transistor.

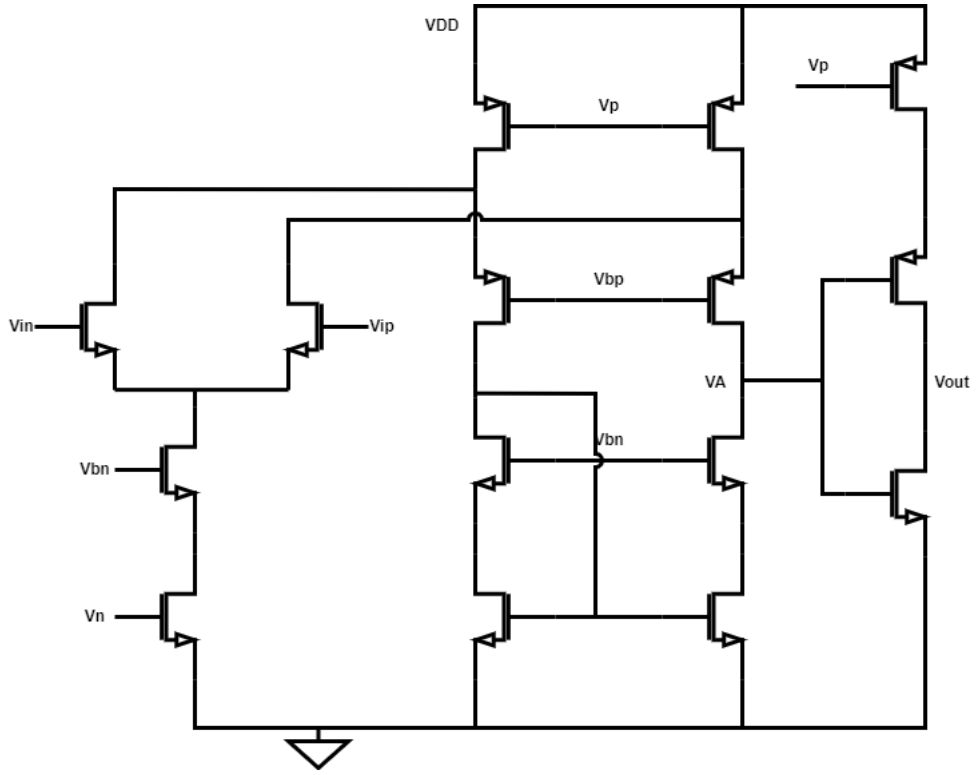


Figure 6.5: Schematic of the comparator in active diode

The performance requirement of the comparator is to keep the latency of the falling edge within 5ms. The noise and mismatch requirements are included in the latency requirement. The biasing circuit of the comparator will also be used to bias the current-starved inverters.

6.5.3. On-Resistance Trade Off

Conventionally, the on-resistance of a CMOS switch should be designed to be small to minimize the conduction losses. In this design, the voltage variation on the positive input is the product of the input current and the on-resistance of the switch. A faster input current or a bigger on-resistance will help trigger the comparator by increasing the voltage difference and slope at the input of the comparator. The system as a whole is simulated and used to optimize the W/L ratio. Using the same comparator and input parameters, Figure 6.6 simulates the output voltage of different W/L ratios from 0.1 to 4. The output voltage is higher for a smaller W/L ratio.

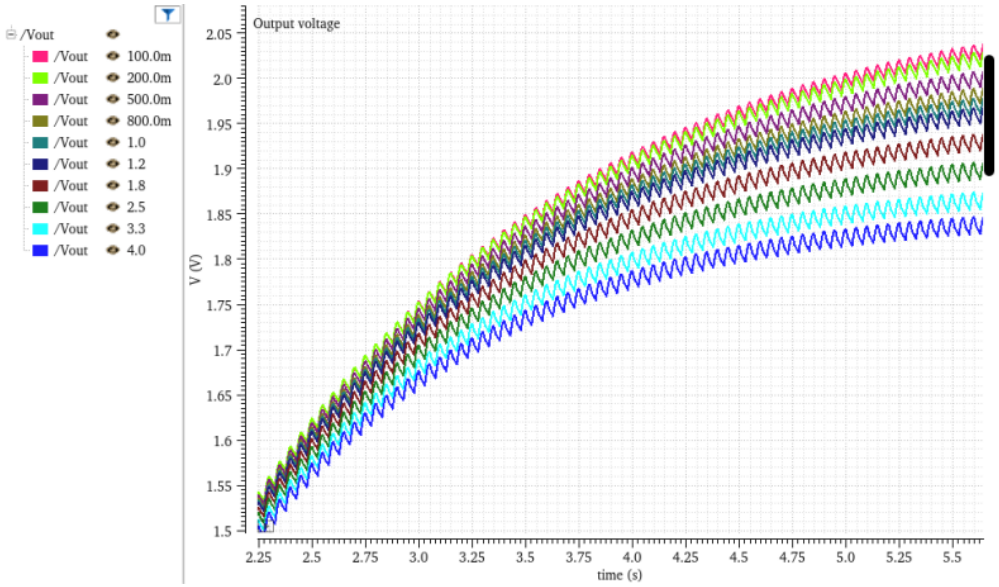


Figure 6.6: Output voltage of different the W/L ratios

However, making the on-resistance too big will decrease the final voltage again because the wasted charge to overcome the switch voltage drop becomes more considerable than the wasted charge caused by the latency of the comparator; for example, if the switch voltage drop becomes the threshold voltage of a diode, then a big portion of the output power will be used to overcome this voltage drop. This design uses a W/L ratio of 0.2 because the final voltage of the W/L ratio of 0.2 is only less than 10mV lower than the W/L ratio of 0.1, but the W/L ratio of 0.2 saves half of the area. The resulting on-resistance of the active diode switch for 2.5V gate-source voltage is 23kΩ.

6.5.4. Active Diode Stability

The active diode will encounter stability issues as it operates. Figure 6.7 shows the loop of the active diode. The loop includes the following items:

- Comparator: The comparator determines the sign of the voltage across the switch.
- Latency t_d: The latency of the comparator that is discussed in the previous section.
- Voltage difference at the input of the comparator: The voltage difference includes the voltage drop of the switch and a sudden voltage change on the storage capacitor represented by a current source. The current source simulates the current being pulled out from the storage capacitor at the rising and falling edge of the comparator.
- Circuit current consumption: At the rising edge, the current being pulled out from the storage capacitor is relatively small. It only includes the current of the active diode comparator itself, as the SSHC circuits are not working at the rising edge. At the falling edge, the circuit of the SSHC is activated, and a big current is pulled out from the storage capacitor. Therefore, the voltage change on the storage capacitor at the rising edge is much smaller than the change at the falling edge.
- Latency t_1: Latency t_1 is caused by the time difference between the falling edge of the comparator and the activation of the active circuit.

The transient across the active diode and a zoomed-in part of the falling edge are shown in Figure 6.8. The on-resistance of the switch is assumed to be zero. The various phases of operation are explained as follows:

- Before T1, the positive terminal is still higher than the negative terminal, and the comparator output level is still high.
- From T1 to T2, the positive terminal has decreased lower than the negative terminal. However, the comparator has not yet given the correct output at this time. The positive terminal is connected to

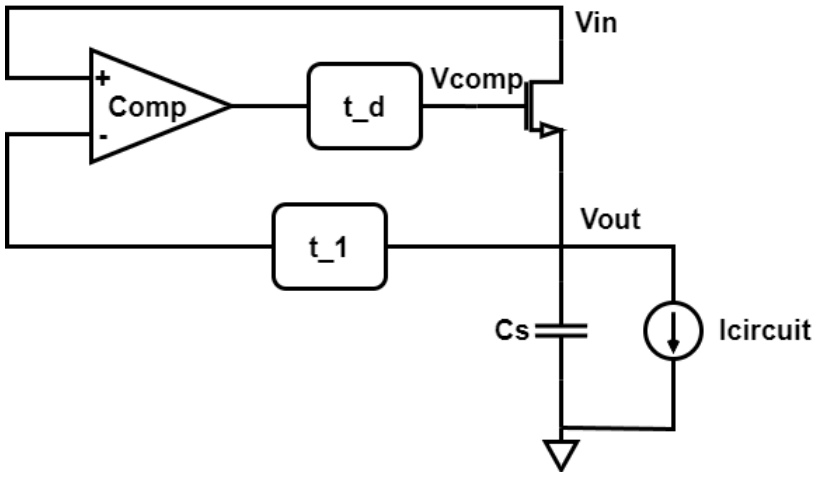
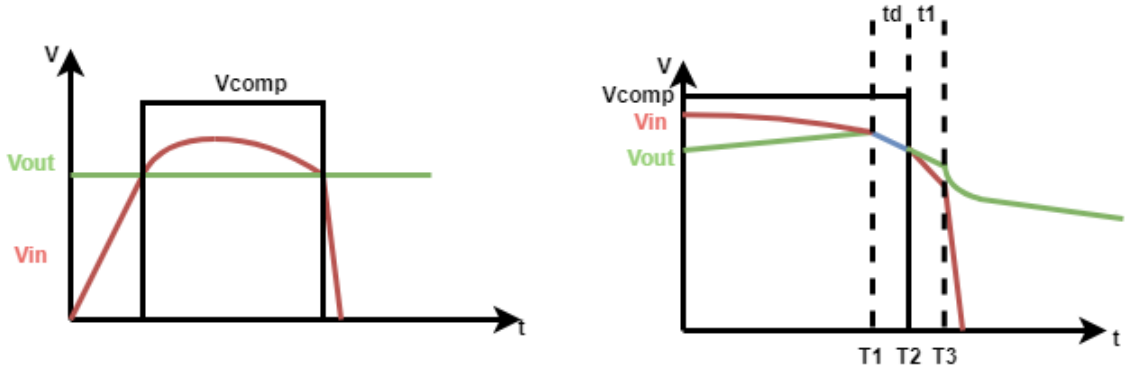


Figure 6.7: Loop of the active diode



(a) Transient in the active diode

(b) Zoom-in of the falling edge

Figure 6.8: Voltage of the active diode

the negative terminal during this period, which causes a reverse current. Both terminals descend at the same rate.

- At T2, the comparator opens the switch. The period from T1 to T2 is the delay of the comparator t_d.
- After T2, the positive terminal will be discharged by the piezo current. Therefore, it will drop faster than the negative terminal.
- At T3, the SSHC circuit is activated, and a current spike is pulled out from the storage capacitor, which causes a voltage drop on the negative terminal. The positive terminal will be pulled down to the ground rapidly by the SSHC technique. The period from T2 to T3 is the latency t_1

Instability can occur when the voltage on the negative terminal drops below the positive terminal. This will make the comparator close the switch when it should not and cause oscillation on the falling edge. The oscillation will be over until the positive terminal is low enough that the voltage drop on the negative terminal cannot affect the comparator.

There are three approaches to maintaining the stability of the comparator. The first approach is to decrease the power consumption of the active circuit. A smaller spike will cause a smaller voltage drop on the storage capacitor. The second approach is to increase the size of the storage capacitor so that the impact of a current spike gets smaller. However, this will come with the sacrifice that it takes longer to reach the desired output voltage. The third approach is to delay the activation of the SSHC technique; then, the negative terminal will not drop below the positive terminal. However, the efficiency of SSHC decreases. The first two approaches are considered since the impact of the third approach is not desired, while a longer start-up time is acceptable.

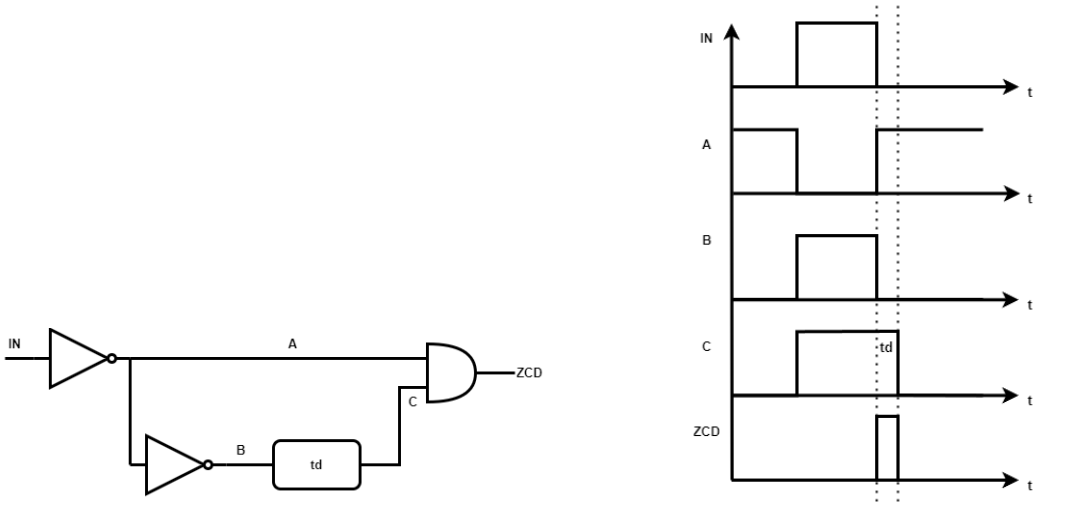
6.6. SSHC Technology

The design of the components in the SSHC technique will be discussed in this section.

6.6.1. Zero-cross Detection

The zero-crossing detection (ZCD) is the falling edge trigger depicted in Figure 6.9. The output pulse only has a minimum width requirement to ensure the direction detection works properly. In this design, it is tuned to 16μs at 2.5V because it is the required pulse width for the direction section circuit to make and lock the correct output.

The delay cell in the ZCD will only create a latency at the falling edge of signal B.



(a) Structure of the zero-crossing detection

(b) Timing diagram of the zero-crossing detection

Figure 6.9: Zero-crossing detection circuit

6.6.2. Direction Detection

The direction detection circuit is implemented with a clocked comparator. The target is to enable the entire cold-start circuit as soon as possible, so the number of stacked transistors should be minimized. The double-tail comparator in Figure 6.10 is implemented as this type of comparator is specifically designed for low-voltage applications. Also, a clocked comparator has very low consumption over time as it only consumes a small charge on the clock-rising edge. However, this topology will reset the output to ground after the clock becomes zero, so a D-latch must be added to lock the output. The double-tail comparator will work as follows:

- When the clock is low, the output of the comparator will be reset to the ground.
- When the clock is high, the input differential pair will sense the input voltage difference and create a differential current. The current difference will create a different rate when pulling up two output nodes. The cross-coupled inverter will latch one output to the supply voltage and the other to the ground.

Since the expected input voltage difference is very big. The comparator response will be extremely fast and accurate even if built with unit-size transistors.

6.6.3. Pulse Generation and Sequencing

The pulse generation and sequencing circuit will be used to control the SSHC technique. The minimum pulse width required is decided to be 10μs, considering two time-constant of the RC network formed by the flying capacitor and the on-resistance of the switches assumed to be 50Ω. The overlapping between pulses needs to be avoided. The overlapping will cause a charge redistribution between flying capacitors. The charge in the first flying capacitor will become less, and the latter will have more charge. This unexpected redistribution will result in a reduction of the flipping efficiency. Although the effect of the overlap obtained through simulation is almost negligible, it should still be avoided.

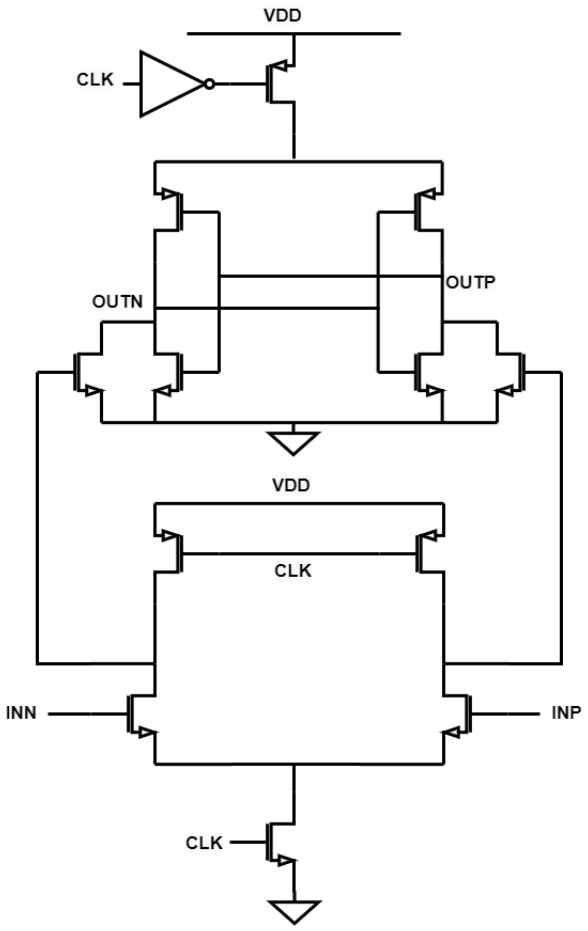


Figure 6.10: Schematic of a double-tail comparator

Bootstrap Pulses

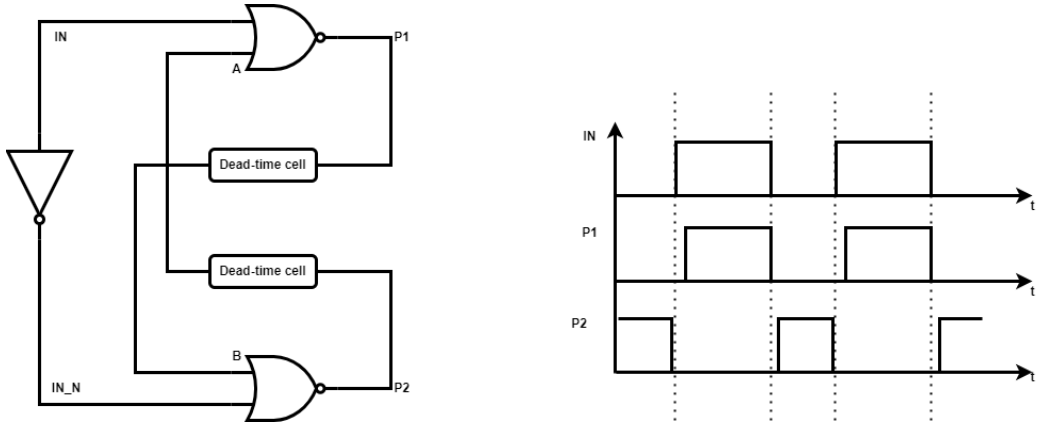
The voltages on the flying capacitors decrease with the number of capacitors. As shown in Figure 3.7, two groups of switches P_{1p} P_{1p} will experience the highest source voltage. Bootstrap circuits are added for these four switches for better flipping performance because these four switches have the smallest gate-overdrive voltage, and the on-resistance can be improved by the bootstrap circuit. It is also possible to implement bootstrap circuits for all switches, but the improvement achieved is not that much compared to only bootstrapping the switches of the first flying capacitors.

6.6.4. Switches in SSHC

NMOS switches are used for the switches in the SSHC circuit in Figure 3.7 because PMOS will have the risk of shorting the parasitic capacitor during start-up. The sizing of the switches needs to be balanced between the on-resistance and the gate losses. Considering the different source voltages that the switch will experience, the size of P0 can be smaller because the source voltage is zero. With the help of the bootstrap circuit, the size of P1 can be designed the same as that of P2, but both P1 and P2 need to be bigger than P0.

6.6.5. Phases Selection

The flipping efficiency of the SSHC technique increases with the number of phases and flying capacitors; therefore, the available charge increases. In the case of a cold start, it is necessary to consider whether the increased charge can compensate for the increase in the current when the pulse is increased. The benefit of increasing from zero flying capacitor to one flying capacitor will buy the circuit at most 50% flipping efficiency. Increasing to two flying capacitors will buy another 17% flipping. However, increasing from two capacitors to three capacitors buys only 9% and 5% if increasing to four capacitors.



(a) Schematic of the non-overlapping clock generator **(b)** Timing diagram of the non-overlapping clock generator

Figure 6.11: Schematic and timing diagram of the non-overlapping clock generator

In addition, it is introduced in Chapter 3 that the flipping efficiency is the highest when the flying capacitor is much larger than the parasitic capacitor of the PEH. In Equation 3.16, the output charge with the help of the flipping technique is related to both the flipping efficiency and the parasitic capacitor. For a fixed flying capacitor, a smaller parasitic capacitor will have a higher flipping efficiency, but the additionally gained charge from a higher flipping efficiency may not be as much as the charge used to generate and sequence the required pulses. Also, a smaller parasitic capacitor will require a lot of cycles to charge the voltage on the flying capacitor to the maximum. With the increase of the output voltage, it is hardly possible to reach the highest flipping efficiency during the cold start.

For a 10nF parasitic capacitor, the simulated current consumption of a signal pulse generating and sequencing circuit indicates that the gained current is worthwhile for increasing the number of flying capacitors to four in the typical corner at 27°C. However, in the FF corner at 85°C, the gained current using three flying capacitors is only enough to supply the increased current consumption of the increased pulses, so no actual performance improvement is achieved from using three flying capacitors. The gained current cannot support the increased current consumption anymore for four flying capacitors. So the most beneficial number of flying capacitors is two, in the FF corner at 85°C. In addition, the above analysis does not consider the fact that, firstly, the flipping efficiency will never reach its maximum during the cold start because the output voltage always keeps rising during the cold start. Secondly, losses to drive the additional switches will also increase.

A smaller parasitic capacitor will further reduce the gained current from increasing the flying capacitors, thus making it even less worthwhile to increase the number of flying capacitors. Although it is always worthwhile to increase the number of flying capacitors to four for larger parasitic capacitors (e.g., 100nF parasitic capacitor), a successful start-up for all parasitic capacitors, corners, and temperatures is more important than obtaining the maximum current for one specific parasitic capacitor. Therefore, it is decided that only two flying capacitors will be used for the cold-start circuit.

6.7. Bootstrap Circuit

The bootstrap circuit will require two non-overlapping clocks to generate the bootstrapped voltage. The schematic of a conventional non-overlapping clock generator and its timing diagram are shown in Figure 6.11. A current-starved dead-time cell is used to ensure the non-overlapping between pulses. The dead time is set to 5ns, considering the rising speed and falling speed of the pulses.

The bootstrap circuit will be used in the active diode and some of the SSHC pulses. The bootstrap circuit is shown in Figure 6.12. M1 to M5 implements the five switches in Figure 4.14. The gate voltages of M2 and M3 are replaced by VG to ensure the correct opening and closing. M7 is added to protect switch M5 from high-voltage breakdown. M6 and an inverter INV_1 are added to protect M4 from high voltages and ensure its correct closing.

For the application of bootstrapping the SSHC pulses, overlapping needs to be avoided between the bootstrapped pulse and the non-bootstrapped pulse. Because of the non-overlapping clocks, the actual falling edge of the bootstrapped voltage is behind the original pulse. It will not be a critical problem for

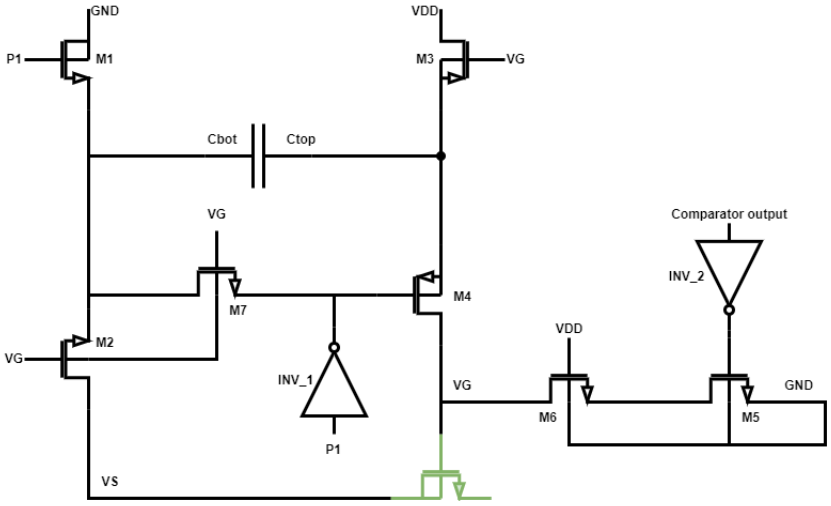


Figure 6.12: Schematic of the bootstrap circuit

the active diode switch because the latency of 5ns only wastes negligible charge. However, for the pulses in the SSHC technique, the latency from the actual falling edge and the limited slew rate at the falling edge will cause an overlapping with the next pulse. Therefore, the gate signal of M5 is changed to the inverted comparator output so that the gate of the conducting switch will be connected to the ground once the input pulse goes to zero. The output and timing diagram of the modified bootstrap circuit is shown in Figure 6.13

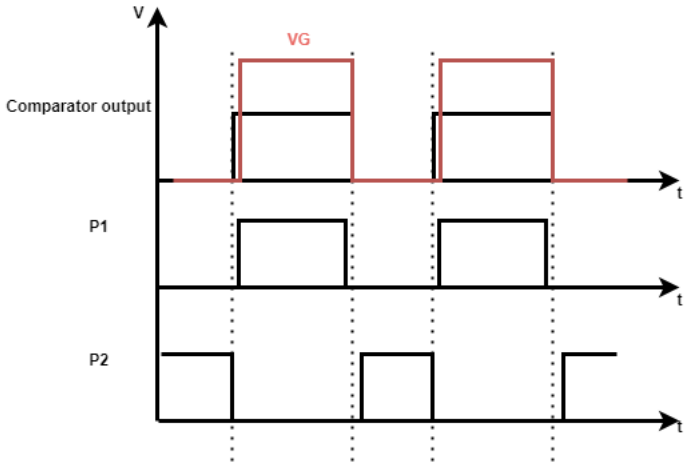


Figure 6.13: Output and timing diagram of the modified bootstrap circuit

Off-resistance of medium-VT Devices

Medium-VT devices are used in the bootstrap circuit to reduce the required voltage to close the switch so that the circuit can start up earlier. However, the leakage current of medium-VT devices can be relatively large at some specific temperatures and corners. Figure 6.14 measures the off-resistance of a nominal-VT NMOS and medium-VT NMOS with the same area across the temperature at the FF corner. The gate-source and bulk-source voltages are set to 0V for both devices.

In the FF corner and at 85°C, the off-resistance of a medium-VT NMOS is only 2.7MΩ, which is too low for a switch, while a nominal-VT NMOS can still have 13GΩ off-resistance. The leakage current is a critical issue for M1 and M5. The leakage current of M1 will create a path from VS to the ground, and the leakage current of M5 will connect the top plate of the bootstrap capacitor to the ground while the bootstrap capacitor should be connected to the gate of the conducting transistor. Both paths are unacceptable.

Although decreasing the W/L ratio will help to fix the leakage issue, it brings another issue. A big

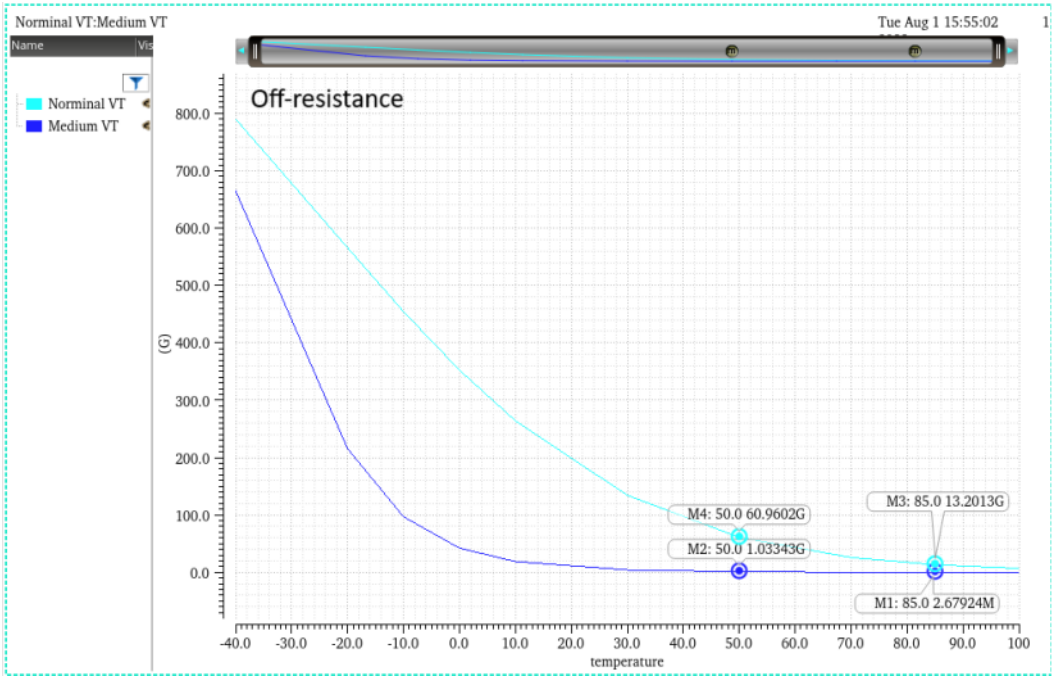


Figure 6.14: Off resistance of nominal -VT and medium-VT devices across the temperature

on-resistance from a small W/L ratio will limit the discharging speed of the gate voltage. While this can be accepted in the active diode, it will cause overlap for the pulses in the SSHC. To reduce the leakage current while guaranteeing a sufficient discharging speed, switches M1 and M5 are replaced with nominal-VT devices. The rest of the transistors are fine to work with medium-VT devices.

6.8. Pulse Chain

The rising edge and falling edge of the comparator output will be affected by the capacitive coupling of the subsequent blocks. A clean input signal for some blocks is very critical to avoid repeated triggering. For example, the zero-crossing detection will read the falling edge from the comparator. A jump on the falling edge that is caused by the subsequent blocks will cause the zero-crossing signal to be triggered multiple times.

The cleanest signal in the circuit is the signal that comes out of the non-overlapping clock generator. Since the non-overlapping clock generator only produces a very small dead time, the falling edge of P2 and the rising edge of P1 almost follow the falling edge of the comparator output. Therefore, the input of the zero-crossing detection will use pulse P2, and the input of the pulse generation in SSHC will use pulse P1.

6.8.1. Schmitt Trigger Inverter

Schmitt trigger inverters make the subsequent circuits less susceptible to the output of the preceding circuits. The schematic is shown in Figure 6.15. The Schmitt trigger inverter is used in the non-overlapping clock generator and pulse generation circuit. The Schmitt trigger will regulate the signal from the comparator in the former one and will regulate the output from the current-starved delay cells in the latter one. The schmitt trigger will also be applied in the zero-crossing detection to minimize the impact of the falling edge slew rate.

6.9. Voltage-Level Detector

The voltage level detector will be used to finish the cold-start stage. It is implemented with ideal blocks because it is beyond the scope of this work. The voltage-level detector will be turned on at 2.5V and turn off with a hysteresis of -0.5V.

The output of the voltage level detector is connected to the gates of several NMOS switches. The

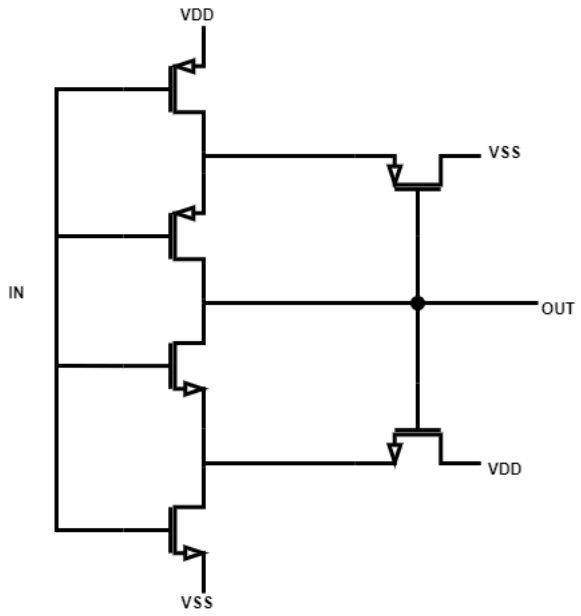


Figure 6.15: Schematic of a Schmitt trigger inverter

first NMOS switch connects the gate of the NMOS current mirror in the PTAT current source to the ground since the current source provides biasing for many active circuits. The second switch shorts the gate of NMOS in the folded-cascode comparator to ensure the shut-down of the comparator. The comparator controls all the subsequent circuits, so shutting down the comparator will stop the triggering of the SSHC circuit.

However, the cross-coupled rectifier is still passively connected. Three additional switches are implemented to disconnect two input terminals and one output terminal in the cross-coupled rectifier from the energy source.

It is also noticed that there are still floating nodes at the AND gate in the zero-crossing detection. One more switch is used to stabilize the voltage around the AND gate.

6.10. Conclusions

The schematic design of the cold-start circuit is discussed in this chapter. Except for two switches in the bootstrap circuit, all transistors are implemented with medium-VT devices.

A PTAT current source is used as the cold-start current source. The resistor will be implemented by a self-cascode MOSFET. The PTAT current source will support a wide range of supply voltages and bias the active diode comparator and the current-starved delay cells. The PTAT current is designed to be 4.28nA in the typical case.

The active diode comparator will be implemented with a folded-cascode comparator. The maximum allowed latency for the comparator output when the positive terminal drops below the negative terminal is 5ms. The switch of the active diode has to be an NMOS switch to ensure the switch is opened in the beginning. The on-resistance needs to be properly balanced to provide both a relatively small voltage drop and a large enough voltage difference for the comparator to work. A big storage capacitor has to be used to ensure the stability of the active diode.

The output pulse of the zero-crossing detection circuit has a width of 16μs. The direction detection is implemented with a double-tail clocked comparator. The pulses of the SSHC technique have a minimum width of 10μs.

As a suitable trade-off between the achieved charge from increasing the flying capacitors and the increased current due to increasing the phases, a two-capacitor, five-phase SSHC rectifier will be used for the cold-start circuit.

The gate voltage of the active diode will be bootstrapped for sufficient gate-overdrive voltage. The gate voltage of the switches in the first flying capacitor will also be bootstrapped for less conduction

loss.

The cold-start will be accomplished by shutting down the current source and active diode comparator through the voltage level detector at 2.5V. The cross-coupled rectifier will be disconnected. The cold-start circuit will be turned on again when the output voltage drops below 2V.

7
Result

7.1. Introduction

This chapter discusses the verification results from the schematic simulation of the cold-start circuit. The test results for each block will be discussed first. The cold-start system-level test will follow next. The lowest input power and excitation frequency of the cold-start circuit will be tested. The integration with the voltage-level detector will also be verified during the cold-start test.

As explained in Section 5.5.3, a start-up from either 100pF or 1nF parasitic capacitor with 1uW input power is impossible due to the lack of current. Therefore, unless otherwise stated, the typical input definition for the verification is 1uW power, 10nF parasitic capacitor and 10Hz excitation frequency because first, the parasitic capacitor of commercial piezoelectric energy harvester is close to 10nF. Second, 1uW is the minimum power from which the cold-start circuit should be able to operate.

The ability of the circuit being used for normal harvesting will be verified. The output power will be simulated by measuring the output current for a given output voltage. Then, the distribution of the power consumption will be measured.

7.2. Sub-block Test

The verification results of each block will be discussed in this section. The current source will be simulated separately. The rest of the circuits will be simulated within the cold-start circuit to check the impacts of the non-idealities on the overall performance.

7.2.1. Current Source

The current source is designed as 4.28nA at 2.5V in the typical corner and 27°C. Table 7.1 shows the maximum and minimum start-up voltage, temperature and voltage sensitivity and the PTAT current at 2.5V. The process corner and temperature of these results are noted; the first two letters represent the corner, and the last two letters represent the temperature. The current increases almost linearly with the supply voltage and temperature. The spread of the PTAT current across process corners and temperatures ranges within $\pm$30% of the current in the typical case.

Table 7.1: Current source summary

	Min	Typ	Max
Start-up voltage	452mV (FF85)	567mV (TT27)	688mV (SS-40)
Temperature sensitivity	10.9pA/°C (SS)	12.23pA/°C (TT)	13.65pA/°C (FF)
Voltage sensitivity (0.8V-3V)	231.3pA/V (SF27)	251.1pA/V (TT27)	282.5pA/V (FS85)
Current at 2.5V	3.26nA (SS-40)	4.28nA (TT27)	5.365nA (FF85)

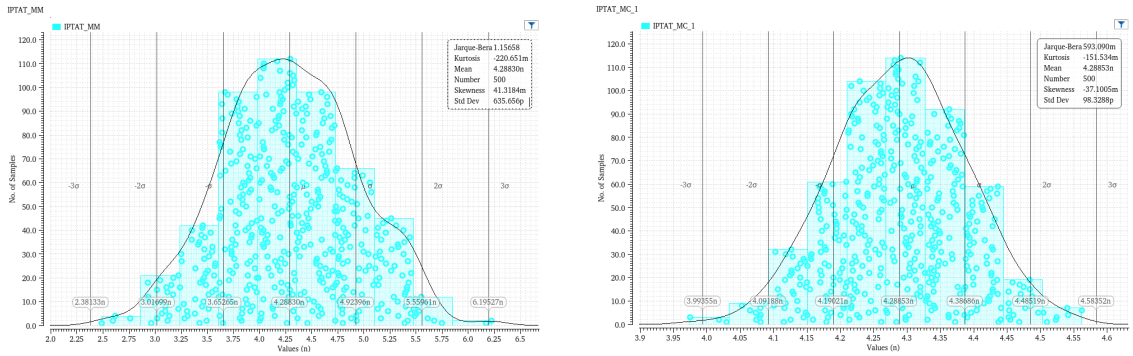
Mismatch and Process Variation

Table 7.2 summarizes the Monte Carlo simulation result of process variations across temperatures and the mismatch. The distribution of the mismatch and process variations at 27°C is shown in Figure 7.1.

Since the mismatch has nothing to do with temperature variation, the impact of the mismatch is only simulated at 27°C. The mismatch in the current source comes mainly from the PMOS current mirror and then the NMOS current mirror.

Table 7.2: Mismatch and process summary

	-40°C	27°C	85°C
Process (Mean)	3.48nA	4.28nA	5.01nA
Process (Std Dev)	69.39pA	98.35pA	123.06pA
Mismatch (Mean)		4.28nA	
Mismatch (Std Dev)		635.7pA	



(a) Monte Carlo simulation results of the mismatch

(b) Monte Carlo simulation results of the process variations

Figure 7.1: Summary of the Monte Carlo simulation of the current source at 27°C

Noise

The noise is simulated by the noise simulation with a noise bandwidth from 0Hz to 100kHz. The target frequency of the circuit is below 10Hz, so 100kHz is enough. The simulation result shows that the RMS current noise is about 37.6pA, which will not be an issue for the cold-start circuit.

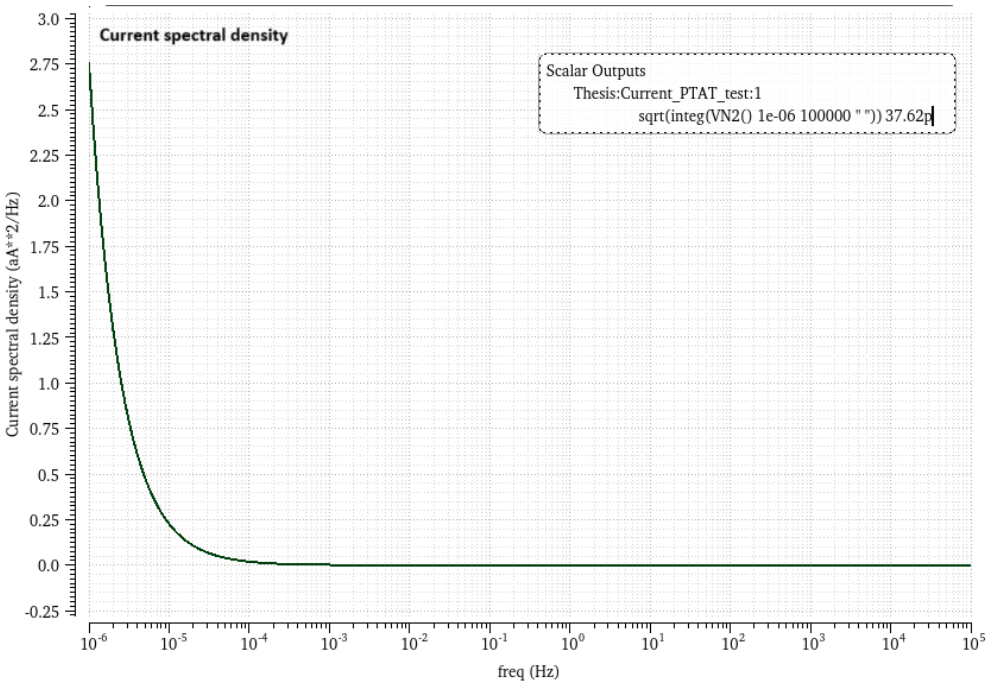


Figure 7.2: Current spectral density of the current source from 0Hz to 100kHz

Start-up

The start-up of the current source is tested by slowly ramping up the supply voltage. A ramp from 0 to 2.5 V in 8s is given as the supply voltage. Figure 7.3 shows the transient current and supply voltage during the start-up test.

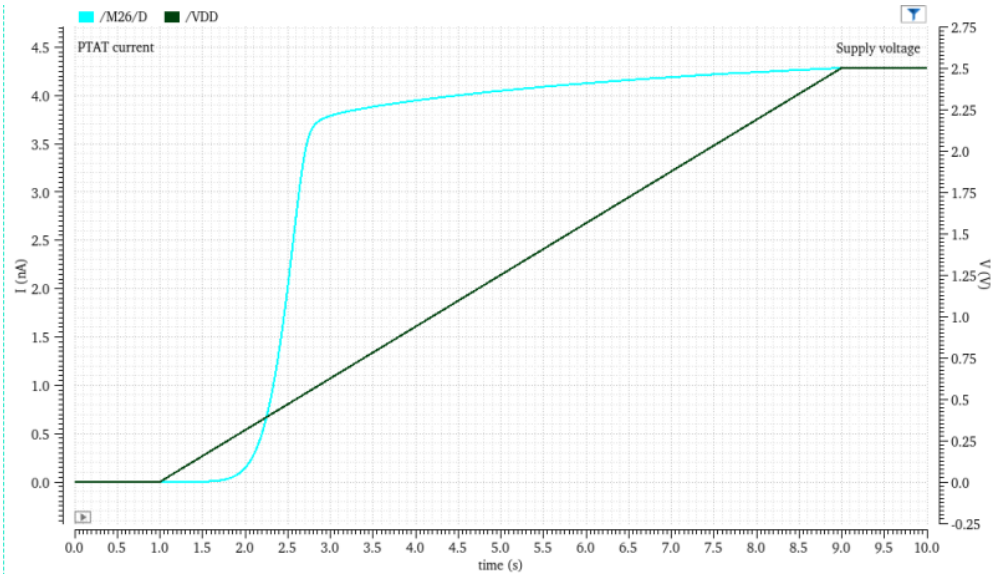


Figure 7.3: Start-up and transient noise of the PTAT current source

7.2.2. Active-Diode Comparator

In Section 6.5.2, the performance of the comparator is shown to be mainly limited by the latency of the comparator falling edge; therefore, the active-diode comparator is tested by measuring the latency between the comparator falling edge and the zero-crossing point of the current. The measured latency has two components: the latency caused by the voltage drop of the switch and the latency in the comparator. The latency is measured for different supply voltages and temperatures.

Figure 7.4 shows the latency caused by the voltage drop of the switch. As the output voltage increases, the effect of the bootstrap circuit becomes more pronounced, and the delay decreases. At low temperatures, the bootstrap circuit is less affected by the switch leakage, and therefore, a higher average gate-overdrive voltage is provided, and the on-resistance and latency are smaller. As the temperature increases, both the leakage in the bootstrap circuit and the conductivity of the switch increase, so the delay first increases. The latency decreases again as the switch conductivity increases and becomes more dominant than the leakage current.

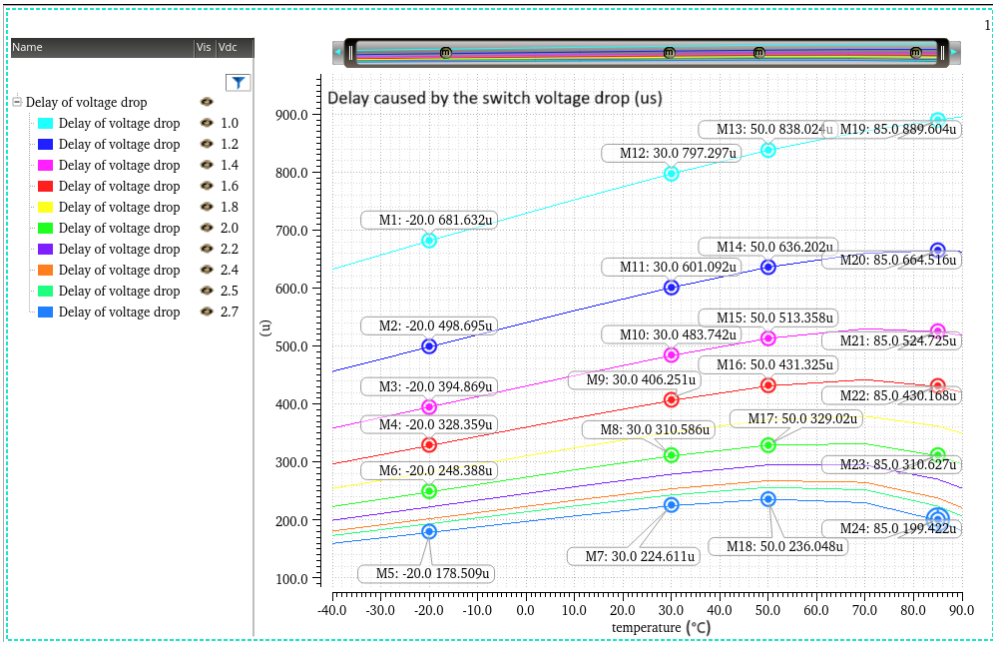


Figure 7.4: Delay caused by the voltage drop of the switch

The latency of the comparator is shown in Figure 7.5. The comparator operates faster as the temperature increases. However, when the supply voltage is small, the bootstrap circuit is less effective, so the on-resistance of the switch is larger. The bigger voltage difference at the comparator input makes the comparator faster when giving the output.

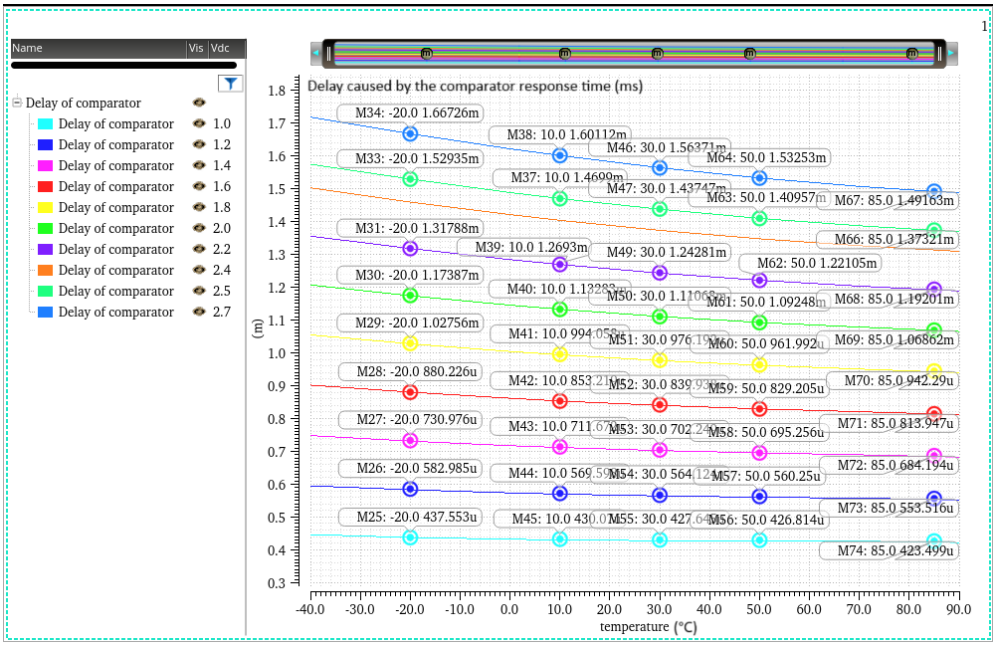


Figure 7.5: Delay caused by the comparator

Process and Mismatch

The process variation and effect of mismatch are simulated when the supply voltage is 2.5V. Table 7.3 summarizes the result from the simulation. The mismatch in the comparator is mainly caused by the NMOS current mirrors. In the mismatch results, the standard deviation is quite big compared with the mean value. This will introduce a 7ms latency caused by the comparator if considering the 3σ case. The efficiency of the flipping technique will be reduced by that, but the theoretical calculation shows

that 7ms latency can still maintain a very high efficiency. So, the conclusion is that it is slightly beyond the specification but still acceptable from the system level.

Table 7.3: Mismatch and process summary of the comparator

	-40°C	27°C	85°C
Process (Mean)	1.573ms	1.44ms	1.374ms
Process (Std Dev)	32.416us	28.878us	30.905us
Mismatch (Mean)		1.742ms	
Mismatch (Std Dev)		1.708ms	

Noise of the Comparator

The impact of noise is studied from transient-noise simulations. A total of 10 transient noise simulations are run to check the impact of the noise. The simulation results show that the effect of the noise on the comparator output only introduces several ns drifting on the rising and falling edge, but the shapes of all ten simulations are the same. The previously mentioned risk that the noise causes the comparator output to trigger repeatedly is not seen across PVT simulations because the comparator is not that sensitive to the small input variation caused by the noise.

7.2.3. Zero-Crossing Detection

The pulse width of the zero-crossing detection circuit is measured across process corners, temperatures, and supply voltages. The pulse width for different supply voltages across temperatures is shown in Figure 7.6.

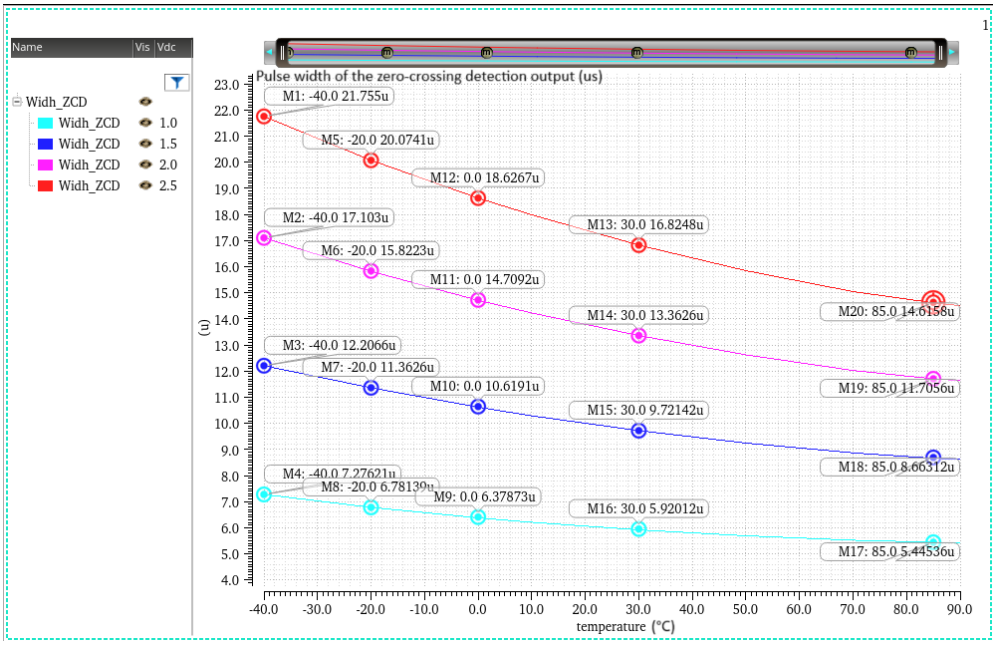


Figure 7.6: Pulse width of ZCD from 1V to 2.5V across temperatures

The current source is already stable from 1V, so the pulse width at all temperatures almost increases linearly with the supply voltage. The pulse width decreases for higher temperatures because the biasing current increases with the current source, and the load capacitor is charged faster at high temperatures. The result of the Monte Carlo simulation is summarized in Table 7.4. The pulse width varies between 15μs and 22.6μs by temperature, and the maximum standard deviation is 5μs due to the process variation at -40°C. Since zero-crossing detection is mostly constructed by logic gates, the mismatch effect should be small. The simulated mismatch result will also contain the effect of the mismatches from the comparator biasing circuit and the current source. So, the effect of the mismatch in the zero-crossing detection will not be checked separately.

Table 7.4: Process variation summary of the zero-crossing detection

	-40°C	27°C	85°C
Process (Mean)	22.58us	17.45us	15.03us
Process (Std Dev)	5.053us	3.273us	2.344us

7.2.4. Direction Detection

The direction detection is verified in a transient simulation as shown in Figure 7.7. There is a latency between when the circuit crosses zero and the output of the comparator, which is mainly caused by the delay of the falling edge of the comparator. The comparator always gives correct outputs for different supply voltages.

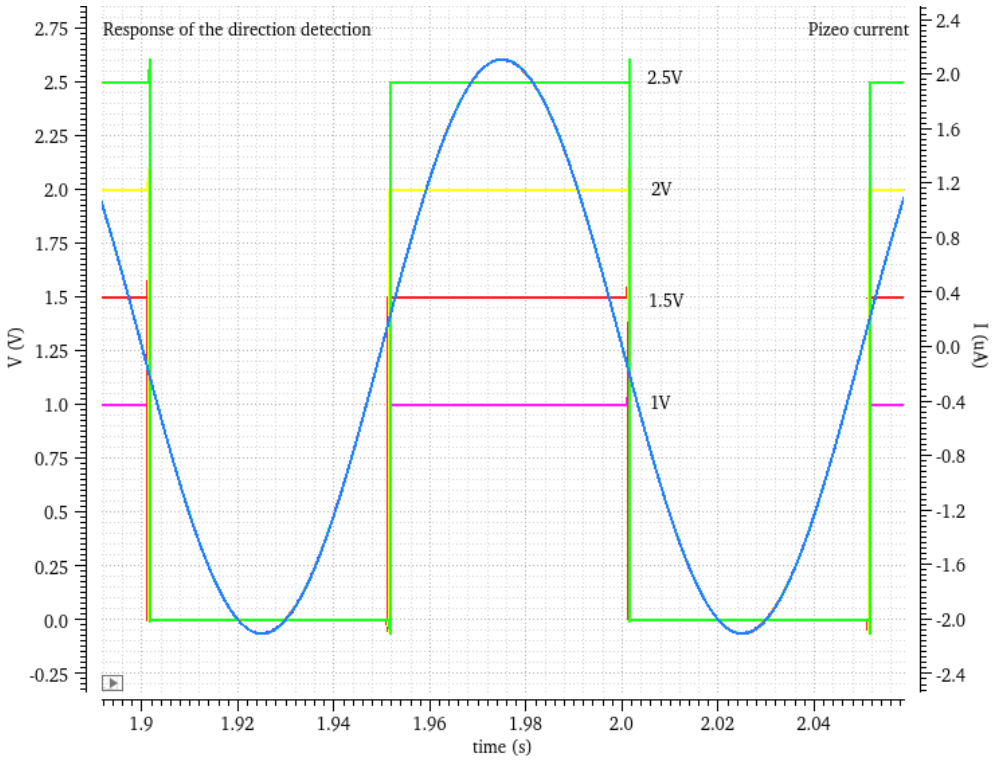


Figure 7.7: Result of direction detection

The comparator works correctly for different processes and temperatures in the system-level test and will thus not be tested here separately. Since the input-voltage difference of the comparator is very big, the mismatch or the noise will not impact the output of the comparator. The response speed of the comparator will not be checked as well because of the big input difference.

7.2.5. Pulse Generation and Sequencing

The pulse-generation and sequencing blocks are verified in two aspects. First, the width and sequence of the pulses will be verified. Second, whether there are overlaps between pulses will be checked.

The pulse width at different supply voltages and temperatures are simulated in Figure 7.8. The pulse width decreases with the temperature and increases with the supply voltage, the same results as the results of the ZCD pulse since the principle of the two circuits is the same.

The impact of process variations is summarized in Table 7.5. At 85 degrees, the pulse width suffers from large variation. The impact is that the flipping process will cost more time or less time. However, there is only a very small chance that the pulse width drops below the required 10us, considering the 3σ value. The effect of mismatch will not be checked for the same reason that the mismatch of ZCD will not be checked.

The overlap of the pulses and sequence are checked for different supply voltages as well. The

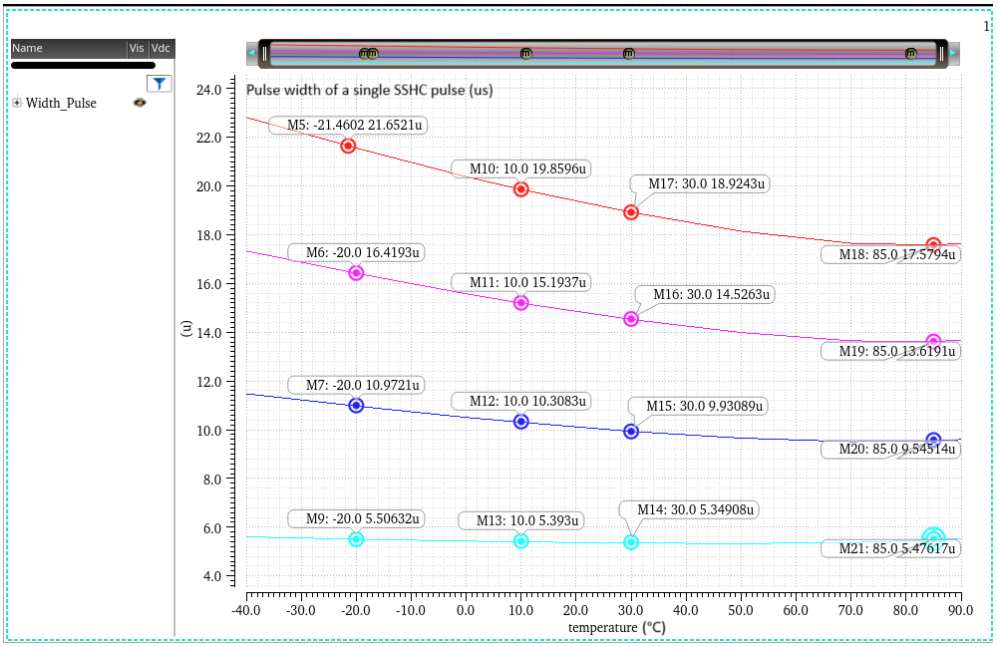


Figure 7.8: Pulse width of SSHC from 1V to 2.5V supply voltage across temperatures

Table 7.5: Process-variations summary of the pulse generation

	-40°C	27°C	85°C
Process (Mean)	22.81us	19.07us	18.15us
Process (Std Dev)	303.6ns	268.4ns	3us

sequence is correct, and there is no overlap between bootstrapped and non-bootstrapped pulses. A non-overlap time of 9ns is kept between pulses.

7.3. Cold-Start Test

After every sub-block is verified, the start-up process will be verified. The verification will be done for a storage capacitor of 20μF. First, a typical input level is tested. The case of FF85 is tested separately because it takes too long to charge the storage capacitor to 2.5V at FF85. The behaviour of sub-blocks and the transition of the circuit from a passive circuit to an active circuit is checked. Second, other cases of input power and parasitic capacitors are verified. The effect of the voltage-level detector is checked as well. Last, the lowest input power and frequency of the cold-start circuit are simulated.

7.3.1. Typical Case

The result of the typical input parameters is shown in Figure 7.9. All process corners can reach above 2.5V within 90 seconds except FF85. The slope of the start-up waveform also indicates the current consumption of different process corners and temperatures. With a faster slope, the current consumption is smaller. The flipping efficiency of the SSHC techniques is about 57.7% when the output reaches 2.5V in the typical corner and 60% in the FF corner.

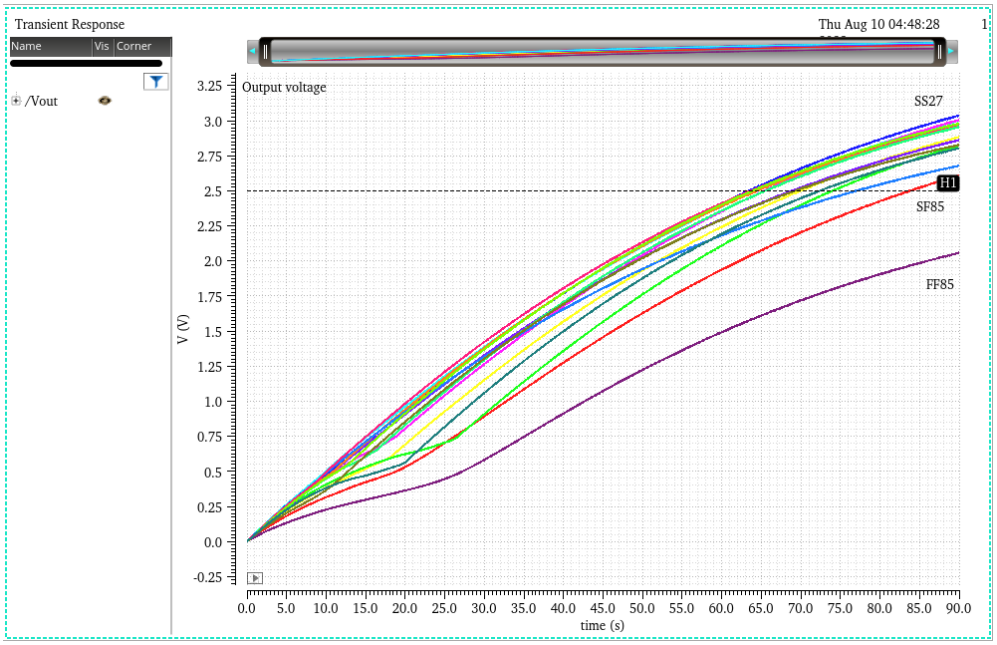


Figure 7.9: Output voltage of all corners with 1uW input power and 10nF parasitic capacitor

Start-up in the FF Corner at 85°C

The circuit can charge the storage capacitor to 2V at FF85 in the previous simulation result. Whether the storage capacitor can be kept charging to 2.5V will be verified by pre-charging to 2.5V and continuing to be charged. If the voltage does not drop below 2.5V afterwards, the start-up at FF85 is also successful. The result can be seen in Figure 7.10.

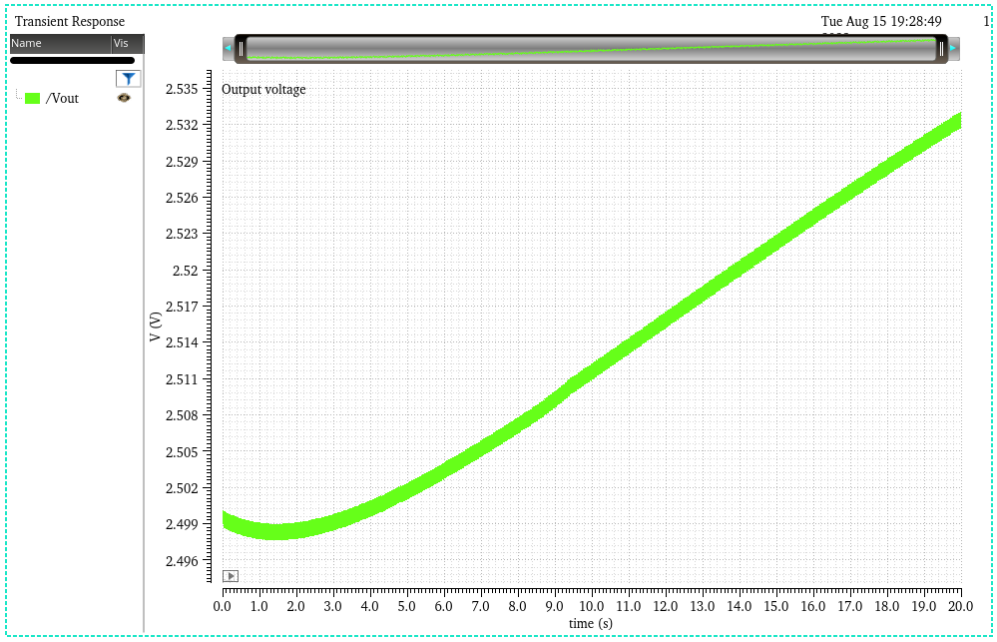


Figure 7.10: Output voltage at FF85 starting from 2.5V with 1uW input power and 10nF parasitic capacitor

Because the voltages on the flying capacitors are zero initially, and the circuit cannot support the current consumption of the active circuits at 2.5V, the output voltage drops in the first three seconds. The flipping efficiency increases gradually as the voltages on the flying capacitors build up. The output voltage starts rising when the flipping efficiency is high enough to support the output current. Eventually, the output voltage in the FF corner at 85°C can exceed 2.5V.

7.3.2. Transition during Start-up

Figure 7.11 shows the transition of the circuit in a typical case. Comparing the voltage across the active diode, the transition of the circuit from passive to active rectification can be seen. The difference between the two waveforms is the voltage drop of the active diode. In the beginning, there is a voltage drop of the body diode across the switch. The transition of the circuit occurs when the output voltage is near the threshold voltage. As the gate-source voltage of the switch gradually exceeds the threshold voltage, the switch works actively, and the voltage drop of the active diode decreases. The switch voltage drop is very small at high supply voltages.

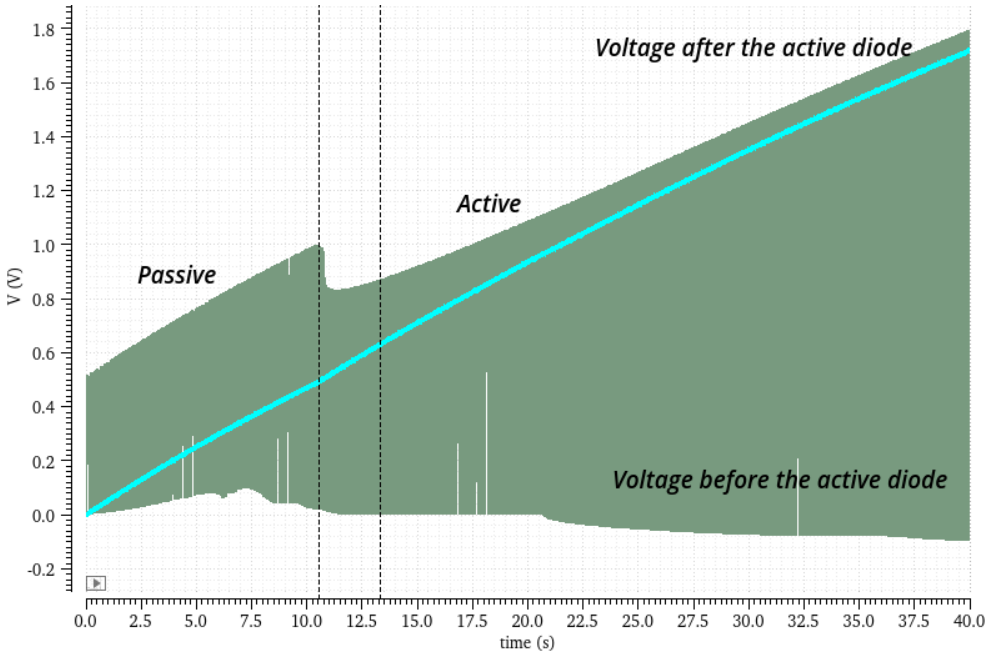


Figure 7.11: Transition of the circuit from passive circuit to active circuit

7.3.3. Behaviour of Sub-Blocks during the Start-Up

The behaviour of each sub-block during the start-up is checked. Figure 7.12 shows the output of the main circuit blocks, including the active-diode comparator, direction detection and zero-crossing detection. The pulses from the SSHC circuit are not shown because the circuit has basically the same structure as the zero-crossing detection circuit, and the output during the start-up is similar.

The active-diode comparator starts working first. The output voltage of the active-diode comparator is zero in the beginning. The input of the zero-crossing detection (Figure 6.9) is the signal from the active-diode comparator. The PMOS in the inverter is closed, and as the supply voltage increases above the operating voltage of the inverter, the output of the first inverter (point A) follows the supply voltage. In addition, the NMOS current source of the current-starved delay cell has not reached the operating region yet. Point C also follows the supply voltage. So the output of the ZCD/AND gate follows the supply voltage. Because the output of the ZCD is not very stable at low voltages, and the discrete-time comparator is not fast enough to reset the output at low voltages, the direction detection did not give the correct indication at low voltages. However, this unstable condition only happens at very low supply voltages. And the output stabilizes after about 250mV. The direction detection is affected by the output of the zero-crossing detection, as the output of the zero-crossing detection starts following the supply voltage. The discrete-time comparator sees a rising edge at the clock signal, so it gives an output. The start-up behaviour is affected by PVT variations, as different threshold voltages cause each block to operate at a different voltage.

In the initial state of the circuit, the zero-crossing and direction detection circuits that are built on the falling edge of the active diode comparator can already work when the active diode is still passive. When the zero-cross detection circuit has a pulse output, the output of the direction detection circuit is always correct. The physical meaning of the zero-crossing detection output should indicate the moment

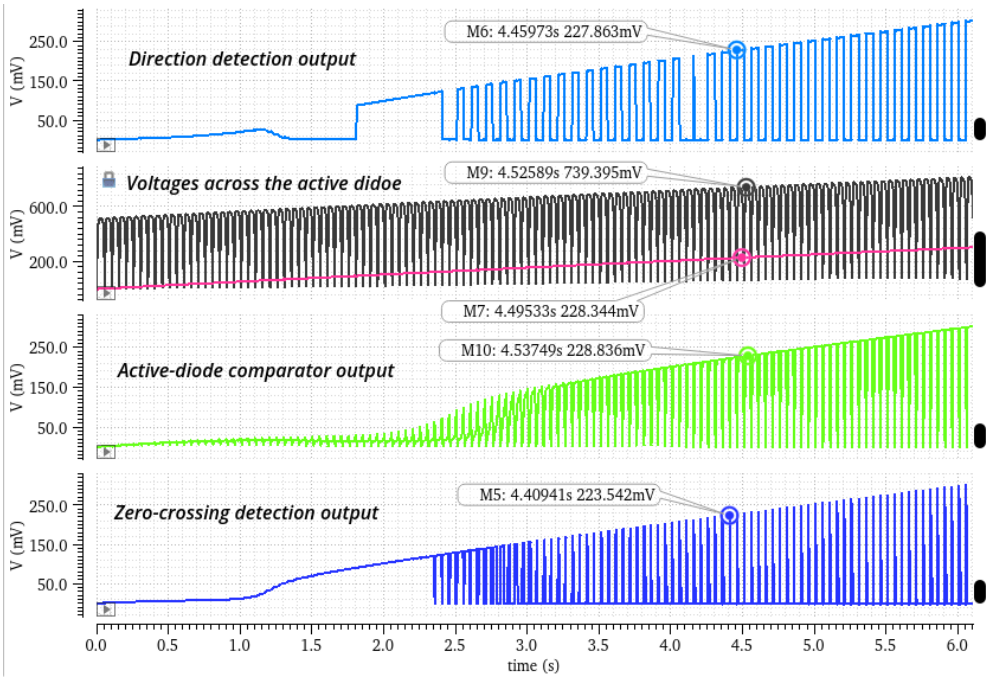


Figure 7.12: Behaviour of sub-blocks during the start-up

that the current crosses zero if the voltage drop of the active diode switch is small. However, because of the voltage drop of one body-diode voltage, the output of the zero-crossing detection circuit is correctly triggered by the falling edge of the comparator but it cannot represent the actual moment that the current crosses zero. This behaviour will not affect the general performance of the circuit because the cold-state circuit is still in the passive state and the supply voltage is not high enough for the active circuit to work effectively.

7.3.4. Other Input Scenarios

Other input power and parasitic capacitors are also verified. Verifying all input conditions in Table 5.2 is unnecessary because increasing the input power level will only make the start-up easier. Therefore, the input scenarios that will be checked are 100nF&1uW, 100nF&10mW and 100pF&10mW so that the corner cases are checked. These results are sufficient to illustrate the trend of increasing input power and parasitic capacitance. Figure 7.13 shows the result of start-ups from these input scenarios at the typical corner, 27°C and FF corner, 85°C, the upper waveform is the result in the typical corner, 27°C and lower one is the result in FF corner, 85°C. The start-up in the FF corner at 85°C is slightly slower, and the final voltage is lower than the results in the typical corner because of the increased current consumption.

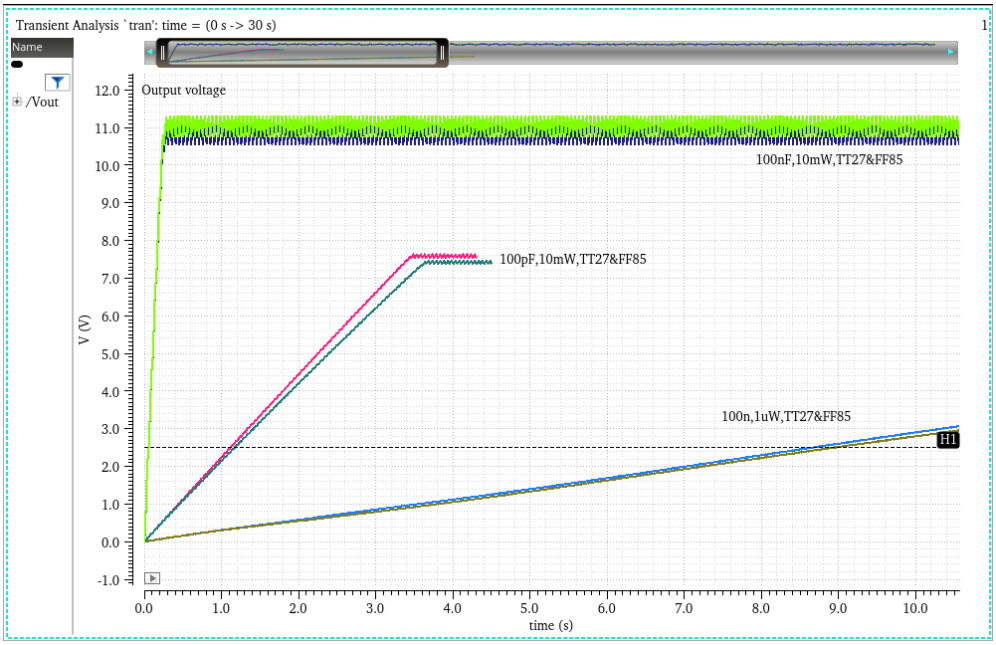


Figure 7.13: Start-up of other input power and parasitic capacitors

High-frequency inputs are also verified for 1uW input power and 10nF parasitic capacitor. The simulation results are shown in Figure 7.14. Increasing the frequency will make the start-up faster. The results show that the cold-start circuit can support up to 200Hz excitation frequency. Higher frequencies will not be verified as they exceed both the frequency of the project application and the main harvester's frequency range [49].

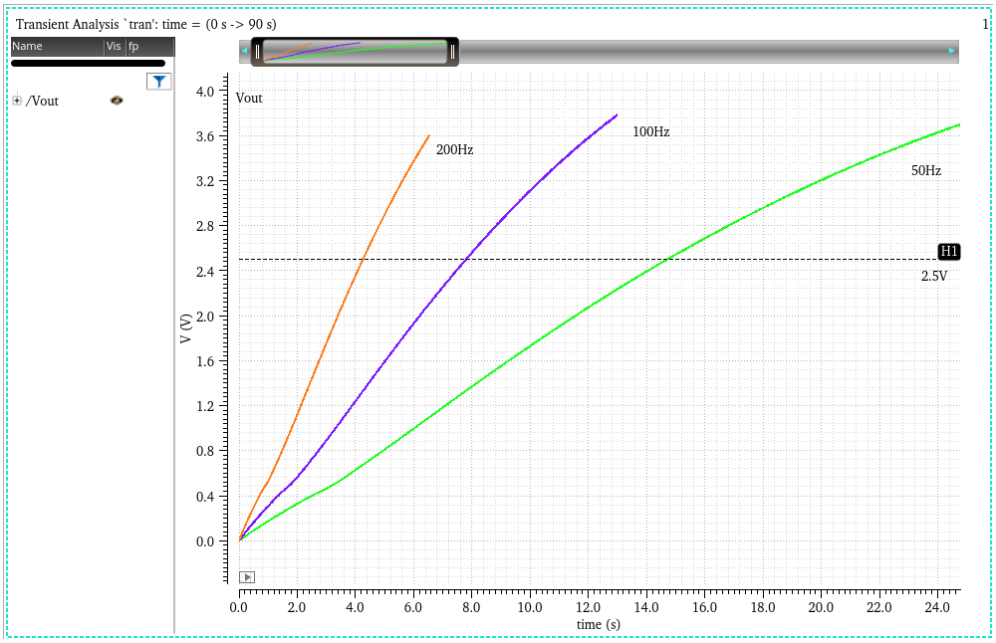


Figure 7.14: Start-up result of 10nF&1uW input at 50, 100 and 200Hz excitation frequency

Lower input frequencies will also be verified in the following section. As the application is to harvest energy from human movement, the feasibility of the start-up from 1Hz input frequency will be studied in Chapter 7.3.7.

7.3.5. Voltage-Level-Detector Test

The function of the voltage-level detector is tested by pre-charging the storage capacitor to 2.45V and then checking the behaviour when the output voltage reaches 2.5V. Figure 7.15 shows that the circuit is shut down when the output voltage reaches 2.5V. The circuit is turned on again when the output voltage drops below 2V. In addition, the leakage current of the circuit, when it is not operating, is measured. The leakage current of the circuit is 2.4nA at 2.5V. The VLD will not be checked in more detail since it is not part of the design.

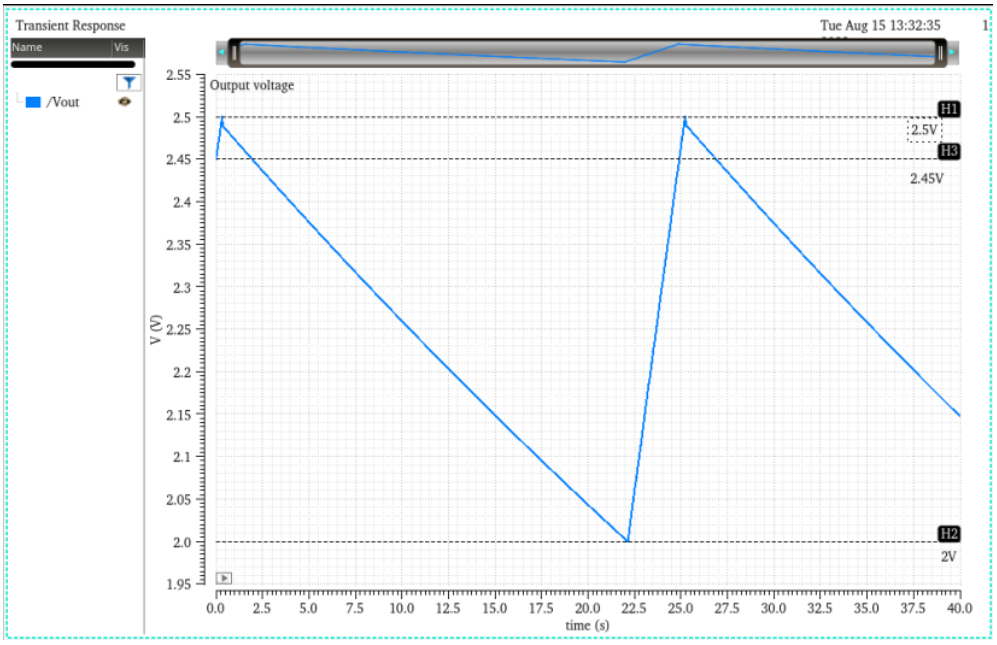


Figure 7.15: Verification result of the voltage-level detector

7.3.6. Start-up Voltage of Each Block

Table 7.6 summarizes the start-up voltage of every component. The start-up voltage is defined as the voltage at which the blocks start working steadily, so even though the circuits give some response at 250mV in Figure 7.12, 250mV is not the start-up voltage of those blocks, as the response is still vague and chaotic. The PTAT current stabilizes around 550mV, but the active-diode comparator can already start working with the unstabilized current from the current source. The zero-crossing detection will give an output as long as there is a falling edge on the comparator output, and the direction detection basically follows the zero-crossing detection. The pulse width of the ZCD and the SSHC pulse is not correct before the start-up voltage. The effect of the flipping process becomes visible at around 440mV for FF85 and TT27 and 780mV for SS-40 because of threshold voltage differences at different corners.

Table 7.6: Start-up voltage of the main components

	FF85	TT27	SS-40
Current source	452mV	567mV	688mV
active-diode comparator	180mV	290mV	600mV
Zero-crossing detector	200mV	270mV	590mV
Bootstrap	400mV	550mV	800mV
Flipping behaviour	420mV	440mV	780mV
Pulse generation	370mV	310mV	630mV
Direction detector	200mV	280mV	670mV

7.3.7. Minimum input power and frequency of the System

Although the target minimum input power is 1uW, it has been proven that the circuit can charge the storage capacitor higher than 2.5V in some cases. The minimum input power level of the circuit is summarized in this section. The complete result will be shown in Appendix A. Table A.1 shows the minimum required input power level for 1Hz and 10Hz excitation frequencies to reach 2.5V in the typical corner for parasitic capacitors from 100pF to 100nF. Depending on the relation between the source and load impedance, when the frequency increases, the required input power increases for parasitic capacitors smaller than 5nF or decreases when the parasitic capacitor is larger than 5nF.

The minimum input power for the worst case, FF85, is also simulated. Since the current consumption increases by approximately four times at FF85, the estimation 0is that the required input power will also increase by around four times. Table A.2 summarizes the minimum input power for 1Hz excitation frequency. The results show that the minimum input power increases by 2.5X to 5.76X, depending on the size of the parasitic capacitors. 10Hz excitation frequency is not further studied because it will follow the pattern of 1Hz excitation frequency.

The required frequency for 1uW input power to reach 2.5V is also determined for different parasitic capacitors at the typical corner. Figure A.3 summarizes the simulation result. The required frequency decreases for a bigger parasitic capacitor. When the parasitic capacitor is 25nF, the minimum frequency required to reach 2.5V is exactly 1Hz. Increasing the parasitic capacitors will require less power to reach 2.5V at 1Hz excitation frequency.

The minimum frequencies of 1uW input power for 100pF are calculated by Equation 5.2. Because the latency of the active-diode comparator and the time required for the flipping process take too much time during one cycle, the 2.5V output cannot be achieved by simulation.

7.4. Normal Operation Verification

The performance of the circuit is studied for normal operation. The circuit is verified after a long run to ensure the flying capacitors are charged to the maximum voltage.

7.4.1. Output Power

The feasibility of the cold-start circuit being used for normal harvesting is verified. The output power is measured by fixing the output voltage and measuring the output current at 1uW input power level and 10nF parasitic capacitor. Figure 7.16 prints the output power from the cold-start circuit, the power consumption of the circuit, and the output power from an ideal harvester with 67% flipping efficiency.

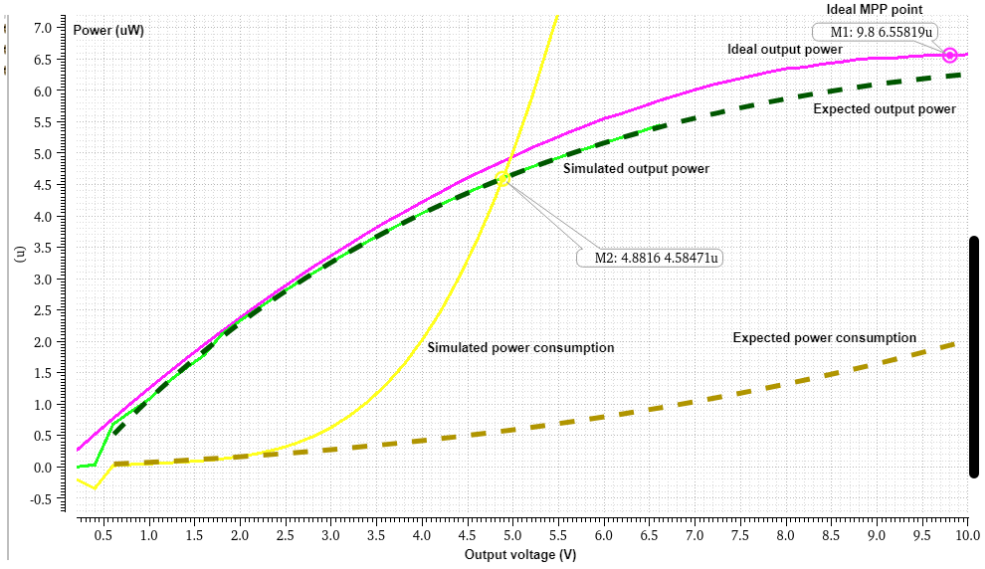


Figure 7.16: Simulated and expected output power and circuit's power consumption and the output power from an ideal circuit

In Equation 3.18, the theoretical maximum output point voltage can be calculated for a given input power, parasitic capacitor and flipping efficiency. For the given 1uW and 10nF input, the theoretical

maximum output voltage should occur at about 9.8V output voltage, and the output power is about 6.6uW. The results from the ideal circuit confirm the calculation result and the shape of the curve is quadratic. The theoretical maximum F.o.M is 5.8.

In the actual simulation, the output power increases with the output voltage, as the ideal circuit does. The actual output power is slightly smaller than the output power from an ideal circuit because of the multiple losses in the circuit. The shape of the proposed circuit also follows the shape of the ideal circuit. In general, the output power of the proposed circuit matches one of the ideal circuits.

Ideally, the power consumption of the circuit should increase slowly as the brown curve indicated with the supply voltage because a current reference should be relatively insensitive to the supply voltage. However, the PTAT current from the cold-start current source is no longer stable after the supply voltage exceeds 3.5V, and the current consumption increases rapidly as the yellow curve shows. When the output voltage is about 4.8V, the output power of the circuit is the same as the circuit's power consumption, so the maximum output voltage the circuit can support, with the 1uW input power and 10nF parasitic capacitor, is 4.8V. Considering the circuit is self-powered, the maximum output power occurs when the difference between the output power and power consumption of the circuit is maximal, which is when the output voltage is about 3V while the output power is 2.75uW.

7.4.2. Power-Consumption Breakdown

The consumption of the system is measured after the charging of the flying capacitor is completed. Table 7.7 summarizes the minimum, typical and maximum current consumption of each block. In the typical corner at 27°C, the circuit only consumes 128nA current. The maximum current consumption happens at FF85 for all blocks. The current consumption of the bootstrap and SSHC circuit increased the most because those circuits contain medium-VT-based inverters without any current limitation. The increment is mainly caused by the leakage current due to the high temperature at the FF corner and the short-circuit current of some logic gates.

Table 7.7: Power consumption breakdown

	Min	Typ	Max
Current source	19.77nA	26nA	32.61nA
active-diode comparator (include biasing)	21.55nA	34.09nA	77.85nA
Non-overlap clock generator	30.53nA	53.95nA	113.4nA
Bootstrap	1nA	1.3nA	60.656nA
SSHC (Pulse, sequence, bootstrap)	8.12nA	11.76nA	126.6nA
Single pulse	1.5nA	2.4nA	22.2nA
Zero-crossing detector	0.817nA	1.223nA	6.313nA
Direction detector	0.15nA	0.24nA	17.75nA
Sum	90.21nA	127.8nA	437.5nA

7.5. Layout and Extraction Result

Figure B.1 presents the layout of the circuit, the total area of the cold-start is 300μm*230μm, 0.7μm^2. The layout and extraction of two comparators, the current source and the cross-coupled rectifier are finished. The layouts of some blocks that were built with standard logic gates and the switches for the SSHC techniques are not finished. The connection between every component is not routed either.

Due to the time limitation, the extraction results of the finished circuits are only checked for a given supply voltage. The results show that the performance of these circuits changes slightly compared to the performance before the extraction. The current consumption increases by 5nA in the typical corner at 27°C. Therefore, the minimum input power level will increase a little, but the start-up from 1uW will not be affected.

7.6. Overview of the Test Results

This chapter shows the verification result of the cold-start circuit. It has been demonstrated that each sub-block can operate properly across supply voltages up to 2.5V, temperatures and process corners. The start-up gets easier with bigger parasitic capacitors, bigger input power, or higher frequency. The

worst case of the cold-start circuit is FF85 when the current consumption is increased approximately four times. The start-up requirement can be met for 1uW input power across all temperatures and corners for parasitic capacitors from 10nF to 100nF. 100pF and 1nF parasitic capacitors will require a higher input power at 10Hz, 2.2uW and 1.7uW respectively. The lowest required input power for 1Hz and 10Hz and the required frequency for 1uW input power in the typical corner is noted. The minimum input power for 1Hz at FF85 is measured as well. It turns out that the cold-start circuit can support an input power as low as 120nW for 10Hz and 100nF input. The current source can only provide stable current until 4V supply voltage. The circuit's maximum output voltage and maximum output power are greatly limited by the current source if the circuit is self-powered. Nevertheless, the circuit can meet the start-up requirements.

The verification results show the circuit achieves the lowest power consumption and area compared to other designs while maintaining the same flipping efficiency as other designs using the same number of flying capacitors.

8

Discussion

With the schematic design and verification finished, this chapter will review the design process and the results. First, the design process is discussed. Secondly, verification results that deviate from the expectation are evaluated. Finally, the result is compared to other designs, and some overall remarks on the cold-start circuit are given.

8.1. Design Result

Although the simulation results of the cold-start circuit pass the requirement in Table 5.2, the cold-start circuit is not verified through the actual measurement. The layout of the cold-start circuit is not completely finished by the time of writing. Simulation of the entire start-up process after the extraction will be hard to check because the storage capacitor will require at least 70 seconds of transient simulation on the simulator to reach 2.5V for minimum input power, and it already takes long enough before the extraction. However, the extraction of some of the key components shows that the parasitics will not affect the overall performance too much.

In addition, although the supporting frequency of the cold-start circuit covers the frequency of human movement as low as 1Hz, it will not perfectly simulate real-life vibration. The vibration from the actual human movement will not be a single-frequency sinusoidal movement. So, a much more complicated input is expected in the actual movement. Circuits will switch on and off more frequently; the voltage amplitude on the parasitic capacitor will also be different in every vibration. The multiple-frequency input might affect the SSHC technique's flipping behaviour. The effect of the non-idealities, for example, the latency of the comparator and the pulse width of the SSHC pulses, will also cause more issues with the vibration frequency changing. The possible solutions for this issue are implementing a mechanical filter that filters the harmonics or implementing the Adaptive Synchronized Switch Harvesting (ASSH) introduced in Chapter 3.6.7 that is particularly designed for multi-mode vibrations.

The simulated piezoelectric energy source is assumed to vary across a range of input power and parasitic capacitors. The performance of a commercial piezoelectric energy harvester needs to be verified with the cold-start circuit after the tape-out.

8.2. Verification Result

The verification has shown that the general performance of the cold-start circuit is good. Despite two input levels, 1uW input power with 100pF and 1nF parasitic capacitors, in Table 5.2 that are impossible to start up, the rest of the table has met the cold-start requirement. In the typical case, the minimum input powers required for 100pF and 1nF parasitic capacitors are 2.2uW and 1.7uW at 10Hz, respectively.

The mismatch results from the active-diode comparator show that the latency can go up to 6ms while the previously decided maximum latency is 5ms. The theoretical calculation shows that the efficiency of the SSHC flipping can still be maintained above 90% for 10Hz excitation frequency. And the impact of the latency decreases for lower frequencies. Measurement results are required to find the impact of the mismatch after the chip is manufactured.

The pulse width of the SSHC goes up to 60us at FF corner, 85°C. In total, the flipping period at FF85 will take 300us. For low vibration frequencies, this will not cause too severe issues. However,

the highest input frequency will be limited by the flipping period. The highest input frequency in the verification is kept to 200Hz to cover the frequency range of the main SSHC harvester.

There are undefined states for some of the circuits in specific corners and temperatures. However, these undefined states do not stop the start-up in all simulations and only exist for a very short period. The risk remains that the undefined state might stop the start-up in the actual measurement.

The pulses for the SSHC technique will have a single shot of the wrong pulse in the beginning, as seen in Figure 8.1. It is caused by the time for the discrete-time comparator to output the correct direction signal. The pulses for the SSHC technique are generated and sequenced immediately after the zero-crossing detection signal. However, the comparator requires several ns to give the correct output after the zero-crossing detection signal. When the pulses are sequenced in the first 51ns, the direction signal is still the signal from the last flipping. So, a wrong shot is given in the beginning. It will cause the first flying capacitor to charge the parasitic capacitor reversely, thereby decreasing the flipping efficiency.

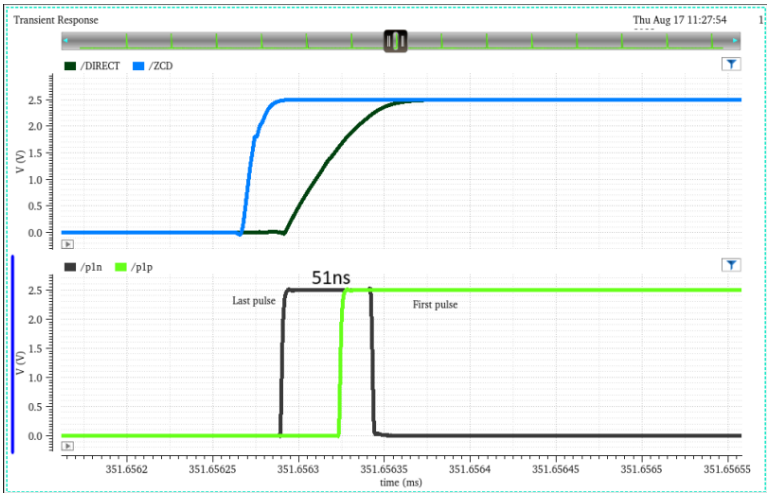


Figure 8.1: Beginning of the SSHC pulses

8.3. Comparison to Other Designs

Table 8.1 compares the proposed design to other designs. The Figure-of-Merit for PEH introduced in Chapter 3.5 is calculated. All efforts to reduce power consumption achieved a power consumption of 317nW, much lower than other designs. The power consumption of some designs is not indicated. Also, some designs require external supporting blocks, such as a biasing current or a voltage regulator. In contrast, even if all supporting blocks are included in this design, the area and the power consumption of the designed circuit are still much smaller.

The F.o.M is slightly lower than the F.o.M of the other SSHC designs. The main reason is that the circuit does not work at the theoretical maximum power point because the current source no longer provides a steady current after 3.5V. The circuit can only deliver maximum power at about 3V output voltage, while the actual maximum power point voltage should be around 9V. Nevertheless, the intention of the circuit is only to perform the cold-start, and it will not be hard to fix the issues in the current source.

Table 8.1: Comparison to other results

	[9]	[49]	[27]
Technique	SSHI (1mH)	31-phase SSHC	3-phase SSHC
Frequency	82Hz	1-200Hz	188Hz
Parasitic capacitor	69nF	1-100nF	22nF
Area	8.96mm^2	2.1mm^2	63.1mm^2
Cold-start	Yes (off-chip regulator)	No	Yes
Consumption	1.164uW	-	7uW
F.o.M	3.8-10	20	2.6-3.24
	[10]	[4]	This work
Technique	3/17-phase SSHC	21-phase SSHC	5-phase SSHC
Frequency	92Hz	200Hz	1-200Hz
Parasitic capacitor	45nF	22nF	100p-100nF
Area	2.9mm^2	710mm^2	0.07mm^2
Cold-start	No	No	Yes
Consumption	1.7uW	-	317nW
F.o.M	2.7-6.1	5.9-9.3	2.33

8.4. Discussion

There are still some remarks on the cold-start circuit. They will be given in the following paragraphs:

- Some circuit blocks give outputs that are zero or supply voltage at different corners when the output voltage starts rising. It is caused by the threshold voltage difference of NMOS and PMOS at different process corners. It will not affect the start-up because the active circuits are still not working yet, the behaviour of these circuits is not that important in the beginning.
- The flipping efficiency after a long run did not reach the theoretical maximum flipping efficiency due to some undesired behaviours. The major one is the wrong pulse at the beginning of the flipping process. Nevertheless, the cold-start circuit does not need the highest flipping efficiency to reach the 2.5V output voltage. Therefore, these undesired behaviours are acceptable in the cold-start scenario.
- The benefit of the SSHC technique changes reversely with the flipping efficiency. When there is a small parasitic capacitor, the charge wasted by the parasitic capacitor is also not too much. Even with a higher flipping efficiency, the not wasted charge from the flipping is little. For a large parasitic capacitor, although the flipping efficiency is lower, the not wasted charge from the SSHC technique is considerable. The flipping efficiency is not the most important performance indicator during a cold start. In addition, increasing the flipping efficiency does not outweigh the increase in consumption during the cold start and the increase in system complexity.
- The important features of the proposed circuit include low power consumption, being self-powered, and cold-start capability. Optimizing output power from the energy source is not the priority. The MPPT circuit is not included in the cold-start circuit because it is too big for a cold-start circuit and is already available in the main harvester. However, the traditional input power definition of a piezoelectric energy harvester assumes that impedance matching is guaranteed and this is not the case in the cold-start. An input power definition is proposed in this project that detaches the impact of the impedance matching by defining the input power on a fixed load impedance. The proposed input power definition is more suitable for cold-start applications and can be transmitted into the traditional definition flexibly.
- The simulation for the output power in normal operation assumes the ideal impedance matching. In comparison, some other designs use an actual matching circuit that might introduce tracking errors where the load impedance is not perfectly matched with the source impedance. The tracking error is not considered in this project.

9 Conclusions

This thesis project aims to design the cold-start circuit for a piezoelectric energy harvester. This chapter will summarize the thesis project, highlight the contributions made, and give recommendations to improve the performance further.

9.1. Overview

The thesis project starts with a literature study of various energy sources in energy harvesting. The energy harvesting of vibration energy on the human body is studied. Four mechanisms for kinetic energy harvesting, viz. Piezoelectric, triboelectric, electrostatic and magnetostatic. Piezoelectric energy harvesting is studied in more detail for its good adaptation to the CMOS technology, high energy density and mature commercial development. Vibrations found on the human body are low-frequency, normally below 10Hz. The power level can range from hundreds of nW to several mW. For the interest of the project, the minimum interested input power in this project is 1uW.

Next, the techniques for piezoelectric energy harvesting are studied. In general, the techniques can be split into two types: extracting more charge from the energy source and isolating the load impedance from the source impedance. The SSHC technique is better for compatibility with the integrated circuit and the current main harvester. The load isolation technique is not applied because it is less important for the cold-start application, and the area consumption is too much because this technique normally requires an inductor. The flying capacitors are selected to be 1uF to ensure optimum flipping efficiency and consistency with the main harvester.

Subsequently, the topology of the cold-start circuit is determined. A rectifier is mandatory because the mean values of the current and voltage from a piezoelectric energy source are zero. The cold-start circuit must be able to operate passively in the beginning when there is no power supply for the active circuit. The cross-coupled rectifier and an active diode will be used as the rectifier for the cold-start circuit. The body diode of the rectifier will be used to charge the storage capacitor when the storage capacitor is completely empty. The active circuits switch on when the output voltage reaches a certain level. The two-stage rectifier ensures both cold-start capability and low rectifier voltage drop. The SSHC technique will be added to extract more charge from the piezoelectric energy source to support the output current. The output current includes leakage current and active circuits' current. Thanks to the working principle of the active diode, simple but robust circuits are proposed to provide the direction and zero-crossing information for the SSHC technique. A falling-edge trigger of the comparator output is used as the zero-crossing detection. A discrete-time comparator is used for direction detection. The comparator is clocked by the falling-edge trigger and compares the voltage across the parasitic capacitor of the piezo element.

The designed cold-start circuit includes a Proportional To Absolute Temperature (PTAT) current source with self-cascode MOSFETs, a cross-coupled rectifier, an active diode with a folded-cascode comparator and its bootstrap circuit, pulse generation and sequencing circuits, a falling-edge trigger, a double-tail comparator and switches for the SSHC technique. The on-resistance of the active-diode switch balances the switch's conduction loss and the comparator's accuracy. The requirements on the comparator are derived from the impact of the latency of the falling edge on the efficiency of the SSHC

technique. The noise, mismatch and process-variation requirements are all included in the latency requirement. The requirements on the pulse-generation blocks are mainly about the pulse width. The delay cells are built with current-starved inverters to reduce the short-circuit current and the dynamic power. The design of the double-tail comparator is kept simple since the requirements are not high.

The cold-start circuit has a built-in SSHC technique without any voltage-level detector to control the switching of the SSHC circuits. A 2-flying-capacitor and 5-phase SSHC technique is used to balance the gained and consumed current in the FF corner at 85°C.

After the cold-start circuit is designed, a verification plan is set up for the circuit. An input-power definition is proposed for the cold-start scenario to detach the load mismatch from the input power. The requirements for the cold start are specified as charging the storage capacitor to at least 2.5V and supporting 500nA leakage current at 2.5V. The limitation of the cold start is essentially a balance between the input and output current.

The circuits designed have been tested by means of circuit simulations for various supply voltages, process corners, temperatures and mismatch conditions. The results show that the circuits can work properly across a wide range of supply voltages. The cold-start simulation results show that the circuit can do the cold-start successfully for various parasitic capacitors, frequencies and input power levels. The circuit will transit from a passive circuit to an active circuit during the start-up. The lowest input power is simulated for different parasitic capacitors and frequencies in the typical corner at 27°C and FF corner at 85°C. The input power level for a 10nF PEH parasitic capacitor to reach 2.5V output voltage can be as low as 0.5uW for 10Hz excitation frequency and 1.2uW for 1Hz excitation frequency in the typical corner and 27°C. The input power levels further decrease for larger parasitic capacitors. The circuit is also verified for the feasibility of normal harvesting. It turns out that the circuit's maximum output voltage is limited by the supply voltage range of the current source, but it does have the potential for normal harvesting.

In conclusion, the proposed cold-start circuit has met the requirements. The start-up ability of the circuit has been verified across different input power levels and frequencies. The simulation results show that the circuit can complete the cold-start task and has the potential to be further developed for normal harvesting.

9.2. Contributions

This section summarizes the contribution of this project to piezoelectric energy harvesting.

- Compared to other designs implementing the SSHC technique, the proposed circuit is cold-start capable and has the lowest current consumption while maintaining the flipping efficiency for the same number of flying capacitors.
- The SSHC technique is integrated with the cold-start circuit, eliminating the need for any voltage-level detectors to control the switching of the SSHC technique.
- The voltage at which the active circuit intervenes during startup is very low, about 500mV, which is the lowest operating voltage compared to other cold-start circuits used for piezoelectric energy harvesting.
- A novel detection mechanism for the SSHC technique is proposed. The proposed mechanism is simple in structure but robust, thanks to the working principle.
- The response of an active diode can be improved by increasing the on-resistance of the switch when the performance and the power consumption of the active diode comparator are limited.

9.3. Future Work

Some suggestions for further improvement of the cold-start circuit are given in this section, apart from the actual measurements after the chip has been manufactured.

- The circuit does have the potential to perform normal harvesting. An MPPT algorithm can be designed to optimize the power matching for normal harvesting. And the current source needs to be fixed to support a larger supply voltage.
- Additional flying capacitors can be utilized to increase the flipping efficiency for other input power levels and parasitic-capacitor values if the current gained is worth it.

- The short-circuit current at FF85 increased a lot. Current-limitation techniques or nominal-VT devices can be used to decrease the short-circuit current at the expense of start-up voltage.
- The mismatch and the performance of the active-diode comparator can still be further improved. The comparator is allowed to consume a bit more current to facilitate this.
- Currently, the pulse width is set to at least 10us to leave enough time for the flying capacitors and the parasitic capacitor to balance the charge. The simulation results show that the voltages of two capacitors are already balanced within 10us. It would be possible to decrease the pulse width in the SSHC technique.
- The short pulse spike at the beginning of the SSHC pulses, due to the response time of the discrete-time comparator, decreases the system performance. It can be fixed by adding a dead time before the pulse generation to wait for the correct output of the comparator.
- Using different flying-capacitor values in each stage can be studied to balance the maximum flipping efficiency and the time required to reach the maximum flipping efficiency.
- ESD protection and other protection circuitry are required to protect the circuit from high-voltage breakdown.
- Although the cold-start circuit passes all simulation tests, there may still be risks of unsuccessful start-up in large production. A low-voltage voltage-level detector might still be required to fix the initial condition of the components. However, this is not the intention of this project.
- The voltage-level detector in the current design only shuts down the cold-start circuit. A circuit is required to connect the energy source to the main harvester and disconnect the cold-start circuit simultaneously.

A

Boundary of the start-up

This appendix presents the minimum required input power for 1Hz and 10Hz excitation frequency of various parasitic capacitors at TT27 and FF85, respectively. Also, the required excitation frequency for 1uW input power of various parasitic capacitors at TT27.

A.1. Minimum input power for different frequencies at TT27

Table A.1: Minimum input power for different frequencies at typical corners

	Cp (nF)	fp (Hz)	Pin,min (uW)
TT27	0.1	1	1.70
		10	2.20
	0.6	1	1.60
		10	1.80
	1	1	1.55
		10	1.70
	5	1	1.50
		10	0.8
	25	1	1
		10	0.66
	10	1	1.20
		10	0.5
	50	1	0.7
		10	0.16
	100	1	0.4
		10	0.12

A.2. Minimum input power for 1Hz excitation frequency at FF85

Table A.2: Minimum input power for 1Hz frequency at FF85

	Cp (nF)	fp (Hz)	Pin,min (uW)
FF85	0.1	1	9.8
	0.6	1	9.2
	1	1	8.3
	5	1	7.7
	10	1	5.9
	25	1	4.2
	50	1	2.2
	100	1	1

A.3. Minimum input frequency for 1uW input power at TT27

Table A.3: Minimum excitation frequency for 1uW input power to reach 2.5V

	Cp (nF)	Pin (uW)	fp (Hz)
TT27	0.1	1	300*
	0.6		180
	1		80
	5		6
	10		2
	25		1

B

Layout

The layout of the cold-start will be presented in this appendix.

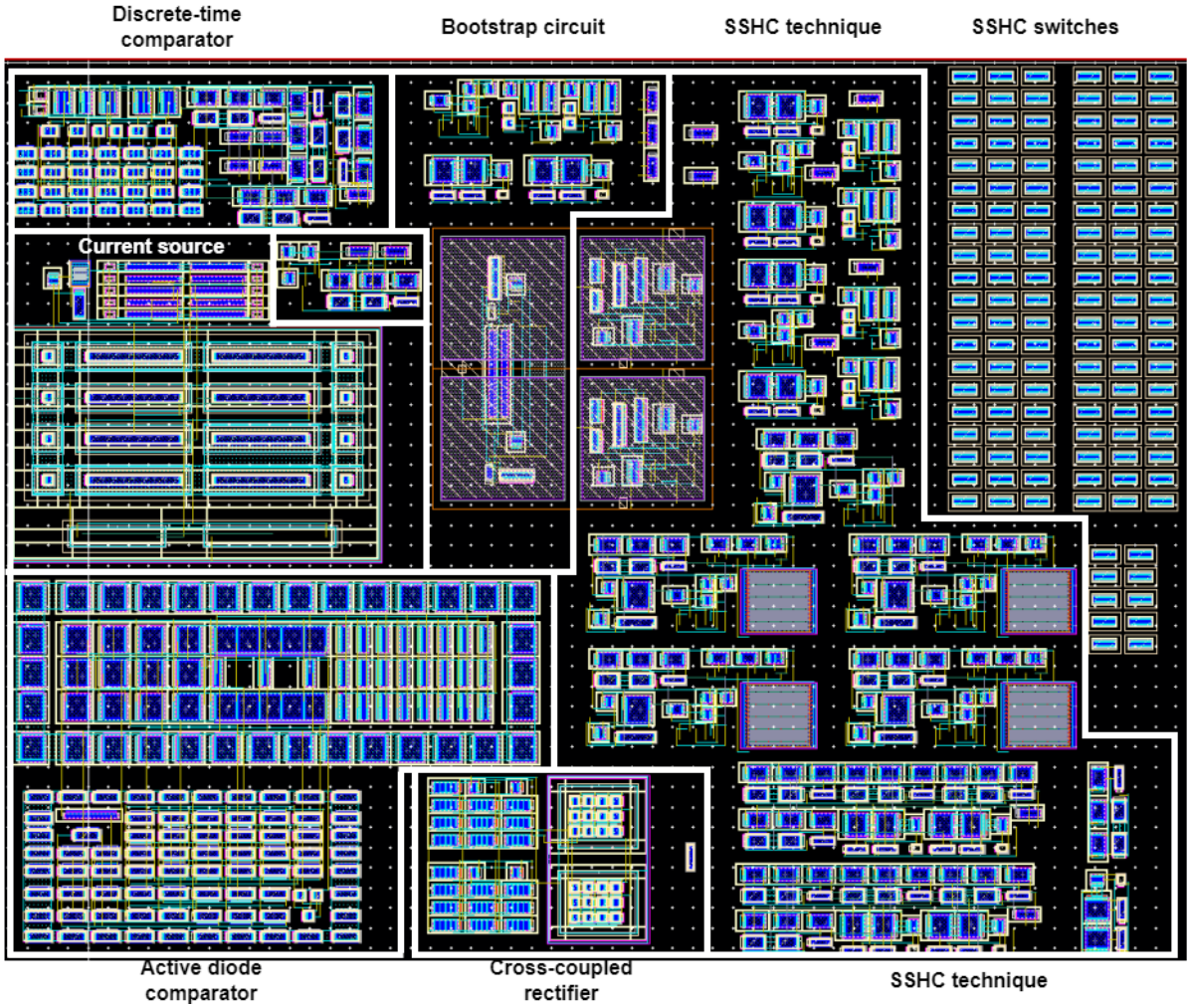


Figure B.1: Layout of the cold-start circuit

Bibliography

[1] Amay J. Bandodkar. “Soft, stretchable, high power density electronic skin-based biofuel cells for scavenging energy from human sweat”. In: *Energy Environ. Sci.* 10 (7 2017), pp. 1581–1589. DOI: 10.1039/C7EE00865A. URL: http://dx.doi.org/10.1039/C7EE00865A.

[2] Joe Briscoe. “Piezoelectric nanogenerators – a review of nanostructured piezoelectric energy harvesters”. In: *Nano Energy* 14 (2015). Special issue on the 2nd International Conference on Nanogenerators and Piezotronics (NGPT 2014), pp. 15–29. ISSN: 2211-2855. DOI: https://doi.org/10.1016/j.nanoen.2014.11.059. URL: https://www.sciencedirect.com/science/article/pii/S2211285514002663.

[3] Zhiyuan Chen. “22.2 A 1.7mm2 inductorless fully integrated flipping-capacitor rectifier (FCR) for piezoelectric energy harvesting with 483% power-extraction enhancement”. In: *2017 IEEE International Solid-State Circuits Conference (ISSCC)*. 2017, pp. 372–373. DOI: 10.1109/ISSCC.2017.7870416.

[4] Zhiyuan Chen. “Piezoelectric Energy-Harvesting Interface Using Split-Phase Flipping-Capacitor Rectifier With Capacitor Reuse for Input Power Adaptation”. In: *IEEE Journal of Solid-State Circuits* 55.8 (2020), pp. 2106–2117. DOI: 10.1109/JSSC.2020.2989873.

[5] Sphelar Power Corporation. *Sphelar Array F12 KSP-F12-*S*P-W1-X*. https://www.sphelarpower.com/product/pdf/datasheet_KSP-F12-xSxP-W1-X_v0912(E).pdf. Nov. 2022.

[6] M. Defosseux. “Highly efficient piezoelectric micro harvester for low level of acceleration fabricated with a CMOS compatible process”. In: *2011 16th International Solid-State Sensors, Actuators and Microsystems Conference*. 2011, pp. 1859–1862. DOI: 10.1109/TRANSDUCERS.2011.5969866.

[7] Francesco Dell’Anna. “State-of-the-Art Power Management Circuits for Piezoelectric Energy Harvesters”. In: *IEEE Circuits and Systems Magazine* 18.3 (2018), pp. 27–48. DOI: 10.1109/MCAS.2018.2849262.

[8] Sijun Du. “A Cold-Startup SSHI Rectifier for Piezoelectric Energy Harvesters With Increased Open-Circuit Voltage”. In: *IEEE Transactions on Power Electronics* 34.1 (2019), pp. 263–274. DOI: 10.1109/TPEL.2018.2815536.

[9] Sijun Du. “An Efficient SSHI Interface With Increased Input Range for Piezoelectric Energy Harvesting Under Variable Conditions”. In: *IEEE Journal of Solid-State Circuits* 51.11 (2016), pp. 2729–2742. DOI: 10.1109/JSSC.2016.2594943.

[10] Sijun Du. “An Inductorless Bias-Flip Rectifier for Piezoelectric Energy Harvesting”. In: *IEEE Journal of Solid-State Circuits* 52.10 (2017), pp. 2746–2757. DOI: 10.1109/JSSC.2017.2725959.

[11] Energy Education. *Photovoltaic effect*. Nov. 2022. URL: https://energyeducation.ca/wiki/index.php?title=Photovoltaic_effect&oldid=2120.

[12] Rui Feng. “Flexible, High-Power Density, Wearable Thermoelectric Nanogenerator and Self-Powered Temperature Sensor”. In: *ACS Applied Materials & Interfaces* 11.42 (2019), pp. 38616–38624. DOI: 10.1021/acsami.9b11435. URL: https://doi.org/10.1021/acsami.9b11435.

[13] Runar Finanger. *What is energy harvesting?* URL: https://www.onio.com/article/what-is-energy-harvesting.html.

[14] FlexSolarCells. *PowerFilm Solar Cell: SP3-12 Flexible Solar Panel 3V @ 12mA*. http://www.flexsolarcells.com/index_files/OEM_Components/Flex_Cells/specification_sheets/00_FlexSolarCells.com_PowerFilm_Solar_SP3-12_Specification_Sheet.pdf. Nov. 2022.

[15] Lauric Garbuio. “Mechanical Energy Harvester With Ultralow Threshold Rectification Based on SSHI Nonlinear Technique”. In: *IEEE Transactions on Industrial Electronics* 56.4 (2009), pp. 1048–1056. DOI: 10.1109/TIE.2009.2014673.

[16] P. Glynne-Jones. “Towards a piezoelectric vibration-powred microgenerator”. In: *Science, Measurement and Technology, IEE Proceedings* - 148 (Apr. 2001), pp. 68–72. DOI: 10.1049/ip-smt:20010323.

[17] Emanuele Guglielmi. “High-Value Tunable Pseudo-Resistors Design”. In: *IEEE Journal of Solid-State Circuits* 55.8 (2020), pp. 2094–2105. DOI: 10.1109/JSSC.2020.2973639.

[18] Miah A. Halim. “A non-resonant, frequency up-converted electromagnetic energy harvester from human-body-induced vibration for hand-held smart system applications”. In: *Journal of Applied Physics* 115.9 (2014), p. 094901. DOI: 10.1063/1.4867216. URL: https://doi.org/10.1063/1.4867216.

[19] Mengdi Han. “Coupling of Piezoelectric and Triboelectric Effects: from Theoretical Analysis to Experimental Verification”. In: *Advanced Electronic Materials* 1.10 (2015), p. 1500187. DOI: https://doi.org/10.1002/aelm.201500187. eprint: https://onlinelibrary.wiley.com/doi/pdf/10.1002/aelm.201500187. URL: https://onlinelibrary.wiley.com/doi/abs/10.1002/aelm.201500187.

[20] Xilong Kang. “Highly efficient pyroelectric generator for waste heat recovery without auxiliary device”. In: *Nano Energy* 88 (2021), p. 106245. ISSN: 2211-2855. DOI: https://doi.org/10.1016/j.nanoen.2021.106245. URL: https://www.sciencedirect.com/science/article/pii/S2211285521005000.

[21] Dong Wook Kim. “Material aspects of triboelectric energy generation and sensors”. In: *NPG Asia Materials* 12.1 (Jan. 2020), p. 6. ISSN: 1884-4057. DOI: 10.1038/s41427-019-0176-0. URL: https://doi.org/10.1038/s41427-019-0176-0.

[22] Min-Ki Kim. “Wearable thermoelectric generator for harvesting human body heat energy”. In: *Smart Materials and Structures* 23.10 (Sept. 2014), p. 105002. DOI: 10.1088/0964-1726/23/10/105002. URL: https://dx.doi.org/10.1088/0964-1726/23/10/105002.

[23] Sun Jin Kim. “A wearable thermoelectric generator fabricated on a glass fabric”. In: *Energy Environ. Sci.* 7 (6 2014), pp. 1959–1965. DOI: 10.1039/C4EE00242C. URL: http://dx.doi.org/10.1039/C4EE00242C.

[24] Michail Kiziroglou. “Non-resonant electrostatic energy harvesting from a rolling mass”. In: July 2008, pp. 318–321. DOI: 10.1109/ISSMDBS.2008.4575083.

[25] Ali Kubba. “A Comprehensive Study on Technologies of Tyre Monitoring Systems and Possible Energy Solutions”. In: *Sensors (Basel, Switzerland)* 14 (June 2014), pp. 10306–10345. DOI: 10.3390/s140610306.

[26] Lianhui Li. “Moisture-Driven Power Generation for Multifunctional Flexible Sensing Systems”. In: *Nano Letters* 19.8 (2019). PMID: 31348665, pp. 5544–5552. DOI: 10.1021/acs.nanolett.9b02081. URL: https://doi.org/10.1021/acs.nanolett.9b02081.

[27] Lianxi Liu. “A 1.5-Cycle Fast Sampling P-SSHC Piezoelectric Energy Harvesting Interface”. In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 69.9 (2022), pp. 3724–3728. DOI: 10.1109/TCSII.2022.3181263.

[28] Yuchi Liu. “Piezoelectric energy harvesting for self-powered wearable upper limb applications”. In: *Nano Select* 2.8 (2021), pp. 1459–1479. DOI: https://doi.org/10.1002/nano.202000242. URL: https://onlinelibrary.wiley.com/doi/abs/10.1002/nano.202000242.

[29] IXYS KOREA LTD. *IXOLARTM High Efficiency SolarBIT*. https://ixapps.ixys.com/DataSheet/KXOB22-12X1F_Nov16.pdf. Nov. 2022.

[30] Y Naruse. “Electrostatic micro power generation from low-frequency vibration such as human motion”. In: *Journal of Micromechanics and Microengineering* 19.9 (Aug. 2009), p. 094002. DOI: 10.1088/0960-1317/19/9/094002. URL: https://dx.doi.org/10.1088/0960-1317/19/9/094002.

[31] NASA. *Electromagnetic spectrum*. May 2015. URL: https://www.nasa.gov/directorates/heo/scan/spectrum/txt_electromagnetic_spectrum.html.

[32] Prusayon Nintanavongsa. “Design Optimization and Implementation for RF Energy Harvesting Circuits”. In: *IEEE Journal on Emerging and Selected Topics in Circuits and Systems* 2.1 (2012), pp. 24–33. DOI: 10.1109/JETCAS.2012.2187106.

[33] Simiao Niu. “A universal self-charging system driven by random biomechanical energy for sustainable operation of mobile electronics”. In: *Nature Communications* 6.1 (Dec. 2015), p. 8975. DOI: 10.1038/ncomms9975. URL: https://doi.org/10.1038/ncomms9975.

[34] Dmitry Pankratov. “Ex vivo electric power generation in human blood using an enzymatic fuel cell in a vein replica”. In: *RSC Adv.* 6 (74 2016), pp. 70215–70220. DOI: 10.1039/C6RA17122B. URL: http://dx.doi.org/10.1039/C6RA17122B.

[35] Giuseppe Papotto. “A 90-nm CMOS Threshold-Compensated RF Energy Harvester”. In: *IEEE Journal of Solid-State Circuits* 46.9 (2011), pp. 1985–1997. DOI: 10.1109/JSSC.2011.2157010.

[36] F. Pathan. “Kinetic Energy Harvesting from Human Hand Movement by Mounting micro Electromagnetic Generator”. In: *E3S Web of Conferences* 115 (Jan. 2019), p. 02005. DOI: 10.1051/e3sconf/201911502005.

[37] M. Toyabur Rahman. “A highly miniaturized freestanding kinetic-impact-based non-resonant hybridized electromagnetic-triboelectric nanogenerator for human induced vibrations harvesting”. In: *Applied Energy* 279 (2020), p. 115799. ISSN: 0306-2619. DOI: https://doi.org/10.1016/j.apenergy.2020.115799. URL: https://www.sciencedirect.com/science/article/pii/S0306261920312812.

[38] Wei Ren. “High-performance wearable thermoelectric generator with self-healing, recycling, and Lego-like reconfiguring capabilities”. In: *Science Advances* 7.7 (2021), eabe0586. DOI: 10.1126/sciadv.abe0586. URL: https://www.science.org/doi/abs/10.1126/sciadv.abe0586.

[39] M. Renaud. “Scavenging energy from human body: design of a piezoelectric transducer”. In: *The 13th International Conference on Solid-State Sensors, Actuators and Microsystems, 2005. Digest of Technical Papers. TRANSDUCERS ’05.* Vol. 1. 2005, 784–787 Vol. 1. DOI: 10.1109/SENSOR.2005.1496534.

[40] Sarah Risquez. “Design of a 3D multilayer out-of-plane overlap electrostatic energy harvesting MEMS for medical implant applications”. In: *2015 Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS (DTIP)*. 2015, pp. 1–5. DOI: 10.1109/DTIP.2015.7160963.

[41] Changxiang Shao. “Wearable fiberform hygroelectric generator”. In: *Nano Energy* 53 (2018), pp. 698–705. ISSN: 2211-2855. DOI: https://doi.org/10.1016/j.nanoen.2018.09.043. URL: https://www.sciencedirect.com/science/article/pii/S2211285518306876.

[42] Rahul Shukla. “Towards the development of efficient low frequency piezoelectric energy harvesters”. In: *2010 IEEE International Symposium on the Applications of Ferroelectrics (ISAF)*. 2010, pp. 1–4. DOI: 10.1109/ISAF.2010.5712228.

[43] Hyun-Cheol Song. “Ultra-Low Resonant Piezoelectric MEMS Energy Harvester With High Power Density”. In: *Journal of Microelectromechanical Systems* 26.6 (2017), pp. 1226–1234. DOI: 10.1109/JMEMS.2017.2728821.

[44] M. Stoopman. “A self-calibrating RF energy harvester generating 1V at −26.3 dBm”. In: *2013 Symposium on VLSI Circuits*. 2013, pp. C226–C227.

[45] Mark Stoopman. “Co-Design of a CMOS Rectifier and Small Loop Antenna for Highly Sensitive RF Energy Harvesters”. In: *IEEE Journal of Solid-State Circuits* 49.3 (2014), pp. 622–634. DOI: 10.1109/JSSC.2014.2302793.

[46] Hucheng Sun. “Design of a High-Efficiency 2.45-GHz Rectenna for Low-Input-Power Energy Harvesting”. In: *IEEE Antennas and Wireless Propagation Letters* 11 (2012), pp. 929–932. DOI: 10.1109/LAWP.2012.2212232.

[47] Panu Thainiramit. “Impact-Driven Energy Harvesting: Piezoelectric Versus Triboelectric Energy Harvesters”. In: *Sensors* 20.20 (2020). ISSN: 1424-8220. URL: https://www.mdpi.com/1424-8220/20/20/5828.

[48] Cam Minh Tri Tien. “Use of a Piezocomposite Generating Element in Energy Harvesting”. In: *Journal of Intelligent Material Systems and Structures* 21.14 (2010), pp. 1427–1436. DOI: 10.1177/1045389X10381658. eprint: https://doi.org/10.1177/1045389X10381658. URL: https://doi.org/10.1177/1045389X10381658.

[49] Joram van der Velden. “Single-Channel Heterogeneous-Source Energy Harvesting PMIC Design”. en. MA thesis. Delft: Delft University of Technology, Aug. 2021.

[50] Maisam Wahbah. “Characterization of Human Body-Based Thermal and Vibration Energy Harvesting for Wearable Devices”. In: *IEEE Journal on Emerging and Selected Topics in Circuits and Systems* 4.3 (2014), pp. 354–363. DOI: 10.1109/JETCAS.2014.2337195.

[51] Changsheng Wu. “Triboelectric Nanogenerator: A Foundation of the Energy for the New Era”. In: *Advanced Energy Materials* 9.1 (2019), p. 1802906. DOI: https://doi.org/10.1002/aenm.201802906. URL: https://onlinelibrary.wiley.com/doi/abs/10.1002/aenm.201802906.

[52] Zehao Wu. “Design and Testing of a New Energy Harvester with Single Piezo-Stack for Pull and Push Input”. In: *2018 IEEE International Conference on Information and Automation (ICIA)*. 2018, pp. 1268–1273. DOI: 10.1109/ICInfA.2018.8812529.

[53] Guobin Xue. “Water-evaporation-induced electricity with nanostructured carbon materials”. In: *Nature Nanotechnology* 12.4 (Apr. 2017), pp. 317–321. ISSN: 1748-3395. DOI: 10.1038/nnano.2016.300. URL: https://doi.org/10.1038/nnano.2016.300.

[54] Hao Xue. “A wearable pyroelectric nanogenerator and self-powered breathing sensor”. In: *Nano Energy* 38 (2017), pp. 147–154. ISSN: 2211-2855. DOI: https://doi.org/10.1016/j.nanoen.2017.05.056. URL: https://www.sciencedirect.com/science/article/pii/S2211285517303440.

[55] Ya Yang. “Pyroelectric Nanogenerators for Harvesting Thermoelectric Energy”. In: *Nano Letters* 12.6 (2012), pp. 2833–2838. DOI: 10.1021/nl3003039. URL: https://doi.org/10.1021/nl3003039.

[56] You Yu. “Biofuel-powered soft electronic skin with multiplexed and wireless sensing for human-machine interfaces”. In: *Science Robotics* 5.41 (2020), eaaz7946. DOI: 10.1126/scirobotics.aaz7946. URL: https://www.science.org/doi/abs/10.1126/scirobotics.aaz7946.

[57] Xinling Yue. “Voltage Flip Efficiency Optimization of SSHC Rectifiers for Piezoelectric Energy Harvesting”. In: *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2021, pp. 1–5. DOI: 10.1109/ISCAS51556.2021.9401330.

[58] Yang Zou. “Recent progress in human body energy harvesting for smart bioelectronic system”. In: *Fundamental Research* 1.3 (2021), pp. 364–382. ISSN: 2667-3258. DOI: https://doi.org/10.1016/j.fmre.2021.05.002. URL: https://www.sciencedirect.com/science/article/pii/S2667325821000698.