Delft University of Technology

Faculty of Electrical Engineering, Mathematics and
Computer Science

Optimization of heterojunction c-Si solar cells with front junction architecture

by

Camilla Massacesi

TU Delft

MSc Thesis

Optimization of heterojunction c-Si solar cells with front junction architecture

by

Camilla Massacesi

to obtain the degree of Master of Science in Sustainable Energy Technology
at the Delft University of Technology,
to be defended publicly on Thursday October 5, 2017 at 9:30 AM.

Student number:	4512308
Project duration:	October 25, 2016 – October 5, 2017
Supervisors:	Dr. O. Isabella,
	Dr. G. Yang
Assessment Committee:	Prof. dr. M. Zeman,
	Dr. M. Mastrangeli,
	Dr. O. Isabella,
	Dr. G. Yang

TU Delft

I know I will always burn to be
The one who seeks so I may find
The more I search, the more my need
Time was never on my side
So you remind me what left this outlaw torn.

Abstract

Wafer-based crystalline silicon (c-Si) solar cells currently dominate the photovoltaic (PV) market with high-thermal budget (T > 700 $^{\circ}C$) architectures (e.g. i-PERC and PERT). However, also low-thermal (T < 250 $^{\circ}C$) budget heterojunction architecture holds the potential to become mainstream owing to the achievable high efficiency and the relatively simple lithography-free process. A typical heterojunction c-Si solar cell is indeed based on textured n-type and high bulk lifetime wafer. Its front and rear sides are passivated with less than 10-nm thick intrinsic (i) hydrogenated amorphous silicon (a-Si:H) and front and rear side coated with less than 10-nm thick doped a-Si:H layers. Finally, transparent conductive oxide (TCO) and metal at both front and rear side terminate the device. Of course, the front side metal is merely a grid, allowing light to impinge on the c-Si wafer. In this project, an HIT heterojunction architecture is investigated, it is used a *double intrinsic* passivating layer at the front and an highly hydrogenated (p) a-Si:H forming the emitter; i/n passivating stack at the rear in the role of back surface field; a TCO formed by $IO{:}H$ and ITO and finally copper as front metal contact.

Contents

1 Introduction **1**
- 1.1 The different PV technologies . . . 1
- 1.2 Theoretical background on heterojunction solar cells . . . 2
  - 1.2.1 Silicon heterojunction with intrinsic thin layer HIT . . . 2
  - 1.2.2 The photovoltaic effect . . . 3
  - 1.2.3 Losses and recombination mechanisms . . . 5
  - 1.2.4 Surface passivation technique . . . 7
  - 1.2.5 Band diagram analysis and carrier transport . . . 8
- 1.3 State of the art of c-Si based solar cell . . . 9
- 1.4 Thesis motivations . . . 10
- 1.5 Scientific questions and structure of the thesis . . . 11

2 Cell Fabrication Process and Characterization **13**
- 2.1 Overview of SHJ baseline process flow . . . 13
- 2.2 Wafer pre-deposition treatments . . . 14
- 2.3 Plasma enhanced chemical vapor deposition . . . 15
- 2.4 Transparent conductive oxide sputtering . . . 16
- 2.5 Metallization . . . 16
- 2.6 Solar cell characterization . . . 18

3 Pre-Deposition Treatments Experiments **23**
- 3.1 Introduction and motivation . . . 23
- 3.2 Experiment setup . . . 24
- 3.3 Wafer texturization and cleaning . . . 25
- 3.4 PECVD conditioning and sample’s holder cleaning . . . 27
- 3.5 Conclusions . . . 29

4 Passivation and Precursor of the Solar Cell Experiments **31**
- 4.1 Experiment set up . . . 32
- 4.2 Passivating layer (i) a-Si:H . . . 33
  - 4.2.1 Introduction and motivation . . . 33
  - 4.2.2 Deposition parameters . . . 34
  - 4.2.3 Application of seed layer . . . 37
- 4.3 Front emitter ((i) a-Si:H / (p) a-Si:H) . . . 38
  - 4.3.1 Introduction and motivation . . . 39
  - 4.3.2 Deposition parameters . . . 40
- 4.4 Back surface field ((i) a-Si:H / (n) a-Si) . . . 48
  - 4.4.1 Optimization of a-Si layers thicknesses . . . 50

4.5 Conclusions 51

5 Front and Back-end Fabrication Process Experiments 53

5.1 Experiment set up 53

5.2 Transparent Conductive Oxide 55

5.2.1 Introduction and Motivation 55

5.2.2 $IO{:}H$-ITO double TCO layer as alternative to ITO single layer 56

5.2.3 Backside TCO influence 59

5.3 Metallization 61

5.3.1 Introduction and motivation 61

5.3.2 Front metallization 62

5.3.3 Back metallization 64

5.4 Conclusions 66

6 Conclusions and Outlook 69

6.1 Outlook 70

Bibliography 73

1

Introduction

1.1. The different PV technologies

Photovoltaic (PV) technologies are gaining importance among the energy sources thanks to the economic competitiveness, the issue related to the exhaustion of oil and gas reserves and the fear for climate change.

The current PV market consists of a wide range of technologies, among which there can be identified two main families: c-Si based solar cells, also referred as *first generation* PV technology and thin film based solar cells, also referred as *second generation*. Besides them, new emerging technologies include dye-sensitized, organic cells and quantum dots, which, however, are still under research stage. It is important to note that c-Si based solar cells are the mainstream PV technology with 94% of the market share (in 2016), while the remaining 6% is accounted for thin film [1].

A further subdivision can be made among c-Si solar cells: monocrystalline (mono c-Si) or polycrystaline (poly or multi c-Si) solar cells. The wafers are about 100-300 μm thick and the power conversion efficiencies range between 15% to 25%. The main differences between mono and multi c-Si rely on the higher quality of the mono c-Si wafer, which, on one side allows to reach higher efficiency, but on the other side it entails higher expenses due to the fabrication procedure.

Since the announcement of the first silicon solar cell realized in 1954 [2], the power conversion efficiency continuously increased. Over the decades the performances of c-Si cells have been extensively improved thanks to progress made in the design, architecture, material properties and processing (see figure 1.1). Nowadays, *Kaneka Corp.* holds the world record for c-Si solar cell with a power conversion efficiency of 26.6% [3].

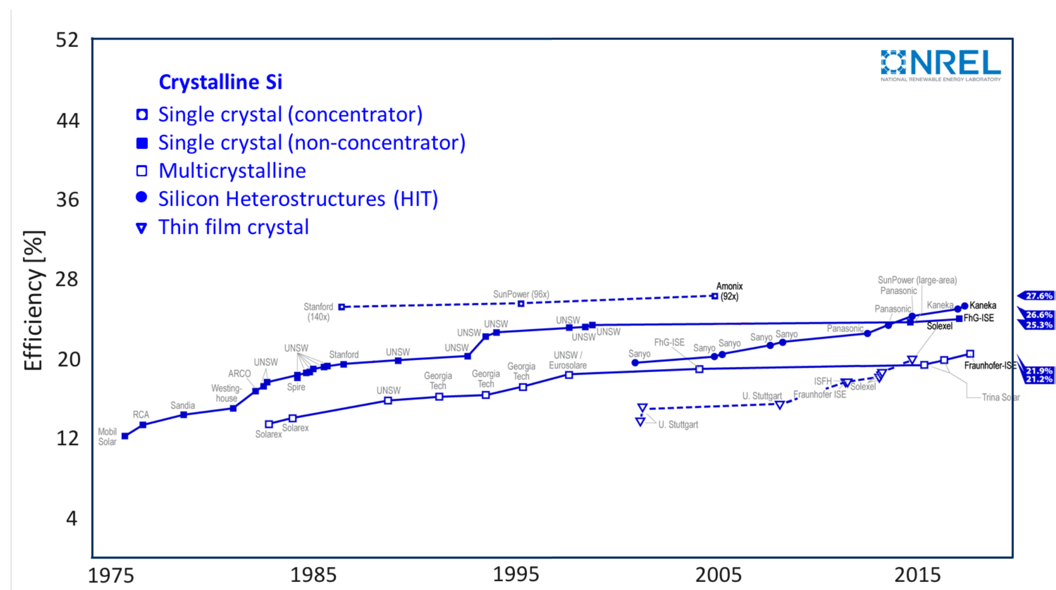


Figure 1.1 – History of confirmed best laboratory c-Si based cell efficiencies extracted from [4].

1.2. Theoretical background on heterojunction solar cells

This thesis work focuses on a specific high efficiency concept of the mono c-Si family: the cristalline silicon *heterojunction* solar cell with *intrinsic thin layer* (HIT) and with a standard front and back metallization. The same concept, but with the *interdigitated back contacts* (IBC) architecture was used by *Kaneka Corp.* to achieve the world record for c-Si [3]. However, the actual record for HIT solar cell with front and back contacts is held by *Sanyo Electric Co.* with 24.7% of power conversion efficiency [5].

This section serves to introduce the fundamentals to understand the c-Si PV solar cell, focusing on the SHJ and HIT concepts. Therefore, we deal with the working principle, losses and recombination mechanisms, surface passivation and carrier transport mechanism. Afterwards, in section 1.3 the state of the art of high efficiency concepts based on c-Si is introduced.

1.2.1. Silicon heterojunction with intrinsic thin layer HIT

Figure 1.2 shows the general layout of a HIT solar cell. The silicon heterojunction (SHJ) is formed by n-type float zone c-Si wafer and hydrogenated amorphous silicon (a-Si:H). The two materials differ in having different crystallographic structures and different bandgaps. As explained in the next section, a SHJ cell has two junctions: one at the front side where a (p) doped a-Si layer will act as emitter and force the holes to move toward the front contact; the other junction at the back side, where a (n) doped a-Si layer will force the electrons to move toward the back contact.

In a HIT cell, a thin layer of intrinsic a-Si:H layer is deposited between the c-Si and the doped a-Si layer. This layer passivates the dangling bonds at the junction, where most of the charge carriers recombination take place. The passivation mechanism is further explained in section 1.2.4.

An important difference of SHJ with respect to a homojunction is the presence of a transparent conductive oxide (TCO) material which is responsible for lateral diffusion of charge carriers to the contact. This cannot be done directly by the emitter layer ((p) a-Si) since it has poor lateral conductivity. The TCO layer acts also as anti-reflective coating. The remarkable advantage of SHJ technology is the low

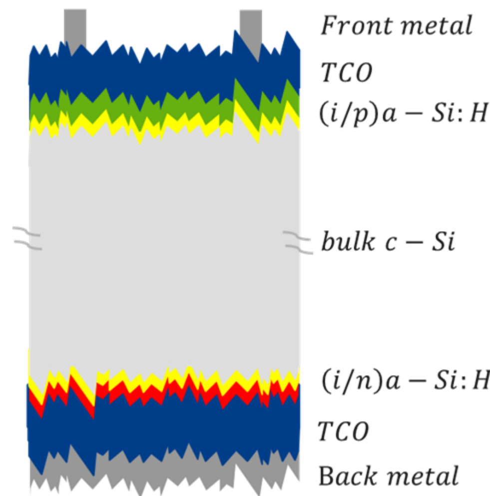


Figure 1.2 – HIT solar cell structure.

temperature fabrication deposition of front and back surface fields with the plasma enahnced chemical vapour deposition (PECVD) technique, which is further explained in section 2.3 [6].

1.2.2. The photovoltaic effect

Photovoltaics is the direct conversion of light into electricity. It relies on the capability of some materials to absorb light (photons) and release electrons. When an external load is applied, current flows in the closed circuit.

The working principle of the solar cell is the following: when a photon, particle of light, is incident on Si with an energy sufficienctly high (E_{ph}>$E_{g,Si}$), it will be absorbed and create the electron-hole pair, which is free to move into the Si lattice.

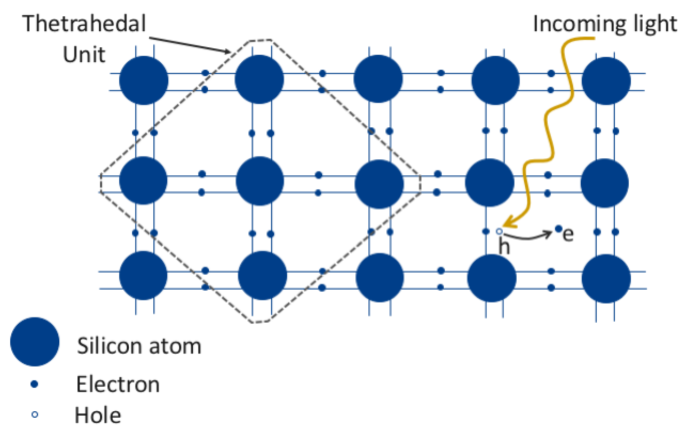


Figure 1.3 – Photons with enoigh energy (E_{ph}>1.12eV) can generate an electron-hole pair, which is free to move in the crystal.

The electrons and holes would randomly move in the crystal and after a certain time, called relaxation time, they would loose their energy and fall back to the initial position. To use their energy it is necessary to produce an electric field. This field induce a potential barrier which will block one type of

carrier and allow the other to flow though it. In the classical mono-junction cell, this is performed by altering the crystallographic structure of the silicon. Specifically, it is done by connecting two materials which present n-type and p-type doping. To make a n-type silicon, impurities atoms with five valence electrons (e.g. phosphorous), can be put in place of a silicon atom. The phosphorous atom has an extra electron with respect to the silicon (which has four valence electrons) and it is not coupled with a hole, making it free to move. Similarly, a silicon atom can be replaced with an impurity atom with three valence electrons (e.g. boron), this would generate a free-hole and form a p-type silicon.

When the n-type and p-type materials are put in contact they will form a *pn junction*. Initially, when the junction is forming, due to the abundance of electrons in the n-type material and leakage of electrons in the p-type material, the electrons will start moving by diffusion from the n-type material toward the p-type material and will fill the holes. A positive charge builds up on the n-side of the junction because of the loss of electrons. Similarly, majority carriers holes in the p region will diffuse into the n region leaving negatively charged boron atoms at the edge of the contact [7].

The junction is now formed and the situation is the following: most of the free electrons in the n-region already moved in the p-region, leaving a large positive charge at the junction. Opposite situation happen for free holes: a negative charge is formed at the junction because of the movement of free holes toward the n-side to fill the voids. Charged carriers that have already crossed the junction set up an electric force (field) that acts as a barrier opposing the further flow of free carriers and creating a potential barrier at the junction, defined as V_{bi}. The electric field opposes the diffusion of majority carriers, however minority carriers are not blocked by the barrier, therefore free electrons on the p-region are driven by the electric field toward the n-region.

Figure 1.4 shows the selective barrier at the junction. Under no illumination, there are very few minority carriers and their movement is null, hence there is thermal equilibrium condition.

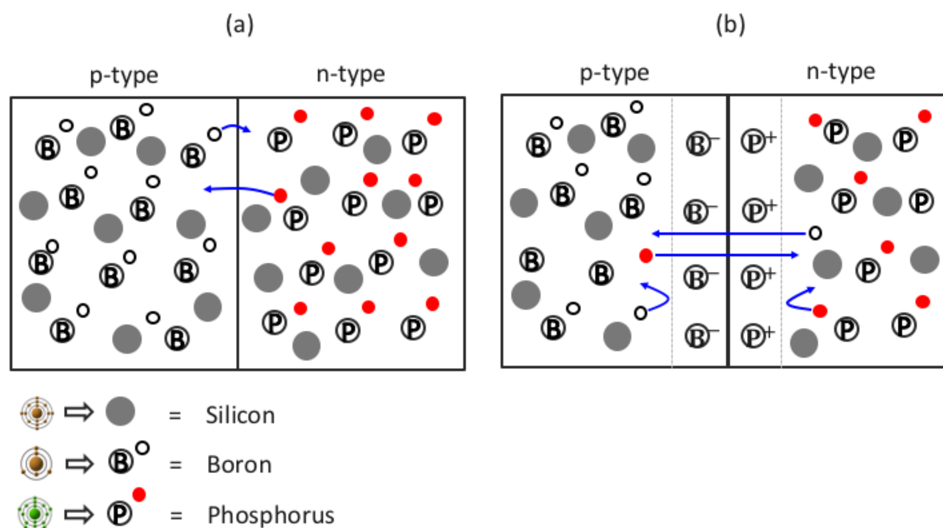


Figure 1.4 – (a) *pn junction* formation: diffusion of majority carriers and creation of fixed charge at the junction. (b) *pn junction* formed: it present a barrier for majority carriers (electrons to n-region and for holes to p-region) but does not hinder minority carriers crossing.

When the *pn junction* is illuminated additional electron-holes pairs are generated. Assuming low injection level, the concentration of majority carriers does not change much, while the concentration

of minority carriers heavily increases, leading the minority carriers to flow across the junction. For example, if an electron-hole pair is generated in the n-type side of the junction, the free electron is repelled by the barrier, while the hole is drifted through the junction toward the p-side. However, the thickness of the n-side has to be thin enough to allow the hole to reach the junction before recombining. Once in the p-side, the hole is free since there are few electrons with which recombining. Thanks to illumination and charge separation there is now an excess of holes in the p-side region and an excess of electrons in the n-type region.

The (separated) charge carriers can be extracted from the solar cell by applying an external load which lets electrons flow through an external circuit. In this way electrons are used to produce electric energy. Finally, after that the electrons pass through the external circuit, then they flow in the p-type material where they recombine with holes [8].

In homojunction solar cells two *pn junctions* are formed: (i) boron doped (p) c-Si with n-type c-Si substrate, and (ii) phosphorous doped (n) c-Si layer with (low doped) n-type c-Si substrate. In heterojunction solar cells two *pn junctions* are formed: (i) p-type a-Si layer with n-type c-Si substrate, where the (p) a-Si acts as hole selective contact and (ii) n-type a-Si layer with n-type c-Si substrate, where the (n) a-Si acts as electron selective contact.

SHJ have the potential to overcome one main efficiency limitation of the homojunction contact: the high recombination between the *direct contact* metal-silicon, which, in a standard c-Si solar cell, account for around 50% of the overall recombination losses [9]. Metals have high recombination velocity, so high recombination take place if similar concentration of electrons and holes is present. If a selective material is inserted close to the metal surface, there will be only one charge carrier type and the surface recombination will be highly decreased.

In SHJ cells the selectivity of carrier is enhanced by the different bandgaps and band offset between the a-Si and the c-Si materials. On the junction between the (n) c-Si / (p) a-Si:H the minority charge carriers (holes) will tunnel across the barrier. On the opposite the majority charge carriers (electrons) will see a further increased barrier due to ΔE_c which will block them to pass toward the (p) a-Si. A similar junction is made at the opposite side of the c-Si where an (n) doped a-Si layer is inserted and will act as electron selective contact, so the junction will permits only to electrons to pass through it.

1.2.3. Losses and recombination mechanisms

SHJ solar cell losses can be divided into two main categories:

1. **Optical losses** decrease the performances of a solar cell by lowering the short-circuit current. They can be divided into two main categories:

   (a) *Spectral utilization*. The J_{sc} is determined by the bandgap of the material. The c-Si has a bandgap of 1.12 eV which correspond to a photon with a wavelength of 1107 nm. Figure 1.5 shows that photons with energy less than E_g do not generate electron-holes pairs, while photons with higher energy are absorbed and the excess energy ($E_{ph} - E_g$) is dissipated by thermalization.

   All the layers above the absorber layer are mainly responsible for optical losses in a SHJ solar cell, because of the optical properties of these material, hence the capability of reflecting or absorbing light, which then cannot reach the absorber layer. Those losses are the reflection of front metal grid line and the parasitic absorption of metal, TCO and a-Si layers. Attention

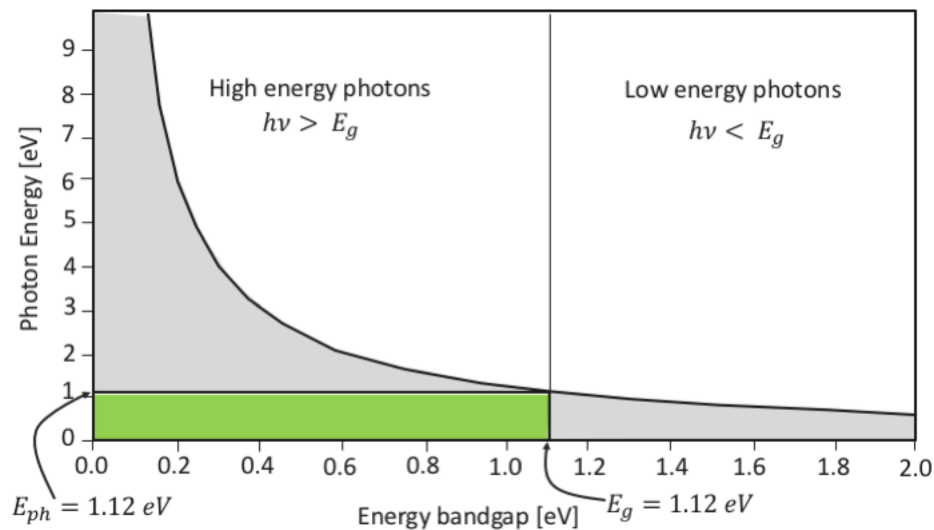


Figure 1.5 – Photons with energy above 1.12 eV don't have enough energy to excite an electron to the conduction band and this energy is lost, photons with higher energy (hence short wavelength) have enough energy to be absorbed, however the energy about 1.12 eV is lost as well in the form of thermalization.

has to be paid when designing front metal patter because this will constitute a shading loss.

(b) *Optical properties* of the materials (absorbance, trasmittance, reflectance): when light arrives at the interface between two material (e.g. air and silicon) a part of the incident light is lost by reflection. The part of the light that penetrates into the material can be either absorbed, this determines the photogenerated current, or transmitted. The latter is an additional loss caused by the limited thickness of the absorber layer. On the respect of optical properties two design choices are of crucial importance in SHJ: first, the use of TCO layer, which acts as antireflective coating; second, a proper texturization which enhances multiple hitting of light and reduce reflections.

2. **Electrical losses**:

   (a) *Recombination losses* due to the recombination of generated carriers can reduce solar cell performances by lowering the V_{oc}. Recombination can take place in the bulk of the c-Si or at the interface between c-Si and a-Si. On this respect different recombination mechanisms can happen:

      i. *Bulk recombination*. This recombination takes place inside the semiconductor material and it can happen in three different ways: (i) **Auger recombination**, which is dominant in highly defective (doped) materials and in indirect bandgaps materials. In this process, firstly an electron and an hole recombine, then the excess energy is transferred to another electron by exciting it to the conduction band and finally the excited electron thermalizes toward the lowest band edge by emitting phonons; (ii) **Radiative recombination** is dominant in direct bandgap materials, in this process the electron makes a transition from the conduction to the valence band and recombines with an hole in the valence band while emitting light; (iii) **Shockley Read Hall recombination** is dominant in highly defective (doped) materials, therefore this recombination process is caused by

a defective state in the (forbidden) bandgap. These defects facilitate the recombination of electron and hole and the excess energy is emitted as a photon or phonon [7].

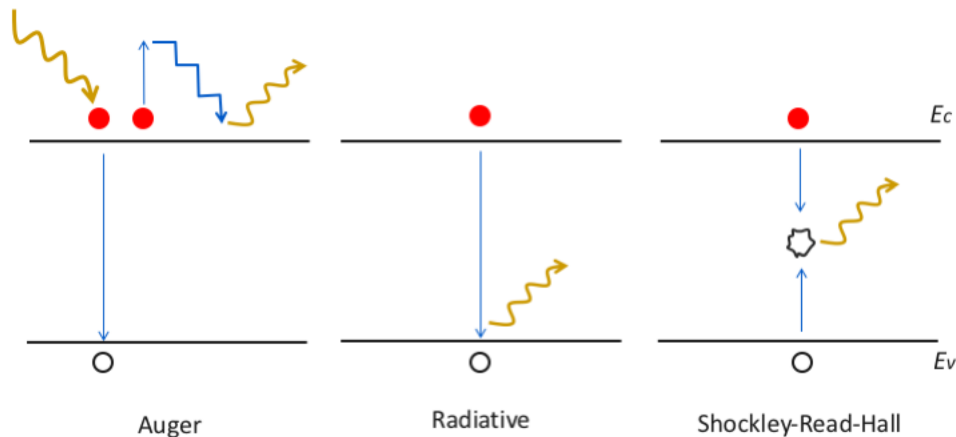


Figure 1.6 – Recombination processes occurring in the bulk of a semiconductor material.

ii. *Surface recombination*. The most critical recombination mechanism in SHJ cells is the one that originates at the interfaces. This is because of the junction made of materials with different crystallographic structures and because of interruption of the lattices. At the interface of c-Si and a-Si silicon, atoms are missing and unpaired valence electrons form the so called *dangling bonds*. These act like defects level within the forbidden bandgap and therefore will induce SRH recombination [10]. The dangling bonds are the main causes for recombination when high quality substrates are used (as in this work, where FZ c-Si substrates are employed). On this respect, section 1.2.4 deals with the surface passivation, which is a technique used to reduce the surface recombination.

(b) *Resistive losses*. Series R_s and shunt R_{sh} resistances generates losses that mainly affect the fill factor (FF) of the solar cell. These losses include the leakage current across the junction, the sheet resistance of the doped layers, the contact resistance between the TCO and the metal, the metal grid pattern (fingers and busbar) and the contact resistance with the back metal [11].

1.2.4. Surface passivation technique

At the silicon surface the Si-Si bonds are broken, this creates dangling bonds which act like a trap for electrons and holes. The surface recombination is the dominant mechanism in solar cell with high quality bulk, therefore surface passivation is the technique employed to reduce dangling bonds. This is a crucial step prior to emitter layer deposition and to achieve it, two passivation techniques have been adopted in this work:

- **Chemical passivation**, which decreases the interface defect density by depositing a passivation layer that contains an abundance of hydrogen atoms, which will bond with silicon forming new Si-H bonds. In this work highly hydrogenated a-Si intrinsic layers ((i)a-Si:H) has been used as passivating layer.

- **Field effect passivation**. Considering that surface recombination rate in c-Si is maximum when the concentration of electrons and holes is equal, therefore this technique is based on unbalancing the carrier concentration. The surface carrier concentration is reduced by inducing a band bending (an electric field) which prevents carriers to accumulate at the interface. This can be done by depositing a fixed negative/positive charged film or introducing an high doped layer. In this work we will refer to the field effect passivation obtained at the rear as Back Surface Field (BSF) and it is obtained by creating a low-high doped junction ((n)c-Si / (n+)a-Si).

For HIT structure dangling bonds saturation is achieved by depositing hydrogenated a-Si, which can provide field effect passivation by further growing doped layers [12]. Other c-Si solar cells architectures use different materials to provide passivation, as for example a-SiN_x:H, SiO_2 and Al_2O_3. Silicon nitride (SiN_x) and aluminum oxide (Al_2O_3) are used as dielectric since they store a high fixed charge carrier density.

1.2.5. Band diagram analysis and carrier transport

Figure 1.7 shows the heterojunction formed in the HIT structure fabricated in this thesis.

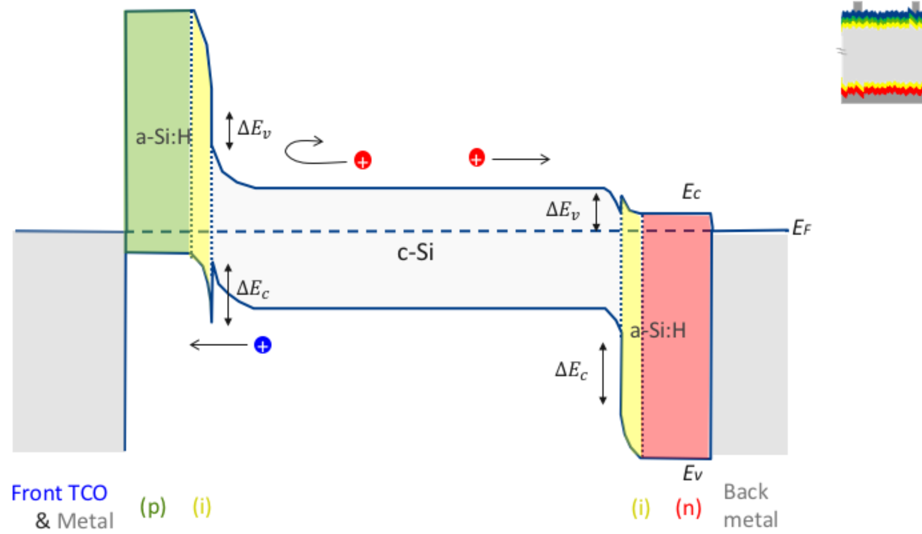


Figure 1.7 – Schematic band diagram of the fabricated silicon heterojunction cell ith intrinsic thin layer.

The a-Si/c-Si heterojunction is characterized by the following properties: bandgaps $E_{g,c-Si}$ = 1.12 eV, $E_{g,a-Si}$ = 1.75 eV (at 300K); electron affinities X_{c-Si} = 4.05 eV, X_{a-Si} = 3.9 eV. Their differences determine the band offsets $\Delta E_c = X_{c-Si} - X_{a-Si}$ = 0.15 eV and $\Delta E_v = \Delta E_c - \Delta E_g$ = 0.45 eV [13].

In the given structure the absorber layer is n-type c-Si and the holes are collected by the front emitter. The large conduction band offset forms a barrier for majority carrier electrons, while the valence band offset is so narrow that allows transport of holes through tunneling toward the (p)a-Si:H emitter. On the rear side a small offset of the conduction band allows electrons to move toward the metal electrode, while the high ΔE_v forms a barrier for holes, hence preventing recombination at the back. The thin intrinsic layer, with fewer defects, provides chemical passivation.

A way to increase the selectivity of each junction is to increase the doping of the a-Si since this would lead to fermi-level pinning. Alternatively, the n-type c-Si can be fewer doped or also the bandgap of the a-Si layer could be increased by introducing oxygen or carbon atoms [14].

1.3. State of the art of c-Si based solar cell

The following section gives an overview of the main high efficiency solar cell fabrication processes that use **n-type** monocrystalline silicon as a bulk (absorber) material.

Aluminum front surface field (Al FSF)

This structure is a small modification to the screen-printed *aluminum back surface field* (Al BSF), which is the cell mostly employed in the PV industries. The Al FSF is based on an n-type wafer and the phosphorous is diffused at the front creating the front surface field. At the back there is the emitter and the aluminum which serves as back contact. For this structure is crucial to use high quality wafer, because the diffusion length of the minority carriers has to be high enough to reach the back junction. Using Float Zone wafers, *Fraunhofer ISE* reached an efficiency of 19.3% [15]. However this structure is not expected to reach record efficiencies because of the high recombination losses at the c-Si/aluminum interface.

Passivated emitter rear contact (PERC): locally (PERL) and totally (PERT)

The first high efficiency solar cell concept is the PERC structure, which involves one main improvement with respect to the standard c-Si solar cell: the introduction of a thin thermal oxide layer (thermal SiO_x) between the doped c-Si and the contacts. This passivation scheme avoids the direct contact of silicon and metal which would lead to high SRH recombination [16]. In the PERC family there are two solar cells technologies named PERL and PERT. In the former the metal/silicon contact is limited to small localized points, while in the latter the contact is extended to the entire back surface. The *University of New South Wales* owns the record with 25% of power conversion efficiency with a structure based on a p-PERL [17]. *IMEC* tried to shift the production line from p-PERL into the n-PERL, where, similarly as the Al FSF concept, the junction passes from front to back side and the (p+) emitter is on the rear.

Interdigitated-back-contacted solar cell (IBC)

Another promising architecture to obtain high power conversion efficiency is the IBC structure, where the contacts (for holes and electrons) are at the back side. This leads to an increase in light absorption due to the absence of the front shading caused by the metal grid. Besides an improvement in light trapping, this structure benefits also of low contact resistance between silicon and metal thanks to a passivation layer. However, the carrier diffusion length becomes critical since all carriers are collected on the back side [18].

Heterojunction solar cell (SHJ)

As explained in section 1.2, SHJ cells are based on the deposition of thin layers of amorphous silicon above and below the c-Si absorber, these two layers serves as emitter and surface field. The most successful SHJ cell is obtained when thin hydrogenated intrinsic a-Si layers are inserted between the doped a-Si and the bulk because these layers reduce the defect density states at the interfaces, hence reducing the recombination probability. On the two doped layers, a transparent conducting oxide (TCO) layer is deposited with sputtering. Along with the improvement in lateral conductivity of carriers, TCO also works as an anti-reflection layer [19].

Finally, besides the standard SHJ structure, hybrid architectures can be employed in which high efficiency concepts are combined (e.g. to achieve the world record *Kaneka Corp.* combined HIT and IBC architectures) [20].

1.4. Thesis motivations

Motivation for SHJ structure

As can be noticed from figure 1.1, in the last decades (since the first cell was invented in 1992 [4]) the efficiency of SHJ cells steadily increased, while the trend is different for c-Si homojunction, which did not make any further progress in efficiency. SHJ solar cells are a promising technology and there is still space for improvements and research progress. Among the advantages of SHJ, the following are of relevance:

- The a-Si layers are deposited by deposition at temperatures below 200 $°C$, hence the low temperature fabrication process decreases the cost of production;
- Cells do not suffer of Staebler-Wronski effect observed in a-Si solar cells [21], since the bulk material of the cell is c-Si;
- It is reported that SHJ cells perform better at high temperature, so they have a lower temperature coefficient with respect to standard c-Si homojunction solar cells ($-0.45\%/K$) [22];
- HIT cells can be used also for bifacial applications thanks to the symmetry of the structure;
- The introduction of the intrinsic hydrogenated a-Si layer, in the HIT architecture, reduces interface state density, determining a reduction of surface recombination and leading to outstanding V_{oc} values;
- From a fabrication point of view, HIT solar cell with front and back metallization is rather simple and involves few process steps, potentially decreasing the costs. However, the main bottleneck for this structure to dominate the market is related to the expenses for the adjustment of the production line [23].

Motivation for <n> c-Si substrate

The solar cells fabricated in this work are made of n-type c-Si <100> high quality Float-Zone (FZ) wafer with a thickness of 280 $\pm$ 20 μm and with a resistivity between 1 and 5 $\Omega \cdot cm^2$.

Currently, most of the solar cells produced by the industry are based on p-type bulks, nevertheless it is believed that n-type solar cells can lead to higher efficiency, because of its favorable material properties. Among these properties, there is the absence of oxygen-boron defects which leads p-type c-Si to degrade upon illumination. Furthermore, n-type c-Si is more tolerant to metallic impurities such as iron, which is used in the production line for making silicon wafers [24].

A shift toward n-type substrates is expected soon, however nowadays the highest barrier that prevents n-type to be used for large scale production is related to the higher costs of production of n wafers with respect to p wafers.

Motivation for front-junction

Considering the typical heterojunction cell in which n type bulk is used, there are two possible configurations that can be adopted:

- The standard front-junction cell, in which the emitter is deposited at the front of the c-Si and at the back an (n) doped a-Si:H layer is used as back surface field (BSF).
- The other structure is the rear-junction cell, in which the (i/n) stack is used a the front as front surface field (FSF) and the (i/p) stack is deposited at the rear in the role of emitter.

The emitter has the task of collecting holes-minority-carriers which have been generated (separated) in the bulk. However, when the junction is at the rear, the diffusion length of the minority carriers has to be high enough to reach the back junction since, from Lambert-Beer law (equation 1.1), it is known that most of the carriers are photogenerated toward the front.

$$I(x) = I_0 \cdot exp(-\alpha x) \tag{1.1}$$

Where I_0 is the magnitude of the irradiance at the front surface of the bulk, α is the absorption coefficient, x is the distance travelled in the bulk [7].

On one side, it can be understood that most of the light is absorbed in the first 10 μm of the bulk, but on the other side the generation profile does not follow the exponential decrease behavior because the absorption coefficient of the materials is wavelength dependent.

When designing an heterojunction, besides the bulk c-Si, all layers influence the solar cell performances. In this thesis work, thanks to the front-junction structure we could avoid to use TCO at the back of the cell, which constitutes two main advantages: (1) it is a simplification in the process line and (2) it is avoided to sputter TCO on the thin (n) a-Si layer, which can be damaged by the strong sputtering deposition.

1.5. Scientific questions and structure of the thesis

The aim of this project is to fabricate an high efficiency front junction SHJ solar cells.

The main research areas which have been investigated are the following:

1. Optimization of pre-treatments before the PECVD depositions:
    - How to achieve the optimal textured surface morphology?
    - How to prepare the proper clean environment for the PECVD depositions?
    - How to reduce the effect of residual boron atoms/molecules on the sample holders of the PECVD reactor?
2. Optimization of solar cell precursor
    (a) Optimization of intrinsic a-Si:H passivation layer on the emitter side:
        - How to increase the surface passivation of the c-Si?
    (b) Optimization of front emitter (i/p) a-Si:H:
        - How does the thickness of i-p stack affect the passivation quality of HIT solar cell?
        - How to find the optimal trade-off between a low activation energy and an high passivation quality for the front emitter?

(c) Optimization of back surface field (i/n) a-Si:H stack:

- How to design the optimal BSF?

3. Optimization of front and back end fabrication process:

(a) Optimization of transparent conductive oxide:

- Which is the optimal material to be employed as TCO?
- Does the back TCO influence positively the performance of the solar cell?

(b) Optimization of metal contact:

- How to improve the metallization of the HIT solar cell by targeting an increase in FF?

The report is structured as follow: chapter 2 introduces the general process line and characterization equipment used; chapter 3 is dedicated to the pre-deposition treatments and aims at understanding the importance of texturization and cleaning steps; chapter 4 investigates the emitter and back surface field design, focusing on their roles and issues. A double intrinsic layer is proposed in order to enhance the passivation quality and thicknesses of the thin a-Si layers are calibrated in order to reduce parasitic absorption. Finally high short circuit current and open circuit voltage are obtained in the solar cell; chapter 5 present experiments on the electrical and optical properties of the TCO and based on simulation results a discussion on the optimal work function that it should have to foster carrier transport toward the contacts. In addition, it also shows that a replacement of e-beam evaporated Aluminum with electroplated Copper for the front metallization leads to a significant increase in fill factor.

2

Cell Fabrication Process and Characterization

This chapter aims at explaining in detail the processes and deposition techniques used for the construction of the SHJ solar cells. An initial explanation of the functions and the issues of each layer will be given in order to introduce the motivations of the experiments, which will be treated in detail in the following chapters. Additionally, the working principles of the equipment used for the characterization of the cells are explained.

2.1. Overview of SHJ baseline process flow

Figure 2.1 shows the overall process used to fabricate the front emitter SHJ solar cell in *Clean Room 10000* in EKL, TU Delft. N-type Float-Zone (FZ) c-Si with <100> surface orientation is used, the wafer thickness is 280 ± 20 μm and resistivity is between 1 and 5 $\Omega \cdot cm$. The wafer is textured in a solution of deionized water (DI water), tetramethyl ammonium hydroxide (TMAH) and *Alkatex Zero* (figure 2.1 (a)). After four nitric acid oxidation of silicon cycle (NAOC) [25], the sample is loaded into plasma enhanced chemical vapor deposition (PECVD) reactor and the intrinsic hydrogenated amorphous silicon ((i)a-Si:H) is deposited on both sides of the wafer in order to provide chemical passivation. Next, doped a-Si:H layers are deposited in different dedicated chambers (in order to avoid cross contamination) and the carrier selective emitter and BSF are formed (figure 2.1 (b)). The cell precursor is then moved into the RF magnetron sputtering system and 75 nm of transparent conductive oxide (TCO) is deposited on the front side (figure 2.1 (c)). Lastly, the front metal contact is deposited by electro-plating of copper and the back contact is deposited by electron-beam and thermal evaporation of silver, chromium and aluminum (figure 2.1 (d)).

On one wafer four cells with an area of 9 cm^2 each are fabricated, distinguished by the front metallization pattern. Different metal coverage are used in order to study their influence on the solar cell performance. An example of the 4 DIE fabricated with one wafer is shown in figure 2.2.

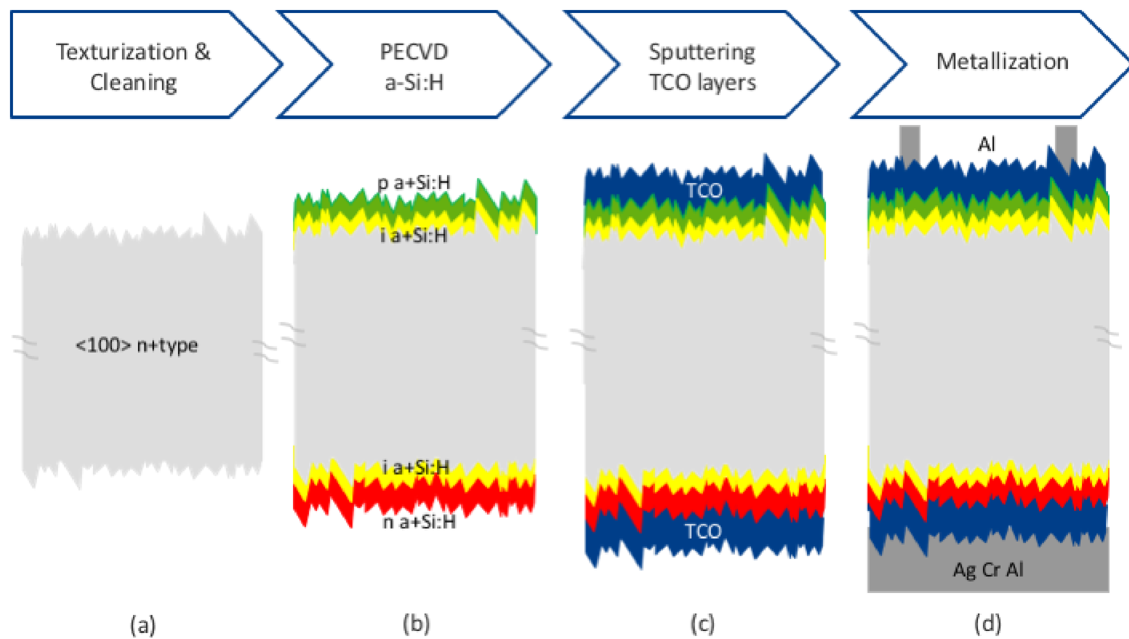


Figure 2.1 – Process flow to fabricate SHJ-HIT solar cells.

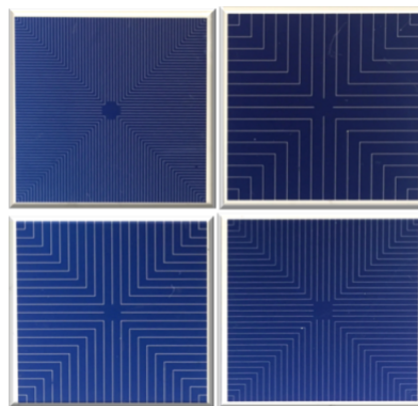


Figure 2.2 – Four cells fabricated with different metallization patterns.

2.2. Wafer pre-deposition treatments

Light trapping, using textured surfaces, is a treatment that contributes to achieve high performance solar cells. Front texturization promotes the short wavelength absorption due to the increased front surface area (by a factor of 1.73 with respect to the planar c-Si [26]), and gives the opportunity of internal bouncing of photons. This results in an increase of photons collected, hence an increase in J_{sc}. However, the texturization has also side effects that arise from the increased surface area (higher probability of surface recombination) affecting mainly the V_{oc} [27].

A proper texturization can result in an overall gain in performance and in this thesis work the classical random pyramids growth by wet etching is applied: <100> c-Si is converted into pyramid textured c-Si surface with <111> facades by applying anisotropic wet chemical etching. The wafer is submerged into a solution at around 80 $°C$ for 20 minutes. The solution used is composed of: 4 l of DI water, 1 l of standard commercialized tetramethyl ammonium hydroxide 25% diluted solution and 120 ml of *Alkatex*

Zero.

Temperature, timing and composition are variables that have been optimized in order to achieve the desired pyramid density and dimension. Then, *Alkatex Zero* is used as alternative to isopropanol (IPA) in order to accelerate and promote a uniform formation of pyramids on the planar facets. Besides the fact that *Alkatex Zero* is less noxious and has an higher evaporation temperature with respect to IPA, it also guarantees a texturization with smaller pyramids size and higher density of pyramids [28] [29]. However, the formation of pyramids makes more critical the cleaning process, since pyramids constitute contaminant deposition centers and therefore the cleaning procedure becomes of crucial importance.

In this work the wafer is cleaned following four cycles of NAOC. This cleaning procedure involves three steps: (1) Immersion for 10 minutes in HNO_3 99% at room temperature, (2) 10 minutes in HNO_3 69.5% at 110$°C$, (3) Dipping for 3 minutes in HF 0.55%.

Between each step the wafer is rinsed in DI water to avoid cross contamination of the baths. The two baths with HNO_3 are needed to grow an oxide layer which traps contaminants and dust and then the final dip in HF remove the silicon oxide layer and the trapped contaminants. The cleaning is of crucial importance especially for textured surfaces and in previous thesis work it has been proved that the optimal number of NAOC cycles is four [30].

2.3. Plasma enhanced chemical vapor deposition

Radio Frequency Plasma Enhanced Chemical Vapor Deposition (RF-PECVD) is a process used for the deposition of thin a-Si layers. Silane (SiH_4) and hydrogen (H_2) are the precursor gasses used to deposit the intrinsic layer, while phosphine (PH_3) and diborane (B_2H_6) are added as dopant gasses to form respectively (n)a-Si:H and (p)a-Si:H layers.

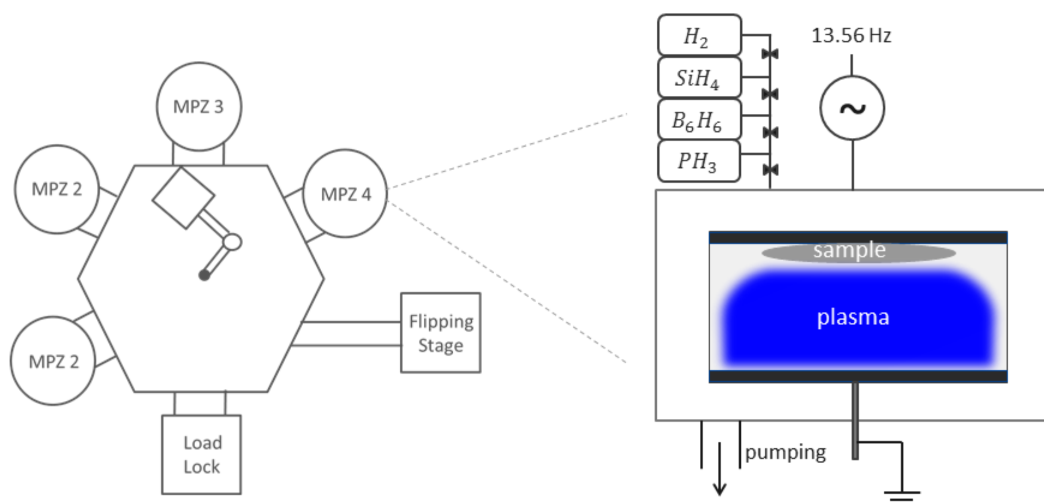


Figure 2.3 – PECVD reactor cross section.

Figure 2.3 shows a schematic section of a PECVD reactor. The reactor used is equipped with

four processing chambers (MPZ1 for the deposition of (p)a-Si:H, MPZ2 for (n)a-Si:H, MPZ3 for (i)a-Si and MPZ4 for (i)a-Si:H). In each chamber a plasma is ignited by applying a radio frequency of 13.56 MHz between two parallel electrodes. On the lower electrode there is a gas shower head that homogeneously vaporizes the gasses in the chamber. At a distance of 6-10 mm there is the second electrode where the sample is positioned. The deposition chamber is under vacuum (the pressure is around 10^{-8} and 10^{-8} $mbar$) and the process pressure ranges between 0.7 and 8 $mbar$. The deposition temperature of the heater is between 290 and 305 $°C$, such that the temperature on the substrate does not exceed 180 $°C$, and lastly the controller valves accurately regulate the amount of precursor gasses flow.

2.4. Transparent conductive oxide sputtering

At the front side of the cell, between the emitter ((p)a-Si:H) and the metal contact, an additional transparent and conductive layer is inserted to guarantee the lateral transport of carriers to the metallic front electrode and improve optical properties of the cell by ensuring anti-reflection. In order to fulfill this tasks the front TCO material should be highly conductive, highly transparent, and have a refractive index which is the geometric mean of the refractive indices of silicon and air (or glass).

At the back side of the cell, between the back surface field ((n)a-Si:H) and the metal contact, the TCO may be inserted as well. Given that on the back side of the cell there is no need for lateral transport, because the metallization has a full area coverage, it is necessary to get an insight on the TCO and metal deposition techniques and on the a-Si/TCO/metal bands alignments in order to understand if a TCO layer is favorable. Indeed, if the workfunction of the TCO is misaligned with the bands of the back surface field ((n)a-Si:H), this would lead to the formation of a Schottky barrier, which would act against the extraction of the charge carriers. In this respect, simulations and experimental studies have been carried in section 5.2.

The TCO films were deposited by radio frequency sputtering, which is a physical vapor deposition technique based on the bombardment of high energetic argon ions. The plasma is maintained by RF excitation and the ions are accelerated from the plasma to the target sample by an electric field. Two different dopant indium oxide films are tested in this work: (i) Indium Tin Oxide (ITO), where In_2O_3 is doped with SnO_2 and (ii) Hydrogenated Indium Oxide (IO:H), in which H_2O vapor is inserted in the gas flux in order to incorporate hydrogen into the In_2O_3 [31].

2.5. Metallization

The last goal of this research is the study of the metal contacts in order to increase the Fill Factor (FF) without reducing the other parameters of the cell. The reasoning why we target the FF in the metallization tests relies on the definition of FF, which is mainly influenced by series and shunt resistances. The former includes different components among which (i) the fingers resistance (ii) the busbar resistance (iii) the contact resistance between the a-Si and the metal and (iv) the back contact resistance. The definition of FF and the strategies to improve it are shown in chapter 5. The tasks of the contacts are the collection and transportation of carriers, however different issues have to be addressed during the fabrication of the back and front metalizzation.

The back metal contact is full area and is formed by 200 nm of Ag, 30 nm of Cr and 1200 nm of Al. Silver is used because it has a lower contact resistance with respect to any other metal, because it is

more conductive and lastly because it is highly reflective, allowing low wavelength photons, which were not absorbed at first, to be reflected back toward the absorber layer. Chromium is used to prevent the formation of $AgAl$ alloy, which has an high resistivity, while aluminum is used as main metal because of his high resistance to oxidation.

The design of the front metal contact is more critical and therefore the goal is to get the highest aspect ratio in order to minimize the contact resistance without increasing the shaded areas. For this purpose different top metals materials and metallization techniques are studied:

- Al e-beam evaporation;
- Cu plating on a Ti seed layer;
- Ag paste screen printing.

Evaporation is a *Physical Vapor Deposition* (PVD) technique and relies upon the change in physical state of the metal. Starting from a solid state, the metal is heated until the evaporation occurs and then it condensates on the surface of the sample. There are two ways to transfer heat: (i) thermal evaporation and (ii) electron beam evaporation. In the thermal evaporation, heat is generated by applying an high voltage to a tungsten crucible (a resistor), then the material is heated by direct contact with the crucible. In e-beam evaporation the heat transfer is indirect, therefore a strong electron beam is generated and accelerated. The highly energetic electrons strikes the metal and their kinetic energy is transformed into thermal energy, when the atoms reach enough energy they leave the surface, cross the vacuum chamber and finally get deposited into the sample surface. Thermal evaporation is usually used for low melting point materials (e.g. Ag at 961 $°C$), however aluminum, regardless the low melting temperature (660.3 $°C$), it is deposited by e-beam evaporation because of the risk of alloying with the tungsten crucible [30].

$Ti-Cu$ electroplating has been also experimented. In this technique a conductive surface (titanium) is covered with a metal (copper). Two electrodes (the copper and the sample) are connected in a circuit and are immersed into an electrolyte solution which contains dissolved Cu ions. When a constant current flows though the circuit the Cu ions deposits on the cathode-titanium surface. Figure 2.4 shows a schematic of the process and a cross section of the final device.

As it will be explained in chapter 5, the main advantage that electroplating allows compared to evaporation is the increase in the aspect ratio. Indeed, with electroplating up to 40 μm of copper can be grown in height, while evaporation allows only 2-4 μm of aluminum in height. Potentially electroplating could lead to even higher performances than the one obtained in this thesis work, because a substitution of titanium with nickel would avoid e-beam evaporation process which is very aggressive and leads to detrimental effects on the a-Si passivation [32].

Screen printing metallization technique is generally the most used in the industry. The process consists of applying silver paste at room temperature on the sample through polymeric meshes, which are spaced between each other such that the paste can deposit on the wafer. Afterward, the silver is sintered by annealing for an hour at 170 $°C$ [33]. Unfortunately, in our group this technique is still under optimization. The front grid masks for silver screen printing are different with respect to the one used for aluminum and copper metallizations, this make the comparison of the devices somehow not precise. Therefore with Ag screen printing the cell is 2.7 cm x 2.7 cm and the design at the front is *H-grid*, while for Al evaporation and Cu plating the cell is 3 cm x 3 cm and the design at the front is *squared* as shown in figure 2.2.

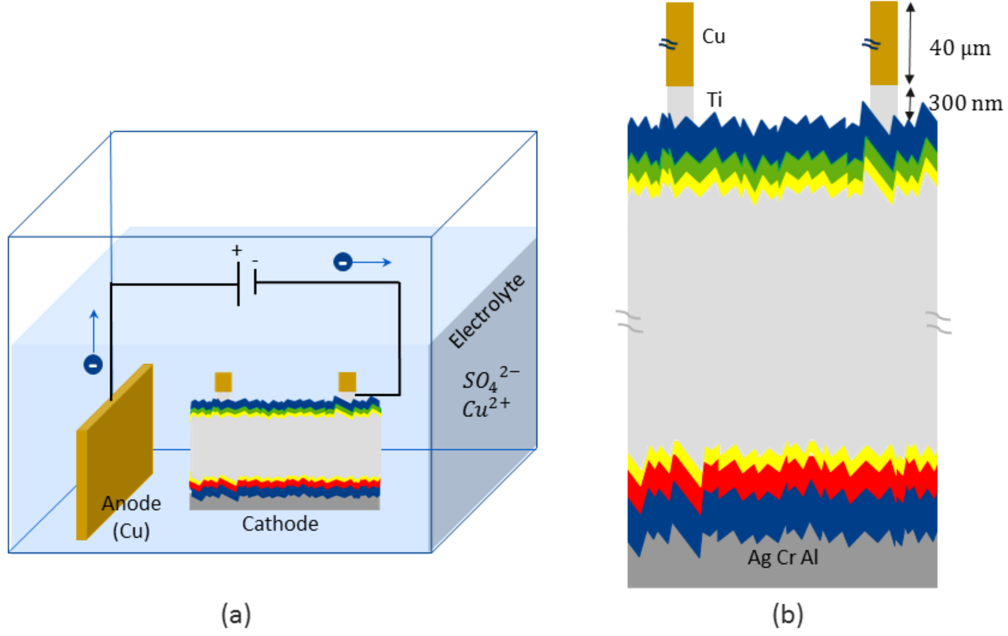


Figure 2.4 – Cu plating: (a) A Titanium cathode electroplated with copper in a electrolyte solution containing copper anode that oxidises and gives up electrons which go toward the cathode (b) final device cross section

2.6. Solar cell characterization

In this section, the solar cell characterization methods and the equipments are presented. During this thesis work measurements were carried out not only to establish the performances of the final working device (e.g spectral response, external parameters and efficiency) but also to characterize the working of all deposited layers (e.g charge carrier lifetimes).

Implied-Voc and minority carriers lifetime measurements

Sinton WCT-120 lifetime measurement has been used to determine the minority-carrier lifetime τ_{eff} and the implied open circuit voltage iV_{oc}.

The continuity equation, which identifies the evolution over time of the excess minority carrier density (Δn), provides us the generalized expression for τ_{eff}:

$$\frac{\partial \Delta n}{\partial t} = G - U + \frac{1}{q}\nabla J \tag{2.1}$$

By using $U = \dfrac{\Delta n}{\tau_{eff}}$ we can then explicit τ_{eff}:

$$\tau_{eff}(\Delta n) = \frac{\Delta n(t)}{G(t) - \dfrac{d\Delta n(t)}{dt}} \tag{2.2}$$

In this work *Sinton* was always settled to *transient mode* therefore the lifetime was always higher than 500 μm which means that it is larger than the duration of the flash lamp and at this circumstance the excess carrier generation rate G can be assumed to be zero, as consequence the equation simplify to:

$$\tau_{eff}(\Delta n)_{transient} = \frac{\Delta n(t)}{\frac{d\Delta n(t)}{dt}} \tag{2.3}$$

All reported values for τ_{eff} were evaluated at a constant carrier injection density, Δn = Δp = 1.0 $\cdot 10^{15} cm^{-3}$. *Sinton* has been specifically used to monitor and optimize the fabrication process layer-by-layer before the metalizzation. On this purpose iV_{oc} can give you some insight since it represents the V_{oc} value when the effect of R_s is not considered. iV_{oc} is defined by the following equation:

$$iV_{oc} = \frac{kT}{q}\ln(\frac{\Delta n(N_A + \Delta n)}{n_i^2} + 1) \tag{2.4}$$

External quantum efficiency

The *External Quantum Efficiency* (EQE) measurements were performed using a ”spectral response set-up”, which is composed by a light source lamp, a beam splitter and monocromators. With this set up the spectral response of the tested cell is measured at each wavelength in the range from 300 nm to 1200 nm with a step of 10 nm.

As shown in equation 2.5 EQE is defined as the ratio of the collected photons over the incoming photon flow, meaning that EQE is 1 when all absorbed photons are converted into electrons-holes pairs. In practice EQE is always less than 1 because of electrical losses (e.g. recombination) and optical losses (e.g. reflection and parassitic absorption) [12].

$$EQE = \frac{J_{ph}(\lambda)}{q \cdot \Psi_{ph,\lambda}} \tag{2.5}$$

The EQE set up is also used to calculate the J_{sc} of a solar cell, this is done by considering the current produced from a given photon flux and the integration is given in equation 2.6. This is more accurate than the one defined by the illuminated J-V simulator since it is not based on the contact area, which can be less accurate [34].

$$J_{sc} = q\int_{\lambda_{min}}^{\lambda_{max}} EQE(\lambda)\cdot\Phi(\lambda)\cdot d(\lambda) \tag{2.6}$$

Illuminated J-V solar simulator

AAA class Wacom WXS-156S solar simulator is used to measure the J-V curve, the conversion efficiency and the external parameters (J_{sc}, V_{oc}, P_{out} and FF) of a solar cell under standard test conditions (which correspond to AM1.5 solar spectrum, 1000 $W \cdot m^{-2}$ of illumination and room temperature 25 $°C$). In order to emit a continuous light source, which matches the entire solar spectrum from the UV to the IR part, the simulator is made by xenon and halogen lamps.

The set up is the following: firstly two reference cells from *Fraunhofer Institute* are used for calibration purposes, then the sample is placed under vacuum on a stage made of brass and coated with gold such that a precise temperature control can be obtained and then the device is contacted by using two probes.

The IV curve is drawn by varying the load resistance and figure 2.5 shows a typical example of an illuminated JV curve. From the JV curve the external parameters are determined:

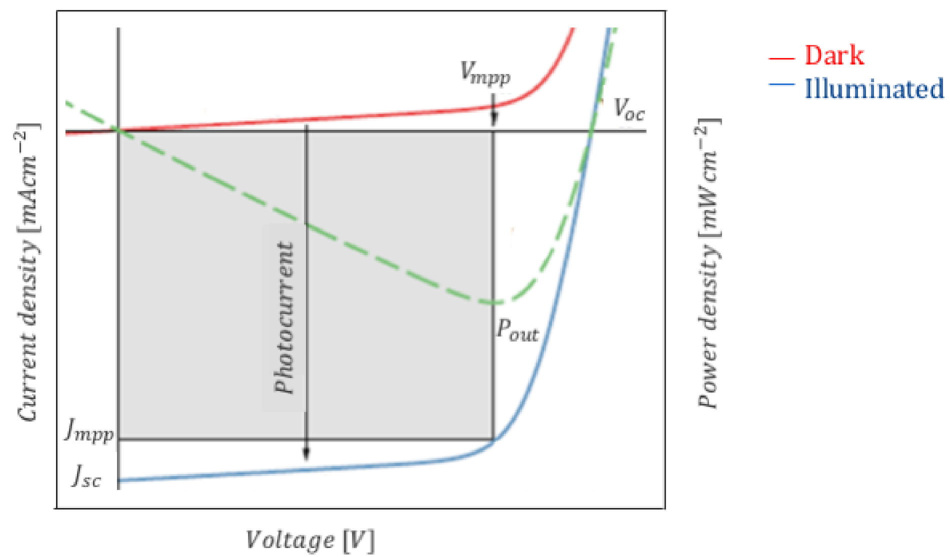


Figure 2.5 – Typical dark (in red) and illuminated (in blu) JV curve of a solar cell. The external parameters (J_{sc} V_{oc}) and (J_{mpp} V_{mpp}) are indicated, the FF is reflected by the grey area. The green line represent the power density.

- The J_{sc} is the maximum current delivered by the solar cell under short circuit conditions ($V_{oc} = 0$). In SHJ structure it depends on the optical properties of the front layers, therefore to increase the J_{sc}: (i) the absorption of the c-Si absorber layer should be enhanced, (ii) the reflection and (parasitic) absorption of the front a-Si and TCO layers should be minimized and (iii) the front metal grid should be reduced such that the shadows is limited. Other light management technique, as a proper texturization, should also be applied in order to enhance the light management.

- The V_{oc} is the maximum voltage delivered by the solar cell under open circuit conditions ($J_{sc} = 0$) and it is the distance between the quasi Fermi levels of holes and electrons. The V_{oc} is defined as:

$$V_{oc} = \frac{nkT}{q} ln(\frac{J_{sc}}{J_o}) \tag{2.7}$$

  This equation shows that V_{oc} depends on J_{sc} and J_o. The latter is the saturation current and depends on recombination. For the SHJ structure it depends mainly on the interfaces quality between the c-Si and the a-Si layers. Among the others, the recombination at the interfaces are influenced by three fabrication processes (i) texturization, (ii) cleaning and (iii) doping density of a-Si. A textured surface leads to an increase of the surface by a factor of 1.73 [26], which means more recombination centers than a flat surface, so a proper cleaning procedure become crucial. Lastly a trade off between high doping layers and low defect density has to be found in order to obtain high V_{oc}.

- The Fill Factor (FF) is a measure of the "squareness" of the J-V curve and is defined as the ratio of the maximum power that can be delivered by a cell to the product of open circuit voltage and short circuit current:

$$FF = \frac{P_{out}}{V_{oc} \cdot I_{sc}} \tag{2.8}$$

It is complicated to evaluate the factors that influence the FF. Indeed, it depends mainly on the shunt and series resistances, which in turns depend on several parameters: shunt resistance is caused by the leakage current across the junction, while series resistance depends on: (i) the conductivity of the absorber, (ii) the conductivity of the (p) a-Si emitter, (iii) the contact resistance between the TCO and the metal, (iv) the metal grid pattern (fingers and busbar), (v) the contact resistance with the back metal. The fill factor benefits from having the highest shunt resistance and the lowest series resistance [35].

Analyzing J_{sc}, V_{oc} and FF's influencing parameters is crucial in the fabrication process optimization. It is therefore important to find the optimal trade off between the contrasting effects that the different design choices have on the external parameters. For example, we already mentioned, that texturization on one side increases J_{sc} by light trapping and scattering, but on the other side decreases V_{oc} because of the more recombination centers.

A second example is related to the optimal thickness of the intrinsic a-Si layer, therefore a thicker layer is desired to obtain a good passivation, hence high V_{oc}. However, this is detriment to J_{sc}, since it would lead to an increase in parassitic absorption [35].

A third example is related to the optimal thickness of the front (i/p) stack. Here, a thicker emitter layer leads to an increase of the conductivity of the a-Si, which reduces the R_s and increases the FF. However, the (i/p) stack should maintain a minimal thickness to avoid the increase of parassitic absorptions, hence if the emitter is increased in thickness of 2 nm, for example, then the intrinsic layer should be reduced by 2 nm, which in turns would lead to a decrease in passivation quality (V_{oc}). On the opposite, if the (i) layer is increased by 2 nm and the (p) layer is reduced by 2 nm, the parassitic absorption is reduced since the intrinsic layer is less absorbing than the doped layer, but the doped layer may be not sufficient to provide band bending and carrier collection.

Those examples prove that the design choices are not trivial and that a trade off needs to be found. The following chapters go in dept into each layer design. Tasks and issues are figured out such that finally the optimal SHJ-HIT structure has been fabricated by merging theoretical with experimental outcomes.

3

Pre-Deposition Treatments Experiments

3.1. Introduction and motivation

Texturization of the solar cell front surface is a light management method which reduces the optical losses of the solar cell by decreasing the reflection of the incoming solar light and by scattering it into oblique directions. This results in an increase of photons absorbed in the bulk of the solar cell, hence increase in J_{sc}. In a textured surface two important mechanisms take place: (i) incoming photons can bounce multiple times increasing the probability of being absorbed and (ii) light gets more easily trapped due to propagation in an oblique path.

Figure 3.1 illustrates the results of optical simulations which prove that, in SHJ structure, texturization lead to an increase of c-Si absorbance from 73.2% to 84.6%. This gain mainly results from a decrease in reflectance. The reference polished c-Si wafer reflects 20.15% of incoming lights, while the textured wafer reflects only 4.06%. Therefore in the latter case the light can hit the textured surface several times as shown in figure 3.1 (c) [36].

In literature several techniques of light-management methods have been studied: random texturization, periodic texturization, back reflector, modulated surface textures, metallic nano-particles, and photonic crystals [37] [38]. In this thesis work a wet-chemical anisotropic texturization is applied on the (100) c-Si wafer. On this respect, in section 3.3 we aim at finding the optimal solution composition and immersion timing in order to obtain a randomly textured uniform surface.

To obtain high efficiency devices an effective cleaning procedure is also important. This task become even more critical when the c-Si is textured, since sharp peaks and valleys of the pyramids are accumulation centers for contaminants. Table 3.1 shows the different type of contaminants that can be present on the wafer surface and the detrimental effects they would generate [39].

Several wet-chemical cleaning techniques are used by different research centers, in this thesis work a *Nitride Acid Oxidation Cycle* (NAOC) [25] procedure has been used. As it will be presented in section 3.3.

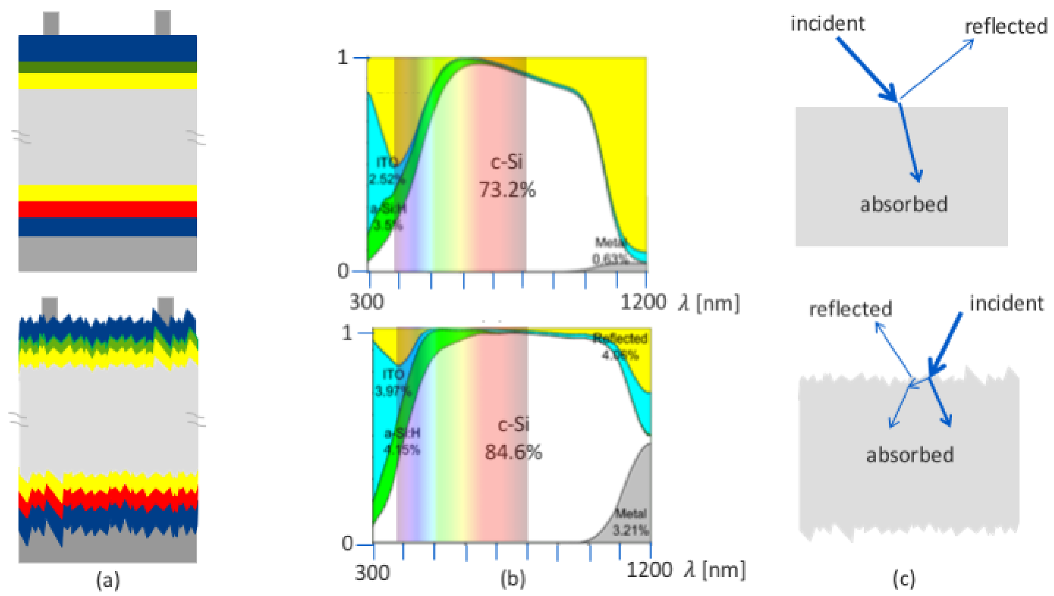


Figure 3.1 – On the top: polished SHJ solar cell; on the bottom: textured SHJ solar cell. Characteristics: (a) schematic layers structure, with equal layers materials and thicknesses, (b) the spectral response (reflectance and absorbance) of the simulated SHJ solar cells over the relevant wavelength range between 300 nm and 1200 nm (c) light trapping mechanisms of the absorber c-Si layer (adapted fromn[36]).

Table 3.1 – List of contaminants that can be found on c-Si surfaces, sources and detrimental effects on solar cells performances.

Contaminant	Sources	Effects
organic	room air, storage boxes	oxidation rate
metal	chemical, other equipment	leakage, interface properties, carrier lifetime
native oxide	room air, DI dryer, chemicals	interface oxide
micro-roughness	texturization	leakage, interface properties

The last step that should be done before loading the cleaned wafer on the PECVD reactor is the conditioning of the reactor's chambers and of the wafer's holders, these steps allow an increase in passivation quality of the tested c-Si samples thanks to the prevention of cross contamination.

The issue of cross contamination between chambers and holders has been addressed by many researchers and different technique have been developed to prevent this problem. For example the chamber can be treated with CO_2 plasma and with short vapor flush of H_2O and reactive gasses (e.g NF_3) [40] [41]. In this work to reduce the residual boron contamination it has been applied high power H_2 plasma on the chambers and a dummy layer deposition on the holders is adopted, the results are presented in section 3.4.

3.2. Experiment setup

For the investigation of the pre-deposition procedures, n-type FZ c-Si (100) wafers, with resistivity 1 - 5 $\Omega \cdot cm$ and thickness of 280±20 μm, were used. The samples were firstly textured in an activated

solution composed by 4 l of deionized (DI) water, 1 l of *tetramethyl ammonium hydroxide* (TMAH) 25 % and 60 to 120 ml of *Alkatex Zero* etchant, at a temperature of around 80 $°C$ and for a varying times between 5 and 25 minutes. The wafers were cleaned though the NAOC procedure which consist on three-steps wet-chemical cleaning line. First the wafers are subjected to two oxidizing steps (HNO_3) and then to an etching step (HF). For the symmetric structures only one NAOC cycle was carried out, such that experimental timing where accelerated (while for precursor and device structures, four NAOC cycles are used).

To test the effect of different texturization solution and duration, 20 nm of (i) a-Si:H were deposited on the textured FZ c-Si sample. A thick a-Si:H was used for maximizing the passivation reproducibility by minimizing the thickness influence of the a-Si:H layer [25]. To test the effect of residual gasses and boron contamination on the PECVD chambers, 6 nm of (i) a-Si:H and 8 nm (p) a-Si:H layers were deposited on the wafers.

3.3. Wafer texturization and cleaning

Texturization

Random pyramidal texture on the front and back surfaces of c-Si wafers lead to a reduction of reflection loss and enhanced light trapping. The random pyramidal texture can be obtained by anisotropic wet etching with an alkaline solution (DI water, TMAH and an additive, as mentioned above). Conventionally, in the PVMD group, IPA was used as additive. However substituting IPA with *Alkatex Zero* can results in several advantages: firstly, from literature, we find that texturization with *Alkatex Zero* is beneficial because it results in lower surface state density. Secondly, IPA is a volatile material and it evaporates at 80 $°C$, which coincides with the temperature used for texturization, and therefore makes difficult to control the solution composition over time [29].

Solution composition, timing and temperatures are variables that influence the morphology of the surface, hence the optical and electrical characteristics.

On this respect, two sets of textured samples have been prepared with (i) systematically varied dilution of *Alkatex Zero* from 60 to 120 ml and (ii) systematically varied duration of texturization from 5 to 25 minutes. Lastly a morphological analysis was done using a *Scanning Electron Microscope* (SEM) to reveal the pyramid size and uniformity.

From the test in which the dilution of *Alkatex Zero* was varied from 60 to 120 ml, we observe that using a solution with 120 ml of *Alkatex Zero* results in a faster manufacturing of uniformly distributed pyramids, therefore the *Alkatex Zero* acts as etching rate accelerator and promotes uniformity. For this reasons in the following experiments the composition of the texturing solution will be:

- $4\ l$ of *deionized* (DI) water,
- $1\ l$ of *tetramethyl ammonium hydroxide* (TMAH) 25%,
- $120\ ml$ of *Alkatex Zero*

The aim of the second set of experiments is to determine the optimal time for which it is sufficient to cover the whole surface with pyramids and avoid extra-timing since it would lead to appearing more pyramids without a reduction of reflectance [42]. Figure 3.2 shows a 10 μm wafer section tilted by 45$°C$ after 15 minutes (a) and 25 minutes (b) of texturization. The surface after a short texturization duration (figure 3.2 (a)) still present some (100) facets, and the pyramids are irregular in size and distribution,

on the opposite after a prolonged texturing time (figure 3.2 (b)), the pyramids started increasing in size and increased in density on the top of each other. Keeping on increasing the texturization time will lead to an increase of pyramids' density.

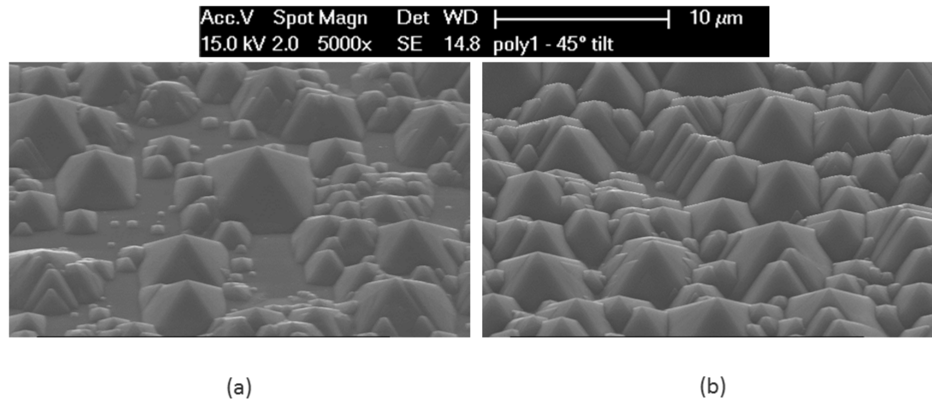


Figure 3.2 – SEM images of 10 μm c-Si section with tilt = 45°C. Same texturing solution: 4 l DI water, 1 l of TMAH 25% and 120 ml Alkatex Zero, but different texturing timing: (a) t = 15 minutes (b) t = 25 minutes.

The SEM images show that an intermediate texturization time lead to the desired surface morphology, 20 minutes of texturization results in uniform pyramid distribution with a size ranging between 0.5 - 4 μm. This is shown in figure 3.3 (note the different unit length with respect to 3.2). The fact that small pyramids (0.5 μm) are surrounded by bigger pyramids (4 μm) favours the multiple reflection which increases the probability of absorption of light.

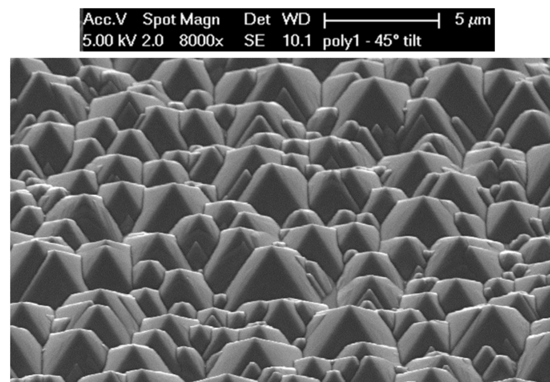


Figure 3.3 – SEM images of 5 μm c-Si section with tilt = 45°C. texturing solution: 4 l DI water, 1 l of TMAH 25% and 120 ml *Alkatex Zero*. Texturing timing = 20 minutes.

Cleaning of sample

In this work the wafer is cleaned following four cycles of *Nitric Acid Oxidation of silicon Cycle* (NAOC). This cleaning procedure involves three steps:

1. Immersion for 10 minutes in HNO_3 99% at room temperature,
2. Immersion for 10 minutes in HNO_3 69.5% at 110 $°C$,
3. Dipping for 3 minutes in HF 0.55%.

The submersion in the nitric adic baths, lead to the growth of a thin oxide layer which traps the dust and contaminants. The dipping in hydrofluoric acid, etches the oxide layer and with it the impurities. The reasons why two HNO_3 baths are used is related to the fact that, depending on the dilution and temperature of the solution, different contaminants get trapped, in particular, the bath with low dilution of HNO_3 traps inorganic metallic contaminants; while the bath with 99 % of HNO_3 traps organic contaminants. The dipping time in the HF bath has been optimized such that it can etch all the oxide and smoother the pyramids' peaks [29].

3.4. PECVD conditioning and sample's holder cleaning

Contamination and diffusion of unwanted particles into the bulk of the c-Si have detrimental effects on the performances of solar cells. Therefore, very clean production equipment and cleaning of holders are necessary [43].

A rigorous study of the effects of boron contamination on (i) a-Si:H and bulk c-Si can be performed by measuring the boron incorporation with the *Secondary Ion Mass Spectroscopy* (SIMS) and by analyzing the material structure with *X-Ray Diffraction* (XRD) and with *Raman* measurements. However a simplified argumentation can be carried by looking at the change of lifetime when a holder with and without p-type a-Si:H layer is used. The problem relies of the fact that B_2H_6 molecules are very reactive. When the plasma is ignited, boron atoms or boron oxides molecules, can escape and be incorporated into the new deposited layer [44] [45].

Indeed, in this work, to understand if residuals of p-type a-Si:H layer on the holder deteriorate the passivation quality of the samples, the following test has been performed: Two holders are cleaned with IPA, then they are loaded into the PECVD reactor, holder-1 is loaded in MPZ 4 and 70 nm of (i) a-Si:H were deposited, while holder-2 is loaded in MPZ 1 and 70 nm of (p) a-Si:H were deposited. Two wafers are divided into halves. One half of each wafer is placed in a holder such that in holder-1 (i dummy covered) there is half of each sample and in holder-2 (p dummy covered) there are the other two halves. The advantage of halving the wafers rather than simply placing one wafer per holder relies on the fact that, in this way, the initial difference present because of the different wafer bulk lifetimes is not going to alter the lifetime comparison.

Symmetric structures with 6 nm of (i) a-Si:H/8 nm of (p) a-Si layers are deposited on both sides of the two specimens and the lifetime of the four halves is measured with *Sinton*. The results, shown in figure 3.4, prove that when a dummy intrinsic layer is deposited on the holder, the lifetime is around two times larger than the one which results when dummy (p) a-Si layer was used to cover the holder. We can therefore conclude that residuals of boron atoms or boron-containing-molecules on the holder deteriorate the passivation quality of the samples [46].

It is also important to have a clean production equipment. To avoid cross contamination within the multi-chamber PECVD reactor, each chamber is specifically used for the deposition of one specific layer (i, n or p); additionally, samples are mounted in the top electrode such that dust deposition on the films is prevented; prior to any deposition, a H_2 plasma treatment of the chamber is performed, which consists of exposing the chamber walls to 50 $sccm$ of H_2 flow at pressure p = 2 $mbar$ and at high power

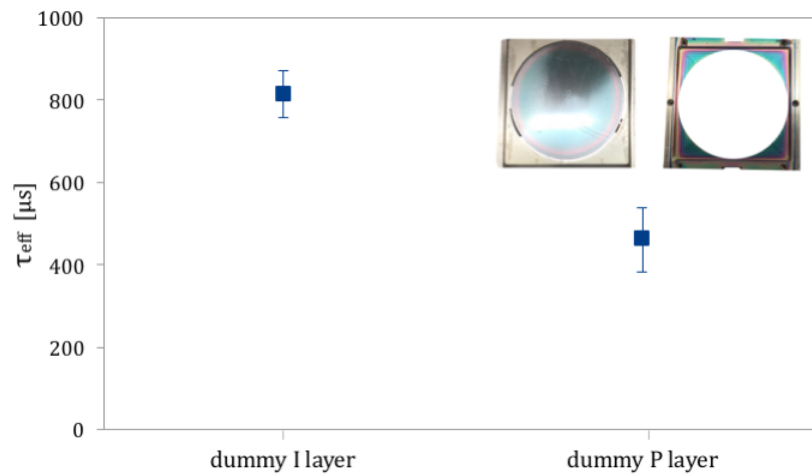


Figure 3.4 – The x-axis represents the layers pre-covered on the holer, the y-axis represents the lifetime measurements. The symmetric structure measured is (p) a-Si:H / (i) a-Si:H / c-Si / (i) a-Si:H / (p) a-Si:H. In the holders were deposited 70 nm of intrinsic layer or 70 nm boron doped layer.

P = 60 W for 10 minutes [41].

All these pre-treatment methods can reduce, and possibly eliminate, the residual boron atoms/molecules which otherwise can be released during the deposition of the intrinsic a-Si:H layer, resulting into more defective layer.

3.5. Conclusions

Texturing and cleaning pre-PECVD-deposition are crucial in order to increase the performances of solar cells. Firstly wafers are textured for 20 minutes in a solution of $4\ l$ of DI water, $1\ l$ of TMAH 25% and $120\ ml$ of *Alkatex Zero*, the TMAH acts as etchant and the *Alkatex Zero* acts as etching rate accelerator and promoter of uniformity.

- *How to achieve the optimal textured surface morphology?*

20 minutes results to be the optimal time for which a surface with uniformly distributed pyramids is formed. A shorter texturization duration would lead to a surface which still presents some (100) facets, while a longer texturization duration would lead to an increase in size of pyramids and the tendency of pyramids to appear on the top of each other. SEM images revealed that 20 minutes, for the given solution composition, leads to the desired surface morphology with a uniform distribution of pyramids. Moreover, the probability of absorption of light is increased thanks to the fact that small pyramids (height = 0.5 μm) are surrounded by bigger pyramids (height = 4 μm), favoring the reflection of hitting photons.

- *How to prepare the proper clean environment for the PECVD depositions?*

After texturization the wafers are cleaned through four NAOC. the PECVD reactor has to be properly cleaned as well before loading the samples. Therefore, a H_2 plasma treatment of the chambers is performed, which consists of exposing the chamber walls to 50 $sccm$ of H_2 gas flow (p = 2 $mbar$ and P = 60 W) for 10 minutes.

- *How to reduce the effect of residual boron atoms/molecules on the sample holders of the PECVD reactor?*

Holders contamination is also an issue which has been addressed: the problem arises from residuals of p-type a-Si:H on the holders. When the plasma is ignited, boron atoms or boron oxides molecules, can escape and be incorporated into the new deposited film, resulting into a more defective layer. To reduce the effect of residual boron atoms/molecules, the holders are pre-covered with 70 nm of dummy intrinsic layer.

4

Passivation and Precursor of the Solar Cell Experiments

The a-Si:H/c-Si hetero-junction is formed by depositing the emitter (p-type a-Si:H layer) and the *back surface field* (BSF) (n-type a-Si:H layers) over the surface of the n-type c-Si absorber. In this chapter we aim at designing the a-Si:H/c-Si junctions, able to properly select and conduct one type of carrier.

First difficulties arise because of the connection between two materials with different bandgaps, lattice and electrical properties. These lead to band's discontinuity and crystallographic lattice defects (dangling bonds) [12]. It is therefore necessary to passivate c-Si surface dangling bonds. For this purpose highly hydrogenated a-Si intrinsic layer ((i)a-Si:H) is used. The high hydrogen content reduces the number of dangling bonds by forming new Si-H bonds at the c-Si/a-Si:H interface.

Secondly, a proper emitter and BSF have to be deposited above the intrinsic a-Si:H layers in the back and front side. They ensure band bending and formation of a build-in potential which block one charge carrier type while allowing the other to cross the junction by tunneling. It is largely argued that the (p) a-Si:H layer is responsible to hamper the device performance. Therefore the exposition of B_2H_6 and SiH_4 on a surface may cause the growth of $a - SiB_x : H$ layers which are highly defective and results in low (p/i) interface quality [47].

During this thesis work, experiments have been carried out to optimize the layers deposition and fabrication processes. The chapter is organized as follow: after the introducntion of the experiment setup introduction in section 4.1; first, in section 4.2, the optimization of the deposition parameters for the intrinsic a-Si:H layer is presented. It is also proposed an innovative *double intrinsic layer* with which higher passivation quality can be achieved. Then, section 4.3, deals with the optimization of the emitter fabrication and here a trade off needs to be found between high doping level (for obtaining a lower activation energy) and low defect density (for a better passivation). Lastly, in section 4.4, the back surface field, the n-type a- Si:H layer, is studied and simulations are carried to calculate the optimal thicknesses of the back (i/n) stack.

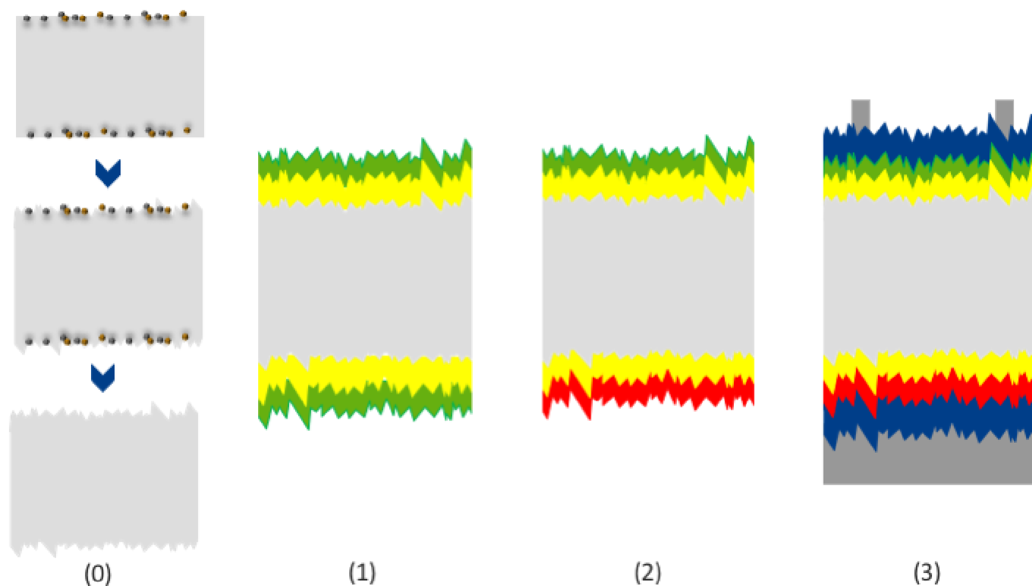


Figure 4.1 – Fabricated structures: (0) the pre-treatments seen in chapter 3; (1) symmetric structure: (i) a-Si:H / c-Si / (i) a-Si:H; (2) precursor cell: (p) a-Si:H / (i) a-Si:H / c-Si / (i) a-Si:H / (p) a-Si:H; (3) finished device: metal / TCO / (p) a-Si:H / (i) a-Si:H / c-Si / (i) a-Si:H / (p) a-Si:H / TCO / metal.

4.1. Experiment set up

Figure 4.1 shows the three different structures that were fabricated: the symmetric structure (4.1 (1)), the precursor cell (4.1 (2)) and the finished device (4.1 (3)).

N-type *Float-Zone* (FZ) c-Si, with <100> surface orientation, resistivity of 1-5 $\Omega \cdot cm$ and a thickness of 280 μm were used. After texturization and cleaning, the c-Si wafers were loaded into the load lock of the PECVD and then taken to the specific chamber dedicated for deposition of the intrinsic layers (MPZ4). This has to be done immediately after HF dipping, because silicon exposed to air is subject to oxidation. All chambers are under vacuum and therefore, prior to deposition, the base pressure is at 10^{-7} $mbar$. In the fabrication process for the precursors and the full devices, in order to avoid cross contamination, different dedicated chambers were used to deposit (p) and (n) a-Si:H layers.

For all layers a high H_2 deposition regime was chosen. The deposition pressure varied between 0.6 - 8 $mbar$, the power between 2.6 - 7.2 W. The specific precursor gasses flow and deposition parameters are tabulated in 4.1.

Table 4.1 – PECVD deposition parameters used for a-Si thin layers.

	$(i)a-Si$	$(i)a-Si:H$	$(n)a-Si:H$	$(p)a-Si:H$
Chamber	4	4	2	1
SiH_4 flow $[sccm]$	40	4	40	1.5
H_2 flow $[sccm]$	0	200	40	1.5
PH_3 flow $[sccm]$	-	-	11	-
B_2H_6 flow $[sccm]$	-	-	-	4.5
Substrate Temperature $[°C]$	180	180	180	180
Process pressure $[mbar]$	0.7	8	0.6	2.5
RF Power $[W]$	2.2	7.2	2.6	2.6

The three structures shown in figure 4.1 were fabricated in order to analyze independently each layer. The symmetric structure (4.1 (1)) was fabricated to study the deposition parameters of the a-Si:H films; the precursor structure (4.1 (2)) was fabricated to see the effect of variation in thicknesses on τ_{eff} and iV_{oc}; and lastly the finished solar cell (4.1 (3)) was fabricated to analyze the external parameters and find the optimal trade off among them.

The need to find the optimal trade off is the main design issue. For example, the doping of the emitter, has conflicting effects. To obtain high band bending and high collection of holes (high J_{sc}), the (p) a-Si:H has to be highly doped, but this would lead to increase the defect density which, in turn, decreases the passivation quality (low V_{oc}). Another example is related to the thickness of the i/p front stack. On one side a thicker emitter is desired to obtain higher lateral conductivity (high FF), on the other side a thicker intrinsic layer is desired to provide proper passivation (high V_{oc}). However an increase in i/p overall stack should be avoided since it would lead to high parasitic absorptions (low J_{sc}) [12]. The variation in thicknesses has also affects the carrier transport, therefore the (i) a-Si:H should be enough thin to allow tunneling and hopping of minority carriers toward the emitter/BSF.

4.2. Passivating layer (i) a-Si:H

In this section the optimization of the deposition parameters for the intrinsic a-Si:H layer is presented, furthermore the introduction of a seed layer and the formation of a *double intrinsic layer* is proposed as alternative to standard (i) a-Si:H *single layer*, which increases passivation quality and device performances.

4.2.1. Introduction and motivation

The passivation of dangling bonds is of crucial importance, this can be achieved adopting different materials, in this work is employed an intrinsic a-Si:H buffer layer. By means of this passivation technique, outstanding efficiencies have been obtained (e.g. it was used by *Kaneka* to achieve the world record conversion efficiency for c-Si based solar cells [3]). However there is limited information in literature regarding the process parameters that yield to the highest performances. On this respect, experiments have been performed, in which the deposition parameters were varied. Two key features need to be attained: (i) the minimum surface defect density and (ii) an abrupt interface [28].

Firstly, to understand the importance of reducing the surface defect density, we can refer to figure 4.2

that shows the c-Si surface (4.2(a)), the a-Si surface (4.2(b)) and the interface when the two materials are connected to form a pn junction (4.2(c)). The interface may be highly defective because of the crystal structures mismatch [48] and therefore high probability of recombination is expected. These dangling bonds can be saturated by inserting a thin highly hydrogenated undoped a-Si layer. The H atoms will bound with the unbounded Si atoms and chemical passivation is achieved.

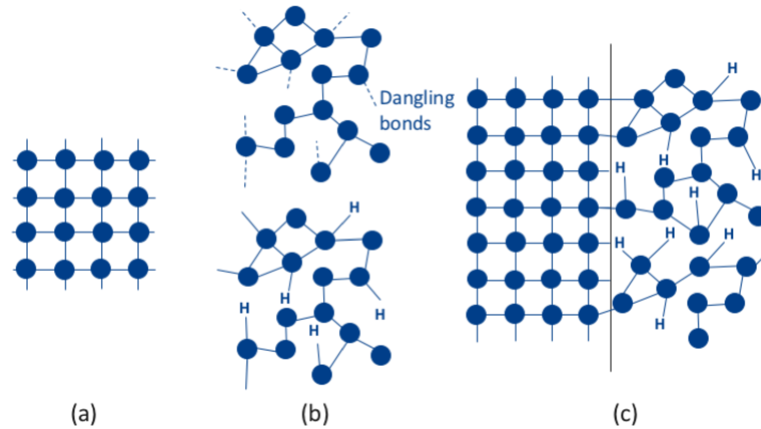


Figure 4.2 – Schematic structures of: (a) crystalline silicon, (b-top) amorphous silicon with many unbounded Si atoms, (b-bottom) amorphous hydrogenated silicon and (c) a-Si/c-Si pn junction with dangling bonds resulting from the different crystal structure of c-Si and a-Si.

Secondly, in order to obtain an abrupt interface, the doped a-Si layer is used to induce an high band bending, hence a strong electrical field, This is defined to be the field-effect passivation and is explored in detail in section 4.3 [49].

Established that the intrinsic a-Si:H layer is desired to reduce surface recombination, the optimization of this layer is experimentally performed. Firstly, the deposition parameters (distance specimen-plasma and precursors gas flow) are investigated, then the implementation of a *double intrinsic layer* is proposed. The *double intrinsic layer* is formed by a first layer, adjacent the c-Si, which has SiH_4 as the only precursor gas, and by a second layer, which is has an high hydrogen content (precursor gasses: SiH_4 and H_2).

4.2.2. Deposition parameters

The aim of this set of experiments is to find the influence of the deposition input parameters on the passivation quality and on the carrier transport.

Influence of plasma-specimen distance on deposition uniformity

To study the uniformity of deposition of the (i) a-Si:H layer in relation to the distance plasma-sample, three symmetric structures were prepared in MPZ 4. All the process parameters used in this set of experiment were kept constant beside the distance between the top electrode (specimen) and the bottom electrode (plasma). The specific distances are: 6 mm for sample 1, 8 mm for sample 2, 10 mm for sample 3. Figure 4.3 shows the lifetime values resulting from the three different distances.

Given that the power of the plasma is 7.2 W, when the sample is placed too close to the bottom electrode, then the decreased lifetime may be caused by the plasma damaging the surface due to strong ion bombardments. On the other hand, when the distance is too high, the lifetime drops completely

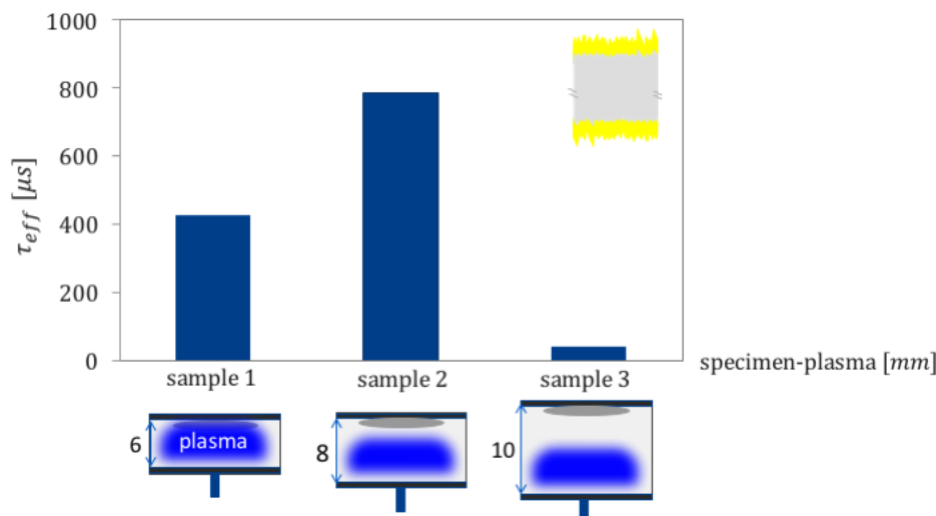


Figure 4.3 – Effective lifetime obtained with 6 nm thick (i) a-Si:H layers deposited in MPZ 4 at different electrodes distance varying from 6 to 8 mm.

and by visual inspection of the sample it is clear that the deposition of the film is not uniform on the c-Si surface. Hence, 8 mm is the optimal distance which has minimized plasma damage and ensure film uniformity.

Sections 4.3 and 4.4 address the issues of the optimization of deposition parameters for the doped (n) a-Si:H and (p) a-Si:H layers, deposited respectively in MPZ 2 and MPZ 1. In these chambers the electrode distance is fixed, respectively to 11 mm for MPZ 1 and 21 mm for MPZ 2.

Variation of precursor gasses flow

The passivation quality depends on the relative amount of SiH_4 and H_2, therefore this determines the hydrogen content and the density of the film. Based on this, the gasses' flow were varied so that we could investigate their influence on the passivation [50].

The film structure is characterized by the hydrogen to silane ratio ($R = H_2/\ SiH_4$). In the first series of experiments the SiH_4 flow was fixed to 4 $sccm$ while the hydrogen flow was varied from 0 to 200 $sccm$ with a step of 66 $sccm$ (refer to table 4.2).

Table 4.2 – Deposition rate variation as function of hydrogen flow.

$R = \frac{H_2}{SiH_4}$	$SiH_4[sccm]$	$H_4[sccm]$	deposition rate $[nm/sec]$
50	4	200	0.077
33	4	133	0.069
16, 5	4	66	0.041
4	4	0	–

Firstly, to find the deposition rates, 10 minutes of deposition on glass was performed and the film thickness was revealed by SE. The general trend is that an increase in hydrogen content leads to a decrease in deposition rate, which is desired because it allows a more controllable deposition.

Afterwards, 6 nm of (i) a-Si:H were deposited on four samples and lifetime measurements were carried with $Sinton$. Figure 4.4 shows the variation of τ_{eff} and iV_{oc} as function of R. The ratio is "limited" to 50 due to equipment constraints, therefore the PECVD reactor has a maximum hydrogen flow of 200 $sccm$. The results obtained for R = 4 and R = 16.5 are not reliable because the film deposited on the samples was visibly not uniform and during the depositions the plasma was visibly unstable, causing a drop in τ_{eff}.

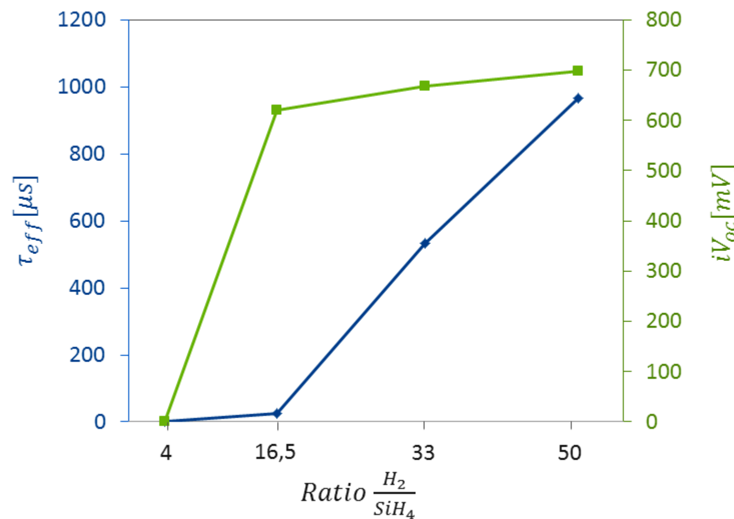


Figure 4.4 – Minority carriers lifetime τ_{eff} and implied open circuit voltage iV_{oc} to quantify the passivation quality of (i) a-Si:H / c-Si / (i) a-Si:H symmetric structures as function of variation of hydrogen flow. The thickness of the intrinsic layer is 6 nm. The samples were cleaned with one NAOC only, 70 nm of dummy intrinsic a-Si was pre-deposited on both sides of the holders and the H_2 plasma treatment was applied to the chamber prior to sample loading.

In this set of experiment all deposition parameters were kept constant besides ratio of precursor gasses. It has been chosen an high pressure (8 $mbar$) and low power (0.088 W/cm^2) regimes and a moderate deposition temperature ($T_{substrate}$ = $180°C$). The low power minimizes the possible damages due to ion bombardment [51], the moderate temperature prevents the layer crystallization [52].

The minority carrier lifetime, τ_{eff}, correlates to the change in structure of the material, which in turn is determined by the change in hydrogen dilution [53]. A film with diluted silane lowers the defect density and improves passivation, however too much hydrogen would change the microscopic structure of the film and it can lead to epitaxial growth, which has detrimental effects on passivation [23].

From literature it is known that when $R \leq R_{optimal}$ the film presents an higher voids density due to an excess of $Si-H_2$ bonds. When $R \geq R_{optimal}$ crystalline epitaxial growth leads to the degradation of film quality [50]. The goal is, indeed, to find the value of $R_{optimal}$. The problem is that the various research groups found a wide range of $R_{optimal}$ values [54] [55]. This is because $R_{optimal}$ does not depends only on the precursor gasses flows, but also on the deposition pressure, power and temperature. For example $\mu c - Si$ formation is fostered by: (i) high hydrogen content, (ii) low pressure, (iii) low power and (iv) high temperature [56]. This means that we need to find our $R_{optimal}$ and we cannot compare it with other researches finding. In particular with this given process parameters a ratio R of 50 resulted to be the optimal, therefore with a gas flow of SiH_4 = 4 $sccm$ and H_2 = 200 $sccm$ it was obtained the highest iV_{oc} = 700 mV and τ_{eff} around 1 ms.

Fundamental is to know the microstructure of the deposited film and therefore to know the amount of $Si - H_2$ and $Si - H$ bonds. High $Si - H_2$ bonds are a sign of highly porous material (hence many microvoids). On the opposite, high amount of $Si-H$ bonds, is desired since it ensure good passivation. There are different equipment that can be used to study the microstructure of the film: (i) the *Fourier Transform Infrared Spectroscopy*, which gives information about the H_2 concentration and the bounding configuration, (ii) the *Raman Spectroscopy* and (iii) *Spectroscopic Ellipsometry*, which can be used to get insight on the optical properties of the film and (iv) the *Transmission Electron Microscope Images*, which can reveal the cross-section of the a-Si/c-Si interface [57]. However, it has been shown that, a simplified method can be applied to get information about the abruptness of the interface, which is annealing of the samples [52]. Indeed, when the epitaxial grows at the interface a-Si/c-Si, then annealing reduces the minority carrier lifetime, τ_{eff} [58].

In this work (look at table 4.3) the samples were annealed at 190 $°C$ for 60 minutes and every 30 minutes the lifetime was measured. It has been observed that all samples resulted in an increase in lifetime upon annealing. Another set of samples, were annealed for 30 minutes, but at 240 $°C$. In this case the sample with high hydrogen dilution shows a slight decrease in lifetime while the sample with H_2 flow shows again a linear increase in lifetime with annealing time. No further increase in annealing temperature has tested since it is expected to have diffusion of hydrogen at around 300 $°C$ [59].

Table 4.3

temperature	$25°C$	$190°C$		$240°C$
time	$0'$	$30'$	$60'$	$30'$
SiH_4 = 40 $sccm$, H_2 = 0 $sccm$	623 μs	712 μs	730 μs	743 μs
SiH_4 = 4 $sccm$, H_2 = 200 $sccm$	918 μs	939 μs	1018 μs	972 μs

The highest passivation was obtained for the sample with ratio R = 50. But upon annealing at 240 $°C$ the specimen suffered of slight decrease in lifetime, while the samples with lower R= 0 handled better this high temperature annealing. To combine both advantages we developed a *double intrinsic* a-Si layer, as presented in next section.

4.2.3. Application of seed layer

From the previous set of experiments it is speculated that, with the given deposition parameters, we obtained an intrinsic layer close to a-Si:H / μ c-Si:H transition regime.

Based on this, this thesis proposes a passivation mechanism where in between c-Si and the the high hydrogen diluted (i) a-Si:H layer is introduced a non-hydrogenated diluted intrinsic layer, also called *seed layer*. With this *double intrinsic* layer we aim at obtaining a passivation layer with higher temperature stability from the lowly H_2 diluted (i) a-Si:H layer and better passivation properties from the highly H_2 diluted (i) layer. The new passivation layer consist of: the first 2 nm adjacent to the c-Si substrate are grown with only SiH_4 gas precursor, and subsequently 4 nm of highly hydrogen diluted a-Si:H. refer to table 4.4 for the specific deposition paramenters.

Table 4.4 – Parameters used for (i) a-Si:H / c-Si / (i) a-Si:H versus (i) a-Si:H / seed layer / c-Si / seed layer / (i) a-Si:H symmetric structures.

	$(i)a-Si:H$	$seed\ layer + (i)a-Si:H$
Thickness $[nm]$	6	$2+4$
Deposition rate $[nm/sec]$	0.069	$0.126+0.069$
SiH_4 flow $[sccm]$	4	$40+4$
H_2 flow $[sccm]$	200	$0+200$
Substrate Temperature $[^{\circ}C]$	180	180
Process pressure $[mbar]$	8	$0.7+8$
RF Power $[W]$	7.2	$2.2+7.2$

Besides lifetime improvement it is noticed that the structure with the seed layer also leads to a decrease in saturation current density J_0. The sample with 6 nm of (i) a-Si:H layer has a saturation current of 4.2 fA/cm^2 while the sample with 2 nm of a-Si + 4 nm of a-Si:H has a saturation current of 2.7 fA/cm^2. The low saturation current it is a further prove of low interfacial defect states and epitaxial-free interface [60].

It is important to notice that these results are in agreement with the studies which have been done on the influence of the H_2 plasma treatment on the microstructure of the c-Si [61]. A H_2 plasma treatment (which consists on a flow of 200 $sccm$ of H_2 at low pressure and low power regimes) directly on the c-Si surface (so prior to a-Si:H deposition) has negative effects, since it introduces micro-structural damage of the crystallographic structure of the c-Si [62]. The *double intrinsic* layer proposed overcome this by shielding and protecting the c-Si surface with a seed layer and then permits the deposition of a highly hydrogenated a-Si layer which perform better passivation.

It can be concluded that the double intrinsic passivation layer permits the adding up of the advantages of each layer:

- the seed layer, with no hydrogen, results in a smooth interface with the c-Si and avoids possible micro-structural damage on the c-Si surface [44],
- the highly diluted film (close to the amorphous-to-crystalline silicon transition) by H diffusion into the c- Si/seed a-Si:H layer interface, allows the maximal saturation of dangling bonds at the c-Si surface.

4.3. Front emitter ((i) a-Si:H / (p) a-Si:H)

This section is divided into four subsections, after an introduction of the importance and problematic of the front surface passivation and selective collection of holes, results of the experiments for the optimization of the process parameters are presented. In particular are investigated the effect of: (i) variation of the intrinsic and doped layers' thicknesses on passivation quality, shown in section ; (ii) variation of precursor gasses flow and change in activation energy and diborane diffusion, shown in section and (iii) variation of RF power in order to obtain a delicate but stable plasma, shown in section
.

4.3.1. Introduction and motivation

When designing the front emitter for n-type bulk cell,, two main issues needs to be addressed, (i) provide chemical passivation by saturating dangling bonds (as seen in section 4.2) and (ii) perform good carrier selectivity. The (p) a-Si:H layer, to have good carrier selectivity, has to form a barrier for electrons which are moving toward the front. This can be achieved by a sufficient high band off set (ΔE_c). At the same time, on the opposite, as to allow holes to move toward the front such that they can be collected. This can be achieved by holes tunneling of the smaller and narrow barrier (ΔE_c). The heterojunction band diagram of the precursor is shown in figure 4.5.

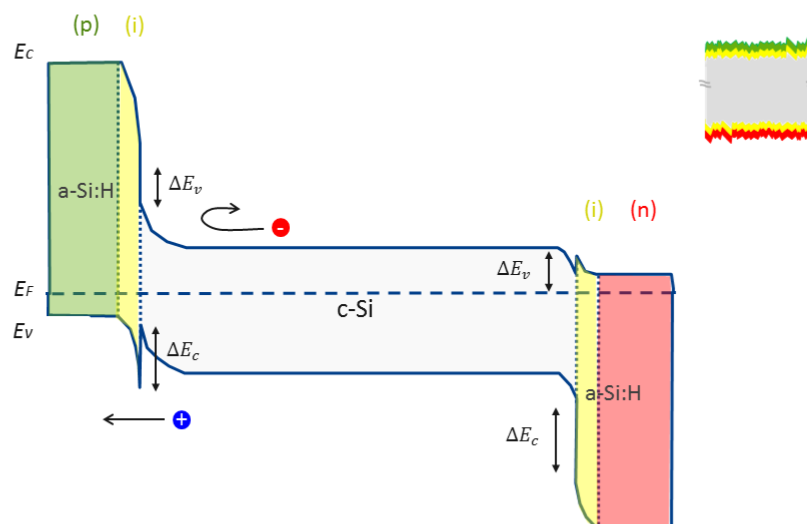


Figure 4.5 – Band diagram of a precursor solar cell and in particular showing the band off-sets ΔE_c and ΔE_v and the carriers transport.

One of the most challenging part when designing a solar cell is finding the optimal emitter layer. On one side an highly (p) doped layer is desired in order to obtain an high field effect passivation by inducing an high electric field and high band bending (hence selectivity). On the other side a highly doped layer is a very defective layer. To make the situation even more critical is the effect of borane atoms which can diffuse in the intrinsic layer degrading the chemical passivation.

Figure 4.6 shows the effect of low doped layers in terms of bandgap alignment and junction formation. A higher doping lead to a higher V_{oc} since the fermi level gets closer to the valence and conduction bands.

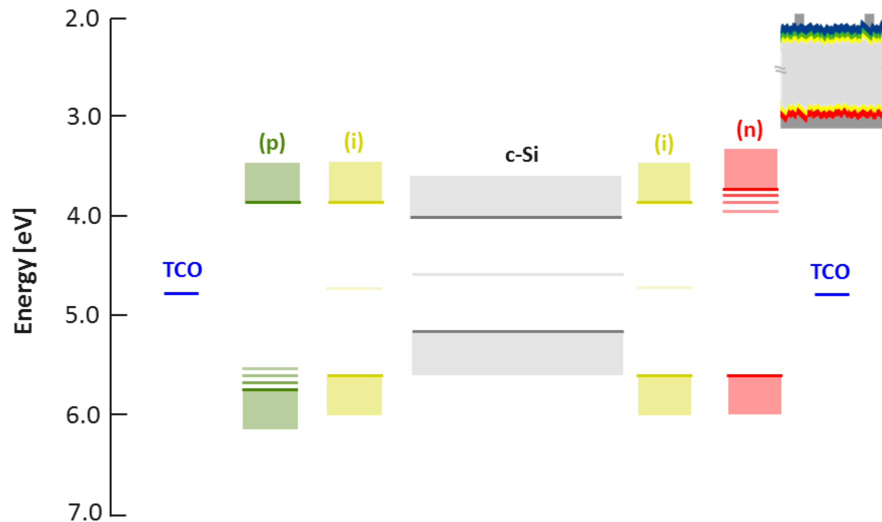


Figure 4.6 – Energy levels before the junction formation and variation of doped a-Si bandgap with variation of doping level.

The deposition process has to be optimized to find a trade off between optical and electrical characteristics. The thickness of the intrinsic layer has to be thin to reduce parassitic absorption, but think to decrease surface defect density.

A proper passivation scheme cannot be implemented with an (i) a-Si:H / c-Si / (i) a-Si:H structure, but rather with a (p) a-Si:H / (i) a-Si:H /c-Si / (i) a-Si:H / (p) a-Si:H structure, therefore the (p) doped layer has influence on the electronic properties of the interface, due to unavoidable borane diffusion into the intrinsic layer. The optimization of the (i)/(p) stack is complex because different combination of thicknesses need to be tested. Generally the overall stack has to be enough thin in order to minimize parassitic absorption. But, for example, the FF and V_{oc} are influenced by the (i) layer thickness in a contrary way: the FF benefits from a thin layer, thanks to an enhancement in tunneling and hopping of holes, while the V_{oc} benefits from a thick layer, thanks to a better passivation [63].

4.3.2. Deposition parameters

This part of the report presents the results of the experiments carried on (i) layers thickness, (ii) precursor gasses flow and (iii) variation of RF power.

Optimization of a-Si:H layers thicknesses

Intrinsic a-Si:H layer thickness affect the interface passivation quality, therefore, as shown in table 4.5, the lifetime increases with the increase in thickness of the intrinsic layer.

Table 4.5 – Symmetric structures (p)a-Si:H / (i)a-Si:H / c-Si / (i)a-Si:H / (p)a-Si:H with varying intrinsic thickness (note: this values are obtained for only 1 NAOC cycle cleaning).

$a - Si : H(i)$ $[nm]$	$a - Si : H(p)$ $[nm]$	τ_{eff} $[\mu s]$
3	8	221
4.5	8	353
6	8	638
7.5	8	908

However the passivation quality is not solely determined by the intrinsic layer, therefore the doped layers also influences the electrical and chemical properties at the interface [64]. In this set of experiments the passivation quality will be analyzed by comparing precursor structures with varied thicknesses of (i) a-Si and (p) a-Si stack. The inspected range of variation of the thicknesses is 4 nm and 6 nm for the intrinsic layer and from 5.2 nm to 10 nm for the p-doped layer (see figure 4.7).

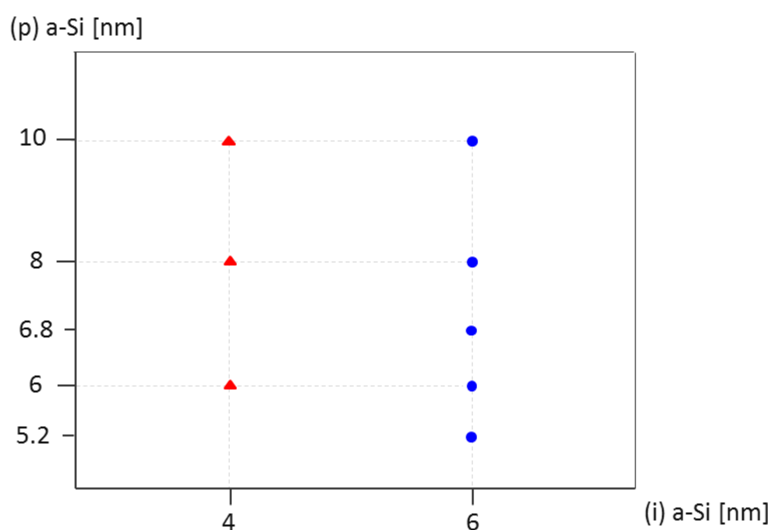


Figure 4.7 – Matrix of the samples fabricated to test the optimal i/p a-Si:H stack thicknesses.

All the precursors prepared for these sets of experiments are textured and cleaned with 3 NAOC. They have identical BSF and differ only in the i/p thicknesses.

In the first set of experiments the i/p stack will consist of: fixed *double intrinsic* layer (2 nm of a-Si+ 4 nm of a-Si:H) and varied the p layer thickness (5.2 nm, 6 nm and 6.8 nm). From figure 4.8 we can see the results of the passivation analysis. The best passivation is obtained for the stack 6 nm + 6 nm = 12 nm.

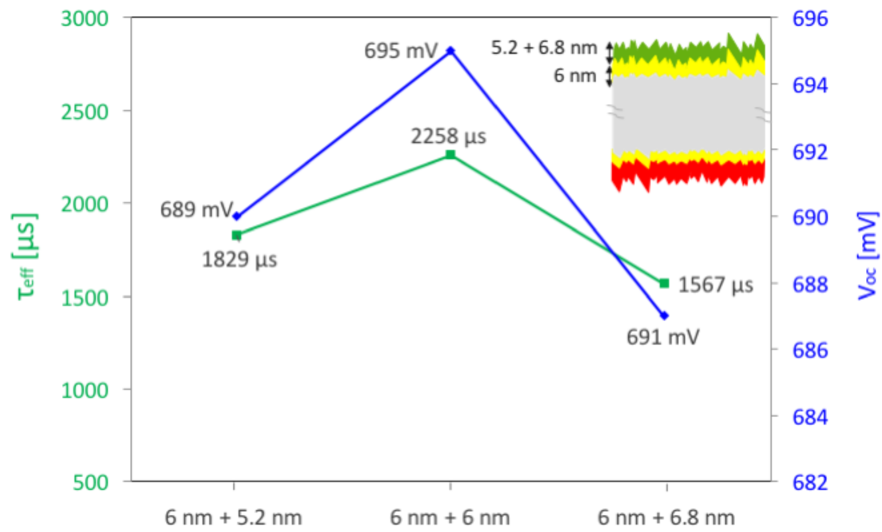


Figure 4.8 – Minority carriers lifetime (τ_{eff}) and iV_{oc} as function of variation of emitter layer thickness (5.2 nm, 6 nm and 6.8 nm) and *double intrinsic* layer = 2 nm of a-Si+ 4 nm of a-Si:H.

In a second set of experiments it has been reduced and kept fixed the intrinsic thickness to 4 nm (2 nm of (i) a-Si and 2 nm of (i) a-Si:H) and varied the p layer thickness (6 nm, 8 nm and 10 nm). From figure 4.9 can be seen that the best passivation is obtained for the stack 4 nm + 8 nm = 12 nm.

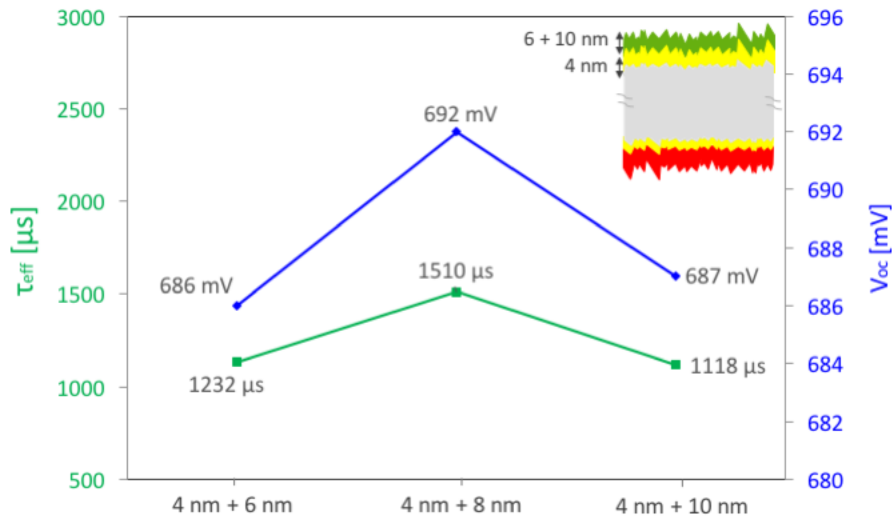


Figure 4.9 – Minority carriers lifetime (τ_{eff}) and iV_{oc} as function of variation of emitter layer thickness (6 nm, 8 nm and 10 nm) and (i) a-Si:H thickness = 4 nm.

Comparing the two set of experiments, it is evident that the two highest passivations are obtained for the stacks which have overall thickness of 12 nm. However the average τ_{eff} value in the second set is lower. Which is because the intrinsic layer is too thin and do not provide sufficient passivation.

Conclusion cannot be drawn until full devices performances are compared, this is because of the effects that the TCO has on the thin i/p stack. This is particularly due to: (i) the deposition method of the TCO, which is a strong ion-bombardment which may damage the a-Si film and (ii) the junction formation between the emitter and the TCO, which may affect the emitter/c-Si junction or induce an

energy barrier due to the TCO workfunction. Two cells were fabricated for the best performing cell of each set of experiment and the external parameters of the cells are reported in table 4.6.

Table 4.6 – External parameters of the SHJ solar cells for different i/p a-Si:H thicknesses. Note that this characteristics are taken from DIE 1 of both cells which does not necessarily coincide with the best performing DIE.

	$characteristics$	$J_{sc}[mA/cm^2]$	$V_{oc}[mV]$	$FF[\%]$
solar cell 1	$(i)a-Si:H$ 6 nm + $(p)a-Si:H$ 6 nm	39.1	694	59
solar cell 2	$(i)a-Si:H$ 4 nm + $(p)a-Si:H$ 8 nm	36.8	672	61

The J_{sc} of the cell with i/p = 4 nm / 8 nm is 2.3 mA/cm^2 less than the 6 nm / 6 nm cell, given that the front metal grid and TCO material are the same, the cause for the decrease in J_{sc} is that the (p) a-Si layer is more absorbive than the (i) layer and, while the 30 % of the carrier absorbed by the (i) a-Si:H can be collected, no carriers absorbed by the (p) a-Si:H can be collected due to the high defect density of the material [65].

The increase in FF is given by three main reasons: (1) the (p) layer used has high activation energy (this issue will be addressed in the next section) and using a thicker layer will decrease the weakening influence of workfunction difference between the TCO and the (p) layer; (2) a better lateral conductivity of the doped layer with respect to the intrinsic layer [66] lead to lower series resistance, hence higher fill factor and (3) the FF benefits of a thinner (i) layer because it enhances the holes tunneling of the hetero-junction.

The external parameter on main interest in this series of experiments is the V_{oc} since we are now addressing the issue of obtaining high passivation. The V_{oc} is mainly influenced by the chemical passivation provided by the intrinsic layer. Evidently the thinner (i) layer has lower passivation cababilities and high recombination take place on the interface.

Despite the fact that in this devices were used the optimized i/n stack and TCOs (presented in section 4.4 and 5.2). The external parameters of this devices, and specifically the FF, is lower with respect to the best performing devices obtained in this thesis work, the explanation relies on the adopted front and back metallization. Which are, respectively, 2 μm of aluminum in the front and 1.2 μm of aluminum in the back. In section 5.3 simulations and experiments have been carried out for different metals and improvements were obtained.

As it will be seen in the next section, (p) a-Si:H layer is responsible to deteriorate the passivation quality. This is because boron atoms penetrate the intrinsic layer and break Si-H bonds resulting into a defective interface. When a thicker (p) layer is adopted, the sample is subject to boron injection for a longer time which lead to stronger degradation of the intrinsic passivation.

Doping precursor gasses' flow variation for p-layer

The band bending on the emitter side is essential to obtain a high selectivity of holes and it is mainly influenced by: (i) the band offsets between a-Si:H and c-Si and (ii) by the doping of the a-Si:H layer. Given that the band gap of the a-Si is taken to be 1.72 eV and that the valence band offset is 0.45 eV [67] we wan work on the doping of the emitter to minimize the activation of p-layer and therefore increase the selectivity.

It is common to find in literature *qualitative* analysis of selectivity (namely is based on a simple principle: the junction block one carrier type and conduct the other), however it is difficult to find a *quantitative* analysis which defines the selectivity of a given material.

To do so we have to start by defining of the basic transport mechanism in a *pn junction*. When a *pn junction* is under illumination excess electron-holes pairs are generated. The concentration of majority carrier doesn't change significantly while the concentration of minority carriers strongly increases; the electrons and holes concentration profile is shown in figure 4.10 [7].

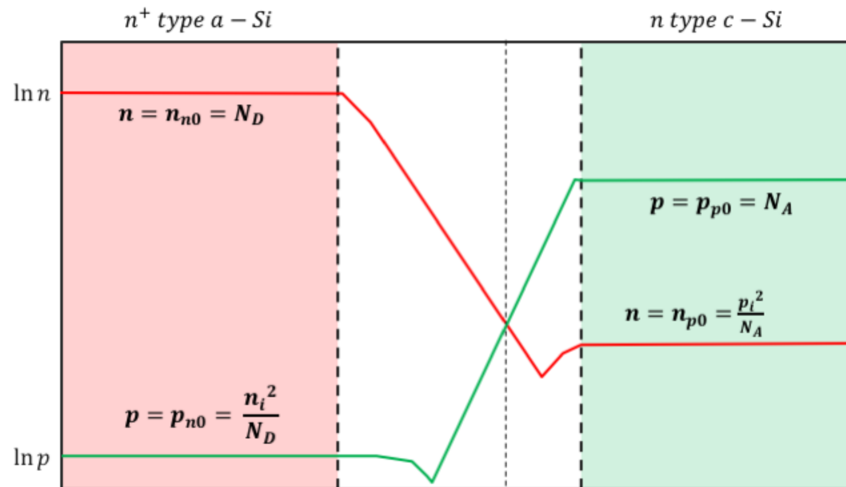


Figure 4.10 – Concentration profile in an illuminated *pn heterojunction* (with uniform generation-rate approximation).

Because there is a gradient of carrier concentrations, a diffusion current will form. The minority carrier drift component can be neglected since it is assumed that the electric field is zero at the space charge edges [10]. The current density equation is therefore composed only of the diffusion terms. Figure 4.11 shows the carriers current density component in the depletion region and quasi-neutral region of a *pn junction*.

From the figure it can be noticed that the total current is constant though the *pn junction* and it is given by the sum of the minority carrier electron diffusion and the minority carrier hole diffusion. The total current density is then:

$$J = J_p(x_n) + J_n(-x_p) \tag{4.1}$$

based on mathematical manipulations (not shown here) it can be written as function of applied voltage V_a:

$$J = J_0 \cdot [exp(\frac{eV_a}{kT} - 1)] \tag{4.2}$$

Where kT/e is the thermal voltage, V_a is the applied voltage and J_0 is the saturation current which is defined as:

$$J_0 = e \cdot n_i^2 \cdot [\frac{D_n}{L_n \cdot N_A} + \frac{D_p}{L_p \cdot N_D}] \tag{4.3}$$

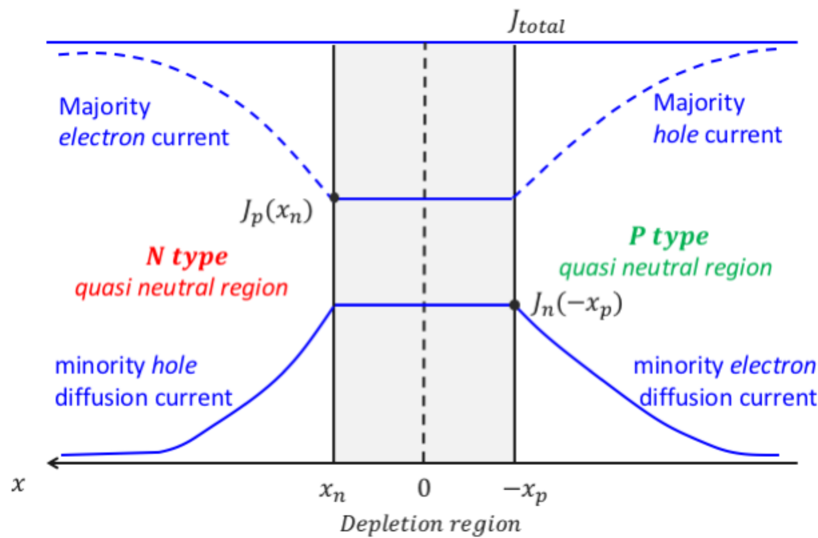


Figure 4.11 – Ideal electron and hole current components though a *pn junction* under forward bias.

Where n_i is the intrinsic carrier concentration in the semiconductor material, D_p and D_n are diffusion currents of holes and electrons, L_p and L_n are the diffusion lengths of minority carriers and N_D and N_A are the impurity carrier concentrations.

To obtain an high current though the *pn junction* it is desired to have a low saturation current. To obtain low saturation current we can increased the doping.

The key criterion for increasing selectivity is now clear. By increasing the doping of the emitter the material selectivity increases [68] [69].

Thus in this section of experiments it is addressed the issue of doping, whose variation determines the density of effective fixed charges in the films and the band bending.

(p) a-Si:H/(i) a-Si:H symmetric structures are fabricated. The deposition characteristics are shown in table 4.7.

Table 4.7 – PECVD deposition parameters for the emitter. The diborane flow is varied between 0.75 to 4.5 $sccm$ while the other process parameters are kept constant. Note that the PECVD reactor injection flux of B_2H_6 is limited to 4.5 $sccm$.

	$(p)a-Si:H$
Chamber	1
SiH_4 flow [$sccm$]	1.5
H_2 flow [$sccm$]	200
B_2H_6 flow [$sccm$]	$0.75-4.5$
Substrate temperature [$°C$]	180
Process pressure [$mbar$]	2.5
Power density [W]	7.2
Layer thickness [nm]	6

Figure 4.12 shows the lifetime and activation energy E_a values for varying B_2H_6 flow from 0.75 to 4.5 $sccm$. τ_{eff} gives information about passivation quality. E_a gives information about the doping level

of the semiconductor material.

By definition the activation energy is the energy required by a particle to overcome a potential barrier and it is dependent on the Fermi level: $E_a = E_F - E_v$. For an intrinsic semiconductor at T= 0 $°C$ $E_a = \frac{1}{2} \cdot E_g$. The lower is the activation energy, the higher is the doping of the semiconductor [70].

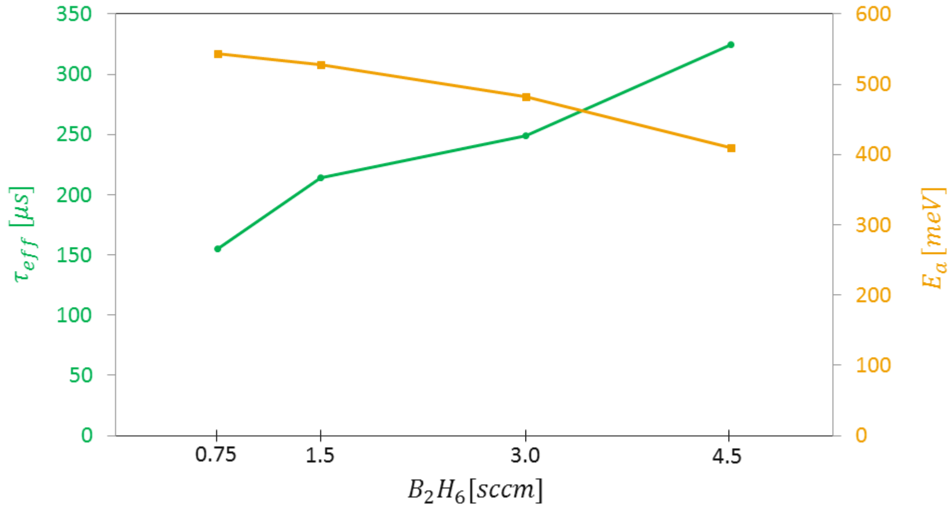


Figure 4.12 – Minority carriers lifetime (τ_{eff}) and activation energy E_a as function of B_2H_6 flow rate which ranges from 0.75 to 4.5 $sccm$. For the other PECVD deposition parameters of the emitter refer to table 4.7. The activation energy was measured in the *dark IV* set up, and layers of 20 nm were deposited on glass.

The lifetime increases with increase in doping of the p-layer, this behaviour is expected since the highest V_{oc} is obtained when the Fermi level in the (p)/(n) a-Si layers is as close as possible to the valence/conduction band. In addition, from the theory on the selectivity explained above, it is clear that high doping means high selectivity, which is what we aim at obtaining.

Figure 4.13 shows the *IV curves* of two solar cells fabricated with the lowest doped emitter (E_a = 543 meV)(blu line) and the highest doped emitter (E_a = 410 meV)(red line).

The blue line shows a *S-shape* in the high voltage level, this indicates high R_s and bad selectivity of holes.

A second important issue need to be addressed and it is related to the chemical bounds that the diborane causes: We have seen that an increase in doping determines a decrease in activation energy. The lowest E_a obtained is 410 meV that is still quite high (compared to the BSF which has an E_a = 212 meV).

However a further decrease in E_a would lead to negative effects on the passivation. This has been proven by a work performed by another student of the *PVMD group* and it is based on the recipe used so far in the *PVMD group*.

Table 4.8 summarizes the characteristics of the best performing emitter used in this thesis work with respect to the reference emitter used so far in the *PVMD group*.

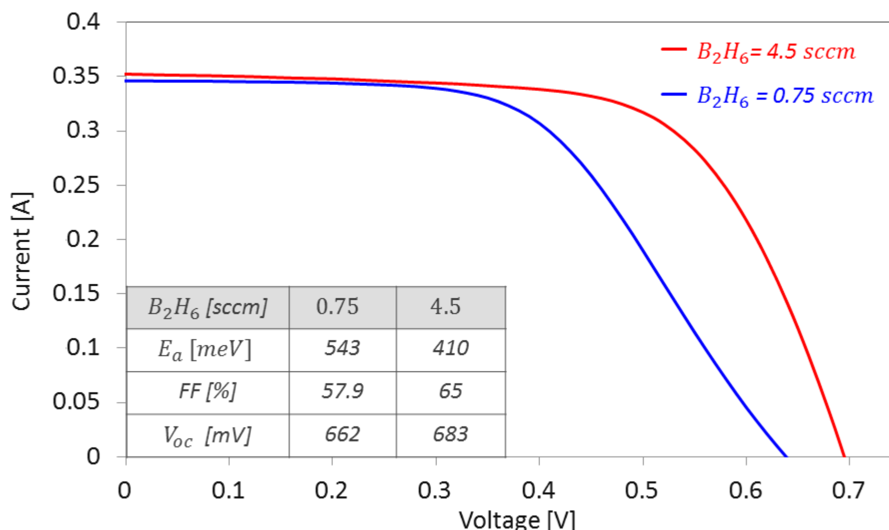


Figure 4.13 – *IV* characteristic of the SHJ solar cells with highly doped (B_2H_5 = 0.75 $sccm$) emitter (red line) and slightly doped (B_2H_5 = 0.75 $sccm$) emitter (blue). For the other p layer deposition specifications please refer to table 4.7. (note that even if they are not the best performing cells, DIE 2 of both cells have been chosen for comparison).

Table 4.8 – PECVD deposition parameters, activation energy and lifetime measurements of the emitter films used in this work with respect to the standard recipe used in the PVMD group [62].

	reference $(p)a-Si$	failed $(p)a-Si$	$(p)a-Si:H$
Chamber	1	1	1
SiH_4 flow [$sccm$]	20	20	1.5
H_2 flow [$sccm$]	-	-	200
B_2H_6 flow [$sccm$]	**1**	**5**	4.5
Substrate Temperature [$°C$]	180	180	180
Process pressure [$mbar$]	0.7	0.7	2.5
Power [W]	2.8	2.8	7.2
E_a [meV]	608	317	410
τ_{eff} [μs] (symmetric)	350	< 50	908
τ_{eff} [μs] (precursor)	1483	–	3400

A crucial drawback of the reference emitter was that an increase in B_2H_6 lead to detrimental effects on the passivation, therefore it has been reported that with a emitter gasses flow of B_2H_6 = 5 $sccm$ and SiH_4 = 20 $sccm$ even though the activation energy decreased to 317 meV, the passivation dropped to $\leq$ 50 μs proving that an elevate quantity of doping destroy the chemical passivation.

This is because boron is a small and reactive particle which can bound and diffuse into the intrinsic layer. As consequence the passivation is deteriorated since the boron particles introduce defects on the passivating layer [64]. This effect is specifically drastic in the used a-Si:H film because of the highly diluted and reactive plasmas used [41].

One more time, the critical part of the fabrication is to find the optimal trade off between high band

bending and low defect density [71].

Influence of RF power

The a-Si:H film growth conditions vary the physical and structural properties of the material. In this set of experiment it is aimed to find a proper power regime while keeping a fixed medium pressure regime of 2.5 $mbar$. Table 4.9 gives an overview of the samples fabricated, an increase in RF power determines an increase in deposition rate.

Table 4.9 – PECVD deposition parameters. The power regime vary from low (2.6 W) to high (7.2 W) while all other parameters are kept constant. In particular the precursor gasses flow is the one which presented best performance from the previous experiments and the pressure is fixed at a medium regime.

$SiH_4[sccm]$	$B_2H_6[sccm]$	$H_2[sccm]$	$p[mbar]$	$P[W]$	$rate[nm/s]$
1.5	4.5	200	2.5	2.6	0.025
1.5	4.5	200	2.5	4.8	0.033
1.5	4.5	200	2.5	7.2	0.039

Lifetime measurements reveal that the best passivation come from a power P = 7.2 W (same power used for the intrinsic layer), since at this condition the plasma is stable and the power soft on the fragile thin layer [72].

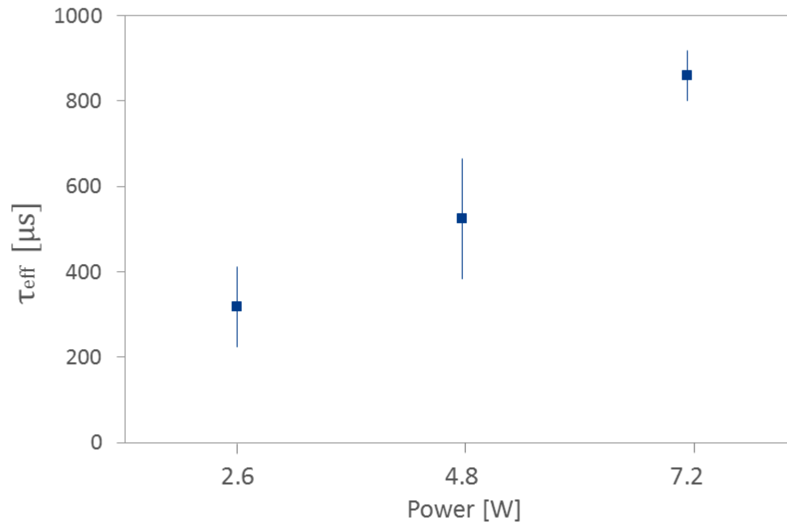


Figure 4.14 – Passivation as function of deposition power which vary between 2.6 W and 7.2 W.

4.4. Back surface field ((i) a-Si:H / (n) a-Si)

In this study, we focus on the optimization of the BSF with particular focus on the effect of the contact with the back metal. Thanks to simulation analysis with *Sentaurus* it is proposed an optimal (i/n) stack thickness. Experimental test evidence that the used (i) a-Si:H / (n) a-Si:H stack guarantee an excellent electron selective contact.

Introduction and Motivation

The electron carrier selective contact in the SHJ cells designed in this work is created by depositing highly doped (n) a-Si layer on the rear side of the c-Si substrate. A very thin (i) a-Si:H layer is inserted to provide chemical passivation. The PECVD deposition parameters for the (i) a-Si:H / (n) a-Si:H stack are reported in table 4.10.

Table 4.10 – PECVD deposition parameters for the BSF.

	$(i)a-Si:H$	$(n)a-Si$
Chamber	4	2
SiH_4 flow $[sccm]$	4	40
H_2 flow $[sccm]$	200	–
PH_3 flow $[sccm]$	–	11
Substrate Temperature $[°C]$	180	180
Process pressure $[mbar]$	8	0.6
Power density $[W]$	7.2	2.6

The back side designed in this work fulfill three main requirements: (i) intrinsic layer provide excellent surface passivation, which contribute to the reduction of recombination losses, (ii) the (n) doped layer present a very low activation energy (E_a = 212 meV), which guarantee the appropriate high band bending for a selective collection of electrons, (iii) a good electrical contact with the metal is achieved, which contributes to limit the series resistance of the device.

Figure 4.15, is the result of simulations for the c-Si / (n) a-Si and (n) a-Si / metal hetero-junctions.

The c-Si / (n) a-Si junction has to facilitate the transport of electron and blocks the holes. With an highly doped (n) a-Si layer the spike at the conduction band is quite reduced and the electrons' transport across the junction is provided by thermionic emission and tunnelling mechanisms. At the valence band, thanks to the high offset, holes are effectively pushed back, diminishing the carrier recombination probability.

The connection of (n) a-Si and the back metal determines the formation of another hetero-junction which results in a local band bending and in a variation of the effective E_a of the a-Si:H layer. The depletion region will rely mostly in the (n) a-Si:H part. If this depletion region will penetrate in the (i) a-Si and c-Si it will affect also the c-Si / a-Si junction. In section 4.4.1, the optimal thickness of the BSF is found by simulations. Depending on the difference of workfunctions (ΔWF = ϕ_{metal} - ϕ_{a-Si}) a schottky barrier may form, this issue is addressed in section 5.3.3.

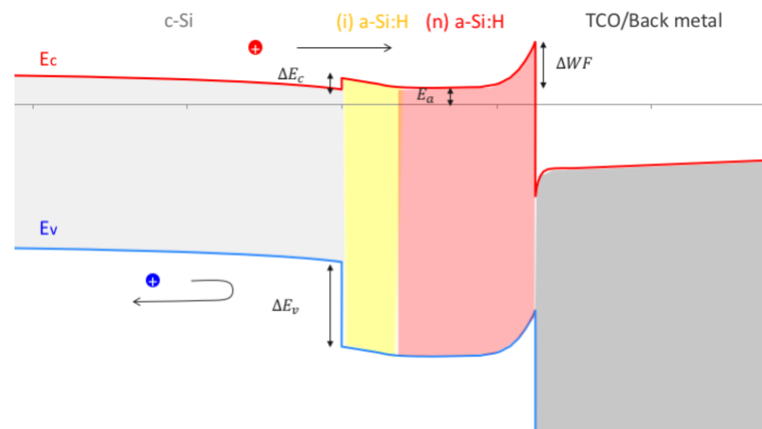


Figure 4.15 – Band diagram of $c-Si$ / $(n)a-Si$ hetero-junction and $(n)a-Si$ / back contact as calculated with the *Sentaurus* simulation tool. E_a = 0.2eV, E_g = 1.7 eV χ_{a-Si} = 3.9 eV, ϕ_{metal} = 4.26 eV.

4.4.1. Optimization of a-Si layers thicknesses

N-type wafers, symmetrically passivated with (i) a-Si:H / (n) a-Si:H show higher lifetime than wafer passivated with just intrinsic layers, this is because the (n) a-Si provide field effect passivation in addition to the chemical passivation (provided by (i) a-Si:H) [4]. However the study of the passivation quality with only with a symmetric structure does not provide a complete picture of the situation. Therefore the a-Si:H/metal junction influence the transport and interface properties of the back side of the solar cell. The design optimization of the BSF has been carried out with simulation on *Sentaurus* and solar cell device fabrication has been done to confirm the simulated results.

The depletion region width of a *pn junction* is given by:

$$w = \sqrt{\frac{2\epsilon_s \cdot (V_{bi} - V)}{e \cdot N_D}} \tag{4.4}$$

where ϵ_s is the dielectric permittivity, V_{bi} difference between the semiconductor and metal work function, V is the applied voltage and N_D is the donor concentration.

Equation 4.4 shows the relation between the depletion width and the doping level, in particular w is inversely proportional to the doping.

This relation implies that in the metal side of the junction, the depletion width w is negligible, while on the semiconductor side it is few nm thick. If the depletion region is thicker than the (n) a-Si:H then the metal/ (n) a-Si:H junction will influence also the c-Si / (n) a-Si:H junction.

Figure 4.16 shows the results of the simulation carried to address the issue of optimization of the BSF thickness.

The worse case is the 4.5 nm + 6 nm structure, for which and increase in recombination in the c-Si/a-Si junction is caused by an induced band bending. This effect can be neutralized with a thicker n layer.

Two cells have been tested to compare the effective performances for the 4.5/6 and 3/7.5 thicknesses. The precursor with thicknesses 3/7.5 present a τ_{eff}= 2300 μs which shows that 3 nm of (i) a-Si layer is sufficient to provide high passivation. In section 5.2 the possible detrimental effect of the back TCO sputtering/metal e-beam evaporation on the thin a-Si layer is treated in detail.

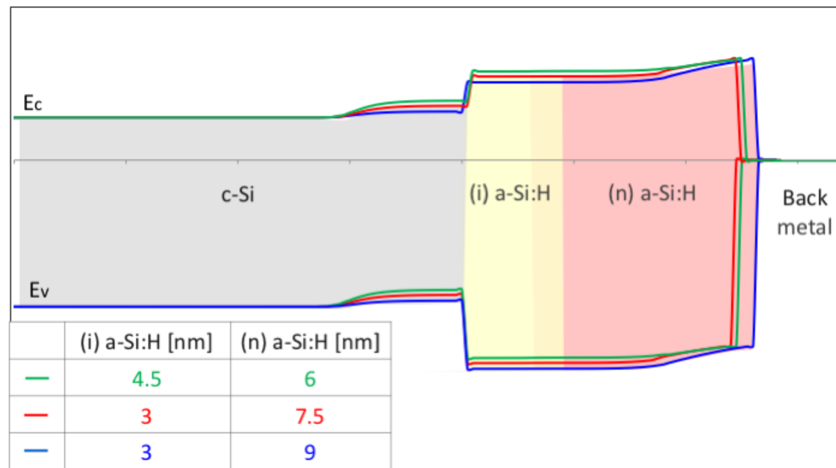


Figure 4.16 – (n) a-Si / back metal junction effects on c-Si - (i) a-Si band bending. In this case it has been simulated an (n) a-Si$_{H}layerwithahigher$E$_{a}$ in order to stress on the induced c-Si band bending.

4.5. Conclusions

The influence of plasma-enhanced chemical vapour deposition (PECVD) process parameters on the properties of amorphous layers is investigated with the aim of enhancing the passivation quality and the external parameters of the solar cells.

- *How to increase the surface passivation of the c-Si?*

Firstly, the intrinsic layer is optimized. On this purpose the distance specimen-plasma is investigated, and 8 mm resulted to be the optimal distance that avoids plasma damage and ensures film uniformity. Then the precursor gasses flow (SiH_4 and B_2H_6) is studied. A film with diluted silane is willed since it lowers the voids density of the film and improves passivation, however too much hydrogen changes the microscopic structure of the film and lead to epitaxial growth, which has detrimental effects on passivation. This thesis proposes a passivation mechanism where in between c-Si and the (i) a-Si:H layer is introduced a non-hydrogenated intrinsic layer, the *seed layer*. The so called *double intrinsic layer* is formed by a first layer, adjacent the c-Si, of 2 nm and which has SiH_4 = 40 as only precursor gas. The second layer is of 4 nm and has an high hydrogen content (precursor gasses: SiH_4 = 4 $sccm$ and H_2 = 200 $sccm$). With this structure we aimed at preventing the growth of the epitaxial layer as well as at the reduction of defects density state and enhance the transportation of minority carriers toward the selective contacts. The seed layer protects the c-Si bulk from the high hydrogen bombardment which would introduce micro-structural damage on the crystallographic structure and the highly diluted film (close to the amorphous-to-crystalline silicon transition) allows the maximal saturation of dangling bonds.

- *How does the thickness of i-p stack affect the passivation quality of HIT solar cell?*
- *How to find the optimal trade-off between a low activation energy and an high passivation quality for the front emitter?*

The study of the front emitter has been one of the most challenging part of this work, since it is well known that the (p) a-Si:H layer is responsible to hamper device performance. A trade-off between

optical (parassitic absorption) and electrical (passivation and FF) characteristics needs to be found when designing the thicknesses of the (i/p) stack. Experimental evidence showed that the optimal thicknesses are 6 nm for both intrinsic and emitter layers.

Moreover, a trade-off between carrier selectivity (high doping) and induced defects on the intrinsic layer needs to be addressed. The problem is related to the fact that when the E_a of the (p) a-Si:H decreases, the amount of boron introduced in the structure increases. These particles are highly reactive and small, hence they can diffuse into the passivating layer which would result in a defective interface with the c-Si. One more time, the critical part of the fabrication was to find the optimal trade-off between high band bending and low defect density, we concluded that the gasses flow for the emitter should be H_2 = 200 $sccm$, SiH_4 = 1.5 $sccm$, B_2H_4 = 4.5 $sccm$ at high power regime = 7.2 W and medium pressure regime = 2.5 $mbar$. With this emitter E_a = 410 meV and τ_{eff} = 3400 μs were obtained. Compared to the reference emitter which had a E_a = 608 meV and τ_{eff} = 1483 μs. It should also be noted that the (p) a-Si:H layer employed is highly hydrogenated which prevents the formation of an highly defective layer and favors the formation of Si-H bonds by further improving the chemical passivation.

- *How to design the optimal BSF?*

The (n) a-Si:H layer employed in this work has a very low activation energy (E_a = 212 meV) and it is able to induce a strong electrical field. The BSF/back contact junction is critical because it may cause an induced band bending in the c-Si/ (n) a-Si junction, which would lead to more recombination. This effect can be neutralized with a thicker n layer.

5

Front and Back-end Fabrication Process Experiments

This chapter offers an analysis of the differences in electrical and optical properties of TCO materials. A double TCO layer formed by $IO{:}H/ITO$ is proposed as alternative to the reference ITO single layer. Finally, different metallization techniques and materials are proposed in order to address the issue of a low FF due to high metal series resistance.

The chapter is organized as follow: section 5.1 summarizes the full device fabrication process; in section 5.2 is presented a double $IO{:}H/ITO$ stack as alternative to the reference single ITO layer. Lastly, in section 5.3 copper front metal contact is proposed as alternative to aluminum contact.

5.1. Experiment set up

Starting from an n-type FZ c-Si (100) wafers, with resistivity 1 - 5 $\Omega \cdot cm$ and thickness of 280±20 μm, the solar cell fabrication process is as follows:

1. Wet chemical *texturization* and *cleaning* (as seen in section 3.3);
2. Front *emitter* and *back surface field* deposited by PECVD (as seen in section 4.3and 4.4);
3. *Transparent conductive oxide* (TCO) deposited by RF sputtering;
4. *Front metal* contacts deposited by thermal and electron-beam evaporation or alternatively by electroplating;
5. *Back metal* contact deposited by thermal and e-beam evaporation.

Transparent conductive oxide films are deposited by radio frequency sputtering, which is a physical vapor deposition technique based on the bombardment of high energetic argon ions. Two different dopant indium oxide films are tested in this work: (i) *Indium Tin Oxide* (ITO), where In_2O_3 is doped with SnO_2 and (ii) *Hydrogenated Indium Oxide* (IO:H), in which H_2O vapor is inserted in the gas flux in order to incorporate hydrogen into the In_2O_3. The process parameters used are shown in table 5.1 [73].

Table 5.1 – TCO sputtering process parameters.

	$IO:H$	ITO
Target	$Ln_2O_3:H$	$Ln_2O_3:SnO_2$
Substrate Temperature [$°C$]	room	110
Process pressure [Pa]	5.7×10^{-3}	1.2×10^{-2}
H_2O partial pressure [Pa]	3×10^{-5}	-
Power [W]	$25 - 135$	200
Ar flow [sccm]	40	40
O_2 flow [sccm]	0	0

RF sputtering is a hard deposition method which may damage the thin amorphous films. To address this issue, a gradual increase in deposition power has been adopted for the two TCOs that have been tested during this thesis work:

1. The first TCO is formed by $IO:H$ and ITO. The stack is composed by 65 nm of $IO:H$ and 10 nm of ITO. The first 10 nm of $IO:H$ were deposited at 25 W, the next 55 nm of $IO:H$ were deposited at 135 W and the last 10 nm of ITO were deposited at 200 W; this last layer of ITO is inserted because the contact resistivity between ITO and metal is lower than the contact resistivity between the $IO:H$ and the metal [31].
2. The second TCO is formed by 75 nm of ITO. For this single ITO layer, initial sputtering power of 20 W was used for 10 nm and the other 65 nm were deposited at 200 W.

The gradual increase in deposition power guarantee a softer deposition in the part close to the a-Si:H and high electrical properties of the TCO achieved with high deposition power [74]. $IO:H$ needs a post-deposition annealing at $190°C$ for 25 minutes such that the deposited amorphous film crystallizes.

Front metal contacts are deposited by thermal and electron-beam evaporation or alternatively by electroplating. When *aluminum* is used as contact, photolitography is used to make the pattern: few micrometers of photoresist are deposited on the sample by spin coating, then the sample is exposed to ultraviolet light though a mask with the desired pattern. Then the wafer with the developed photoresist, is placed in the evaporator. In this way the photoresist protect the part of the surface of the wafer where the metal should not be deposited. After the evaporation the photoresist is dissolved in the acetone and with it also the metal that was deposited on top. The aluminum is now present only in the areas where no photoresist was present and it has a typical height h = 2 μm.

When *copper* is used as contact, a seed layer need to be deposited before the copper. The seed layer has three main tasks: (i) protect the Si from Cu contamination (copper is an heavy metal and it can diffuse easily into silicon causing defects states of the bulk), (ii) it is a conductive layer for the electroplating process, (iii) the ITO dissolves when a negative current is fed to it, so it has to be isolated from the electrolyte solution. In this work 300 nm of titanium are used as seed layer, and it is deposited by e-beam evaporated. After the photoresist layer is deposited and photolitography make the pattern, the sample can be immersed in the electrolyte solution; the current is conducted though four clamps attached to the wafer. After plating, the photoresist is removed by rinsing in acetone. The last step is the wet etching of the Ti seed layer. The cupper has typical height h = 40 μm.

Back metal contact is composed by a stack of 200 nm of Ag thermally evaporated, 30 nm of Cr and 1.5 μm of Al e-beam evaporated.

For each wafer four solar cells are obtained (each with an area A_{cell} = 9 cm^2) with different coverage in order to study their influence on the solar cell performances. The percentage of shading is DIE1 = 4.9%, DIE2 = 2%, DIE3 = 2.64%, DIE4 = 3.64%. Therefore, it is expected to find the highest J_{sc} in DIE 2, because of the lowest shading percentage, while the highest FF is expected from DIE1 due to the better carrier collection (mainly due to a lower series resistance because of the higher metal fraction).

The cell characterization is obtained with (i) *EQE measurement* and (ii) illuminated *IV solar simulator* (as seen in section 2.6). The TCO electrical and optical characterization is obtained with (i) *four-point probe method*, to calculate the sheet resistance and (ii) *Perkin-Elmer 950 spectrophotometer*, to measure trasmittance and reflectivity [73].

5.2. Transparent Conductive Oxide

5.2.1. Introduction and Motivation

An important difference of SHJ solar cells with respect to conventional homojunction arises from the very low conductivity (σ) of a-Si:H. In SHJ cells a *transparent conductive oxide* (TCO) layer is inserted between a-Si:H and the metal in order to enhance lateral conductivity and increase the collected photogenerated carriers.

Most commonly used TCO is *indium tin oxide* (ITO). Its material properties have been studied extensively and the sputtering deposition parameters have been optimized. Recently, however, *hydrogenated indium oxide* ($IO{:}H$) is gaining interest thanks to it's electrical and optical properties. Normally the TCO is inserted in between the a-Si films and the front and back metals. The front TCO is clearly essential due to the need for lateral transport. On the back side, instead, the metallization is full area, however often the TCO is used since it increases the internal reflection, thus the light absorption, and also it decreases the metal absorption from the back side. The thicknesses are modulated such that the front TCO has maximum transparency at around 450 nm, while the back TCO at around 800 nm.

In order to choose the optimal material, we have to understand which are the characteristics that the ideal TCO should have:

- High *electrical conductivity* (σ) to act as carrier transport medium;
- High *optical transparency* (T) to minimize the parasitic absorption;
- A *refractive index* that is the geometric mean of those of silicon and air (n_{Si} = 4.2 and n_{air} = 1) to serve as anti-reflection coating

As mentioned above, the first requirement for a good TCO is the high conductivity. By definition the conductivity, σ [$\Omega \cdot cm$], is given by the following equation:

$$\sigma = \mu \cdot N_e \cdot e \tag{5.1}$$

where: μ = mobility [$\frac{cm^2}{Vs}$], N_e= carrier density [cm^{-3}], e= electric charge [$1.602 \cdot 10^{-19} C$].

Secondly, the TCO should be transparent and by definition a material become transparent to a given *EM wave* propagation when the material plasma frequency is lower than the *EM wave* plasma

frequency. It is therefore desired that the plasma frequency of the TCO is as low as possible, such that it is transparent to most of the light hitting it. The plasma frequency is defined as:

$$f_{pe} = \frac{1}{2\pi} \cdot \sqrt{\frac{4 \cdot \pi \cdot N_e \cdot e^2}{m^*}} \tag{5.2}$$

where: N_e= carrier density [cm^{-3}], e = electric charge [$1.602 \cdot 10^{-19} C$] and m^*= effective mass of the electron [kg].

It should be noticed that the carrier density (N_e) is present in both equations 5.1 and 5.2. To obtain an high conductivity, N_e should be as high as possible; on the contrary, to obtain high transparency, N_e should be as low as possible. Therefore, a trade off between the electrical and optical properties of the material has to be be found [75]. Typical values of carrier density for ITO and $IO{:}H$ are: $N_{e_{ITO}} = 10^{-19} - 10^{-21} cm^{-3}$ and $N_{e_{IO:H}} = 10^{-20} cm^{-3}$ [74]. The other term that appears in equation 5.1 is the mobility (μ), which is defined as:

$$\mu = \frac{e \cdot \tau}{m^*} \tag{5.3}$$

where τ is the relaxation time and hence the mobility, which is dependent on (i) the crystalline structure, (ii) the defect density and (iii) the grain size of the material. ITO typically has mobility μ = 20-40 $cm^2V^{-1}s^{-1}$, while $IO{:}H$ after deposition has mobility $\mu_{deposition}$ = 50 $cm^2V^{-1}s^{-1}$, which is improved by annealing to $\mu_{annealing}$ = 150 $cm^2V^{-1}s^{-1}$.

5.2.2. $IO{:}H$-ITO double TCO layer as alternative to ITO single layer

In this section, the analysis of different TCO materials is presented. As mentioned above, the TCO should be highly transparent and conductive. The ITO is most commonly used because it fulfills both requirements, however, as seen in the previous section, a difficulty arises from the opposite influence that the carrier density (N_e) has on electrical (σ) and optical (T) properties. A trade-off has to be found between high conductivity and high transparency. One way to overcome this limitation is to increase the mobility, which increases the material conductivity. On this respect, the ITO has low mobility value, while $IO{:}H$ seems an interesting alternative since it has high mobility ≥ 100 $cm^2V^{-1}s^{-1}$. On the other hand, ITO/metal contact has lower contact resistivity than $IO{:}H$/metal.

Two solar cells have been fabricated with the identical characteristics, besides the TCO. One cell had ITO and the other had $IO{:}H/ITO$. In both cells the thicknesses were as follow: 75 nm at the front and 120 nm at the back. Figure 5.1 shows a comparison of the EQE curves. The main difference is present in the short wavelength range (from 400 nm to 500 nm) where $ITO/IO{:}H$ performs better.

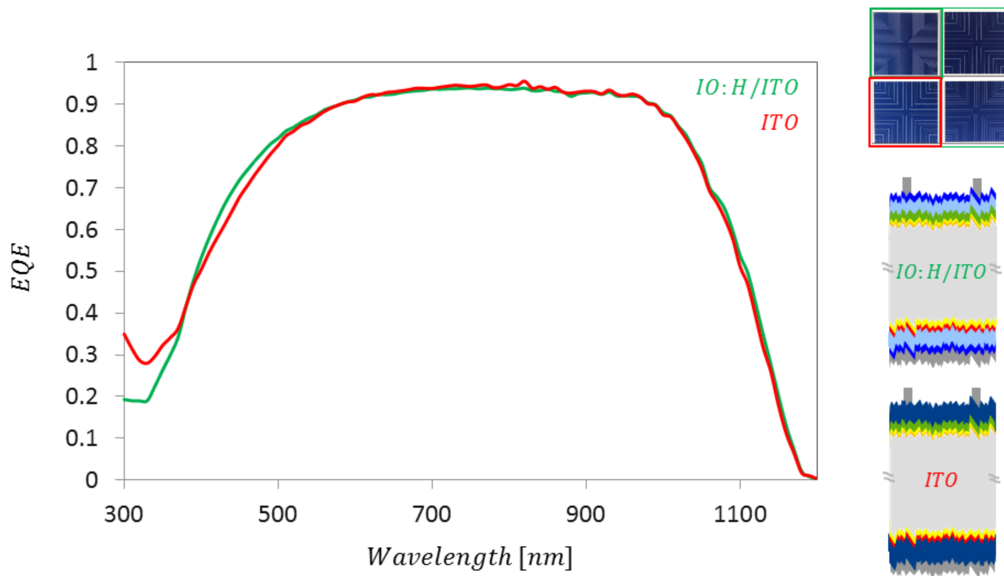


Figure 5.1 – Measured external quantum efficiency (EQE) as function of the wavelength of the fabricated SHJ-HIT solar cells with TCO deposited at the front and the back. Two TCO materials are compared: standard ITO (red line) and $IO{:}H/ITO$ stack (green line).

In order to understand the difference in EQE shapes we can refer to the absorption spectra of $IO{:}H/ITO$ stack and ITO. From 5.2 it can be noticed that $IO{:}H$ is less absorptive in the short wavelengths [76].

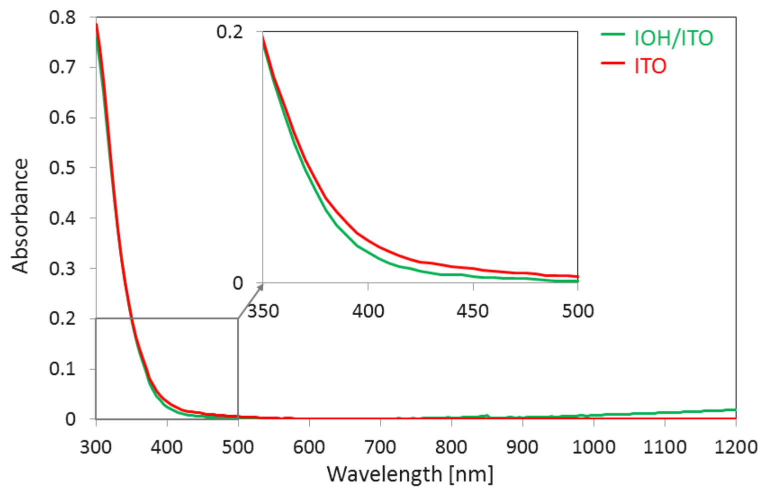
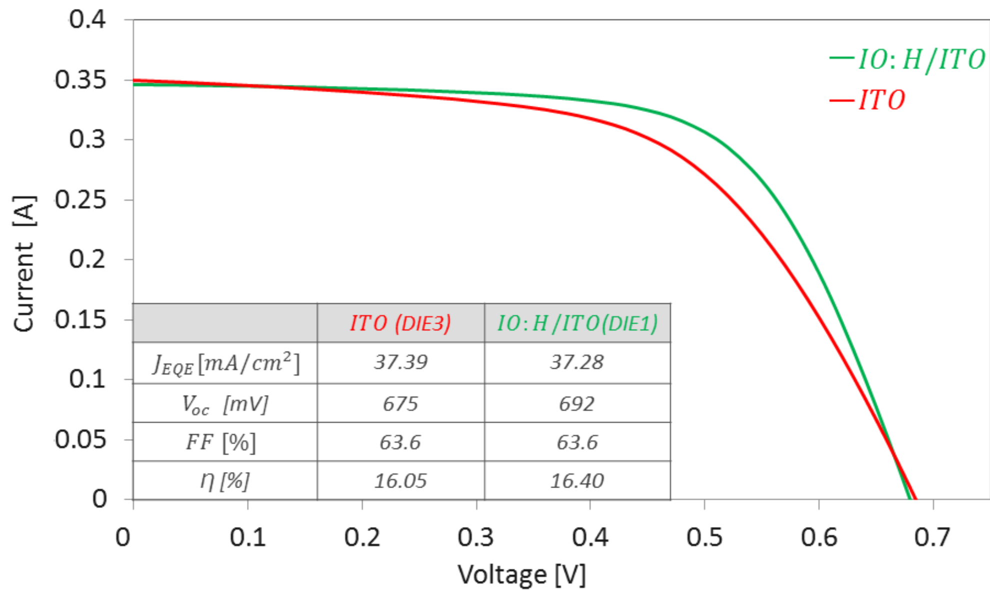


Figure 5.2 – Absorption spectra for ITO (red line) and $IO{:}H/ITO$ stacks (green line) ($IO{:}H$ film annealed 25 minutes at 180 $°C$ in air). An insert it presented in the plot to highlight the short-wavelength range of the spectrum. The absorbance is obtained by the formula $A = 1 - T - R$. Data extracted from [76].

Figure 5.3 shows the comparison of the I-V curves: a pronounced difference is in the V_{oc} and FF. After TCO sputtering the samples presented a degradation in passivation. When $IO{:}H$ was used, annealing recovered the sputtering damage, while it could not be recovered in the cells with ITO.

In order to understand the FF values we have to look at the R_s and R_{sh}. The series resistance is slightly lower in the ITO samples. $R_{s_{ITO}}$ = 3.08 $\Omega \cdot cm^2$ and $R_{s_{IO:H/ITO}}$ = 3.78 $\Omega \cdot cm^2$. Several

factors influence the value of the series resistance, such as the resistivity of the TCO and the contact resistance between the TCO and the metal. Measurements with the *four probe method* have been done to determine the resistivity values of the two materials, but the results obtained are unreliable since there was a problem on reproducibility. even though the $R_s(IOH)$ is higher than that for $R_s(ITO)$, the IO:H cell shows the same FF as the ITO cell, which may related to the workfunction difference of ITO and IO:H which determines the barrier height between TCO and amorphous silicon layers.



	ITO (DIE3)	$IO:H/ITO$(DIE1)
$J_{EQE}[mA/cm^2]$	37.39	37.28
V_{oc} [mV]	675	692
FF [%]	63.6	63.6
η [%]	16.05	16.40

Figure 5.3 – *IV* characteristic of the SHJ solar cell with ITO (red line) or $IO{:}H/ITO$ stack (green line).

One of the most significant difference between the two TCOs is their respective behavior upon annealing. A series of experiments on variation of with varying annealing times have been tested on $IO{:}H$. When the oven is at 190 $°C$ the optimal annealing time is 25 minutes. Figure 5.4 shows the lifetime of: the precursor (blu), the sample after the TCO sputtering (red) and after 25 minutes of annealing (green).

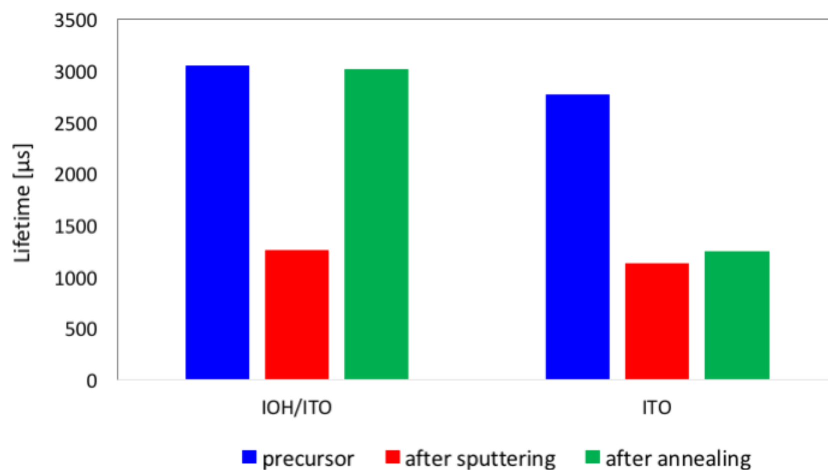


Figure 5.4 – Effect of RF sputtering and annealing on the lifetime of samples with $IO{:}H/ITO$ and ITO.

The sputtering process causes a damage on passivation. However, the lifetime of the $IO{:}H/ITO$

stack can be recovered thanks to the crystallization of the $IO{:}H$ at high temperature. In the case of ITO the annealing does not help. This is a critical point, since the sputtering is a rather strong deposition technique, which damages the thin a-Si layer and, regardless the fact that the power has been calibrated to minimize this damage, still cannot be prevented. Annealing also affects the electrical characteristics of the $IO{:}H/ITO$ stack, whose mobility before annealing is μ = 60 $cm^2V^{-1}s^{-1}$ and after annealing it increases to μ = 120 $cm^2V^{-1}s^{-1}$. The mobility of the ITO remains in the range μ = 25-28 $cm^2V^{-1}s^{-1}$.

5.2.3. Backside TCO influence

Figure 5.5 shows the effect of the back side $IO{:}H/ITO$ on the EQE. As expected, there is a negligible difference in EQE for all the wavelengths below 1000 nm, while between 1000 $nm \leq \lambda \leq$ 1200 nm, when the back $IO{:}H/ITO$ is applied, a small increase in EQE can be noted.

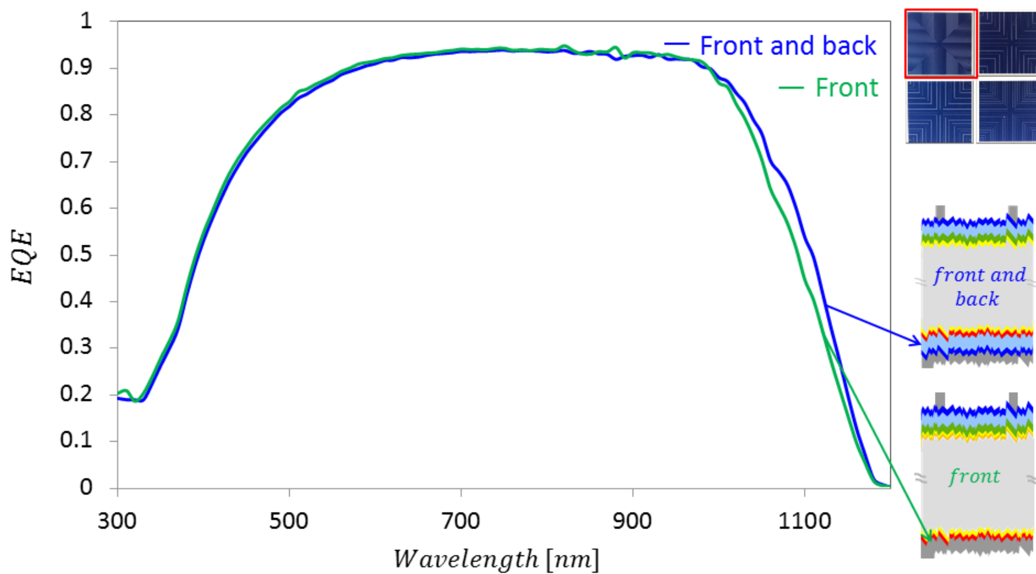
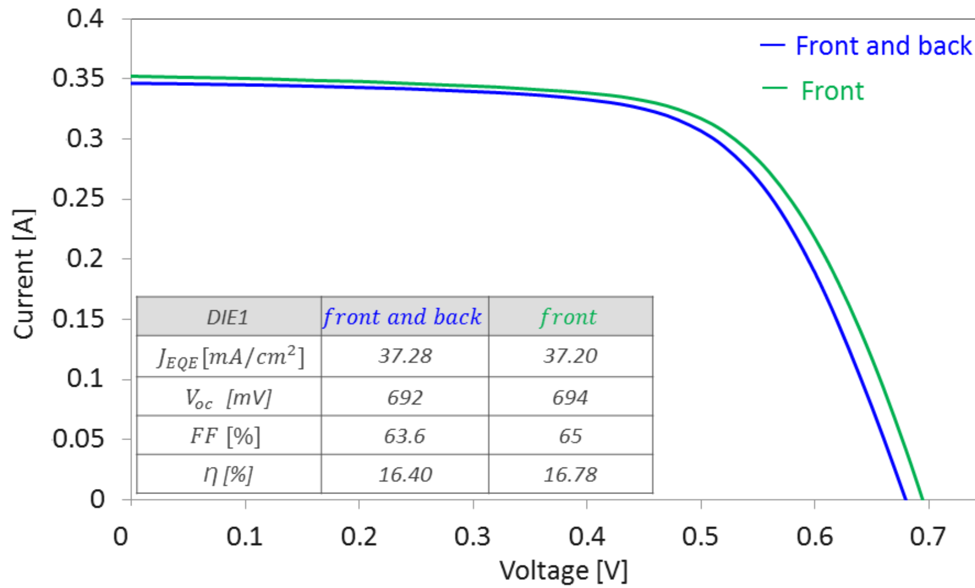


Figure 5.5 – Measured external quantum efficiency (EQE) as function of the wavelength of the fabricated SHJ-HIT solar cells with 75 nm of $IO{:}H/ITO$ deposited at the front and either no TCO in the back (green line) or 120 nm of $IO{:}H/ITO$ deposited at the back (blu line).

Figure 5.6 shows the performance differences of the solar cell with and without back TCO. As deduced from the EQE, the J_{sc} of the cells with back TCO is higher because of the light absorbed from the back side. Due to the fact that internal reflection comes from the back side TCO layer. At the same time, the lower reflective index induces the smaller absorption from the metal.

The V_{oc} and FF of the cells without back $IO{:}H/ITO$ are higher than those with back TCO. In order to understand this difference we can analyze table 5.2, which shows the implied open circuit voltage (iV_{oc}) and the real device V_{oc}. The iV_{oc} is measured on the precursor, while the V_{oc} is the voltage of the final device, so after the TCO sputtering. The reduction in V_{oc} indicates that the TCO decreases the passivation quality. This concern is addressed by different research groups which are trying to find a softer deposition technique, since the sputtering damages the ultra-thin a-Si layers due to particle bombardment over prolonged timing. Studies carried with FTIR about the microstructural changes of a-Si:H prove that sputtering (and post-annealing) changes the hydrogen bonding, specifically lead to dangling bonds originated from the rupture of Si-H or Si-Si bonds [77].



DIE1	front and back	front
$J_{EQE}[mA/cm^2]$	37.28	37.20
V_{oc} [mV]	692	694
FF [%]	63.6	65
η [%]	16.40	16.78

Figure 5.6 – *IV* characteristic of the SHJ solar cell with $IO{:}H/ITO$ deposited at the front (green line) and at the front and back (blu line).

The very low FF is a sign of low shunt or high R_s. The pFF is defined as the fill factor when R_s is not taken into account. Hence, the 18.1% difference between the pFF and the FF in the front/back TCO sample is a sign of high R_s. The high R_s probably results from a barrier in the (n)a-Si/TCO contact. Therefore, ideally, to form an ohmic contact with the n-doped (a)-Si:H the work function of the TCO should be as close as possible to the workfunction of the (n) a-Si:H. Considering that $X_{a-Si(n)}$ = 3.9 eV, $\chi_{IO:H}$ = 4.6 - 4.8 eV, χ_{ITO} = 5.3 - 5.4 eV and χ_{metal} = 4.07 - 4.26 eV, we can conclude that the work function mismatch between the BSF and the TCO may lead to a strong decrease in FF.

Table 5.2 – Implied open circuit voltage iV_{oc}, real open circuit voltage $real\ V_{oc}$, pico fill factor pFF and real fill factor FF values for two solar cells fabricated with 75 nm of $IO{:}H/ITO$ deposited at the front and one without back TCO while the other with 120 nm of $IO{:}H/ITO$.

$IO{:}H/ITO$ stack	front and back	front only
iV_{oc} $[mV]$	702	707
$real\ V_{oc}$ $[mV]$	692	694
pFF [%]	81.4	77.8
FF [%]	63.3	65.0
$pFF - FF$ [%]	18.1	12.8

We can conclude that the HIT solar cell with TCO deposited at the back can gain in photo-generated current, but this gain cannot counterbalance (i) the reduction of FF resulting from the contact resistivity among the (n) BSF / (n) TCO and TCO / metal interface and (ii) the reduction in V_{oc} which results from the damage of thin a-Si:H due to the hard sputtering process. However, the deposition parameters and the post annealing have been already optimize to minimize the sputtering counter-effect. For this reasons the the TCO at the back is not employed in this research.

5.3. Metallization

At this point of the work we obtained devices with very high value of current (J_{ph} = 40.4 mA/cm^2) and voltage (V_{oc} = 694 mV). Nevertheless, the performances of the cells were still limited due to the low fill factor.

Metallization has crucial influence on FF, therefore in section 5.3.2 we aim at increasing the FF by testing two front metallization techniques and in section 5.3.3 the optical properties and the carrier transport mechanism are analyzed for different metals of the back metallization.

5.3.1. Introduction and motivation

The fill factor is mainly influenced by the and parallel resistances. To understand their effect on the IV characteristic we can refer to the equivalent circuit of a solar cell with one diode and see how each of them deviate the *IV curve* from the ideal ”squared” shape.

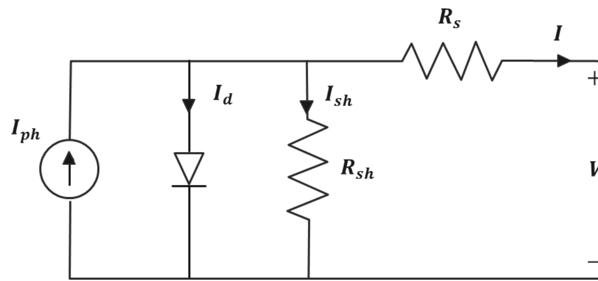


Figure 5.7 – Equivalent circuit diagram of the solar cell including the parasitic series and shunt resistances.

The governing equation for this circuit is given by Kirchoff’s current law:

$$I = I_{ph} - I_D - I_{sh} \tag{5.4}$$

Where I_{ph} is the light-generated current in the cell, I_D is the current through the diode and I_{sh} the current lost due to shunt. Equation 5.4 can be re-written in the extended form:

$$I = I_{ph} - I_0[exp(\frac{V + IR_s}{n \cdot V_T} - 1)] - (\frac{V + IR_s}{R_{sh}}) \tag{5.5}$$

where I_0 is the saturation current, n is the diode ideality factor, V_T is the thermal voltage, R_s is the series resistance and R_{sh} is the shunt resistance. On the purpose of focusing on the fill factor, we are mainly interested in the R_s and R_{sh} terms. The shunt resistance in the equivalent circuit is in parallel, which means that it is desired to have it as high as possible. A decrease in R_{sh} will mainly affect the low voltage range of operation where the *IV curve* will acquire higher negative slope. On the opposite, a lower R_s is desired. Indeed, the influence of the series resistance in the *IV curve* can be seen towards the open-circuit voltage, where a high R_s will increase the slope of the curve.

On a fabrication point of view the **shunt resistance** arises from a fabrication fail, for example a short circuit of the device by connecting the front and back TCO that offers an alternative path for the current which will not follow anymore the external circuit hence power will not be extract from the solar cell. The **series resistance**, instead, is mainly composed by three parts: (i) the *lateral resistance* $R_{lateral}$

of the emitter (already addressed in chapter 4), (ii) the *metal resistance* R_{metal}, critical for the front metallization, and (iii) the *contact resistance* $R_{contact}$, critical in the back metallization and related to the (n) a-Si:H / metal junction transport mechanism.

$$R_s = R_{lateral} + R_{metal} + R_{contact} \tag{5.6}$$

In the next section we will get insight on R_{metal} and $R_{contact}$ and we will try to reduce them by testing different metal contact [78].

5.3.2. Front metallization

This part of the experiment focuses on obtaining low series resistance, which will determine an increase in FF by acting on the metal resistance (R_{metal}). The latter is defined as:

$$R_{metal} = \frac{\rho \cdot l}{h \cdot w} \tag{5.7}$$

Where ρ is the electrical resistivity, l is the length and $(h \cdot w)$ is the area of the section of the finger/busbar. Equation 5.7 shows that it is desired to have a low metal resistivity and high $A_{fingers}$ to obtain a low metal resistance. The resistivity ρ is a material property and table 5.3 shows the values of the used metals.

Table 5.3 – Electrical resistivity of used metal for the front metallization. The higher the resistivity, the stronger the metal opposes to the flow of electric current. The resistivity of silicon (semiconductor) is also provided as comparison value. All ρ are calculated at $20°C$ [79].

	$\rho\ [\Omega \cdot m]$
Aluminum	$2.8 \cdot 10^{-8}$
Copper	$1.68 \cdot 10^{-8}$
Silver	$1.59 \cdot 10^{-8}$
Silicon	$6.4 \cdot 10^{+2}$

To reduce R_{metal}, the $A_{fingers}$ should be as big as possible, however an increase in $A_{fingers}$ would determine an increase in optical shadowing, unless the only the height (h) and not the width (w) of the fingers is increased. In other words we aim to obtain a high aspect ratio, which is defined as:

$$Aspect\ Ratio = \frac{h}{w} \tag{5.8}$$

In the *PVMD group*, aluminum is the standard metallization material used for the front contact of c-Si based solar cells, nevertheless the e-beam evaporation of aluminum limits the height of the fingers to $2\mu m$, holding the aspect ratio to $\backsim 0.02$ [80]. We are therefore driven to test different metallization techniques, for which higher fingers height can be achieved. On this respect, two groups of samples were fabricated to be compared: (i) SHJ with aluminum e-beam evaporated and (ii) SHJ with copper electroplated.

Figure 5.8 shows the IV characteristics of the final devices metallized both with copper and aluminum. It also illustrates the external parameters and from these we can see that the cell metallized with copper has lower J_{sc} and V_{oc}, but the FF is 6.5% higher compared to aluminum. This determine

an overall improvement in the performance of the solar cell, whose power conversion efficiency is η = 18.44%, compared to η = 17.71% obtained with Al metallization.

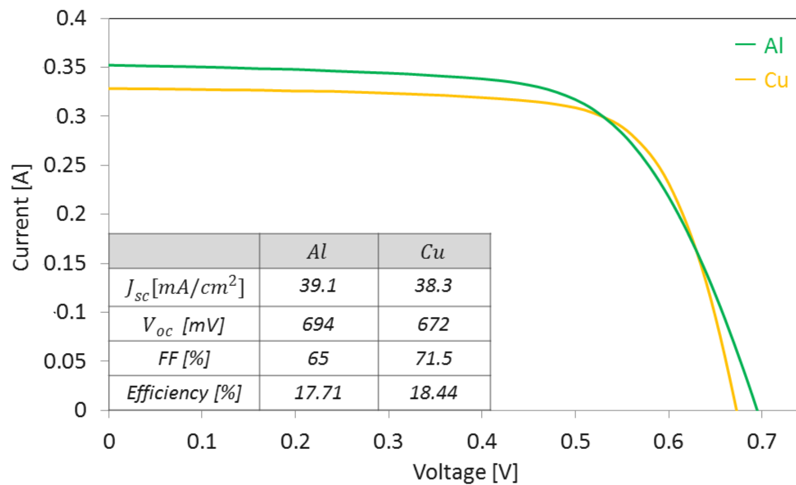


Figure 5.8 – I-V characteristic of the SHJ solar cell (DIE 2) with Copper and Aluminum front metallization (the J_{sc} is given by the EQE measurement and then corrected for the shading losses).

Since the V_{oc} with copper is lower than the one obtained with aluminum, interesting conclusions can be drawn by comparing their V_{oc} before and after metallization (refer to table 5.4). In both cases the iV_{oc} is higher than 700 mV, however after copper is deposited there is a drop of 33 mV (while in the case of aluminum is only 13 mV), this indicates that the copper has a detrimental effects on the SHJ.

Table 5.4 – iV_{oc} and $real\ V_{oc}$ with front metallization with Aluminum or Copper.

metallization	Copper	Aluminum
iV_{oc} $[mV]$	705	707
$real\ V_{oc}$ $[mV]$	672	694

To understand the cause for the decrease in V_{oc} we have to consider the drawbacks that copper metallization involves: firstly, copper has poor adhesion on TCO, secondly it diffuses through the a-Si and contaminates the c-Si damaging the performance of the cell. To solve this issues, a seed material can be deposited between the TCO and the metal. Optimal candidates are nickel and titanium, which can improve the adhesion of fingers and form barrier against copper diffusion. Nickel can be chemically grown, but this process has not yet been optimized in our group. Hence, we opted for titanium that is deposited by e-beam evaporation, which, in turns, may damage the under-layers due to high energetic particle bombardment.

The lower J_{sc} obtained with copper is caused by a decreased carrier transport at the junction between the (n) TCO / Cu. Since the TCO workfunction is χ_{TCO} = 4.6 - 4.8 eV and, being an n-doped material, it is desired to connect it to a metal with a similar work function, thus forming a Schottky barrier [32]. In literature we find that the work function of aluminum is 4.07-4.25 eV, while the work function of copper is 4.6-4.7 eV [81].

5.3.3. Back metallization

In the previous section we saw that, by fabricating contacts with high aspect ratio, we could reduce metal resistance and shadow losses at the front of the SHJ device. In this part of the thesis we focus on the back metallization. Here, there is no shadow related issue and hence it is possible to fully cover the back side of the SHJ, lowering the R_{metal}. However, now the $R_{contact}$ becomes critical and we have to understand which are the characteristics of the material for which the contact resistance is minimized.

The contact resistance depends mostly on the band diagram at the junction between the metal and the semiconductor. The metal work function will determine the formation of either an *accumulation contact* or a *depletion contact*:

1. In the **depletion contact** a Schottky barrier will form and its height is given by the difference between the metal work function (ϕ_{metal}) and the semiconductor workfunction (ϕ_{a-Si}) (this is in fact a simplified and idealized definition of Schottky barrier, but in reality it is also a function of the surface states and the electric field in the semiconductor) [82][83].

   Simulation on *Sentaurus* have been implemented in order to study the effect of different metal work functions on the band bending of the (n) a-Si:H layer. The relevant parameters used for the simulation are listed in table 5.5.

Table 5.5 – Relevant input parameters used for simulations with *Sentaurus*. The thickness of the semiconductor layer has been settled to 20 nm in order to avoid the effect of penetration of the $(n)a - Si : H$ / metal depletion region in the bulk.

	a-Si (n)	metal
Thickness $[nm]$	20	1500
Electron affinity / workfunction $[eV]$	3.9	4.26 − 2.74
Bandgap $[eV]$	1.72	−
Activation energy $[meV]$	212	−

   Figure 5.9 shows the resulting band diagram. The worse case is for an increase in χ_{metal} because it would lead to and increase in barrier height.

   Given that silver has workfunction $\chi_{Ag} \simeq$ 4.5 eV, in the (n) a-Si:H / Ag junction a Schottky barrier will form. However, the (n) a-Si:H is highly doped an this will allow the barrier to be narrow, hence allowing electrons to tunnel it. The low difference $\chi a - Si - \phi metal$ determine a low Schottky barrier, hence few electron can overcome it by thermionic emission.

2. In the **accumulation contact** the carrier can flow over the junction with no contact resistance and therefore this is the junction we are willing to obtain. Simulations were carried in which all parameters are kept the same (as shown in table 5.5) but the metal work function is varied in the range 4.03 - 4.09 eV

   Considering that aluminum has workfunction $\chi_{Al} \simeq$ 4.07 eV, in the (n) a-Si / Al junction is ideal, since the current can flow toward the metal with no contact resistance.

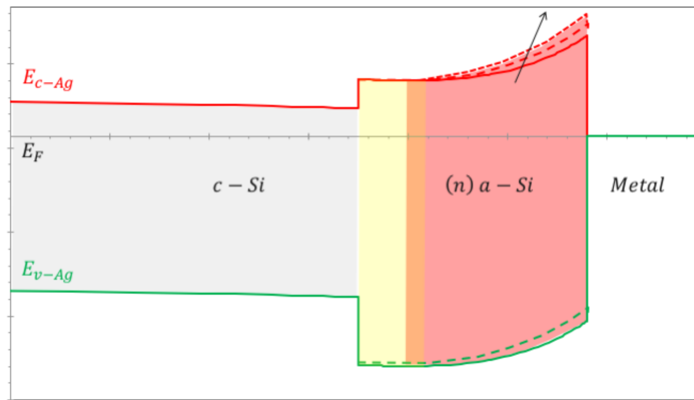


Figure 5.9 – The simulation result shows the schematic band diagram of $(n)a - Si : H$ / metal hetero-junction. The metal work function is higher than $(n)a - Si : H$. E_a = 0.2 eV, E_g = 1.7 eV $\chi a - Si$ = 3.9 eV ϕ_{metal} = 4.3 - 4.7 eV. The arrow indicates the increase in work function mismatch.

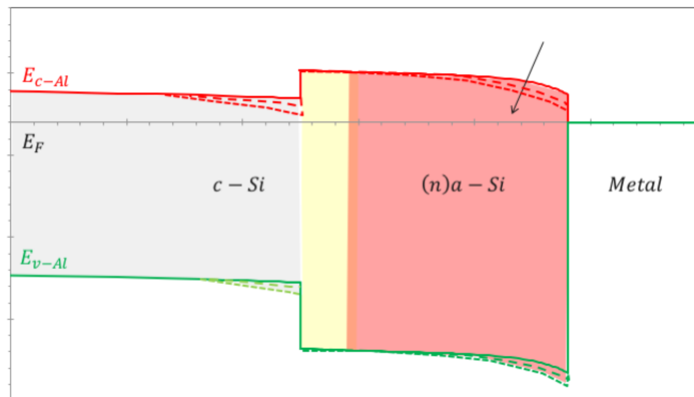


Figure 5.10 – Schematic band diagram of $(n)a - Si : H$ / $metal$ heterojunction with TCO work function lower than $(n)a - Si : H$. E_a = 0.2 eV, E_g = 1.7 eV $\chi a - Si$ = 3.9 eV ϕ_{metal} = 4.03 - 4.09 eV. The arrow indicates the decrease in work function mismatch.

From a carrier transport point of view aluminum is preferred over silver, nevertheless experiment results reveal that the back metallization with silver, chromium and aluminum (200 nm of Ag + 30 nm of Cr + 1 μm of Al) gives better performances, which has to be related to the good internal reflection given by Silver.

5.4. Conclusions

- *Which is the optimal material to be employed as TCO?*

Despite the several advantages offered by heterojunction, the a-Si:H suffers of very low conductivity. Therefore, the need for a conductive layer is necessary to foster later conductivity from the emitter to the front contact. For this task, a TCO layer is used and the optimal TCO should have (i) high electrical conductivity (σ) to act as carrier transport medium, (ii) high optical transparency (T) to minimize the parasitic absorption and (iii) a mean refractive index to serve as anti-reflection coating.

Two cells were fabricated with two TCO materials: the first TCO is formed by 65 nm of $IO{:}H$ and 10 nm ITO, the second TCO is formed by 75 nm of ITO. EQE curves show that the ITO generates less carriers in the short wavelength range, this is because of the absorbance of the ITO, which is higher with respect to the one of the $IO{:}H$ for short wavelengths. Sputtering has detrimental effects on the a-Si:H layer, due to the strong particle bombardment. After sputtering the lifetime of all the samples collapsed, however when the $IO{:}H/ITO$ stack is used the lifetime can be recovered thanks to the crystallization of the $IO{:}H$ at high temperature. Annealing has also positive effects on the electrical characteristics, indeed the mobility before annealing is μ = 60 $cm^2V^{-1}s^{-1}$ and after annealing it increases to μ = 120 $cm^2V^{-1}s^{-1}$. On the contrary, when ITO is employed the collapse in lifetime after sputtering cannot be recovered.

- *Does the back TCO influence positively the performance of the solar cell?*

Another set of experiment was carried to compare the effect of the back TCO. Two solar cells were fabricated with 75 nm of $IO{:}H/ITO$ deposited at the front. One was without back TCO while the other had 120 nm of $IO{:}H/ITO$. When back TCO is used an increase in EQE in the long wavelength is noticed, due to the increased internal reflection at the back, hence there is a gain in photogenerated current, however this cannot counterbalance the reduction in V_{oc} and FF. The low V_{oc} is, once more, a prove of the sputtering damages on the thin film. The low fill factor, instead, is sign of shunt or high R_s. The difference between pFF and FF is very high (pFF - FF = 18.1%), which implies the presence of high series resistance. The high R_s probably results from the workfunction mismatch at the a-Si(n) / TCO contact. Given that the electron affinity of the BSF is $X_{a-Si(n)}$ = 3.9 eV and that the workfunctions of the used TCO are $\chi_{IO:H}$ = 4.6-4.8 eV and χ_{ITO} = 5.3-5.4 eV, the resulting ΔWF is too high and it leads to Schottky barrier formation.

- *How to improve the metallization of the HIT solar cell by targeting an increase in FF?*

At this point of the work we obtained devices with very high value of current J_{ph} = 40.4 mA/cm^2 and voltage V_{oc} = 694 mV. Nevertheless, the performances of the cells were still limited due to the low fill factor. To address the issue of a low fill factor, an alternative metallization technique is used in the front. Thanks to electroplating we could grow copper fingers with height = 40 μm (compared to the reference Al fingers with height = 2 μm). The increase in finger height, hence aspect ratio, allows to drastically decrease the R_s. Two solar cells were fabricated with Al and Cu front metals, the cell metallized with copper has lower J_{sc} and V_{oc}, but the increase in FF by 6.5% determined an overall improvement in the power conversion efficiency η = 18.44% compared to η = 17.71% obtained with Al metallization. Potentially the cell fabricated with copper can be further improved, since the decrease in V_{oc} proved that copper diffused on the c-Si bulk destroying the passivation. In this cell 300 nm of seed material

(titanium) were deposited by e-beam evaporation, which may damage the under-layers due to high energetic particle bombardment. The lower J_{sc} obtained with copper is caused by a decreased carrier transport at the junction between the (n) TCO / Cu. Copper has higher workfunction than aluminum and this lead to the formation of a Schottky barrier in the (n) TCO / Cu junction.

At the back contact, depending on the magnitude of the workfunction of the metal either an *accumulation contact* or a *depletion contact* is formed. When low workfunction aluminum is used, an ohmic junction will form and the carrier can flow over the junction with no contact resistance.

6

Conclusions and Outlook

Pre-PECVD-deposition treatments are crucial to increase the performances of solar cells. Wafers are textured for 20 minutes in a solution of $4\ l$ of DI water, $1\ l$ of TMAH 25% and $120\ ml$ of *Alkatex Zero*. The resulting surface morphology has a uniform distribution of pyramids. Moreover, the probability of absorption of light is increased due to the fact that small pyramids (height = 0.5 μm) are surrounded by bigger pyramids (height = 4 μm), favoring the reflection of hitting photons. After texturization the wafers are cleaned through four *Nitridic acid oxidation cycles*. H_2 plasma treatment on the PECVD chambers is performed (50 $sccm$ of H_2 gas flow at p = 2 $mbar$ and P = 60 W for 10 minutes). Holder contamination is also an issue due to the residuals of boron atoms/molecules on the holders. An increase in lifetime was observed when the holders were pre-covered with 70 nm of dummy intrinsic layer.

The influence of *plasma-enhanced chemical vapour deposition* process parameters on the properties of amorphous layers is investigated with the aim of enhancing the passivation quality and the external parameters of the solar cells.

Firstly, the intrinsic layer is optimized. This thesis proposes a passivation mechanism where in between c-Si and the highly hydrogenated intrinsic a-Si:H layer, a non-hydrogenated intrinsic layer, the *seed layer* is introduced. With this structure, we aimed at preventing the growth of the epitaxial layer (with the intrinsic seed layer) as well as at the maximum saturation of dangling bonds (with the intrinsic highly hydrogenated layer) and at enhancing the transportation of minority carriers toward the selective contacts.

The study of the front emitter is very challenging, since the (p) a-Si:H layer is responsible for hampering the device performance. A trade-off between high carrier selectivity (high doping) and induced defects on the intrinsic layer needs to be addressed. The problem is related to the fact that when the E_a of the (p) a-Si:H decreases, the amount of boron introduced in the structure increases. These particles are highly reactive and small, therefore they can diffuse into the passivating layer resulting in a defective interface with the c-Si. Again, the critical part of the fabrication was to find the optimal trade-off, in this case between high band bending and low defect density. The emitter used (H_2 = 200 $sccm$, SiH_4 = 1.5 $sccm$, B_2H_4 = 4.5 $sccm$) has E_a = 410 meV and $\tau_{eff_{precursor}}$ = 3400 μs. Thus an improvement with respect to the reference emitter which had E_a = 608 meV and $\tau_{effprecursor}$ = 1483

μs was obtained. It should also be noted that the (p) a-Si:H layer employed is highly hydrogenated so it prevents the formation of a highly defective layer and favors the formation of Si-H bonds by further improving the chemical passivation.

At the back side, the (n) a-Si:H layer employed in this work has a very low activation energy (E_a = 212 meV) and it is able to induce a strong electrical field, while the (i) a-Si:H chemically passivates the dangling bonds. The BSF/back contact junction is critical because it may lead to a penetration of the band bending imposed at the BSF/metal junction through the entire BSF stack and diminish the c-Si band bending, which would lead to more recombination. This effect can be neutralized with a thick enough BSF layer.

Despite the several advantages offered by heterojunction, the a-Si:H suffers of very low conductivity. Therefore, a TCO conductive layer which fosters lateral conductivity from the emitter to the front contact is required. The optimal TCO should have (i) high electrical conductivity to act as carrier transport medium, (ii) high optical transparency to minimize the parasitic absorption and (iii) a mean refractive index to serve as anti-reflection coating.

The front TCO used is formed by 65 nm of IO:H and 10 nm ITO, this structure shows higher transparency and mobility while maintaining low resistance with the metal if compared to the reference TCO. Annealing of IO:H/ITO is essential to crystallize the film and increase the electrical properties and recover the lifetime which collapsed after sputtering the TCO.

With a TCO deposited at the back we can gain in photogenerated current, but this gain cannot counterbalance the reduction in V_{oc} and FF.

At this point of the work we obtained devices with very high value of current J_{ph} = 40.4 mA/cm^2 and voltage V_{oc} = 694 mV. Nevertheless, the performances of the cells were still limited due to the low fill factor. To address this issue, an alternative metallization technique is used in the front. With electroplating we could grow copper fingers with height = 40 μm (compared to the reference Al fingers with height = 2 μm). The cell metallized with copper has lower J_{sc} and V_{oc}, but the increase in FF by 6.5% determined an overall improvement in the power conversion efficiency η = 18.44% (V_{oc} = 672 mV, J_{sc} = 39.1 mV and FF = 71.71 mV) compared to η = 17.71% obtained with reference Al metallization.

6.1. Outlook

There is still a substantial gap between the highest efficiency achieved and the record efficiency. Although the results on the fabricated devices presented in this thesis represent a self-contained piece of work, further improvements can be applied.

Device fabrication

In terms of solar cell processing, there are few consideration to be done. Most important is the (p) a-Si:H which has been proven to be the main cause of hampering the device performances. The proposed (p) a-Si:H shows two main problems:

1. It is highly hydrogenated, which results in a structural modification and change in chemical bonding of the c-Si/ (i/p) a-Si:H interfaces and risks of etching away the (i) a-Si:H layer,

2. It is lowly doped, which results in low band bending. However the problem is that B_2H_6 particles are very reactive and boron diffuses easily through the passivating layer, so we cannot increase the doping level of the emitter.

These two problems can be overcome by incorporating other elements (oxygen and carbon) into the a-Si:H network. CO_2 guarantees a good passivation, by favoring the substitution of the weak $Si-Si$ and $Si-H$ bonds with $Si-O$. The emitter would benefits of a wider bandgap which would increase band bending (hence carrier selectivity) while avoiding the need to increase the B_2H_6 gas flow and, at the same time, would reduce parassitic absorption of these front layers. On the back side of the solar cell further improvements can be achieved by depositing intrinsic $a-SiO_x:H$ or $a-SiC_x:H$. iI this way, besides excellent surface passivation and symmetry, there is no more need to texturize the back of the c-Si, since the proposed a-Si alloy can guarantee a better internal reflection with respect to the reference a-Si:H [23].

The calculation of pFF and FF revealed that pFF = 81.4 % when IO:H/ITO is deposited at the front and the back while pFF = 77 % when IO:H/ITO is deposited only at the front. Nevertheless the $real\ FF$ is higher for the latter case. This proves that the sputtering process causes a damage which should be further investigated. A comparison of the FF, pFF and iFF could also help to understand to which extend the shunt and the series resistances individually hamper the device performances.

From a fabrication methodology point of view, for each TCO deposition, a film on a bar glass should be co-deposited such that TCO properties (thickness, resistivity, carrier density and carrier mobility) can be measured. Another issue of the fabricated devices is the low shunt resistance. So far the TCO has been sputtered on the entire surface of the wafer, therefore in future it is advisable to adopt masks or a proper edge isolation step to avoid any shunt in the cell.

The metallization also requires further optimization.

The front metallization with copper is very promising but fabrication improvements are still required, i has been already mentioned the necessity of using a seed layer, currently it is employed Titanium (300 nm), but it present two disadvantages:

1. It is deposited on the whole surface of the wafer, which implies the need of etching it away after the plating of copper, on this respect the use of alignment markers would simplify the process.

2. It is deposited by e-beam evaporation, which is a hard deposition technique which can damage the thin a-Si:H layer.

The titanium can be replaced with nickel, which is chemically grown, this has two main advantages: (i) it would avoid the strong ion bombardment of evaporation, (ii) a thicker layer (around 1 μm) can be grown which ensures that copper do not diffuse and contaminate the c-Si.

The best back metallization resulted to be the one with silver, chromium and aluminum. In this work it is proved that, from a carrier transport point of view, aluminum is better than silver, nevertheless, from an optical point of view, silver has higher reflective index which allows better internal reflection. Further studies should be implemented in finding the optimal trade off between the electrical and optical characteristics of the back contact.

Fundamental aspects

The microscopic structure of the a-Si:H layers should be analyzed with FTIR, Raman and TEM after the PECVD deposition and after the deposition of all subsequent layers, to verify bonds composition and the eventual change in microstructure characteristics.

The simulations of the band bending were performed based on work function values found in literature, specific UPS measurements should be done to find the exact work function value of the a-Si, TCO and metal fabricated.

Bibliography

[1] I. Fraunhofer Institute for Solar Energy Systems. Photovoltaic report. *https://www.ise.fraunhofer.de/content/dam/ise/de/documents/publications/studies/Photovoltaics-Report.pdf*, 2006.

[2] T. Sawada, N. Terada, S. Tsuge, T. Baba, T. Takahama, K. Wakisaka, S. Tsuda, and S. Nakano. High-efficiency a-si/c-si heterojunction solar cell. In *Photovoltaic Energy Conversion, 1994., Conference Record of the Twenty Fourth. IEEE Photovoltaic Specialists Conference-1994, 1994 IEEE First World Conference on*, volume 2, pages 1219–1226. IEEE, 1994.

[3] K. Yoshikawa, H. Kawasaki, W. Yoshida, T. Irie, K. Konishi, K. Nakano, T. Uto, D. Adachi, M. Kanematsu, H. Uzu, et al. Silicon heterojunction solar cell with interdigitated back contacts for a photoconversion efficiency over 26%. *Nature Energy*, 2:17032, 2017.

[4] Conversion efficiencies of best research solar cells worldwide. *https://www.nrel.gov/solar/*, 03-09-2017.

[5] M. Taguchi, A. Yano, S. Tohoda, K. Matsuyama, Y. Nakamura, T. Nishiwaki, K. Fujita, and E. Maruyama. 24.7% record efficiency hit solar cell on thin silicon wafer. *IEEE Journal of Photovoltaics*, 4(1):96–99, 2014.

[6] R. Islam, K. N. Nazif, and K. C. Saraswat. Si heterojunction solar cells: A simulation study of the design issues. *IEEE Transactions on Electron Devices*, 63(12):4788–4795, 2016.

[7] A. Smets, K. Jager, O. Isabella, R. van Swaaij, and M. Zeman. *Solar Energy, the physics and engineering of photovoltaic conversion technologies and systems*. UIT Cambridge Ltd, 2016.

[8] K. Z. Paul Hersch. *basics photovoltaic principles and methods*. Solar information module 6213, 1982.

[9] C. Battaglia, A. Cuevas, and S. De Wolf. High-efficiency crystalline silicon solar cells: status and perspectives. *Energy & Environmental Science*, 9(5):1552–1576, 2016.

[10] D. A. Neamen. *Semiconductor Physics and Devices*. University of New Mexico, 2010.

[11] Y. Tao and A. Rohatgi. *Nanostructured Solar cells*. Intech, 2017.

[12] M. Agarwal, A. Pawar, N. Wadibhasme, and R. Dusane. Controlling the c-si/a-si: H interface in silicon heterojunction solar cells fabricated by hwcvd. *Solar Energy*, 144:417–423, 2017.

[13] A. Gudovskikh, S. Ibrahim, J.-P. Kleider, J. Damon-Lacoste, P. R. i Cabarrocas, Y. Veschetti, and P.-J. Ribeyron. Determination of band offsets in a-si: H/c-si heterojunctions from capacitance–voltage measurements: Capabilities and limits. *Thin Solid Films*, 515(19):7481–7485, 2007.

[14] A. J. Bard, A. B. Bocarsly, F. R. F. Fan, E. G. Walton, and M. S. Wrighton. The concept of fermi level pinning at semiconductor/liquid junctions. consequences for energy conversion efficiency and selection of useful solution redox couples in solar devices. *Journal of the American Chemical Society*, 102(11):3671–3677, 1980.

[15] C. Schmiga, M. Rauer, M. Rüdiger, K. Meyer, J. Lossen, H.-J. Krokoszinski, M. Hermle, and S. W. Glunz. Aluminium-doped p+ silicon for rear emitters and back surface fields: results and potentials of industrial n-and p-type solar cells. In *Proceedings of 25th European Photovoltaic Solar Energy Conference*, pages 1163–1168, 2010.

[16] M. A. Green. The passivated emitter and rear cell (perc): From conception to mass production. *Solar Energy Materials and Solar Cells*, 143:190–197, 2015.

[17] M. A. Green. The path to 25% silicon solar cell efficiency: history of silicon cell evolution. *Progress in Photovoltaics: Research and Applications*, 17(3):183–189, 2009.

[18] M. A. Green, Y. Hishikawa, W. Warta, E. D. Dunlop, D. H. Levi, J. Hohl-Ebinger, and A. W. Ho-Baillie. Solar cell efficiency tables (version 50). *Progress in Photovoltaics: Research and Applications*, 25(7):668–676, 2017.

[19] S. Glunz, R. Preu, and D. Biro. 16: Crystalline silicon solar cells–state-of-the-art and future developments. *Comprehensive renewable energy*, 1:353–387, 2012.

[20] W. van Sark, L. Korte, and F. Roca. *Physics and technology of amorphous-crystalline heterostructure silicon solar cells*. Springer, 2012.

[21] A. Mahan and M. Vanecek. A reduction in the staebler-wronski effect observed in low h content a-si: H films deposited by the hot wire technique. In *AIP Conference Proceedings*, volume 234, pages 195–202. AIP, 1991.

[22] H. E. D. A. Aissa, Kivambe and Tabet. Emerging frontiers of n-type silicon material for photovoltaic applications: the impurity-defect interactions. *Front Nanosci Nanotech*, 1(1):2–12, 2015.

[23] S. M. De Nicolas. *a-Si: H/c-Si heterojunction solar cells: back side assessment and improvement*. PhD thesis, Université Paris Sud-Paris XI, 2012.

[24] M. Mikolášek. Silicon heterojunction solar cells: The key role of heterointerfaces and their impact on the performance. In *Nanostructured Solar Cells*. InTech, 2017.

[25] D. Deligiannis, V. Marioleas, R. Vasudevan, C. C. Visser, R. A. van Swaaij, and M. Zeman. Understanding the thickness-dependent effective lifetime of crystalline silicon passivated with a thin layer of intrinsic hydrogenated amorphous silicon using a nanometer-accurate wet-etching method. *Journal of Applied Physics*, 119(23):235307, 2016.

[26] C. S. Solanki and H. K. Singh. Principle of texturization for enhanced light trapping. In *Anti-reflection and Light Trapping in c-Si Solar Cells*, pages 65–82. Springer, 2017.

[27] M. Abdullah, M. Alghoul, H. Naser, N. Asim, S. Ahmadi, B. Yatim, and K. Sopian. Research and development efforts on texturization to reduce the optical losses at front surface of silicon solar cell. *Renewable and Sustainable Energy Reviews*, 66:380–398, 2016.

[28] K. Patel and P. K. Tyagi. Technological advances in a-si: H/c-si heterojunction solar cells. *International Journal Of Renewable Energy Research*, 4(2):528–538, 2014.

[29] J. Kegel, H. Angermann, U. Stürzebecher, and B. Stegemann. Ipa-free texturization of n-type si wafers: correlation of optical, electronic and morphological surface properties. *Energy Procedia*, 38:833–842, 2013.

[30] F. R. D. Simone. Hjt/topcon hybrid solar cell, 2016.

[31] M. Izzi, M. Tucci, L. Serenelli, P. Mangiapane, E. Salza, R. Chierchia, M. Della Noce, I. Usatii, E. Bobeico, L. Lancellotti, et al. Tco optimization in si heterojunction solar cells on p-type wafers with n-siox emitter. *Energy Procedia*, 84:134–140, 2015.

[32] J. Geissbühler, S. De Wolf, A. Faes, N. Badel, Q. Jeangros, A. Tomasi, L. Barraud, A. Descoeudres, M. Despeisse, and C. Ballif. Silicon heterojunction solar cells with copper-plated grid electrodes: status and comparison with silver thick-film techniques. *IEEE Journal of Photovoltaics*, 4 (4):1055–1062, 2014.

[33] A. Ebong and N. Chen. Metallization of crystalline silicon solar cells: a review. In *High Capacity Optical Networks and Enabling Technologies (HONET), 2012 9th International Conference on*, pages 102–109. IEEE, 2012.

[34] R. Vasudevan. Characterization of n-type silicon oxide for use in thin film solar cells. 2011.

[35] M. Dadu, A. Kapoor, and K. Tripathi. Effect of operating current dependent series resistance on the fill factor of a solar cell. *Solar energy materials and solar cells*, 71(2):213–218, 2002.

[36] I. A. Digdaya. Optical enhancement for heterojunction silicon solar cells. 2012.

[37] A. Deinega, S. Eyderman, and S. John. Coupled optical and electrical modeling of solar cell based on conical pore silicon photonic crystals. *Journal of Applied Physics*, 113(22):224501, 2013.

[38] H.-C. Lee, S.-C. Wu, T.-C. Yang, and T.-J. Yen. Efficiently harvesting sun light for silicon solar cells through advanced optical couplers and a radial pn junction structure. *Energies*, 3(4):784–802, 2010.

[39] F. Sevenig, L. Breitenstein, A. Oltersdorf, K. Zimmermann, and M. Hermle. Investigation on the impact of metallic surface contaminations on minority carrier lifetime of a-si: H passivated crystalline silicon. *Energy Procedia*, 8:288–293, 2011.

[40] U. Kroll, C. Bucher, S. Benagli, I. Schönbächler, J. Meier, A. Shah, J. Ballutaud, A. Howling, C. Hollenstein, A. Büchel, et al. High-efficiency pin a-si: H solar cells with low boron cross-contamination prepared in a large-area single-chamber pecvd reactor. *Thin solid films*, 451:525–530, 2004.

[41] Z. Xiao-Dan, S. Fu-He, W. Chang-Chun, S. Jian, Z. De-Kun, G. Xin-Hua, X. Shao-Zhen, and Z. Ying. Research on the boron contamination at the p/i interface of microcrystalline silicon solar cells deposited in a single pecvd chamber. *Chinese Physics B*, 18(10):4558, 2009.

[42] C. Tool, P. Manshanden, A. Burgers, and A. Weeber. Wafer thickness, texture and performance of multi-crystalline silicon solar cells. *Solar energy materials and solar cells*, 90(18):3165–3173, 2006.

[43] D. Zhang, I. Digdaya, R. Santbergen, R. Van Swaaij, P. Bronsveld, M. Zeman, J. Van Roosmalen, and A. Weeber. Design and fabrication of a sio x/ito double-layer anti-reflective coating for heterojunction silicon solar cells. *Solar Energy Materials and Solar Cells*, 117:132–138, 2013.

[44] S. De Wolf and M. Kondo. Nature of doped a-si: H/c-si interface recombination. *Journal of Applied Physics*, 105(10):103707, 2009.

[45] S. Alivizatos. Investigation of textured c-si wafers for application in silicon heterojunction solar cells. 2013.

[46] M. Zeman, O. Isabella, K. Jäger, R. Santbergen, S. Solntsev, M. Topic, and J. Krc. Advanced light management approaches for thin-film silicon solar cells. *Energy Procedia*, 15:189–199, 2012.

[47] M. Tanaka, M. Taguchi, T. Matsuyama, T. Sawada, S. Tsuda, S. Nakano, H. Hanafusa, and Y. Kuwano. Development of new a-si/c-si heterojunction solar cells: Acj-hit (artificially constructed junction-heterojunction with intrinsic thin-layer). *Japanese Journal of Applied Physics*, 31(11R): 3518, 1992.

[48] M. Kondo, S. De Wolf, and H. Fujiwara. Understanding of passivation mechanism in heterojunction c-si solar cells. *MRS Online Proceedings Library Archive*, 1066, 2008.

[49] J. Ge, Z. Ling, J. Wong, T. Mueller, and A. Aberle. Optimisation of intrinsic a-si: H passivation layers in crystalline-amorphous silicon heterojunction solar cells. *Energy Procedia*, 15:107–117, 2012.

[50] H. Meddeb, T. Bearda, Y. Abdelraheem, H. Ezzaouia, I. Gordon, J. Szlufcik, and J. Poortmans. Structural, hydrogen bonding and in situ studies of the effect of hydrogen dilution on the passivation by amorphous silicon of n-type crystalline (1 0 0) silicon surfaces. *Journal of Physics D: Applied Physics*, 48(41):415301, 2015.

[51] B. Kalache, A. Kosarev, R. Vanderhaghen, and P. R. i Cabarrocas. Ion bombardment effects on microcrystalline silicon growth mechanisms and on the film properties. *Journal of Applied physics*, 93(2):1262–1273, 2003.

[52] D. Deligiannis. Surface passivation for silicon heterojunction solar cells, 2016.

[53] Y.-S. Cho, C.-H. Hsu, S.-Y. Lien, D.-S. Wuu, and I.-C. Hsieh. Effect of hydrogen content in intrinsic a-si: H on performances of heterojunction solar cells. *International Journal of Photoenergy*, 2013, 2013.

[54] B. Sopori, X. Deng, J. Benner, A. Rohatgi, P. Sana, S. Estreicher, Y. Park, and M. Roberson. Hydrogen in silicon: a discussion of diffusion and passivation mechanisms. *Solar Energy Materials and Solar Cells*, 41:159–169, 1996.

[55] B. Yan, J. Yang, and S. Guha. Effect of hydrogen dilution on the open-circuit voltage of hydrogenated amorphous silicon solar cells. *Applied physics letters*, 83(4):782–784, 2003.

[56] J. Geissbühler, S. De Wolf, B. Demaurex, J. P. Seif, D. T. Alexander, L. Barraud, and C. Ballif. Amorphous/crystalline silicon interface defects induced by hydrogen plasma treatments. *Applied Physics Letters*, 102(23):231604, 2013.

[57] S. Kim, V. A. Dao, C. Shin, J. Cho, Y. Lee, N. Balaji, S. Ahn, Y. Kim, and J. Yi. Low defect interface study of intrinsic layer for c-si surface passivation in a-si: H/c-si heterojunction solar cells. *Thin Solid Films*, 521:45–49, 2012.

[58] L. He. *Optical Second Harmonic Generation Measurements for Characterization of Amorphous Silicon Interfaces*. PhD thesis, University of Colorado at Boulder, 2014.

[59] M. Fischer, H. Tan, J. Melskens, R. Vasudevan, M. Zeman, and A. H. Smets. High pressure processing of hydrogenated amorphous silicon solar cells: Relation between nanostructure and high open-circuit voltage. *Applied Physics Letters*, 106(4):043905, 2015.

[60] L. Zhao, H. Diao, X. Zeng, C. Zhou, H. Li, and W. Wang. Comparative study of the surface passivation on crystalline silicon by silicon thin films with different structures. *Physica B: Condensed Matter*, 405(1):61–64, 2010.

[61] T. Hsu, B. Anthony, R. Qian, J. Irby, S. Banerjee, A. Tasch, S. Lin, H. Marcus, and C. Magee. Cleaning and passivation of the si (100) surface by low temperature remote hydrogen plasma treatment for si epitaxy. *Journal of electronic materials*, 20(3):279–287, 1991.

[62] R. D. Perunta. Heterojunction solar cell with graded i-n fsf, 2016.

[63] S. Avasthi, S. Lee, Y.-L. Loo, and J. C. Sturm. Role of majority and minority carrier barriers silicon/organic hybrid heterojunction solar cells. *Advanced materials*, 23(48):5762–5766, 2011.

[64] T. Schulze. Structural, electronic and transport properties of amorphous/crystalline silicon heterojunction, 2011.

[65] Z. Ling, J. Ge, T. Mueller, J. Wong, and A. Aberle. Optimisation of p-doped μc-si: H emitter layers in crystalline-amorphous silicon heterojunction solar cells. *Energy Procedia*, 15:118–128, 2012.

[66] L. Mazzarella, S. Kirner, O. Gabriel, L. Korte, B. Stannowski, B. Rech, and R. Schlatmann. Nanocrystalline silicon oxide emitters for silicon hetero junction solar cells. *Energy Procedia*, 77: 304–310, 2015.

[67] K. Ghosh, C. Tracy, S. Goodnick, and S. Bowden. Effect of band bending and band offset in the transport of minority carriers across the ordered/disordered interface of a-si/c-si heterojunction solar cell. In *Photovoltaic Specialists Conference (PVSC), 2012 38th IEEE*, pages 000221–000226. IEEE, 2012.

[68] P. L. Koswatta. *Quantifying Carrier Selective Contacts in Solar Cells*. PhD thesis, Arizona State University, 2016.

[69] R. Brendel and R. Peibst. Contact selectivity and efficiency in crystalline silicon photovoltaics. *IEEE Journal of Photovoltaics*, 6(6):1413–1420, 2016.

[70] J. L. Martins and A. Zunger. Stability of ordered bulk and epitaxial semiconductor alloys. *Physical review letters*, 56(13):1400, 1986.

[71] T. Mueller, J. Wong, and A. G. Aberle. Heterojunction silicon wafer solar cells using amorphous silicon suboxides for interface passivation. *Energy Procedia*, 15:97–106, 2012.

[72] L. Martinu, O. Zabeida, and J. Klemberg-Sapieha. Plasma-enhanced chemical vapor deposition of functional coatings. *Handbook of Deposition Technologies for Films and Coatings*, pages 394–467, 2010.

[73] G. Carroy, D. Muñoz, F. Ozanne, A. Valla, P. Mur, and G. Rodriguez. Analysis of different front and back tco on heterojunction solar cells. *30th EU PVSEC*, pages 359–364, 2015.

[74] A. Budhi. Hydrogenated indium oxide (ioh) tco for thin film solar cell, 2016.

[75] Z. Ma, Z. Li, K. Liu, C. Ye, and V. J. Sorger. Indium-tin-oxide for high-performance electro-optic modulation. *Nanophotonics*, 4(1):198–213, 2015.

[76] H. Ge. Development of high efficiency shj poly-si passivating contact hybrid solar cells, 2017.

[77] B. Demaurex, S. De Wolf, A. Descoeudres, Z. Charles Holman, and C. Ballif. Damage at hydrogenated amorphous/crystalline silicon interfaces by indium tin oxide overlayer sputtering. *Applied Physics Letters*, 101(17):171604, 2012.

[78] Dc module iv diode equivalent circuit. *https://pvpmc.sandia.gov/modeling-steps/2-dc-module-iv/diode-equivalent-circuit-models/*.

[79] Electrical conductivity in metals. *https://www.thebalance.com/electrical-conductivity-in-metals-2340117*, 10-09-2017.

[80] Y. D. Groot. Metallization for high efficiency c-si solar cells based on cu-plating, 2017.

[81] E. Mitchell and J. Mitchell. The work functions of copper, silver and aluminium. In *Proceedings of the Royal Society of London A: Mathematical, Physical and Engineering Sciences*, volume 210, pages 70–84. The Royal Society, 1951.

[82] D. K. Schroder and D. L. Meier. Solar cell contact resistance—a review. *IEEE Transactions on electron devices*, 31(5):637–647, 1984.

[83] W. Lisheng, C. Fengxiang, and A. Yu. Simulation of high efficiency heterojunction solar cells with afors-het. In *Journal of Physics: Conference Series*, volume 276, page 012177. IOP Publishing, 2011.

Aknowledgements

Firstly I would like to express my gratitude to my supervisor Dr. Olindo Isabella, who gave me the opportunity to work on this thesis project, thanks for your comments, enthusiasm and questions which inspired me to keep on learning and solve problems, it has been an honor to have you as professor and employer, because you are an explosion of ideas and knowledge. I am very grateful to my daily supervisor Dr. Guangtao Yang, I admire your dedication and patience, I want to thanks you for your daily help, guidance and planning. Moreover, I would like to give a special thanks to all the c-Si team and especially Gianluca Limodio and Dr. Paul Procel, you have been always kind and helpful with me and you made me feel has I had two more supervisors on my side. I would like to thank Prof. dr. Miro Zeman and the entire PVMD group for providing me a firm foundation for accomplishing this project, a motivating environment and an pleasant workplace. Thanks to Martijn Tijssen and Stefaan Heirman, I appreciate you all for your technical support and helpfulness; My appreciation goes also to Dr. Massimo Mastrangeli for showing interest to my thesis project by accepting to be the external member of my MSc defence committee.

On a personal level I would like to thanks all the people who have, on their way, gotten me here. To my family (papà, mamma, Ilaria e Niccolò) and my enlarged family (Giovanni e Francesca, Filippo, Roberta, Marco e Andrea, Pietropaolo, Daniela, Giulia, Giuseppe e Chiara) because you were always standing by me; to my housemate (Benedicte, Francis, Jonathan and Tim) because you are not simply that, you are my Dutch family; to the students of the PVMD group (especially the c-Si bosses team and Andres), with who I have spent most of my days with; to my roman friends (Gaia, Giorgio, Luca and Maria) with who everything started; to my group of friends (Alessandro, Davide, Edoardo, Federica, Federico, Francesco, Giulia, Greta, Luca, Luca, Lucrezia, Luigi, Matteo, Matteo, Simone and Umberto) those have been two years on amazing friendship and experiences together; and above all to Simone, you are the most beautiful gift the Netherlands could have given to me.