A Continuous-Time BJT-Based Temperature-to-Digital Converter

By

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Abstract

This thesis presents a BJT-based CMOS temperature-digital converter (TDC). With a continuous-time readout, the TDC avoids the kT/C noise limit incurred by previous discrete-time (switched-capacitor) TDCs. An energy-efficient BJT front-end generates PTAT and CTAT currents for being digitized by an incremental ADC through a charge balancing operation. Simulated in a standard 0.18 μm CMOS process, the TDC achieves a (3σ) inaccuracy of $\pm$0.13°C from -40°C to 125°C after one-point trimming. Moreover, the TDC achieves 4 mK resolution in a 202 millisecond conversion time, while consuming 4.9 μW. This corresponds to a resolution FoM of 15.7 pJ.K^2

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1 Introduction

1.1 Motivation

Temperature measurement is important in many precision integrated systems, such as frequency references and current-sensors, because it facilitates the compensation of their temperature dependencies. CMOS-compatible temperature-to-digital converters (TDCs) are well-suited for this purpose [1] [2]. To avoid degrading system performance, such TDCs should have high resolution and low inaccuracy. Moreover, their energy consumption should be minimized to prolong battery life or reduce self-heating errors.

It is well known that there is a trade-off between a TDC's temperature resolution and its energy consumption [5]. This trade-off is captured by the resolution Figure-of-Merit (R-FoM), which is equal to the product of conversion energy (E_{conv}) and resolution squared (σ^2)[3]. A lower R-FoM corresponds to superior energy efficiency. Commonly used types of CMOS-compatible TDCs are BJT-based and resistor-based TDCs. Each type has its advantages and disadvantages. Resistor-based TDCs can achieve excellent R-FoMs, below 50 fJ.K^2. But they require a two-point calibration to achieve low inaccuracy, e.g. 0.1°C [6]. In contrast, BJT-based TDCs require only a one-point calibration to achieve similar inaccuracy. Also, a R-FoM below 200 fJ.K^2 can be achieved by BJT-based TDCs [12].

Based on these observations, the objective of this work is to design an energy-efficient and accurate BJT-based TDC.

1.2 Operation principle of BJT-based temperature sensors

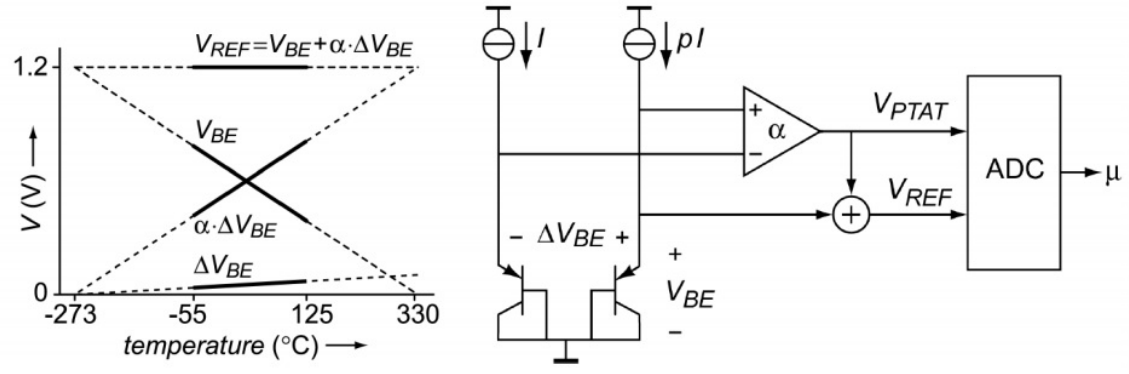


Figure 1.1: Block diagram of a BJT-based temperature sensor showing the generation of V_{be}, ΔV_{be}, and V_{ref} [10]

The heart of a BJT-based temperature sensor consists of two diode-connected BJTs biased at a current density ratio of 1:p, which generates complementary-to-absolute-temperature (CTAT) voltage V_{be} and proportional-to-absolute-temperature (PTAT) ΔV_{be} voltage, as shown in Figure 1.1. For large BJT collector currents, V_{be}

can be formulated as:

$$V_{be} = \frac{kT}{q} ln(\frac{I_c}{I_s}) \tag{1.1}$$

where k is the Boltzmann constant, T is the temperature in Kelvin, q is the elementary electron charge, I_c is the collector current, and I_s is the saturation current. Due to the temperature dependency of I_s, the voltage V_{be} has a CTAT nature with a sensitivity of approximately -2 mV/°C, while, the voltage ΔV_{be} can be expressed as follows:

$$\Delta V_{be} = \frac{kT}{q} ln(p) \tag{1.2}$$

It is clear that ΔV_{be} is independent of both I_c and I_s, and exhibits a linear and well-defined PTAT behavior. Hence, ΔV_{be} is a highly suitable voltage for extracting the required temperature information. A reference voltage V_{ref} with nominally zero temperature-coefficient is required for performing a ratiometric measurement of the temperature. V_{ref} is generated by scaling ΔV_{be} with constant α such that the positive temperature coefficient of $\alpha.\Delta V_{be}$ compensates for the negative temperature coefficient of V_{be}. The result can be linearly combined as:

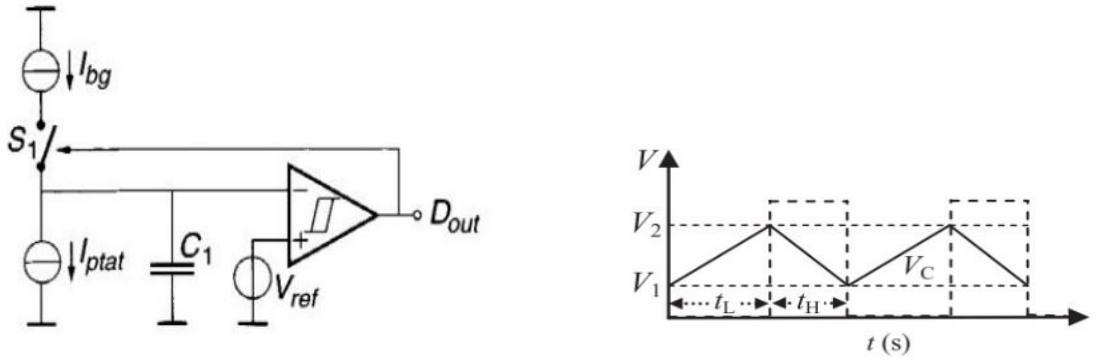
$$V_{ref} = V_{be} + \alpha \Delta V_{be} \tag{1.3}$$

A BJT-based sensor is typically followed by a single-bit modulator in which the analog-to-digital conversion takes place. The modulator provides a ratiometric output μ expressed as:

$$\mu = \frac{\alpha.\Delta V_{be}}{\alpha.\Delta V_{be} + V_{be}} \tag{1.4}$$

Typically, duty-cycle and delta-sigma ($\Delta\Sigma$) modulators are used. Their operation is briefly described in the following sections.

1.3 BJT-based temperature sensors with duty-cycle modulated output



(a) (b)

Figure 1.2: Schematic diagram showing the concept of duty-cycle modulation in temperature-sensing. (a) Basic principle (b) the voltage across C_1 [8]

The use of a duty-cycle modulator in a BJT-based temperature sensor is shown in Figure 1.2. A relatively large capacitor C_1 acting as a passive integrator is charged by the $(I_{bg} - I_{PTAT})$ current, and discharged by the PTAT current I_{PTAT}, according to the output of the Schmitt-trigger (ST) comparator. In steady-state, the charge on C_1 will be the same at the end of each period. This can be formulated as:

$$T_H \, I_{bg} = (T_H + T_L) \, I_{PTAT} \tag{1.5}$$

Therefore, the average duty cycle is proportional to the absolute temperature. This can be expressed as follows:

$$D_{out} = \frac{T_H}{T_H + T_L} = \frac{I_{PTAT}}{I_{bg}} \tag{1.6}$$

The main advantage of duty-cycle modulators is that their output D_{out} is independent of the C_1 value, the ST threshold values, and the frequency of the output signal. It does depend on the values of the current I_{PTAT} & I_{bg}, which can both be generated with the same type of resistor. As a result, the absolute value of the two current-setting resistors is not crucial. By using highly matched resistors, good temperature inaccuracy can be achieved. One realization of a duty-cycle modulator in a BJT-based temperature sensor is shown in Figure 1.3. The sensor achieves 3σ inaccuracy equal to ± 0.15°C over a temperature range of -45°C to 130°C, and an excellent resolution FoM equal to 3.2 pJ.K^2 [8].

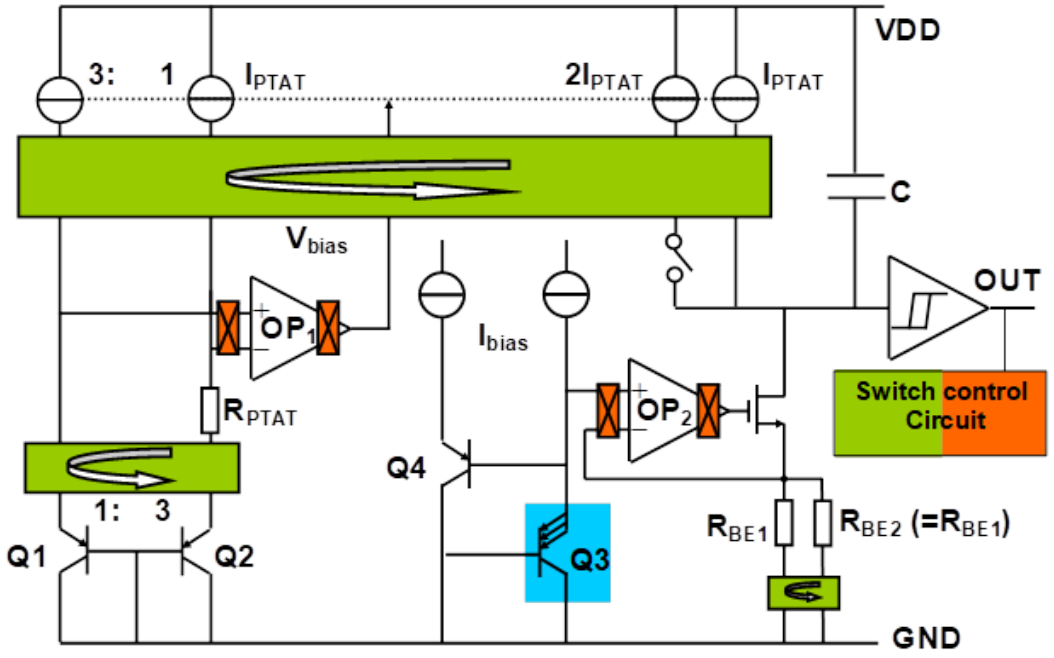


Figure 1.3: Circuit schematic of BJT-based temperature sensor with duty-cycle modulated output [8]

The significant drawback of [8] is that its duty-cycled output is still a quasi-analog signal, and therefore an external high speed (72 MHz) counter is required to

determine the duty-cycle and thus obtain a digital temperature reading. In other words, [8] is only part of a TDC. Moreover, it consumes 55 μA, which may be problematic for ultra-low power temperature-sensing applications.

An intermediate solution for digitizing the duty-cycle modulated output of such BJT-based temperature sensor is to perform time-discretization on-chip. However, parasitic coupling may lead to undesirable frequency-locking occurring between the output signal and the high-speed counter clock, since the output signal is not synchronized to a specific clock. This can easily deteriorate temperature inaccuracy and resolution [28]. To avoid this problem, the duty-cycle modulated signal can be synchronized to a sampling clock by adding a flip-flop after the comparator, as shown in Figure 1.4. The result is a $\Delta\Sigma$ modulator. In the following section, the types of the $\Delta\Sigma$ modulator employed in BJT-based temperature sensors are discussed briefly.

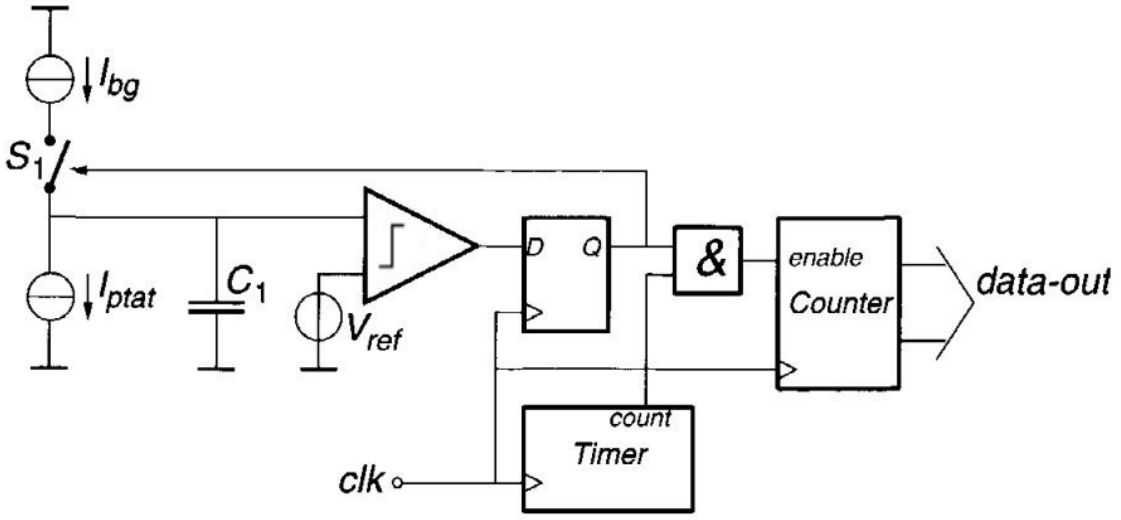


Figure 1.4: Block diagram showing the principle of the $\Delta\Sigma$ modulator in BJT-based temperature sensor [28]

1.4 BJT-based temperature sensors with $\Delta\Sigma$ modulators

$\Delta\Sigma$ modulators can achieve high resolution at the slow speeds of temperature signals. While the majority of TDCs employ discrete-time (DT) $\Delta\Sigma$ modulators, there have also been a few designs with continuous-time (CT) $\Delta\Sigma$ modulators, due to their higher energy-efficiency and simpler implementation [7][8][12][13].

Discrete-time (switched-capacitor) TDC read-outs are popular because the scaling factor α is determined by the ratio of sampling capacitors, which match better than on-chip resistors. Moreover, capacitors have much lower voltage and temperature coefficients. As a result, such TDCs achieve excellent accuracy. However, the spread and offset of V_{be} along with the spread of p and α are still the main sources of temperature error.

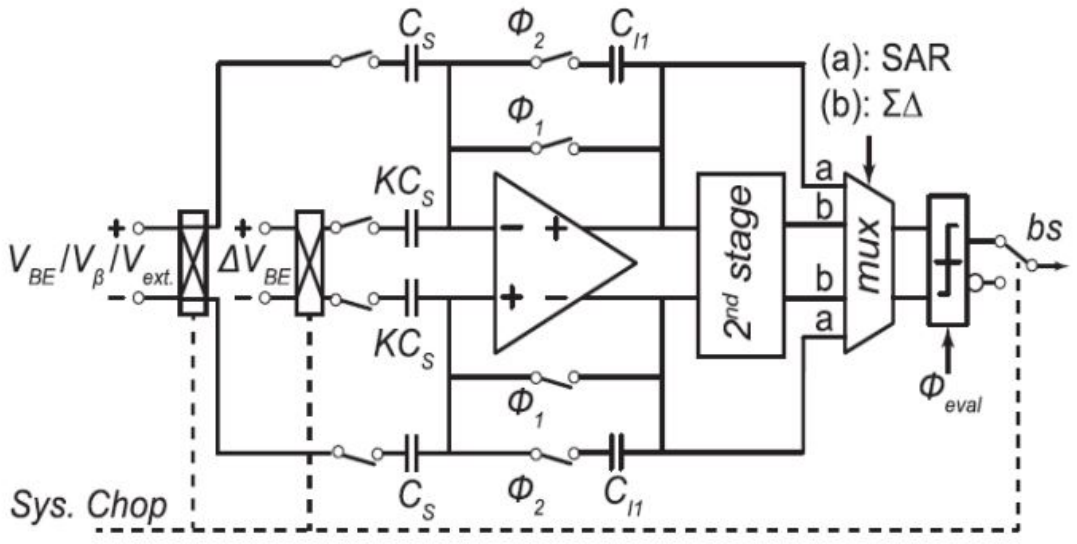
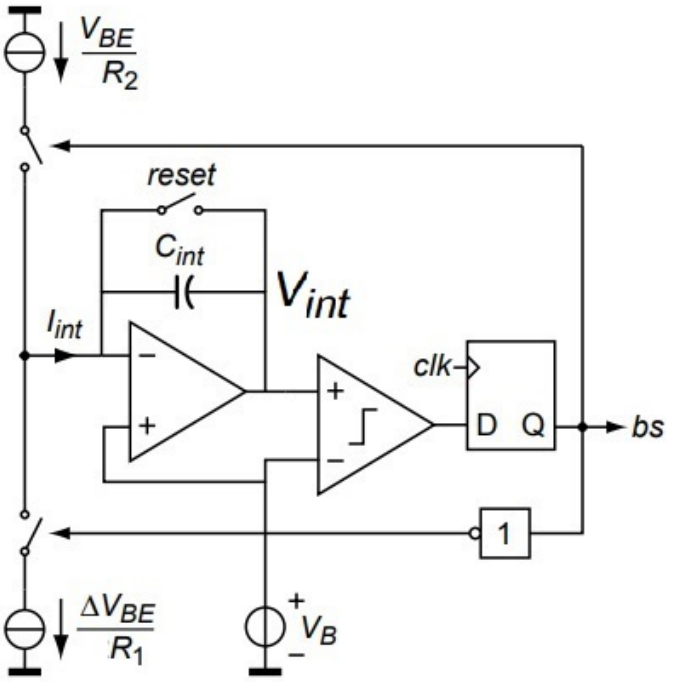


Figure 1.5: Two-step TDC showing the scaled sampling capacitors [2]

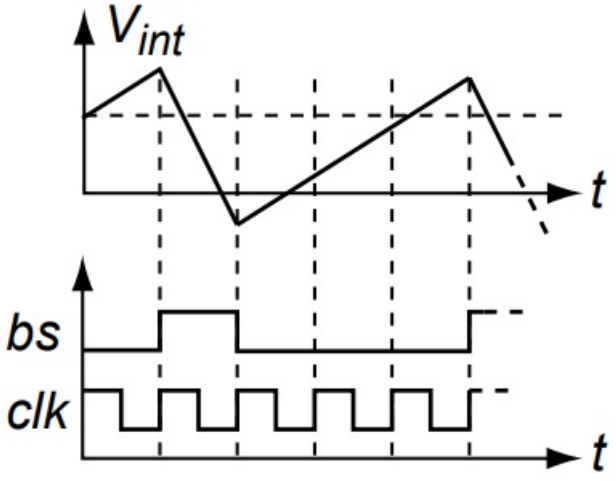
The main drawback of employing switched capacitor read-outs in TDCs is that they suffer from kT/C noise, which can easily degrade the temperature resolution. A workaround is to increase the size of the sampling capacitors, which attenuates the sampled noise. However, this comes at the expense of greater TDC area. Furthermore, it degrades the settling of the BJT front-end, which requires larger biasing currents, and thus reduces the energy efficiency of the TDC.

Another workaround for mitigating kT/C noise is to increase the frequency of the TDC sampling clock, which spreads the noise over a wider bandwidth and decreases the in-band sampled noise. This also requires larger biasing currents to achieve quick settling in a shorter sampling period. The switched capacitor-based TDC with the highest energy efficiency to date is [4], with a resolution FoM equal to 7.8 pJ.K^2. Figure 1.5 shows an example of a switched-capacitor $\Delta\Sigma$ TDC. Although a highly efficient integration technique is employed compared to the conventional charge-balancing scheme introduced earlier, the TDC resolution is still limited by kT/C noise.

The current-driven CT read-out architecture employed for TDC is shown in Figure 1.6 [10]. The transfer function of such TDC is optimized in a current-balancing operation. According to the bitstream value, the TDC either integrates a PTAT current (proportional to ΔV_{be}), or CTAT current (proportional to V_{be}). These currents are generated by active voltage-to-current converters. In this current-driven TDC, the reference current is not needed to be explicitly generated. The scaling factor α is fixed by the ratio equal to R_2/R_1.



(a)



(b)

Figure 1.6: (a) Schematic of current-driven CT $\Delta\Sigma$ readout (b) timing diagram [10]

The TDC negative feedback loop maintains zero average for the integrated current, which can be expressed in the following charge balancing equation:

$$(1-\mu)(\Delta V_{be}/R_1) - \mu(V_{be}/R_2) = 0 \tag{1.7}$$

where μ is the average of the bitstream. Therefore, μ can be formulated as:

$$\mu = \frac{\Delta V_{be}/R_1}{\Delta V_{be}/R_1 + V_{be}/R_2} \tag{1.8}$$

The realization of α is crucial, as any inaccuracy corresponds directly to an error in the temperature. The accuracy of α is then limited by the matching of the resistors.

1.5 Comparison between duty-cycle and delta-sigma modulators

The main difference between duty-cycle and $\Delta\Sigma$ modulators is that the former requires an extra off-chip DSP for providing a digital temperature reading, while the latter already provides a digital reading on-chip. The main overhead required to implement a $\Delta\Sigma$ modulator compared to a duty-cycle modulator is the sampling clock generation. Table 1.1 shows a performance summary and comparison between state-of-the-art BJT-based temperature sensors with CT read-outs. With the duty-cycle modulators, an excellent R-FoM (3.2 pJ.K^2) is achieved in [8]. While the best R-FoM (190 fJ.K^2) to date for a BJT-based sensor is achieved with a current-mode $\Delta\Sigma$ modulator in [12].

The motivation of this work is to explore the use of a CT $\Delta\Sigma$ modulator in a BJT-based temperature sensor in order to provide a fully digital temperature reading on-chip in a bid to achieve optimum energy-efficiency and resolution.

1.6 Thesis overview

This thesis is organized as follows. To start with, Chapter 2 introduces the system-level and design considerations of the BJT-based TDC. Chapter 3 presents an energy efficient current-output BJT front-end in terms of the circuit implementation and noise analysis. Chapter 4 covers the design considerations and circuit-level implementation of a CT $\Delta\Sigma$ modulator. In addition, it describes the use of return-to-zero switching to improve the modulator's inaccuracy and resolution. Simulation results are presented in Chapter 5. Finally, the thesis concludes in Chapter 6 with suggestions for future work.

Table 1.1: Literature survey for state-of-the-art BJT-based temperature sensors with CT read-outs

	Modulator type	Clock[1] (kHz)	Rel. IA (%)	Resolution (mK)	Conv. time (ms)	Power (μW)	R-FoM (pJ.K^2)	PSS (°C/V)
ISSCC'20 [12]	Delta-sigma	9600	-	0.65	0.72	620	0.19	-
A-SSCC'19 [13]		16	0.16	1.7	213	9	5.4	0.008
TCAS-II'19 [14]		1000	2.06	20	32.8	37	490	1.5
ISSCC'17 [15]		-	2.47	150	8.2	18.8	3500	-
ESSCIRC'15 [16]		25000	2	400	0.27	1210	52000	-
JSSC'05 [7]		16	0.5	30	100	351	31590	0.3
TE TSYS01 [17]		-	0.6	10	8.22	41.25	34	0.2
ADI ADT7410 [18]		-	0.98	7.8	240	693	10119	0.1
ADI ADT7312 [19]		-	1.3	7.8	240	880	12849	0.1
TI TMP117 [20]		-	0.29	7.8	15.5	446	421	0.006
TI LM96163 [21]		-	2	125	38.3	1505	56300	-
E-Letters'18 [22]	Duty-cycle	3	0.69	32	2.4	30.6	75	0.3
TCAS-II'17 [23]		3.7	1.1	39	8.1	0.9	11	0.7
TIE'17 [8]		4	0.3	3	1.8	198	3.2	0.1
Smartec SMT172 [24]		-	0.46[2]	0.2[3]	1000	198[4]	7.92	0.1

1-Sampling clock frequency for $\Delta\Sigma$ modulator & output-signal frequency for duty-cycle modulator at RT.
2-TO18 package (-45°C to 130°C & second-order interpolation between resulting duty-cycle and temp.)
3-At temp.=25°C & V_{cc}=5 V
4-At V_{cc}=3.3 V & no load at the output pin

2 System Analysis

2.1 Target specifications

Table 1.1 provides a good starting point for the target specifications of the BJT-based TDC. The TDC in [13] achieves the best relative inaccuracy (0.16%) with a continuous-time $\Delta\Sigma$ modulator. While the best relative inaccuracy with a duty-cycle modulator is 0.3%, achieved in [8]. The TDC in [12] achieves a superior resolution equal to 0.65 mK in a conversion time of 0.72 ms. However, being a part of a MEMS oscillator whose output frequency is already compensated with a 3rd-order temperature calibration, the inaccuracy of the TDC itself is not crucial. The TDC in [13] is the most energy-efficient, as it consumes 5 μA from a 1.8 V supply. With a resolution of 1.27 mK in a conversion time of 320 ms, this leads to a good R-FoM equal to 4.5 pJ.K^2. The design in [8] achieves an excellent resolution of 3 mK in 1.8 ms conversion time. With a relatively high power consumption of 198 μW, the achieved R-FoM is 3.2 pJ.K^2.

The supply-sensitivity (0.008 °C/V) of [13] is also excellent. While the best supply-sensitivity is achieved in [20], equal to 0.006 °C/V. Motivated by this analysis, Table 2.1 summarizes the set of target specifications for the proposed BJT-based TDC. In the following section, we shall investigate the top-level architecture of the BJT-based TDC with a CT $\Delta\Sigma$ modulator.

Table 2.1: Target specifications of the BJT-based TDC

Specifications	**Value**
Current	$<$ 5 μA
Supply range	1.6 V to 2 V
Inaccuracy (3σ)	$\pm$0.12°C
Temperature range	-40°C to 125°C
Supply sensitivity	8 m°C/V
Resolution	3 mK
Conversion time	320 ms
R-FoM	$<$ 26 pJ.K^2

2.2 Architecture

Figure 2.1 shows the block diagram of the proposed BJT-based TDC with a CT $\Delta\Sigma$ modulator. The BJT front-end generates single PTAT current I_{PTAT} and CTAT current I_{CTAT} to be integrated by the CT $\Delta\Sigma$ modulator in a linear charge balancing operation, as will be discussed later in Chapter 4. The output bitstream is decimated by an off-chip filter to extract the temperature reading in degree Celsius

(°C). An on-chip oscillator is required for generating the sampling clock of the ΔΣ modulator, accompanied with dividers for generating the dynamic error-correction clocks in the front-end, as will be discussed later in Chapter 3. The sampling clock of the ΔΣ modulator needs to be read-out of the chip to eliminate the resolution degradation due to the phase noise of the oscillator.

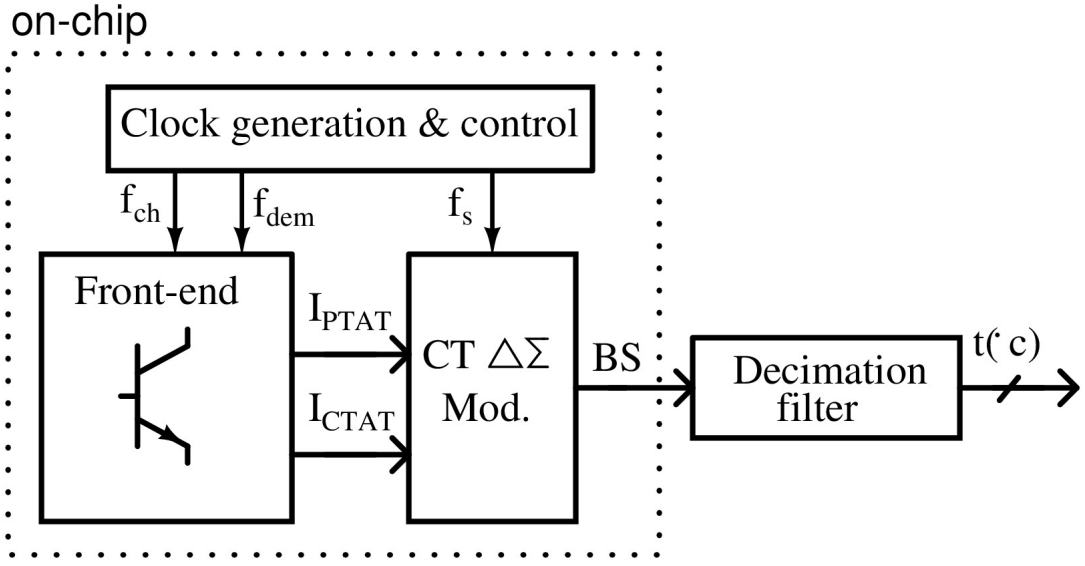


Figure 2.1: Block diagram of the BJT-based TDC with continuous-time ΔΣ modulator

2.3 Design considerations

ΔΣ modulator: order and sampling frequency

The loop-filter order and the sampling frequency of the ΔΣ modulator are key parameters in the TDC performance. From Table 2.1, to achieve the target thermal-noise limited resolution (3 mK) across the temperature range from -40°C to 125°C, the ΔΣ modulator should achieve an ENOB equal to 16 bits. With a 1st order modulator, this ENOB requires 2^{16} ΔΣ clock cycles. Since the target conversion time is 320 ms, this leads to a sampling frequency to be higher than 200 kHz. As this would lead to an undesirably high power consumption and a significant increase in errors related to charge injection, a 2nd order modulator is employed, which can provide the desired resolution at a much lower clock frequency.

Using a 2nd order modulator provides a wide stable input range and more aggressive (-40 dB/decade) quantization-noise shaping compared to a 1st order one [10]. With a 2nd order modulator followed by a triangular (sinc^2) decimation, the required ENOB is achieved at 2^{10} ΔΣ clock cycles, as shown in Figure 2.2. This leads to a minimum sampling frequency of 3.2 kHz at a conversion time of 320 ms. To compensate for the ΔΣ modulator's various non-idealities, i.e. the integrator leakage, the sampling frequency of the ΔΣ modulator is increased to be 16 kHz.

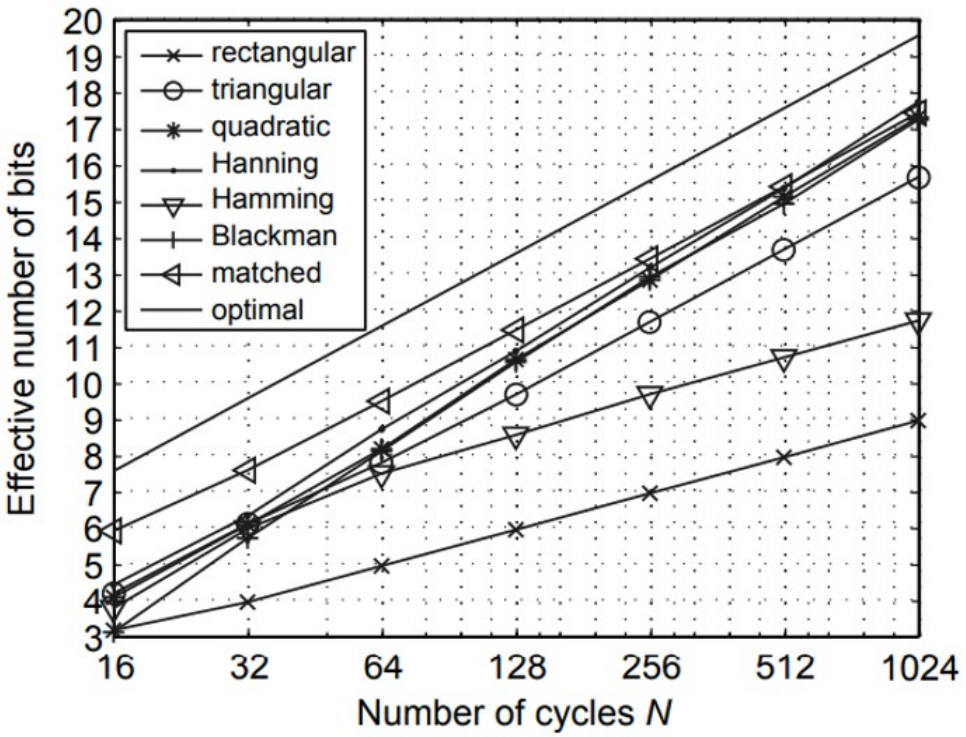


Figure 2.2: Second-order $\Delta\Sigma$ modulator: ENOB versus the number of clock cycles [10]

BJT front-end: PTAT and CTAT current levels

In this section, I_{PTAT} and I_{CTAT} levels are set for the target resolution (3 mK) at conversion time of 320 ms, as shown in Table 2.1. In every $\Delta\Sigma$ clock cycle, the modulator accumulates either a charge Q_{PTAT} proportional to I_{PTAT}, or a charge Q_{CTAT} proportional to I_{CTAT}, in a charge balancing operation discussed later in Chapter 4. The accumulated charge after number of $\Delta\Sigma$ clock cycles N is expressed as:

$$Q_{total} = N\Big[(1-\mu).Q_{PTAT} - \mu.Q_{CTAT}\Big] + q_{n,total} \tag{2.1}$$

where μ is the average value of the output bitstream, and $q_{n,total}$ is the accumulated noise charge. Denoting the rms noise charge associated with Q_{PTAT} and Q_{CTAT} as $q_{n,PTAT}$ and $q_{n,CTAT}$, respectively. The accumulated noise charge can be formulated as:

$$q^2_{n,total} = N\Big[(1-\mu).q^2_{n,PTAT} + \mu.q^2_{n,CTAT}\Big] \tag{2.2}$$

Since the average value of Q_{total} is ideally zero, due to the feedback of the $\Delta\Sigma$ modulator. Solving Equation 2.1 for μ yields:

$$\mu = \frac{Q_{PTAT}}{Q_{PTAT}+Q_{CTAT}} + \frac{q_{n,total}}{(Q_{PTAT}+Q_{CTAT}).N} \tag{2.3}$$

where the first term is the desired average value of μ, and the second term is the accumulated output noise charge. The standard deviation of the latter can be found

by substituting in Equation 2.2:

$$\sigma_{\mu} = \frac{1}{Q_{PTAT} + Q_{CTAT}} \sqrt{\frac{(1-\mu).q_{n,PTAT}^2 + \mu.q_{n,CTAT}^2}{N}} \tag{2.4}$$

Converting σ_{μ} to a temperature resolution σ_T yields:

$$\sigma_T = \frac{A}{Q_{PTAT} + Q_{CTAT}} \sqrt{\frac{(1-\mu).q_{n,PTAT}^2 + \mu.q_{n,CTAT}^2}{N}} \tag{2.5}$$

where A is a factor used to convert μ into a temperature reading in degrees Celsius. Reformulating Equation 2.5 in the current domain yields:

$$\sigma_T = \frac{A}{I_{PTAT} + I_{CTAT}} \sqrt{\frac{(1-\mu).i_{n,PTAT}^2 + \mu.i_{n,CTAT}^2}{N}} \tag{2.6}$$

where N corresponds to the number of $\Delta\Sigma$ clock cycles within the target conversion time (320 ms). While $i_{n,PTAT}^2$ and $i_{n,CTAT}^2$ are expressed in Equations 3.24 and 3.25, respectively, derived later in Chapter 3.

The value of I_{PTAT} is already set to 53 nA at RT equal to that of the silicon-approved front-end in [13]. While using Equation 2.6, I_{CTAT} is set to 49 nA at RT. These current levels result in σ_T equal to 1.6 mK at a conversion time of 320 ms, which is well below the target specification of σ_T equal to 3 mK at the same conversion time, shown in Table 2.1.

2.4 Summary

This chapter presents the target specifications along with top level architecture of the proposed BJT-based TDC with a CT $\Delta\Sigma$ modulator. The global design considerations of the TDC are also discussed including the $\Delta\Sigma$ modulator order and sampling frequency. Moreover, setting the PTAT and CTAT current levels for the target resolution of the TDC.

3 Current-output BJT-based Front-end

This chapter introduces a BJT front-end based on the silicon-approved front-end in [13], yet with single PTAT and CTAT current output. The design considerations and circuit implementation of the PTAT and CTAT current generators, including the employed dynamic error correction techniques, are presented. Finally, the white-noise of the BJT front-end is analyzed.

3.1 PTAT current generation

In Chapter 1, PNP BJTs are used to realize all the sensors, however, if available, NPN BJTs are more advantageous. They can be biased directly via the collectors, which provides more circuit design flexibility. As will be shown later, no amplifier is required to force ΔV_{be} over R_{bias}, so that the theoretical energy efficiency of the choice of NPN-based sensors is higher compared to PNP-based ones. One drawback of using NPNs is their high stress-sensitivity to package stress compared to PNPs [10] [11], however, this can be tolerated if energy-efficiency is the primary goal.

As shown in Figure 3.1, two identical NPN BJTs, Q_{RB} and Q_{LB}, are used to generate a PTAT voltage ΔV_{be}. They are biased with a current density ratio of 1:p using (p+1) unity current sources I_u, and the NPNs' base current is provided by a separate branch. Since the emitters of the NPNs are connected to ground, a closed loop can be formed by connecting their bases together with R_{bias} inserted in the loop. Consequently, the resulting emitter current is given by:

$$I_{E,LB} = \frac{V_{BE,RB} - V_{BE,LB}}{R_{bias}} \tag{3.1}$$

On the other hand, the biasing collector current is affected by β_f spread in the BJTs. A resistor R_{bias}/p is added in series with the base of Q_{RB} to compensate for this [13]. In this case, Equation 3.1 is modified to:

$$I_{E,LB} = \frac{(V_{BE,RB} + pI_{B,LB} \times \frac{R_{bias}}{p}) - V_{BE,LB}}{R_{bias}} \tag{3.2}$$

Hence, Equation 3.2 can be simplified to:

$$I_{E,LB} = \frac{V_{BE,RB} - V_{BE,LB}}{R_{bias}} + I_{B,LB} \tag{3.3}$$

Basically, a base current component has been added to the emitter current, thus canceling out the β_f dependency, such that the collector current is set to what was originally intended, as expressed in Equation 3.4:

$$I_{C,LB} = \frac{V_{BE,RB} - V_{BE,LB}}{R_{bias}} \tag{3.4}$$

This current $I_{C,LB}$ is then copied through a current mirror and sent to the readout circuit.

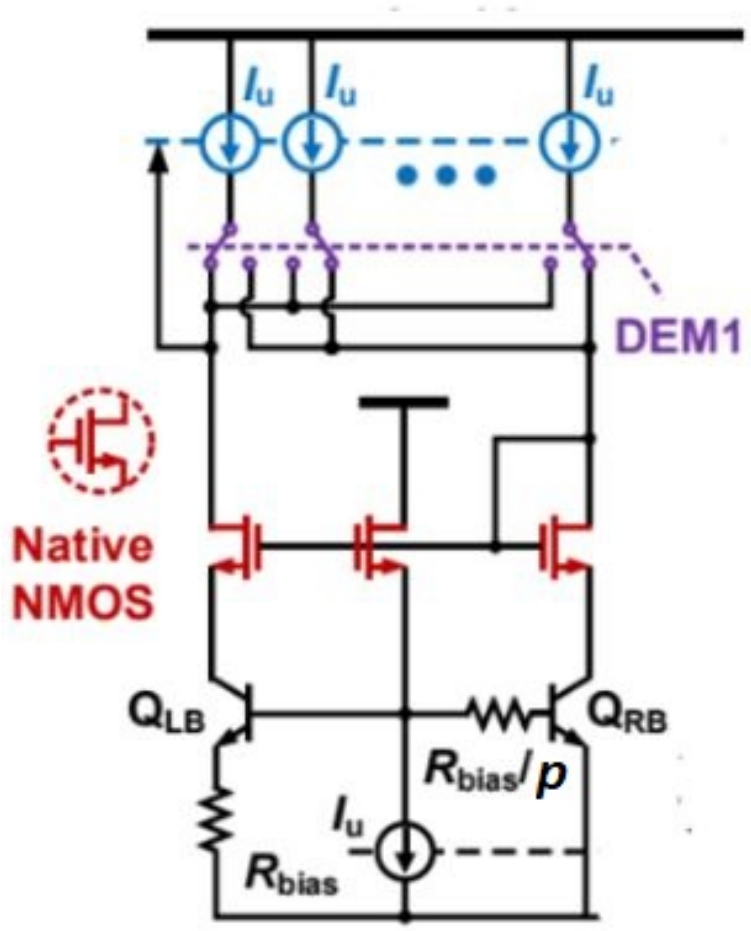


Figure 3.1: Schematic of NPN-based PTAT current generator [13]

To improve the temperature inaccuracy, the biasing resistors should have a low temperature coefficient [13]. In the chosen process (0.18-μm CMOS), the best candidate is the p+ poly-resistor (TC$\approx$ -0.02%/°C). As a result, the generated PTAT current is highly linear over the target temperature range. To improve the supply dependency, the collector voltage difference of the NPN pair is suppressed by NMOS cascodes. Native NMOS transistors are used, so that the voltage headroom is mainly limited with V_{be} of the NPN BJTs at nominal conditions [13].

The circuit realization of the PTAT current generator is shown in Figure 3.2. The emitter areas of Q_{RB} and Q_{LB} equal $10\,\mu m \times 10\,\mu m$. I_{PTAT} is generated by forcing the ΔV_{be} across the resistor R_{bias} with a value of 957 KΩ. As illustrated in Chapter 2, the generated I_{PTAT} is 53 nA at RT. The current density ratio between Q_{LB} and Q_{RB} is set to 1:7. This ratio maximizes the temperature sensitivity of I_{PTAT}, while maintaining nearly constant forward current gain β_f across the collector current density. Moreover, I_{PTAT} is much higher than the saturation current of the NPN BJT ($\sim 3 \times 10^{-17}$A). The NPN diode-connected configuration is implemented via a source follower stage, which is realized by a native NMOS transistor that also provides the NPNs' base current [13].

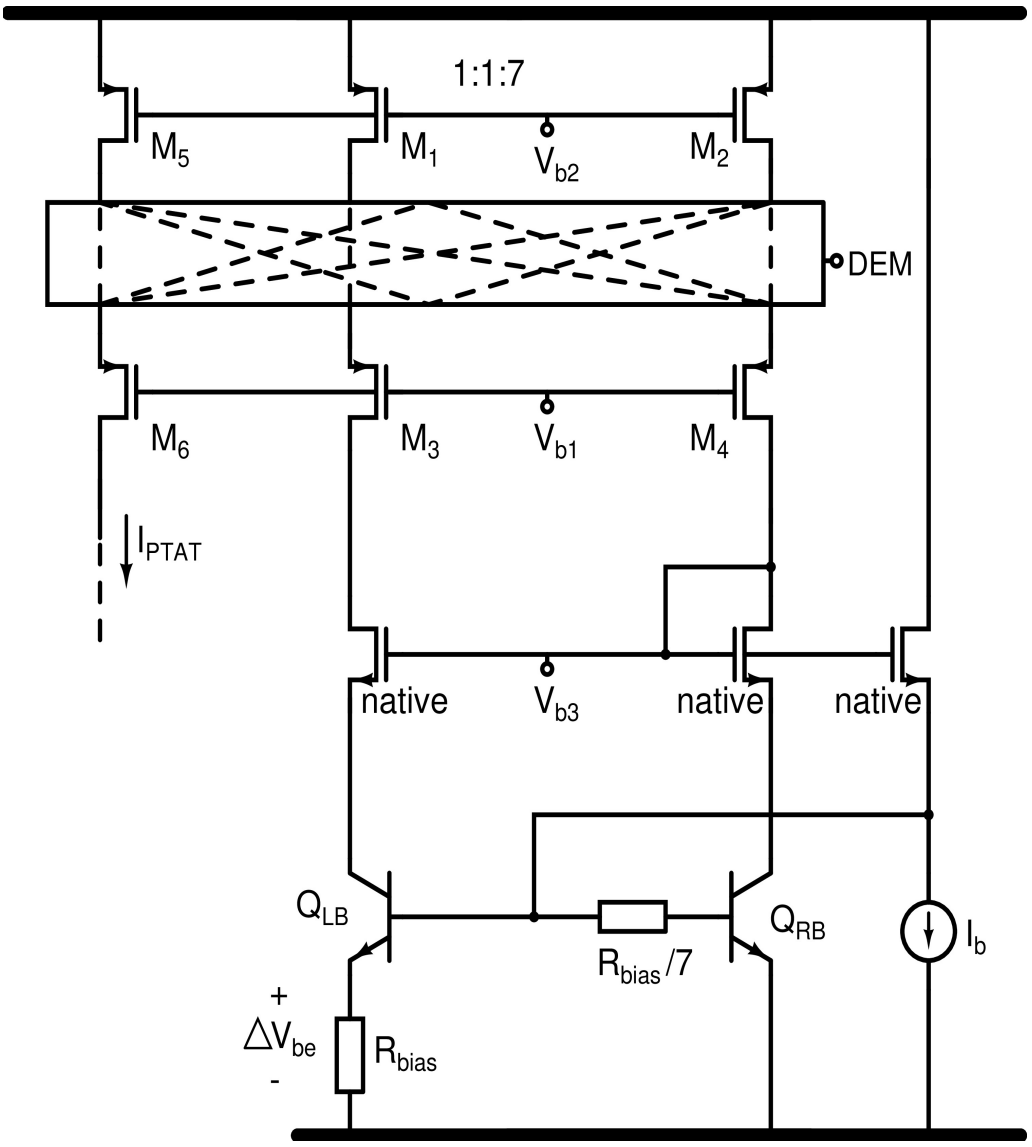


Figure 3.2: Detailed circuit realization of the PTAT current generator

The unity current sources I_u are realized with PMOS cascode transistors M_{1-6}, as shown in Figure 3.2, mainly for improving the supply dependency of the TDC. One significant source of temperature inaccuracy is the current mismatch between the PMOS current source transistors $M_{1,2,5}$. Since this current mismatch is temperature-dependent, additional non-linear spread affects I_{PTAT}. This is mitigated by employing the dynamic element matching (DEM) technique on the biasing current sources [13]. DEM modulates the $1/f$ noise and DC offset associated with $M_{1,2,5}$. To suppress the voltage transients during DEM, the DEM switches are inserted in low-voltage swing nodes between the current source transistors $M_{1,2,5}$ and their cascodes $M_{3,4,6}$ [12].

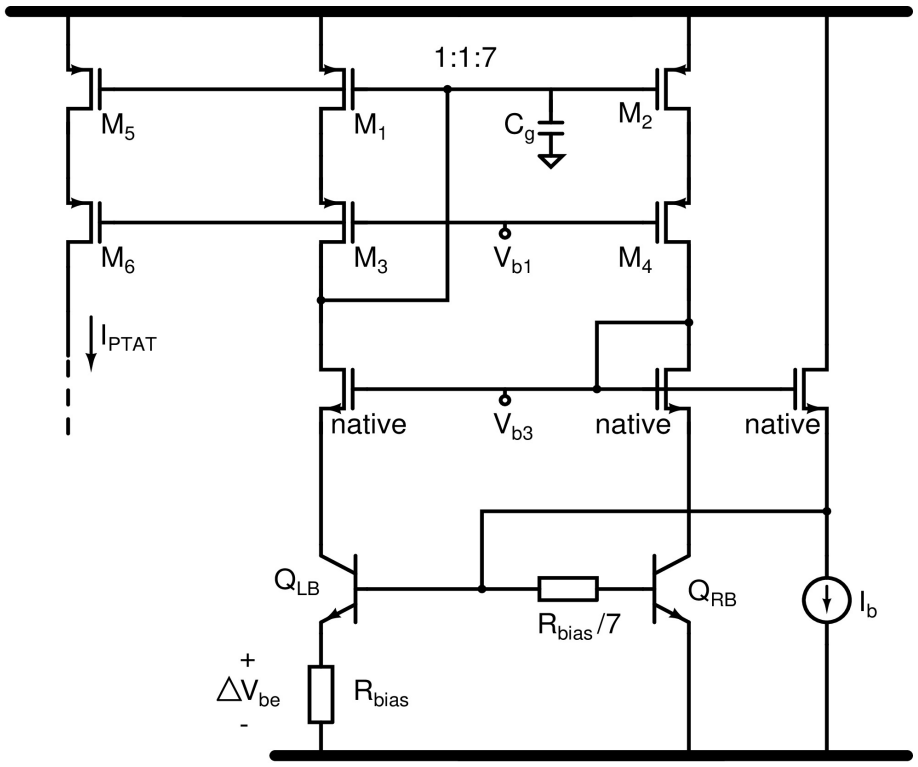


Figure 3.3: Snapshot taken for the PTAT current generator during one DEM state condition (DEM switches are not shown for clarity)

The dominant pole governing I_{PTAT} settling is determined by the high gate capacitance C_g driven by the diode-connected loop along with the low transconductance achieved from transistors $M_{1,2,5}$, as shown in Figure 3.3. Lengthy transistors are required for $M_{1,2,5}$ to achieve an accurately matched current ratio. This can easily deteriorate I_{PTAT} settling speed, which leads to slow rising/falling times for the generated I_{PTAT}. However, the current settling specification is relaxed due to the return-to-zero (RTZ) switching scheme employed in the following $\Delta\Sigma$ modulator. This will be discussed later in Chapter 4. Therefore, the PMOS current source transistors $M_{1,2,5}$ are designed with fairly long lengths to gain an accurate current matching.

Transistors $M_{1,2,5}$ are sized to $W/L = 3\,\mu m/16\,\mu m$, achieving considerably large overdrive voltage ($V_{dsat} = 90$ mV) for mitigating their thermal noise contribution. According to the process mismatch model, this sizing leads to a mismatch of 1.4%. The residual temperature error after DEM is less than 20 m°C [10]. Since the $1/f$ noise of the transistors $M_{3,4,6}$ is not modulated within the employed DEM, they are sized to a relatively large area while also not deteriorating I_{PTAT} settling speed. Thus, $M_{3,4,6}$ are sized to $W/L = 1\,\mu m/0.36\,\mu m$. The DEM clock frequency is set to one-fourth of the sampling clock frequency (16 kHz/4) of the $\Delta\Sigma$ modulator, which will be discussed later in Chapter 4. Finally, the generated I_{PTAT} is plotted across the temperature range from -40°C to 125°C, as shown in Figure 3.4. The resulting temperature error is bounded within $\pm$ 0.1°C across the full temperature range, as shown in Figure 3.5.

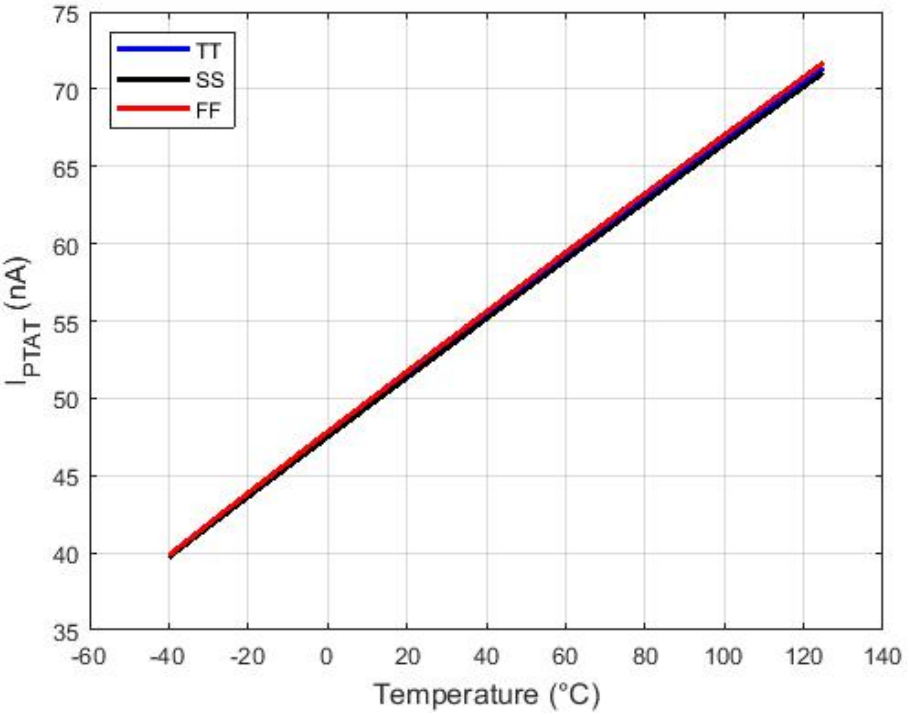


Figure 3.4: I_{PTAT} current across the temperature at different process corners

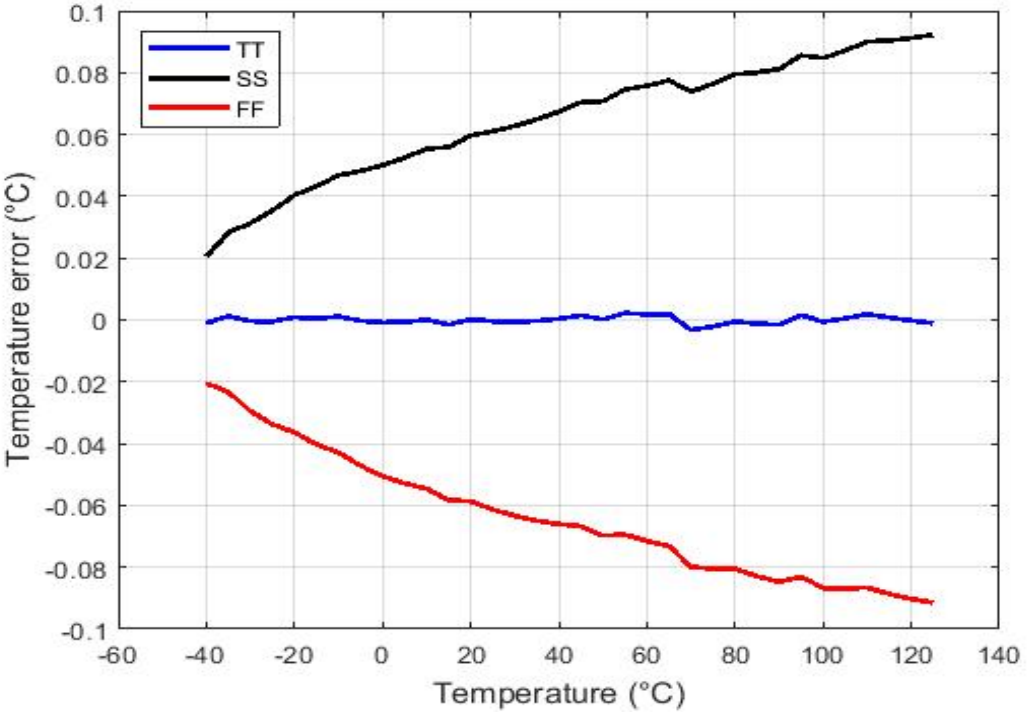


Figure 3.5: Temperature error at different process corners

3.2 CTAT current generation

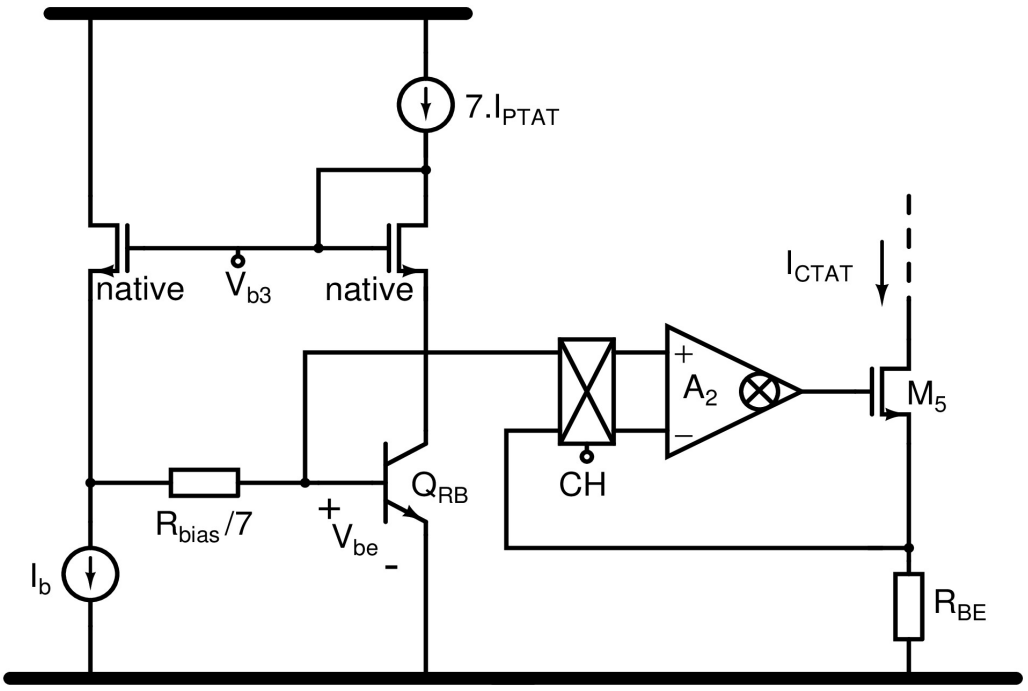


Figure 3.6: Schematic of the CTAT current generator

As shown in Figure 3.6, by reusing the NPN BJT Q_{RB} of the PTAT current generation circuit, a CTAT current I_{CTAT} is generated by forcing a voltage across the resistor R_{BE}, the same as V_{be}. This is achieved by negative feedback using an operational transconductance amplifier (OTA) A_2, shown in Figure 3.7, which is chopped to suppress the offset error [8]. To reduce the spread, the resistor type of R_{BE} is the same as that of R_{bias} in the PTAT current generation circuit. Moreover, R_{BE} and R_{bias} should be very well matched in layout commonly with a common-centroid pattern, since that any mismatch between R_{BE} and R_{bias} leads to temperature inaccuracy.

I_{CTAT} is set to 49 nA at RT, as discussed in Chapter 2, generated by an R_{BE} with a value of 12.15 MΩ. While A_2 consumes 450 nA at RT. The transistors sizing of A_2 is presented in Table 3.1. The chopping clock frequency of A_2 is set to half of the sampling clock frequency (16 kHz/2) of the ΔΣ modulator. This chopping frequency is higher than the $1/f$ noise corner frequency of A_2 and its clock can be easily generated from the sampling clock using a simple divide-by-two circuit. Finally, the generated I_{CTAT} is plotted across the temperature range from -40°C to 125°C, as shown in Figure 3.8. The resulting temperature error exhibits a PTAT spread across the temperature range, as shown in Figure 3.9. A trimmable error range of 1.56°C is achieved at 125°C.

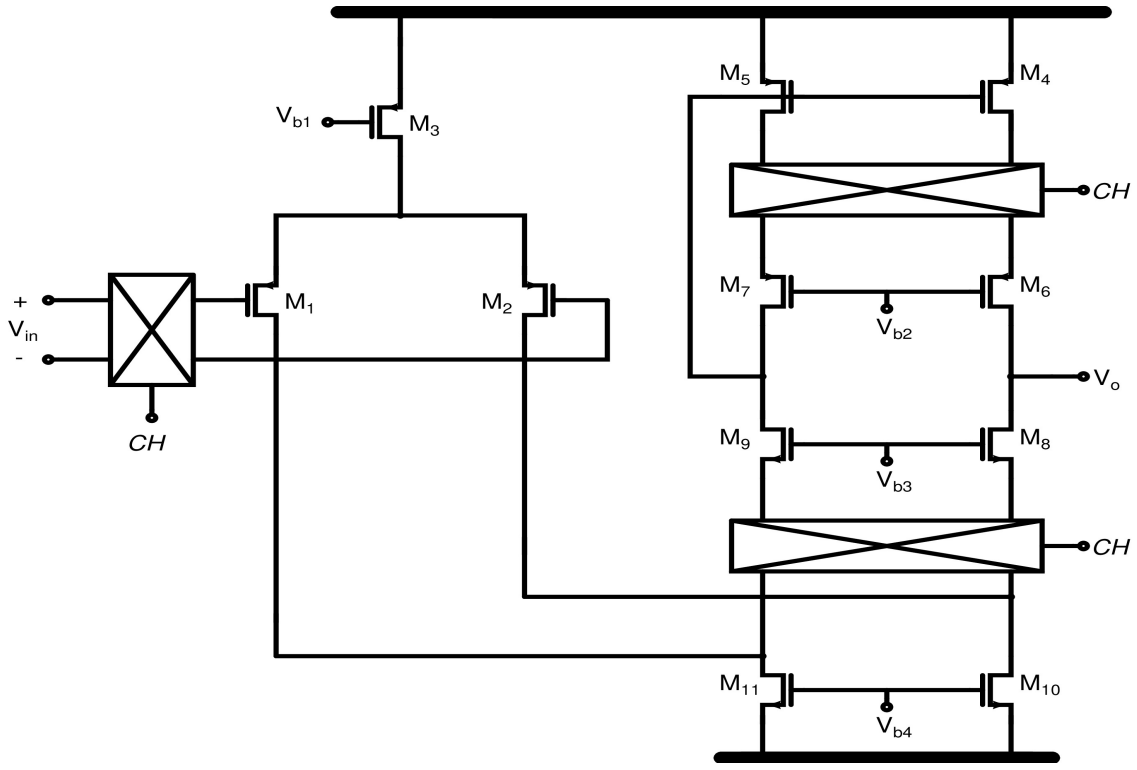


Figure 3.7: Schematic of the chopper folded-cascode OTA A_2 in the CTAT current generator

Table 3.1: Transistor sizing of A_2 in Figure 3.7

Transistor	**W(um)/L(um)**
$M_{1,2}$	20/1
M_3	12/12
$M_{4,5}$	1/12
$M_{6,7}$	1/0.3
$M_{8,9}$	1/1
$M_{10,11}$	3/17

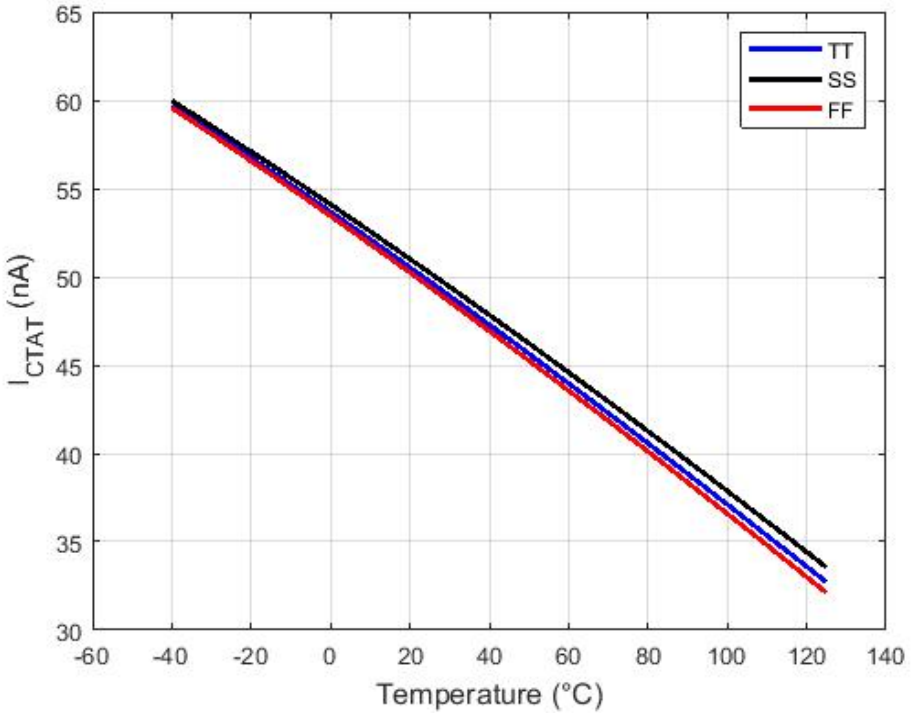


Figure 3.8: I_{CTAT} current across the temperature at different process corners

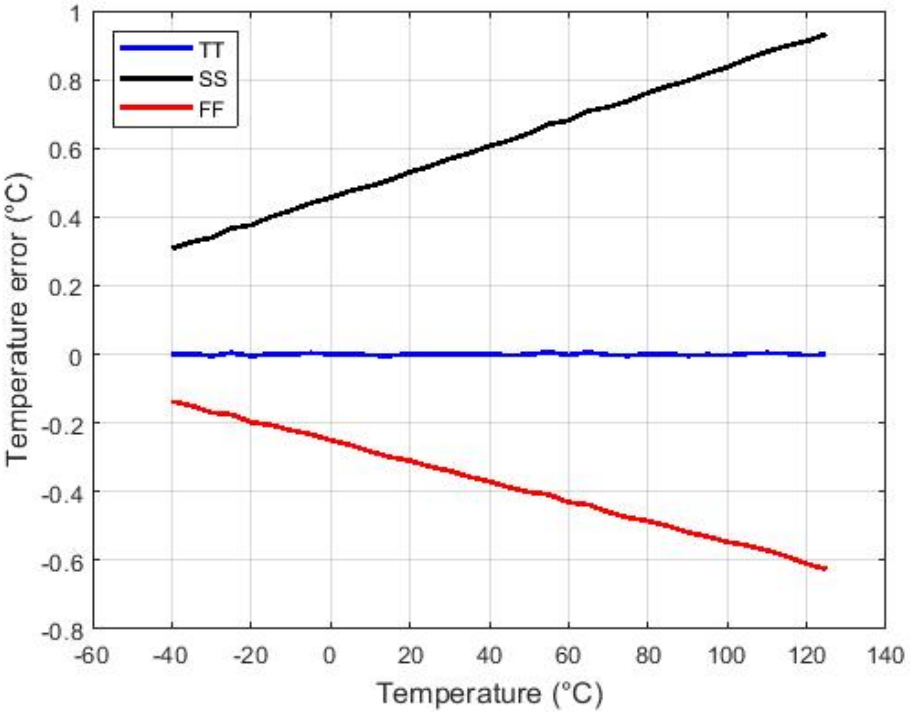


Figure 3.9: Temperature error at different process corners

3.3 Noise due to PTAT current

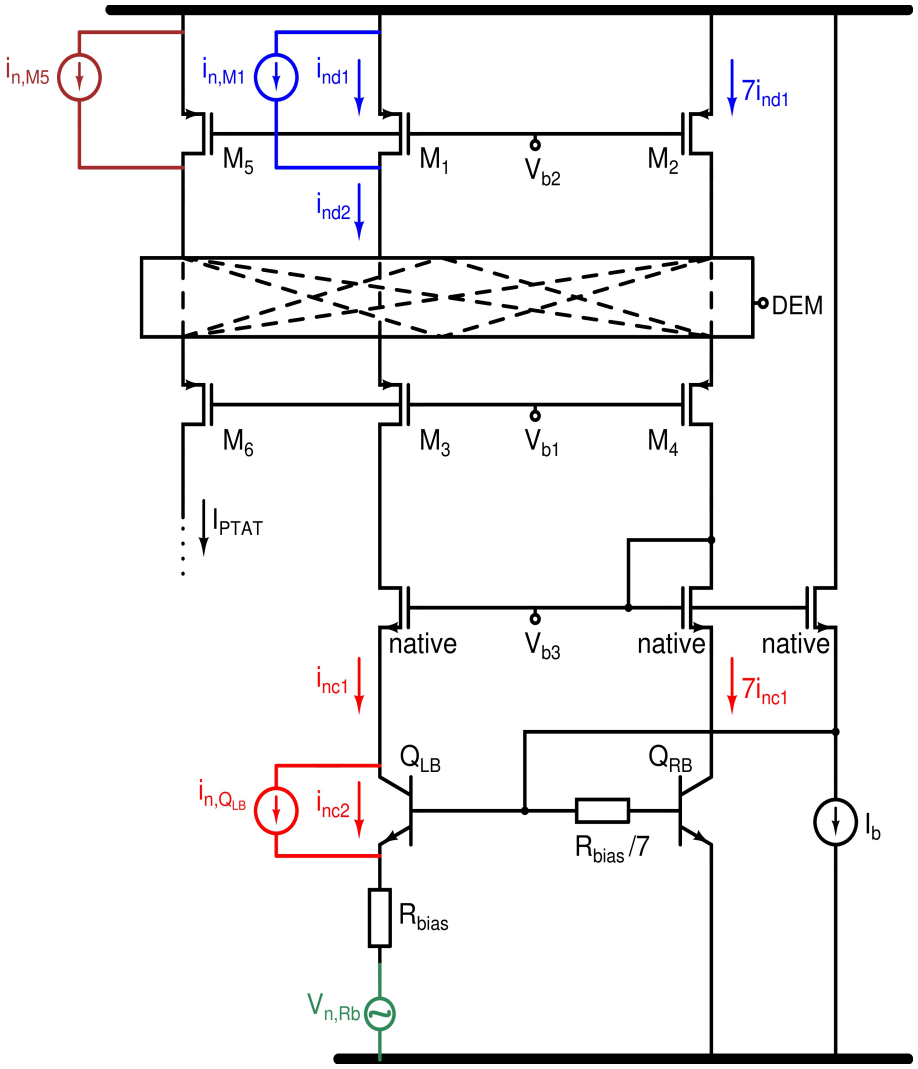


Figure 3.10: Schematic of the PTAT current generator with the dominant white-noise sources annotated (the white-noise sources of Q_{RB} and M_2 are not shown for simplicity)

The $1/f$ noise of $M_{1,2,5}$ is not considered in this analysis, due to the DEM employment. While the dominant white-noise sources, including the thermal noise of MOS transistors and resistors along with the shot noise of the BJTs' collectors, are annotated on Figure 3.10. The contribution of each noise source in the PTAT current generation circuit is calculated separately. Then, the total noise PSD is derived by summing up their contributions to I_{PTAT}.

The shot noise associated with the collector current of Q_{LB} is represented by $i_{n,QLB}$ and its effect is represented by i_{nc1} and i_{nc2} in the various branches, as shown in Figure 3.10. As stated earlier, M_1 and M_2 are scaled to a drain current ratio equal to 1:7 resulting in an equal collector current ratio between Q_{RB} and Q_{LB}, when neglecting the effect of the base currents. The generated I_{PTAT} is expressed

as:

$$I_{PTAT} = I_{c,Q_{LB}} = \frac{kT}{qR_{bias}} \, ln\, 7 \tag{3.5}$$

where k is the Boltzmann constant, T is the absolute temperature in Kelvin, and q is the electron charge. This leads to:

$$g_{m,QLB} \, R_{bias} = \, ln\, 7 \tag{3.6}$$

It is clear that:

$$i_{nc1} = i_{n,QLB} + i_{nc2} \tag{3.7}$$

Furthermore, it holds that:

$$7 \, i_{nc1} \, (\frac{1}{g_{m,QRB}}) = i_{nc1} \, R_{bias} + i_{nc2} \, (\frac{1}{g_{m,QLB}}) \tag{3.8}$$

Substituting $g_{m,QRB} = 7 \, g_{m,QLB}$ yields:

$$i_{nc1} = i_{nc1} \, R_{bias} \, g_{m,QLB} + i_{nc2} \tag{3.9}$$

Considering Equation 3.6 and comparing Equations 3.7 with 3.9, the noise contribution of Q_{LB} in I_{PTAT} is expressed as follows:

$$i_{nc1} = \frac{i_{n,QLB}}{ln\, 7} \tag{3.10}$$

Given that collector current shot noise PSD of Q_{LB} is represented by $S_{n,QLB} = 2qI_{c,QLB}$ and using Equation 3.5, the shot noise PSD contribution S_{nc1} of Q_{LB} to the PTAT current equals:

$$S_{nc1} = 1.03 \, \frac{kT}{R_{bias}} \tag{3.11}$$

Similarly, the shot noise PSD contribution S_{nc3} of Q_{RB} to the PTAT current equals:

$$S_{nc3} = 0.15 \, \frac{kT}{R_{bias}} \tag{3.12}$$

Therefore, the total shot noise PSD contribution of Q_{RB} and Q_{LB} to the PTAT current is calculated by adding Equations 3.11 and 3.12, amounting to:

$$S_{BJT} = 1.18 \, \frac{kT}{R_{bias}} \tag{3.13}$$

The thermal noise current of M_1 is represented by $i_{n,M1}$ and its effect on the current branches are represented by i_{nd1} and i_{nd2}, as shown in Figure 3.10. Hence:

$$7 \, i_{nd1} \, (\frac{1}{g_{m,QRB}}) = i_{nd2} \, R_{bias} + i_{nd2} \, (\frac{1}{g_{m,QLB}}) \tag{3.14}$$

While it is clear that:

$$i_{nd2} = i_{n,M1} + i_{nd1} \tag{3.15}$$

Given that thermal noise PSD of M_1 is represented by $S_{n,M1} = \frac{8}{3}kTg_{m,M1}$ and substituting $g_{m,QRB} = 7\,g_{m,QLB}$ yield:

$$i_{nd2} = \frac{1}{ln\,7}\,i_{n,M1} \tag{3.16}$$

Therefore, the thermal noise PSD contribution S_{nd2} of M_1 to the PTAT current equals:

$$S_{nd2} = 0.7kTg_{m,M1} \tag{3.17}$$

Considering that $g_{m,M2} = 7\,g_{m,M1}$. Similarly, the thermal noise contribution of M_2 is calculated to be:

$$S_{nd3} = 1.4kTg_{m,M1} \tag{3.18}$$

Given that $g_{m,M1} = g_{m,M5}$, the thermal noise PSD of M_5 is directly related to the PTAT current, equals:

$$S_{n,M5} = \frac{8}{3}kTg_{m,M1} \tag{3.19}$$

The thermal noise contributions of the cascode transistors, $M_{3,4,6}$ and native transistors, are negligible. Hence, the total thermal noise contribution of M_1, M_2 and M_5 to the PTAT current is calculated by adding Equations 3.17, 3.18 and 3.19 amounting to:

$$S_{MOS} = 4.77\,kTg_{m,M1} \tag{3.20}$$

The thermal noise PSD contribution of R_{bias} to the PTAT current equals:

$$S_{Rb} = 4\,\frac{kT}{R_{bias}} \tag{3.21}$$

The total white-noise PSD associated with the PTAT current S_{PTAT} is calculated by adding the results of Equations 3.13, 3.20, and 3.21, yielding:

$$S_{PTAT} = 1.18\,\frac{kT}{R_{bias}} + 4.77\,kTg_{m,M1} + 4\,\frac{kT}{R_{bias}} \tag{3.22}$$

Finally, the dominant white-noise sources along with their contributions to I_{PTAT} are summarized in Table 3.2. It is clear that the transistors M_1, M_2, and M_5 along with the resistor R_{bias} contribute by 87% of the calculated S_{PTAT}, equal to 195 fA/$\sqrt{Hz}$. This value is reasonably close to its corresponding simulated value (210 fA/$\sqrt{Hz}$), shown in Figure 3.12. The discrepancy is mainly due to the unconsidered noise contributions of the DC biasing and start-up circuits along with the DEM switches and digital logic circuits.

Table 3.2: Dominant white-noise sources associated with I_{PTAT}

Noise source	**Cont. to** I_{PTAT}	**Value** (A^2/Hz)	**Cont. to** I_{PTAT} **(%)**
Q_{RB} and Q_{LB}	$1.18\,\frac{kT}{R_{bias}}$	5.1×10^{-27}	13
M_1, M_2 and M_5	$4.77\,kTg_{m,M1}$	1.6×10^{-26}	42
R_{bias}	$4\,\frac{kT}{R_{bias}}$	1.7×10^{-26}	45

3.4 Noise due to CTAT current

Chopping attenuates the $1/f$ noise of A_2, therefore it is not considered in this analysis. Figure 3.11 shows the CTAT current generation circuit with the dominant white-noise sources are annotated. The thermal noise voltages of A_2 and R_{BE} are represented by $V_{n,A2}$, and $V_{n,BE}$, respectively. The total thermal noise PSD associated with the CTAT current S_{CTAT} is expressed as:

$$S_{CTAT} = \frac{S_{n,A2}}{R_{BE}^2} + 4\,\frac{kT}{R_{BE}} \tag{3.23}$$

where $S_{n,A2}$ is the thermal noise PSD of A_2.

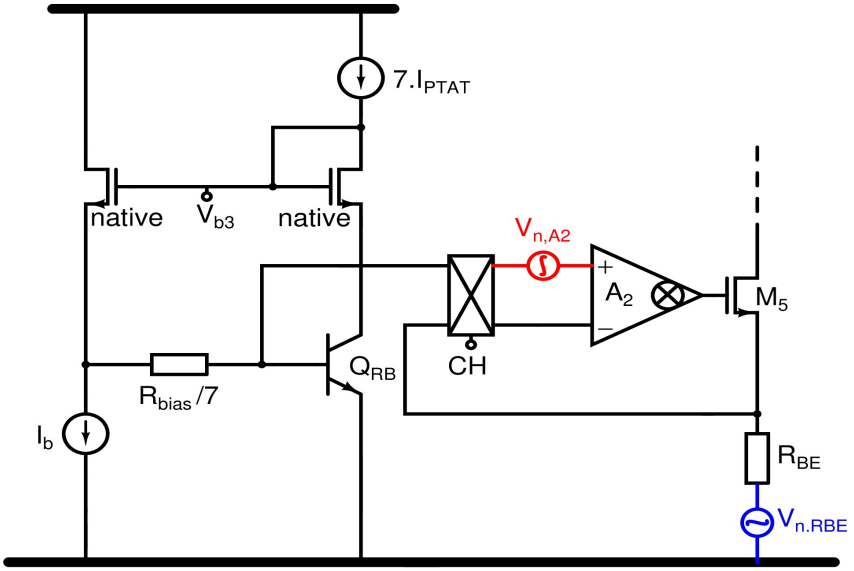


Figure 3.11: Schematic of the CTAT current generator with the dominant white-noise sources annotated

The thermal noise of the cascode M_5 is negligible. Since $1/(g_{m,QRB}R_{BE}) \ll 1$, the noise contributions of the biasing current source ($7.I_{PTAT}$) and Q_{RB} to I_{CTAT} are also negligible by design [25]. Finally, the dominant white-noise sources along with their contributions to I_{CTAT} are summarized in Table 3.3. It is clear that R_{BE} contributes by 67% of the calculated S_{CTAT}, equal to 46 fA/$\sqrt{Hz}$. This value reasonably agrees with its corresponding simulated value (52 fA/$\sqrt{Hz}$), shown in Figure 3.12.

Table 3.3: Dominant white-noise sources associated with I_{CTAT}

Noise source	**Cont. to** I_{CTAT}	**Value** (A^2/Hz)	**Cont. to** I_{CTAT} **(%)**
R_{BE}	$4\,\frac{kT}{R_{BE}}$	1.4×10^{-27}	67
A_2	$\frac{S_{n,A2}}{R_{BE}^2}$	7×10^{-28}*	33

*Simulated value from PNOISE analysis at RT

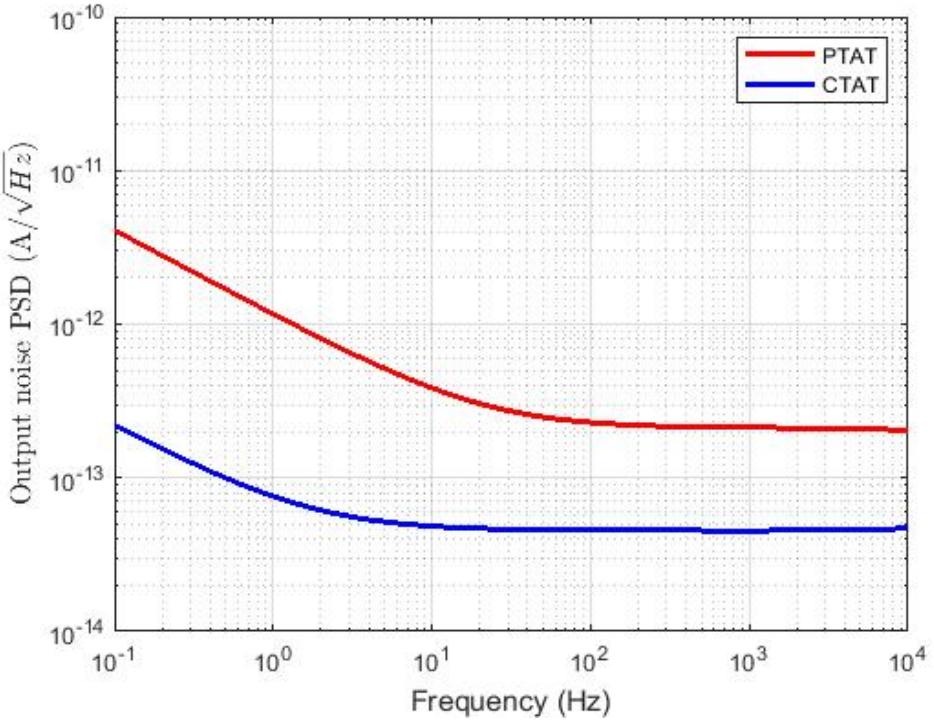


Figure 3.12: Simulated output noise current PSD ($A/\sqrt{Hz}$) associated with I_{PTAT} and I_{CTAT}

Assuming that a succeeding ideal $\Delta\Sigma$ modulator integrates S_{PTAT} and S_{CTAT} during a conversion time T_{conv}, which is equivalent to filtering the noise with a sinc filter with a noise bandwidth equal to $(1/2T_{conv})$, the integrated noise currents can then be expressed as:

$$i_{n,PTAT} = \sqrt{\left(1.18\,\frac{kT}{R_{bias}} + 4.77\,kT g_{m,M1} + 4\,\frac{kT}{R_{bias}}\right).\frac{1}{2T_{conv}}} \tag{3.24}$$

$$i_{n,CTAT} = \sqrt{\left(\frac{S_{n,A2}}{R_{BE}^2} + 4\,\frac{kT}{R_{BE}}\right).\frac{1}{2T_{conv}}} \tag{3.25}$$

Hence, the front-end resolution σ can be readily calculated as:

$$\sigma^2 = S_{I,PTAT}^T(t)^2.i_{n,PTAT}^2 + S_{I,CTAT}^T(t)^2.i_{n,CTAT}^2 \tag{3.26}$$

where $S_{I,PTAT}^T(t)$ and $S_{I,CTAT}^T(t)$ are the temperature sensitivities of I_{PTAT} and I_{CTAT}, respectively.

Using the simulated values of $i_{n,PTAT}$ and $i_{n,CTAT}$ in Figure 3.12 and the derived $S_{I,PTAT}^T(t)$ and $S_{I,CTAT}^T(t)$ at RT from Figures 3.4 and 3.8, respectively, the resulting σ is 1.5 mK at T_{conv} equal to 320 ms. While the front-end consumes 1.3 μA from 1.8 V power supply, the front-end R-FoM is 1.7 pJ.K^2.

3.5 Summary

This chapter presents the BJT front-end generating single PTAT and CTAT currents, this includes the transistor-level implementation and design considerations. Also, how various precision techniques are employed in the favor of the TDC's resolution. A detailed noise analysis for the front-end is also presented.

4 Continuous-time Delta-sigma Modulator

This chapter introduces the design considerations for the continuous-time $\Delta\Sigma$ modulator based on the charge-balancing operation. The errors due to switching transients and how return-to-zero switching mitigates these errors are discussed. The circuit implementation of the modulator key building blocks is presented.

4.1 Modulator implementation

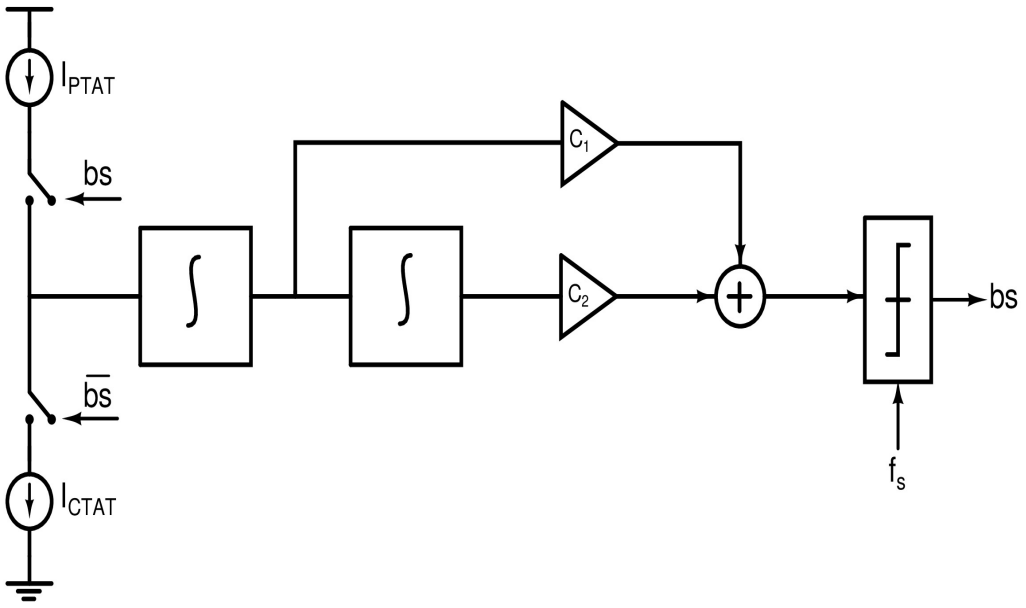


Figure 4.1: Diagram of the linear charge-balancing feed-forward 2nd order $\Delta\Sigma$ modulator

The $\Delta\Sigma$ modulator based on a linear charge-balancing operation is shown in Figure 4.1. Either a sourcing PTAT current I_{PTAT} or sinking CTAT current I_{CTAT} is applied to the 1st integrator, depending on the output bitstream (bs) value. The bitstream average value (μ) tracks the temperature information, is expressed as follows:

$$\mu = \frac{I_{PTAT}}{I_{PTAT} + I_{CTAT}} \tag{4.1}$$

A CT current integrator is chosen for the 1st stage, while a switched-capacitor (SC) integrator is employed for the 2nd stage to minimize the current consumption and chip area. Moreover, the coefficients of the SC integrator are set by a capacitor ratio, which is highly insensitive to process spread.

The $\Delta\Sigma$ modulator employs an energy-efficient feed-forward architecture, as shown in Figure 4.1, to reduce the internal signal swing. As discussed in Chapter 2, based on the target resolution equal to 3 mK in a conversion time of 320 ms, the sampling frequency of the $\Delta\Sigma$ modulator is set to 16 kHz.

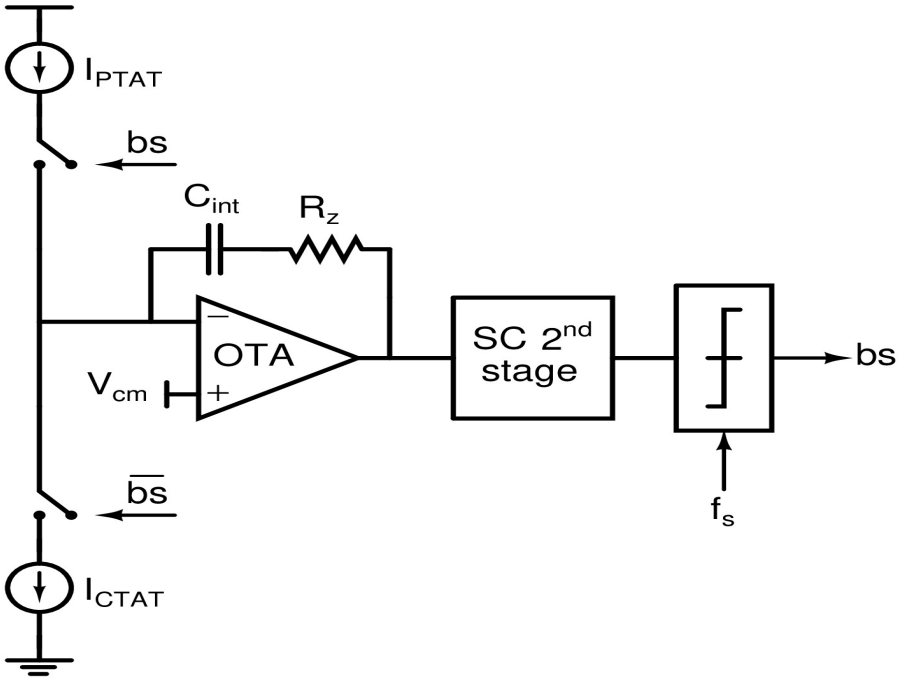


Figure 4.2: Schematic showing the 1st integrator of the $\Delta\Sigma$ modulator

The 1st stage of the $\Delta\Sigma$ modulator consists of an OTA-based current integrator, as shown in Figure 4.2. The $\Delta\Sigma$ loop ensures the integration current average is ideally zero. The output currents of the BJT front-end are connected to the virtual ground of the 1st integrator. For a 1-V_{pp} voltage swing at the output of the 1st integrator, an 8 pF MIM capacitor is employed for implementing the integration capacitor C_{int}. With the MIM capacitance density (2.063 fF/μm^2) in the design process, the expected area of C_{int} is 3878 μm^2. V_{cm} is a PTAT voltage set to $V_{DD}/2$, mainly for maintaining the OTA transistors to be well-saturated.

The OTA has finite gain due to its finite transconductance G_m and therefore also finite closed-loop input impedance ($1/G_m$). This results in non-zero overdrive voltage (I_{int}/G_m) at the OTA input. With the high output impedance of the PTAT and CTAT current sources $R_{out,p,c}$, the effect of this overdrive voltage on I_{int} becomes negligible. G_m is designed to have a reasonable swing ($\pm$ 5 mV) for such overdrive voltage at the OTA input. To achieve the required ENOB (16-bits) in 2^{10} number of clock cycles, as discussed in Chapter 2, the 1st and 2nd integrator-leakage coefficients p_1 and p_2 should be 0.999 and 0.99, respectively, as shown in Figure 4.3 [10]. This leads to a worst-case DC gain of the OTA in the 1st integrator to be higher than 80 dB.

Furthermore, the DC offset and in-band noise of the OTA have a negligible effect on the temperature resolution since they affect I_{int} also via the high impedance $R_{out,p,c}$. In other words, such DC offset and in-band noise are attenuated by a factor equal to $R_{bias}/R_{out,p}$ or $R_{BE}/R_{out,c}$, when referred back to the input of the PTAT or CTAT current generators, respectively.

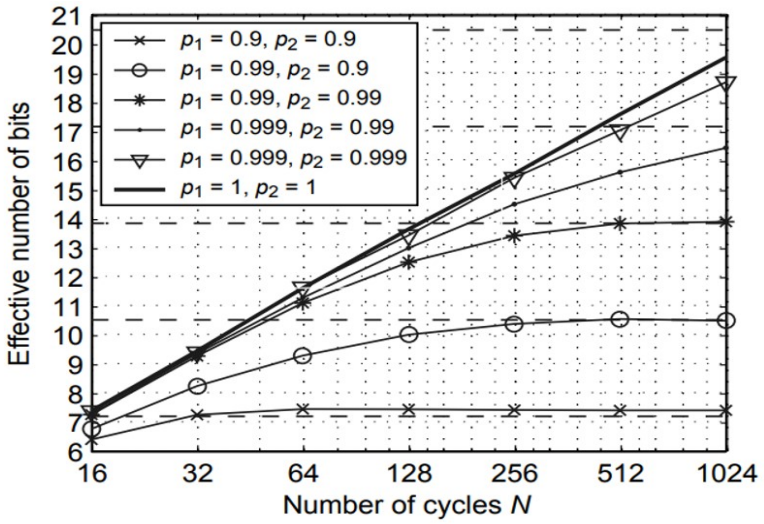


Figure 4.3: Second-order $\Delta\Sigma$ modulator: ENOB versus the number of clock cycles for different 1st and 2nd integrator-leakage coefficients p_1 and p_2, respectively. [10]

Using an OTA-based topology for realizing the CT integrator results in a right-half-plan (RHP) zero, due to the feed-forward path of C_{int} in parallel with the OTA. Thus, a zero-canceling resistor $R_z = 1/G_m$ is inserted in series with C_{int} to compensate for the phase shift. In this design, R_z is 100 kΩ.

A folded-cascode topology is chosen for realizing the OTA of the 1st stage in the $\Delta\Sigma$ modulator. The circuit schematic and transistors sizing of the OTA are shown in Figure 4.4 and Table 4.1, respectively. The output current capability of the OTA should be well above the maximum value of I_{PTAT} and I_{CTAT} across the full temperature range. The tail current source transistor M_3, limiting the OTA output current capability, consumes 700 nA at RT, while the OTA consumes 900 nA at RT.

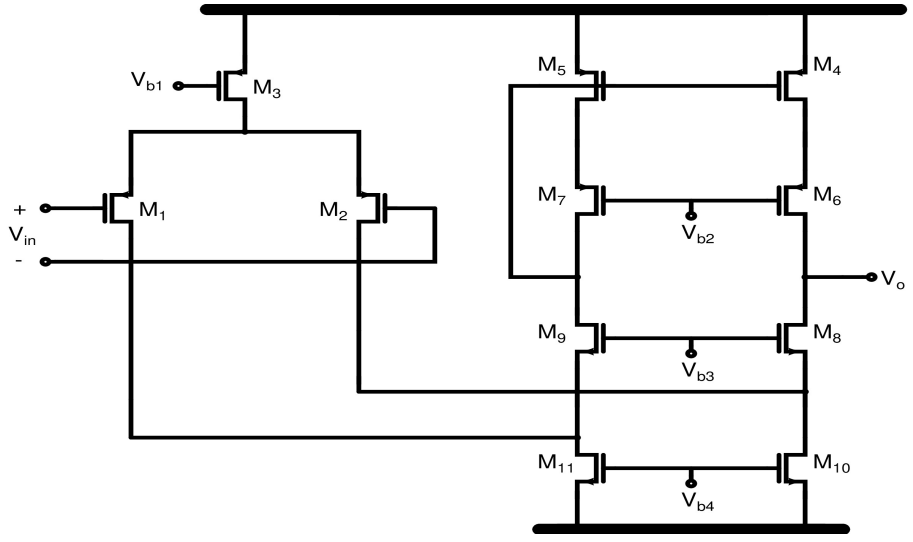


Figure 4.4: Schematic of the folded-cascode OTA of the $\Delta\Sigma$ modulator 1st integrator

Table 4.1: Transistor sizing of the folded-cascode OTA in Figure 4.4

Transistor	W(um)/L(um)
$M_{1,2}$	80/1
M_3	42/12
$M_{4,5}$	1/12
$M_{6,7}$	1/0.3
$M_{8,9}$	1/1
$M_{10,11}$	8/17

4.2 RTZ switching

Switching transients occur in the integrated current, as shown in Figure 4.5, due to the switching between the PTAT and CTAT current sources. These transients are mainly due to the finite bandwidth of the 1st integrator, which is caused by its load capacitance and any parasitic capacitance at its input, as illustrated in [10]. This results in a charge error ΔQ in the integrated charge as shown in Figure 4.6, which can easily degrades the inaccuracy and the noise floor of TDC.

With the asymmetric rise/fall times of switching transients, different ΔQ is incurred with the bitstream switching. Therefore, the integrated charge in a given clock cycle depends on the bitstream value of the previous clock cycle. This is commonly known as inter-symbol interference (ISI), leading to excess in-band quantization noise and non-linearity of the $\Delta\Sigma$ modulator [10].

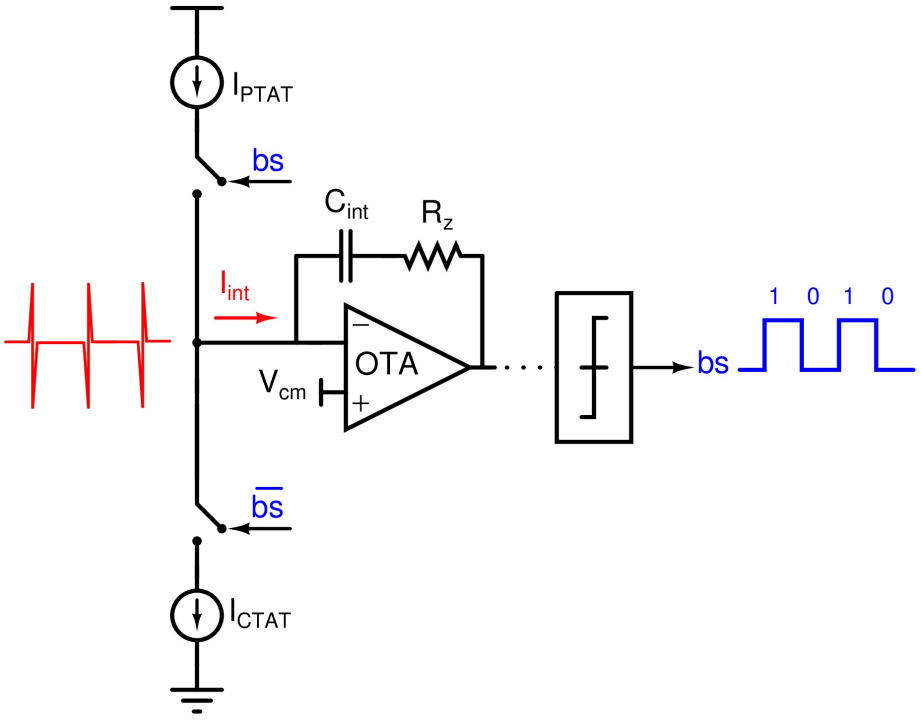


Figure 4.5: Simplified schematic for the $\Delta\Sigma$ modulator showing the switching transients of I_{int}

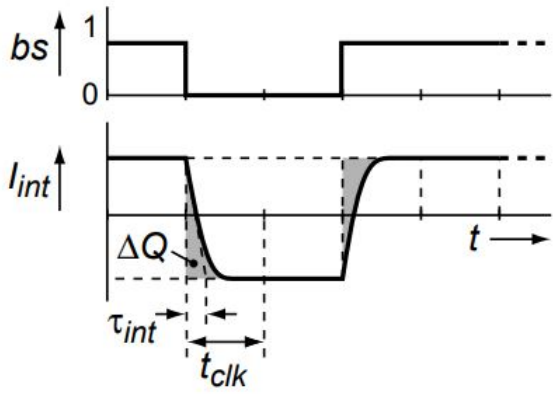


Figure 4.6: switching transients in the integrated current I_{int} lead to inter-symbol interference [10]

Switching transients may also result from the employment of dynamic error correction techniques in the BJT front-end. For instance, applying DEM to the biasing current sources in the PTAT current generator leads to DEM residuals associated with the generated PTAT current. Similarly, the chopping applied in the CTAT current generator leads to a modulated offset associated with the generated CTAT current. In both cases, the DEM residuals and modulated offset undesirably intermodulate with the bitstream of the $\Delta\Sigma$ modulator causing quantization noise folding in-band. This leads to degraded temperature resolution and inaccuracy [10].

Using the RTZ switching mitigates the charge error due to switching transients [10]. This can be done by switching I_{PTAT} and I_{CTAT} into current dumpers for a certain period, commonly known as deadband, at the end of every clock cycle. The current dumpers are implemented using cascoded diode-connected transistors, as shown in Figure 4.8(a). This eliminates the dependency on the previous clock cycle and defines rising/falling transients for every clock cycle, so that switching transients are prevented from being integrated. However, the drawback of such dumper implementation is that the generated virtual ground is not precisely equal to the virtual ground of the OTA. This results in a residual ISI leading to quantization noise folding in-band.

The timing of the $\Delta\Sigma$ modulator should be well-arranged in the way that the BJT front-end output current (i.e.integrated current) corresponds to the correct bitstream average. The BJT front-end output current should settle during the deadband. Chopping and DEM clock transitions should occur also during the deadband. Finally, the sampling clock of the $\Delta\Sigma$ modulator should be set at the beginning of the integration time, as shown in Figure 4.8(b).

To achieve an inaccuracy ($\pm 3\sigma$) due to switching transients equal to 20 mK, the employed deadband is 25% of the sampling clock period T_{CLK}, as shown in Figure 4.7. The residual temperature error is due to the mismatch of the integration time constant between I_{PTAT} and I_{CTAT} [10].

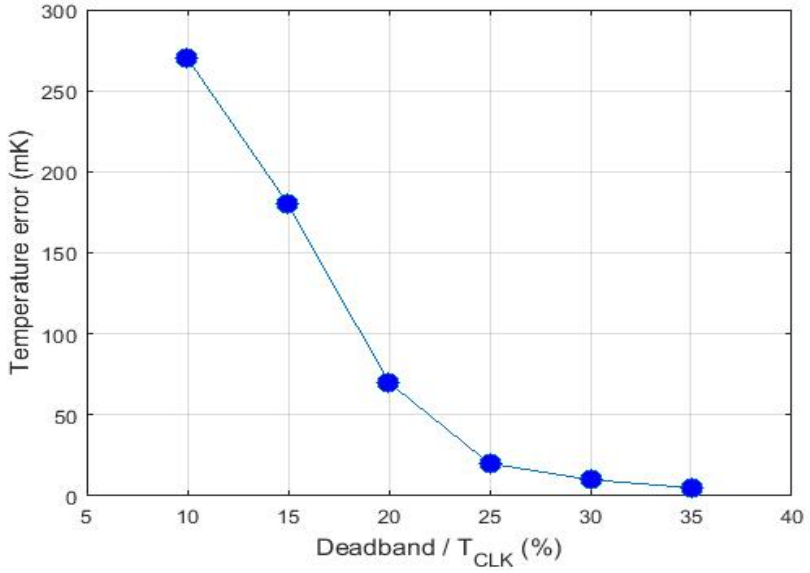
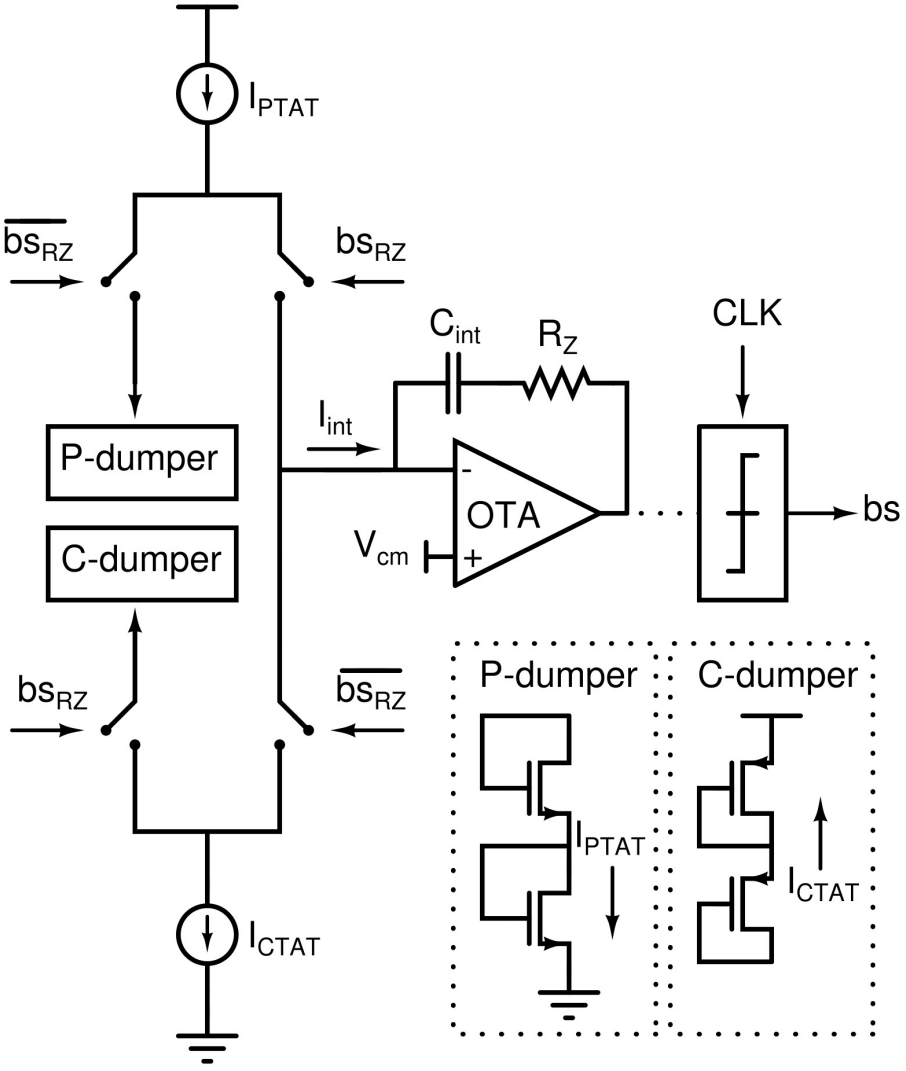


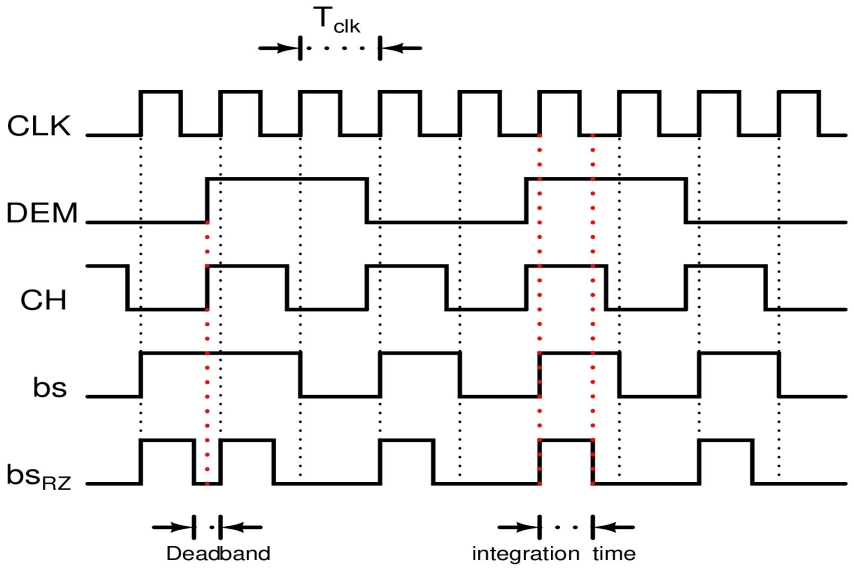
Figure 4.7: Simulated temperature error across the deadband percentage of the sampling clock period

4.3 Summary

This chapter presents the CT $\Delta\Sigma$ modulator in terms of the design steps and the circuit implementation of the key building blocks. Employing the RTZ switching scheme to mitigate the errors associated with switching transients is discussed.



(a)



(b)

Figure 4.8: (a) Schematic for the 1st integrator showing the RTZ switching scheme, (b) timing diagram

5 Simulation Results

This chapter introduces the simulation results for the BJT-based TDC in a standard 0.18-μm CMOS process. The sensor consumes 2.7 μA from a 1.8-V power supply, of which the BJT front-end and the CT $\Delta\Sigma$ modulator contribute approximately equally to the total current consumption.

5.1 Temperature inaccuracy

Figure 5.1 shows the TDC characteristic across the temperature range from -40°C to 125°C derived from Monte-Carlo (MC) simulation of 100 runs. The temperature error after systematic non-linearity removal is calculated from the difference between each bitstream average μ and the mean of all bitstream averages. This temperature error, shown in Figure 5.2, has an expected PTAT behavior, due to V_{be} PTAT spread. In this case, the residual (3σ) temperature error is ±1.3°C after removing the systematic non-linearity. After one-point trim at 25°C and removing the systematic error, the (3σ) temperature error is ±0.13°C, as shown in Figure 5.3.

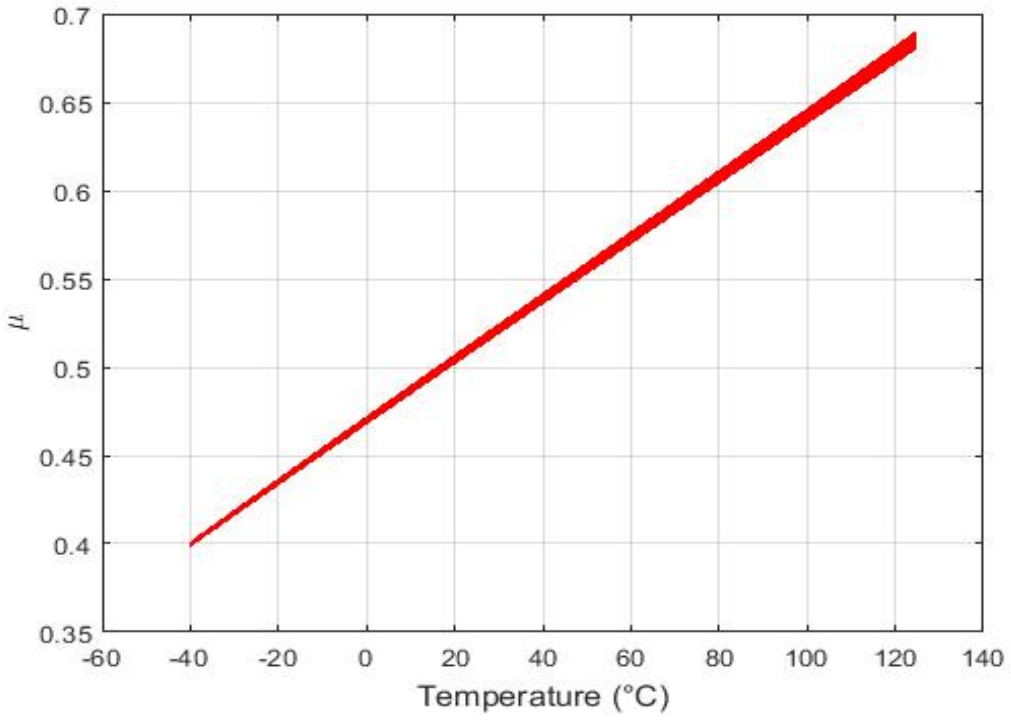


Figure 5.1: MC simulation: bitstream average μ over the temperature

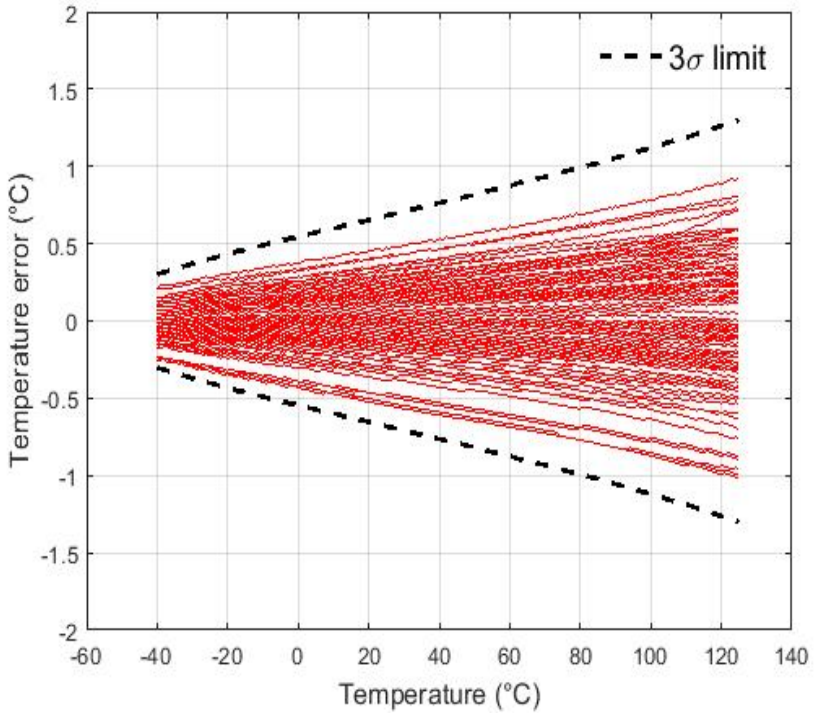


Figure 5.2: MC simulation: residual temperature error after systematic non-linearity removal

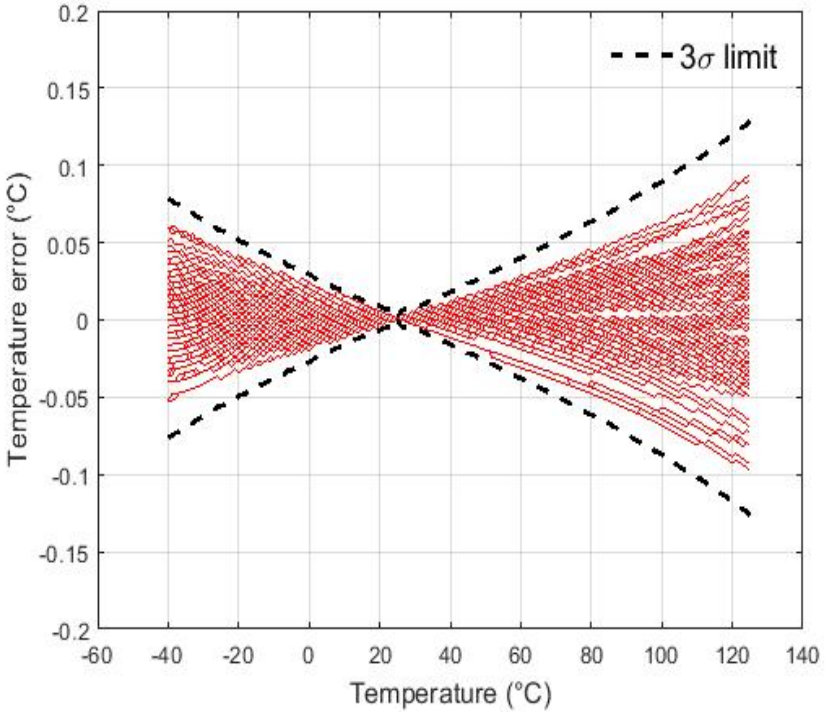


Figure 5.3: MC simulation: temperature error after one-point trim and systematic error removal

5.2 Resolution performance

To get an insight into the resolution of the designed TDC, the noise spectrum of the bitstream output, shown in Figure 5.4, is generated by allowing the TDC to run freely for 2^{18} $\Delta\Sigma$ clock cycles without any resets in between. The modulator is thus operating in a continuous mode rather than the incremental mode. The resulting noise-floor is mainly defined by the thermal noise of the sensor along with the quantization noise folded in-band due to the intermodulation between the bitstream and the DEM residuals associated with I_{PTAT}.

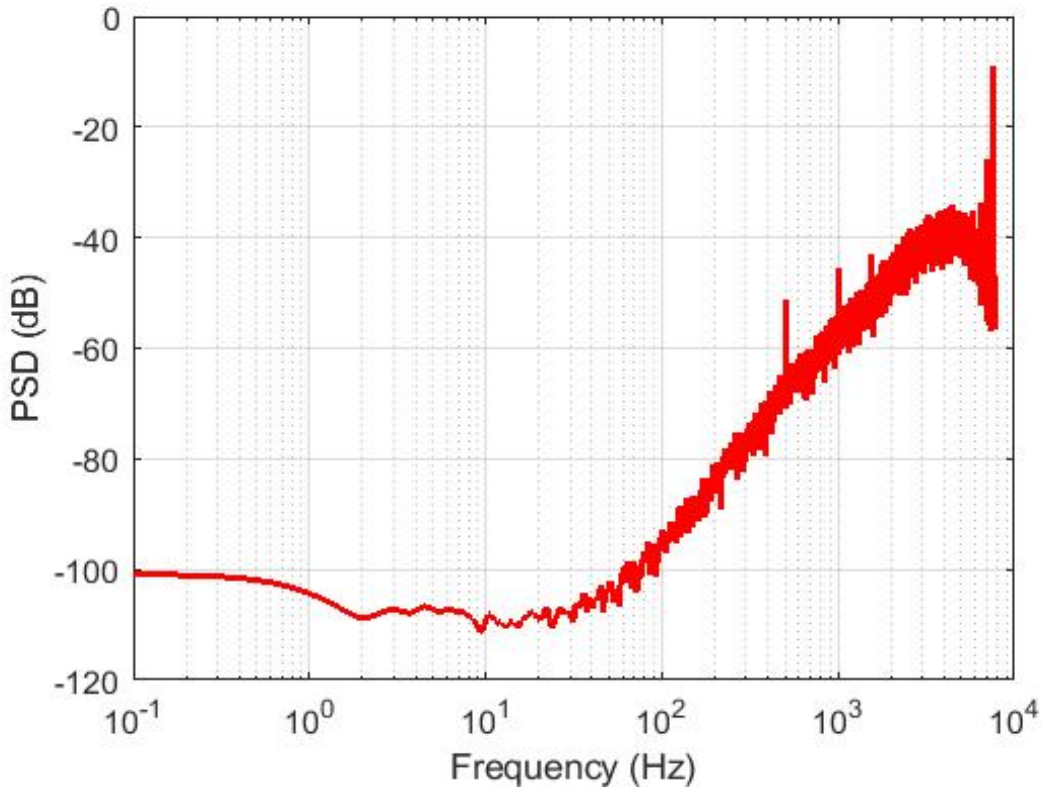


Figure 5.4: Noise FFT spectrum (dB) of the TDC bitstream

The resolution is evaluated by decimating the bitstream with a sinc^2 filter for a given conversion time T_{conv}. The temperature resolution is derived by performing multiple conversions at a stable temperature and then computing the standard deviation of the resulting temperature readings.

Figure 5.5 shows the resulting temperature resolution across the conversion time on a log-log scale. The resolution is limited by quantization noise for conversion times below 50 msec. While for larger conversion times, it is limited by the thermal noise. A temperature resolution equal to 4 mK is achieved at a conversion time equal to 202 ms. While a resolution of 3.7 mK is achieved at the target conversion time equal to 320 ms. This corresponds to a temperature noise density higher than that the derived from the bitstream noise-spectrum by a factor of $\sqrt{2}$. The discrepancy

is due to the estimation via the FFT considers an ideal brick-wall filter with a bandwidth equals to $1/2T_{conv}$. While in an incremental operation, a sinc^2 filter is employed with an effective noise bandwidth that is 1.33 times larger than that of a brick-wall filter [26]. This means that the resolution achieved at a certain conversion time needs to be scaled by a factor of $\sqrt{1.33}$. Moreover, residual quantization noise is included, as the sinc^2 filter has a 2$^{\text{nd}}$ order roll-off similar to the noise shaping behavior of the TDC.

The R-FoM is 21.3 pJ.K^2 achieved in the target conversion time of 320 msec. While the R-FoM is 15.7 pJ.K^2 in a conversion time of 202 msec, corresponding to 3156 $\Delta\Sigma$ clock cycles per conversion. However, according to Figure 5.4, the TDC should be thermal noise limited within a 40 Hz bandwidth, which corresponds to a conversion time of 12.5 msec, equivalent to around 200 $\Delta\Sigma$ clock cycles. As stated earlier, this discrepancy is due to the wider bandwidth of the sinc^2 filter compared to the ideal brick-wall filter. The achieved resolution is below the target specification as result of the quantization noise folding in-band, due to the intermodulation between the DEM residuals and the bitstream.

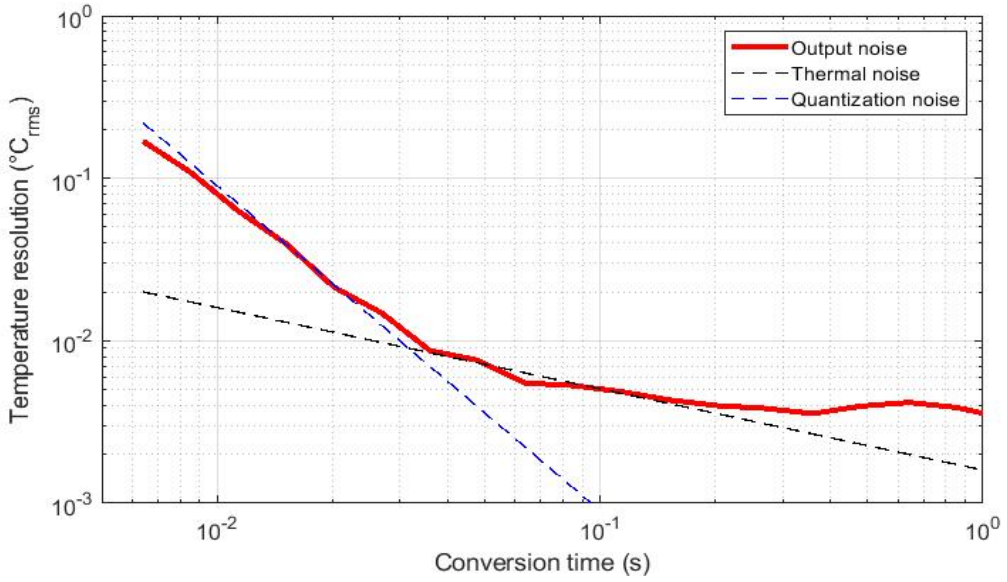


Figure 5.5: Temperature resolution (°C) across the conversion time (s)

5.3 Power-supply sensitivity

The temperature error at 25°C is plotted across the supply voltage in Figure 5.6. The supply sensitivity of the TDC is expressed by a linear extrapolation between two chosen supply voltage points. Hence, the worst-case supply sensitivity is 7.1 mK/V, simulated across the supply range of 1.6 V to 2.2 V.

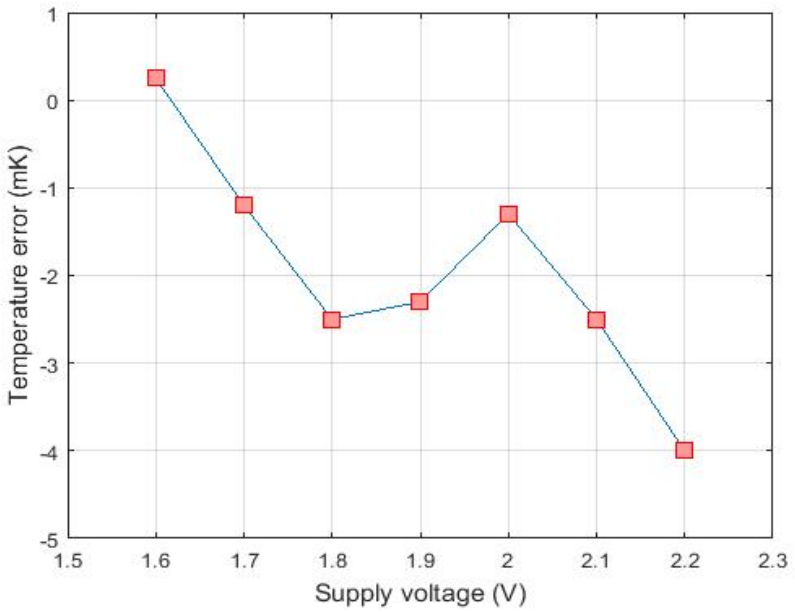


Figure 5.6: Temperature error (mK) across supply voltage (V) at 25°C

5.4 Summary

The performance of the designed TDC is summarized in Table 5.1, along with a comparison to other recent BJT-based TDCs. The designed TDC is very power-efficient with a total consumption of 4.9 μW. A resolution of 4 mK is achieved in a conversion time equal to 202 ms. This leads to a R-FoM equal to 15.7 pJ.K^2 for the designed BJT-based TDC. The supply sensitivity is excellent (0.004 °C/V). After a one-point trimming at 25°C, the TDC achieves a (3σ) inaccuracy of 0.13°C over the temperature range from -40°C to 125°C.

Table 5.1: Performance summary and comparison with the state-of-the-art BJT-based TDCs

	JSSC'17 Yousefzadeh [4]	JSSC'15 Zaliasl [1]	JSSC'17 Shalmany [2]	JSSC'13 Souri [9]	A-SSCC'19 Kumar [13]	ISSCC'20 Shalmany [12]	**This work***
Sensor type	PNP	NPN	PNP	PNP	NPN	NPN	**NPN**
Tech. (nm)	160	180	130	160	180	110	**180**
Supply-voltage (V)	1.5-2	1.5-4.5	1.5	1.5-2	1.6-2	1.125	**1.6-2**
Supply-current (μA)	4.6	4.5	4	3.4	5.5	550	**2.7**
Supply-sensitivity (°C/V)	0.01	-	0.5	-	0.005	-	**0.004**
(3σ) inaccuracy (°C) (trimming points)	±0.06 (1)	-	±0.5 (1)	±0.15 (1)	±0.12 (1)	-	**±0.13 (1)**
Temperature range	-55°C to 125°C	-40°C to 85°C	-55°C to 85°C	-55°C to 125°C	-40°C to 125°C	-35°C to 95°C	**-40°C to 125°C**
Resolution (mK)	15	25	10	20	1.67	0.65	**4**
Conversion time (ms)	5	6	18	5.3	218	0.72	**202**
Resolution FoM (pJ.K^2)	7.8	24	11	11	5.4	0.19	**15.7**

*Based on simulation results

6 Conclusion and Future work

6.1 Conclusion

This thesis introduces a BJT-based TDC architecture based on a continuous-time readout. This is mainly to get rid of the kT/C noise limitations associated with the switched-capacitor TDCs. The main objective of this work is employing a $\Delta\Sigma$ modulator for BJT front-end to provide a fully digital temperature reading on-chip. Furthermore, an optimum energy-efficiency and resolution for a BJT-based TDC are achieved, while also achieving good inaccuracy and supply sensitivity.

6.2 Future work

Some improvements to the designed TDC are suggested below as future work, mainly for improving the temperature resolution:

- Non-linear charge-balancing can be employed for the $\Delta\Sigma$ modulator for widening its range of operation. This increases the temperature sensitivity of I_{PTAT} and I_{CTAT}, which improves the resolution. This is realized in a manner different from the operation principle presented in Figure 4.1, where I_{PTAT} is digitized with respect to a temperature-independent current (I_{PTAT}+I_{CTAT}). Then, a temperature reading is extracted from μ, expressed as:

$$\mu = \frac{I_{PTAT}}{I_{PTAT} + I_{CTAT}} \tag{6.1}$$

  Alternatively, a monotonic ratio X, but a non-linear function of temperature, is digitized. X comprises precisely scaled copies of I_{PTAT} and I_{CTAT}, as both currents contain all the necessary temperature information. Thus, no need to generate the reference current. X can be mapped to the PTAT function μ through the scaling factor α, as shown in Figure 6.1. This can be easily done in the digital domain. Since α is a constant in the digital domain, it is immune to process spread. Also, α can even be made variable for trimming purposes [9] [27].

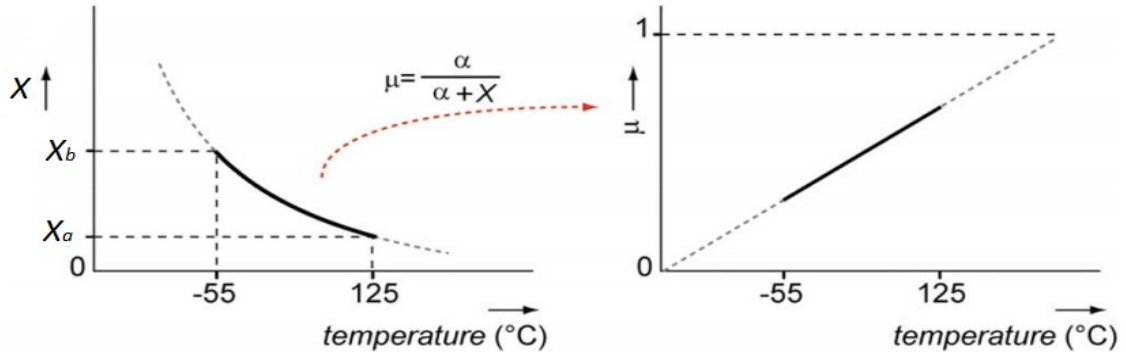


Figure 6.1: Non-linear charge balancing example: $X = f(m.I_{PTAT}, n.I_{CTAT})$ and linearized $\mu = \alpha/(\alpha + X)$ across the temperature (m and n are current-scaling factors)

- Employing a highly accurate, low power, and bi-directional current dumper serving both I_{PTAT} and I_{CTAT}. This improves the TDC resolution, since it mitigates the residual ISI caused by the mismatch between the dumper-generated and the OTA virtual grounds.
- Sharing a single OTA between the CTAT current generation and the 1^{st} integrator of the $\Delta\Sigma$ modulator. This helps to improve the energy-efficiency of the TDC. Furthermore, it leads to the removal of the CTAT current dumper, as I_{CTAT} will be continuously integrated [12].
- Third-order architecture can be employed in the $\Delta\Sigma$ modulator for providing more aggressive noise shaping, which helps in reducing the conversion time required for reaching a thermal noise limited resolution of the TDC. However, it comes at the expense of slightly increased current consumption from adding a 3^{rd} integrator to the $\Delta\Sigma$ modulator.

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