Restabilizing Mechanisms After the Onset of Thermal Instability in Bipolar Transistors

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***Abstract*—The electrothermal behavior of single- and two-finger bipolar transistors at medium- and high-current operations is studied through theoretical modeling, experimental measurements, and computer simulations. Bias conditions that border thermally stable and unstable operation regimes are described by novel analytical formulations, which for the first time include simultaneously all relevant parameters that weaken the electrothermal feedback at high currents such as ballasting resistors, current dependence of the base–emitter-voltage temperature coefficient, and high-injection effects. Hence, besides giving a correct description of thermal instability mechanisms, the developed formulations also allow the prediction and physical understanding of restabilization phenomena. The models are supported by measurements on silicon-on-glass n-p-n bipolar junction transistors and by simulation results from a novel SPICE-based electrothermal macromodel for bipolar transistors. Furthermore, the models are employed to analyze the influence of the germanium percentage in the base of SiGe heterojunction bipolar transistors on the thermal ruggedness of the device.**

***Index Terms*—Ballasting resistors, bipolar transistors, electrothermal feedback, electrothermal modeling, electrothermal restabilization, high-injection effects, silicon-on-glass technology, substrate transfer, thermal instability.**

I. Introduction

IT IS WIDELY recognized that the behavior of today's high-frequency bipolar devices and circuits is governed by coupled electrical and thermal phenomena [1]–[5], rather than by purely electrical effects. The positive current–temperature feedback may not only adversely affect the safe operating area of devices but also threatens to impose a fundamental limit to the speed [6]. Electrothermal effects in bipolar transistors have been the subject of extensive investigations in recent literature. In our previous papers [7]–[10], an extensive analysis of the two ways in which thermal instability manifests itself in bipolar transistors has been given: 1) "flyback," the onset of a negative resistance branch that also is referred to as "snapback" or "turnover" and 2) "bifurcation," the onset of an uneven current distribution among seemingly identical emitter fingers. The role of internal and external series resistances for the electrothermal response of the transistor was clarified; while the emitter and the base series resistances readily increase the power at which thermal instability occurs, the collector series resistance is less effective. However, it was observed that, at high-current levels, the voltage drop across even a relatively small external collector resistance could become so large that a thermally unstable transistor could restabilize.

In this paper, other high-current-regime restabilizing effects are identified for the first time: current and temperature dependence of the current gain, and current and temperature dependence of the base–emitter-voltage temperature coefficient. Transition points between thermally stable and unstable device operations are modeled through a novel analytical formulation applicable for both single- and two-finger bipolar transistors operating at medium- and high-current regimes. For the first time, all relevant effects are simultaneously accounted for in an analytical model. In addition, a SPICE-based macromodel for the electrothermal simulation of bipolar devices is developed, with which not only relatively simple single- and two-finger devices can be characterized but also multifinger transistors and complete circuits can be electrothermally simulated. Both the analytical formulation and SPICE macromodel are verified by experimental measurements on n-p-n bipolar junction transistors (BJTs) fabricated in a substrate-transfer silicon-on-glass technology [11]. The models are applied to investigate the effects of different device parameters on restabilization mechanisms and to compare thermal robustness of Si- and SiGe-base transistors.

II. Analytical Formulation of Thermal Instability

A. Single-Finger Bipolar Transistors

A very simple dc circuit diagram of a single-finger bipolar transistor with lumped resistors and a subcircuit accounting for self-heating are given in Fig. 1(a). r_E, r_B, and r_C represent the internal (parasitic) emitter, base, and collector resistances, respectively, while R_E, R_B, and R_C are the external (ballasting) resistors. The collector, emitter, and base currents are denoted with I_C, I_E, and I_B, respectively, and the external base–emitter, collector–base, and collector–emitter voltages are

Manuscript received July 14, 2005; revised December 27, 2005. This work was supported by the Dutch Technology Foundation (STW) and the Stichting voor Fundamenteel Onderzoek der Materie (FOM). The review of this paper was arranged by Editor C. McAndrew.

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Digital Object Identifier 10.1109/TED.2006.870277

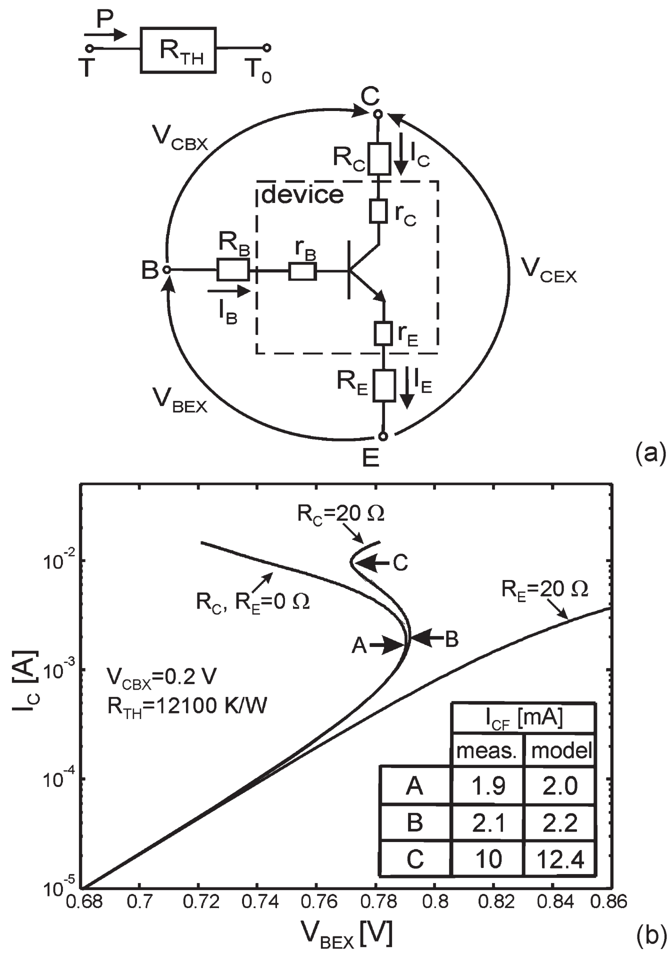

Fig. 1. (a) DC circuit diagram of an ideal single-finger bipolar transistor with lumped resistors and thermal network. (b) Measured I_E-controlled $I_C - V_{\mathrm{BEX}}$ characteristics. The inset table shows the comparison between measured and analytically modeled $I_{C,\mathrm{crit}}$ by (14).

V_{BEX}, V_{CBX}, and V_{CEX}, respectively. Fig. 1(b) shows various examples of measured I_E-controlled $I_C - V_{\mathrm{BEX}}$ characteristics.

The points in which

$$\left.\frac{\partial V_{\mathrm{BEX}}}{\partial I_C}\right|_{V_{\mathrm{CBX}}=\mathrm{const}} = 0 \tag{1}$$

determine borders of stable operation. It is well established that the flyback behavior at the points A and B is the consequence of positive current–temperature feedback [12]. Moreover, the condition (1) is also met in the point C, in which the $I_C - V_{\mathrm{BEX}}$ characteristic returns to a stable situation. In order to analyze the behavior described by (1), the bipolar transistor is modeled as follows in an analysis that is limited to the case in which avalanching does not play a significant role, i.e., for $V_{\mathrm{CE}} \ll \mathrm{BV}_{\mathrm{CE0}}$, where $\mathrm{BV}_{\mathrm{CE0}}$ is the collector–emitter breakdown voltage (BV).

In the forward active mode, the base current I_B and current gain β_F can be expressed as

$$I_B = I_{B0} \exp\left(\frac{V_{\mathrm{BEI}} + \varphi_{\mathrm{BE}}(I_C,T)\Delta T(I_C)}{nV_{T0}}\right) \tag{2}$$

$$\beta_F = \beta_0\left(1 + \frac{V_{\mathrm{CEX}} - R_{\mathrm{EC}} I_C}{V_{\mathrm{A}}}\right) \times \exp\left[\frac{\varphi_\beta(I_C,T)\Delta T(I_C) - R_{\mathrm{HI}}(I_C,T) I_C}{nV_{T0}}\right] \tag{3}$$

where I_{B0} is a temperature-insensitive parameter; $V_{\mathrm{BEI}} = V_{\mathrm{BEX}} - R_{\mathrm{EB}} I_C$; $R_{\mathrm{EB}} \approx R_E + r_E + (R_B + r_B)/\beta_0$; n is the ideality factor; V_{T0} is the thermal voltage at ambient temperature T_0; $T = T_0 + \Delta T(I_C)$ is the junction temperature; $\beta_0 \gg 1$ is the current gain at medium current levels, at ambient temperature, and under conditions with negligible Early effects; V_A is the Early voltage; and $R_{\mathrm{EC}} = R_E + R_C$. The temperature coefficients $\varphi_{\mathrm{BE}}(I_C,T)$ and $\varphi_\beta(I_C,T)$ are defined as

$$\varphi_{\mathrm{BE}}(I_C,T) = -\left.\frac{\partial V_{\mathrm{BEI}}}{\partial T}\right|_{I_B=\mathrm{const}} \tag{4}$$

which is the absolute value of the temperature coefficient of the base–emitter voltage for a fixed I_{B} and

$$\varphi_\beta(I_C,T) = -\frac{nV_{T0}}{\Delta T}\frac{\Delta E_G - B}{k}\left(\frac{1}{T} - \frac{1}{T_0}\right) \tag{5}$$

which represents a temperature coefficient of the current gain at medium currents. $\Delta E_G = E_{\mathrm{GB}} - E_{\mathrm{GE}}$ is the difference in the bandgaps of the base and the emitter, which is positive in Si BJTs [13] due to the bandgap-narrowing (BGN) mechanism in highly doped emitters [14] and is negative in GaAs and SiGe heterojunction bipolar transistors (HBTs) [15]–[17]. B is a fitting parameter needed to account for the different temperature dependence of the diffusion coefficient of holes and electrons [18], and k is the Boltzmann's constant. Moreover, the temperature-dependent gain lowering at high-injection levels is described by

$$R_{\mathrm{HI}}(I_C,T) = \frac{nV_{T0}}{I_C}\ln\left\{1 + \left[\frac{I_C}{I_H(T)}\right]^{m_{\mathrm{H}}(T)}\right\} \tag{6}$$

through the temperature-dependent parameters $I_H(T)$ and $m_H(T)$. Note that the term R_{HI} is negligible at low and medium currents, whereas it becomes a decisive parameter at high-current levels.

The collector current can then be calculated as $I_C = \beta_F I_B$ to give (7), shown at the bottom of the page, where $I_{C0} = \beta_0 I_{B0}$, and

$$\varphi_{\mathrm{TOT}}(I_C,T) = \varphi_{\mathrm{BE}}(I_C,T) + \varphi_\beta(I_C,T). \tag{8}$$

$$I_C = I_{C0}\exp\left[\frac{V_{\mathrm{BEX}} + \varphi_{\mathrm{TOT}}(I_C,T)\Delta T(I_C) + nV_{T0}\varepsilon(I_C) - R_{\mathrm{EQ}}(I_C,T) I_C}{nV_{T0}}\right] \tag{7}$$

This is the absolute value of the temperature coefficient of the base–emitter voltage for an assigned medium-level I_C, i.e., $\varphi_{\mathrm{TOT}} \simeq -\partial V_{\mathrm{BEI}}/\partial T|_{I_C}$. $\varepsilon(I_C)$ is

$$\varepsilon(I_C) = \ln\left(1 + \frac{V_{\mathrm{CEX}} - R_{\mathrm{EC}} I_C}{V_A}\right) \tag{9}$$

and the equivalent resistance term $R_{\mathrm{EQ}}(I_C, T) = R_{\mathrm{EB}} + R_{\mathrm{HI}}(I_C, T)$ accounts for the attenuation of I_C at current levels where high-injection and/or resistive effects dominate. The dissipated power

$$P = I_C(V_{\mathrm{CEX}} - R_{\mathrm{EC}} I_C) \tag{10}$$

is related to the device temperature as

$$\Delta T(I_C) = T(I_C) - T_0 = R_{\mathrm{TH}} P = R_{\mathrm{TH}} I_C (V_{\mathrm{CEX}} - R_{\mathrm{EC}} I_C) \tag{11}$$

where R_{TH} is the self-heating thermal resistance. Combining the above equations gives

$$V_{\mathrm{BEX}} = n V_{T0} \ln\left(\frac{I_C}{I_{C0}}\right) + I_C R_{\mathrm{EB}} - V_{\Delta T}(I_C) \tag{12}$$

where

$$V_{\Delta T}(I_C) = \varphi_{\mathrm{TOT}}(I_C)\Delta T(I_C) + n V_{T0}\varepsilon(I_C) - R_{\mathrm{HI}}(I_C) I_C. \tag{13}$$

Note that the function $V_{\Delta T}$ accounts for:

1) β_{F} dependence on I_C and T;
2) φ_{BE} dependence on I_C and T;
3) Early effect; and
4) self-heating.

Substituting relation (12) into (1) yields

$$I_{C,\mathrm{crit}} = \frac{n V_{T0}}{\left.\frac{dV_{\Delta T}(I_C)}{dI_C}\right|_{I_{C,\mathrm{crit}}} - R_{\mathrm{EB}}} \tag{14}$$

which implicitly relates the biasing points at the borders between thermally stable and unstable regions of single-finger bipolar transistors with all the relevant parameters. For $R_{\mathrm{EC}} = 0$ and at medium-current levels, the above expression can be written as (15), shown at the bottom of the page, which, under the conditions $\varphi_{\mathrm{TOT}} = \mathrm{const}$, can be simplified to the well-known expression [9], [19]

$$I_{C,\mathrm{crit}} = \frac{n V_{T0}}{\varphi_{\mathrm{TOT}} R_{\mathrm{TH}} V_{\mathrm{CEX}} - R_{\mathrm{EB}}}. \tag{16}$$

Contrary to (16), the more accurate (14) can have multiple solutions that determine all the transition points between stable and unstable operation.

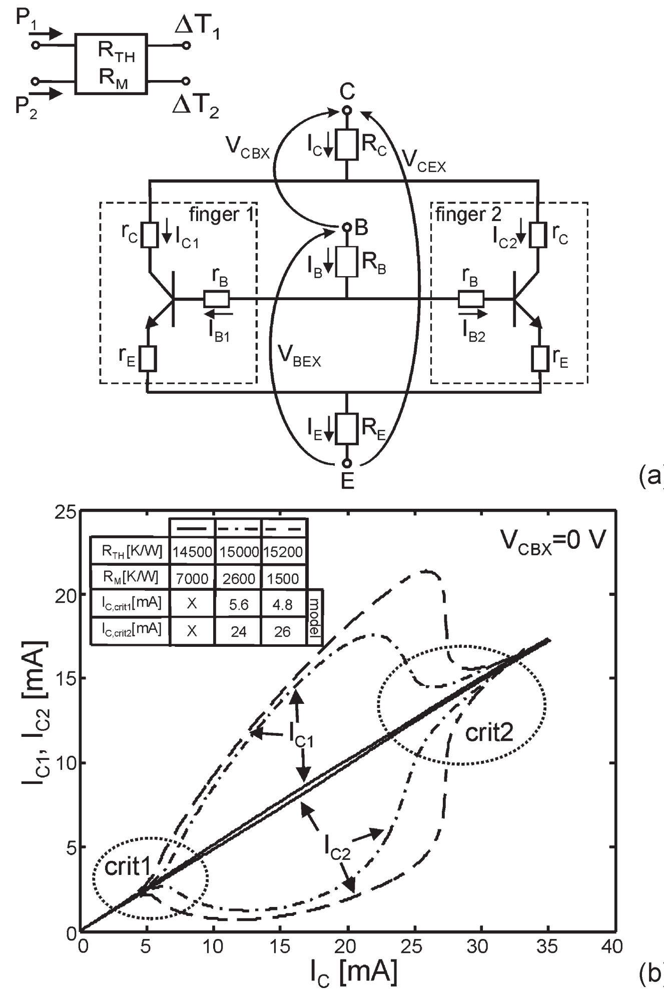

Fig. 2. (a) DC circuit diagram of an ideal two-finger bipolar transistor with lumped resistors and thermal network. (b) Measured I_E-controlled collector-current distribution for three different transistors. The inset reports results obtained from (22).

B. Two-Finger Bipolar Transistors

A simplified dc circuit diagram of a two-finger bipolar transistor is shown in Fig. 2(a). In the ideal case, where the two fingers are perfectly identical, the total currents would be equally divided between them. In reality, however, there are always small unintended differences that will be responsible for an asymmetry in current distribution in the current-controlled situation [8], [10], [20], [21]. On the other hand, as demonstrated by the measurements shown in Fig. 2(b), electrothermal interactions at high-current levels can induce restabilization, even in the absence of ballasting resistors.

In order to model this behavior, the set of relations given by (2)–(9) are applied to each finger individually identified by

$$I_{C,\mathrm{crit}} = \frac{n V_{T0}}{R_{\mathrm{TH}} V_{\mathrm{CEX}}\left(\varphi_{\mathrm{TOT}}(I_{C,\mathrm{crit}}) + I_{C,\mathrm{crit}} \left.\frac{d\varphi_{\mathrm{TOT}}(I_C)}{dI_C}\right|_{I_{C,\mathrm{crit}}}\right) - R_{\mathrm{EB}}} \tag{15}$$

subscripts 1 and 2. Expressions for I_{C1} and I_{C2} can be derived from (7) and combined to yield

$$\begin{aligned} nV_{T0} \ln\left(\frac{I_{C1}}{I_{C2}}\right) &= \varphi_{\mathrm{TOT}}(I_{C1}, T_1)\Delta T(I_{C1}, I_{C2}) - R_{\mathrm{HI}}(I_{C1}, T_1) I_{C1} \\ &\quad - \varphi_{\mathrm{TOT}}(I_{C2}, T_2)\Delta T(I_{C2}, I_{C1}) + R_{\mathrm{HI}}(I_{C2}, T_2) I_{C2} \\ &\quad - r_{\mathrm{EB}}(I_{C1} - I_{C2}) \end{aligned} \tag{17}$$

where $r_{\mathrm{EB}} \approx r_E + r_B/\beta_0$. The finger temperatures can be calculated as

$$\Delta T(I_{Ci}, I_{Cj}) = R_{\mathrm{TH}} V_{\mathrm{CE}} I_{Ci} + R_M V_{\mathrm{CE}} I_{Cj} \tag{18}$$

where $i, j (i \neq j)$ are the finger numbers, R_M is the mutual thermal coupling resistance, and $V_{\mathrm{CE}} = V_{\mathrm{CEX}} - (I_{C1} + I_{C2}) R_{\mathrm{EC}}$. In the following, I_{C1} and I_{C2} are expressed as

$$I_{C1} = \frac{I_C}{2} + \frac{\Delta I_C}{2}, \quad I_{C2} = \frac{I_C}{2} - \frac{\Delta I_C}{2}. \tag{19}$$

After some manipulation, (17) becomes

$$\begin{aligned} nV_{T0} \ln\left(\frac{I_C + \Delta I_C}{I_C - \Delta I_C}\right) &= V_{\Delta T}\left(\frac{I_C + \Delta I_C}{2}, I_C\right) \\ &\quad - V_{\Delta T}\left(\frac{I_C - \Delta I_C}{2}, I_C\right) - r_{\mathrm{EB}} \Delta I_C \end{aligned} \tag{20}$$

where

$$\begin{aligned} V_{\Delta T}(x, y) &= \varphi_{\mathrm{TOT}}(x, T_0 + xV_{\mathrm{CE}}(R_{\mathrm{TH}} - R_M) + yV_{\mathrm{CE}} R_M) \\ &\quad \times [xV_{\mathrm{CE}}(R_{\mathrm{TH}} - R_M) + yV_{\mathrm{CE}} R_M] \\ &\quad - R_{\mathrm{HI}}(x, T_0 + xV_{\mathrm{CE}}(R_{\mathrm{TH}} - R_M) + yV_{\mathrm{CE}} R_M) \cdot x \end{aligned} \tag{21}$$

with R_{HI} and φ_{TOT} defined as (6) and (8), respectively. Compared to the single-finger situation, $V_{\Delta T}$ now accounts for the mutual thermal coupling R_M, while Early effect and external resistors do not play any role due to the symmetry of the system [see Fig. 2(a)]. The boundary points of thermal stability seen in Fig. 2(b) can be found from (20) for $\Delta I_C \to 0$. This leads to

$$I_{C,\mathrm{crit}} = \frac{2nV_{T0}}{\left.\frac{\partial V_{\Delta T}(x,y)}{\partial x}\right|_{\substack{x = \frac{I_{C,\mathrm{crit}}}{2} \\ y = I_{C,\mathrm{crit}}}} - r_{\mathrm{EB}}}. \tag{22}$$

Note that the mathematical form of (14) and (22) is the same. When a constant φ_{TOT} is assumed and both external resistors and high-current effects are excluded, (22) reduces to

$$I_{C,\mathrm{crit}} = \frac{2nV_{T0}}{V_{\mathrm{CEX}} \varphi_{\mathrm{TOT}} (R_{\mathrm{TH}} - R_M) - r_{\mathrm{EB}}} \tag{23}$$

which can have only one solution and coincides with the expression derived in [10].

III. SPICE-Based Macromodel for Electrothermal Simulations

In contrast to the relatively simple computer code necessary for calculating the "critical" points by using (14) and (22), the evaluation of the overall current–voltage characteristics, such as those shown in Figs. 1(b) and 2(b), requires a higher level of complexity; for example, the calculation can be based on solving the nonlinear algebraic system of the equations that are for each finger given by (2)–(11). A more circuit-oriented approach to the problem is to modify transistor models available in already-existing commercial tools for circuit simulations and make them capable of solving electronics problems in which electrothermal coupling cannot be neglected. The program SPICE, for example, is in itself not equipped for the description of electrothermal behavior, since the temperature of the entire circuit is assigned prior to simulation and remains constant, independent of dissipated power. Thus, self-heating of individual devices and thermal coupling are not accounted for.

The method usually adopted to enable electrothermal simulations in SPICE is the structural macromodeling technique by which the built-in device model is expanded with supplementary passive and active standard components in order to describe specific transistor phenomena such as the thermal interactions [22], [23]. An effective alternative is the analog behavioral macromodeling (ABM), which makes use of a powerful facility introduced in latest SPICE versions [24]. A number of the laws governing the electrical and thermal device behavior can be easily modeled by means of voltage-controlled voltage and current sources (denoted with ABM and ABM/I in the SPICE schematic, respectively) that allow a straightforward "in-line" implementation of a large variety of algebraic equations. The effectiveness of this approach for the electrothermal simulation of power MOSFETs and BJTs has been clearly demonstrated in the past [25], [26]. The developed macromodels have proven to be flexible and accurate, while at the same time requiring an analysis time comparable to that needed when using standard SPICE elements. Lastly, it is noteworthy that ABM-based electrothermal subcircuits are manageable in all the modern SPICE-like simulation codes that support the ABM facilities.

An example of an electrothermal SPICE ABM-based macromodel is shown in Fig. 3. The subcircuit representing the elementary transistor [see Fig. 3(a)] is encased by a dashed line. It is fully derived from the mathematical expressions given by (2)–(10). The macromodel is built for the simulation of bipolar device behavior in the forward active mode, and in Fig. 3(a) it is connected in a common-base configuration. The input quantities are the base voltage "B," the emitter current "E," the collector voltage "C," and the increase of junction temperature "ΔT" above ambient presented as an input voltage. The diode "D" is used to describe the "internal" base–emitter junction behavior. Since this intrinsic SPICE device has a constant temperature T_0 during the whole simulation run, it draws a temperature-independent current given by

$$I_{B,\mathrm{diode}} = I_B(V_{\mathrm{BEI}}, T_0) = I_{B0} \exp\left(\frac{V_{\mathrm{BEI}}}{nV_{T0}}\right). \tag{24}$$

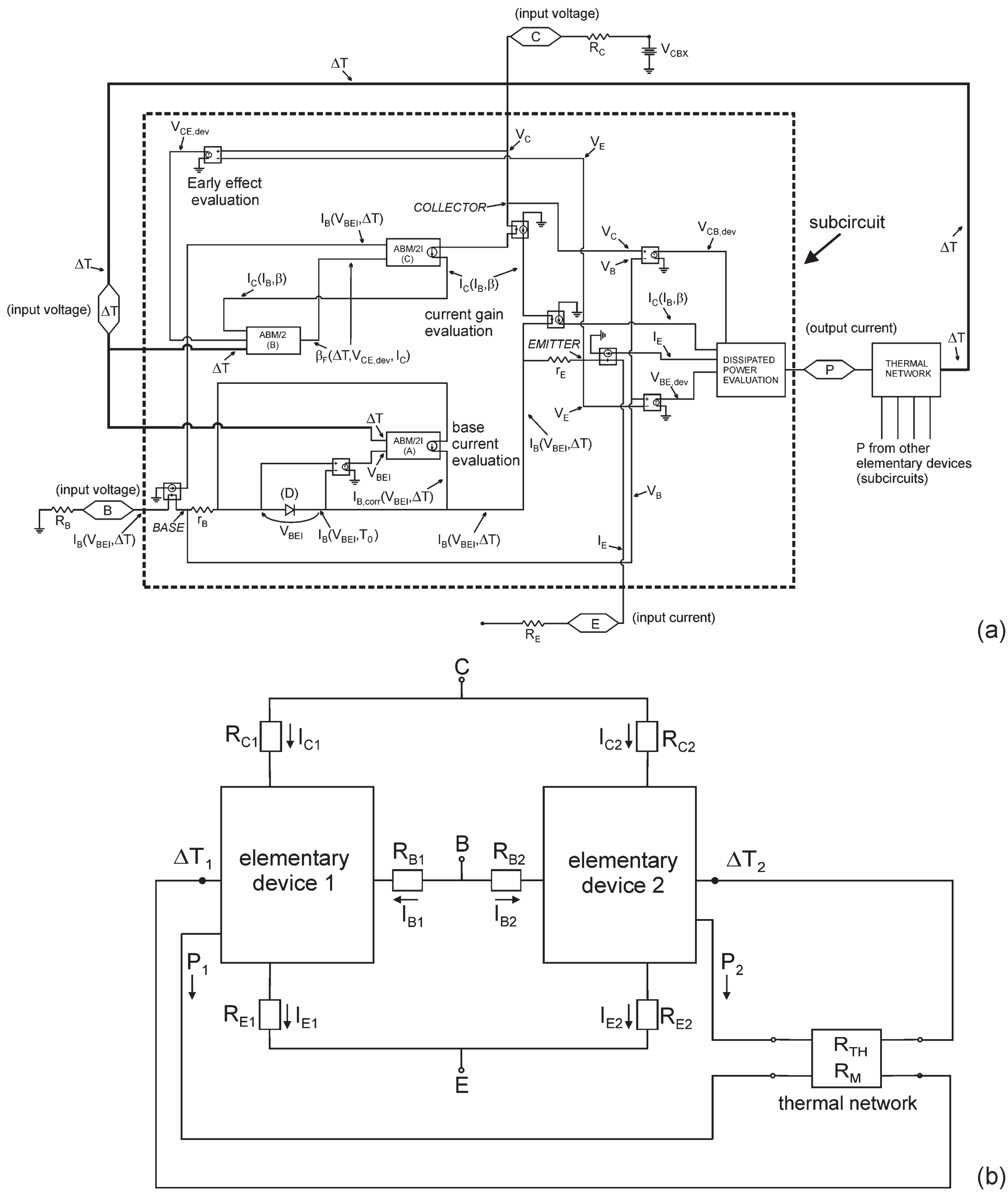

Fig. 3. (a) Detailed diagram of the ABM-based SPICE macromodel for BJTs in the common–base configuration. The subcircuit corresponding to a single transistor is depicted. (b) Block diagram of a two-finger transistor.

To introduce temperature dependence, a correction current

$$I_{B,\text{corr}}(V_{\text{BEI}}, \Delta T) = I_{B0} \cdot \left[\exp\left(\frac{V_{\text{BEI}} + \varphi_{\text{BE}}\Delta T}{nV_{T0}}\right) - \exp\left(\frac{V_{\text{BEI}}}{nV_{T0}}\right)\right] \quad (25)$$

is added to the model through the element ABM/2I (A), where the "2" refers to the number of block inputs. The sum of the two currents $I_{B,\text{diode}}$ and $I_{B,\text{corr}}$ gives the temperature-dependent base current I_B expressed by (2).

The source ABM/2 (B) forces a voltage corresponding to β_F, which is computed from I_C, V_{CEX}, and ΔT, according to (3). I_C is, in turn, computed through ABM/2I (C) by simply multiplying the base current I_B and the current gain β_F.

In the common–base configuration, the dissipated power given by (10) can be expressed as a function of the base–emitter voltage and collector–base voltage

$$P = V_{\text{BE,dev}} I_E + V_{\text{CB,dev}} I_C \quad (26)$$

with

$$\begin{aligned} V_{\text{BE,dev}} &= V_{\text{BEI}} + r_E I_E + r_B I_B \\ V_{\text{CB,dev}} &= V_{\text{CBX}} - R_C I_C + R_B I_B. \end{aligned} \quad (27)$$

The above expression for P is implemented in the SPICE model and is used as an input variable of the thermal feedback network represented by an equivalent electrical circuit. In a more general case where N elementary devices are connected in a circuit of N transistors, or form an N-finger device, the thermal network is described by

$$\Delta T_i = \sum_{j=1}^{N} R_{\mathrm{TH},ij} P_j \tag{28}$$

where ΔT_i is the increase of the temperature of the ith finger with respect to T_0. Note that the thermal resistances $R_{\mathrm{TH},ij}$ are treated as electrical ones. In Fig. 3(b), the two elementary transistors are connected in parallel to form a two-finger device; similarly, a multifinger device or a circuit that consists of a number of transistors can be effortlessly created.

The proposed dc approach can readily be extended to the dynamic case, by including the inherent transistor capacitances in the electrical subcircuit and considering an *RC* thermal equivalent network. However, care should be taken in the dissipated power evaluation: (26) may lead to inaccuracies due to energy storage elements in the transistor subcircuit, which do not contribute to the self-heating and should not be accounted for [27].

To conclude this section, we want to remark that some tools currently adopted in the IC computer-aided design (CAD) area include bipolar transistor models that allow activation of self-heating (e.g., the BJT model MEXTRAM 504 [28] available in ADS [29]); such models are equipped with a thermal node and the temperature increase above ambient is evaluated through an internal thermal circuit. A possible alternative to the above SPICE approach would lie in adopting these codes after enabling the still absent mutual coupling between transistors (as in, e.g., [30]). On the other hand, exploiting the model described in Section I, which is based on a straightforward parameter-extraction methodology, is simple and gives accurate results (see Section V).

IV. Experimental Verification

All the electrical measurements are performed on silicon-on-glass bipolar test structures [11]: single- and two-finger n-p-n BJTs with emitter areas of 20×1 μm^2 and $2 \times (20 \times 1)$ μm^2 are considered. The model parameters are extracted from isothermal characteristics of single-finger devices. For example, $\varphi_{\mathrm{BE}}(I_C, T)$, $\varphi_\beta(I_C, T)$, and $R_{\mathrm{HI}}(I_C, T)$ from (4)–(6) are extracted and modeled from the measured data given in Fig. 4(a) and (b), as suggested in [7], [31], and [32]

$$\varphi_{\mathrm{BE}}(I_C, T) = \varphi_0 - \varphi_1 \ln \frac{I_C}{\beta_F I_{\mathrm{B0}}} \tag{29}$$

and

$$\begin{aligned} I_{\mathrm{H}}(T) &= I_{\mathrm{H0}} - a_{\mathrm{H}} \Delta T \\ m_{\mathrm{H}}(T) &= m_{\mathrm{H0}} - b_{\mathrm{H}} \Delta T. \end{aligned} \tag{30}$$

R_{TH} and R_M are measured using the lock-in measurement technique described in [33]. The extracted parameters are given in Table I.

The $I_C - V_{\mathrm{BEX}}$ characteristics of a single-finger device with $R_{\mathrm{TH}} = 12\,100$ K/W are measured in an I_E-controlled setup. Fig. 1(b) shows three characteristics for $V_{\mathrm{CBX}} = 0.2$ V: one without external resistors and the other two with an added R_C or R_E of 20 Ω. The arrows indicate the critical points, which are also calculated through an iterative process applied to condition (14) and reported in the inset. A very good agreement between the model and experiments is observed. It is shown that, although an external collector resistance provides a restabilizing effect, it is much less effective than ballasting the emitter in weakening the electrothermal feedback. This is due to the fact that R_E directly reduces the internal base–emitter voltage, which governs the current handled by the device, while R_C only lowers the dissipated power level.

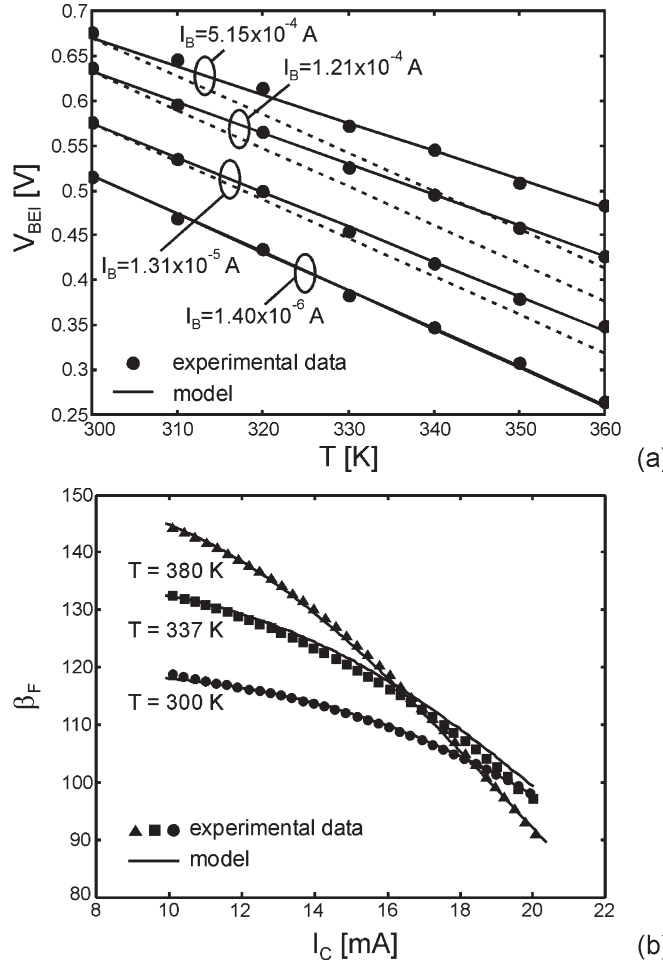

Fig. 4. Isothermal (pulsed) measurements of: (a) internal base–emitter voltage as a function of temperature for different I_B values. The symbols are measured data extracted from the Gummel plots at different temperatures; the dashed lines are parallel to the lowest I_B-fixed curve (φ_{BE} independent of the base current); the solid lines are the modeled curves that guarantee the best fit with the experimental data. (b) Current gain as a function of collector current for various temperatures.

In Fig. 2(b), the measured collector-current distribution is shown for several two-finger devices with different (R_{TH}, R_M) values. The measurements are performed in an I_E-controlled setup for $V_{\mathrm{CBX}} = 0$ V. The critical points are calculated by the model (22) and reported in the inset of the figure. As can be seen, the model gives a good prediction of both the critical point 1 and the critical point 2. In the case of the most thermally coupled fingers, the device remains stable for any value of the biasing current, as foreseen by the model.

TABLE I
EXTRACTED MODEL PARAMETERS

Parameters	***Values***
I_{B0} [A]	2.5×10^{-19}
β_0	120
V_A [V]	12
n	1
φ_0 [V/K]	3.8×10^{-3}
φ_1 [V/K]	7.8×10^{-5}
m_{H0}	4.17
b_H [1/K]	6.1×10^{-3}
I_{H0} [A]	0.0287
a_H [A/K]	7.825×10^{-5}
B [meV]	65
N_E [cm^{-3}]	10^{21}
N_B [cm^{-3}]	10^{18}
r_E [Ω]	3
r_B [Ω]	60
r_C [Ω]	3

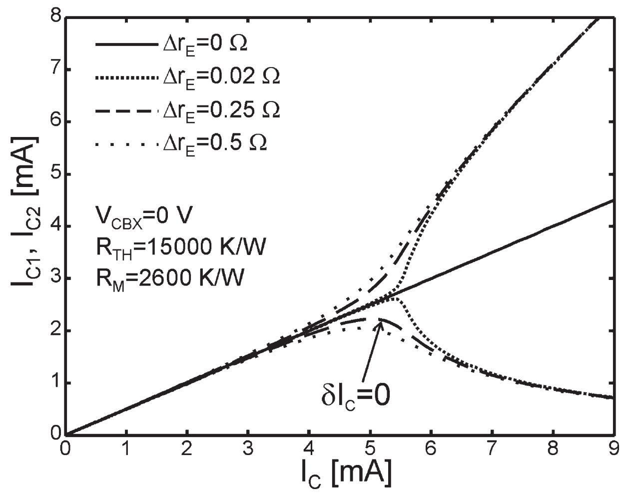

Fig. 6. SPICE-simulated collector current as a function of discrepancy between the two fingers. The bifurcation is induced through a difference Δr_{E} between the internal emitter resistances.

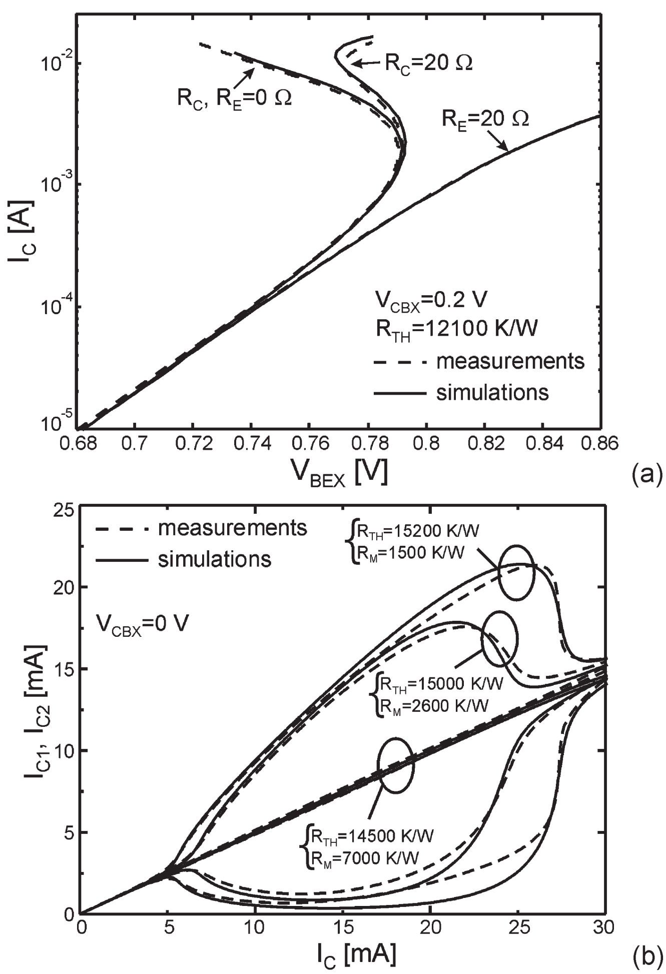

Fig. 5. Collector-current distribution of I_E-controlled (a) one-finger and (b) two-finger silicon-on-glass BJTs: comparison between measured and SPICE-simulated characteristics.

Experimental measurements are also compared with the characteristics simulated by the SPICE macromodel. This comparison for the same set of devices from Figs. 1(b) and 2(b) is presented in Fig. 5; as can be seen, a very good agreement is obtained for each situation and for any value of the input bias.

V. DISCUSSION AND MODEL APPLICATIONS

As mentioned in Section II-B, the current-bifurcation phenomenon in two-finger bipolar devices results from the fact that the two fingers are never identical in a realistic case. In order to simulate the experimental behavior by SPICE, a difference in the parameters of the two elementary devices must be introduced. For example, this can be achieved by assigning a slightly different value of the emitter series resistance to the finger 1 as compared to the finger 2. In Fig. 6, the region around the current-bifurcation point is plotted for different values of $\Delta r_E = r_{E1} - r_{E2}$. The critical-point condition given by (22) defines the current bifurcation for the case in which there is an infinitely small difference between the fingers, i.e., $\Delta r_E \to 0$. As the difference in device parameters grows, the abruptness of the transition from stable to unstable case is less sharp, and the critical point must be defined in another way, for example, as the point at which the lower current has reached its maximum, i.e., where $\delta I_{C1} = 0$ [8]. Nevertheless, since the elementary devices are in principle made with the smallest possible differences, expression (22) is in practice a very useful approximation. When external ballasting resistors are connected to each individual finger (e.g., R_{E1}, R_{B1}, and R_{C1} for finger 1 and R_{E2}, R_{B2}, and R_{C2} for finger 2), inequalities (e.g., $R_{E1} \neq R_{E2}$) produce an effect similar to that of Δr_E shown in Fig. 6.

The existence and position of the critical points depend on several compounded effects, rather than only on one dominating factor. This is illustrated in Fig. 7, where the SPICE electrothermal simulations of a two-finger BJT are presented as a function of the model complexity. Compared to the complete model (solid line), an unacceptable error occurs even for low current values if the thermal coupling is not accounted for (long dashes). The correct values for the coefficient φ_{BE} are modeled through an appropriate choice of the parameters φ_0 and φ_1.

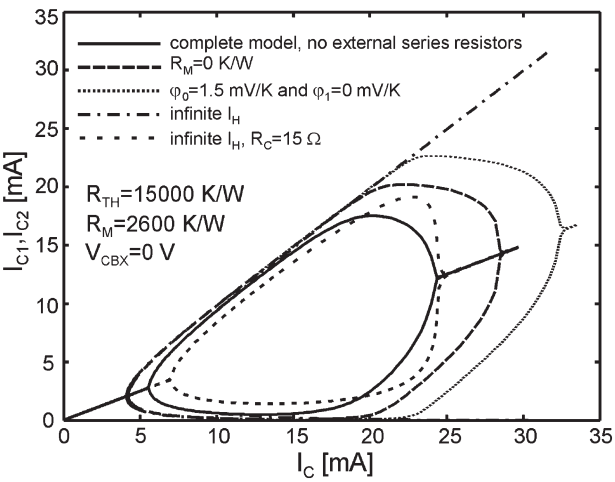

Fig. 7. SPICE-simulated collector-current distribution of two-finger bipolar transistors as a function of device-model complexity.

Adopting a constant value for $\varphi_{\rm BE}$ (as in, e.g., [8], [12], [19], and [34]) fails to accurately predict the device behavior (dotted line) since the current dependence modeled by (29) weakens the electrothermal feedback in the system. Likewise, a reduction of the temperature coefficient of the current gain also introduces a negative feedback at high currents [31], [32]; isothermal measurements from Fig. 4(b) indicate that φ_β can even become negative at high-injection levels, and thus can be decisive for the restabilization. Indeed, it can be seen that neglecting such an effect $(I_H \rightarrow \infty)$ actually leads to the switching off of the colder finger (dot–dashed line). Finally, it is also observed that the stabilization can be restored by introducing sufficiently high external resistors (small dashes).

Fig. 8(a) and (b) depicts the curves attained for various values of ballasting resistors per finger on the emitter, $R_{E1} = R_{E2}$, and on the base, $R_{B1} = R_{B2}$. This shows how the ballasting not only increases the $I_{C,\rm crit}$ for bifurcation but also decreases the $I_{C,\rm crit}$ for restabilization, giving an overall more stable device.

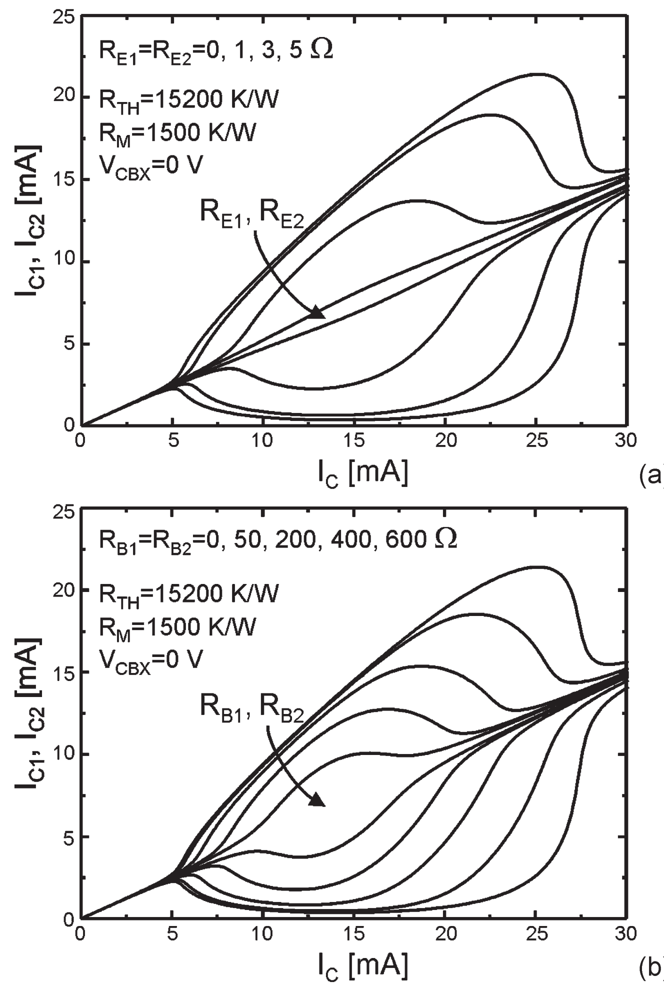

Fig. 8. SPICE-simulated individual collector currents for two-finger silicon-on-glass transistors in I_E-controlled conditions at $V_{\rm CBX} = 0$ V. (a) Effect of ballasting each emitter finger with a resistance value $R_{E1} = R_{E2}$. (b) Effect of ballasting the base of each emitter finger with a resistance value $R_{B1} = R_{B2}$.

A. Safe Operating Area

Fig. 9 illustrates the solution loci of (22) in the ($V_{\rm CEX}$, I_C) plane for I_E-controlled two-finger BJTs with equal $R_{\rm TH}$ and different R_M values. The curves represent the borders between stable (left) and unstable (right) operation regimes. For low $V_{\rm CEX}$ values, all transistors are unconditionally stable. As the collector voltage increases, the devices are triggered into the asymmetrical operating mode and the current instability range increases with the applied voltage. It is noteworthy that the thermal ruggedness increases with increasing R_M. This has in the past also been empirically demonstrated by the beneficial influence of thermal shunt resistors between emitters in GaAs-based HBTs [35], [36].

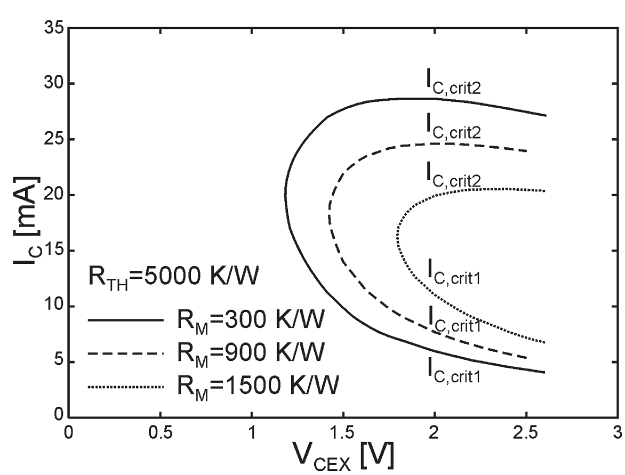

Fig. 9. Solution loci of (22) in the ($V_{\rm CEX}$, I_C) plane for several two-finger bipolar transistors with equal $R_{\rm TH}$ and different R_M values.

B. Si- Versus SiGe-Base Transistors

From (14), the aggregate effect of coefficients $\varphi_{\rm BE}$ and φ_β, and their derivatives with respect to I_C determines the thermal behavior. While Si transistors can restabilize at high-current levels due to reduction of $\varphi_{\rm BE}$ and φ_β as I_C increases, SiGe-base devices [16], [17] and GaAs-based HBTs [15] can both be designed so that even for low and medium currents, φ_β will

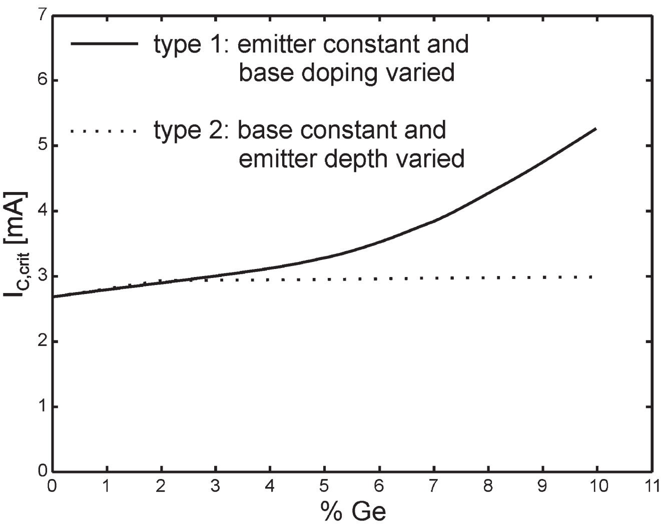

Fig. 10. Modeled critical current of single-finger SiGe-base transistors as a function of germanium percentage. Model (14) is used for the calculations.

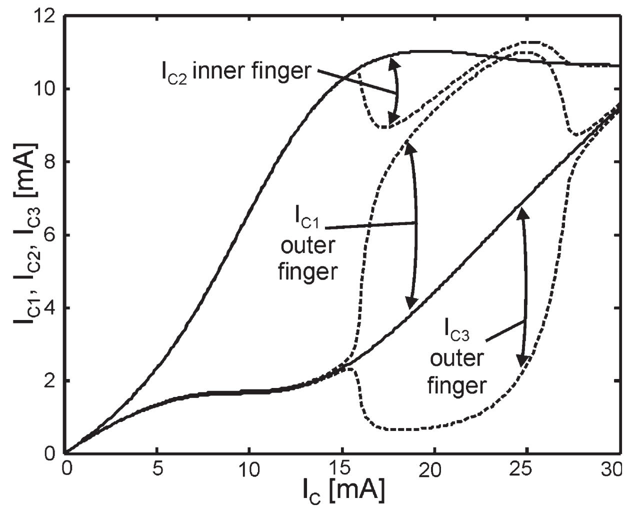

Fig. 11. SPICE-simulated electrothermal behavior of a three-finger device; the case of ideally identical fingers (solid lines) is compared to the "unbalanced" outer fingers case (dashed lines).

be negative and φ_{BE} will still decrease as I_C increases. For example, in SiGe transistors with uniform Ge percentage in the base (%Ge), the base bandgap is reduced by $7.4 \times$ %Ge meV [37]. This reduction is included in E_{GB} from (5) and can result in a negative φ_β.

The potential thermal robustness of single-finger SiGe devices is investigated here by varying the %Ge. For the sake of simplicity, devices with uniform %Ge in the base are considered, and the functional dependence of φ_β with I_C is neglected, i.e., $I_H \rightarrow \infty$. To allow a manageable basis for comparison, the emitter–base profiles are tailored to give a $\beta_0 = 120$ for all %Ge. A higher %Ge will increase the collector current at ambient temperature. This means that other device parameters must be modified to meet the request for constant β_0. Two device categories are studied: type 1, in which the base doping is increased, and type 2, in which the emitter depth is reduced for higher %Ge [38]. The calculated $I_{C,\mathrm{crit}}$ is plotted in Fig. 10 as a function of %Ge. It is noteworthy that increasing %Ge leads to better thermal stability of the type-1 devices; in this case, all transistors have identical emitters, and thus identical coefficients φ_{BE}. On the other hand, for the type-2 transistors, electrothermal stability is not improved; shallower emitter depths yield higher I_{B0}, which means higher φ_{BE} for the same I_C. This implies that the benefits of reducing φ_β are counteracted and, from the electrothermal point of view, the type-2 transistors only marginally take advantage of the higher %Ge.

C. Generalization of SPICE Macromodel—Three-Finger Devices

As mentioned in Section III, the SPICE macromodel can be generalized to simulate the behavior of circuits and multifinger transistors with a large number of elementary devices. As an example, the case of a three-finger silicon-on-glass BJT is presented here. The investigated device is symmetrical around the inner finger with index "2." The physical model parameters from Table I are assigned to each finger, and R_{TH} and R_M values are typical for silicon-on-glass transistors [7], [11], [39]: $R_{\mathrm{TH}} = 10\,500$ K/W, $R_{\mathrm{TH12}} = R_{\mathrm{TH23}} = 5000$ K/W, $R_{\mathrm{TH13}} = 2000$ K/W. The total emitter current is controlled while the collector–base voltage is fixed at $V_{\mathrm{CBX}} = 0.75$ V. The collector currents versus the total collector current I_C are shown in Fig. 11. Solid lines refer to the case of identical fingers. Due to the inherent difference in thermal coupling between inner and outer fingers, an uneven current distribution arises at low/medium I_C levels: the innermost finger starts conducting more and more current due to the strong thermal coupling with both neighboring devices, which each handle the same amount of current due to the perfect system symmetry. Nevertheless, at high-current levels, the system approaches a stable situation because the central finger enters the region of negative feedback. A more complex behavior is observed when a slight discrepancy exists between the parameters of the two outer fingers. Such behavior for $\Delta r_E = 0.1\ \Omega$ is illustrated by the dashed lines. As can be seen, when $I_C = 15$ mA, the applied unbalancing condition gives rise to a current bifurcation between these fingers. Due to the higher positive temperature coefficient of the collector current, the outer finger 1 draws more current at the expense of both the inner and the other outer finger. However, for current values larger than $I_C = 27$ mA, the effect of the introduced Δr_E becomes insignificant due to the compounded restabilization mechanisms.

VI. Conclusion

It has been demonstrated that the analytical formulation developed in Section II provides a fast and reliable means of determining the boundary between stable and unstable regions for single- and two-finger bipolar transistor configurations operating at medium and high currents. Moreover, the formulation accounts for and gives new insight into both individual and combined mechanisms that are relevant for the onset of instability and restabilization. Impact ionization effects that lead to electrical breakdown and enhance electrothermal breakdown have not been included in this study; on the contrary, the focus has been on the effects that can reduce the electrothermal feedback and lead to restabilization of the transistor after the onset of thermal instability: the decrease of the temperature coefficients of base–emitter voltage and current gain with increasing current, and the factors that attenuate the actual collector current at high-enough currents, i.e., high-injection effects and ballasting/series resistances. Predictions could therefore be made for which combination of effects would lead to more stable Si- and SiGe-base transistors.

For a simulation of the complete multifinger-transistor/circuit characteristics, a novel ABM-based SPICE macromodel for bipolar devices was developed to include the same set of electrothermal mechanisms as the analytical model. It was built for direct application in the electrothermal circuit simulator SPICE. Its effectiveness in simulating more complex structures was demonstrated for the case of a multifinger transistor.

References

[1] W. Liu, S. Nelson, D. G. Hill, and A. Khatibzadeh, "Current gain collapse in microwave multifinger heterojunction bipolar transistors operated at very high power densities," *IEEE Trans. Electron Devices*, vol. 40, no. 11, pp. 1917–1927, Nov. 1993.

[2] L. L. Liou, B. Bayraktaroglu, and C. I. Huang, "Theoretical thermal runaway analysis of heterojunction bipolar transistors: Junction temperature rise threshold," *Solid State Electron.*, vol. 39, no. 1, pp. 165–172, Jan. 1996.

[3] W. Zhou, S. Sheu, J. J. Liou, and C. I. Huang, "A multi-emitter finger AlGaAs/GaAs HBT model including the effects of two-dimensional temperature distribution on emitter fingers," *Solid State Electron.*, vol. 42, no. 5, pp. 693–698, May 1998.

[4] T. Grasser and S. Selberherr, "Fully coupled electrothermal mixed-mode device simulation of SiGe HBT circuits," *IEEE Trans. Electron Devices*, vol. 48, no. 7, pp. 1421–1427, Jul. 2001.

[5] D. J. Walkey, D. Celo, T. J. Smy, and R. K. Surridge, "A thermal design methodology for multifinger bipolar transistor structures," *IEEE Trans. Electron Devices*, vol. 49, no. 8, pp. 1375–1383, Aug. 2002.

[6] N. Nenadović, L. K. Nanver, and J. W. Slotboom, "Electrothermal limitations on the current density of high-frequency bipolar transistors," *IEEE Trans. Electron Devices*, vol. 51, no. 12, pp. 2175–2180, Dec. 2004.

[7] N. Nenadović, V. d'Alessandro, L. K. Nanver, F. Tamigi, N. Rinaldi, and J. W. Slotboom, "A back-wafer contacted silicon-on-glass integrated bipolar process—Part II: A novel analysis of thermal breakdown," *IEEE Trans. Electron Devices*, vol. 51, no. 1, pp. 51–62, Jan. 2004.

[8] N. Nenadović, V. d'Alessandro, F. Tamigi, A. Rossi, A. Griffo, L. K. Nanver, and J. W. Slotboom, "Thermal instability in two-finger bipolar transistors," in *Proc. IEEE ESSDERC*, 2003, pp. 203–206.

[9] N. Rinaldi and V. d'Alessandro, "Theory of electrothermal behavior of bipolar transistors: Part I—Single-finger devices," *IEEE Trans. Electron Devices*, vol. 52, no. 9, pp. 2009–2021, Sep. 2005.

[10] ——, "Theory of electrothermal behavior of bipolar transistors: Part II—Two-finger devices," *IEEE Trans. Electron Devices*, vol. 52, no. 9, pp. 2022–2033, Sep. 2005.

[11] L. K. Nanver, N. Nenadović, V. d'Alessandro, H. Schellevis, H. W. van Zeijl, R. Dekker, D. B. de Mooij, V. Zieren, and J. W. Slotboom, "A back-wafer contacted silicon-on-glass integrated bipolar process—Part I: The conflict electrical versus thermal isolation," *IEEE Trans. Electron Devices*, vol. 51, no. 1, pp. 42–50, Jan. 2004.

[12] C. Popescu, "Selfheating and thermal runaway phenomena in semiconductor devices," *Solid State Electron.*, vol. 13, no. 4, pp. 441–450, Apr. 1970.

[13] D. Buhanan, "Investigation on current-gain temperature dependence in silicon transistors," *IEEE Trans. Electron Devices*, vol. ED-16, no. 1, pp. 117–124, Jan. 1969.

[14] J. W. Slotboom and H. C. de Graaff, "Bandgap narrowing in silicon bipolar transistors," *IEEE Trans. Electron Devices*, vol. ED-24, no. 8, pp. 1123–1125, Aug. 1977.

[15] W. Liu, S.-K. Fan, -T. Henderson, and D. Davito, "Temperature dependences of current gains in GaInP/GaAs and AlGaAs/GaAs heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 40, no. 7, pp. 1351–1353, Jul. 1993.

[16] G. H. R. Krishna, A. K. Aditya, N. B. Chakrabarti, and S. Banerjee, "Analysis of temperature dependence of Si-Ge HBT," in *Proc. VLSI Design Conf.*, 1995, pp. 268–271.

[17] Z. Deshu, X. Chen, C. Jianxin, S. Chen, D. Jinyu, D. Jun, Z. Li, and S. Guangdi, "SiGe/Si HBTs with current gain of negative temperature dependence," in *Proc. IEEE Solid-State Integ.-Circuit Tech. Conf.*, 2001, pp. 607–609.

[18] S. M. Sze, *Physics of Semiconductor Devices*. New York: Wiley, 1981.

[19] R. H. Winkler, "Thermal properties of high-power transistors," *IEEE Trans. Electron Devices*, vol. ED-14, no. 5, pp. 260–263, May 1967.

[20] W. Liu, "Thermal coupling in 2-finger heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 42, no. 6, pp. 1033–1038, Jun. 1995.

[21] K. Lu and C. M. Snowden, "Analysis of thermal instability in multi-finger power AlGaAs/GaAs HBT's," *IEEE Trans. Electron Devices*, vol. 43, no. 11, pp. 1799–1805, Nov. 1996.

[22] E. Schurack, T. Latzel, W. Rupp, and A. Gottwald, "Nonlinear effects in transistors caused by thermal power feedback: Simulations and modeling in SPICE," in *Proc. IEEE ISCAS*, 1992, vol. 2, pp. 879–882.

[23] D. T. Zweidinger, S.-G. Lee, and R. M. Fox, "Compact modeling of BJT self-heating in SPICE," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 12, no. 9, pp. 1368–1375, Sep. 1993.

[24] *PSPICE 9.1 by ORCAD, User's Manual*, Cadence Design Systems, San Jose, CA, 1998.

[25] A. Maxim, D. Andreu, and J. Boucher, "High performance power MOSFET SPICE macromodel," in *Proc. IEEE ISIE*, 1997, pp. 189–194.

[26] A. Maxim and G. Maxim, "Electrothermal SPICE macromodeling of the power bipolar transistor including the avalanche and secondary breakdowns," in *Proc. IEEE IECON*, 1998, pp. 348–352.

[27] C. C. McAndrew, "A complete and consistent electrical/thermal HBT model," in *Proc. IEEE BCTM*, 1992, pp. 200–203.

[28] J. C. J. Paasschens, W. J. Kloosterman, and R. van der Toorn, "Mextram (level 504). The Philips model for bipolar transistors," presented at the FSA Modeling Workshop, Santa Clara, CA, 2002. [Online]. Available: http://www.semiconductors.philips.com/Philips_Models/bipolar/mextram

[29] *Advanced Design System (ADS) User's Manual*, Agilent, Palo Alto, CA, 2004.

[30] F. M. De Paola, V. d'Alessandro, G. Breglio, N. Rinaldi, and P. Spirito, "Enhancing commercial CAD tools toward the electrothermal simulation of power transistors," *Proc. IEEE Int. Symp. Power Semiconductor Devices*, to be published.

[31] M. Macchiaroli, N. Rinaldi, V. d'Alessandro, G. Breglio, and P. Spirito, "A new electrothermal simulation tool for the analysis of bipolar devices and circuits," in *Proc. Thermal Investigations ICs and Systems (THERMINIC) Workshop*, 2001, pp. 281–286.

[32] V. d'Alessandro, N. Nenadović, F. Tamigi, N. Rinaldi, L. K. Nanver, and J. W. Slotboom, "A novel SPICE macromodel of BJTs including the temperature dependence of high-injection effects," in *Proc. IEEE MIEL*, 2004, pp. 253–256.

[33] N. Nenadović, S. Mijalković, L. K. Nanver, L. J. K. Vandamme, V. d'Alessandro, H. Schellevis, and J. W. Slotboom, "Extraction and modeling of selfheating and mutual thermal coupling impedance of bipolar transistors," *IEEE J. Solid-State Circuits*, vol. 39, no. 10, pp. 1764–1772, Oct. 2004.

[34] M. G. Adlerstein, "Thermal stability of emitter ballasted HBT's," *IEEE Trans. Electron Devices*, vol. 45, no. 8, pp. 1653–1655, Aug. 1998.

[35] B. Bayraktaroglu, R. Fitch, J. Barrette, R. Scherer, L. Kehias, and C. I. Huang, "Design and fabrication of thermally-stable AlGaAs/GaAs microwave power HBTs," in *Proc. IEEE Cornell Conf. Adv. Concepts High Speed Semicond. Dev. Circuits*, 1993, pp. 83–92.

[36] L. L. Liou, D. Barlage, J. Barrette, C. Bozada, R. Dettmer, T. Jenkins, R. Lee, M. Mack, and J. Sewell, "Thermal analysis and characterization of thermally shunted AlGaAs/GaAs heterojunction bipolar transistors," in *Proc. IEEE Cornell Conf. Adv. Concepts High Speed Semicond. Dev. Circuits*, 1995, pp. 563–572.

[37] R. J. E. Hueting, J. W. Slotboom, A. Pruijmboom, W. B. de Boer, C. E. Timmering, and N. E. B. Cowern, "On the optimization of SiGe-base bipolar transistors," *IEEE Trans. Electron Devices*, vol. 43, no. 9, pp. 1518–1524, Sep. 1996.

[38] L. C. M. van den Oever, L. K. Nanver, and J. W. Slotboom, "Comparing the high-frequency performance of box-Ge and graded-Ge SiGe HBT's," in *Proc. STW/SAFE*, 2000, pp. 119–123.

[39] W. D. van Noort and R. Dekker, "Thermal resistance of (H)BT on bulk Si, SOI and glass," in *Proc. IEEE BCTM*, 2003, pp. 129–132.

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