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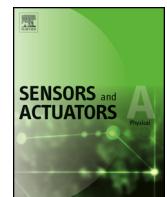
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Design of a temperature sensor with optimized noise-power performance

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ABSTRACT

This paper presents the design aspect of a BJT-based temperature sensor implemented in standard CMOS technology that is optimized for its noise-power performance. The interface electronics of the sensor consists of a continuous-time duty-cycle modulator, where a capacitor is periodically charged and discharged, with two temperature-dependent current sources, between two thresholds determined by a Schmitt trigger. In order to optimize the noise properties of the sensor, the major noise sources have been analyzed and optimized using target specifications of the manufacturer. Experimental results are in agreement with those of simulations and analytical calculations. The sensor has been implemented in 0.7 μm CMOS technology. At 3.3V supply, the measured temperature resolution amounts to 3mK for a measurement time of 1.8ms. The test results show that a Resolution Figure of Merit (RFoM) of 3.2pJ/K² has been achieved in this design, which is the best reported result for BJT-based temperature sensors in the market.

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1. Introduction

FOR battery-operated systems, energy efficiency is an important issue. This holds also true for temperature sensors applied in such systems. Moreover, for temperature sensors, minimization of energy consumption is also important to reduce self-heating. But decreasing power will lead to increasing noise and therefore deteriorating the temperature resolution (minimum detectable signal) [1]. This means that there is a trade-off between the noise performance and the power consumption. In this paper the noise performance has been analyzed, and the power-versus-noise behavior has been optimized, while taking into account target specifications of the sensor manufacturer, regarding temperature range (-45°C to 130°C), supply voltage (2.7 V to 5.5 V) and applied technology (CMOS). For sensing element in CMOS technology, resistors, CMOS transistors [2], or bipolar junction transistors (BJTs) can be used. Because of their favorable properties regarding precision, calibration and trimming, substrate (PNP) bipolar transistors

(BJTs) have been selected as temperature-sensing elements [3,4]. An additional important feature of using BJTs is that with the same transistors also (bandgap) reference voltages and currents can be generated, which enables to perform ratio metric measurements [4].

Noise minimization of the temperature sensor is important for two reasons:

- 1) To optimize the sensor's resolution,
- 2) For a given required resolution a better noise performance will allow shortening of the measurement time. In this way, the energy consumption per measurement can be reduced.

The latter point is applied, for instance, in autonomous sensor system, where after one measurement, the system goes into a power-down mode and when needed to the power-up mode again [5]. The ability to achieve a certain resolution while minimizing energy consumption, the system performance can be characterized with its Resolution Figure of Merit (RFoM) [6]. In [7] the basic principles of the sensor have been presented, together with an analysis of the systematic errors and experimental results. In this paper, the noise behavior will be analyzed together with a discussion of design

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constraints and opportunities regarding to noise/resolution of the sensor.

Firstly, a short summary of the main concepts of the temperature sensor is presented. Next, the approach for the noise analysis is discussed. Finally, the analytical results are compared with those of simulations and experiments.

2. Sensor architecture

The operating principles of the sensor [3] are as illustrated in Fig. 1(a) and (b). Under the control of a Schmitt trigger (ST), a capacitor C is alternately charged by a constant current I_1 and discharged by another constant current I_2 . In that case, for the duty-cycle D of the resulting oscillation (Fig. 1(b)) it is found that:

$$D = \frac{T_H}{T_H + T_L} = \frac{I_1}{I_1 + I_2}. \quad (1)$$

The currents I_1 and I_2 are temperature dependent, and are composed of a scaled component I_{PTAT} which is Proportional-To-Absolute-Temperature ϑ_K ¹(PTAT) and a scaled component I_{CTAT} , which is Complementary proportional-To-Absolute-Temperature [1,2]. In this paper, we assume that temperature changes are so slow, that during the time intervals T_H and T_L the currents I_1 and I_2 can be considered as being quasi-stationary. The current I_{CTAT} is derived from the base-emitter voltage V_{BE} of a substrate PNP transistor, while I_{PTAT} is derived from the difference ΔV_{BE} between the base-emitter voltages of two PNP transistors, with different biasing [8].

The scaling factors have been chosen in such a way that the duty cycle D changes linearly over the desired temperature range of -45°C to 130°C , and has been optimized for maximum sensitivity. This is achieved by selecting

$$I_1 = 3I_{\text{PTAT}} - 0.5I_{\text{CTAT}}, \quad (2)$$

$$I_2 = I_{\text{CTAT}} - I_{\text{PTAT}}, \quad (3)$$

$$I_1 + I_2 = I_{\text{ref}}, \quad (4)$$

where, the sum I_{ref} of the currents I_1 and I_2 is temperature independent. Fig. 1(c) shows the temperature dependency of the three currents I_1 , I_2 and I_{ref} . The symbol ϑ_C denotes the temperature in $^\circ\text{C}$, while ϑ_A is the same temperature in Kelvin.

Fig. 2 shows a simplified block diagram of the actual sensor [7]. Substrate PNPs Q_1 and Q_2 are biased at a 1:9 current-density ratio, and an op-amp (OP_1) forces the resulting voltage $\Delta V_{\text{BE}} = V_{\text{BE}1} - V_{\text{BE}2} = (k\vartheta_A/q) \ln 9$ across resistor R_{PTAT} , to generate a PTAT current $I_{\text{PTAT}} = \Delta V_{\text{BE}}/R_{\text{PTAT}}$.

Similarly, OP_2 and another resistor R_{BE} (with closed switch Sw_2) convert the base-emitter voltage $V_{\text{BE}3}$ of Q_3 into a CTAT current $I_{\text{CTAT}} = V_{\text{BE}3}/R_{\text{BE}}$. These currents are then linearly combined so that the capacitor C is charged by a current $3I_{\text{PTAT}} - 0.5I_{\text{CTAT}}$ (Sw_1 closed and Sw_2 open) and is discharged by a current $I_{\text{CTAT}} - I_{\text{PTAT}}$ (Sw_1 open and Sw_2 closed). To achieve a high accuracy over a wide supply-voltage range, all the associated current mirrors/sources are cascaded. As in [3], the sum of the charge and discharge currents, i.e. $2I_{\text{PTAT}} + 0.5I_{\text{CTAT}}$, is designed to have a slightly positive temperature coefficient (not shown in Fig. 1(c)), which effectively compensates the curvature of $V_{\text{BE}3}$. As shown in Fig. 1, this scheme ensures that D now varies from about 10% to 90% over the desired temperature range [3]. To make the sensor compatible with previous products

¹ In this paper the symbols T and t are used for time intervals and time, respectively. Therefore, for temperature the symbol ϑ is used instead of a more standard symbol. The symbols ϑ_K and ϑ_C denote the temperatures in Kelvin and degrees Celsius, respectively.

[17], the range has been fine-tuned in such a way that duty cycle D changes with the temperature ϑ_C according to the equation:

$$D = 0.0047\vartheta_C + 0.32. \quad (5)$$

An additional target specification is related to the output frequency, which depends on resistor and capacitance values. The value of this frequency doesn't contain relevant signal information and is not important for the sensor accuracy. However, for practical reasons, the frequency should neither be too low, because this would slow down the maximum measurement speed, nor it should be too high, because this would yield more quantization noise (see Section 4). As a compromise, the frequency has been chosen to be between 1 kHz and 4 kHz. This determines the design of current sources I_{PTAT} and I_{CTAT} , as well as the capacitance of C. I_{PTAT} has been chosen to be about 1 μA at room temperature, and the capacitance of C to be 150 pF. With the mentioned target specs, still some design freedom was available to select smaller currents and thus smaller capacitance, which would save energy consumption and chip area. However, then the error due to leakage at high temperatures would be larger too. Therefore, the mentioned selection of current and capacitor values is considered as being adequate.

The Schmitt trigger has been designed in such a way that the swing range at the input is within the maximum acceptable value for the desired ranges of the supply voltage and the temperature. Such a design not only makes the voltage jitter at its input negligible with respect to the total circuit noise, but also helps to reduce the value of capacitance C, for given current and period requirements.

In order to minimize the systematic errors caused by component mismatching, circuit techniques such as chopping and dynamic element matching (DEM) have been applied [7,9]. A complete DEM cycle consists of eight output periods. Accurate results are obtained by taking the averaged result of the duty cycles over a full DEM cycle of eight sequential periods [7].

3. Noise analysis of the interface

From Fig. 1(a) it might be expected that the jitter of the output signal on the one hand is caused by the noisy currents I_1 and I_2 and on the other hand by the input-referred voltage noise of the Schmitt trigger. However, it can be shown that thanks to the large voltage swing at the input of the Schmitt trigger and applying common ways of interference reduction, the jitter caused by the Schmitt trigger can be neglected. Moreover, as shown in [10], for both types of noise sources, the duty cycle is immune to disturbing signals with frequencies higher than that of the relaxation oscillator. Therefore, in this paper, the noise analysis mainly refers to the effects of the low-frequency-part of the noise in the currents I_1 and I_2 .

In Section 3.1, firstly it will be shown how to calculate the jitter of the output signal (Fig. 1(b)) as caused by low-frequency noise components of these currents. Next, the noise-power spectral density of I_1 and I_2 is analyzed. Finally, it is shown how to convert the jitter to temperature readout resolution.

The calculation of the noise power spectral densities of I_1 and I_2 can be performed in various ways. It will be shown that with some circuit simplifications, this calculation can be performed with Cadence software, which provides an easy way to include many higher-order effects too. However, in order to identify the main noise sources of the circuit and to understand their contributions to I_1 and I_2 , we will firstly use analytical calculations to find the white-noise levels of I_1 and I_2 . These analytical results are used to optimize the Op-Amps designs regarding their noise property in relation to their energy consumption. Next, it will be shown that the results of this analysis are in good agreement of those the Cadence simulations in which also the effects of 1/f noise are included. As

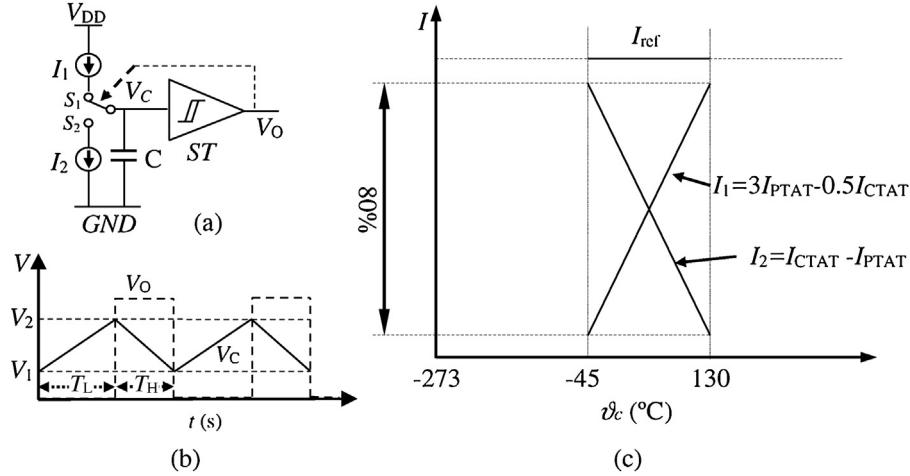


Fig. 1. Operating principle of the relaxation oscillator with duty-cycle modulated output: a) basic circuit diagram; b) input voltage V_c and output voltage V_0 of the Schmitt trigger versus time t ; c) the basic currents versus temperature ϑ_c (in °C).

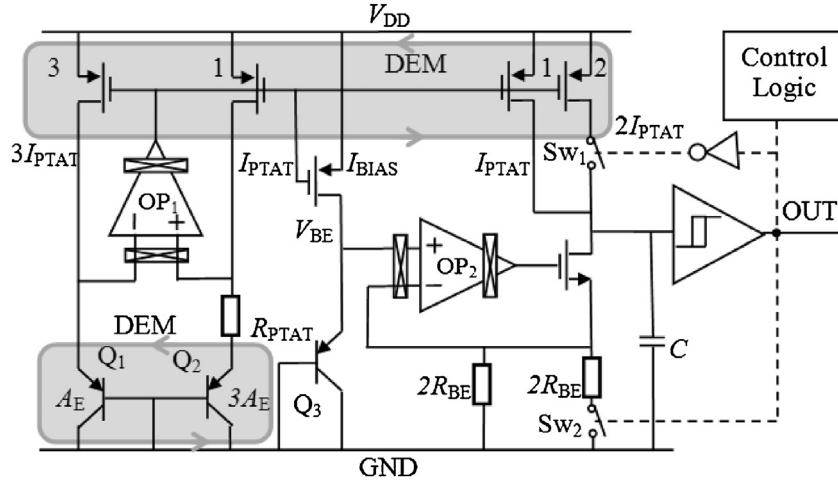


Fig. 2. Simplified sensor block diagram.

will be shown, the effect of $1/f$ noise is negligible, thanks to the applied chopper.

3.1. Calculation of noise in different domains

In this section, the noise in the temperature readout caused by noise of I_1 and I_2 will be calculated. For our analysis we simply start with the noise within one period.

Suppose that a capacitor is discharged or charged with a noisy current $I_{\text{nom}} + i_n(t)$, where I_{nom} is the nominal, noise-free current and $i_n(t)$ is the noise component [11]. Then, the voltage $V_C(t)$ over capacitor C (Fig. 3) amounts to:

$$v_c(t) = v_{\text{nom}}(t) + v_n(t) \quad (6)$$

where $v_{\text{nom}}(t)$ is the nominal voltage (the solid line with slope $\tan\phi$ in Fig. 3) and $v_n(t)$ is the noise component of the capacitor voltage, which equals:

$$v_n(t) = \frac{1}{C} \int_{t_1}^t i_n(t) dt. \quad (7)$$

For the moment t_{cr} , which is the time that the capacitor voltage crosses the threshold voltage V_{th} of the Schmitt trigger, the extrapolated noise voltage is converted in time jitter Δt_{cr} with respect to

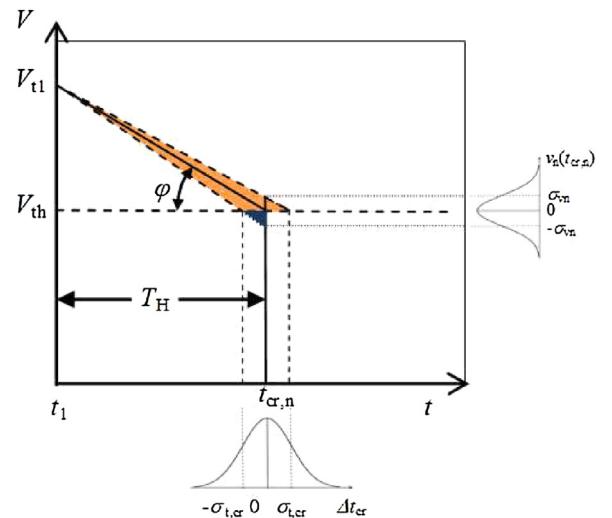


Fig. 3. Conversion of voltage noise at the input of the Schmitt trigger to the jitter of time interval.

the nominal crossing moment $t_{\text{cr},n}$. By good approximation it holds that [12]:

$$\Delta t_{\text{cr}} = \frac{v_n(t_{\text{cr}})}{\tan \varphi} \approx v_n(t_{\text{cr}}) \frac{C}{I_{\text{nom}}}. \quad (8)$$

For the standard deviation $\sigma_{t,\text{cr}}$ of Δt_{cr} it holds by good approximation that:

$$\sigma_{t,\text{cr}} = \frac{\sigma_{vn}(t_{\text{cr}})}{\tan \varphi} \approx \sigma_{vn}(t_{\text{cr}}) \frac{C}{I_{\text{nom}}}. \quad (9)$$

Additionally the high-frequency voltage noise ($f > 1/T_H$) at the input of Schmitt trigger will always cause a crossing moment earlier than the nominal value [13]. However, as we will show later in Eq. (14), high frequency noise will be filtered by integration and therefore Eq. (8) is valid for our analysis.

Using Eq. (1), and supposing that noise of T_H is not correlated with that of T_L , the standard deviation of the duty cycle σ_D can be calculated as:

$$\sigma_D = \sqrt{\left(\frac{T_H}{(T_H + T_L)^2} \right)^2 \sigma_{T,L}^2 + \left(\frac{T_L}{(T_H + T_L)^2} \right)^2 \sigma_{T,H}^2}, \quad (10)$$

where, $\sigma_{T,L}$ and $\sigma_{T,H}$ represent the standard deviation of time intervals T_L and T_H , respectively.

Using Eq. (5), for the corresponding standard deviation σ_ϑ in the temperature readout it is found that:

$$\sigma_\vartheta = \frac{\sigma_D}{0.0047}. \quad (11)$$

From the spectral density of the current noise, the jitter in frequency domain can be derived. First consider a single harmonic component of the current noise:

$$i_n(t) = I_n(f) \cos(2\pi f t), \quad (12)$$

where, $I_n(f)$ is the amplitude of this harmonic component.

Combining Eqs. (7), (8) and (12), the standard deviation $\sigma_T(f)$ of the jitter caused by this harmonic, is found to be:

$$\sigma_T(f) = \frac{T}{I} I_n(f) \operatorname{sinc}(2\pi f T). \quad (13)$$

where, T is integration time which equals to T_H or T_L . Similarly, in case of a continuous noise spectrum with current-noise power spectral density $S_{in}(f)$, the total jitter caused by all noise harmonics will be:

$$\sigma_T = \frac{T}{I} \sqrt{\int_0^\infty S_{in}(f) \operatorname{sinc}^2(2\pi f T) df}. \quad (14)$$

Eq. (14) shows the well-known fact that integrating a noisy current in the time domain corresponds to filtering its power spectral density with a sinc-function in the frequency domain [14].

To finalize the noise analysis the noise-power spectral density of the charge and the discharge currents is calculated. Using Eqs. (2) and (3), the noise power spectral densities S_1 and S_2 of the currents I_1 and I_2 can be calculated as:

$$S_1 = 0.25 S_{\text{CTAT}} + 9 S_{\text{PTAT}}, \quad (15)$$

$$S_2 = S_{\text{CTAT}} + S_{\text{PTAT}}, \quad (16)$$

where, S_{PTAT} and S_{CTAT} are the noise-power spectral densities of the currents I_{PTAT} and I_{CTAT} , respectively. In Eqs. (15) and (16) we suppose that the noise of I_{CTAT} and I_{PTAT} are uncorrelated. It could be argued, that the biasing current of Q_3 , which is used to generate the CTAT current, is a PTAT current (Fig. 2) and that therefore the noise of I_{CTAT} is partly correlated to noise of I_{PTAT} . However as will be shown in Section 3.3, this correlated part is insignificant.

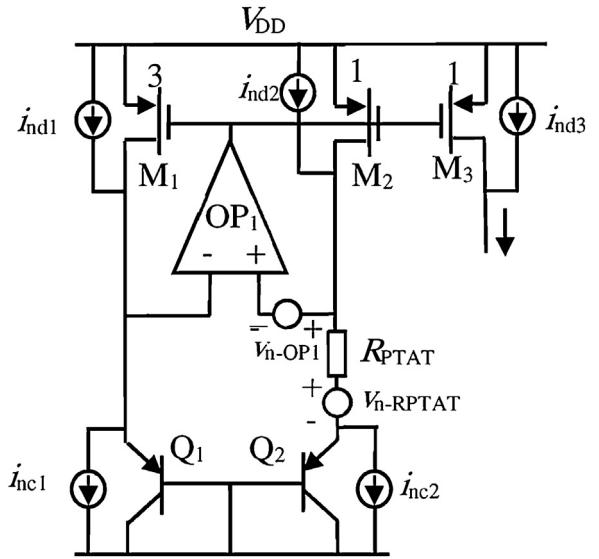


Fig. 4. PTAT current generator with different noise sources.

Once S_1 and S_2 are known, we can calculate $\sigma_{T,L}$ and $\sigma_{T,H}$ using Eq. (14), and finally, from Eqs. (9) and (11) the standard deviations in duty cycle (σ_D) and temperature (σ_ϑ) can be derived.

The current-noise power spectral densities S_1 and S_2 can directly be found by simulation with, for instance, Cadence software. This is performed as discussed in Section 3.4 and has been used in our further calculations. Yet, for better insight in the different sources of noise and also to facilitate proper power budgeting of the sensor design, in the following we will present the details of the calculation of S_{PTAT} and S_{CTAT} and the resulting values of S_1 and S_2 .

3.2. Noise sources of the PTAT current

Fig. 4 shows a simplified circuit for the PTAT current generator [8] including the major noise sources, which are indicated as external sources. In order to simplify the calculation of the white-noise, which is mainly due to thermal noise of resistors and MOS transistors and shot noise of the bipolar transistors, we removed the chopper of OP_1 since it has no effect on thermal noise. On the other hand, the chopper has effect for the influence of 1/f noise. This will be discussed in Section 3.5. The noise contribution of each of these sources on the PTAT current I_{PTAT} can be calculated separately. Afterwards, the total noise is found by adding the different noise-power contributions.

As an example, Fig. 5 shows the PTAT current generator with the noise source i_{nc2} (shot noise) of bipolar transistor Q_2 and its effect i_{nc21} , i_{nc11} in the various branches.

As mentioned before, the CMOS transistors M_1 and M_2 have been scaled, so that $I_{D1} = 3I_{D2}$. When neglecting the effects of base currents, for the collector currents of the bipolar transistors it holds $I_{C1} = 3I_{C2}$ and therefore $g_{m,Q1} = 3g_{m,Q2}$. Also the bipolar transistors Q_1 and Q_2 have been scaled, so that for their corresponding emitter areas A_E it holds that $A_{E2} = 3A_{E1}$. For the input differential voltage V_i of op-amp OP_1 it holds that $V_i = V_{BE2} + I_{C2}R_{\text{PTAT}} - V_{BE1}$. Due to the applied negative feedback, this voltage equals virtually zero, so that:

$$I_{C2} = I_{\text{PTAT}} = \frac{k\vartheta_A}{qR_{\text{PTAT}}} \ln 9, \quad (17)$$

Where, ϑ_A represents the absolute temperature. For the transconductance $g_{m,Q2}$ of bipolar transistor Q_2 it holds that:

$$g_{m,Q2} = \frac{qI_{C2}}{k\vartheta_A}. \quad (18)$$

Table 1

White-noise sources and their contributions to I_{PTAT} .

Noise source	Noise spectral density in I_{PTAT}	
	Contribution to I_{PTAT}	Value (in A^2/Hz)
Resistor R_{PTAT}	$\frac{4k\vartheta_A}{R_{\text{PTAT}}}$	3.3×10^{-25}
Current mirror, mainly M_2 and M_3	$\frac{25}{3}k\vartheta_A g_{m,M2}$	3.8×10^{-25}
BJT pair, mainly Q_2	$1.2 \frac{k\vartheta_A}{R_{\text{PTAT}}}$	1.0×10^{-25}
Equivalent input noise voltage of OP_1	$\frac{S_{vn,\text{OP1}}}{R_{\text{PTAT}}^2}$	4.0×10^{-25}

current is negligible. The noise of M_3 is outside the feedback loop. Therefore, its noise contribution on PTAT current, $S_{\text{ind}3}$, is simply:

$$S_{\text{ind}3} \cong \frac{8}{3} k\vartheta_A g_{m,M3}. \quad (36)$$

Moreover $g_{m,M2}=g_{m,M3}$, and therefore the total noise contribution of MOS transistors M_1 , M_2 and M_3 on the PTAT current amounts to:

$$S_{\text{in-MOS}} \cong \frac{25}{3} k\vartheta_A g_{m,M2}. \quad (37)$$

The total spectral density of the noise of the PTAT current can be calculated by adding the results of Eqs. (28)–(30) and (37), which yields:

$$S_{\text{PTAT}} = 4 \frac{k\vartheta_A}{R_{\text{PTAT}}} + 1.2 \frac{k\vartheta_A}{R_{\text{PTAT}}} + \frac{S_{vn,\text{OP1}}}{R_{\text{PTAT}}^2} + \frac{25}{3} k\vartheta_A g_{m,M2}. \quad (38)$$

Summarizing, the main white-noise sources and their contributions to the PTAT current are as listed in Table 1.

As mentioned before, to set the frequency range, I_{PTAT} is set to about $1 \mu\text{A}$ at room temperature. This can be achieved by selecting $R_{\text{PTAT}}=50\text{k}\Omega$. Therefore, noise generated by the PTAT resistor and the BJT core (the first and the third term in Table 1) equal $3.3 \times 10^{-25} \text{ A}^2/\text{Hz}$ and $1.0 \times 10^{-25} \text{ A}^2/\text{Hz}$, respectively ($g_{m,Q2}=45\mu\text{S}$). Although $g_{m,M2}$ depends on the current and the W/L ratio, for better matching we have selected its size for operation in strong inversion with $g_{m,M2}=10\mu\text{S}$. As a result, the noise spectral density of current mirror (the second term in Table 1) amounts to $3.8 \times 10^{-25} \text{ A}^2/\text{Hz}$.

Op-amp OP_1 has been configured as a folded-cascode OTA. To minimize the input-referred noise of OP_1 for a given supply current, the size of the input transistors has been chosen to be large enough for operation in weak inversion. In this way, the maximum transconductance can be achieved [15,16]. Moreover, to minimize the noise contribution of other transistors of OP_1 , the size of these transistors has been chosen to be small enough for operation in strong inversion, with about 0.2 V overdrive voltage [15]. Next, an important design issue is to optimize op-amp OP_1 regarding its power consumption in relation to its input-referred noise. For folded-cascode op-amps, the noise contribution of the op-amp decreases with about the square root of the supply current. As a compromise between energy consumption and noise, the supply current of op-amp OP_1 has been chosen so that the noise contribution of OP_1 is in the same range as other major terms in Table 1. For this op-amp it holds that $\sqrt{S_{vn,\text{OP1}}} = 32\text{nV}/\sqrt{\text{Hz}}$, which yields a noise contribution in PTAT current of $4.0 \times 10^{-25} \text{ A}^2/\text{Hz}$.

This yields a total white-noise contribution of $S_{\text{PTAT}} = 1.21 \times 10^{-24} \text{ A}^2/\text{Hz}$, which corresponds to a current noise of $1.1 \text{ pA}/\sqrt{\text{Hz}}$ in I_{PTAT} .

3.3. Noise sources of the CTAT current

Fig. 7 shows the simplified circuit of the CTAT current generator including six noise sources. Similar to what was discussed in the previous subsection, the chopper for OP_2 has been removed, because this simplifies the calculation of the white-noise, while

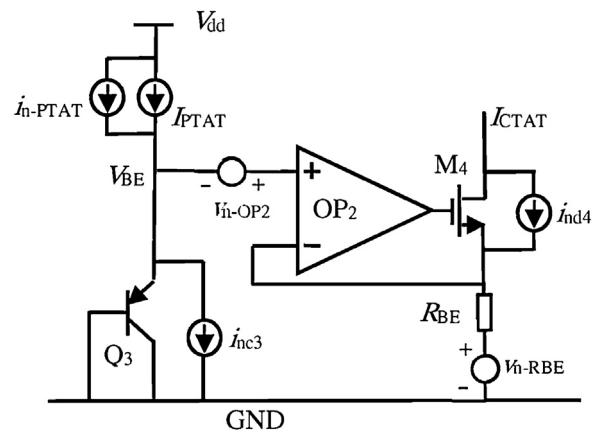


Fig. 7. The CTAT current generator.

Table 2

White-noise sources and their contribution to I_{CTAT} .

Noise source	Noise spectral density	
	Contribution to I_{CTAT}	Value (in A^2/Hz)
Resistor R_{BE}	$\frac{4k\vartheta_A}{R_{\text{BE}}}$	1.1×10^{-25}
Equivalent input noise voltage of OP_2	$\frac{S_{vn,\text{OP2}}}{R_{\text{BE}}^2}$	1.25×10^{-25}

removing the chopper doesn't influence the effect of white noise. On the other hand, the chopper has effect for the influence of $1/f$ noise. This will be discussed in Section 3.5.

In this subsection, it is shown that the main noise sources that contribute to the white noise in the CTAT current are the noise voltage $v_{n-\text{RBE}}$ of resistor R_{BE} and the input-referred noise voltage $v_{n-\text{OP2}}$ of amplifier OP_2 (Fig. 7). For these two sources, straightforward calculations show that their contribution to the total white-noise spectral density S_{CTAT} in CTAT current amounts to:

$$S_{\text{CTAT}} = \frac{4k\vartheta_A}{R_{\text{BE}}} + \frac{S_{vn,\text{OP2}}}{R_{\text{BE}}^2}. \quad (39)$$

The main white-noise sources are listed in Table 2.

That the noise contribution of R_{BE} is close to that of op-amp OP_2 is not a coincidence. Similar to the design of the PTAT amplifier OP_1 , the target for the noise of amplifier OP_2 was that its noise contribution was allowed to be close to that of R_{BE} .

Fig. 7 shows three other noise sources, such as $i_{n-\text{PTAT}}$ of the biasing current I_{PTAT} and the noise i_{nc3} of Q_3 . To calculate the effect on the CTAT current I_{CTAT} of the noise, we just need to divide these two noise currents with the product $(g_{m,Q3}R_{\text{BE}})$. In our design, it holds that $1/(g_{m,Q3}R_{\text{BE}}) \ll 1$, so that the effects of these two noise sources for I_{CTAT} is negligible. As we will show now, also the contribution of noise current i_{nd4} of transistor M_4 to I_{CTAT} is negligible. As shown in Fig. 8, i_{nd4} , is split into two parts: i_{nd41} and i_{nd42} .

So:

$$i_{nd4} = i_{nd41} + i_{nd42}. \quad (40)$$

It will be clear, that with infinite gain of the amplifier OP_2 , the amplifier differential input equals virtually zero so that, thanks to the applied negative feedback, i_{nd41} equals zero. In that ideal case, i_{nd4} would circulate in the loop with M_4 and would not affect the output current i_{nd41} at the drain side of M_4 . However, in case of a limited voltage gain a of amplifier OP_2 , i_{nd41} causes a voltage v_{n-h} across R_{BE} that equals:

$$v_{n-h} = R_{\text{BE}} i_{nd41}. \quad (41)$$

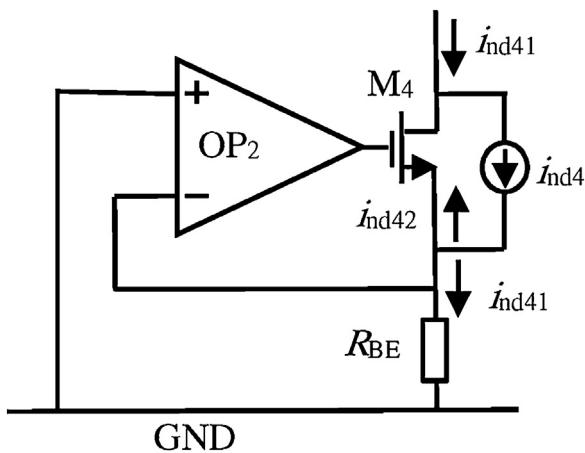


Fig. 8. Part of CTAT current generator to calculate the noise effect of M_4 .

Consequently, the noise contribution at the output of the amplifier or gate of M_4 with respect to the ground level will be:

$$v_{ng4} = -aR_{BE}i_{nd41}, \quad (42)$$

and the gate-source voltage noise of M_4 amounts to:

$$v_{ngs4} = -(1+a)R_{BE}i_{nd41}, \quad (43)$$

which causes that i_{nd42} equals:

$$i_{nd42} = -g_{m,M4}(1+a)R_{BE}i_{nd41}, \quad (44)$$

Where, $g_{m,M4}$ is the transconductance of transistor M_4 . Substitution of Eq. (44) into Eq. (40) yields:

$$i_{nd41} = \frac{i_{nd4}}{1 + g_{m,M4}(1+a)R_{BE}i_{nd41}}. \quad (45)$$

This equation shows that only a very small part of current noise of M_4 will contribute to the CTAT current noise. Therefore, the noise effect of M_4 is negligible too.

In our design, we have: $R_{BE} = 155\text{k}\Omega$, $g_{m,Q3} = 45\mu\text{S}$ and $\sqrt{S_{vin-OP2}} = 55\text{nV}/\sqrt{\text{Hz}}$. With these values, different terms in right-hand side of Eq. (39) amount to 1.1 and 1.25 multiplied by $10^{-25} \text{ A}^2/\text{Hz}$, respectively. This yields a total noise $S_{CTAT} = 2.5 \times 10^{-25} \text{ A}^2/\text{Hz}$, which corresponds to a current noise of $0.5 \text{ pA}/\sqrt{\text{Hz}}$. Comparing this noise with the noise of the PTAT current ($1.1 \text{ pA}/\sqrt{\text{Hz}}$) shows that there is some room for decreasing the power consumption of OP_2 without significant degradation of the total noise performance. However, since OP_2 consumes only about 15% of the supply current, decreasing its supply current will not significantly affect the sensor supply current.

3.4. Sensor resolution based on calculated noise

In this section the sensor temperature readout resolution is calculated based on the simple analytical white-noise calculation presented in Sections 3.2 and 3.3.

Substituting the values of S_{PTAT} and S_{CTAT} into Eq. (38) and Eq. (39) yields:

$$\sqrt{S_1} = 3.3 \text{ pA}/\sqrt{\text{Hz}},$$

$$\sqrt{S_2} = 1.2 \text{ pA}/\sqrt{\text{Hz}}.$$

With the nominal values: $I_1 = 1.72 \mu\text{A}$, $I_2 = 2.11 \mu\text{A}$, $T_H = 99 \mu\text{s}$, $T_L = 124 \mu\text{s}$ ($V_{DD} = 3.3 \text{ V}$), and numerical integration of Eq. (14), the calculated jitters for T_H and T_L amounts to 2.4 ns and 9.1 ns respectively. Substituting these values in Eq. (9), yields a standard deviation of 1.86×10^{-5} for the duty cycle D , corresponding to a standard deviation of 4 mK in the temperature readout.

The above result is valid for a single period. For a complete DEM cycle of eight periods the resolution amounts to $4 \text{ mK}/\sqrt{8} = 1.4 \text{ mK}$, for a measurement time of $8(T_H + T_L) = 1.8 \text{ ms}$.

3.5. Verification by simulation

Up to now, the noise calculations were limited to white noise only. Low-frequency noise and the effect of the chopper and DEM for the noise spectrum have not yet been taken into account.

To evaluate the precision of this approximation and also to determine the amount of low-frequency noise, in this section we present the simulation results for the noise-power spectral density of the currents I_1 and I_2 for the extended circuit shown in Fig. 9. Applying chopping technique to OP_1 and OP_2 not only reduces the error caused by the offsets, but also reduces the effect of $1/f$ noise of the op-amps. Applying DEM reduces systematic errors, and for a part also low-frequency noise. However, due to implementation of the current mirror with very large transistor size, which is needed for required matching, the corner frequency of the $1/f$ noise is very low. Therefore, the effect of DEM for low frequency noise can be neglected. According to Eqs. (10) and (11), the temperature-readout resolution can be calculated from the jitter in T_H and T_L of the output signal, while the jitter of T_H and T_L can be found by substituting the current noise spectral densities of I_1 and I_2 in Eq. (14).

The temperature readout resolution varies slightly with temperature and supply voltage. However, in this paper the analysis has been performed for room temperature and 3.3 V supply voltage, only.

To simulate the current-noise spectral density of I_1 and I_2 , the Schmitt trigger and logic control circuit have been removed, switches Sw_1 and Sw_2 are set to ON or OFF according to the simulation requirements. Fig. 9 shows the switch positions for noise simulation of current I_1 . A similar simulation has been performed for I_2 by setting Sw_1 and Sw_2 to OFF and ON respectively.

In the actual circuit, the applied square-wave modulation signal CH for the choppers of OP_1 and OP_2 is derived from the output signal via a frequency divider. In this way, the frequency of the control signal for the chopper is half that of the output signal. However, in contrast with the output signal, the duty-cycle is 50%. It can be shown that with a duty-cycle of 50% the low-frequency noise is less than what it would have been with a duty cycle equal to that of the output signal. Similar to the actual situation, also in the simulation, such a control signal has been applied.

Because of the use of a switch-capacitor time-variant relaxation oscillator, the conventional frequency-domain noise analysis is not applicable. Instead, we used the so-called "pnoise analysis" of Cadence software. The component characteristics have been taken from the design kit of $0.7 \mu\text{m}$ standard CMOS technology of On-Semiconductor.

As a result of this simulation, Fig. 10 shows the current-noise spectral densities of I_1 and I_2 at room temperature and 3.3 V supply voltage. The peaks at 2.25 kHz represent the up-modulated flicker noise of the amplifier at the chopping frequency. This peak has no significant effect on jitter since it is filtered by a sinc-function, as shown in Eq. (14). From this figure it can be concluded that the simulated white-noise levels at, for instance, $f = 500 \text{ Hz}$, ($\sqrt{S_1} = 3.6 \text{ pA}/\sqrt{\text{Hz}}$ and $\sqrt{S_2} = 1.4 \text{ pA}/\sqrt{\text{Hz}}$) are quite close to that of the simple analytical calculations presented in Section 3.4 ($\sqrt{S_1} = 3.3 \text{ pA}/\sqrt{\text{Hz}}$ and $\sqrt{S_2} = 1.2 \text{ pA}/\sqrt{\text{Hz}}$).

With the same nominal values as presented in Section 3.4 ($I_1 = 1.72 \mu\text{A}$, $I_2 = 2.11 \mu\text{A}$, $T_H = 99 \mu\text{s}$, $T_L = 124 \mu\text{s}$) ($V_{DD} = 3.3 \text{ V}$), and numerical integration of the simulated spectra of S_1 and S_2 in Eq. (14), for T_H and T_L jitters of 2.7 ns and 10 ns , are found, respectively. Substituting of these values in Eq. (9) yields a standard deviation of 2.1×10^{-5} for the duty cycle D , corresponding to a standard deviation of 4.5 mK in the temperature readout. As Section 3.4, this

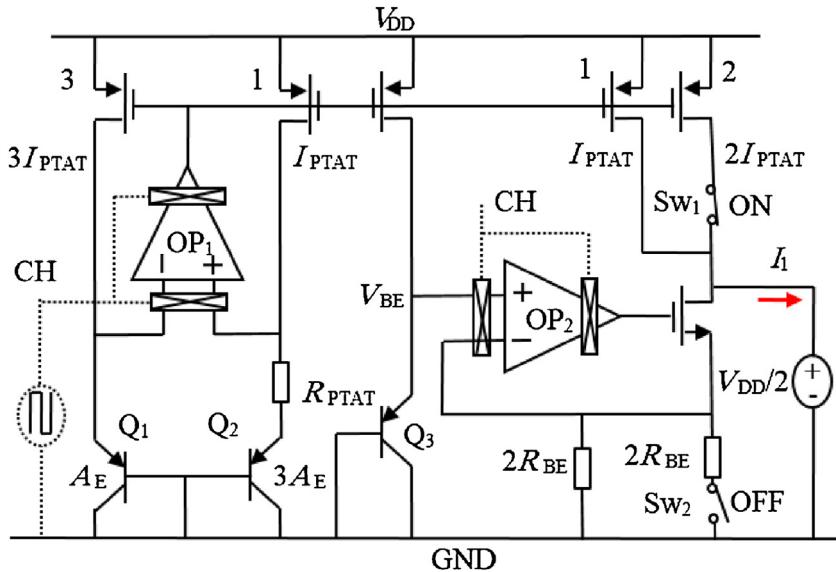


Fig. 9. Simplified sensor schematic to simulate the noise power spectral density of I_1 and I_2 .

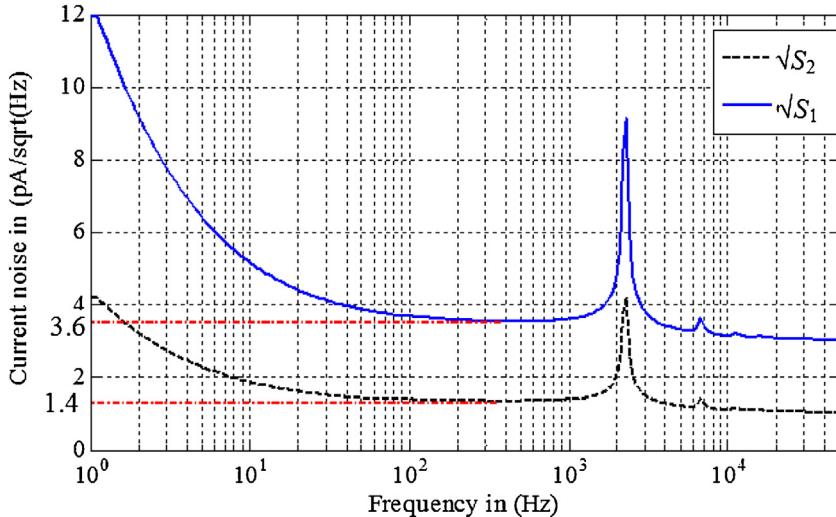


Fig. 10. The current noise power spectral density $\sqrt{S_1}$ and $\sqrt{S_2}$ for current I_1 and I_2 at room temperature (27°C) and 3.3 V supply voltage.

result is valid for a single period. For a complete DEM cycle of eight periods the resolution amounts to $4.5 \text{ mK}/\sqrt{8} = 1.6 \text{ mK}$.

As can be realized the result of our approximate calculation for temperature readout resolution (1.4 mK) is quite close to the result of more accurate simulations (1.6 mK), which includes the effects of the chopper, low-frequency noise and also some correlation effects too.

4. Implementation and measurement result

The sensor has been fabricated in $0.7 \mu\text{m}$ CMOS technology of On Semiconductor [7]. Fig. 11 shows a photograph of the chip. The sensor is designed for a supply-voltage range from 2.7 V to 5.5 V. At 3.3 V, the current consumption amounts to $60 \mu\text{A}$. The sensor outputs a rail-to-rail square-wave signal, whose frequency varies from about 1 kHz to 4 kHz over the full temperature range (-45°C to 130°C) and the supply-voltage range mentioned above. Note that not the frequency but only the duty cycle contains the temperature information.

In our test set-up, the output signal has been measured by an ARM microcontroller (STM32F103), where the time intervals T_H and T_L are digitized with one of its timers operated with an internal clock signal of 72 MHz.

Because of the applied DEM technique, for an accurate result, 8 sequential periods must be averaged [7], according to the equation:

$$D_{avg} = \frac{1}{8} \sum_{i=1}^8 \frac{T_{Hi}}{T_{Hi} + T_{Li}}. \quad (46)$$

Measurement of the low-frequency part of the noise spectrum of the sensor, requires special measures to distinguish fluctuations due to sensor noise from those caused by changes in the sensor temperature. As a first measure, the sensors were assembled in a thermal buffer, which was implemented with a big aluminum block and thermal isolation with respect to the environment, which stabilized the temperature of the devices under test. Nearby the sensors and in good thermal contact with them a reference temperature sensor [7] (Pt100) has been assembled as well. With respect to the

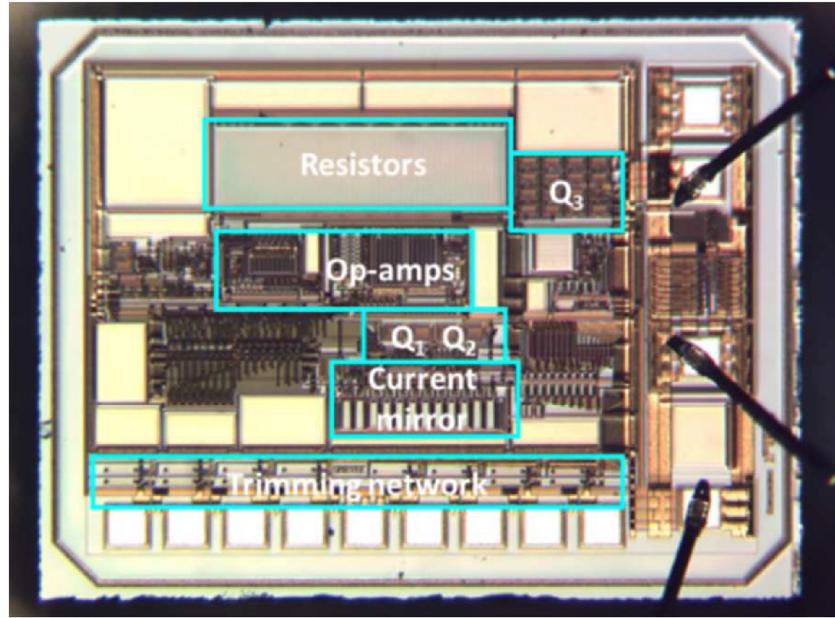


Fig. 11. The chip photograph.

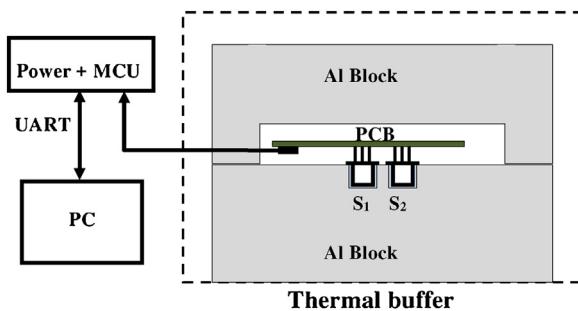
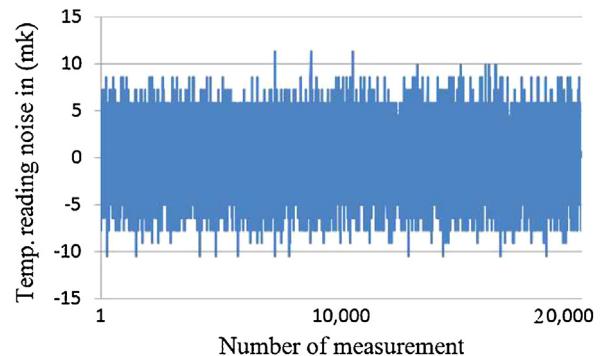


Fig. 12. The set up for the test of noise versus measurement time.

Fig. 13. The temperature reading result of $((\vartheta_1 - \vartheta_2) - (\vartheta_1 - \vartheta_2)_{DC})/\sqrt{2}$.

effects of white noise, it should be expected that, the resolution will improve proportionally to the square root of the measurement time t_m . On the other hand, for residual effects of $1/f$ noise this will not be valid. However, due to the effect of the applied choppers, these effects should be negligible. For experimental confirmation of this noise behavior, we tested the sensor resolution up to very large measurement times. However, for large measurement times, the noise levels are very low, so that in spite of using thermal buffers, the residual effects of temperature fluctuations of the sensors are larger than the noise levels to be measured. This problem has been solved as shown in Fig. 12 [7]. Instead of measuring each single sensor, at the same moment, we measured the temperature of two sensors that have been positioned close to each other, in the same thermal buffer. With proper thermal design, we can assure that the temperature differences $(\vartheta_1 - \vartheta_2)$ of these two sensors are less than the sensor resolution. Then, by subtracting the readouts of two sensors we can remove the effects of low-frequency temperature drift of the thermal buffer. However, due to differences in the calibration errors, the temperature differences $(\vartheta_1 - \vartheta_2)$ has also a constant DC value. This DC value $(\vartheta_1 - \vartheta_2)_{DC}$ can be found, as the average value over a (very) long measurement time. In our case we used 20,000 readings to find this value and simply removed it by subtracting it during post processing. As an example, Fig. 13 shows the result after performing the calculation of $((\vartheta_1 - \vartheta_2) - (\vartheta_1 - \vartheta_2)_{DC})/\sqrt{2}$, where each measurement corresponds to a full DEM cycle of about 1.8 ms.

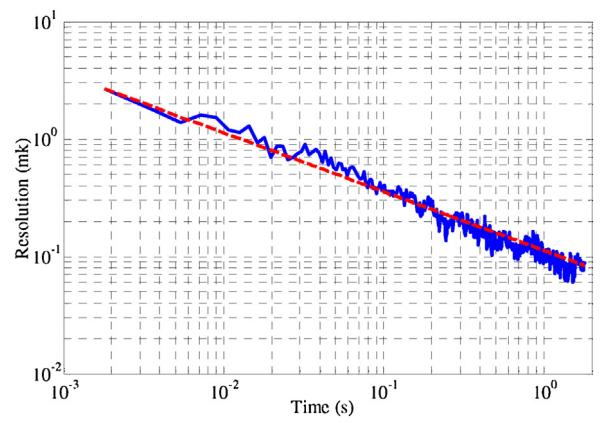


Fig. 14. The resolution versus measurement time.

This result is equivalent to the noise of a single sensor output. The standard deviation amounts to 3 mK. Fig. 14 shows the result of resolution versus measurement time. For a measurement time of 2 s, a resolution of 0.1 mK can be achieved. The dotted red line presents the reduction of the resolution with the square root of the measurement time.

The measurement results shown in Fig. 13 also include quantization noise induced by sampling the signal with the microcontroller timers. To compare the measurement results with the calculated ones we should exclude this quantization noise. For the standard deviation of the duty cycle σ_{D-q} caused by quantization noise it can be shown that [17]:

$$\sigma_{D-q} = \frac{t_s}{\sqrt{6t_m t_p}}, \quad (47)$$

Where, $t_s = 1/f_{clock}$ is sampling period, $t_m = N(T_H + T_L)$ is the measurement time and $t_p = T_H + T_L$ is the period time. In our measurements, with $f_{clock} = 72$ MHz, $T_H = 99\mu s$, $T_L = 124\mu s$ and $N = 8$, the quantization noise amounts to 8.9×10^{-6} , which is equivalent to a standard deviation of 1.9 mK in the temperature readout. Removing this quantization noise from the total measured noise (3 mK) results in the measured sensor noise of $((3\text{ mK})^2 - (1.9\text{ mK})^2)^{0.5} = 2.3\text{ mK}$, which is quite close to the calculation result of 1.6 mK presented in Section 3.5. Some parts of this difference can be explained by clock jitter, and interference.

The noise performance of the sensor in relation to its energy consumption can be characterized by its Resolution Figure of Merit: RFoM [6]. With a resolution of 3 mK (rms) for a conversion time of 1.8 ms , taking into account the sensor power of $198\mu W$, the RFoM amounts to 3.2 pJ/K^2 , which is the best reported RFoM for BJT-based temperature sensor up to now [18].

5. Conclusions

The design aspects regarding the noise characteristics of a BJT-based temperature sensor with a duty-cycle-modulated output signal have been presented. Noise analysis was performed with a combination of analytical and numerical methods. In the design phase of the sensor, analytical methods were used to identify the main noise sources and to optimize the design. The sensor circuit contains time-variant parts, such as those needed to implement dynamic element matching and chopping, and to generate a duty-cycle modulated output signal. These time-variant parts pose some complications on performing a straightforward direct noise analysis. It has been shown how for such circuits, the analysis can be performed by on one hand simplifying the circuit and on the other hand using powerful computer tools to check the critical circuits, part-by-part. Thus, the analysis was performed for simplified subcircuits of the sensor, while numerical methods were performed for the more complex circuit, to check the validity of the simplifications. The sensor has been implemented in $0.7\mu m$ CMOS technology. For the measurement time of 1.8 ms , corresponding to one DEM cycle, the measured value of the sensor noise (2.3 mK) is quite close to the 1.6 mK calculated with the simple method presented in this paper. Measurement of the noise spectrum up to very low frequencies requires care and special measures that have been evaluated in this paper. The sensor has achieved a state-of-art resolution figure of merit, RFoM of 3.2 pJ/K^2 for BJT-based temperature sensor. By increasing the measurement time up to 2 s , a resolution of 0.1 mK can be achieved.

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he is a Consultant in the field of sensor systems. In addition to many journal and conference papers, he is also an author and editor of books in the field of sensor systems, published by IOP, Kluwer, Springer, and Wiley. Prof. Meijer is a Member of the IEEE Industrial Electronics Society and a Senior Member of the IEEE Solid-State Circuits Society. In 1999, the Dutch Technology Foundation STW awarded him with the honorary degree "Simon Stevin Meester," and in 2001, he was awarded the Antoni van Leeuwenhoek Chair at TU Delft.